Optimized Design of Logic Gates Using Memristor and their Application to Design of Analog Digital Differential Amplifier

DISSERTATION

SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIRMENTS FOR THE AWARD OF THE DEGREE OF

MASTER OF TECHNOLOGY
IN
CONTROL & INSTRUMENTATION
(2015-2017)

SUMITTED BY:
MUKESH KUMAR
2K15/C&I/11

UNDER THE SUPERVISION OF
Dr. Madan Mohan Tripathi
(Associate professor)

DEPARTMENT OF ELECTRICAL ENGINEERING

DELHI TECHNOLOGICAL UNIVERSITY

(FORMERLY DELHI COLLEGE OF ENGINEERING)

BAWANA ROAD, DELHI-110042

JULY, 2017

DEPARTMENT OF ELECTRICAL ENGINEERING

DELHI TECHNOLOGICAL UNIVERSITY

(Formerly Delhi College of Engineering)

Bawana Road, Delhi-110042

Candidate's Declaration

I, **Mukesh kumar**, Roll No. **2K15/C&I/11**, student of **M. Tech (Control & Instrumentation)**, herewith declare that the dissertation entitled **"optimized design of logic gates using memristor and their application to design analog digital differential amplifier"**, under the supervision of Associate Prof. Dr. Madan Mohan Tripathi of Electrical Engineering Department, Delhi Technological University, in partial fulfilment of the need for the award of the degree of Master of Technology, has not been submitted elsewhere for the award of any degree.

I herewith solemnly and sincerely affirm that all the particulars declared above by me are true and correct to the best of my knowledge and belief.

Place: Delhi **Mukesh kumar**

Date: 28 .07.2017 **2K15/C&I/11**

Department of Electrical Engineering

Delhi Technological University

(Formerly Delhi College of Engineering)

Bawana Road, Delhi-110042

Certificate

This is to certify that the dissertation entitled **"optimized design of logic gates using memristor and their application to design analog digital differential amplifier"**, submitted by **Mukesh kumar** in completion of major project dissertation for the master of Technology degree in **Control & Instrumentation** at Delhi Technological University is an authentic work carried out by him underneath my superintendence and guidance.

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

Place: Delhi

Date: 28.7.2017

Dr. Madan Mohan Tripathi

(Associate professor)

Electrical Engineering Department

Delhi Technological University, Delhi

ACKNOWLEDGEMENT

It gives me a great pleasure to express my profound gratitude to my supervisor and project guide **Dr. Madan Mohan Tripathi,** Department of Electrical Engineering, Delhi Technological University (formerly Delhi College of Engineering), for his invaluable guidance, encouragement and patient reviews throughout the progress of this dissertation. It has been a great experience to get a chance under his rich experience.

I would conjointly wish to extend my heartfelt thanks to Prof. Madhusudan Singh, head of the department and all faculty of department of Electrical Engineering, Delhi Technological University, for keeping the spirits high and clearing the visions to work on the project.

I am conjointly grateful to my family and friends for their constant support and motivation throughout this work.

Finally, I am thankful to the almighty because without his blessing, this work was not possible.

Mukesh Kumar

2K15/C&I/11

ABSTRACT

The CMOS based devices have reached the Moore's limit and cannot be scaled down further; also there is not much improvement in the power consumption and the speed of these devices in past years. Research is going on to find a suitable alternative to CMOS based devices. Memristor is one such alternative to CMOS. This thesis gives a brief introduction of memristor and its modeling. Memristor digital logic gates have been designed and their application to design of analog digital differential amplifier presented based on memristor ratioed logic (MRL) in Cadence Virtuoso. Simulation results show that memristor based gates have a fast response time and less power consumption, which make them ideal for digital architecture design and a suitable alternative for CMOS designs. The focus of this research is on developing memristor-based applications at the circuit and architecture levels. Memristors are investigated from the point of view of circuit designer and computer architect, including describing the desired device for different applications

CONTENTS

LIST OF FIGURES

Figures **Caption** **page no.**

LIST OF TABLES

LIST OF SYMBOLS, ABBREVIATIONS

S. No	Symbols	Descriptions
1.	M(q)	Memresistance
2.	W(ϕ)	Memconductance
3.	R_{OFF}	Off state resistance
4.	R_{ON}	On state resistance
5.	μ_D	average drift velocity
6.	β	scale of magnetic flux
7.	D	thickness of titanium-dioxide film
8.	*q(t)*	total charge flowing in memristor device
9.	*W*	the doped active length of the memristor
10.	v_{ths}	Threshold voltage
11.	MRL	Memristor ratioed logic
12.	TEAM	Threshold Adaptive Memristor

Chapter 1

INTRODUCTION

.

There are three standard basic components in circuit theory like resistor, capacitor and inductor –are well understood. These components are outlined in terms of the relation between two of the four basic circuit variables, namely, current, voltage, charge and flux . The relation between current and voltage (dv = Rdi) offers resistance , current and flux (dϕ = Ldi) offers inductance and voltage and charge (dq = Cdv) offers capacitance.

As we tend to see within the fig1 Out of the six potential mixtures of the four basic circuit variables, 5 are defined . In 1971, Prof. Leon Chua sees that there's hole wherever a plain relation looks to be missing projected that there ought to be a fourth basic circuit component to line up the relation between charge(q) and magnetic flux(ϕ) . so as to possess symmetry the mathematically explicit relation between charge (q) and flux (φ) offers memristor as dφ=Mdq wherever M is memristance.

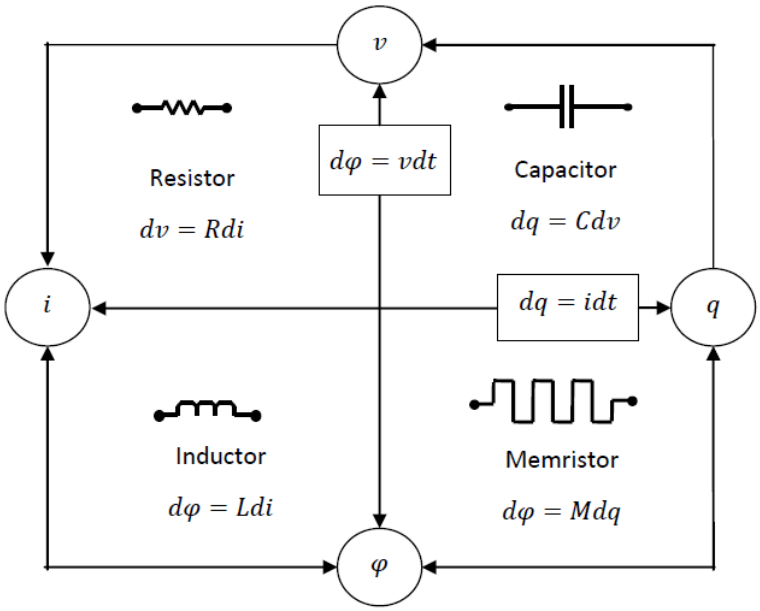


Figure 1.1: Four Basic Circuit Elements

L. O. Chua generalizes the circuit theory to non-linear system and gives a formal mathematical proofs that Relation between φ and q an effect, not the cause, of memristance M is a "memory resistor" – it is a nonvolatile resistive memory! Proved that no equivalent circuit to M could be made using any R, C and L – is a new and unique „basis function" and also Built equivalent circuit using transistors .
In 2008 Stanley Williams, et al., Hewlett Packard connected the speculation of the memristive devices to TiO2 resistive switches proclaimed initial unreal memristor

In this thesis a linear circuit memristor model is implemented in OrCAD PSpice as well as a practical memristor model is modeled using Cadence Virtuoso. Using memristor ratioed logic **(**MRL) which is a hybrid Memristor-CMOS family, implementation of AND, NOR, XOR, NOT gate has been done. Also comparison between the power consumption of CMOS based NOT gate and hybrid memristor based NOT gate has been presented [7]. It is a hybrid of memristor and CMOS logic, also called Mi-MOS. In MRL, OR and AND logic gates are purely memristive in nature and CMOS inverter is integrated to provide a perfect logic structure and signal integrity [8]. The MRL family is compatible with CMOS logic since the logical state is shown in MRL is by voltage as in CMOS. A memristor based digital differential amplifier also be implemented .

1.1 HISTORICAL BACKGROUND

Before Leon Chua_s publication on the memristor in 1971 the idea of electrical device with memory existed. In 1960 , a brand new circuit component named the ― "memistor" developed by professor. Bernard Widrow of Stanford University.

The memistor was a three-terminal device that the conductance between two of the terminals was controlled by the time-integral of the current into the third terminal. Thus, the resistance of the memistor was controlled by charge. Memistors shaped the fundamental parts of the neural-network design referred to as ADALINE (ADAptive LInear NEuron). Later, it absolutely was verified that the memistor and memristor are totally different devices.

In 1968, F. Argall revealed a paper ―Switching phenomena in oxide skinny films, that shows results almost like that of the memristor model projected by Stanley Williams and his team afterward.

In 1971, Leon Chua mathematically foreseen [3] that there's a fourth elementary circuit component characterised by a relationship between charge and flux linkage.

In 1976, Leon Chua and Sung Mo Kang revealed a paper entitled ―Memristive devices and systems, generalizing the idea of memristors and memristive systems, together with a property of zero crossing within the Lissajous curve characterizing current versus voltage behaviour.

In 1990, S.Thakoor, et al., incontestable a tungsten-oxide variable-resistance device that's electrically reprogrammable.

Four years later, in 1994, Buot and Rajgopal printed a piece entitled ―Binary data storage at zero bias in quantum-well diodes‖. The article delineate current–voltage characteristics the same as that of the memristor in AlAs/GaAs/AlAs quantum-well diodes. The analysis showed no direct association to Chua's memristor

.

In 2000, Beck, et al., of IBM_s metropolis science laboratory, delineated reproducible resistance shift effects in skinny chemical compound films. The hysteretic options of those switches square measure almost like those of the memristor.

In 2001, Liu, et al., researchers within the area Vacuum growing Center of the University of Houston, conferred results throughout a non-volatile memory conference command in San Diego, California, showing the importance of chemical compound bilayers to attain high-to-low resistance magnitude relation.

Apart from the devices mentioned on top of, it's attention-grabbing to notice that between 1994 and 2008, there have been several alternative devices developed with behaviour almost like that of the memristor, however solely the HP scientists were productive find a link between their work and also the memristor postulated by Chua.

In 2008, 37 years once Leon Chua"s proposal, the memristor in device type was developed by Stanley Williams and his cluster within the info and Quantum Systems (IQS) research laboratory at HP. Dmitri Strukov, Gregory Snider, Duncan Stewart, and Stanley Williams, of HP Labs, revealed a commentary [5] distinguishing a link between the two-terminal resistance change behaviour found in nanoscale systems and Leon Chua‘s memristor. The model planned by them is represented thoroughly in Chapter four of this report. However, Victor Erokhin and M. P. Fontana claimed to possess developed a polymeric memristor before the titanium-dioxide memristor developed by Stanley Williams‘ cluster.

Since the announcement of the breakthrough by Stanley Williams‘ cluster, various papers with the aim to research the elementary attributes of the memristor and its applications in numerous areas of circuit style are revealed as shown in Figure 2.

Later in 2008, J. Joshua yang, Matthew D. Pickett, Xuema Li, Douglas A. A. Ohlberg, Duncan R. Stewart and R. Stanley Williams published a commentary demonstrating the memristive change behaviour and mechanism in nanodevices.

In Oct 2008, Yu V. Pershin, S. La Fontaine, and M. Di Ventra revealed a commentary distinguishing memristive behaviour in amoeba's learning.

In Jan 2009, Sung Hyun Jo, Kuk-Hwan Kim, and Wei lu of the University of Michigan revealed a commentary describing an amorphous-silicon–based memristive material capable of being integrated with CMOS devices.

In June 2009, scientists at NIST reported that that they had invented non-volatile memory employing a versatile memristor that's each cheap and low-power.

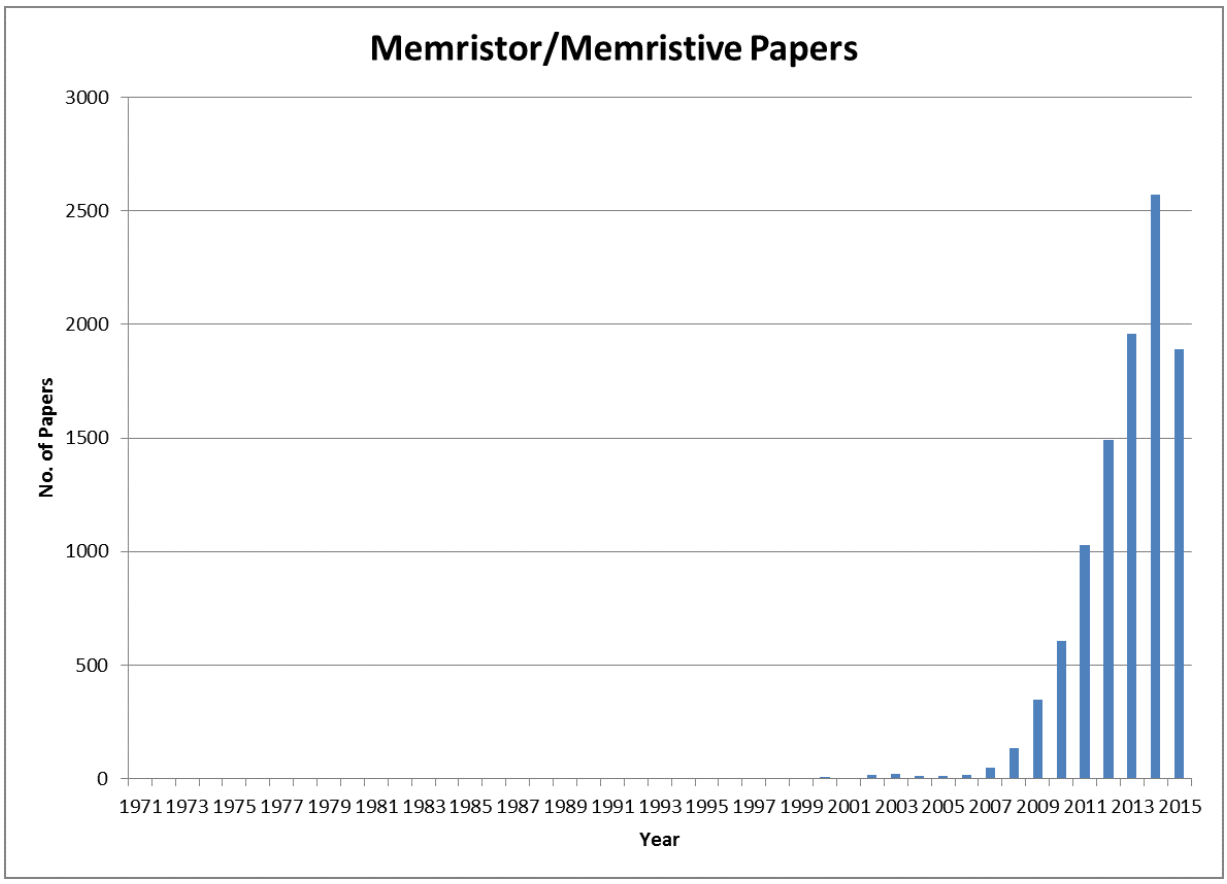


Figure:1.2 published paper related to the memristor research every year

1.2 MEMRISTOR THEORY

1.2.1 Memristor origin

There are four basic circuit variables in circuit theory. they're current i, voltage v, charge Q and flux ϕ. There are six potential combos of the four elementary circuit variables. we've a decent understanding of five of the doable six combos. The three basic two-terminal devices of circuit theory - particularly, the resistance, the capacitor and also the inductance - are outlined in terms of the relation between 2 of the four basic circuit variables. A resistance is outlined by the link between voltage and current (dv = Rdi), the capacitor is outlined by the connection between charge and voltage (dq = Cdv) and also the inductance is outlined by the link between flux and current (dϕ = Ldi). additionally, the current i is outlined because the time spinoff of the charge Q and in line with Faraday_s law, the voltage v is outlined because the time derivative of the flux ϕ. These relations are shown in Figure 3

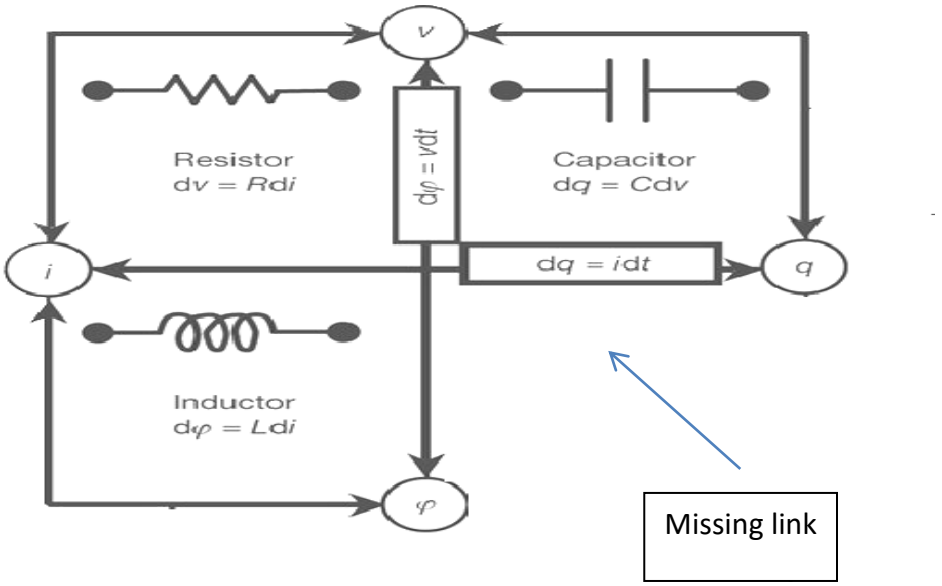


Figure 1.3: The circuit components outlined as a relation between four circuit variables

Leon Chua compared this fashion of process circuit components to Aristotle‘s theory of matter. per this theory, all matter consisted of the subsequent four elements:

Earth
Water
Air
Fire

Each of those components exhibited 2 of the four basic properties - wetness, dryness, coldness and hotness.

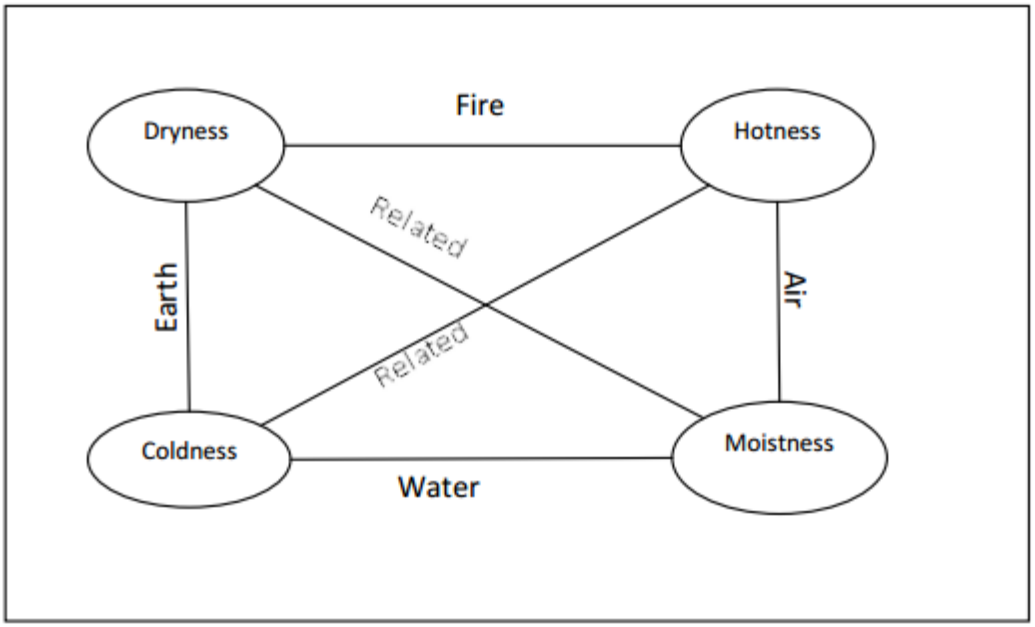


Figure 1.4: Aristotle's outlined relationship

Leon Chua saw a putting likeness between the relation among components and also the relation among numerous circuit variables. He reasoned that there ought to be a fourth elementary circuit component to finish the symmetry. He referred to as this component,that sets up a relation between flux and charge, the memristor.

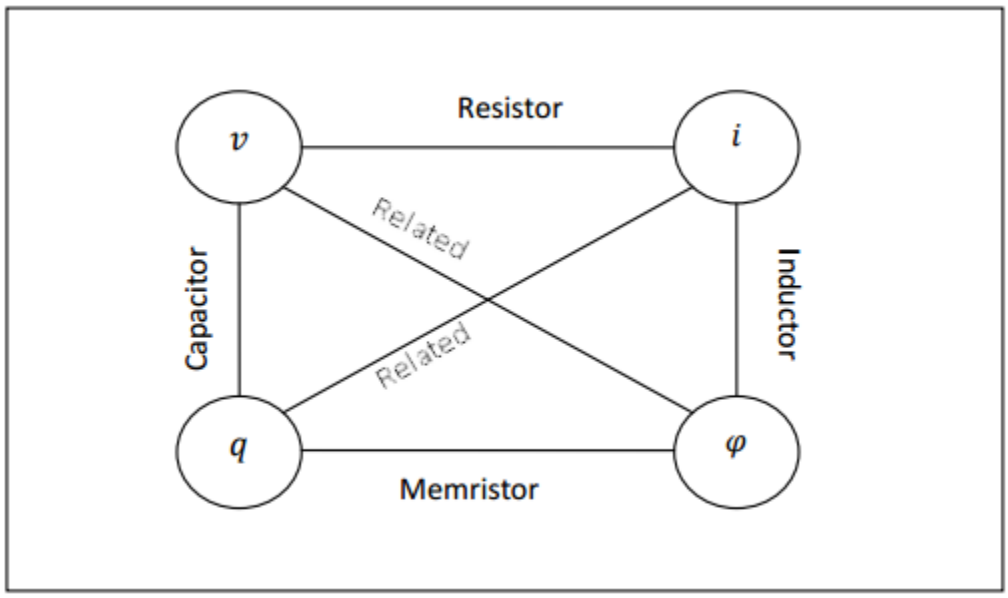


Figure1.5: The missing circuit element (Memristor) relationship

1.2.2 Definition of memristor

Memristor, the contraction of — "memory resistor", may be a passive device that gives a practical relation between charge and flux. —It is outlined as a two-terminal circuit component during which the flux ϕ between the 2 terminals may be a perform of the amount of electrical charge q that has gone through the device. Memristor isn't an energy-storage component. Figure vi shows the image for a memristor

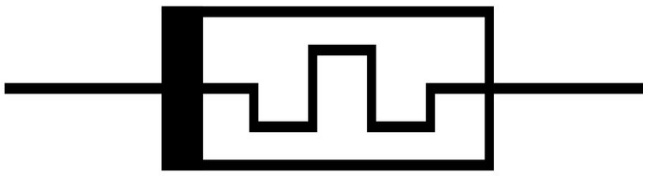


Figure1.6: Memristor symbol

An alternative definition might be, — "A memristor may be a two-terminal part whose resistance depends on the magnitude, direction and period of the applied voltage".

A memristor same|is claimed|is alleged} to be charge-controlled if the relation between flux and charge is expressed as a operate of electrical charge Q and it's said to be flux-controlled if the relation between flux and charge is expressed as a operate of the flux linkage ϕ [3].

For a charge-controlled memristor,

$$\varphi = f(q) \qquad (1)$$

Differentiating equation (1)

$$\frac{d\varphi}{dt} = \frac{df(q)}{dq}\frac{dq}{dt} \qquad (2)$$

Now giving the voltage $v(t) = \frac{d\varphi}{dt}$ as

$$v(t) = M(q)i(t) \qquad (3)$$

Where

$$M(q) = \frac{df(q)}{dq} \qquad (4)$$

M(q) is termed as memristance, and it's the units of resistance. Memristance defines a linear relationship between current and voltage, as long because the charge doesn't vary. Thus, if M is constant, a memristor behaves as a electrical device.

For a flux-controlled memristor ,

$$q = f(\varphi) \qquad (5)$$

Differentiating equation (5) yields

$$\frac{d(q)}{d(t)} = \frac{df(\varphi)}{d(\varphi)}\frac{d\varphi}{dt} \qquad (6)$$

giving the voltage $v(t) = \frac{d(q)}{d(t)}$ as

$$i(t) = w(q)v(t) \qquad (7)$$

Where

$$w(\varphi) = \frac{df(\varphi)}{d\varphi} \qquad (8)$$

$w(\varphi)$ is called as memconductance and it has the unit of conductance

1.2.3 Memristance and Memristor Analogy

Memristance may be a property of the memristor [4]. once the charge flows in one direction through a circuit, the resistance of the memristor will increase, and its resistance decreases once the charge flows within the other way within the circuit. If the applied voltage is turned off, so stopping the flow of charge, the memristor — "remembers" the last resistance that it had. once the flow of charge is started once more, the resistance of the circuit are going to be what it absolutely was once it had been last active.

An analogy of a memristor is delineated in [4]. A resistor is analogous to a pipe through that water flows. The pressure of water at the input of the pipe is analogous to the voltage, and water is analogous to charge. the speed of flow of water through the pipe is comparable to current. If the pipe features a larger diameter, the flow of water through the pipe is quicker, rather like a lot of current flows through resistor with alittle worth of resistance. associate analogy for a memristor may be a totally different reasonably pipe, whose diameter expands or shrinks counting on the direction of the water flow through it. The diameter of the pipe will increase once the water flows in one direction, sanctioning water to flow quicker, and therefore the diameter of the pipe decreases once the water flows within the other way, so fastness down the water flow. If no water is let into the pipe, the pipe can retain its most up-to-date diameter till the water is turned back on. Thus, the pipe remembers the number of the water that has flowed through it.

1.3 MEMRISTOR PROPERTY

1.3.1 ϕ-q curve of memristor

The ϕ-q curve of a memristor could be a monotonically increasing. The memristance is that the slope of the ϕ-q curve. per the memristor passivity condition, a memristor is passive if and on condition that memristance M(q) is non-negative [3]. If M(q) ≥ 0, then the instant power dissipated by the memristor, p(i)=M(q)(i(t))^2, is usually positive, and then the memristor could be a passive device. The memristor is only dissipative, sort of a electrical device. Thus, the ϕ-q curve of a memristor is usually a monotonically increasing operate. Figure 7 shows some samples of typical ϕ-q curves of memristors.

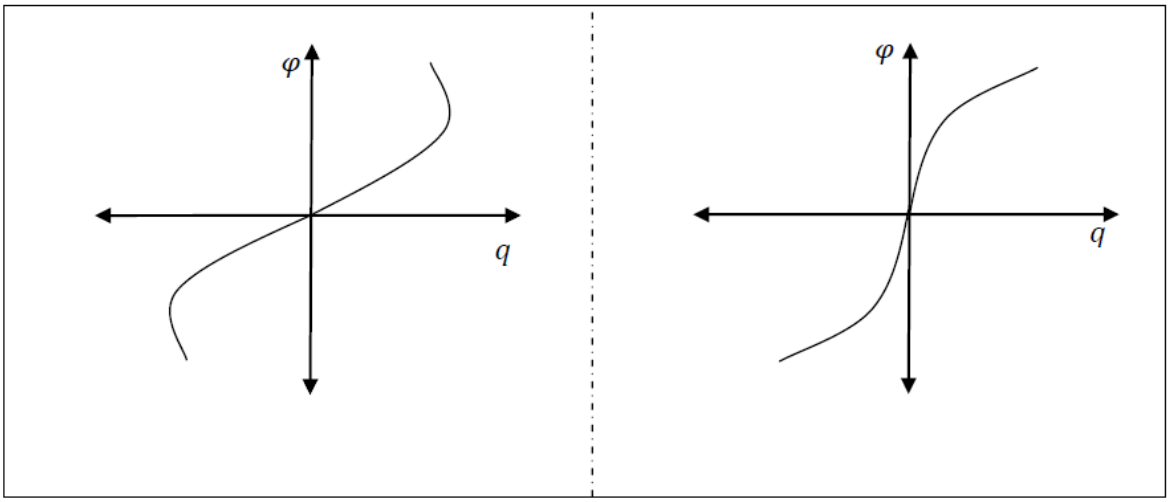


Figure 1.7: Typical ϕ-q Curves of Memristors

1.3.2 current –voltage curve of memristor

An important fingerprint of a memristor is that the — "pinched physical phenomenon loop" current-voltage characteristic. For a memristor excited by a periodic signal, once the voltage v(t) is zero, the present i(t) is additionally zero and contrariwise. Thus, each voltage and current have identical zero-crossing. If any device encompasses a current–voltage physical phenomenon curve, then it's either a memristor or a memristive device. Another signature of the memristor is that the — "pinched hysteresis loop" shrinks with the rise within the excitation frequency.

Figure 8 shows the — “pinched hysteresis loop” associated an example of the loop shrinking with the rise in frequency. In fact, once the excitation frequency will increase towards time, the memristor behaves as a traditional resistance.

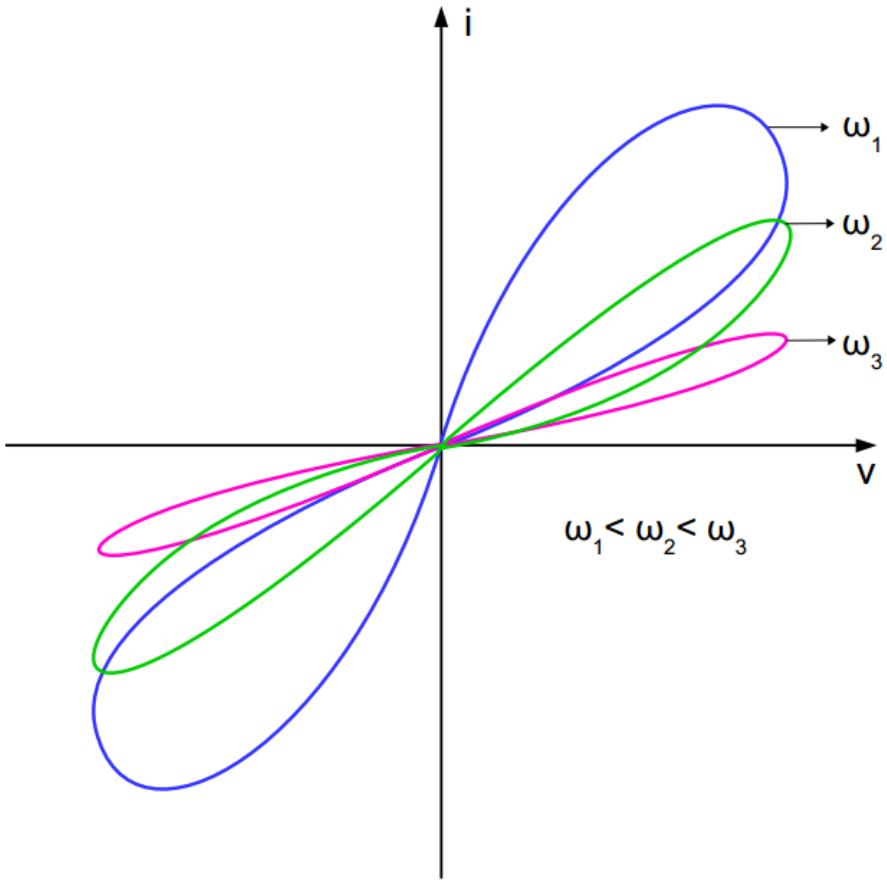


Figure 1.8: The pinched-hysteresis loop and also the loop shrinking with the rise in frequency

1.4 Memristive system

Memristor is a passive device with two terminals and shows variable resistance. Any modification within the memristance is said with the previous resistance/ state of the memristor device. In 1971 , Leon Chua outlined the memristor as “Memristor- the missing circuit part ” within which he offers a mathematical proofs and subsequently he expanded the conception to –“Memristive system” in 1976[11] . The memristive systems are delineated by

$$v = M(w, i)i \qquad (9)$$

and

$$\frac{dw}{dt} = f(w, i) \qquad (10)$$

where w is a variable representing state, f and M may be functions of time, v and i are the voltage across memristor and current flowing in memristor severally.

1.4 Structure of the Thesis

Chapter 2 gives a brief description of the Memristor models. Chapter 3 presents the implementation of memristor. The logic gate based on memristor is described in Chapter 4. Application based on memristor logic gates are discussed in Chapters 5. Finally, Chapter 6 provides an apt conclusion.

Chapter 2

MEMRISTOR MODELS

After chua projected the memristor, In 2008 Stanley Williams together with his analysis cluster at HP Labs fancied the memristor within the style of device [6] then later alternative completely different model were planned like .

1. Linear ion Drift
2. Simmons Tunnel Barrier
3. TEAM – Threshold adaptive Memristor
4. nonlinear ion Drift
5. VTEAM – Voltage ThrEshold adaptive Memristor

2.1 HP Lab Memristor Model

The HP model of the memristor is delineate in [6]. to understand a memristor, they used a really skinny film of titanium dioxide (TiO2). the skinny film is sandwiched between two Pt (Platinum) contacts and one aspect of TiO2 is doped with oxygen vacancies. The O_2 vacancies are charged ions. Thus, there's a TiO2 junction wherever one aspect is doped and therefore the different aspect is undoped. The device established by HP is shown in Figure 2.1.

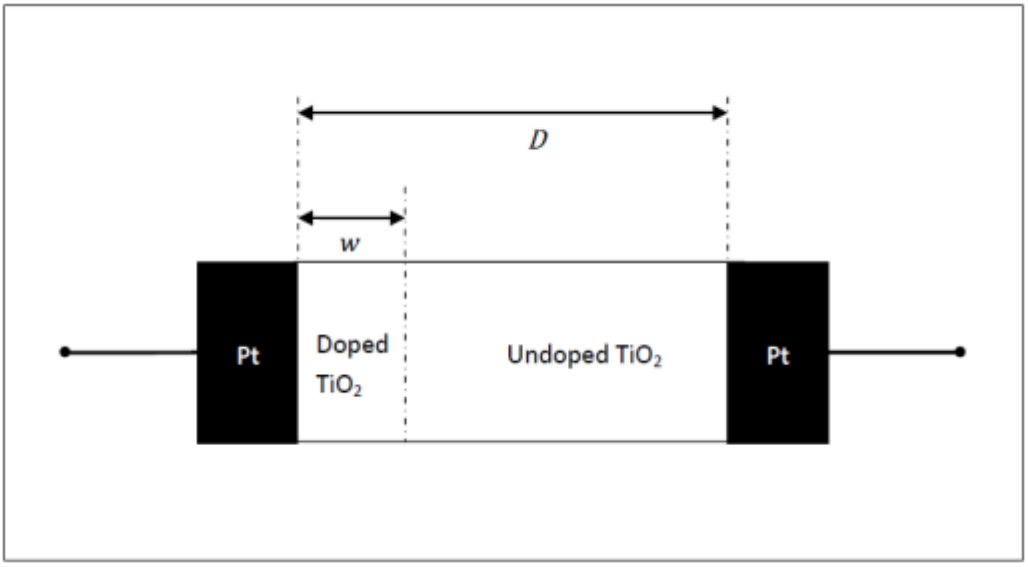


Figure 2.1: Schematic of HP Memristor

In Figure 9, D represent the length of device and w represent the length of the doped region. Pure TiO2 is a semiconductor and has high electrical resistance. The doped element vacancies create the TiO2-x material conductive . The operating of the memristor established by HP is delineated in [2]. once a positive voltage is applied, the charged element vacancies within the TiO2-x layer are repelled, moving them towards the undoped TiO2 layer. As a result, the boundary between the two materials moves, inflicting a rise within the proportion of the conducting TiO2-x layer. This will increase the conductivity of the entire device. once a negative voltage is applied, the charged element vacancies are attracted, pull them out of TiO2 layer. This will increase the number of insulating TiO2, so increasing the electrical resistance of the entire device. once the voltage is turned off, the element vacancies don't move. The boundary between the two oxide layers is frozen. this can be however the memristor "remembers" the voltage last applied. Figure 10 explains the behaviour of the memristor model once positive and negative voltage is applied. Figure 2.2(a) shows the skinny film of titanium-dioxide wherever one aspect is doped with positive element vacancies and also the alternative aspect is that the undoped. Figure 2.2(b) shows the behaviour once a positive voltage is applied. The positive element vacancies are repelled and that they move towards the undoped TiO2 layer, reducing the share of the insulating TiO2, so decreasing the electric resistance. Figure 2.2(c) shows the behaviour once a negative voltage is applied. The positive element vacancies are attracted and that they move towards the doped TiO2-x layer, increasing the share of the insulating TiO2, so increasing the ohmic resistance.

Figure 2.2: Behaviour of HP memristor once positive and negative voltages are applied

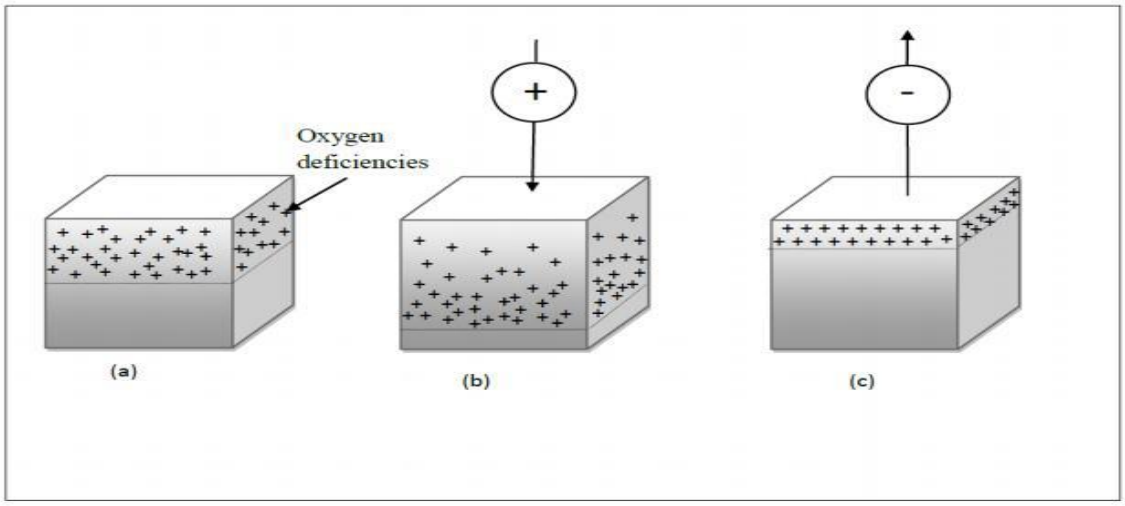


Figure 2.2: Behaviour of HP memristor w.r.t +ve and -ve voltages

The memresistance basic mathematical expression of the HP memristor is represented in eq. (11) [5]

$$M(q) = R_{OFF}\,(1 - \frac{R_{ON}}{\beta} q(t)) \qquad (11)$$

Where $\beta = \frac{D^2}{\mu_D}$ has the scale of magnetic flux;
μ_D = average drift velocity ;
D = thickness of titanium-dioxide film;
R_{OFF} and R_{ON} = "off-state" and "on-state" resistance;
q(t) = total charge flowing in memristor device.

2.1.1 Linear Ion Drift Model

The schematic of this model is shown in fig. 2.3 below that is completely different than the HP model. in this model the dimension of the doped region W(t) is given by eq. 12 in presence of uniform field of force across the memristor device.

Therefore,

$$w(t) = carrier\ velocity * \ carrier\ drift\ time$$

This implies,

$$w(t) = \mu_D\, E(t) * \frac{q(t)}{i(t)}$$

$$= \mu_D \frac{v(t)}{D} \frac{q(t)}{i(t)}$$

$$w(t) = \mu_D \frac{R_{ON}}{D} q(t) \qquad (12)$$

Variable *w(t)* is bound in between 0 and *D*.

Representing the doped and undoped regions in terms of resistances, we get

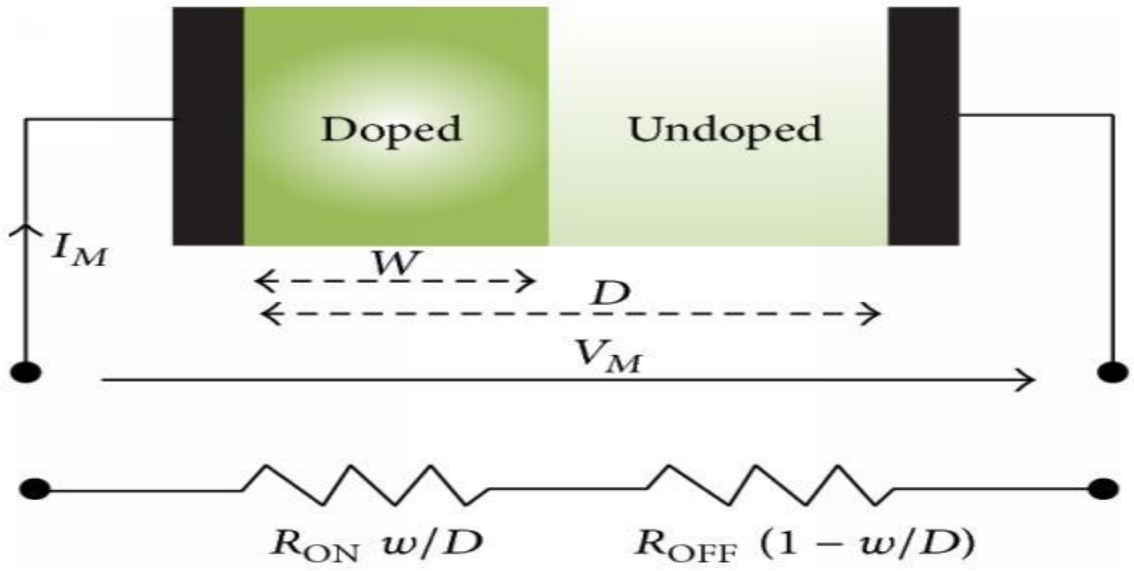


Figure 2.3: doped and undoped regions of memristor

From figure,

R_{ON} = resistance of doped layer of length D

R_{OFF} = resistance of undoped layer of length D

W = the doped active length of the memristor

D = the total active length of the memristor

On applying Kirchoff's law,
We get,

$$v(t) = (R_{ON}\ \frac{w(t)}{D} + R_{OFF}\ (1 - \frac{w(t)}{D})) \qquad (13)$$

Assuming thatR_{ON} is very small compared toR_{OFF}
Therefore,

$$M(q) = \frac{v(t)}{i(t)} = (R_{ON} - R_{OFF})\frac{w(t)}{D} + R_{OFF}$$

$$= R_{OFF}(1 - \frac{w(t)}{D}) \qquad (14)$$

On putting the value of w(t) in eq.(14)
We get,

$$M(q) = R_{OFF}(1 - \frac{\mu_D R_{ON}}{D^2} \mathrm{q(t)}) \qquad (15)$$

Due to smallest value of D, the memristance shows improved characteristics. Nowadays, memristance becomes a lot of necessary for understanding because the dimensions of electronic devices area unit shrinking to nanometre scale.

2.1.2 Window Function

Every model has there definite region in which they work entirely. for example in linear ion drift model , the restricted value of the state variable is varied in the interval [0,*D*]. To keep the state variable into the certain limit, and to add more non-linear behaviour near to the bound , equation (13) is multiplied by a function that nullifies the derivative, and forces equation (13) to be identical to zero when *w* is at a bound. Many window function were projected in literature and there contrast shown in table 2.1.

Table 2.1 Contrast of some window functions

function	**joglekar**	**Biolek**	**Prodromakis**	**TEAM**
f(x)/f(w)	$1-(\frac{2W}{D}-1)^{2p}$	$1\text{-}(\frac{W}{D}-stp(-i)^2$	$j(1-[(\frac{W}{D}-0.5)^2 + 0.75]^p$	$\exp[-\exp\lvert x - x_{on,off}\rvert / w_c]$
symmetric	Yes	Yes	Yes	Not required
Resolve boundary conditions	No	Yes	Partially yes	Partially yes
Scalable factor $f_{max} \leq 1$	No	No	Yes	No
Impose nonlinear drift	Partially	Partially	Partially	Yes
Fits memristive device model	Linear / non-linear ion drift/TEAM	Linear / non-linear ion drift/TEAM	Linear / non-linear ion drift/TEAM	TEAM for simmons tunnelling barrier fitting

2.1.3 Comparison Of Memristor Model

As the linear ion drift model follows the fundamental memristive system eqation and it's self-generated. The behaviour of memristor has shown by experiment is quit nonlinear and linear ion drift model isn't therefore correct. The nonlinear ion drift model is voltage controlled and having nonlinear dependency between state spinoff and voltage. we even have other different model that has been projected and there contrast listed in table 2.2.

Table 2.2 Represent a contrast of memristor models

Model	**Linear ion drift model**	**Nonlinear ion drift model**	**Simmons tunnelings model**	**TEAM**
Control mechanism	$0 \leq w \leq d$ Doped region physical width	$0 \leq w \leq 1$ Doped region normalized width	$\alpha_{off} \leq x \leq \alpha_{on}$ Undoped region width	$x_{on} \leq x \leq x_{off}$ Undoped region width
current-voltage relationship and memristance deduction	Current controlled	Voltage controlled	Current controlled	Current controlled
Generic	No	No	No	Yes
Accuracy	Lowest accuracy	Low accuracy	Highest accuracy	Sufficient acuuracy
Threshold exists	No	No	Partially exist	Yes

Chapter 3

MEMRISTOR IMPLEMENTATION

3.1 ORCAD PSPICE SIMULATION OF MEMRISTOR

To study the properties of memristor, the following circuit as given in fig.3.1 was simulated in the software OrCAD PSpice.

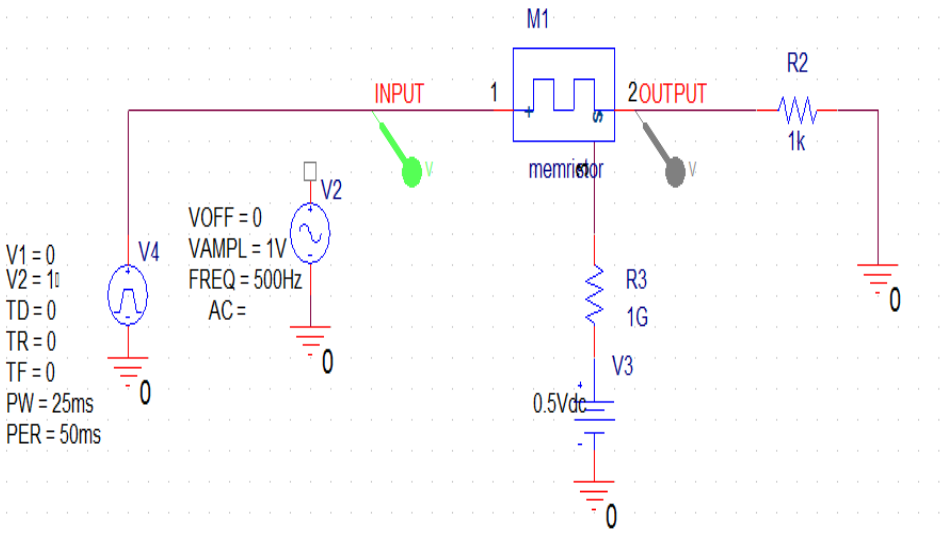


Fig. 3.1: Circuit Diagram of a linear HP model of memristor, modeled in PSpice

The input is a sine wave with 1 Volt amplitude and 500 Hz frequency. The memristive coefficients are R_{on} = 0.001Ω, R_{off} = 1000MΩ and the current are measured on the memristor.

Following are the simulation results shown below

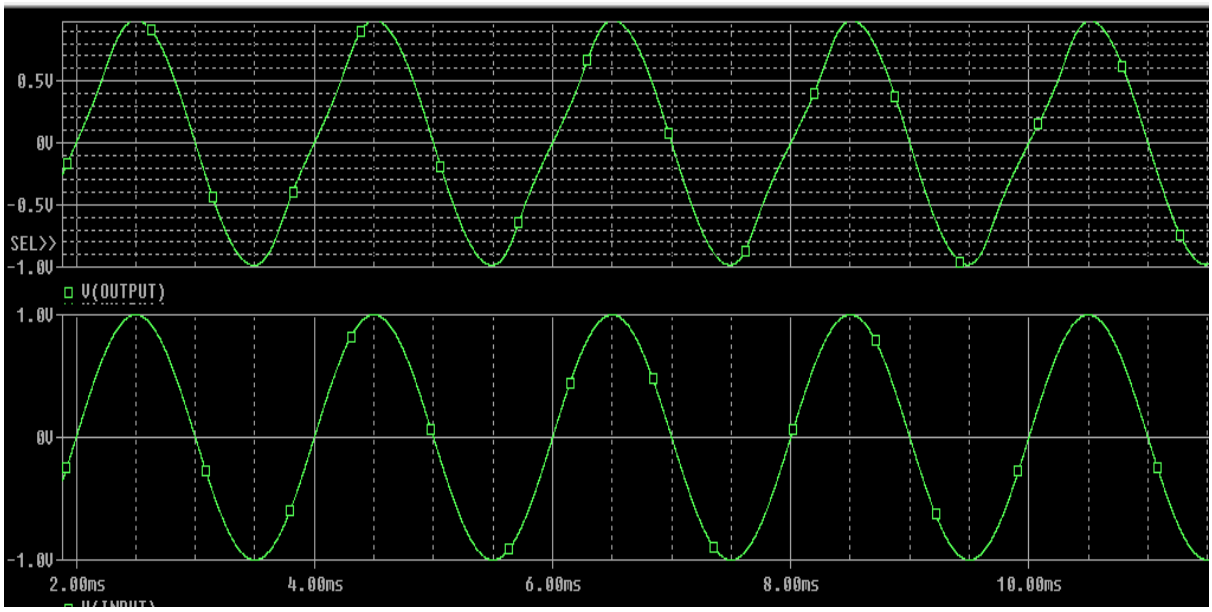


Fig.3.2: Waveform of input voltage and output voltage w.r.t time, simulation is done using Linear HP model in PSpice

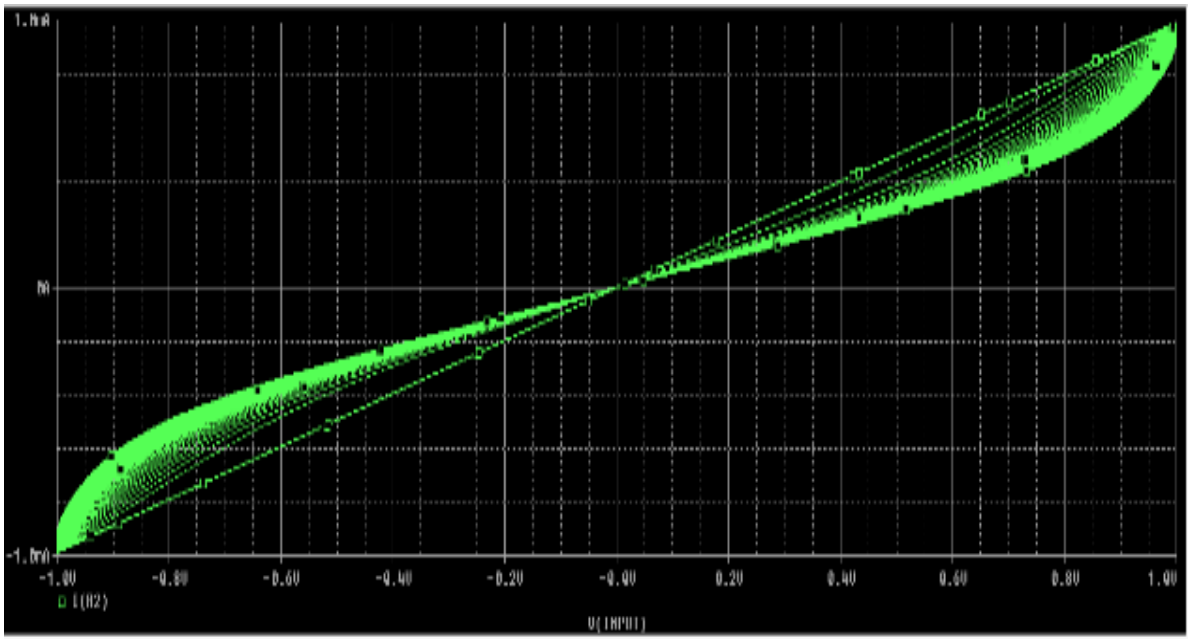


Fig. 3.3: The pinch loop curve between the current and input voltage of a linear HP memristor model

Memristor's hysteresis curve and the input and output voltage w.r.t time are observed and plotted. Fig. 3.2 shows the Input and output voltage waveform w.r.t time. It can be seen from the waveform that both input and output are in same phase with negligible delay, whereas in CMOS device there is always some delay in the output response. Fig. 3.3 shows the pinch loop curve between current and voltage across memristor. The loop is pinched in the origin (0 Amp & 0 V). It can be seen from the figure that the curve is symmetric about the origin.

3.2 PRACTICAL MEMRISTOR MODEL SIMULATION

A practical memristor model VTEAM is designed and implemented using cadence virtuoso platform [9]. It has shown adequate accuracy as compared to memristor models in use. In the schematic of memristor shown in fig. 3.4, input voltage is taken as 1V, frequency is taken as 50 MHz, the value of Roff is taken as 0.2 MΩ and Ron is1000 Ω. Waveforms of output voltage in and output current is presented in fig. 3.5 and current vs. input voltage pinch loop curve is shown in fig. 3.6

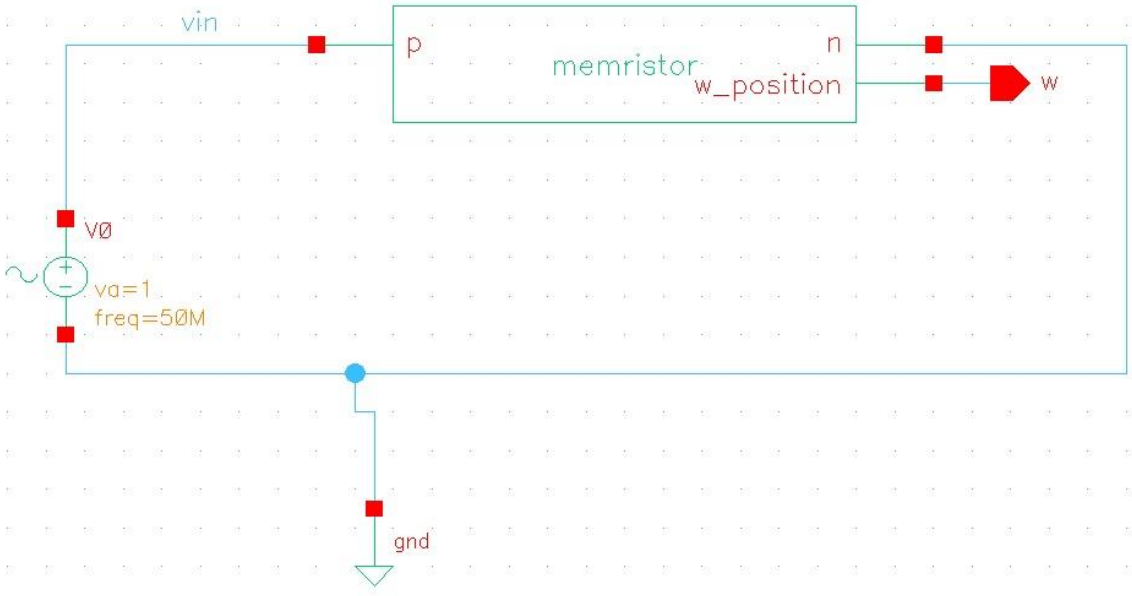


Fig. 3.4: Circuit diagram of a practical memristor model, modeled Using Cadence Virtuoso Platform

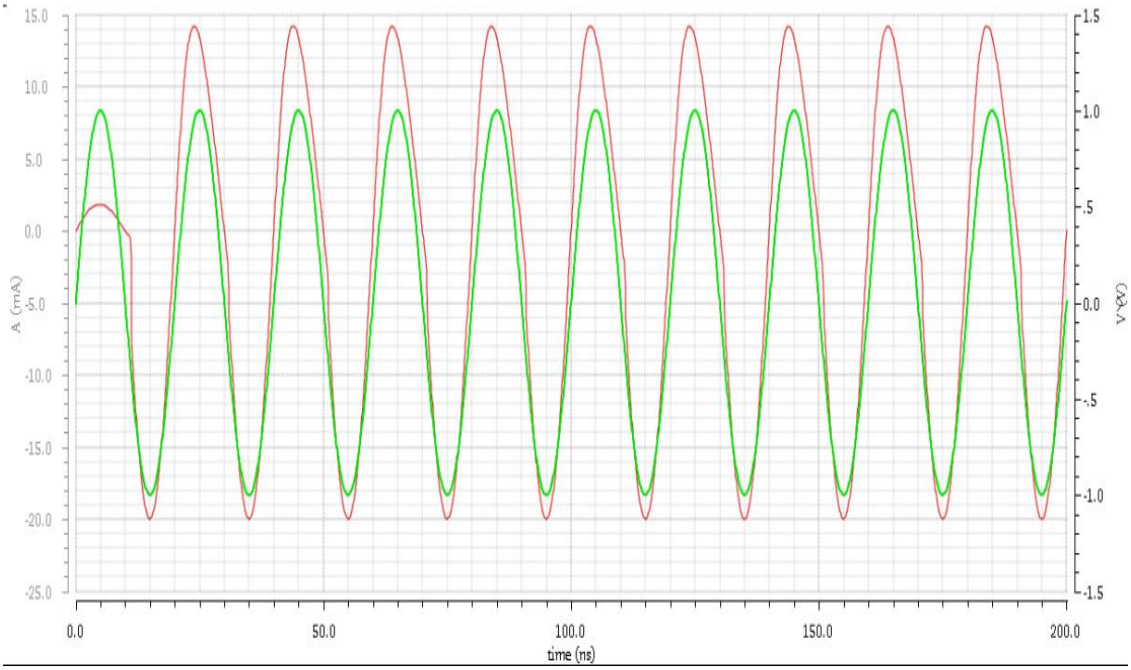


Fig. 3.5: Waveforms of output voltage and output current w.r.t of a practical memristor, simulation done in Cadence Virtuoso

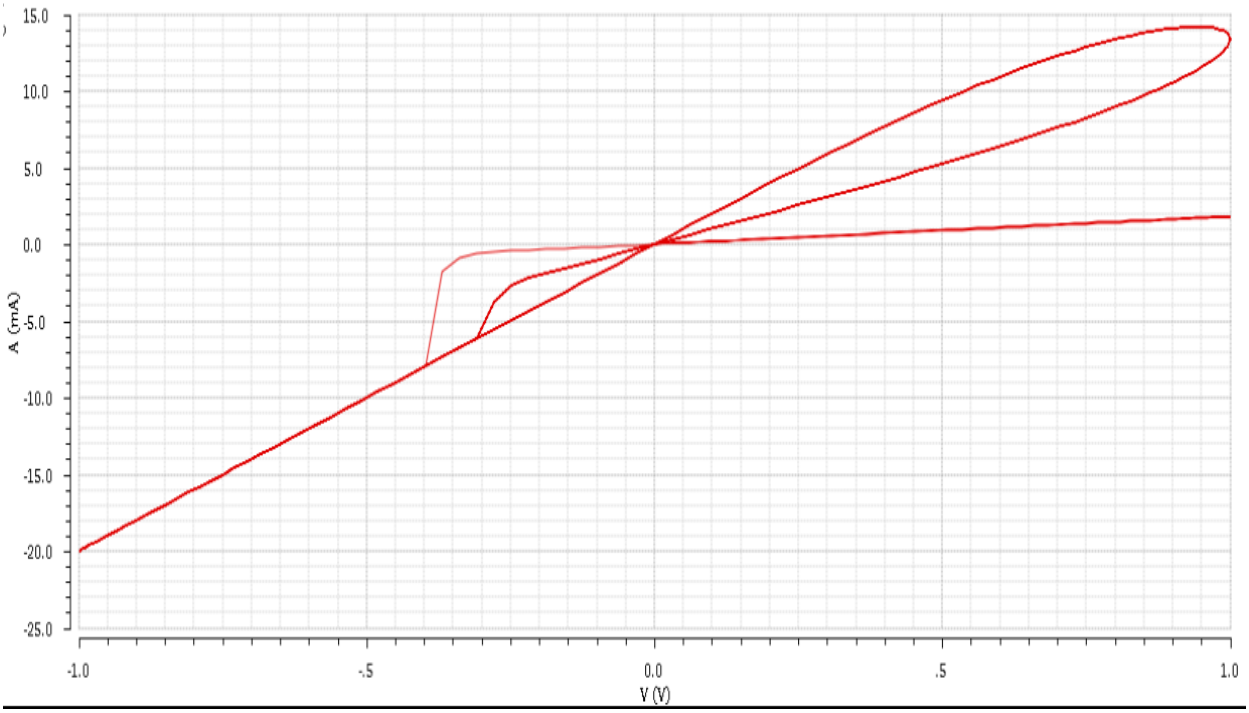


Fig.3.6: Current vs. input voltage pinch loop curve of a practical memristor

Fig. 3.6 shows the pinch loop curve of a practical memristor at 50 MHz, it be seen that the practically the two loops don't have equal area; it is slightly distorted in shape as compared to the pinch loop curve of an ideal memristor.

Chapter 4

LOGIC CIRCUITS

In electronics, logic gates are used for implement Boolean expressions, logical operations. Logical gate are primarily implemented using some transistor or diode for switching, relay etc.

Logic circuit includes such as ALU, multiplexer, registers and microprocessor, which may contains many logic gates. Now a days, mostly gates are manufacture using FET and MOSFET.

In this chapter to implement memristor based logic gates we are using memristor model. Basically integration of memristor with CMOS is travers for logic circuit and memory. Using memristor ratioed logic (MRL) which is a hybrid Memristor-CMOS family, implementation of AND, NOR, XOR, NOT gate has been done.

4.1 MRL (Memristor ratioed logic)

Memristor ratioed logic (MRL) - is one among the method in which integrating memristor with normal CMOS logic or it's a hybrid memristor-CMOS family through which memristor based mostly logic gates enforced. we are able to build AND , OR gate using this methodology for implementation of NOT gate CMOS – inverter is employed and accessorial to produce complete structure and signal restoration . during this logical family, voltage represent the logical state, that is in line with CMOS .
The memristor devices don't seem to be use for storing a logic state however it's used just for logical computation. The initial state solely have an effect on the procedure time, and also the procedure result's freelance of initial state of memristive device.

4.2 LOGIC GATES IMPLEMENTATION

Various memristor models are projected in literatures. For designing the logic gates we've used the threshold adaptative Memristor Model (TEAM) is a memristor model proposed by Shahar Kvatinsky[10], this model is extremely versatile and generic and might be used for any memristor based mostly application. this is often a sufficiently correct model which might be accustomed design the digital logic. This model follows a nonlinear relationship between current and voltage to behave as an actual memristor.

4.2.1 Memristor Based AND and OR GATE

To implement AND/ OR logic gates, it consist two memristor and the connection of these two memristor should be in series with opposite polarity. The common point of two memristor is the output terminal of the gate while the other side we have two input terminals through which input is given to the logic gate. Because of the polarity in memristor, when we pass current to the OR gate the resistance decreases. Similarly, for the AND gate when inputs current flows from one terminal of the AND gate, it is observed that the resistance increases

The memristor AND logic schematic is shown in fig. 4.1, in which input of provided to the p terminal of the memristor which is connected in series and output taken from common terminal .The waveforms are shown in figure 4.2(a)and (b) with different inputs. As seen in figure 4.2(b) there is some spikes shown when there is a change in the input from one state to another, i.e. from high logic to low logic level or visa-versa.

..

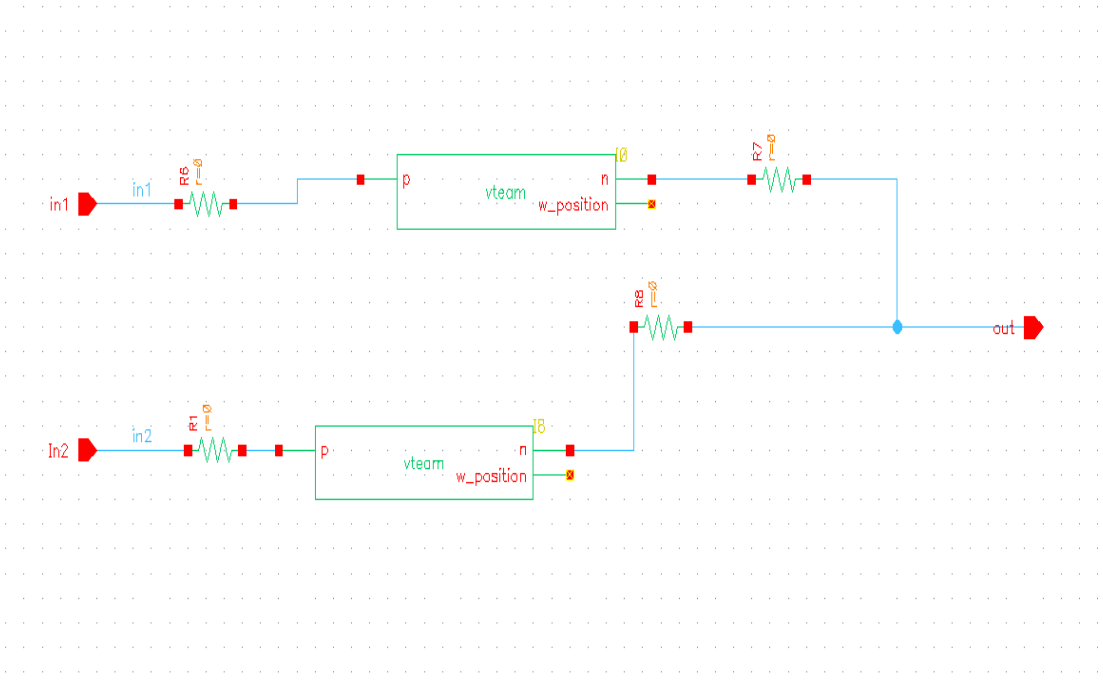
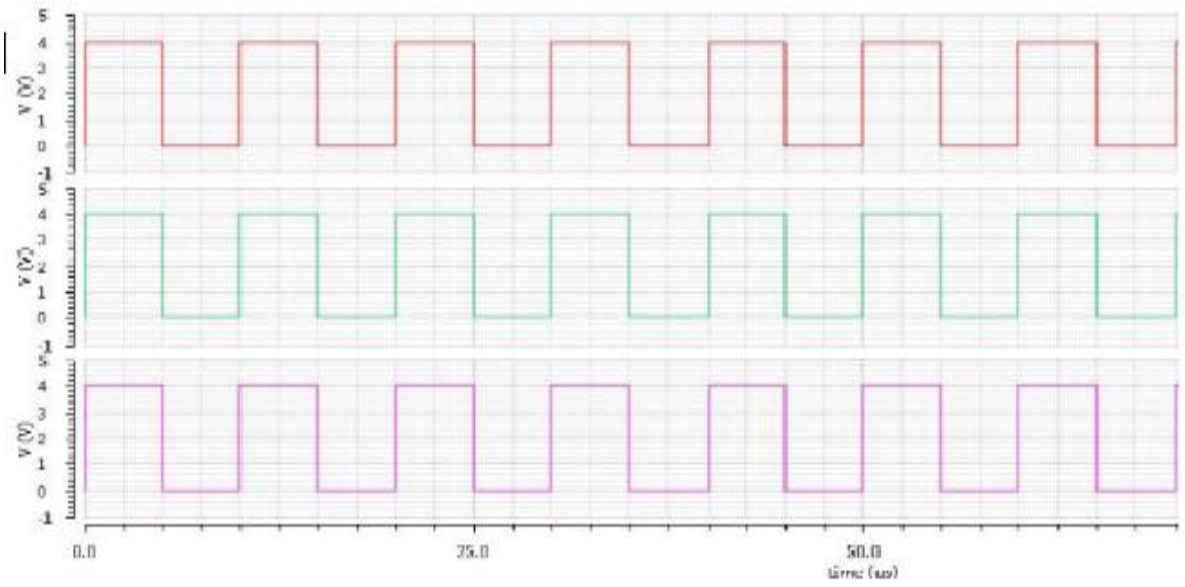
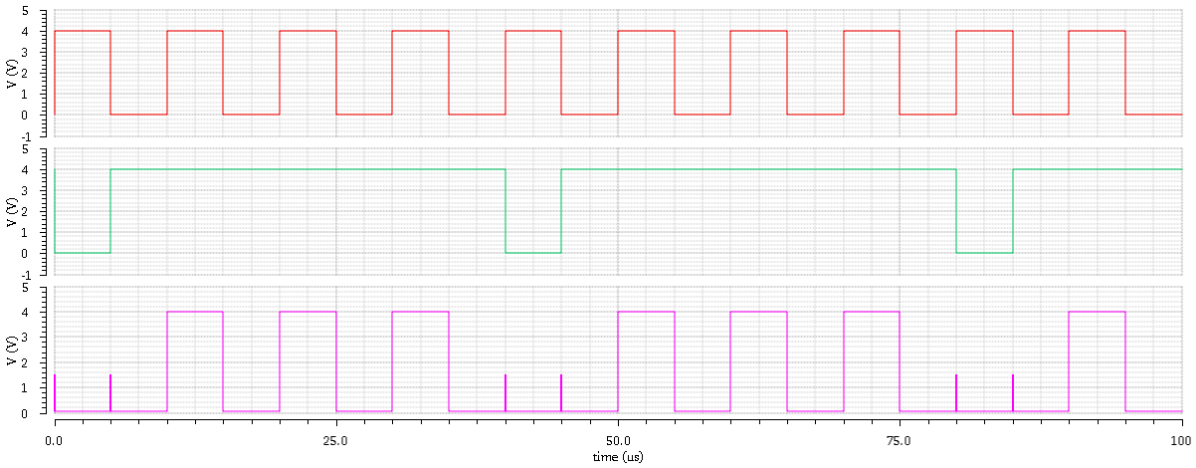


Fig. 4.1: Schematic Diagram of a Memristor AND gate based on MRL

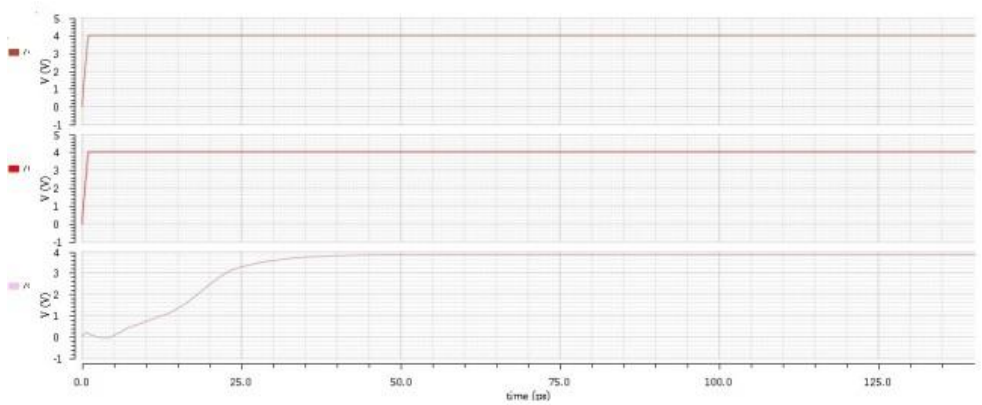


(a)



(b)

Fig. 4.2: Simulation waveform of "AND gate". Simulation is done on Virtuoso Platform



(a)

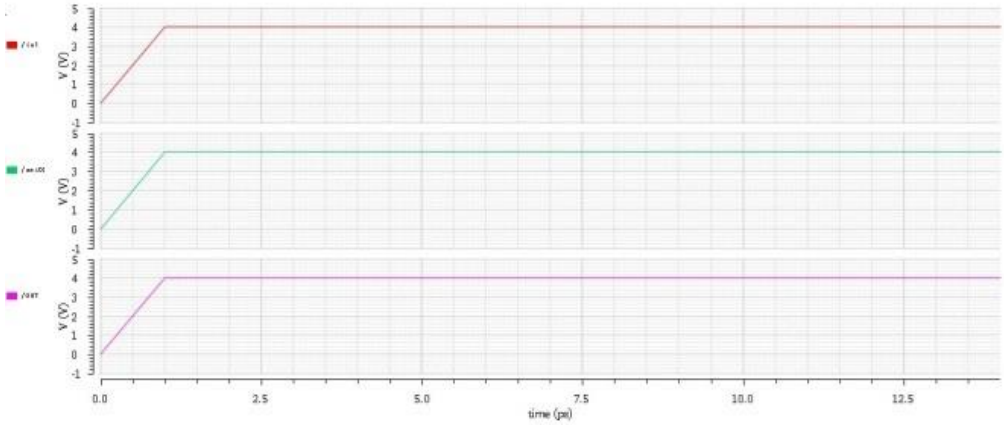


Figure4.3: (a) CMOS AND gate rise time delay, (b) MRL AND rise time delay

Fig. 4.3(a)and (b) shows the input and output rise time delays of CMOS AND gate and MRL AND gate respectively. From these waveforms we can conclude that there is negligible delay in the rise time of MRL gate whereas in CMOS gate there is considerable delay (50ps) to reach its final value. Hence Memristor gives a delay optimized approach in digital logic design

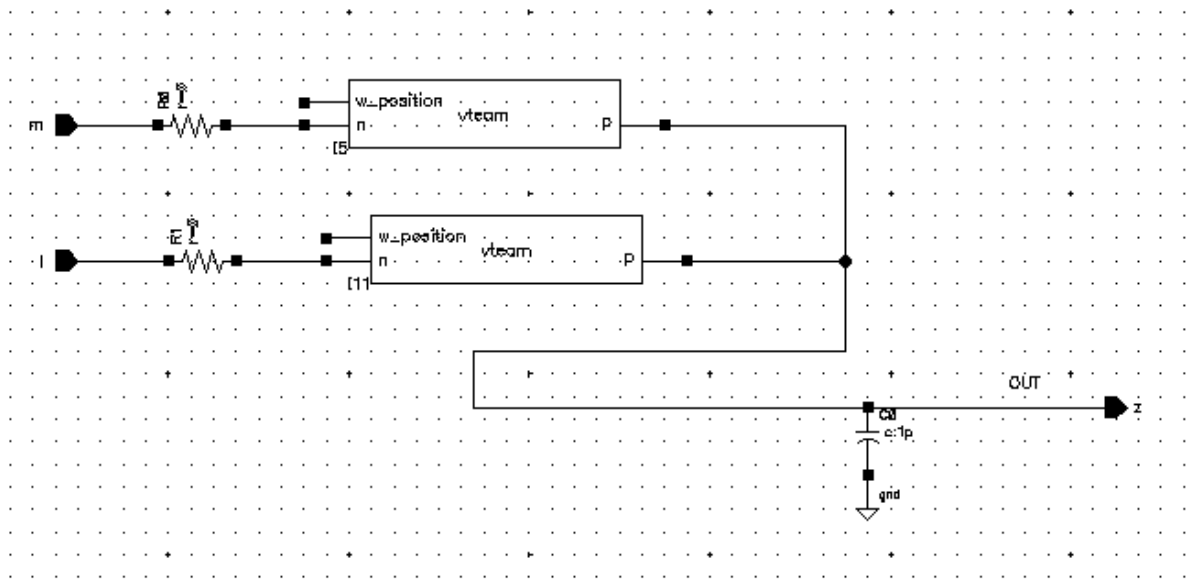


Fig. 4.4: Schematic Diagram of Memristor" OR" gate based on MRL

In fig. 4.4, the schematic of memristor OR logic gate is shown. Input to the memristor OR is given to the opposite polarity or as shown in figure to the n terminal of memristor. Using this memristor based OR gate NOR gate is implemented .

4.2.2 Memristor Based NOR Gate

The NOR logic gate is implemented using a CMOS inverter at the output of the OR gate the schematic is shown in fig. 4.5. The behaviour of Memristor NOR gate with different inputs is shown below in fig. 4.6 (a), (b) and (c). In

this figure we can also observe that Y1 shows the behaviour of memristor OR gate and Y0 is the NOR gate output.

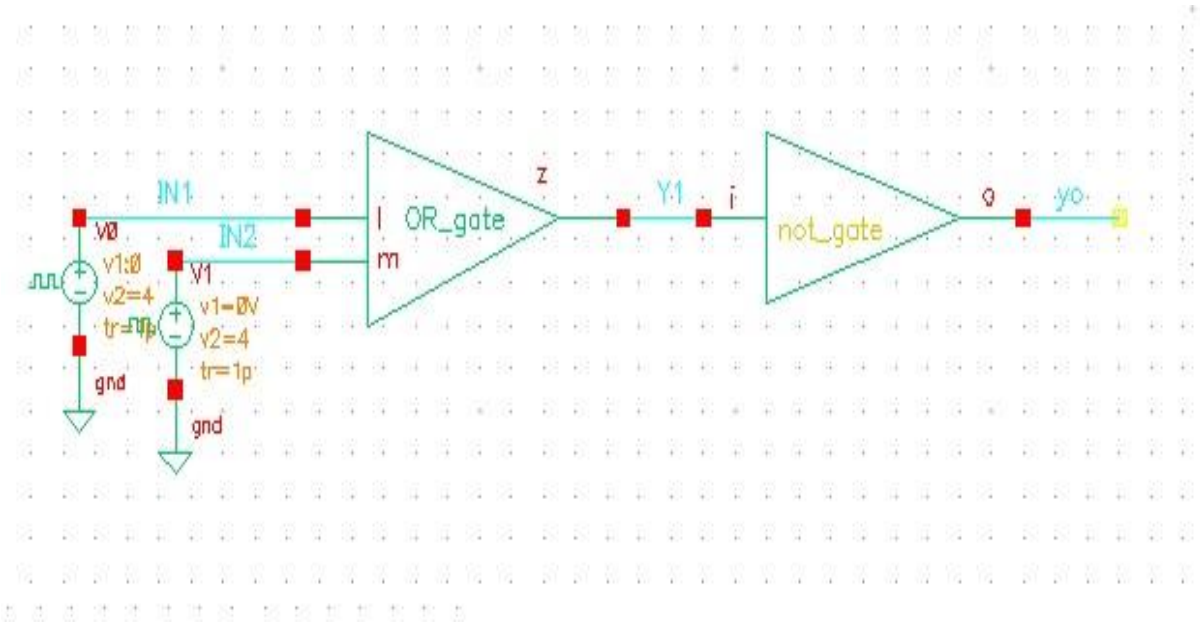
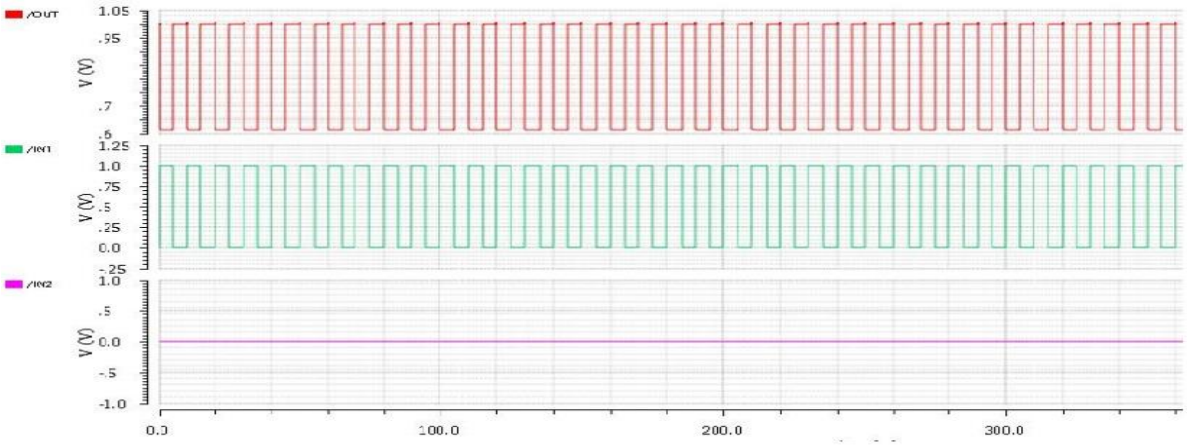
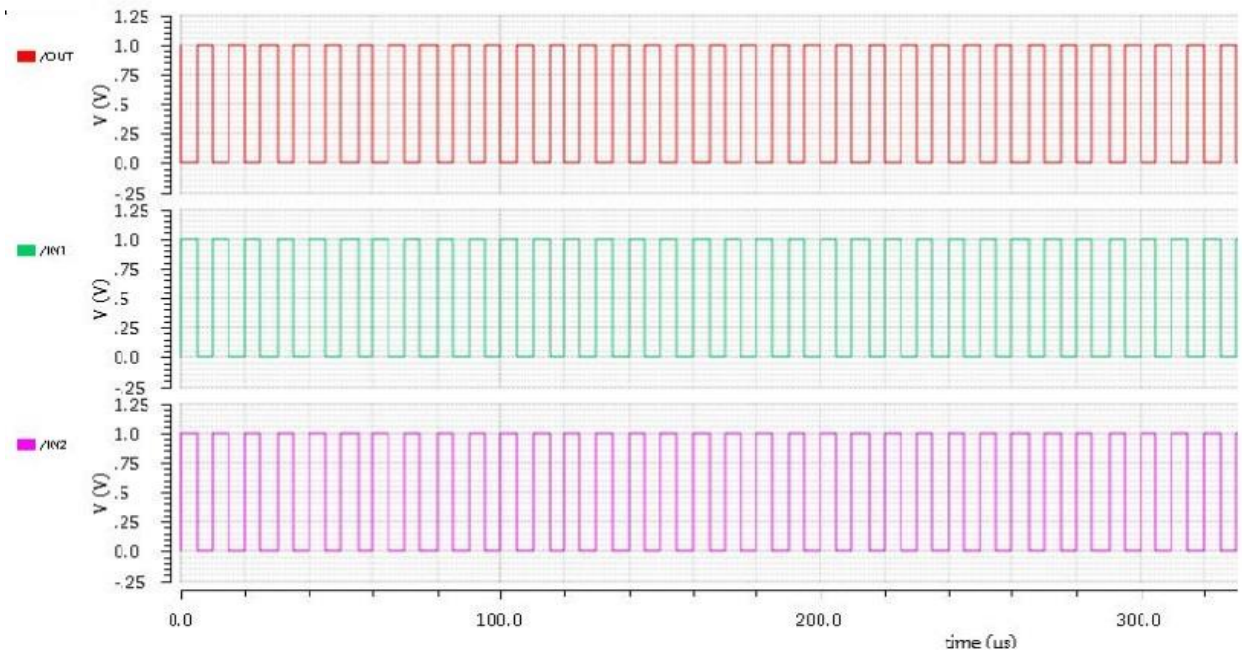


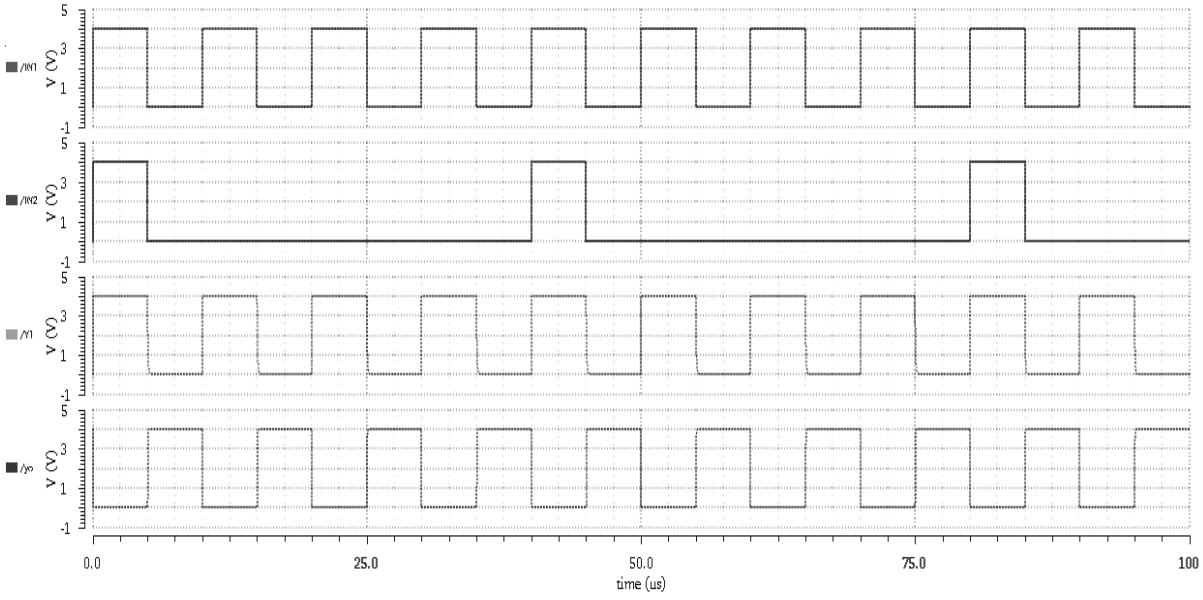
Fig. 4.5: Schematic Diagram of Memristor" NOR" gate based on MRL, It is a combination or a Memristor OR gate and CMOS inverter.



(a)



(b)



(c)

Fig.4.6: Simulation Waveform of a NOR gate where (a), (b) and (c) represent the output of a NOR MRL gate for different input values.

4.2.3 Memristor Based XOR Gate

In this chapter memristor based AND, OR gate is implemented and a hybrid CMOS based NOT gate also implemented with the help of these implemented gate. Now, XOR gate is design.

Using MRL logic gate, implementation of memristor XOR gate schematic shown in fig.4.7 and the output of XOR gate with different inputs shown in fig.4.8. It uses 6 memristor and 4 MOS transistors as compared to 8 MOS transistors used in CMOS XOR gate. Thus, the area of Memristor based XOR gate is significantly reduced. In schematic two NOT gate , two memristor based AND gate and one memristor based OR used. Generalized equation for XOR gate is $A\overline{B} + B\bar{A}$ or in a simplest way we can say that when the both the input is equal the output is zero and when both the input is opposite out will be one.

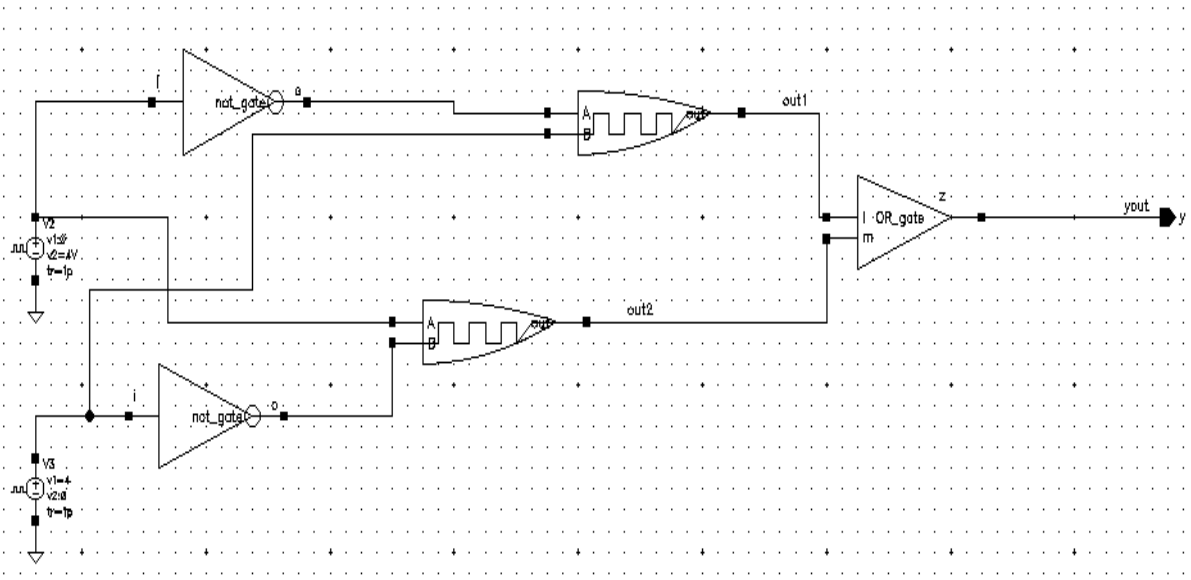


Fig. 4.7: Schematic diagram of memristor based Hybrid XOR gate

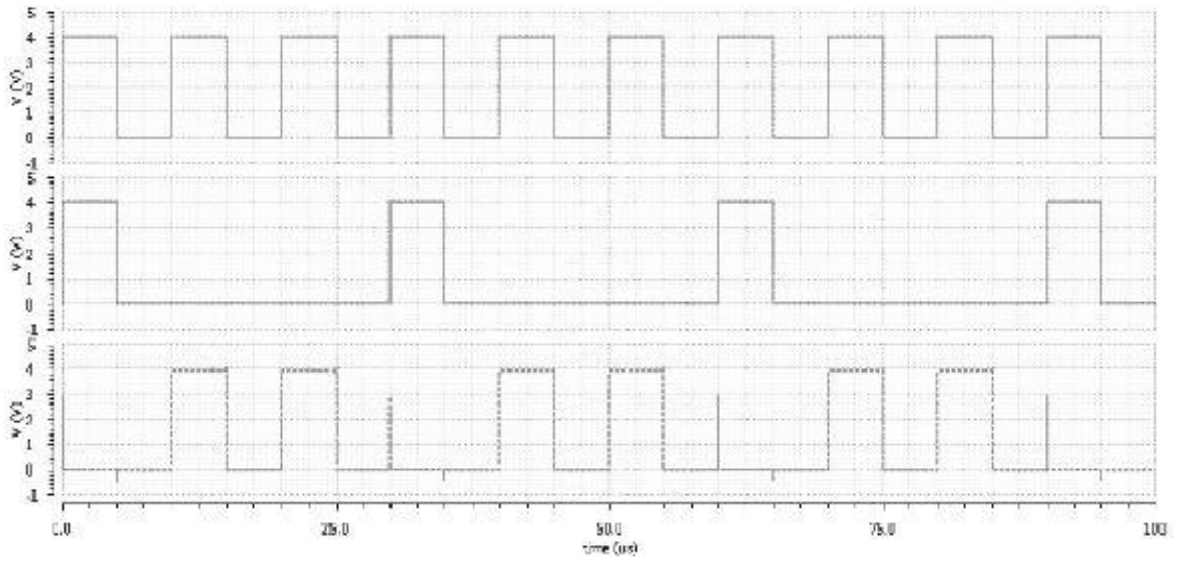


Fig. 4.8: Simulation Waveform represents the output of a XOR gate for different input values

4.2.4 Memristor Based NOT gate

Memristor based NOT gate is implemented using a PMOS and two memristor. PMOS has length of 180nm and width of 1.44 μm based on gpdk 180 nm technology library in cadence virtuoso. A linear drift ion model is used for the simulation for memristor based NOT gate [10]. A CMOS based inverter requires 2 MOS transistors whereas Memristor NOT gate requires only 1 MOS transistor and 2 Memristor. The schematic is shown in fig.4.8 input provided to the p terminal of the memristor and to the gate terminal of PMOS with vdd (voltage source) connected to source terminal. Two memristor n-terminal is connected together with output node and PMOS transistor act as switch. Input to the PMOS $v_i = 0$ is in on state, the output voltage will be shown below

$$v_0 = R_{eq} * I_D$$

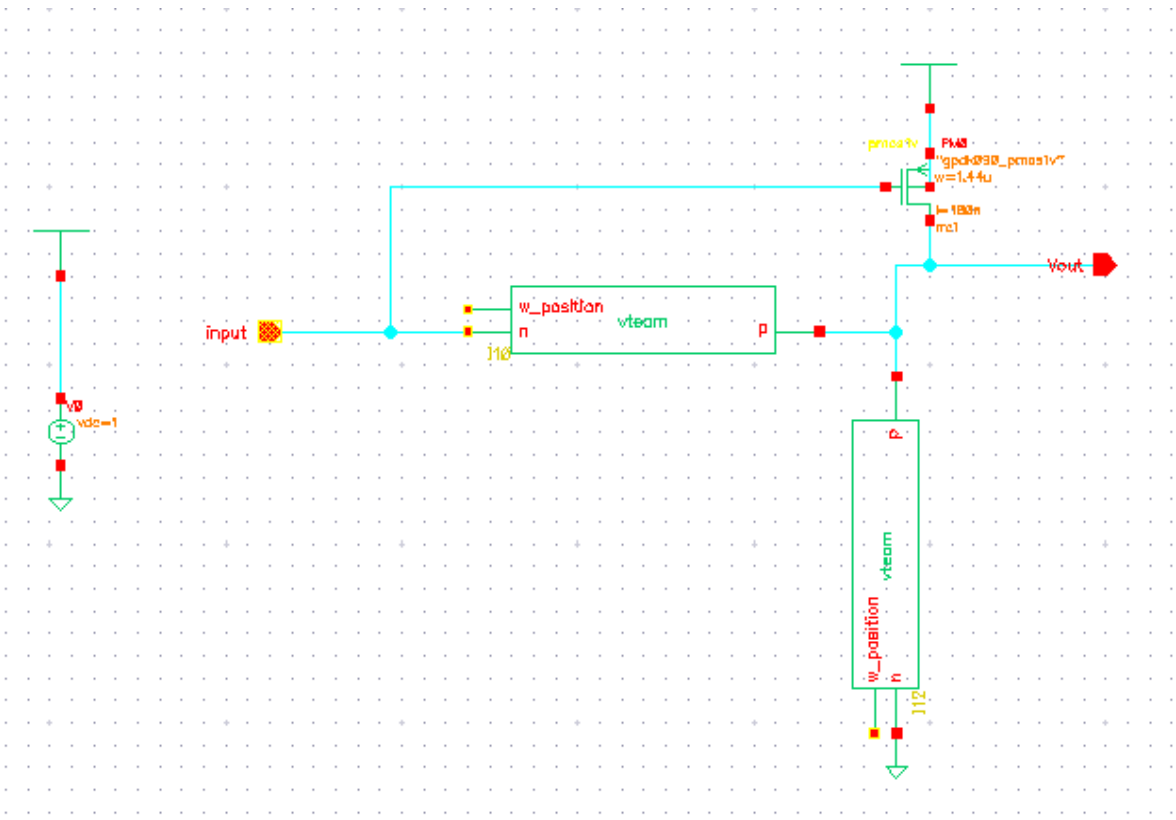


Fig.4.9: Schematic diagram of Memristor NOT gate which has a PMOS transistor with length=180 nm and width =1.44um

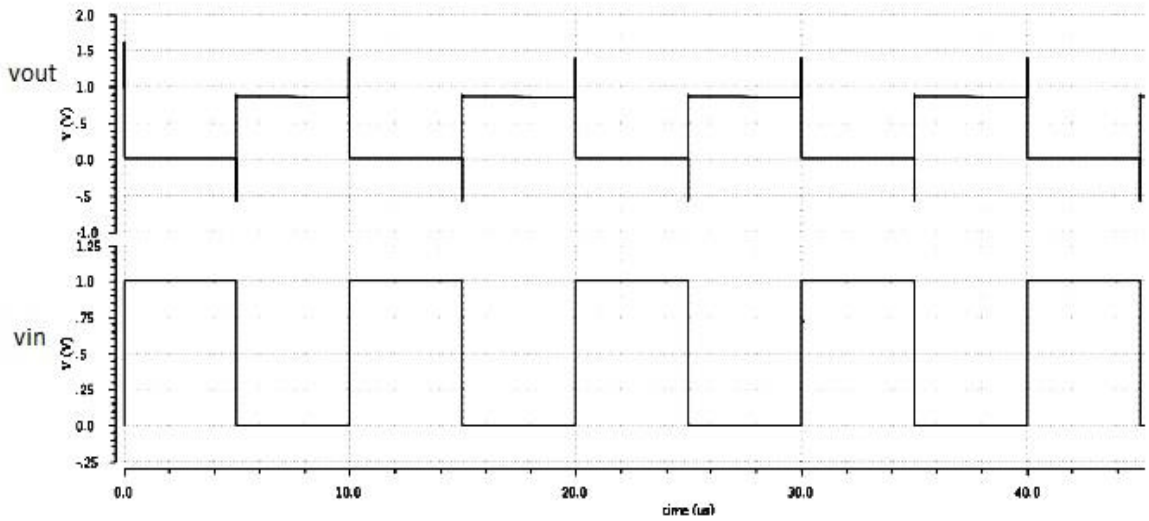


Fig. 4.10: Output waveform of a Memristor inverter

In figure 4.10 output of memristor based NOT gate has been shown. As you look in the output wave form, when we provide logic one to the memristor NOT gate output is showing logic zero simultaneously if we provide logic zero as a input it shows logic one approximately and it behaves like NOT gate . There is some spikes also comes may be due to the memristor model has been used.

4.2.5 POWER CONSUMPTION COMPARISION

In the above section we implemented memristor based NOT gate and we all are commonly familiar with CMOS based inverter (NOT gate). We always looking forward towards the low power consumption and less area. Integration of memristor with CMOS for designing the complex digital logic circuits helps to overcome the area and also significantly reduce power consumption of the computing system. As seen in fig. 4.11 and 4.12 there is a significantly less power consumption in memristor based NOT gate as compare to the CMOS based inverter.

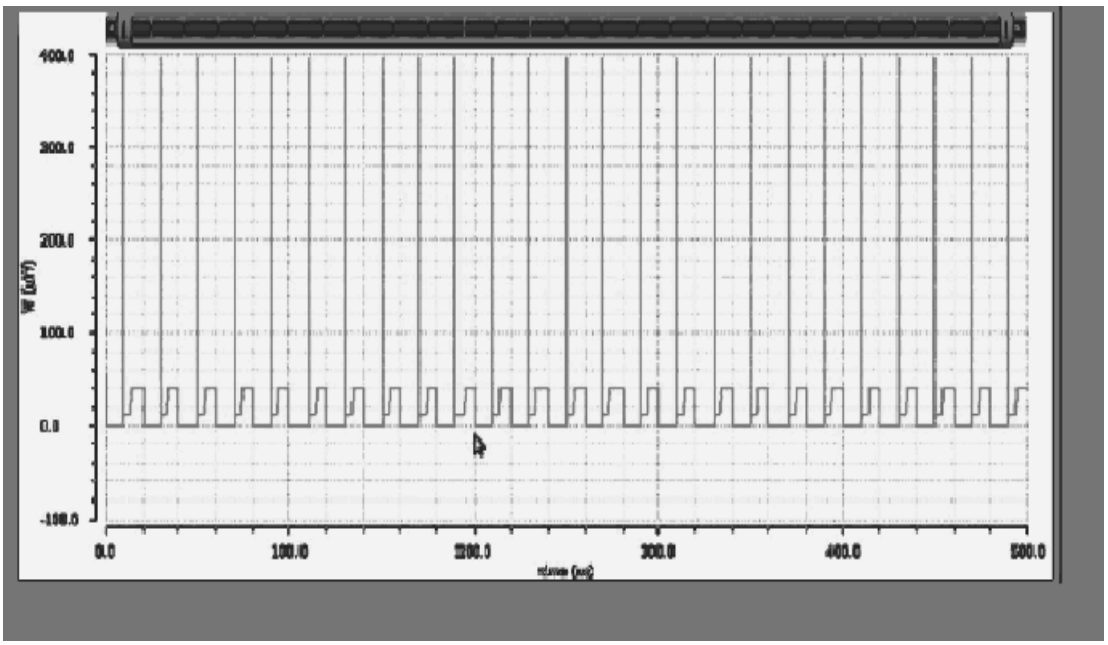


Fig. 4.11: power consumption of memristor based NOT gate (38 µW)

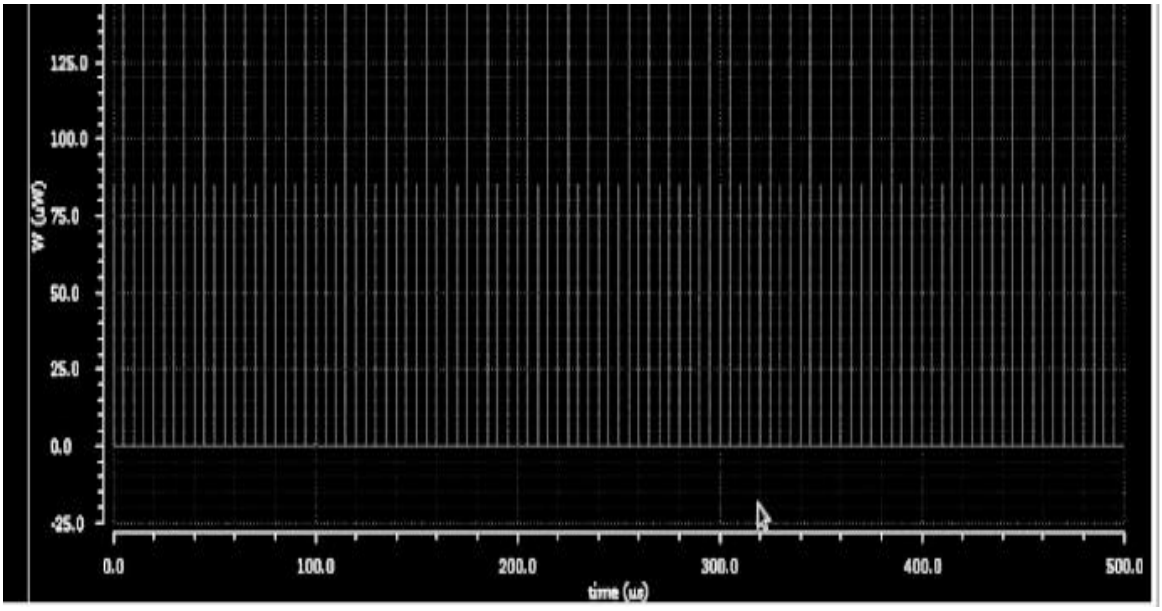


Fig. 4.12: power consumption of CMOS based NOT gate (78 µW)

In the above figure power graph has been shown, looking in the graph we can easily compute that memristor based NOT gate has power 38 µW and CMOS based inverter has power around 78 µW. On comparison, it has 40µW difference of power and these result is computed in cadence virtuoso platform .

Chapter 5

APPLICATIONS

Memristor-Based Digital Analog Differential Circuit

5.1 AN ANALOG DIFFERENTIAL CIRCUIT

A circuit which amplifies the difference of two input voltage $v^+ and\ v^-$ is well known difference or differential amplifier.

$$v_o = A(v^+ - v^-) \qquad (1)$$

A: Differential gain or Differential mode gain

Common mode output is the output voltage of a differential amplifier when $v^+ = v^-$ and for ideal differential amplifier CM output is zero but in practical amplifier CM output is non-zero because of dissimilarity in two transistors i.e , output voltage is given by

$$v_{cm} = \frac{v^+ + v^-}{2} \qquad (2)$$

$$v_D = v^+ - v^- \qquad (3)$$

A typical circuit is shown in fig 5.1 which is CMOS technology based having two source coupled MOS transistor M1 and M2 both are identical and biased in saturation region by a constant source I_O .

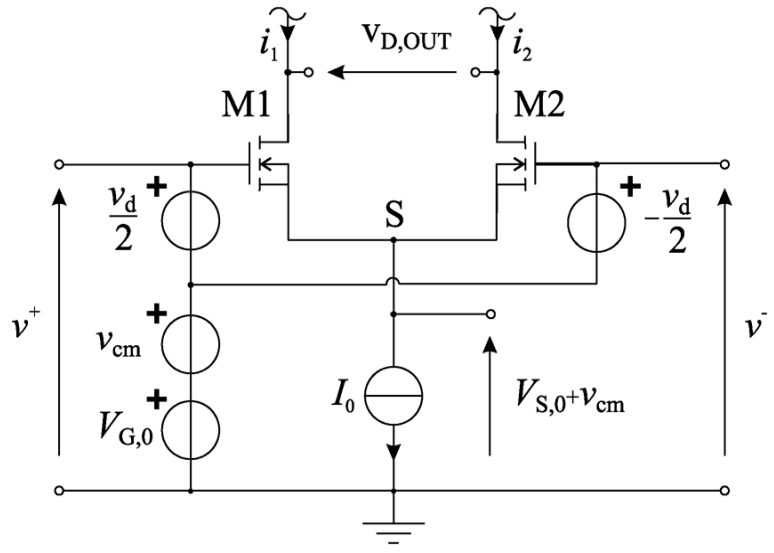


Fig 5.1. A CMOS differential pair

5.2 A MEMRISTOR BASED DIGITAL DIFFERENTIAL CIRCUIT

A memristor- based digital differential circuit is derived from [12] . In which two a pair of single ended buffer is used as a digital implementation of digital stage

if input signal $v_{input} > v_{ths}$ the output of each buffer provide "HIGH" output = "1" i.e $v_{out} = v_{oh} > v_{ths}$

Similarly, when the input signal $v_{input} < v_{ths}$ the output is "LOW" i.e, $v_{out} = v_{ol} < v_{ths}$ shown in fig.5.2

The out of buffer is related to DM input voltage in a differential circuit.

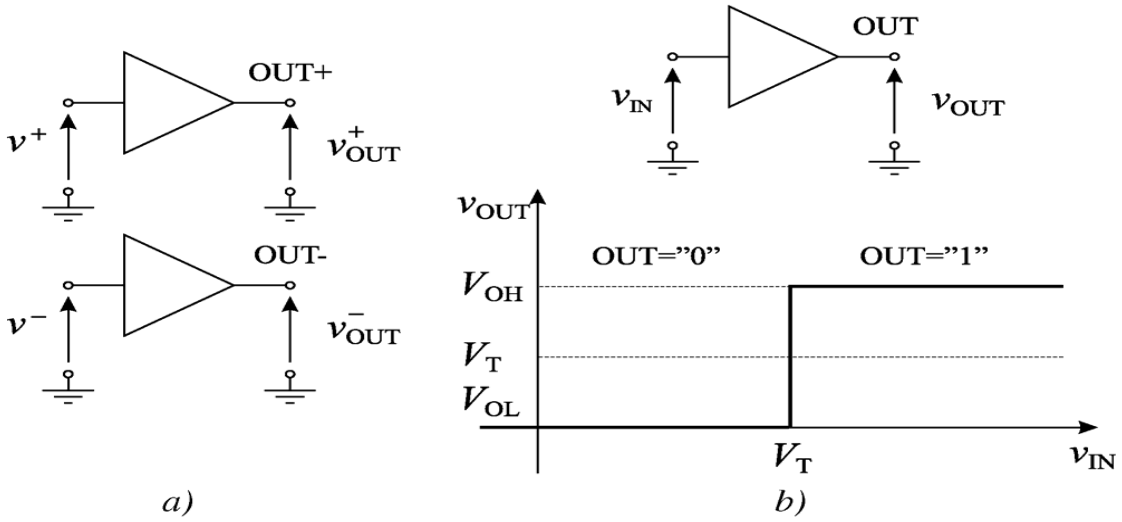


Fig5.2. (a) A pair of single ended buffer

(b) input /output characteristic

$$v^+ > v_{ths}\ and\ v^- < v_{ths} \rightarrow v_D > 0 \quad (4)$$

It follows that,

$$(v_{out+}, v_{out-}) = (1,0) \rightarrow v_D > 0 \quad (5)$$

Similarly,

$$v^+ < v_{ths}\ and\ v^- > v_{ths} \rightarrow v_D < 0 \quad (6)$$

It follows that,

$$(v_{out+}, v_{out-}) = (0,1) \rightarrow v_D < 0 \quad (7)$$

In the case, when we have the condition

$$(v^+ > v_{ths}\ \&\ v^- < v_{ths} \rightarrow v_D)$$

$and\ (v^+ < v_{ths}\ \&\ v^- > v_{ths})$, the input expressed as

$$v^+ = v_{ths} + \frac{v_D}{2} + v_{cm} \qquad (8)$$

$$v^- = v_{ths} - \frac{v_D}{2} + v_{cm} \qquad (9)$$

$$\text{With, } |v_{cm}| = \left|\frac{v_D}{2}\right| \qquad (10)$$

In order that,

$$v^+ > v_{ths}\ and\ v^- > v_{ths} \rightarrow v^+ + v^- > 2v_{th}$$

It follows,

$$(v_{out+}, v_{out-}) = 1 \rightarrow v_{CM} > v_{th} \quad (11)$$

Similarly,

$$(v_{out+}, v_{out-}) = (0,0) \rightarrow v_{CM} < V_{th} \quad (12)$$

When the equation (10) is satisfied by external inputs figure.5.2 (a) will operate like a differential stage only.

In figure 5.3 derived Memristor Based Differential Amplifier circuit has been shown . we added a v_{cmp} which is a compensated voltage to the inputs so that we can express the input voltage of buffer as

$$v^{+\prime} = \frac{v^+ + v_{cmp}}{2} \qquad (13)$$

$$v^{-\prime} = \frac{v^- + v_{cmp}}{2} \qquad (14)$$

The relation of external differential mode and common mode component as

$$v_D{}' = \frac{v_D}{2} \quad \text{and} \quad v_{cm}{}' = \frac{v_{cm}+v_{cmp}}{2} \quad (15)$$

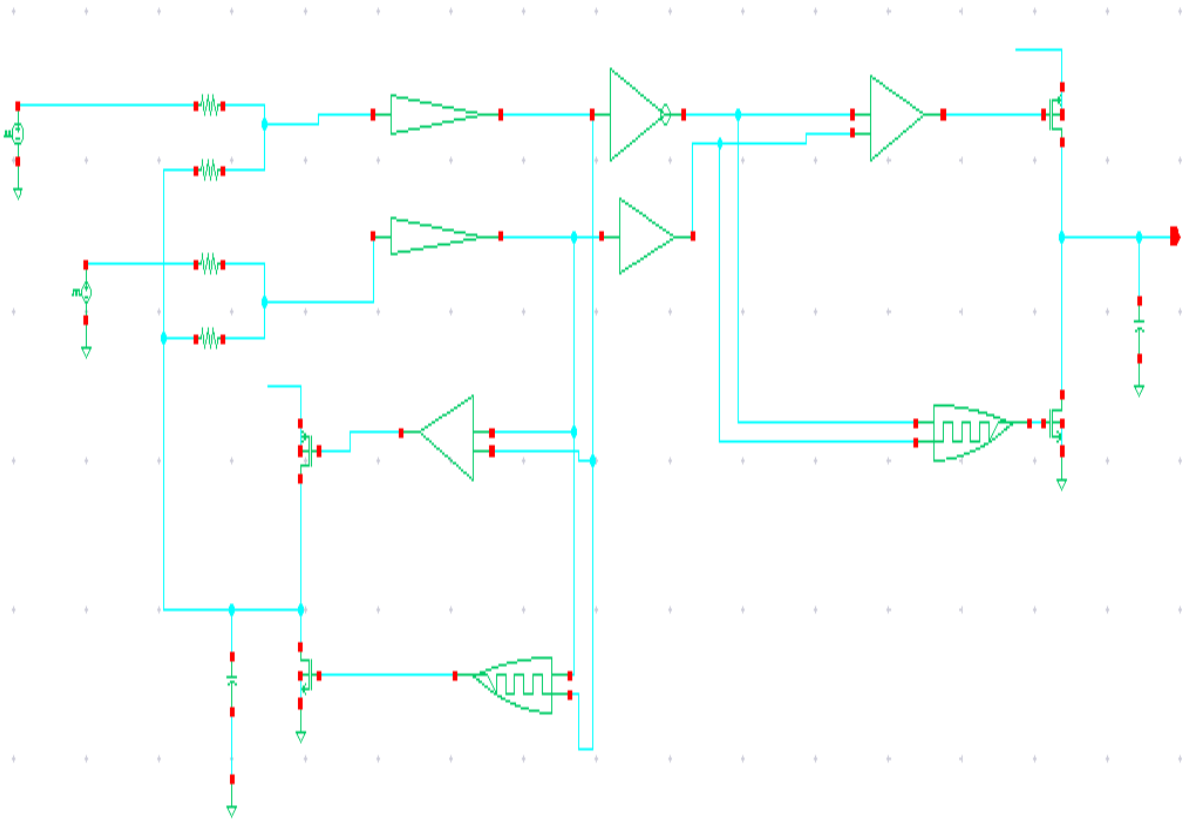


Fig.5.3 A Memristor based digital- differential circuit

The behavior of CM extractor block is as follow that when we have the output voltage of buffer $(v_{out+}, v_{out-}) = (0,0)$ the PMOS transistor is turn on and current is passed into the capacitor ,so that vcmp increase and consequently $v_{cmp}{}'$expressed in (15) similarly when we have the (1,1) as a output of buffer NMOS get turn on there is decrease in $v_{cmp}{}'$.

The output stage behaviour is include M3and M4 and a c_{out} capacitor when we applied (0,0) and (1,1) , CM control active and both M3 and M4 are off and $vout$ is kept constant but when we applied the (1,0) configuration , M3 is turn on and the voltage increased on other hand (0,1) configuration M4 is turn on so that the output voltage decreases .

In conclusion the complete circuit can be called as a (OTA) operational transconductance amplifier so that it has input as a voltage and output as a current .

In figure 5.4 we have shown the power consumed by theDigital-based analog differential circuit .

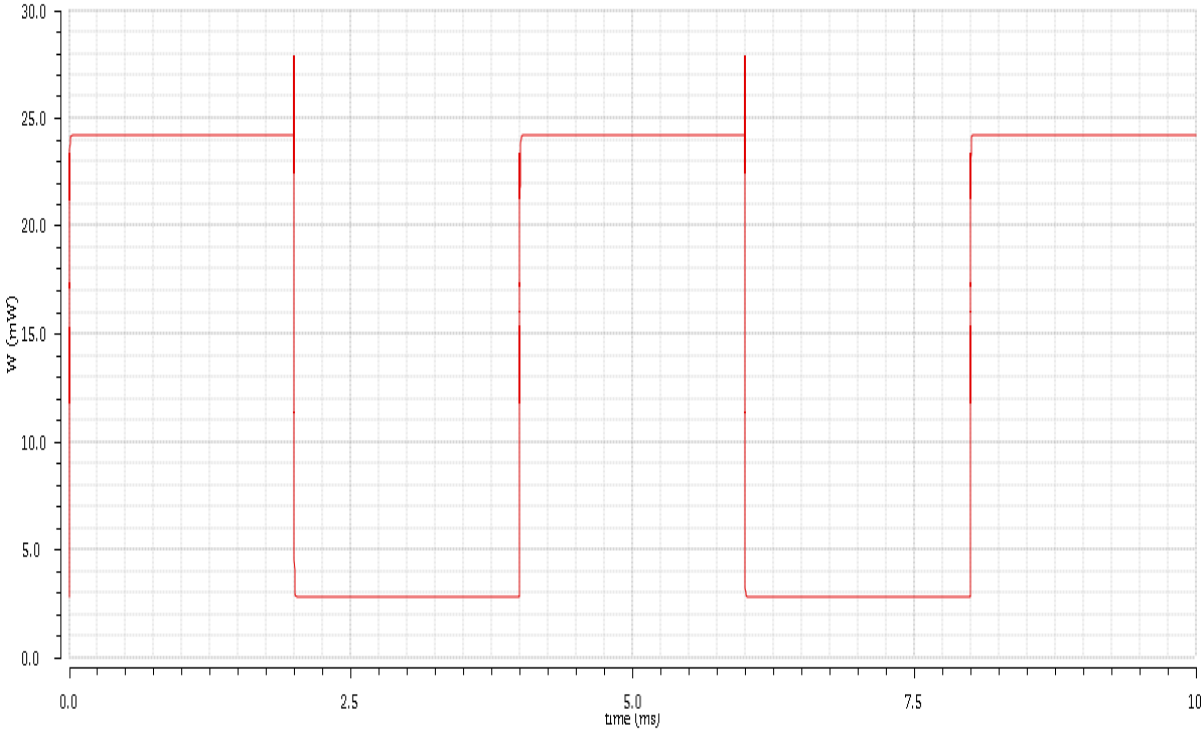


Figure 5.4 power consumed by digital based differential amplifier

It can be seen that it is approximately 24.23mw on other hand in figure 5.5 memristor-based digital analog differential amplifier power graph shown and we can conclude from there that is around 19mw . we can see that it has a difference around 5 mw and it is not so much but we have lots of research in this area we can get better results.

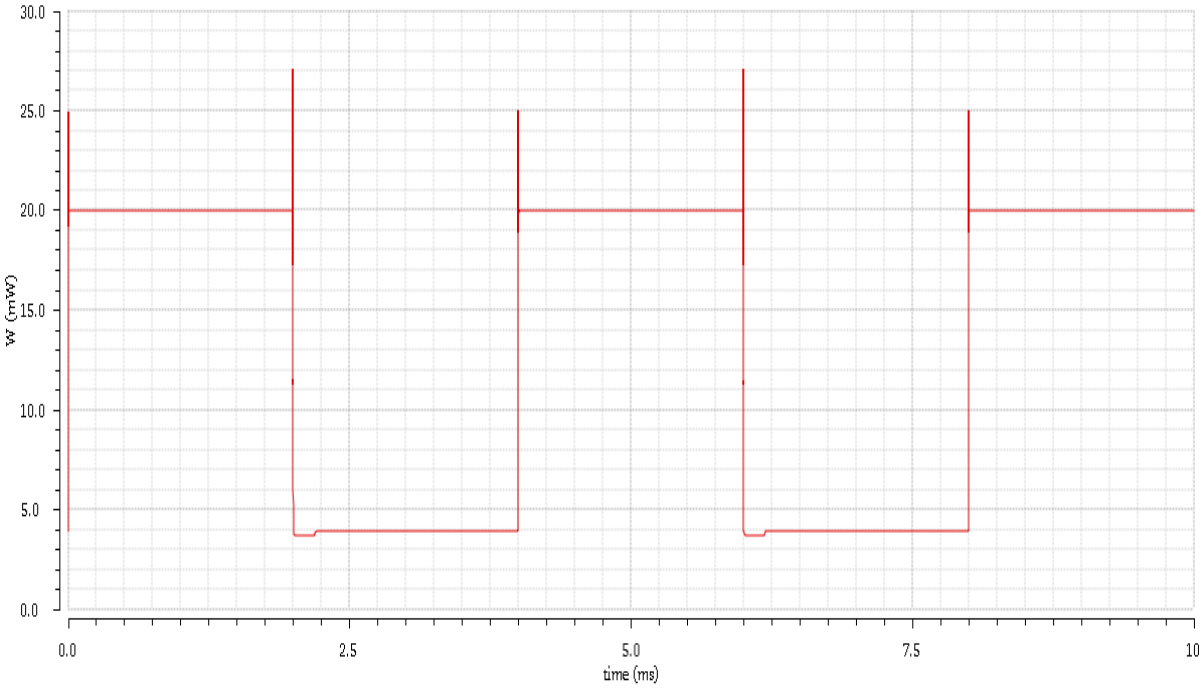


Figure5.5 power consumed by memristor-based digital differential amplifier

5.3 Memristor Based Half Adder

Half Adder consists of one XOR gate and one AND gate. In the half adder circuit we get the SUM from the output terminal of XOR gate and CARRY from the output terminal of AND gate. The schematic of memristor-based half adder shown in fig 5.6.

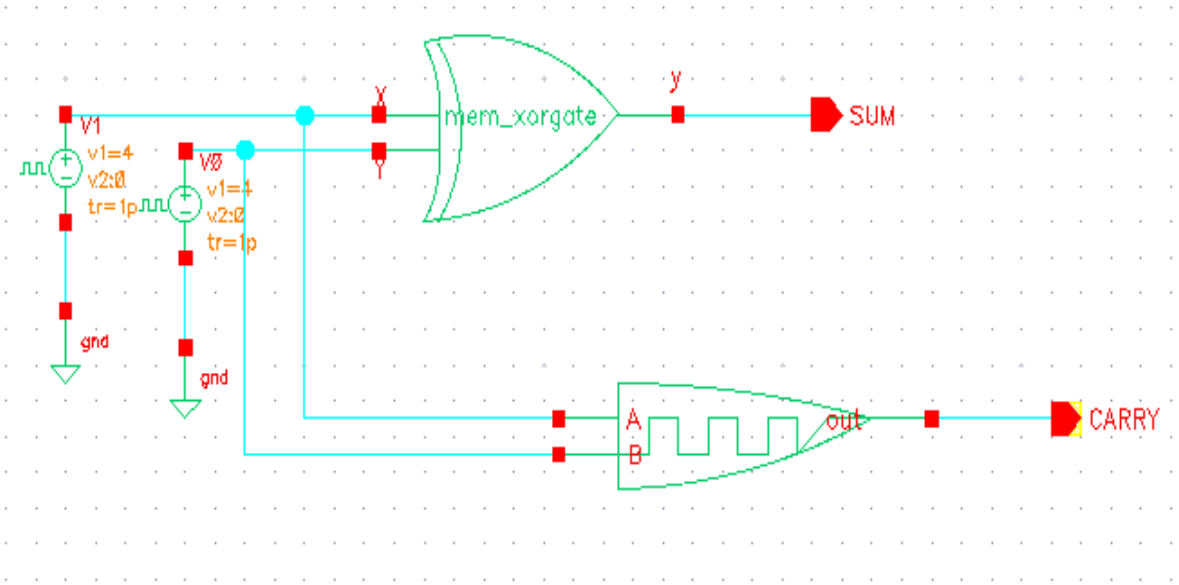


Fig5.6 schematic of memristor-based Half adder

Logical expressions,

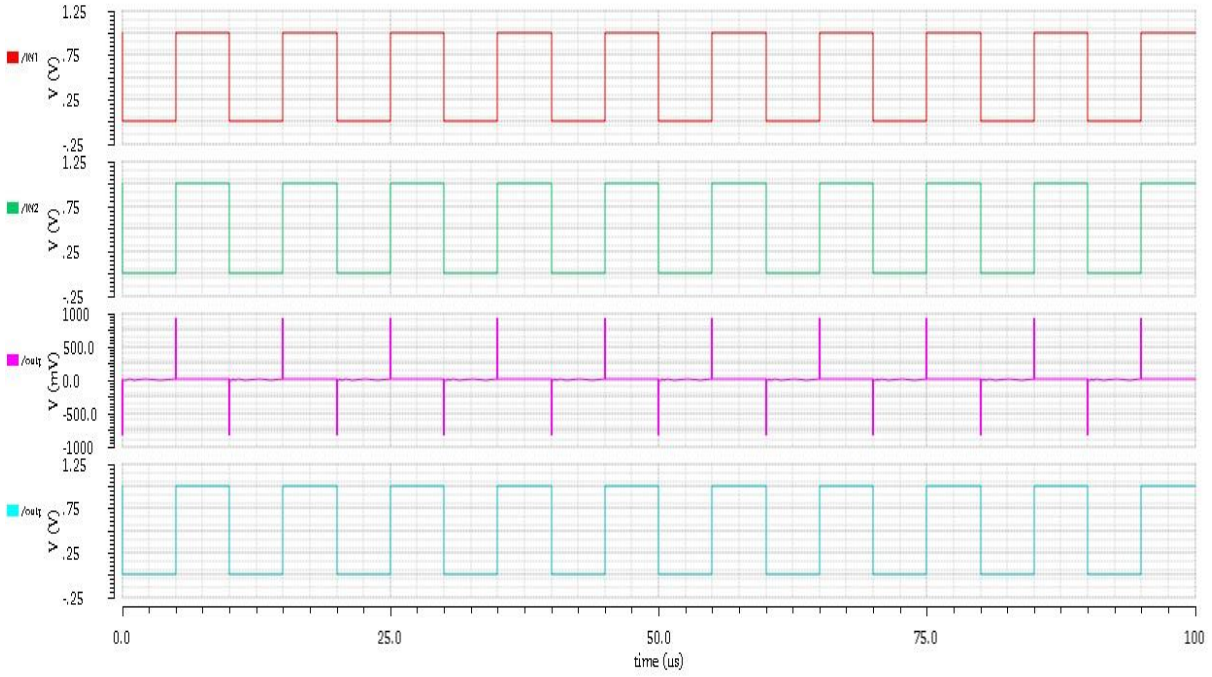
$$\text{SUM} = \bar{A}B + A\bar{B} = A\ XOR\ B$$

CARRY= A.B

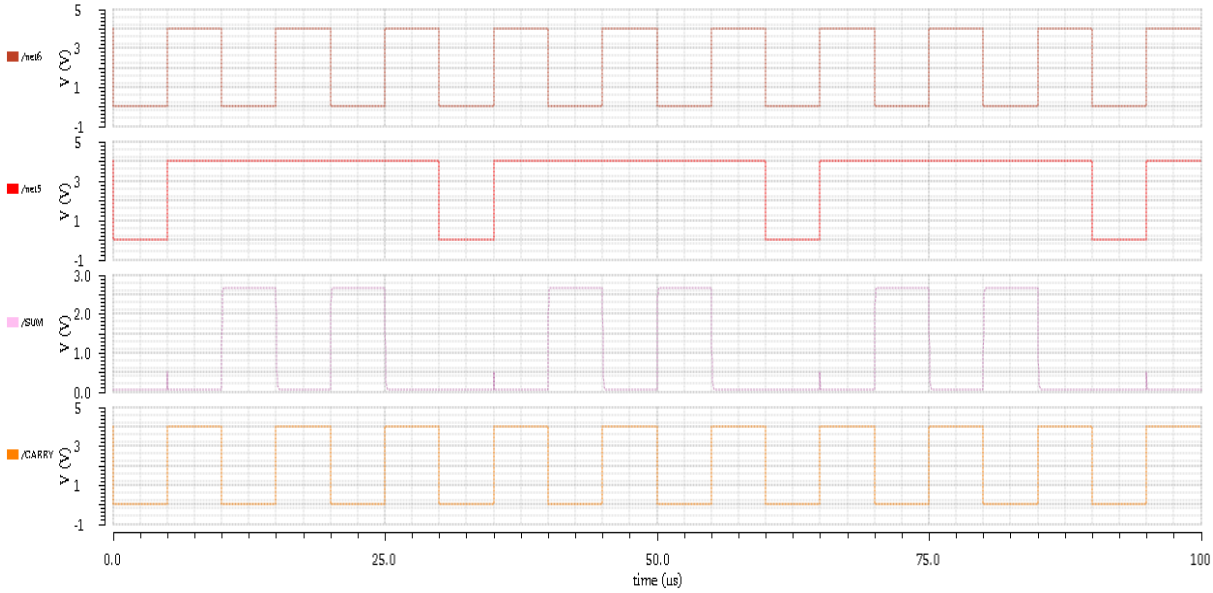
Truth table

A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

In figure 5.7, simulated result of memristor-based Half Adder has been shown which is implemented in cadence virtuoso.



(a)



(b)

Figure 5.7 simulated result of memristor bsed half adder

Chapter 6

CONCLUSION

This Thesis presents a detailed study of the memristor based digital designs. The properties of the memristor and the model by HP are discussed. The practical model of memristor is simulated in Cadence Virtuoso Platform subjecting it to various input voltages, frequencies of operation, initial resistances of the memristor, and phases of input sinusoidal voltage and noting the results obtained.

As inferred from this paper memristor based systems are better than CMOS based system in terms of trade of such as power, area and delay. They have a fast response time and less power consumption and less area, which make them ideal for digital architecture design. However, more research is required and more analysis need to be done on a large architectural scale using all the models and window functions so that an optimum Model is used for the design.

The future work will focus of the design of digital architectures such as combinational and sequential circuits such as Decoders, Multiplexers, Latches and Flip Flops so that a clear analysis is done.

Published paper

4th International Conference on 'Microelectronics, Circuits and Systems', Micro2017

Optimized Design of Digital Logic Gates Based On Memristor

Agrawal P, Kumar M and Tripathi. M.M
Delhi Technological University, New Delhi – 110042, INDIA
pratyushagrawaldtu@gmail.com, kumarashu216@gmail.com, mmtripathi@dce.ac.in

ABSTRACT

The CMOS based devices have reached the Moore's limit and cannot be scaled down further; also there is not much improvement in the power consumption and the speed of these devices in past years. Research is going on to find a suitable alternative to CMOS based devices. Memristor is one such alternative to CMOS. This paper gives a brief introduction of memristor and its modeling. Memristor digital logic gates have been designed and presented based on memristor ratioed logic (MRL) in Cadence Virtuoso. Simulation results show that memristor based gates have a fast response time and less power consumption, which make them ideal for digital architecture design and a suitable alternative for CMOS designs.

Keywords: Memristor, Memristive systems, TEAM, logic gates design, SPICE

I. INTRODUCTION

There are three well known fundamental elements in circuit theory such as resistor, capacitor and inductor. The fourth fundamental element stated to be the memristor by Chua in 1971 [1]. The relation between current and voltage gives resistance, current and flux gives inductance and voltage and charge gives capacitance. In order to have symmetry the mathematically stated relation between charge (q) and flux (φ) gives memristor as dφ=Mdq Where M is memristance.

Memristor is a passive device with two terminals and shows variable resistance. Any change in the memristance is related with the previous resistance/ state of the memristor device. A time-invariant, current controlled memristive device as represented by eq. 1 and eq. 2 is used to represent a memristive system [2].

$$\frac{dw}{dt} = f(w,i), \qquad (1)$$

$$v(t) = R(w,i)\cdot i(t), \qquad (2)$$

Where 'w' is a variable representing state, current flowing in memristor at any time is given as i(t), v(t) represents voltage across the memristor and memristance is R(w, i) at any given time t.

Memristor have many applications such as analog circuit design, filters, oscillators, logic design, memory, neural networks. Memristor provides different merits such as non-volatility, zero leakage current, small size and potential as compared with MOS technology. In this paper a linear circuit memristor model is implemented in OrCAD PSpice as well as a practical memristor model is modeled using Cadence Virtuoso. Using memristor ratioed logic (MRL) which is a hybrid Memristor-CMOS family, implementation of AND, NOR, XOR, NOT gate has been done. Also comparison between the power consumption of CMOS based NOT gate and hybrid memristor based NOT gate has been presented [3]. It is a hybrid of memristor and CMOS logic, also called Mi-MOS. In MRL, OR and AND logic gates are purely memristive in nature and CMOS inverter is integrated to provide a perfect logic structure and signal integrity [5]. The MRL family is compatible with CMOS logic since the logical state is shown in MRL is by voltage as in CMOS.

Rest of the paper is arranged in following manner. Section II discusses the memristor model. Section III presents the ORCAD Pspice simulation of memristor and simulation of practical memristor model is presented in section IV. Logic gates using memristor models are implemented and presented in section V. Section VI presents the conclusion.

II. MEMRISTOR MODELS

Two different memristor models are discussed below.

A. HP Lab memristor model

In 2008 Stanley Williams with his research group at HP Labs fabricated the memristor in the form of device. [6]. A very thin film of titanium dioxide (TiO_2) was kept between platinum (Pt) electrodes having one side of TiO_2 doped with oxygen vacancies to fabricate a memristor [7]. The device fabricated by HP is shown in fig. 1.

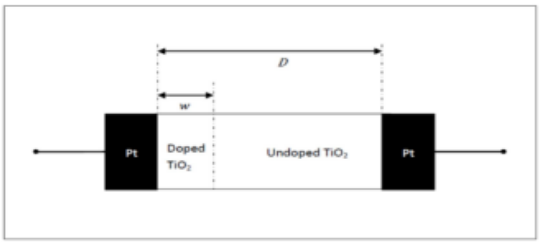


Fig. 1: Schematic of HP memristor

The memresistance in this simple mathematical model of the HP memristor is given by eq. 3 [8].

$$M(q) = R_{OFF}\left(1 - \frac{R_{ON}}{\beta} q(t)\right) \quad (3)$$

Where q(t) is the charge passing through the memristor at a time t, R_{ON} is "on-state" resistances and ß= D2/μD and μD is the average drift velocity.

B. Linear Ion Drift Model

The schematic of this model is shown in fig. 2 below which is different than the HP model. In this model the width of the doped region W(t) is given by eq. 4 in presence of uniform electric field across the memristor device.

W(t) = carrier velocity X carrier drifting time

$$W(t) = \mu D\, E(t) \times \frac{q(t)}{i(t)}$$
$$= \mu D\left(\frac{v(t)}{D}\right) \times \frac{q(t)}{i(t)}$$
$$W(t) = \mu D \frac{Ron}{D} q(t) \quad (4)$$

Variable W(t) is limited to values between 0 and D.

Applying Kirchhoff's law, we get the potential across memristor by eq. 5.

$$V(t) = \left(Ron\frac{w(t)}{D} + Roff\left(1 - \frac{w(t)}{D}\right)\right) i(t) \quad (5)$$

Assuming that Ron is very small as compared to Roff, memresistance is given by eq. 6.

$$M(q) = \frac{v(t)}{i(t)} = (Ron - Roff)\frac{w(t)}{D} + Roff = Roff\left(1 - \frac{w(t)}{D}\right) \quad (6)$$

Putting the value of w(t) in eq. 6, we get the memresistance from eq. 7 below.

$$M(q) = Roff\left(1 - \frac{\mu d\, Ron}{D} q(t)\right) \quad (7)$$

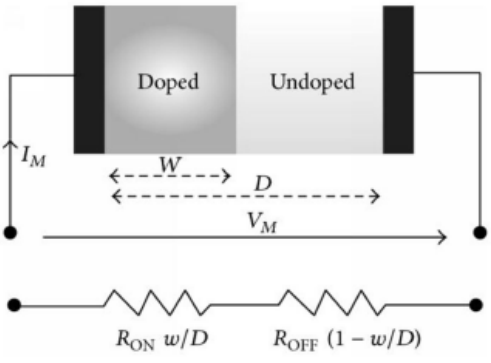


Fig. 2: Detailed schematic of HP memristor

III. ORCAD PSPICE SIMULATION OF MEMRISTOR

To study the properties of memristor, the following circuit as given in fig. 3was simulated in the software OrCAD PSpice.

The input is a sine wave with 1 Volt amplitude and 500 Hz frequency. The memristive coefficients are R_{on} = 0.001Ω, R_{off} = 1000MΩ and the current are measured on the memristor.

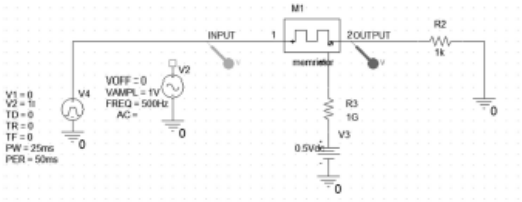


Fig. 3: Circuit Diagram of a linear HP model of memristor, modeled in PSpice

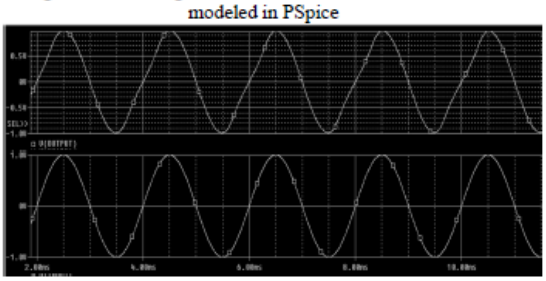


Fig. 4: Waveform of input voltage and output voltage w.r.t time, simulation is done using Linear HP model in PSpice

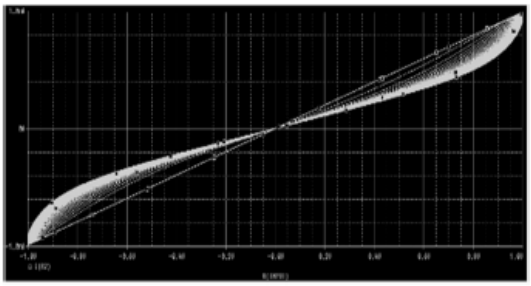


Fig. 5: The pinch loop curve between the current and input voltage of a linear HP memristor model

Memristor's hysteresis curve and the input and output voltage w.r.t time are observed and plotted. Fig. 4 shows the Input and output voltage waveform w.r.t time. It can be seen from the waveform that both input and output are in same phase with negligible delay, whereas in CMOS device there is always some delay in the output response. Fig. 5 shows the pinch loop curve between current and voltage across memristor. The loop is pinched in the origin (0 Amp & 0 V). It can be seen from the figure that the curve is symmetric about the origin.

IV. PRACTICAL MEMRISTOR MODEL SIMULATION

A practical memristor model VTEAM is designed and implemented using cadence virtuoso platform [8]. It has shown adequate accuracy as compared to memristor models in use. In the schematic of memristor shown in fig. 6, input voltage is taken as 1V, frequency is taken as 50 MHz, the value of Roff is taken as 0.2 MΩ and Ron is1000 Ω. Waveforms of output voltage in and output current is presented in fig. 6 and current vs. input voltage pinch loop curve is shown in fig. 7.

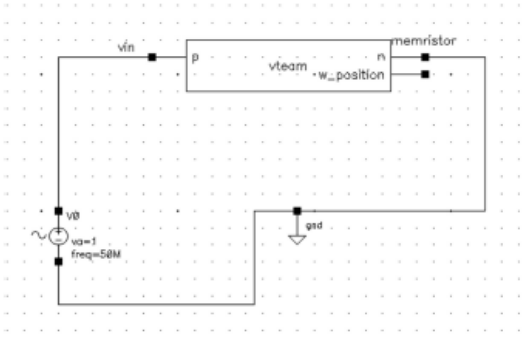


Fig. 6: Circuit diagram of a practical memristor model, modeled Using Cadence Virtuoso Platform

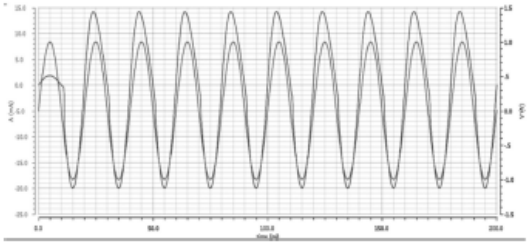


Fig. 7: Waveforms of output voltage and output current w.r.t of a practical memristor, simulation done in Cadence Virtuoso

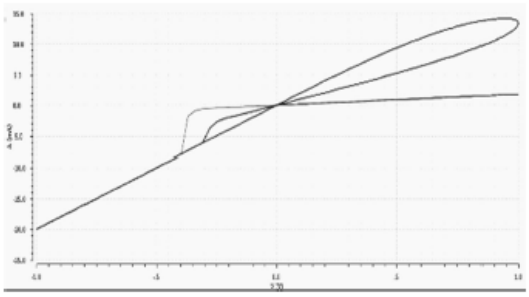


Fig.8: Current vs. input voltage pinch loop curve of a practical memristor

Fig. 8 shows the pinch loop curve of a practical memristor at 50 MHz, it be seen that the practically the two loops don't have equal area; it is slightly distorted in shape as compared to the pinch loop curve of an ideal memristor.

V. LOGIC GATES IMPLEMENTATION USING MEMRISTOR MODELS

Various memristor models have been proposed in literatures. For designing the logic gates we have used the ThrEshold Adaptive Memristor Model (TEAM) is a memristor model proposed by Shahar Kvatinsky[4], this model is very flexible and generic and can be used for any memristor based application. This is a sufficiently accurate model which can be used to design the digital logic. This model follows a nonlinear relationship between current and voltage to behave as an actual memristor.

To implement AND/ OR logic gates, it consist two memristor and the connection of these two memristor should be in series with opposite polarity. The common point of two memristor is the output terminal of the gate while the other side we have two input terminals through which input is given to the logic gate. Because of the polarity in memristor, when we pass current to the OR gate the resistance decreases. Similarly, for the AND gate when inputs current flows from one terminal of the AND gate, it is observed that the resistance increases.

The memristor AND logic schematic is shown in fig. 9, in which input of provided to the p terminal of the memristor which is connected in series and output taken from common terminal .The waveforms are shown in figure 10(a)and (b) with different inputs. As seen in figure 10(b) there is some spikes shown when there is a change in the input from one state to another, i.e. from high logic to low logic level or visa-versa.

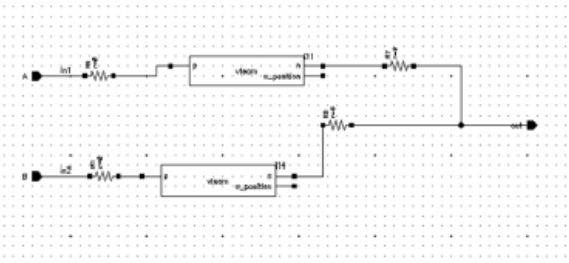
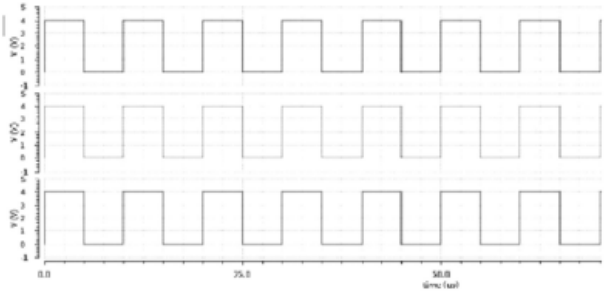
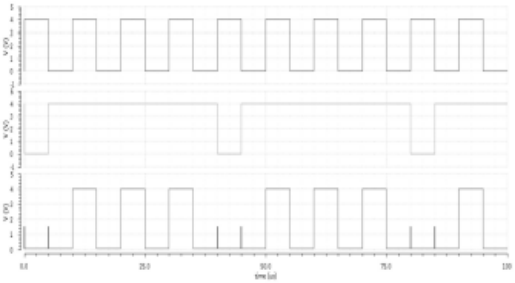


Fig. 9: Schematic Diagram of a Memristor AND gate based on MRL



(a)



(b)

Fig. 10: Simulation waveform of "AND gate". Simulation is done on Virtuoso Platform

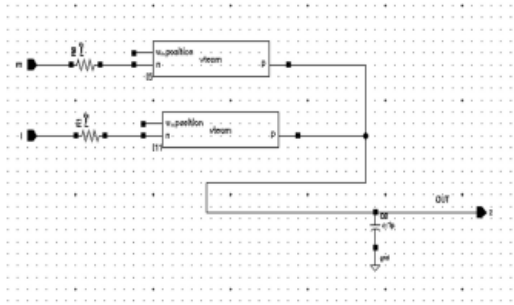


Fig. 11: Schematic Diagram of Memristor" OR" gate based on MRL

In fig. 11, the schematic of memristor OR logic gate is shown. Input to the memristor OR is given to the opposite polarity or as shown in figure to the n terminal of memristor. The NOR logic gate is implemented using a CMOS inverter at the output of the OR gate the schematic is shown in fig. 12. The behavior of Memristor NOR gate with different inputs is shown below in fig. 13 (a), (b) and (c).

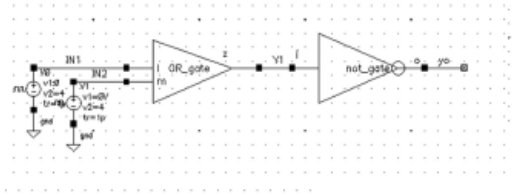
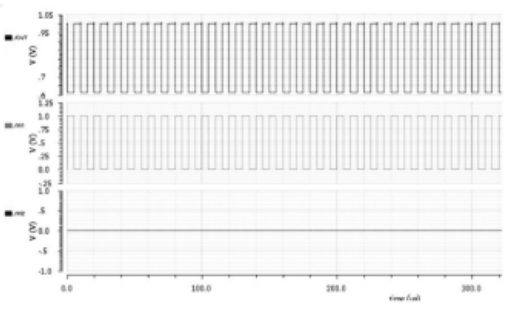
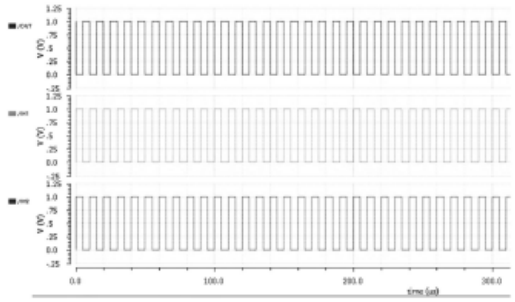


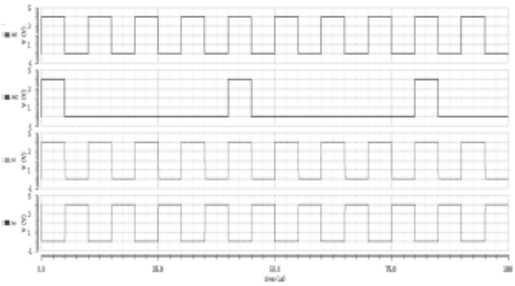
Fig. 12: Schematic Diagram of Memristor" NOR" gate based on MRL, It is a combination or a Memristor OR gate and CMOS inverter.



(a)



(b)



(c)

Fig.13: Simulation Waveform of a NOR gate where (a), (b) and (c) represent the output of a NOR MRL gate for different input values.

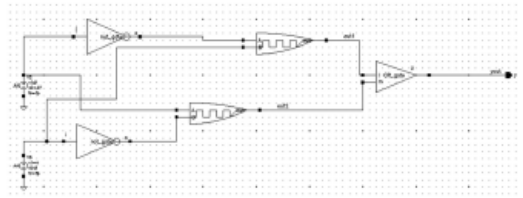


Fig. 14: Schematic diagram of memristor based Hybrid XOR gate

Using MRL logic gate, implementation of memristor XOR gate shown in fig. 15 with different inputs provided. It uses 6 memristor and 4 MOS transistors as compared to 8 MOS transistors used in CMOS XOR gate. Thus, the area of Memristor based XOR gate is significantly reduced.

The NOT gate is implemented using a PMOS and two memristor. PMOS has length of 180nm and width of 1.44 um based on gpdk 180 nm technology library in cadence virtuoso. A linear drift ion model is used for the simulation for memristor based NOT gate [4]. A CMOS based inverter requires 2 MOS transistors whereas Memristor NOT gate requires only 1 MOS transistor and 2 Memristor. The schematic is shown in figure 16 with the dynamic behavior of the memristor NOT gate and CMOS inverter in fig. 17 and fig. 18.

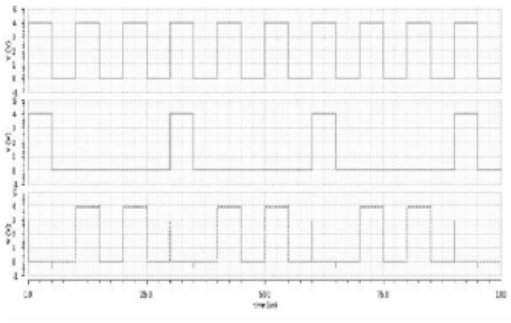


Fig. 15: Simulation Waveform represents the output of a XOR gate for different input values

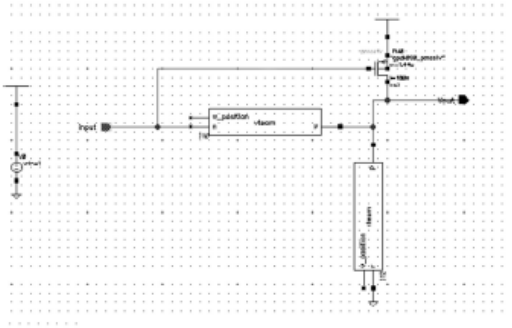


Fig.16: Schematic diagram of Memristor NOT gate which has a PMOS transistor with length=180 nm and width =1.44um

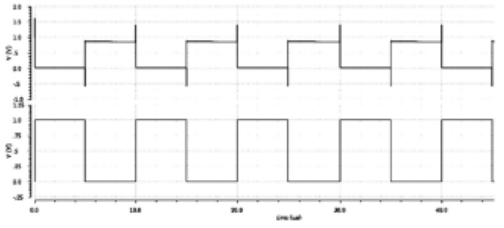


Fig. 17: Output waveform of a Memristor inverter

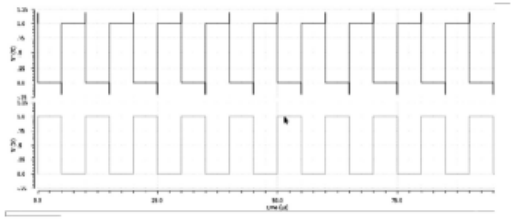


Fig .18: Output waveform of a CMOS inverter

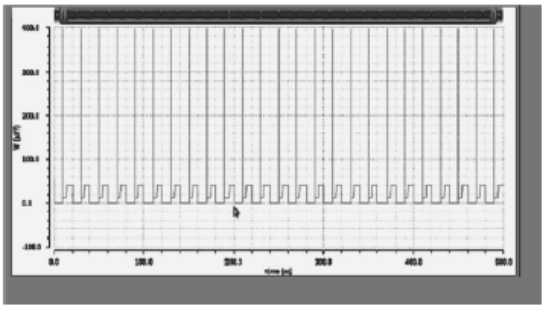


Fig. 19: power consumption of memristor based NOT gate (38 µW)

Integration of memristor with CMOS for designing the complex digital logic circuits helps to overcome the area and also significantly reduce power consumption of the computing system. As seen in fig. 19 and 20 there is a significantly less power consumption in memristor based NOT gate as compare to the CMOS based inverter.

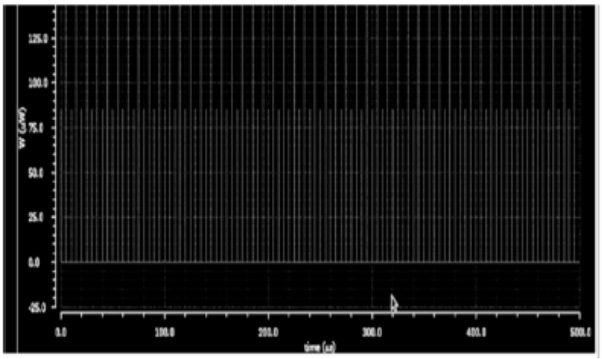


Fig. 20: power consumption of CMOS based NOT gate (78 µW)

VI. CONCLUSION

This paper presents a detailed study of the memristor based digital designs. The properties of the memristor and the model by HP are discussed. The practical model of memristor is simulated in Cadence Virtuoso Platform subjecting it to various input voltages, frequencies of operation, initial resistances of the memristor, and phases of input sinusoidal voltage and noting the results obtained.

As inferred from this paper memristor based systems are better than CMOS based system in terms of trade off such as power, area and delay. They have a fast response time and less power consumption and less area, which make them ideal for digital architecture design. However, more research is required and more analysis need to be done on a large architectural scale using all the models and window functions so that an optimum Model is used for the design.

The future work will focus of the design of digital architectures such as combinational and sequential circuits such as Decoders, Multiplexers, Latches and Flip Flops so that a clear analysis is done.

REFERENCES

[1] L. O. Chua, "Memristor – the Missing Circuit Element," IEEE Transactions on Circuit Theory, Vol. 18, No. 5, pp. 507-519, September 1971.

[2] L. O. Chua and S. M. Kang, "Memristive devices and systems," Proc.IEEE, vol. 64, no. 2, pp. 209–223, Feb. 1976.

[3] S. Kvatinsky, N. Wald, G. Satat, E. G. Friedman, A. Kolodny, and U. C. Weiser, "MRL – Memristor Ratioed Logic for Hybrid CMOS-Memristor Circuits," IEEE Transactions on Nanotechnology

[4] S. Kvatinsky, E. G. Friedman, A. Kolodny, and U. C. Weiser, "TEAM - ThrEshold Adaptive Memristor Model," IEEE Transactions on Circuits and Systems I: Regular Papers, Vol. 60, No. 1, pp. 211-221, January 2013

[5] K. Eshraghian, course notes on "Memristive Circuits and Systems," Technion, June 2011.

[6] How We Found the Missing Memristor The memristor—the functional equivalent of a synapse— could revolutionize circuit design By R. Stanley Williams

[7] Biolek, Z., Biolek, D., and Biolkova, V., "SPICE model of memristor with nonlinear dopant drift'', Radioengineering J., vol. 18, no. 2, June 2009, pp. 210-214.

[8] S. Kvatinsky, M. Ramadan, E. G. Friedman, and A. Kolodny, "VTEAM – A General Model for Voltage Controlled Memristor," Transactions on Circuits and Systems II: Express Briefs, Vol. 62, No. 8, pp. 786-790, August 2015

[9] D. B. Strukov, G. S.Snider, D. R. Stewart, and R. S. Williams, "The Missing Memristor Found," Nature, Vol. 453, pp. 80-83, May 2008.

[10] Behrooz Andoli, Amirali Amirsoleimani, Jafar Shamsi, Karim Mohammadi, Arash Ahmadi "A Novel CMOS-Memristor Based Inverter Circuit Design" (ICEE), 2014 22nd Iranian Conference on Electrical Engineering

[11] Baker Mohammad, Dirar Homouz, and Hazem Elgabra "Robust Hybrid Memristor-CMOS Memory: Modeling and Design" IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Volume: 21, Issue: 11, Nov. 2013

REFERENCES

[1] R. Williams, ―How We Found The Missing Memristor,‖ *Spectrum, IEEE*, vol. 45, no. 12, pp. 28–35, December 2008.

[2] S. P. Mohanty, "Memristor: From Basics to Deployment," *Potentials, IEEE*, vol. 32, pp. 34-39, 2013.

[3] Chua, L.O., ―Memristor- the missing circuit element‖, *IEEE Trans. Circuit Theory*, 1971, vol. CT-18, no. 5, pp. 507-519.

[4] ―HP Memristor FAQ‖, http://www.hpl.hp.com/news/2008/apr-jun/memristor_faq.html

[5] Strukov, D.B., Snider, G.S., Stewart, D.R., Williams, R.S., ―The missing memristor found‖, *Nature, 2008*, 1 May 2008, vol. 453, pp. 80-83.

[6] Biolek, Z., Biolek, D., and Biolkova, V., ―SPICE model of memristor with nonlinear dopant drift‖, *Radioengineering J.*, vol. 18, no. 2, June 2009, pp. 210-214.

[7]S. KVATINSKY, N. WALD, G. SATAT, E. G. FRIEDMAN, A. KOLODNY, AND U. C. WEISER, "MRL – MEMRISTOR RATIOED LOGIC FOR HYBRID CMOS-MEMRISTOR CIRCUITS," IEEE TRANSACTIONS ON NANOTECHNOLOGY

[8]K. Eshraghian, course notes on "Memristive Circuits and Systems," Technion, June 2011.

[9] S. Kvatinsky, M. Ramadan, E. G. Friedman, and A. Kolodny, "VTEAM – A General Model for Voltage Controlled Memristor," Transactions on Circuits and Systems II: Express Briefs, Vol. 62, No. 8, pp. 786-790, August 2015

[10] S. Kvatinsky, E. G. Friedman, A. Kolodny, and U. C. Weiser, "TEAM - ThrEshold Adaptive Memristor Model," IEEE Transactions on Circuits and Systems I: Regular Papers, Vol. 60, No. 1, pp. 211-221, January 2013

[11] L. O. Chua and S. M. Kang, “Memristive devices and systems,” Proc.IEEE, vol. 64, no. 2, pp. 209–223, Feb. 1976

[12] paolo s. crovetti,member,IEEE (2013) *A digital-based analog differential circuit,* : IEEE

[13]Behrooz Andoli, Amirali Amirsoleimani, Jafar Shamsi, Karim Mohammadi, Arash Ahmadi "A Novel CMOS-Memristor Based Inverter Circuit Design" (ICEE), 2014 22nd Iranian Conference on Electrical Engineering

[14] Baker Mohammad, Dirar Homouz, and Hazem Elgabra "Robust Hybrid Memristor-CMOS Memory: Modeling and Design" IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Volume: 21, Issue: 11, Nov. 2013