TCAD ANALYSIS AND SIMULATION OF GATE ELECTRODE WORKFUNCTION ENGINEERED (GEWE) SILICON NANOWIRE MOSFET FOR HIGH PERFORMANCE ANALOG AND RF APPLICATIONS

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By

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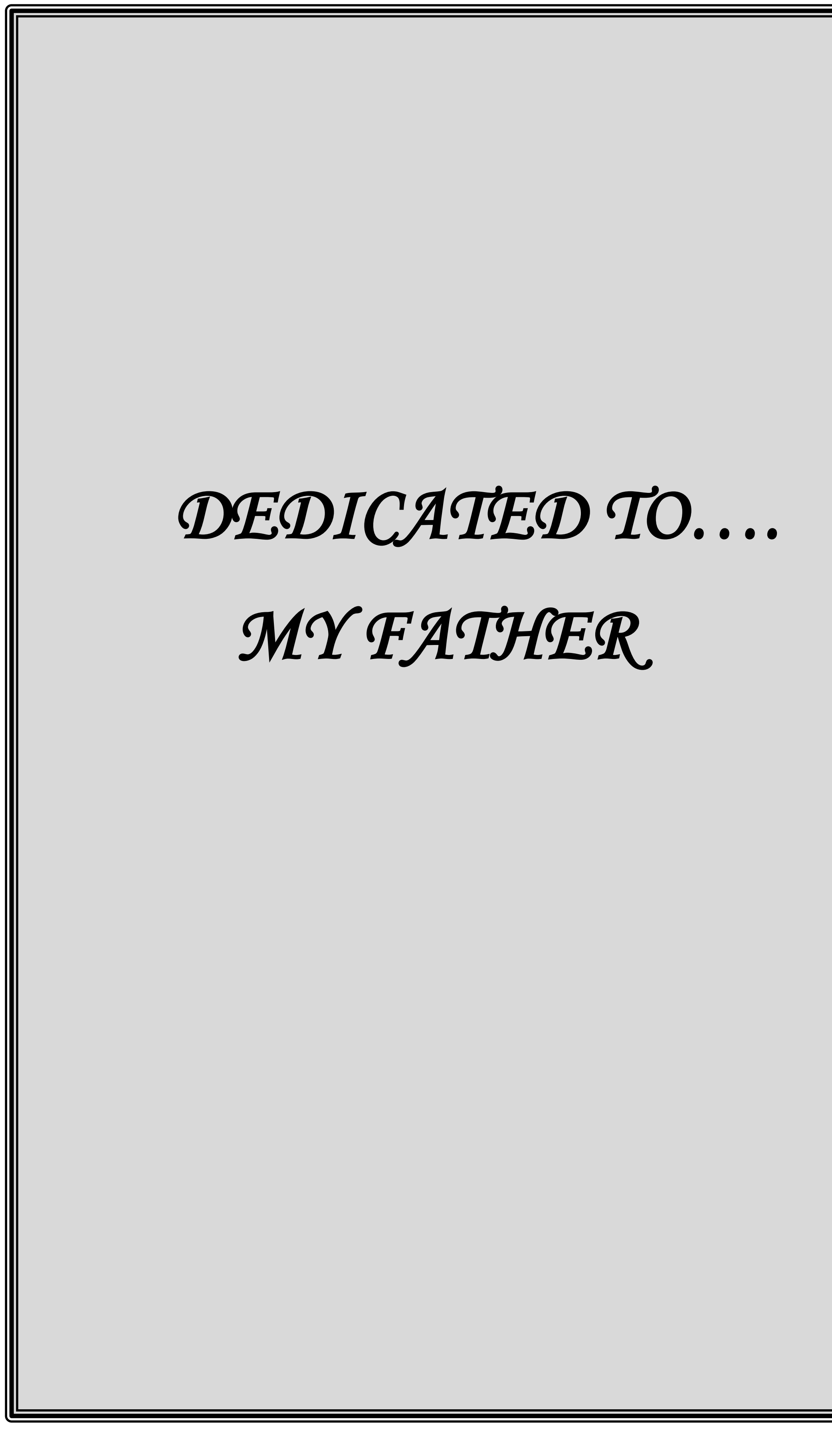
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CERTIFICATE

This is to certify that the thesis entitled "***TCAD Analysis and Simulation of Gate Electrode Workfunction Engineered (GEWE) Silicon Nanowire MOSFET for High Performance Analog and RF Applications***" submitted by **Miss. NEHA GUPTA** with registration number **(2K12/Ph.D. AP/02)** to Delhi Technological University, Delhi for the award of degree of Doctor of Philosophy. The work is based on original research work carried out by me under the supervision of **Dr. Rishu Chaujar**. It is further certified that the work embedded in this thesis has neither partially nor fully submitted to any other university or institution for the award of any degree or diploma.

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ABSTRACT

TCAD Analysis and Simulation of Gate Electrode Workfunction Engineered (GEWE) Silicon Nanowire MOSFET for High Performance Analog and RF Applications

Scaling MOSFETs beyond sub-nm gate lengths is extremely challenging using planar device architecture due to the stringent criteria required for the transistor switching. The development of three dimensional devices like Multi-gate MOSFETs, ultra-thin SOI MOSFETs, FinFETs, Silicon Nanowires, Nanotubes etc. become important for the further advancement in the integrated chip industry. The top-down fabricated, gate-all-around architecture with a Si nanowire channel is a promising candidate among these for future technology generations. The gate-all-around geometry enhances the electrostatic control and hence gate length scalability and also suppress short channel effects effectively. Silicon nanowire MOSFET in gate all around configuration has proved to be good candidate due to its ability to suppress short channel effects. In nanoscale MOSFET, to improve speed and performance of a device, several engineering schemes have been proposed but the main problem associated is gate transport efficiency. As dual gate-MOSFET and Split Gate-MOSFET structures cannot improve both carrier transport efficiency and short-channel effect. Gate Electrode Workfunction Engineering structure opens a new way to improve device performance. To eliminate polysilicon depletion width effects and polysilicon dopant penetration, polysilicon gates need to be replaced by metal gates. In 1997, Wei

Long and Ken K. Chin proposed a novel structure the Dual Material Gate MOSFET, which suppress short channel effects and enhance carrier velocity. In the DMG-MOSFET, the gate consists of two contacting materials with different work functions. The metal with higher work function is close to source and metal with lower work function is close to drain, and hence threshold voltage $V_{T1}>V_{T2}$ which improve the carrier transport efficiency. It is observed the step potential profile in the channel region because of two metal gates of different work function, which ensures reduction in short channel effects without sacrificing other device characteristics, unlike in dual gate or other gate structures.

In this dissertation, gate metal workfunction engineering scheme is amalgamated onto SiNW MOSFET and its Hot-Carrier fidelity and DIBL are studied to scrutinize its efficacy in high power CMOS applications. It is found that with k = 21(HfO_2) as gate oxide, device performance in terms of hot-carrier reliability further enhanced due to increased capacitance and thus offer its effectiveness in sub-nm range analog applications. Extensive device simulation results shows that GEWE-SiNW MOSFET exhibit improved RF performance in terms of high cut-off and maximum oscillator frequency and its performance further intensified with tuning of device parameters such as gate length, radius of nanowire, oxide thickness and workfunction of gate metals. Thus, providing detailed knowledge about the device's RF performance at such aggressively scaled dimensions. For comprehensive RF analysis of GEWE-SiNW MOSFET and its effectiveness at HF, the small signal behaviour in terms of scattering parameters is also discussed. This would be useful for evaluating the microwave performance of the device in terms of forward and reverse gains. In addition, noise metrics have also been evaluated which affects the device performance at HF. The RF investigation carried over is circumscribed to intrinsic components of MOSFET only. However,

at GHz frequency range, the importance of extrinsic component (the part outside the channel region) dominates to that of its intrinsic counterpart. Therefore, there is a need for an RF model which should consider the behaviour of both the intrinsic and the extrinsic components of a device for achieving accurate and predictive results in the simulation of designed circuit. Thus, the extrinsic and intrinsic parameters of GEWE-SiNW MOSFET and numerical modelling of small signal parameters such as Z and Y parameters are also studied in this work.

Furthermore, as oxide thickness scales down to 1.5 nm or below, the leakage current increases up to 1 A/cm^2 at 1 V due to direct tunneling of carriers which, consequently increases the static power and hence affect the circuit operation. So, high-k films are proved to be the most promising solution. Though, these films result in high fringing fields from gate to source/drain regions and thus degrading the device performance. This constraint can be overcome by using gate stack architecture consisting of SiO_2 layer as a passivation between high-k films and bulk by keeping the effective oxide thickness (EOT) constant, high-k dielectrics permit the increase in physical oxide thickness to prevent gate tunneling and thus improves the carrier efficiency. Thus, stack gate (SG) is amalgamated onto GEWE-SiNW MOSFET to examine its performance in terms of analog and linearity FOMs. It is observed that SiNW MOSFET modeled with HfO_2 as a gate stack over SiO_2 interfacial layer, and gate metal workfunction difference (ΔW) of 4.4 eV can be considered as a promising potential for low power switching component in ICs and Linear RF amplifiers. Moreover, a reliability issue of Stacked Gate (SG)-Gate Electrode Workfunction Engineered (GEWE)-Silicon Nanowire (SiNW) MOSFET is examined over a wide range of ambient temperatures (200–600 K). It is observed that at low temperature SG-

GEWE-SiNW shows improved Analog/RF performance in terms of I_{on}/I_{off}, Subthreshold Swing (SS), device efficiency, f_T, noise conductance and noise figure and also unveil highly stable linearity performance owing to reduced distortions. The results so obtained can be serving as a worthy design tool for circuits operating at wide range of temperatures.

Immunity against SCEs, high current driving capability, optimum high frequency performance and suitability at low temperature makes GEWE-SiNW MOSFET a promising device for low power, high performance CMOS applications.

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IN INTERNATIONAL REFEREED JOURNALS (7)

1. **Neha Gupta**, Ajay Kumar and Rishu Chaujar, "Investigation of Frequency Dependent parameter of GEWE-SiNW MOSFET for Microwave and RF Applications", International Journal of Advanced Technology in Engineering and Science, Vol. 2, Sept. 2014, ISSN (Online): 2348 – 7550.
2. **Neha Gupta**, Ajay Kumar and Rishu Chaujar," Oxide Bound Impact on Hot-Carrier Degradation for Gate Electrode Workfunction Engineered (GEWE) Silicon Nanowire MOSFET", in Microsystem Technologies, Springer, Vol. 22(11), pp. 2655-26642015. Doi: 10.1007/s00542-015-2557-9.
3. **Neha Gupta**, Ajay Kumar and Rishu Chaujar, "Impact of Device Parameter Variation on RF performance of Gate Electrode Workfunction Engineered (GEWE)-Silicon Nanowire (SiNW) MOSFET", Journal of Computation Electronics, Springer, Vol. 14(3), pp. 798-810, 2015. Doi: 10.1007/s10825-015-0715-z
4. **Neha Gupta** and Rishu Chaujar, "Influence of Gate Metal Engineering on Small Signal and Noise Behaviour of Silicon Nanowire MOSFET for Low Noise Amplifiers" Applied Physics A, Springer, Vol.122(8), pp. 717 (1-9), 2016. Doi: 10.1007/s00339-016-0239-9
5. **Neha Gupta** and Rishu Chaujar, "Optimization of High-k and Gate Metal Workfunction for Improved Analog and Intermodulation Performance of Gate Stack (GS)-GEWE-SiNW MOSFET", Superlattices and Microstructures, Elsevier, Vol. 97, pp. 630-641, 2016. Doi: 10.1016/j.spmi.2016.07.021
6. **Neha Gupta** and Rishu Chaujar, "Effect of Temperature on Analog/RF Performance of Stacked Gate GEWE-Silicon Nanowire MOSFET", Microelectronics Reliability, Elsevier, Vol. 64, pp. 235-241, September 2016. Doi: 10.1016/j.microrel.2016.07.095.
7. **Neha Gupta** and Rishu Chaujar, "Quantum Simulation Based Extraction of Frequency Dependent Intrinsic and Extrinsic Parameters for GEWE-SiNW

MOSFET", Journal of Computational Electronics, Vol. 16 (1), pp. 61-73, Springer, 2016.

In International Conferences (9)

1. **Neha Gupta** and Rishu Chaujar, "Implications of transport models on the analog performance of Gate Electrode Workfunction Engineered (GEWE) Silicon Nanowire MOSFET", Devices, Circuits and Systems (ICDCS), 2014 2nd IEEE International Conference, pp.1-5, 6-8 March 2014. Doi: 10.1109/ICDCSyst.2014.6926154
2. **Neha Gupta**, Ajay Kumar and Rishu Chaujar, "Simulation analysis of Gate Electrode Workfunction Engineered (GEWE) Silicon Nanowire MOSFET for hot carrier reliability" IEEE 1st International Conference on Microelectronics, Circuits and Systems", Kolkata, pp. 150-153, 11-13th July, 2014.
3. **Neha Gupta**, Ajay Kumar and Rishu Chaujar, "TCAD Analysis of Noise and Small signal behaviour of Gate Electrode Workfunction Engineering (GEWE) Silicon Nanowire (SiNW) MOSFET", 3rd International Conference Nanocon-014, Pune, 14th-15th October, 2014.
4. **Neha Gupta**, Ajay Kumar and Rishu Chaujar, "Impact of Channel Doping and Gate Length on Small Signal Behaviour of Gate Electrode Workfunction Engineered Silicon Nanowire MOSFET at THz Frequency", Fifth International Symposium on Electronic System Design, Mangalore, Karnataka, 15-17th December, 2014. Doi 10.1109/ISED.2014.46
5. **Neha Gupta,** Ajay Kumar and Rishu Chaujar, "TCAD Analysis of Frequency Dependent Intrinsic and Extrinsic parameters of GEWE-SiNW MOSFET", Tech-Connect World Innovation Conference & Expo, 14-17th June 2015, Washington DC, USA.
6. **Neha Gupta**, Ajay Kumar and Rishu Chaujar, "TCAD AC Analysis of Gate Electrode Workfunction Engineered Silicon Nanowire MOSFET for High Frequency Applications", Tech-Connect World Innovation Conference & Expo, 14-17th June 2015, Washington DC, USA.

7. **Neha Gupta**, Ajay Kumar and Rishu Chaujar, "Effect of Dielectric Engineering on Analog and Linearity performance of Gate Electrode Workfunction Engineered (GEWE) Silicon Nanowire MOSFET", 15th IEEE International Conference on Nanotechnology, pp. 928-931, 27 - 30 July 2015, ROME, ITALY. Doi: 978-1-4673-8156-7/15/$31

8. **Neha Gupta**, Ajay Kumar and Rishu Chaujar, "Gate Electrode Workfunction Engineered (GEWE) Silicon Nanowire (SiNW) MOSFET: A Solution for LNA at RF Frequency", 2nd International Conference on Microelectronics, Circuits and Systems MICRO-2015, Kolkata, 11-12th July, 2015.

9. **Neha Gupta**, Ajay Kumar and Rishu Chaujar, "Quantum Mechanical C-V Analysis of Gate Electrode Workfunction Engineered (GEWE) Silicon Nanowire MOSFET for HF Applications", 18th International Workshop on Physics of Semiconductor Devices (IWPSD-2015), Bangalore, 7-10 Dec 2015.

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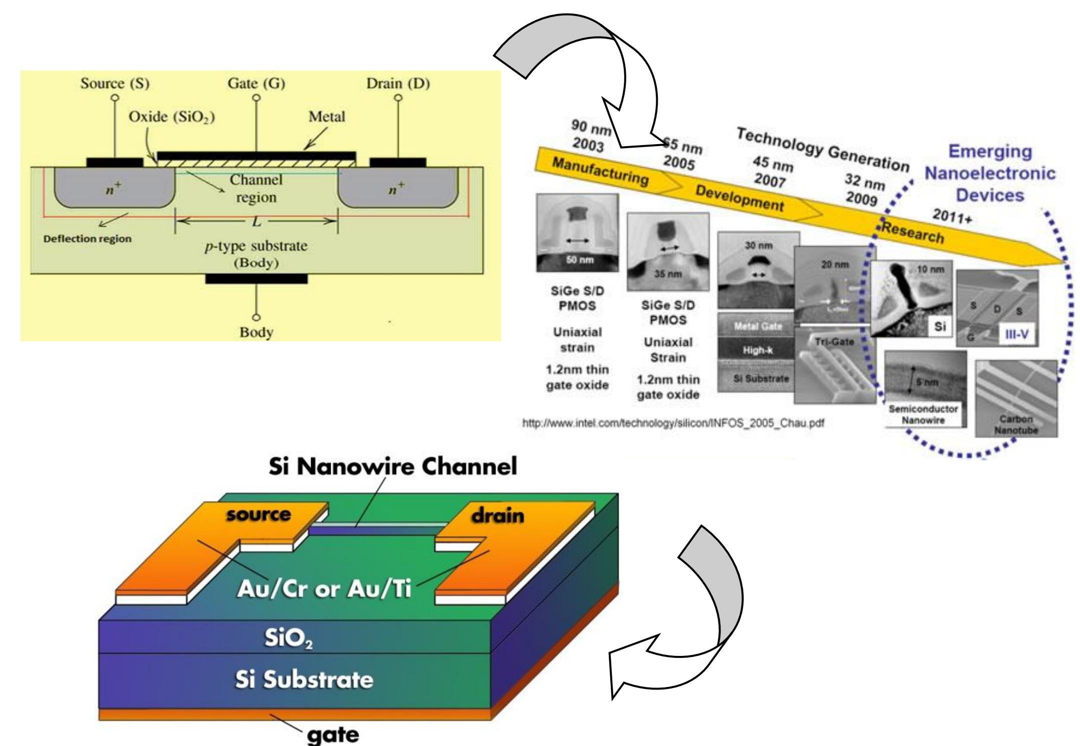
CHAPTER-1

INTRODUCTION

- *This chapter gives a brief overview of Evolving of Nanoscale Metal Oxide Semiconductor Field Effect Transistor (MOSFET).*
- *Various adverse effects arise due to the scaling of dimensions and to overcome these limitations, different engineering schemes have been discussed in this chapter.*
- *Numerous device structures and innovative materials are reviewed and found silicon nanowire MOSFET as a suitable candidate for improved device performance.*
- *Advantages and Disadvantages of Silicon Nanowire MOSFET along with its electrical properties are reviewed in this chapter*
- *In addition, fabrication feasibility of Gate All Around SiNW MOSFET and gate metal workfunction engineering scheme for CMOS processes is presented.*
- *In the end, the objectives and brief outline of the thesis are presented*



1.1 OVERVIEW: GROWING OF NANOSCALE MOSFET

One of the essential developments in modern engineering history is monolithic integrated circuits (IC) technology. From last few decades, incredible improvement in IC technology has miraculously changed our lives and the whole world by providing a boost to Information technology (IT). The main reason behind this is downscaling of CMOS dimensions (the key component of IC), and increasing the package density (by increasing the total number of transistors in one chip). According to Moore's law (Bondyopadhyay, 1998), the number of transistors on one IC chip would duple every year which finally paraphrased as a doubling in transistor count every two years in 1975 (Moore, 2004) and thus efficaciously predicted the device scaling as evidently shown in Fig. 1.01.

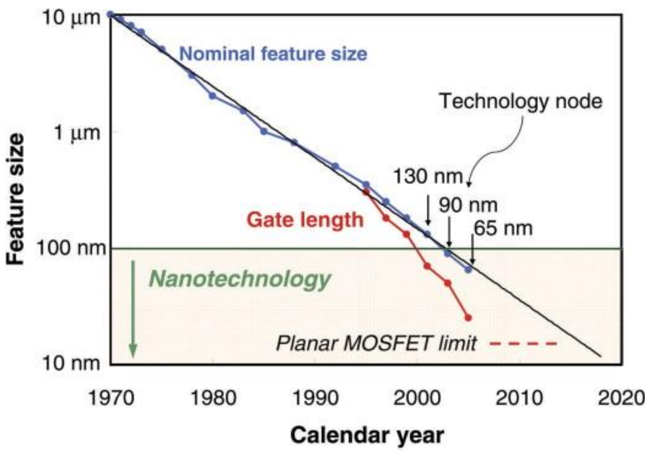


Figure 1.01: Moore's Law predicting the downscaling of device features (Thompson & Parthasarathy, 2006)

For upholding consecutive improvements in IC technology, continuous device scaling is essential. However, as the channel length enters into nm-regime, the so-called short channel effects (SCEs) arises such as threshold voltage (V_{th}) roll-off, drain induced barrier lowering (DIBL), hot-carrier effects (HCEs) and Punchthrough etc, which

hinders the device performance and also restricts the scaling ability of conventional silicon MOSFET (Abuelma'atti, 2013; Khanna, 2016; Veeraraghavan & Fossum, 1989). To overcome such effects, various device engineering schemes have been proposed to alleviate the issue of SCEs which will be discussed in next section. In addition, lower carrier (electron) mobility of silicon in comparison to other semiconductor results in degradation of MOSFET's I-V characteristics which eventually hampers the device analog and RF performance. Therefore, novel device structure and materials such as Silicon Nanowire (SiNW) MOSFET (Shirak et al, 2012; Singh et al, 2006a; Wang et al, 2003), carbon nanotube FETs (Guo et al, 2002), molecular transistors (Reed, 1999), novel materials (e.g., strained silicon, pure germanium) to enhance the mobility and thus device performance (Lee et al, 2005; Leitz et al, 2001), are being widely investigated. Among all these promising CMOS candidates, SiNW MOSFET has its inimitable benefit, Firstly, the SiNW is based on silicon, which is abundant in nature and also IC industry has been working on it over last few decades. Also, from device and circuit developers, they have procured remarkable attention because of its potential for high performance and building highly dense electronic circuits and therefore emerge as a possible solution for future silicon based nano-devices (Bangsaruntip et al, 2009; Yang et al, 2004).

1.2 Literature Review

1.2.1 Scaling of MOSFET

The main aim of the VLSI/ULSI electronics is to lower down the cost per logic function and simultaneously upsurge the switching speed of logic gates and this aim has been achieved by scaling down the device dimensions and thus resulted in new

generations ICs (Nair, 2002). MOS transistors has been systematically scaled down in dimensions in order to achieve higher circuit density (more circuit functions in a given silicon area), higher switching speed and lower power dissipation etc. (Arora, 1993). Scaling was first proposed by Dennard et al. with the idea of reducing the device dimensions without affecting its voltage-current behavior of large devices (Dennard et al, 2007; Veeraraghavan & Fossum, 1989). Rules of scaling given by him are known as constant field scaling. In constant field scaling, all the dimensions and voltages are reduced by a scaling factor α(>1), that result constant electric field inside the device as those of an original device (Borkar, 1999; Davari et al, 1995) as shown in Fig. 1.02.

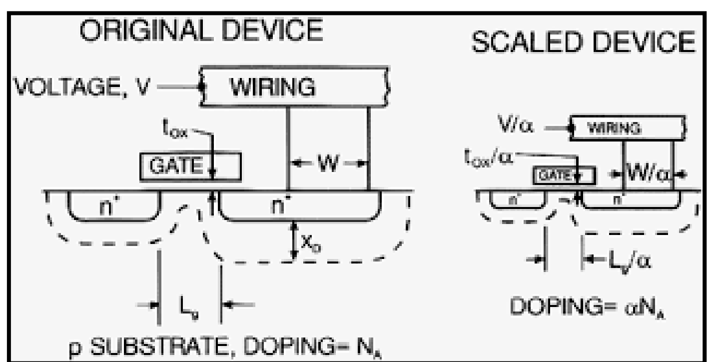


Figure 1.02: Principles of constant-electric-field scaling for MOSFETs and integrated circuits. (Frank et al, 2001)

When developed in 1960, the channel length of the MOSFET was around 10μm. Today most of the integrated circuits utilize CMOS technology with channel length around sub-nm range. Following are the advantages of scaling (Abuelma' atti, 2013):

1. ***Low Cost***: Due to small size of transistor, more and more transistors can be integrated onto small wafer and thus leads to cheaper circuits.
2. ***High Speed***: Smaller transistors and shorter interconnects lead to reduced capacitances and hence higher IC speed.

3. It also lead to reduced power supply voltages and little power consumption instead of rise in switching frequency.

However, downscaling has its own problem at very short gate length (sub-nm range) (Hu, 2010). These are:

- Static and dynamic power consumption.
- Overheating and possible evaporation become major concerns.
- Increased electric field within the oxide and increased leakage gate-current.

1.2.2 Short Channel Effects (SCEs)

To apprehend high circuit density and maximum operational frequency for future ICs, the channel length and width of device must be reduced. But, diminishing the channel length leads to short channel effects, whereas decreasing the width causes a reduction in current drive. MOSFET scaling thus results in increased SCEs, the most pronounced of which is threshold voltage (V_{th}) roll-off, DIBL, HCEs.

A. Threshold Voltage (V_{th}) Roll-off

The key parameter that characterizes SCE is the degradation of V_{th} with decrease in channel length. The shrinkage of threshold voltage with lessening in channel length is a well-known SCE called the "Threshold voltage roll-off". As the channel of the device is reduced to sub-nm range, then the charge sharing in the channel is influenced by the field originating from the source/drain. Consequently, the potential barrier at the source end is pull down, which causes increased flow of carriers, and thus results in higher sub-threshold drain current. Due to this, standby leakage power dissipation increases which is given by $V \times I_{off}$ (V is the applied voltage and I_{off} is the leakage current). Methodically, threshold voltage roll-off is the difference between the

threshold voltage of a short channel MOSFET and that of a long channel MOSFET (Arora, 1993; Taur & Ning, 2013).

B. Drain Induced Barrier Lowering (DIBL)

Kit Man Cham et.al reported that DIBL result an increase in the residual leakage current in short channel devices as the drain to source voltage is increased (Troutman, 1979).

In scaled MOSFETs, the potential barrier in inversion regime is controlled by both the bias voltage i.e., gate-to-source voltage (V_{gs}) and the drain-to-source voltage (V_{ds}). If V_{ds} is increased, the potential barrier in the channel decreases, which results increase in drain current. This effect is known as drain-induced barrier lowering (DIBL). The lowering of the barrier eventually allows more carriers to flow between the source and the drain, even if the V_{gs} is lesser than the threshold voltage as evidently reflected in Fig. 1.03(a). The drain current that flows under this situation ($V_{gs}<V_{th}$) is called the sub-threshold or leakage current which is not desirable (Chamberlain & Ramanan, 1986).

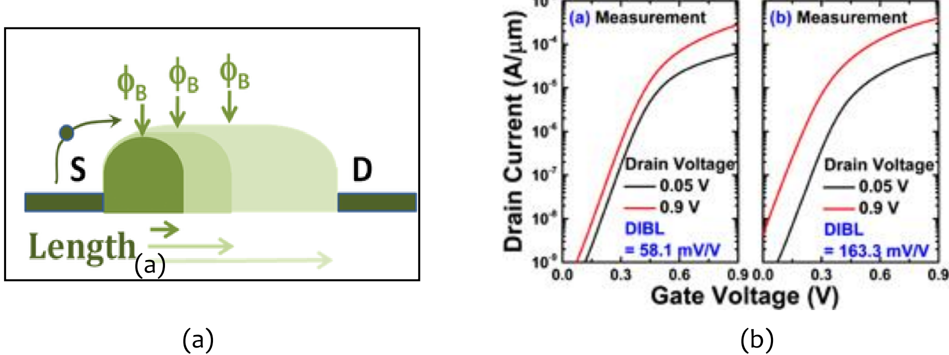


Figure 1.03: Drain Induced Barrier Lowering (Jung et al, 2014)

Mathematically, DIBL effect can be calculated by the lateral shift of the transfer curve (I_{ds}-V_{gs}) in the weak inversion regime divided by the V_{ds} difference of the two curves and is given in units (mV/V) as reflected in Fig. 1.03(b).

C. Hot-carrier effects (HCEs)

During scaling down the device dimensions, device voltages are not scale down properly and thus lead to high electric fields. Due to which, several hot-carrier effects appears in short channel MOSFET as shown in Fig. 1.04. High electric field at the drain junctions can lead to avalanche injection from channel region to drain depletion region and impact ionization which results in dislocating of e-h pairs. These holes contribute to substrate current (or leakage current) and some of them move towards source end, lower the potential barrier and results in electron injection from source to channel and thus loses the gate control from the drain current (Hu, 1989). In addition, some of the high-field electrons tunnel through the substrate-gate oxide barrier and get trapped into the oxide or at the interface. These trapped electrons degrade the sub-threshold swing, modify the threshold voltage and transfer characteristics of the device (Takeda et al, 1995). Thus, they need to be controlled for sub-nm range devices.

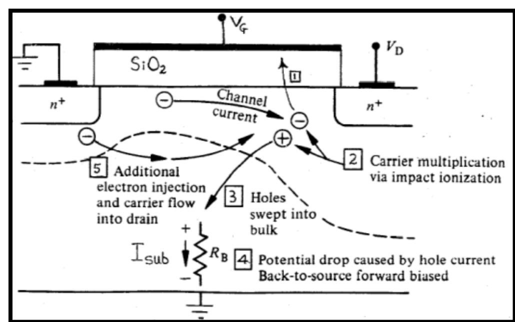


Figure 1.04: Cross-Sectional View of n-channel MOSFET showing Injection of Hot-Carriers due to shortening of channel length (Wolf, 1995)

1.2.3 Ways to Overcome SCEs

Since, short channel effects obstruct the device operation and degrade device characteristics, therefore these effects should be removed, so that physical short

channel device can preserve the electrical long channel behaviour. Numerous device engineering schemes have been reported in literature from last few years to get over these problems which are discussed below.

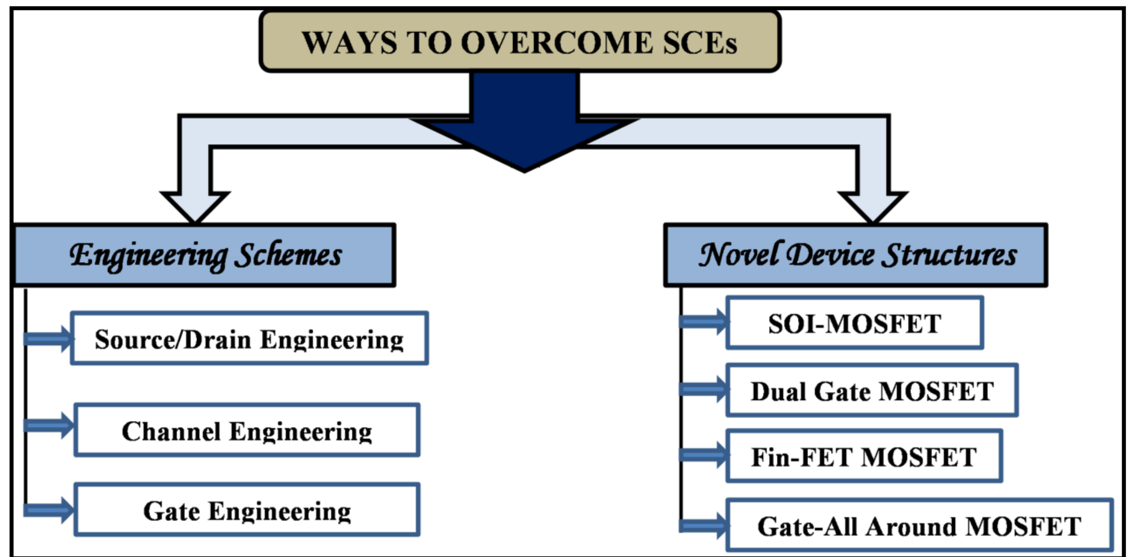


Figure 1.05: Different schemes to alleviate SCEs in nano-scale MOSFET

A. Engineering Schemes

i. Source/Drain Engineering

By decreasing the doping concentration in the source/drain regions, the junction fields become smaller and thus reduce HCEs. Conversely, lightly doped source/drain regions are incompatible with nm-range devices because of contact resistances and other similar problems. Fig. 1.06 depicts the compromise design of MOSFET, called *Lightly Doped Drain* (*LDD*) (Rubel et al, 2015), using two doping levels with heavy doping over most of the source and drain areas with light doping in a region adjacent to the channel. The LDD structure decreases the field between drain and channel regions, thereby reducing injection into the oxide, impact ionization and other hot electron effects (Bampi & Plummer, 1986; Kaga & Sakai, 1988).

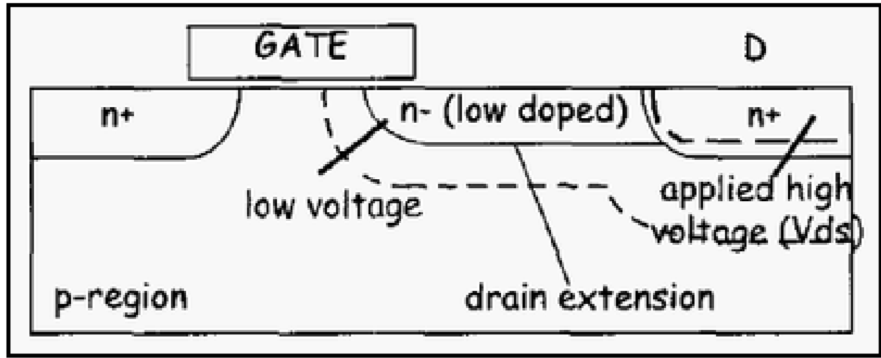


Figure 1.06: Cross-Section of n-type MOSFET considering low doped extension from drain side. (Hower & Pendharkar, 2005)

ii. Channel engineering

When the channel length of the device is below 100 nm, it shows significant threshold V_{th} roll off and DIBL effects. These are the most daunting road block for future MOSFET design. It was found that V_{th} roll-off can be reduced or even reversed by locally raising the channel doping next to the drain or drain/source junctions (Mohankumar et al, 2010). In the past few years, the locally high doping concentration in the channel near source/drain junctions has been implemented via lateral channel engineering, e.g., halo (Ravindhran et al, 1995) or pocket implants (Nandakumar et al, 1999) as shown in Fig. 1.07. The two terms are used interchangeably here although a halo may indicate a pocket that is deeper than the drain. The implant can be either symmetric or asymmetric with respect to source and drain. The pocket, implant technology is very promising in the effort to *tailor* the short-channel performance of deep-submicron MOSFET's, although careful tradeoffs need to be made between and other device electrical parameters.

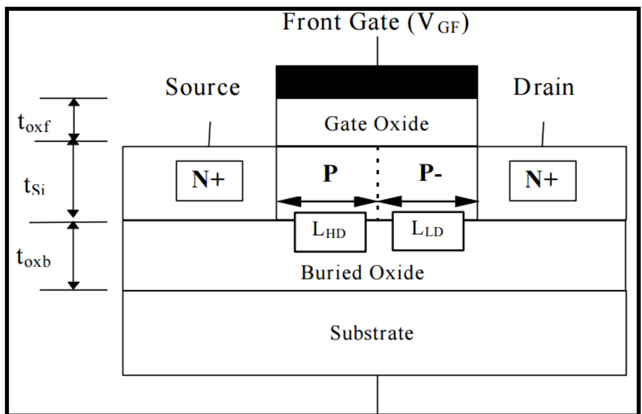


Figure 1.07: ***Schematic View of n-channel SOI-MOSFET showing graded channel doping (Galeti et al, 2006)***

iii. Gate Engineering Scheme

➢ ***Gate dielectric material engineering (high-k gate dielectric materials)***

As the dimension of the device decreases, the gate oxide thickness simultaneous decreases, causing an increase in tunneling current. Hence, gate-tunneling current is a concern in sub-nanometer regime. To surmount the limitation of gate oxide thickness, high-k materials in oxide could be helpful. However, the difficulties of adopting high-k dielectric in VLSI include chemical reaction between them and the silicon substrate and the gate (Frank et al, 2009). In addition, they also lack thermal stability. Moreover, the use of high- k dielectric gate materials may also result in dielectric thickness comparable to the device gate length and arises an increased fringing fields from gate to source/drain (Inani et al, 1999; Mohapatra et al, 2001). Thereby, affecting the sub-threshold characteristics and DIBL. Thus, high-k gate dielectric stacked with SiO_2 (gate stack engineering) is a possible candidate to replace thinner silicon-dioxide layer in a nanoscale MOSFETs (Lee et al, 2006) as depicted in Fig. 1.08.

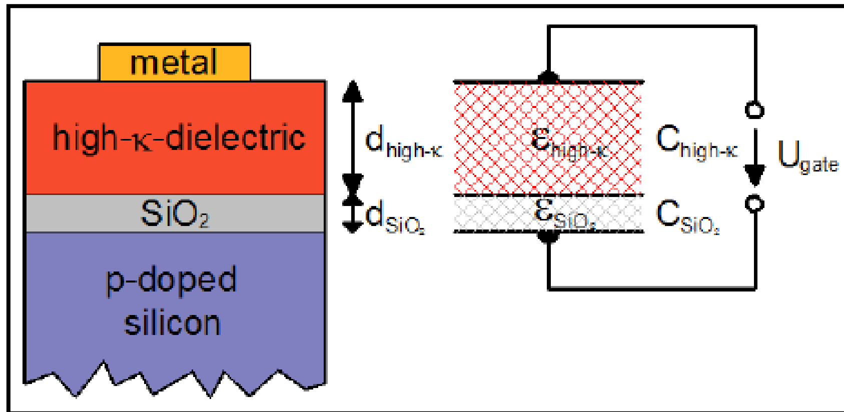


Figure 1.08: Schematic structure of a gate stack with a high-k dielectric layer. A series capacitance has to be taken into account to evaluate the dielectric constant of the high-k material. (Moers et al, 2010)

An extremely thin interfacial oxide can be used to passivate the interface and minimize interface states when high-*K* gate materials are deposited. The concept of equivalent oxide thickness (EOT) is to provide a suitable alternative gate dielectric or gate stack dielectric structure having similar characteristics, when using SiO_2 gate dielectric, but having greater physical thickness to improve gate control over the channel and limit the tunneling transport in sub-nm MOSFETs.

- ***Dual Material Gate (DMG) Engineering***

To improve speed and performance of a device, several engineering schemes have been proposed such as use of higher quality material, gate reduction etc. but the main problem associated is gate transport efficiency. As reported earlier, the Dual Gate-MOSFET and Split Gate MOSFET structures cannot improve both carrier transport efficiency and short-channel effects. Moreover, to eliminate polysilicon depletion width effects and polysilicon dopant penetration, polysilicon gates need to be replaced by metal gates. In 1997, Wei Long and Ken K. Chin Z proposed a novel structure the

Dual Material Gate MOSFET as shown in Fig. 1.09, which suppress the SCEs and enhance carrier velocity (Long & Chin, 1997; Long et al, 1999). In the DMG-MOSFET, the gate consists of two contacting materials with different work functions. The metal with higher work function is close to source end and metal with lower work function is close to drain end, and hence threshold voltage $V_{T1}>V_{T2}$.

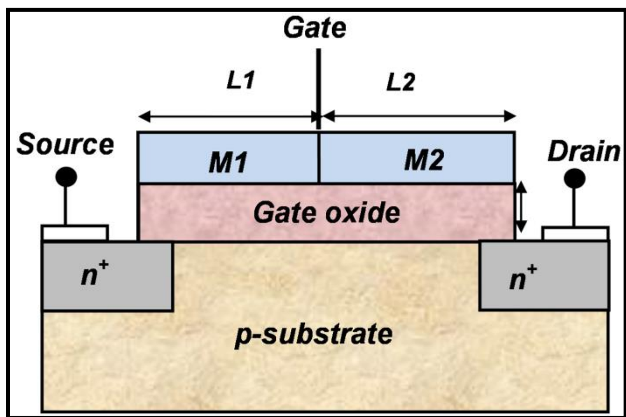


Figure 1.09: Schematic Structure of Dual Material Gate MOSFET (Modified from (Long et al, 1997))

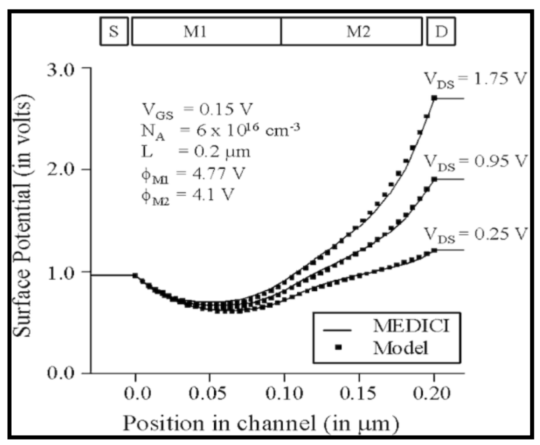


Figure 1.10: Surface channel potential profiles of a fully depleted DMG SOI MOSFET. (Kumar & Chaudhry, 2004)

The step function profile of the surface potential owing to two dissimilar metal gates as shown in Figure 1.10 ensures screening of the channel region under the material on the source side (M1) from drain-potential variations. After saturation, M2 absorbs any

additional V_{ds} and, hence, the region under M1 is screened from drain-potential variations and hence reduces channel length modulation and drain conductance. Moreover, workfunction difference creates an electric field peak at the interface of two metal gates in the channel, which results in increase in electric field near the source end as compared to drain region as clear from Fig. 1.10. Hence, the average electron velocity becomes higher at source region and results improvement in the carrier transport efficiency (Long et al, 1999) and thereby reduces the hot electron effect. Since, two gates are laterally joined into one single gate; it overcomes the problem of fringing capacitance in DMG-MOSFET. Also, in DMG-MOSFET, lower work function metal gate reduces the electric field near the drain side, which further suppresses the hot carrier effects (Kumar et al, 2006; Polishchuk et al, 2001).

B. Novel Device Concepts

Researchers around the world are trying to develop new devices in order to continue increase the speed of operation and the packaging density of integrated circuits. Eventually the classical MOSFET structure will disappear and new devices with new structures using new materials will be introduced. In addition to the ongoing scaling process, novel design concepts have arisen to enable a further increase in the integration density. These concepts span from strained-silicon MOS devices where the silicon channel is replaced by strained silicon to improve the mobility, to depleted-substrate devices such as single-gate or double-gate silicon on insulator (SOI) devices, FinFETs, vertical transistors, and even carbon nanotubes (CNTs) which represent a completely new device structure.

i. Silicon on Insulator (SOI)

Young (Young, 1989) analyzed and concluded that SCEs are well suppressed in thin-film SOI MOSFET's when compared to bulk MOSFETs. This may be due to the difference in source/drain junction depths between the two kinds of devices. One can obtain significant reduction of SCEs by sandwiching a fully depleted SOI device between two gate electrodes connected together. Fig. 1.11 shows SOI technology which employs a thin layer of silicon isolated from a silicon substrate by a relatively thick layer of silicon oxide (Choi & Fossum, 1991; Choi et al, 1999). The SOI technology dielectrically isolates components and in conjunction with the lateral isolation, reduces various parasitic circuit capacitances, and thus, eliminates the possibility of latch-up failures.

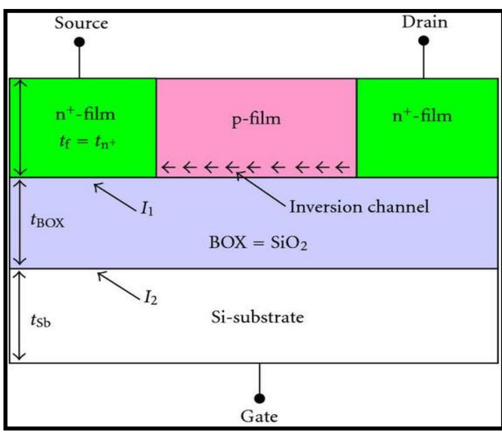


Figure 1.11: Schematic view of n-channel SOI MOSFET (Ravariu & Babarada, 2011)

SOI technology offers superior devices with excellent radiation hardness and high device density. Without the reverse-biased junctions used for isolation as in bulk CMOS, leakage current is small. In addition, for scaling devices into deep-submicron regime, SOI devices are more suitable with their steeper sub threshold slope which facilitates scaling of the threshold voltage for low-voltage low-power applications.

They are attractive devices for low-power high-speed VLSI applications because of their small parasitic capacitances.

ii. Dual Gate MOSFET

In 1987, F. Balestra et.al (Balestra et al, 1987) proposed a new structure the “Double-Gate” which appears to be one of the most promising due to the shield-effect played by double gate, which strongly reduces drain-induced barrier lowering and minimizes threshold sensitivity to channel length. In planar double-gate transistors the channel is sandwiched between two independently fabricated gate/gate oxide stacks. The main idea of a Double Gate MOSFET is to control the Si channel efficiently by choosing the Si channel width to be very small and by applying a gate contact to both sides of the channel. This concept helps to suppress short channel effects and leads to higher currents as compared with a MOSFET having only one gate. The main problem with this structure however, is fabrication, since it requires alignment of the two gates.

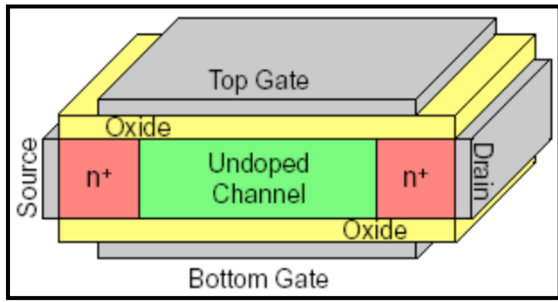


Figure 1.12: Schematic view of n-channel Double gate MOSFET (Brown et al, 2002)

iii. Fin-FET

In contrast to planar MOSFETs, the channel between source and drain is built as a three dimensional bar on top of the silicon substrate, called fin.

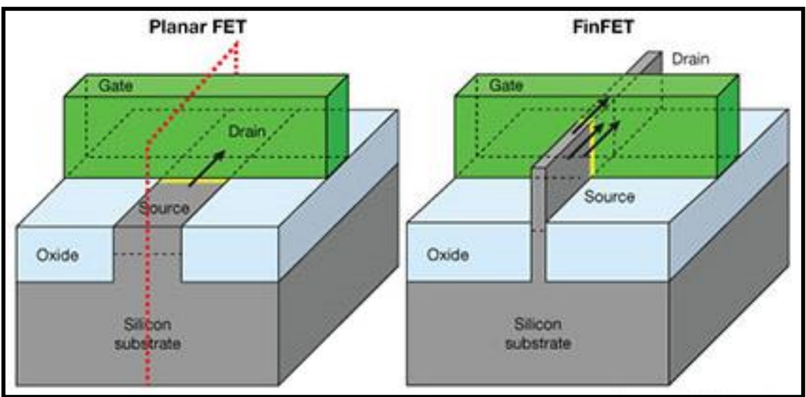


Figure 1.13: Schematic view of both planar MOSFET and FinFETs (Bohr & Mistry, 2011)

The gate electrode is then wrapped around the channel, so that there can be formed several gate electrodes on each side which leads to reduced leakage effects and an enhanced drive current (Choi et al, 2001; Yang et al, 2002).

Fin-FET offers several advantages such as:

- Low wafer cost
- Low defect density
- No floating body effect
- High heat transfer rate to substrate
- Good process compatibility

iv. Gate-All-Around (GAA) MOSFET

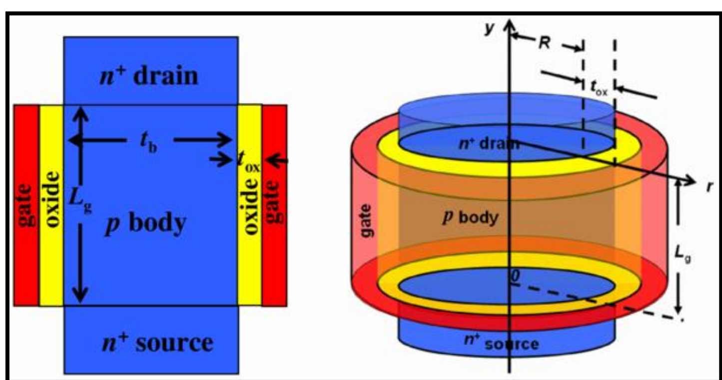


Figure 1.14: Cross-sectional view of cylindrical gate MOSFET with the coordinate system (Jin et al, 2012)

The scaling of classical MOSFET is approaching its limit due to the short channel effects. So, to overcome this problem multiple gate MOSFETs were introduced as a replacement of classical single gate MOSFET (Colinge, 2008; Lu et al, 2007). As the number of gate increases, multiple gate MOSFETs offer superior control over the channel, which helps to reduce short channel effects and leakage current. According to the number of gates, multiple gate MOSFETs are of various types, like Double gate MOSFET, Tri gate MOSFET, Gate all around (GAA) MOSFET (Cylindrical and Square). Among these multiple gate structures, gate all around structure offers superior control over the channel due to its surrounding gate structure, which in turn reduces the short channel effect effectively (Jiménez et al, 2004). Besides, GAA MOSFETs offer several advantages over single and other multiple gate MOSFETs like higher current drivability, mobility enhancement and so on. So, due to these advantages, gate all around MOSFETs are considered as the excellent candidates for future CMOS integration. Square gate all around MOSFET has higher current drive capability compared to cylindrical gate all around MOSFET. Despite these advantages, square gate all around MOSFET exhibits a very undesirable characteristic known as corner effect which occurs due to the electrostatic coupling of two adjacent gates at the corners. This effect degrades the device performance by increasing the off-state leakage current. The corner effect can be minimized by rounding the corner regions. Thus, surrounding-gate MOSFET is considered the most attractive device to succeed the planar MOSFET (Auth & Plummer, 1997). By wrapping the gate completely around the channel, the gate gains increased control of the potential in the channel and SCEs can be greatly suppressed. Besides the short channel benefit,

surrounding-gate MOSFETs have a higher packing density due to their increased current drive over the planar MOSFETs. It is well-known that scaling of device dimensions has been the primary factor driving improvements in integrated circuit performance and cost, which contributes to the rapid growth in the semiconductor industry.

1.3 RESEARCH GAPS

- Scale Down to few nm-a scale that is challenging to obtain using conventional device structures (using bulk silicon)
- As devices are scaled, the benefits of higher electric fields saturate while the associated reliability problems get worse.
- Design of RF CMOS circuits in real products remains a challenge due to the strong constraints on power consumption. In addition, the issue of noise is still an active area of investigation for amplifiers and receivers for RF communication.
- Gate Leakage is another deleterious issue that occurs as gate oxide thickness is order of 1-2nm. This leakage is result of quantum mechanical tunneling, an effect that actually possess a fundamental limitation for further MOSFET scaling and also degrades the device performance.
- Densely packed circuits such as VLSI or ULSI circuits often operate at elevated temperatures due to heat generation. Also, as the properties of semiconductor depend upon the temperature, thus there is a need to study the effect of temperature in order to investigate the stability of the device.

1.4 POSSIBLE SOLUTIONS

1.4.1 Silicon Nanowires

Silicon Nanowire (SiNW) is a possible way as its body thickness (diameter) can readily be reduced to few nm that is challenging to obtain using bulk silicon.

Silicon nanowires (NWs) have recently gained attention as a new class of nanoscale materials for the next generation devices. These nanoscale materials with high degree of freedom are realizing various one-dimensional structures. These offer the possibility of enhanced electrostatic control and quasi- ballistic transport (Cui & Lieber, 2001).

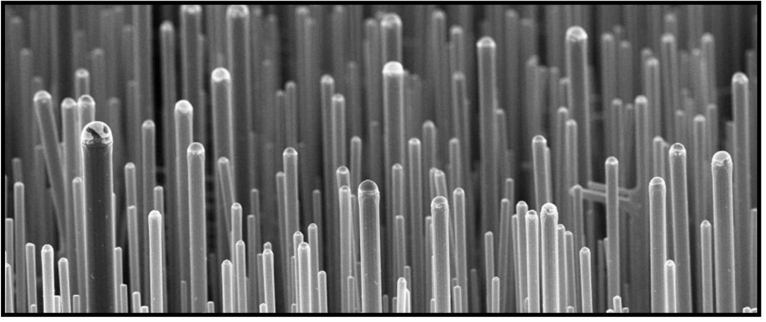


Figure 1.15: SEM image of silicon nanowires (SiNW)

A. Electronic properties of SiNW

From applications point of view, it has been observed that p type and n type doped SiNWs can be assembled to form p-n junctions, bipolar transistors, and complementary inverters and thus leads to an important suggestion that SiNWs may become fundamental components for nanoscale electronics. The band gap, valley splitting, and effective masses as functions of wire dimension-all properties are suitable for high performance nano-transistors fabricated with SiNWs. An increased bandgap exponentially suppresses parasitic interband tunneling which is a

fundamental limit to scaling of Silicon transistors (Solomon et al, 2004). The effective mass of nanowire affects both the mobility and the density of states. Moreover, mobility will still be a parameter that governs some performance metrics in nano-transistors. The density of states directly affects the quantum capacitance and current drive which therefore affects the performance of sub-nm range transistors (Zhao et al, 2004; Zheng et al, 2005). Fig. 1.16 illustrates the effect of quantum confinement on the bandgap of silicon nanowire as a function of wire thickness. It is evident from the figure that the bandgap is 2.5 eV for a 1.2nm wire and it falls to 1.56 eV for a 2.7nm wire.

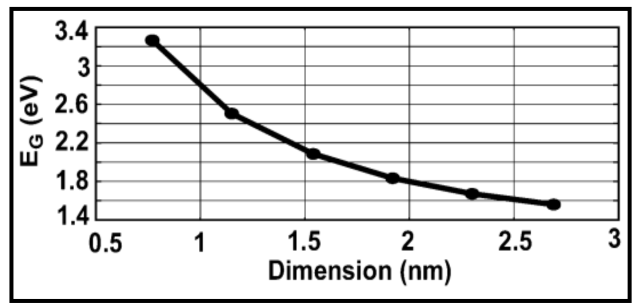


Figure 1.16: SiNW bandgap as a function of SiNW thickness (Zheng et al, 2005)

B. Physical Properties of SiNWs

1. It has been found that when quantum confinement effects are combined with surface phenomena, photoluminescence from Si nano-objects appears (Ma et al, 2003).

2. Many other structural parameters i.e. growth directions, cross section, may also influence band-structure and thus the physical properties of SiNWs, especially for sub-nm SiNWs (Migas & Borisenko, 2007).

3. Ramayya *et al*. reported that the small-diameter SiNWs still have high carrier mobility. The high carrier mobility is essential for fabricating high performance FETs (Ramayya et al, 2007)

4. It is also pointed out that SiNWs arrays pose to be more sufficient light absorbers than bulk silicon. These novel properties indicate that SiNWs are very attractive for applications in Nano-devices (Wan et al, 2009).

5. The SiNWs that employed as building blocks in Nano-devices such as FETs, sensors, solar cells and lithium battery, at the present time, usually are not ultra-tiny nanowires. Their typical diameter and length are tens of nanometers and hundreds of nanometers, respectively.

All of these novel properties indicate that SiNWs are very attractive for applications in nano-devices.

1.4.2 Silicon Nanowire Transistors

SiNWs MOSFET have been demonstrated as one of the promising building blocks for next generation circuit and have attracted much interest. Silicon nanowire transistors with various types of cross-sections are being extensively explored by several experimental groups. Fig. 1.17 shows the various cross-sections of SiNW MOSFET. There are many techniques to fabricate SiNWs related FETs. The methodology can totally be divided into “top-down”, “bottom-up” and the hybrid of both. The “top-down” technique is based on the conversional complementary metal oxide-semiconductor (CMOS) technique that usually employs lithography performance on SOI (Melosh et al, 2003).

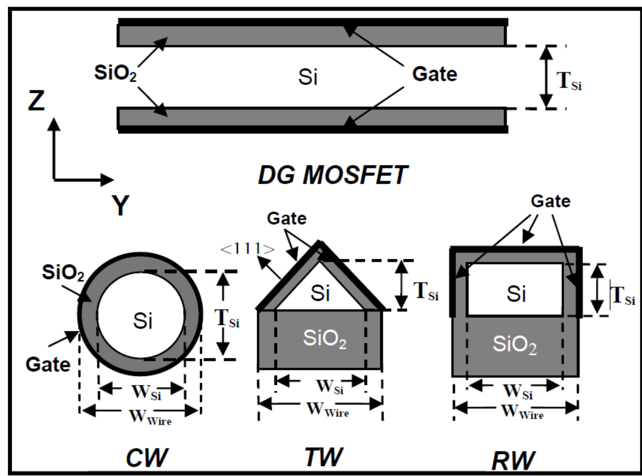


Figure 1.17: Various cross-sections of silicon nanowire transistor (Wang, 2005)

Exceptionally, a novel pathway called super-lattice nanowire pattern transfer (SNAP) which makes use of super-lattice grown by molecular beam epitaxy (MBE) is also reported. Generally, the "top-down" technique has perfect control on the morphology and location of SiNWs. Among all the cross-sections, circular cross-section being the most prominent one as it offers outstanding electrostatic control as shown in Fig. 1.18

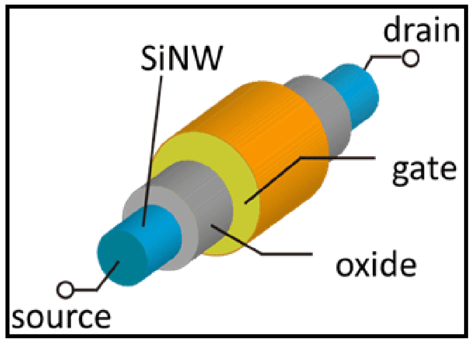


Figure 1.18: Cross-sections of silicon nanowire transistor

A. ***Advantages of SiNW MOSFET*** (Goldberger et al, 2006; Singh et al, 2006b)

1. The ability of the suppression of short-channel effects and thus, the suppression of the off-leakage current of Si nanowire FETs are expected to be very good, because of the gate surrounding configuration.

2. Secondly, SiNW MOSFETs are expected to have high on-current because of the following reasons.

- One is the nature of quasi-one-dimensional conduction of thin nanowire with small freedom of the carrier scattering angle. Because of the small freedom of the carrier scattering, its conduction will be high.
- Second is the use of multi-quantum channels for the conduction. Si nanowire band structure is quite different from that of the bulk and many conduction sub-bands appear near the lowest sub-band. Those sub-bands contribute to the conduction as the gate voltage increase.

B. Drawback of SiNW MOSFET

One major problem facing SiNW MOSFET with SiO_2 gate oxide is the higher threshold voltage than required by ULSI technology. To overcome this discrepancy and to improve the device performance of SiNW, there is required some effective ways to overcome this.

1.5 OBJECTIVES OF THESIS

Today CMOS ICs are everywhere and essential in our life, ranging from portable electronics to telecommunications and transportation. Therefore, there is a need to study comprehensively the physics and applications of new device structure which extend Moore’s Law. The present thesis mainly aims to incorporate the advantages of both novel device structure (SiNW) and gate engineering scheme (GEWE) to examine its efficacy for high frequency and low power CMOS applications.

In this dissertation, all types of scaling issues mainly HCEs and DIBL of proposed device structure i.e., Gate Electrode Workfunction Engineered (GEWE)-Silicon Nanowire (SiNW) MOSFET have been critically scrutinized and compared with the conventional structures using device simulations obtained using ATLAS 3D device simulator. The analysis exemplified that this device structure has overcome the drawbacks faced by the planar structures and improves the device performance. Further, a comprehensive examination comprising of RF gain analysis including main FOMs, S-parameters and Noise evaluation, small signal model considering the effect of extrinsic and intrinsic parameters, linearity and intermodulation evaluation considering the gate stack architecture and study of device reliability at different ambient temperatures. The entire work in the present thesis is divided into seven chapters based on the following objectives listed below:

- To investigate the hot-carrier reliability of proposed device and compare it with its conventional counterparts in terms electron temperature, HE-gate current, electric field along the channel for high performance CMOS applications.
- AC analysis in terms of power gains, cut-off frequency etc. will be carried out for RF applications. Cut-off frequency, parasitic capacitances, intrinsic delay etc. would be evaluated and its superior performance over the conventional FETs would strengthen the idea of using it for switching applications, thereby giving a new opening for HF wireless communications.
- Examine the detailed high frequency performance of device in terms of scattering parameters and developed a small signal quasi-static model

considering both extrinsic and extrinsic parameters which calculates impedance and admittance of device at THz frequency range.

- To explore the noise behaviour that is of significant importance for Low-Noise Amplifiers and its applications in terms of noise performance metrics such as Noise Figure, Auto Correlation, Cross-Correlation etc., hence, presenting it as an attractive solution for the on-going integration process in analog and digital design technology.

- As oxide thickness scales down below 1.5nm, tunneling of carriers causes degradation in device analog performance and therefore, stack gate is amalgamated onto proposed device structure and study its analog and intermodulation behaviour for low power switching and Linear RF amplifiers.

- Investigate the Reliability issues of SG-GEWE-SiNW MOSFET at different ambient temperatures (200-600k) in terms of Analog, RF, Noise and Linearity FOMs which can be served as a worthy design tool for circuits operating at wide range of temperatures.

The intention behind these objectives is to find a new device structure with substantially reduced SCEs that provides an attractive design in view of a system on chip realization, where digital, mixed- signal base band and RF transceiver block would be integrated on a single chip.

1.6 ORGANIZATION OF DISSERTATION

In this present study, scaling issues such as HCEs, DIBL, V_{th} roll-off, leakage current etc. have been critically scrutinized and GEWE-SiNW MOSFET have been proposed for high performance analog and RF applications. This thesis is organized into seven chapters to accommodate all the research objectives. Each chapter is organized to be fundamentally self-contained.

Chapter-1 describes the review of the MOSFET basics, scaling issues and short channel effects. The chapter progresses towards need for advanced MOSFET structures such as GAA MOSFET, Nanowire MOSFET to extend Moore' and immunity against short channel effects. The architecture of SiNW MOSFET and the device physics considering the advantages of SiNW is explained in detail along with the simulation approaches. Further, a detailed description of Gate Electrode Workfunction Engineering Scheme and fabrication feasibility of GEWE-SiNW FETs is presented and lastly the overall organization of the thesis along with the importance of the research work is presented.

Chapter-2 explores the hot-carrier fidelity of GEWE-SiNW MOSFET using 3D device simulation. This chapter addresses the comparison of three different transport models with an aim to find which model is appropriate for sub-nm range device. Hot-carrier reliability is studied in terms of band bending, electron temperature, electron velocity, electric field and hot electron-gate current. Further, a comparative investigation for different values of oxide thickness and high-k has also been done to analyze the performance of GEWE-SiNW MOSFET.

Chapter-3 explores the quantitative investigation of the high-frequency performance of GEWE-SiNW MOSFET and results so obtained are simultaneously compared with SiNW MOSFET. Following figure of merits are analyzed such as transconductance (gm), cut-off frequency (f_T), maximum oscillator frequency (f_{MAX}), power gains (Gma, G_{MT}) parasitic capacitances, stern's stability factor and intrinsic delay. In addition, the efficacy of parameter variations such as oxide thickness, radius of silicon nanowire, channel length and gate metal workfunction engineering are analyzed on RF/microwave figure of merits of GEWE-SiNW MOSFET. Thus this chapter provides the detailed knowledge about the device's RF performance at such aggressively scaled dimensions.

Chapter-4 investigates the comparative analysis of small signal behaviour (S-parameters) and RF noise performance between GEWE-SiNW, SiNW and conventional MOSFET at THz frequency range. This chapter examines reflection and transmission coefficients, noise conductance, minimum noise figure and cross-correlation factor. This chapter also explains that S-parameters of GEWE-SiNW MOSFET further enhances by modulating the channel length, channel doping and workfunction difference of gate metal. Moreover, the efficacy of gate metal workfunction engineering is also studied on Noise behaviour and the results validate that tuning of workfunction difference results further improvement in device small-signal behaviour and noise performance as discussed in latter part of this chapter.

Chapter-5 examines the bias independent and dependent extrinsic and intrinsic parameters of GEWE-SiNW MOSFET by considering the quantum effects using

Pinch-off Cold-FET method and then these parasitic are removed from the device under consideration that is known as de-embedding. Further, to examine the effect of device parameter on these parameters, metal gate engineering and bias variation is also observed. Further, to examine the effect of device parameter on these parameters, metal gate engineering and bias variation is also observed. In addition, the nonquasi-static small signal model has also been studied in terms of Z and Y-parameters and the results show good agreement with 3D simulated results at thousands of GHz.

Chapter-6 optimizes the gate engineering scheme (both gate stack and gate metal workfunction engineering) of Stacked Gate (SG)-GEWE-SiNW MOSFET at room temperature for improved analog and intermodulation performance. This has been done by evaluating and analyzing the metrics such as Switching Ratio, Sub-threshold Swing (SS), Device Efficiency, channel and output resistance, VIP3, IIP3, 1-dB Compression Point, IMD3, HD2 and HD3. Further, the characteristics/performance is modulated by adjusting the workfunction difference of metal gate. The second part of this chapter explains the reliability issues of SG-GEWE-SiNW MOSFET over a wide range of ambient temperatures (200–600 K) using 3D-technology computer aided design quantum simulation. Analog, RF Noise and Linearity performance of SG-GWEW-SiNW is observed as a performance metrics. Hence, the results so obtained can be served as a worthy design tool for circuits operating at wide range of temperatures.

Chapter-7 summarizes the overall research work illustrated in this thesis along with the concrete conclusions drawn from the results presented. This chapter also discusses

about the future scope of the present work and how can this work be extended and used in future for further research directions.

1.7 References

Abuelma'atti, M. T. (2013) MOSFET Scaling Crisis and the Evolution of Nanoelectronic Devices: The Need for Paradigm Shift in Electronics Engineering Education. *Procedia-Social and Behavioral Sciences*, 102, 432-437.

Arora, N. (1993) MOSFET Models for VLSI Circuit Simulation Theory and Practice Springer. *New York*.

Auth, C. P. & Plummer, J. D. (1997) Scaling theory for cylindrical, fully-depleted, surrounding-gate MOSFET's. *IEEE Electron Device Letters*, 18(2), 74-76.

Balestra, F., Cristoloveanu, S., Benachir, M., Brini, J. & Elewa, T. (1987) Double-gate silicon-on-insulator transistor with volume inversion: A new device with greatly enhanced performance. *IEEE Electron Device Letters*, 8(9), 410-412.

Bampi, S. & Plummer, J. D. (1986) A modified lightly doped drain structure for VLSI MOSFET's. *IEEE Transactions on Electron Devices*, 33(11), 1769-1779.

Bangsaruntip, S., Cohen, G. M., Majumdar, A., Zhang, Y., Engelmann, S., Fuller, N., Gignac, L., Mittal, S., Newbury, J. & Guillorn, M. (2009) High performance and highly uniform gate-all-around silicon nanowire MOSFETs with wire size dependent scaling, *Electron Devices Meeting (IEDM), 2009 IEEE International*. IEEE.

Bohr, M. & Mistry, K. (2011) Intel's revolutionary 22 nm transistor technology. *Intel website*.

Bondyopadhyay, P. K. (1998) Moore's law governs the silicon revolution. *Proceedings of the IEEE*, 86(1), 78-81.

Borkar, S. (1999) Design challenges of technology scaling. *IEEE micro*, 19(4), 23-29.

Brown, A. R., Watling, J. R. & Asenov, A. (2002) A 3-D atomistic study of archetypal double gate MOSFET structures. *Journal of Computational Electronics*, 1(1-2), 165-169.

Chamberlain, S. G. & Ramanan, S. (1986) Drain-induced barrier-lowering analysis in VLSI MOSFET devices using two-dimensional numerical simulations. *IEEE Transactions on Electron Devices*, 33(11), 1745-1753.

Choi, J.-Y. & Fossum, J. G. (1991) Analysis and control of floating-body bipolar effects in fully depleted submicrometer SOI MOSFET's. *IEEE Transactions on Electron Devices*, 38(6), 1384-1391.

Choi, Y.-K., Asano, K., Lindert, N., Subramanian, V., King, T.-J., Bokor, J. & Hu, C. (1999) Ultra-thin body SOI MOSFET for deep-sub-tenth micron era, *Electron Devices Meeting, 1999. IEDM'99. Technical Digest. International*. IEEE.

Choi, Y.-K., Lindert, N., Xuan, P., Tang, S., Ha, D., Anderson, E., King, T.-J., Bokor, J. & Hu, C. (2001) Sub-20 nm CMOS FinFET technologies, *Electron Devices Meeting, 2001. IEDM'01. Technical Digest. International*. IEEE.

Colinge, J.-P. (2008) *FinFETs and other multi-gate transistors*, *73*Springer.

Cui, Y. & Lieber, C. M. (2001) Functional nanoscale electronic devices assembled using silicon nanowire building blocks. *science*, 291(5505), 851-853.

Davari, B., Dennard, R. H. & Shahidi, G. G. (1995) CMOS scaling for high performance and low power-the next ten years. *Proceedings of the IEEE*, 83(4), 595-606.

Dennard, R. H., Gaensslen, F. H., Kuhn, L. & Yu, H. (2007) Design of micron MOS switching devices. *IEEE Solid-State Circuits Society Newsletter*, 12(1), 35-35.

Frank, D. J., Dennard, R. H., Nowak, E., Solomon, P. M., Taur, Y. & Wong, H.-S. P. (2001) Device scaling limits of Si MOSFETs and their application dependencies. *Proceedings of the IEEE*, 89(3), 259-288.

Frank, M. M., Kim, S., Brown, S. L., Bruley, J., Copel, M., Hopstaken, M., Chudzik, M. & Narayanan, V. (2009) Scaling the MOSFET gate dielectric: From high-k to higher-k? *Microelectronic Engineering*, 86(7), 1603-1608.

Goldberger, J., Hochbaum, A. I., Fan, R. & Yang, P. (2006) Silicon vertically integrated nanowire field effect transistors. *Nano letters*, 6(5), 973-977.

Guo, J., Lundstrom, M. & Datta, S. (2002) Performance projections for ballistic carbon nanotube field-effect transistors. *Applied Physics Letters*, 80(17), 3192-3194.

Hower, P. L. & Pendharkar, S. (2005) Short and long-term safe operating area considerations in LDMOS transistors, *Reliability Physics Symposium, 2005. Proceedings. 43rd Annual. 2005 IEEE International*. IEEE.

Hu, C. (1989) Hot carrier effects. *Advanced MOS Device Physics*, 18, 119-160.

Hu, C. (2010) *Modern semiconductor devices for integrated circuits*Prentice Hall.

Inani, A., RAMGOPAL RAO, V., Cheng, B., Zeitzoff, P. & Woo, J. (1999) Capacitance degradation due to fringing field in deep sub-micron MOSFETs with High-K gate dielectrics.

Jiménez, D., Saenz, J., Iniguez, B., Sune, J., Marsal, L. & Pallares, J. (2004) Modeling of nanoscale gate-all-around MOSFETs. *IEEE Electron Device Letters*, 25(5), 314-316.

Jin, X., Liu, X., Wu, M., Chuai, R., Lee, J.-H. & Lee, J.-H. (2012) A continuous current model of ultra-thin cylindrical surrounding-gate inversion-mode Si nanowire nMOSFETs considering a wide range of body doping concentration. *Semiconductor Science and Technology*, 28(1), 015002.

Jung, S.-M., Mizutani, T. & Hiramoto, T. (2014) Effect of drain-induced barrier lowering on performance of ultralow-supply-voltage CMOS circuits operating in subthreshold region. *Japanese Journal of Applied Physics*, 53(12), 124301.

Kaga, T. & Sakai, Y. (1988) Effects of lightly doped drain structure with optimum ion dose on p-channel MOSFETs. *IEEE Transactions on Electron Devices*, 35(12), 2384-2390.

Khanna, V. K. (2016) Short-Channel Effects in MOSFETs, *Integrated Nanoelectronics*Springer, 73-93.

Kumar, M. J. & Chaudhry, A. (2004) Two-dimensional analytical modeling of fully depleted DMG SOI MOSFET and evidence for diminished SCEs. *IEEE Transactions on Electron Devices*, 51(4), 569-574.

Kumar, M. J., Orouji, A. A. & Dhakad, H. (2006) New dual-material SG nanoscale MOSFET: analytical threshold-voltage model. *IEEE transactions on Electron Devices*, 53(4), 920-922.

Lee, B. H., Oh, J., Tseng, H. H., Jammy, R. & Huff, H. (2006) Gate stack technology for nanoscale devices. *materials today*, 9(6), 32-40.

Lee, M. L., Fitzgerald, E. A., Bulsara, M. T., Currie, M. T. & Lochtefeld, A. (2005) Strained Si, SiGe, and Ge channels for high-mobility metal-oxide-semiconductor field-effect transistors. *Journal of Applied Physics*, 97(1), 1.

Leitz, C., Currie, M., Lee, M., Cheng, Z.-Y., Antoniadis, D. & Fitzgerald, E. (2001) Hole mobility enhancements in strained Si/Si1− yGeyp-type metal-oxide-semiconductor field-effect transistors grown on relaxed Si1− xGex (x< y) virtual substrates. *Applied Physics Letters*, 79(25), 4246-4248.

Long, W. & Chin, K. K. (1997) Dual material gate field effect transistor (DMGFET), *Electron Devices Meeting, 1997. IEDM'97. Technical Digest., International*. IEEE.

Long, W., Ou, H., Kuo, J.-M. & Chin, K. K. (1999) Dual-material gate (DMG) field effect transistor. *IEEE Transactions on Electron Devices*, 46(5), 865-870.

Lu, D. D., Dunga, M. V., Lin, C.-H., Niknejad, A. M. & Hu, C. (2007) A multi-gate MOSFET compact model featuring independent-gate operation, *Electron Devices Meeting, 2007. IEDM 2007. IEEE International*. IEEE.

Ma, D., Lee, C., Au, F., Tong, S. & Lee, S. (2003) Small-diameter silicon nanowire surfaces. *Science*, 299(5614), 1874-1877.

Melosh, N. A., Boukai, A., Diana, F., Gerardot, B., Badolato, A., Petroff, P. M. & Heath, J. R. (2003) Ultrahigh-density nanowire lattices and circuits. *Science*, 300(5616), 112-115.

Migas, D. & Borisenko, V. (2007) Tailoring the character of the band-gap in-,-and-oriented silicon nanowires. *Nanotechnology*, 18(37), 375703.

Moers, J., Hagedorn, M. & Zhao, Q.-T. (2010) Fabrication of MOS-Capacitors for characterization of high κ-materials.

Mohankumar, N., Syamal, B. & Sarkar, C. K. (2010) Influence of channel and gate engineering on the analog and RF performance of DG MOSFETs. *IEEE transactions on Electron Devices*, 57(4), 820-826.

Mohapatra, N. R., Dutta, A., Desai, M. P. & Rao, V. R. (2001) Effect of fringing capacitances in sub 100 nm MOSFETs with high-K gate dielectrics, *VLSI Design, 2001. Fourteenth International Conference on*. IEEE.

Moore, G. E. (2004) Progress in digital integrated electronics. *SPIE MILESTONE SERIES MS*, 178, 179-181.

Nair, R. (2002) Effect of increasing chip density on the evolution of computer architectures. *IBM Journal of Research and Development*, 46(2.3), 223-234.

Nandakumar, M., Chatterjee, A., Rodder, M. S. & Chen, I.-C. (1999) Semiconductor devices with pocket implant and counter doping. Google Patents.

Polishchuk, I., Ranade, P., King, T.-J. & Hu, C. (2001) Dual work function metal gate CMOS technology using metal interdiffusion. *IEEE Electron Device Letters*, 22(9), 444-446.

Ramayya, E. B., Vasileska, D., Goodnick, S. M. & Knezevic, I. (2007) Electron mobility in silicon nanowires. *IEEE Transactions on Nanotechnology*, 6(1), 113-117.

Ravindhran, K., Han, Y. P., Jhota, R. & Parmantie, W. D. (1995) MOSFET with gate-penetrating halo implant. Google Patents.

Ravariu, C. & Babarada, F. (2011) Modeling and simulation of special shaped SOI materials for the nanodevices implementation. Journal of Nanomaterials, 2011, 4.

Reed, M. A. (1999) Molecular-scale electronics. *Proceedings of the IEEE*, 87(4), 652-658.

Rubel, D., Sun, K., Hall, S., Ashburn, P. & Hakim, M. (2015) Effect of lightly doped drain on the electrical characteristics of CMOS compatible vertical MOSFETs, *Advances in Electrical Engineering (ICAEE), 2015 International Conference on*. IEEE.

Shirak, O., Shtempluck, O., Kotchtakov, V., Bahir, G. & Yaish, Y. (2012) High performance horizontal gate-all-around silicon nanowire field-effect transistors. *Nanotechnology*, 23(39), 395202.

Singh, N., Agarwal, A., Bera, L., Liow, T., Yang, R., Rustagi, S., Tung, C., Kumar, R., Lo, G. & Balasubramanian, N. (2006a) High-performance fully depleted silicon nanowire (diameter/spl les/5 nm) gate-all-around CMOS devices. *IEEE Electron Device Letters*, 27(5), 383-386.

Singh, N., Lim, F., Fang, W., Rustagi, S., Bera, L., Agarwal, A., Tung, C., Hoe, K., Omampuliyur, S. & Tripathi, D. (2006b) Ultra-narrow silicon nanowire gate-all-around CMOS devices: Impact of diameter, channel-orientation and low temperature on device performance, *Electron Devices Meeting, 2006. IEDM'06. International*. IEEE.

Solomon, P. M., Jopling, J., Frank, D. J., D'Emic, C., Dokumaci, O., Ronsheim, P. & Haensch, W. (2004) Universal tunneling behavior in technologically relevant P/N junction diodes. *Journal of applied physics*, 95(10), 5800-5812.

Takeda, E., Yang, C. Y.-W. & Miura-Hamada, A. (1995) *Hot-carrier effects in MOS devices*Academic Press.

Taur, Y. & Ning, T. H. (2013) *Fundamentals of modern VLSI devices*Cambridge university press.

Thompson, S. E. & Parthasarathy, S. (2006) Moore's law: the future of Si microelectronics. *Materials today*, 9(6), 20-25.

Troutman, R. R. (1979) VLSI limitations from drain-induced barrier lowering. *IEEE Journal of Solid-State Circuits*, 14(2), 383-391.

Veeraraghavan, S. & Fossum, J. G. (1989) Short-channel effects in SOI MOSFETs. *IEEE Transactions on Electron Devices*, 36(3), 522-528.

Wan, Y., Sha, J., Chen, B., Fang, Y., Wang, Z. & Wang, Y. (2009) Nanodevices based on silicon nanowires. *Recent patents on nanotechnology*, 3(1), 1-9.

Wang, J., Polizzi, E. & Lundstrom, M. (2003) A computational study of ballistic silicon nanowire transistors, *Electron Devices Meeting, 2003. IEDM'03 Technical Digest. IEEE International*. IEEE.

Wang, J. (2005) Device physics and simulation of silicon nanowire transistors.

Wolf, S. (1995) Silicon processing for the VLSI era, LATTICE.

Yang, F.-L., Chen, H.-Y., Chen, F.-C., Chan, Y.-L., Yang, K.-N., Chen, C.-J., Tao, H.-J., Choi, Y.-K., Liang, M.-S. & Hu, C. (2002) 35 nm CMOS FinFETs, *VLSI Technology, 2002. Digest of Technical Papers. 2002 Symposium on*. IEEE.

Yang, F.-L., Lee, D.-H., Chen, H.-Y., Chang, C.-Y., Liu, S.-D., Huang, C.-C., Chung, T.-X., Chen, H.-W., Huang, C.-C. & Liu, Y.-H. (2004) 5nm-gate nanowire FinFET, *VLSI Technology, 2004. Digest of Technical Papers. 2004 Symposium on*. IEEE.

Young, K. K. (1989) Short-channel effect in fully depleted SOI MOSFETs. IEEE Transactions on Electron Devices, 36(2), 399-402.

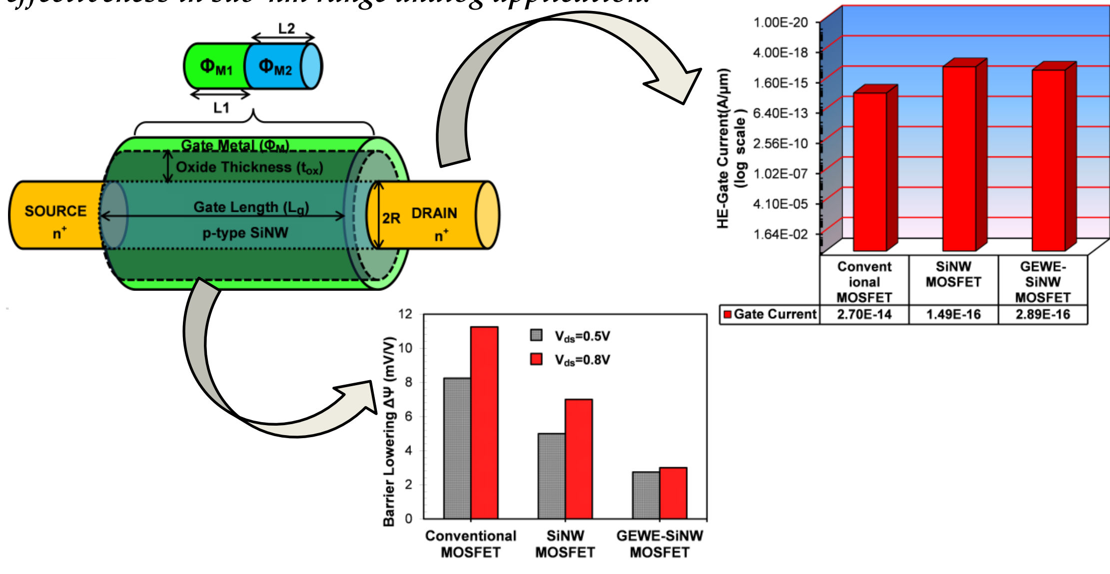
Zhao, X., Wei, C., Yang, L. & Chou, M. (2004) Quantum confinement and electronic properties of silicon nanowires. *Physical review letters*, 92(23), 236805.

Zheng, Y., Rivas, C., Lake, R., Alam, K., Boykin, T. B. & Klimeck, G. (2005) Electronic properties of silicon nanowires. *IEEE transactions on electron devices*, 52(6), 1097-1103.

CHAPTER 2

Investigation of Hot-Carrier Degradation in Gate Electrode Workfunction Engineered (GEWE) Silicon Nanowire (SiNW) MOSFET

- *Gate Electrode Workfunction Engineered (GEWE) is amalgamated onto Silicon Nanowire (SiNW) MOSFET*
- *Hot carrier fidelity of GEWE-SiNW MOSFET has been explored at 300 K using DEVEDIT-3D device editor and ATLAS device simulation software.*
- *Reliability of GEWE SiNW MOSFET is studied in terms of electron temperature, electron velocity and hot electron gate current for reflecting its efficacy in high power CMOS applications.*
- *Further, a comparative investigation for different values of oxide thickness and high-k has been done to analyze the hot-carrier performance of GEWE-SiNW MOSFET.*
- *It has been observed that with oxide thickness 0.5 nm, the hot-carrier reliability and device performance improves in comparison to oxide thickness 2.5 nm.*
- *In addition, with k = 21(HfO_2) as gate oxide, device performance in terms of hot-carrier reliability is further enhanced due to increased capacitance and thus offer its effectiveness in sub-nm range analog application.*



2.1 INTRODUCTION

From past few eras, the foremost concern for CMOS devices is scaling effects known as SCEs and it results in many problems such as an escalation in power consumption, leakage current (De & Borkar, 1999), punch-through effect etc. Hot-electron degradation is another detrimental effect of short-channel devices (Krieger et al, 1991; Orouji & Kumar, 2005). As discussed in previous chapter that in scaled devices the hot carriers have ample of high energies and thrust to allow them to be injected from the semiconductor into the surrounding oxide films such as the gate and sidewall silicon oxides (Groeseneken, 2001). These free mobile carriers in the oxide evoke several physical devastation processes that can highly change the device characteristics over continuous periods. Continuous damage eventually causes the circuit to fail as crucial parameters such as threshold voltage shift due to above-mentioned destruction (Kaur et al, 2007; Pan et al, 1994). Drain Induced Barrier Lowering (DIBL) is an another significant parameter to examine SCEs in VLSI MOSFET devices (Arora, 1993). It affects the transfer characteristic in sub-threshold regime by a lateral shift (Jeon et al, 2010). To overcome such effects, number of device engineering schemes such as source/drain engineering (Kranti & Armstrong, 2006), gate metal workfunction engineering (Deb et al, 2012; Dubey et al, 2013; Long & Chin, 1997), channel engineering (Yu et al, 1997) and some novel device structures such as double gate MOSFET (Barsan, 1981; Venkatesan et al, 1992), Fin-FETs (Sohn et al, 2012), cylindrical gate MOSFET (Sharma & Vishvakarma, 2013), nanowire MOSFET (Iwai et al, 2011; Wang et al, 2013) have been explored and employed during the past few years. Among them, due to ideal symmetry, excellent

gate controllability and potential benefits of the silicon nanowire, gate-all-around (GAA) silicon nanowire MOSFET has emerged as a most favorable candidate for future silicon based nano-devices (Chen & Tan, 2014; Wang et al, 2007). This configuration manifest a superior control of short channel effects (SCEs) because of tremendous electrostatic coupling between the conducting channel and the surrounding gate. The nanowire (NW) transistors can be seen as the highest integration of the innovative nano-devices, and it is one of the most promising means of overwhelming the limits of planar silicon devices because of their suitability with gate all around design. Existing approaches in nano-scale fabrication techniques have shown that semiconductor nanowires may turn into an aspirant for next generation technologies. Silicon (Si) and Germanium (Ge) nanowire transistors are also significant because of their flexibility with the CMOS technology (Mukherjee & Maiti, 2012). Silicon nanowires (NWs) have recently gained attention as a new class of nano-scale materials for the next generation devices. These nano-scale materials with high degree of freedom are realizing various one-dimensional structures. These offer the possibility of enhanced electrostatic control and quasi-ballistic transport (Mikolajick & Weber, 2015). However, as with many novel device architectures, the SiNW MOSFET has problems of its own. One major problem facing nanowire MOSFETs with SiO_2 gate stack is the lower threshold voltage than desired. But, channel doping to correct the threshold voltage, is difficult due to the narrow radius of nanowire. In addition, carrier mobility is also impacted with higher channel doping. Hence, there is need of integration of some engineering schemes to overcome such effect. Gate work function tuning would thus make a better solution (Long et al,

1999), as it improves the transport efficiency of carriers by modifying electric field in the channel and surface potential along the channel which results in enhanced transconductance and reduced SCEs (Zheng, 2011). In this chapter, for the first time, gate electrode workfunction engineering (GEWE) scheme is amalgamated onto Gate All Around Silicon Nanowire (SiNW) MOSFET to enhance the device performance in terms of current driving capability and thus carrier efficiency which is an important parameter of any electronic device. Moreover, as the problem of hot carrier and DIBL becomes important in deep-submicron MOSFETs, it is thus increasingly required to investigate the hot carrier reliability of device in terms of hot-electron-injected gate current (HE-I_g), impact-ionization substrate current, electron velocity and electron temperature near the drain end to study their effect on the overall chip performance.

The complete work in this chapter is outlined as follows: First part of this chapter examines the immunity of GEWE-SiNW MOSFET towards SCEs in terms of Hot-Carrier and DIBL and compared with SiNW MOSFET at room temperature. In the later part of chapter, the impact of gate oxide thickness (t_{ox}) and different high-k materials on the performance of hot-carrier efficiency has also been examined with an aim to analyse the reasonable restraints in device designs and its parameter optimization.

2.2 Device Structure and its Parameters

The simulated device structure i.e. GEWE SiNW MOSFET consists of gate metal M1 and M2 of length L_1 and L_2 as shown in Fig 2.01. The total gate length (L_g) is 30 nm and thickness of oxide (t_{ox}) is 1.5 nm. In this case, substrate/channel doping is p-type with a concentration (N_A) of $1\times10^{16}cm^{-3}$; source and drain are n-type with uniform

doping profiles (N_D) of $5\times10^{19}cm^{-3}$. The metal gate work function at the source end (Φ_{m1}) is 4.8 eV (Gold) and metal gate work function at the drain end (Φ_{m2}) is 4.4 eV (Titanium). All simulations have been achieved using ATLAS and DEVEDIT-3D device simulator (SILVACO, 2016).

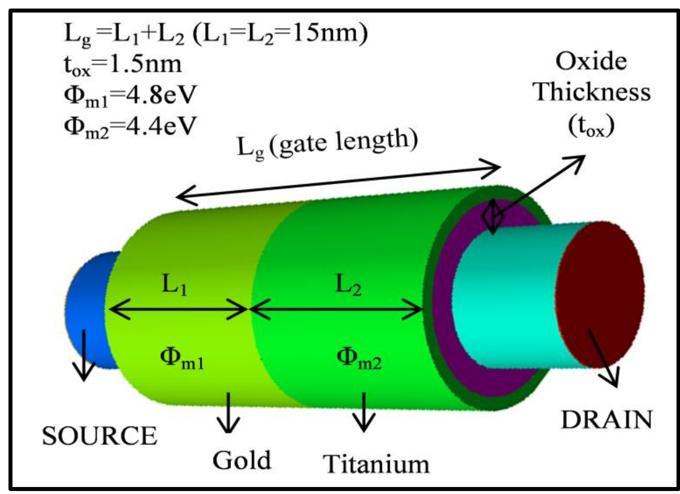


***Figure 2.01:** Simulated 3-D structure of GEWE-SiNW MOSFET. Default device parameters are: Channel Length (L_g) =30nm, Oxide thickness (t_{ox}) =1.5nm, Radius of Silicon pillar (R) = 5nm, Source/Drain Doping (N_D) =5x10^{19} cm^{-3}, Channel Doping (N_A) =1x10^{16} cm^{-3}, Gate Metal workfunction (Φ_{M1}) = 4.8 eV (Gupta et al, 2015b)*

Models like, concentration-dependent low field mobility (CONMOB) model, parallel electric-field-dependent (FLDMOB) model, inversion layer Lombardi CVT mobility model and Shockley-Read-Hall (SRH) for carrier recombination have been incorporated. Moreover, drift-diffusion transport model (DDM) is not suitable for sub-50 nm gate length devices, since it neglects the nonlocal effects. Therefore, the influence of different transport models, i.e., classical (Drift Diffusion Model) and semi-quantum (Hydrodynamic and Energy Balance Transport model) on the electrical performance of GEWE-SiNW MOSFET (Gupta & Chaujar, 2014) is also studied. It is

found that hydrodynamic model (HDM) is most appropriate in comparison to classical Drift-diffusion model for GEWE-SiNW as is clearly revealed from Fig. 2.02 (a-d).

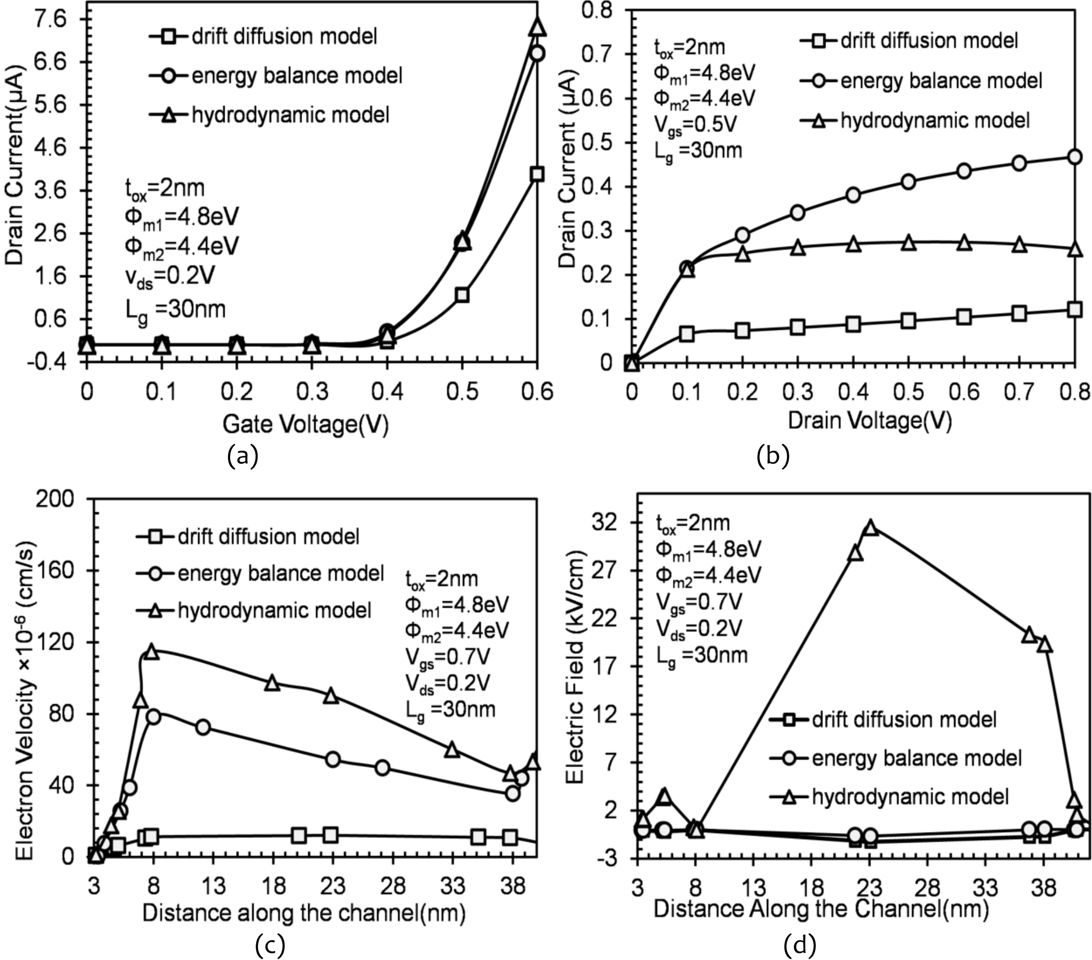


***Figure 2.02:** (a) Transfer Characteristics, (b) Output Characteristics of GEWE-SiNW MOSFET for different transport models. (c) Electron Velocity, (d) Electric Field as a function of position along the channel for GEWE-SiNW MOSFET at V_{ds}=0.2 V and V_{gs}=0.7 V for different transport models (Gupta & Chaujar, 2014).*

Fig. 2.02 (c) shows the variation of electron velocity along the channel. In DDM, there is a simple linear relationship between the electron velocity and the electric field. It is evident from the figure that carrier velocity is increasing from source to

channel region and then saturates to a constant value (V_S=10^7cm/s). However, in energy balance model and hydrodynamic model, the carrier velocity in the active region exceeds the saturation velocity since, in EB model, two additional equations i.e. conservation of carrier energy and energy flux are taken into account, which makes electron velocity dependent on relaxation time and effective mass. Since non-stationary effects are governed by relaxation time, the carrier velocity is greater than saturation velocity. Fig. 2.02 (d) shows the variation of electric field along the channel. Since, V_{t1} (threshold voltage due to first metal gate)>V_{t2}(threshold voltage due to second metal gate) owing to GEWE engineering scheme (Long et al, 1999), the electric field along the channel suddenly increases near the interface of two gate metals which results in an increase in gate transport efficiency. It can be seen that in HDM, the peak of the electric field in the channel region is higher as compared to others. HDM makes use of electron temperature for the description of charge transport and considers inertia effects as well. The lessening in the electric field at the drain end can be interpreted as a reduction in hot carrier effects, lower impact ionization and higher breakdown voltage. Therefore in this analysis, HDM model is incorporated along with the default physical simulation models. The HDM transport model includes the continuity equations, momentum transport equations, energy balance equations of the carriers, and the Poisson equation. It can model the nonlocal transport phenomenon and is more accurate than the drift–diffusion method. The HD Model can be solved as follows:

The Energy Balance Transport (EBT) Model follows the derivation by Stratton (Stratton, 1972) which is derived starting from the Boltzmann Transport Equation

(BTE). By applying certain assumptions, this model decomposes into the hydrodynamic model (Yang et al, 2003) where Boltzmann statistics are preferred over the Fermi statistics. This model is modeled by following equations (SILVACO, 2016):

$$\xi_n = \frac{d(\ln \mu_n)}{d(\ln T_n)} = \frac{T_n}{\mu_n} \qquad (2.1)$$

$$\xi_p = \frac{d(\ln \mu_p)}{d(\ln T_p)} = \frac{T_p}{\mu_p} \qquad (2.2)$$

The parameters ξ_n and ξ_p are dependent on the carrier temperatures. Different assumptions concerning ξ_n and ξ_p correspond to different non-local models. In the high-field saturated velocity limit, which corresponds to velocity saturation, the carrier mobilities are inversely proportional to the carrier temperatures. By putting $\xi_n = 0$; this would correspond to the simplified HDM for electrons. The parameter, ξ_n can be specified using the KSN parameters on the MODELS statement (SILVACO, 2016). For the study of gate currents, the Selberherr's impact ionization and hot-electron-injection models are used to provide an accurate measure of hot-carrier-injection in short-channel devices. Default simulator coefficients for all parameters have been employed. In order to fairly analyze the device performances, all the three devices are optimized to have the same threshold voltage, i.e., 0.32V.

2.2.1. Calibration

Figure 2.03 shows simulation result compared with the experimental data of SiNW MOSFET reported in the literature (Suk et al, 2005) at V_{ds}=1.0V. The calibration of

model parameters used in simulation has been performed according to the published results to validate the simulation results.

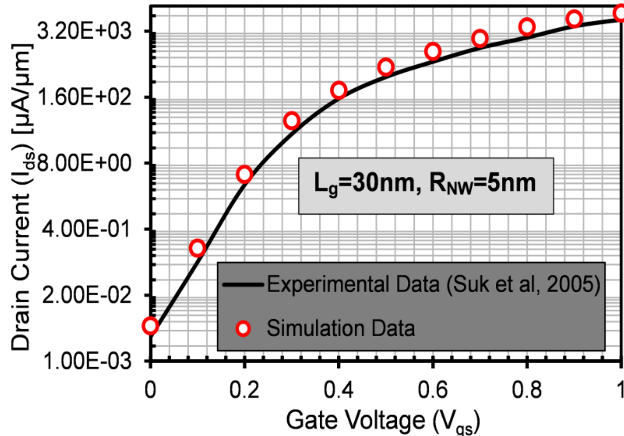


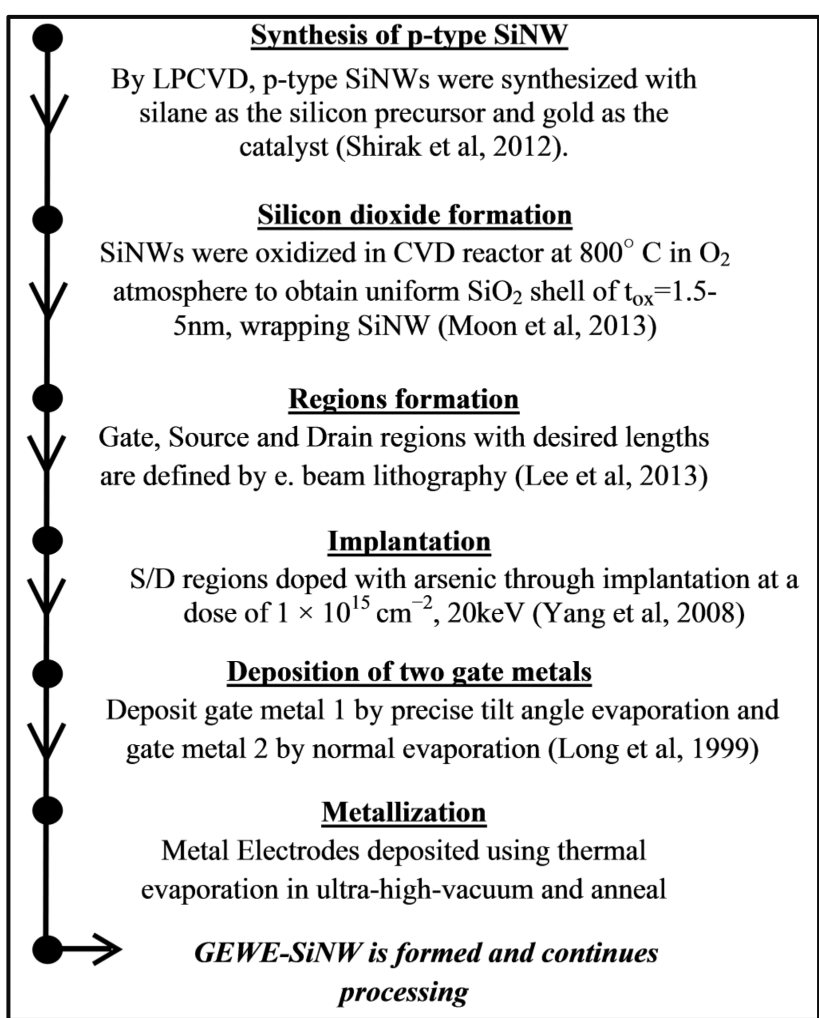
Figure 2.03: Calibration with the experimental result, I_{ds}-V_{gs} characteristics of SiNW MOSFET(Suk et al, 2005).

2.3 FABRICATION FEASIBILITY

The fabrication feasibility of SiNW MOSFET has been reported in the literature using several integration schemes. Yang et al, (Yang et al, 2008) fabricated vertical gate-all-around silicon nanowire MOSFET. Rustagi et al., (Rustagi et al, 2007) reported the fabrication of CMOS inverter based GAA SiNW MOSFETs using top-down approach. Moreover, for the realization of GEWE architecture, numerous schemes have been suggested such as tilt angle evaporation metal gate deposition (Long et al, 1999), metal interdiffusion process (Polishchuk et al, 2001) and fully silicided (FUSI) metal gate (Liu et al, 2005). Further, CMOS with dual metal gate has also been successfully fabricated using poly-Si gate doping control of the source and drain side gate individually (Na & Kim, 2006). Thus, the proposed device (GEWE-SiNW MOSFET) can be fabricated using the above design schemes, in which the advantages

of GEWE scheme are amalgamated with SiNW MOSFET making it a promising design for system on chip and RF/microwave applications. A proposed summary of the process flow, outlining the fabrication process of GEWE-SiNW MOSFET and its integration with the standard CMOS process, is shown in Table 2.01.

Table 2.01: Summary of the Standard Process Flow of GEWE-SiNW (Lee et al, 2013; Moon et al, 2013; Shirak et al, 2012; Yang et al, 2008)



2.4. Results And Discussion

Fig.2.04 (a) shows the drain current and gate transconductance characteristics of GEWE-SiNW MOSFET at a drain bias, V_{ds}=0.4 V. As shown in Fig. 2.04(a), the

current driving capability of Nano-scale GEWE-SiNW MOSFET is enhanced by 100% in comparison to SiNW MOSFET. This improvement is due to the integration of metal gate engineering scheme onto nanowire which causes gradual step change of surface potential at the interface of two metals and hence increases the gate efficiency of device. The larger the transconductance, the greater the gain (amplification) it is capable of delivering when all other factors are held constant.

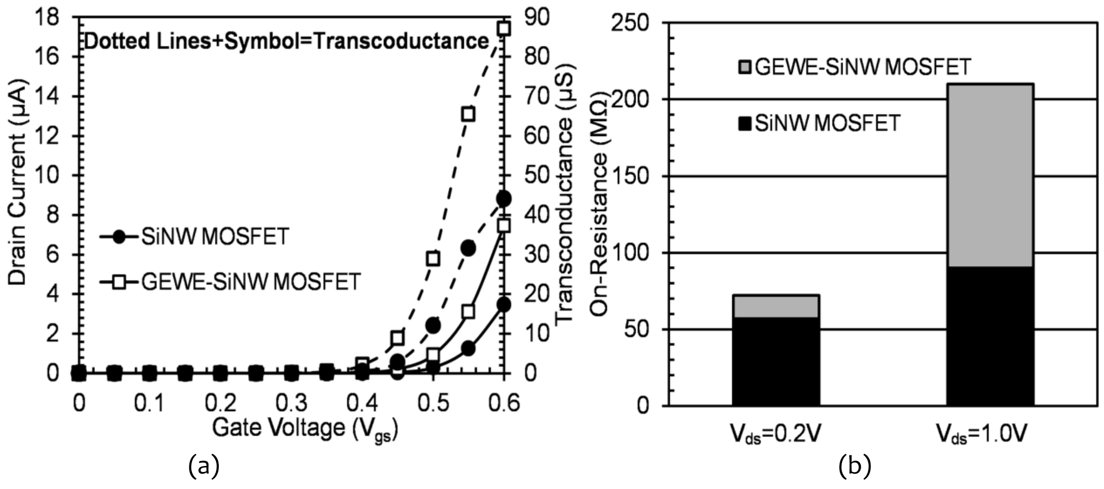


Figure 2.04: (a) Transfer and Transconductance characteristics of SiNW and GEWE-SiNW MOSFET at V_{ds}=0.4 V respectively. (b) On-resistance of SiNW and GEWE-SiNW MOSFET in active and a saturation region (Gupta et al, 2015b).

It is clearly evident from Fig. 2.04(a) that transconductance of GEWE-SiNW is higher in comparison to conventional SiNW MOSFET due to enhanced on-current. CMOS is commonly used as a switch in the linear region, and in the saturation region it can be used as an amplifier due to high on-resistance which results significant gain for the amplifier. Fig. 2.04(b) clearly shows that in linear and saturation regions, GEWE-SiNW MOSFET exhibits smaller and higher on-resistance respectively compared to SiNW MOSFET. Fig. 2.05 (a) shows the variation of conduction band and valence band along the channel length for conventional MOSFET, SiNW and GEWE SiNW

MOSFET at V_{gs}=0.37V and V_{ds}=0.55V. As shown in Fig. 2.05(a), the significant barrier lowering just below the gate in conventional MOSFET leads to leakage current. The improvement in DIBL effect in GEWE is due to the step in conduction band energy in the channel region, owing from metal gate workfunction difference. In SiNW and GEWE-SiNW, there is improved gate controllability over the channel due to cylindrical gate design and hence DIBL is significantly lowered as shown in Fig.2.05 (b) in comparison to conventional MOSFET. V_{ds}=0.1V is used as a reference for calculating barrier lowering in all three devices.

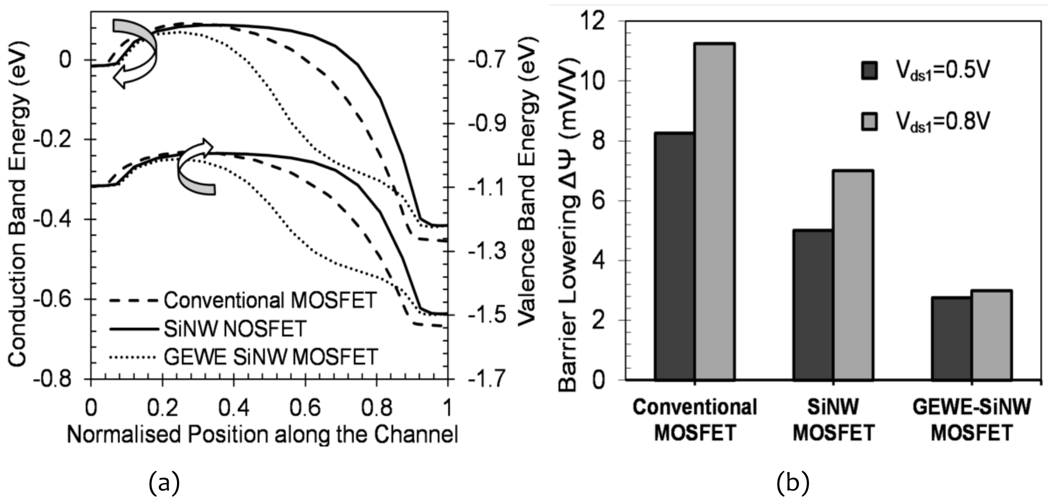


Figure 2.05: (a) Conduction band energy and Valence band energy variation along the channel for V_{gs}=0.4V for Conventional, SiNW and GEWE-SiNW MOSFET at V_{ds}=0.6 V (b) DIBL versus V_{ds} variation for Conventional, SiNW and GEWE-SiNW MOSFET at V_{gs}=0V for two different values of V_{ds1} (Gupta et al, 2015b).

Moreover, with an increase in the drain to source bias, the DIBL effect increases, but this increase is more prominent in conventional MOSFET in comparison to the GEWE-SiNW. The DIBL is calculated as follows:

$$DIBL = \frac{V_{Th1} - V_{Th0}}{V_{ds1} - V_{ds0}} \quad \text{.... (2.3)}$$

where V_{Th1} is the threshold voltage of device when V_{ds1} bias is applied and V_{Th0} is the threshold voltage of device when reference bias voltage i.e. V_{ds0}=0.1V is applied.

Fig.2.06 predicts the variation of electron temperature along the channel length from source to drain for conventional, SiNW and GEWE-SiNW MOSFET. As is evident from the results, a considerable reduction in electron temperature for GEWE- SiNW at the drain side is observed which is due to a decrease in the electric field at the drain side, which in turn reduces the leakage current and hence improves hot carrier immunity in comparison to conventional MOSFET.

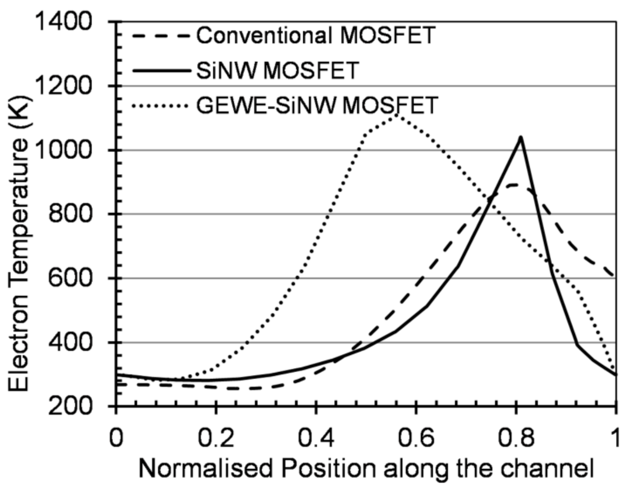


Figure 2.06: Electron temperature variation along the channel for Conventional, SiNW and GEWE-SiNW MOSFET at V_{ds}=0.6 V, V_{gs}=0.4V (Gupta et al, 2015b)

The reduction in the electric field at drain side in GEWE-SiNW is because of GEWE scheme, which causes a step in potential profile at the interface of two metal gates (Long & Chin, 1997). The gate current of conventional MOSFET is comparatively higher than SiNW MOSFET because of short channel effects which exist in conventional MOSFET. Hot-Electron (HE)-Injection Gate Current (I_g) is a key

parameter to evaluate the hot-carrier reliability of the device. It is due to the injection of hot-carriers into the oxide and transport of these carriers towards the gate electrode. Fig.2.07 shows the HE-I_g of conventional, SiNW and GEWE-SiNW MOSFET at V_{ds}=0.55V. HE-I_g in SiNW MOSFET is reduced significantly in comparison to GEWE-SiNW since GEWE favors high electric field in the channel because of step potential profile due to dissimilar metal gates in the channel, which causes tunneling of electrons from channel to gate oxide causing gate tunneling current thereby increasing HE-I_g in comparison to SiNW MOSFET.

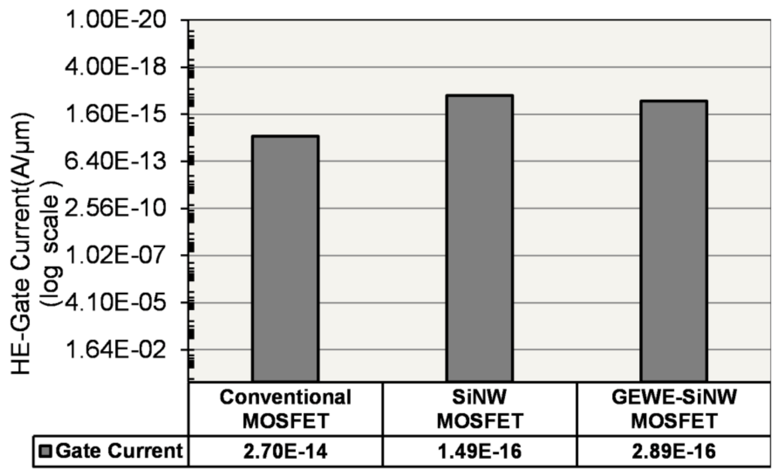


Figure 2.07: HE gate current for conventional MOSFET, SiNW and GEWE-SiNW MOSFET at V_{ds}=0.6V (Gupta et al, 2015b).

To improve the carrier transport efficiency in the channel, the carrier velocity near the source should be more than near the drain. Fig.2.08 predicts the electron velocity of conventional, SiNW and GEWE-SiNW MOSFET along the channel. Higher electron velocity (3.59×10^7 cm/s) near the source side is obtained for GEWE-SiNW in contrast to 3.5×10^7 cm/s and 0.9×10^7 cm/s obtained for SiNW and conventional MOSFET respectively as shown in Fig.2.08 enhancing the source carrier injection into the

channel and hence results in hot carrier immunity in GEWE-SiNW MOSFET. For low-power and low-voltage analog circuit applications, lower electron velocity near the drain end is an important design parameter.

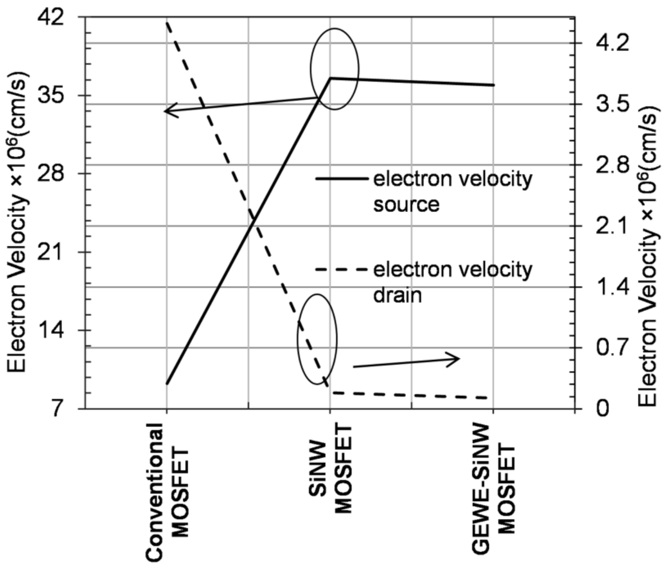


Figure 2.08: Electron velocity for source and drain side for conventional MOSFET, SiNW and GEWE-SiNW MOSFET at V_{ds}=0.6V, V_{gs}=0.4 (Gupta et al, 2015b).

2.4.1 Effect of Gate Oxide Thickness

In this subsection, the influence of scaling the oxide thickness is examined in terms of Hot-Carrier FOMs. Fig.2.09 (a) shows the variation of conduction band energy of GEWE-SiNW MOSFET with the normalized position along the channel. The result shows that as we scale down the oxide thickness from 0.5 to 2.5nm, step in conduction band profile increases and hence results in lowering of DIBL as is indicated in Fig.2.09 (b). It is clearly manifest from the figure that when oxide thickness is 0.5nm, barrier lowering is 13.9 mV/V compared to 24.3mV/V at 2.5nm, thereby reflecting significant improvement in SCEs at the sub-nm range.

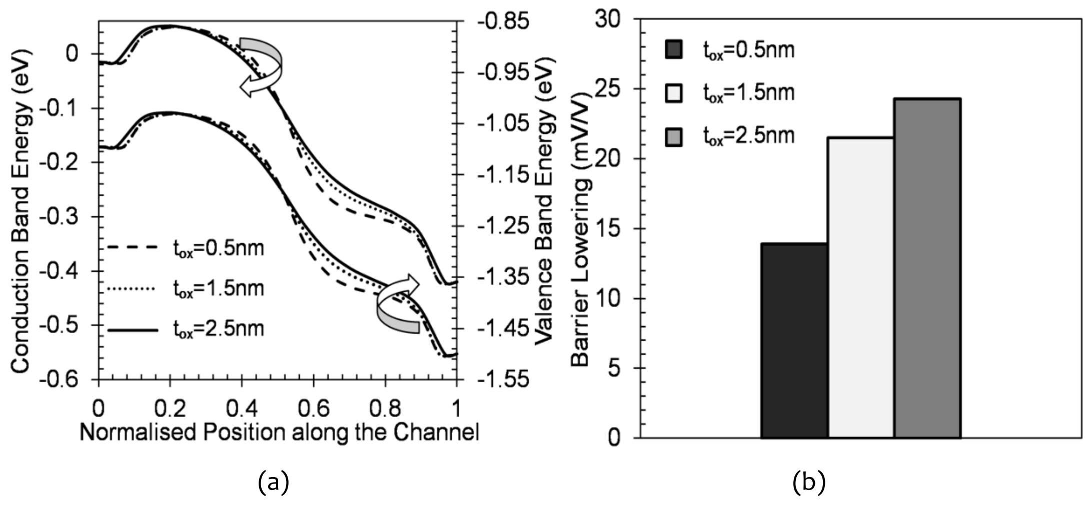


Figure 2.09: (a) Conduction Band Profile for GEWE-SiNW MOSFET at different values of oxide thickness. (b) Barrier Lowering for GEWE-SiNW MOSFET at different values of oxide thickness (Gupta et al, 2015b).

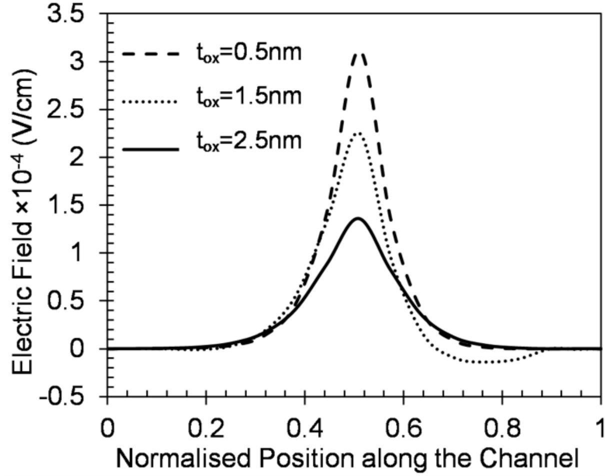


Figure 2.10: Electric Field for GEWE-SiNW MOSFET at different values of oxide thickness (Gupta et al, 2015b)

Fig.2.10 depicts the variation of the electric field of GEWE-SiNW MOSFET at different oxide thickness. The drain electric field reduces as oxide thickness decreases due to the incorporation of lower workfunction of the metal gate and thinning of gate oxide, which results in less number of hot-carriers at the drain end and thus improves

the hot-carrier reliability of the device. Also, as shown in the figure 2.10, the peak electric field in the channel increases due to the difference in metal gate workfunction, which results in improvement in the electron velocity and thus enhances the carrier efficiency.

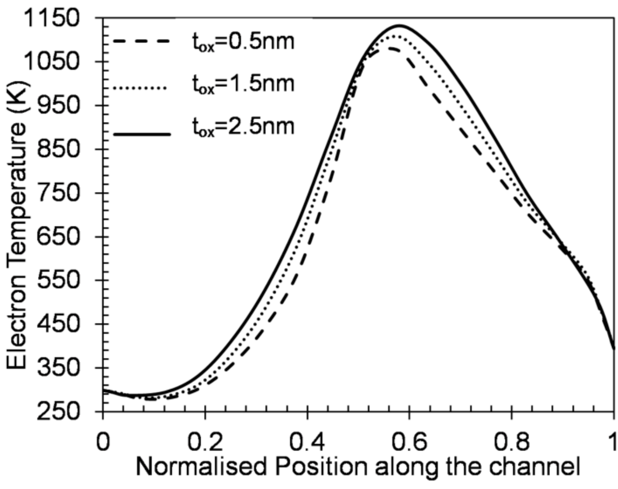


Figure 2.11: Electron Temperature for GEWE-SiNW MOSFET for V_{gs}=0.6V and V_{ds}=0.4 at different values of oxide thickness (Gupta et al, 2015b).

Fig.2.11 depicts a noticeable reduction in electron temperature of GEWE-SiNW MOSFET at the drain end as we scale down the oxide thickness. This is due to lessening in the electric field at the drain end, which results in less number of hot-carriers and thus lowers the temperature, which accounts for improvement in hot-carrier reliability. Fig.2.12 shows the effect of oxide thickness on electron velocity of GEWE-SiNW MOSFET. To upgrade the carrier efficiency, electron velocity near the source end should be greater than the velocity near the drain end. Results depicted that electron velocity at source side is 0.63×10^7 cm/s for a 1.5nm oxide thickness in contrast to 0.3×10^7 cm/s for 2.5nm, thereby enhancing the carrier injection into the channel.

Further scaling down of the oxide thickness to 0.5nm results in improvement in electron velocity near the source (1.2×10^7 cm/s), due to improved gate controllability over the channel and effectiveness of dual material gate, hence leading to improvement in carrier efficiency and driving current capability of the device.

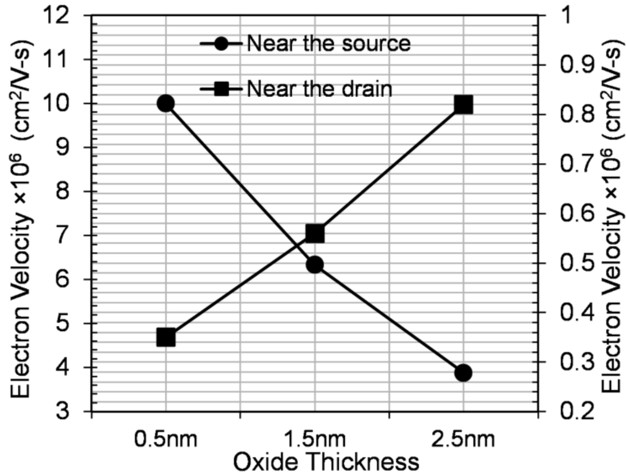


Figure 2.12: Electron velocity for source and drain side for GEWE-SiNW MOSFET for V_{gs}=0.6V and V_{ds}=0.4 at different values of oxide thickness (Gupta et al, 2015b).

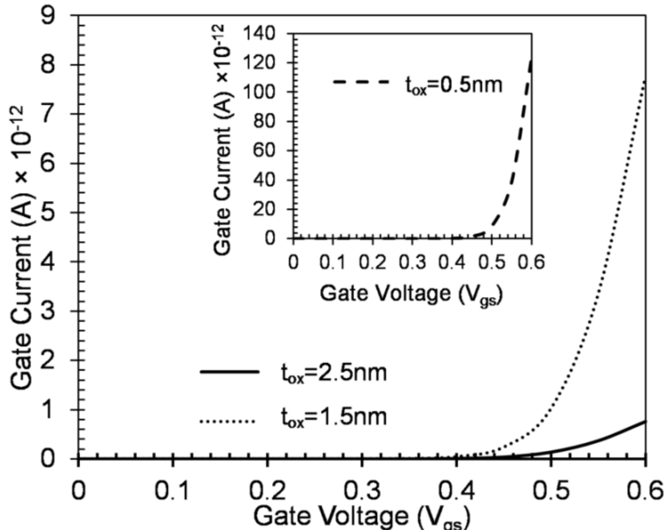


Figure 2.13: Hot-Electron Injection Gate Current for GEWE-SiNW MOSFET at different values of oxide thickness (Gupta et al, 2015b).

Further, Fig.2.12 also validates a lower electron velocity of 0.35×10^7 cm/s at the drain end for 0.5nm thickness in contrast to 0.56×10^7 cm/s and 0.82×10^7 cm/s for 1.5 and 2.5nm respectively, thus imparting outstanding hot-carrier immunity. Fig.2.13 depicts the variation of gate current as a function of the gate to source voltage. It is observed as oxide thickness goes on decreasing from 2.5 to 0.5nm, gate current increases owing to tunneling of electrons through the gate oxide which causes a rise in gate current and thus hampers the device performance.

2.4.2 Effect of Dielectric Constant (High-k)

As discussed in the previous section, with scaling of oxide thickness below 1.5nm, such an ultra-thin gate oxide will induce a high direct tunneling current (leakage gate current) which hampers the device performance and therefore, it is required for the high dielectric constant (k) material to replace SiO_2 as a gate dielectric to reduce standby power dissipation.

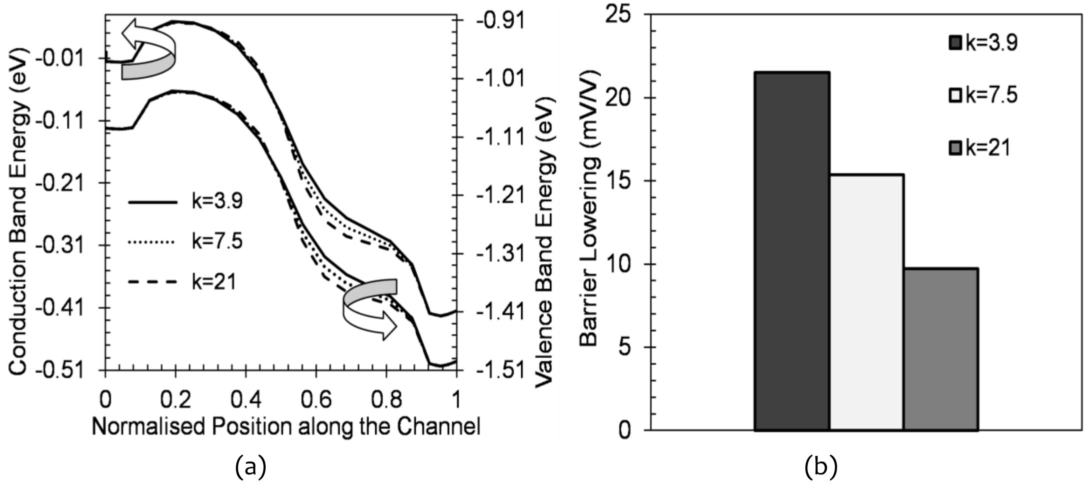


Figure 2.14: (a) Conduction band and Valence band energy variation along the channel for GEWE-SiNW MOSFET at different values of oxide thickness. (b) DIBL variation for GEWE-SiNW MOSFET for V_{gs}=0.6V and V_{ds}=0.4 at various values of High-k (Gupta et al, 2015b).

In this subsection, effect of different high-k materials on hot-carrier reliability of GEWE-SiNW MOSFET has been examined by keeping gate oxide thickness as 1.5nm. Fig. 2.14 (a) shows the variation of conduction band energy of GEWE-SiNW MOSFET at different values of high-k. As the value of dielectric constant increases, the step in conduction band profile increases due to metal gate workfunction difference and also due to increased gate capacitance, thus providing an enhancement in DIBL. DIBL is significantly reduced as value of high-k dielectric increases as is shown in Fig.2.14 (b), thereby reflecting SCE immunity. Fig.2.15 shows the variation of electric field with normalized position along the channel for GEWE-SiNW MOSFET. It is evident from the figure that the peak electric field at the interface of two metal gates increases with increase in dielectric constant of high-k oxide, which results in an improvement in average velocity of carriers.

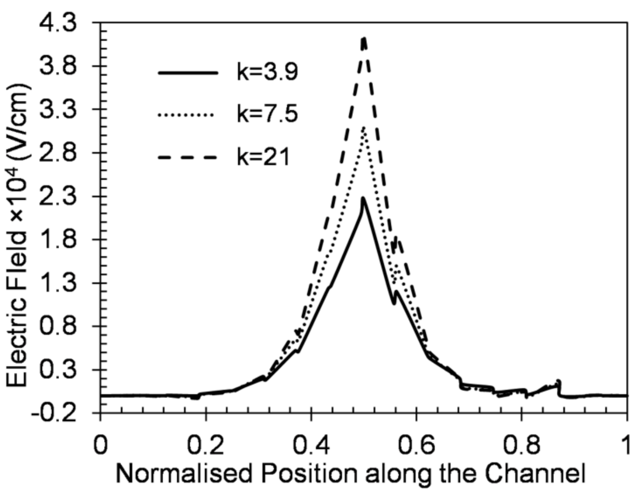


Figure 2.15: Electric field for GEWE-SiNW MOSFET at different values of High-k (Gupta et al, 2015b).

In addition, there is a prominent reduction in field at the drain end due to incorporation of lower metal workfunction at the drain end and due to the fact that gate capacitance is directly proportional to dielectric constant. As the dielectric

constant increases the gate capacitance increases the control of gate on the channel and therefore, enhances the driving capability of device, hereby reducing field at the drain end. Electron temperature in the channel decreases with increase in high k value as is evident from Fig.2.16. As carriers move from source to drain, carrier temperature gradient is reduced significantly giving a remarkable reduction in electron temperature to 980K for HfO_2 in comparison to 1018K for SiO_2 as shown in Fig.2.16, due to increased gate controllability of device and reduction of the field at the drain end which results in enhancement of hot-carrier reliability.

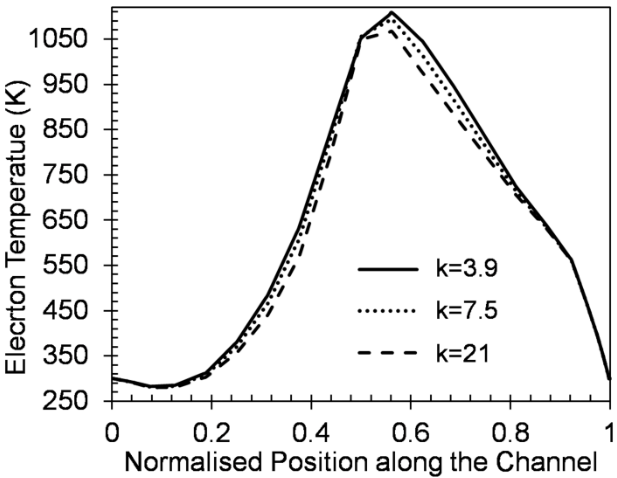


Figure 2.16: Electron Temperature variation along the channel for GEWE-SiNW MOSFET for V_{gs}=0.6V and V_{ds}=0.4 at different values of High-k (Gupta et al, 2015b) .

Fig. 2.17 demonstrates the electron velocity of GEWE-SiNW MOSFET at different values of dielectric constant. It is evident from the result, as dielectric constant increases from 3.9 to 21, electron velocity at source increases and decreases near drain end due to enhancement in electric field in the channel which improves the carrier efficiency and reliability of device at low power applications.

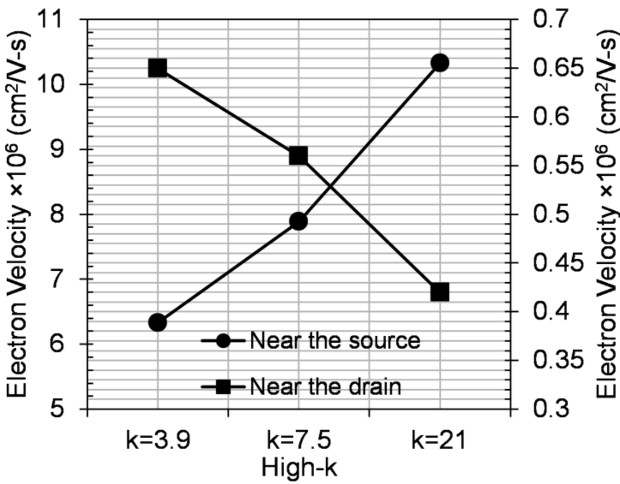


Figure 2.17: Electron velocity for source and drain side for GEWE-SiNW MOSFET for V_{gs}=0.6V and V_{ds}=0.4 at different values of High-k (Gupta et al, 2015b).

Fig.2.18 shows the HE-I_g of GEWE-SiNW MOSFET at V_{ds}=0.4V. It is clearly shown that with the incorporation of HfO_2, gate current (7.77×10^{-16} A/μm) decreases appreciably in comparison to SiO_2 (6.35×10^{-15} A/μm). This reduction in gate current is due to large gate capacitance which inhibits the tunneling of electrons at 1.5nm oxide thickness, thus reducing the power dissipation and hence finds its efficacy in low power analog applications.

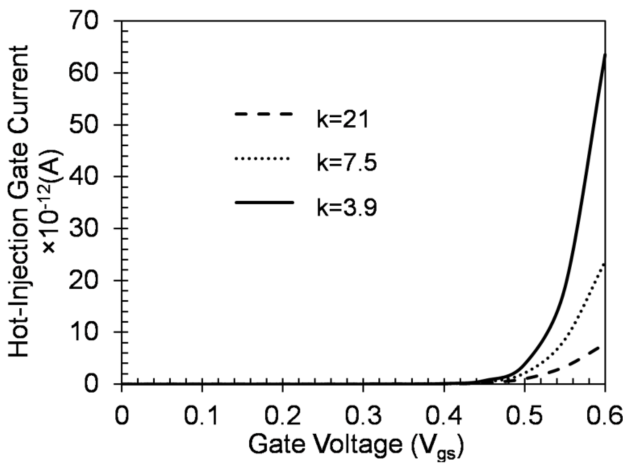


Figure 2.18 Hot-Electron Injection Gate Current for GEWE-SiNW MOSFET at various values of High-k (Gupta et al, 2015b).

Further, the hot-carrier reliability metrics values for three different oxide thickness and dielectric values are listed in Table 2.02.

Table 2.02: Extracted parameters at different values of oxide thickness and high-k

Permittivity value	Parameters		Oxide Thickness (t_{ox}) 0.5nm	1.5nm	2.5nm
k=3.8 (SiO_2)	Electric Field ($\times10^4$ V/cm)	Near Source	3.11	2.25	1.36
		Near Drain	0.3	0.86	0.9
	Gate Current($\times10^{-16}$ A/µm)		123	7.77	0.75
	Electron temperature(K)		1043	1108	1131
	Electron Mobility(cm^2/V-s)		1092	1020	897
	Electron Velocity ($\times10^7$ cm/s)	Near Source	0.99	0.634	0.38
		Near Drain	0.035	0.056	0.082
k=7.5 (Si_3N_4)	Electric Field ($\times10^4$ V/cm)	Near Source	3.66	3.0	1.98
		Near Drain	0.2	0.22	0.24
	Gate Current($\times10^{-16}$ A/µm A)		0.8	2.36	7.6
	Electron temperature(K)		1062.1	1091	1135.0
	Electron Mobility(cm^2/V-s)		1112.1	1018	915.2
	Electron Velocity ($\times10^7$ cm/s)	Near Source	1.2	0.78	0.56
		Near Drain	0.013	0.056	0.004
k=21 (HfO_2)	Electric Field ($\times10^4$ V/cm)	Near Source	4.12	4.15	2.92
		Near Drain	0.016	0.012	0.029
	Gate Current(A)		0.55	0.7	1.2
	Electron temperature(K)		1047	1065	1116.6
	Electron Mobility(cm^2/V-s)		1127	1066	962
	Electron Velocity ($\times10^7$ cm/s)	Near Source	1.33	1.55	0.82
		Near Drain	0.0108	0.042	0.0105

2.5 SUMMARY

In this chapter, first and foremost the performance of GEWE-SiNW MOSFET is examined by implicating the three different transport models i.e., classical Drift Diffusion Model (DDM) and semi-quantum transport models i.e., Energy Balance (EBM) and Hydrodynamic Model (HDM). It is observed that DDM fails when device length goes to sub-micrometer range since it neglects the non-linear effects and carrier diffusions. However, in case of HDM, high electric field peak in channel region and lowering of mobility at the drain makes it appropriate for sub-micron device. In addition, high $I_{on/off}$ ratio of GEWE-SiNW in case of HDM makes it suitable for low power switching applications. For the exact analysis of short channel MOSFETs such as heat flow analysis and thermal diffusion effects, both carrier and lattice energy transport equations should be solved. Hence, both EB and HD model needs to be considered for such applications. In addition to the effective suppression of short channel effects due to the improved gate strength, the GEWE-SiNW MOSFET show excellent current drive and has the merit that it is compatible with conventional CMOS processes.

In the second part of chapter, GEWE-SiNW MOSFET is proposed for improved hot carrier reliability applications over conventional and SiNW MOSFET. The reduction in electron velocity and temperature near the drain end is achieved with GEWE-SiNW MOSFET which reflects its effectiveness in high-performance applications where device reliability is a major concern. Besides, notable reduction in SCEs such as DIBL in GEWE-SiNW increases its current drive ability and also there is significant reduction in HE-I_g in GEWE-SiNW MOSFET compared to conventional

MOSET, which results in improving its standby power consumption in electrical appliances and logic gates. Further, the scaling of oxide thickness shows an outstanding performance by GEWE-SiNW MOSFET with an exception of high HE-Ig at 0.5 nm. With incorporation of high-k, HE-Ig reduces significantly and improves the device reliability at 300 K. Thus, an oxide thickness 0.5 nm and oxide dielectric 21 (HfO_2) with GEWE-SiNW MOSFET is an effective candidate for low power CMOS applications such as amplifiers and switching applications. After assessing the device hot-carrier reliability and analog performance of GEWE-SiNW MOSFET, the next chapter discusses the high frequency analysis of GEWE-SiNW MOSFET with an aim to analyse its effectiveness at RF applications. The influence of device parameters such as channel length, oxide thickness, radius of nanowire and gate metal engineering is also discussed in the next chapter.

2.6 REFERENCES

Arora, N. (1993) MOSFET Models for VLSI Circuit Simulation Theory and Practice Springer. *New York*.

Barsan, R. M. (1981) Analysis and modeling of dual-gate MOSFET's. *IEEE Transactions on Electron Devices*, 28(5), 523-534.

Chen, X. & Tan, C. M. (2014) Modeling and analysis of gate-all-around silicon nanowire FET. *Microelectronics Reliability*, 54(6), 1103-1108.

De, V. & Borkar, S. (1999) Technology and design challenges for low power and high performance, *Proceedings of the 1999 international symposium on Low power electronics and design*. ACM.

Deb, S., Singh, N. B., Islam, N. & Sarkar, S. K. (2012) Work function engineering with linearly graded binary metal alloy gate electrode for short-channel SOI MOSFET. *IEEE Transactions on Nanotechnology*, 11(3), 472-478.

Dubey, S., Santra, A., Saramekala, G., Kumar, M. & Tiwari, P. K. (2013) An analytical threshold voltage model for triple-material cylindrical gate-all-around (TM-CGAA) MOSFETs. *IEEE Transactions on Nanotechnology*, 12(5), 766-774.

Groeseneken, G. V. (2001) Hot carrier degradation and ESD in submicrometer CMOS technologies: How do they interact? *IEEE transactions on device and materials reliability*, 1(1), 23-32.

Gupta, N. & Chaujar, R. (2014) Implications of transport models on the analog performance of Gate Electrode Workfunction Engineered (GEWE) Silicon Nanowire MOSFET, *Devices, Circuits and Systems (ICDCS), 2014 2nd International Conference on*. IEEE.

Gupta, N., Kumar, A. & Chaujar, R. (2015) Oxide bound impact on hot-carrier degradation for gate electrode workfunction engineered (GEWE) silicon nanowire MOSFET. *Microsystem Technologies*, 1-10.

Iwai, H., Natori, K., Shiraishi, K., Iwata, J.-i., Oshiyama, A., Yamada, K., Ohmori, K., Kakushima, K. & Ahmet, P. (2011) Si nanowire FET and its modeling. *Science China information sciences*, 54(5), 1004-1011.

Jeon, H., Kim, Y.-B. & Choi, M. (2010) Standby leakage power reduction technique for nanoscale CMOS VLSI systems. *IEEE transactions on instrumentation and measurement*, 59(5), 1127-1133.

Kaur, R., Chaujar, R., Saxena, M. & Gupta, R. (2007) Hot-carrier reliability and analog performance investigation of DMG-USEGas MOSFET. *IEEE transactions on electron devices*, 54(9), 2556-2561.

Kranti, A. & Armstrong, G. A. (2006) Engineering source/drain extension regions in nanoscale double gate (DG) SOI MOSFETs: Analytical model and design considerations. *Solid-state electronics*, 50(3), 437-447.

Krieger, G., Sikora, R., Cuevas, P. & Misheloff, M. (1991) Moderately doped NMOS (M-LDD)-hot electron and current drive optimization. *IEEE Transactions on Electron Devices*, 38(1), 121-127.

Lee, J.-H., Kim, B.-S., Choi, S.-H., Jang, Y., Hwang, S. W. & Whang, D. (2013) A facile route to Si nanowire gate-all-around field effect transistors with a steep subthreshold slope. *Nanoscale*, 5(19), 8968-8972.

Liu, J., Wen, H., Lu, J. & Kwong, D.-L. (2005) Dual-work-function metal gates by full silicidation of Poly-Si with Co-Ni bi-layers. *IEEE electron device letters*, 26(4), 228-230.

Long, W. & Chin, K. K. (1997) Dual material gate field effect transistor (DMGFET), *Electron Devices Meeting, 1997. IEDM'97. Technical Digest., International*. IEEE.

Long, W., Ou, H., Kuo, J.-M. & Chin, K. K. (1999) Dual-material gate (DMG) field effect transistor. *IEEE Transactions on Electron Devices*, 46(5), 865-870.

Mikolajick, T. & Weber, W. M. (2015) Silicon Nanowires: Fabrication and Applications, *Anisotropic Nanomaterials*Springer, 1-25.

Moon, D.-I., Choi, S.-J., Duarte, J. P. & Choi, Y.-K. (2013) Investigation of silicon nanowire gate-all-around junctionless transistors built on a bulk substrate. *IEEE Transactions on Electron Devices*, 60(4), 1355-1360.

Mukherjee, C. & Maiti, C. (2012) *Silicon Nanowire FinFETs*INTECH Open Access Publisher.

Na, K.-Y. & Kim, Y.-S. (2006) Silicon complementary metal–oxide–semiconductor field-effect transistors with dual work function gate. *Japanese journal of applied physics*, 45(12R), 9033.

Orouji, A. A. & Kumar, M. J. (2005) Shielded channel double-gate MOSFET: a novel device for reliable nanoscale CMOS applications. *IEEE transactions on device and materials reliability*, 5(3), 509-514.

Pan, Y., Ng, K. & Wei, C. (1994) Hot-carrier induced electron mobility and series resistance degradation in LDD NMOSFET's. *IEEE electron device letters*, 15(12), 499-501.

Polishchuk, I., Ranade, P., King, T.-J. & Hu, C. (2001) Dual work function metal gate CMOS technology using metal interdiffusion. *IEEE Electron Device Letters*, 22(9), 444-446.

Rustagi, S., Singh, N., Fang, W., Buddharaju, K., Omampuliyur, S., Teo, S., Tung, C., Lo, G., Balasubramanian, N. & Kwong, D. (2007) CMOS inverter based on gate-all-around silicon-nanowire MOSFETs fabricated using top-down approach. *IEEE Electron Device Letters*, 28(11), 1021-1024.

Sharma, D. & Vishvakarma, S. K. (2013) Precise analytical model for short channel cylindrical gate (CylG) gate-all-around (GAA) MOSFET. *Solid-State Electronics*, 86, 68-74.

Shirak, O., Shtempluck, O., Kotchtakov, V., Bahir, G. & Yaish, Y. (2012) High performance horizontal gate-all-around silicon nanowire field-effect transistors. *Nanotechnology*, 23(39), 395202.

SILVACO, I. (2016) ATLAS User's Manual. *Santa Clara, CA, Ver*, 5.

Sohn, C.-W., Kang, C. Y., Baek, R.-H., Choi, D.-Y., Sagong, H. C., Jeong, E.-Y., Baek, C.-K., Lee, J.-S., Lee, J. C. & Jeong, Y.-H. (2012) Device design guidelines for nanoscale FinFETs in RF/analog applications. *IEEE Electron Device Letters*, 33(9), 1234-1236.

Stratton, R. (1972) Semiconductor current-flow equations (diffusion and degeneracy). *IEEE Transactions on Electron Devices*, 19(12), 1288-1292.

Suk, S. D., Lee, S.-Y., Kim, S.-M., Yoon, E.-J., Kim, M.-S., Li, M., Oh, C. W., Yeo, K. H., Kim, S. H. & Shin, D.-S. (2005) High performance 5 nm radius twin silicon nanowire MOSFET (TSNWFET): Fabrication on bulk Si wafer, characteristics, and reliability. *IEDM Tech. Dig*, 717-720.

Venkatesan, S., Neudeck, G. W. & Pierret, R. F. (1992) Dual-gate operation and volume inversion in n-channel SOI MOSFET's. *IEEE electron device letters*, 13(1), 44-46.

Wang, R., Zhuge, J., Huang, R., Tian, Y., Xiao, H., Zhang, L., Li, C., Zhang, X. & Wang, Y. (2007) Analog/RF performance of Si nanowire MOSFETs and the impact of process variation. *IEEE transactions on Electron Devices*, 54(6), 1288-1294.

Wang, T., Lou, L. & Lee, C. (2013) A junctionless gate-all-around silicon nanowire FET of high linearity and its potential applications. *IEEE Electron Device Letters*, 34(4), 478-480.

Yang, B., Buddharaju, K., Teo, S., Singh, N., Lo, G. & Kwong, D. (2008) Vertical silicon-nanowire formation and gate-all-around MOSFET. *IEEE Electron Device Letters*, 29(7), 791-794.

Yang, G., Wang, S. & Wang, R. (2003) An efficient preconditioning technique for numerical simulation of hydrodynamic model semiconductor devices. *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*, 16(4), 387-400.

Yu, B., Wann, C. H., Nowak, E. D., Noda, K. & Hu, C. (1997) Short-channel effect improved by lateral channel-engineering in deep-submicronmeter MOSFET's. *IEEE Transactions on Electron Devices*, 44(4), 627-634.

Zheng, C.-y. (2011) The using of dual-material gate MOSFET in suppressing short-channel effects: a review, *Electronics, Communications and Control (ICECC), 2011 International Conference on*. IEEE.

CHAPTER-3

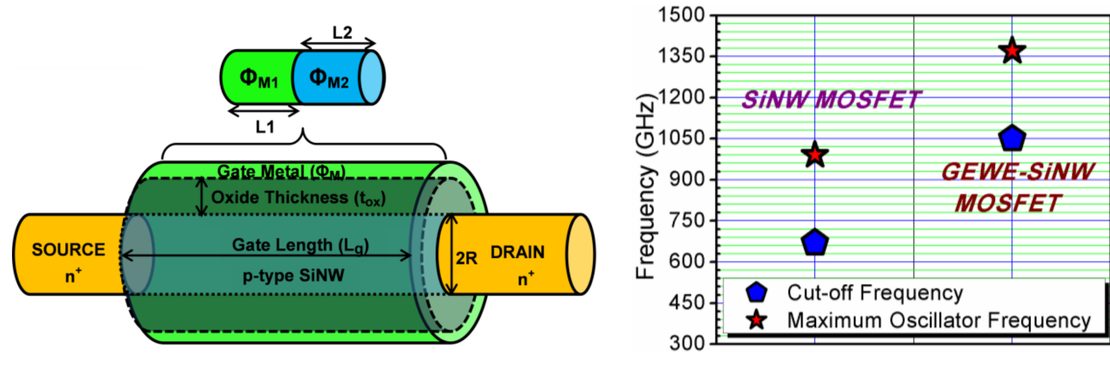
Impact of Device Parameter Variation on RF Performance of Gate Electrode Workfunction Engineered (GEWE) Silicon Nanowire (SiNW) MOSFET

☞ *In this chapter, quantitative investigation of high-frequency performance of GEWE-SiNW MOSFET has been explored and compared with SiNW MOSFET using device simulators: ATLAS and DEVEDIT 3D.*

☞ *Significant enhancement in f_T and f_{MAX} is observed; and a reduction in switching time in GEWE-SiNW MOSFET due to alleviated short channel effects (SCEs), improved drain current and smaller parasitic capacitance has been obtained.*

☞ *Further, we have also examined the efficacy of parameter variations in terms of oxide thickness, radius of silicon nanowire, channel length and gate metal workfunction engineering on RF/microwave figure of merits of GEWE-SiNW MOSFET.*

☞ *Thus, detailed knowledge is provided about the device's RF performance at such aggressively scaled dimensions*



3.1 INTRODUCTION

Silicon based transistors have become an appealing low cost solution for many low power and high frequency applications such as mobile telecommunication. The relentless scaling of CMOS toward nanometer-scale gate lengths has produced MOSFETs with digital and RF performance that is suitable for mixed signal applications (Enz, 2002; Larson, 2003; Saijets et al, 2002; Woerlee et al, 2001). However, scaling down arises the so-called SCEs such as mobility degradation, hot carrier effects, drain induced barrier lowering, parasitic capacitances etc. making the scaled devices inapt for RF/wireless applications (Chen, 2013). To surpass these hindrances, new device architectures with 3-D gate structures have been intensively studied. Among them, cylindrical gate MOSFET (Jimenez et al, 2005) has emerged as a most promising candidate in recent years. Recently, many theoretical and experimental studies on cylindrical gate MOSFET have been reported in literature to eliminate SCEs, to achieve high transconductance and nearly ideal Subthreshold slope i.e., 60 mV/decade (Gupta & Baishya, 2013; Sharma & Vishvakarma, 2013). It allows excellent electrostatic control of the gate over the channel hence overcoming the scaling limitations caused due to the SCEs, thereby improving the device performance. Further, Silicon nanowire emerged as a most promising in electronic devices due to the fact that its properties such as concentration, dopant type can be changed during synthesis. Also, its mobility is higher than bulk silicon due to stronger quantum confinement. The body thickness (diameter) of the nanowire can readily be reduced to a few nanometers in size scale that is challenging to obtain using bulk silicon. Therefore, to get further improvement against SCEs the concept of silicon

nanowire MOSFET was put forward by Cui et al. (Cui et al, 2003) in 2003 concluded that silicon nanowires MOSFET as building blocks for future nano-electronics. Also, the small volume and low leakage current of nanowire MOSFETs make them attractive for high density memory arrays and logic chips (Fu et al, 2008; Rustagi et al, 2007). Yang et al. (Yang et al, 2008) fabricated vertical gate-all-around silicon nanowire MOSFET and showed excellent transistor characteristics compared to conventional devices. Also it was proven that it has a merit of outstanding maximum oscillation frequency (f_{MAX}) (Wang et al, 2007). In 1989, Shur introduced the notion of split gate which escalate the carrier transport efficiency of device (Shur, 1989). But the misalignment of two gates during fabrication and fringing capacitances between the gates limits the device speed. Hence, to overcome this drawback, gate electrode workfunction engineering scheme was proposed by Zhou and Long (Long & Chin, 1997) in 1999. With this scheme, there is appreciable reduction in the SCEs, improvement in current capabilities due to two dissimilar metal gates and reduction in electric field at the drain end thus providing hot-carrier reliability (Zheng, 2011). Pal et al. (Pal & Sarkar, 2014) reported a 2-D analytical drain current model of DMG-GAA MOSFET which employs gate material engineering scheme to reduce SCEs. To incorporate the advantage of gate electrode engineering scheme, combined with silicon nanowire MOSFET, a novel device structure called gate electrode workfunction engineered (GEWE) silicon nanowire (SiNW) MOSFET is proposed (Gupta & Chaujar, 2014; Zhou et al, 2011). As it has been studied in previous chapter, the GEWE-SiNW is immune to SCEs mainly hot-carrier, DIBL and improved analog behaviour of GEWE-SiNW MOSFET has also examined. Moreover, due to the

increased demand for high-speed electronics products, the accurate analysis of MOSFET at high frequencies (HF) is necessary to represent the behavior of device in microwave circuits and systems (Doan et al, 2005). However, the reported work mentioned above (about GAA MOSFET) does not discuss about the Quantum RF behaviour and the impact of device parameter variation especially radius, length and oxide thickness. Therefore, in this paper, for the first time, the quantum 3D-numerical simulation of GEWE-SiNW MOSFET has been carried out in terms of RF FOMs to study the effect of HF (GHz) on the performance of GEWE-SiNW MOSFET and simulations results so obtained are compared with the conventional SiNW MOSFET. Further, Section 3.2 of the chapter describes the device structure and its default parameters followed by quantum simulation methodology invoked during this analysis. Section 3.3 contains the results obtained by device variation and also explores the dependency of GEWE-SiNW MOSFET's performance on metal workfunction at the drain end, gate oxide thickness, channel length and radius of silicon nanowire which would be indispensable for optimizing the device designs at millimeter range frequency.

3.2 DEVICE STRUCTURE: PARAMETERS AND SIMULATION MODELS

Figure 3.01 shows the simulated 3D device structure of GEWE-SiNW MOSFET. All simulations have been performed using ATLAS and DEVEDIT 3D device simulator. The Source/Drain region is highly doped with n-type impurity of a length of 5 nm. The SiNW is doped with a p-type impurity and a thick oxide layer t_{ox} is embodied in it as shown in Fig. 3.01. In order to fairly analyze the device performance, both the devices are optimized to have the same threshold voltage, i.e., 0.4V.

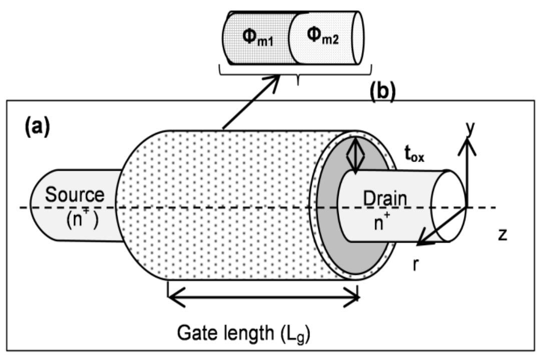


Figure 3.01: Simulated 3-D structure of GEWE-SiNW MOSFET. Default device parameters are: Channel Length (L_g)=30nm, Oxide thickness (t_{ox})=1.5nm, Radius of Silicon pillar (R)=5nm, Source/Drain Doping (N_D)=5x10^{19} cm^{-3}, Channel Doping (N_A)=1x10^{16} cm^{-3}, Gate Metal workfunction (Φ_{M1})=4.8 eV, Gate Metal workfunction (Φ_{M2})=4.4 eV (Gupta et al, 2015a)

Table 3.01: Default design parameters used in the analysis

DESIGN PARAMETERS of SiNW and GEWE-SiNW MOSFET DEVICE DESIGN	
Channel Length (L_g)	30nm
Substrate Doping (N_A)	1x10^{16} cm^{-3}
Radius of Nanowire (R)	5nm
Source/Drain Doping (N_D^+)	5x10^{19} cm^{-3}
Physical Oxide Thickness (t_{ox})	1.5nm
Permittivity of SiO_2 (ε_{ox})	3.9
Gate to Source voltage (V_{gs})	0.7V
Drain to Source voltage (V_{ds})	0.2V
Work function for SiNW-MOSET (Φ_m)	4.8eV
Work function for GEWE-SiNW MOSFET	Φ_{m1}=4.8eV [Gold] Φ_{m2}=4.4eV [Titanium]
The design parameters as discussed above are the default parameters used in the analysis, unless otherwise stated.	

In this simulation, all the junctions of the structure are assumed to be abrupt and the biasing conditions are considered at room temperature (T=300K) with the doping profiles being uniform. The detailed description of default parameters used in the simulations is shown in Table 3.01. Further, numerical methods such as biconjugate

gradient stabilized (BICGST) have been considered to obtain the solutions with improved convergence in 3D device structure (SILVACO, 2016). To obtain the convergence in the inversion region, the DIRECT parameter is added for more robust solution.

3.2.1 Simulation Methodology and Calibration

All the simulations have been performed using the models as shown in Table 3.02. It is important to define the carrier transport with proper models to characterize the device performance accurately.

Table 3.02: Simulations Models

S.No.	Physical Models	Description
1.	**Mobility Models**	*Lombardi CVT and Constant Low Field Mobility Model.*
2.	**Recombination Model**	*Shockley Read Hall (SRH)* Recombination is included to incorporate minority recombination effects with carrier lifetime=1×10^{-7}s.
3.	**Statistics**	*Boltzmann Transport model,* The use of Boltzmann statistics is normally justified in semiconductor device theory, but Fermi-Dirac statistics are necessary to account for certain properties of very highly doped (degenerate) materials.
4.	**Impact ionization and Tunneling Model**	No such model is used in current work as we are not interested in evaluating hot-carrier performance.
5.	**Energy Transport Model**	*Hydrodynamic Model* is used as it includes all nonlocal effects and is more accurate than the drift-diffusion method. Drift diffusion Model show short comings as channel length scales down to 50nm.
6.	**Quantum Mechanical Model**	*Quantum Mechanical Model* plays an important role in determining the performance of surrounding gate MOSFET In this paper we take into account QMEs.

The most popular one is drift-diffusion (DD) model, which is widely used in engineering field. For deep submicron device simulation, the hydrodynamic transport

model is commonly used to examine in detail the carrier energy in the carrier transport. It is argued that hydrodynamic model produces the carrier velocity overshoot even in the ballistic regime, which overestimates the drain current level (Yang et al, 2003). Furthermore, the quantum confinement effect in the deep scaled device may not be negligible (Chaudhry & Roy, 2010). This is because the inversion charge layer thickness in the conducting silicon nanowire channel is comparable to the nanowire dimension and hence the quantization effect model is included in the device simulation. The Bohm Quantum Potential (BQP) model (Patnaik et al, 2010) can also be used with energy balance and hydrodynamic models, where the semi-classical potential is modified by the quantum potential in a similar way as for the continuity equations. The model introduces a position dependent quantum potential, Q, which is added to the Potential Energy of a given carrier type. This quantum potential is derived using the Bohm interpretation of quantum mechanics (Iannaccone et al, 2004) and is described below:

Time independent Schrodinger equation can be written as:

$$\left(\frac{-\hbar}{2m^{*}}\nabla^{2} - V\phi\right)\psi_{j} = E_{j}\psi_{j} \quad \text{….. (3.1)}$$

According to Bohm's interpretation of quantum mechanics, the wave function in a polar representation can be written as:

$$\psi = R.\exp\left(\frac{iS}{\hbar}\right) \quad \text{….. (3.2)}$$

where R is the probability density per unit volume and S has dimensions of action (energy×time)

By substituting equation (3.2) in (3.1), the Schrodinger equation can be written as:

$$\frac{\hbar^2}{2}\nabla\left\{M^{-1}\nabla\left[R.\exp\left(\frac{iS}{\hbar}\right)\right]\right\}+V.\mathrm{Re}\,xp\left(\frac{iS}{\hbar}\right)=E.R.\exp\left(\frac{iS}{\hbar}\right) \quad \text{..... (3.3)}$$

where M^{-1} is the inverse of effective mass tensor and $M^{-1}\nabla S$ is local velocity of particle associated to wave function.

Real part of eq. 3.3 is interpreted as continuity equation of probability density while imaginary part states that the total energy, E is conserved and equal to sum of potential (V) and kinetic energy (0.5 $M^{-1}\nabla S$). Therefore, Quantum potential is defined as:

$$V=\frac{-\hbar^2}{2}\frac{\nabla\left(M^{-1}\nabla R\right)}{R} \quad \text{..... (3.4)}$$

Potential V is obtained by the single particle Schrodinger equation and use "*mean field approximation*" and consider an effective quantum Bohm Potential defined as the weighted average potential for all carriers constrained in confining potential.

Effective Quantum Potential is written as:

$$Q_{eff}=\frac{-\hbar^2}{2}\gamma\nabla\frac{[M^{-1}\nabla\left(n^{\alpha}\right)]}{n^{\alpha}} \quad \text{..... (3.5)}$$

where α and γ are two adjustable parameters, M^{-1} is the inverse effective mass tensor, n is the electron (or hole) density and h is a Planck's constant. Bohm Quantum

Potential (BQP) Model with alpha=0.5 and gamma=1.2 was used to take quantum mechanical effects into consideration. Additionally, numerical methods such as BICGST (bi-conjugate gradient stabilized) have been considered to obtain the

solutions with improved convergence in 3D device structure (SILVACO, 2016). Default simulator coefficients for all parameters have been employed.

Figure 3.02 shows the drain current and gate transconductance characteristics of GEWE-SiNW MOSFET at V_{ds}=0.2V. It is observed that the current driving capability of nano-scale GEWE-SiNW MOSFET is enhanced by 20% in comparison to SiNW MOSFET. This enhancement is due to incorporation of gate-metal engineering scheme which causes gradual step change of surface potential at the interface of two metals and hence, increase the gate efficiency of device. The MOSFET transconductance ($g_m = \partial I_{ds}/\partial V_{gs}$) is typically measured in the linear regime and is used as an indirect monitor of inversion carrier mobility.

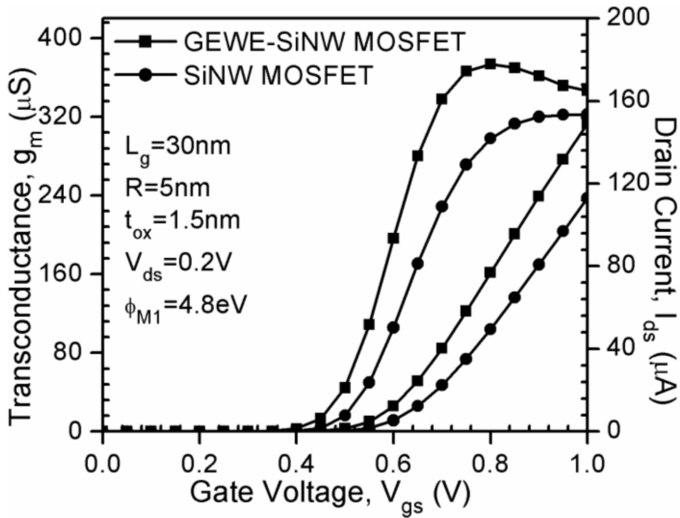


Figure 3.02: Transfer and Transconductance characteristics of SiNW and GEWE-SiNW MOSFET at V_{ds}=0.2V respectively (Gupta et al, 2015a).

Transconductance is useful in designing linear amplifiers and does not have any significance in switching power supplies. In general, the larger the transconductance of a device, the greater the gain (amplification) it is capable of delivering, when all other factors are held constant. It is clearly evident from Fig. 3.02 that

transconductance of GEWE-SiNW is higher in comparison to conventional SiNW MOSFET due to enhanced on-current. Also, significant enhancement in g_m of GEWE-SiNW device is obtained as compared to the previously reported work (Ghosh et al, 2012).

3.3 RF PERFORMANCE METRICS INQUISITION

In deep sub micrometer regime, it is very challenging to design RF devices for ultra-low power applications due to aggressive scaling of MOSFETs. In this section, we investigate the comparison of conventional SiNW and our device in which we incorporated GEWE scheme onto conventional SiNW MOSFETs to examine the efficacy of high frequency in terms of RF metrics. Further, the impact of device parameters variation of GEWE-SiNW MOSFET on the same has been studied.

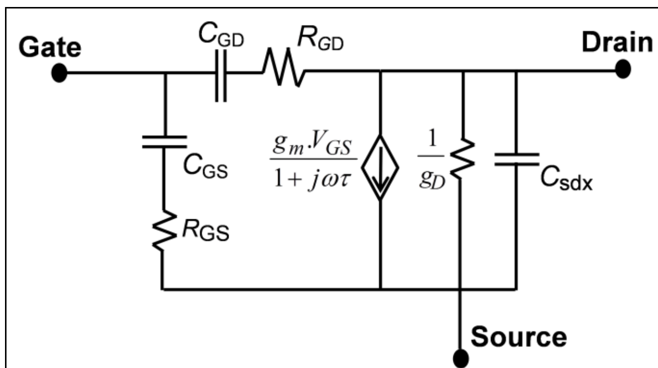


Figure 3.03: Non-quasi-static (NQS) equivalent circuit model of SiNW MOSFET at RF region operating in the strong inversion region (Gupta et al, 2015a).

Figure 3.03 shows the non-quasi-static equivalent circuit of a MOSFET to extract small signal parameters of GEWE-SiNW MOSFET and conventional SiNW MOSFET that is based on conventional MOSFET's small signal microwave modeling. Here, R_{gs} and R_{gd} are distributed channel resistance and g_{dsi} and g_{mi} are

intrinsic gate-to-drain conductance and transconductance. C_{ds} and C_{gs} are intrinsic gate-to-drain and gate-to-source capacitances respectively (Tsividis & McAndrew, 2011). The capacitances between each pair of electrodes are calculated through AC small signal analysis after post processing operation of DC solution. Parasitic capacitance in RF amplifiers may cause these amplifiers to have low gain due to parasitic loss. In some cases, it may cause these amplifiers to oscillate. In digital switching circuits, the rise time and fall time of the digital signal greatly affect the maximum speeds achievable (Malik et al, 2012). The intrinsic parasitic capacitances are extracted from small signal analysis after post processing operation of DC solution at an operating frequency of 1MHz. The parasitic capacitance on the inputs and outputs of the digital devices increases the rise and fall times. Thus, it is required to investigate the parasitic capacitances at high frequency. Figure 3.04 shows the variation of bias-dependent parasitic capacitances such as gate-source (C_{gs}), gate-drain (C_{gd}) and gate-gate (C_{gg}) capacitance as a function of gate voltage for GEWE-SiNW MOSFET and SiNW MOSFET. The capacitance value changes depending on the voltage that appears across the drain-source and also across the gate-source of the device. It is evident from Fig. 3.04(a) that GEWE-SiNW exhibits smaller C_{gs}, C_{gd} in comparison to its conventional SiNW MOSFET due to metal gate workfunction difference which results in improved screening of conducting channel from drain bias variations. A similar kind of behaviour is also observed in (Cho et al, 2011). A parameter generally described when comparing transistors for RF applications is the cut-off frequency, f_T (Pozar, 2009; Sarkar et al, 2012).

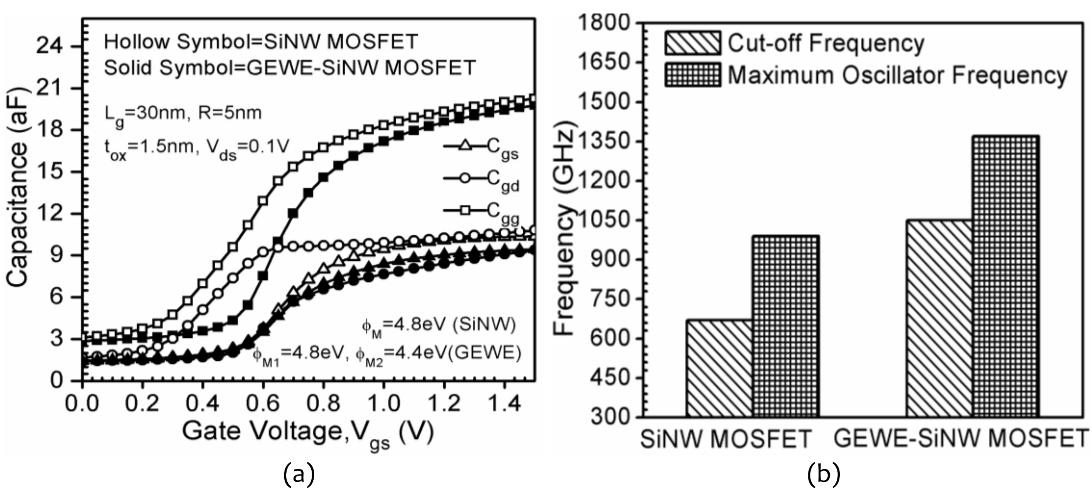


Figure 3.04: (a) Intrinsic capacitances of SiNW MOSFET and GEWE-SiNW MOSFET as a function of V_{gs}, (b) Cut-off and Maximum Oscillator Frequency of SiNW MOSFET and GEWE-SiNW MOSFET at V_{gs}=0.7V and V_{ds}=0.2V

f_T is a specification for high-speed digital applications (speed and high swing) and can be defined as follow:

$$f_T = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)} \quad .... (3.6)$$

where g_m is the transconductance, C_{gs} and C_{gd} are parasitic capacitances.

Also, the incorporation of GEWE design enhances the carrier mobility of a device, leading to increase in cut-off frequency as is evident from Fig. 3.04(b). For characterizing a device for tuned RF amplifiers and oscillators, maximum oscillation frequency is an important parameter to consider. f_{MAX} is the maximum oscillation frequency which is defined as the frequency where the maximum unilateral power gain falls to unity (0 dB) (Nae et al, 2009).

$$f_{MAX} = \frac{f_T}{\sqrt{4R_g\left(g_{ds} + 2\pi f_T C_{gd}\right)}} \quad .... (3.7)$$

where R_g is gate resistance, g_{ds} is drain transconductance

Further, f_{MAX}, as is seen from Fig. 3.04 (b), is higher for GEWE-SiNW MOSFET than SiNW MOSFET, which is due to lower parasitic capacitance in GEWE-SiNW MOSFET, thereby giving the GEWE-SiNW design a new strength for switching applications and wireless communication. Intrinsic Delay is another important measure for switching applications. The increasing capacitance between the gate and the overlapped S/D region deteriorates the intrinsic gate delay (Khakifirooz & Antoniadis, 2008). Intrinsic delay metric is defined as:

$$\tau = \frac{C_{gg}.V_d}{I_{ON}} \quad \text{…. (3.8)}$$

where C_{gg} is the parasitic gate capacitance, V_{ds} is the bias voltage applied to drain and I_{ON} is the on-current.

Inset of Fig. 3.05 shows the comparison of GEWE-SiNW with SiNW MOSFET in terms of intrinsic delay parameter. As is evident from the figure, there is notable reduction in intrinsic delay of GEWE-SiNW MOSFET than its conventional counterpart due to incorporation of two dissimilar metal gates and cylindrical silicon nanowire which increases on-current, reduces parasitic capacitances, hence leads to considerable reduction of intrinsic delay. Power gains play an important role in designing RF amplifiers. For low noise amplifier (LNA) design, maximum available power gain and stability are two important criterions. Stability measures the ability of LNA to oscillate at high frequencies. When designing an amplifier for RF frequency range, our aim is to get void of any oscillations. The standard way to scrutinize stability is by so-called stern stability factor. The stern's stability factor (K) is usually less than 1 at low frequency and greater than 1 at high frequency (Oh & Rieh, 2013; Voinigescu, 2013).

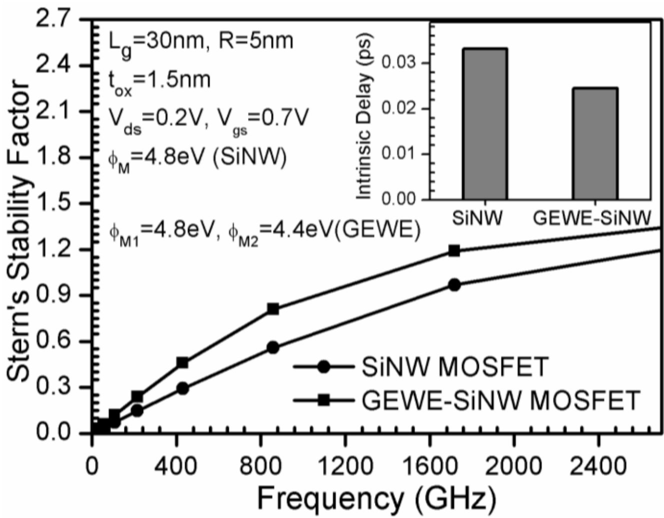


Figure 3.05: Stern's Stability factor of SiNW and GEWE-SiNW MOSFET. Inset: Intrinsic delay of SiNW and GEWE-SiNW MOSFET at V_{ds}=0.2V.

The factor K is defined as in the following equation:

$$K = \frac{1+|\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2.|S_{12.} \cdot S_{21}|} \quad \text{…. (3.9)}$$

Where, S_{11} and S_{22} are the reflection coefficients; S_{12} and S_{21} are transmission coefficients and s-matrix Δ is defined as

$$\Delta = S_{11} \times S_{22} - S_{12} \times S_{21} \quad \text{….. (3.10)}$$

Figure 3.05 shows the variation of stability factor as a function of frequency. As is clear from the figure, at high frequency, K is significantly higher for GEWE-SiNW in comparison to SiNW MOSFET. This is due to increased gate control, which causes maximum power transfer from source to load. Figure 3.06 shows the improvement of HF maximum available power gain (G_{ma}) of GEWE-SiNW MOSFET over SiNW MOSFET. This is due to better gate controllability and higher silicon nanowire mobility which results in enhanced transconductance and reduced parasitic capacitances.

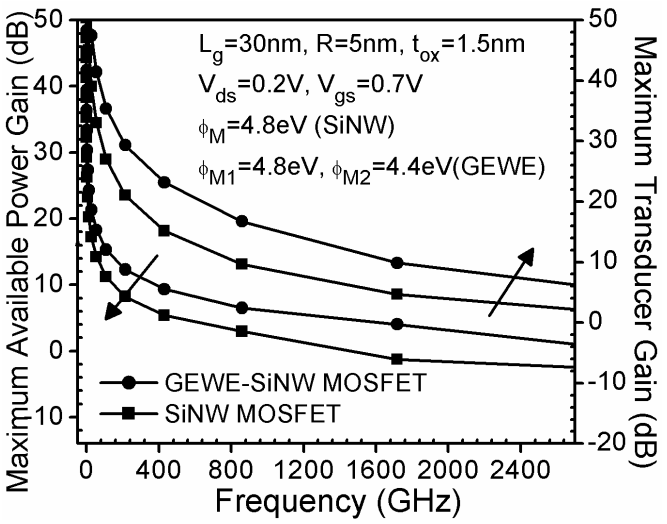


Figure 3.06: Maximum Available Power Gain and Maximum Transducer Power Gain of SiNW and GEWE-SiNW MOSFET at V_{ds}=0.2V and V_{gs}=1.0V.

The Maximum transducer power gain (G_{MT}) of a two port network is defined as the ratio of average power delivered to the load by a source to a maximum available power from the source. This is a measure of efficacy of the two ports (Golio, 2003; Grebennikov, 2011). Figure 3.06 evaluates the device performance in terms of maximum transducer gain and is clear from the graph that G_{MT} is improved in GEWE-SiNW in comparison to SiNW. This enhancement is due to integration of GEWE design onto SiNW which augments current driving capability and results in higher power at the load end i.e. at drain end, hence suitable for RF/wireless applications.

3.3.1 Effect of Gate Metal Engineering

In this sub-section, the effect of metal workfunction engineering on the RF metrics of GEWE-SiNW MOSFET is examined by keeping the workfunction of the metal gate at the source side constant and varying the workfunction of metal gate at the drain end. Figure 3.07(a) indicates the transfer and transconductance characteristics of

GEWE-SiNW MOSFET for different values of metal workfunction at drain side (Φ_{M2}).

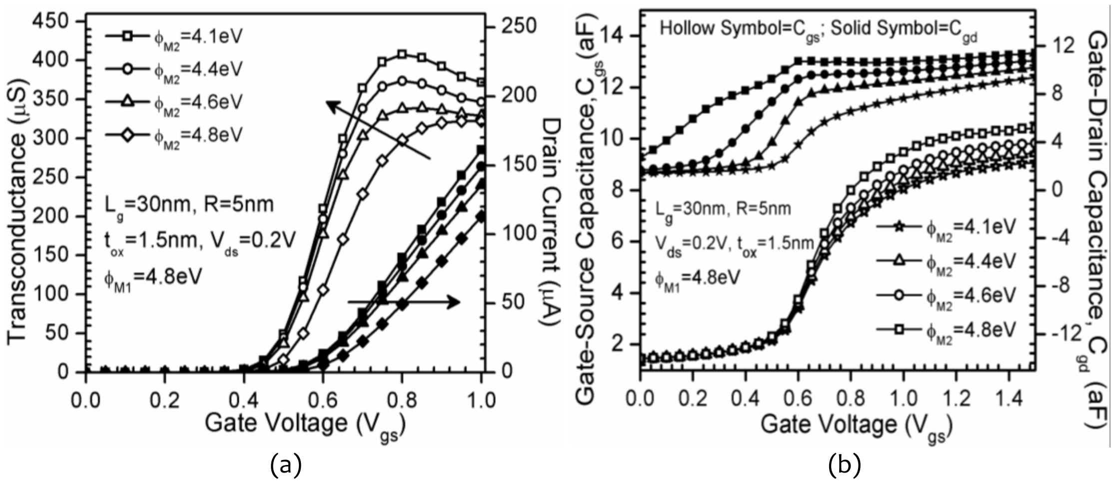


Figure 3.07: (a)Transfer and transconductance characteristics of GEWE-SiNW MOSFET at V_{ds}=0.2V, (b) Gate-Source and Gate-Drain Capacitance of GEWE-SiNW MOSFET as a function of gate voltage for various metal workfunction values at V_{ds}=0.2V.

As is evident from Fig. 3.07(a) that as we increase the workfunction difference from 0 to 0.2 eV, the on current increased by 10.13% and further increment in workfunction difference to 0.7 eV, results in 20% enhancement in drain current. Also, significant enhancement in transconductance is observed as we decrease the metal workfunction at the drain end due to better improvement of carrier transport efficiency with increase in workfunction difference as stated in (Long & Chin, 1997), thus, signifying the suppression of short channel effects. Fig. 3.07 (b) depicts that there is a prominent degradation of parasitic capacitances as we increase the metal gate workfunction difference. Capacitance decreases due to enhanced screening of channel region from drain bias variations thus, reducing the turn-on delay time. Figure 3.08 compares the cut off and maximum oscillator frequency of GEWE-SiNW MOSFET for different metal workfunction. It is clearly evident from Fig. 3.08 that as the metal work

function at the drain end decreases, the cut off frequency increases which leads to higher switching speed.

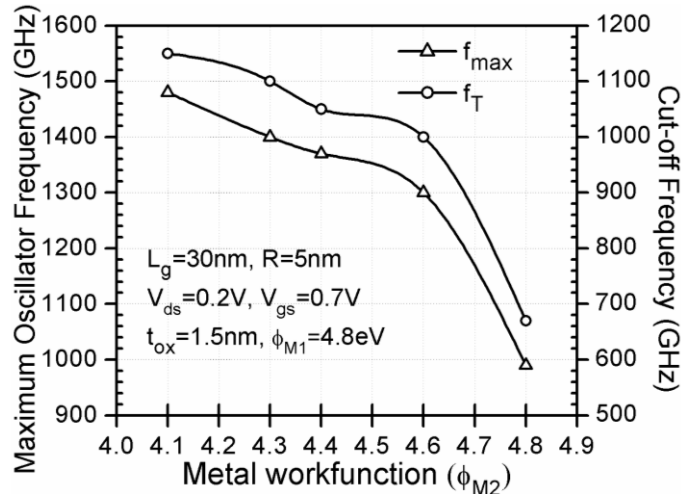


Figure 3.08: Cut-off and Maximum Oscillator Frequency of GEWE-SiNW MOSFET for various metal workfunction values (Φ_{M2}).

Further, with increase in metal workfunction difference, the cut-off frequency increases as is shown in Fig. 3.08. This is due to enhanced gate control over channel and screening of potential from the drain side, which increases the transconductance, leading to increase in cut-off frequency and device packaging density, thereby making the device suitable for CMOS wireless applications. Also, the use of metal gates results in reduced gate resistance, and hence increases f_{MAX}. An appreciable accretion of maximum oscillation frequency is observed by increasing gate metal workfunction difference due to reduced parasitic capacitances [see Fig. 3.07(b)]. Further, increasing the metal workfunction difference increases the K-factor as shown in Fig. 3.09. This is due to improvement of screening effect and I_{on} thus, maximizing power transfer from source to load. Hence, GEWE-SiNW is suitable for low noise amplifier and RF applications.

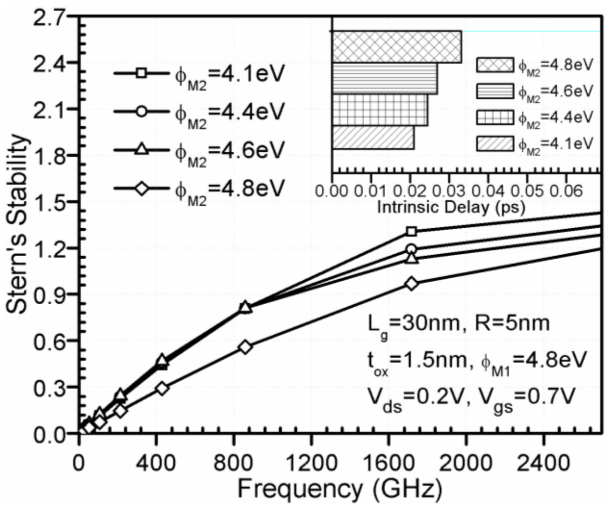


Figure 3.09: Stern's Stability factor of GEWE-SiNW MOSFET for various metal workfunction values. Inset: Intrinsic delay of GEWE-SiNW MOSFET for various metal workfunction values.

Also, with increase in metal workfunction difference, delay reduces due to enhanced gate control and redistribution of electric field in the channel which results in higher mobility leading to improvement in carrier transport efficiency as shown in inset of Fig. 3.09. G_{MT} also improves with the tuning of metal gate workfunction at drain end.

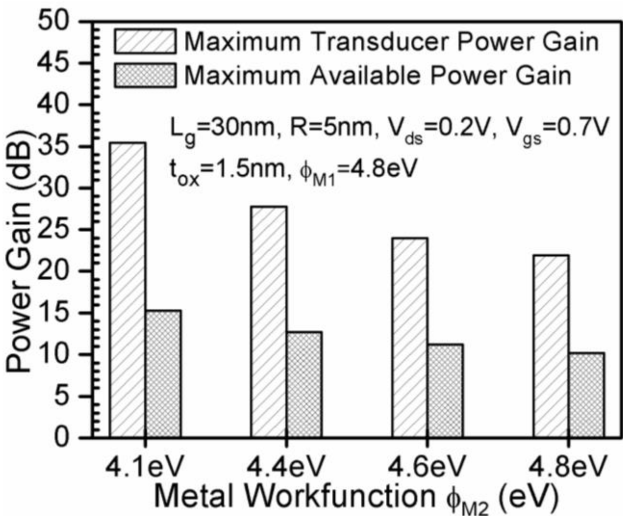


Figure 3.10: Maximum Available power gain and Maximum Transducer Power Gain of GEWE-SiNW MOSFET as a function of Φ_{M2}.

Higher the metal gate workfunction difference, higher the electric field in the channel due to which mobility increases and hence significantly enhances the power gain. Further, tuning of structural parameters of GEWE-SiNW in terms of increased metal workfunction difference can enhance Gma as is evident from Fig. 3.10 due to enhanced transconductance owing to improved carrier efficiency and alleviated SCEs. Thus, GEWE-SiNW MOSFET proves to be a promising candidate for RF amplifiers and high speed applications.

3.3.2 Effect of Oxide Thickness

This section studies the impact of oxide thickness on RF metrics. It is clearly evident from Fig. 3.11(a) that scaling down the gate oxide thickness from 3 to 1 nm results in a better gate controllability over the channel which significantly enhances the driving current capability and improves the transconductance.

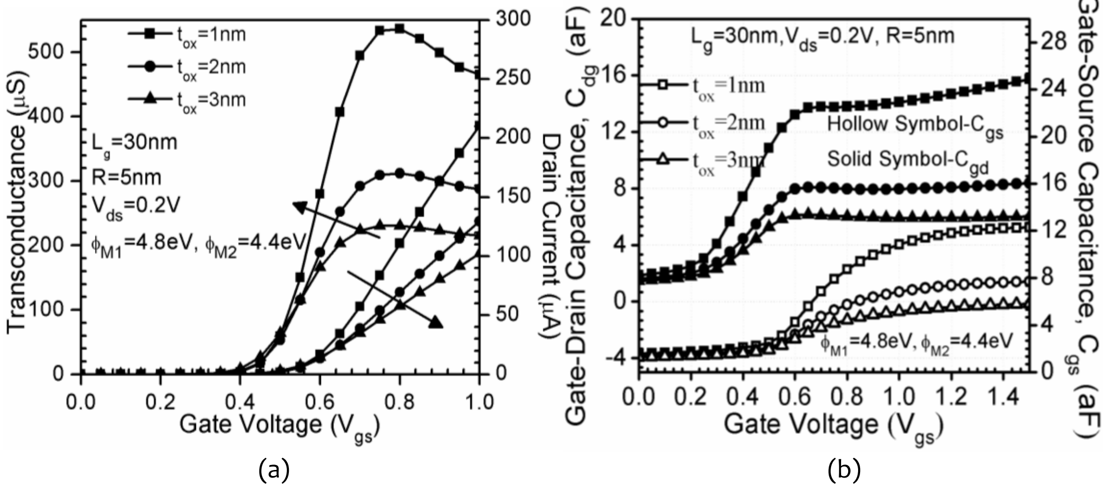


Figure 3.11: (a) Transfer and transconductance characteristics of GEWE-SiNW MOSFET at V_{ds}=0.2V for different oxide thickness, (b) Gate-Drain and Gate-Source Capacitance of GEWE-SiNW MOSFET as a function of gate voltage for different oxide thickness.

This overcomes the drawback of mobility degradation due to increased channel doping. When oxide thickness scales down from 3 to 1 nm, the on-current increases

by 77% and transconductance by approximately 100% thereby, reflecting significant improvement in SCEs at sub-nm range. However, at high frequencies the picture is completely reversed, where the efficacy of the gate oxide capacitance dominates the RF behavior of devices. Figure 3.11(b) reflects the intrinsic parasitic gate-source and gate-drain capacitances as a function of gate voltage. It can be seen that as oxide thickness increases, parasitic capacitances decreases due to reduction in inversion charge (Dastjerdy et al, 2012; Pati et al, 2014).

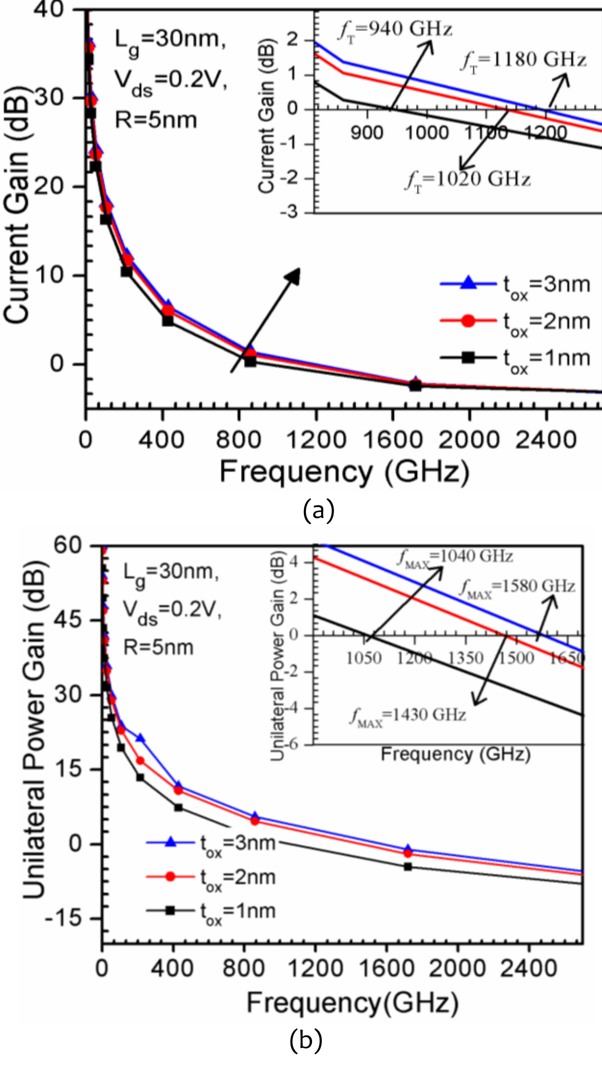


Figure 3.12: (a) Current Gain of GEWE-SiNW MOSFET at V_{ds}=0.2V for different oxide thickness as a function of gate voltage, (b) Unilateral Power Gain of GEWE-SiNW MOSFET for different oxide thickness. Inset (a-b): shows the cut-off and maximum frequency respectively.

The enhancement of transconductance due to better gate control on the channel for oxide thickness 1nm compared to 3 nm does not counter balance the effect of the gate capacitances. As a result, t_{ox}=3nm has better cut-off frequency and maximum oscillator frequency as can be clearly shown in Fig. 3.12 (a-b). Further, current gain and unilateral power gains are extracted for determining the values of cut off frequency and maximum oscillation frequency respectively.

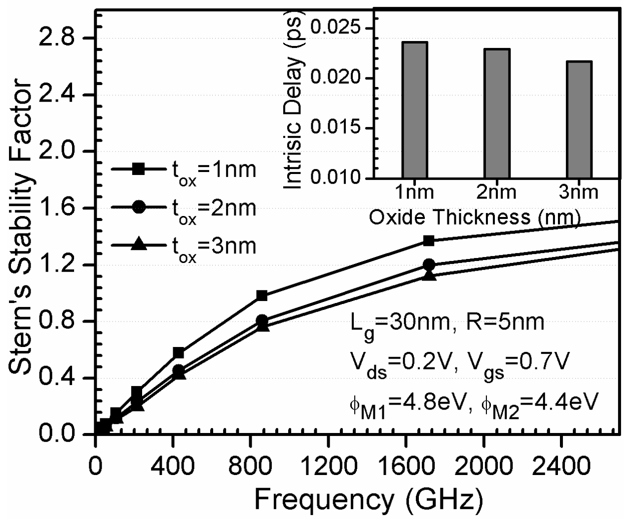


Figure 3.13: Stern's Stability Factor of GEWE-SiNW MOSFET for various metal workfunction values. Inset: Intrinsic delay of GEWE-SiNW MOSFET at V_{ds}=0.2V for different oxide thickness.

In addition, the Stern's stability factor also significantly improves as oxide thickness scales down from 3 to 1 nm as shown in Fig. 3.13. This enhancement is due to higher value of transconductance and better gate controllability. Inset of Fig. 3.13 shows the intrinsic delay ratio of GEWE-SiNW MOSFET for three different oxide thicknesses. Since, delay depends upon gate capacitance and transconductance, therefore, intrinsic delay reduces as oxide thickness increases. Hence, scaling of oxide thickness significantly degrades the speed and the matching of the device in RF circuits.

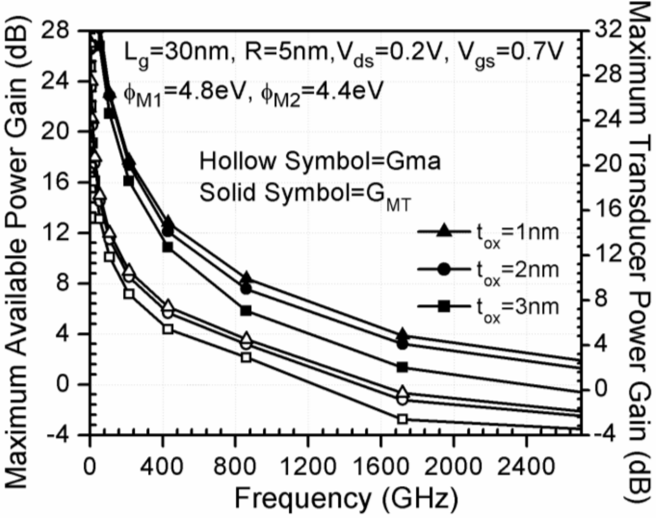


Figure 3.14: Maximum Available and Maximum Transducer Power Gain of GEWE-SiNW MOSFET for different oxide thickness.

Moreover, power gains such as maximum available power gain and maximum transducer gain also increases with thinning of gate oxide as clearly is evident from Fig. 3.14, thus, providing maximum voltage gain owing to improved transconductance.

3.3.3 Effect of channel length (L_g)

In this section, the impact of channel length is studied on various parameters. Figure 3.15(a) shows as we scale down the channel length of SiNW, the transfer characteristics improves due to better gate controllability and incorporation of dissimilar metal gates. This enhances the transconductance of device, and hence, overcomes the SCEs associated due to scaling of channel length. Further, Fig. 3.15(b) depicts that there is a prominent degradation of gate-source and gate-drain capacitances. Since, as we reduce the channel length, the inversion charge density of nanowire increases which results in improvement in the mobility across the channel

due to reduction in scattering from nearby atoms and hence, results in reduction in C_{gs} and C_{gd}.

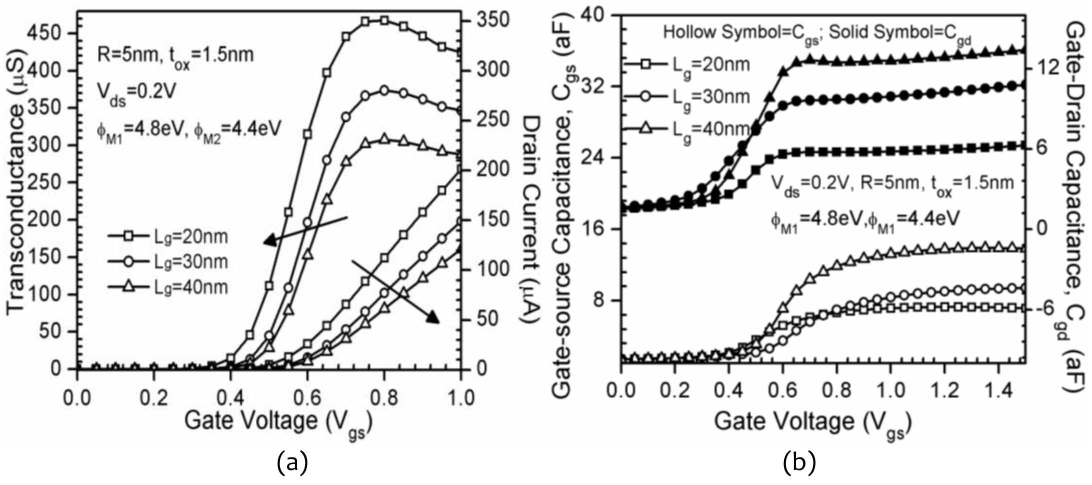


Figure 3.15: Transfer and Transconductance characteristics of GEWE-SiNW MOSFET for different channel lengths, (b) Gate-Source and Gate-Drain Capacitance of GEWE-SiNW MOSFET as a function of gate voltage for different channel lengths.

Fig. 3.16 (a-b) shows the Current Gain and Unilateral Power Gain as a function of frequency. As we have already mentioned that f_T and f_{MAX} are extracted from current gain and unilateral power gain respectively, it is clearly evident that as channel length scales down, both cut-off and maximum oscillator frequency increases due to increase in transconductance and reduction in parasitic capacitance as is shown in eq. (3.6) and (3.7).

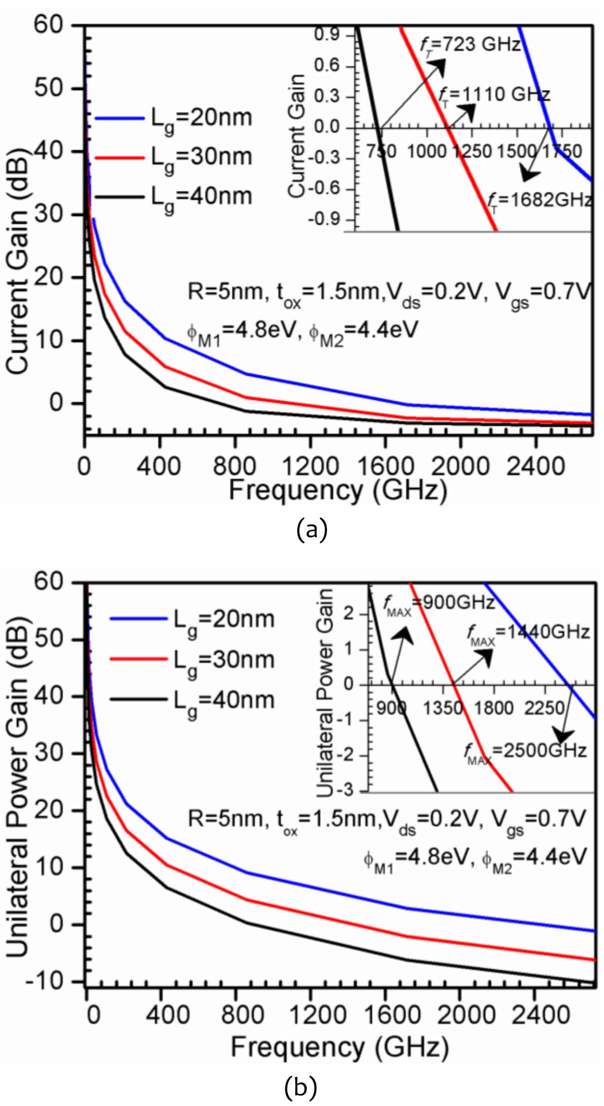


Figure 3.16: (a) Current Gain and (b) Maximum Unilateral Power Gain of GEWE-SiNW MOSFET V_{ds}=0.2V for different channel lengths. Inset (a-b): shows the cut-off and maximum frequency respectively

Moreover, stern's stability factor which determines the stability of a device at high frequency decreases as we scale down the channel length due to overlapping of source and drain fields which results in a commuted gate control in scaled devices, thus causing instability as is shown in Fig. 3.17. Intrinsic Delay of GEWE-SiNW improves further as we scale down the channel length from 40nm to 20nm as shown in inset of Fig. 3.17. This is due to reduction in gate parasitic capacitance and improvement in I_{on}.

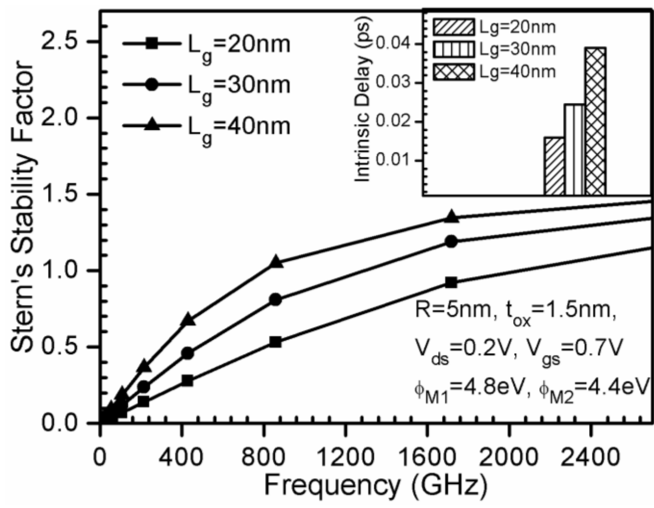


Figure 3.17: Stern's Stability Factor of GEWE-SiNW MOSFET for different channel lengths. Inset: Intrinsic delay of GEWE-SiNW MOSFET at V_{ds}=0.2V for different channel lengths.

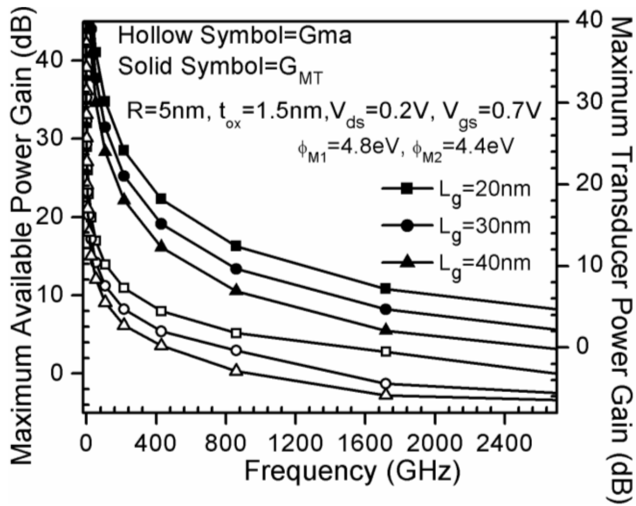


Figure 3.18: Maximum Available and Maximum Transducer Power Gain of GEWE-SiNW MOSFET at V_{ds}=0.2V for different channel lengths.

Fig. 3.18 shows the Maximum Available and Maximum Transducer power gain as a function of frequency for different gate lengths. The Power gain of GEWE-SiNW improves further as channel length of nanowire scales down to 20nm due to enhancement in current gain.

3.3.4 Effect of Radius of Silicon Nanowire (R)

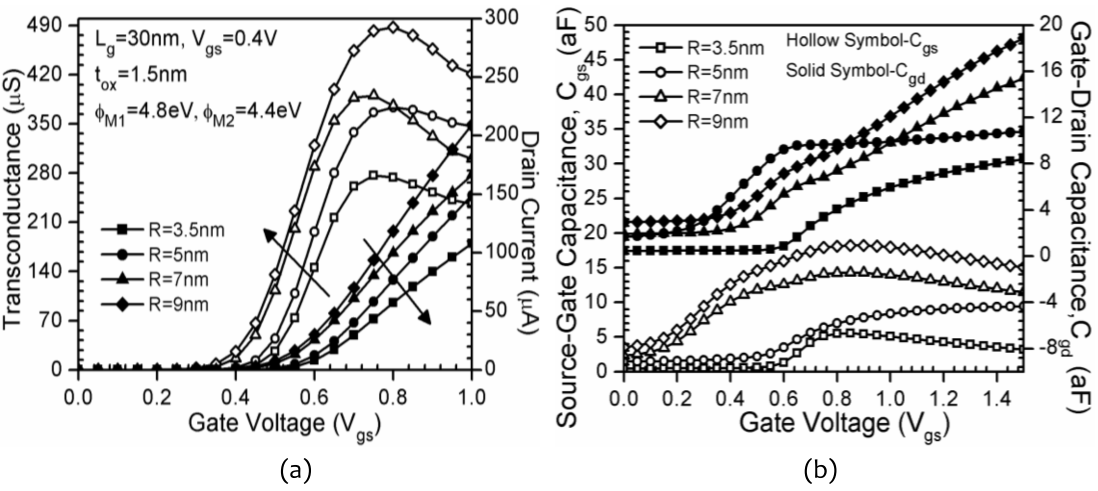


Figure 3.19: (a) Transfer and transconductance characteristics of GEWE-SiNW MOSFET for different radius of SiNW, (b) Gate-Drain and Gate-Source Capacitance of GEWE-SiNW MOSFET as a function of gate voltage for different radius of SiNW

In this section, we examine the efficacy of silicon nanowire radius on RF performance of GEWE-SiNW MOSFET. Fig. 3.19(a) shows that as radius of nanowire decreases, drain current decreases due to the decrement in inversion charge density which increases the threshold voltage as a result of which the on-state current decreases and hence the transconductance. On the other hand, parasitic gate capacitance which is a sum of the gate-source and the gate-drain capacitance degrade as radius of SiNW decreases. Smaller values of these capacitances play an important role in device switching performance due to reduction in the turn-on delay time. Fig. 3.19 (b) shows the behaviour of C_{gd} and C_{gs} as a function of gate voltage as is also predicted by Li et al. (Li & Hwang, 2009). Fig. 3.20 depicts the cut-off and maximum oscillator frequency of GEWE-SiNW MOSFET as a function of SiNW radius. As is shown, f_T increases as radius decreases due to degradation in parasitic gate capacitance. But f_{MAX} decreases as we reduce the radius of nanowire. This might be due to increment current

driving capability and drain transconductance. So we have to choose optimal value of radius so that we can achieve desirable cut-off and maximum oscillator frequency for CMOS wireless applications.

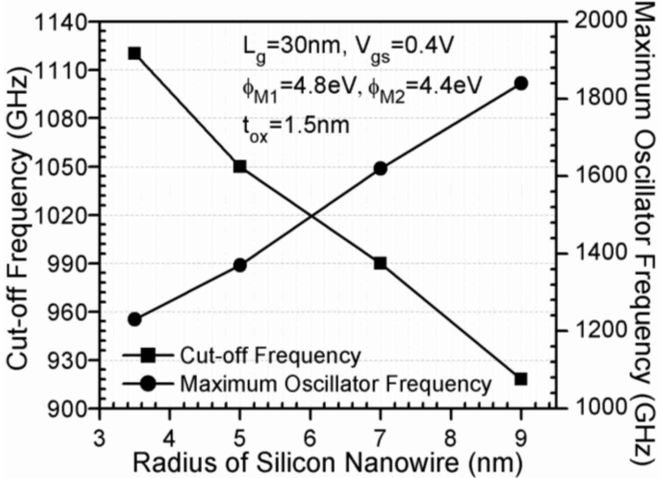


Figure 3.20: Cut-off and Maximum Oscillatory Frequency of GEWE-SiNW MOSFET for different radius of silicon nanowire.

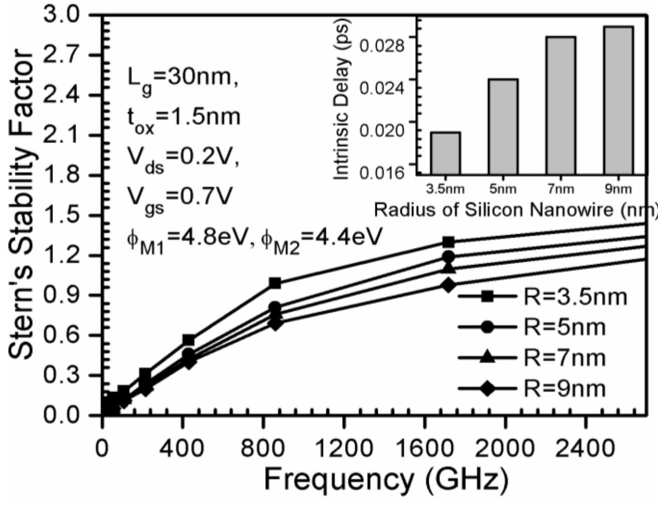


Figure 3.21: Stern's Stability Factor of GEWE-SiNW MOSFET for different channel radius. Inset: Intrinsic delay of GEWE-SiNW MOSFET

Fig. 3.21 shows the stern's stability factor as a function of frequency and its inset shows the intrinsic delay of GEWE-SiNW as a function of radius of nanowire. It is

clearly evident that at high frequency, K >1 for GEWE-SiNW but its value enhances as radius scales down, which makes it suitable for low noise amplifiers. Also, intrinsic delay reduces by 50% as we scale down the radii of nanowire due to degradation of parasitic capacitance as shown in Fig. 3.19(b). In addition, power gains degrade as we reduce the radius of nanowire. Both maximum available power gain and maximum transducer power gain reduces 1.5 times as clearly shown in Fig. 3.22. Hence, for millimeter wave applications, we have to optimize the value of silicon nanowire radius.

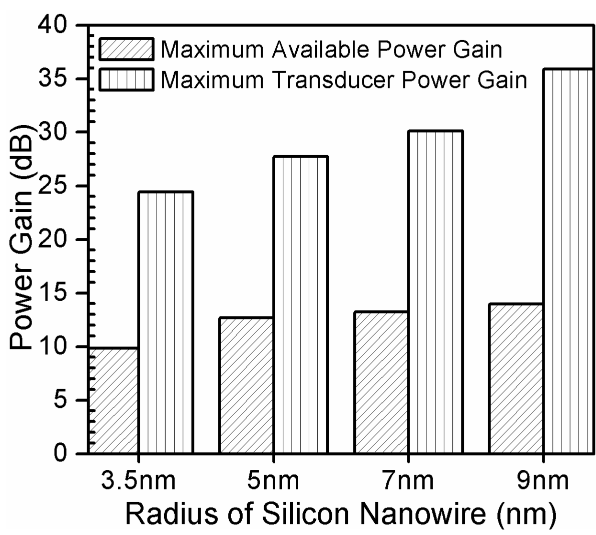


Figure 3.22: Maximum Available Power Gain and Maximum Transducer Power Gain of GEWE-SiNW MOSFET at V_{ds}=0.2V for different silicon nanowire radius.

3.4 SUMMARY

This chapter explores the quantitative investigation of high-frequency performance of GEWE-SiNW MOSFET and the results so obtained are simultaneously compared with SiNW MOSFET using 3D TCAD device simulator. Following performance metrics are studied such as, parasitic capacitance, power gains (Gma, G_{MT}), cut-off frequency

(f_T), maximum oscillator frequency (f_{MAX}), stability factor and intrinsic delay. It has been found that due to improved transconductance, gate controllability and carrier mobility, GEWE-SiNW MOSFET exhibit superior performance in all RF metrics compared to its counterpart, thus providing its use in high frequency amplifier and microwave applications. Further, it is observed that by increasing the workfunction difference of gate metal, noticeable improvement in RF performance is observed since current driving capability and gain of the device enhances due to lower metal gate workfunction at the drain end. Also, the performance of GEWE-SiNW MOSFET further improves by scaling down the channel length to 20nm which is towards 32nm CMOS node technology, hence, giving a new opening for HF wireless and switching applications. Moreover, thinning of oxide thickness to 1nm degrades the RF performance of GEWE-SiNW MOSFET owing to high parasitic capacitance. RF performance of GEWE-SiNW improves as compared to conventional SiNW and thus optimum values of device parameters must be chosen for better device performance in RF/Wireless applications. For comprehensive RF analysis of GEWE-SiNW MOSFET and its efficacy at high frequency, the small signal behaviour of GEWE-SiNW in terms of scattering parameters is required which would be useful for evaluating the microwave performance of the device in terms of forward and reverse gains. This has, hence, been discussed in the next chapter along with the noise metrics that affects the device performance at HF.

3.5 REFERENCES

Chaudhry, A. & Roy, J. (2010) MOSFET models, quantum mechanical effects and modeling approaches: a review. *JSTS: Journal of Semiconductor Technology and Science*, 10(1), 20-27.

Chen, Q. B. (2013) Compact modeling of multi-gate MOSFETs for RF designs, *2013 IEEE International Wireless Symposium (IWS)*.

Cho, S., Kim, K. R., Park, B.-G. & Kang, I. M. (2011) RF performance and small-signal parameter extraction of junctionless silicon nanowire MOSFETs. *IEEE Transactions on Electron Devices*, 58(5), 1388-1396.

Cui, Y., Zhong, Z., Wang, D., Wang, W. U. & Lieber, C. M. (2003) High performance silicon nanowire field effect transistors. *Nano letters*, 3(2), 149-152.

Dastjerdy, E., Ghayour, R. & Sarvari, H. (2012) Simulation and analysis of the frequency performance of a new silicon nanowire MOSFET structure. *Physica E: Low-dimensional Systems and Nanostructures*, 45, 66-71.

Doan, C. H., Emami, S., Niknejad, A. M. & Brodersen, R. W. (2005) Millimeter-wave CMOS design. *IEEE Journal of solid-state circuits*, 40(1), 144-155.

Enz, C. (2002) An MOS transistor model for RF IC design valid in all regions of operation. *IEEE Transactions on Microwave Theory and Techniques*, 50(1), 342-359.

Fu, J., Singh, N., Buddharaju, K., Teo, S., Shen, C., Jiang, Y., Zhu, C., Yu, M., Lo, G. & Balasubramanian, N. (2008) Si-nanowire based gate-all-around nonvolatile SONOS memory cell. *IEEE Electron Device Letters*, 29(5), 518-521.

Ghosh, P., Haldar, S., Gupta, R. & Gupta, M. (2012) An investigation of linearity performance and intermodulation distortion of GME CGT MOSFET for RFIC design. *IEEE Transactions on Electron Devices*, 59(12), 3263-3268.

Golio, M. (2003) *Microwave and RF product applications*CRC Press.

Grebennikov, A. (2011) *RF and microwave transmitter design*, *234*John Wiley & Sons.

Gupta, N. & Chaujar, R. (2014) Implications of transport models on the analog performance of Gate Electrode Workfunction Engineered (GEWE) Silicon Nanowire MOSFET, *Devices, Circuits and Systems (ICDCS), 2014 2nd International Conference on*. IEEE.

Gupta, N., Kumar, A. & Chaujar, R. (2015) Impact of device parameter variation on RF performance of gate electrode workfunction engineered (GEWE)-silicon nanowire (SiNW) MOSFET. *Journal of Computational Electronics*, 14, 798-810.

Gupta, S. K. & Baishya, S. (2013) Modeling of cylindrical surrounding gate MOSFETs including the fringing field effects. *Journal of Semiconductors*, 34(7), 074001.

Iannaccone, G., Curatola, G. & Fiori, G. (2004) Effective Bohm Quantum Potential for device simulators based on drift-diffusion and energy transport, *Simulation of Semiconductor Processes and Devices 2004*Springer, 275-278.

Jimenez, D., Iniguez, B., Roig, J., Sune, J., Marsal, L., Pallares, J. & Flores, D. (2005) Physics-based model of the surrounding-gate MOSFET, *Conference on Electron Devices, 2005 Spanish*. IEEE.

Khakifirooz, A. & Antoniadis, D. A. (2008) MOSFET performance scaling—Part I: Historical trends. *IEEE Transactions on Electron Devices*, 55(6), 1391-1400.

Larson, L. E. (2003) Silicon technology tradeoffs for radio-frequency/mixed-signal" systems-on-a-chip". *IEEE Transactions on Electron Devices*, 50(3), 683-699.

Li, Y. & Hwang, C.-H. (2009) DC baseband and high-frequency characteristics of a silicon nanowire field effect transistor circuit. *Semiconductor Science and Technology*, 24(4), 045004.

Long, W. & Chin, K. K. (1997) Dual material gate field effect transistor (DMGFET), *Electron Devices Meeting, 1997. IEDM'97. Technical Digest., International*. IEEE.

Malik, P., Gupta, R., Chaujar, R. & Gupta, M. (2012) AC analysis of nanoscale GME-TRC MOSFET for microwave and RF applications. *Microelectronics Reliability*, 52(1), 151-158.

Nae, B., Lazaro, A. & Iniguez, B. (2009) High frequency and noise model of gate-all-around MOSFETs, *2009 Spanish Conference on Electron Devices*. IEEE.

Oh, Y. & Rieh, J.-S. (2013) Effect of device layout on the stability of RF MOSFETs. *IEEE Transactions on Microwave Theory and Techniques*, 61(5), 1861-1869.

Pal, A. & Sarkar, A. (2014) Analytical study of dual material surrounding gate MOSFET to suppress short-channel effects (SCEs). *Engineering Science and Technology, an International Journal*, 17(4), 205-212.

Pati, S. K., Koley, K., Dutta, A., Mohankumar, N. & Sarkar, C. K. (2014) Study of body and oxide thickness variation on analog and RF performance of underlap DG-MOSFETs. *Microelectronics Reliability*, 54(6), 1137-1142.

Patnaik, V. S., Gheedia, A. & Kumar, M. J. (2010) 3D Simulation of nanowire FETs using quantum models. *arXiv preprint arXiv:1008.3006*.

Pozar, D. M. (2009) *Microwave engineering*John Wiley & Sons.

Rustagi, S., Singh, N., Fang, W., Buddharaju, K., Omampuliyur, S., Teo, S., Tung, C., Lo, G., Balasubramanian, N. & Kwong, D. (2007) CMOS inverter based on gate-all-around silicon-nanowire MOSFETs fabricated using top-down approach. *IEEE Electron Device Letters*, 28(11), 1021-1024.

Saijets, J., Andersson, M. & Åberg, M. (2002) A comparative study of various MOSFET models at radio frequencies. *Analog Integrated Circuits and Signal Processing*, 33(1), 5-17.

Sarkar, A., De, S., Dey, A. & Sarkar, C. K. (2012) Analog and RF performance investigation of cylindrical surrounding-gate MOSFET with an analytical pseudo-2D model. *Journal of Computational Electronics*, 11(2), 182-195.

Sharma, D. & Vishvakarma, S. K. (2013) Precise analytical model for short channel cylindrical gate (CylG) gate-all-around (GAA) MOSFET. *Solid-State Electronics*, 86, 68-74.

Shur, M. (1989) Split-gate field-effect transistor. *Applied Physics Letters*, 54(2), 162-164.

SILVACO, I. (2011) ATLAS User's Manual. *Santa Clara, CA, Ver*, 5.

Tsividis, Y. & McAndrew, C. (2011) *Operation and Modeling of the MOS Transistor*Oxford Univ. Press.

Voinigescu, S. (2013) *High-frequency integrated circuits*Cambridge University Press.

Wang, R., Zhuge, J., Huang, R., Tian, Y., Xiao, H., Zhang, L., Li, C., Zhang, X. & Wang, Y. (2007) Analog/RF performance of Si nanowire MOSFETs and the impact of process variation. *IEEE transactions on Electron Devices*, 54(6), 1288-1294.

Woerlee, P. H., Knitel, M. J., Van Langevelde, R., Klaassen, D. B., Tiemeijer, L. F., Scholten, A. J. & Zegers-van Duijnhoven, A. T. (2001) RF-CMOS performance trends. *IEEE Transactions on Electron Devices*, 48(8), 1776-1782.

Yang, B., Buddharaju, K., Teo, S., Singh, N., Lo, G. & Kwong, D. (2008) Vertical silicon-nanowire formation and gate-all-around MOSFET. *IEEE Electron Device Letters*, 29(7), 791-794.

Yang, G., Wang, S. & Wang, R. (2003) An efficient preconditioning technique for numerical simulation of hydrodynamic model semiconductor devices. *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*, 16(4), 387-400.

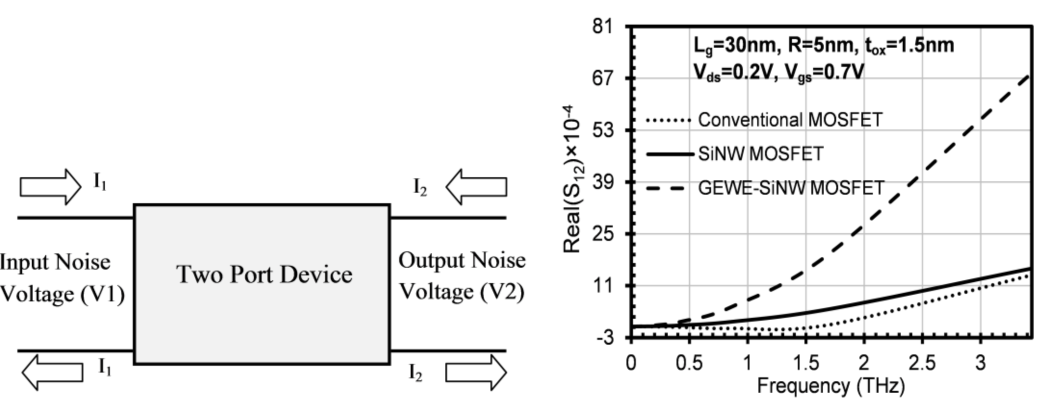
Zheng, C.-y. (2011) The using of dual-material gate MOSFET in suppressing short-channel effects: a review, *Electronics, Communications and Control (ICECC), 2011 International Conference on*. IEEE.

Zhou, W., Zhang, L., Chen, L., Xu, Y., Wu, W. & He, J. (2011) Simulation study on a new dual-material nanowire MOS surrounding-gate transistor. *Journal of nanoscience and nanotechnology*, 11(12), 11006-11010.

CHAPTER-4

Investigation of Small Signal and Noise Behaviour of GEWE-SiNW MOSFET for Low-Noise Amplifiers

- *Small signal behaviour in terms of scattering parameters and RF Noise performance of GEWE-SiNW MOSFET has been studied and the results so obtained are simultaneously compared with SiNW and Conventional MOSFET at THz frequency range.*
- *This work examines reflection and transmission coefficients; noise conductance, minimum noise figure and cross-correlation factor.*
- *Results reveal significant reduction in input/output reflection coefficient and an increase in forward/reverse transmission coefficient owing to improved transconductance in GEWE-SiNW in comparison to conventional counterparts.*
- *It is also observed that minimum noise figure (NF_{MIN}) and noise conductance (NC) of GEWE-SiNW is reduced by 17.4% and 31.2% respectively in comparison to SiNW, thus, fortifying its potential application for Low Noise Amplifiers (LNAs) at radio frequencies.*
- *Moreover, efficacy of gate metal workfunction engineering is also studied, and the results validate that tuning of workfunction difference improves the device small signal behaviour and noise performance.*



4.1 INTRODUCTION

As the MOSFET dimensions shrink, more of high order effects become apparent and have important influence in the device performance specifically at HF (Woerlee et al, 2001). Thus, the proper determination of the associated parameters is necessary to accurately predict the device's behavior under a wide variety of conditions. The most appropriate method to examine small signal behaviour of MOSFET at high frequencies involves S-parameter measurements (Matthews, 1955), which can be accurately measured with a vector network analyzer (VNA) and subsequently, simple conversion equations allow obtaining the other equivalent representations, like impedance (Z), admittance (Y), and hybrid (H) parameters (Álvarez-Botero et al, 2011; Pozar, 2009). S-parameters are most commonly employed for those networks that are operating at RF and microwave frequencies where signal power and energy analysis are more easily computed than voltages and currents. Since, at high frequency it is very difficult to estimate current and voltages. Short and open circuits (used by definitions of most n-port parameters) are hard to realize at high frequencies (Lovelace et al, 1994). As a result, microwave engineers work with S parameters, which utilises waves and matched terminations (normally 50Ω). This approach also minimizes reflection problems (Liou & Schwierz, 2003). They are theoretically simple, methodically expedient, and providing great insight of device under test. When an RF signal incident on port 1, some part of that signal gets returned back out of the incident port where as some of it go in into the incident port and then exit at port 2 (Deen & Fjeldly, 2002) as shown in Fig. 4.01.

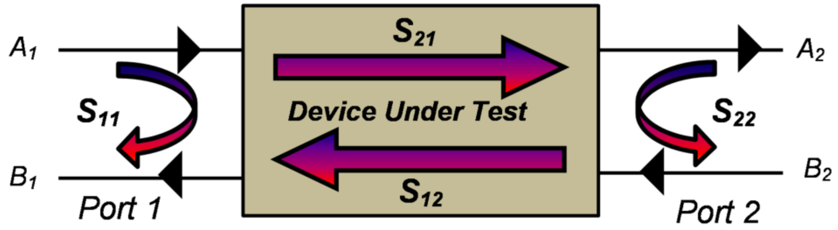


Figure 4.01: A two port S-parameters showing reflection and transmission coefficients (Mavaddat, 1996)

$$\text{Forward Return Loss} = S_{11} = \left.\frac{B_1}{A_1}\right|_{A_2 = 0} \quad \text{… (4.01)}$$

$$\text{Forward Insertion Loss} = S_{21} = \left.\frac{B_2}{A_1}\right|_{A_2 = 0} \quad \text{… (4.02)}$$

$$\text{Reverse Return Loss} = S_{22} = \left.\frac{B_2}{A_2}\right|_{A_1 = 0} \quad \text{… (4.03)}$$

$$\text{Reverse Insertion Loss} = S_{12} = \left.\frac{B_1}{A_2}\right|_{A_1 = 0} \quad \text{… (4.04)}$$

For a two-port device as shown in Fig. 4.01 there are four S-parameters i.e., S_{11}, S_{21}, S_{12}, and S_{22}. S_{11} and S_{22} are simply the forward and reverse reflection coefficients, with the opposite port terminated in Z_0 (usually 50 ohms.) S_{21} and S_{12} are simply the forward and reverse gains assuming a Z_0 source and load (again usually 50 ohms). S-parameters are complex numbers, having real and imaginary parts or magnitude and phase parts, because both the magnitude and phase of the incident signal are changed by the network (Vittoria, 1998). The benefit of S-parameters does not only lie in the complete description of the device performance at microwave frequencies but also its capability to convert to other parameters such as hybrid (H) or admittance (Y) parameters. Likewise, stability factor (K) and many gain and power parameters can

also be computed using S-parameters (Nguyen, 2015). Moreover, the measured S-parameters of multiple devices can be cascaded to predict the overall system performance at RF/Microwave. The de-embedding of extrinsic parasitics is omitted in this chapter, and it will be emphasized in chapter-5

Moreover, it has been studied that short channel MOSFETs have comparatively higher channel thermal noise than long channel MOSFET devices in the strong inversion and saturation region (Asgaran et al, 2004; Chen & Deen, 2002; Han et al, 2004). This appearance is due to short channel effects (SCEs) associated with channel length modulation (CLM), velocity saturation (VS), and hot-carrier effect. As a result of accounting for these effects, it was shown that the major contribution to the drain current noise mainly comes from the linear channel region (Chen & Deen, 2002). However, this issue of surplus noise is still an active area of investigation (Tsividis & McAndrew, 2011; Yu, 2013) for RF amplifiers and receivers for communication. Therfore, in this chapter, the small signal behaviour in terms of scattering (S) parameters is discussed by an extensive 3D TCAD device simulation at 300K. The results so obtained are compared with conventional MOSFET and SiNW MOSFET at THz frequency range. Further, effect of channel length (L_g), channel doping (N_a) and efficacy of GEWE scheme is also examined on the S-parameters of GEWE-SiNW MOSFET. In the latter part of chapter, Noise performance of GEWE-SiNW have been studied by exploring various parameters like Minimum Noise Figure (NF_{MIN}), Noise Conductance (N.C) and Cross Correlation. The effect of gate metal workfunction at the drain end on Noise FOMs has also been discussed in this chapter.

4.2 Device Structure and Physical Models

Fig. 4.02 (a-b) shows the simulated device structure of n-type conventional, SiNW and GEWE SiNW MOSFET respectively. GEWE-SiNW consists of two gate metals M1 and M2 of length L1 and L2 of 15nm each respectively as shown in Fig.4.02 (c) which is towards the 45nm node CMOS technology as stated in ITRS Roadmap (Hu, 2010). The radius of SiNW is 5nm, the oxide thickness is 1.5 nm of permittivity 3.9, source and drain region are of n-type with uniform doping profiles of $5\times10^{19}cm^{-3}$ of length 5nm for all device designs. The doping profile is assumed to be uniform. The metal gate work function is 4.8eV for conventional and SiNW MOSFET; for GEWE metal gate workfunction at the source end (Φ_{M1}) is 4.8 eV (Au) and metal gate work function at the drain end (Φ_{M2}) is 4.4 eV (Ti). A schematic cross-sectional view of simulated device structure i.e. GEWE-SiNW MOSFET having gate length 30nm as shown in Fig. 4.02(d).

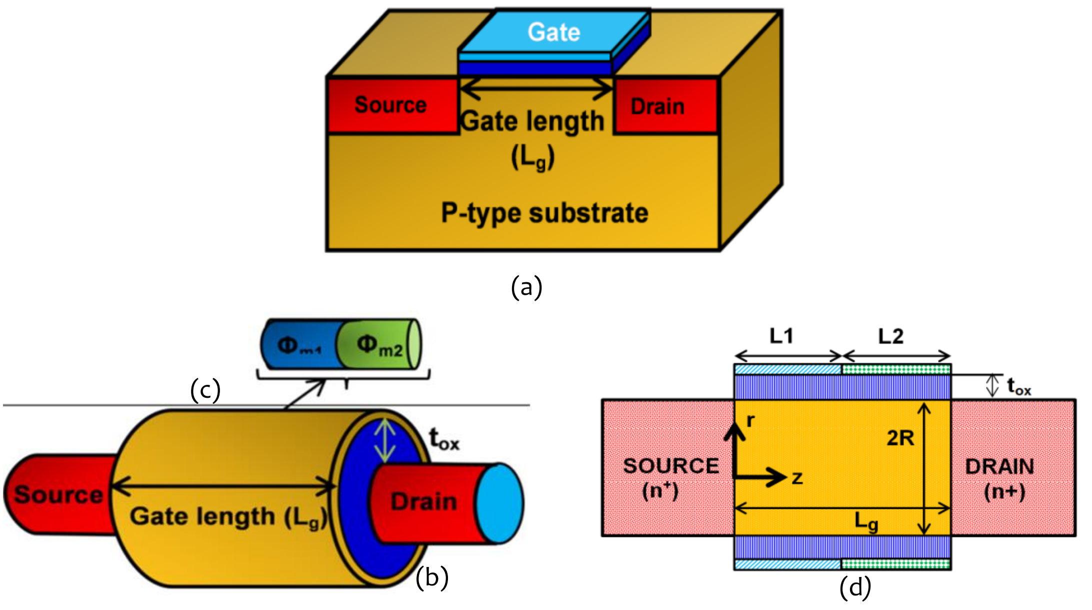


Figure 4.02: Simulated Device Structure of (a) Conventional MOSFET, (b) SiNW MOSFET, (c) GEWE-SiNW MOSFET and (d) Schematic Cross-sectional view of GEWE-SiNW MOSFET

All the simulations have been performed using physical models accounting for the electric field-dependent and concentration-dependent carrier mobilities, Shockley–Read–Hall recombination/generation with doping dependent carrier lifetime, inversion layer Lombardi CVT mobility model, where in concentration-dependent mobility, high field saturation model are all included (SILVACO, 2016). To incorporate all non-local effects and quantum effects, Bohm Quantum Potential (BQP) Model with alpha=0.5 and gamma=1.2 was used to take quantum mechanical effects into consideration as previously discussed in Chapter-3.

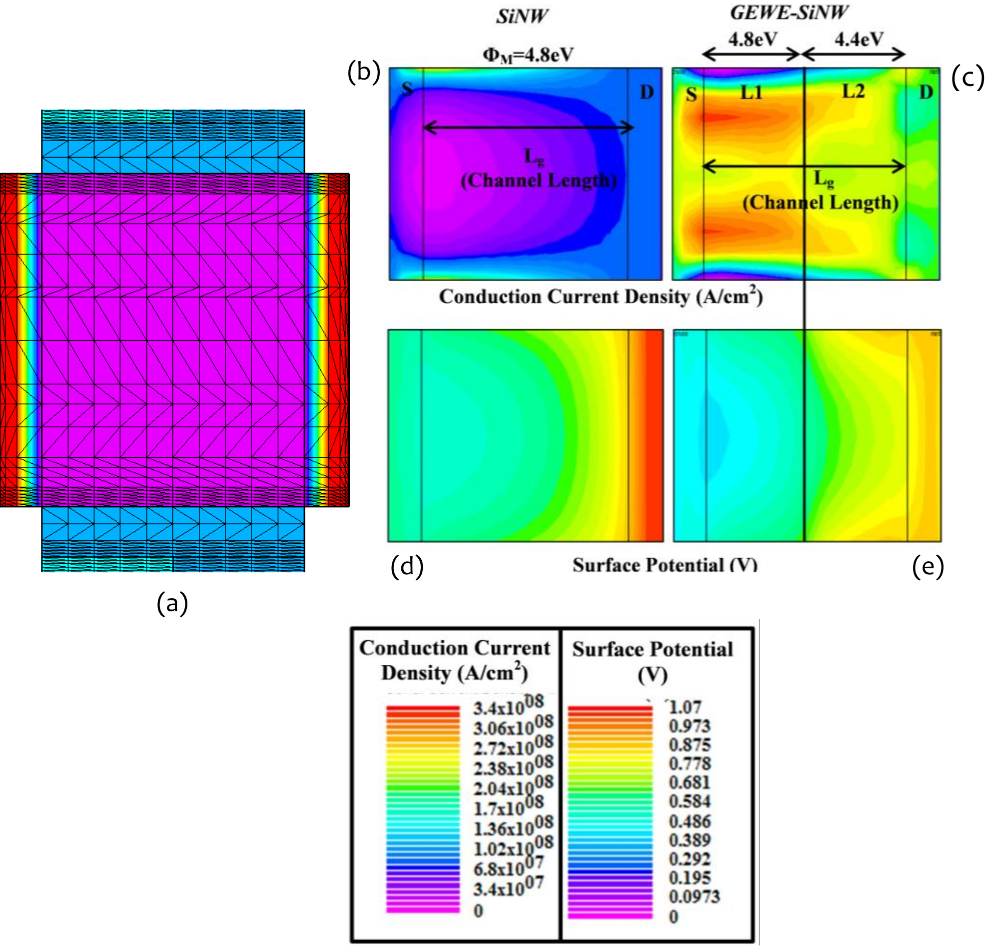


Figure 4.03: (a) 2-D Cross-sectional view of Meshed Structure of GEWE SiNW MOSFET, (b-c) Contours distribution of Conduction current density and (d-e) Surface Potential along the channel for SiNW and GEWE-SiNW MOSFET respectively. (Gupta & Chaujar, 2016a)

Default simulator coefficients for all parameters have been employed. In order to fairly analyze the device performances, all the three devices are optimized to have the same threshold voltage, i.e., 0.32V by changing channel doping and keeping the doping of source and drain constant of uniform doping i.e. 5e19cm^{-3}. Here, threshold voltage (V_{th}) is defined as the minimum gate to source voltage (V_{gs}) at which current starts flowing between source and drain or it is defined as that voltage at which I_{ds}=10^{-8}A. For more precise calculations in nanoscale MOSFET, mesh size should be considered fine at the junctions and in channel regions as shown in Fig. 4.03(a) (Rahimian & Orouji, 2013). The contour plot of conduction current density and surface potential along the channel of SiNW and GEWE-SiNW are shown in Fig. 4.03(b-c) and 4.03(d-e) respectively. As is evident from contours that with the incorporation of GEWE scheme, conduction density of electron enhances which results in higher current driving capability in comparison to SiNW MOSFET. The calibration of model parameters used in the simulation has been performed according to the experimental results (Suk et al, 2005) using above mentioned models.

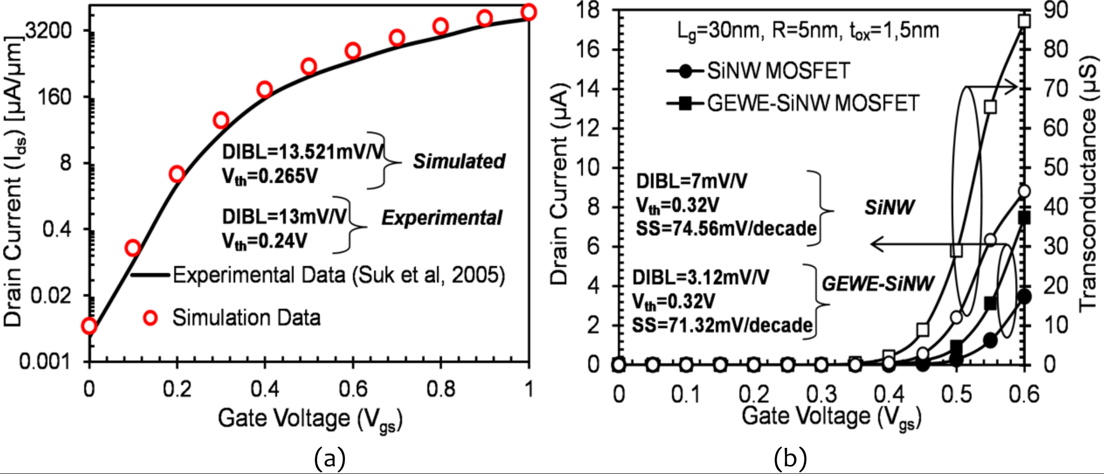


Figure 4.04: (a) Calibration with the experimental results. I_{ds}-V_{gs} characteristics of 5nm radius with 30nm short channel cylindrical gate SiNW MOSFET with t_{ox}=2nm and TiN as metal gate at V_{ds}=1.0V, (b) I_{ds}-V_{gs} and transconductance characteristics of GEWE-SiNW MOSFET at V_{ds}=0.2V

Fig. 4.04(a) shows the simulated I_{ds}-V_{gs} characteristics of 30nm short channel cylindrical gate SiNW MOSFET at V_{ds}=1.0V and the transfer characteristics of extracted experimental data. The results are in close proximity, thus validating the choice of models parameters taken in simulation. Fig. 4.04(b) shows the transfer characteristics of GEWE SiNW and SiNW MOSFET at 0.2V drain voltage. As evident from the figure that with the integration of gate engineering scheme, the on-current of GEWE-SiNW increases 2.2 times in comparison to SiNW MOSFET due to redistribution of electric field in the channel which enhances the mobility and hence improves the driving current capability of a device. The MOSFET transconductance is defined by, $g_m = \partial I_{ds}/\partial V_{gs}$ where I_{ds} drain current and V_{gs} (gate voltage). It is typically measured in the linear regime and used as indirect monitor of inversion carrier mobility. Transconductance is useful in designing linear amplifiers and larger the transconductance for a device, the greater the gain (amplification) it is capable of delivering, when all other factors are held constant. As is apparent from Fig. 4.04(b), the transconductance is much higher in case of GEWE-SiNW MOSFET owing to enhancement in drain current. Moreover, noteworthy improvement in DIBL (or barrier lowering) is also observed in GEWE-SiNW due to step potential profile at the interface of dissimilar metal gates as is shown in contours of Fig. 4.03(d-e). Sub-threshold Swing (SS) also reduces in case of GEWE-SiNW as shown in Fig. 4.04(b), thus implies that GEWE-SiNW is immune to SCEs in comparison to SiNW MOSFET

4.3 RESULTS AND DISCUSSION

In this section, the small signal behaviour of GEWE-SiNW MOSEFT in terms of scattering (reflection and transmission coefficients) parameters is investigated.

Further, the efficacy of gate metal engineering, channel length and channel doping are also studied on S-parameters of GEWE-SiNW in THz frequency regime.

4.3.1 Scattering Parameter Analysis

S_{11} and S_{22} are defined as input and output reflection coefficient at port 1 and port 2 respectively and is a measure of quality of match between the port and terminating impedance. S_{11} is the most commonly used parameter to characterize small signal behaviour of active device at high frequency. Matching is generally required in RF circuits. When there is a perfect match, there is no reflected wave and reflection coefficient is zero. Fig.4.05 (a-b) shows the real part of input and output reflection coefficient of conventional, SiNW and GEWE-SiNW MOSFET.

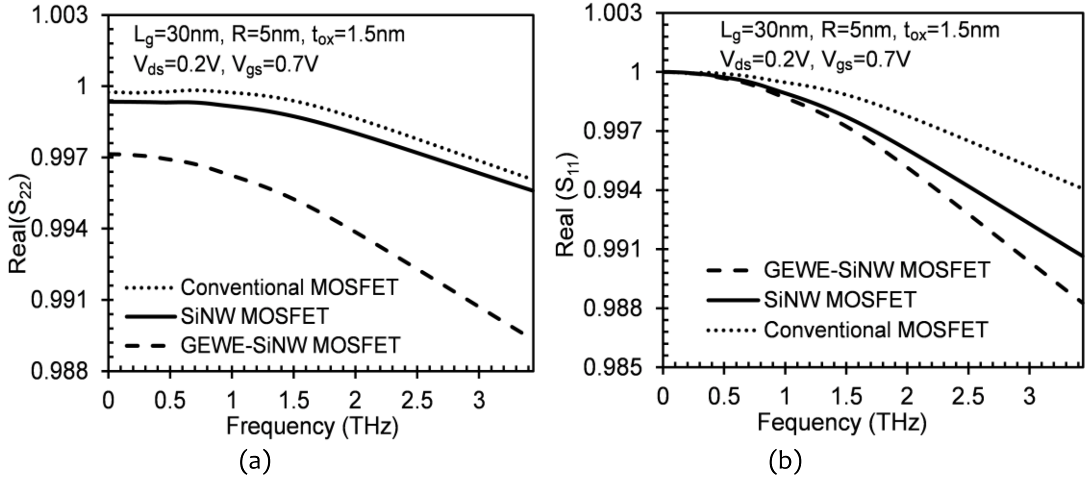


Figure 4.05: (a) Real part of input reflection coefficient, (b) Real part of output reflection coefficient as a function of frequency for Conventional, SiNW and GEWE-SiNW MOSFET at V_{gs}=0.7 V and V_{ds}=0.2 V.

As is evident from figure that both input and output coefficient decreases with increase in frequency and decrement in reflection coefficient is more in GEWE-SiNW as compared to its counterparts. Due to the incorporation of two dissimilar metals onto cylindrical gate, current driving capability increases due to redistribution of electric

field at the interface of two metals owing to step potential which causes enhancement in carrier velocity and thus current driving capability increases that result in increased transconductance and hence leading to improvement in reflection coefficient.

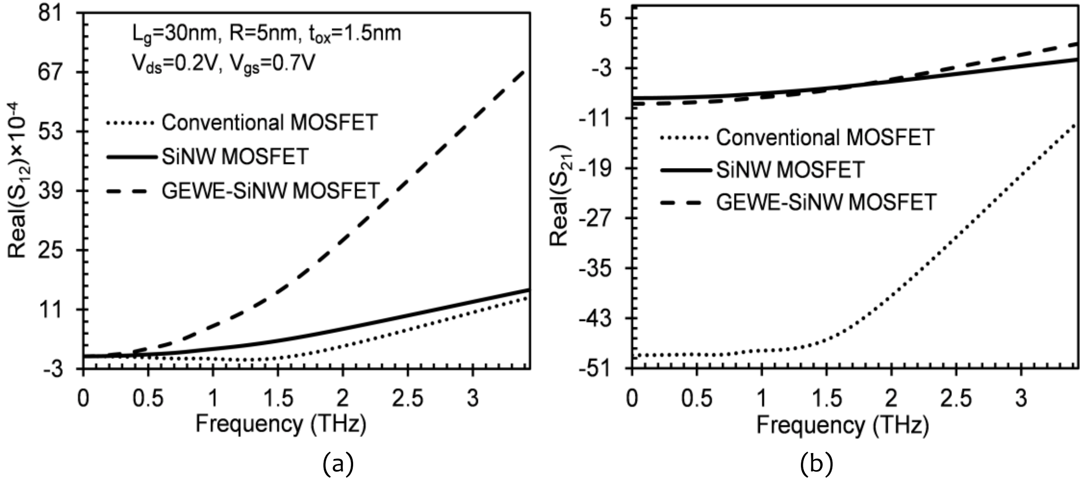


Figure 4.06: (a) Real part of reverse transmission coefficient, (b) Real part of forward transmission coefficient as a function of frequency for Conventional, SiNW and GEWE-SiNW MOSFET at V_{gs}=0.7 V and V_{ds}=0.2 V.

As the matching between the ports and characteristic impedance improve, reflection coefficient decreases due to smaller reflected power. The reverse isolation parameter S_{12} determines the measure of feedback from the output of an amplifier to the input and thus supremacies its stability at high frequency (Belostotski & Haslett, 2008). Fig. 4.06(a) shows the variation of real part of reverse transmission coefficient of Conventional, SiNW and GEWE-SiNW MOSFET. Result unveils that the reverse transmission coefficient of GEWE-SiNW increases to 5.07 and 4.2 times at 3.4 THz due to enhancement of transconductance in comparison to conventional and SiNW MOSFET respectively. Fig. 4.06(b) shows the forward transmission coefficient as a function of frequency which is also defined as forward gain of a two port device. The S_{21} (voltage gain) increases to 7.14 times in SiNW and 13.5 times in GEWE-SiNW

MOSFET compared to conventional MOSFET as depicted in Fig. 4.06(b). This enhancement is due to cylindrical gate designs and GEWE engineering scheme which enhances device performance and alleviates SCEs. Table 4.01 compares the value of S_{12} and S_{21} of GEWE-SiNW MOSFET at f_T, f_{MAX} (found in previous chapter) and at 3.4 THz (where the effect of Small signal behaviour is more prominent).

Table 4.01: Extracted S-parameters of GEWE-SiNW and SiNW MOSFET

S-Parameters / Frequency	S_{12} of GEWE-SiNW MOSFET w.r.t		S_{21} of GEWE-SiNW MOSFET w.r.t	
	SiNW MOSFET (times)	*Conventional MOSFET (times)*	*SiNW MOSFET (times)*	*Conventional MOSFET (times)*
f_T=1110GHz	**4.25**	**8.5**	**1.057**	**6.928**
f_{MAX}=1440GHz	**4.375**	**13.5**	**1.061**	**7.23**
At 3400 GHz	**4.2**	**5.07**	**7.14**	**13.5**

A. Effect of Gate Metal Workfunction (Φ_{M2})

As studied in previous chapter, the performance of GEWE-SiNW MOSFET augments with modulating the workfunction difference of metal gates. Therefore, in this section influence of metal gate workfunction on S-parameters of GEWE-SiNW MOSFET is investigated at THz frequency range. Fig. 4.07(a) and 4.07(b) shows the input and output reflection coefficient of GEWE-SiNW at different metal gate workfunction of drain end. As is evident from figure 4.07(a), the effect of workfunction difference is very less on input reflection coefficient and also its value increases with increase in workfunction difference which is not desirable. Further, output reflection coefficient decreases with increase in workfunction difference as reflected through figure 4.07(b) which is desirable for RF amplifiers and receivers.

This is due to excellent gate control which results in higher transconductance and hence improves reflection coefficient.

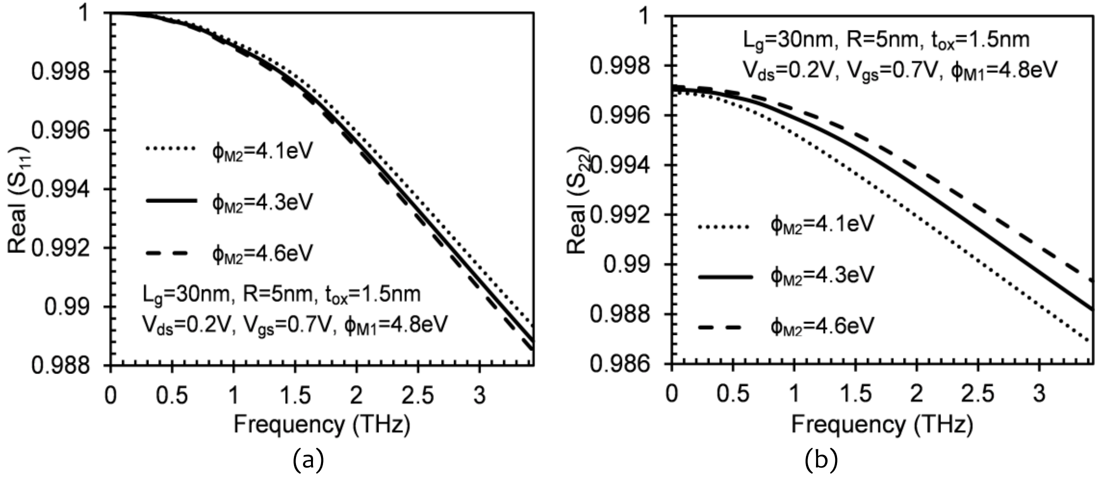


Fig.4.07: (a) Real part of input reflection coefficient, (b) Real part of output reflection coefficient as a function of frequency for different metal gate workfunction at the drain side at V_{gs}=0.7 V and V_{ds}=0.2 V

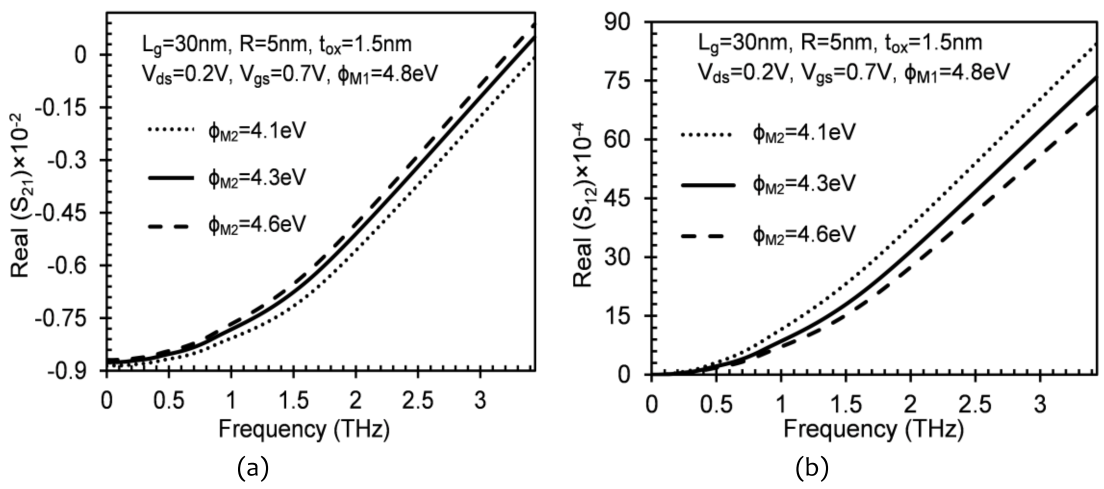


Figure 4.08: (a-b) Real part of reverse transmission coefficient, (b) Real part of forward transmission coefficient as a function of frequency for different metal gate workfunction at the drain side at V_{gs}=0.7 V and V_{ds}=0.2 V

As we increase the metal gate workfunction difference to 0.7eV, reverse transmission coefficients increases to 1.25 times at 3.4 THz compared to other workfunction

difference due to improvement in on-current and reduced short channel effects owing to improvement of screening effect with increase in metal workfunction difference as is evident from Fig. 4.08 (a). Whereas, forward transmission coefficient decreases as we increase the workfunction difference which is not desirable at THz. But the deprivation is very less as is shown in Fig. 4.08(b). Thus, there is a need to optimize the value of metal gate workfunction for optimal small signal performance for RF amplifier and high speed applications.

B. Effect of Channel Length (L_g)

The effect of downscaling of channel length is investigated in this subsection as downscaling improves the HF performance of CMOS devices.

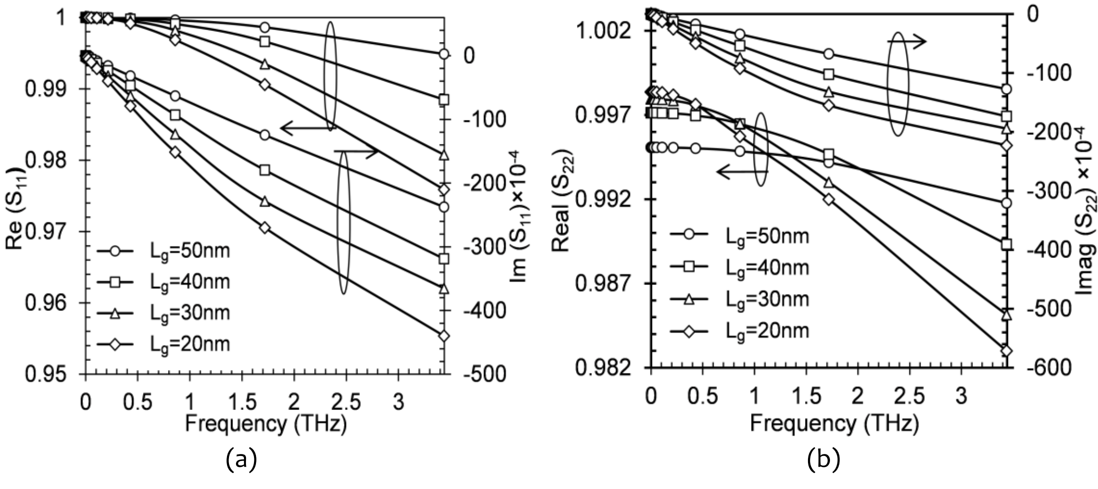


Figure 4.09: (a) Real and Imaginary part of input reflection coefficient (S_{11}), (b) Real and Imaginary part of output reflection coefficient (S_{22}) as a function of frequency for GEWE-SiNW MOSFET at different channel length (L_g) at V_{gs}=0.7 V and V_{ds}=0.2 V

For improved RF performance in terms of S-parameters, GEWE-SiNW MOSFET has been studied under the different channel length (L_g=20, 30, 40 and 50nm) at frequency range from 100Hz to several THz. Fig. 4.09(a) and 4.09(b) shows the variation of S-parameters (S_{11} and S_{22}) both in real and imaginary form at different

channel lengths as a function of frequency ranging from 0 to 3.5 THz. It is observed from Fig. 4.09(a-b), both input reflection scattering coefficient (S_{11}) at port 1 and output reflection scattering coefficient (S_{22}) at port 2 enhances as gate length reduces down to 20nm. This is because the drain current depends on the channel length. As gate length shortens, current increases due to excellent gate controllability over channel that results in increased transconductance, leading to improvement in reflection coefficients. Additionally, value of S_{11} and S_{22} are perfectly matched at THz frequency, which is an important part of amplifier design in RF applications. Many applications require impedance matching to ensure the best possible power transfer at a certain frequency.

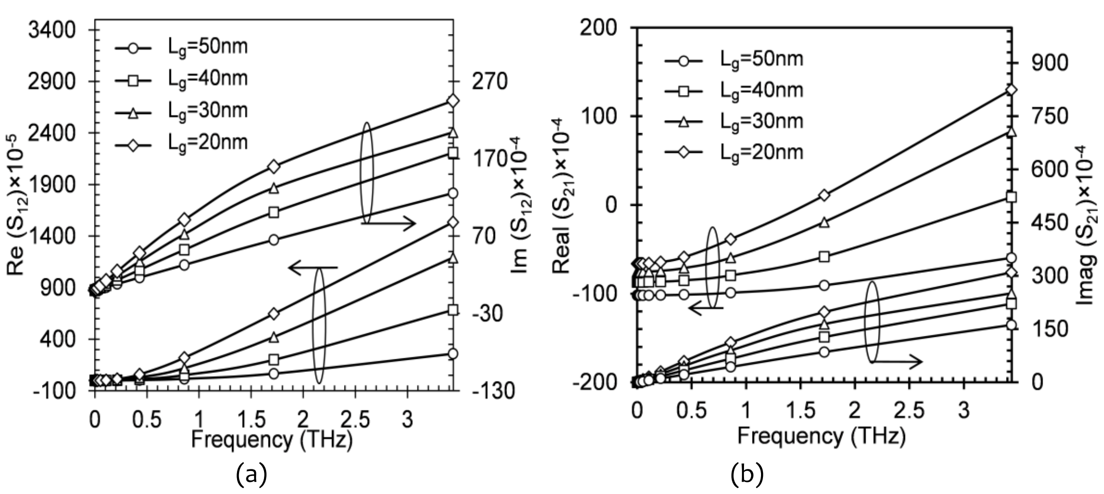


***Figure 4.10:** (a) Real and Imaginary part of reverse transmission coefficient (S_{21}) and (b) Real and Imaginary part of forward transmission coefficient (S_{22}) as a function of frequency for GEWE-SiNW MOSFET at different channel length at V_{gs}=0.7 V and V_{ds}=0.2 V*

It is also found that with the reduction in channel length, real part of the reverse transmission coefficient (S_{12}) shifts towards positive value which is most desirable as evident from figure 4.10(a). This reduction is due to cylindrical gate design which enhances device performance as we scale down the gate length and also due to the

incorporation of two dissimilar metal gates. The reverse isolation parameter (S_{12}) governs the level of feedback from the output of an amplifier to the input and therefore influences its stability at high frequency. Forward transmission coefficient (S_{21}) also improves with decrease in channel length as it is evident from Fig. 4.10(b). This makes GEWE-SiNW MOSFET suitable for microwave amplifier and oscillator design.

C. Effect of Channel Doping (N_a)

From Fig. 4.11(a-b), it is clearly shown that as the channel doping increases, both the input and output reflection coefficient in real and imaginary form decreases. As the channel doping of GEWE-SiNW MOSFET increases from 1e15 to 5e17 cm^{-3}, the inversion charge density decreases which increases the threshold voltage as a result of which the on-state current decreases. As on-state current decreases, the transconductance also decreases which leads to reduction in reflection parameters.

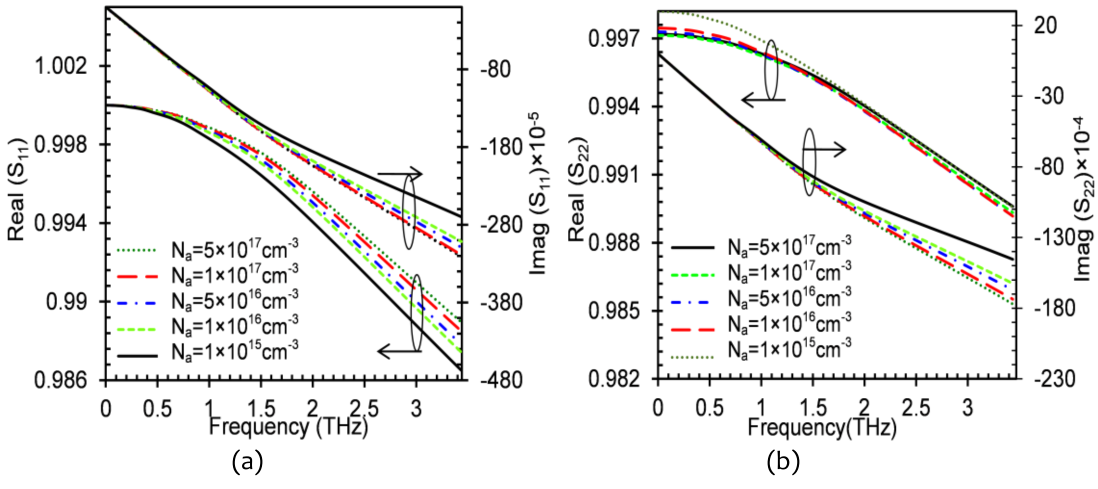


Figure 4.11: (a) Real and Imaginary part of input reflection coefficient (S_{11}) and (b) Real and Imaginary part of output reflection coefficient (S_{22}) as a function of frequency for GEWE-SiNW MOSFET at different channel doping at V_{gs}=0.7 V and V_{ds}=0.2 V

This reduction is more pronounced at very high frequency (3-4 THz) as is apparent from the Figure 4.11(a-b). In most amplifiers at high frequency, isolation of source and load is an important consideration. An amplifier which has lower value of $|S_{12}|$ can be used as a buffer amplifier. Fig. 4.12 (a-b) unveils the real and imaginary part of transmission coefficient at different channel doping concentrations. As is evident from the figures that transmission coefficient increases with increase in channel doping concentration. An amplifier with input and output ports ideally secluded from each other would have infinite scalar log magnitude isolation or the linear magnitude of S_{12} would be zero. Such an amplifier is said to be unilateral. Hence, with proper tuning of channel length and channel doping concentration in GEWE-SiNW MOSFET, it can be used as a buffer amplifier at very high frequency.

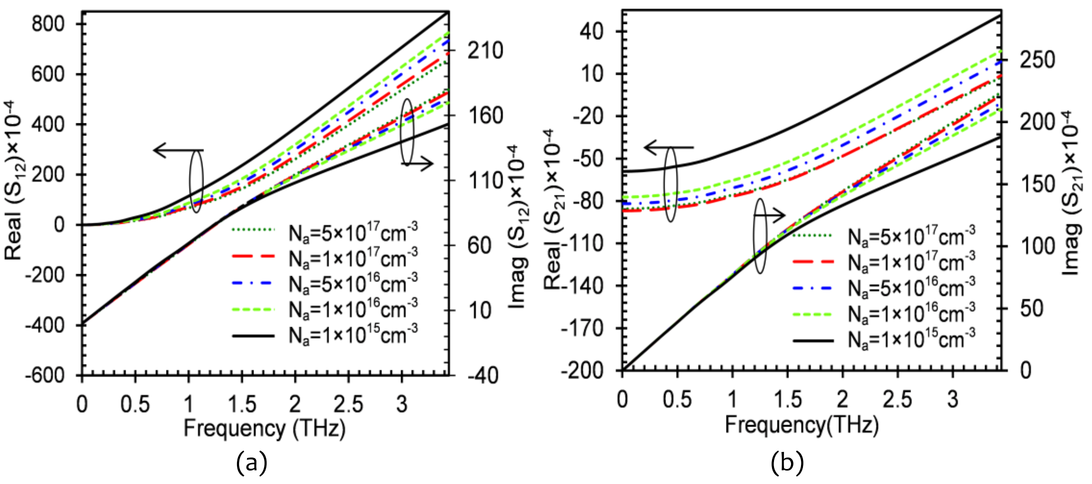


***Figure 4.12:** (a) Real and Imaginary part of reverse transmission coefficient (S_{12}), (b) Real and Imaginary part of forward transmission coefficient (S_{21})as a function of frequency for GEWE SiNW MOSFET at different channel doping at V_{gs}=0.7 V and V_{ds}=0.2*

4.3.2 Noise Metrics

Further, for the design of CMOS RF circuits, investigation of noise conductance and noise figure (Coquand et al) is of paramount importance at high frequency. The

effectiveness of Low Noise Amplifier (LNA) is determined by an important metric called Noise Figure. Noise Conductance is generally used to estimate the power spectral density of noise current generators. Low noise conductance is required in RF amplifiers and LNAs. Fig. 4.13 depicts the noise conductance as a function of frequency for conventional, SiNW, GEWE-SiNW MOSFET. In GEWE-SiNW MOSFET, noise conductance decreases due to reduced hot-carrier phenomenon which results in lower impact ionization of carriers at the Si-SiO_2 interface and thus reduces noise.

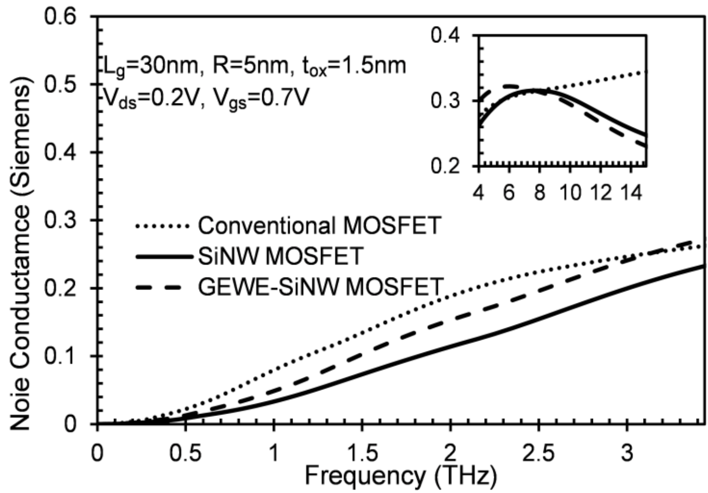


Figure 4.13: Noise Conductance as a function of frequency for Conventional, SiNW and GEWE-SiNW MOSFET at V_{gs}=0.7 V and V_{ds}=0.2V

Additionally, as silicon nanowire phonon-phonon scattering is less observed, noise conductance also decreases. Hence, its dominance, for low power and low noise applications where noise is a major concern, is significant. Noise figure is an estimation of deterioration of signal to noise ratio caused by a component in RF signal chains. It is generally used to evaluate the performance of an amplifier or a radio receiver, with lower values specifying better performance. Fig.4.14 displays the

variation of NF_{MIN} as a function of frequency. As is evident from figure that minimum noise figure decreases with increase in frequency but this decline is more prominent in GEWE SiNW MOSFET.

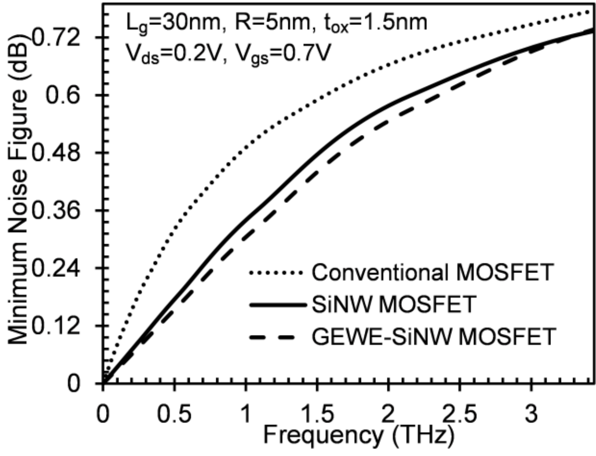
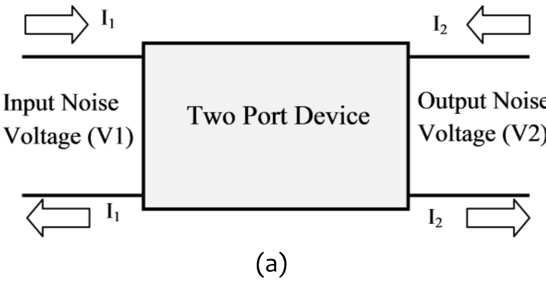
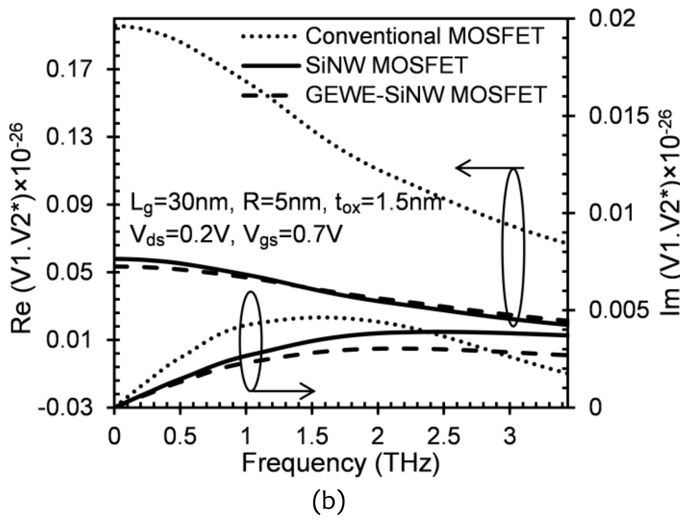


Figure 4.14: Minimum Noise Figure as a function of frequency for Conventional, SiNW and GEWE-SiNW MOSFET at V_{gs}=0.7 V and V_{ds}=0.2V

The minimum noise figure is proportional to intrinsic gate resistance and inversely proportional to transconductance (Golio, 2003). In GEWE-SiNW, there is a step potential created at the interface of two dissimilar metals workfunction which redistributes the electric field in the channel and hence, increases the carrier efficiency which results in improved transconductance and low noise figure in comparison to its conventional counterparts. A low noise figure reflects that a very little noise is being added by the network. Thus, GEWE-SiNW MOSFET is a reliable candidate for low noise amplifiers (LNAs).



(a)



(b)

Figure 4.15: (a) MOSFET as a two port device where the input noise is replaced by a voltage V1 and the noise received at output is replaced by V_2, (b) Cross correlation as a function of frequency for Conventional, SiNW and GEWE-SiNW MOSFET at V_{gs}=0.7V and V_{ds}=0.2V.

Fig.4.15 (a) depicts MOSFET as a two port device where noise induced at the gate terminal is separated from the MOSFET and is depicted by V1 and the noise received at the output is depicted by V2 (Pozar, 2009). It is clearly shown in Fig.4.15 (b) that real and imaginary part of cross-correlation is reduced in comparison to conventional devices with change in frequency. Since, with the incorporation of GEWE scheme, electric field reduces at the drain end and therefore less isotropic scattering is observed. Due to this reduced isotropic scattering, the scattering mechanism is not so effective in breaking the correlation between gate current and drain current (Pozar, 2009). Thus, cross correlation (i.e. V1.V2*) reduces in GEWE SiNW-MOSFET at higher frequencies. Moreover, noise performance of GEWE-SiNW MOSFET is further enhanced by tuning the workfunction difference by keeping the workfunction at the source side constant and varying the workfunction at the drain end. As we increase the workfunction difference to 0.7eV, minimum noise figure decreases in

comparison to 0.2eV as is evident from Fig. 4.16. It is very clear that change is observable at very high frequency (around 2.5-3THz); around 7.82% decrement is observed when workfunction at the drain end is 4.1 eV owing to enhancement in transconductance and carrier transport efficiency.

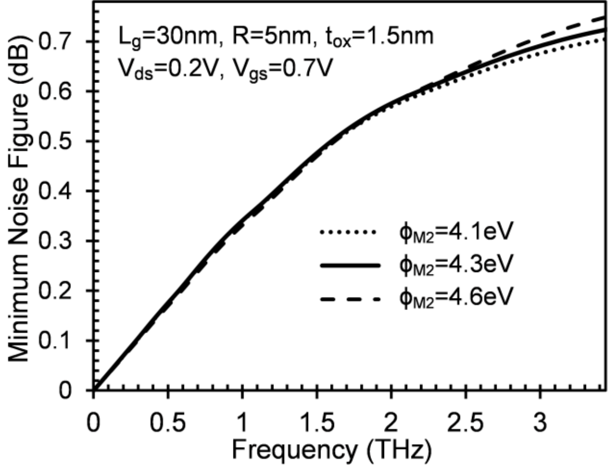


Figure 4.16: Minimum Noise Figure as a function of frequency for GEWE-SiNW MOSFET for different gate metal workfunction values at drain end.

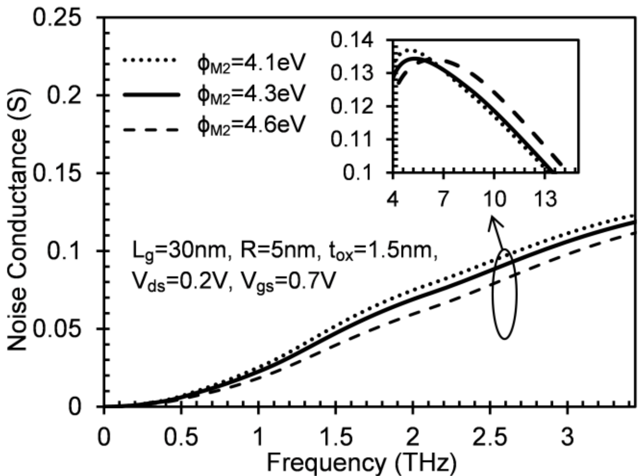


Figure 4.17: Noise Conductance as a function of frequency for GEWE-SiNW MOSFET for different gate metal workfunction values at drain end.

Moreover, Noise Conductance also decreases with increase in workfunction difference but more prominent at high frequency as is evident from inset of Fig. 4.17.

Therefore, noise FOMs are not affected much with change in workfunction difference. Another parameter which decides the noise performance of a device is cross-correlation factor. Fig. 4.18 shows the cross-correlation factor of GEWE-SiNW MOSFET of different metal gate workfunction at drain end and result shows that with workfunction 4.1eV, electric field reduces at the drain end which results in less scattering of carriers and thus correlation between input and output is less observed which is desirable for RF communication.

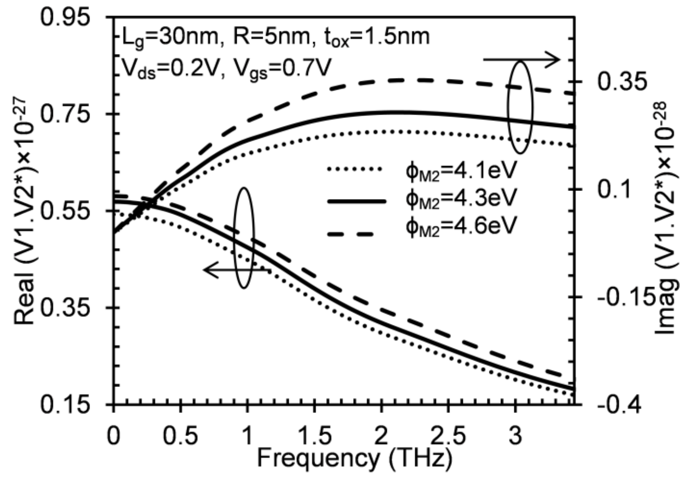


Figure 4.18: Cross correlation as a function of frequency for GEWE-SiNW MOSFET for different gate metal workfunction values at drain end.

4.4 SUMMARY

In this chapter, a comprehensive small-signal behaviour and noise analysis of GEWE-SiNW MOSFET is explained in terms of S-parameters and noise FOMs at THz frequency range. The numerical simulation results so obtained shows that with the incorporation of GEWE scheme onto SiNW, reflection coefficient decreases and transmission coefficient increases in comparison with SiNW and conventional MOSFET. Likewise, tuning of gate length and channel doping enhances the S-

parameter characteristics for GEWE-SiNW MOSFET. This is because, decrease in gate length and decrease in channel doping results in the increased driving-current which enhances transconductance and thus results improvement in high frequency device behaviour. In addition, prominent reduction in noise metrics such as minimum noise figure (by 18%), noise conductance (by 35%) and cross-correlation (by 78%) of GEWE-SiNW MOSFET in comparison to SiNW and Conventional MOSFET has been observed. This makes GEWE-SiNW MOSFET appropriate for microwave amplifier and oscillator designs. Moreover, tuning of gate metal workfunction difference further advances the noise metrics due to reduction in SCEs and improvement in transconductance but degrades the forward gain (S_{21}). Thus, we should choose the optimum value of gate metal workfunction for better device performance at HF communication circuits and LNAs.

The investigation carried over in the chapter 3 and 4 are circumscribed to intrinsic components of MOSFET only where the external components were not taken into account. However, at GHz frequency range, the importance of extrinsic component (the part outside the channel region) dominates to that of its intrinsic counterpart. Therefore, there is a need for an RF model which should consider the behaviour of both the intrinsic and the extrinsic components of a device for achieving accurate and predictive results in the simulation of designed circuit. Thus, the next chapter discusses the impact of extrinsic and intrinsic parameters of GEWE-SiNW MOSFET at THz range and numerical modelling of small signal parameters such as Z and Y parameters has also been carried out.

4.5 REFERENCES

Álvarez-Botero, G., Torres-Torres, R. & Murphy-Arteaga, R. (2011) Using S-parameter measurements to determine the threshold voltage, gain factor, and mobility degradation factor for microwave bulk-MOSFETs. *Microelectronics Reliability*, 51(2), 342-349.

Asgaran, S., Deen, M. J. & Chen, C.-H. (2004) Analytical modeling of MOSFETs channel noise and noise parameters. *IEEE Transactions on Electron devices*, 51(12), 2109-2114.

Belostotski, L. & Haslett, J. W. (2008) Two-port noise figure optimization of source-degenerated cascode CMOS LNAs. *Analog Integrated Circuits and Signal Processing*, 55(2), 125-137.

Chen, C.-H. & Deen, M. J. (2002) Channel noise modeling of deep submicron MOSFETs. *IEEE Transactions on Electron Devices*, 49(8), 1484-1487.

Coquand, R., Barraud, S., Cassé, M., Leroux, P., Vizioz, C., Comboroure, C., Perreau, P., Ernst, E., Samson, M. P., Maffini-Alvaro, V., Tabone, C., Barnola, S., Munteanu, D., Ghibaudo, G., Monfray, S., Boeuf, F. & Poiroux, T. (2013) Scaling of high-κ/metal-gate TriGate SOI nanowire transistors down to 10nm width. *Solid-State Electronics*, 88, 32-36.

Deen, M. J. & Fjeldly, T. A. (2002) *CMOS RF Modeling, Characterization and Applications*, *24*World Scientific.

Golio, M. (2003) *Microwave and RF product applications*CRC Press.

Gupta, N. & Chaujar, R. (2016) Influence of gate metal engineering on small-signal and noise behaviour of silicon nanowire MOSFET for low-noise amplifiers. *Applied Physics A*, 122(8), 1-9.

Han, K., Shin, H. & Lee, K. (2004) Analytical drain thermal noise current model valid for deep submicron MOSFETs. *IEEE Transactions on Electron Devices*, 51(2), 261-269.

Hu, C. (2010) *Modern semiconductor devices for integrated circuits*Prentice Hall.

Liou, J. J. & Schwierz, F. (2003) RF MOSFET: recent advances, current status and future trends. *Solid-State Electronics*, 47(11), 1881-1895.

Lovelace, D., Costa, J. & Camilleri, N. (1994) Extracting small-signal model parameters of silicon MOSFET transistors, *Microwave Symposium Digest, 1994., IEEE MTT-S International*. IEEE.

Matthews, E. (1955) The use of scattering matrices in microwave circuits. *IRE transactions on microwave theory and techniques*, 3(3), 21-26.

Mavaddat, R. (1996) Network scattering parameters, 2, World Scientific.

Nguyen, C. (2015) Radio-frequency integrated-circuit engineering John Wiley & Sons.

Pozar, D. M. (2009) *Microwave engineering*John Wiley & Sons.

Rahimian, M. & Orouji, A. A. (2013) Investigation of the Electrical and Thermal Performance of SOI MOSFETs with Modified Channel Engineering. *Materials Science in Semiconductor Processing*, 16(5), 1248-1256.

SILVACO, I. (2016) ATLAS User's Manual. *Santa Clara, CA, Ver*, 5.

Suk, S. D., Lee, S.-Y., Kim, S.-M., Yoon, E.-J., Kim, M.-S., Li, M., Oh, C. W., Yeo, K. H., Kim, S. H. & Shin, D.-S. (2005) High performance 5 nm radius twin silicon nanowire MOSFET (TSNWFET): Fabrication on bulk Si wafer, characteristics, and reliability. *IEDM Tech. Dig*, 717-720.

Tsividis, Y. & McAndrew, C. (2011) *Operation and Modeling of the MOS Transistor*Oxford Univ. Press.

Vittoria, C. (1998) Elements of Microwave Networks: Basics of Microwave EngineeringWorld Scientific.

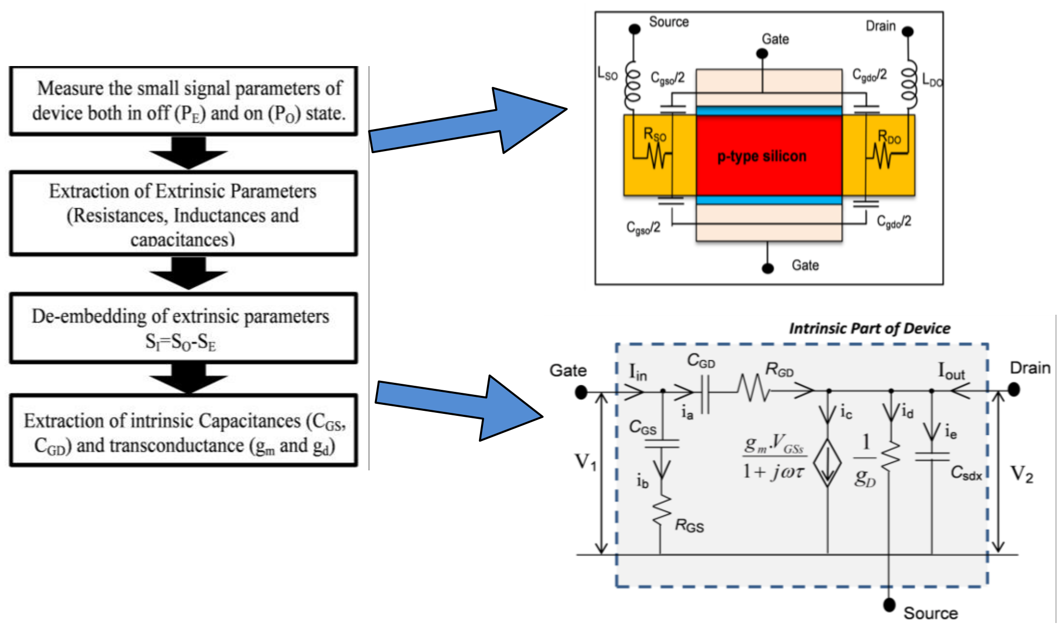
Woerlee, P. H., Knitel, M. J., Van Langevelde, R., Klaassen, D. B., Tiemeijer, L. F., Scholten, A. J. & Zegers-van Duijnhoven, A. T. (2001) RF-CMOS performance trends. *IEEE Transactions on Electron Devices*, 48(8), 1776-1782.

Yu, S. D. (2013) A Unified Channel Thermal Noise Model for Short Channel MOS Transistors. *JSTS: Journal of Semiconductor Technology and Science*, 13(3), 213-223.

CHAPTER-5

Extraction of Frequency Dependent Intrinsic and Extrinsic Parameters for GEWE-SiNW MOSFET

- *Intrinsic Parameters of Gate Electrode Workfunction Engineered (GEWE)-SiNW MOSFET is extracted by de-embedding the effect of extrinsic parameters.*
- *Effect of extrinsic parameters is less pronounced in GEWE-SiNW in comparison to conventional MOSFET SiNW MOSFET.*
- *Intrinsic Parameters such as transconductance, parasitic capacitance, distributed resistance, time constant and capacitance due to DIBL (Csdx) improves significantly by modulation of workfunction difference of gate metal.*
- *NQS small signal model of device structure has also been studied in terms of Z and Y parameters and the modeled results show good agreement with the 3D device simulation*
- *Thus, provides a detailed knowledge of GEWE-SiNW MOSFET to RF engineers at GHz range for RFIC design.*



5.1 INTRODUCTION

There is a requirement for accurate modeling of the non-linear transistor for RF and microwave circuits. As the intricacy of the HF circuits and systems continues to increase, there is a need to reduce the design cost, expand the performance and to fulfill the tight governing restraints on spurious discharges/emissions. For RF modeling, the transistor is usually divided into two parts: the intrinsic part, that includes the nonlinear elements describing the operation of the transistor, and the extrinsic part, that account for the metallization, substrate, and semiconductor connecting the intrinsic model to the outside world (Deen & Fjeldly, 2002; Wood et al, 2008). The intrinsic components are generally voltage-dependent, whereas the extrinsic components are usually considered to be independent of voltage, i.e., passive components. As the operating frequency increases into the GHz range, the importance of extrinsic component (the part outside the channel region) dominates to that of its intrinsic counterpart. Therefore, there is a need for an RF model which should consider the behavior of both the intrinsic and the extrinsic components of a device for achieving accurate and predictive results in the simulation of a designed circuit (Cheng et al, 2005; Ytterdal et al, 2003). Earlier work reported the effect of extrinsic and intrinsic parameters on CMOS RF performance (Woerlee et al, 2001). Moreover, in 2004, Alam et al., has also reported the extrinsic series resistance of RF MOSFET using small signal model (Alam & Armstrong, 2010). In addition to this, highly scaled CMOS device shows the short channel effects (SCEs) making them inapt for HF applications (Buss, 1999). To overcome such drawback, different device structures have been proposed to alleviate the issue of SCEs at high frequencies

(Kumar et al, 2016a; b; Subramanian et al, 2010). SiNW is the most promising candidate due to the stronger quantum confinement which results in higher mobility than bulk silicon and also due to its scalability to few nm which is challenging to obtain via conventional Silicon technology (Chen & Tan, 2014; Cui et al, 2003; Iwai et al, 2011).

Improved Analog and RF performance of SiNW has already been reported in the literature (Wang et al, 2007). Also, the effect of the source to drain capacitance due to DIBL in SiNW MOSFET is investigated by S. Cho et al. in 2010 (Cho et al, 2010). In 2011, S. Cho et al. has also examined the intrinsic and extrinsic parameters of junctionless SiNW including the small signal behavior in terms of Y-parameters (Cho et al, 2011). Gupta et al. in 2015, demonstrates that with the incorporation of GEWE on GAA SiNW, SCEs alleviates in terms of DIBL, Hot-Carrier (Gupta & Chaujar, 2014; Gupta et al, 2016) and also showed that GEWE-SiNW MOSFET achieved cut-off frequency in thousands of GHz making it suitable for RF/Microwave applications (Gupta et al, 2015a). Also, the effect of extrinsic and intrinsic parameters is not reported for GEWE-SiNW MOSFET till now. Therefore, in this work, the effect of extrinsic and intrinsic parameters are evaluated using Pinch-off Cold-FET method (Lai & Hsu, 2001) and then these parasitics are removed from the device under consideration that is known as de-embedding. Further, to examine the effect of device parameter on these parameters, metal gate engineering and bias variation is also observed. The small signal Z-and Y-components of GEWE-SiNW MOSFET is also studied by excluding the effect of extrinsic parameters.

5.2 Results and Discussion

5.2.1 Extrinsic Parameters

When MOSFET is operated at a low frequency, extrinsic parameters are behave as virtual components in the I-V expression to account for the DC voltage drop across these resistances and thus, obscure by the high-frequency signal. Therefore, external mechanisms for these components need to be included outside the intrinsic model to precisely describe the high-frequency device behavior (Iwai, 2009). Further, the extrinsic network plays a significant role in determining the scaling rules for the complete transistor model. The extrinsic network has to describe the electrical behavior of the device layout, and how this layout changes with device size determines how the extrinsic network component values scale. However, the detailed knowledge of extrinsic parameters is also essential for precise modeling of RF transistor, so that the extrinsic components can be de-embedded accurately to gain access of intrinsic behavior of the transistor.

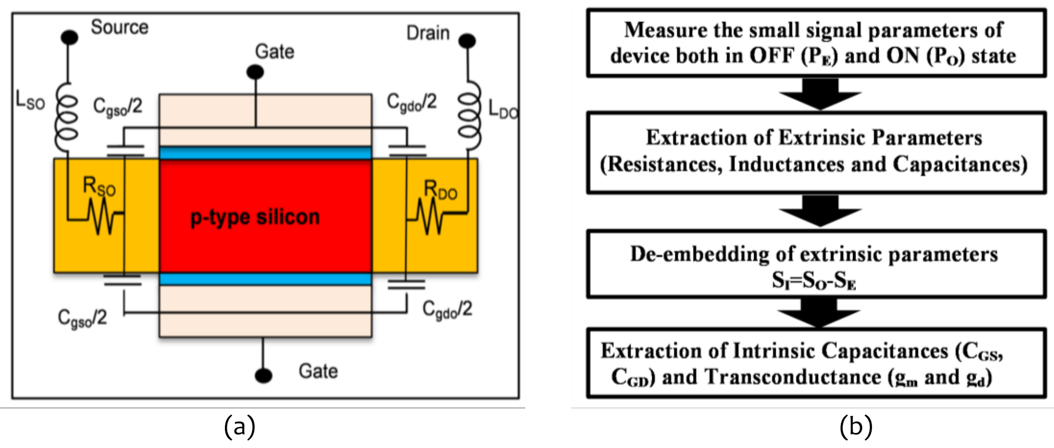


Figure 5.01: (a) Procedure of extracting extrinsic and intrinsic parameters. (b) Schematic representation of the Equivalent circuit of SiNW MOSFET in a cold FET pinch-off condition (V_{gs}=0V, V_{ds}=0)

For extracting the extrinsic parameters, the MOSFET is biased at zero gate and drain bias which is known as zero-cold FET condition (Lovelace et al, 1994; Raghavan et al, 2008). C_{gdo} and C_{gso} are extrinsic gate-to-drain and gate-to-source capacitances, respectively. R_{SO} and R_{DO} are the source and drain extrinsic resistances respectively. L_{SO}, L_{DO} and L_{GO} are source, drain and gate extrinsic inductances respectively as shown in the equivalent circuit in Fig. 5.01(a). The process of extracting the parameters is described in Fig. 5.01(b). In this subsection, extrinsic parameters of GEWE-SiNW MOSFET is examined as a function of frequency and then compared with conventional devices of identical geometry.

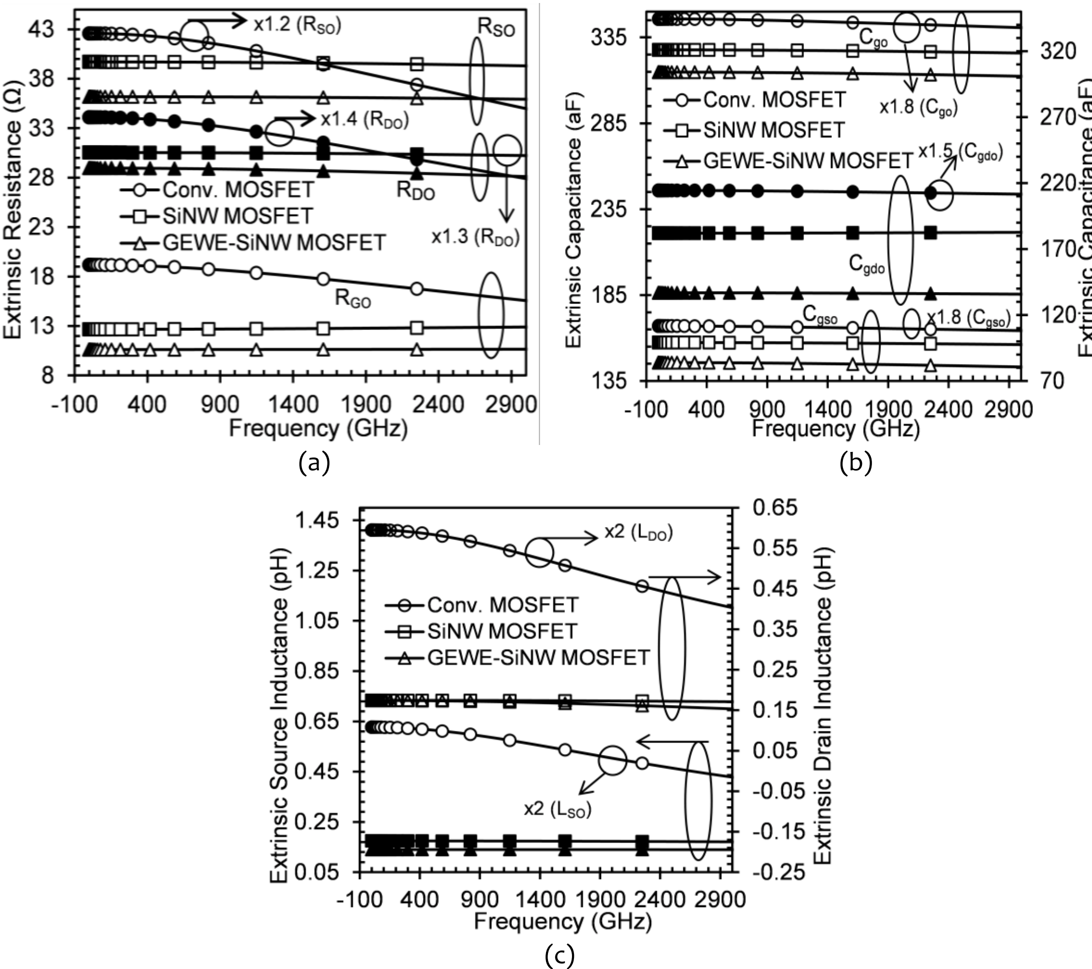


Figure 5.02: (a) Extrinsic Resistance, (b) Capacitance and (c) Inductance as a function of frequency for Conventional, SiNW and GEWE-SiNW MOSFET.

As is evident from Fig. 5.02(a), with an increase in frequency, all the parasitic resistances due to the gate, source and drain are almost constant but in SiNW, their effects are comparatively lower in comparison to conventional MOSFET and with the incorporation of GEWE scheme, resistance effect reduces appreciably. Similarly, both extrinsic capacitances and inductances also reduce in our proposed device compared to SiNW and conventional MOSFET as shown in Fig. 5.02 (b-c).

5.2.2 Intrinsic Parameters

Direct extraction techniques for drawing out the intrinsic small-signal parameters were performed after de-embedding the effect of extrinsic parameters such as C_{gdo}, C_{gso} , R_{SO}, $R_{DO,}$ L_{SO} and L_{DO}. Fig. 5.03 shows the non-quasi-static equivalent circuit of MOSFET to extract intrinsic parameters of GEWE-SiNW, conventional SiNW and conventional MOSFET that is based on conventional MOSFET's small signal microwave modeling (Tsividis & McAndrew, 2011).

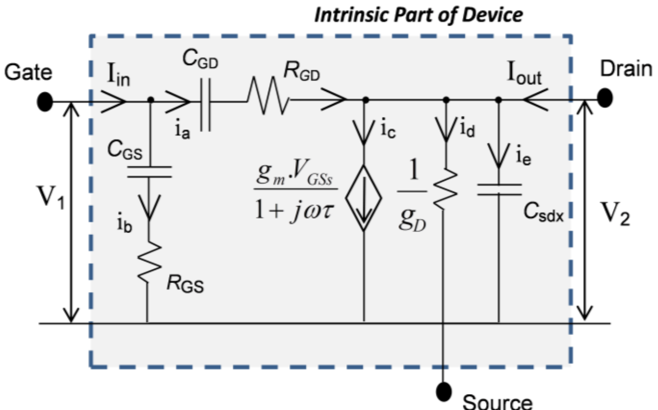


Figure 5.03: Non-quasi-static (NQS) equivalent circuit model of SiNW MOSFET at RF region operating in the strong inversion region

Here, R_{GS} and R_{GD} are distributed channel resistance and C_{DS} and C_{GS} are intrinsic gate-to-drain and gate-to-source capacitances respectively. g_D and g_m are intrinsic

drain and gate transconductance respectively. Fig. 5.04(a) illustrates the bias dependence small-signal parameters in terms of the gate and drain transconductance of GEWE-SiNW and conventional SiNW MOSFET at gate and drain bias respectively.

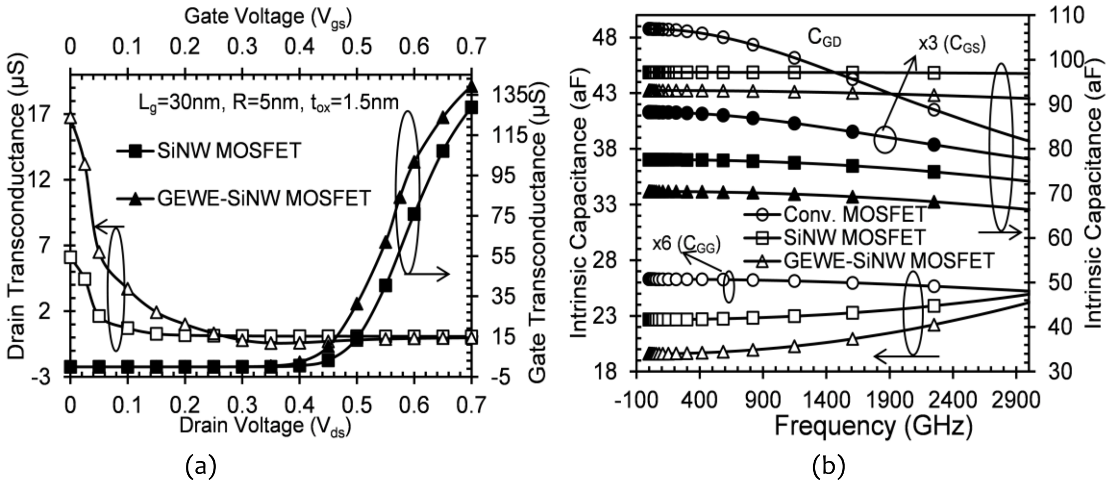


Figure 5.04: (a) Intrinsic gate and drain transconductance of Conventional, SiNW and GEWE-SiNW MOSFET as a function of bias voltage, (b) Intrinsic Capacitance as a function of the frequency of Conventional, SiNW and GEWE-SiNW MOSFET.

As is evident from Fig. 5.04(a), there is a significant increment in g_m with an increase in V_{gs} in comparison to SiNW MOSFET. This is due to the enhanced current driving capability of GEWE-SiNW MOSFET in contrast to conventional SiNW MOSFET, thereby improving gain of the device. Further, g_D decreases with increase in V_{ds} but its value is comparatively higher in the case of GEWE-SiNW MOSFET, since g_D is inversely related to output resistance. As is evident that when device is in the active region (V_{ds}=0 to 0.4V), g_D decreases rapidly which indicates output resistance decreases and enhancement in on-current is achieved; and in the saturation region (V_{ds}=0.4 to 1.0V), g_D becomes almost constant which results in saturation of drain current as shown in Fig. 5.04(a). Parasitic capacitances such as C_{GS}, C_{GD} and C_{GG} in

RF amplifiers degrade the performance in terms of low gain and in some cases; it may cause these amplifiers to oscillate. In digital logic circuits, the rise and fall time of the digital signal greatly influence the maximum achievable device speed (Malik et al, 2012). Thus, it is necessary to examine the effect of parasitic capacitances at HF. Capacitances of SiNW MOSFET turned out to be smaller than that of Conventional MOSFET, as shown in Fig. 5.04(b). With the incorporation of GEWE scheme onto SiNW MOSFET, the parasitic capacitances decrease further with an increase in frequency. This is due to improved screening of channel region from drain bias variations. Hence, lower values of intrinsic parasitic capacitances mean a lower intrinsic delay that is suitable for switching applications such as in logic gates.

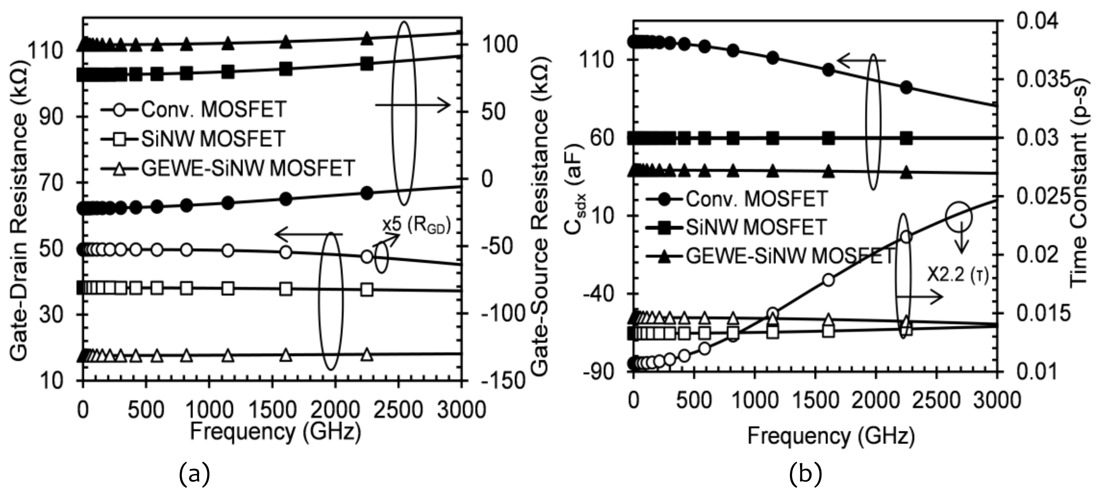


Figure 5.05: (a) Intrinsic gate to drain and gate to source resistance of Conventional, SiNW and GEWE-SiNW MOSFET as a function of frequency, (b) C_{sdx} and Time Constant of Conventional, SiNW and GEWE-SiNW MOSFET respectively as a function of frequency.

At low frequency, the gate of MOSFET is treated as purely capacitive. This assumption fails as frequency goes beyond the GHz range (Razavi et al, 1994). Also, distributed gate resistance plays a major role in evaluating the noise figure and power gains of the transistor. Fig. 5.05(a) exhibits the distributed channel resistances i.e. R_{GD}

and R_{GS} of GEWE-SiNW, SiNW and Conventional MOSFETs as a function of frequency. R_{GD} for GEWE-SiNW MOSFET is much smaller than its conventional counterparts and hence results in maximum power gain and maximum oscillation frequency. Also, in highly scaled MOSFETs, the unexpected change of inversion channel charge in MOSFETs is due to the DIBL effect. Since the source and drain capacitance of the transistor is determined by inversion channel charge, the value of C_{SD} is affected by DIBL (Je & Shin, 2003). To study the exact effect of DIBL on C_{SD}, C_{sdx} is the additional component reflecting the charge variation due to DIBL in short channels MOSFETs (Cho et al, 2010). Fig. 5.05(b) shows the variation of C_{sdx} as a function of frequency. The effect of DIBL is highly pronounced in conventional MOSFET at HF in comparison to SiNW MOSFET. With the incorporation of GEWE, SCEs such as hot-carrier, DIBL reduces as reported in (Gupta & Chaujar, 2014). It is clearly shown that DIBL effect is reduced in GEWE-SiNW MOSFET due to a reduction in C_{sdx} owing to a decline in the electric field at drain end because of lower metal workfunction. Secondary axis of Fig. 5.05(b) shows the time constant of Conventional, SiNW and GEWE-SiNW MOSFET as a function of frequency. The time constants for charging delay are exhibited by $R_{GS}C_{GS}$ and $R_{GD}C_{GD}$, and the charging delay is affected by the transport delay τ (Tsividis & McAndrew, 2011). As is evident from Fig. 5.05(b) that τ of SiNW MOSFET is greater than conventional MOSFET due to higher inversion channel charges owing to cylindrical geometry. With the incorporation of two dissimilar metal gates, time constant increases. Therefore, the distributed channel resistance, R_{GS} of a GEWE-SiNW MOSFET is higher than that of the conventional one.

A. Effect of Gate Metal Workfunction Engineering

In this subsection, the effect of metal gate engineering is observed on the intrinsic parameters of GEWE-SiNW MOSFET by keeping the workfunction at the source side constant (4.8eV) and varying the workfunction of metal gate at the drain end. Fig. 5.06 shows the variation of bias dependent gate and drain transconductance for different gate workfunction at the drain end.

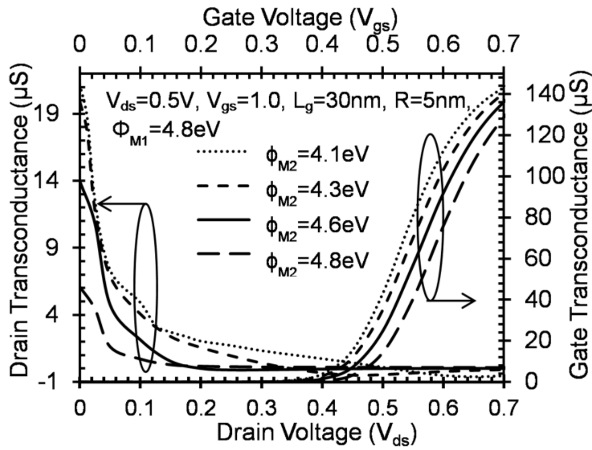


Figure 5.06: Intrinsic gate and drain transconductance of GEWE-SiNW MOSFET for different metal workfunctions.

With the increase in workfunction difference, gate transconductance (g_m) increases due to improved carrier transport efficiency and enhanced current driving capability; thereby delivering higher gain. Drain transconductance (g_d) decreases with increase in drain bias and it is more pronounced as workfunction difference increases as shown in Fig. 5.06. Moreover, as the workfunction difference increases, there is a prominent reduction in C_{GS} and C_{GD} with an increase in frequency as observed in Fig. 5.07 (a-b) due to enhanced screening of potential from bias variations, thus, reducing the turn-on delay time. Similarly, with an increase in workfunction difference, distributed R_{GD}

decreases, and R_{GS} increases and these gate resistances are independent of frequency as shown in Fig. 5.08(a).

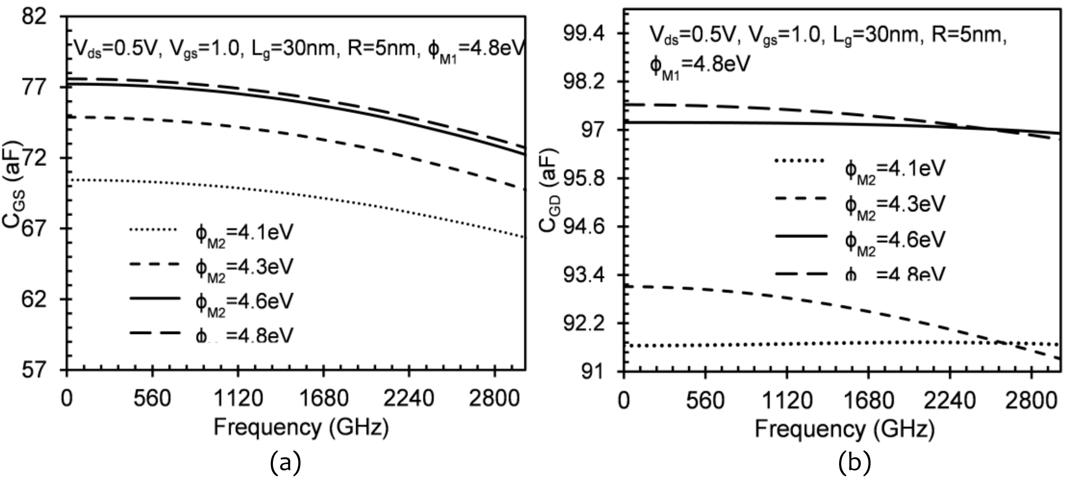


Figure 5.07: (a-b) Intrinsic Capacitance of GEWE-SiNW MOSFET as a function frequency for different gate metal workfunction.

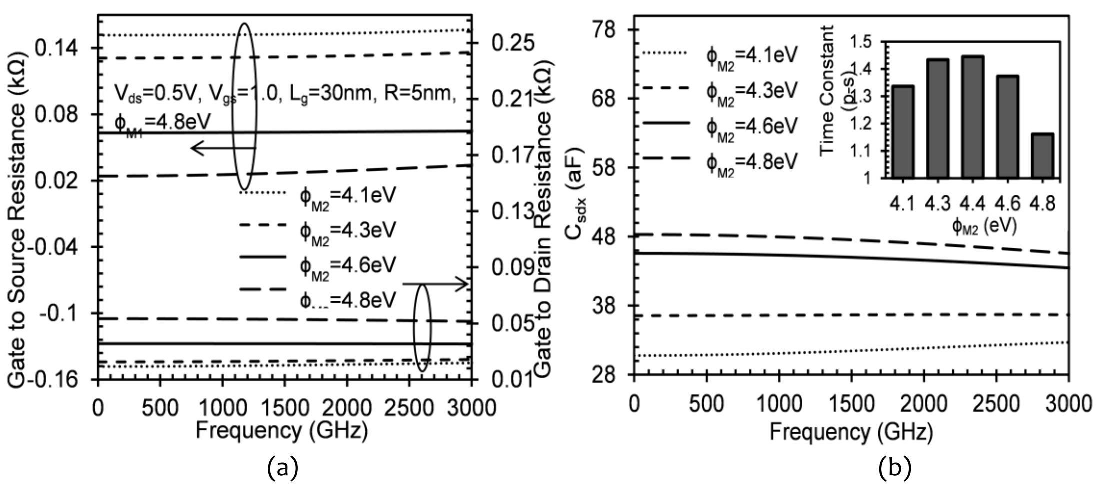


Figure 5.08: (a) Intrinsic gate to drain and gate to source resistance of GEWE-SiNW MOSFET for different metal workfunction, (b) C_{sdx} and Time-Constant of GEWE-SiNW MOSFET for different metal workfunction.

As is evident from Fig. 5.08(b) that by decreasing the workfunction of a metal gate at drain end, the effect of C_{sdx} reduces in GHz frequency regime which directly indicates that higher workfunction difference leads to immunity against DIBL and hence, the SCEs. Further, time constant also enhances to 32% with an increase in workfunction

difference as is shown in 5.08(b) due to enhancement in the on-current and carrier mobility.

B. Bias dependent Intrinsic Parameters

In the previous section, intrinsic parameters of GEWE-SiNW MOSFET is evaluated as a function of frequency and results show that these parameters are almost constant with change in frequency in GHz range. In this section, the effect of bias variation is observed on the intrinsic parasitic capacitance, transconductance, distributed gate capacitance and time constant. The MOSFET gate transconductance ($g_m = \partial I_{DS}/\partial V_{GS}$) is defined in the linear regime and is used as an indirect monitor of inversion charge carrier mobility. Transconductance is an important parameter needed for designing high-frequency amplifiers. As is evident from Fig. 5.09(a), g_m increases remarkably as drain voltage increases from 0.1V to 0.5V. Fig. 5.09(a) also indicates the drain transconductance dependence on drain voltage for different gate voltages. As drain voltage increases, drain transconductance increases and then reduces to zero due to flow of high drain current which saturates at higher V_{ds}. The rate of decrease of drain transconductance with drain voltage is more than with an increase in gate voltage. The effect of drain bias on parasitic capacitance is observed in Fig. 5.09(b). As is evident from the figure 5.09 (b) that with increase in drain bias, all the parasitic capacitances increase due to shifting of pinch-off point towards source side which leads to accumulation of charge carriers resulting in an increment in C_{GS}. To maintain charge neutrality, charges near the drain decreases and hence C_{GD} decreases as shown in Fig. 5.09(b).

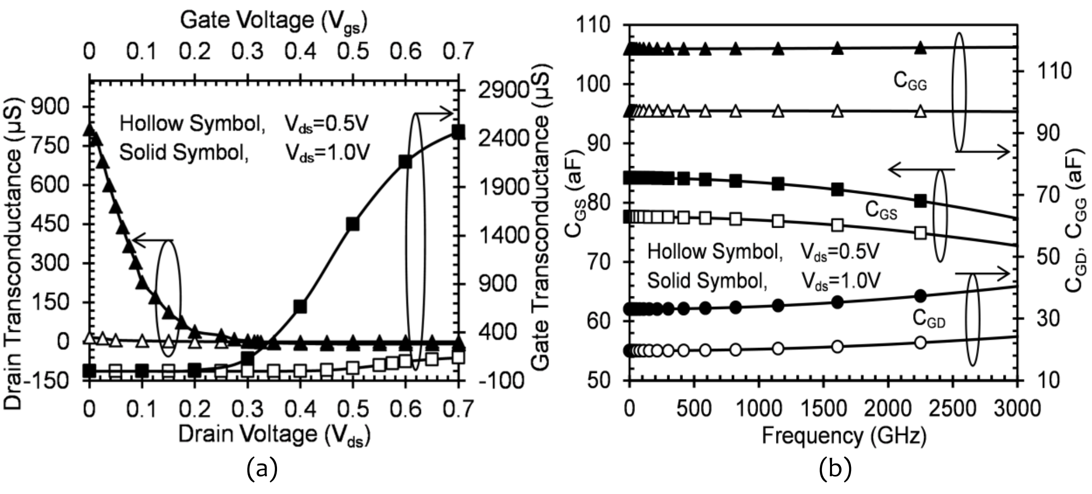


Figure 5.09: (a) Intrinsic gate and drain transconductance of GEWE-SiNW MOSFET for different bias value, (b) Intrinsic Bias dependent parasitic capacitance of GEWE-SiNW MOSFET

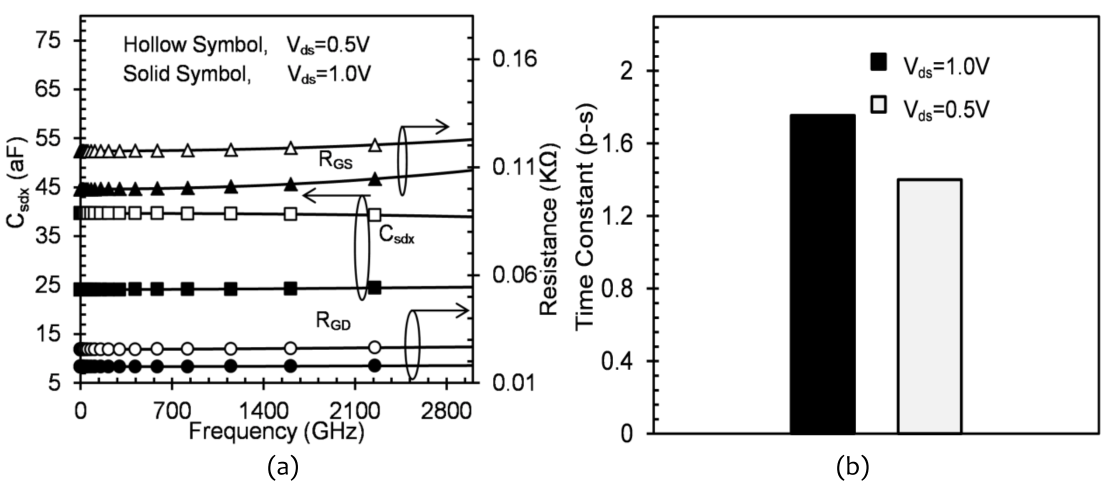


Figure 5.10: (a-b) C_{sdx} and Distributed gate resistance; and time constant of GEWE-SiNW MOSFET respectively for different drain bias values.

Fig. 5.10(a) indicates the variation of C_{sdx} as a function of frequency for different drain bias. It is evident that with an increase in drain bias, the effect of DIBL is reduced as is reflected through C_{sdx}. This reduction is due to improved gate controllability of GEWE-SiNW MOSFET over the channel due to the cylindrical gate and step in conduction band energy profile in the channel region, which is further because of metal gate workfunction difference. Also, both the distributed gate

resistance (R_{GS} and R_{GD}) decreases as the device moves from linear to saturation region as is evident from Fig. 5.10(a). Moreover, the time constant of GEWE-SiNW MOSFET degrades with an increase in drain bias due to enhancement in inversion charge carriers as is shown in Fig. 5.10(b).

5.2.3. Small Signal Model Parameters: Z and Y

The small-signal behavior of MOSFET is generally expressed in terms of impedance (Z-parameters) and admittance (Y-parameters) and is commonly employed for those networks that are operating at RF/microwave frequencies. With knowledge of the parasitic parameters, the intrinsic Z-parameters can be determined in a similar way as intrinsic parameters are extracted. The choice of parameter is generally determined by suitability or usage, e.g. if shunt feedback is applied in RF amplifiers, Y parameters are of utmost convenient, whereas series feedback recommends Z parameters. After de-embedding the extrinsic parameters, the intrinsic Z and Y parameters are evaluated by solving the small signal equivalent model as shown in Fig.5.03.

Total current flowing at the input port (gate) $= i_a + i_b$

Total current flowing at the output port (drain) $= i_c + i_d + i_e - i_b$

By applying nodal analysis,

$$\frac{V_1}{X_1} + \frac{V_1 - V_2}{X_2} = 0 \qquad \text{[At input node]} \qquad \ldots\ldots (5.1)$$

$$\frac{V_2}{X_3} + \frac{V_2 - V_1}{X_2} + \frac{g_m V_{gs}}{1 + j\omega\tau} = 0 \qquad \text{[At output node]} \qquad \ldots\ldots (5.2)$$

where $X_1 = \frac{1 + j\omega R_{GS} C_{GS}}{j\omega C_{GS}}$; $X_2 = \frac{1 + j\omega R_{DS} C_{DS}}{j\omega C_{DS}}$; $X_3 = \frac{1}{g_D + j\omega C_{sdx}}$

By solving equation (5.1) and (5.2), and using approximations $\omega^2 R_{GS}^2 C_{GS}^2 << 1,\ \omega^2 R_{GD}^2 C_{GD}^2 << 1$ and $\omega^2 \tau^2 << 1$, we get,

1. ***Driving Point Short Circuit Input Admittance***

$$Y11 \cong \omega^2 (a_1 + a_2) + j\omega(C_{GS} + C_{GD}) \qquad \ldots\ldots (5.3)$$

2. ***Driving point short circuit output admittance***

$$Y22 \cong g_D + \omega^2 a_2 + j\omega(C_{GD} + C_{sdx}) \qquad \ldots\ldots (5.4)$$

3. ***Reverse Transfer Admittance***

$$Y12 \cong -\omega^2 a_2 - j\omega C_{GD} \qquad \ldots\ldots (5.5)$$

4. ***Forward Transfer Admittance***

$$Y21 \cong -\omega^2 a_2 - j\omega C_{GD} + g_m(1+\tau) \qquad \ldots\ldots (5.6)$$

Similarly, Z-parameters are evaluated using Y-parameters and we get,

1. ***Driving point input impedance***

$$Z11 \cong \frac{g_D + \omega^2 a_2 + j\omega(C_{GD} + C_{sdx})}{\xi} \qquad \ldots\ldots (5.7)$$

2. ***Open-Circuit reverse transfer impedance***

$$Z12 \cong \frac{\omega a_2 + j\omega C_{GD}}{\xi} \qquad \ldots\ldots (5.8)$$

3. ***Open-Circuit forward transfer impedance***

$$Z21 \cong \frac{\omega^2 a_2 + j\omega C_{GD} - g_m(1+\tau)}{\xi} \qquad \ldots\ldots (5.9)$$

4. ***Driving point output impedance***

$$Z22 \cong \frac{\omega^2 (a_1 + a_2) + j\omega(C_{GS} + C_{GD})}{\xi} \qquad \ldots\ldots (5.10)$$

where,
$$\left\{ \begin{aligned} &\xi = [\,j\omega(C_{GS} g_D + C_{GD} g_D + C_{GD} g_m + \tau C_{GD} g_m) + \\ &\quad \omega^2 (a_1 g_D + a_2 g_D - C_{GS} C_{sdx} - C_{GD} C_{sdx} + a_2 g_m (1+\tau) + C_{GD}^2) + \\ &\quad j\omega^3 (a_1 C_{GD} + a_2 C_{GS} + C_{sdx}(a_1 + a_2)) + a_1 a_2 \omega^4] \\ &\quad a_1 = R_{GS} C_{GS}^2, a_2 = R_{GD} C_{GD}^2 \end{aligned} \right\}$$

Z11 and Z22 are essentially used for impedance matching at high-frequency applications. For impedance matching, input impedance should be equal to output impedance, and it is necessary for maximum power transfer from source to the load. Fig. 5.11(a-b) shows the variation of real component of input and output impedance of conventional, SiNW and GEWE-SiNW MOSFET as a function of frequency. It is clearly shown that input impedance of GEWE-SiNW is comparatively higher than its conventional counterparts owing to cylindrical geometry and GEWE scheme. Further, with the tuning of metal workfunction at the drain end, both input and output impedance improves as frequency increases in GHz range shown in Fig. 5.12(a-b).

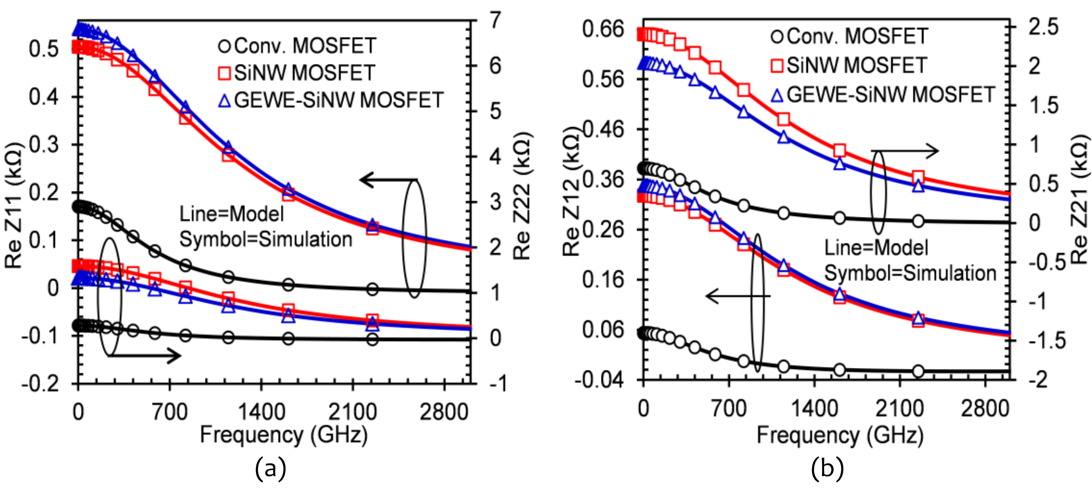


Figure 5.11: (a-b) Z-parameters of Conventional, SiNW and GEWE-SiNW MOSFET as a function of frequency at V_{ds}=1.0V and V_{gs}=0.5V

For RF amplifiers, ideally Z12 should be as high as possible so that maximum transfer of impedance takes place from input to output. It is clear from results that Z12 for SiNW MOSFET is comparatively greater than conventional MOSFET due to reduced SCEs and maximum volume inversion and with the incorporation of GEWE engineering onto SiNW; Z12 improves as shown in Fig. 5.11(b). Further, with

increasing the gate workfunction difference in GEWE-SiNW, Z12 enhances due to enhancement in carrier mobility and hence transport efficiency as is evident from Fig. 5.12(b). At low frequencies, AC voltages and currents can be easily measured, but at HF, the measurement of these parameters becomes exceptionally complicated. Then, another set of parameters is S-parameters which can be measured at such high frequencies.

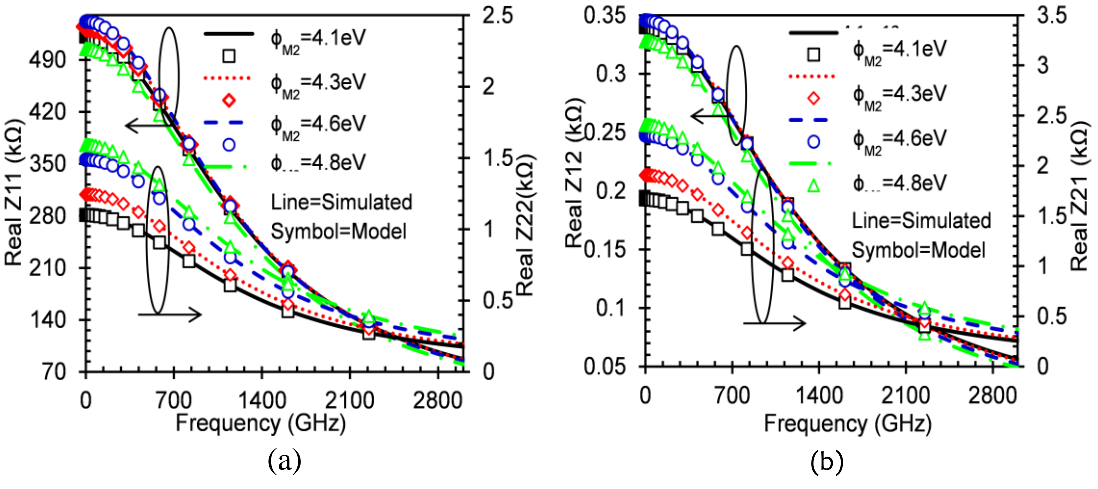


Figure 5.12: (a-b) Z-parameters of GEWE-SiNW MOSFET for different gate metal workfunction as a function of frequency at V_{ds}=1.0V and V_{gs}=0.5V

However, as Y-parameters are more closely related to device physics and design, so S-parameters are again being converted into Y parameters and hence, the study of Y-parameters becomes necessary. Fig. 5.13(a) shows that the real component of input admittance of GEWE- SiNW MOSFET is comparatively lower than its conventional counterparts and its value gradually increases with increase in frequency. Similarly, Y22 increases in GEWE-SiNW compared to SiNW and conventional MOSFET, which means current driving capability of GEWE-SiNW MOSFET enhances due to metal workfunction engineering which further enhances carrier velocity and hence on-current as shown in Fig. 5.13(a). Y12 and Y21 of GEWE-SiNW MOSFET are lower

and higher respectively as shown in Fig. 5.13(b). Y21 is defined as forward transconductance of a device, and ideally its value should be as high as possible for achieving high gain RF amplifier.

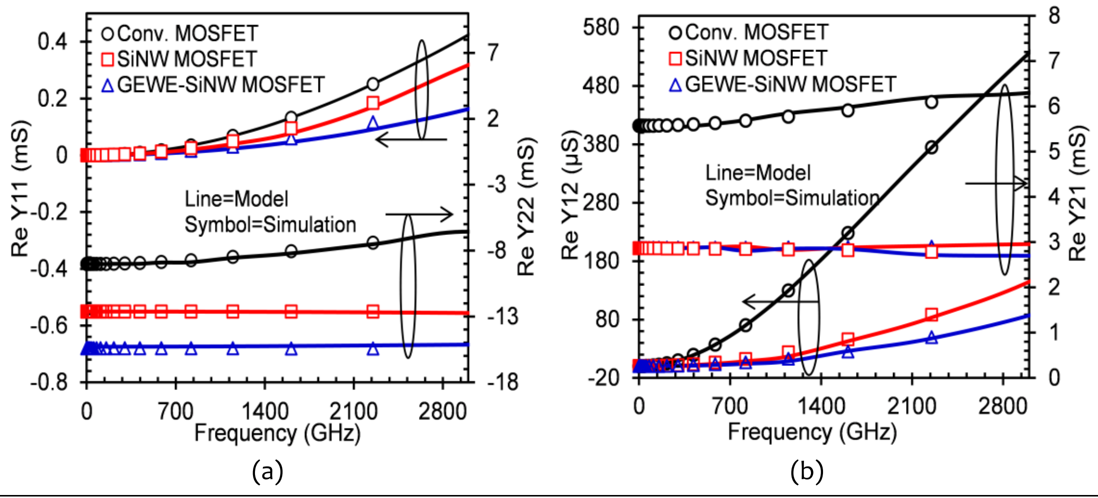


Figure 5.13: (a-b) Y-parameters of Conventional, SiNW and GEWE-SiNW MOSFET as a function of frequency at V_{ds}=1.0V and V_{gs}=0.5V.

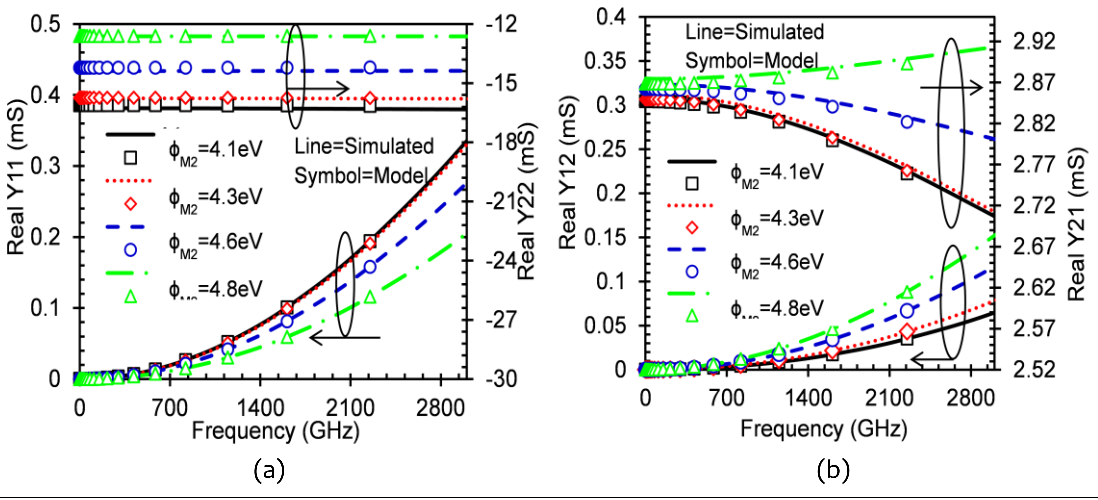


Figure 5.14: (a-b) Y-parameters of GEWE-SiNW MOSFET for different gate metal workfunction as a function of frequency at V_{ds}=1.0V and V_{gs}=0.5V.

Also, with workfunction difference of 0.7eV, the device small signal performance in terms of the real component of Y11, Y12, Y21 and Y22 improves as shown in Fig. 5.14(a-b) owing to better enhancement in transconductance. The modeled Z and Y –

parameters (line) generated from the NQS model and the extracted parameters from 3D-simulation (symbol) demonstrate excellent agreements. Thus, the proposed model is highly reliable for RF/millimeter-wave applications and hence suitable for providing information to RF engineers. All the parameters extracted in the linear (V_{ds} = 0.5 V) and saturation (V_{ds} = 1.0 V) regions have been summarized in Table 5.01. Also, the effect of metal workfunction engineering on all the parameters is summarized in Table 5.02.

Table 5.01: Extracted Parameters of all three devices for linear and saturation region

Device / Parameter	Conventional MOSFET		SiNW MOSFET		GEWE-SiNW MOSFET	
	V_{ds}=0.5	V_{ds}=1.0	V_{ds}=0.5	V_{ds}=1.0	V_{ds}=0.5	V_{ds}=1.0
C_{GS} (aF)	251.5	287.87	76.2	81.32	69.25	82.189
C_{GD} (aF)	310.4	340.87	97.2	103.34	92.54	117.44
R_{GS} (kΩ)	14.88	12.34	81.8	79.34	118.9	102.19
R_{GD} (kΩ)	244.65	220.98	37.8	31.98	26.1	17.82
g_m (µS)	50	65.96	128	200.98	139.3	2470
g_D (µS)	0.1	1.02	0.711	7.47	3.70	228.3
τ (p-s)	0.431	0.65	1.161	1.4	1.39	1.89
C_{sdx} (aF)	309	289.34	59.829	52.56	38.57	24.31
R_{SO} (Ω)	46.8	46.8	39.585	39.585	36.11	36.11
R_{DO} (Ω)	44.14	44.14	39.585	39.585	28.68	28.68
L_{SO} (pH)	1.07	1.07	0.1725	0.1725	0.1399	0.1399
L_{DO} (pH)	1.014	1.014	0.1735	0.1735	0.167	0.167
C_{GSO} (aF)	298	298	157	157	144	144
C_{GDO} (aF)	319	319	182	182	136	136

Table 5.02: Extracted Parameters of GEWE-SiNW MOSFET for different metal workfunction (Φ_{M2})

Workfunction (Φ_{M2}) / Parameter	GEWE-SiNW MOSFET (Φ_{M1}= 4.8 eV, V_{ds}=0.5, V_{gs}=1.0)			
	4.1eV	4.3eV	4.6eV	4.8eV
C_{GS} (aF)	69.25	73.4	75.80	76.2
C_{GD} (aF)	91.7	92.81	97.14	97.6
R_{GS} (kΩ)	152	132.2	63.87	27.38
R_{GD} (kΩ)	20.5	23.16	35.53	52.78
g_m (μS)	143.7	140	136	128
g_D (μS)	4.92	4.07	2.146	0.711
τ (p-s)	1.54	1.478	1.378	1.161
C_{sdx} (aF)	31.53	36.72	44.93	46.67

5.3 SUMMARY

Both the extrinsic and intrinsic parameters of GEWE-SiNW MOSFET are directly extracted based on quantum simulations and simultaneously compared with SiNW and conventional MOSFET at a GHz range with an aim to analyse the effect of these parameters for RF applications. Simulation result demonstrates a noticeable reduction in extrinsic parameters such as resistances, inductances and capacitances in GEWE-SiNW MOSFET compared to its conventional counterparts. Also, reduction in intrinsic C_{sdx} implies that DIBL is less pronounced in the proposed device at HF. Moreover, with the tuning of workfunction difference effect of parasitics can be lowered which hinders the performance of a device at RF. Admittance and impedance parameters also improve with the incorporation of GEWE scheme due to reduced SCEs and maximum volume inversion owing to the cylindrical gate, thus providing

the necessary information to RF engineers for microwave communications. The modeling results matched well with the Z and Y-parameters extracted from the 3D-device simulation.

However, at HF gate leakage due to thinning of oxide thickness hinders the device RF performance owing to high off-current. Therefore, stacked gate is amalgamated onto GEWE-SiNW MOSFET to overcome this problem. Thus, the next chapter discusses the comprehensive device performance of SG-GEWE-SiNW MOSFET and also the reliability issues of SG-GEWE-SiNW MOSFET at different ambient temperatures are also examined.

5.4 REFERENCES

Alam, M. & Armstrong, G. (2010) Extraction of extrinsic series resistance in RF CMOS.

Buss, D. (1999) Device issues in the integration of analog/RF functions in deep submicron digital CMOS, *Electron Devices Meeting, 1999. IEDM'99. Technical Digest. International*. IEEE.

Chen, X. & Tan, C. M. (2014) Modeling and analysis of gate-all-around silicon nanowire FET. *Microelectronics Reliability*, 54(6), 1103-1108.

Cheng, Y., Deen, M. J. & Chen, C.-H. (2005) MOSFET modeling for RF IC design. *IEEE Transactions on Electron Devices*, 52(7), 1286-1303.

Cho, S., Kang, I. M. & Kim, K. R. (2010) Investigation of source-to-drain capacitance by DIBL effect of silicon nanowire MOSFETs. *IEICE Electronics Express*, 7(19), 1499-1503.

Cho, S., Kim, K. R., Park, B.-G. & Kang, I. M. (2011) RF performance and small-signal parameter extraction of junctionless silicon nanowire MOSFETs. *IEEE Transactions on Electron Devices*, 58(5), 1388-1396.

Cui, Y., Zhong, Z., Wang, D., Wang, W. U. & Lieber, C. M. (2003) High performance silicon nanowire field effect transistors. *Nano letters*, 3(2), 149-152.

Deen, M. J. & Fjeldly, T. A. (2002) *CMOS RF Modeling, Characterization and Applications*, *24*World Scientific.

Gupta, N. & Chaujar, R. (2014) Implications of transport models on the analog performance of Gate Electrode Workfunction Engineered (GEWE) Silicon Nanowire MOSFET, *Devices, Circuits and Systems (ICDCS), 2014 2nd International Conference on*. IEEE.

Gupta, N., Kumar, A. & Chaujar, R. (2015) Impact of device parameter variation on RF performance of gate electrode workfunction engineered (GEWE)-silicon nanowire (SiNW) MOSFET. *Journal of Computational Electronics*, 14, 798-810.

Gupta, N., Kumar, A. & Chaujar, R. (2016) Oxide bound impact on hot-carrier degradation for gate electrode workfunction engineered (GEWE) silicon nanowire MOSFET. *Microsystem Technologies*, 22(11), 2655-2664.

Iwai, H. (2009) Roadmap for 22nm and beyond. *Microelectronic Engineering*, 86(7), 1520-1528.

Iwai, H., Natori, K., Shiraishi, K., Iwata, J.-i., Oshiyama, A., Yamada, K., Ohmori, K., Kakushima, K. & Ahmet, P. (2011) Si nanowire FET and its modeling. *Science China information sciences*, 54(5), 1004-1011.

Je, M. & Shin, H. (2003) Accurate four-terminal RF MOSFET model accounting for the short-channel effect in the source-to-drain capacitance, *2003 International Conference on Simulation of Semiconductor Processes and Devices*.

Kumar, A., Gupta, N. & Chaujar, R. (2016a) Power gain assessment of ITO based transparent gate recessed channel (TGRC) MOSFET for RF/wireless applications. *Superlattices and Microstructures*, 91, 290-301.

Kumar, A., Gupta, N. & Chaujar, R. (2016b) TCAD RF performance investigation of transparent gate recessed channel MOSFET. *Microelectronics Journal*, 49, 36-42.

Lai, Y.-L. & Hsu, K.-H. (2001) A new pinched-off cold-FET method to determine parasitic capacitances of FET equivalent circuits. *IEEE Transactions on Microwave Theory and Techniques*, 49(8), 1410-1418.

Lovelace, D., Costa, J. & Camilleri, N. (1994) Extracting small-signal model parameters of silicon MOSFET transistors, *Microwave Symposium Digest, 1994., IEEE MTT-S International*. IEEE.

Malik, P., Gupta, R., Chaujar, R. & Gupta, M. (2012) AC analysis of nanoscale GME-TRC MOSFET for microwave and RF applications. *Microelectronics Reliability*, 52(1), 151-158.

Park, D., King, Y.-c., Lu, Q., King, T.-J., Hu, C., Kalnitsky, A., Tay, S.-P. & Cheng, C.-C. (1998) Transistor characteristics with Ta/sub 2/O/sub 5/gate dielectric. *IEEE Electron Device Letters*, 19(11), 441-443.

Raghavan, A., Srirattana, N. & Laskar, J. (2008) *Modeling and design techniques for RF power amplifiers*John Wiley & Sons.

Razavi, B., Yan, R.-H. & Lee, K. F. (1994) Impact of distributed gate resistance on the performance of MOS devices. *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, 41(11), 750-754.

Subramanian, V., Mercha, A., Parvais, B., Dehan, M., Groeseneken, G., Sansen, W. & Decoutere, S. (2010) Identifying the bottlenecks to the RF performance of FinFETs, *2010 23rd International Conference on VLSI Design*. IEEE.

Tsividis, Y. & McAndrew, C. (2011) *Operation and Modeling of the MOS Transistor*Oxford Univ. Press.

Wang, R., Zhuge, J., Huang, R., Tian, Y., Xiao, H., Zhang, L., Li, C., Zhang, X. & Wang, Y. (2007) Analog/RF performance of Si nanowire MOSFETs and the impact of process variation. *IEEE transactions on Electron Devices*, 54(6), 1288-1294.

Woerlee, P. H., Knitel, M. J., Van Langevelde, R., Klaassen, D. B., Tiemeijer, L. F., Scholten, A. J. & Zegers-van Duijnhoven, A. T. (2001) RF-CMOS performance trends. *IEEE Transactions on Electron Devices*, 48(8), 1776-1782.

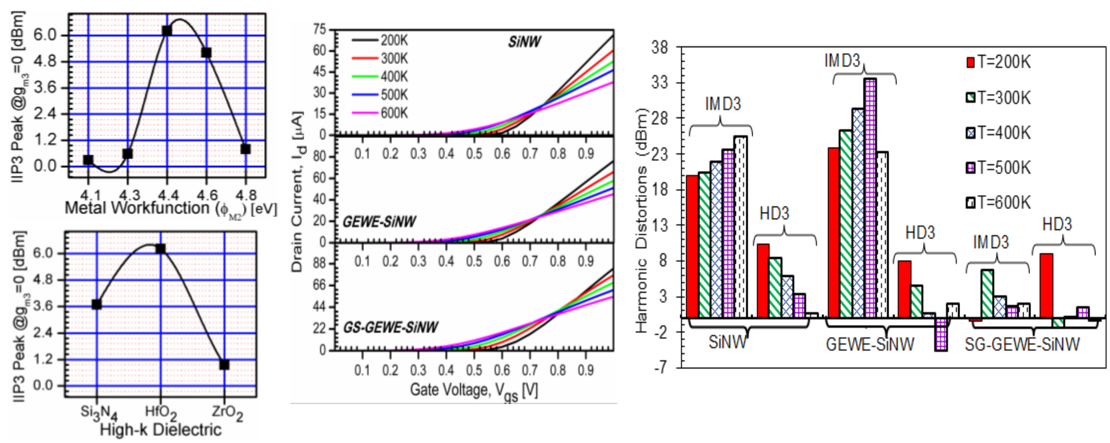
Wood, J., Lamey, D., Guyonnet, M., Chan, D., Bridges, D., Monsauret, N. & Aaen, P. (2008) An extrinsic component parameter extraction method for high power RF LDMOS transistors, *Microwave Symposium Digest, 2008 IEEE MTT-S International*. IEEE.

Ytterdal, T., Cheng, Y. & Fjeldly, T. A. (2003) *Device Modeling for Analog and RF CMOS Circuit Design*Wiley Online Library.

CHAPTER-6

Influence of Stacked Gate on Comprehensive Device Performance of GEWE-SiNW MOSFET

- ***Optimizes the gate engineering scheme of Stacked Gate GEWE-SiNW MOSFET.***
- ***Results exhibit that HfO_2 as a gate stack exhibit high linearity at a comparatively low gate bias of 0.56V with higher IIP3 (6.21dBm) and low IMD3 (9.6 dBm).***
- ***Characteristics/performance is further modulated by adjusting the workfunction difference of metal gate.***
- ***SiNW MOSFET with HfO_2 as a gate stack and ΔW of 4.4 eV, considered as promising one for low power ICs and Linear amplifiers.***
- ***Reliability issues of Stacked Gate-GEWE-SiNW MOSFET are investigated by modulating ambient temperature.***
- ***SG-GEWE-SiNW is more reliable at low temperatures owing to reduced off-current and parasitic gate capacitance.***
- ***ZTC/TCP observed at lower gate bias for SG-GEWE-SiNW, results into improvement in static and dynamic performance.***
- ***Linearity FOMs slightly degrades at 200K in SG-GEWE-SiNW and will not hinder much to the device performance.***



6.1 INTRODUCTION

The foremost limitation in scaling of CMOS devices is the gate dielectric thickness. The silicon dioxide (SiO_2) as conventional gate dielectric in MOSFET has reached its critical value i.e., the level where the physical thickness is 1nm thick (few atomic layers). As oxide thickness scales down to this dimension, the gate leakage current increases up to $1A/cm^2$ at 1V due to direct tunneling of carriers which, consequently increases the static power and hence, affects the circuit operation as reported by (Lo et al, 1997; Ribes et al, 2005). To overcome this problem, high-k dielectric have been incorporated directly onto silicon wafer but these films result in high fringing fields from gate to source/drain regions and thus degrading the device performance as previously discused in Chapter-1. This constraint can be overcome by using gate stack architecture consisting of SiO_2 layer as a passivation layer between high-k dielectric and silicon wafer by keeping the effective oxide thickness (EOT) constant, high-k dielectrics permit the increase in physical oxide thickness to prevent gate tunneling (Chau et al, 2004; Lee et al, 2006) and thus improves the carrier efficiency but at the same time, the gate capacitance also increases. Fig. 6.01 briefly shows the dielectric constants of high-k materials (Brezeanu et al, 2010; Ribes et al, 2005; Shannon, 1993; Wilk et al, 2000), and was reported that TiO_2 and barium strontium titanate (BST) showing exceptionally higher permittivity are not thermally stable with silicon substrates (Register & Ekerdt, 2004). BST with high-k dielectric causes Field Induced Barrier Lowering (FIBL) which degrades the device performance and thus is not suitable for gate dielectric. Moreover, it is also reported that Al_2O_3 has high surface density of states (i.e., interface trap charges).

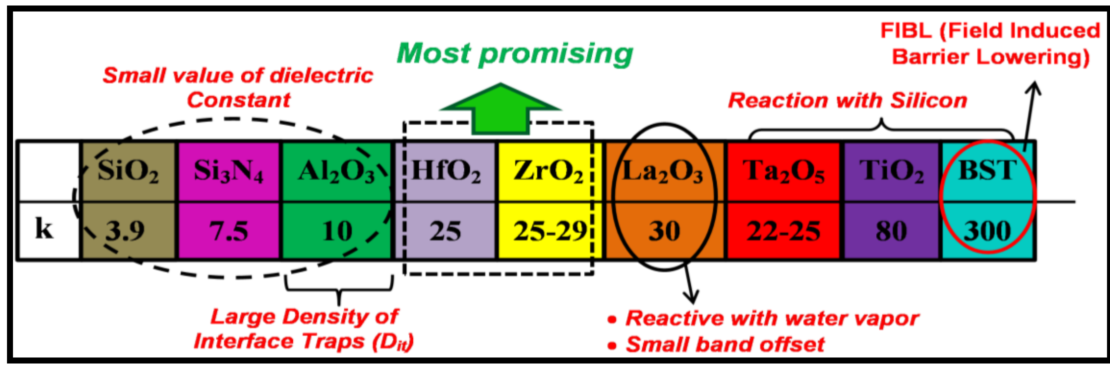


Figure 6.01: Dielectric constant of some high-k dielectrics (He et al, 2012)

The requirements for high-k dielectric applications are (Zeng et al, 2014)

- high dielectric constant and large band gap
- high band offset with electrodes
- thermally and chemically stable in contact with semiconductor substrate
- scalable equivalent oxide thickness EOT < 10Å
- compatibility with gate electrode material
- density of interface states comparable to SiO_2
- low lattice mismatch and similar thermal expansion coefficient with Si mobility comparable to SiO_2
- negligible capacitance-voltage hysteresis (< 20mV)
- good reliability (no charge trapping, high breakdown voltage etc.)

Thus, for selection of high-k materials relationship between dielectric constant and band-offset must be considered. The excessive high-k constant is generally undesirable owing to a tradeoff between dielectric constant and band-offset. Based on the requirements as mention above, there are many high-k materials that are being studied nowadays such as Si_3N_4, Al_2O_3, TiO_2, HfO_2, ZrO_2, Ta_2O_5 etc. (He et al, 2012). Among them, bandgap of TiO_2 is 3.5; has a very high dielectric constant of $k \approx 80$, but the band alignment is not favorable (less bandgap) which results in increase of leakage current. Ta_2O_5 has also very low CB offset (0.35) which leads to leakage

current (Wilson, 2013). Also, dielectric material of very high-k value, results in film thickness larger than channel length of the MOSET. On the other hand, Al_2O_3 has high band alignment at 4.3eV, but its dielectric constant is low at k≈9, which counteract the advantage of high bandgap (Wilk et al, 2000). Also, its large threshold voltage and moderately low permittivity make it a relatively short-term solution. And up-to-date, Hf and Zr based high-k dielectric materials are the most commonly studied by academia and industry. The Hf-based high-k dielectrics are thermodynamically stable with silicon and relatively has a very good compatibility with ploysilicon gate dielectric as well as with metal gate dielectric (Houssa, 2003). From past few years, Si_3N_4 is a generally preferred high-k dielectric due to lower tunneling current than oxide of same thickness and also it can easily be integrated with current CMOS technologies. For optimization of device performance for high-k dielectric, Si_3N_4 is preferred for comparison due to its simpler fabrication process as it is easily made from silicon which is abundantly available (Brezeanu et al, 2010; Pradhan et al, 2014; Qi et al, 1999). Therefore, in this section, high-k materials like HfO_2, ZrO_2 and Si_3N_4 has chosen for optimization in Stacked Gate-GEWE SiNW MOSFET. Moreover, surface phonon scattering in high-k dilectric results in mobility degradation and it can be overcome by using substantial metal gates which are active in screening the phonon scattering in high-k dielectric from coupling to the channel under inversion state. Hence, selection of metal material also becomes necessary if high-k dielectric is used as a gate oxide. Thus, optimization of both high-k dilectric and gate metal workfunction of SG-GEWE-SiNW MOSFET has been studied in terms of Analog and Intermodulation metrics of SG-GEWE-SiNW MOSFET, since linearity plays an important role in RFIC designing and high-frequency systems

because nonlinearity causes harmonic generation, gain compression, desensitization etc. (Razavieh et al, 2013; Yu et al, 2004). A high linearity with low distortion is preferred in modern communication systems even while working with a weak signal. Nonlinearity may induce intermodulation (IM), which generate signals with frequencies different from the input ones. These unwanted signals may fall into the band of interest, interfering or even corrupting the desired components (Razavi & Behzad, 1998). Thus, this analysis has been performed with an aim to optimize the value of both high-k dielectric and gate metal workfunction difference (ΔW) of SG-GEWE-SiNW MOSFET which can be used as a reference tool for designing circuits for different analog and RF applications where linearity is a major concern.

Moreover, CMOS devices are extensively used in the field of satellite communications, military, medical equipment, automobile, nuclear sectors, wireless/mobile communications. For these applications, it is important to investigate the device behaviour at a wide range of temperatures (Wong et al, 1999). Also, it has been demonstrated that the performance of MOS devices significantly improves when operating at low temperatures in terms of improved carrier mobilities, on-currents, gain, sub-threshold slope, cut-off frequency, short-channel effects and noise performance (Hong et al, 2008; Sun et al, 1987). The unwanted flow of high leakage current through the junction and the presence of latch-up put a limit on the use of bulk MOS devices at high temperatures. Several technologies have been reported in the literature as an option for both low and high-temperature operations. Some of them are Silicon on Insulator (SOI) (Kim et al, 2012), Recessed Channel (Kumar et al, 2016a), III-V semiconductors (Del Alamo, 2011), Nanowire transistors (Cui et al, 2003), etc.

Among them, SiNW emerged as a most favorable in electronic devices due to the fact that its concentration, dopant type can be changed during synthesis. Also, its mobility is higher than bulk silicon due to stronger 1D quantum confinement. The body thickness of the nanowire can readily be reduced to a few nm in size that is the major challenge to achieve using bulk silicon. Also, since hot carrier degradation is a major concern for short channel MOSFETs (Grasser, 2015), several engineering schemes are reported in literature such as gate metal workfunction engineering (Long & Chin, 1997), drain engineering and channel engineering to overcome this degradation. In this work, for the first time, performance and reliability issues of SG-GEWE-SiNW MOSFET are examined in terms of Analog, RF/Noise and Linearity FOMs at different temperatures (200-600K) with an aim to analyze the temperature at which the device is more reliable for analog and RF applications. The results so obtained are simultaneously compared with GEWE-SiNW and SiNW MOSFET.

6.2 Device Structure

Fig. 6.02(a) shows the simulated 3-D device structure of SG-GEWE-SiNW MOSFET and its 2-D cross-sectional view along with GEWE-SiNW and SiNW MOSFET are shown in Fig. 6.14(b–c). To reduce the mobility deprivation which arises due to coulomb scattering, Source/Drain region is heavily doped with an n-type impurity of 1×10^{19} cm^{-3}, while the SiNW is doped with a p-type impurity of 1×10^{16} cm^{-3}. Effective oxide thickness (EOT) is fixed at 1.5nm for all the cases to maintain a constant capacitance for different high-k dielectrics. SiO_2 layer thickness is fixed at 1.2nm and above this layer; a high-k layer is deposited, so that the EOT reaches 1.5nm. In case of optimization of high-k dielectric, high-k dielectrics such as Si_3N_4,

HfO_2 and ZrO_2 are considered and the corresponding high–k thicknesses are listed in Table. 6.01. The corresponding high-k thickness is calculated using the formula stated as (Salmani-Jelodar et al, 2016):

$$EOT\,(Effective\ Oxide\ Thickness) = T_{ox1} + \frac{\varepsilon_{ox1}}{\varepsilon_{ox2}} T_{ox2} \qquad \ldots.\ (6.1)$$

where t_{ox1} and t_{ox2} is the physical oxide thickness of SiO_2 and high-k dielectric respectievly. ε_{ox1} and ε_{ox2} are dielectric constants of SiO_2 and high-k materials respectively.

In addition, the gate metal work function at the source end (Φ_{m1}) is 4.8 eV (Au) and at the drain end (Φ_{m2}) is 4.4 eV (Ti). The detailed descriptions of all the three device structures are listed in Table 6.02. All the junctions are assumed as abrupt, and the doping profiles are uniform. All simulations have been performed using ATLAS and DEVEDIT 3D device simulator (SILVACO, 2016). Moreover, Table 6.03 lists all the boundary conditions associated with the device structure.

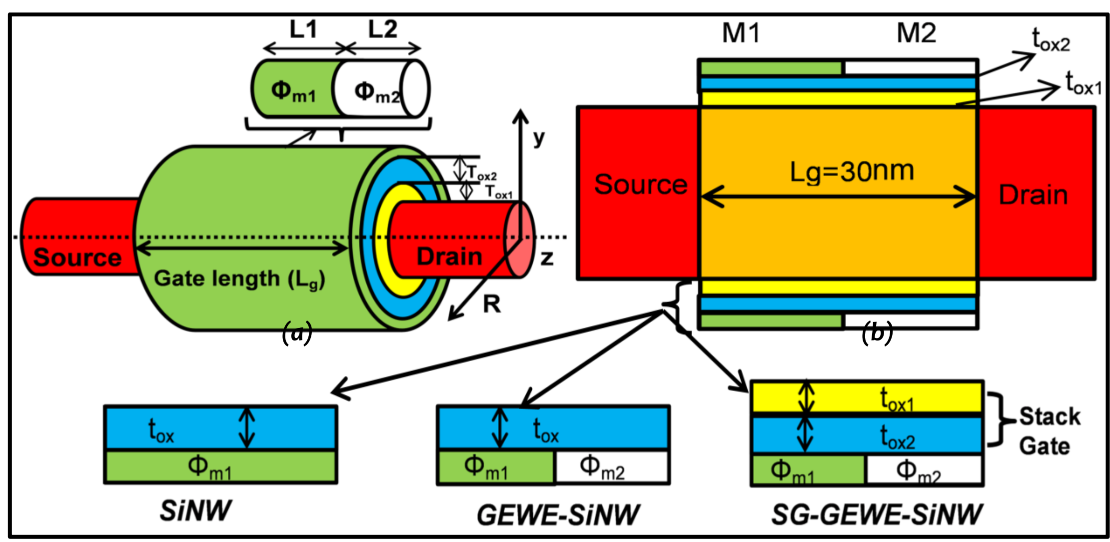


Figure 6.02: (a) Simulated Device Structure of SG-GEWE-SiNW MOSFET, (b) 2-D schematic view of SG-GEWE-SiNW MOSFET.(Gupta & Chaujar, 2016b)

Table 6.01: Default Parameters of High-k

Properties ↓ / Materials →	Si_3N_4	HfO_2	ZrO_2
Dielectric Constant (k)	7.5	25	30
Band-Gap [eV]	5.3	5.8	5-7
Thickness of High-k Dielectric Constant	0.576	1.85	2.3

Table 6.02: Default design parameters used in the analysis

Design Parameters	SiNW	GEWE-SiNW	SG-GEWE-SiNW
Channel Length (L_g)	30nm	30nm	30nm
Substrate Doping (N_A)	$1x10^{16}$ cm^{-3}	$1x10^{16}$ cm^{-3}	$1x10^{16}$ cm^{-3}
Radius of Nanowire (R)	5nm	5nm	5nm
Source/Drain Doping (N_D^+)	$5x10^{19}$ cm^{-3}	$5x10^{19}$ cm^{-3}	$5x10^{19}$ cm^{-3}
Effective Oxide Thickness (t_{ox})	t_{ox}=1.5nm	t_{ox}=1.5nm	t_{ox}=1.5nm t_{ox1}=1.2nm (SiO_2) t_{ox2}=1.85nm (HfO_2)
Dielectric Constant	k=3.9	k=3.9	k_1=3.9, k_2=24
Gate Metal Work function	Φ_m =4.8eV	Φ_{m1}=4.8eV [Gold] Φ_{m2}=4.4eV [Titanium]	Φ_{m1}=4.8eV [Gold] Φ_{m2}=4.4eV [Titanium]

Table 6.03: Boundary Conditions

Boundary Conditions			
1. SURFACE POTENTIAL	**SiNW**	**GEWE-SiNW**	**SG-GEWE-SiNW**
a) At the interface of two metals	φ_m	$\varphi_{m1}=\varphi_{m2}$	$\varphi_{m1}=\varphi_{m2}$
b) At source end (z=0)	$\varphi=V_{bi}$	$\varphi=V_{bi}$	$\varphi=V_{bi}$
c) At drain end	$\varphi=V_{bi}+V_{ds}$	$\varphi_D=V_{bi}+V_{ds}$	$\varphi_D=V_{bi}+V_{ds}$
2. ELECTRIC FIELD			
a) At the interface of two metals	E= $\frac{\partial\varphi_1(r,z)}{\partial z}$	$\frac{\partial\varphi_1(r,z)}{\partial z}=\frac{\partial\varphi_2(r,z)}{\partial z}$ at z=L1	$\frac{\partial\varphi_1(r,z)}{\partial z}=\frac{\partial\varphi_2(r,z)}{\partial z}$ at z=L1
b) At the Centre of Cylindrical Channel	$\frac{\partial\varphi_1(r,z)}{\partial r}=0$	$\frac{\partial\varphi_1(r,z)}{\partial r}=0$	$\frac{\partial\varphi_1(r,z)}{\partial r}=0$
c) At Si/SiO_2 Interface	$\frac{\partial\varphi_1(r,z)}{\partial r}=\frac{q.n_a}{\varepsilon_{si}}=C_{ox}(V_{gs}-V_{FB}-\varphi_s)$ $C_{ox}=\frac{\varepsilon_{SiO_2}}{R\ln\left(1+\frac{t_{ox}}{R}\right)}$	$\frac{\partial\varphi_1(r,z)}{\partial r}=\frac{q.n_a}{\varepsilon_{si}}=C_{ox}(V_{gs}-V_{FB1}-\varphi_s)$ $\frac{\partial\varphi_2(r,z)}{\partial r}=\frac{q.n_a}{\varepsilon_{si}}=C_{ox}(V_{gs}-V_{FB2}-\varphi_s)$ $C_{ox}=\frac{\varepsilon_{SiO_2}}{R\ln\left(1+\frac{t_{ox}}{R}\right)}$	$\frac{\partial\varphi_1(r,z)}{\partial r}=\frac{q.n_a}{\varepsilon_{si}}=C_{ox}(V_{gs}-V_{FB1}-\varphi_s)$ $\frac{\partial\varphi_2(r,z)}{\partial r}=\frac{q.n_a}{\varepsilon_{si}}=C_{ox}(V_{gs}-V_{FB2}-\varphi_s)$ $C_{ox}=\frac{\varepsilon_{SiO_2}}{R\ln\left(1+\frac{t_{eff}}{R}\right)}$ $t_{eff}=t_{SiO_2}+\left(\frac{\varepsilon_{SiO_2}}{\varepsilon_{high-k}}\right)t_{high-k}$
where V_{bi}=built in potential, φ_{m1} and φ_{m2} are surface potentials due to metal gate 1 and 2 respectively, V_{FB1} and V_{FB2} are flat band voltage due to metal gate 1 and 2 respectively, R is the radius of nanowire and t_{eff} is the effective oxide thickness of stack gate design.			

6.3 Simulation Methodology

All the simulations have been performed using the same physical models as mentioned in chapter-2. Also, numerical methods such as BICGST (bi-conjugate gradient stabilized) have been considered to obtain the solutions with improved convergence in 3D device structure. Moreover, fabrication feasibility of SiNW and GEWE scheme has already been discussed in chapter-3. In addition to this, high-k stack gate are formed by reactive sputtering and oxidation, in which high-k layers are formed by sputtering followed by oxidation (Lee et al, 2003). Also, atomic layer deposition technique and plasma nitridation coupled with metal-organic chemical vapor deposition are also available for high-k stack gate architecture (Rittersma et al, 2006).

6.4 Results and Discussion

6.4.1 Optimization of High-k Gate Stack and Gate Metal Workfunction

A. Analog Figure of Merits (FOMs)

In this subsection, the effect of dielectric constant and gate metal workfunction engineering is examined in terms of switching ratio, sub-threshold slope (SS), device efficiency, channel resistance and output resistance as analog FOMs.

i. Switching Ratio and Device Efficiency

As is evident from Fig. 6.03(a), on-current is higher in the case of HfO_2 due to lowering of tunneling current owing to higher band-gap and band-offset in comparison to Si_3N_4 and ZrO_2. Consequently, a switching ratio which is an important criterion for any analog application also enhances with HfO_2 due to reduced off-current as indicated by Fig. 6.03(a). Further, as high-k dielectric increases, the

threshold voltage (V_{th}) increases due to a reduction in off-current but SS decreases as shown in Fig, 6.03(c). Moreover, the effect of workfunction difference is also examined by considering HfO_2 as a gate-stack and varying the workfunction at the drain end (Φ_{M2}) by keeping source side metal workfunction constant (Φ_{M1}).

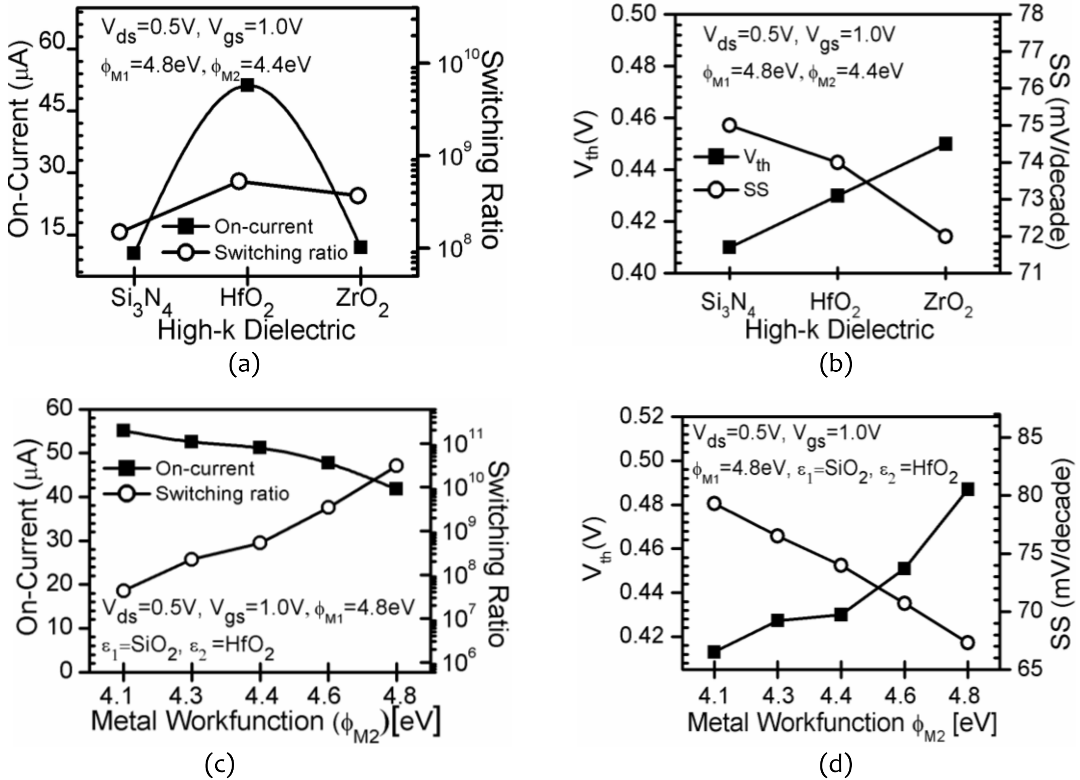


***Figure 6.03:** (a-d) On-Current, switching ratio and Threshold Voltage, Sub-threshold Swing for different high-dielectrics and metal gate workfunction (Φ_{M2}) at V_{ds}=0.5V and V_{gs}=1.0V. (Gupta & Chaujar, 2016c)*

As gate metal workfunction at the drain end (Φ_{M2}) decreases or workfunction difference increases (ΔW), on-current rises significantly as shown in Fig. 6.03(c) due to redistribution of the electric field in the channel region owing to step potential due to workfunction difference which enhances carrier transport efficiency and thus the current driving capability as is manifest from contour plots shown in the Fig. 6.04(a-e) and this effect is more apparent if workfunction difference increases as stated in

(Long & Chin, 1997), thus, also signifies the suppression of short channel effects. On the contrary, switching ratio reduces with increase in workfunction difference as exhibited in Fig. 6.03(c). This reduction is due to workfunction engineering scheme in which there is a high electric field in the channel that results into tunneling of carriers and causes higher off-current and thus degrades the switching ratio.

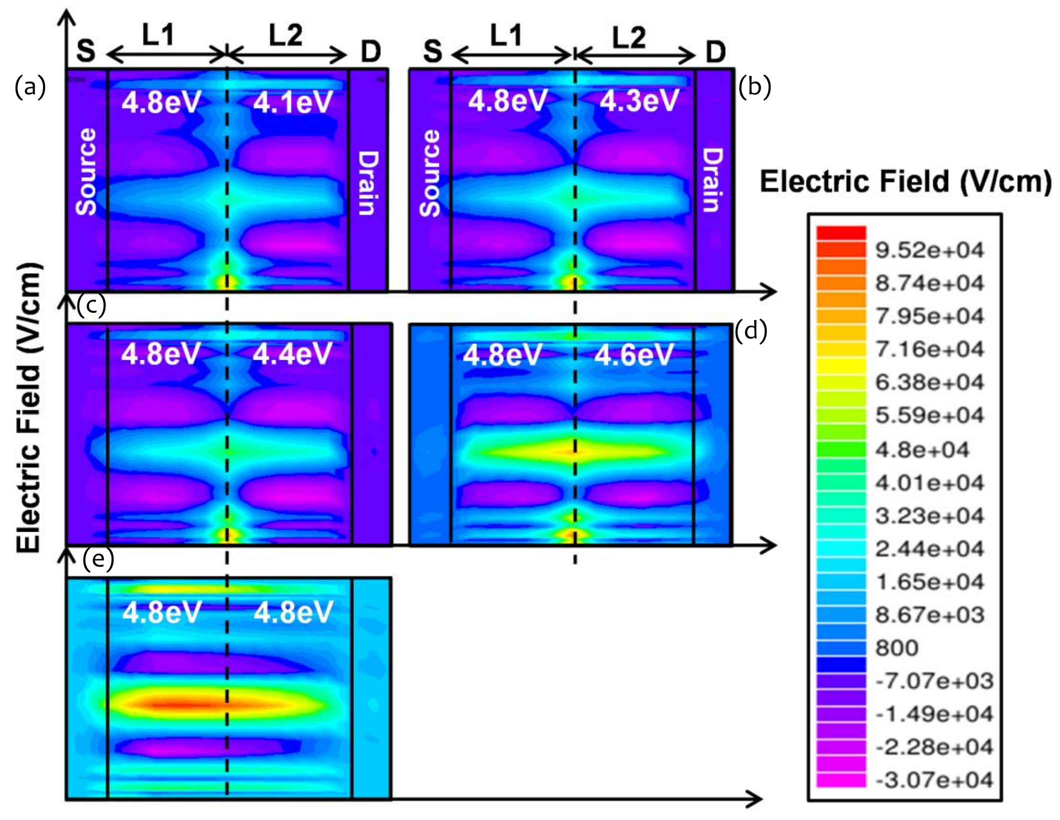


***Figure 6.04:** (a-e) Electric Field Distribution for different metal gate workfunction (Φ_{M2}) at V_{ds}=0.5V and V_{gs}=1.0V.*

Hence, the trade-off between on-current and off-current is required to optimize the switching ratio depending upon the applications. Moreover, V_{th} rises with an increase in workfunction at the drain end. As workfunction difference decreases, the efficacy of GEWE scheme reduces and thus reduces the on-current as shown in Fig. 6.03(c) thereby enhancing threshold voltage as reported in Fig. 6.03(d). As revealed by Fig.

6.03(c), sub-threshold current (off-current) decreases as workfunction difference increases due to which sub-threshold swing reduces as demonstrated in Fig. 6.03(d).

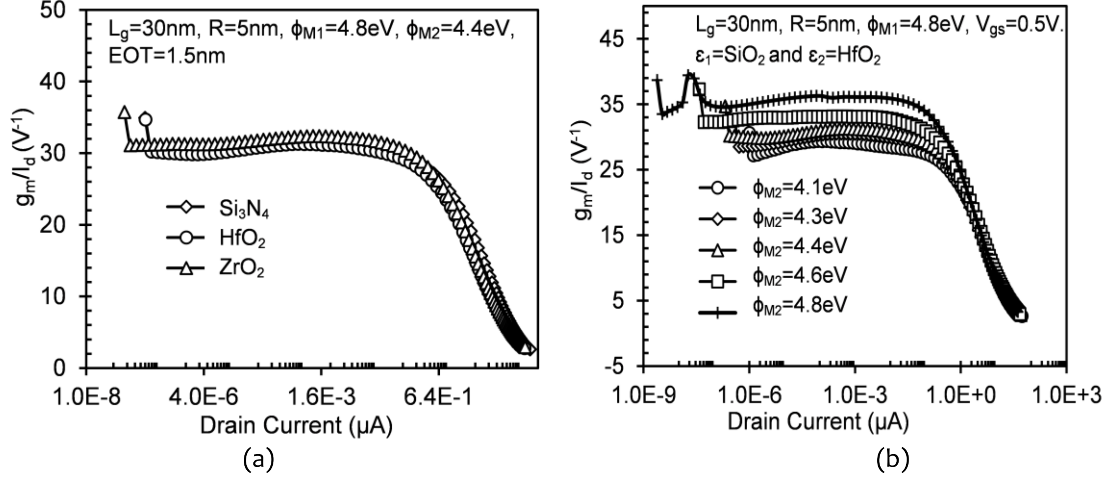


Figure 6.05: (a-b) Device Efficiency as a function of drain current for different high-dielectrics and metal gate workfunction (Φ_{M2}) at V_{ds}=0.5V and V_{gs}=1.0V.

Also, device efficiency [D.E] (g_m/I_d) is an important parameter in the design of analog circuits, which offers the measure of efficiency to convert power into speed. Fig. 6.05 (a) shows the device efficiency as a function of drain current for different high-k materials. It is clearly shown that the variation of D.E occurs mainly at the weak-inversion region of operation and in the saturation region; device efficiency reduces due to a reduction in transconductance and increment in on-current. The decrease in D.E. with HfO_2 is due to large deviation in drain current as compared to transconductance. Further, with the tuning of workfunction difference of metal gates, D.E. of HfO_2 gate stack increases as revealed by Fig. 6.05(b) owing to enhanced transconductance with an increase in workfunction difference.

ii. Output Resistance and Channel Resistance

The output resistance (R_{out}) of a MOSFET is the inverse of the output conductance. The most important characteristics of R_{out} in the circuit design are the maximum R_{out}

which decides the maximum available power gain for the device. Fig.6.06 (a-d) shows that in the linear region (V_{ds}=0-0.4V),

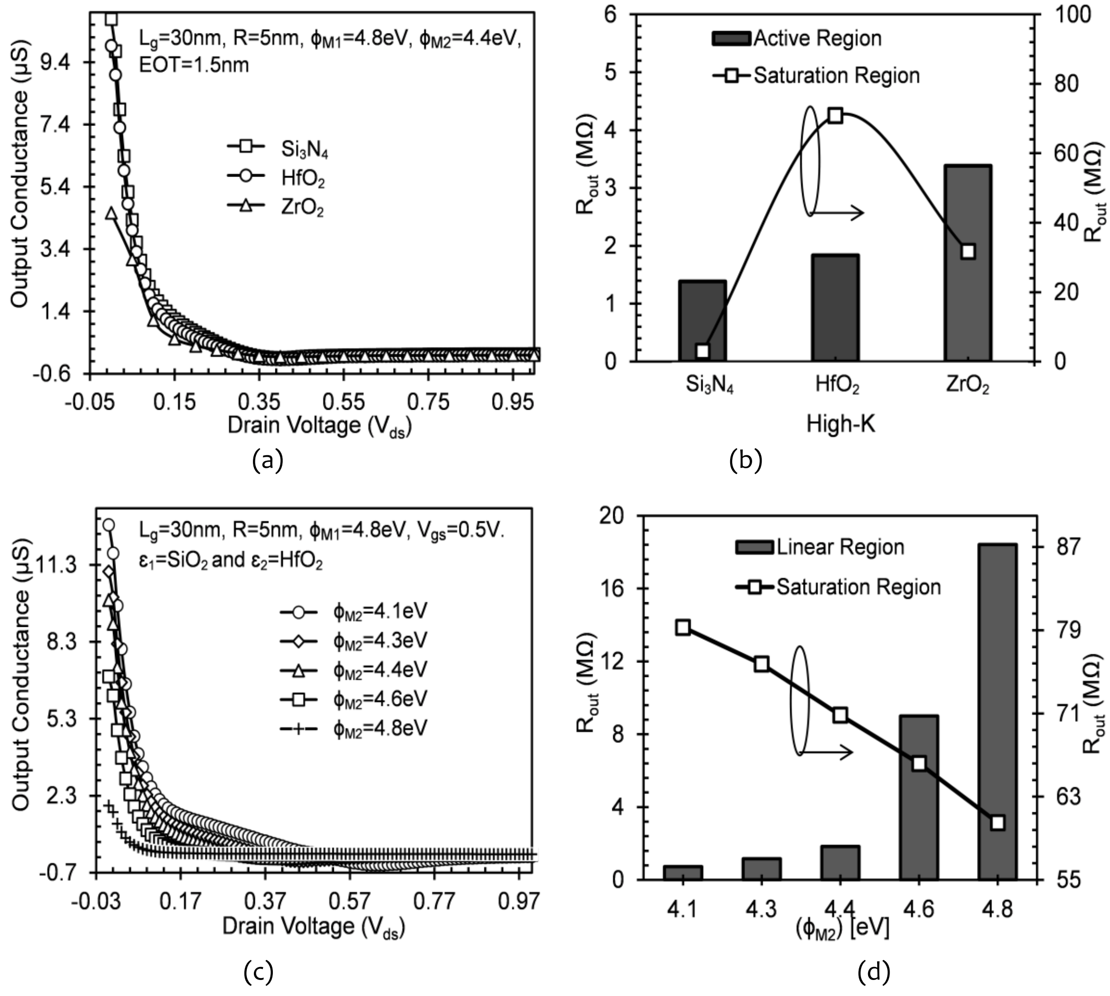


Figure 6.06: (a-d) Output conductance and R_{out} as a function of drain voltage for different high-dielectrics and metal gate workfunction (Φ_{M2}) at V_{gs}=1.0V

R_{out} decreases, and it is desirable when the circuit is to act as an ideal voltage source, and as drain bias reaches saturation (V_{ds}=0.4-0.8V), R_{out} rises due to increasing drain current. This effect is more pronounced for HfO_2 in comparison to other high-k dielectrics. As ΔW increases, output resistance (=1/g_D) reduces in the linear region, and as drain bias increases to saturation, its value increases as evident from Fig. 6.06(c).

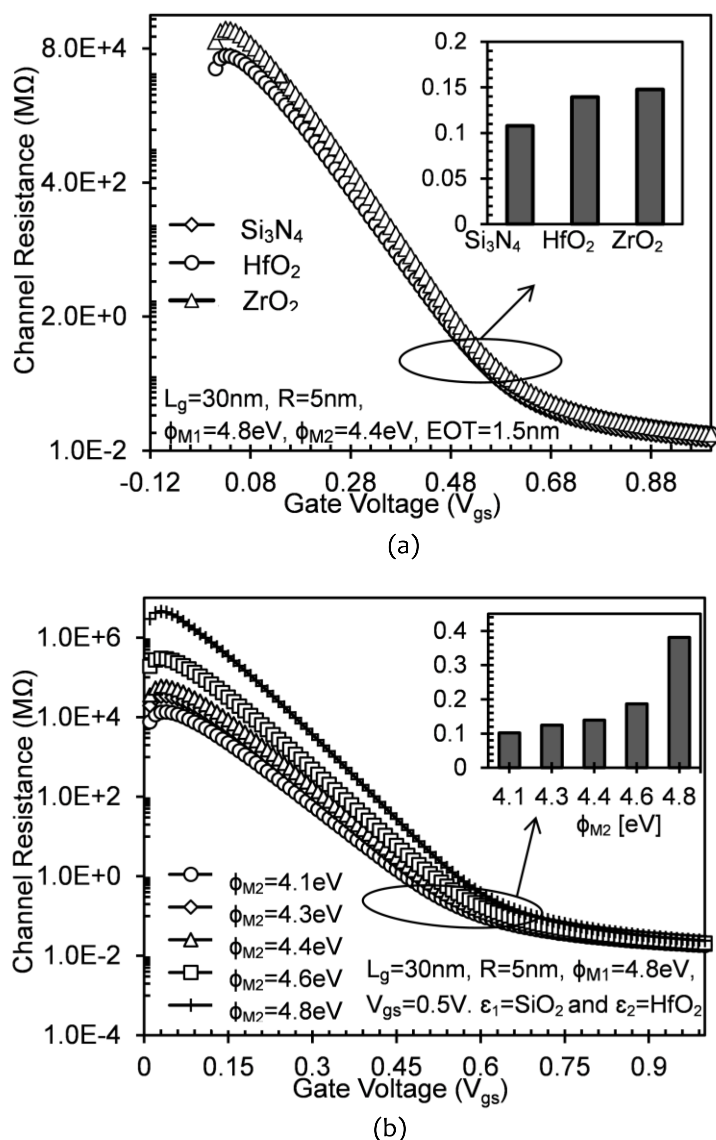


Figure 6.07: (a-b) Channel Resistance as a function of gate voltage for different high-dielectrics at V_{ds}=0.5V.

Thus, higher ΔW (approx. 0.7eV) of SG-GEWE-SiNW is beneficial for analog applications. Likewise, channel resistance (R_{ch}) of a MOSFET reveals the resistance of carriers in the channel region. As is clearly shown in Fig. 6.07(a) that with the incorporation of HfO_2 as a high-k layer onto the interfacial layer, R_{ch} decreases and as V_{gs} increases, electrostatic gate control enhances and thus reduces channel resistance. This region is called linear, ohmic or triode region. On the other hand, as

workfunction at the drain end increases, carrier concentration decreases in the channel as is evident in contours of Fig. 6.08(a-e), due to which R_{ch} increases as shown in Fig. 6.07(b) which implies enhancement in the current driving capability of GS-GEWE-SiNW as ΔW increases. Thus, we have to choose optimum values of both high-k and workfunction difference for improved analog performance.

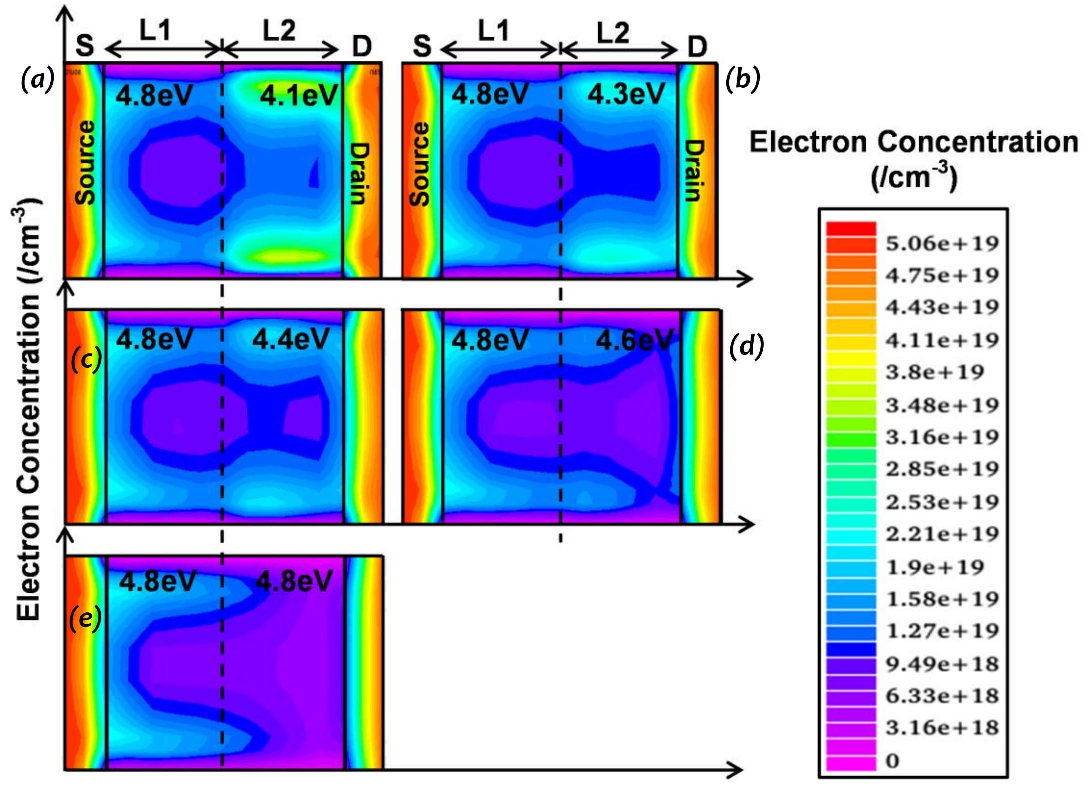


Figure 6.08: (a-e) Electron Concentration Distribution for different metal gate workfunction (Φ_{M2}) at V_{ds}=0.5V and V_{gs}=1.0V.

B. Linearity and Harmonic Distortion Analysis

In this sub-section, linearity and distortion performance of SG-GEWE-SiNW MOSFET is investigated with an aim to find optimum high-k and gate workfunction difference for highly linear performance with low harmonic distortion. Non-linearity of MOS amplifiers is mainly due to higher order transconductance harmonics (g_{m3})

that may interfere with the fundamental frequency and causes non-linearity. The metrics used in this work to evaluate the device linearity performance and intermodulation distortion are higher order transconductance coefficients, VIP3, third-order input intercept point (IIP3), 1-dB intercept point and distortion such as second and third order harmonic distortion (HD2, HD3), third-order intermodulation distortion (IMD3) (Chaujar et al, 2008; O hAnnaidh & Brazil, 2004) which are defined as follows:

$$VIP3 = \sqrt{\frac{24 \times g_{m1}}{g_{m3}}} \quad \text{….. (6.2)}$$

$$IIP3 = \frac{2}{3}\frac{g_{m1}}{g_{m3} \times Rs} \quad \text{…. (6.3)}$$

$$1 - dB\,Compression\ \text{Point} = 0.22 \times \sqrt{\frac{g_{m1}}{g_{m3}}} \quad \text{…. (6.4)}$$

where $g_{m1} = \frac{\partial I_d}{\partial V_{gs}}$, $g_{m3} = \frac{\partial^3 I_d}{\partial V^3_{gs}}$ and R_S=50Ω

g_{m3} is a third-order derivative of I_d-V_{gs} characteristics and its amplitude should be minimized for lower distortion. The value of V_{GS} at which the higher order of transconductance parameters (g_{m3}) becomes zero is known as zero crossover point (ZCP) which decides the optimum DC bias point for device operation. Higher gain can be realized by setting DC bias point close to V_{th}. Fig. 6.09(a-b) shows the variation of g_{m3} as a function of gate overdrive voltage (V_{gs}-V_{th}) and the results indicate that incorporation of GS over GEWE-SiNW MOSFET lowers the amplitude of g_{m3} in comparison to GEWE-SiNW due to lowering of tunneling current which improves gate controllability and hence, transconductance and its harmonic distortion. Also, the DC bias points shifts towards lower V_{gs} by changing the dielectric constant

as shown in Fig. 6.09(b). Among all dielectrics, HfO_2 shows better improvement in terms of lower distortion (g_{m3}) and lower bias point in comparison to other high-k.

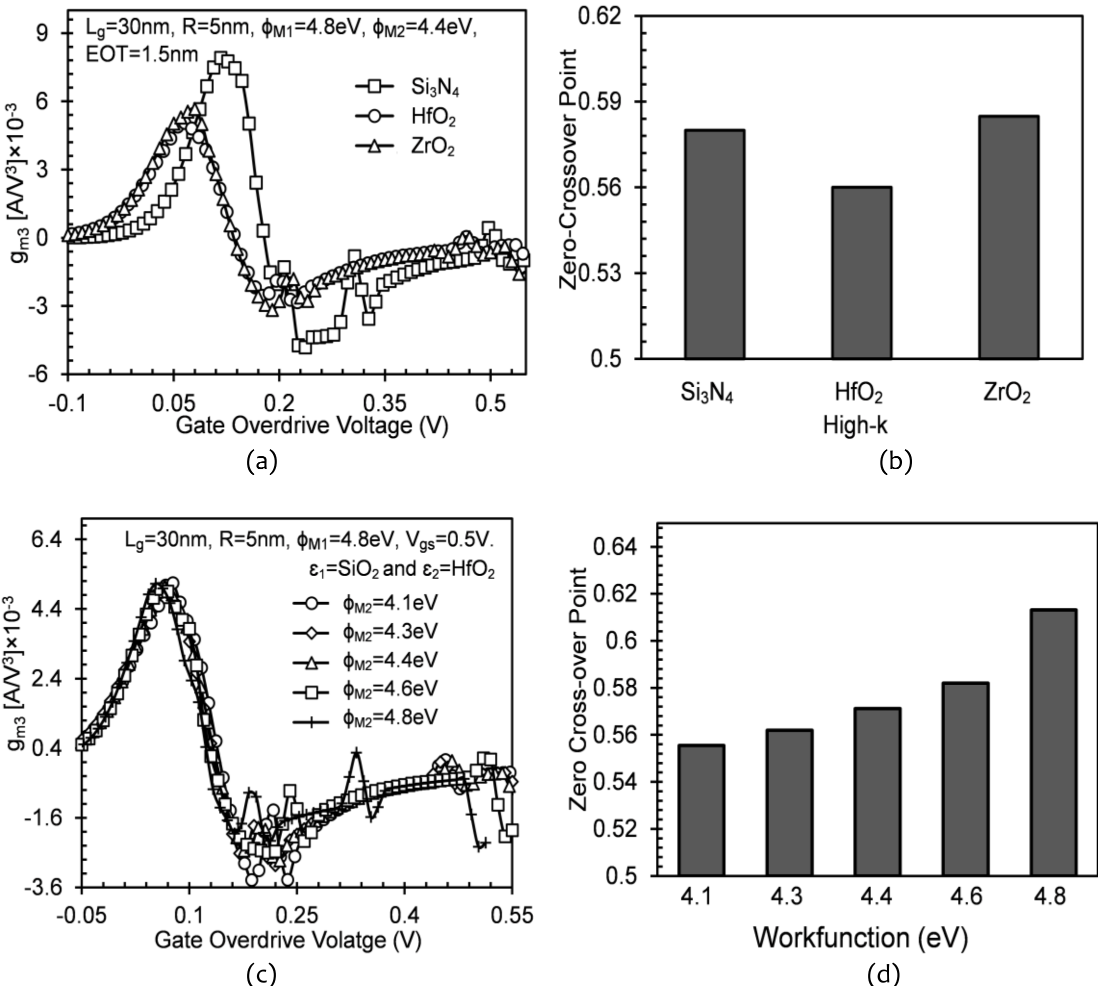


Figure 6.09: (a-c) Higher order transconductance coefficients g_{m3}, (b-d) Zero-Crossover Point for different high-dielectric materials at V_{ds}=0.5V.

With the increase in metal gate workfunction at the drain end (or reduces ΔW), there is not as much change in amplitude of g_{m3} as is evident from Fig. 6.09(c) due to change in on-current as reflected by Fig. 6.03(c) but the DC bias point shifts towards lower V_{gs} if ΔW increases as shown in Fig. 6.09(d).

i. VIP3/IIP3 and 1-dB Compression Point

In all linearity FOMs, generally two peaks are appearing: one at a lower gate bias and maxima at higher gate bias for GS-GEWE-SiNW MOSFET. However, for analog circuit applications, it is desired that device should operate in moderate inversion region and not in the saturation region where power dissipation is more. So, in this analysis, a maximum appearing at a lower value of V_{gs} is considered for comparison. VIP3 represents extrapolated input voltage at which first and third order harmonics of drain current is equal and expressed as in Eq. 6.2. The peak of VIP3 reveals the cancellation of third-order nonlinearity coefficient by device internal feedback around second-order nonlinearity.

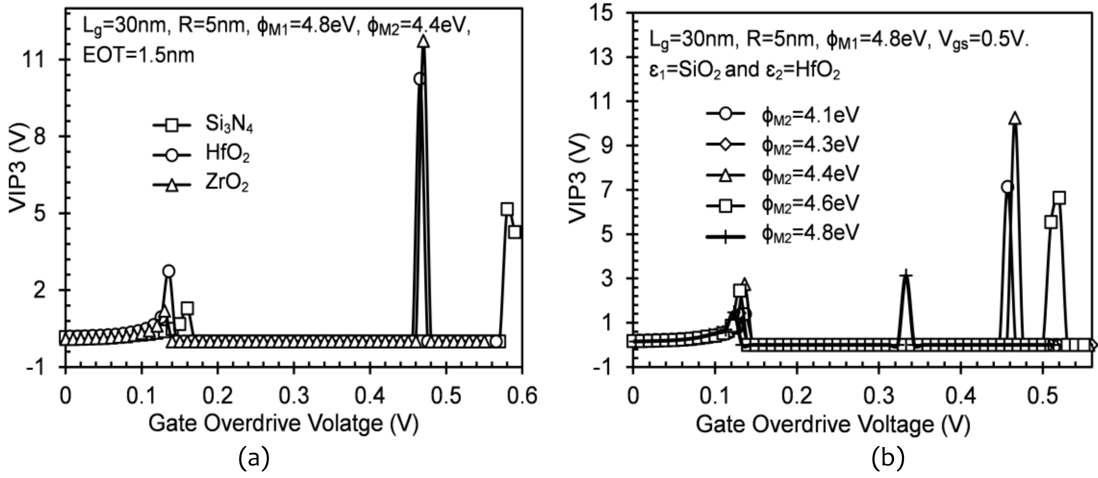


Figure 6.10: (a-b) VIP3 as a function of gate overdrive voltage and VIP3 for different gate metal workfunction at the drain end (Φ_{M2}) at V_{ds}=0.5V and V_{gs}=1.0V

Fig 6.10(a) shows that peak value of VIP3 increases significantly in the case of gate-stack architecture at lower V_{gs}-V_{th} due to lowering of g_{m3} as given by eq.6.2 and enhancement in transconductance (g_{m1}) owing to high on-current and improvement in carrier mobility. The peak value of VIP3 increases by 34% in HfO_2 in comparison to Si_3N_4 and is observed at lower bias voltage as shown in Fig. 6.10(a). By adjusting

ΔW, VIP3 peak value improves appreciably due to imroved transconductance and reduced distortion as evident from Fig. 6.10(b). Moreover, there are two important FOMs which govern amplifier's efficiency and linearity i.e. third-order intercept point (IIP3) and 1-dB compression point (1dB CP). In general for MOS based amplifiers, higher the output at the intercept, the better the linearity.

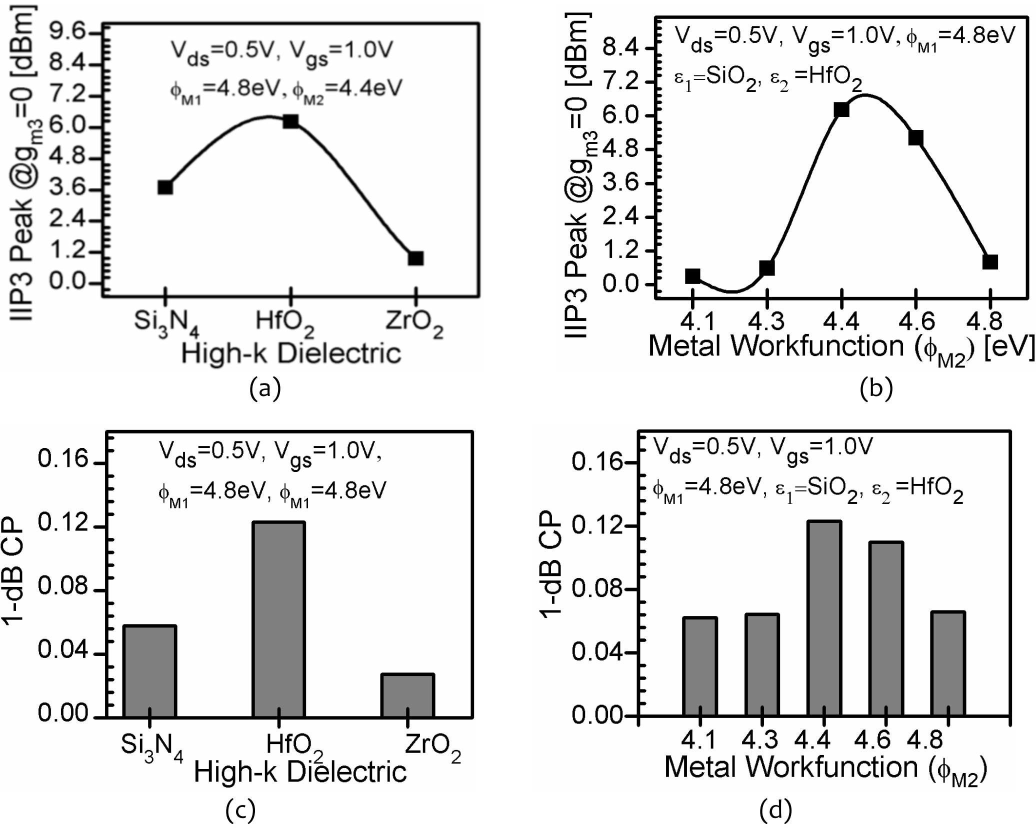


Figure 6.11: (a-d) IIP3 and 1-dB Compression Point for different high-k dielectrics and metal gate workfunction (Φ_{M2}) at V_{ds}=0.5V and V_{gs}=1.0V

Third-order intercept is a theoretical point at which the third-order distortion signal amplitudes equal the input signals, and it is useful in determining the linearity condition of an amplifier. IIP3 increases to a peak value (i.e. g_{m3}=0) and IIP3 peak enhances with the incorporation of gate stack scheme, and its magnitude is higher in the case of HfO_2 due to high band offset which reduces the off-current, improves

transconductance and thus enhances IIP3 as shown in Fig, 6.11(a). The 1-dB compression point is the parameter that describes a circuit's tolerance to desensitization. It is essential to identify at what point compression occurs so that input levels can be limited to prevent distortion. It is usually the input power that causes the gain to decrease 1 dB from the normal linear gain specification. This parameter signifies the maximum input power that the amplifier circuit can handle by providing a fixed amount of gain, and if the input power surpasses the compression point, the gain starts falling. Hence, it is desirable that a 1-dB compression point should be as high as possible for the high linear amplifier. The effect of high-k dielectrics on 1-dB compression point is presented in Fig. 6.11(c). The result shows 1-dB compression point in case of HfO_2 enhances by 1.4 and 2.3 times in comparison to Si_3N_4 and ZrO_2 respectively owing to reduced signal distortions and transconductance as stated in Eq. 6.4. Moreover, by modulating ΔW, linearity improves appreciably in terms of high IIP3 and 1-dB CP peak in comparison to other cases due to a reduction in higher order harmonics and improvement in on-current as is evident from Fig.6.11 (b) and 6.11(d).

ii. Harmonic Distortions

Harmonic distortion (HD) is an essential reliability issue in analog and RF circuit applications that arises owing to the non-linear performance of devices. Nonlinearity may induce intermodulation (IM), which generate signals with frequencies different from the input ones. These unwanted signals may fall into the band of interest, interfering or even corrupting the desired components (Dutta et al, 2014). Therefore, improved linearity performance of GEWE-SiNW MOSFET with HfO_2 as a gate stack is observed in the previous sub-section. In the following sub-section, Harmonic

Distortion FOMs such as 2nd order HD (HD2), 3rd Order HD (HD3) and 3rd Order Intermodulation Distortion (IMD3) for the device are analyzed considering the effect of the gate stack and workfunction engineering. The distortion has been calculated through the integral function method (IFM) since this approach permits the distortion extraction from DC measurements without the need of an AC characterization, contrary to Fourier-based methods (Cerdeira et al, 2004; Doria et al, 2008). The approximate analytical expressions for HD2, HD3 and IMD3 are given as:

$$HD2 = 0.5V_a \frac{\left(\frac{dg_{m1}}{dV_{GT}}\right)}{2g_{m1}} \quad \text{.... (6.5)}$$

$$HD3 = 0.25V_a^2 \frac{\left(\frac{dg_{m1}^2}{dV_{GT}^2}\right)}{6g_{m1}} \quad \text{.... (6.6)}$$

$$IMD3 = \left(\frac{9}{2} \times (VIP3)^3 \times g_{m3}\right)^2 \times R_S \quad \text{... (6.7)}$$

where V_{GT} is gate overdrive voltage (V_{gs}-V_{th}) and V_a is the amplitude of AC signal and considered to be very small, of about 50mV for the IFM analysis.

Fig.6.12 (a) shows HD2 and HD3 as a function of gate overdrive voltage for GEWE-SiNW incorporating different high-k as a gate stack with SiO_2. It is observed that HD2 and HD3 are significantly reduced in HfO_2 at lower overdrive voltage (V_{GT}) in comparison to other high-k materials. This reduction is due to higher transconductance owing to high on-current and is in accordance with Eq. 6.5 and 6.6.

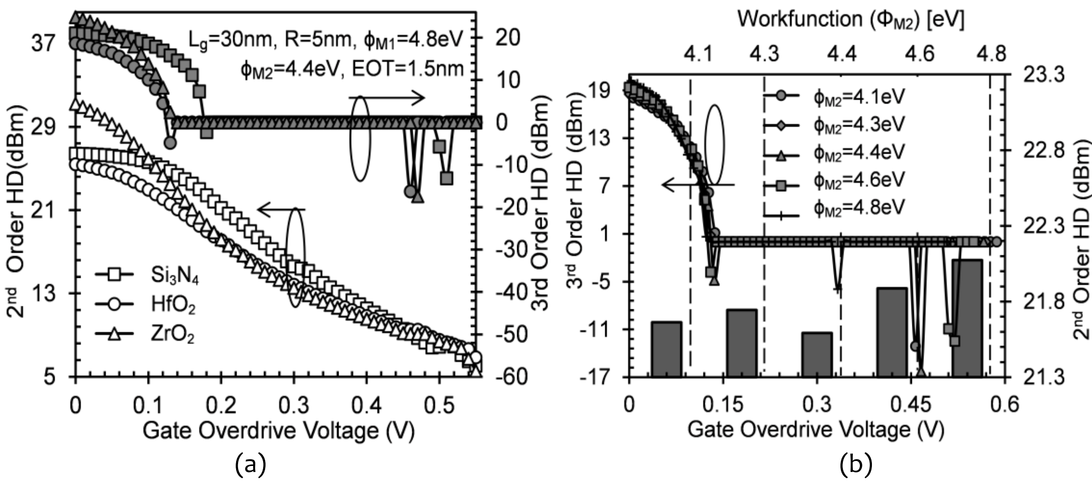


Figure 6.12: (a-b) 2nd order Harmonic Distortion and 3rd Order Harmonic Distortion as a function of V_{GT} for different high-k and metal gate workfunction (Φ_{M2}) at V_{gs}=1.0V, V_{ds}=0.5V.

IMD3 denotes the intermodulation harmonic power at which the first and third order intermodulation harmonic powers are equal. IMD3 plays a major role in determining intermodulation distortion in CMOS RF amplifiers, since these applications make use of both phase and amplitude modulation. Therefore, reduction of IMD3 in the RF front-end transceiver parts is of great importance for maximizing overall system performance and minimizing distortions. Fig 6.13(a) exhibits that IMD3 reduces with the incorporation of gate-stack design on GEWE-SiNW MOSFET, and this decrement is due to a reduction in higher order harmonics (g_{m3}) which originates from the non-linear transistor's I_{ds}-V_{gs} characteristic according to Eq. 6.7. Moreover, distortions in GS (HfO_2+SiO_2)-GEWE-SiNW is further reduced by tuning gate metal workfunction as indicated by Fig. 6.12(b) and 6.13(b). As ΔW increases, gate controllability improves due to enhancement in carrier velocity which enhances g_{m1} and so from Eq. 6.5-6.6 again, it is reflected that HD2, HD3 and IMD3 reduces. Thus, by appropriate selection of high-k material and gate metal workfunction, GS-GEWE-SiNW achieves high linearity with minimum distortion for RF amplifier

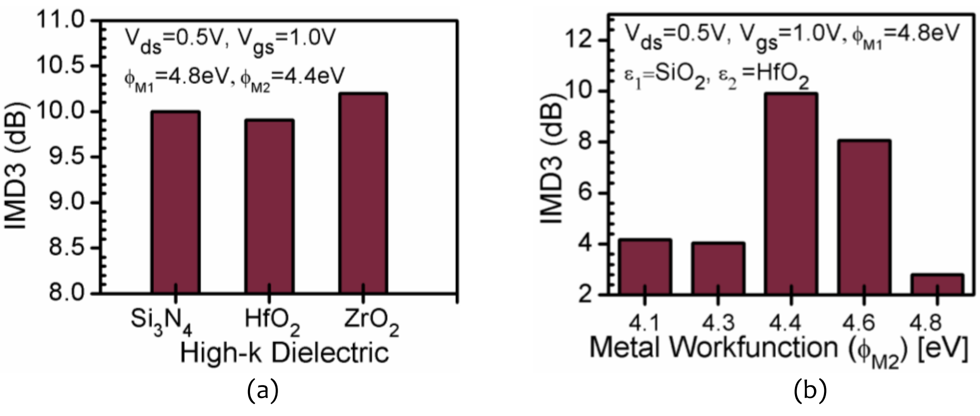


Figure 6.13: (a-b) IMD3 for different high-k and metal gate workfunction (Φ_{M2}) at V_{gs}=1.0V, V_{ds}=0.5V

6.4.2 Reliability Issues of SG-GEWE-SINW MOSFET

A. Analog Performance

In this sub-section, the analog performance of all three device structures is studied under different temperatures (200K-600K) with an aim to analyze the reliability issues in terms analog FOMs such as on-current, device efficiency, switching ratio, Sub-threshold swing (SS) and Threshold Voltage (V_{th}). Fig. 6.14(a) shows the transfer characteristics of SiNW, GEWE-SiNW and GS-GEWE-SiNW MOSFET for different temperatures. With an increase in temperature, the drain current rises but at a particular bias point, current starts decreasing with increase in temperature. This point is called Zero Crossing Point (ZCP) or Temperature Compensation Point (TCP). At this point, the effect of temperature is cancelled by two main controlling terms i.e. channel mobility (decreases I_D) and threshold voltage (increases I_D), since the temperature dependency of the drain current is influenced by V_{th} as given by:

$$I_D \approx \mu_{eff}\left[V_{gs} - V_{th}(T)\right] \qquad \text{...... (6.8)}$$

The TCP is desirable for wide temperature ICs applications where the *V-I* characteristics show little or no variation with respect to temperature. With the

increase in temperature, the on-current decreases due to degradation in mobility of carriers owing to more scattering of carriers. However, on-current of SG-GEWE-SiNW is comparatively high in comparison to GEWE-SiNW due to the incorporation of thin layer of HfO_2, which improves current driving capability of the device.

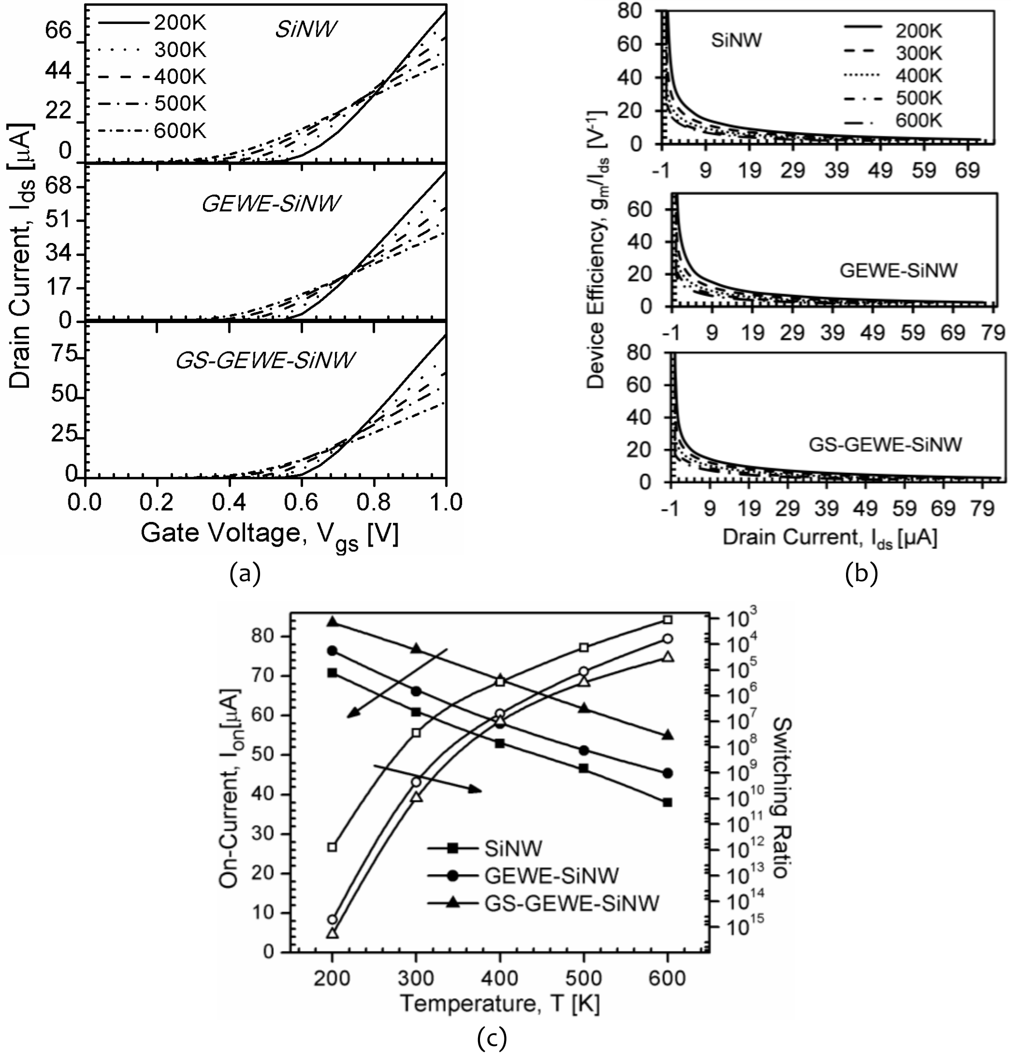


Figure 6.14: (a) Transfer Characteristics, (b) Drain transconductance and (c) Device Efficiency of SiNW, GEWE-SiNW and GS-GEWE-SiNW MOSFET for different temperatures.

Fig. 6.14(b) shows the device efficiency as a function of drain current for different temperatures. It is observed that device efficiency degrades in all three devices as temperature increases due to enhanced drain current in the linear region. Moreover,

switching ratio is an important parameter for digital and analog applications and it is clearly evident from Fig. 6.14(c) that with an increase in temperature switching ratio degrades in an exponential manner for all three devices since phonon scattering is dominant at high temperature which degrades the off-current. SG-GEWE-SiNW shows better switching performance in comparison to GEWE-SiNW due to lowering of tunneling carriers owing to gate stack engineering. Fig. 6.15(a) indicates that the threshold voltage (V_{th}) degrades with an increase in temperature due to shift in Fermi level and band-gap energy. In general, MOSFET's I-V characteristics are proportional to the square of the overdrive voltage. Hence, a small change in V_{th} causes a significant shift in the output current. Therefore, it is essential to calculate the V_{th} accurately with temperature changes. This change is more prominent at high temperature (600K) in SG-GEWE-SiNW MOSFET compared to its conventional counterparts.

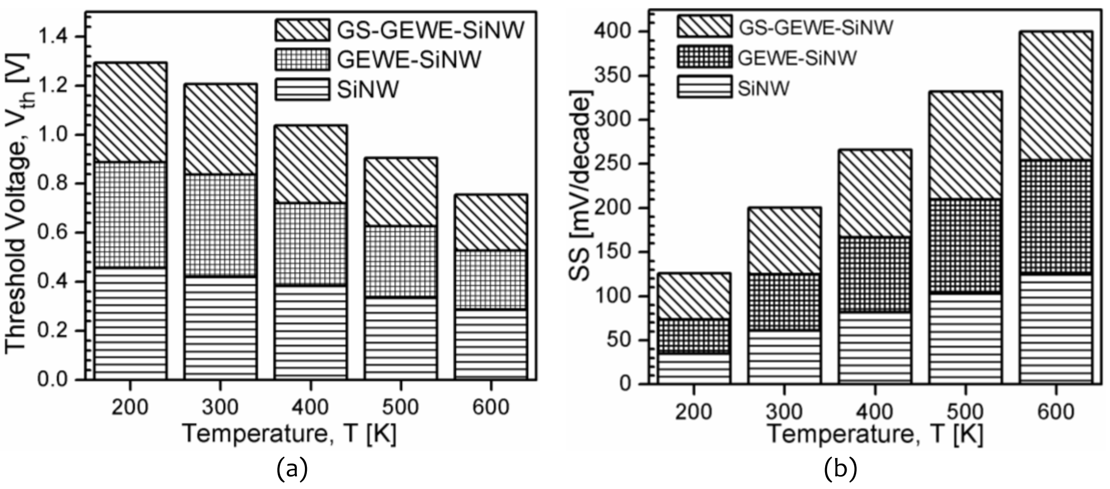


Figure 6.15: (a) Threshold Voltage, (b) Sub-threshold Swing and of SiNW, GEWE-SiNW and GS-GEWE-SiNW MOSFET

Further, the Subthreshold Swing (SS) is an important parameter for calculating the off-state current. At 200K, a low sub-threshold swing results in high I_{on}/I_{off} ratio

which indicates a faster transition between off and on states compared to 600K. SS of SG-GEWE-SiNW is 53mV/decade and 146mV/decade for 200K and 600K respectively in comparison to GEWE-SiNW and SiNW MOSFET as shown in Fig. 6.15(b). These results show SG-GEWE-SiNW is more reliable for analog and switching applications, at a lower temperature.

B. RF Noise Performance

In this sub-section, the impact of ambient temperature has been studied on the characteristics such as gate capacitance, cut-off frequency, intrinsic delay, energy delay product, noise conductance and minimum noise figure for SG-GEWE-SiNW MOSFET, GEWE-SiNW and SiNW MOSFET.

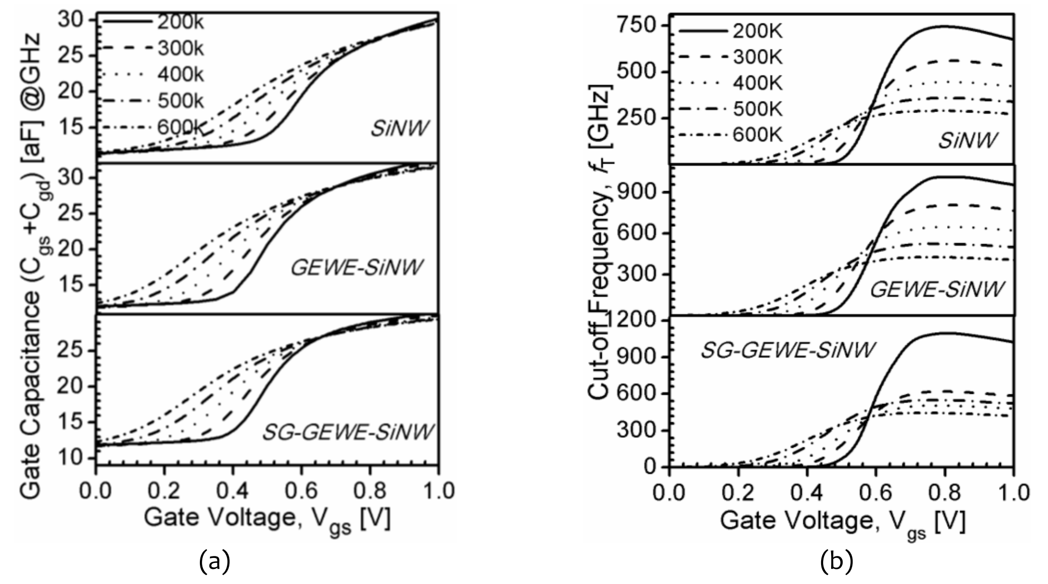


Figure 6.16: (a) Total Gate Capacitance (C_g) and (b) Cut-off frequency (f_T) of SiNW, GEWE-SiNW and GS-GEWE-SiNW MOSFET at V_{ds}=0.5V

If a MOSFET is operating in the linear region, both S/D regions are connected to the inversion layer, and C_g which is total gate capacitance is equally partitioned between source/drain i.e., $C_{gd} \approx C_{gs} \approx C_g/2$ where as in the saturation region, $C_{gs} \approx 2/3 \times C_g$ and $C_{gd} \approx 0$. Fig. 6.16(a) shows the bias dependent intrinsic parasitic gate capacitance (C_g)

at different temperatures, and it is observed that as temperature decreases, C_g also decreases resulting in device high speed which is desirable for switching and digital applications. Since, the gate capacitance is due to charges present in the inversion region including the depletion charges of source and drain regions. These charge carriers are temperature and bias dependent. C_g is sufficiently lower in the case of SG-GEWE-SiNW due to gate stacking engineering scheme and GEWE scheme which results in the improved screening of conducting channel from drain variations. For evaluating the RF performance of the device, cut-off frequency (f_T) is one of the utmost important parameter. As is evident from Fig. 6.16(b), the peak value of f_T enhances in the case of GEWE-SiNW in comparison to SiNW and its value further enhances with the incorporation of GS technology. As the temperature reduces, peak value of f_T enhances. This is due to a reduction in parasitic capacitance as shown in Fig. 6.16(a) and improvement in current driving capability as shown in Fig. 6.14(a) at a lower temperature (200K). Also, TCP in f_T is observed at 0.6V in the case of GEWE-SiNW MOSFET, which is useful for RF applications operating at low or high temperatures. Intrinsic Delay (τ) is another significant parameter defined as a measure of switching performance of the device. Fig. 6.17(a) reveals as temperature increases; delay degrades due to degradation in parasitic capacitance with an increase in temperature as shown in Fig. 6.16(a). A noticeable reduction in intrinsic delay of SG-GEWE-SiNW MOSFET than its conventional counterpart is also observed due to the incorporation of HfO_2 as a gate stack which increases the physical oxide thickness, reduces leakage current and thus enhances the on-current as is evident from Fig. 6.14(b),

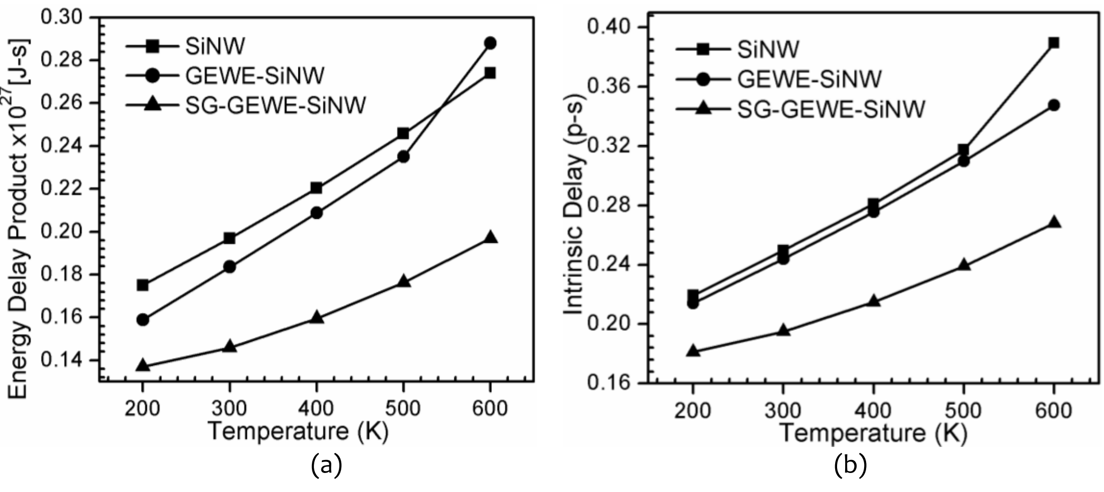
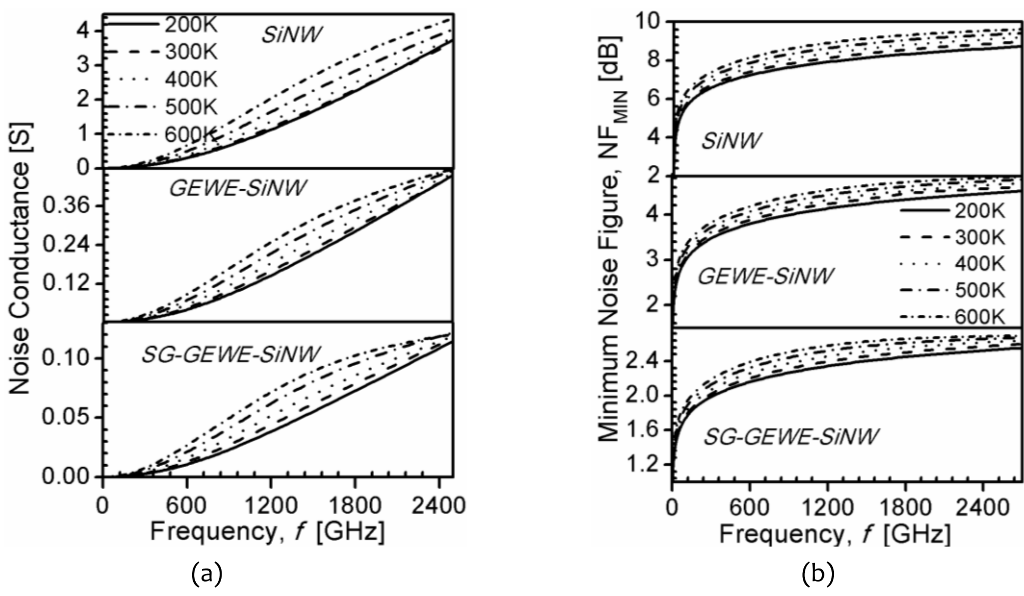


Figure 6.17: (a) Intrinsic Delay and (b) Energy Delay Product (EDP) of SiNW, GEWE-SiNW and GS-GEWE-SiNW MOSFET at V_{ds}=0.5V

In addition, reduction in parasitic capacitances also leads to a considerable reduction of intrinsic delay. Apart from these FOMs, Energy Delay Product (EDP) is a valuable FOM as far as circuit applications are concerned. The EDP is a measure of energy and is defined by the product of the average energy (E_{ave}) and the gate delay (τ). It calculates the energy consumed per switching event (such as in logic families). EDP improves at lower values of temperature due to a reduction in intrinsic delay and parasitic gate capacitance (C_g) as evident from Fig. 6.17(b). Thus, SG-GEWE-SiNW MOSFET emerged as a promising device for RF applications such as microwave/wireless at low temperature. Moreover, Noise FOMs such as Minimum noise figure (NF_{MIN}) and Noise Conductance (NC) are of utmost important for the designing of CMOS RF circuits at high frequency. Noise figure is an assessment of deterioration of signal to noise ratio caused by a component in RF signal chains. It is used to evaluate the performance of an amplifier or a radio receiver, with lower values specifying better performance.



(a) (b)

Figure 6.18: (a) Minimum Noise Figure (NF_{MIN}) and (b) Noise Conductance as a function of frequency for SiNW, GEWE-SiNW and SG-GEWE-SiNW MOSFET at V_{ds}=0.5V and V_{gs}=1.0V.

NC is used to estimate the power spectral density of noise current generators and low noise conductance is required in RF amplifiers and LNAs. As ambient temperature increases, both the NF_{min} and NC degrades for all three devices as shown in Fig. 6.18(a-b) due to high phonon scattering and the effect of temperature on noise FOMs is less observed in the case of SG-GEWE-SiNW, and its magnitude is comparatively low in comparison to other devices. Thus, the proposed design (SG-GEWE-SiNW) is more reliable and more thermally stable compared to SiNW at low temperatures.

C. Linearity and Harmonic Distortions

Non-linearity of MOS amplifiers is generally from transconductance higher order harmonics term (g_{m3}) that may interfere with fundamental frequency (ω_0) and causes non-linearity. It is a major reliability concern at device level. Lower the amplitude of g_{m3}, higher the linearity of the device. Fig. 6.19(a) shows that the amplitude of g_{m3} reduces as temperature increases, and SG-GEWE-SiNW is more linear in comparison

to other conventional devices owing to reduced off (leakage) current due to the amalgamation of HfO_2 layer over SiO_2, which results in enhanced on-current and thus lowering of g_{m3}.

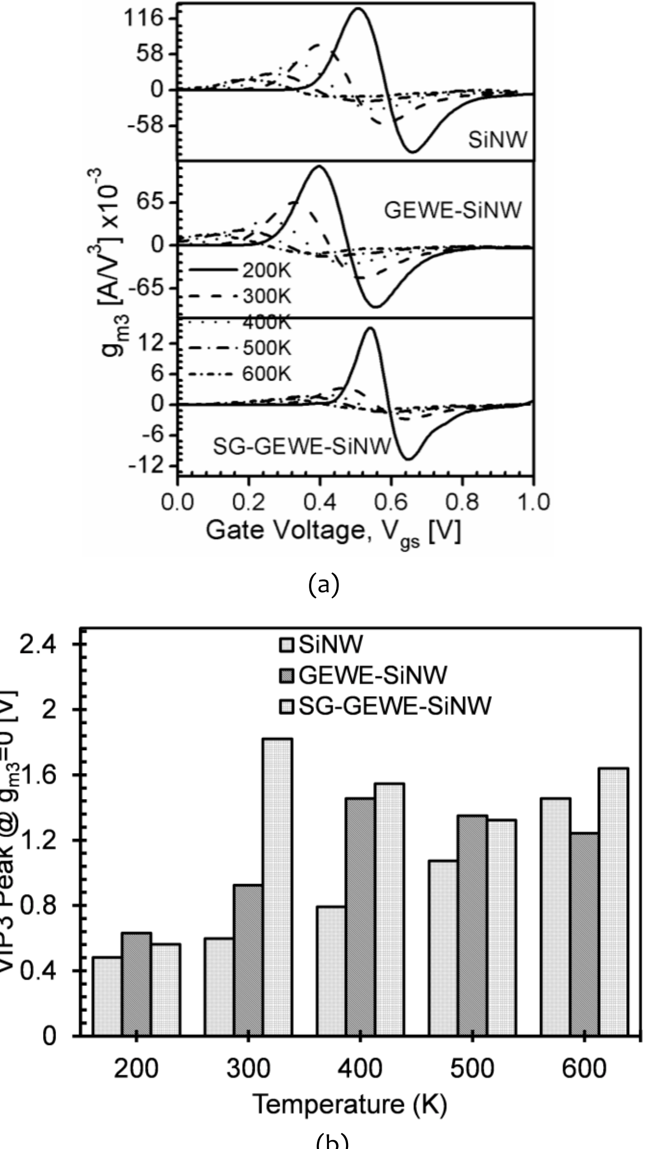


Figure 6.19: (a) g_{m3} and (b) VIP3 of SiNW, GEWE-SiNW and GS-GEWE-SiNW MOSFET for different temperatures at V_{gs}=1.0V and V_{ds}=0.5V.

The peak of VIP3 reveals the cancellation of third-order nonlinearity coefficient by device internal feedback around second-order nonlinearity. Fig 6.19(b) shows that peak value of VIP3 increases significantly in the case of gate-stack architecture at

300K due to lowering of g_{m3} and enhancement in transconductance (g_m) owing to high on-current and improvement in carrier mobility. Moreover, the main FOM which governs amplifier's efficiency and linearity is the third-order intercept point (IIP3). Third-order intercept is a theoretical point at which the third-order distortion signal amplitudes equal the input signals, and it is useful in determining the linearity condition of an amplifier. The peak value of IIP3 attains maximum value at 300K in SG-GEWE-SiNW and as temperature increases its value deteriorates but in the case of GEWE-SiNW and SiNW, peak value of IIP3 increases as temperature increases as is shown in Fig. 6.20, thus signifying that SG-GEWE-SiNW MOSFET is more linear and thus more reliable at a lower temperature. Another important parameter which decides the reliability in Analog and RF circuits is Harmonic distortion (HD) that arises owing to the non-linear performance of device.

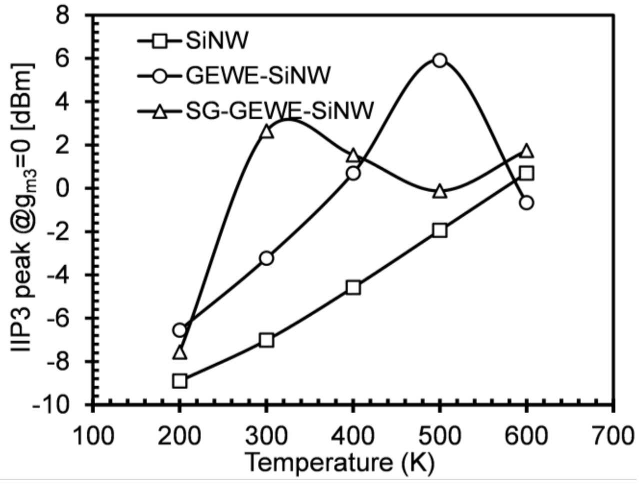


Figure 6.20: VIP3 of SiNW, GEWE-SiNW and GS-GEWE-SiNW MOSFET for different temperatures at V_{gs}=1.0V and V_{ds}=0.5V.

Nonlinearity sometimes induces intermodulation (IM), which generate signals with frequencies different from the input ones. These surplus signals may perhaps either

fall into the desired frequency band or even corrupting the desired components (Dutta et al, 2014). Therefore, Harmonic Distortions such as 2nd order HD (HD2), 3rd Order HD (HD3) and 3rd Order Intermodulation Distortion (IMD3) has also been studied. Fig.6.21 show HD3 significantly reduces as temperature increases due to higher transconductance owing to high on-current and is in accordance with Eq. 6.6 and reduction of HD3 is more prominent in SG-GEWE-SiNW MOSFET in comparison to its conventional counterparts. Furthermore, IMD3 plays a significant role in determining intermodulation distortion in CMOS RF amplifiers, since these applications make use of both phase and amplitude modulation. Therefore, reduction of IMD3 in the RF front-end transceiver parts is of great importance for maximizing overall system performance and minimizing distortions.

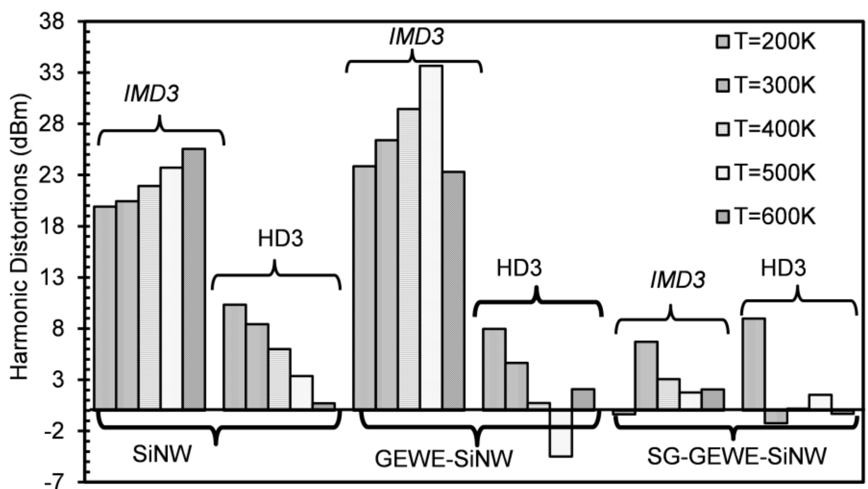


Figure 6.21: IIP3 of SiNW, GEWE-SiNW and GS-GEWE-SiNW MOSFET for different temperatures at V_{gs}=1.0 V and V_{ds}=0.5 V.

It is noticeably apparent from Fig. 6.21 that IMD3 is reduced appreciably as temperature reduces due to a reduction in higher order harmonics and VIP3. Thus, linearity performance of SG-GEWE-SiNW MOSFET degrades at low temperature and the performance improves as temperature rises.

6.5 SUMMARY

In this chapter, improved analog and intermodulation performance of GS-GEWE-SiNW MOSFET is demonstrated by considering the effect of both high-k materials and metal gate workfunction difference. It is observed that high-k material (HfO_2) as a gate stack over SiO_2 interfacial layer in GEWE-SiNW significantly influence the analog performance of the device by enhancing the current driving capability and lowering of leakage current owing to large band-gap of HfO_2. Moreover, reduction in the electric field at the drain end and high carrier concentration in the channel region is achieved by tuning of gate workfunction difference which results in improved analog metrics such as switching ratio, channel resistance, device efficiency for low power analog applications. The enhancement in on-current and lowering of g_{m3} results into 2.14 and 2.28 times improvement in VIP3 in comparison to Si_3N_4 and ZrO_2 respectively and the input power rises to 0.128 dB in HfO_2 with ΔW=0.4eV, which the device can handle without compression. It is also examined that the DC bias point is shifted towards lower input voltage which indicates lowering of dynamic power consumption for circuit applications.

In addition, effect of temperature on the Analog/RF and Linearity performance has also been studied with an aim to analyze the reliability issues of SG-GEWE-SiNW. Results reveal that SG-GEWE-SiNW MOSFET exhibits 1.1 and 1.2 times improvement in I_{on} and thus 29% and 9.3% enhancement in f_T at low temperature (200 K) in comparison to GEWE-SiNW and SiNW MOSFET owing to decrement in off-current and gate capacitance. Moreover, Noise FOMs also improved at 200 K but linearity FOMs slightly degrade but show high linearity at 300 K in SG-

GEWE-SiNW which might not hinder much with the device performance. Therefore, SG-GEWE-SiNW can an attractive solution at low temperatures for analog/digital circuits and space technology. In addition, it is found that ZTC is observed at lower gate bias for SG-GEWE-SiNW, which leads to significant improvement in static and dynamic performance. Thus, the results so obtained are serving as a worthy design tool for circuits operating at wide range of temperatures.

6.6 REFERENCES

Brezeanu, G., Brezeanu, M. & Bernea, F. (2010) High-K Dielectrics in Nano & Microelectronics, *Nat'l Seminar of Nanoscience & Nanotechnology, September edition*.

Cerdeira, A., Alemán, M. A., Estrada, M. & Flandre, D. (2004) Integral function method for determination of nonlinear harmonic distortion. *Solid-State Electronics*, 48(12), 2225-2234.

Chau, R., Datta, S., Doczy, M., Doyle, B., Kavalieros, J. & Metz, M. (2004) High-κ/metal-gate stack and its MOSFET characteristics. *IEEE Electron Device Letters*, 25(6), 408-410.

Chaujar, R., Kaur, R., Saxena, M., Gupta, M. & Gupta, R. (2008) Intermodulation distortion and linearity performance assessment of 50-nm gate length L-DUMGAC MOSFET for RFIC design. *Superlattices and Microstructures*, 44(2), 143-152.

Cui, Y., Zhong, Z., Wang, D., Wang, W. U. & Lieber, C. M. (2003) High performance silicon nanowire field effect transistors. *Nano letters*, 3(2), 149-152.

Del Alamo, J. A. (2011) Nanometre-scale electronics with III-V compound semiconductors. *Nature*, 479(7373), 317-323.

Doria, R. T., Cerdeira, A., Raskin, J.-P., Flandre, D. & Pavanello, M. A. (2008) Harmonic distortion analysis of double gate graded-channel MOSFETs operating in saturation. *Microelectronics Journal*, 39(12), 1663-1670.

Dutta, A., Koley, K. & Sarkar, C. K. (2014) Analysis of Harmonic distortion in asymmetric underlap DG-MOSFET with high-k spacer. *Microelectronics Reliability*, 54(6), 1125-1132.

Grasser, T. (2015) *Hot Carrier Degradation in Semiconductor Devices*Springer.

Grebennikov, A. (2011) *RF and microwave transmitter design*, *234*John Wiley & Sons.

Gupta, N. & Chaujar, R. (2016b) Investigation of temperature variations on analog/RF and linearity performance of stacked gate GEWE-SiNW MOSFET for improved device reliability. *Microelectronics Reliability*, 64, 235-241.

Gupta, N. & Chaujar, R. (2016c) Optimization of high-k and gate metal workfunction for improved analog and intermodulation performance of Gate Stack (GS)-GEWE-SiNW MOSFET. *Superlattices and Microstructures*, 97, 630-641.

He, G., Sun, Z., Li, G. & Zhang, L. (2012) Review and perspective of Hf-based high-k gate dielectrics on silicon. *Critical Reviews in Solid State and Materials Sciences*, 37(3), 131-157.

Hong, S.-H., Choi, G.-B., Baek, R.-H., Kang, H.-S., Jung, S.-W. & Jeong, Y.-H. (2008) Low-temperature performance of nanoscale MOSFET for deep-space RF applications. *IEEE Electron Device Letters*, 29(7), 775-777.

Houssa, M. (2003) *High k Gate Dielectrics*CRC Press.

Kim, J., Krishnan, S. A., Narayanan, S., Chudzik, M. P. & Fischetti, M. V. (2012) Thickness and temperature dependence of the leakage current in hafnium-based Si SOI MOSFETs. *Microelectronics Reliability*, 52(12), 2907-2913.

Kumar, A., Gupta, N. & Chaujar, R. (2016a) Power gain assessment of ITO based transparent gate recessed channel (TGRC) MOSFET for RF/wireless applications. *Superlattices and Microstructures*, 91, 290-301.

Lee, B. H., Oh, J., Tseng, H. H., Jammy, R. & Huff, H. (2006) Gate stack technology for nanoscale devices. *materials today*, 9(6), 32-40.

Lee, J., Suh, Y.-S., Lazar, H., Jha, R., Gurganus, J., Lin, Y. & Misra, V. (2003) Compatibility of dual metal gate electrodes with high-k dielectrics for CMOS, *Electron Devices Meeting, 2003. IEDM'03 Technical Digest. IEEE International*. IEEE.

Lo, S.-H., Buchanan, D., Taur, Y. & Wang, W. (1997) Quantum-mechanical modeling of electron tunneling current from the inversion layer of ultra-thin-oxide nMOSFET's. *IEEE Electron Device Letters*, 18(5), 209-211.

Long, W. & Chin, K. K. (1997) Dual material gate field effect transistor (DMGFET), *Electron Devices Meeting, 1997. IEDM'97. Technical Digest., International*. IEEE.

O hAnnaidh, B. & Brazil, T. J. (2004) An accurate nonlinear MOSFET model for intermodulation distortion analysis. *IEEE microwave and wireless components letters*, 14(7), 352-354.

Pradhan, K., Mohapatra, S., Sahu, P. & Behera, D. (2014) Impact of high-k gate dielectric on analog and RF performance of nanoscale DG-MOSFET. *Microelectronics Journal*, 45(2), 144-151.

Qi, W.-J., Lee, B. H., Nieh, R., Kang, L., Jeon, Y., Onishi, K. & Lee, J. C. (1999) High-K gate dielectrics, *Microelectronic Manufacturing'99*. International Society for Optics and Photonics.

Razavi, B. & Behzad, R. (1998) *RF microelectronics*, *1*Prentice Hall New Jersey.

Razavieh, A., Janes, D. B. & Appenzeller, J. (2013) Transconductance linearity analysis of 1-D, nanowire FETs in the quantum capacitance limit. *IEEE Transactions on Electron Devices*, 60(6), 2071-2076.

Register, L. F. & Ekerdt, J. G. (2004) A study on the material and device characteristics of hafnium oxynitride MOSFETs with TaN gate electrodes.

Ribes, G., Mitard, J., Denais, M., Bruyere, S., Monsieur, F., Parthasarathy, C., Vincent, E. & Ghibaudo, G. (2005) Review on high-k dielectrics reliability issues. *IEEE Transactions on Device and materials Reliability*, 5(1), 5-19.

Rittersma, Z., Vertregt, M., Deweerd, W., Van Elshocht, S., Srinivasan, P. & Simoen, E. (2006) Characterization of mixed-signal properties of MOSFETs with high-k

(SiON/HfSiON/TaN) gate stacks. *IEEE Transactions on Electron Devices*, 53(5), 1216-1225.

Salmani-Jelodar, M., Ilatikhameneh, H., Kim, S., Ng, K., Sarangapani, P. & Klimeck, G. (2016) Optimum high-k oxide for the best performance of ultra-scaled double-gate MOSFETs. *IEEE Transactions on Nanotechnology*, 15(6), 904-910.

Shannon, R. D. (1993) Dielectric polarizabilities of ions in oxides and fluorides. *Journal of Applied Physics*, 73(1), 348-366.

SILVACO, I. (2016) ATLAS User's Manual. *Santa Clara, CA, Ver*, 5.

Sun, J.-C., Taur, Y., Dennard, R. H. & Klepner, S. P. (1987) Submicrometer-channel CMOS for low-temperature operation. *IEEE Transactions on Electron Devices*, 34(1), 19-27.

Wilk, G., Wallace, R. & Anthony, J. (2000) Hafnium and zirconium silicates for advanced gate dielectrics. *Journal of Applied Physics*, 87(1), 484-492.

Wilson, L. (2013) International technology roadmap for semiconductors (ITRS). *Semiconductor Industry Association*.

Wong, H.-S., Frank, D. J., Solomon, P. M., Wann, C. H. & Welser, J. J. (1999) Nanoscale cmos. *Proceedings of the IEEE*, 87(4), 537-570.

Yu, C., Yuan, J. & Yang, H. (2004) MOSFET linearity performance degradation subject to drain and gate voltage stress. *IEEE Transactions on device and materials reliability*, 4(4), 681-689.

Zeng, Q., Oganov, A. R., Lyakhov, A. O., Xie, C., Zhang, X., Zhang, J., Zhu, Q., Wei, B., Grigorenko, I. & Zhang, L. (2014) Evolutionary search for new high-k dielectric materials: methodology and applications to hafnia-based oxides. *Acta Crystallographica Section C: Structural Chemistry*, 70(2), 76-84.

CHAPTER-7

Conclusion and Future Scope

- ☞ *This chapter summarizes the overall research work illustrated in this thesis*
- ☞ *In addition, the concrete conclusions drawn from the results presented in this thesis are also discussed.*
- ☞ *This chapter also discusses about the future scope of the present work; and how can this work be extended and used in future for further research directions.*

7.1 CONCLUSION

According to Moore's Law, the transistor size has shrunk to get higher device performance and reduce its cost, but short channel effects (SCEs) such as Drain Induced Barrier Lowering (DIBL), Hot-Carrier Effects (HCEs), Punch through, V_{th} roll-off, etc., hinders its performance. To overcome such limitations, various device designs and engineering schemes are reported in literature such as Dual Gate, Recessed channel, Multi-Gate, CNT FET, Nanowire FET, etc. In this thesis, SiNW MOSFET is mainly emphasized to overcome the scaling limitations and further to overcome the inherent drawback of silicon nanowire, gate engineering scheme i.e., Gate electrode workfunction engineering (GEWE) scheme is amalgamated onto SiNW MOSFET. To simulate this device, accurate transport model is required to assess their performance limits, since cross-sections of the device is expected to be a few nanometers wide. When the radius of the silicon nanowires is scaled down to a few nanometers, the classical model used may be inaccurate; therefore investigation of different transport models such as drift diffusion (DDM), energy balance (EBM) and hydrodynamic model (HDM) has been explored in ***Chapter-2*** in terms of analog metrics and found that for GEWE-SiNW MOSFET, HDM shows superior performance in terms of switching ratio owing to velocity overshoot, which has strong impact on the terminal currents. Also, high output impedance in case of DDM is observed and it is found that EBM is efficient for depicting the behavior of sub-micron devices. After scrutinizing the implications of transport models on GEWE-SiNW MOSFET, immunity against SCEs such as hot-carrier effects, DIBL, leakage current etc., is also explored in ***Chapter-2***. Simulation results reveal that with the incorporation of GEWE engineering scheme onto SiNW MOSFET, current driving

capability enhances significantly and thus transconductance owing to step potential profile and quantum confinement. DIBL is lowered in case of SiNW due to improved gate controllability over the channel owing to cylindrical gate design and with the amalgamation of GEWE scheme, DIBL further reduces in comparison to conventional MOSFET. GEWE-SiNW shows significant lessening in electron temperature and electron velocity at the drain end and lowering of gate current which indicates immunity against hot-carrier effects and thus reflecting its effectiveness in low power CMOS applications. Further, effect of scaling of oxide thickness and high-k oxide is also examined on above mentioned parameters and it is found that with t_{ox}=0.5nm, hot-carrier reliability, DIBL and thus device performance improves in comparison to t_{ox}= 2.5nm. In contrast, gate current increases due to tunneling of carriers through gate oxide and thus hampers the device performance and this anomaly is overcome by incorporating high-k oxide instead of SiO_2. GEWE-SiNW MOSFET with oxide thickness 0.5 nm and oxide dielectric 21 (HfO_2) is a suitable candidate for low power CMOS amplifiers and switching applications.

With the development of a highly-information-oriented society, the RF wireless communications market intensely grows up. Design of RF CMOS circuits in real products remains a challenge due to the strong limitations on power consumption and noise that leave very little design margin. Therefore, ***Chapter-3*** discusses the qualitative investigation of RF performance of GEWE-SiNW MOSFET using 3D device simulation. In GEWE-SiNW MOSFET, RF metrics such as cut-off and maximum oscillation frequency, key parameters for RF amplifiers and receivers demonstrates notable improvement. Power gains such as maximum available power

gain and maximum transducer power gain also improves owing to reduced parasitic capacitance and improved current driving capability. Moreover, device parameter variations is also observed in ***Chapter-3***, which indicates that with downscaling of gate length and modulation of workfunction difference of metal gates, RF metrics of GEWE-SiNW MOSFET improves further. But thinning of oxide thickness and radii of nanowire leads to degradation in RF performance of GEWE-SiNW MOSFET. Therefore, we have to select optimum values of device parameters for enhanced device performance at RF/Wireless applications.

As the MOSFET dimensions shrink, more of high order effects become apparent and have vital influence in the device performance at HF. Thus, the proper determination of the associated parameters is necessary to accurately predict the device's behavior under a wide variety of conditions. S-parameters are the most commonly used parameters that determine the small signal behaviour of device at RF. ***Chapter-4*** investigated the small signal behaviour of GEWE-SiNW MOSFET in terms of S-parameters and it is found that both reflection parameters (S_{11} and S_{22}) decreases appreciably owing to improved transconductance; and both transmission parameters (S_{21} and S_{12}) increases and thus signify higher gain at HF. Moreover, it is also observed that with modulating the gate length, channel doping and gate metal workfunction we can achieve desired s-parameters of GEWE-SiNW MOSFET. Furthermore, short channel MOSFETs has comparatively higher thermal noise than long channel MOSFET. This is due to short channel effects (SCEs) associated with hot-carrier effect. However, this issue of excess noise is an active area of investigation for amplifiers and receivers for RF communication. Chapter-4 also addresses the noise performance of GEWE-SiNW MOSFET for low noise amplifiers. Noticeable

reduction in minimum noise figure, noise conductance and cross-correlation of GEWE-SiNW MOSFET is found in comparison to SiNW and Conventional MOSFET. Moreover, tuning of gate metal workfunction difference improves noise metrics due to reduction in SCEs and improvement in transconductance. Thus, indicates its potential application for low-noise amplifiers (LNAs) at RF. At operating frequency moves into GHz range, then extrinsic parameters of a device come into consideration and dominate the intrinsic one. Thus, there is need to examine the extrinsic parameters and intrinsic parameters for realizing precise and predictive results in the simulation of designed circuit. In ***Chapter-5***, the extrinsic parameters of GEWE-SiNW MOSFET has evaluated using Cold-FET pinch-off method in which zero gate and drain bias is provided for device and then extract extrinsic resistances, capacitances and inductances. The effect of these parameters at high frequency is almost constant and comparatively less than SiNW MOSFET. After extracting, the effect of these parameters is de-embedding (removed) from intrinsic parameters. Thus, this chapter concludes that the de-embedded intrinsic parameters are improved significantly in GEWE-SiNW due to reduced effect of extrinsic parameters. Moreover, decrement in C_{sdx} (capacitance due to charge carriers in the channel region owing to DIBL) implies that DIBL is less pronounced in GEWE-SiNW MOSFET ar high frequency. In addition, quasi-static small signal model are solved analytically for GEWE-SiNW MOSFET in terms of Z and Y parameters. The modeling results match well with the Z and Y parameters extracted from 3D device simulations and thus validate the model.

Thinning of oxide thickness to 1.5nm or below causes tunneling of carriers and leads to surplus leakage current which degrades the device transfer characteristics

and thus analog/linearity performance. Therefore, to overcome this issue, stacked gate is integrated onto GEWE-SiNW MOSFET which is discussed in ***Chapter-6***. The main aim of this chapter is to first optimize the value of both high-k gate stack and gate metal workfunction for optimum device performance. This optimization is done in terms of analog and linearity FOMs such as switching Ratio, Sub-threshold Swing (SS), Device Efficiency, channel and output resistance, VIP3, IIP3, 1-dB Compression Point, IMD3, HD2 and HD3. It is found that with HfO_2 as a high-k layer and SiO_2 as an interfacial layer, analog performance improves appreciably due to lowering of leakage current and enhancement in current driving capability. HfO_2 stacked-GEWE-SiNW reveals high linearity at lower gate bias in comparison to GEWE-SiNW MOSFET.

For temperature dependent CMOS applications which require high or low temperature and demand of nano-transistors for that application, it is thus required to examine the device behaviour at wide range of temperatures. Therefore, after optimizing the stack gate in previous section, this section studied the reliability issues of SG-GEWE-SiNW MOSFET over a wide range of operating temperature (200-600K). Results so obtained are simultaneously compared with SiNW and GEWE-SiNW MOSFET. Comprehensive device performance is examined in terms of analog, linearity, and RF Noise FOM and found two temperature compensation point where device FOMs become independent of temperature one for analog and linearity and another for RF Noise performance. Results reveal that performance metrics enhances noticeably at low temperature in SG-GEWE-SiNW owing to improvement in drain current and reduction in parasitic capacitances in comparison to its counterparts. Linearity FOMs shows a slight degradation in performance at 200K but improves significantly at

300K. Therefore, SG-GEWE-SiNW can be considered as an attractive and promising device for low temperature analog/digital circuits and in space technology. Moreover, these results can be served as a worthy design tool for circuits/ devices operating at wide range of temperatures.

7.2 FUTURE RESEARCH DIRECTIONS

The work discussed in this thesis mainly emphasized on analog and RF performances of proposed nanowire MOSFET using extensive 3D-TCAD device simulation. However, some aspects of proposed device structure still needs examination at sub-nm regime. Thus, based on exploration carried out in the present thesis, some ideas for future work is included in this section

- This work can be further extended by performing quantum analytical modelling of GEWE-SiNW MOSFET considering the effect of SCEs in terms of threshold voltage, drain current etc. to verify the simulated results.
- Moreover, the work discussed here neglected the effect of defects arises during fabrication and due to SCEs and thus this can be done in future work to examine the comprehensive device reliability of GEWE-SiNW MOSFET considering the defects.
- Further, the effect of fringing field becomes prominent when gate stacking is used. Therefore, there is a need to consider this effect to accurately depict the device behaviour at sub-nm regime.

- Device performance of GEWE-SiNW MOSFET can further be studied as circuit response for digital circuit applications such as for CMOS inverters and other gated logic designs.
- Nano-electronics especially nanowires emerge as most promising candidate in sensors, radiation therapy etc. Thus an effort can be made to study the sensing-application of this proposed device structure.

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Quantum analysis based extraction of frequency dependent intrinsic and extrinsic parameters for GEWE-SiNW MOSFET

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Abstract This paper examines the bias-independent and bias-dependent extrinsic and intrinsic parameters of the gate electrode workfunction engineered (GEWE) silicon nanowire (SiNW) metal–oxide–semiconductor field-effect transistor (MOSFET) by considering quantum effects. The results reveal that the effect of extrinsic parameters such as the resistance, capacitance, and inductance of the electrodes is less pronounced in the GEWE-SiNW compared with the conventional SiNW or conventional MOSFET. The intrinsic transconductance of the GEWE-SiNW device can be further improved by tuning the gate metal workfunction difference, which results in shorter time constant and lower parasitic capacitance, making it suitable for radiofrequency integrated circuit (RFIC) design. It is also observed that, in the saturation region, the device exhibits improved transconductance and noticeable reduction in C_{sdx} [due to drain-induced barrier lowering (DIBL)] but the parasitic capacitance and time constant also reduce. In addition, a non-quasi-static small-signal model has been studied in terms of Z and Y parameters; the results show good agreement with the results of three-dimensional (3D) simulations at thousands of GHz.

Keywords Extrinsic and intrinsic parameters · Gate electrode workfunction engineering (GEWE) · Quantum models · Silicon nanowire (SiNW) · Z and Y parameters · Modeling

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1 Introduction

Accurate modeling of nonlinear transistors for RF and microwave circuits is required. As the complexity of high-frequency (HF) circuits and systems continues to increase, there is also a need to reduce design cost, enhance performance, and meet tight limits regarding spurious discharge/emission. For RF modeling, a transistor is usually divided into two parts: an intrinsic part, which includes the nonlinear elements describing the operation of the transistor, and an extrinsic part, which accounts for the metallization, substrate, and semiconductor that connect the intrinsic model to the outside world [1,2]. The intrinsic components are generally voltage dependent, whereas the extrinsic components are usually considered to be independent of voltage, i.e., passive components. As operating frequencies increase into the GHz range, the importance of the extrinsic component (the part outside the channel region) dominates over its intrinsic counterpart. Therefore, there is a need for RF models that consider the behavior of both the intrinsic and extrinsic components of a device to achieve accurate predictions from simulations of designed circuits [3,4]. Earlier work reported the effect of extrinsic and intrinsic parameters on complementary metal–oxide–semiconductor (CMOS) RF performance [5]. Moreover, Alam et al. [6] reported the extrinsic series resistance of a RF MOSFET using a small-signal model. In addition, highly scaled CMOS devices show short-channel effects (SCEs), making them inappropriate for use in HF applications [7]. To overcome this drawback, various device structures have been proposed to alleviate the issue of SCEs at high frequency [8–10]. SiNW devices are the most promising candidates due to the stronger quantum confinement, which results in higher mobility compared with bulk silicon, as well as their scalability to a few nanometers, which is challenging to obtain via conventional silicon technology [11–13].

Improved analog and RF performance of SiNW devices have already been reported in literature [14]. Also, the effect of the source-to-drain capacitance due to DIBL in the SiNW MOSFET was investigated by Cho et al. [15]. Cho et al. [16] also examined the intrinsic and extrinsic parameters of junctionless SiNW devices, including the small-signal behavior in terms of Y parameters. However, the SiNW MOSFET with a SiO_2 gate faces the major problem of lower threshold voltage than desired in the very large-scale integration (VLSI) industry. Tuning the channel doping to correct V_{th} is difficult due to the narrow cylindrical NWs, and carrier mobility is also impacted by higher channel doping. Hence, tuning via gate electrode work function engineering (GEWE) [17] represents a better solution. In this regard, Gupta et al. [18,19] demonstrated that, using GEWE on gate-all-around (GAA) SiNW devices alleviated SCEs including DIBL and hot-carrier effects (HCEs), and also showed that the GEWE-SiNW MOSFET achieved cutoff frequency of thousands of GHz, making it suitable for use in RF/microwave applications [20]. Also, the effect of extrinsic and intrinsic parameters has not been reported for the GEWE-SiNW MOSFET till now. Therefore, in this work, the effect of extrinsic and intrinsic parameters was evaluated using the pinch-off cold-FET method, then these parasitics were removed from the device under consideration, a technique known as de-embedding. Furthermore, to examine the effect of device parameters on these parameters, metal gate engineering and bias variation were also investigated. The small-signal Z and Y parameters of the GEWE-SiNW MOSFET were also studied by excluding the effect of the extrinsic parameters. This paper is an extension of [21].

2 Device description and simulation methodology

Figure 1a and b present the simulated 3D device structure of the SiNW and GEWE-SiNW MOSFET, respectively. The default structural parameters and their values for these devices are stated in Table 1. In the GEWE-SiNW MOSFET, the metal gate consists of two regions: region 1 (near the source, L1 = 15 nm) and region 2 (near the drain L2 = 15 nm), which is towards 45-nm-node CMOS technology as stated in the International Technology Roadmap for Semiconductors (ITRS) [22]. Region 1 consists of gate metal with workfunction of 4.8 eV (gold), whereas region 2 is a titanium metal gate with workfunction of 4.4 eV. Meanwhile, in the case of the SiNW MOSFET and conventional MOSFET, the entire gate metal is gold. To analyze the device performance fairly, all three devices were optimized for the same threshold voltage, i.e., 0.4 V. All simulations were carried out using the Silvaco Atlas simulator [23]. Figure 1c and d show contour plots of the electron concentration along the channel of the SiNW and GEWE-SiNW device, respectively. It is evident from these contours that, when using the GEWE scheme, the electron concentration in the channel increases, resulting in improved current driving capability compared with the SiNW MOSFET owing to the step potential profile due to the two dissimilar metal gates, thereby reducing the electric field at the drain end and thus providing hot-carrier reliability [24].

Table 1 Default design parameters of the SiNW and GEWE-SiNW MOSFET

Parameter	Value
Channel length (L_g)	30 nm
Radius of SiNW (R)	5 nm
Oxide thickness (t_{ox})	1.5 nm
Source/drain doping (N_D^+)	$5 \times 19\,\text{cm}^{-3}$
Channel doping (N_A)	$1 \times 16\,\text{cm}^{-3}$

The physical models invoked during simulation were electric-field-dependent and concentration-dependent carrier mobilities, Shockley–Read–Hall recombination–generation with doping-dependent carrier lifetime, inversion-layer Lombardi CVT mobility model, high-field saturation model, and quantum-mechanical model [23]. To incorporate channel quantization and ballistic transport phenomena, we adopted the quantum-mechanical model [Bohm quantum potential (BQP)], which is more precise than the drift–diffusion method in the subnanometer range, since the inversion charge layer thickness in the conducting SiNW channel is comparable to the NW dimension. The energy balance model (EBM) and hydrodynamic model (HDM) can also be used in conjunction with the BQP model, where the quantum potential adjusts the semiclassical potential in a similar way as for the continuity equations. The model introduces a position-dependent quantum potential Q, which is added to the potential energy of a given carrier type. This quantum potential is derived using the Bohm interpretation of quantum mechanics [25] and is described below:

According to Bohm's interpretation of quantum mechanics, the wave function in a polar representation can be written as

$$\psi = R \cdot \exp\left(\frac{jS}{\hbar}\right), \tag{1}$$

where $\hbar$ is $h/2\pi$, R is the probability density per unit volume, and S has dimensions of action (energy $\times$ time).

Substituting Eq. (1) into the time-independent Schrödinger equation yields

$$\frac{\hbar^2}{2}\nabla\left\{M^{-1}\nabla\left[R \cdot \exp\left(\frac{jS}{\hbar}\right)\right]\right\} + Q \cdot R \exp\left(\frac{jS}{\hbar}\right) = E \cdot R \cdot \exp\left(\frac{jS}{\hbar}\right), \tag{2}$$

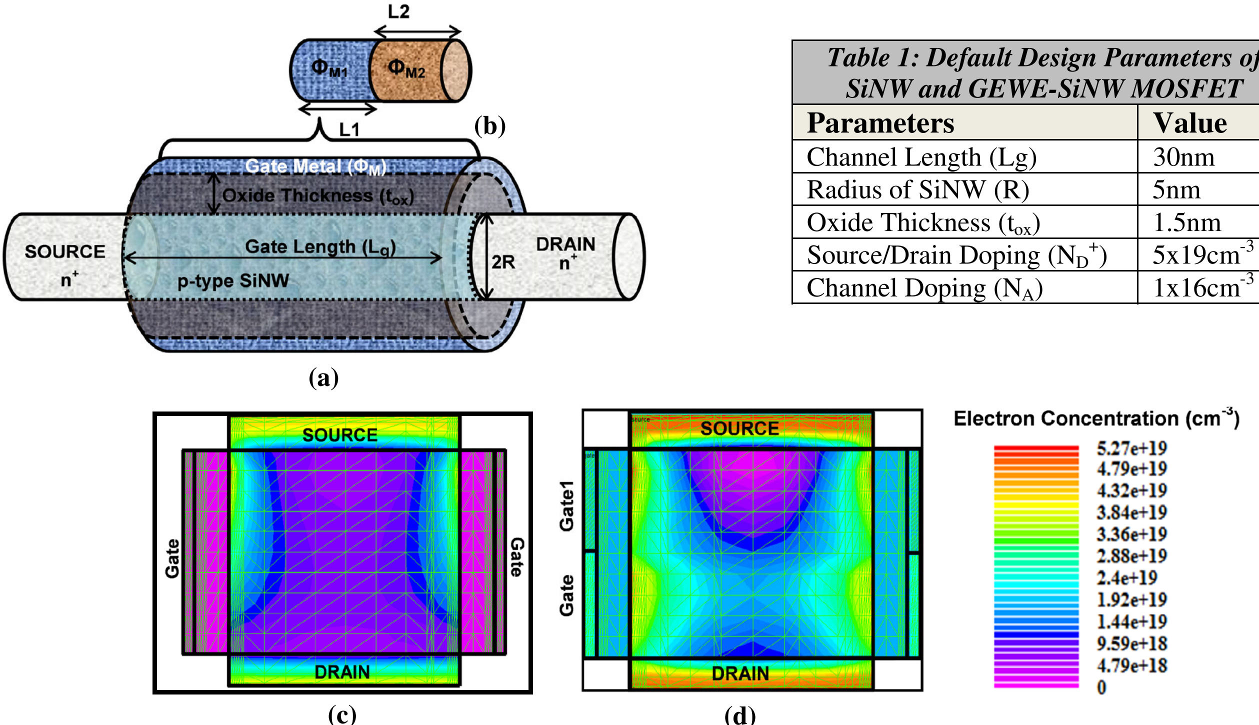

Table 1: Default Design Parameters of SiNW and GEWE-SiNW MOSFET

Parameters	Value
Channel Length (Lg)	30nm
Radius of SiNW (R)	5nm
Oxide Thickness (t_{ox})	1.5nm
Source/Drain Doping (N_D^+)	5x19cm^{-3}
Channel Doping (N_A)	1x16cm^{-3}

Fig. 1 3D device structure of **a** SiNW MOSFET and **b** GEWE-SiNW MOSFET, **c**, **d** two-dimensional (2D) cross-sectional contour plots of the electron concentration in the SiNW

where M^{-1} is the inverse of the effective mass tensor and $M^{-1}\nabla S$ is the local velocity of the particle associated with the wave function. The real part of Eq. 2 is interpreted as the continuity equation of the probability density, while the imaginary part states that the total energy E is conserved and equal to the sum of the potential (Q) and kinetic energy ($0.5\, M^{-1}\nabla S$). Thus, the quantum potential is defined as

$$Q = \frac{-\hbar^2}{2}\frac{\nabla\left(M^{-1}\nabla R\right)}{R}. \tag{3}$$

The potential Q is obtained from the single-particle Schrödinger equation using the mean-field approximation and considering an effective quantum Bohm potential defined as the weighted average potential for all carriers constrained in the confining potential. Therefore, the effective quantum potential can be written as

$$Q_{\text{eff}} = \frac{-\hbar^2}{2}\gamma\nabla\frac{\left[M^{-1}\nabla\left(n^{\alpha}\right)\right]}{n^{\alpha}}, \tag{4}$$

where α and γ are two adjustable parameters, M^{-1} is the inverse effective mass tensor, n is the electron (or hole) density, and h is Planck's constant.

Additionally, numerical techniques such as the biconjugate gradient stabilized (BICGST) method were considered to obtain solutions with improved convergence for the 3D device structures [23]. Default simulator coefficients were employed for all parameters. To calibrate the BQP model, the two adjustable parameters were tuned to $\alpha = 0.5$ and $\gamma = 1.2$ to obtain the best fit with experimental data. Calibration of the model parameters used in the simulation was performed according to the experimental results [26] using the above-mentioned models. Figure 2 shows the simulated I_d–V_{gs} characteristic of the 30-nm cylindrical gate SiNW MOSFET at $V_{ds} = 1.0$ V and the transfer characteristic of extracted data from [26]. The results are in close proximity, thus validating the choice of model parameters used in the simulation.

2.1 Fabrication feasibility

The fabrication feasibility of the SiNW MOSFET has been reported in literature using several integration schemes. Yang et al. [27] fabricated a vertical gate-all-around silicon nanowire MOSFET. Rustagi et al. [28] reported fabrication of CMOS inverter-based GAA SiNW MOSFETs using a top-down approach. Moreover, to realize the GEWE architecture, numerous schemes have been suggested, such as tilt angle evaporation metal gate deposition [17], a metal interdiffusion process [29], and the fully silicide (FUSI) metal gate technique [30]. Furthermore, CMOS with dual metal gate has also been successfully fabricated with poly-Si gate doping control of the source and drain side gate individually [31]. Thus, the

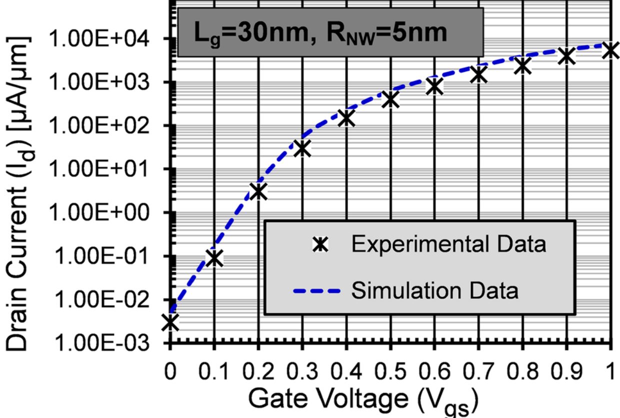

Fig. 2 Calibration with published result: I_{ds}–V_{gs} characteristic of the silicon nanowire MOSFET at $V_{ds} = 1.0$ V [26]

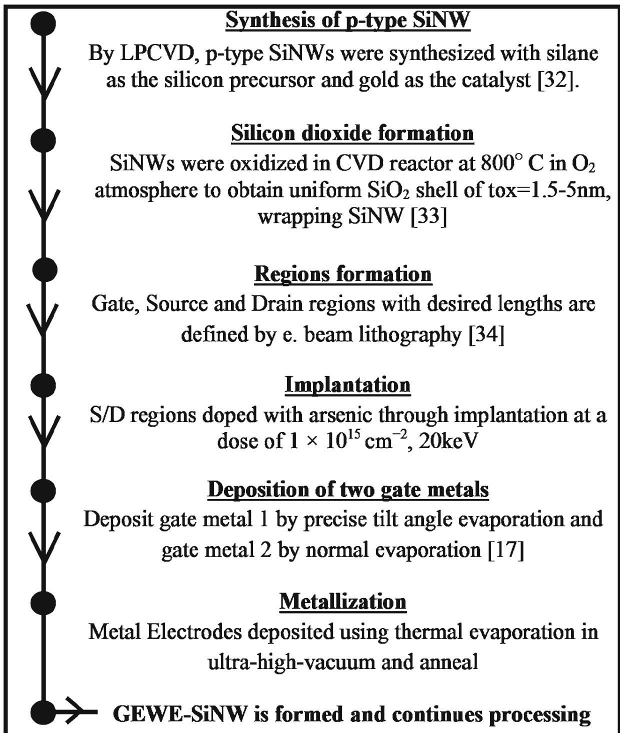

Fig. 3 Summary of typical process flow of a GEWE-SiNW MOSFET [17,32–34]

proposed device (GEWE-SiNW MOSFET) can be fabricated using the above design schemes, in which the advantages of the GEWE scheme are combined with the SiNW MOSFET structure, yielding a promising design for system-on-chip and RF/microwave applications. A proposed summary of the process flow, outlining the fabrication method of the GEWE-SiNW MOSFET and its integration with the standard CMOS process, is shown in Fig. 3.

3 Results and discussion

3.1 Extrinsic parameters

When a MOSFET is operated at low frequency, the extrinsic parameters behave as virtual components in the I–V expression to account for the direct-current (DC) voltage drop across these resistances, an effect obscured for high-frequency signals. Therefore, external mechanisms for these components must be included beyond the intrinsic model to precisely describe high-frequency device behavior [35]. Furthermore, the extrinsic network plays a significant role in determining the scaling rules for the complete transistor model. The extrinsic network has to describe the electrical behavior of the device layout, and the way in which this layout changes with device size determines how the extrinsic network component values scale. However, detailed knowledge of the extrinsic parameters is also essential for precise modeling of RF transistors, so that the extrinsic components can be de-embedded accurately to gain access to the intrinsic behavior of the transistor. To extract the extrinsic parameters, the MOSFET is biased at zero gate and drain bias, which is known as the zero-cold FET condition [36,37]. The process of extracting the parameters is described in Fig. 4a. C_{gdo} and C_{gso} are the extrinsic gate-to-drain and gate-to-source capacitance, respectively. R_{SO} and R_{DO} are the source and drain extrinsic resistance, respectively. L_{SO}, L_{DO}, and L_{GO} are the source, drain, and gate extrinsic inductance, respectively, as shown in the equivalent circuit in Fig. 4b.

In this subsection, the extrinsic parameters of the GEWE-SiNW MOSFET are examined as functions of frequency, then compared with conventional devices having identical geometry. As is evident from Fig. 5a, with increase in the frequency, all parasitic resistances due to the gate, source, and drain remain almost constant. Moreover, in the SiNW, their effects are comparatively smaller compared with in the conventional MOSFET, and with incorporation of the GEWE scheme, the resistance effect reduces appreciably. Similarly, both extrinsic capacitances and inductances also reduce in our proposed device compared with the SiNW and conventional MOSFET, as shown in Fig. 5b, c.

3.2 Intrinsic parameters

Direct techniques for extracting intrinsic small-signal parameters were performed after de-embedding the effect of extrinsic parameters such as C_{gdo}, C_{gso}, R_{SO}, R_{DO}, L_{SO}, and L_{DO}. Figure 6 shows the non-quasi-static equivalent circuit of the MOSFET used to extract the intrinsic parameters of the GEWE-SiNW, conventional silicon nanowire, and conventional MOSFET, which is based on conventional MOSFET small-signal microwave modeling [38]. Here, R_{GS} and R_{GD} represent the distributed channel resistance, and C_{DS} and

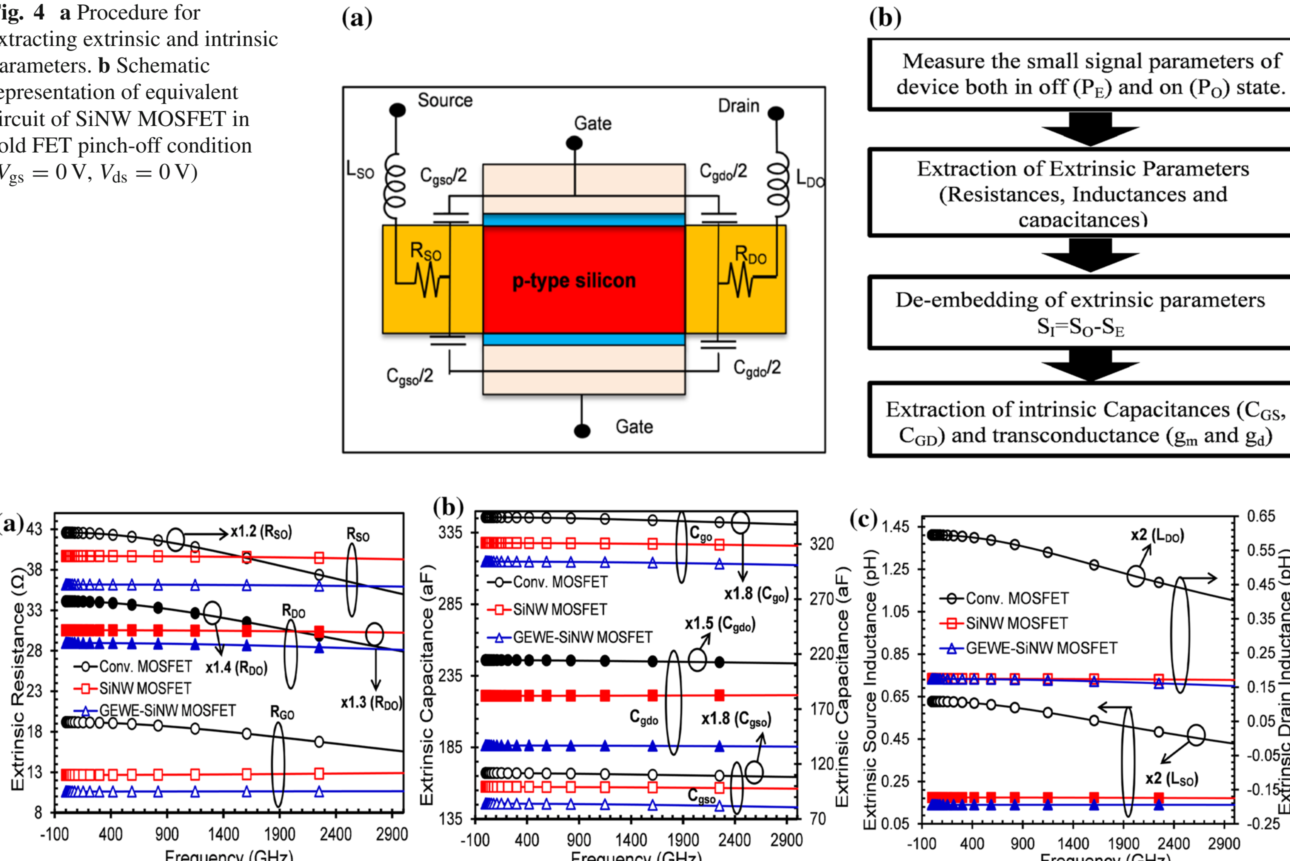

Fig. 4 **a** Procedure for extracting extrinsic and intrinsic parameters. **b** Schematic representation of equivalent circuit of SiNW MOSFET in cold FET pinch-off condition ($V_{gs} = 0\,V$, $V_{ds} = 0\,V$)

Fig. 5 **a** Extrinsic resistance, **b** capacitance, and **c** inductance as functions of frequency for the conventional, SiNW, and GEWE-SiNW MOSFET

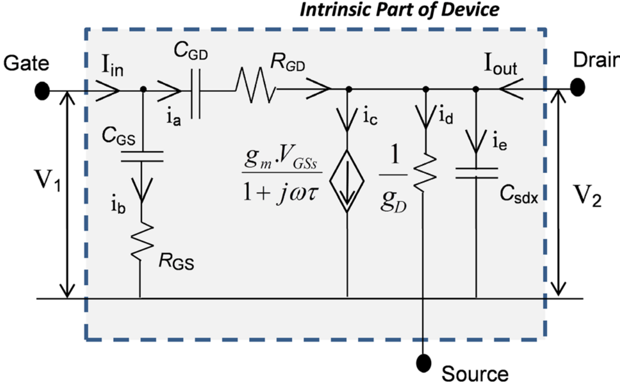

Fig. 6 Non-quasi-static (NQS) equivalent circuit model of the SiNW MOSFET in RF regime operating in strong inversion region

C_{GS} are the intrinsic gate-to-drain and gate-to-source capacitance, respectively. g_D and g_m are the intrinsic drain and gate transconductance, respectively.

Figure 7a illustrates the bias dependence of the small-signal parameters in terms of the gate and drain transconductance of the GEWE-SiNW and conventional SiNW MOSFET at gate and drain bias, respectively. As is evident from Fig. 7a, there is a significant increment in g_m with an increase in V_{gs}, compared with the SiNW MOSFET. This is due to the enhanced current driving capability of the GEWE-SiNW MOSFET compared with the conventional SiNW MOSFET, thereby improving the gain of the device. Furthermore, g_D decreases with increase in V_{ds}, but its value is comparatively higher in the case of the GEWE-SiNW MOSFET, since g_D is inversely related to the output resistance. It is evident that, when the device is in the active region ($V_d = 0$–$0.3\,V$), g_D decreases rapidly, indicating that the output resistance decreases with enhancement of the on-current; while in the saturation region ($V_d = 0.4$–$1.0\,V$), g_D becomes almost constant, which results in saturation of the drain current, as shown in Fig. 7a. Parasitic capacitances such as C_{GS}, C_{GD}, and C_{GG} in RF amplifiers degrade the performance in terms of low gain and, in some cases, may cause such amplifiers to oscillate. In digital logic circuits, the rise and fall times of the digital signal greatly influence the maximum achievable device speed [39]. Thus, it is necessary to examine the effect of parasitic capacitances at HF. The capacitances of the SiNW MOSFET turned out to be smaller than those of the conventional MOSFET, as shown in Fig. 7b. On incorporation of the GEWE scheme into the SiNW MOSFET, the parasitic capacitances decrease further with increase in fre-

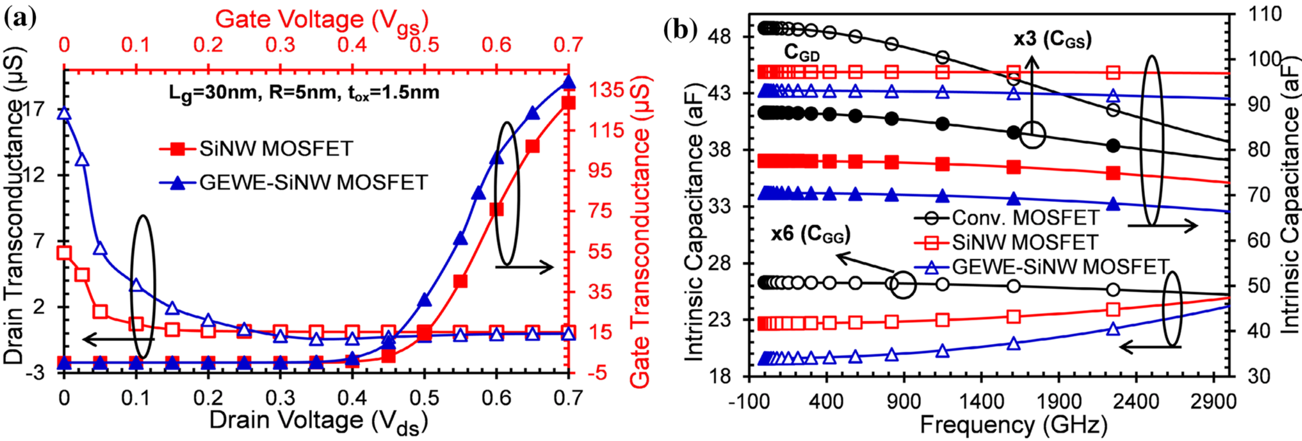

Fig. 7 **a** Intrinsic gate and drain transconductance of a conventional, SiNW, and GEWE-SiNW MOSFET as functions of bias voltage, **b** intrinsic capacitance as function of frequency for conventional, SiNW, and GEWE-SiNW MOSFET

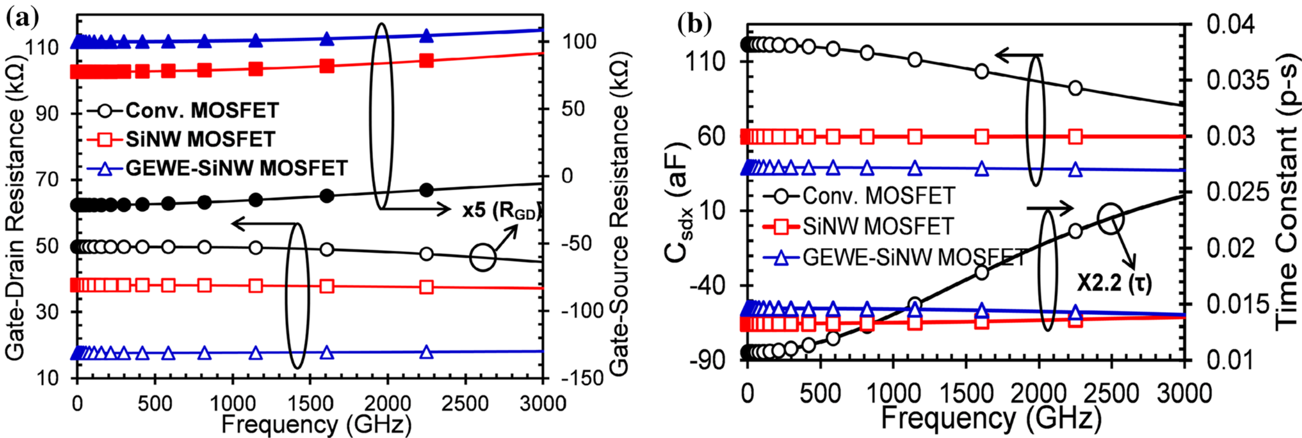

Fig. 8 **a** Intrinsic gate-to-drain and gate-to-source resistances of conventional, SiNW, and GEWE-SiNW MOSFET as functions of frequency, **b** C_{sdx} and time constant of a conventional, SiNW, and GEWE-SiNW MOSFET as functions of frequency

quency. This is due to improved screening of the channel region from drain-bias variations. Hence, lower values of the intrinsic parasitic capacitances mean lower intrinsic delay, which is suitable for switching applications such as in logic gates. At low frequency, the gate of the MOSFET is treated as purely capacitive. However, this assumption fails when the frequency exceeds the GHz range [40]. Also, the distributed gate resistance plays a major role in evaluating the noise figure and power gain of the transistor. Figure 8a exhibits the distributed channel resistances, i.e., R_{GD} and R_{GS}, for the GEWE-SiNW, SiNW, and conventional MOSFET as functions of frequency. R_{GD} for the GEWE-SiNW MOSFET is much smaller than for its conventional counterparts, resulting in the maximum power gain and maximum oscillation frequency.

Also, in highly scaled MOSFETs, the unexpected change of the inversion channel charge is due to the DIBL effect. Since the source and drain capacitance of the transistor are determined by the inversion channel charge, the value of C_{SD} is affected by DIBL [41]. To study the effect of DIBL on C_{SD} in detail, one can use C_{sdx} as an additional component reflecting the charge variation due to DIBL in short-channel MOSFETs [15]. Figure 8b shows the variation of C_{sdx} as a function of frequency. The effect of DIBL is highly pronounced in the conventional MOSFET at HF compared with the SiNW MOSFET. With incorporation of the GEWE, SCEs such as hot-carrier effects and DIBL are reduced, as reported in literature [18]. It is clearly shown that the DIBL effect is reduced in the GEWE-SiNW MOSFET due to the reduced C_{sdx} owing to a decline in the electric field at the drain end because of the lower metal workfunction. Figure 7b shows the time constant of the conventional, SiNW, and GEWE-SiNW MOSFET as a function of frequency. The time constants for charging delay are obtained as $R_{GS}C_{GS}$ and $R_{GD}C_{GD}$, and the charging delay is affected by the transport delay τ [38]. It is evident from Fig. 7b that τ for the SiNW MOSFET is greater than for the conventional MOSFET due to the higher inversion channel charge owing to its cylindrical geometry.

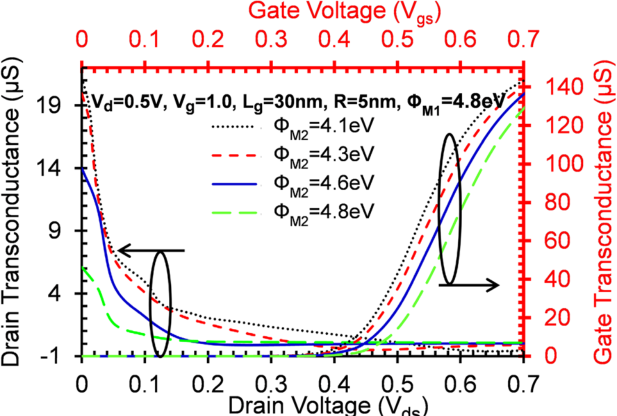

Fig. 9 Intrinsic gate and drain transconductance of the GEWE-SiNW for different metal workfunctions

On incorporation of two dissimilar metal gates, the time constant increases. Therefore, the distributed channel resistance R_{GS} of the GEWE-SiNW MOSFET is higher than that of the conventional device.

3.2.1 *Effect of gate metal workfunction engineering*

In this subsection, the effect of metal gate engineering on the intrinsic parameters of the GEWE-SiNW MOSFET is investigated by keeping the workfunction at the source side constant (4.8 eV) while varying the workfunction of the metal gate at the drain end. Figure 9 shows the variation of the bias-dependent gate and drain transconductance for different workfunctions at the drain end. With increase in the workfunction difference, the gate transconductance (g_m) increases due to improved carrier transport efficiency and enhanced current driving capability, hence delivering higher gain. The drain transconductance (g_d) decreases with increase in the drain bias, an effect that becomes more pronounced as the workfunction difference increases, as shown in Fig. 9.

Moreover, with increase in the workfunction difference, there is a prominent reduction in C_{GS} and C_{GD} with increase in frequency, as observed in Fig. 10a, b, due to enhanced screening of the potential from bias variations, thus reducing the turn-on delay time. Similarly, with increase in the workfunction difference, the distributed R_{GD} decreases and R_{GS} increases, and these gate resistances are independent of frequency, as shown in Fig. 11a. It is evident from Fig. 11b that, by decreasing the workfunction of the metal gate at the drain end, the effect of C_{sdx} reduces in the GHz frequency regime, directly indicating that a higher workfunction difference leads to immunity against DIBL and hence SCEs. Furthermore, the time constant is also enhanced by 32 % with an increase in the workfunction difference, as shown in Fig. 11b, due to the enhancement in the on-current and carrier mobility.

3.2.2 *Bias-dependent intrinsic parameters*

In the previous section, the intrinsic parameters of the GEWE-SiNW MOSFET were evaluated as functions of frequency; the results showed that these parameters are almost constant with frequency in the GHz range. In this section, the effect of bias variation on the intrinsic parasitic capacitance, transconductance, distributed gate capacitance, and time constant is investigated. The MOSFET gate transconductance ($g_m = \partial I_{DS}/\partial V_{GS}$) is defined in the linear regime and used as an indirect monitor of the inversion charge carrier mobility. The transconductance is an important parameter needed for designing high-frequency amplifiers. As is evident from Fig. 12a, g_m increases remarkably as the drain voltage is increased from 0.1 to 0.5 V. Figure 12a also indicates the dependence of the drain transconductance on the drain voltage for different gate voltages. As the drain voltage is increased, the transconductance increases and then reduces to zero in the saturation region. The rate of decrease of the

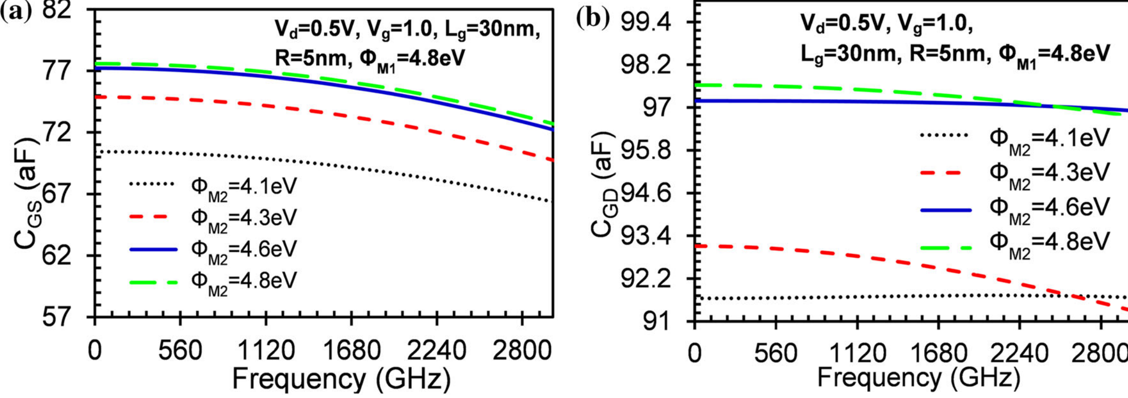

Fig. 10 Intrinsic capacitance of the GEWE-SiNW MOSFET as function of frequency for different gate metal workfunctions

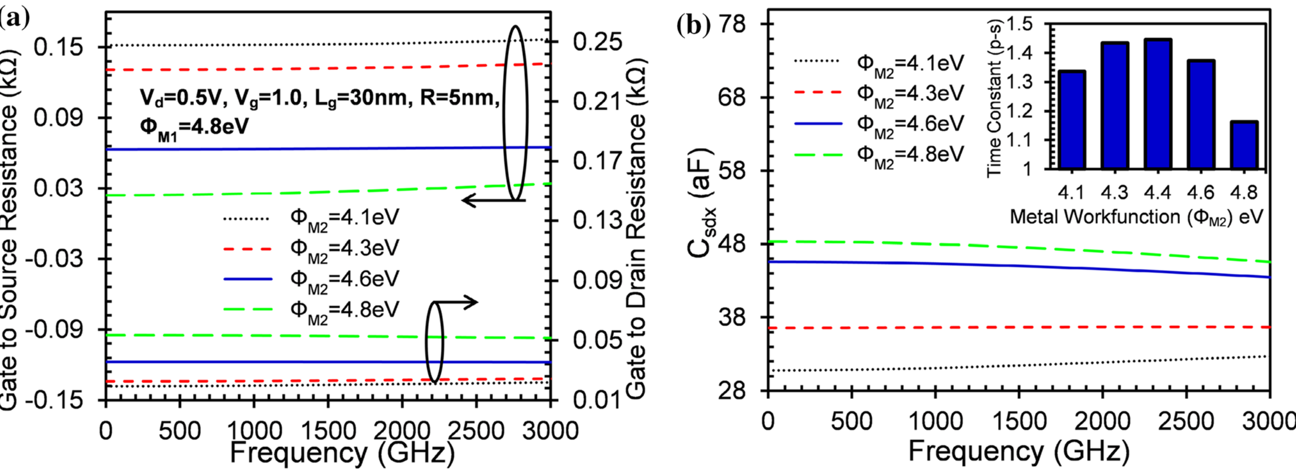

Fig. 11 **a** Intrinsic gate-to-drain and gate-to-source resistance of the GEWE-SiNW MOSFET for different metal workfunctions, **b** C_{sdx} and time constant of the GEWE-SiNW MOSFET for different metal workfunctions

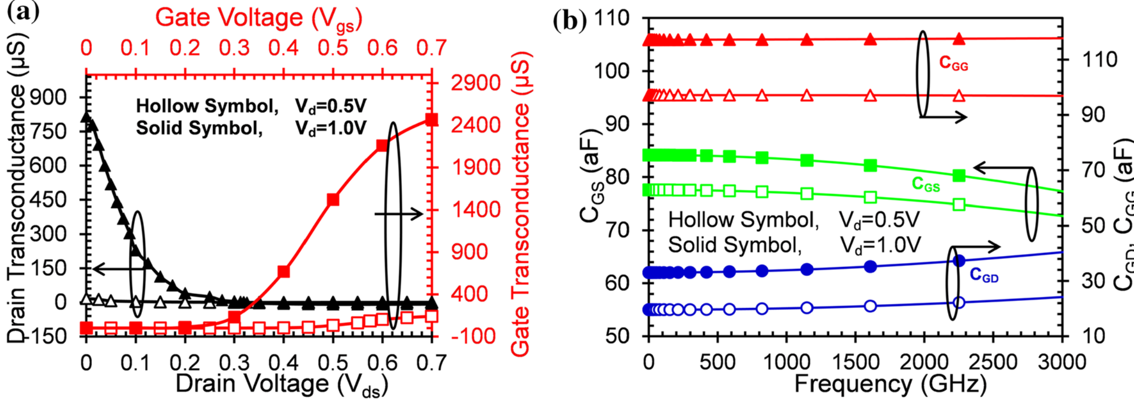

Fig. 12 **a** Intrinsic gate and drain transconductance of the GEWE-SiNW MOSFET for different bias values, **b** intrinsic bias-dependent parasitic capacitance of the GEWE-SiNW MOSFET

drain transconductance with the drain voltage is greater than that with the gate voltage.

The effect of the drain bias on the parasitic capacitance is shown in Fig. 12b. It is evident from this figure that, with increase in the drain bias, all the parasitic capacitances increase due to the shift of the pinch-off point towards the source side, which leads to accumulation of charge carriers, resulting in an increment in C_{GS}. To maintain charge neutrality, charges near the drain decrease, hence C_{GD} decreases, as shown in Fig. 12b. Figure 13a indicates the variation of C_{sdx} as a function of frequency for different drain bias values. It is evident that, with increase in the drain bias, the DIBL effect is reduced, as reflected in C_{sdx}. This reduction is due to the improved gate controllability of the GEWE-SiNW MOSFET over the channel due to the cylindrical gate and step in the conduction-band energy profile in the channel region, which itself is a result of the metal gate workfunction difference. Also, both distributed gate resistances (R_{GS} and R_{H}) decrease as the device moves from the linear to saturation region, as is evident from Fig. 13a. Moreover, the time constant of the GEWE-SiNW MOSFET degrades with increase in the drain bias due to enhancement of the inversion charge carriers, as shown in Fig. 13b.

3.3 Small-signal model parameters: *Z* and *Y*

The small-signal behavior of a MOSFET is generally expressed in terms of the impedance (Z parameters) and admittance (Y parameters), being commonly employed for networks that operate at RF/microwave frequencies. Based on knowledge of the parasitic parameters, the intrinsic Z parameters can be determined in a similar way as the intrinsic parameters are extracted. The choice of the parameter used is generally determined by suitability or usage; e.g., if shunt feedback is applied in RF amplifiers, Y parameters are most convenient, whereas Z parameters are recommended for series feedback. After de-embedding the extrinsic parameters, the intrinsic Z and Y parameters were evaluated by solving the small-signal equivalent model as shown in Fig. 6.

The total current flowing at the input port (gate) is $i_{\mathrm{a}} + i_{\mathrm{b}}$.

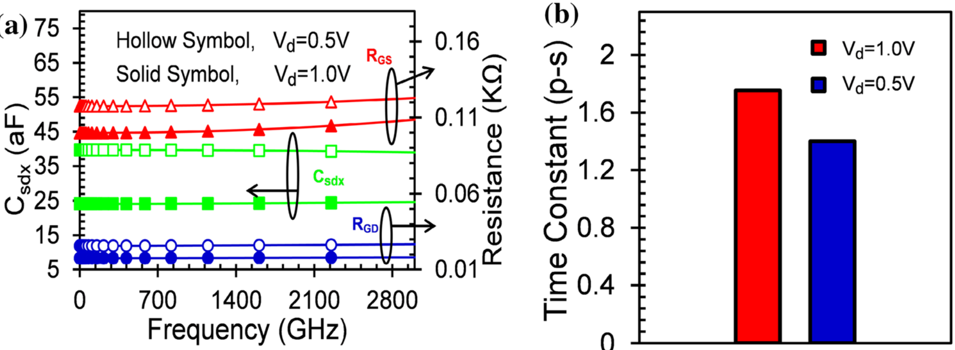

Fig. 13 C_{sdx}, distributed gate resistance, and time constant of the GEWE-SiNW MOSFET for different drain bias values

The total current flowing at the output port (drain) is $i_c + i_d + i_e - i_b$.

Applying nodal analysis,

$$\frac{V_1}{X_1} + \frac{V_1 - V_2}{X_2} = 0 \quad \text{[at input node]}, \tag{5}$$

$$\frac{V_2}{X_3} + \frac{V_2 - V_1}{X_2} + \frac{g_m V_{gs}}{1 + j\omega\tau} = 0 \quad \text{[at output node]}, \tag{6}$$

where $X_1 = \frac{1+j\omega R_{GS}C_{GS}}{j\omega C_{GS}}$, $X_2 = \frac{1+j\omega R_{DS}C_{DS}}{j\omega C_{DS}}$, and $X_3 = \frac{1}{g_D + j\omega C_{sdx}}$.

Solving Eqs. 1 and 2 using the approximations $\omega^2 R_{GS}^2 C_{GS}^2 \ll 1$, $\omega^2 R_{GD}^2 C_{GD}^2 \ll 1$, and $\omega^2\tau^2 \ll 1$ yields

1. The driving-point short-circuit input admittance

$$Y_{11} \cong \omega^2(a_1 + a_2) + j\omega(C_{GS} + C_{GD}) \tag{7}$$

2. The driving-point short-circuit output admittance

$$Y_{22} \cong g_D + \omega^2 a_2 + j\omega(C_{GD} + C_{sdx}) \tag{8}$$

3. The reverse transfer admittance

$$Y_{12} \cong -\omega^2 a_2 - j\omega C_{GD} \tag{9}$$

4. The forward transfer admittance

$$Y_{21} \cong -\omega^2 a_2 - j\omega C_{GD} + g_m(1 + \tau) \tag{10}$$

Similarly, the Z parameters can be evaluated from the Y parameters as follows:

1. The driving-point input impedance

$$Z_{11} \cong \frac{g_D + \omega^2 a_2 + j\omega(C_{GD} + C_{sdx})}{\xi} \tag{11}$$

2. The open-circuit reverse transfer impedance

$$Z_{12} \cong \frac{\omega a_2 + j\omega C_{GD}}{\xi} \tag{12}$$

3. The open-circuit forward transfer impedance

$$Z_{21} \cong \frac{\omega^2 a_2 + j\omega C_{GD} - g_m(1 + \tau)}{\xi} \tag{13}$$

4. The driving-point output impedance

$$Z_{22} \cong \frac{\omega^2(a_1 + a_2) + j\omega(C_{GS} + C_{GD})}{\xi} \tag{14}$$

where $\xi = [j\omega(C_{GS}g_D + C_{GD}g_D + C_{GD}g_m + \tau C_{GD}g_m) + \omega^2(a_1 g_D + a_2 g_D - C_{GS}C_{sdx} - C_{GD}C_{sdx} + a_2 g_m(1 + \tau) + C_{GD}^2) + j\omega^3(a_1 C_{GD} + a_2 C_{GS} + C_{sdx}(a_1 + a_2)) + a_1 a_2 \omega^4]$.

$$a_1 = R_{GS}C_{GS}^2, \quad a_2 = R_{GD}C_{GD}^2.$$

Z_{11} and Z_{22} are essentially used for impedance matching in high-frequency applications. For impedance matching, the input impedance should be equal to the output impedance, which is necessary for maximum power transfer from source to load. Figure 14a, b shows the variation of the real component of the input and output impedance of the conventional, SiNW, and GEWE-SiNW MOSFET as functions of frequency. It is clearly shown that the input impedance of the GEWE-SiNW device is higher than that of its conventional counterparts owing to the cylindrical geometry and GEWE scheme. Furthermore, when tuning the metal workfunction at the drain end, both the input and output impedance improve as the frequency increases in the GHz range, as shown in Fig. 14c, d. For RF amplifiers, ideally Z_{12} should be as high as possible so that maximum impedance can transfer from input to output. It is clear from these results that Z_{12} for the SiNW MOSFET is greater than for the conventional MOSFET due to the reduced SCEs and maximum volume inversion, and with the incorporation of GEWE engineering into the SiNW device, Z_{12} improves, as shown in Fig. 14d. Furthermore, with increasing gate workfunction difference in the GEWE-SiNW device, Z_{12} is enhanced due to the enhancement in

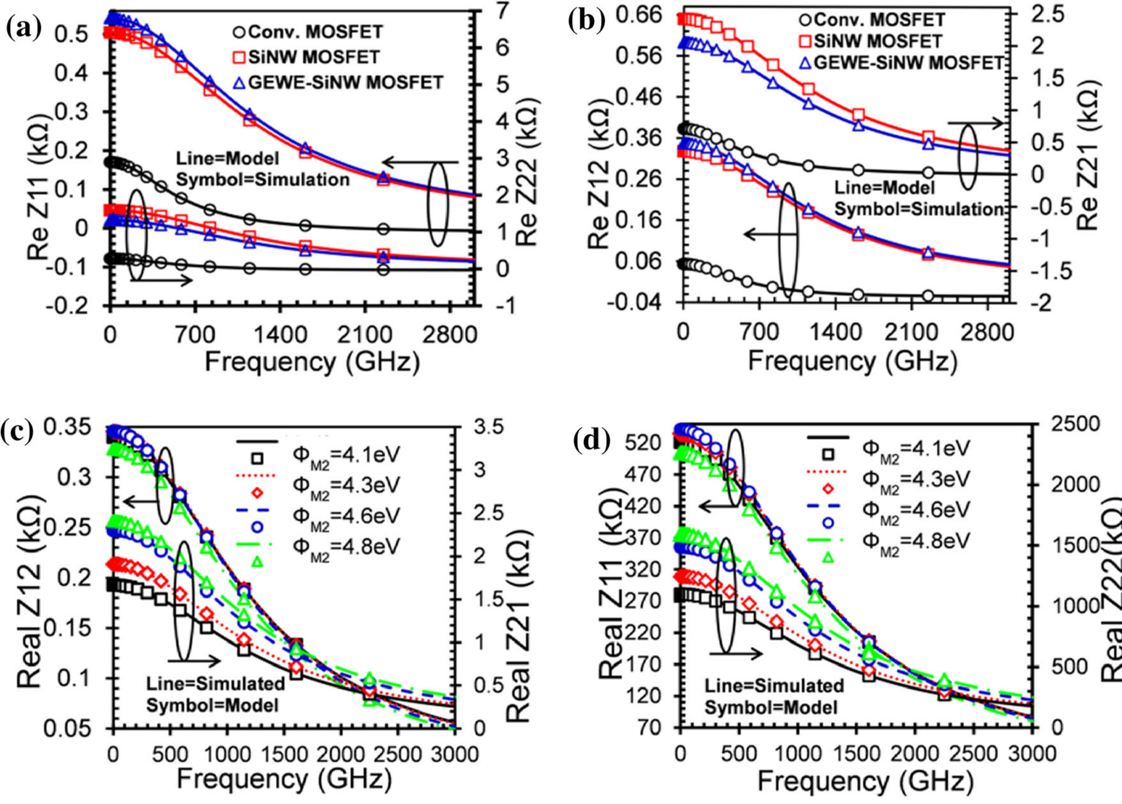

Fig. 14 **a**, **b** *Z* parameters of conventional, SiNW, and GEWE-SiNW MOSFET; **c**, **d** *Y* parameters of GEWE-SiNW MOSFET for different gate metal workfunctions

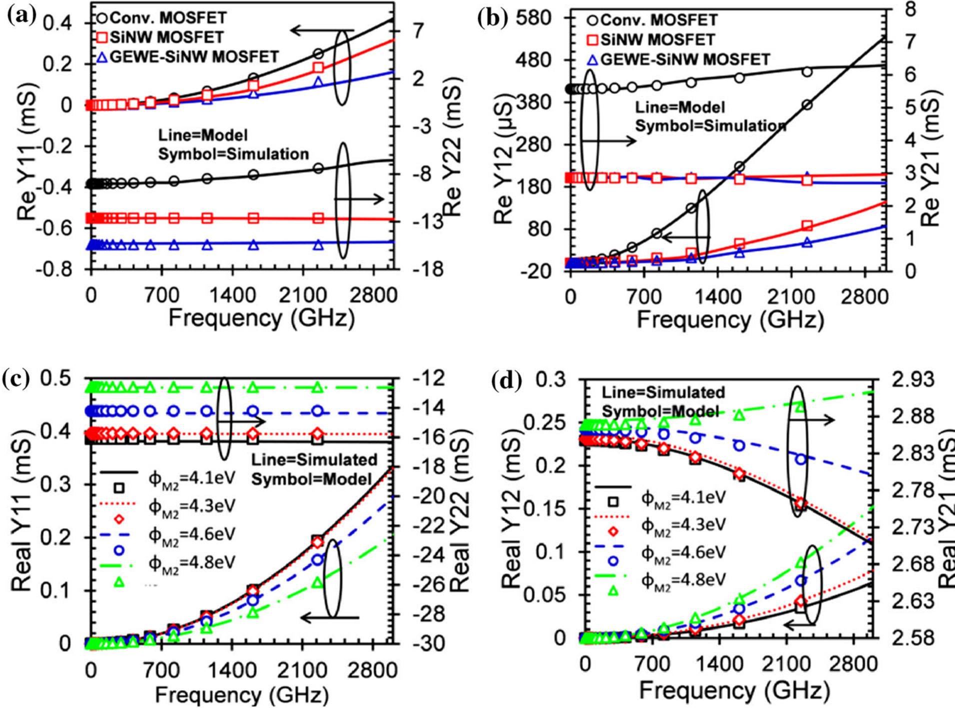

Fig. 15 **a**, **b** *Y* parameters of conventional, SiNW, and GEWE-SiNW MOSFET; **c**, **d** *Y* parameters of GEWE-SiNW MOSFET for different gate metal workfunctions

the carrier mobility and hence transport efficiency, as is evident from Fig. 14d. At low frequency, alternating-current (AC) voltages and currents can be easily measured, but at HF, measurement of these parameters becomes exceptionally complicated. Another set of parameters, i.e., the *S* parameters, can be measured at high frequency.

Table 2 Extracted parameters for all three devices for the linear and saturation regions

Parameter	Device					
	Conventional MOSFET		SiNW MOSFET		GEWE-SiNW MOSFET	
	$V_d = 0.5\,V$	$V_d = 1.0\,V$	$V_d = 0.5\,V$	$V_d = 1.0\,V$	$V_d = 0.5\,V$	$V_d = 1.0\,V$
C_{cs} (aF)	251.5	287.87	76.2	81.32	69.25	82.189
C_{GD} (aF)	310.4	340.87	97.2	103.34	92.54	117.44
R_{GS} (kΩ)	14.88	12.34	81.8	79.34	118.9	102.19
R_{GD} (kΩ)	244.65	220.98	37.8	31.98	26.1	17.82
g_m (μS)	50	65.96	128	200.98	139.3	2470
g_D (μS)	0.1	1.02	0 711	7.47	3.70	228.3
τ (ps)	0.431	0.65	1.161	1.4	1.39	1.89
C_{sdx} (aF)	309	289.34	59.829	52.56	38.57	24.31
R_{SO} (Ω)	46.8	46.8	39.585	39.585	36 11	36.11
R_{DO} (Ω)	44.14	44.14	39.585	39.585	28.68	28.68
L_{SO} (pH)	1.07	1.07	0.1725	0.1725	0.1399	0.1399
L_{DO} (pH)	1.014	1.014	0.1735	0.1735	0.167	0.167
C_{GSO} (aF)	298	298	157	157	144	144
C_{GDO} (aF)	319	319	182	182	136	136

Table 3 Extracted parameters for the GEWE-SiNW MOSFET for different metal workfunctions (Φ_{M2})

Parameter	Workfunction (Φ_{M2}) GEWE-SiNW MOSFET ($\Phi_{MI} = 4.8\,eV$, $V_d = 0.5\,V$, $V_g = 1.0\,V$)			
	4.1	4.3	4.6	4.8
C_{GS} (aF)	69.25	73.4	75.80	76.2
C_{GD} (aF)	91.7	92.81	97.14	97.6
R_{GS} (kΩ)	152	132.2	63.87	27.38
R_{GS} (kΩ)	20.5	23.16	35.53	52.78
g_m (μS)	143.7	140	136	128
g_D (μS)	4.92	4.07	2.146	0.711
τ (ps)	1.54	1.478	1.378	1.161
C_{sdx} (aF)	31.53	36.72	44.93	46.67

However, as the Y parameters are more closely related to the device physics and design, the S parameters are converted to Y parameters. Hence, study of the Y parameters becomes necessary. Figure 15a shows that the real component of the input admittance of the GEWE-SiNW MOSFET is comparatively lower than for its conventional counterparts, and its value gradually increases with increase in frequency. Similarly, Y_{22} is higher for the GEWE-SiNW device compared with the SiNW or conventional MOSFET, indicating that the current driving capability of the GEWE-SiNW MOSFET is enhanced due to the metal workfunction engineering, which further enhances the carrier velocity and hence on-current, as shown in Fig. 15a. The Y_{12} and Y_{21} values for the GEWE-SiNW MOSFET are lower and higher, respectively, as shown in Fig. 15b. Y_{21} is defined as the forward transconductance of the device; ideally, its value should be as high as possible to achieve high-gain RF amplifiers.

Also, for a workfunction difference of 0.7 eV, the small-signal performance of the device in terms of the real component of Y_{11}, Y_{12}, Y_{21}, and Y_{22} improves, as shown in Fig. 15c, d, owing to the greater enhancement in the transconductance. The modeled Z and Y parameters (lines) generated using the non-quasi-static (NQS) model and the parameters extracted from the 3D simulations (symbols) demonstrate excellent agreement. Thus, the proposed model is highly reliable for RF/millimeter-wave applications and hence suitable for providing information to RF engineers. All the parameters extracted in the linear ($V_d = 0.5\,V$) and saturation ($V_d = 1.0\,V$) regions are summarized in Table 2. Also, the effect of the metal workfunction engineering on all the parameters is summarized in Table 3.

4 Conclusions

Both the extrinsic and intrinsic parameters of the GEWE-SiNW MOSFET were directly extracted based on quantum simulations and compared with those of the SiNW and

conventional MOSFET in the GHz range to analyze their use in RF applications. The simulation results demonstrate a noticeable reduction in parasitic resistance, inductance, and capacitance for the GEWE-SiNW MOSFET compared with its conventional counterparts. Also, the reduction in the intrinsic C_{sdx} implies that the DIBL effect is less pronounced in the proposed device at HF. Moreover, by tuning the workfunction difference, the effect of parasitics, which hinder device performance at RF, can be decreased. Also, the admittance and impedance parameters are improved with incorporation of the GEWE scheme, due to reduced SCEs and maximum volume inversion owing to the cylindrical gate, thus providing necessary information to RF engineers for microwave communications. The modeling results match well with the Z and Y parameters extracted from 3D device simulations.

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References

1. Deen, M.J., Fjeldly, T.A.: CMOS RF Modeling. Characterization and Applications. World Scientific, Singapore (2002)
2. Wood, J., Lamey, D., Guyonnet, M., Chan, D., Bridges, D., Monsauret, N., Aaen, P.H.: An extrinsic component parameter extraction method for high power RF LDMOS transistors. In: IEEE MTT-S International Microwave Symposium Digest, pp. 607–610 (2008)
3. Ytterdal, T., Cheng, Y., Fjeldly, T.A.: Device Modeling for Analog and RF CMOS Circuit Design. Wiley, New York (2000)
4. Cheng, Y., Deen, M.J., Chen, C.-H.: MOSFET modeling for RF IC design. IEEE Trans. Electron Devices **52**(7), 1286–1303 (2005)
5. Woerlee, P.H., et al.: RF-CMOS performance trends. IEEE Trans. Electron Devices **48**(8), 1776–1782 (2001)
6. Alam, M.S., Armstrong, G.A.: Extraction of extrinsic series resistance in RF CMOS. In: NSTI-Nanotech, pp. 136–139 (2004)
7. Buss, D.: Device issue in the integration of analog/RF functions in deep sub-micron digital CMOS. In: IEDM Technology Digest, pp. 423–426 (1999)
8. Kumar, A., Gupta, N., Chaujar, R.: Power gain assessment of ITO based transparent gate recessed channel (TGRC) MOSFET for RF/wireless applications. Superlattices Microstruct. **91**, 290–301 (2016)
9. Kumar, A., Gupta, N., Chaujar, R.: TCAD RF performance investigation of transparent gate recessed channel MOSFET. Microelectron. J. **49**, 36–42 (2016)
10. Subramanian, V., Abdelkarim, M., Bertrand, P., Morin, D., Guido, G., Willy, S., Stefaan, D.: Identifying the bottlenecks to the RF performance of FinFETs. In: IEEE 23rd International Conference on VLSI Design, pp. 111–116 (2010)
11. Cui, Y., Zhong, Z., Wang, D., Wang, W.U., Lieber, C.M.: High performance silicon nanowire field effect transistors. Nano Lett. **3**(2), 149–152 (2003)
12. Chen, X., Tan, C.M.: Modeling and analysis of gate-all-around silicon nanowire FET. Microelectron. Reliab. **54**(6–7), 1103–1108 (2014)
13. Iwai, H., et al.: Si nanowire FET and its modeling. Sci. China Inf. Sci. **54**(5), 1004–1011 (2011)
14. Wang, R., Zhuge, J., Huang, R., Tian, Y., Xiao, H., Zhang, L., Li, C., Zhang, X., Wang, Y.: Analog/RF performance of Si nanowire MOSFETs and the impact of process variation. IEEE Trans. Electron Devices **54**(6), 1288–1294 (2007)
15. Cho, S., Kang, I.M., Kim, K.R.: Investigation of source-to-drain capacitance by DIBL effect of silicon nanowire MOSFETs. IEICE Electron. Express **7**(19), 1499–1503 (2010)
16. Cho, S., Kim, K.R., Park, B.G., Kang, I.M.: RF Performance and small-signal parameter extraction of junctionless silicon nanowire MOSFETs. IEEE Trans. Electron Devices **58**(5), 1388–1396 (2011)
17. Long, W., Ou, H., Kuo, J.M., Chin, K.K.: Dual material gate (DMG) field effect transistor. IEEE Trans. Electron Devices **46**(5), 865–870 (1999)
18. Gupta, N., Chaujar, R.: Implications of transport models on the analog performance of gate electrode workfunction engineered (GEWE) SiNW MOSFET. In: IEEE 2nd International Conference on Devices, Circuits and Systems, pp. 1–5 (2014)
19. Gupta, N., Kumar, A., Chaujar, R.: Oxide bound impact on hot-carrier degradation for gate electrode workfunction engineered (GEWE) silicon nanowire MOSFET. Microsyst. Technol. **22**(11), 2655–2664 (2015)
20. Gupta, N., Kumar, A., Chaujar, R.: Impact of device parameter variation on RF performance of gate electrode workfunction engineered (GEWE)-silicon nanowire (SiNW) MOSFET. J. Comput. Electron. **14**(3), 798–810 (2015)
21. Gupta, N., Kumar, A., Chaujar, R.: TCAD analysis of frequency dependent intrinsic and extrinsic parameters of GEWE-SiNW MOSFET. In: Nanoelectronics, Materials & Devices, pp. 185–188 (2015)
22. Hu, C.: Modern Semiconductor Device for Integrated Circuit, pp. 261–274. Prentice Hall, Englewood Cliffs (2009)
23. ATLAS User's Manual: SILVACO Int. Santa Clara, CA (2014)
24. Gupta, N., Chaujar, R.: Influence of gate metal engineering on small-signal and noise behaviour of silicon nanowire MOSFET for low-noise amplifiers. Appl. Phys. A **122**(8), 1–9 (2016)
25. Iannaccone, G., Curatola, G., Fiori, G.: Effective Bohm Quantum potential for device simulators based on drift-diffusion and energy transport. In: Simulation of semiconductor processes and devices (SISPAD), pp. 275–278 (2004)
26. Suk, S.D., et al.: High performance 5 nm radius twin silicon nanowire MOSFET (TSNWFET): fabrication on bulk Si wafer, characteristics, and reliability. In: IEEE IEDM Technology Digest, pp. 717–720 (2005)
27. Yang, B., Buddharaju, K.D., Teo, S.H.G., Singh, N., Lo, G.Q., Kwong, D.L.: Vertical silicon-nanowire formation and gate-all-around MOSFET. IEEE Electron Device Lett. **29**(7), 791–794 (2008)
28. Rustagi, S.C., et al.: CMOS Inverter based on gate-all-around silicon-nanowire MOSFETs fabricated using top-down approach. IEEE Electron Device Lett. **28**(11), 1021–1024 (2007)
29. Polishchuk, I., Ranade, P., King, T.J., Hu, C.: Dual work function metal gate CMOS technology using metal interdiffusion. IEEE Electron Device Lett. **22**(9), 444–446 (2001)
30. Liu, J., Wen, H.C., Lu, J.P., Kwong, D.L.: Dual-work-function metal gates by full silicidation of Poly-Si with Co-Ni bi-layers. IEEE Electron Device Lett. **26**(4), 228–230 (2005)
31. Na, K.Y., Kim, Y.S.: Silicon complementary metal-oxide semiconductor field-effect transistors with dual work function gate. Jpn. J. Appl. Phys. **45**(12), 9033–9036 (2006)
32. Shirak, O., Shtempluck, O., Kotchtakov, V., Bahir, G., Yaish, Y.E.: High performance horizontal gate-all-around silicon nanowire field-effect transistors. Nanotechnology **23**, 395202 (2012)

33. Moon, D., Choi, S.-J., Duarte, J.P., Choi, Y.-K.: Investigation of silicon nanowire gate-all-around junctionless transistors built on a bulk substrate. IEEE Trans. Electron Devices **60**, 1355–1360 (2013)
34. Lee, J.-H., Kim, B.-S., Choi, S.-H., Jang, Y., Hwangc, S.W., Whang, D.: A facile route to Si nanowire gate-all-around field effect transistors with a steep subthreshold slope. Nanoscale **5**, 8968–8972 (2013)
35. Iwai, H.: Roadmap for 22 nm and beyond. Microelectron. Eng. **86**(7), 1520–1528 (2009)
36. Raghavan, A., Srirattana, N., Laskar, J.: Modelling and Design Techniques for RF Power Amplifiers. Wiley, New York (2007)
37. Lovelace, D., Costa, J., Camilleri, N.: Extracting small- signal model parameters of silicon MOSFET transistors. In: Proceedings IEEE MTT-S, pp. 865–868 (1994)
38. Tsividis, Y.: Operation and Modeling of the MOS Transistor, 2nd edn. Oxford Universiy Press, New York (2010)
39. Malik, P., Gupta, R.S., Chaujar, R., Gupta, M.: AC analysis of nanoscale GME-TRC MOSFET for microwave and RF applications. Microelectron. Reliab. **52**(1), 151–158 (2012)
40. Razavi, B., Yan, R.H., Lee, K.F.: Impact of distributed gate resistance on the performance of MOS devices. IEEE Trans. Circuits Syst. I Fundam. Theory Appl. **41**(11), 750–754 (1994)
41. Je, M., Shin, H.: Accurate four-terminal RF MOSFET model accounting for the short-channel effect in the source to drain capacitance. In: Simulation of Semiconductor Processes and Devices (SISPAD), pp. 247–250 (2003)

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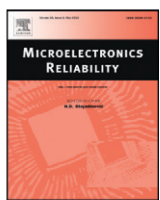

Investigation of temperature variations on analog/RF and linearity performance of stacked gate GEWE-SiNW MOSFET for improved device reliability

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MOSFET

ABSTRACT

In this paper, reliability issues of Stacked Gate (SG)-Gate Electrode Workfunction Engineered (GEWE)-Silicon Nanowire (SiNW) MOSFET is examined over a wide range of ambient temperatures (200–600 K) and results so obtained are simultaneously compared with conventional SiNW and GEWE-SiNW MOSFET using 3D-technology computer aided design quantum simulation. The results indicate that two temperature compensation points (TCP) are obtained: one for drain current (I_{ds}) and other for cut-off frequency (f_T) where device Figure Of Merits (FOMs) become independent of temperature, and it is found at 0.65 V in SG-GEWE-SiNW in comparison to other devices, hence will open opportunities for wide range of temperature applications. Furthermore, significant improvement in Analog/RF performance of SG-GWEW-SiNW is observed in terms of I_{on}/I_{off}, Subthreshold Swing (SS), device efficiency, f_T, noise conductance and noise figure as temperature reduces. It is also observed that at low temperature SG-GEWE-SiNW unveils highly stable linearity performance owing to reduced distortions. These results explain the improved reliability of SG-GEWE-SiNW at low temperatures over GEWE-SiNW MOSFET.

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1. Introduction

CMOS devices are extensively used in the field of satellite communications, military, medical equipment, automobile, nuclear sectors, and wireless/mobile communications. For these applications and the demand of nanoscale transistor, it is important to investigate the device behavior at a wide range of temperatures [1]. Also, it has been demonstrated that the performance of MOS devices significantly improves when operating at low temperatures in terms of improved carrier mobilities, on-currents, gain, sub-threshold slope, cut-off frequency, short-channel effects and noise performance [2,3]. The unwanted flow of high leakage current through the junction and the presence of latch-up put a limit on the use of bulk MOS devices at high temperatures. Several technologies have been reported in the literature as an option for both low and high-temperature operations. Some of them are Silicon on Insulator (SOI) [4], Recessed Channel [5], III–V semiconductors [6], Nanowire transistors [7], etc. Among them, SiNW emerged as most favorable in electronic devices due to the fact that its concentration, dopant type can be changed during synthesis. Also, its mobility is higher than bulk silicon due to stronger 1D quantum confinement. The body thickness of the nanowire can readily be reduced to a few nm in size that is the major challenge to achieve using bulk silicon. Also, since hot carrier degradation is a major concern for short channel MOSFETs [8], several engineering schemes are reported in literature such as gate metal workfunction engineering [9], drain engineering and channel engineering to overcome this degradation. Moreover, the high-k gate dielectric is required for suppressing the leakage current with scaling of gate oxide. The high-k gate stack also improves Short Channel Effects (SCEs) and increases I_{on}/I_{off} ratio in sub-100 nm regime. Therefore, a novel device is proposed in which stacked gate architecture is implemented on Gate Electrode Workfunction Engineered (GEWE) Silicon Nanowire MOSFET. In this work, for the first time performance and reliability issues of SG-GEWE-SiNW MOSFET are examined in terms of Analog, RF/Noise and Linearity FOMs at different temperatures (200–600 K) with an aim to analyze the temperature at which the device is more reliable for analog and RF applications. The results so obtained are simultaneously compared with GEWE-SiNW and SiNW MOSFET. Section 2 explains the 2D cross-sectional view of three different device structures including all the necessary boundary conditions. In Section 3, all the default simulation models are described along with the calibration of simulation models with experimental results. Section 4 contains the results obtained by device variation at 200–600 K and conclusions are drawn in Section 5.

2. Device structure and its description

Fig. 1(a) shows the simulated 3-D device structure of SG-GEWE-SiNW MOSFET and its 2-D cross-sectional view along with GEWE-SiNW and SiNW MOSFET are shown in Fig. 1(b–c). The detailed

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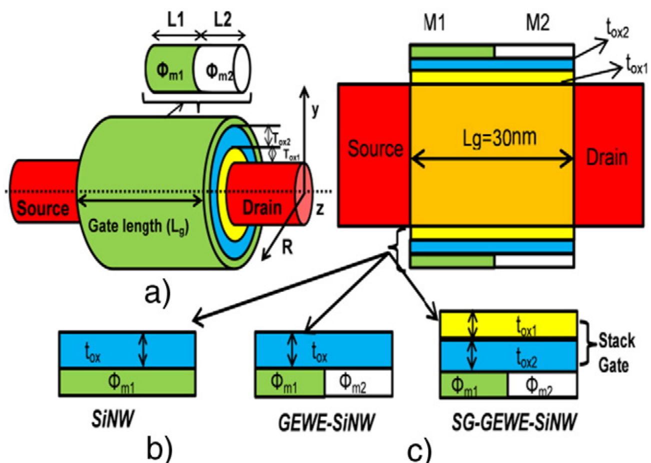

Fig. 1. (a) Simulated device structure of SG-GEWE-SiNW MOSFET, (b–c) 2-D schematic view of SiNW, GEWE-SiNW and SG-GEWE-SiNW MOSFET.

descriptions of all the three device structures are listed in Table 1. All simulations have been performed using ATLAS and DEVEDIT 3D device simulator.

With GEWE (workfunction transition) scheme, there is a significant reduction in the SCEs, current driving capability improves due to step potential which is due to two dissimilar metal gates, reduced electric field at the drain end thus providing hot-carrier reliability [10]. Further, we have already shown that integration of GEWE scheme onto GAA-SiNW MOSFET improves device efficiency, enhanced on-current, reduces short channel effects [11,12]. Moreover, Table 2 lists all the boundary conditions associated with the device structure.

3. Simulation methodology

All simulations have been performed using the ATLAS device simulator [13]. The physical models used during simulations are shown in Table 3. Moreover, the quantum confinement in the sub-nm scaled device may not be negligible [14] because the inversion layer thickness in the conducting silicon nanowire channel is comparable to the nanowire dimension. Thus, the quantization effect is also taken care of in the simulation. To incorporate all non-local effects, we have adopted the quantum mechanical models which are more accurate than drift-diffusion method. The Bohr Quantum Potential (BQP) Model [15] with alpha (α) = 0.5 and gamma (γ) = 1.2 was used to taking quantum mechanical effects into consideration. This model introduces a position dependent quantum potential, Q, which is added to the Potential Energy of a given carrier type. This quantum potential is derived using the Bohm interpretation of quantum mechanics [16] and is described below:

$$Q_{eff} = \frac{-\hbar^2}{2}\gamma\nabla\frac{\left[M^{-1}\nabla(n^{\alpha})\right]}{n^{\alpha}} \tag{1}$$

where M^{-1} is the inverse effective mass tensor, α and γ are two adjustable parameters, n is the electron (or hole) density and h is a Planck's constant. Additionally, numerical methods such as BICGST (bi-conjugate gradient stabilized) have been considered to obtain the solutions with improved convergence in 3D device structure [13]. Default simulator coefficients for all parameters have been employed. To fairly analyze the device performances, all the three devices are optimized to have the same threshold voltage, i.e. 0.4 V by changing channel doping. The calibration of model parameters used in simulation has been performed according to the experimental results [17] and closed proximity of simulated results with the experimental results as shown in Fig. 2 validates the choice of parameters invoked during simulation.

4. Results and discussion

4.1. Analog performance

In this sub-section, the analog performance of all three device structures is studied under different temperatures (200 K–600 K) with an aim to analyze the reliability issues in terms of analog FOMs such as on-current, device efficiency, switching ratio, Subthreshold swing (SS) and Threshold Voltage (V_{th}). Fig. 3(a) shows the transfer characteristics of SiNW, GEWE-SiNW and GS-GEWE-SiNW MOSFET for different temperatures. With the increase in temperature, the drain current rises but at a particular bias point, current starts decreasing with increase in temperature. This point is called Zero Crossing Point (ZCP) or Temperature Compensation Point (TCP). At this point, the effect of temperature is cancelled by two main controlling terms i.e. channel mobility (decreases I_D) and threshold voltage (increases I_D), since the temperature dependency of the drain current is influenced by V_{th} as given by $I_D \approx \mu_{eff}(T)\,[V_{gs} - V_{th}(T)]$. The TCP is desirable for wide temperature IC applications where the V—I characteristics show little or no variation with respect to temperature. With the increase in temperature, the on-current decreases due to degradation in mobility of carriers owing to more scattering of carriers. However, on-current of SG-GEWE-SiNW is comparatively high in comparison to GEWE-SiNW due to the incorporation of thin layer of HfO_2, which improves current driving capability of the device. The switching ratio is an important parameter for digital and analog applications and it is clearly evident from Fig. 3(b) that with an increase in temperature switching ratio degrades in an exponential manner for all three devices since phonon scattering is dominant at high temperature which degrades off-current. SG-GEWE-SiNW shows better switching performance in comparison to GEWE-SiNW due to lowering of tunneling carriers owing to gate stack engineering. Fig. 3(c) shows the device efficiency as a function of drain current for different temperatures. It is observed that device efficiency degrades in all three devices as temperature increases due to enhanced drain current in the linear region.

Fig. 4(a) indicates that the threshold voltage (V_{th}) degrades with an increase in temperature due to shift in Fermi level and band-gap energy. In general, MOSFET's I—V characteristics are proportional to the square of the overdrive voltage. Hence, a small change in V_{th} causes a significant

Table 1
Default design parameters used in the analysis.

Design parameters	SiNW	GEWE-SiNW	SG-GEWE-SiNW
Channel length (L_g)	30 nm	30 nm	30 nm
Substrate doping (N_A)	1×10^{16} cm^{-3}	1×10^{16} cm^{-3}	1×10^{16} cm^{-3}
Radius of nanowire (R)	5 nm	5 nm	5 nm
Source/drain doping (N_D^+)	5×10^{19} cm^{-3}	5×10^{19} cm^{-3}	5×10^{19} cm^{-3}
Effective oxide thickness (t_{ox})	t_{ox} = 1.5 nm	t_{ox} = 1.5 nm	t_{ox} = 1.5 nm t_{ox1} = 1.2 nm (SiO_2) t_{ox2} = 1.85 nm (HfO_2)
Dielectric constant	$k = 3.9$	$k = 3.9$	$k_1 = 3.9$, $k_2 = 24$
Gate metal work function	Φ_m = 4.8 eV	Φ_{m1} = 4.8 eV [Gold] Φ_{m2} = 4.4 eV [Titanium]	Φ_{m1} = 4.8 eV [Gold] Φ_{m2} = 4.4 eV [Titanium]

Table 2
Boundary conditions.

Boundary conditions	SiNW	GEW-SiNW	SG-GEWE-SiNW
1. Surface potential			
a) At the interface of tow metals	φ_m	$\varphi_{m1}=\varphi_{m2}$	$\varphi_{m1}=\varphi_{m2}$
b) At source end ($z=0$)	$\varphi=V_{bi}$	$\varphi=V_{bi}$	$\varphi=V_{bi}$
c) At drain end	$\varphi=V_{bi}+V_{ds}$	$\varphi_D=V_{bi}+V_{ds}$	$\varphi_D=V_{bi}+V_{ds}$
2. Electric field			
a) At the interface of two metals	$E=\frac{\partial\varphi_1(r,z)}{\partial z}$	$\frac{\partial\varphi_1(r,z)}{\partial z}=\frac{\partial\varphi_2(r,z)}{\partial z}$ at $z=L1$	$\frac{\partial\varphi_1(r,z)}{\partial z}=\frac{\partial\varphi_2(r,z)}{\partial z}$ at $z=L1$
b) At the center of cylindrical channel	$\frac{\partial\varphi_1(r,z)}{\partial r}=0$	$\frac{\partial\varphi_1(r,z)}{\partial r}=0$	$\frac{\partial\varphi_1(r,z)}{\partial r}=0$
c) At Si/SiO$_2$ interface	$\frac{\partial\varphi_1(r,z)}{\partial r}=\frac{q.n_a}{\varepsilon_{si}}=C_{ox}(V_{gs}-V_{FB}-\varphi_s)$ $C_{ox}=\frac{\varepsilon_{SiO_2}}{R\,,\ln(1+\frac{t_{ox}}{R})}$	$\frac{\partial\varphi_1(r,z)}{\partial r}=\frac{q.n_a}{\varepsilon_{si}}=C_{ox}(V_{gs}-V_{FB1}-\varphi_s)$ $\frac{\partial\varphi_2(r,z)}{\partial r}=\frac{q.n_a}{\varepsilon_{si}}=C_{ox}(V_{gs}-V_{FB2}-\varphi_s)$ $C_{ox}=\frac{\varepsilon_{SiO_2}}{R\,,\ln(1+\frac{t_{ox}}{R})}$	$\frac{\partial\varphi_1(r,z)}{\partial r}=\frac{q.n_a}{\varepsilon_{si}}=C_{ox}(V_{gs}-V_{FB1}-\varphi_s)$ $\frac{\partial\varphi_2(r,z)}{\partial r}=\frac{q.n_a}{\varepsilon_{si}}=C_{ox}(V_{gs}-V_{FB2}-\varphi_s)$ $C_{ox}=\frac{\varepsilon_{SiO_2}}{R\,,\ln(1+\frac{t_{eff}}{R})}$ $t_{eff}=t_{SiO_2}+(\frac{\varepsilon_{SiO_2}}{\varepsilon_{high-k}})t_{high-k}$

Where V_{bi} = built in potential, φ_{m1} and φ_{m2} are surface potentials due to metal gates 1 and 2 respectively, V_{FB1} and V_{FB2} are flat band voltage due to metal gates 1 and 2 respectively, R is the radius of nanowire and t_{eff} is the effective oxide thickness of stack gate design.

shift in the output current. Therefore, it is essential to calculate the V_{th} accurately with temperature changes. This change is more prominent at high temperature (600 K) in SG-GEWE-SiNW MOSFET compared to its conventional counterparts. Further, the Subthreshold Swing (SS) is an important parameter for calculating the off-state current. At 200 K, a low sub-threshold swing results in high I_{on}/I_{off} ratio which indicates a faster transition between off and on states compared to 600 K. SS of SG-GEWE-SiNW is 53 mV/decade and 146 mV/decade for 200 K and 600 K respectively in comparison to GEWE-SiNW and SiNW MOSFET as shown in Fig. 4(b). These results show that SG-GEWE-SiNW is more reliable for analog and switching applications, at a lower temperature.

4.2. RF noise performance

In this sub-section, the impact of ambient temperature has been studied on the characteristics such as gate capacitance, cut-off frequency, intrinsic delay, energy delay product, noise conductance and minimum noise figure for SG-GEWE-SiNW MOSFET, GEWE-SiNW and SiNW MOSFET. If a MOSFET is operating in the linear region, both S/D regions are connected to the inversion layer, and C_g which is total gate capacitance is equally partitioned between source/drain i.e., $C_{gd} \approx C_{gs} \approx C_g/2$ where as in the saturation region, $C_{gs} \approx 2/3 \times C_g$ and $C_{gd} \approx 0$. Fig. 4(a) shows the bias dependent intrinsic parasitic gate capacitance (C_g) at different temperatures, and it is observed as temperature decreases, C_g also decreases resulting in device high speed which is desirable for switching and digital applications. Since, the gate capacitance is due to charges present in the inversion region including the depletion charges of source and drain regions. These charge carriers are temperature and bias dependent. C_g is sufficiently lower in the case of SG-GEWE-SiNW due to gate stacking engineering scheme and GEWE scheme which results in the improved screening of conducting channel from drain variations. For evaluating the RF performance of the device, cut-off frequency (f_T) is one of the utmost important parameter. It is a specification for high-speed digital applications and can be defined as follows:

$$f_T = \frac{g_m}{2\pi C_g} \quad (2)$$

where g_m is the transconductance. As is evident from Fig. 5(b), the peak value of f_T enhances in the case of GEWE-SiNW in comparison to SiNW and its value further enhances with the incorporation of GS technology. As the temperature reduces, peak value of f_T enhances. This is due to a reduction in parasitic capacitance as shown in Fig. 5(a) and improvement in current driving capability as shown in Fig. 3(a) at a lower temperature (200 K). Also, TCP in f_T is observed at 0.6 V in the case of GEWE-SiNW MOSFET, which is useful for RF applications operating at low or high temperatures. Intrinsic Delay (τ) is another significant parameter

Table 3
Physical Models.

S·No.	Physical models	Description
1.	*Mobility models*	Lombardi CVT and Constant Low Field Mobility Model
2.	*Recombination model*	Shockley Read Hall (SRH) Recombination is included to incorporate minority recombination effects with carrier lifetime = 1×10^{-7} s.
3.	*Statistics*	Boltzmann Transport Model The use of Boltzmann statistics is normally justified in semiconductor device theory, but Fermi-Dirac statistics are necessary to account for certain properties of very highly doped (degenerate) materials.
4.	*Energy transport model*	Hydrodynamic Model is used as it includes all nonlocal effects and is more accurate than the drift-diffusion method. Drift Diffusion Model shows shortcomings as channel length scales down to 50 nm.
5.	*Quantum mechanical model*	Quantum Mechanical Model plays an important role on determining the performance of surrounding gate MOSFET In this paper we take into account QMEs.

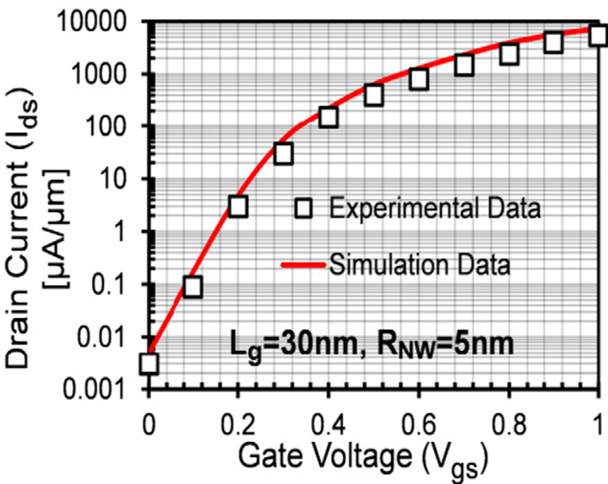

Fig. 2. Calibration of simulation model with experimental result to validate our simulation models [17].

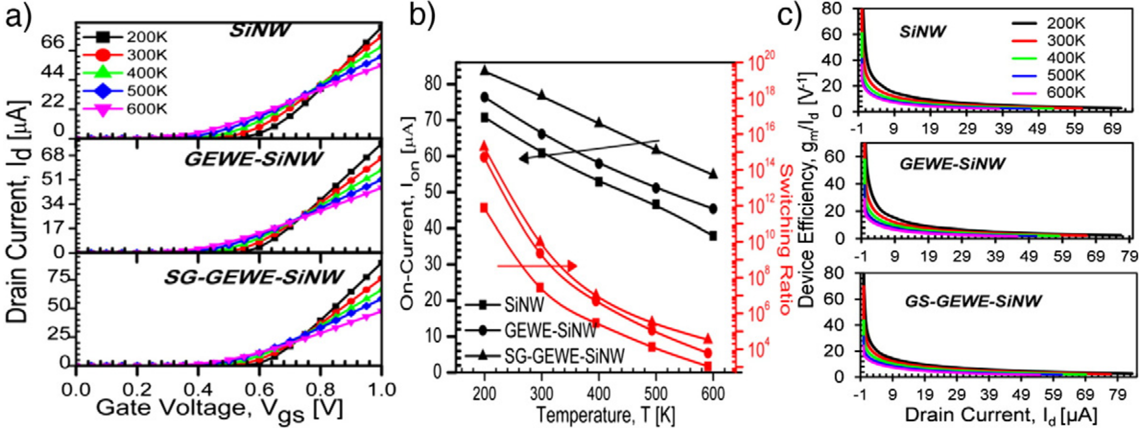

Fig. 3. (a) Transfer characteristics, (b) drain transconductance and (c) device efficiency of SiNW, GEWE-SiNW and GS-GEWE-SiNW MOSFET for different temperatures.

defined as a measure of switching performance of the device and is expressed as:

$$\tau = \frac{C_g . V_{ds}}{I_{ON}} \quad (3)$$

where V_{ds} is the bias voltage applied to drain and I_{on} is the on-current. Fig. 6(a) reveals as temperature increases; delay degrades due to degradation in parasitic capacitance with an increase in temperature as shown in Fig. 5(a). It is also observed that there is a noticeable reduction in intrinsic delay of SG-GEWE-SiNW MOSFET than its conventional counterpart due to the incorporation of HfO_2 as a gate stack which lowers the effective oxide thickness (EOT), reduces leakage current and thus enhances the on-current as is evident from Fig. 3(b), in addition reduction in parasitic capacitances also leads to a considerable reduction of intrinsic delay.

Apart from these FOMs, Energy Delay Product (EDP) is a valuable FOM as far as circuit applications are concerned. The EDP is a measure of energy and is defined by the product of the average energy (E_{ave}) and the gate delay (τ). It calculates the energy consumed per switching event (such as in logic families). EDP improves at lower values of temperature due to a reduction in intrinsic delay and parasitic gate

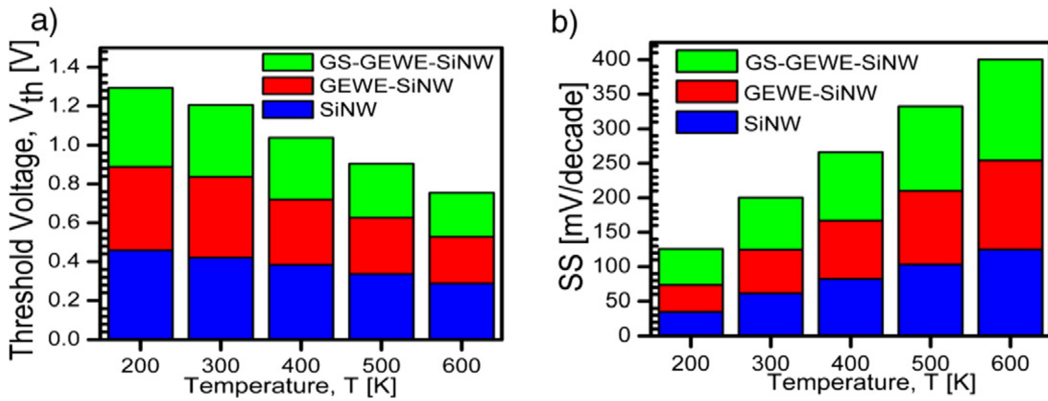

Fig. 4. (a) Threshold voltage, (b) subthreshold swing and of SiNW, GEWE-SiNW and GS-GEWE-SiNW MOSFET.

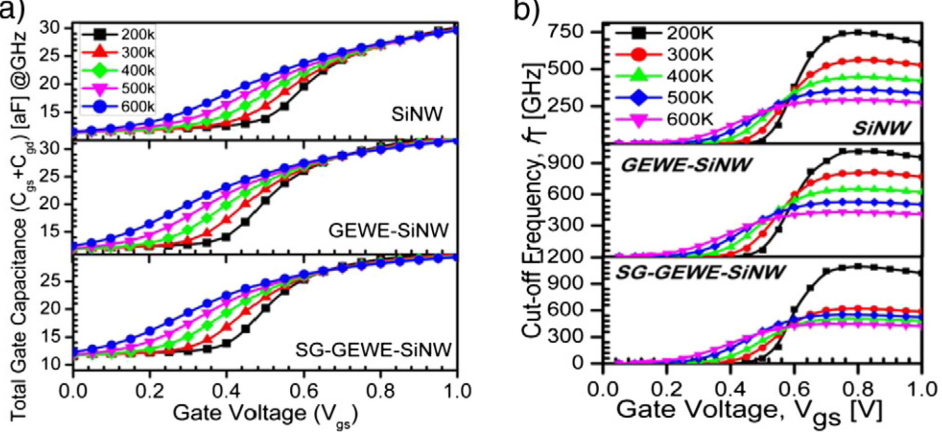

Fig. 5. (a) Total gate capacitance (C_g) and (b) cut-off frequency (f_T) of SiNW, GEWE-SiNW and GS-GEWE-SiNW MOSFET at $V_{ds} = 0.5$ V.

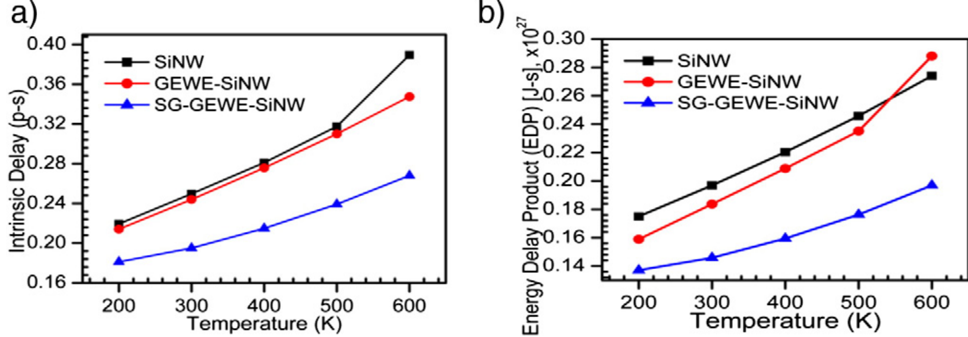

Fig. 6. (a) Intrinsic delay and (b) energy delay product (EDP) of SiNW, GEWE-SiNW and GS-GEWE-SiNW MOSFET at $V_{ds} = 0.5$ V.

capacitance (C_g) as evident from Fig. 6(b). Thus, SG-GEWE-SiNW MOSFET emerged as a promising device for RF applications such as in microwave/wireless working at low temperature in comparison to a higher temperature. Moreover, Noise FOMs such as Minimum noise figure (NF_{MIN}) and Noise Conductance (NC) are of utmost important for the designing of CMOS RF circuits at high frequency. Noise figure is an assessment of deterioration of signal to noise ratio caused by a component in RF signal chains. It is used to evaluate the performance of an amplifier or a radio receiver, with lower values specifying better performance. NC is used to estimate the power spectral density of noise current generators and low noise conductance is required in RF amplifiers and LNAs. As ambient temperature increases, both the NFmin and NC degrade for all three devices as shown in Fig. 7(a–b) due to high phonon scattering and the effect of temperature on noise FOMs is less observed in the case of SG-GEWE-SiNW, and its magnitude is comparatively low in comparison to other devices. Thus, the proposed design (SG-GEWE-SiNW) is more reliable and more thermally stable compared to SiNW at low temperature.

4.3. Linearity and harmonic distortions

Non-linearity of MOS amplifiers is generally from transconductance higher order harmonics term (g_{m3}) that may interfere with fundamental frequency (ω_0) and causes non-linearity. It is a major reliability concern at a device level. The lower the amplitude of g_{m3} the higher the linearity of the device. Fig. 8(a) shows that the amplitude of g_{m3} reduces as temperature increases, and SG-GEWE-SiNW is more linear in comparison to other conventional devices owing to reduced off (leakage) current due to the amalgamation of HfO_2 layer over SiO_2, which results in enhanced on-current and thus lowering of g_{m3}. VIP3 represents

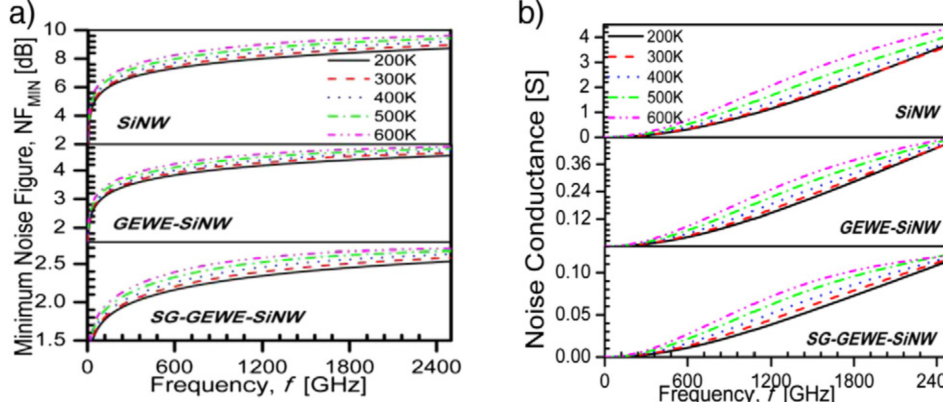

Fig. 7. (a) Minimum noise figure (NF_{MIN}) and (b) noise conductance as a function of frequency for SiNW, GEWE-SiNW and SG-GEWE-SiNW MOSFET at $V_{ds} = 0.5$ V and $V_{gs} = 1.0$ V.

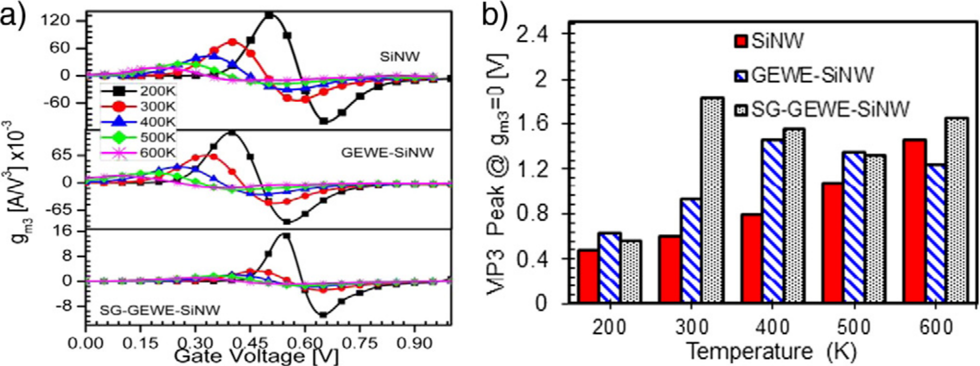

Fig. 8. (a) g_{m3} and (b) VIP3 of SiNW, GEWE-SiNW and GS-GEWE-SiNW MOSFET for different temperatures at $V_{gs} = 1.0$ V and $V_{ds} = 0.5$ V.

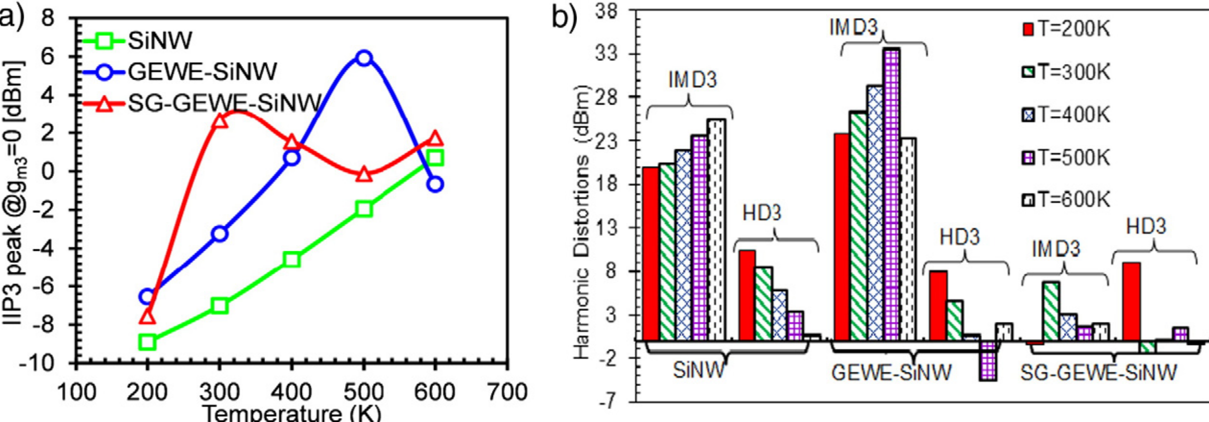

Fig. 9. (a) VIP3 and (b) IIP3 of SiNW, GEWE-SiNW and GS-GEWE-SiNW MOSFET for different temperatures at $V_{gs} = 1.0$ V and $V_{ds} = 0.5$ V.

extrapolated input voltage at which first and third order harmonics of drain current are equal. The peak of VIP3 reveals the cancellation of third-order nonlinearity coefficient by device internal feedback around second-order nonlinearity. Fig. 8(b) shows that peak value of VIP3 increases significantly in the case of gate-stack architecture at 300 K due to lowering of g_{m3} and enhancement in transconductance (g_m) owing to high on-current and improvement in carrier mobility.

Moreover, the main FOM which governs amplifier's efficiency and linearity is the third-order intercept point (IIP3). Third-order intercept is a theoretical point at which the third-order distortion signal amplitudes equal the input signals, and it is useful in determining the linearity condition of an amplifier. The peak value of IIP3 attains maximum value at 300 K in SG-GEWE-SiNW and as temperature increases its value deteriorates but in the case of GEWE-SiNW and SiNW peak value of IIP3 increases as temperature increases as is shown in Fig. 9(a). Thus to signify SG-GEWE-SiNW MOSFET is more linear and thus more reliable at a lower temperature. Harmonic distortion (HD) is another important reliability issue in analog and RF circuit applications that arises owing to the non-linear performance of devices. Nonlinearity may induce intermodulation (IM), which generates signals with frequencies different from the input ones. These unwanted signals may fall into the band of interest, interfering or even corrupting the desired components [18]. Therefore, Harmonic Distortions such as 2nd order HD (HD2), 3rd Order HD (HD3) and 3rd Order Intermodulation Distortion (IMD3) has also been studied.

$$HD3 = 0.25\, V_a^2 \frac{\left(\frac{d^2 g_{m1}}{dV^2{}_{GT}}\right)}{6g_{m1}} \quad (4)$$

where V_a is the amplitude of AC signal and considered to be very small, of about 50 mV for the IFM analysis. Fig. 9(b) shows that HD3 significantly reduces as temperature increases due to higher transconductance owing to high on-current and is in accordance with Eq. (4) and reduction of HD3 is more prominent in SG-GEWE-SiNW MOSFET in comparison to its conventional counterparts. Furthermore, IMD3 plays a significant role in determining intermodulation distortion in CMOS RF amplifiers, since these applications make use of both phase and amplitude modulation. Therefore, reduction of IMD3 in the RF front-end transceiver parts is of great importance for maximizing overall system performance and minimizing distortions. It is clearly evident from Fig. 9(b) that IMD3 is reduced appreciably as temperature reduces due to a reduction in higher order harmonics and VIP3. Thus, linearity performance of SG-GEWE-SiNW MOSFET degrades at low temperature and performance improves as temperature rises.

5. Conclusion

The effect of temperature on the Analog/RF and Linearity performance has been studied with an aim to analyze the reliability issues of SG-GEWE-SiNW. Results reveal that with the incorporation of Stack Gate scheme, device performance enhances significantly due to reduction in leakage current. SG-GEWE-SiNW MOSFET exhibits 1.1 and 1.2 times improvement in I_{on} and thus 29% and 9.3% enhancement in f_T at low temperature (200 K) in comparison to GEWE-SiNW and SiNW MOSFET owing to decrement in off-current and gate capacitance. Moreover, Noise FOMs also improved at 200 K but linearity FOMs slightly degrade but show high linearity at 300 K in SG-GEWE-SiNW and will not hinder that much to the device performance. Therefore, SG-GEWE-SiNW can be very attractive for low temperature analog/digital circuits and in space technology. In addition, it is found that ZTC is observed at lower gate bias for SG-GEWE-SiNW, which leads to significant improvement in static and dynamic performance. Thus, the results so obtained can be serving as a worthy design tool for circuits operating at wide range of temperatures.

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References

[1] H.-.S.P. Wong, et al., Nanoscale CMOS, Proc. IEEE 87 (4) (1990) 537–570.
[2] J. Sun, Y. Taur, R. Dennard, S. Klepner, Submicrometer-channel CMOS for low temperature operation, IEEE Trans. Electron Devices 34 (1) (1987) 19–27.
[3] S. Hong, et al., Low-temperature performance of nanoscale MOSFET for deep-space RF applications, IEEE Electron Device Lett. 29 (7) (2008) 775–777.
[4] J. Kim, et al., Thickness and temperature dependence of the leakage current in hafnium-based Si SOI MOSFETs, Microelectron. Reliab. 52 (12) (2012) 2907–2913.
[5] A. Kumar, N. Gupta, R. Chaujar, Power gain assessment of ITO-based transparent gate recessed channel (TGRC) MOSFET for RF/wireless applications, Superlattice. Microst. 91 (2016) 290–301.
[6] J.A. del Alamo, Nanometre-scale electronics with III–V compound semiconductors, Nature 479 (2011) 317–323.
[7] Y. Cui, et al., High performance silicon nanowire field effect transistors, Nano Lett. 3 (2003) 149–152.
[8] T. Grasser, Hot Carrier Degradation in Semiconductor Devices, Springer, 2014.
[9] W. Long, H. Ou, J.M. Kuo, K.K. Chin, Dual-material gate (DMG) field effect transistor, IEEE Trans. Electron Devices 46 (5) (May 1999) 865–870.
[10] C.Y. Zheng, The using of dual-material gate MOSFET in suppressing short-channel effects: a review, Presented at IEEE Int. Conference on Electronics, Communications and Control (ICECC) 2011, pp. 2979–2982.

[11] N. Gupta, A. Kumar, R. Chaujar, Oxide bound impact on hot-carrier degradation for gate electrode workfunction engineered (GEWE) silicon nanowire MOSFET, Microsyst. Technol. (May 2015) 1–10.
[12] N. Gupta, A. Kumar, R. Chaujar, Impact of device parameter variation on RF performance of gate electrode workfunction engineered (GEWE)-silicon nanowire (SiNW) MOSFET, J. Comput. Electron. 14 (3) (Sep. 2015) 798–810.
[13] ATLAS, User's Manual, SILVACO Int., Santa Clara, CA, 2014.
[14] A. Chaudhry, J.N. Roy, MOSFET models, quantum mechanical effects and modeling approaches: a review, J. Semicond. Technol. Sci. 10 (2010) 20–27.
[15] V.S. Patnaik, A. Gheedia, M.J. Kumar, 3D simulation of nanowire FETs using quantum models, July, August, September, 2008.
[16] G. Iannaccone, G. Curatola, G. Fiori, Effective Bohm quantum potential for device simulators based on drift-diffusion and energy transport, Simulation of Semiconductor Processes and Devices (SISPAD) 2004, pp. 275–278.
[17] S.D. Suk, et al., High performance 5 nm radius twin silicon nanowire MOSFET (TSNWFET): fabrication on bulk Si wafer, characteristics, and reliability, IEEE IEDM Tech. Dig. (2005) 717–720.
[18] A. Dutta, K. Koley, C.K. Sarkar, Analysis of harmonic distortion in asymmetric underlap DG-MOSFET with a high-k spacer, Microelectron. Reliab. 54 (2014) 1125–1132.

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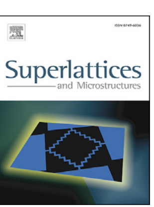

Optimization of high-k and gate metal workfunction for improved analog and intermodulation performance of Gate Stack (GS)-GEWE-SiNW MOSFET

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ABSTRACT

This work optimizes the gate engineering scheme (both gate stack and gate metal workfunction engineering) of Stacked Gate (SG) Gate Electrode Workfunction Engineered (GEWE)-Silicon Nanowire MOSFET at 300 K for improved analog and intermodulation performance. This has been done by evaluating and analyzing the metrics such as Switching Ratio, Subthreshold Swing (SS), Device Efficiency, channel and output resistance, VIP3, IIP3, 1-dB Compression Point, IMD3, HD2 and HD3. Simulation results exhibit that HfO_2 as a gate stack exhibit high linearity at a comparatively low gate bias of 0.56 V with higher IIP3 (6.21 dBm) and low IMD3 (9.6 dBm). Further, the characteristics/performance is modulated by adjusting the workfunction difference of metal gate. This study demonstrates that SiNW MOSFET modeled with HfO_2 as a gate stack over SiO_2 interfacial layer, and gate metal workfunction difference (ΔW) of 4.4 eV can be considered as a promising potential for low power switching component in ICs and Linear RF amplifiers.
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1. Introduction

According to Moore's Law, the transistor size has shrunk to get higher device performance and reduce its cost, but short channel effects (SCEs) such as DIBL, HCEs, Punch through, V_{th} roll-off, etc., hinders its performance. To overcome such limitations, various device designs and engineering schemes are reported in literature such as Dual Gate [1], Recessed channel [2], Multi-Gate [3], CNT FET [4], Nanowire FET [5], etc. Among them, Silicon Nanowire (SiNW) emerged as a most promising in electronic devices because its properties such as concentration, dopant type can be changed during synthesis. Also, its mobility is higher than bulk silicon due to stronger quantum confinement. The body thickness (diameter) of the nanowire can readily be reduced to a few nanometers in size scale that is challenging to obtain using bulk silicon [6] and to get further improvement against SCEs the concept of SiNW MOSFET was put forward by Cui et al. [7] in 2003 concluded that silicon nanowires MOSFET as building blocks for future nano-electronics.

Moreover, the most common issue of scaling is oxide thickness. As oxide thickness scales down to 1.5 nm or below, the leakage current increases up to 1 A/cm^2 at 1 V due to direct tunneling of carriers which, consequently increases the static power and hence affect the circuit operation as reported by Ref. [8,9]. High-k films are proved to be the most promising solution. However, these films result in high fringing fields from gate to source/drain regions and thus degrading the device

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performance. This constraint can be overcome by using gate stack architecture consisting of SiO_2 layer as a passivation between high-k films and bulk by keeping the effective oxide thickness (EOT) constant, high-k dielectrics permit the increase in physical oxide thickness to prevent gate tunneling [10,11] and thus improves the carrier efficiency but at the same time, gate capacitance increases. Therefore, for selection of high-k materials relationship between dielectric constant and band-offset must be considered. The excessive high-k constant is generally undesirable owing to a tradeoff between dielectric constant and band-offset. Hence, selection of metal material becomes necessary. This work is an extension of [12], mainly focusing on effect of high-dielectric constant (such as Si_3N_4, HfO_2, ZrO_2) and gate metal workfunction in terms of Analog and Intermodulation metrics, since linearity plays an important role in RFIC designing and high-frequency systems because nonlinearity causes harmonic generation, gain compression, desensitization etc. [13,14]. A high linearity with low distortion is preferred in modern communication systems even while working with a weak signal. Thus, previously performed analysis has been extended with an aim to optimize the value of high-dielectric constant and gate metal workfunction difference (ΔW) which can be used as a reference tool for designing circuits for different analog and RF applications where linearity is a major concern.

2. Device structure and its description

Fig. 1 (a–b) shows the 3D and 2D cross-sectional view of gate stack (GS) GEWE SiNW MOSFET. The channel length of the device is 30 nm and radius of SiNW is 5 nm. The length of region 1 (L_1) and region 2 (L_2) are 15 nm each which is towards the 45 nm node CMOS technology as stated in ITRS Roadmap [15]. The Source/Drain region is heavily doped with an n-type impurity of 1×10^{19} $cm^{-3}$of 5 nm long, while the SiNW is doped with a p-type impurity of 1×10^{16} $cm^{-3}$and effective oxide thickness is 1.5 nm. The gate metal work function at the source end (Φ_{m1}) is 4.8 eV (Au) and metal gate work function at the drain end (Φ_{m2}) is 4.4 eV (Ti) as shown in Fig. 1. In this analysis, all the junctions are assumed as abrupt, and the doping profiles are uniform. All simulations have been performed using ATLAS and DEVEDIT 3D device simulator [16].

3. Simulation methodology

All the simulations have been executed using physical models accounting for the electric field-dependent and concentration-dependent carrier mobilities, Shockley–Read–Hall (SRH) recombination/generation with doping dependent carrier lifetime, inversion layer Lombardi CVT mobility model, wherein concentration-dependent mobility, high field saturation model are all included [15]. To incorporate all non-local effects, we have adopted the quantum mechanical models which are more accurate than drift-diffusion method. To characterize the device performance accurately, it is very important to define the carrier transport with proper models. The quantum confinement effect in the deep scaled device may not be negligible [17]. Since the inversion charge layer thickness in the conducting silicon nanowire channel is comparable to the nanowire dimension, thus the effect of quantum confinement in the sub-nm device may not be negligible. The Bohr Quantum Potential (BQP) model [18] can also be used with Energy balance and hydrodynamic models, where the semi-classical potential is modified by the quantum potential in a similar way as for the continuity equations. The model introduces a position dependent quantum potential, Q, which is added to the Potential Energy of a given carrier type. This quantum potential is derived using the Bohm interpretation of quantum mechanics [19] and is described below:

Time-independent Schrodinger equation can be written as:

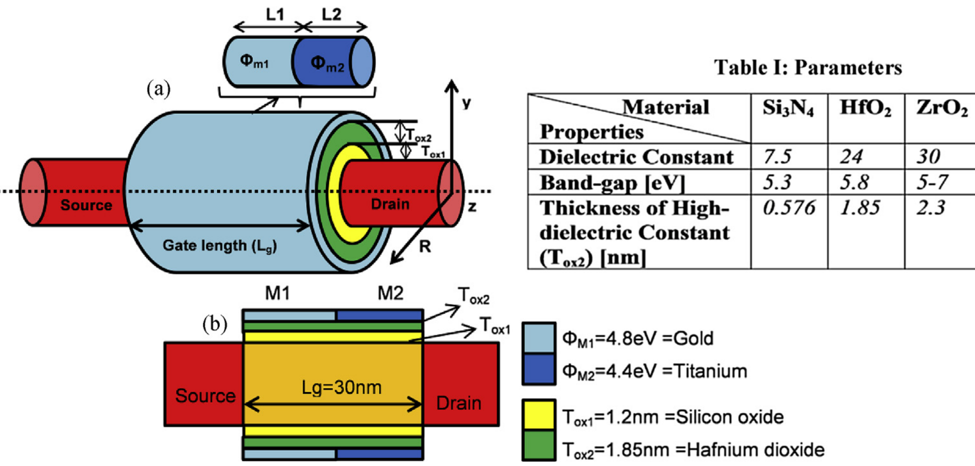


Table I: Parameters

Material / Properties	Si_3N_4	HfO_2	ZrO_2
Dielectric Constant	7.5	24	30
Band-gap [eV]	5.3	5.8	5-7
Thickness of High-dielectric Constant (T_{ox2}) [nm]	0.576	1.85	2.3

Fig. 1. (a–b): Schematic Representation and its 2D cross-sectional view of GS-GEWE-SiNW MOSFET, Table 1 show the default parameters of high-k.

Table 1
Parameters.

Properties	Material		
	Si_3N_4	HfO_2	ZrO_2
Dielectric constant	7.5	24	30
Band gap [eV]	5.3	5.8	5–7
Thickness of high-dielectric constant (T_{ox2}) [nm]	0.576	1.85	2.3

$$\left(\frac{-\hbar}{2m^*}\nabla^2 - V\phi\right)\psi_j = E_j\psi_j \tag{1}$$

According to Bohm's interpretation of quantum mechanics, the wave function in a polar representation can be written as:

$$\psi = R\cdot\exp\left(\frac{iS}{\hbar}\right) \tag{2}$$

where R is probability density per unit volume, S has dimensions of action (energy $\times$ time).

By substituting equation (2) in (1), the Schrodinger equation can be written as:

$$\frac{\hbar^2}{2}\nabla\left\{M^{-1}\nabla\left[R\cdot\exp\left(\frac{iS}{\hbar}\right)\right]\right\} + V\cdot R\exp\left(\frac{iS}{\hbar}\right) = E\cdot R\cdot\exp\left(\frac{iS}{\hbar}\right) \tag{3}$$

where M^{-1} is the inverse of effective mass tensor and $M^{-1}\nabla S$ is the local velocity of particle associated to wave function. Real part of Eq. (3) is interpreted as continuity equation of probability density while imaginary part states that the total energy, E is conserved and equal to the sum of potential (V) and kinetic energy (0.5 $M^{-1}\nabla S$). Therefore, Quantum potential is defined as:

$$V = \frac{-\hbar^2}{2}\frac{\nabla\left(M^{-1}\nabla R\right)}{R} \tag{4}$$

Potential V is obtained by the single particle Schrodinger equation and use "*mean field approximation*" and consider an effective quantum Bohm Potential defined as the weighted average potential for all carriers constrained in confining potential. Effective Quantum Potential is written as:

$$Q_{eff} = \frac{-\hbar^2}{2}\gamma\nabla\frac{\left[M^{-1}\nabla(n^\alpha)\right]}{n^\alpha} \tag{5}$$

where α and γ are two adjustable parameters, M^{-1} is the inverse effective mass tensor, n is the electron (or hole) density and h is a Planck's constant.

Bohr Quantum Potential (BQP) Model with alpha = 0.5 and gamma = 1.2 was used to take quantum mechanical effects into consideration. Additionally, numerical methods such as BICGST (bi-conjugate gradient stabilized) have been considered to obtain the solutions with improved convergence in 3D device structure [16]. Default simulator coefficients for all parameters have been employed. In order to fairly analyze the device performances, all the three devices are optimized to have the same threshold voltage, i.e., 0.32 V by changing channel doping. The calibration of model parameters used in simulation has been performed according to the experimental results [20] and closed proximity of simulated results with the experimental results as shown in Fig. 2 validates the choice of parameters invoked during simulation. A proposed summary of the process flow, outlining the fabrication process of GEWE-SiNW MOSFET is shown in Table 2.

4. Results and discussion

4.1. Analog figure of merits (FOMs)

In this subsection, the effect of dielectric constant and gate metal workfunction engineering are examined in terms of switching ratio, subthreshold swing (SS), device efficiency, channel resistance and output resistance as analog FOMs.

4.1.1. Switching ratio and device efficiency

As is evident from Fig. 3(a), on-current is higher in the case of HfO_2 due to lowering of tunneling current owing to higher band-gap and band-offset in comparison to Si_3N_4 and ZrO_2. Consequently, a switching ratio which is an important criterion for any analog application also enhances in HfO_2 due to reduced off-current as indicated by Fig. 3(a). Further, as high-k

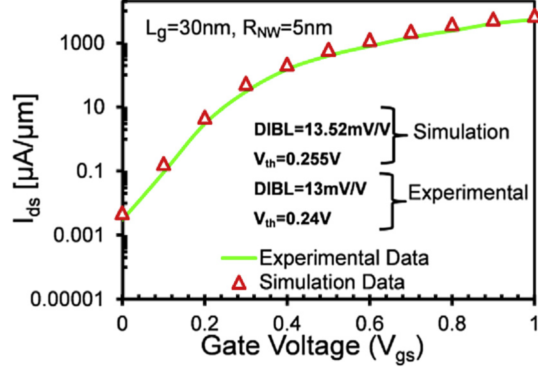
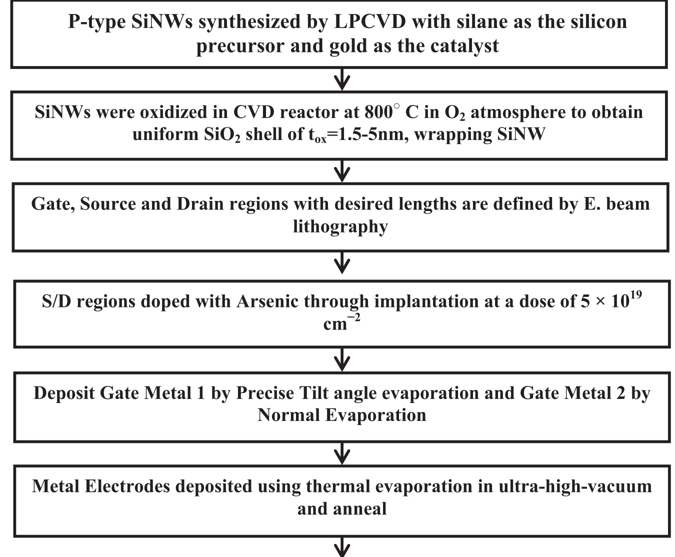


Fig. 2. Calibration of simulated models with experimental results with L = 30 nm, R = 5 nm and V_d = 1.0 V.

Table 2
Process flow of GEWE-SiNW MOSFET [21–24].



dielectric increases, the threshold voltage (V_{th}) increases due to a reduction in off-current but subthreshold swing (SS) decreases as shown in Fig. 3(b).

Moreover, the effect of workfunction difference is also examined by considering HfO_2 as a gate-stack and varying the workfunction at the drain end (Φ_{M2}) by keeping source side metal workfunction constant (Φ_{M1}). As gate metal workfunction at the drain end (Φ_{M2}) decreases or workfunction difference increases (ΔW), on-current rises significantly as shown in Fig. 3(b) due to redistribution of the electric field in the channel region owing to step potential due to workfunction difference which enhances carrier transport efficiency and thus current driving capability as is manifest from contour plots shown in Fig. 4(a–e) and this effect is more apparent if workfunction difference increases as stated in Ref. [25], thus, also signifying the suppression of short channel effects. On the contrary, switching ratio reduces with increase in workfunction difference as exhibited in Fig. 3(c). This reduction is due to workfunction engineering scheme in which there is a high electric field in the channel that results into tunneling of carriers and causes higher off-current and thus degrades switching ratio. Hence, the trade-off between on-current and off-current is required to optimize the switching ratio depending upon the applications. Moreover, V_{th} rises with an increase in workfunction at the drain end. As workfunction difference decreases, the efficacy of GEWE scheme reduces and thus reduces the on-current as shown in Fig. 3(c) thereby enhancing threshold voltage as reported in Fig. 3(d). As revealed by Fig. 3(c) that sub-threshold current (off-current) decreases as workfunction difference increases due to which subthreshold swing reduces as demonstrated in Fig. 3(d).

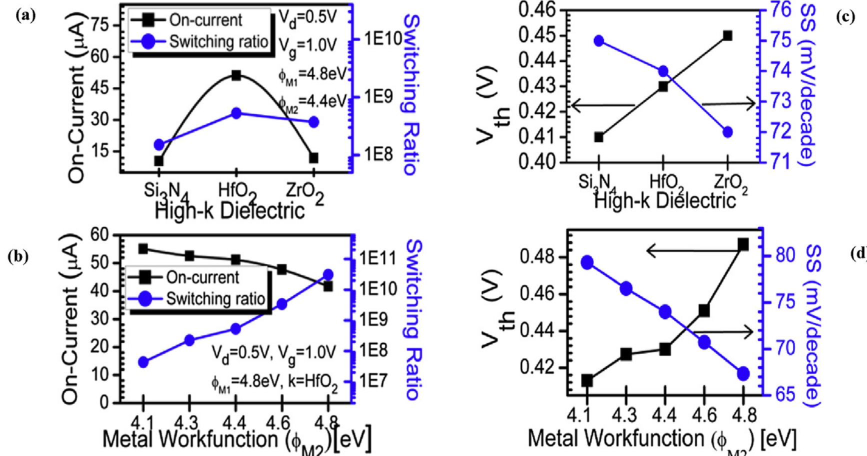


Fig. 3. (a–d) On-Current, switching ratio and Threshold Voltage, Subthreshold Swing for different high-dielectrics and metal gate workfunction (Φ_{M2}) at $V_d = 0.5$ V and $V_g = 1.0$ V.

Also, device efficiency [D.E] (g_m/I_d) is an important parameter in the design of analog circuits, which offers the measure of efficiency to convert power into speed. Fig. 5 (a) shows the device efficiency as a function of drain current for different high-k materials. It is clearly shown that the variation of D.E occurs mainly at the weak-inversion region of operation and in the saturation region, device efficiency reduces due to a reduction in transconductance and increment in on-current. The decrease in D.E. with HfO_2 is due to large deviation in drain current as compared to transconductance. Further, with the tuning of workfunction difference of metal gates, D.E. of HfO_2 gate stack increases as revealed by Fig. 5(b) owing to enhanced transconductance with an increase in workfunction difference.

4.1.2. Output resistance and channel resistance

The output resistance (R_{out}) of a MOSFET is the inverse of the output conductance. The most important characteristics of R_{out} in the circuit design are maximum R_{out} which decides the maximum available power gain for the device. Fig. 6(a–d) shows that in the linear region ($V_d = 0–0.2$ V), R_{out} decreases, and it is desirable when the circuit is to act as an ideal voltage source, and as drain bias reaches to saturation region ($V_d = 0.4–0.8$ V) R_{out} rises due to increasing drain current. This effect is more pronounced for HfO_2 in comparison to other high-k dielectrics.

As ΔW increases, output resistance ($=1/g_D$) reduces in the linear region, and as drain bias increases to saturation, its value increases as evident from Fig. 6(c). Thus, higher ΔW (approx. 0.7eV) of GS-GEWE-SiNW is beneficial for analog applications. Likewise, channel resistance (R_{ch}) of a MOSFET reveals the resistance of carriers in the channel region. As is clearly shown in Fig. 7(a) that with the incorporation of HfO_2 as a high-k layer onto the interfacial layer, R_{ch} decreases and as V_{gs} increases, electrostatic gate control enhances and thus reduces channel resistance. This region is called linear, ohmic or triode region. On

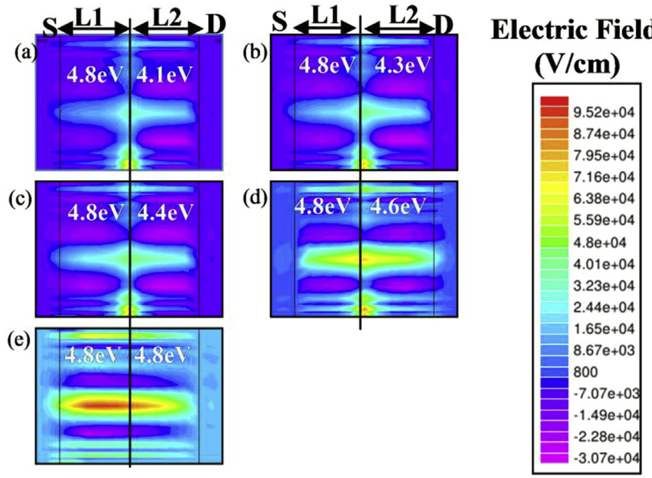


Fig. 4. (a–e) Electric Field Distribution for different metal gate workfunction (Φ_{M2}) at $V_{d;} = 0.5$ V and $V_g = 1.0$ V.

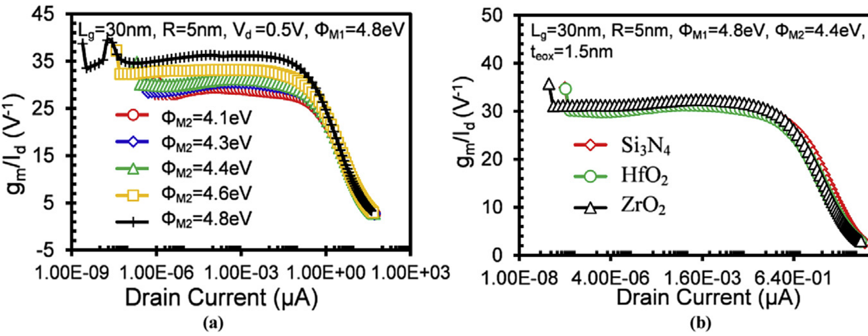


Fig. 5. Device Efficiency as a function of drain current for different high-dielectrics and metal gate workfunction ($Φ_{M2}$) at $V_d = 0.5$ V and $V_g = 1.0$ V.

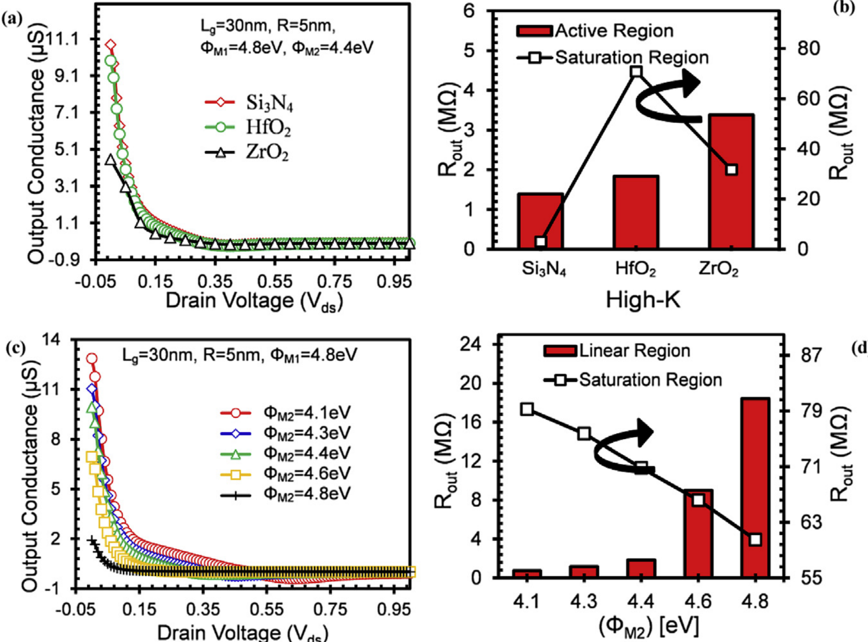


Fig. 6. (a–d): Output conductance as a function of drain voltage for different high-dielectrics and metal gate workfunction ($Φ_{M2}$) at $V_g = 1.0$ V.

the other hand, as workfunction at the drain end increases, carrier concentration decreases in the channel as is evident in contours of Fig. 8(a–e), due to which R_{ch} increases as shown in Fig. 7(b) which implies enhancement in the current driving capability of GS-GEWE-SiNW as ΔW increases. Thus, we have to choose optimum values of both high-k and workfunction difference for improved analog performance.

4.2. Linearity and harmonic distortion analysis

In this sub-section, linearity and distortion performance of GS-GEWE-SiNW MOSFET is investigated with an aim to find optimum high-k and gate workfunction difference for highly linear performance with low harmonic distortion. Non-linearity of MOS amplifiers is mainly from transconductance higher order harmonics (g_{m3}) that may interfere with the fundamental frequency and causes non-linearity. The metrics used in this work to evaluate the device linearity performance and inter-modulation distortion are higher order transconductance coefficients, *V*IP3, third-order input intercept point (IIP3), 1-dB intercept point and distortion such as second and third order harmonic distortion (HD2, HD3), third-order intermodulation distortion (IMD3) [26,27] which are defined as follows:

$$VIP3 = \sqrt{\frac{24 \times g_{m1}}{g_{m3}}} \tag{6}$$

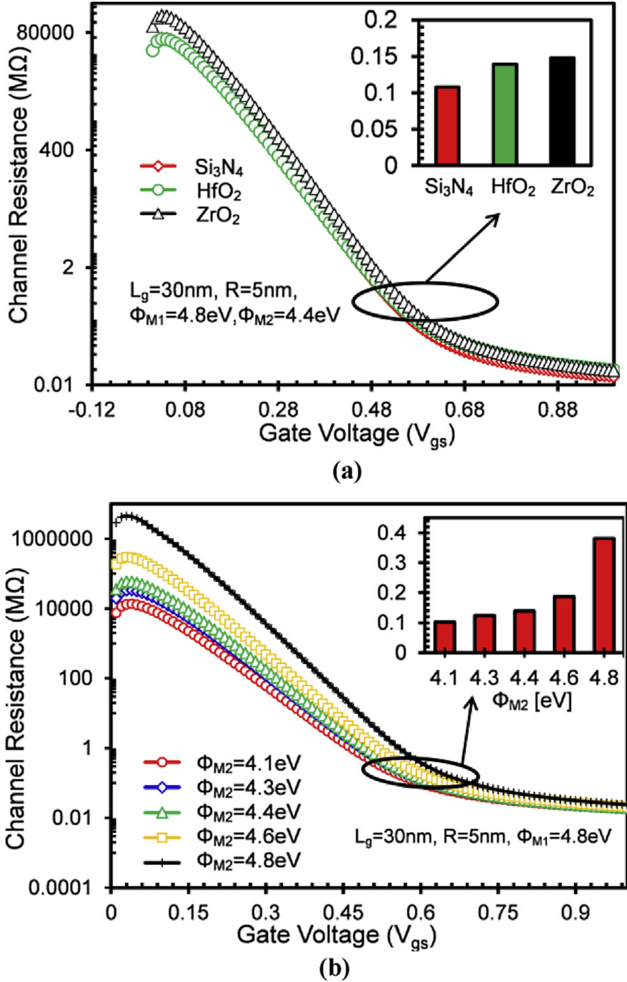


Fig. 7. (a–b): Channel Resistance as a function of gate voltage for different high-dielectrics at $V_d = 0.5$ V.

$$IIP3 = \frac{2}{3}\frac{g_{m1}}{g_{m3} \times Rs} \tag{7}$$

$$1 - dB\ Compression\ \text{Point} = 0.22 \times \sqrt{\frac{g_{m1}}{g_{m3}}} \tag{8}$$

where $g_{m1} = \frac{\partial I_d}{\partial V_{gs}}$, $g_{m3} = \frac{\partial^3 I_d}{\partial V_{gs}^3}$ and $R_S = 50\Omega$.

g_{m3} is a high-order derivative of I_d-V_{gs} characteristics and their amplitudes should be minimized for lower distortion. The value of V_{GS} at which the higher order of transconductance parameters (g_{m3}) becomes zero is known as zero crossover point (ZCP) which decides the optimum DC bias point for device operation. Higher gain can be realized by setting DC bias point close to $V_{th.}$ Fig. 9(a–b) shows the variation of g_{m3} as a function of gate overdrive voltage (V_{gs}-V_{th}) and the results indicate that incorporation of GS over GEWE-SiNW MOSFET lowers the amplitude of g_{m3} in comparison to GEWE-SiNW due to lowering of tunneling current which improves gate controllability and hence, transconductance and its harmonic distortion.

Also, the DC bias points shifts towards lower V_{gs} by changing the dielectric constant as shown in Fig. 9(b). Among all dielectrics, HfO_2 shows better improvement in terms of lower distortion (g_{m3}) and lower bias point in comparison to other high-k. With the increase in metal gate workfunction at the drain end (or reduces ΔW), there is not as much change in amplitude of g_{m3} as is evident from Fig. 9(c) due to change in on-current as reflected by Fig. 3(c) but the DC bias point shifts towards lower V_{gs} if ΔW increases as shown in Fig. 9(d).

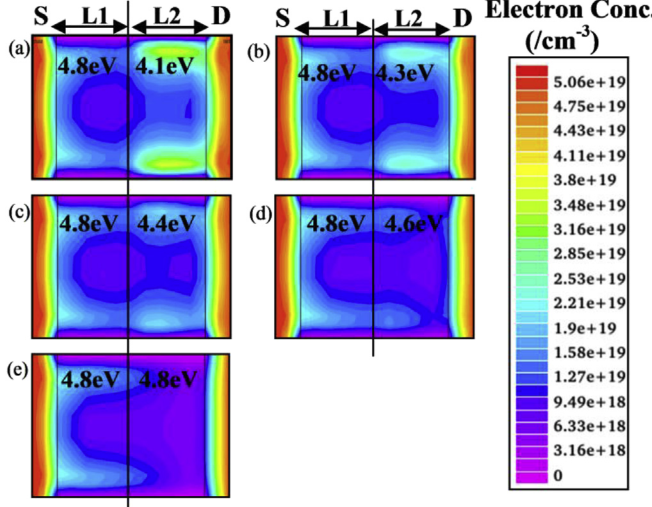


Fig. 8. (a–e) Electron Concentration Distribution for different metal gate workfunction (Φ_{M2}) at $V_d = 0.5$ V and $V_g = 1.0$ V.

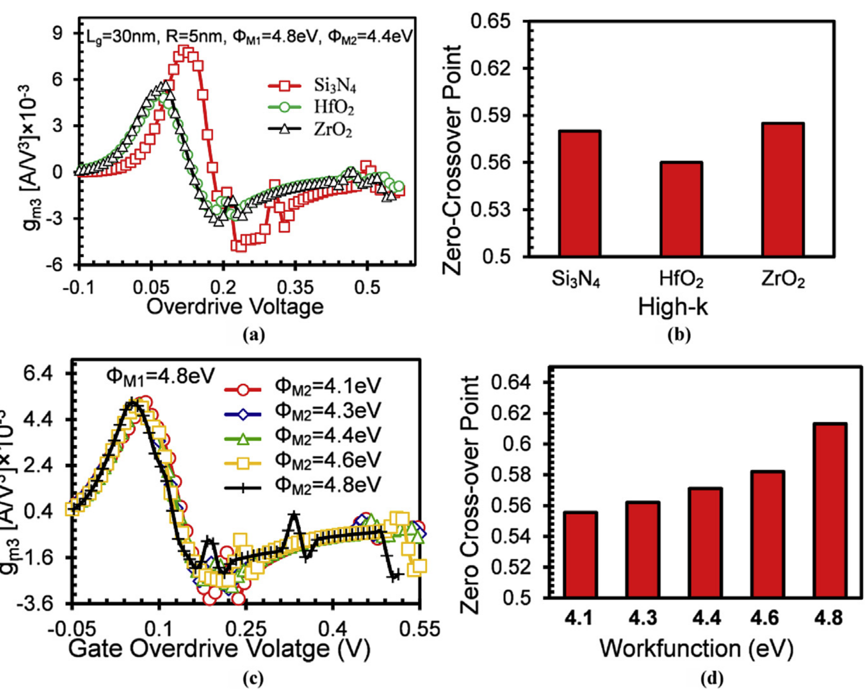


Fig. 9. (a–d): Higher order transconductance coefficients g_{m2} and g_{m3}, (c) Zero-Crossover Point for different high-dielectric materials at $V_d = 0.5$ V.

4.2.1. VIP3/IIP3 and 1-dB compression point

In all linearity FOMs, generally two peaks are appearing: one at a lower gate bias and maxima at higher gate bias for GS-GEWE-SiNW MOSFET. However, for analog circuit applications, it is desired that device should operate in moderate inversion region and not in the saturation region where power dissipation is more. So, in this analysis, a maximum appearing at a lower value of V_{gs} is considered for comparison. VIP3 represents extrapolated input voltage at which first and third order harmonics of drain current are equal and expressed as in Eq. (1). The peak of VIP3 reveals the cancellation of third-order nonlinearity coefficient by device internal feedback around second-order nonlinearity. Fig. 10(a) shows that peak value of VIP3 increases significantly in the case of gate-stack architecture at lower V_{gs}-V_{th} due to lowering of g_{m3} as given by eq. (1) and enhancement in transconductance (g_{m1}) owing to high on-current and improvement in carrier mobility. The peak value of VIP3 increases by 34% in HfO_2 in comparison to Si_3N_4 and is observed at lower bias voltage as shown in Fig. 10(a). Moreover, there are two important FOMs which govern amplifier's efficiency and linearity i.e. third-order intercept point (IIP3) and 1-dB compression

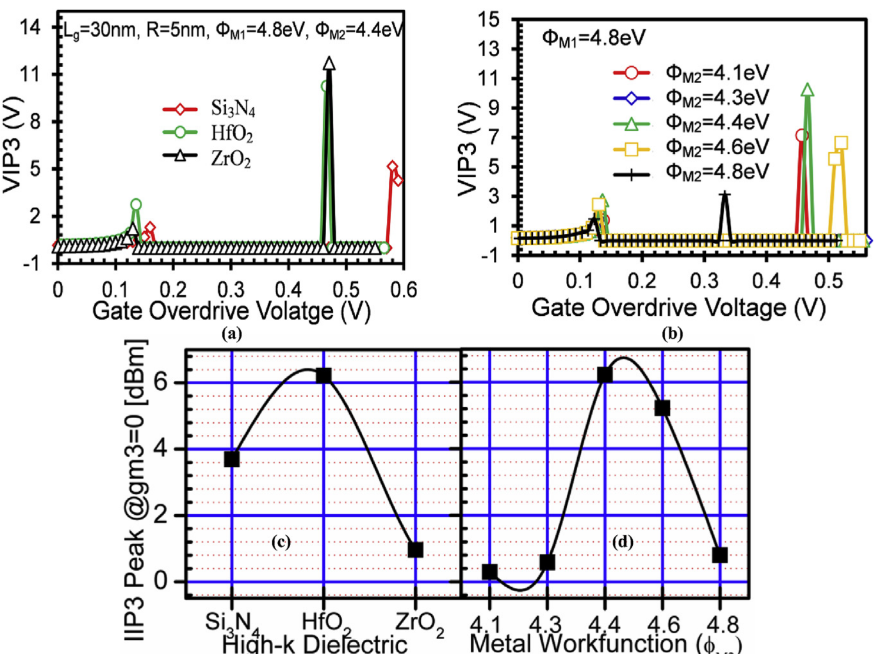


Fig. 10. (a–d): VIP3 as a function of gate overdrive voltage and Peak value of IIP3 for different high-k and gate metal workfunction at the drain end (Φ_{M2}) at $V_d = 0.5$ V and $V_g = 1.0$ V.

point (1 dB CP). In general for MOS based amplifiers, higher the output at the intercept, the better the linearity. Third-order intercept is a theoretical point at which the third-order distortion signal amplitudes equal the input signals, and it is useful in determining the linearity condition of an amplifier. IIP3 increases to a peak value (i.e. $g_{m3} = 0$) and IIP3 peak enhances with the incorporation of gate stack scheme, and its magnitude is higher in the case of HfO_2 due to high band offset which reduces the off-current, improves transconductance and thus enhances IIP3 as shown in Fig. 10(c).

The 1-dB compression point is the parameter that describes a circuit's tolerance to desensitization. It is essential to identify at what point compression occurs so that input levels can be limited to prevent distortion. It is usually the input power that causes the gain to decrease 1 dB from the normal linear gain specification. This parameter signifies the maximum input power that the amplifier circuit can handle by providing a fixed amount of gain, and if the input power surpasses the compression point, the gain starts falling. Hence, it is desirable that a 1-dB compression point should be as high as possible for the high linear amplifier. The effect of high-dielectrics on 1-dB compression point is presented in Fig. 11(a). The result shows 1-dB compression point in case of HfO_2 enhances by 1.4 and 2.3 times in comparison to Si_3N_4 and ZrO_2 respectively owing to reduced signal distortions and transconductance as stated in Eq. (4). Moreover, by modulating ΔW, linearity improves appreciably in terms of high VIP3, IIP3 and 1-dB CP peak in comparison to other cases due to a reduction in higher order harmonics and improvement in on-current as evident from Fig. 10 (b), 10(c) and 11(b).

4.2.2. Harmonic distortions

Harmonic distortion (HD) is an essential reliability issue in analog and RF circuit applications that arises owing to the non-linear performance of devices. Nonlinearity may induce intermodulation (IM), which generate signals with frequencies different from the input ones. These unwanted signals may fall into the band of interest, interfering or even corrupting the desired components [28]. Therefore, improved linearity performance of GEWE-SiNW MOSFET with HfO_2 as a gate stack is observed in the previous sub-section. In the following sub-section, Harmonic Distortion FOMs such as 2nd order HD (HD2), 3rd Order HD (HD3) and 3rd Order Intermodulation Distortion (IMD3) for the device are analyzed considering the effect of the gate stack and workfunction engineering. The distortion has been calculated through the integral function method (IFM) since this approach permits the distortion extraction from DC measurements without the need of an AC characterization, contrary to Fourier-based methods [29,30]. The approximate analytical expressions for HD2, HD3 and IMD3 are given as:

$$HD2 = 0.5 \ V_a \frac{\left(\frac{dg_{m1}}{dV_{GT}}\right)}{2g_{m1}} \quad (9)$$

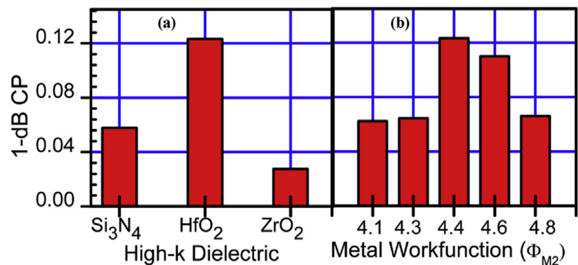


Fig. 11. (a–b): 1-dB Compression Point for different high-dielectrics and metal gate workfunction (Φ_{M2}) at $V_d = 0.5$ V and $V_g = 1.0$ V.

$$HD3 = 0.25\ V_a^2 \frac{\left(\frac{d^2 g_{m1}}{dV_{GT}^2}\right)}{6g_{m1}} \tag{10}$$

$$IMD3 = \left(\frac{9}{2} \times (VIP3)^3 \times g_{m3}\right)^2 \times R_S \tag{11}$$

where V_a is the amplitude of AC signal and considered to be very small, of about 50 mV for the IFM analysis. Fig. 12 (a) shows HD2 and HD3 as a function of gate overdrive voltage for GEWE-SiNW incorporating different high-k as a gate stack. It is observed that HD2 and HD3 are significantly reduced in HfO_2 at lower V_{GT} in comparison to other high-k materials. This reduction is due to higher transconductance owing to high on-current and is in accordance with Eqs. (4) and (5). IMD3 denotes the intermodulation harmonic power at which the first and third order intermodulation harmonic powers are equal.

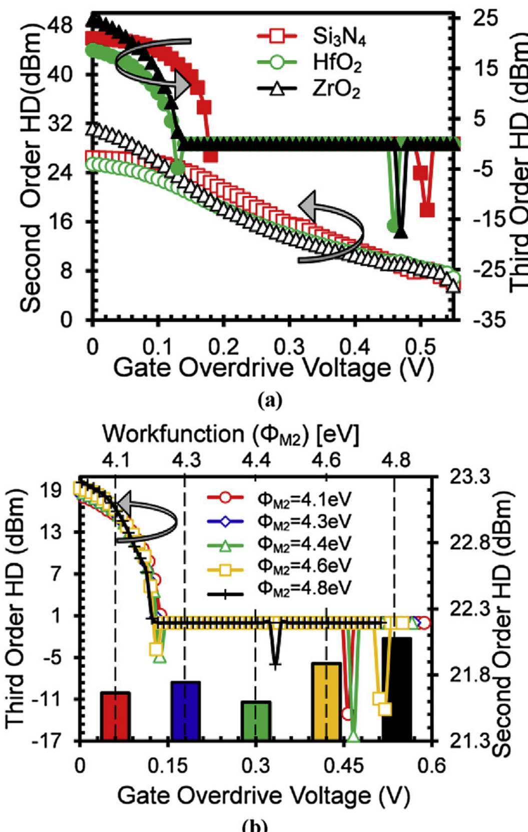


Fig. 12. (a–b): 2nd order Harmonic Distortion and 3rd Order Harmonic Distortion as a function of V_{GT} for different high-k and metal gate workfunction (Φ_{M2}) at $V_g = 1.0$ V, $V_d = 0.5$ V.

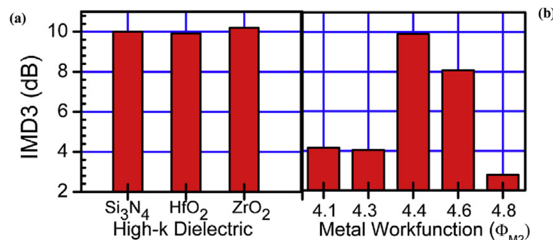


Fig. 13. (a–b): IMD3 for different high-k and metal gate workfunction (Φ_{M2}) at $V_g = 1.0$ V, $V_d = 0.5$ V.

IMD3 plays a major role in determining intermodulation distortion in CMOS RF amplifiers, since these applications make use of both phase and amplitude modulation. Therefore, reduction of IMD3 in the RF front-end transceiver parts is of great importance for maximizing overall system performance and minimizing distortions.

Fig. 13 (a) exhibits that IMD3 reduces with the incorporation of gate-stack design on GEWE-SiNW MOSFET, and this decrement is due to a reduction in higher order harmonics (g_{m3}) which originates from the non-linear transistor's I_d-V_{gs} characteristic according to Eq. (6). Moreover, distortions in GS (HfO_2+SiO_2)-GEWE-SiNW is further reduced by tuning gate metal workfunction as indicated by Figs. 12(b) and 13(b). As ΔW increases, gate controllability improves due to enhancement in carrier velocity which enhances g_{m1} and so from Eqs. (4)–(6) again, it is reflected that HD2, HD3 and IMD3 reduces. Thus, by appropriate selection of high-k material and gate metal workfunction, GS-GEWE-SiNW achieves high linearity with minimum distortion for RF amplifier.

5. Conclusion

In this work, improved analog and intermodulation performance of GS-GEWE-SiNW MOSFET is demonstrated by considering the effect of both high-k materials and metal gate workfunction difference. It is observed that high-k material (HfO_2) as a gate stack over SiO_2 interfacial layer in GEWE-SiNW significantly influence the analog performance of the device by enhancing the current driving capability and lowering of leakage current owing to large band-gap of HfO_2. Moreover, reduction in the electric field at the drain end and high carrier concentration in the channel region is achieved by tuning of gate workfunction difference which results in improved analog metrics such as switching ratio, channel resistance, device efficiency for low power analog applications. The enhancement in on-current and lowering of g_{m3} results into 2.14 and 2.28 times improvement in VIP3 in comparison to Si_3N_4 and ZrO_2 respectively and the input power rises to 0.128 dB in HfO_2 with $\Delta W = 0.4$eV, which the device can handle without compression. It is also examined that the DC bias point is shifted towards lower input voltage which indicates lowering of dynamic power consumption for circuit applications.

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References

[1] R.M. Barsan, Analysis and modeling of dual- gate MOSFETs, IEEE Trans. Electron Devices 28 (1981) 523–534.
[2] A. Kumar, N. Gupta, R. Chaujar, Power gain assessment of ITO-based transparent gate Recessed channel (TGRC) MOSFET for RF/wireless applications, Superlattices Microstruct. 91 (2015) 290–301.
[3] C.P. Auth, J.D. Plummer, Scaling theory for cylindrical, fully-depleted, surrounding-gate MOSFET's, IEEE Electron Device Lett. 18 (1997) 74–76.
[4] E. Gnani, A. Marchi, S. Reggiani, M. Rudan, G. Baccarani, Quantum-mechanical analysis of the electrostatics in silicon-nanowire and carbon nanotube FETs, Solid-State Electron. 50 (2006) 709–715.
[5] W. Xu, H. Wong, K. Kakushima, H. Iwai, Quasi-analytical model of ballistic cylindrical surrounding gate nanowire MOSFET, Microelectron. Eng. 138 (2015) 111–117.
[6] X. Chen, C.M. Tan, Modeling and analysis of gate-all-around silicon nanowire FET, Microelectron. Reliab. 54 (6–7) (July 2014) 1103–1108.
[7] Y. Cui, Z. Zhong, D. Wang, W.U. Wang, C.M. Lieber, High performance silicon nanowire field effect transistors, Nano Lett. 3 (2003) 149–152.
[8] S.H. Lo, D.A. Buchanan, Y. Taur, W. Wang, Quantum-mechanical modeling of electron tunneling current from the inversion layer of ultra-thin-oxide nMOSFET's, IEEE Electron Device Lett. 18 (5) (1997) 209–211.
[9] G. Ribes, J. Mitard, M. Denais, S. Bruyere, F. Monsieur, C. Parthasarathy, E. Vincent, G. Ghibaudo, Review on high-k dielectrics reliability issues, IEEE Trans. Device Mater. Reliab. 5 (1) (2005).
[10] B.H. Lee, J. Oh, H.H. Tseng, R. Jammy, H. Huff, Gate stack technology for nanoscale devices, Mater. Today 9 (2006) 32–40.
[11] R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros, M. Metz, High-k/Metal–Gate stack and its MOSFET characteristics, IEEE Electron Device Lett. 25 (2004) 408–410.
[12] N. Gupta, A. Kumar, R. Chaujar, Effect of dielectric engineering on analog and linearity performance of gate Electrode workfunction engineered (GEWE) silicon nanowire MOSFET, in: Proceedings of the 15th IEEE International Conference on Nanotechnology, 2015, pp. 928–931.
[13] C. Yu, J.S. Yuan, H. Yang, MOSFET linearity performance degradation subject to drain and gate voltage stress, IEEE Trans. Device Mater. Rel 4 (4) (2004) 681–689.

[14] A. Razavieh, D.B. Janes, J. Appenzeller, Transconductance linearity analysis of 1-D, nanowire FETs in the quantum capacitance limit, IEEE Trans. Electron Devices 60 (2013) 2071–2076.
[15] C. Hu, Modern Semiconductor Device for Integrated Circuit, Prentice Hall, 2009, pp. 261–274.
[16] ATLAS User's Manual, SILVACO Int, Santa Clara, CA, 2014.
[17] A. Chaudhry, J.N. Roy, Mosfet models, quantum mechanical effects and modeling approaches: a review, J. Semicond. Technol. Sci. 10 (2010) 20–27.
[18] V.S. Patnaik, A. Gheedia, M.J. Kumar, 3D Simulation of Nanowire FETs Using Quantum Models, 2008. http://web.iitd.ac.in/~mamidala/HTMLobj1227/jul_aug_sep08.
[19] G. Iannaccone, G. Curatola, G. Fiori, Effective Bohm Quantum Potential for device simulators based on drift-diffusion and energy transport, in: Simulation of Semiconductor Processes and Devices (SISPAD), 2004, pp. 275–278.
[20] S.D. Suk, et al., High performance 5 nm radius twin silicon nanowire MOSFET (TSNWFET): fabrication on bulk Si wafer, characteristics, and reliability, IEEE IEDM Tech. Dig. (2005) 717–720.
[21] O. Shirak, O. Shtempluck, V. Kotchtakov, G. Bahir, Y.E. Yaish, High performance horizontal gate-all-around silicon nanowire field-effect transistors, Nanotechnology 23 (2012) 395202 (8pp.).
[22] D. Moon, S.-J. Choi, J.P. Duarte, Y.-K. Choi, Investigation of silicon nanowire gate-all-around junction less transistors built on a bulk substrate, IEEE Trans. Electron Devices 60 (2013) 1355–1360.
[23] J.-H. Lee, B.-S. Kim, S.-H. Choi, Y. Jang, S.W. Hwangc, D. Whang, A facile route to Si nanowire gate-all-around field effect transistors with a steep subthreshold slope, Nanoscale 5 (2013) 8968–8972.
[24] W. Long, H. Ou, J.M. Kuo, K.K. Chin, Dual-material gate (DMG) field effect transistor, IEEE Trans. Electron Devices 46 (5) (May 1999) 865–870.
[25] W. Long, K.K. Chin, Dual material gate field effect transistor (DMGFET), IEDM Tech. Dig. (1997) 549–552.
[26] R. Chaujar, R. Kaur, M. Saxena, M. Gupta, R.S. Gupta, Intermodulation distortion and linearity performance assessment of 50-nm gate length L-DUMGAC MOSFET for RFIC design, Superlattices Microstruct. 44 (2) (August 2008) 143–152.
[27] Ó. Breandán, T.J. Brazil, An accurate nonlinear MOSFET model for intermodulation distortion analysis, IEEE Microw. Wirel. Comp. Lett. 14 (2004) 352–354.
[28] A. Dutta, K. Koley, C.K. Sarkar, Analysis of Harmonic distortion in asymmetric underlap DG-MOSFET with high-k spacer, Microelectron. Reliab. 54 (2014) 1125–1132.
[29] A. Cerdeira, M.A. Alemán, M. Estrada, D. Flandre, Integral function method for determination of nonlinear harmonic distortion, Solid. State. Electron. 48 (2004) 2225–2234.
[30] R.T. Doria, A. Cerdeira, J.P. Raskin, D. Flandre, M.A. Pavanello, Harmonic distortion analysis of double gate graded-channel MOSFETs operating in saturation, Microelectron. J. 39 (2008) 1663–1670.

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Influence of gate metal engineering on small-signal and noise behaviour of silicon nanowire MOSFET for low-noise amplifiers

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Abstract In this paper, we have investigated the small-signal behaviour and RF noise performance of gate electrode workfunction engineered (GEWE) silicon nanowire (SiNW) MOSFET, and the results so obtained are simultaneously compared with SiNW and conventional MOSFET at THz frequency range. This work examines reflection and transmission coefficients, noise conductance, minimum noise figure and cross-correlation factor. Results reveal significant reduction in input/output reflection coefficient and an increase in forward/reverse transmission coefficient owing to improved transconductance in GEWE-SiNW in comparison with conventional counterparts. It is also observed that minimum noise figure and noise conductance of GEWE-SiNW is reduced by 17.4 and 31.2 %, respectively, in comparison with SiNW, thus fortifying its potential application for low-noise amplifiers (LNAs) at radio frequencies. Moreover, the efficacy of gate metal workfunction engineering is also studied and the results validate that tuning of workfunction difference results further improvement in device small-signal behaviour and noise performance.

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1 Introduction

Aggressive scaling of CMOS dimensions had led to enhancement of cut-off frequency and maximum oscillator frequency which leads to a promising candidate for RFICs which was previously overlooked by other active devices [1, 2]. However, conventional CMOS shows shortcomings such as DIBL, hot-carrier effects and mobility degradation as device dimensions go in sub-micrometre. According to ITRS [3], amalgamation of new technologies is becoming crucial for deep sub-micron CMOS devices as recently reported in the literature [4–6]. Si nanowire FETs are more attractive than the conventional dual-gate (DG), SOI, III–V-based FETs and FinFETs because of higher on-current conduction due to stronger quantum confinement which results in higher mobility than bulk silicon, and also its properties such as concentration and dopant type can be changed during synthesis. In addition, the radius of the nanowire can readily be reduced to a few nanometres in size that limits the scaling of conventional MOSFET and also because of their adoptability for high-density integration including that of 3D [7, 8]. It was also found that gate-all-around (GAA) silicon nanowire transistors (SiNWTs) have cut-off frequency larger than that of planar Si MOSFET [9–11]. However, as with many novel device architectures, the SiNW MOSFET has problems of its own. One major problem facing nanowire MOSFETs with SiO_2 gate stack is the lower threshold voltage than desired. But, channel doping to correct the threshold voltage is difficult due to the narrow radius of nanowire. In addition, carrier mobility is also impacted with higher channel doping. Hence, there is a need of integration of some engineering schemes to overcome such effect. Gate workfunction tuning would thus make a better solution [12]; it is the most promising engineering scheme as it improves the transport

efficiency of carriers by modifying electric field in the channel and surface potential along the channel which results in enhanced transconductance and reduced SCEs [13]. It has already been demonstrated in our previous work that incorporation of GEWE engineering scheme onto silicon nanowire MOSFET alleviates short channel effects such as hot-carrier effects and DIBL [14, 15]. Also, improvement in cut-off and maximum oscillator frequency has also reported in our previous work [16, 17]. The most appropriate method to examine small-signal behaviour of MOSFET at high frequencies involves *S*-parameter measurements. *S*-parameters are most commonly employed for those networks that are operating at RF and microwave frequencies where signal power and energy analysis are more easily computed than voltages and currents. Since, at high frequency it is very difficult to estimate current and voltages. Short and open circuits (used by definitions of most n-port parameters) are hard to realize at high frequencies. As a result, microwave engineers work with so-called *S*-parameters, which utilize waves and matched terminations (normally 50 Ω). This approach also minimizes reflection problems [18]. Moreover, it has been scrutinized that short channel MOSFETs have comparatively higher channel thermal noise than long channel MOSFET devices in the strong inversion and saturation region [19–21]. This appearance is due to short channel effects (SCEs) associated with channel length modulation (CLM), velocity saturation (VS) and hot-carrier effect. As a result of accounting for these effects, it was shown that the major contribution to the drain current noise mainly comes from the linear channel region [19]. However, this issue of surplus noise is still an active area of investigation [22, 23] for RF amplifiers and receivers for communication.

In this paper, the small-signal behaviour and noise FOMs of GEWE-SiNW MOSFET is discussed at the simulation point of view. Additionally, owing to the increased demand for high-speed and low-noise devices, an accurate investigation of the MOSFET at high frequencies (HF) is necessary to represent the behaviour of device in microwave circuits and systems [24]. The complete work in this paper is systematized as follow: Sect. 2 describes the 3D device architecture of GEWE-SiNW MOSFET and its default parameters and simulation models used in this analysis. Further, we calibrate our simulation models and then evaluate the small-signal behaviour of our device in terms of scattering parameter (*S*-parameter). Further, we examine the noise analysis of *n*-channel GEWE-SiNW MOSFET at high frequency for the first time. In addition, the effect of GEWE scheme on small-signal parameters and RF FOMs also studied in this work. Finally, the conclusions are drawn in Sect. 4.

2 Device structure and physical models

Figure 1a–c shows the schematic cross-sectional view of the simulated device structure of n-type conventional, SiNW and GEWE-SiNW MOSFET, respectively. GEWE-SiNW consists of gate metals M1 and M2 of length L1 and L2 of 15 nm each, respectively, as shown in Fig. 1c which is towards the 45 nm node CMOS technology as stated in ITRS [25]. The radius of silicon nanowire is 5 nm. The oxide thickness is 1.5 nm; the source and drain region are of n-type with uniform doping profiles of 5×10^{19} cm^{-3} of length 5 nm for all device designs. The metal gate workfunction is 4.8 eV for conventional and SiNW and for GEWE, metal gate workfunction at the source end (Φ_{M1}) is 4.8 eV (Au) and metal gate workfunction at the drain end (Φ_{M2}) is 4.4 eV (Ti). All the device parameters are by default unless stated otherwise. All the simulations have been performed using physical models accounting for the electric field-dependent and concentration-dependent carrier mobilities, Shockley–Read–Hall recombination/generation with doping-dependent carrier lifetime, inversion layer Lombardi CVT mobility model, wherein concentration-dependent mobility, high field saturation model are all included [26]. To incorporate all non-local effects, we have adopted the quantum mechanical models which are more accurate than drift–diffusion method. The detailed description of default parameters used in the simulations is shown in Table 1. To characterize the device performance accurately, it is very important to define the carrier transport with proper models.

The quantum confinement effect in the deep scaled device may not be negligible [27]. Since the inversion charge layer thickness in the conducting silicon nanowire channel is comparable to the nanowire dimension, the effect of quantum confinement in sub-nanometre device may not be negligible. The Bohm quantum potential (BQP) model [28] can also be used with energy balance and hydrodynamic models, where the semi-classical potential is modified by the quantum potential in a similar way as for the continuity equations. The model introduces a position-dependent quantum potential, *Q*, which is added to the Potential Energy of a given carrier type. This quantum potential is derived using the Bohm interpretation of quantum mechanics [29] and is described below:

Time-independent Schrodinger equation can be written as:

$$\left(\frac{-\hbar}{2m^{*}}\nabla^{2} - V\phi\right)\psi_{j} = E_{j}\psi_{j} \tag{1}$$

According to Bohm's interpretation of quantum mechanics, the wave function in a polar representation can be written as:

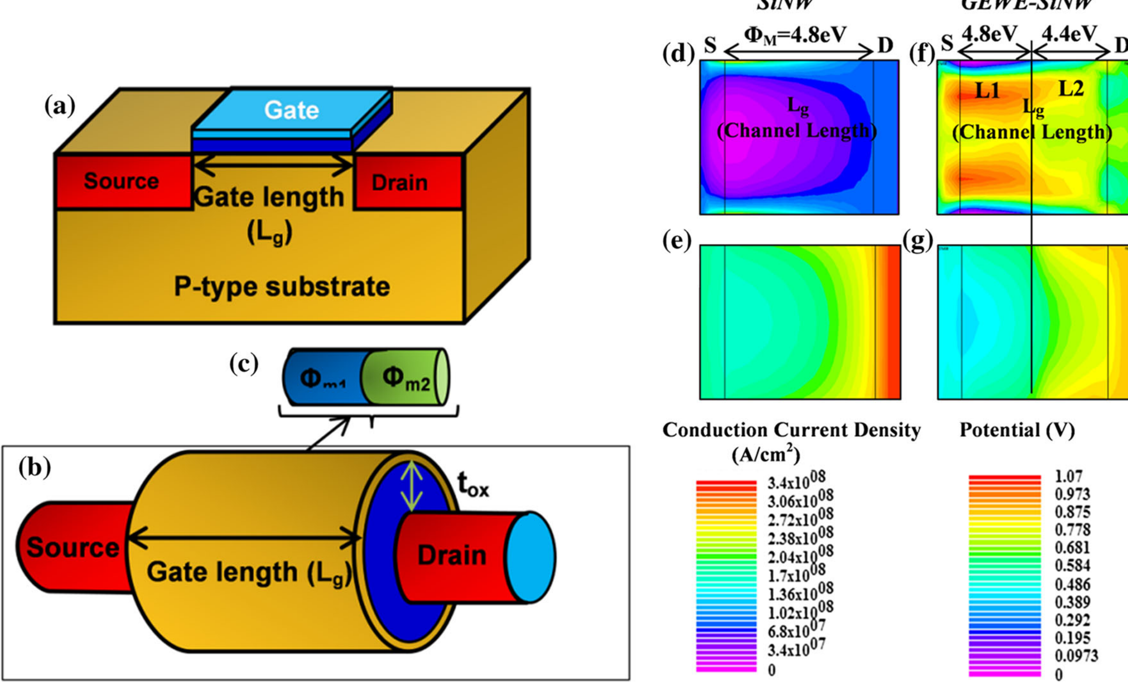


Fig. 1 Schematic cross-sectional view of **a** conventional MOSFET, **b** SiNW MOSFET and **c** GEWE-SiNW MOSFET, **d–f** contours distribution of conduction current density and **e–g** surface potential along the channel for SiNW and GEWE-SiNW MOSFET, respectively

Table 1 Physical models invoked during simulations at room temperature (300 K)

S. no.	Physical models	Description
1.	Mobility models	Lombardi CVT and constant low field mobility model
2.	Recombination model	Shockley–Read–Hall (SRH) recombination is included to incorporate minority recombination effects with carrier lifetime = 1×10^{-7} s
3.	Statistics	Boltzmann transport model, The use of Boltzmann statistics is normally justified in semiconductor device theory, but Fermi–Dirac statistics are necessary to account for certain properties of very highly doped (degenerate) materials
4.	Impact ionization and tunnelling model	No such model is used in current work as we are not interested in evaluating hot-carrier performance
5.	Energy transport model	Hydrodynamic model is used as it includes all non-local effects and is more accurate than the drift–diffusion method. Drift–diffusion model shows short comings as channel length scales down to 50 nm
6.	Quantum mechanical model	Quantum mechanical model plays an important role in determining the performance of surrounding gate MOSFET

$$\psi = R.\ \exp\left(\frac{iS}{\hbar}\right) \tag{2}$$

where R is probability density per unit volume, S has dimensions of action (energy × time).

By substituting Eq. 2 in 1, the Schrodinger equation can be written as:

$$\frac{\hbar^2}{2}\nabla\left\{M^{-1}\nabla\left[R.\exp\left(\frac{iS}{\hbar}\right)\right]\right\} + V.R\exp\left(\frac{iS}{\hbar}\right) = E.R.\exp\left(\frac{iS}{\hbar}\right) \tag{3}$$

where M^{-1} is the inverse of effective mass tensor and $M^{-1}\nabla S$ is local velocity of particle associated with wave function. Real part of Eq. 3 is interpreted as continuity equation of probability density while imaginary part states that the total energy, E is conserved and equal to sum of potential (V) and kinetic energy (0.5 $M^{-1}\nabla S$). Therefore, quantum potential is defined as:

$$V = \frac{-\hbar^2}{2}\frac{\nabla(M^{-1}\nabla R)}{R} \tag{4}$$

Potential V is obtained by the single particle Schrodinger equation and use "*mean field approximation*" and consider an effective Bohm quantum potential defined as the weighted average potential for all carriers constrained in confining potential. Effective quantum potential is written as:

$$Q_{\text{eff}} = \frac{-\hbar^2}{2}\gamma\nabla\frac{[M^{-1}\nabla(n^{\alpha})]}{n^{\alpha}} \tag{5}$$

where α and γ are two adjustable parameters, M^{-1} is the inverse effective mass tensor, n is the electron (or hole) density and h is a Planck's constant.

Bohm quantum potential (BQP) model with $\alpha = 0.5$ and $\gamma = 1.2$ was used to take quantum mechanical effects into consideration. Additionally, numerical methods such as bi-conjugate gradient stabilized (BICGST) have been considered to obtain the solutions with improved convergence in 3D device structure [26]. Default simulator coefficients for all parameters have been employed. In order to fairly analyse the device performances, all the three devices are optimized to have the same threshold voltage, i.e. 0.32 V by changing channel doping and keeping the doping of source and drain constant of uniform doping i.e. 5×19 cm^{-3}. Threshold voltage is defined as minimum gate to source voltage (V_{gs}) at which current starts flowing between source and drain or it is defined as the that voltage at which I_{on}=10^{-8} A. Figure 1d–g shows the contour plot of conduction current density and surface potential along the channel of SiNW and GEWE-SiNW, respectively. It is evident from contours that with the incorporation of GEWE scheme, conduction density of electron enhances which results in higher current driving capability in comparison with SiNW MOSFET.

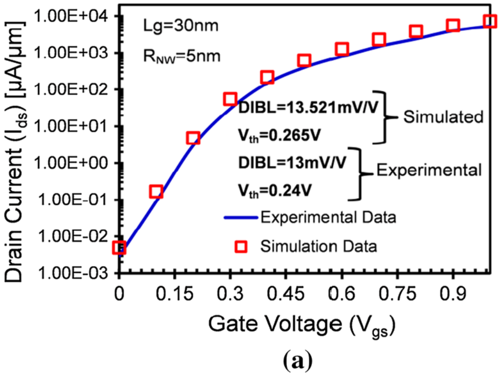
2.1 Calibration

The calibration of model parameters used in the simulation has been performed according to the experimental results [30] using above-mentioned models. Figure 2a shows the simulated I_d–V_{gs} characteristics of 30 nm short channel cylindrical gate silicon nanowire MOSFET at $V_{ds} = 1.0$ V and the transfer characteristics of extracted data of [30]. The results are in close proximity, thus validating the choice of models parameters taken in simulation. Figure 2b shows the transfer characteristics of GEWE-SiNW and SiNW MOSFET at 0.2 V drain voltage. It is evident from the figure that with the integration of gate engineering scheme, the on-current of GEWE-SiNW increases 2.2 times in comparison with silicon nanowire MOSFET due to redistribution of electric field in the channel which enhances the mobility and hence imparts the driving current capability of a device.

The MOSFET transconductance is defined by, $g_m = -\partial I_{ds}/\partial V_{gs}$ where I_{ds} drain current and V_{gs} is gate voltage. It is typically measured in the linear regime and used as indirect monitor of inversion carrier mobility. Transconductance is useful in designing linear amplifiers, and larger the transconductance for a device, the greater the gain (amplification) it is capable of delivering, when all other factors are held constant. As is evident from Fig. 2b, the transconductance is much higher in case of GEWE-SiNW MOSFET owing to enhancement in drain current. Moreover, noteworthy improvement in DIBL (or barrier lowering) is also observed in GEWE-SiNW due to step potential profile at the interface of dissimilar metal gates as is shown in contours of Fig. 1e–g. Subthreshold swing (SS) also reduces in case of GEWE-SiNW as shown in Fig. 2b and thus implies that GEWE-SiNW is immune to SCEs in comparison with SiNW MOSFET

2.2 Fabrication feasibility

The fabrication feasibility of SiNW MOSFET has been reported in the literature using several integration schemes. Yang et al. [31] fabricated vertical gate-all-around silicon nanowire MOSFET. Rustagi et al. [32] in 2007 reported the fabrication of CMOS inverter-based GAA SiNW MOSFETs using top-down approach. Moreover, for the



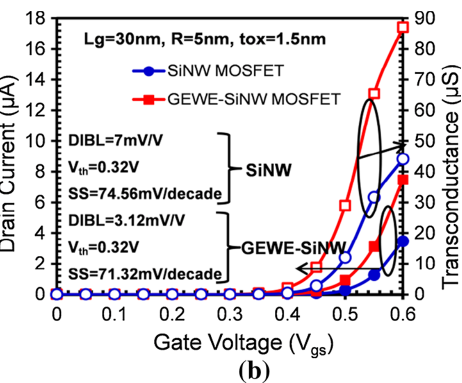
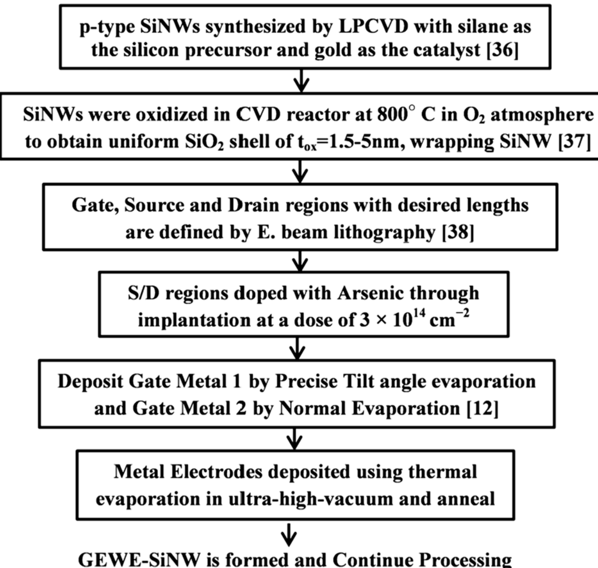


Fig. 2 **a** Calibration with the experimental results. I_{ds}–V_{gs} characteristics of 5 nm radius with 30 nm short channel cylindrical gate silicon nanowire MOSFET with $t_{ox} = 2$ nm and TiN as metal gate at $V_{ds} = 1.0$ V, **b** I_{ds}–V_{gs} and transconductance characteristics of GEWE silicon nanowire MOSFET at $V_{ds} = 0.2$ V

Table 2 Summary of the standard process flow of GEWE-SiNW



realization of GEWE architecture, numerous schemes have been suggested such as tilt angle evaporation metal gate deposition [12], metal interdiffusion process [33] and fully silicided (FUSI) metal gate [34]. Further, CMOS with dual metal gate has also been successfully fabricated using poly-Si gate doping control of the source and drain side gate individually [35]. Thus, the proposed device (GEWE-SiNW MOSFET) can be fabricated using the above design schemes, in which the advantages of GEWE scheme are amalgamated with SiNW MOSFET making it a promising design for system on chip and RF/microwave applications. A proposed summary of the process flow, outlining the fabrication process of GEWE-SiNW MOSFET and its integration with the standard CMOS process, is shown in Table 2.

3 Results and discussion

In this section, we investigate the small-signal behaviour of GEWE-SiNW MOSFET in terms of scattering (reflection and transmission coefficients) parameters. Further, the efficacy of gate metal engineering also studied on S-parameters at THz range by keeping the workfunction at the source side constant (4.8 eV) and varying the workfunction of metal gate at the drain end.

3.1 Small-signal behaviour of GEWE-SiNW MOSFET

S_{11} and S_{22} are defined as input and output reflection coefficient at port 1 and port 2, respectively, and is a measure of quality of match between the port and terminating impedance. S_{11} is the most commonly used parameter to characterize small-signal behaviour of active device at high frequency. Matching is generally required in RF circuits. When there is a perfect match, there is no reflected wave and reflection coefficient is zero. Figure 3a, b shows the real part of input and output reflection coefficient of conventional, SiNW and GEWE-SiNW MOSFET. As is evident from figure, both input and output coefficients decrease with increase in frequency and decrement in reflection coefficient is more in GEWE-SiNW as compared to its counterparts.

Due to the incorporation of two dissimilar metals on cylindrical gate, current driving capability increases due to redistribution of the electric field at the interface of two metals owing to step potential which causes enhancement in carrier velocity, and thus, current driving capability increases that results in increased transconductance and hence leading to improvement in reflection coefficient. As the matching between the ports and characteristics impedance improve, reflection coefficient decreases due to smaller reflected power. The reverse isolation parameter S_{12} determines the measure of feedback from the output of an amplifier to the input and thus supremacies its stability at high frequency [39]. Figure 3c shows the variation of real part of reverse transmission coefficient of conventional, SiNW and GEWE-SiNW MOSFET. Result unveils the reverse transmission coefficient of GEWE-SiNW increases to 5.07 and 4.2 times at 3.4 THz due to enhancement of transconductance in comparison with conventional and SiNW MOSFET, respectively. Figure 3d shows the forward transmission coefficient as a function of frequency also defined as a forward gain of two port device. The S_{21} (voltage gain) increases to 7.14 times in SiNW and 13.5 times in GEWE-SiNW MOSFET compared to conventional MOSFET as depicted in Fig. 3d. This enhancement is due to cylindrical gate designs and GEWE engineering scheme which enhances device performance and alleviates SCEs.

Further, we investigate the effect of metal gate workfunction on small-signal behaviour of GEWE-SiNW MOSFET at THz frequency range. Figure 4a, b shows the input and output reflection coefficient at different metal gate workfunction of drain end. As is evident from Fig. 4a, the effect of workfunction difference is very less on input reflection coefficient and also its value increases with increase in workfunction difference which is not desirable. Further, output reflection coefficient decreases with increase in workfunction difference which is desirable for RF amplifiers and receivers. This is due to excellent gate control which results in higher transconductance and hence improves reflection coefficient. As we increase the metal gate workfunction difference to 0.7 eV, reverse

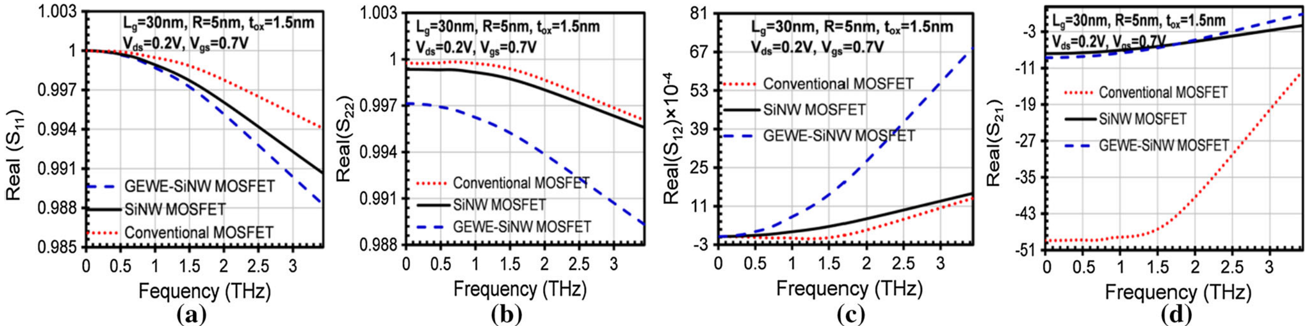


Fig. 3 **a–b** Real part of input output reflection coefficient, **c–d** real part of reverse and forward transmission coefficient as a function of frequency for conventional, SiNW and GEWE-SiNW MOSFET at $V_{gs} = 0.7$ V and $V_{ds} = 0.2$ V

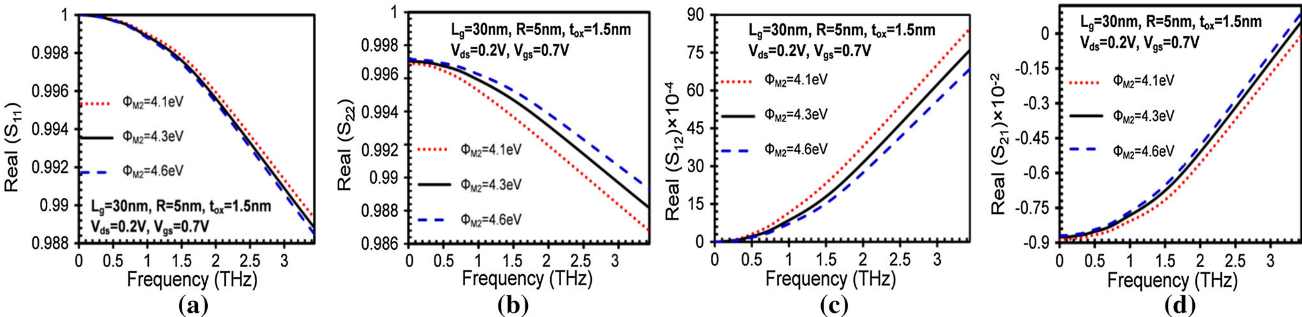


Fig. 4 **a–b** Real part of input and output reflection coefficient, **c–d** real part of reverse and forward transmission coefficient as a function of frequency for different metal gate workfunction at the drain side at $V_{gs} = 0.7$ V and $V_{ds} = 0.2$ V

transmission coefficients increase to 1.25 times at 3.4 THz compared to other workfunction difference due to improvement in on-current and reduced short channel effects owing to improvement of screening effect with an increase in metal workfunction difference as is evident from Fig. 4c, whereas forward transmission coefficient decreases as we increase the workfunction difference which is not desirable at THz. But the deprivation is very less as is shown in Fig. 4d. Thus, there is need to optimize the value of metal gate workfunction for optimal small-signal performance for RF amplifier and high-speed applications.

3.2 Noise metrics

For the design of CMOS RF circuits, investigation of noise conductance and noise figure (NF) is of paramount importance at high frequency. The effectiveness of low-noise amplifier (LNA) is determined by an important metric called noise figure. Noise conductance is generally used to estimate the power spectral density of noise current generators. Low-noise conductance is required in RF amplifiers and LNAs. Figure 5a depicts the noise conductance as a function of frequency for conventional, SiNW, GEWE-SiNW MOSFET. In GEWE-SiNW MOSFET, noise conductance decreases due to reduced hot-carrier phenomenon which results in lower impact ionization of carriers at the Si–SiO_2 interface and thus reduces noise. Additionally, as silicon nanowire phonon–phonon scattering is less observed, noise conductance also decreases. Hence, its dominance, for low-power and low-noise applications where noise is a major concern, is significant. Noise figure is an estimation of deterioration of signal-to-noise ratio caused by a component in RF signal chains. It is generally used to evaluate the performance of an amplifier or a radio receiver, with lower values specifying better performance.

Figure 5b shows the variation of NF_{MIN} as a function of frequency. As is evident from the figure, minimum noise figure decreases with increase in frequency, but this decline is more prominent in GEWE-SiNW MOSFET. The minimum noise figure is proportional to intrinsic gate resistance and inversely proportional to transconductance [40]. In GEWE-SiNW, there is a step potential created at the interface of two dissimilar metals workfunction which redistributes the electric field in the channel and hence increases the carrier efficiency which results in improved transconductance and low noise figure in comparison with its conventional counterparts. A low noise figure reflects that a very little noise is being added by the network. Thus,

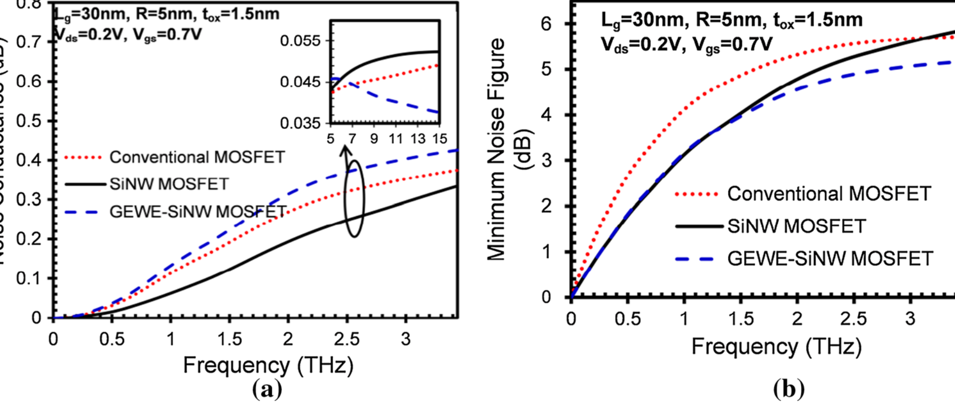


Fig. 5 **a** Noise conductance and **b** minimum noise figure as a function of frequency for conventional, SiNW and GEWE-SiNW MOSFET at $V_{gs} = 0.7$ V and $V_{ds} = 0.2$, respectively

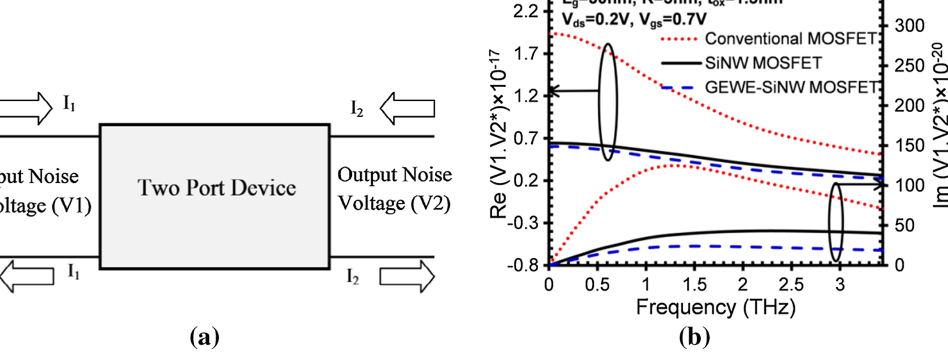


Fig. 6 **a** MOSFET as a two port device where the input noise is replaced by a voltage V1 and the noise received at output is replaced by V_2, **b** cross-correlation as a function of frequency for conventional, SiNW and GEWE-SiNW MOSFET at $V_{gs} = 0.7$ V and $V_{ds} = 0.2$ V

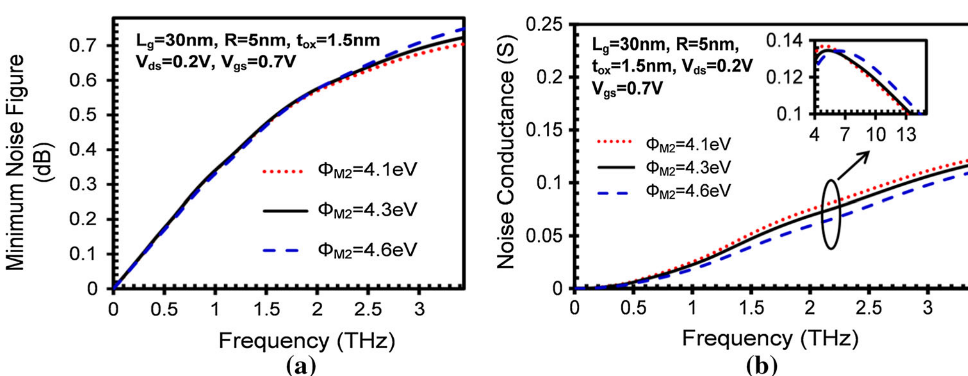


Fig. 7 **a** Minimum noise figure and **b** noise conductance as a function of frequency for GEWE-SiNW MOSFET for different gate metal workfunction values at drain end

GEWE-SiNW MOSFET is a reliable candidate for low-noise amplifiers (LNAs).

Figure 6a depicts MOSFET as a two port device where noise induced at the gate terminal is separated from the MOSFET and is depicted by V1 and the noise received at the output is depicted by V2 [41]. Figure 6b shows that real and imaginary part of cross-correlation is reduced in comparison with conventional devices with change in frequency. Since, with the incorporation of GEWE scheme, electric field reduces at the drain end, less isotropic scattering is observed. Due to this reduced isotropic scattering, the scattering mechanism is not so effective in breaking the correlation between gate current and drain current [41]. Thus, cross-correlation (i.e. V1.V2*) reduces in GEWE-SiNW MOSFET at higher frequencies.

Moreover, the noise performance of GEWE-SiNW MOSFET further enhanced by tuning the workfunction difference by keeping the workfunction at the source side constant and varying the workfunction at the drain end. As we increase the workfunction difference to 0.7 eV, minimum noise figure decreases in comparison with 0.2 eV as is evident from Fig. 7a. It is very clear that change is observable at very high frequency (around 2.5–3 THz); around 7.82 % decrement is observed when workfunction

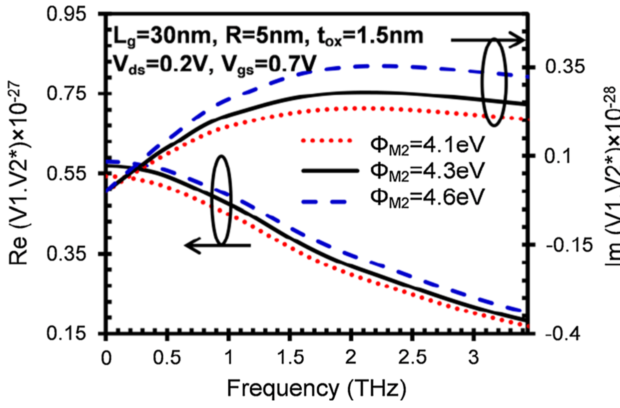


Fig. 8 Cross-correlation as a function of frequency for GEWE-SiNW MOSFET for different gate metal workfunction values at drain end

at the drain end is 4.1 eV owing to enhancement in transconductance and carrier transport efficiency. Moreover, noise conductance also decreases with increase in workfunction difference but more prominent at high frequency as is evident from the inset of Fig. 7b. Therefore, noise FOMs are not affected much with change in workfunction difference. Another parameter which decides the noise performance of a device is cross-correlation factor. Figure 8 shows the cross-correlation factor of GEWE-SiNW MOSFET of different metal gate workfunction at drain end and the result shows that with workfunction 4.1 eV, electric field reduces at the drain end which results in less scattering of carriers, and thus, correlation between input and output is less observed which is desirable for RF communication.

4 Conclusion

In this paper, a comprehensive small-signal behaviour and noise analysis of GEWE-SiNW MOSFET is explained in terms of *S*-parameters and noise FOMs at THz frequency range. The simulation results obtained shows that with the incorporation of GEWE scheme into SiNW, reflection coefficient decreases and transmission coefficient increases in comparison with SiNW and conventional MOSFET. Prominent reduction in noise metrics such as minimum noise figure, noise conductance and cross-correlation of GEWE-SiNW MOSFET in comparison to SiNW and Conventional MOSFET. This makes GEWE-SiNW MOSFET appropriate for microwave amplifier and oscillator designs. Moreover, tuning of gate workfunction difference noise metrics improves due to reduction in SCEs and improvement in transconductance, whereas forward gain degrades. Thus, we have to choose the optimum value of gate metal workfunction for better device performance at HF communication circuits and LNAs.

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References

1. C. Enz, An MOS transistor model for RF IC design valid in all regions of operation. IEEE Trans. Microw. Theory Tech. **50**(1), 342–359 (2002)
2. Q. B. Chen, Compact modeling of multi-gate MOSFETs for RF designs. in *IEEE International Wireless Symposium (IWS)*, pp. 1–4 (2013). doi:10.1109/IEEE-IWS.2013.6616743
3. ITRS, International Technology Roadmap for Semiconductors (2011)
4. A. Kumar, N. Gupta, R. Chaujar, Analysis of novel transparent gate recessed channel (TGRC) MOSFET for improved analog behaviour. Microsyst. Technol. **21**(5) (2015). doi:10.1007/s00542-015-2554-z
5. A. Kumar, N. Gupta, R. Chaujar, Novel design: transparent gate recessed channel (TGRC) MOSFET for improved reliability applications. in *IEEE 1st International Conference on Microelectronics, Circuits and Systems*, pp. 1–5 (2014)
6. A. Kumar, R. Chaujar, Monica, Thermal behavior of novel transparent gate recessed channel (TGRC) MOSFET: TCAD analysis. in *Tech-Connect World Innovation Conference & Expo* (2014)
7. H. Iwai, Roadmap for 22 nm and beyond (Invited Paper). Microelectron. Eng. **86**, 1520–1528 (2009)
8. D. W. Kim et al., Fabrication and electrical characteristics of self-aligned (SA) gate-all-around (GAA) Si nanowire MOSFETs (SNWFET). in IEEE International Conference on IC Design and Technology (ICICDT), pp. 63–66 (2010)
9. R. Wang et al., Analog/RF performance of Si nanowire MOSFETs and the impact of process variation. IEEE Trans. Electron Devices **54**(6), 1288–1294 (2007)
10. A. Sarkar, S. De, A. Dey, C.K. Sarkar, Analog and RF performance investigation of cylindrical surrounding-gate MOSFET with an analytical pseudo-2D model. J. Comput. Electron. **11**(2), 182–195 (2012)
11. S. Cho, K.R. Kim, B.G. Park, I.M. Kang, RF performance and small-signal parameter extraction of Junctionless silicon nanowire MOSFETs. IEEE Trans. Electron Devices **58**(5), 1388–1396 (2011)
12. W. Long, H. Ou, J.M. Kuo, K.K. Chin, Dual-material gate (DMG) field effect transistor. IEEE Trans. Electron. Devices **46**(5), 865–870 (1999)
13. C. Y. Zheng, The using of dual-material gate MOSFET in suppressing short-channel effects: a review. in IEEE International Conference on Electronics, Communications and Control (ICECC), pp. 2979–2982 (2011)
14. N. Gupta, A. Kumar, R. Chaujar, Oxide bound impact on hot-carrier degradation for gate electrode workfunction engineered (GEWE) silicon nanowire MOSFET, Microsyst. Technol. 1–10 (2015). doi:10.1007/s00542-015-2557-9
15. N. Gupta, R. Chaujar, Implications of transport models on the analog performance of gate electrode workfunction engineered (GEWE) SiNW MOSFET. in IEEE 2nd International Conference on Devices, Circuits and Systems (ICDCS), pp. 1–5 (2014)
16. N. Gupta, A. Kumar, R. Chaujar, Impact of device parameter Variation on RF performance of gate electrode workfunction engineered (GEWE)-silicon nanowire (SiNW) MOSFET. J. Comput. Electron. **14**(3), 798–810 (2015)

17. N. Gupta, A. Kumar, R. Chaujar, Investigation of frequency dependent Parameter of GEWE-SINW MOSFET for microwave and RF applications. Int. J. Adv. Technol. Eng. Sci. **2**(1), 35–40 (2015)
18. J.J. Liou, F. Schwierz, RF MOSFET: recent advances, current status and future trends. Solid-State Electron. **47**(11), 1881–1885 (2003)
19. C.H. Chen, M.J. Deen, Channel noise modeling of deep submicron MOSFETs. IEEE Trans. Electron Devices **49**(8), 1484–1487 (2009)
20. S. Asgaran, M.J. Deen, C.H. Chen, Analytical modeling of MOSFETs channel noise and noise parameters. IEEE Trans. Electron Devices **51**(12), 2109–2114 (2004)
21. K. Han, H. Shin, K. Lee, analytical drain thermal noise current model valid for deep submicron MOSFETs. IEEE Trans. Electron Devices **51**(2), 261–269 (2004)
22. Y. Tsividis, C. McAndrew, *Operation and Modeling of the MOS Transistor*, 3rd edn. (Oxford University Press, Oxford, 2013)
23. S.D. Yu, A unified channel thermal noise model for short channel MOS transistors. J. Semicond. Technol. Sci. **13**(3), 213–223 (2013)
24. C.H. Doan, S. Emami, S.M. Niknejad, R.W. Brodersen, Millimeter-wave CMOS design. IEEE J. Solid-State Circuits **40**(1), 144–155 (2005)
25. C. Hu, *Modern Semiconductor Device for Integrated Circuit* (Prentice Hall, Upper Saddle River, 2009), pp. 261–274
26. ATLAS User's Manual (SILVACO Int., Santa Clara, 2014)
27. A. Chaudhry, J.N. Roy, Mosfet models, quantum mechanical effects and modeling approaches: a review. J. Semicond. Technol. Sci. **10**, 20–27 (2010)
28. V. S. Patnaik, A. Gheedia, M. J. Kumar, 3D simulation of nanowire FETs using quantum models (2008)
29. G. Iannaccone, G. Curatola, G. Fiori, Effective Bohm Quantum Potential for device simulators based on drift-diffusion and energy transport. in *Simulation of semiconductor processes and devices (SISPAD)*, pp. 275–278 (2004)
30. S. D. Suk et al, High performance 5 nm radius twin silicon nanowire MOSFET (TSNWFET): fabrication on bulk Si wafer, characteristics, and reliability. in *IEEE International Electron Devices Meeting Technical Digest*, pp. 717–720 (2005). doi:10.1109/IEDM.2005.1609453
31. B. Yang, K.D. Buddharaju, S.H.G. Teo, N. Singh, G.Q. Lo, D.L. Kwong, Vertical silicon-nanowire formation and gate-all around MOSFET. IEEE Electron Device Lett. **29**(7), 791–794 (2008)
32. S.C. Rustagi et al., CMOS inverter based on gate-all-around silicon-nanowire MOSFETs fabricated using top-down approach. IEEE Electron Device Lett. **28**(11), 1021–1024 (2007)
33. I. Polishchuk, P. Ranade, T.J. King, C. Hu, Dual work function metal gate CMOS technology using metal interdiffusion. IEEE Electron Device Lett. **22**(9), 444–446 (2001)
34. J. Liu, H.C. Wen, J.P. Lu, D.L. Kwong, Dual-work-function metal gates by full silicidation of Poly-Si with Co-Ni bi-layers. IEEE Electron Device Lett. **26**(4), 228–230 (2005)
35. K.Y. Na, Y.S. Kim, Silicon complementary metal-oxide semiconductor field-effect transistors with dual work function gate. Jpn. J. Appl. Phys. **45**(12), 9033–9036 (2006)
36. O. Shirak, O. Shtempluck, V. Kotchtakov, G. Bahir, Y.E. Yaish, High performance horizontal gate-all-around silicon nanowire field-effect transistors. Nanotechnology **23**, 395202 (2012)
37. D. Moon, S.-J. Choi, J.P. Duarte, Y.-K. Choi, Investigation of silicon nanowire gate-all-around junctionless transistors built on a bulk substrate. IEEE Trans. Electron Devices **60**, 1355–1360 (2013)
38. J.-H. Lee, B.-S. Kim, S.-H. Choi, Y. Jang, S.W. Hwangc, D. Whang, A facile route to Si nanowire gate-all-around field effect transistors with a steep subthreshold slope. Nanoscale **5**, 8968–8972 (2013)
39. L. Belostotski, J.W. Haslett, Two-port noise figure optimization of source-degenerated cascade CMOS LNAs. Analog Integr. Circ. Sig. Process **55**(2), 125–137 (2008)
40. M. Golio, *Microwave and RF product applications*, 1st edn. (CRC-Press, Boca Raton, 2003)
41. D.M. Pozar, *Microwave engineering*, 4th edn. (Wiley, New York, 2012)

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Impact of device parameter variation on RF performance of gate electrode workfunction engineered (GEWE)-silicon nanowire (SiNW) MOSFET

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Abstract In this paper, we explore the quantitative investigation of the high-frequency performance of gate electrode workfunction engineered (GEWE) silicon nanowire (SiNW) MOSFET and compared with silicon nanowire MOSFET(SiNW MOSFET) using device simulators: ATLAS and DEVEDIT 3D. Simulation results demonstrate the improved RF performance exhibited by GEWE-SiNW MOSFET over SiNW MOSFET in terms of transconductance (g_m), cut-off frequency (f_T), maximum oscillator frequency (f_{MAX}), power gains (Gma, G_{MT}) parasitic capacitances, stern's stability factor and intrinsic delay. Further, using three-dimensional device simulations, we have also examined the efficacy of parameter variations in terms of oxide thickness, radius of silicon nanowire, channel length and gate metal workfunction engineering on RF/microwave figure of merits of GEWE-SiNW MOSFET. Simulation result reveals significant enhancement in f_T and f_{MAX}; and a reduction in switching time in GEWE-SiNW MOSFET due to alleviated short channel effects, improved drain current and smaller parasitic capacitance, thus providing detailed knowledge about the device's RF performance at such aggressively scaled dimensions.

Keywords Power gains · GEWE · RF · Silicon nanowire MOSFET · Parasitic capacitance · f_T and f_{MAX}

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1 Introduction

Silicon based transistors have become an appealing low cost solution for many low power and high frequency applications such as mobile telecommunication. The relentless scaling of CMOS toward nanometer-scale gate lengths has produced MOSFETs with digital and RF performance that is suitable for mixed signal applications [1–4]. However, scaling down arises the so-called SCEs such as mobility degradation, hot carrier effects, drain induced barrier lowering, parasitic capacitances etc. making the scaled devices inapt for RF/wireless applications [5]. To surpass these hindrances, new device architectures with 3-D gate structures have been intensively studied. Among them, cylindrical gate MOSFET [6] has emerged as a most promising candidate in recent years. Recently, many theoretical and experimental studies on cylindrical gate MOSFET have been reported in literature to eliminate SCEs, to achieve high transconductance and nearly ideal subthreshold slope (60 mV/decade) [7,8]. It allows excellent electrostatic control of the gate over the channel hence overcoming the scaling limitations caused due to the SCEs, thereby improving the device performance. Further, Silicon nanowire emerged as a most promising in electronic devices due to the fact that its properties such as concentration, dopant type can be changed during synthesis. Also, its mobility is higher than bulk silicon due to stronger quantum confinement. The body thickness (diameter) of the nanowire can readily be reduced to a few nanometers in size scale that is challenging to obtain using bulk silicon. Therefore, to get further improvement against SCEs the concept of silicon nanowire MOSFET was put forward by Cui et al. [9] in 2003 concluded that silicon nanowires MOSFET as building blocks for future nano-electronics. Also, the small volume and low leakage current of nanowire MOSFETs make them attractive for high density memory arrays

and logic chips [10,11]. Yang et al. [12] fabricated vertical gate-all-around silicon nanowire MOSFET and showed excellent transistor characteristics compared to conventional devices. Also it was proven that it has a merit of outstanding maximum oscillation frequency (f_{MAX}) [13].

In 1989, Shur introduced the notion of split gate which escalate the carrier transport efficiency of device [14]. But the misalignment of two gates during fabrication and fringing capacitances between the gates limits the device speed. Hence, to overcome this drawback, gate electrode workfunction engineering scheme was proposed by Zhou and Long [15] in 1999. With this scheme, there is appreciable reduction in the SCEs, improvement in current capabilities due to two dissimilar metal gates and reduction in electric field at the drain end thus providing hot-carrier reliability [16]. Pal et al. [17] reported a 2-D analytical drain current model of DMG-GAA MOSFET which employs gate material engineering scheme to reduce SCEs. To incorporate the advantage of gate electrode engineering scheme, combined with silicon nanowire MOSFET, a novel device structure called gate electrode workfunction engineered (GEWE) silicon nanowire (SiNW) MOSFET is proposed [18]. Recently, we have reported the hot-carrier performance and [19] and analog behaviour of GEWE-SiNW MOSFET [20].

However, the reported work mentioned above not discuss about the Quantum RF behaviour of GEWE-SiNW MOSFET and the impact of device parameter variation especially radius, length and oxide thickness. Moreover, due to the increased demand for high-speed electronics products, the accurate analysis of MOSFET at high frequencies (HF) is necessary to represent the behavior of device in microwave circuits and systems [21]. Therefore, in this paper, for the first time we carried out the quantum 3D-numerical simulation of GEWE-SiNW MOSFET in terms of RF FOMs to study the effect of HF (GHz) on the performance of GEWE-SiNW MOSFET and simulations results so obtained are compared with the conventional SiNW MOSFET. Further, Sect. 2 describes the device structure and its default parameters followed by simulation methodology. Section 3 contains the results obtained by device variation and also explores the dependency of GEWE-SiNW MOSFET's performance on metal workfunction at the drain end, gate oxide thickness, channel length and radius of silicon nanowire which would be indispensable for optimizing the device designs at millimeter range frequency.

2 Device structure and its description

Figure 1a, b shows the simulated device structure of SiNW MOSFET and GEWE SiNW MOSFET respectively. All simulations have been performed using ATLAS and DEVEDIT 3D device simulator. The Source/Drain region is highly

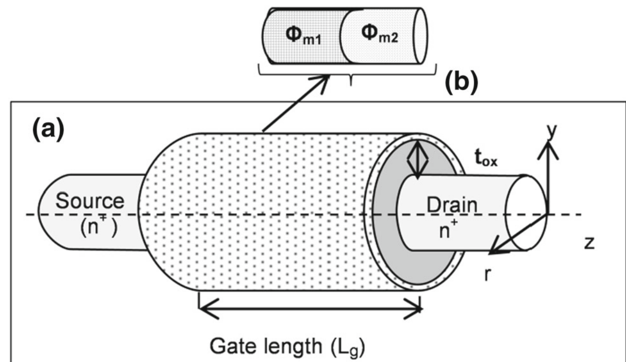


Fig. 1 Schematic cross-sectional view of **a** SiNW MOSFET and **b** GEWE-SiNW MOSFET

doped with n-type impurity of a length of 5 nm. The silicon nanowire is doped with a p-type impurity and t_{ox} thick oxide layer is embodied in it as shown in Fig. 1. In order to fairly analyze the device performances, both the devices are optimized to have the same threshold voltage, i.e., 0.4 V. In this simulation, all the junctions of the structure are assumed to be abrupt and the biasing conditions are considered at room temperature (T = 300 K) with the doping profiles being uniform. The detailed description of default parameters used in the simulations is shown in Table 1. Further, two numerical techniques Gummel and Newton have been considered to obtain the solutions [22]. To obtain the convergence in the inversion region, the DIRECT parameter is added for more robust solution.

2.1 Simulation methodology and calibration

All the simulations have been performed using following models as shown in Table 2.

It is important to define the carrier transport with proper models to characterize the device performance accurately. The most popular one is drift-diffusion (DD) model, which is widely used in engineering field. For deep submicron device simulation, the hydrodynamic transport model is commonly used to examine in detail the carrier energy in the carrier transport. It is argued that hydrodynamic model produces the carrier velocity overshoot even in the ballistic regime, which overestimates the drain current level [23]. Furthermore, the quantum confinement effect in the deep scaled device may not be negligible [24]. This is because the inversion charge layer thickness in the conducting silicon nanowire channel is comparable to the nanowire dimension. Therefore, the quantization effect model is included in the device simulation. Bohr Quantum Potential (BQP) Model [25] with alpha = 0.5 and gamma = 1.2 was used to take quantum mechanical effects into consideration.

The calibration of model parameters used in simulation has been performed according to the published results

Table 1 Default design parameters used in the analysis

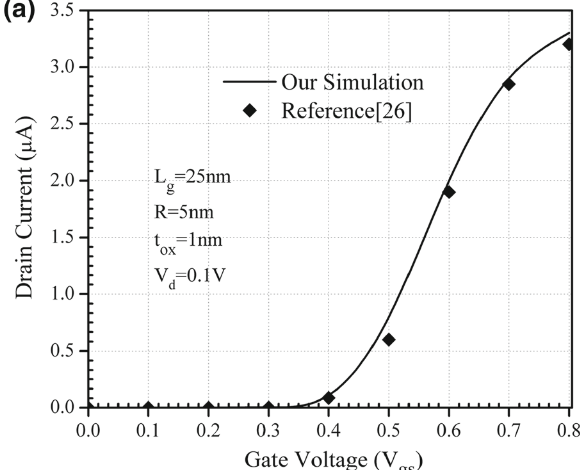
Design parameters of SiNW and GEWE-SiNW MOSFET device design	
Channel length (L_g)	30 nm
Substrate doping (N_A)	1×10^{16} cm^{-3}
Radius of Nanowire (R)	5 nm
Source/drain doping (N_D^+)	1×10^{19} cm^{-3}
Physical oxide thickness (t_{ox})	1.5 nm
Permittivity of SiO_2 (ε_{ox})	3.9
Gate to source voltage (V_{gs})	0.7 V
Drain to source voltage (V_{ds})	0.2 V
Work function for SiNW-MOSET (Φ_m)	4.8 eV
Work function for GEWE-SiNW MOSFET	$\Phi_{m1} = 4.8$ eV (Gold)
	$\Phi_{m2} = 4.4$ eV (Titanium)

The design parameters as discussed above are the default parameters used in the analysis, unless otherwise stated

Table 2 Simulations model

S. No.	Physical models	Description
1.	Mobility models	*Lombardi CVT and Constant Low Field Mobility Model*
2.	Recombination model	*Shockley Read Hall (SRH)* Recombination is included to incorporate minority recombination effects with carrier lifetime = 1×10^7 s
3.	Statistics	*Boltzmann Transport model*, The use of Boltzmann statistics is normally justified in semiconductor device theory, but Fermi-Dirac statistics are necessary to account for certain properties of very highly doped (degenerate) materials
4.	Impact ionization and tunneling model	No such model is used in current work as we are not interested in evaluating hot-carrier performance
5.	Energy transport model	*Hydrodynamic Model* is used as it includes all nonlocal effects and is more accurate than the drift-diffusion method [22]. Drift diffusion Model show short comings as channel length scales down to 50 nm
6.	Quantum mechanical model	*Quantum Mechanical Model* plays an important role in determining the performance of surrounding gate MOSFET In this paper we take into account QMEs

obtained by Gnani et al. [26], using above models and calibrated results are shown in Fig. 2a in order to validate the simulations. Figure 2b shows the drain current and gate transconductance characteristics of GEWE-SiNW MOSFET at drain bias 0.2 V. As it is shown in Fig. 2b, the current driving capability of nano-scale GEWE-SiNW MOSFET is enhanced by 20 % in comparison to SiNW MOSFET. This enhancement



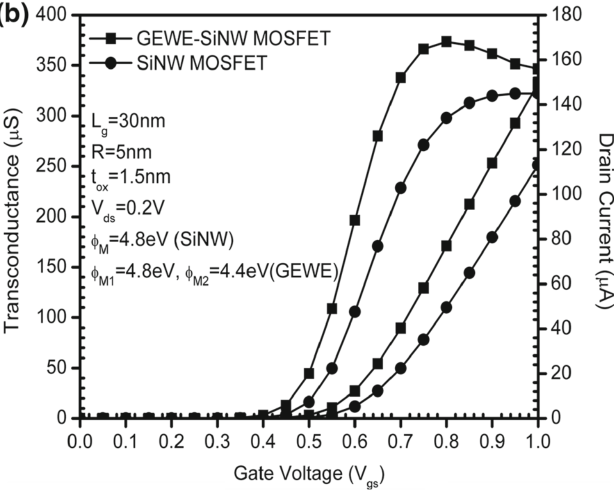


Fig. 2 **a** Calibration with the published result, $I_{ds} - V_{gs}$ characteristics of silicon nanowire MOSFET, **b** transfer and transconductance characteristics of silicon nanowire and GEWE-silicon nanowire MOSFET at $V_{ds} = 0.2$ V respectively

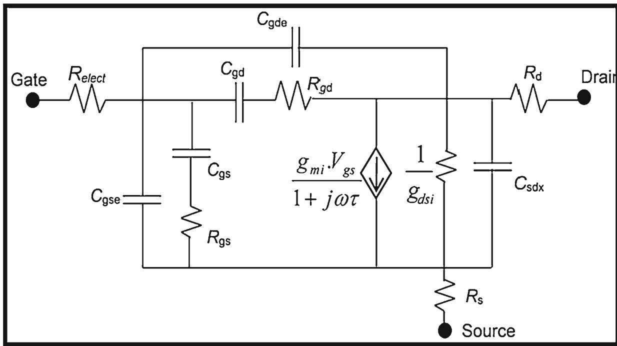


Fig. 3 Non-quasi-static (NQS) equivalent circuit model of SiNW MOSFET at RF region operating in the strong inversion region

is due to incorporation of gate-metal engineering scheme which causes gradual step change of surface potential at the interface of two metals and hence increases gate efficiency of device. The MOSFET transconductance ($g_m = \partial I_{ds}/\partial V_{gs}$) is typically measured in the linear regime and is used as an indirect monitor of inversion carrier mobility. Transconductance is useful in designing linear amplifiers and does not have any significance in switching power supplies. In general, the larger the transconductance of a device, the greater the gain (amplification) it is capable of delivering, when all other factors are held constant. It is clearly evident from Fig. 2b that transconductance of GEWE-SiNW is higher in comparison to conventional SiNW MOSFET due to enhanced on-current. Also, significant enhancement in g_m of our device is obtained as compared to previously reported work [27].

3 RF performance metrics inquisition

In deep sub micrometer regime, it is very challenging to design RF devices for ultra-low power applications due to aggressive scaling of MOSFETs. In this section, we investigate the comparison of conventional SiNW and our device in which we incorporated GEWE scheme onto conventional SiNW MOSFETs to examine the efficacy of high frequency in terms of RF metrics. Further, the impact of device parameters variation of GEWE-SiNW MOSFET on the same has been studied.

Figure 3 shows the non-quasi-static equivalent circuit of a MOSFET to extract small signal parameters of GEWE-SiNW MOSFET and conventional silicon nanowire MOSFET that is based on conventional MOSFET's small signal microwave modeling. Here, R_s and R_d are source and drain resistances respectively. R_{gs} and R_{gd} are distributed channel resistance and C_{gde} and C_{gse} are extrinsic gate-to-drain and gate-to-source capacitances respectively. g_{dsi} and g_{mi} are intrinsic gate-to-drain conductance and transconductance. C_{ds} and C_{gs} are intrinsic gate-to-drain and gate-to-source capacitances respectively [28]. The capacitances between each pair of electrodes are calculated through AC small signal analysis after post processing operation of DC solution.

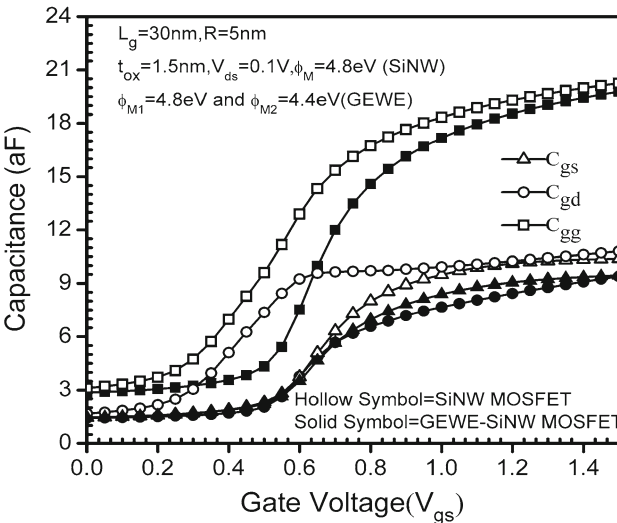


Fig. 4 Intrinsic capacitances of SiNW MOSFET and GEWE-SiNW MOSFET as a function of Vgs

Parasitic capacitance in RF amplifiers may cause these amplifiers to have low gain due to parasitic loss. In some cases, it may cause these amplifiers to oscillate. In digital switching circuits, the rise time and fall time of the digital signal greatly affect the maximum speeds achievable [29]. The intrinsic parasitic capacitances are extracted from small signal analysis after post processing operation of DC solution at an operating frequency of 1 MHz. The parasitic capacitance on the inputs and outputs of the digital devices increases the rise and fall times. Thus, it is required to investigate the parasitic capacitances at high frequency. Figure 4 shows the variation of bias-dependent parasitic capacitances such as gate–source (C_{gs}), gate–drain (C_{gd}) and gate-gate (C_{gg}) capacitance as a function of gate voltage for GEWE-SiNW MOSFET and SiNW MOSFET. The capacitance value changes depending on the voltage that appears across the drain source and also across the gate source of the device. It is evident from Fig. 4 that GEWE-SiNW exhibits smaller C_{gs}, C_{gd} in comparison to its conventional SiNW MOSFET due to metal gate workfunction difference which results in improved screening of conducting channel from drain bias variations. A similar kind of behaviour is also observed in Ref. [30].

A parameter generally described when comparing transistors for RF applications is the cut-off frequency, f_T [31,32]. f_T is a specification for high-speed digital applications (speed and high swing) and can be defined as follow:

$$f_T = \frac{g_m}{2\pi\left(C_{gs}+C_{gd}\right)} \tag{1}$$

where g_m is the transconductance, C_{gs} and C_{gd} are parasitic capacitances.

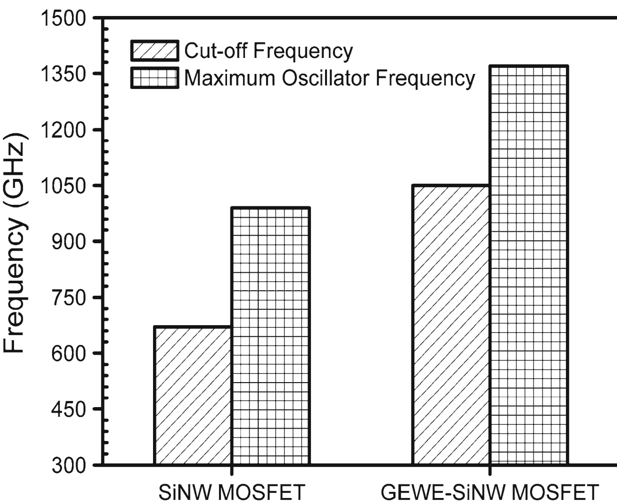


Fig. 5 Cut-off and maximum oscillator frequency of SiNW MOSFET and GEWE-SiNW MOSFET at $V_{gs} = 0.7$ V and $V_{ds} = 0.2$ V

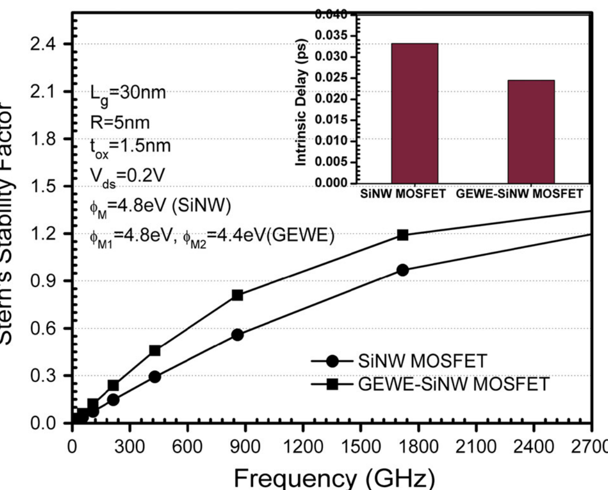


Fig. 6 Stern's stability factor of SiNW and GEWE-silicon nanowire MOSFET. *Inset* intrinsic delay of SiNW and GEWE-silicon nanowire MOSFET at $V_{ds} = 0.2$ V

Also, the incorporation of GEWE design enhances the carrier mobility of a device, leading to increase in cut-off frequency as is evident from Fig. 5. For characterizing a device for tuned RF amplifiers and oscillators, maximum oscillation frequency is an important parameter to consider. f_{MAX} is the maximum oscillation frequency which is defined as the frequency where the maximum unilateral power gain falls to unity (0 dB) [33].

$$f_{MAX} = \frac{f_T}{\sqrt{4R_g\left(g_{ds} + 2\pi f_T C_{gd}\right)}} \tag{2}$$

Further, f_{MAX}, as is seen from Fig. 5, is higher for GEWE-SiNW MOSFET than SiNW MOSFET, which is due to higher parasitic capacitance in the conventional SiNW MOSFET, thereby giving the GEWE-SiNW design a new strength for switching applications and wireless communication.

Intrinsic Delay is another important measure for switching application. The increasing capacitance between the gate and the overlapped S/D region deteriorates the intrinsic gate delay [34]. Intrinsic delay metric is defined as:

$$\tau = \frac{C_{gg}.V_d}{I_{ON}} \tag{3}$$

where C_{gg} is the parasitic gate capacitance, V_d is the bias voltage applied to drain and I_{ON} is the on-current.

Inset of Fig. 6 shows the comparison of GEWE-SiNW with SiNW MOSFET in terms of intrinsic delay parameter. As is evident from the figure, there is notable reduction in intrinsic delay of GEWE-SiNW MOSFET than its conventional counterpart due to incorporation of two dissimilar metal gates and cylindrical silicon nanowire which increases on-current, reduces parasitic capacitances and which leads to considerable reduction of intrinsic delay. Power gains play an important role in designing RF amplifiers. For low noise amplifier (LNA) design, maximum available power gain and stability are two important criterions. Stability measures the ability of LNA to oscillate at high frequencies. When designing an amplifier for RF frequency range, our aim is to get void of any oscillations. The standard way to scrutinize stability is by so-called stern stability factor. The stern's stability factor (K) is usually less than 1 at low frequency and greater than 1 at high frequency [35,36]. The factor K is defined as in the following equation:

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2.\,|S_{12.} \cdot S_{21}|} \tag{4a}$$

where, S_{11} and S_{22} are the reflection coefficients and S_{12} and S_{21} are transmission coefficients and s-matrix Δ is defined as

$$\Delta = S_{11} \times S_{22} - S_{12} \times S_{21} \tag{4b}$$

Figure 6 shows the variation of stability factor as a function of frequency. As is clear from the figure, at high frequency K is significantly higher for GEWE-SiNW in comparison to SiNW MOSFET. This is due to increased gate control, which causes maximum power transfer from source to load. Figure 7 shows the improvement of HF maximum available power gain (Gma) of GEWE-SiNW MOSFET over SiNW MOSFET. This is due to better gate controllability and higher silicon nanowire mobility which results in enhanced transconductance and reduced parasitic capacitances. Also, Maximum transducer power gain (G_{MT}) of a two port network is defined as the ratio of average power delivered to the load by a source to a maximum available power from the

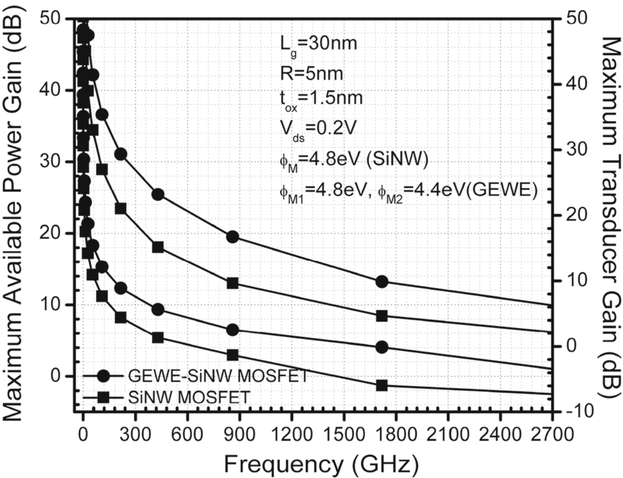


Fig. 7 Maximum available power gain and maximum transducer power gain of SiNW and GEWE-silicon nanowire MOSFET at V_{ds} = 0.2 V and V_{gs} = 1.0 V

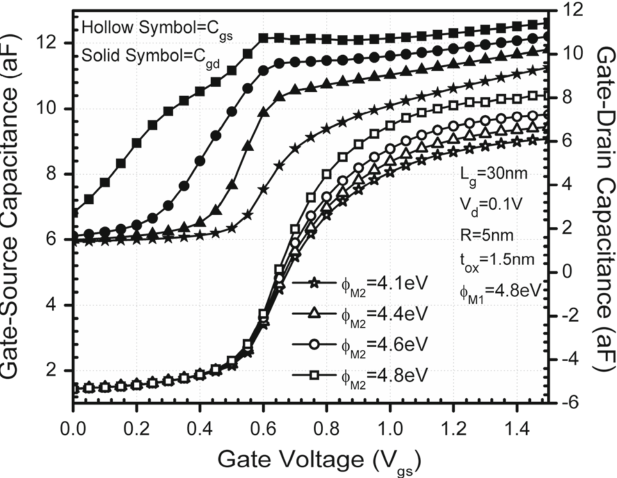


Fig. 9 Gate-source and gate-drain capacitance of GEWE-silicon nanowire MOSFET as a function of gate voltage for various metal workfunction values at V_{ds} = 0.2 V

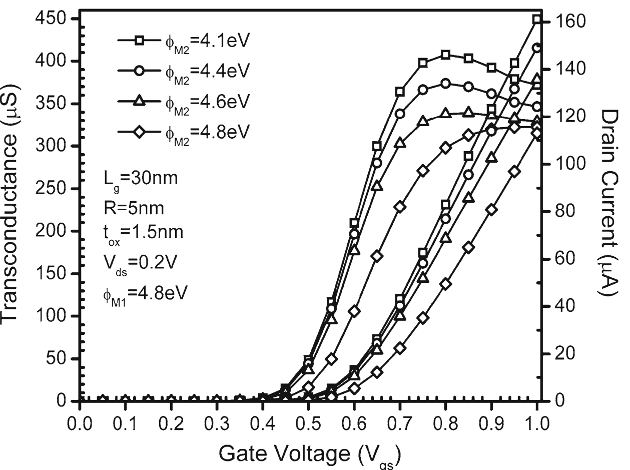


Fig. 8 Transfer and transconductance characteristics of GEWE-silicon nanowire MOSFET at V_{ds} = 0.2 V

source. This is a measure of efficacy of the two ports [37,38]. Figure 7 evaluates the device performance in terms of maximum transducer gain. As it clear from the graph that G_{MT} is improved in GEWE-SiNW in comparison to SiNW. This enhancement is due to integration of GEWE design onto silicon nanowire which augments current driving capability and results in higher power at the load end i.e. at drain end, hence suitable for RF/wireless applications.

3.1 Effect of gate metal engineering

In this sub-section, we examine the effect of metal workfunction engineering on the RF metrics of GEWE-SiNW MOSFET by keeping the workfunction at the source side constant and varying the workfunction of metal gate at the drain end.

Figure 8 indicates the transfer and transconductance characteristics of GEWE-SiNW MOSFET for different values of metal workfunction at drain side (Φ_{M2}). As is evident from Fig. 8 that as we increase the workfunction difference from 0 to 0.2 eV, the on current increased by 10.13 % and further increment in workfunction difference to 0.7 eV, results in 20 % enhancement in drain current. Also, significant enhancement in transconductance is observed as we decrease the metal workfunction at the drain end due to better improvement of carrier transport efficiency with increase in workfunction difference as stated in [39], thus, signifying the suppression of short channel effects.

Figure 9 depicts that there is prominent degradation of parasitic capacitances as we increase the metal gate workfunction difference. Capacitance decreases due to enhanced screening of channel region from drain bias variations thus, reducing the turn-on delay time.

Figure 10 compares the cut off and maximum oscillator frequency of GEWE-SiNW MOSFET for different metal workfunction. It is clearly evident from Fig. 10 that as the metal work function at the drain end decreases, the cut off frequency increases which leads to higher switching speed. Further, with increase in metal workfunction difference, the cut-off frequency increases as is shown in Fig. 10. This is due to enhanced gate control over channel and screening of potential from the drain side, which increases the transconductance, leading to increase in cut-off frequency and device packaging density, thereby making the device suitable for CMOS wireless applications. Also, the use of metal gates results in reduced gate resistance, and hence increases f_{MAX}. An appreciable accretion of maximum oscillation frequency is observed by increasing gate metal workfunction difference due to reduced parasitic capacitances as is shown in Fig. 9.

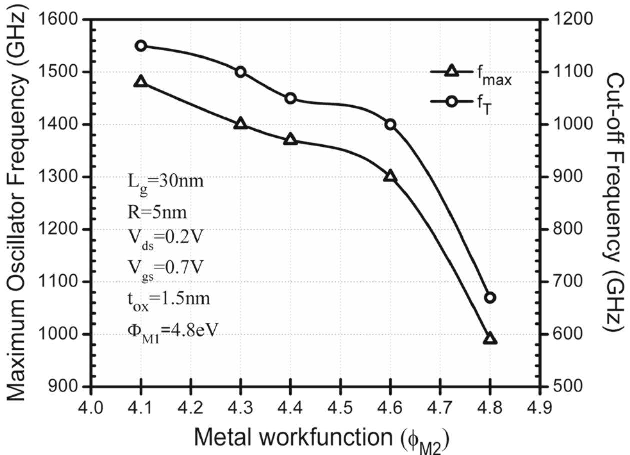


Fig. 10 Cut-off and maximum oscillator frequency of GEWE-SiNW MOSFET for various metal workfunction values

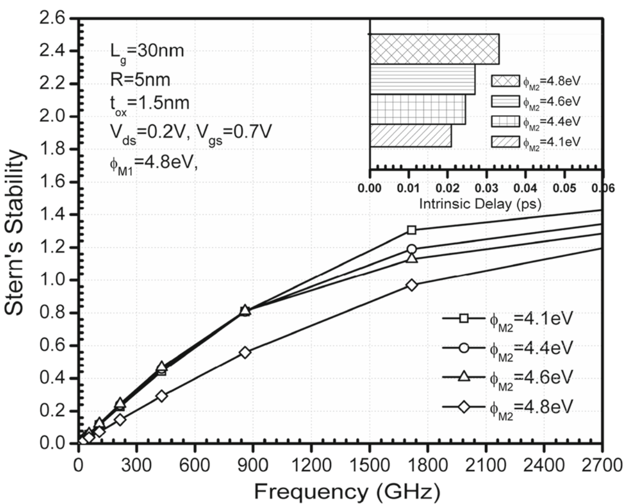


Fig. 11 Stern's Stability factor of GEWE-SiNW MOSFET for various metal workfunction values. *Inset* intrinsic delay of GEWE-SiNW MOSFET for various metal workfunction values

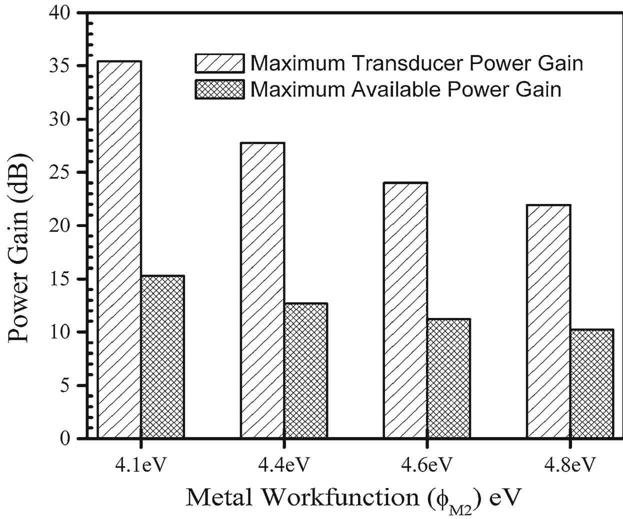


Fig. 12 Maximum available power gain and maximum transducer power gain of GEWE-SiNW MOSFET as a function of Φ_{M2}

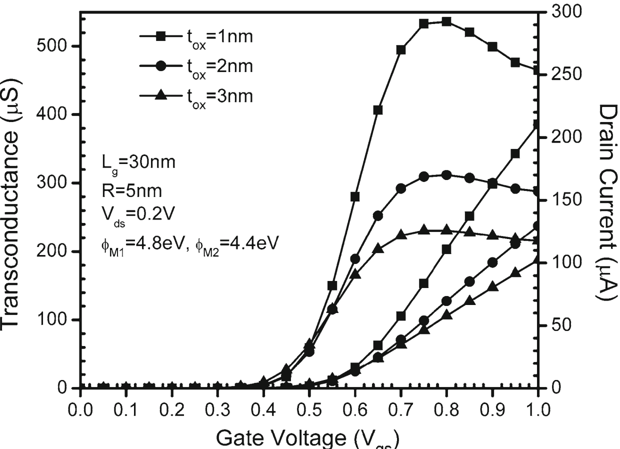


Fig. 13 Transfer and transconductance characteristics of GEWE-silicon nanowire MOSFET at $V_{ds} = 0.2$ V for different oxide thickness

Further, increasing the metal workfunction difference increases the K-factor as shown in Fig. 11. This is due to improvement of screening effect and I_{on} thus, maximizing power transfer from source to load. Hence, GEWE-SiNW is suitable for low noise amplifier and RF applications. Also, with increase in metal workfunction difference, delay reduces due to enhanced gate control and redistribution of electric field in the channel which results in higher mobility leading to improvement in carrier transport efficiency as shown in inset of Fig. 11.

G_{MT} also improves with the tuning of metal gate workfunction at drain end. Since, higher the metal gate workfunction difference, higher the electric field in the channel due to which mobility increases and hence significantly enhances the power gain. Further, tuning of structural parameters of GEWE-SiNW in terms of increased metal workfunction difference can enhance Gma as is evident from Fig. 12 due to enhanced transconductance owing to improved carrier efficiency and alleviated SCEs. Thus, GEWE-SiNW MOSFET proves to be a promising candidate for RF amplifiers and high speed applications.

3.2 Effect of oxide thickness

This section studies the impact of oxide thickness on RF metrics. It is clearly evident from Fig. 13 that scaling down the gate oxide thickness from 3 to 1 nm results in a better gate controllability over the channel which significantly enhances the driving current capability and improves the transconductance. This overcomes the drawback of mobility degradation due to increased channel doping. When oxide thickness

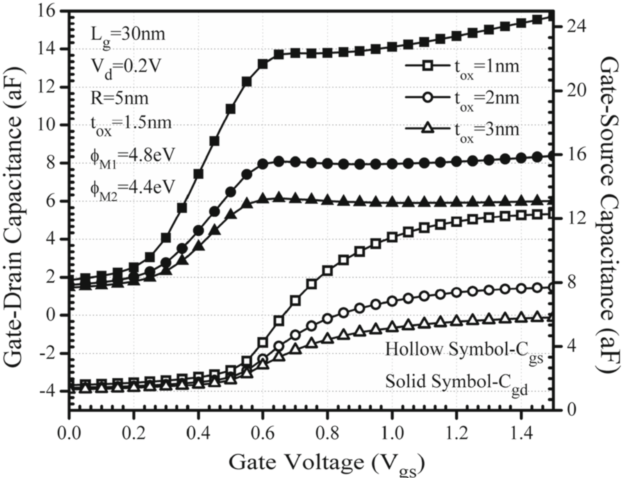
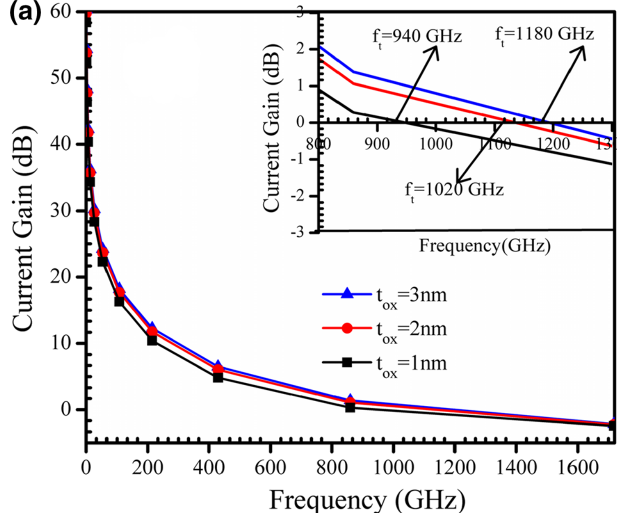


Fig. 14 Gate-drain and gate-source capacitance of GEWE-silicon nanowire MOSFET as a function of gate voltage for different oxide thickness



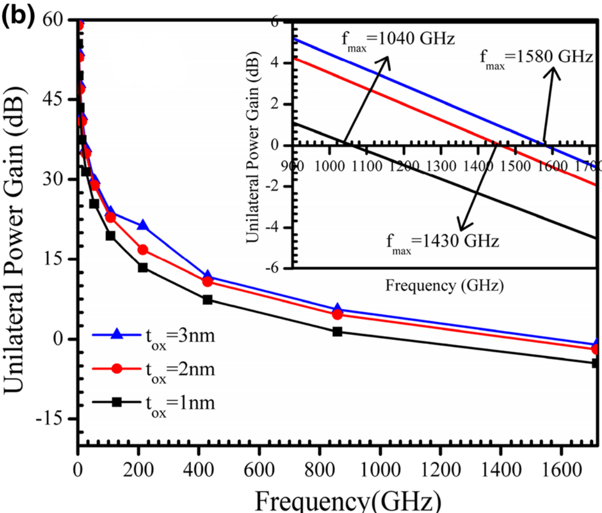


Fig. 15 **a** Cut-off frequency of GEWE-SiNW MOSFET at V_{ds} = 0.2 V for different oxide thickness as a function of gate voltage, **b** Current Gain of GEWE-SiNW MOSFET for different oxide thickness

scales down from 3 to 1 nm, the on-current increases by 77 % and transconductance by approximately 100 % thereby, reflecting significant improvement in SCEs at sub-nm range.

However, at high frequencies the picture is completely reversed, where the efficacy of the gate oxide capacitance dominates the RF behavior of devices. Figure 14 reflects the intrinsic parasitic gate-source and gate-drain capacitances as a function of gate voltage. It can be seen that as oxide thickness increases, parasitic capacitances decreases due to reduction in inversion charge. The same trend is shown by Pati et al. and Dastjerdy et al. [40,41]

The enhancement of transconductance due to better gate control on the channel for oxide thickness 1 nm compared to 3 nm does not counter balance the effect of the gate capacitances. As a result, t_{ox} = 3nm has better cut-off frequency and maximum oscillator frequency as can be clearly shown in Fig. 15 a, b. Further, current gain and unilateral power gains are extracted for determining the values of cut off frequency and maximum oscillation frequency respectively.

In addition, the Stern's stability factor also significantly improves as oxide thickness scale down from 3 to 1 nm as shown in Fig. 16. This enhancement is due to higher value of transconductance and better gate controllability.

Inset of Fig. 16 shows the intrinsic delay ratio of GEWE-SiNW MOSFET for three different oxide thickness. Since, delay depends upon gate capacitance and transconductance, therefore, intrinsic delay reduces as oxide thickness increases. Hence, scaling of oxide thickness significantly degrades the speed and the matching of the device in RF circuits.

Moreover, power gains such as maximum available power gain and maximum transducer gain also increseses with thinning of gate oxide as clearly is evident from Fig. 17, thus, providing maximum voltage gain.

3.3 Effect of channel length (L_g)

In this section, the impact of channel length is studied on various parameters.

Figure 18 shows as we scale down the channel length of silicon nanowire, the transfer characteristics improves due to better gate controllability and incorporation of dissimilar metal gates. This enhances the transconductance of device, and hence overcomes the SCEs associated due to scaling of channel length. Further, Fig. 19 depicts that there is a prominent degradation of gate-source and gate-drain capacitances. Since, as we reduce the channel length the inversion charge density of nanowire increases which results improvement in mobility across the channel due to reduction in scattering from nearby atoms and hence results in reduction in C_{gs} and C_{gd}.

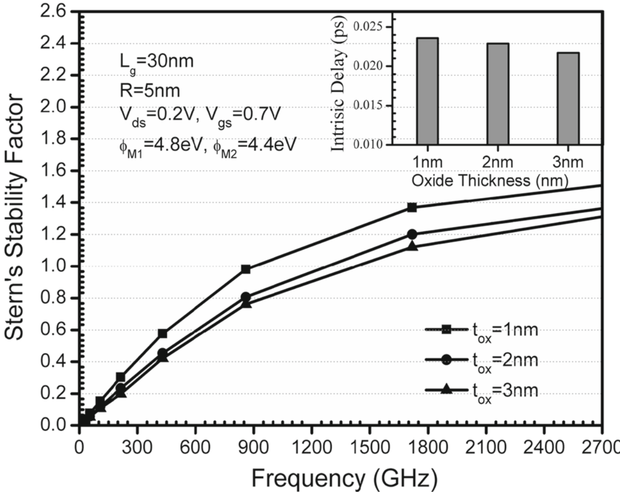


Fig. 16 Stern's stability factor of GEWE-SiNW MOSFET for various metal workfunction values. *Inset* intrinsic delay of GEWE-SiNW MOSFET at $V_{ds} = 0.2$ V for different oxide thickness

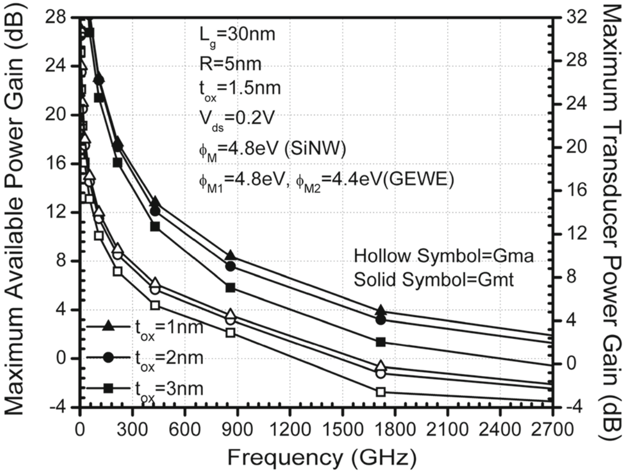


Fig. 17 Maximum available and maximum transducer power gain of GEWE-SiNW MOSFET for different oxide thickness

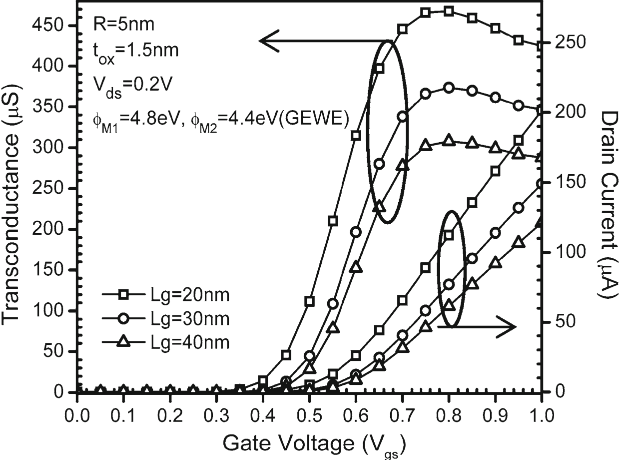


Fig. 18 Transfer and Transconductance characteristics of GEWE-silicon nanowire MOSFET for different channel lengths

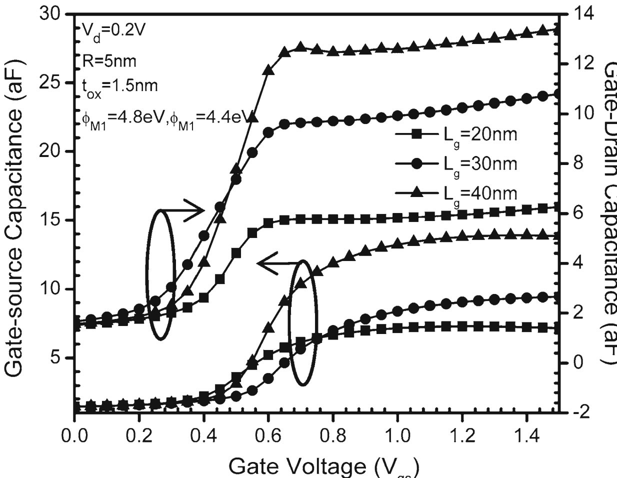


Fig. 19 Gate-source and gate-drain capacitance of GEWE-silicon nanowire MOSFET as a function of gate voltage for different channel lengths

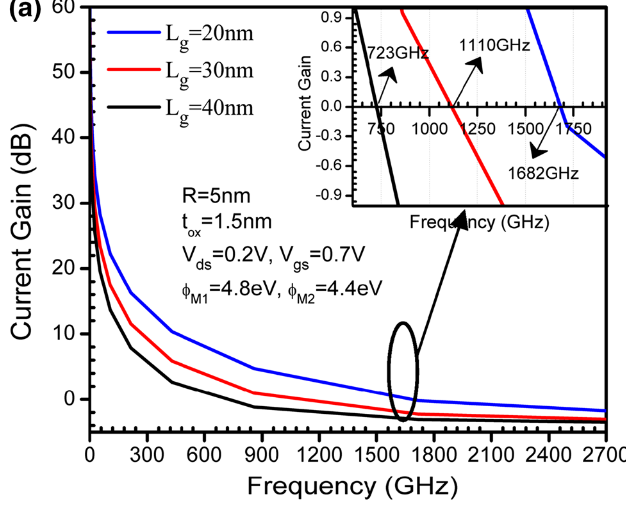
Figure 20a, b shows the current gain and unilateral power gain as a function of frequency. As we have already mentioned that f_T and f_{MAX} are extracted from current gain and unilateral power gain respectively, it is clearly evident that as channel length scales down, both cut-off and maximum oscillator frequency increases due to increase in transconductance and reduction in parasitic capacitance as is shown in Eq. (1) and (2).

Moreover, stern's stability factor which determines the stability of a device at high frequency decreases as we scale down the channel length due to overlapping of source and drain fields which results in a commuted gate control in scaled devices, thus causing instability as is shown in Fig. 21.

Intrinsic Delay of GEWE-SiNW improves further as we scale down the channel length from 40 to 20 nm as shown in inset of Fig. 21. This improvement is due to reduction in gate parasitic capacitance. Figure 22 shows the Maximum Available and Maximum Transducer power gain as a function of frequency for different gate lengths. The Power gain of GEWE-SiNW improves further as channel length of nanowire scales down to 20 nm due to enhancement in current gain.

3.4 Effect of radius of silicon nanowire (R)

In this section, we examine the efficacy of silicon nanowire radius on RF performance of GEWE-SiNW MOSFET. Figure 23 shows that as radius of nanowire decreases drain current decreases due to the decrement in inversion charge density which increases the threshold voltage as a result of which the on-state current decreases and hence the transconductance.



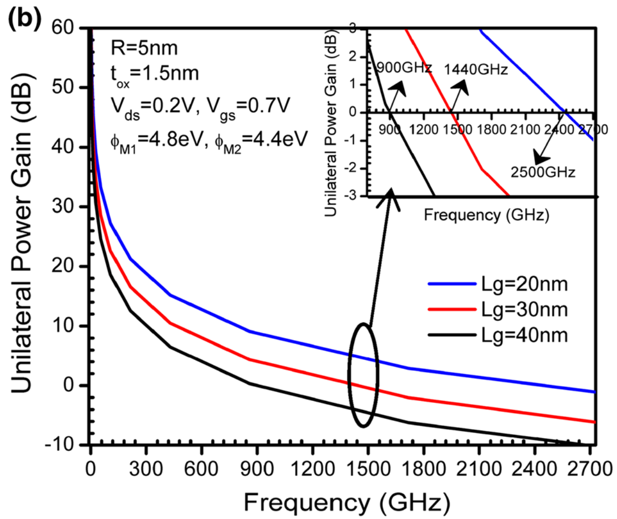


Fig. 20 **a** Current gain and **b** Maximum Unilateral Power Gain of GEWE-SiNW MOSFET $V_{ds} = 0.2$ V for different channel lengths

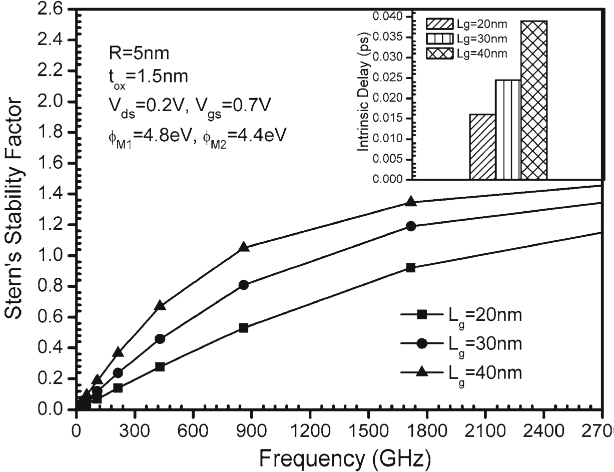


Fig. 21 Stern's stability factor of GEWE-SiNW MOSFET for different channel lengths. *Inset* intrinsic delay of GEWE-SiNW MOSFET at $V_{ds} = 0.2$ V for different channel lengths

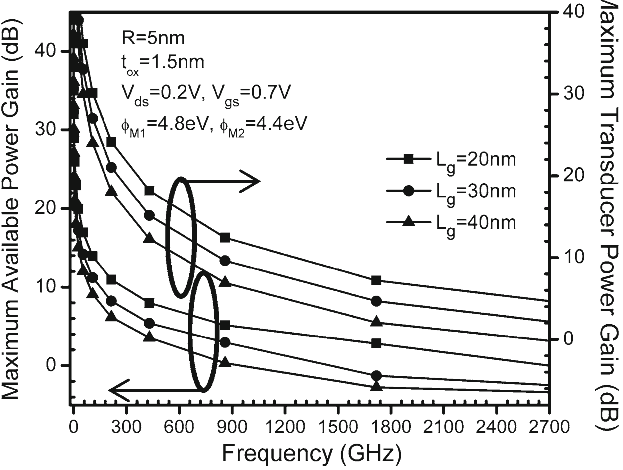


Fig. 22 Maximum available and maximum transducer power gain of GEWE-SiNW MOSFET at $V_{ds} = 0.2$ V for different channel lengths

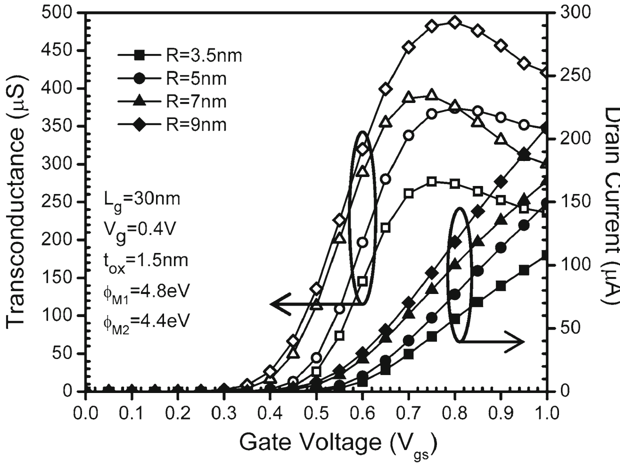


Fig. 23 Transfer and transconductance characteristics of GEWE-Silicon Nanowire MOSFET for different radius of silicon nanowire

On the other hand, parasitic gate capacitance which is sum of the gate-source and the gate-drain capacitance degrade as radius of silicon nanowire decreases. Smaller values of these capacitances play an important role in device switching performance due to reduction in the turn-on delay time. Figure 24 shows the behaviour of C_{gd} and C_{gs} as a function of gate voltage as is also predicted by Li et al. [42].

Figure 25 depicts the cut-off and maximum oscillator frequency of GEWE-SiNW MOSFET as a function of silicon nanowire radius. As is shown, ft increases as radius decreases due to degradation in parasitic gate capacitance. But fmax decreases as we reduce the radius of nanowire. So we have to choose optimal value of radius so that we can achieve desirable cut-off and maximum oscillator frequency for CMOS wireless applications.

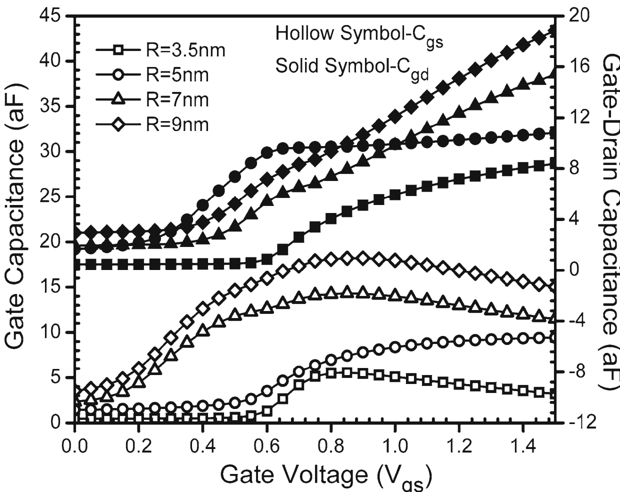


Fig. 24 Gate-drain and gate-source capacitance of GEWE-silicon nanowire MOSFET as a function of gate voltage for different radius of silicon nanowire

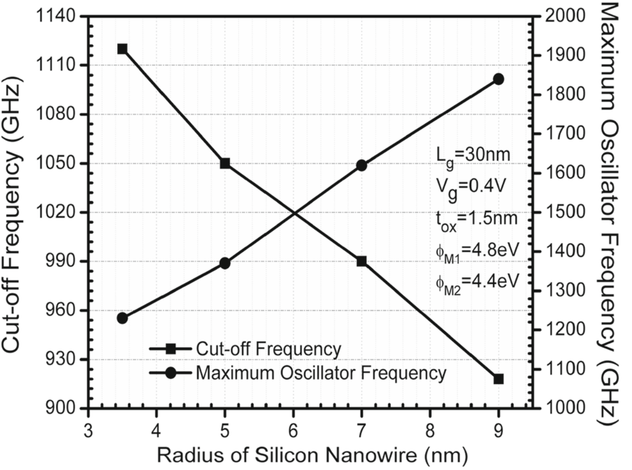


Fig. 25 Cut-off and maximum oscillatory frequency of GEWE-silicon nanowire MOSFET for different radius of silicon nanowire

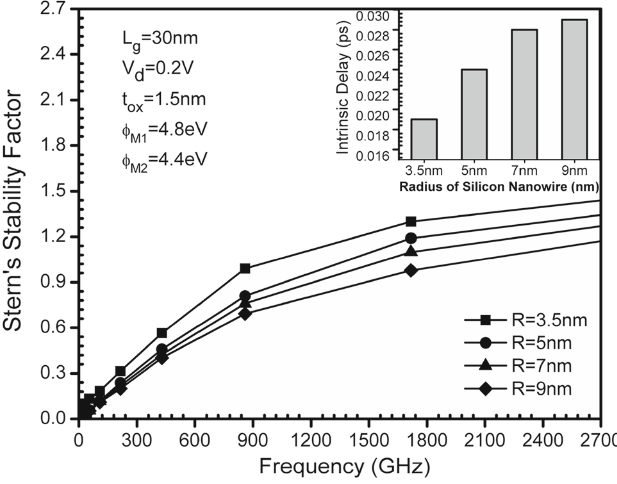


Fig. 26 Stern's stability factor of GEWE-SiNW MOSFET for different channel radius. *Inset* intrinsic delay of GEWE-SiNW MOSFET

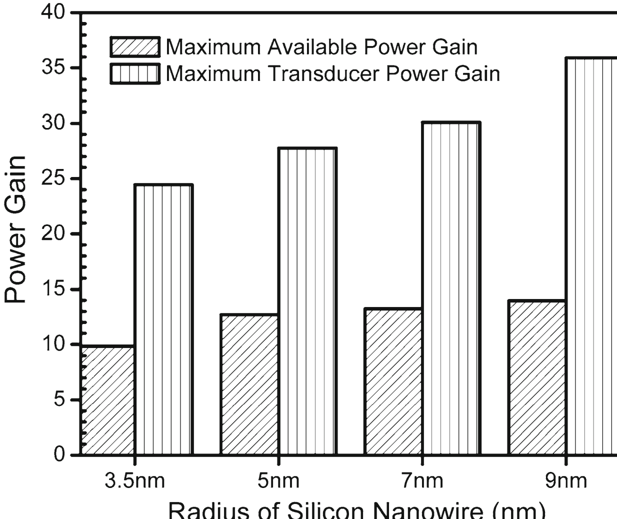


Fig. 27 Maximum available power gain and maximum transducer power gain of GEWE-SiNW MOSFET at $V_{ds} = 0.2$ V for different silicon nanowire radius

Figure 26 shows the stern's stability factor as a function of frequency and its inset shows the intrinsic delay of GEWE-SiNW as s function of radius of nanowire. It is clearly evident that at high frequency, $K > 1$ for GEWE-SiNW but its value enhances as radius scales down, hence make it suitable for low noise amplifiers. Also, intrinsic delay reduces to 50 % as we scale down the radii of nanowire due to degradation of parasitic capacitance as shown in Fig. 24.

In addition, power gains degrade as we reduce the radius of nanowire. Both maximum available power gain and maximum transducer power gain reduces 1.5 times as clearly shown in Fig. 27. Hence, for millimeter wave applications, we have to optimize the value of silicon nanowire radius.

4 Conclusion

The present work focuses on RF performance investigation of Conventional SiNW and GEWE-SiNW MOSFET in terms of parasitic capacitance, power gains, maximum and cut-off frequency, stability and intrinsic delay at high frequency. It has been found that due to improved transconductance, gate controllability and carrier mobility, GEWE-SiNW MOSFET exhibit superior performance in all RF metrics compared to its counterpart, thus providing its use in high frequency amplifier and microwave applications. Further, noticeable improvement in RF performance is observed by varying the device parameters such as metal workfunction at the drain end, channel length of nanowire, hence, giving a new opening for HF wireless and switching applications. Moreover, thinning of oxide thickness degrades the RF performance of GEWE-SiNW MOSFET and reduction in radii of nanowire also leads to degradation of RF metrics but improves as

compared to conventional SiNW. Thus, we have to choose optimum values of device parameters for better device performance at RF/Wireless applications.

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References

1. Larson, L.E.: Silicon technology tradeoffs for radio-frequency/mixed signal systems-on-a-chip. IEEE Trans. Electron Devices **50**, 683–699 (2003)
2. Woerlee, P.H., et al.: RF-CMOS performance trends. IEEE Trans. Electron Devices. **48**, 1776–1782 (2001)
3. Enz, C.: An-MOS transistor model for RF IC design valid in all region of operation. IEEE Trans. Microw. Theory Tech. **50**, 342–359 (2001)
4. Saijets, J., Andersson, M., Berg, M.A.: A comparative study of various MOSFET models at radio frequencies. Analog Integr. Circuits Signal Process. **33**, 5–17 (2002)
5. Chen, Q.: (Brian): Compact Modeling of Multi-Gate MOSFETs for RF Designs. Presented at IEEE International Wireless Symposium (2013). doi:10.1109/IEEE-IWS.2013.6616743
6. Jimenez, D., Iniguez, B., Roig, J., Sune, J., Marsal, L. F., Pallares, J., Flores, D.: Physics-based model of the surrounding-gate MOSFET. In: IEEE Spanish Conference on Electron Devices. pp. 393–396 (2005)
7. Sharma, D., Vishvakarma, S.K.: Precise analytical model for short channel cylindrical gate (CylG) gate-all-around (GAA) MOSFET. Solid-State Electron. **86**, 68–74 (2013)
8. Gupta, S.K., Baishya, S.: Modeling of cylindrical surrounding gate MOSFETs including the fringing field effects. J. Semicond. **34**, 074001 (2013)
9. Cui, Y., Zhong, Z., Wang, D., Wang, W.U., Lieber, C.M.: High performance silicon nanowire field effect transistors. Nano Lett. **3**, 149–152 (2003)
10. Fu, J., Singh, N., Buddharaju, K., Teo, S., Shen, C., Jiang, Y., Zhu, C., Yu, M., Lo, G., Balasubramanian, N., Kwong, D., Gnani, E., Baccarani, G.: Si-nanowire based gate-all-around nonvolatile SONOS memory cell. IEEE Electron Device Lett. **29**, 518–521 (2008)
11. Rustagi, S., Singh, N., Fang, W., Buddharaju, K., Omampuliyur, S., Teo, S., Tung, C., Lo, G., Balasubramanian, N., Kwong, D.: CMOS inverter based on gate-all-around silicon-nanowire MOSFETs fabricated using top-down approach. IEEE Electron Device Lett. **28**, 1021–1024 (2007)
12. Yang, B., Buddharaju, K.D., Teo, S.H.G., Singh, N., Lo, G.Q., Kwong, D.L.: Vertical silicon-nanowire formation and gate-all-around MOSFET. IEEE Electron Device Lett. **29**, 791–794 (2008)
13. Wang, R., Zhuge, J., Huang, R., Tian, Y., Xiao, H., Zhang, L., Li, C., Zhang, X., Wang, Y.: Analog/RF performance of Si nanowire MOSFETs and the impact of process variation. IEEE Trans. Electron Devices. **54**, 1288–1294 (2007)
14. Shur, M.: Split-gate field-effect transistor. Appl. Phys. Lett. **54**, 162–164 (1989)
15. Long, W., Ou, H., Kuo, J.M., Chin, K.K.: Dual material gate (DMG) field effect transistor. IEEE Trans. Electron Devices **46**, 865–870 (1999)
16. Zheng, C. Y.: The using of dual-material gate MOSFET in suppressing short-channel effects: a review. In: IEEE International Conference on Electronics, Communications and Control (2011). doi:10.1109/ICECC.2011.6066420
17. Pal, A., Sarkar, A.: Analytical study of dual material surrounding gate MOSFET to suppress short-channel effects (SCEs). Eng. Sci. Technol. Int. J. **17**, 205–212 (2014)
18. Zhou, W., Zhang, L., Chen, L., Xu, Y., Wu, W., He, J.: Test article sample title placed here. J. Nanosci. Nanotechnol. **11**, 11006–110010 (2011)
19. Gupta, N., Chaujar, R.: Implications of transport models on the analog performance of gate electrode workfunction engineered (GEWE) SiNW MOSFET. In: IEEE 2nd International Conference on Devices, Circuits and Systems (2014). doi:10.1109/ICDCSyst.2014.6926154
20. Gupta, N., Kumar, A., Chaujar, R.: Oxide bound impact on hot-carrier degradation for gate electrode workfunction engineered (GEWE) silicon nanowire MOSFET. Microsyst.Technol. (2015). doi:10.1007/s00542-015-2557-9
21. Doan, C.H., Emami, S., Niknejad, A.M., Brodersen, R.W.: Millimeter-wave CMOS design. IEEE J. Solid-State Circuits. **40**, 144–155 (2005)
22. ATLAS User's Manual. SILVACO Int., Santa Clara (2014)
23. Yang, G., Wang, S., Wang, R.: An efficient preconditioning technique for numerical simulation of hydrodynamic model semiconductor devices. Int. J. Numer. Simul. **16**, 387–400 (2003)
24. Chaudhry, A., Roy, J.N.: Mosfet models, quantum mechanical effects and modeling approaches: a review. J. Semicond. Technol. Sci. **10**, 20–27 (2010)
25. Patnaik, V.S., Gheedia, A., Kumar, M.J.: 3D Simulation of nanowire FETs using quantum models. http://web.iitd.ac.in/~mamidala/HTMLobj-1227/jul_aug_sep08 (2008)
26. Gnani, E., Reggiani, S., Rudan, M., Baccarani, G.: On the electrostatics of double-gate and cylindrical nanowire MOSFETs. J. Comput. Electron. **4**, 71–74 (2005)
27. Ghosh, P., Haldar, S., Gupta, R.S., Gupta, M.: An investigation of linearity performance and intermodulation distortion of GME CGT MOSFET for RFIC design. IEEE Trans. Electron Devices. **59**, 3263–3268 (2012)
28. Tsividis, Y.: Operation and Modeling of the MOS Transistor, 2nd edn. Oxford Universiy Press, New York (1999)
29. Malik, P., Gupta, R.S., Chaujar, R., Gupta, M.: AC analysis of nanoscale GME-TRC MOSFET for microwave and RF applications. Microelectron. Reliab. **52**, 151–158 (2012)
30. Cho, S., Kim, K.R., Park, B.G., Kang, I.M.: RF performance and small-signal parameter extraction of junctionless silicon nanowire MOSFETs. IEEE Trans. Electron Devices **58**, 1388–1396 (2011)
31. Sarkar, A., De, S., Dey, A., Sarkar, C.K.: Analog and RF performance investigation of cylindrical surrounding-gate MOSFET with an analytical pseudo-2D model. J. Comput. Electron. **11**, 182–195 (2012)
32. Pozar, D.M.: Microwave Engineering, 4th edn. Wiley, Hoboken (2011)
33. Nae, B., Lazaro, A., Iniguez, B.: High frequency and noise model of gate-all-around MOSFETs. In: Spanish Conference on Electron Devices (2009). doi:10.1109/SCED.2009.4800443
34. Khakifirooz, A., Antoniadis, D.A.: MOSFET performance scaling-part I: historical trends. IEEE Trans. Electron Devices. **55**, 1391–1400 (2008)
35. Voinigescu, S.: High-Frequency Integrated Circuits. Cambridge University Press, Cambridge (2013)
36. Oh, Y., Rieh, J.S.: Effect of device layout on the stability of RF MOSFETs. IEEE Trans. Microw. Theory Tech. **61**, 1861–1869 (2013)
37. Golio, M.: Microwave and RF Product Applications. CRC Press, Boca Raton (2003)
38. Grebennikov, A.: RF and Microwave Transmitter Design. Wiley, Hoboken (2011)

39. Long, W., Chin, K.K.: Dual material gate field effect transistor (DMGFET). In: IEEE Electron Devices Meeting Tech Dig. pp. 549–552, (1997)
40. Pati, S.K., Koley, K., Dutta, A., Mohankumar, N., Sarkar, C.K.: Study of body and oxide thickness variation on analog and RF performance of underlap DG-MOSFETs. Microelectron. Reliab. **54**, 1137–1142 (2014)
41. Dastjerdy, E., Ghayour, R., Sarvari, H.: Simulation and analysis of the frequency performance of a new silicon nanowire MOSFET structure. Physica E. **45**, 66–71 (2012)
42. Li, Y., Hwang, C.H.: DC baseband and high-frequency characteristics of a silicon nanowire field effect transistor circuit. Semicond. Sci. Technol. **24**, 045004 (2009)

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TECHNICAL PAPER

Oxide bound impact on hot-carrier degradation for gate electrode workfunction engineered (GEWE) silicon nanowire MOSFET

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Abstract In this present work, we explore the hot carrier fidelity of gate electrode workfunction engineered silicon nanowire (GEWE-SiNW) MOSFET at 300 K using DEVEDIT-3D device editor and ATLAS device simulation software. TCAD simulation shows reduction in the hot carrier reliability of a GEWE SiNW MOSFET in terms of electron temperature, electron velocity and Hot Electron gate current for reflecting its efficacy in high power CMOS applications. Further, a comparative investigation for different values of oxide thickness and high-k has been done to analyze the performance of GEWE-SiNW MOSFET in terms of electrical parameters such as conduction band, DIBL, electric field, electron temperature, electric velocity and gate current. It has been clearly shown that with oxide thickness 0.5 nm the hot-carrier reliability and device performance improves in comparison to oxide thickness 2.5 nm. In addition, with k = 21(HfO_2) device performance in terms of hot-carrier reliability further enhanced due to increased capacitance and thus offer its effectiveness in sub-nm range analog applications.

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1 Introduction

From past few decades, the major concern for conventional CMOS devices were scaling effects such as leakage current, hot carrier effects, DIBL and current driving ability. To overcome such effects a number of device engineering schemes such as source/drain engineering (Kranti et al. 2006), metal gate workfunction engineering (Long et al. 1997; Deb et al. 2012; Dubey et al. 2013), channel engineering (Yu et al. 1997) and some novel device structures such as Double gate MOSFET (Barsan 1981; Venkatesan et al. 1992), cylindrical gate MOSFET (Sharma and Vishvakarma 2013), Fin-FETs (Sohn and Kang 2012), Nanowire MOSFET (Iwai et al. 2011; Wang et al. 2007) have been explored and employed during the past few years. Among them, due to ideal symmetry, excellent gate controllability and potential benefits of silicon nanowire, gate-all-around (GAA) silicon nanowire MOSFET (Chen and Tan 2014; Wang et al. 2013) is emerging as a most promising candidate for future silicon based nano-devices. This structure manifest a superior control of short channel effects because of excellent electrostatic coupling between the conducting channel and the surrounding gate. The nanowire (NW) transistors can be seen as the utmost integration of the innovative nano-devices and it is one of the most promising means of overwhelm the limits of planar silicon devices because of their suitability with gate all around design. Also, from device and circuit developers they have procured remarkable attention because of its potential for high performance and building highly dense electronic circuits. Current approaches in nanoscale fabrication techniques have shown that semiconductor nanowires may turn into a candidate for next generation technologies. Silicon and Germanium nanowire transistors are also significant because of their adaptability with the CMOS technology

(Mukherjee and Maiti 2012). Short-channel effects (SCEs) result in many problems such as increase in power consumption and leakage current (De and Borkar 1999). Hot-electron degradation is another unenviable effect of short-channel devices (Orouji and Kumar 2005; Krieger et al. 2001). As the scaling of transistors penetrates into the submicron regime, the electric field grows and causes electrons and holes to gain high kinetic energy, referred to as "hot carriers". These hot carriers have ample of high energies and thrust to allow them to be injected from the semiconductor into the surrounding oxide films such as the gate and sidewall silicon oxides (Groeseneken 2001). The existence of such free mobile carriers in the oxide provokes numerous physical devastation processes that can highly change the device characteristics over prolonged periods. The stack of damage ultimately causes the circuit to fail as decisive parameters such as threshold voltage shift due to aforesaid damage. The accumulation of damage resulting degradation in device behavior due to hot carrier injection is called hot carrier degradation (Pan et al. 1994; Kaur et al. 2007).

Drain induced barrier lowering (DIBL) is an important parameter to examine SCEs in VLSI MOSFET devices (Arora 2012). It is the variation in threshold voltage at different ($\Delta V_{th}/\Delta V_{DS}$) drain to source bias. The variation of the bending energy gap due to the threshold voltage variation is mainly governed by the increase of the drain voltage (Sharma 2012). The high electric field due to a higher V_{ds} enter deeper into the conducting channel and causes more pronounced short channel effect. DIBL tunneling affects the I–V characteristic in sub-threshold regime by a lateral shift it can be determined by the percentage of the shift in barrier height value to the drain voltage difference (Jeon et al. 2009) As the issue of hot carrier and DIBL becomes increasingly important in deep-submicron MOSFETs, it is thus increasingly essential to analyze the hot carrier reliability in terms of hot-electron-injected gate current, impact-ionization substrate current, and electron velocity and temperature near the drain end for their impact on the overall chip performance (Chaujar et al. 2008).

Moreover, the downscaling of MOSFETs dimensions to sub-nm will face the challenges when SiO_2 is used as gate dielectric. When oxide thickness of gate oxide is below 1.5 nm, the electrons tunnel through the gate oxide easily, this increases leakage current and thus leads to excessive power consumption and reduced device reliability. Therefore, it is required for high-k materials to replace SiO_2 as a gate dielectric in order to reduce the high standby power (Momose et al. 1996; Nirmal et al. 2013; Sinha and Chaudhury 2013). The work thus improves and envisions the feasibility of a GEWE-SiNW MOSFET (Gupta and Chaujar 2014) for high-performance applications where hot carrier reliability is a primary concern. TCAD simulations using ATLAS demonstrate that the GEWE-SiNW MOSFET structure exhibits significantly improved hot carrier performance, where low power consumption is required and in digital logic and memory applications where fast switching action of MOS is needed. In addition, the influence of oxide thickness variation and efficacy of different high-k materials on performance of GEWE-SiNW MOSFET has also been discussed in this paper.

The complete work in this paper is systematized as follow: Sect. 2 elucidate the 3D-device architecture and its default parameters used in this work along with simulation models. In Sect. 3, first we calibrate our simulation models with experimental results and then we compare the device performance in terms of hot-carrier reliability and further we examine the impact of thinning of gate oxide thickness and high-K of GEWE-SiNW MOSFET on various parameters including Hot-Carrier Metrics such as HE-Ig, Electron Temperature, electron velocity and DIBL for the n-MOSFET. Finally the conclusions are drawn in Sect. 4.

2 Device structure: parameters and simulation models

Figure 1 shows the simulated device structure of GEWE SiNW MOSFET. All simulations have been performed using ATLAS and DEVEDIT 3D device simulator. Drift–diffusion model is not suitable for sub-50-nm gate length devices, since it neglects the nonlocal effects. In our simulation, we have adopted the hydrodynamic energy transport model which includes the continuity equations, momentum transport equations, energy balance equations of the carriers, and the Poisson equation. It can model the nonlocal transport phenomenon and is more accurate than the drift–diffusion method.

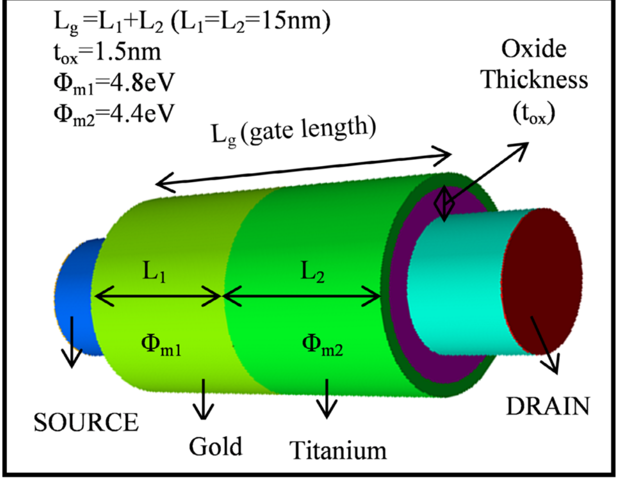


Fig. 1 Simulated device structure: GEWE SiNW MOSFET

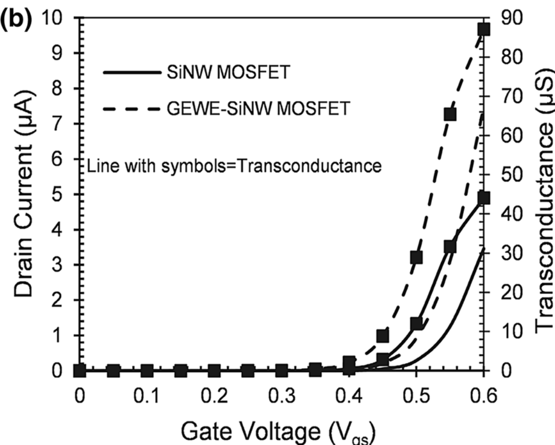
The Energy Balance Transport Model follows the derivation by Stratton (Stratton 1972) which is derived starting from the Boltzmann Transport Equation. By applying certain assumptions, this model decomposes into the hydrodynamic model (Yang et al. 2003). Boltzmann statistics are used in preference to Fermi statistics. This model is modeled by following equations:

$$\xi_n = \frac{d(\ln \mu_n)}{d(\ln T_n)} = \frac{T_n}{\mu_n} \tag{1}$$

$$\xi_p = \frac{d(\ln \mu_p)}{d(\ln T_p)} = \frac{T_p}{\mu_p} \tag{2}$$

The parameters ξ_n and ξ_p are dependent on the carrier temperatures. Different assumptions concerning ξ_n and ξ_p correspond to different non-local models. In the high-field saturated velocity limit that corresponds to velocity saturation the carrier mobilities are inversely proportional to the carrier temperatures. We put $\xi_n = 0$, this would correspond to the simplified Hydrodynamic Model for electrons. The parameter, ξ_n can be specified using the KSN parameters on the MODELS statement (Atlas User's Manual 2014).

For the study of gate currents, the Selberherr's impact ionization and hot-electron-injection models are used to provide an accurate measure of hot-carrier-injection in short-channel devices. All the simulations have been performed using physical models accounting for the electric field-dependent and concentration-dependent carrier mobilities, Shockley–Read–Hall recombination/generation with doping dependent carrier lifetime. The mobility model used is the inversion layer Lombardi CVT mobility model, wherein concentration-dependent mobility, high field saturation model, and mobility degradation at interfaces are all included (Atlas User's Manual 2014). Default simulator coefficients for all parameters have been employed. In order to fairly analyze the device performances, all the three devices are optimized to have the same threshold voltage, i.e., 0.32.



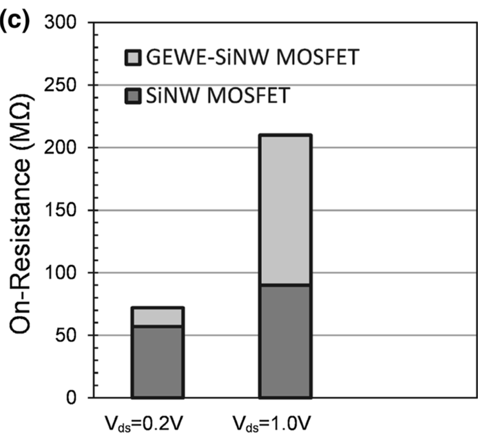


Fig. 2 **a** Calibration with the experimental result, $I_{ds} - V_{gs}$ characteristics of silicon nanowire MOSFET, **b** transfer and transconductance characteristics of silicon nanowire and GEWE-silicon nanowire MOSFET at $V_{DS} = 0.4$ V respectively, **c** On-resistance of SiNW and GEWE-SiNW MOSFET

3 Results and discussion

In this paper, we compare SiNW and GEWE SiNW MOSFETs with the conventional MOSFET. The present analysis is carried out for a channel length, $L_g = 30$ nm, radius of NW, R = 5 nm and thickness of oxide, $t_{ox} = 1.5$ nm, substrate doping is p-type with concentration of 1×10^{16} cm^{-3}; source and drain are n-type with uniform doping profiles is 5×10^{19} cm^{-3}. The metal gate work function at the source end (Φ_{m1}) is 4.8 eV (Au) and metal gate work function at the drain end (Φ_{m2}) is 4.4 eV (Ti) in GEWE and metal gate workfunction is 4.8 eV in SiNW MOSFET.

Figure 2a shows simulation result compared with fabricated SiNW MOSFET reported in literature (Suk et al. 2005). The calibration of model parameters used in simulation has been performed according to the published results to validate our simulations results. Figure 2b shows the drain current and gate transconductance characteristics of GEWE-SiNW MOSFET at drain bias 0.4 V. As shown in Fig. 2b, the current driving capability of nano-scale GEWE-SiNW MOSFET enhanced by 100 % in comparison to SiNW MOSFET. This enhancement is due to incorporation of metal gate engineering scheme which causes gradual step change of surface potential at the interface of two metals and hence increases gate efficiency of device. In

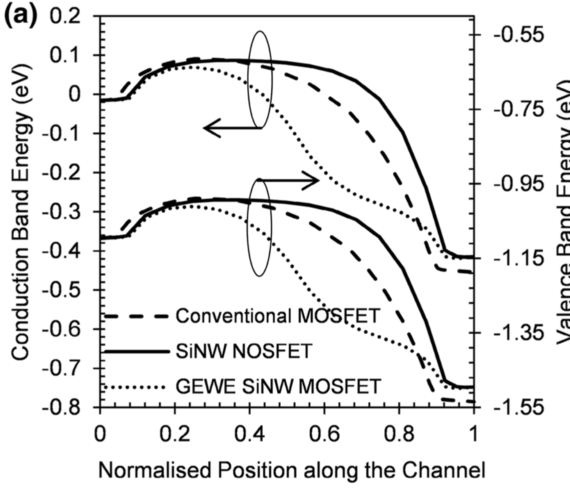


Fig. 3 **a** Conduction band energy and Valence band energy variation along the channel for $V_{gs} = 0.37$ V for conventional, SiNW and GEWE Si NW MOSFET at $V_{ds} = 0.55$ V, **b** DIBL versus V_{ds} variation for conventional MOSFET, SiNW MOSFET and GEWE Si NW MOSFET at $V_{gs} = 0$ V for two different values of V_{ds1}

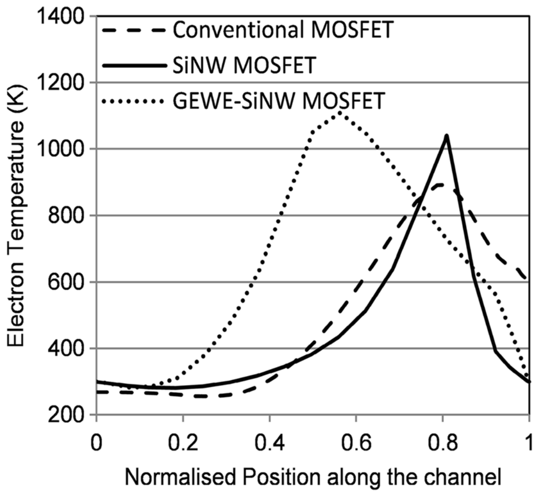


Fig. 4 Electron temperature variation along the channel for conventional MOSFET, SiNW MOSFET and GEWE Si NW MOSFET at $V_{ds} = 0.55$ V, $V_{gs} = 0.37$ V

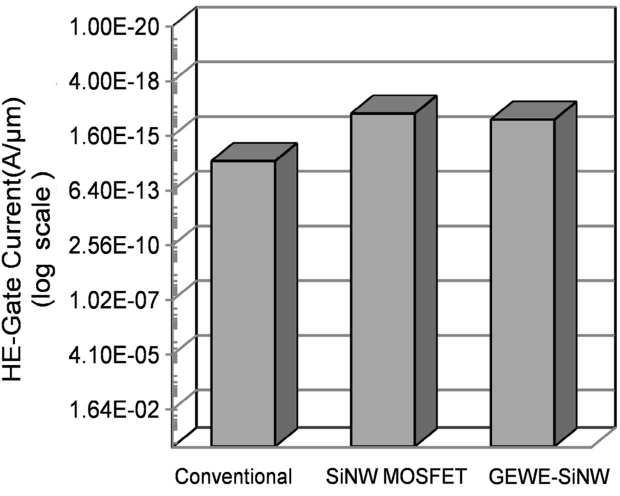


Fig. 5 HE gate current for conventional MOSFET, SiNW and GEWE Si nanowire MOSFET at $V_{ds} = 0.55$ V

general, the larger the transconductance figure for a device, the greater the gain (amplification) it is capable of delivering, when all other factors are held constant. It is clearly evident from Fig. 2b that transconductance of GEWE-SiNW is higher in comparison to conventional SiNW MOSFET due to enhanced on-current. As we know CMOS is used as a switch in linear region, and in saturation region on-resistance should be large so that we get large gain for amplifier Fig. 2c clearly shows that in linear and saturation region GEWE-SiNW MOSFET exhibit smaller and higher on-resistance respectively compared to SiNW MOSFET.

Figure 3a shows the variation of conduction band and valence band along the channel length for conventional MOSFET, SiNW and GEWE Si NW MOSFET at $V_{gs} = 0.37$ V and $V_{ds} = 0.55$ V. As shown in Fig. 3a, the significant barrier lowering just below the gate in conventional MOSFET leads to leakage current. The improvement in DIBL effect in GEWE is due to the step in conduction band energy profile in the channel region, which is resulting from metal gate workfunction difference. In SiNW and GEWE-SiNW, there is improved gate controllability over the channel due to cylindrical gate design hence DIBL is significantly lowered as shown in Fig. 3b in comparison to conventional MOSFET. $V_{ds} = 0.1$ V is used as reference for calculating barrier lowering in all three device. Furthermore, with an increase in the drain to source bias, the DIBL effect increases, but this increase is prominent in compared MOSFET comparison to the GEWE-SiNW. The DIBL is calculated as follows:

$$DIBL = \frac{V_{Th1} - V_{Th0}}{V_{ds1} - V_{ds0}} \tag{3}$$

where V_{Th1} is the threshold voltage of device when V_{ds1} bias is applied and V_{Th0} is the threshold voltage of device when reference bias voltage i.e. $V_{ds0} = 0.1$ V is applied.

Figure 4 predicts the variation of electron temperature along the channel length from source to drain for conventional, SiNW and GEWE-SiNW MOSFET. As it is clear from the results, an appreciable reduction in electron temperature for GEWE-SiNW at the drain side which is due to reduction in electric field at the drain side, which in turn reduces the leakage current and hence improves hot carrier immunity in comparison to conventional MOSFET. The reduction in electric field at drain side in GEWE-SiNW is because of gate electrode function engineering, which causes step potential profile at the interface of two metal gates (Long and Chin 1997).

Gate current of conventional MOSFET is comparatively higher than SiNW MOSFET because of short

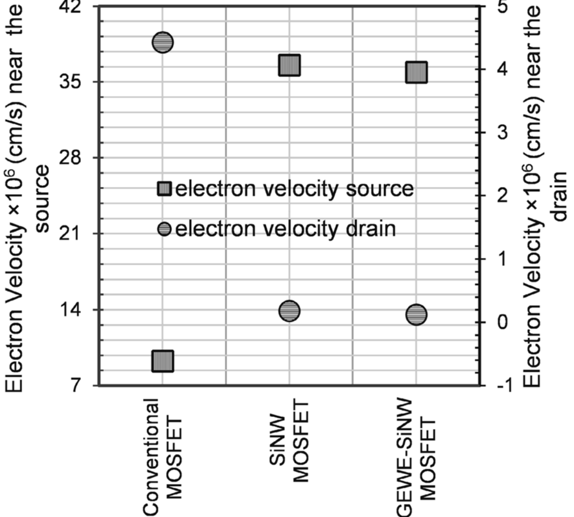
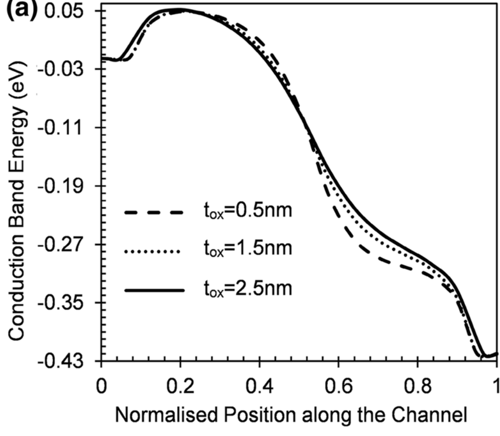


Fig. 6 Electron velocity for source and drain side for conventional MOSFET, SiNW and GEWE Si nanowire MOSFET at $V_{ds} = 0.55$ V, $V_{gs} = 0.37$



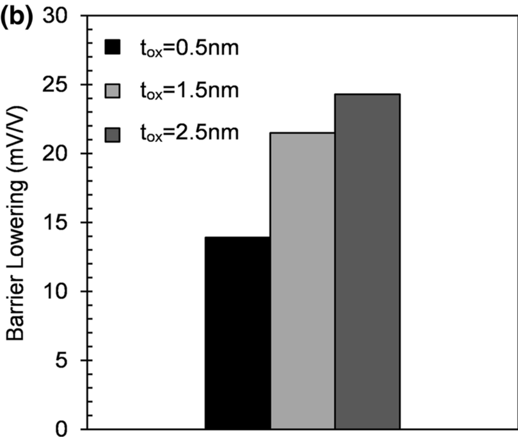


Fig. 7 **a** Conduction band profile for GEWE-SiNW MOSFET at different values of oxide thickness. **b** Barrier lowering for GEWE-SiNW MOSFET at different values of different values of oxide thickness

channel effects which exists in conventional MOSFET. Figure 5 shows the hot electron (HE) injected gate current of conventional, SiNW and GEWE-SiNW MOSFET at $V_{ds} = 0.55$ V. HE–I_g in SiNW MOSFET is reduced significantly in comparison to GEWE-SiNW MOSFET. Since, GEWE favors high electric field in the channel because of step potential profile in the channel, which causes tunneling of electrons from channel to gate oxide causing gate tunneling current thereby increasing HE-I_g current in comparison to SiNW MOSFET.

Figure 6 predicts the electron velocity of conventional, SiNW and GEWE-SiNW MOSFET at $V_{ds} = 0.55$ V along the channel. In order to improve the carrier transport efficiency in the channel, the carrier velocity near the source should be more than near the drain. Higher electron velocity (3.59×10^7 cm/s) near the source side is obtained for GEWE-SiNW in contrast to 3.5×10^7 and 0.9×10^7 cm/s obtained for SiNW and conventional MOSFET, respectively, as shown in Fig. 5, as a result enhancing the source carrier injection into the channel and hence results in hot carrier immunity in GEWE-SiNW MOSFET. For low-power and low-voltage analog circuit applications, lower electron velocity near the drain end are important design parameters.

3.1 Effect of gate oxide thickness

Figure 7a shows the variation of conduction band energy of GEWE-SiNW MOSFET with the normalized position along the channel. The result shows that as we scale down the oxide thickness, step in conduction band profile increases and hence results in lowering of DIBL as is indicated in Fig. 7b. It is clearly evident from the figure that when oxide thickness is 0.5 nm barrier lowering is 13.9 mV/V compared to 24.3 mV/V at 2.5 nm, thereby reflecting significant improvement in SCEs at sub-nm range. Figure 8 depicts the variation of electric field of GEWE-SiNW MOSFET at different oxide thickness with the normalized position along the channel. As is evident from the figure, the drain electric field reduces as oxide thickness decreases due to incorporation of lower workfunction of metal gate and thinning of gate oxide, results in less number of hot-carriers at the drain end and thus improves hot-carrier reliability of device. Also, as shown in figure the peak electric field in the channel increases due to difference in metal gate workfunction, which results in

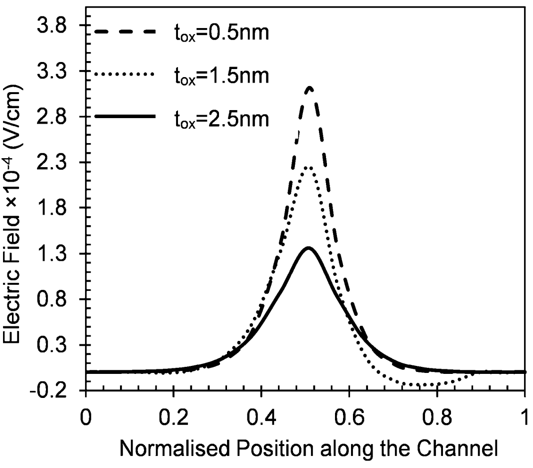


Fig. 8 Electric Field for GEWE-SiNW MOSFET at different values of oxide thickness

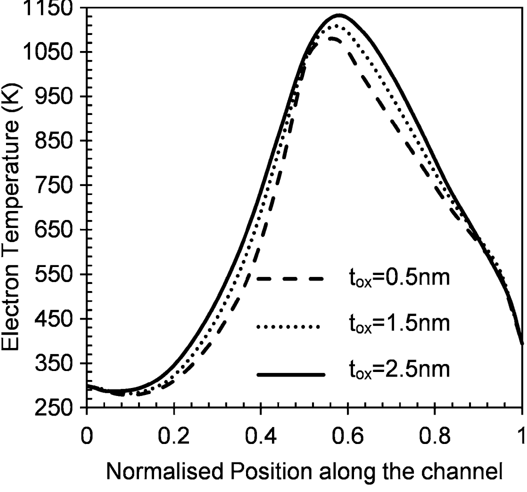


Fig. 9 Electron Temperature for GEWE-SiNW MOSFET for $V_{gs} = 0.6$ V and $V_{ds} = 0.4$ at different values of oxide thickness

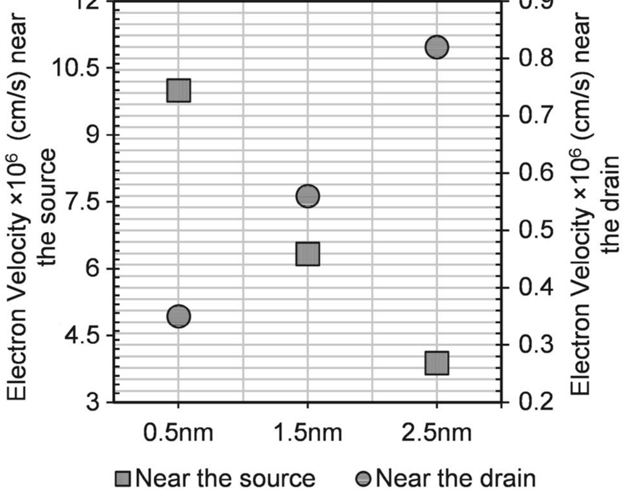


Fig. 10 Electron velocity for source and drain side for GEWE-SiNW MOSFET for $V_{gs} = 0.6$ V and $V_{ds} = 0.4$ at different values of oxide thickness

improvement in electron velocity and thus enhances the carrier efficiency.

Figure 8 depicts an appreciable reduction in electron temperature of GEWE-SiNW MOSFET at the drain end as we scale down the oxide thickness. This reduction in temperature is due to reduction in electric field at the drain end which results less number of hot-carriers and thus lowers the temperature, which accounts improvement in hot-carrier reliability. Figure 9 depicts an appreciable reduction in electron temperature of GEWE-SiNW MOSFET at the drain end as we scale down the oxide thickness. This reduction in temperature is due to reduction in electric field at the drain end which results less number of hot-carriers and thus lowers the temperature, which accounts improvement in hot-carrier reliability.

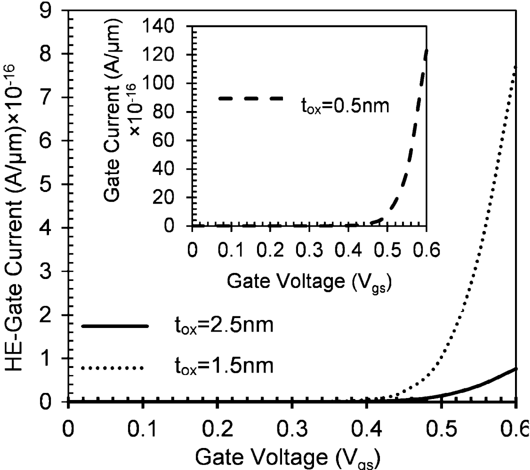


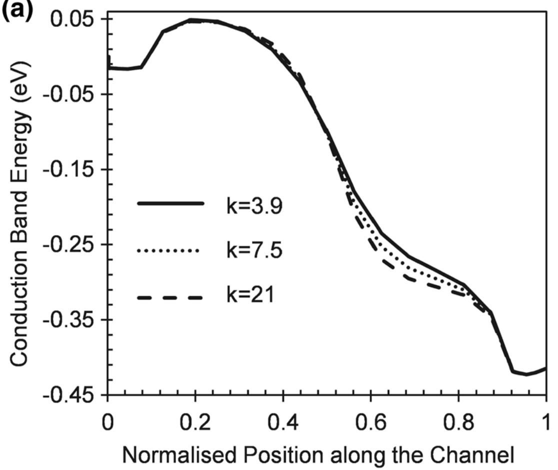
Fig. 11 Hot-electron injection gate current for GEWE-SiNW MOSFET at different values of oxide thickness

Figure 10 shows the effect of oxide thickness on electron velocity of GEWE-SiNW MOSFET. In order to upgrade the carrier efficiency, electron velocity near the source end should be greater than velocity at the drain end. Result depicted electron velocity at source side is 0.63×10^7 cm/s for 1.5 nm oxide thickness in contrast to 0.3×10^7 cm/s for 2.5 nm, thereby enhancing the carrier injection into the channel. If we further scale down the oxide thickness to 0.5 nm results in improvement in electron velocity near the source (1.2×10^7 cm/s), due to improved gate controllability over the channel and effectiveness of dual material gate, hence leading to improvement in carrier efficiency and driving current capability of device. Further, Fig. 10 also validates a lower electron velocity of 0.35×10^7 cm/s at the drain end for 0.5 nm thickness in contrast to 0.56×10^7 and 0.82×10^7 cm/s for 1.5 and 2.5 nm respectively, thus imparting outstanding hot-carrier immunity.

Hot-Electron Injection Gate Current (HE-I_g) is a key parameter to evaluate the hot-carrier reliability of a device. Figure 11 depicts the variation of gate current as s function of gate to source voltage. As is evident from figure that when oxide thickness goes on decreasing from 2.5 to 0.5 nm gate current increases, due to tunneling of electrons through the gate oxides which causes increment in gate current and thus hinders the device performance.

3.2 Effect of dielectric constant (high-k)

As we have seen in previous section, with scaling of oxide thickness below 1.5 nm such an ultra-thin gate oxide will induce high direct tunneling current (leakage gate current) therefore, it is required for high dielectric constant (k) material to replace SiO_2 as a gate dielectric to reduce standby power dissipation.



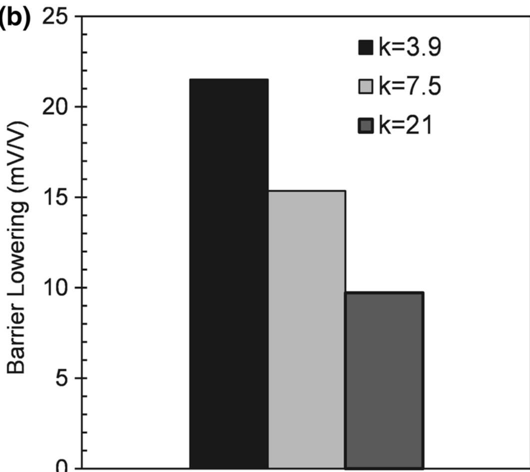


Fig. 12 **a** Conduction band and valence band energy variation along the channel for GEWE-SiNW MOSFET at different values of oxide thickness. **b** DIBL variation for GEWE-SiNW MOSFET for $V_{gs} = 0.6$ V and $V_{ds} = 0.4$ at different values of High-k

Figure 12a shows the variation of conduction band energy of GEWE-SiNW MOSFET at different values of high-k. As value of dielectric constant increases, the step in conduction band profile increases due to metal gate workfunction difference and also due to increased gate capacitance, thus providing improvement in DIBL. DIBL is significantly reduced as we increase the value of permittivity as is shown in Fig. 12b, thereby reflecting SCE immunity.

Figure 13 shows the variation of electric field with normalized position along the channel for GEWE-SiNW MOSFET. It is evident from the Fig. 13, the peak electric field at the interface of two metal gates increases with increase in permittivity value of insulators, which results in an improvement in average velocity of carriers. In addition, there is prominent reduction in field at the drain end due to incorporation of lower metal workfunction at the drain end and due to fact that gate capacitance is directly proportional to dielectric constant and as the dielectric constant increases the gate capacitance increases also the control of gate on the channel becomes stronger therefore enhances the driving capability of device and hence reduces field at the drain end.

Electron temperature in the channel decreases with increase in high k value as is evident from Fig. 14. As carriers move from source to drain, carrier temperature gradient is reduced significantly giving a remarkable reduction in electron temperature to 980 K for HfO_2 in comparison to 1018 K for SiO_2 as shown in Fig. 14, due to increased gate controllability of device and reduction of field at the drain end which results in enhancement of hot-carrier reliability.

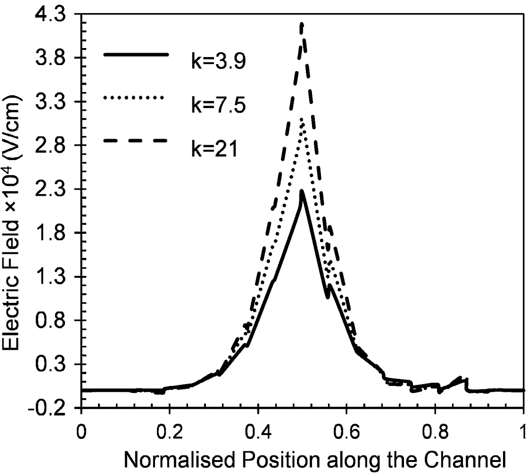


Fig. 13 Electric field for GEWE-SiNW MOSFET at different values of High-k

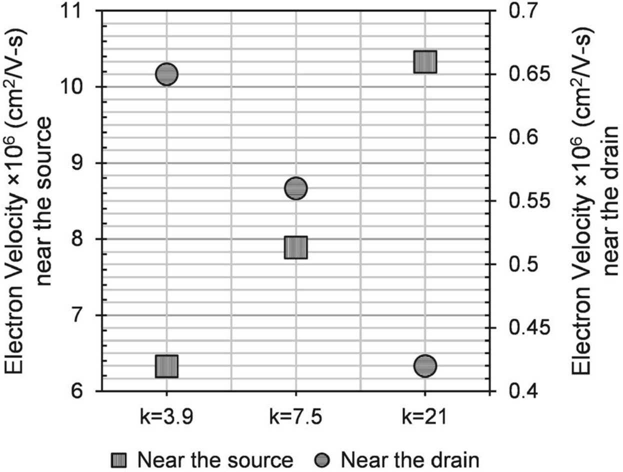


Fig. 15 Electron velocity for source and drain side for GEWE-SiNW MOSFET for $V_{gs} = 0.6$ V and $V_{ds} = 0.4$ at different values of High-k

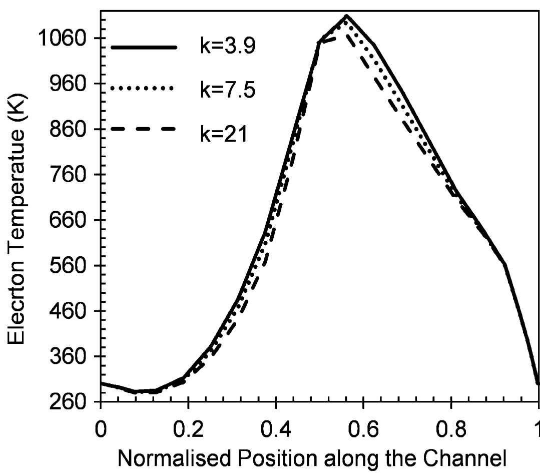


Fig. 14 Electron temperature variation along the channel for GEWE-SiNW MOSFET for $V_{gs} = 0.6$ V and $V_{ds} = 0.4$ at different values of High-k

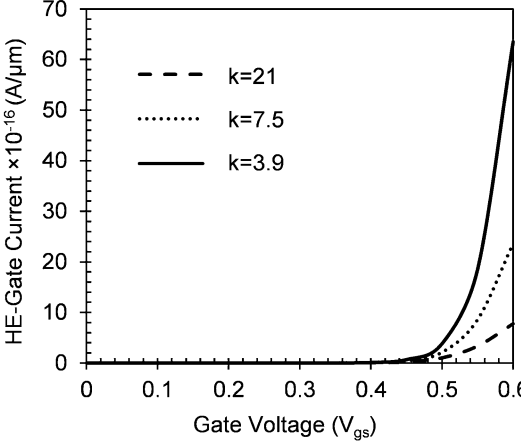


Fig. 16 Hot-electron injection gate current for GEWE-SiNW MOSFET at different values of High-k

Table 1 Extracted parameters at different values of oxide thickness and high-k

Permitivity value	Parameters		Oxide thickness		
			0.5 nm	1.5 nm	2.5 nm
k = 3.8 (SiO_2)	Electric field (×10^4 V/cm)	Near source	3.11	2.25	1.36
		Near drain	0.3	0.86	0.9
	Gate current (×10^{-16} A/μm)		123	7.77	0.75
	Electron temperature (K)		1043	1108	1131
	Electron mobility (cm^2/V -s)		1092	1020	897
	Electron velocity (×10^7 cm/s)	Near source	0.99	0.634	0.38
		Near drain	0.035	0.056	0.082
k = 7.5 (Si_3N_4)	Electric field (×10^4 V/cm)	Near source	3.66	3.0	1.98
		Near drain	0.2	0.22	0.24
	Gate current (×10^{-16} A/μm)		0.8	2.36	7.6
	Electron temperature (K)		1062.1	1091	1135.0
	Electron mobility (cm^2/V -s)		1112.1	1018	915.2
	Electron velocity (×10^7 cm/s)	Near source	1.2	0.78	0.56
		Near drain	0.013	0.056	0.004
k = 21 (HfO_2)	Electric field (×10^4 V/cm)	Near source	4.12	4.15	2.92
		Near drain	0.016	0.012	0.029
	Gate current (×10^{-16} A/μm)		0.55	0.7	1.2
	Electron temperature (K)		1047	1065	1116.6
	Electron mobility (cm^2/V -s)		1127	1066	962
	Electron velocity (×10^7 cm/s)	Near source	1.33	1.55	0.82
		Near drain	0.0108	0.042	0.0105

Figure 15 demonstrates the electron velocity of GEWE-SiNW MOSFET at different values of dielectric constant. It is evident from result, as dielectric constant increases from 3.9 to 21 electron velocity at source increases and decreases at drain end due to enhancement in electric field in the channel thus improves the carrier efficiency and reliability of device at low power applications.

The hot-electron gate current is due to the injection of hot-carriers into the oxide and transport of these carriers towards the gate electrode. Figure 16 shows the HE-I_g of GEWE-SiNW MOSFET at V_{ds} = 0.4 V. It is clearly shown than with incorporation of HfO_2, gate current (7.77 × 10^{-16} A/μm) decreases appreciably in comparison to SiO_2 (6.35 × 10^{-15} A/μm). This reduction in gate current is due to large gate capacitance which inhibits the tunneling of electrons at 1.5 nm oxide thickness. Thus reducing the power dissipation and finds its efficacy in low power analog applications. Table 1 gives the hot-carrier reliability metrics values for three different oxide thickness and dielectric values.

4 Conclusion

The present work proposes GEWE-SiNW MOSFET for improved hot carrier reliability applications over conventional and SiNW MOSFET. The reduction in electron velocity and electron temperature near the drain end is achieved with GEWE-SiNW MOSFET which reflects its effectiveness in high-performance applications where device reliability is a major concern. Furthermore, notable reduction in SCEs such as DIBL in GEWE-SiNW increases its current drive ability and also there is significant reduction in hot-electron gate current in GEWE-SiNW MOSFET compared to conventional MOSET, which results in improving its standby power consumption in electrical appliances and logic gates. Further, the scaling of oxide thickness shows an outstanding performance by GEWE-SiNW MOSFET with an exception of high HE-I_g at 0.5 nm. With incorporation of high-k, HE-Ig reduces significantly and improves the device reliability at 300 K. Thus, an oxide thickness 0.5 nm and oxide dielectric 21 (HfO_2) with GEWE-SiNW MOSFET is an effective candidate for low power CMOS applications such as amplifiers and switching applications.

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References

Arora N (2012) MOSFET models for VLSI circuit simulation: theory and practice. Springer, New York

ATLAS User's Manual (2014) SILVACO Int., Santa Clara, CA

Barsan RM (1981) Analysis and modeling of dual-gate MOSFET's. IEEE Trans Electron Devices 28:523–534. doi:10.1109/T-ED.1981.20377

Chaujar R, Kaur R, Saxena M, Gupta M, Gupta RS (2008) TCAD assessment of gate electrode workfunction engineered recessed channel (GEWE-RC) MOSFET and its multilayered gate architecture—part I: hot-carrier-reliability evaluation. IEEE Trans Electron Devices 55:2602–2612. doi:10.1109/TED.2008.2003085

Chen X, Tan CM (2014) Modeling and analysis of gate-all-around silicon nanowire FET. Microelectron Reliab 54:1103–1108. doi:10.1016/j.microrel.2013.12.009

De V, Borkar S (1999) Technology and design challenges for low power and high performance. In Proceedings of international symposium on low power electronics and design 163–168

Deb S, Singh NB, Islam N, Sarkar SK (2012) Work function engineering with linearly graded binary metal alloy gate electrode for shortchannel SOI MOSFET. IEEE Trans Nanotechnol 11:472–478. doi:10.1109/TNANO.2011.2177669

Dubey S, Santra A, Saramekala G, Kumar M, Tiwari PK (2013) An analytical threshold voltage model for triple material cylindrical gate all around (TMCGAA) MOSFETs. IEEE Trans Nanotechnol 12:766–774. doi:10.1109/TNANO.2013.2273805

Groeseneken GV (2001) Hot carrier degradation and ESD in submicrometer CMOS technologies: how do they interact? IEEE Trans Device Mater Reliab 1:23–32. doi:10.1109/7298.946457

Gupta N, Chaujar R (2014) Implications of transport models on the analog performance of gate electrode work function engineered (GEWE) SiNW MOSFET. IEEE 2nd international conference on devices, circuits and systems (ICDCS), 1–5. doi:10.1109/ICDCSyst.2014.6926154

Iwai H, Natori K, Shiraishi K, Iwata J, Oshiyama A, Yamada K, Ohmori K, Kakushima K, Ahmet P (2011) Si nanowire FET and its modeling. Sci China Inf Sci Springer 54:1004–1011. doi:10.1007/s11432-011-4220-0

Jeon HJ, Kim YB, Choi M (2009) Standby leakage power reduction technique for nanoscale CMOS VLSI systems. IEEE Trans Instrum Meas 59(5):1127–1133. doi:10.1109/TIM.2010.2044710

Kaur R, Chaujar R, Saxena M, Gupta RS (2007) Hot-carrier reliability and analog performance investigation of DMG-ISEGaS MOSFET. IEEE Trans Electron Devices 54:2556–2560. doi:10.1109/TED.2007.902855

Kranti A, Armstrong GA (2006) Engineering source/drain extension regions in nanoscale double gate (DG) SOI MOSFETs: analytical model and design considerations. Solid State Electron 50:437–447. doi:10.1016/j.sse.2006.02.012

Krieger G, Sikora R, Cuevas PP, Misheloff MN (2001) Moderately doped NMOS (M-LDD)-hot electron and current drive optimization. IEEE Trans Electron Devices 38:121–127. doi:10.1109/16.65745

Long W, Chin KK (1997) Dual material gate field effect transistor (DMGFET). Electron devices meeting tech dig 549–552. doi:10.1109/IEDM.1997.650445

Momose HS, Ono M, Yoshitomi T, Ohguro T, Nakamura S, Saito M, Iwai H (1996) 1.5 nm direct-tunneling gate oxide Si MOSFET's. IEEE Trans Electron Devices 43:1233–1242. doi:10.1109/16.506774

Mukherjee C, Maiti CK (2012) Silicon nanowire FinFETs. In: X. Peng (ed) Nanowires: recent advances. doi: 10.5772/52591

Nirmal D, Vijayakumar P, Thomas DM, Jebalin BK, Mohankumar N (2013) Subthreshold performance of gate engineered FinFET devices and circuit with high-k dielectrics. Microelectron Reliab 53:499–504. doi:10.1016/j.microrel.2012.09.008

Orouji AA, Kumar MJ (2005) Shielded channel double-gate MOSFET: a novel device for reliable nanoscale CMOS applications. IEEE Trans Device Mater Reliab 5:509–514. doi:10.1109/TDMR.2005.853505

Pan Y, Ng KK, Wei CC (1994) Hot-carrier induced electron mobility and series resistance degradation in LDD NMOSFE's. IEEE Electron Device Lett 15:499–501. doi:10.1109/55.338416

Sharma S (2012) Comparative analysis of low power and high performance PTM models of CMOS with HiK-metal gate technology at 22 nm. Int J Soft Comput Eng 2:257–261

Sharma D, Vishvakarma SK (2013) Precise analytical model for short channel cylindrical gate (CylG) gate-all-around (GAA) MOSFET. Solid-State Electron 86:68–74. doi:10.1016/j.sse.2012.08.006

Sinha SK, Chaudhury S (2013) Impact of oxide thickness on gate capacitance—a comprehensive analysis on MOSFET, nanowire FET, and CNTFET devices. IEEE Trans Nanotechnol 12:958–964. doi:10.1109/TNANO.2013.2278021

Sohn CW, Kang CY et al (2012) Device design guidelines for nanoscale FinFETs in RF/analog applications. IEEE Electron Device Lett 33:1234–1236. doi:10.1109/LED.2012.2204853

Stratton R (1972) Semiconductor current-flow equations (diffusion and degeneracy). IEEE Trans Electron Devices 19:1288–1292. doi:10.1109/T-ED.1972.17592

Suk SD, Lee S-Y, Kim S-M et al (2005) High performance 5 nm radius twin silicon nanowire MOSFET(TSNWFET): fabrication on bulk Si wafer, characteristics, and reliability. IEEE IEDM Tech Digest. doi:10.1109/IEDM.2005.1609453

Venkatesan S, Neudeck GW, Pierret RF (1992) Dual-gate operation and volume inversion in n-channel SOIMOSFET's. IEEE Electron Device Lett 13:44–46. doi:10.1109/55.144946

Wang R, Zhuge J, Huang R, Tian Y, Xiao H, Zhang L, Li C, Zhang X, Wang Y (2007) Analog/RF performance of Si nanowire MOSFETs and the impact of process variation. IEEE Trans Electron Devices 54:1288–1294. doi:10.1109/TED.2007.896598

Wang T, Lou L, Lee C (2013) A junctionless gate-all-around silicon nanowire FET of high linearity and its potential applications. IEEE Electron Device Lett 34:478–480. doi:10.1109/LED.2013.2244056

Yang G, Wang S, Wang R (2003) An efficient preconditioning technique for numerical simulation of hydrodynamic model semiconductor devices. Int J Numer Simul Electron Netw Devices Fields 16:387–400. doi:10.1002/jnm.507

Yu B, Wann CHJ, Nowak ED, Noda K, Hu C (1997) Short-channel effect improved by lateral channel engineering in deep-submicronmeter MOSFET's. IEEE Trans Electron Devices 44:627–634. doi:10.1109/16.563368

INVESTIGATION OF FREQUENCY DEPENDENT PARAMETER OF GEWE-SiNW MOSFET FOR MICROWAVE AND RF APPLICATIONS

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ABSTRACT

This paper presents the RF and high frequency performance of Gate Electrode Workfunction Engineered-Silicon Nanowire (GEWE-SiNW) MOSFET and the results so obtained are compared with Silicon Nanowire (SiNW) and Conventional MOSFET by using DEVEDIT-3D and ATLAS device simulator. The simulation results unfold the reduction in parasitic capacitances and lowering of intrinsic delay in GEWE-SiNW MOSFET. Furthermore, significant improvement in stern stability factor (K) has also been observed for GEWE-SiNW MOSFET as compared to conventional and SiNW MOSFETs, thus, reinforcing its use for high frequency wireless applications.

Keywords: Cut-Off Frequency (F_t), GEWE, Maximum Frequency (F_{max}), RF, Stability.

I. INTRODUCTION

The rapid growth of the mobile telecommunication markets emphasizes the need for reliable analog IC design at high frequencies. The RF performance of the Silicon MOSFET has been improved considerably during the late 1990s and early 2000s due to scaling of MOSFET. The reduction of the channel length in CMOS technologies has significantly improved the high frequency properties of the MOSFETs, making CMOS technology suitable for wireless communications and other RF applications [1-2]. Although, scaled technologies leads to undesirable effects such as short channel effects, leakage current, hot carrier effects (HCE), parasitic capacitances which results in degradation of device characteristics such as transconductance, voltage gains, subthreshold slope etc., which is unsuitable for RF/wireless applications [3]. GAA SiNW MOSET [4] is getting more attention for its advantages of small DIBL, small subthreshold swing etc. Also, it has found that their cut-off frequency can be much larger than that of planar Si-MOSFET [5]. Further, to enhance the carrier efficiency of a device, Zhou and Long [6] in 1999 proposed the concept of GEWE. With this scheme there is appreciable reduction in short channel effects and improvement in on-current due to step potential profile at the interface of metal gates owing to difference in metal workfunctions which results in enhanced lateral electric field allowing the carriers to travel faster hence improving the gate transport efficiency. Moreover, integration of GEWE scheme onto SiNW MOSFET ameliorates device efficiency, enhanced driving capability, minimizes short channel effects etc. [7-8]. Also, due to the increased demand for high-speed electronics products, the accurate analysis of the MOSFET at high frequencies (HF) is requisite to represent the behavior of device in microwave circuits and systems [9]. In

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this work, TCAD simulation tool is used to evaluate RF figure of merits of GEWE-SiNW MOSFET in terms of enhanced digital and RF performance of scaled devices in comparison to its conventional counterparts.

II. DEVICE STRUCTURE AND SIMULATION

Fig.1 shows a schematic cross-sectional view of GEWE-SiNW MOSFET where L1 and L2 are lengths of two different gate materials with workfunction Φ_{M1}=4.8eV and Φ_{M2}=4.4eV respectively. For n-channel MOSFET, we select two gate materials in such a way that the gate material having highest work function is placed near the source end and the gate material having lowest workfunction is placed near the drain end.

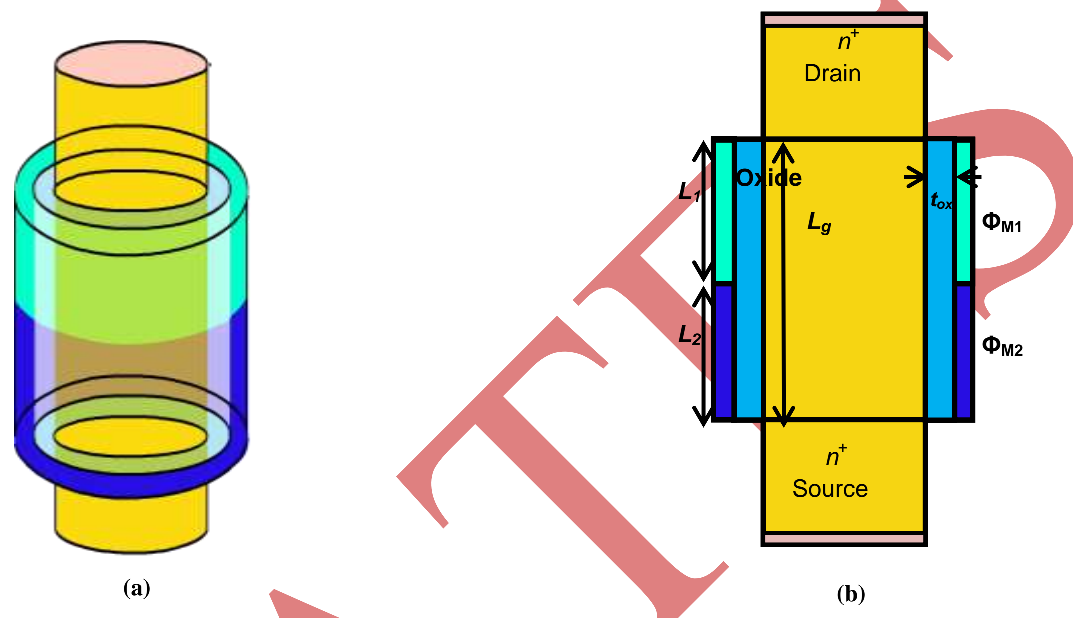
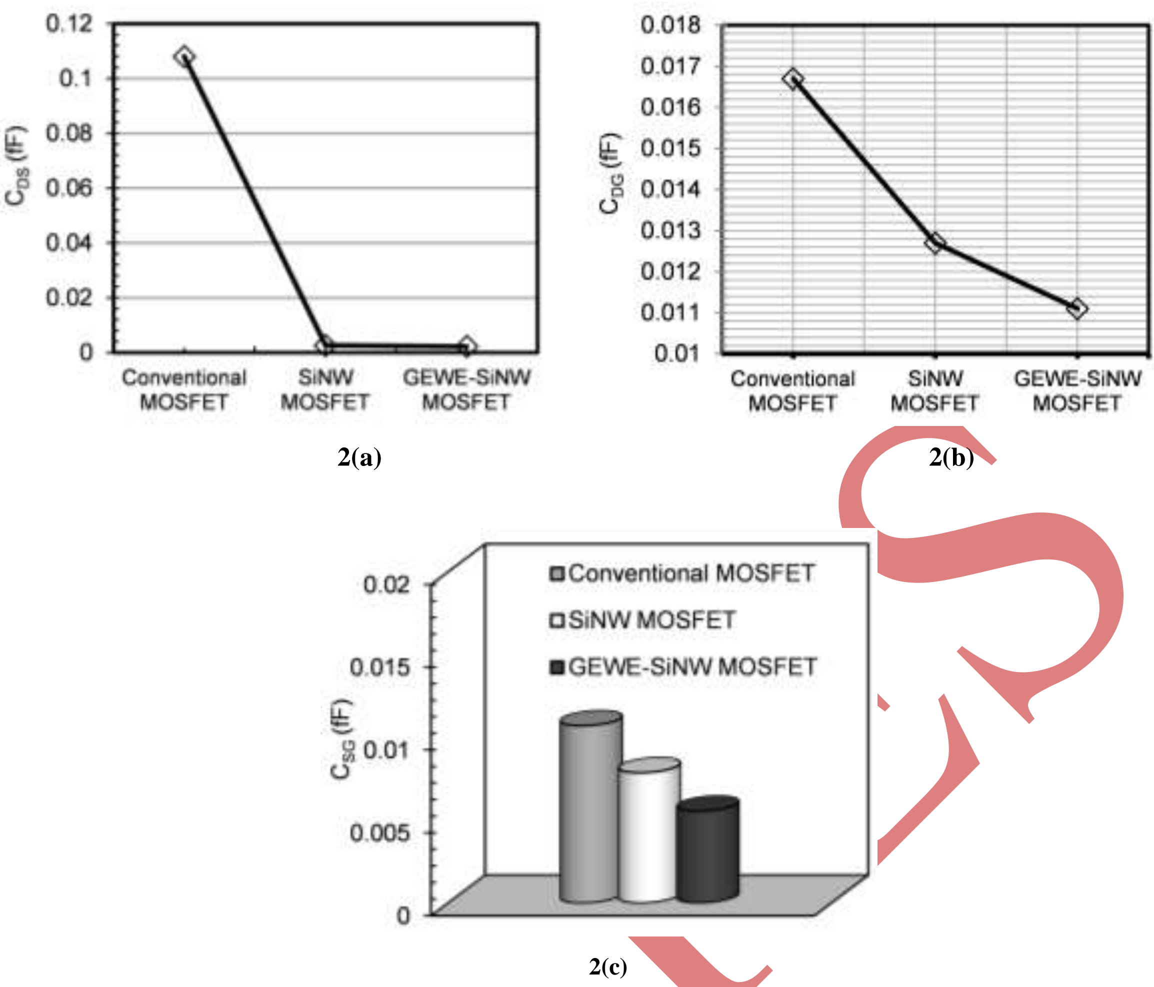


Fig. 1(a-b): Simulated structure and cross section of GEWE-SiNW MOSFET respectively

All the simulations have been performed using physical models accounting for the electric field-dependent and concentration-dependent carrier mobilities, Shockley–Read–Hall recombination/generation with doping dependent carrier lifetime, inversion layer Lombardi CVT mobility model, wherein concentration-dependent mobility, high field saturation model are all included [10]. In our simulation, we have adopted the hydrodynamic energy transport model which includes all nonlocal effects and is more accurate than the drift-diffusion method.

III. RESULTS AND DISCUSSION

In this paper, we compare GEWE-SiNW MOSFET with its conventional counterparts. The present analysis is carried out for a channel length, L_g=30 nm, radius of NW, R=5nm and thickness of oxide, t_{ox}= 1.5 nm, substrate doping concentration is $1\times10^{16}cm^{-3}$. It is evident from Fig. 2(a-c) that GEWE-SiNW exhibits smaller C_{SG}, C_{DG} and C_{DS} in comparison to its conventional MOSFET at 240 GHz due to metal gate workfunction difference which results in improved screening of conducting channel from drain variations. In addition, due to Silicon nanowire carrier mobility across the channel is enhanced [11-12], thereby reducing the parasitic capacitances. The higher value of these capacitances acts as an obstruction in device switching performance due to increase in the turn-on delay time.



2(a) 2(b)

2(c)

Fig. 2 (a-c): Parasitic capacitance (femto farad) of Drain to source, Drain to Gate and Source to gate for Conventional, SiNW and GEWE-SiNW MOSFET respectively at 240 GHz.

The stern stability factor (K) determines the stability of a device. This factor estimates whether the device is conditionally/unconditionally stable. It must satisfy the condition K>1 for a device to be unconditionally stable [13-15].

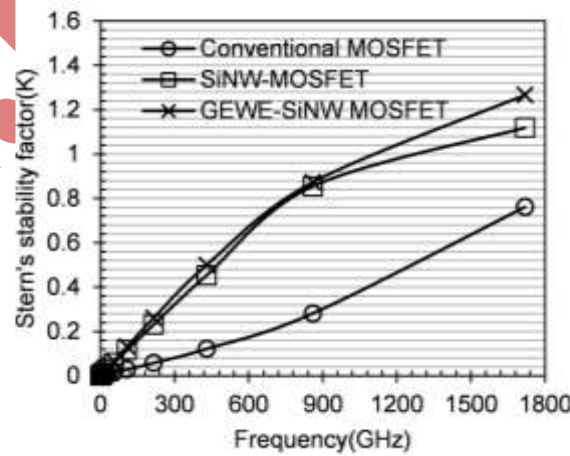
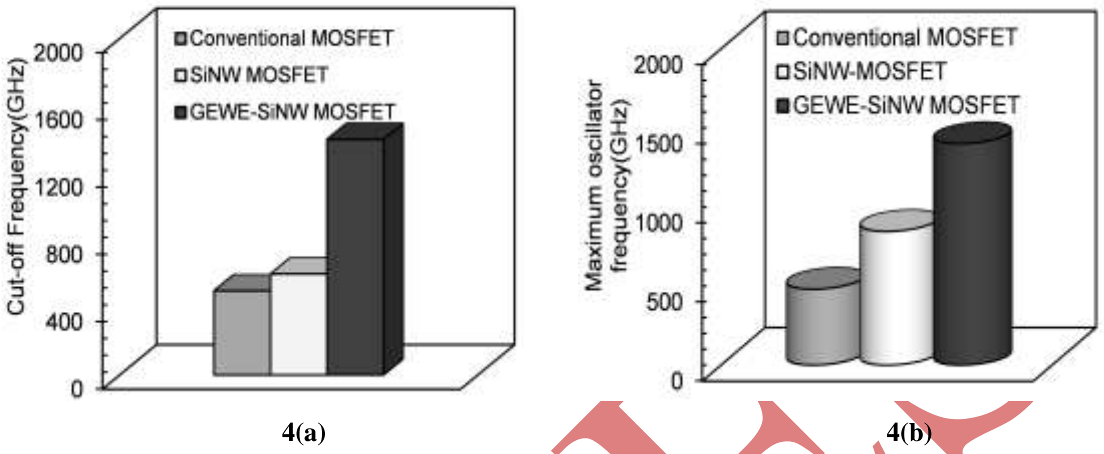


Fig. 3: Variation of Stern's stability (K) factor for Conventional, SiNW and GEWE-SiNW MOSFET

Fig. 3 shows the variation of stern's stability factor at higher frequencies. As is clear from the figure, K is significantly larger (greater than 1) as frequency increases, for GEWE-SiNW MOSFET in comparison to its counterpart where K is approaching 1.1 in SiNW MOSFET and 0.76 in conventional MOSFET. This is due to increased control of gate, which causes maximum power transfer from source to load. Hence, GEWE-SiNW is suitable for Low noise amplifier and RF applications.



4(a) 4(b)

Fig. 4: (a-b) Maximum oscillator frequency and Cut-off frequency for Conventional, SiNW and GEWE-SiNW MOSFET respectively

Further, the cut-off frequency f_T is the frequency when the current gain is unity, whereas f_{MAX} is the frequency when the power gain is unity [16-17]. f_T is a specification for high-speed digital applications (speed and high swing) while f_{MAX} analogous to the transit frequency of the maximum available power gain that is a realistic parameter of the optimization of microwave amplifiers. The f_{MAX}, as is seen from Fig.4 (a), for GEWE-SiNW MOSFET, is higher than for SiNW and Conventional MOSFET, which shows large parasitic capacitance in the conventional and SiNW MOSFET, thereby giving the GEWE-SiNW design a new strength for switching applications and wireless communication. Also, the use of metal gates results in reduced gate resistance, and hence increases in f_{MAX}. Fig. 4(b) shows the cut-off frequency of GEWE-SiNW MOSFET is greater than the cut-off frequency for bulk MOSFET. Due to the enhanced gate control over channel and screening of potential from drain side, it reduces the short channel effects and enhances the transconductance, leading to increase the cut-off frequency and packing density, thereby making the device suitable for CMOS wireless applications.

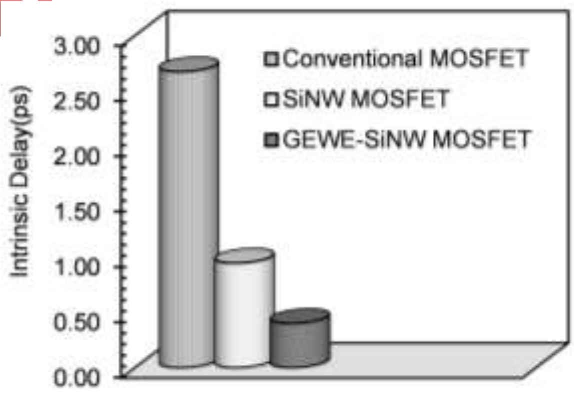


Fig. 5: Intrinsic Delay for Conventional, SiNW and GEWE-SiNW MOSFET

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The increasing capacitance between the gate and the overlapped S/D region degrades the intrinsic gate delay. Fig. 5 shows the comparison of GEWE-SiNW with SiNW and conventional MOSFET in terms of intrinsic delay parameter. As is evident from the figure, there is notable reduction in intrinsic delay of GEWE-SiNW MOSFET than its conventional counterparts due to cylindrical gate which increases on-current, reduces parasitic capacitances and incorporation of two dissimilar metal gates, which leads to considerable reduction of intrinsic delay by 55.5%.

IV. CONCLUSION

In this work, we have investigated the improved RF performance of GEWE-SiNW MOSFET and compared it with conventional and SiNW MOSFET, it has been scrutinized that GEWE SiNW MOSFET exhibit lower parasitic capacitances, enhanced cut-off and maximum frequency with an appreciably low intrinsic delay, hence suitable for RF/wireless applications. Furthermore, GEWE-SiNW is found to be more stable than its conventional counterparts, thereby providing its efficacy for high-performance RF applications.

V. ACKNOWLEDGMENT

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REFERENCES

[1] Larson, L. E., "Silicon technology tradeoffs for radio-frequency/mixed-signal system-on-a-chip", IEEE Trans Electron Devices 50(3), 2003, 683–99.

[2] Saijets. J., Andersson. M. and Berg. M. A., "A Comparative Study of Various MOSFET Models at Radio Frequencies", Analog Integrated Circuits and Signal Processing 33(1), 2002, 5–17

[3] Chen. Q., "Compact Modeling of Multi-Gate MOSFETs for RF Designs", IEEE International Wireless Symposium, Bejing , 2013, 1-4

[4] Kim. D. W., Yeo. K. H., Suk. S. D., Li. M., Yeoh. Y. Y., Kyun. S. D. and Chung. C., "Fabrication and electrical characteristics of self-aligned (SA) gate-all-around (GAA) Si nanowire MOSFETs (SNWFET)", IC Design and Technology (ICICDT), IEEE International Conference, 2010, Grenoble, 63-66.

[5] Wang. C., Zhuge. C., Huang. R., Tian. Y., Xiao. H., Zhang. L., Li. C., Zhang. X. and Wang. Y., "Analog/RF performance of Si nanowire MOSFETs and the impact of process variation", IEEE Trans. Electron Devices 54(6), 2007, 1288–1294.

[6] Long. W. and Chin. K. K., **"**Dual Material Gate Field Effect Transistor (DMGFET)", Electron Devices Meeting Tech Dig., 1999, Washington, DC, USA, 549-552.

[7] Gupta. N and Chaujar. R, "Implications of Transport models on the analog performance of gate electrode workfunction engineered (GEWE) SiNW MOSFET", IEEE Second International conference on Devices, Circuits and Systems (ICDCS'2014), 2014, Coimbatore, India, 278-282.

IJATES

[8] Gupta. N, Chaujar. R and Kumar. A, "Simulation analysis of Gate Electrode Workfunction Engineered (GEWE) Silicon Nanowire MOSFET for hot carrier reliability", IEEE 1st International conference on Microelectronics, Circuits and Systems, 2014, Kolkata, India, 150-153

[9] Doan. C.H., Emami. S., Niknejad. A.M. and Brodersen. R.W., "Millimeter-wave CMOS design", IEEE J. Solid-State Circuits 40(1), 2005, 144–155.

[10] ATLAS User's Manual, SILVACO Int., Santa Clara, 2011, CA.

[11] Frey. M., Esposito. A. and Schenk. A., "Computational comparison of conductivity and mobility models for silicon nanowire devices", J. Appl. Phys. 109(8), 2011, 083707 - 083707-6

[12] Ramayya. E. B., Vasileska. D., Goodnick. R.W. and Knezevic. I., "Electron Mobility in Silicon Nanowires", IEEE Transactions on Nanotechnology, 6(1), 2008, 113-116.

[13] Voldman. S. H., (ESD: RF technology and circuits, Wiley, 2006)

[14] Cho. S., Kim. K. R., Park. B. G. and Kang. I. M., "RF performance and small-signal parameter extraction of junctionless silicon nanowire MOSFETs", IEEE Trans. Electron Devices 58(5), 2011, 1388–1396.

[15] Oh. Y. and Rieh. J. S., "Effect of Device Layout on the Stability of RF MOSFETs", IEEE Transactions on Microwave Theory and Techniques 61(5), 2013, 1861-1869.

[16] Nae. B., Lazaro. A. and Iniguez. B., "High Frequency and Noise Model of Gate-All-Around MOSFETs, Spanish Conference on Electron Devices", 2009, Santiago de Compostela, 112-115.

[17] Sarkar. A., De. S., Dey. A. and Sarkar. C. K., "Analog and RF performance investigation of cylindrical surrounding-gate MOSFET with an analytical pseudo-2D model", Journal of Computational Electronics, 2012, 11(2), 182-185.

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