A DISSERTATION ON

CURRENT CONVEYOR BASED VLSI DESIGN

SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENT FOR THE AWARD OF THE DEGREE OF

MASTER OF TECHNOLOGY
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CERTIFICATE

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This is certified that the dissertation entitled "**Current Conveyor Based VLSI Design"** is a work of **Yogendra Singh Baghel** (University Roll No. – 2K11/VLS/12) is a student of Delhi Technological University. This work is completed under my direct supervision and guidance and forms a part of Master of Technology (Electronics & Communication Engineering) course and curriculum. He has completed his work with utmost sincerity and diligence.

The work embodied in this major project has not been submitted for the award of any other Institute / University for the award of any other degree to the best of my knowledge.

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ABSTRACT

Current conveyor is a current mode circuit. In recent years, the current conveyor is receiving considerable attention as they offer analog designers some significant advantages over the conventional op-amp. The current conveyor is a good choice for low voltage applications. It provides some notable features like high gain-bandwidth product ,flexibility of driving current or voltage signal output at its two separate nodes, relatively high slew rate, reduced supply voltage of integrated circuits. In addition, it requires smaller number of passive components to perform a specific function. Hence, it is suitable for both current and voltage mode devices. Current mode design technique offers voltage independence, high bandwidth in analog circuits with properties of accuracy and versatility in a wide range of applications. In this report we present a rail-to-rail low voltage (±2.5 V) differential current conveyor (DDCC) circuit in standard CMOS technology that is suited for low voltage operation. The simulated circuit uses a low-voltage current-mirror. In this report, a few applications of the DDCC like Full Wave Rectifier , Quadrature Oscillator and Current Multiplier & Divider have also been simulated. For simulation, 0.5 µm technology of SPICE has been used. The need for low-voltage low-power circuits is immense in portable electronic equipments like laptop computers, pace makers, cell phones etc. Voltage Mode Circuits are rarely used in low-voltage circuits as the minimum bias voltages depend on the threshold voltages of the MOSFETs

TABLE OF CONTENTS

LIST OF FIGURES

CHAPTER-1

1.1 INTRODUCTION

THE current-conveyor [1], published in 1968, represented the first building block intended for current signal processing. In 1970 appeared the enhanced version of the current-conveyor: the second-generation current-conveyor CCII. They used high quality PNP - NPN transistors of a like polarity and match each other but difference in current gain reduced the circuit accuracy. This is due to the base current error. The other current conveyor was devised in 1984 by G. Wilson where another current-mirror configuration; known as Wilson current mirror was employed. It consists of an operational amplifier and external PNP transistors. A second generation current conveyor (CCII) was presented in 1990 using an operational amplifier and external CMOS transistors. Both circuits were subject to the OP-AMP performance and again to the transistor mismatching. During that time, research societies started to notice that the voltage-mode operational amplifier is not necessarily the best solution to all analogue circuit design problems. New research findings regarding current mode signal processing using current-conveyors were presented. Furthermore, a commercial product became available: the current-feedback operational amplifier. The high slew rate and wide bandwidth of this amplifier resulted in its popularity in video amplifier applications. The current conveyor is receiving considerable attention as they offer analog designers some significant advantages over the conventional op-amp. These advantages can be pointed out as follows:

- Improve AC performance with better linearity.
- Wider and nearly constant bandwidth independent of closed loop gain.
- Relatively High slew rate (typically 2000V/us).
- Flexibility of driving current or voltage signal output at its two separate nodes, hence suitable for current and voltage mode devices.
- Reduced supply voltage of integrated circuits.
- Accurate port transfer ratios equal to unity hence employed in low sensitivity design.
- Requirement of smaller number of passive components to perform a specific function.

In 1988 the principle of a MOS current copier was presented , which enabled analogue circuit designers to design different Current Conveyors using only MOS-transistors.

Therefore, apart from above advantages following are the driving force behind the development of MOS Current Conveyor:

 Analog VLSI addresses almost all real world problems and finds exciting new information processing applications in variety of areas such as integrated sensors, image processing, speech recognition, hand writing recognition etc.

The need for low-voltage low-power circuits is immense in portable electronic equipments like laptop computers, pace makers, cell phones etc. Voltage Mode Circuits are rarely used in low-voltage circuits as the minimum bias voltages depend on the threshold voltages of the MOSFETs. However, in current mode circuits (CMCs), the currents decide the circuit operation and enable the design of the systems that can operate over wide dynamic range. MOS current-mirrors are more accurate and less sensitive to process variation. Therefore, MOS-transistor circuits should be simplified by using current signals in preference to voltage signals. For this reason, integrated current mode system realizations are closer to the transistor level than the conventional voltage-mode realizations. When signals are widely distributed as voltages, the parasitic capacitances are charged and discharged with the full voltage swing, which limits the speed and increases the power consumption of voltage-mode circuits. Current-mode circuits cannot avoid nodes with high voltage swing either but these are usually local nodes with less parasitic capacitances. Therefore, it is possible to reach higher speed and lower dynamic power consumption with current-mode circuit techniques. Current-mode interconnection circuits in particular show promising performance.

1.2: BASIC CURRENT CONVEYOR

A CC is a three or more port (X, Y, Z) network.

Whose input-output relationship is given by:

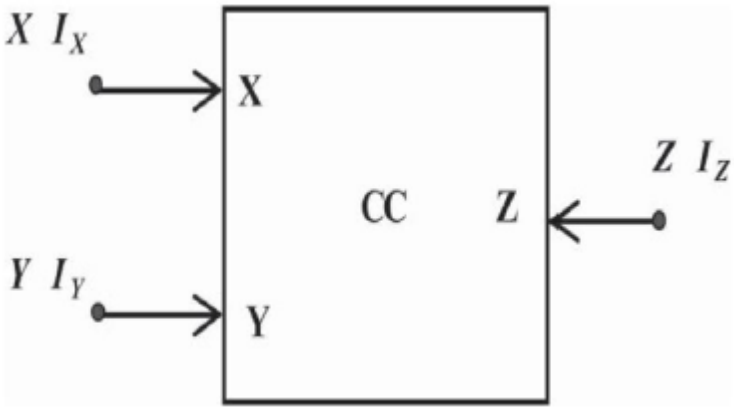

Figure: 1.1 Basic current conveyor

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & A & 0 \\ B & R_X & 0 \\ 0 & C & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix}$$

where A, B, C assume a value either 1, 0 or – 1 and RX is the intrinsic resistance offered by the port X to the input currents. For an ideal CC VX = VY and the input resistance (RX) at port X is zero[1]. But in practical CCs, RX is a nonzero positive value. The commonly used block representation of a CC is shown in Figure 1, where X and Y are the input terminals and Z is the output terminal.

Second-generation current conveyors (CCll) [2] is possessed a very high slew rate and bandwidth compared to the traditional op-amp. This makes the CCII of primary importance in the design of modem analog integrated circuits. Several circuits based on CCII for realizing full-wave rectification have been proposed in the literature .The circuits employ diodes and resistors in addition to CClls. The circuit employs bipolar current mirrors in addition to a CCII and a number of resistors. circuit employs four CCClls and resistors. The circuit employs two CCII and two MOS transistors. However, all of these circuits suffer from an excessive number of active of passive components. Recently, the full-wave rectifier circuit realized by using All MOS transistors has been reported, it is suitable for implementation in monolithic form.

Current conveyors have found wide use in a variety of electronic applications since their inception**.** The advantages of processing current-mode signals have led to an increase in interest and activities in the area of current-mode signal processing. Although much research on current conveyor circuits has been done in recent years, circuits employing CCIIs have received the most attention. Both CCI and CCII can be used in the CCCS based adjoint networks obtained from voltage mode circuits to realize current-mode cascadable biquadratic circuits having zero input impedance**.** However, cascadable current-mode complex pole circuits having high output impedance and utilizing a single CCI as the only active device have only been reported for an all-pass network.

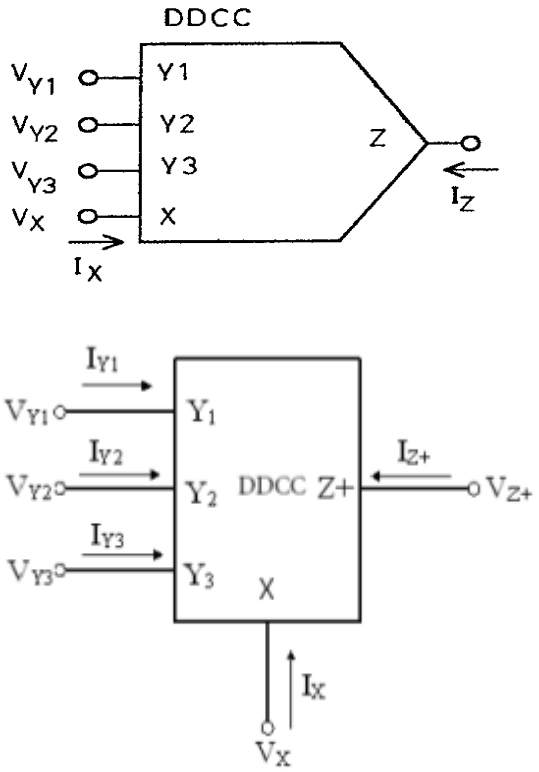

Figure: 1.2 Block dig of CCII

At present, the first- and second-generation current-conveyors are widely used for vlsi design and implementation of high performance current-mode and voltage-mode analog electronic circuits. These conveyors have a fixed current gain = k. Current-conveyors with arbitrary current gains are more attractive, especially for the realization of current mode counterparts of the classical voltage-mode analog electronic circuits. This explains the recent growing interest in designing variable gain current-conveyors and current controlled current-conveyors. In variable-gain current-conveyors are realized using two operational amplifiers, two resistors and a couple of cross-coupled cui-rent-mirrors. These realizations are not suitable for monolithic implementation and are intended for discrete designs only. In the current-conveyor input-cell is tied from a mixed translinear loop composed of complementary bipolar transistors**.** In these realizations, the bias-dependent output parasitic resistance on port *X* is exploited to advantage for realizing current-controlled conveyors. While this realization is suitable for monolithic implementation, it exhibits the

disadvantages which result from the temperature dependence of the parasitic bias-dependent output resistance on port *X* .

The electrical symbol of DDCC is shown in Fig. 1.1. It has three voltage input terminals: Y1, Y2 and Y3, which have high input impedance. Terminal X is a low impedance current input terminal. There is a high impedance current output terminal Z. The CMOS realization of the DDCC is shown in Fig. 2. The input-output characteristics of ideal DDCC is described as

$$I_{Y1} = I_{Y2} = I_{Y3} = 0$$
$$V_X = V_{Y1} - V_{Y2} + V_{Y3}$$
$$I_Z = \pm I_X$$

CHAPTER-2

BLOCKS USED IN ANALOG DESIGN

2.1 TRANSIMPEDANCE AMPLIFIER

Transimpedance amplifier[2] consists of an inverting amplifier accepting the input signal in form of a current from a high impedance signal source, such as a photodiode or a semiconductor based detector for radiation particles, and converts it into an output voltage. The transimpedance at DC and low frequencies is $\frac{v_o}{i} = R_f$. However, the high impedance signal source inevitably has a stray capacitance C_i , which deprives the amplifier from the feedback at high frequencies. Therefore the amplifier's feedback loop must be stabilized by a suitably chosen phase margin compensation capacitance C_f . Owed to the presence of these capacitances, and because of the amplifier's own limitations, the system response at high frequencies will be reduced accordingly.

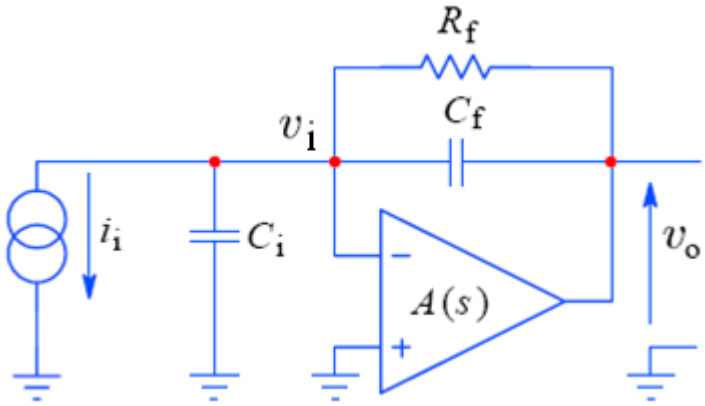

Figure 2.1 Generalized transimpedance system schematic diagram

The amplifier's inverting open loop voltage gain is modeled as:

$$\frac{v_o}{v_i} = -A(s) = -Ao\frac{-So}{S-So} = -Ao\frac{\omega o}{S+\omega o} \qquad (2.1)$$

where: S is the complex frequency variable;

A_O is the amplifier's open loop DC gain;

S_O is the amplifier's real dominant pole, so that:

$\omega o = 2\pi f_O$, f_o is the open loop cutoff frequency

2.2 OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

The operational transconductance amplifier (OTA) is an amplifier whose differential input voltage produces an output current [3]. Thus, it is a voltage controlled current source (VCCS). There is usually an additional input for a current to control the amplifier's transconductance. The OTA is similar to a standard operational amplifier in that it has a high impedance differential input stage and that it may be used with negative feedback.

The OTA is not as useful by itself in the vast majority of standard op-amp functions as the ordinary op-amp because its output is a current. One of its principal uses is in implementing electronically controlled applications such as variable frequency oscillators and filters and variable gain amplifier stages which are more difficult to implement with standard op-amps. In the ideal OTA, the output current is a linear function of the differential input voltage, and is given by:

$$I_{out} = (V_{in+} - V_{in-}).g_m \tag{2.2a}$$

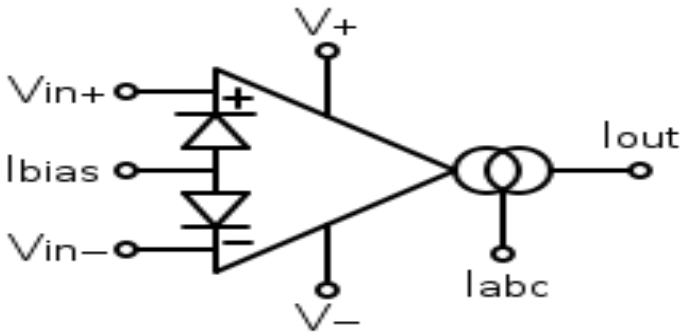

Figure 2.2 OTA Model

The amplifier's output voltage is the product of its output current and its load resistance:

$$V_{out} = I_{out} \,.\, R_d \tag{2.2b}$$

The voltage gain is then the output voltage divided by the differential input voltage:

$$G_{voltage} = R_d \,.\, g_m \tag{2.2c}$$

The transconductance of the amplifier is usually controlled by an input current, denoted I_{abc} . The amplifier's transconductance is directly proportional to this current. This is the feature that makes it useful for electronic control of amplifier gain, etc.

As an ideal OTA is usually considered to have the following properties and they are considered to hold for all input voltages:

- Infinite input impedance
- Infinite output impedance (i.e., $R_{out} = \infty$).
- G_m is variable and $G_m = \frac{I_{abc}}{2V_T}$, we cannot make G_m infinite.

2.3 CURRENT FEEDBACK OPERATIONAL AMPLIFIER

The current feedback operational amplifier (CFOA) is a type of electronic amplifier whose inverting input is sensitive to current, rather than to voltage as in a conventional voltage-feedback operational amplifier (VFA). The CFA was invented by David Nelson at Comlinear Corporation, and first sold in 1982 as a hybrid amplifier, the CLC103. The first integrated circuits CFAs were introduced in 1987 by both Comlinear and Elantec (designer Bill Gross). They are usually produced with the same pin arrangements as VFAs, allowing the two types to be interchanged without rewiring when the circuit design allows. In simple configurations, such as linear amplifiers, a CFA can be used in place of a VFA with no circuit modifications, but in other cases, such as integrators, a different circuit design is required. The circuit symbol of CFOA is as shown in fig.2.3. Its port relations can be characterized by the following matrix form:

$$\begin{bmatrix} I_y \\ V_x \\ I_z \\ V_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \\ I_o \end{bmatrix}$$

Therefore, this active element can be characterized with the following equations:

$i_y=0,\ v_x = v_y,\ i_{z=i_x},\ v_o = v_z$
(2.3)

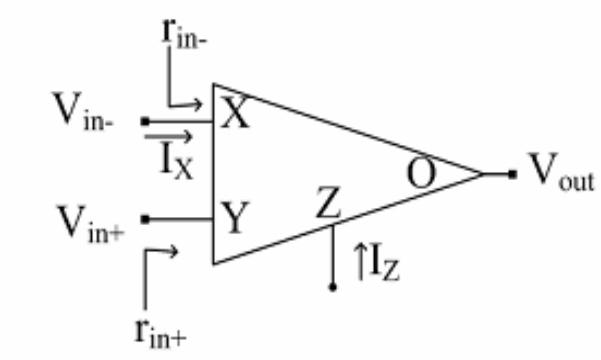

Figure.2.3 Circuit Symbol of CFOA

Current-Feedback Operational Amplifiers (CFOAs) are employed as an alternative to conventional voltage opamps because of their inherent advantages:

- The CFOA closed-loop bandwidth is independent of its close-loop gain, provided that the feedback resistance is kept constant
- The CFOA input and output stages work both in class AB and give high slew-rate values AD844A is CFOA chip which is commercially available in the market.

2.4 OPAMP

An operational amplifier, which is often called an op-amp, is a DC-coupled high-gain electronic voltage amplifier with a differential input and, usually, a single-ended output. Ideally the op-amp amplifies only the difference in voltage applied between its two inputs (V_+ andV_-), which is called the differential input voltage. The output voltage of the op-amp is given by the equation,

$$V_{out} = (V_+ - V_-).G_{open-loop} \quad (2.4)$$

Where V_+ is the voltage at the non-inverting terminal and V_- is the voltage at the inverting terminal and G open-loop is the open-loop gain of the amplifier.

The ideal operation is difficult to achieve and the non-ideal conditions often raise limitations like finite impedances and drift, their primary limitation being not especially fast. The typical performance degrades rapidly for frequencies greater than 1MHz, although some models are designed especially for higher frequencies. High input impedance at the input terminals (ideally infinite) and low output impedance at the output terminal(s) (ideally zero) are important typical characteristics. The other important fact about op-amps is that their open-loop gain is huge. This is the gain that would be measured from a configuration in which there is no feedback loop from output back to input. A typical open-loop voltage gain is ~ 10^4 -10^5 .

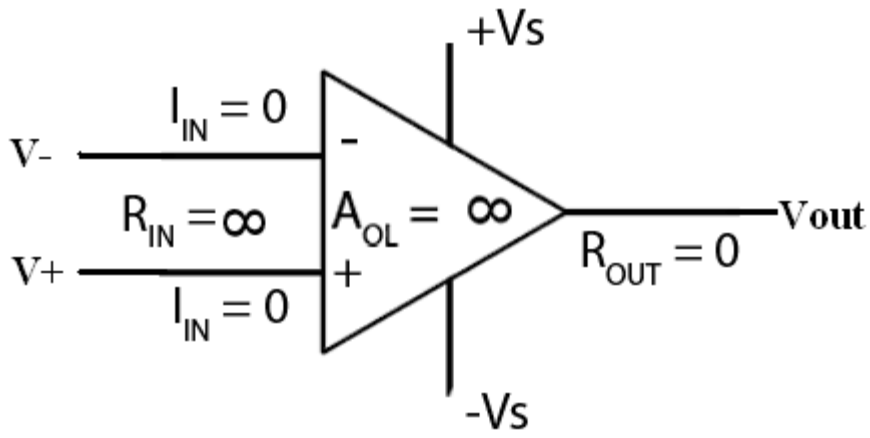

Figure 2.4 Ideal internal circuit of Op-amp

An ideal op-amp is usually considered to have the following properties, and they are considered to hold for all input voltages:

- Infinite open-loop gain.
- Infinite voltage range available at the output (V_{out}) (in practice the voltages available from the output are limited by the supply voltages Vs_+ and Vs_-)
- Infinite bandwidth
- Infinite input impedance
- Zero input current
- Zero input offset voltage

- ❖ Infinite slew rate
- ❖ Zero output impedance
- ❖ Infinite Common-mode rejection ratio (CMRR)
- ❖ Infinite Power supply rejection ratio for both power supply rails.

2.5 CURRENT CONVEYOR

The current conveyor (CC) is the basic building block of a number of applications both in the current and voltage and the mixed modes. The principle of the current conveyor of the first generation was published in 1968 by K. C. Smith and A. S. Sedra [3]. Two years later, today's widely used second-generation CCII was described in [4], and in 1995 the third-generation CCIII [5]. However, initially, during that time, the current conveyor did not find many applications because its advantages compared to the classical operational amplifier were not widely appreciated. An IC Current Conveyor, namely PA630, was introduced by Wadsworth in 1989 and about the same time, the now well known CFOA AD844 was recognized to be internally a CCII+ followed by a voltage follower [6]. Today, the current conveyor is considered a universal analog building block with wide spread applications in the current mode, voltage mode, and mixed mode signal processing. Several generations of current conveyors have been defined over the years. Undoubtedly, the second generation conveyor (CCII) is the more well known of the device. The terminal relations of a CCII can be characterized by

$$\begin{bmatrix} V_x \\ I_y \\ I_z \end{bmatrix} = \begin{bmatrix} \beta & 0 & 0 \\ 0 & 0 & 0 \\ 0 & \pm\alpha & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix}$$

where $\alpha = 1 - \epsilon_i$ and $\beta = 1 - \epsilon_v$,$| \epsilon_i | << 1$ and $| \epsilon_v | << 1$ (2.5)

represent the current and voltage tracking errors, respectively, where the subscripts x, y, and z refer to the terminals labeled X, Y and Z in fig1 The CCII is defined in both a positive and a negative version where the +sign in the matrix is used for the CCII+ type conveyor and the –sign is used for the CCII- type conveyor. Its features find most

applications in the current mode, when its voltage input y is grounded and the current, flowing into the low-impedance input x, is copied by a simple current mirror into the z output.

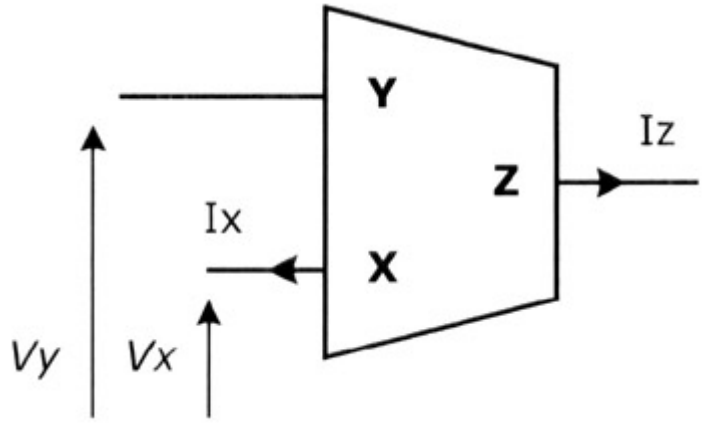

Figure 2.5 Block diagram of CCII

2.6 OPERATIONAL TRANSRESISTANCE AMPLIFIER

As signal processing extends to higher frequencies, traditional design methods based on voltage op-amps are no longer adequate. It is well known that a traditional operational amplifier has bandwidth which is dependent on the closed-loop voltage gain. The attempt to overcome this problem has led to a renewed interest in circuits which operate in current mode.

The OTRA is a current mode device that uses current mirrors and common source amplifier to give a current difference signal as input which in turn produce an appropriate voltage signal as output. The OTRA is a three terminal analog building block. Both the input and output terminals are characterized by low impedance. The circuit symbol of the OTRA is illustrated in Fig.2.6. The port relations of an OTRA can be characterized by the following matrix form [7].

$$\begin{bmatrix} v_p \\ v_n \\ v_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{bmatrix} \begin{bmatrix} i_p \\ i_n \\ i_z \end{bmatrix}$$

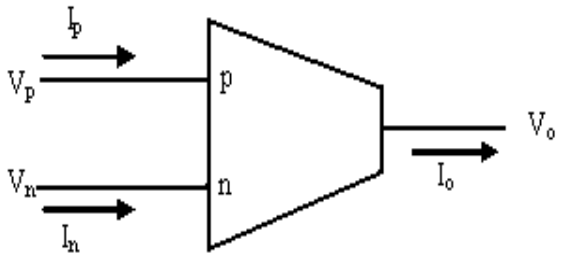

Figure 2.6 Circuit symbol of OTRA

It eliminates response limitations incurred by capacitive time constants leading to circuits that are insensitive to the stray capacitances at the input terminals. For ideal OTRA, the Transresistance gain, R_m, approaches infinity and external negative feedback must be used which forces the input currents to be equal [8]. Thus the OTRA must be used in a negative feedback configuration. Practically the Transresistance gain is finite and its effect should be considered.

The important advantages offered by OTRA are:

- Since the OTRA has one output terminal with low impedance and two input terminals that are virtually grounded, most effects of parasitic capacitances disappear and the remainder can be compensated without adding any extra components.
- Using current feedback techniques, OTRAs have a bandwidth almost independent of the closed loop-voltage gain.
- Due to the input terminals being virtually grounded, they are cascadable.

2.7 CURRENT DIFFERENCING TRANS-CONDUCTANCE AMPLIFIER

Current differencing transconductance amplifier (CDTA) is a new active circuit element. The CDTA is free from parasitic input capacitances and it can operate in a wide frequency range due to current mode operation. Some voltage and current mode applications using this element have already been reported in literature, particularly from the area of frequency filtering: general higher-order filters, biquad circuits, all-pass sections, gyrators,

simulation of grounded and floating inductances and LCR ladder structures. Other studies propose CDTA-based high-frequency oscillators. Nonlinear CDTA applications are also expected, particularly precise rectifiers, current-mode Schmitt triggers for measuring purposes and signal generation, current-mode multipliers, etc.

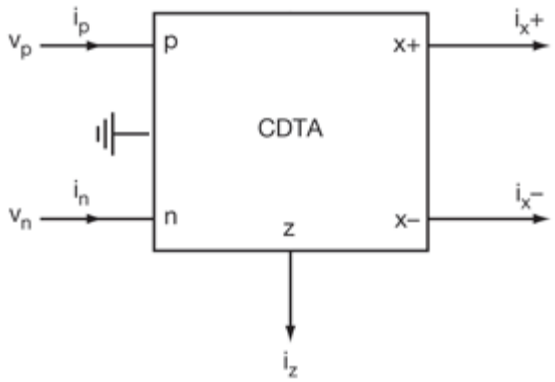

Figure 2.7 Block diagram of CDTA

The CDTA element with its schematic symbol in Fig 2.7 has a pair of low-impedance current inputs p, n and an auxiliary terminal z, whose outgoing current is the difference of input currents. Here, output terminal currents are equal in magnitude, but flow in opposite directions, and the product of transconductance (g_m) and the voltage at the z terminal gives their magnitudes. Therefore, this active element can be characterized with the following equations:

1. $V_P = V_N = 0$, (2.6a)
2. $I_Z = I_P - I_N$ (2.6b)
3. $I_{X+} = g_m V_Z$ (2.6c)
4. $I_{X-} = -g_m V_Z$. (2.6d)

Where $V_{Z-} = I_Z Z_Z$ and Z_Z is the external impedance connected to z terminal of the CDTA. CDTA can be thought as a combination of a current differencing unit followed by a dual-

output operational transconductance amplifier, DO-OTA. Ideally, the OTA is assumed as an ideal voltage-controlled current source and can be described by $I_X = g_m(V_+ - V_-)$, where I_X is output current, V_+ and V_- denote non-inverting and inverting input voltage of the OTA, respectively. Note that g_m is a function of the bias current. When this element is used in CDTA, one of its input terminals is grounded (e.g., V_- = 0V). With dual output availability, $I_{X+} = -I_{X-}$ condition is assumed.

2.8 CURRENT DIFERENCING BUFFERED AMPLIFIER

CDBA, current differencing buffered amplifier, is a multi-terminal active component with two inputs and two outputs [9]. Its block diagram can be seen from figure 2.8. It is derived from current feedback amplifier (CFA).

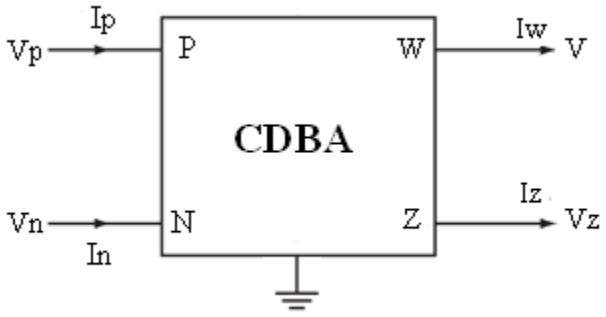

Figure 2.8 Block Diagram for CDBA

The characteristic equation of this element can be given as:

1. $V_P = V_N = 0$ (2.7a)

2. $I_Z = I_P - I_N$ (2.7b)

3. $V_W = V_Z$ (2.7c)

Here, current through z-terminal follows the difference of the currents through p-terminal and n-terminal. Input terminals p and n are internally grounded. The difference of the input currents are converted into the output voltage V_W, therefore CDBA element can be considered as a special type of current feedback amplifier with differential current input and grounded y input.

The CDBA is simplifying the implementation, free from parasitic capacitances, able to operate in the frequency range of more than hundreds of MHz (even GHz), and suitable for current mode operation while, it also provides a voltage output. Several voltage and current mode continuous-time filters, oscillators, analog multipliers, inductance simulators and a PID controller have been developed using this active element.

The CDBA offers several advantageous features viz., high slew rate, improved bandwidth, and accurate port tracking characteristics when configured with a pair of matched current feedback amplifier (AD-844-CFA) devices which leads to extremely low active circuit sensitivity.

CHAPTER-3

LITERATURE SURVEY

Extensive literature survey shows that a lot of work has been done on current mode logic devices using the current conveyors. The analog integrated circuit design in current mode is receiving increased attention due to some potential performance features like wide bandwidth, less circuit complexity, wide dynamic range, low power consumption, and high operating speed. The current mode approach has emerged as an alternate method besides the traditional voltage mode circuits. The current mode active elements are appropriate to operate with signals in current or voltage or mixed mode and are gaining acceptance as building blocks in high-performance circuit designs. A number of current mode active elements such as operational transconductance amplifier (OTA), current conveyors (CCs), differential voltage current conveyor (DVCC), differential difference current conveyor (DDCC) , current feedback operational amplifier (CFOA) are available in the literature. Full-wave rectifier is used in RF demodulator, piecewise linear function generator, AC voltmeter, watt meter, and various nonlinear analog signal processing circuits. The typical rectifier realizes by using diodes but this device cannot rectify signals whose amplitudes are less than the threshold voltage (approximately 0.7V for silicon diode and approximately 0.3V for gernanium diode). As a result diode-only rectifiers are used in only those applications in which the precision in the range of threshold voltage is insignificant, such as RF demodulators and DC voltage supply rectifiers, but for applications requiring accuracy the range of threshold voltage the diode-only rectifier cannot be used. This can overcome by using integrated circuit rectifiers instead. The precision rectifiers based on operational amplifier (op-amp), diodes and resistors are presented. However, the classical problem with conventional precision rectifiers based on op-amps and diodes is that during the non-conduction/conduction transition of the diodes, the op-amps must recover with a finite small-signal, dv/dt, (slew-rate) resulting in significant distortion during the zero crossing of the input signal. The use of the high slew-rate op-amps does not solve this problem because it is a small signal transient problem. The gain-bandwidth is a parameter op-amp that limits the high frequency performance of this scheme. Moreover, since these structures use the op-amp and the resistors, it is not suitable for IC fabrication.

3.1: First Generation Current- Conveyor CCI:

The first generation current conveyor CCI [2] forces both the currents and the voltages in ports X and Y to be equal and a replica of the currents is mirrored (or conveyed) to the output port Z. Port Y is used as input for voltage signals and it should not load the input voltage source by drawing current. But, in some applications, it is desirable to draw currents from the input voltage source. When A = 1, port Y draws a current equal to the current injected at port X and the configuration is termed as CCI. Figure 2 presents a simple MOS implementation of the first generation current-conveyor CCI. In this circuit, the NMOS transistors M1 and M2 form a current mirror that forces the drain currents of the PMOS transistors M3 and M4 to be equal and hence the voltages at the terminals X and Y are forced to be identical.

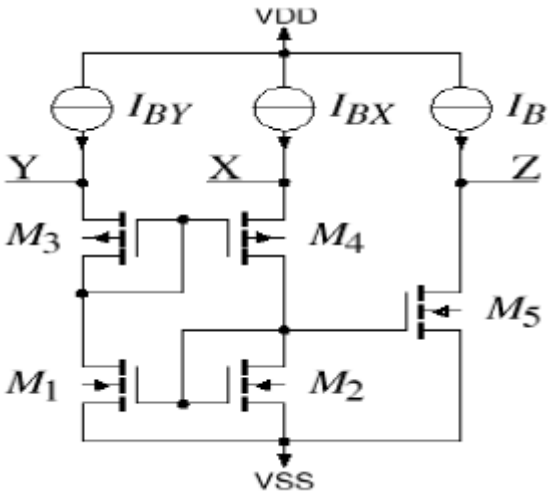

Figure : 3.1 CCI

Because of this low impedance at the input terminal CCI circuit can be used as an accurate current amplifier. In addition, the DC-voltage level at the current input X can be easily set to a desired value by the voltage at the Y-terminal and input voltage-to-current conversion is easier .It can also be used as a negative impedance converter (NIC) [12], if the Yterminal is terminated with a grounded resistance R.

3.2:Second Generation Current Conveyor CCII:

In many applications, only one of the virtual grounds in terminals X and Y of the first generation current-conveyor is used and the unused terminal must be grounded or otherwise connected to a suitable potential. This grounding must be done carefully since a poorly grounded input terminal may cause unwanted negative impedance at the other input terminal. Moreover, for many applications a high impedance input terminal is preferable. For these reasons, the second generation current-conveyor was developed. It has one high and one low impedance input rather than the two low impedance inputs of the CCI [2].

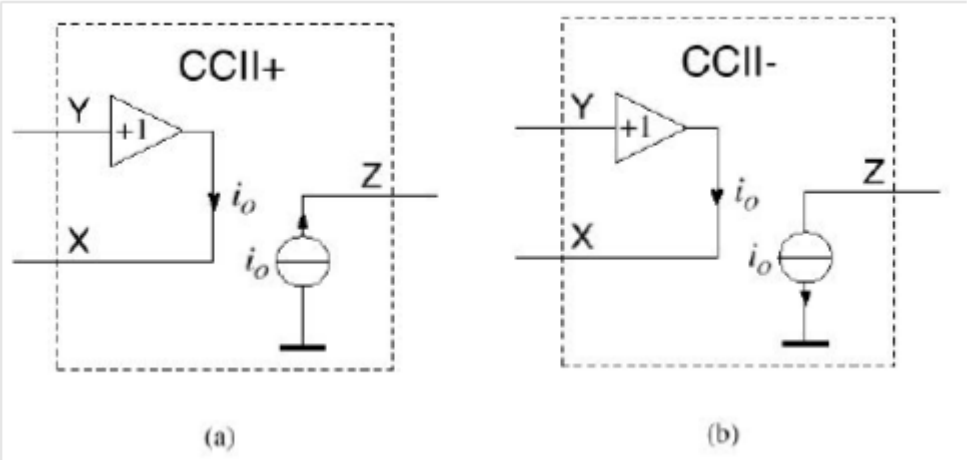

Figure : 3.2 Positive and Negative Current Conveyors

This current-conveyor differs from the first generation conveyor in that the terminal Y is a high impedance port, i.e. there is no current flowing into Y(A = 0). The Y-terminal of the second generation current- conveyor is a voltage input and the Z-terminal is a current output, the X-terminal can be used both as a voltage output and as a current input. Therefore, this conveyor can easily be used to process both current and voltage signals unlike the first generation current- conveyor or the operational amplifier. A further enhancement to the second generation current-conveyor is that there are two types of conveyors: in the positive current-conveyor CCII+, the currents Ix and Iz have the same

direction as in a current- mirror and in the negative current-conveyor CCII-the currents Ix and Iz have opposite direction as in a current buffer. The second-generation current-conveyor is in principle a voltage-follower with a voltage input, Y, and a voltage output, X, and a current-follower (or current-inverter) with a current input X and a current output Z connected together. The negative second-generation current-conveyor CCII- can also be considered an idealized MOS transistor, where the currents Iy =Ig =0 and Iz =Id = - Ix = - is and the voltages Vx = Vs = Vy = Vg. An ideal MOS transistor is one that has a zero threshold voltage Vt and zero channel length modulation parameter and operates in the saturation region regardless of the drain-source voltage (positive or negative).

2.3: Third Generation Current Conveyor CCIII:

Current-conveyor III was proposed in 1995 [5]. The operation of the third generation current-conveyor CCIII is similar to that of the first order current-conveyor CCI, with the exception that the currents in ports X and Y flow in opposite directions (A= -1). As the input current flows into the Y-terminal and out from the X-terminal, the CCIII has high input impedance with common-mode current signals, i.e. identical currents are fed both to Y- and X-terminals. Therefore common-mode currents can push the input terminals out from the proper operation range. Therefore this conveyor is used as current probing.

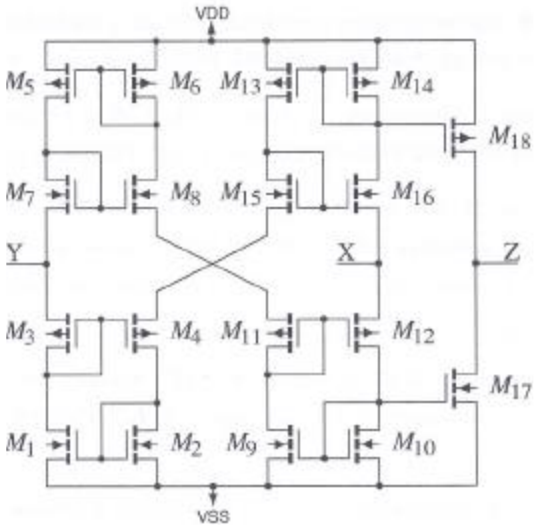

Figure : 3.3 CCIII

CHAPTER-4

CMOS REALIZATION OF CURRENT CONVEYOR

INTRODUCTION

Current-mode circuits have begun to emerge as an important class of circuits, with properties of accuracy, good high-frequency performance, and versatility in a wide range of applications. Since the second generation current conveyor (CCII) was introduced in 1970 El], several applications, such as amplifiers, filters, oscillators, and signal-processing circuits using CCII have been proposed in the literature. Recently, the differentia1 difference amplifier (DDA) was proposed [2] and numerous applications have been found [7-91. Because of the high input impedance and arithmetic operation capability of the DDA, the component count of the circuits using DDAs can be lower than that of the circuits using CCII.

The DDCC, whose electrical symbol is shown in Fig. 1, is a five-port building block which is defined by the following matrix equation

$$\begin{bmatrix} Iy1 \\ Iy2 \\ Iy3 \\ Vx \\ Iz+ \\ Iz- \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & -1 & 0 & 0 \end{bmatrix} \begin{bmatrix} Vy1 \\ Vy2 \\ Vy3 \\ Ix \\ Vz+ \\ Vz- \end{bmatrix}$$

…….(1)

where the plus and minus signs indicate whether the conveyor is configured as a minus or plus type circuit, termed DDCC- or DDCC+, respectively.

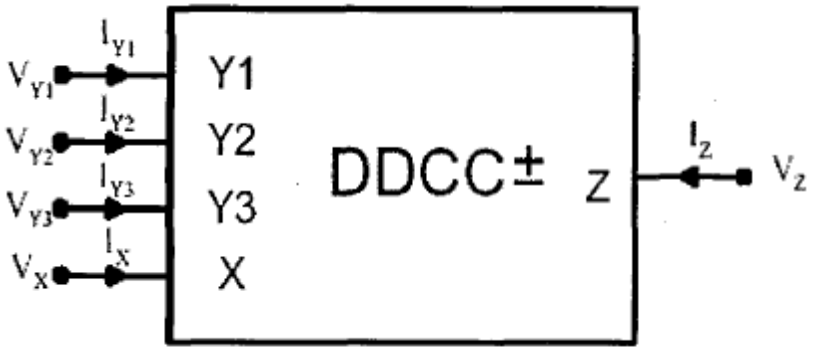

Figure 4.1: Block dig of current conveyor

4.1 DDCC REALIZATION -1

The circuit structure of this CMOS DDCC is similar to that of the CCII+ in [8] and to the DDA realisation in [6]. The input transconductance elements are realised with two differential stages (M1 and M2, M3 and M4). The high-gain stage is composed of a current mirror (M5 and M6) which converts the differential current to a single-ended output current (M7). The output voltage of this amplifier can be expressed as

$$V_x = A_0[(V_{y1}-V_{y2})-(V_{G3}-V_{Y3})] \qquad (2)$$

where *A.* is the open-loop gain of the amplifier and *VG3* is the gate voltage of M3. Negative feedback was then applied from the output node of the gain stage (node X) to the input node (gate of M3). If the open-loop gain of the amplifier is much larger than one, the relationship

between the four input terminal voltages can be obtained as

VX= -*A0* (VY1 - VY2 + VY3) ,2 VYl - VY2 *3*- VY3 (3)

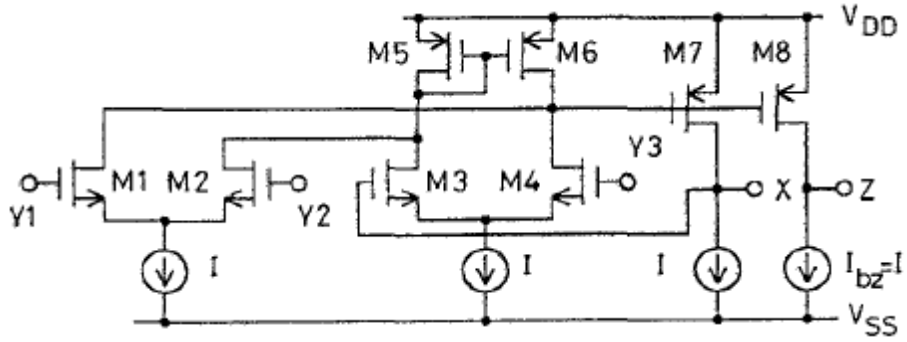

Figure 4.2 DDCC 1

The PSpice schematic of DDCC is shown in fig 4.2 and its simulated DC response is shown in fig.

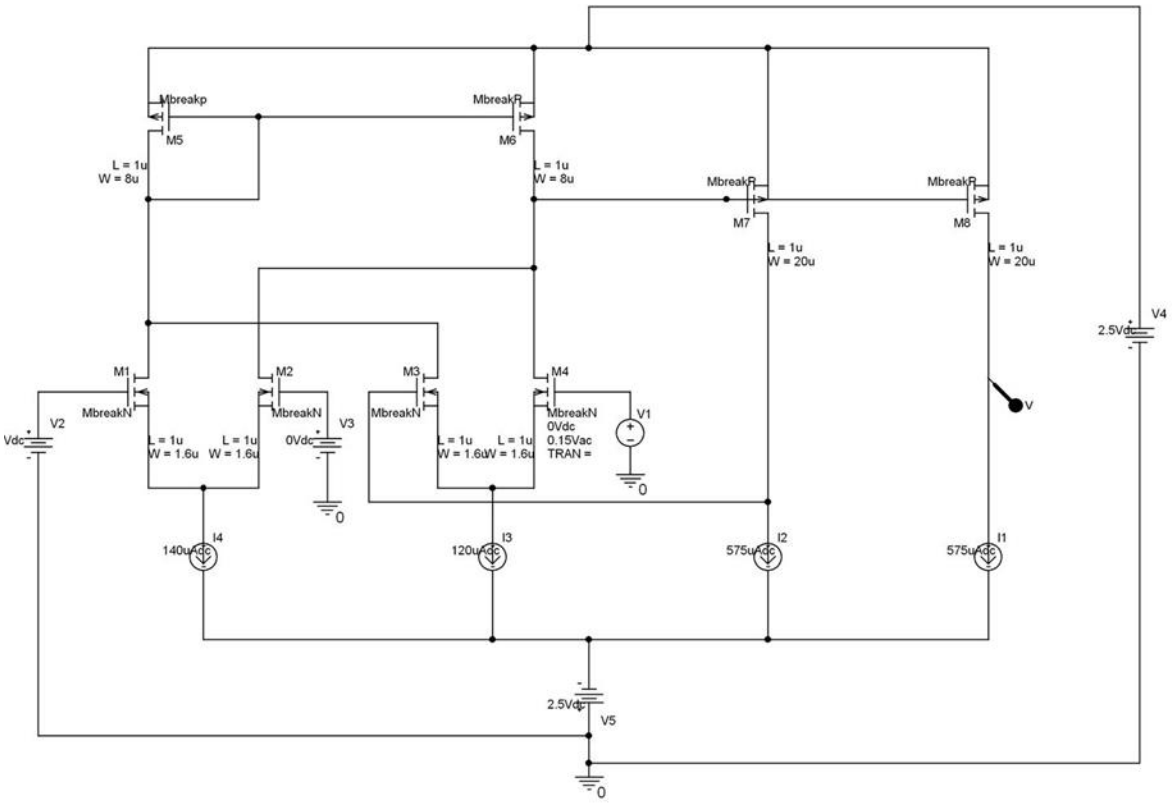

Figure:4.3 Pspice schematic of DDCC 1

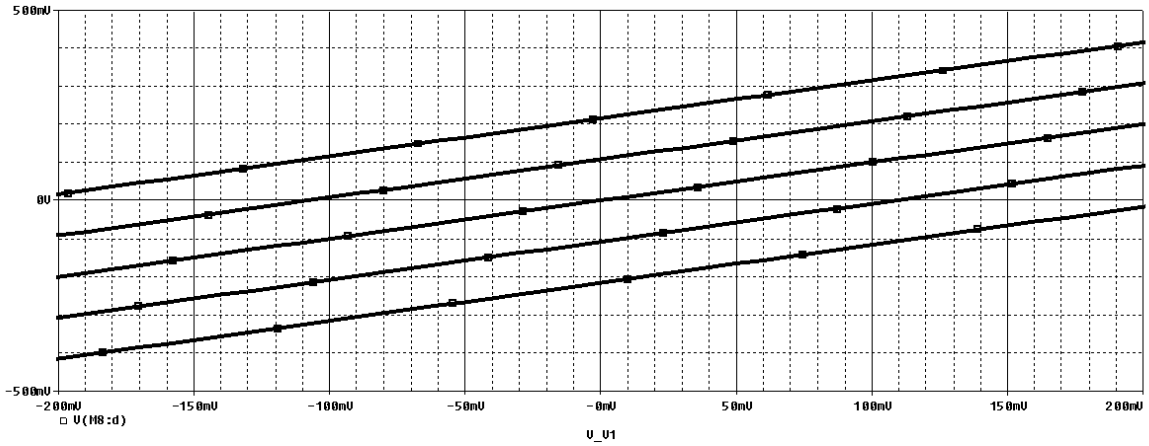

Figure:4.4 DC characteristic

4.2 DDCC REALIZATION -2

The CMOS realization of the DDCC is illustrated in Fig.2 [9]. The input transconductance elements are realized with two differential stages (M1 and M2, M3 and M4). The high-gain stage is composed of a current mirror (M5 and M_6) which converts the differential current to a single ended output current (M7). The output voltage of this amplifier can be expressed as

$$V_x = A_0[(V_{y1}-V_{y2})-(V_{G3}-V_{Y3})] \quad \text{……..(2)}$$

where A. is the open-loop gain of the amplifier and VG3 is the gate voltage of M3. Negative feedback was then applied from the output node of the gain stage (terminal X) to the input node (gate of M3) (then VG3=VX).

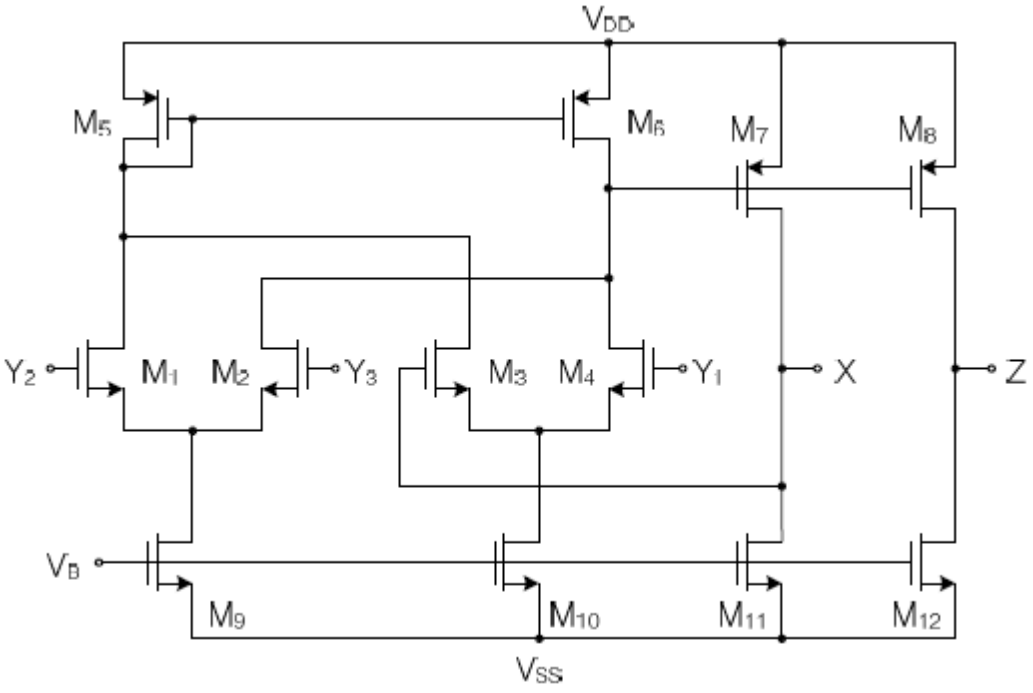

Figure 4.5 The CMOS implementation of DDCC 2

If the open-loop gain of the amplifier is much larger than one, the relationship between the input terminal voltages can be obtained as

$$V_X = \frac{A0}{A0+1}(V_{Y1}-V_{Y2}+V_{Y3})$$

$$V_X \cong V_{Y1} - V_{Y2} + V_{Y3} \quad \text{.....(3)}$$

$$I_{Y1}=I_{Y2}=I_{Y3}=0 \quad \text{.....(4)}$$

$$I_{Z\pm} = \pm I_X \quad \text{.....(5)}$$

Where

V_{Y1}= Voltage at node

V_{Y2}= Voltage at node

V_{Y3}= Voltage at node

V_x= Voltage at node

I_{Z+} = Current at Z+ terminal

I_{Z-} = Current at Z- terminal

I_X = Current at X terminal

The output terminal Z is constituted with M_{12} and M_8 which duplicates the current of the transistor M_7. It can be clearly seen that both **Ix** and **Iz** flow simultaneously towards or away from the DDCC. Therefore, the circuit in Fig.2 realizes a DDCC.

In a DDCC, terminals Y1, Y2 and Y3 exhibit infinite input impedances. Thus no current flows in terminal Y1, Y2 and Y3. The terminal X exhibits zero input impedance. The PSpice schematic of DDCC is shown in fig 4.2 and its simulated DC response is shown in fig.

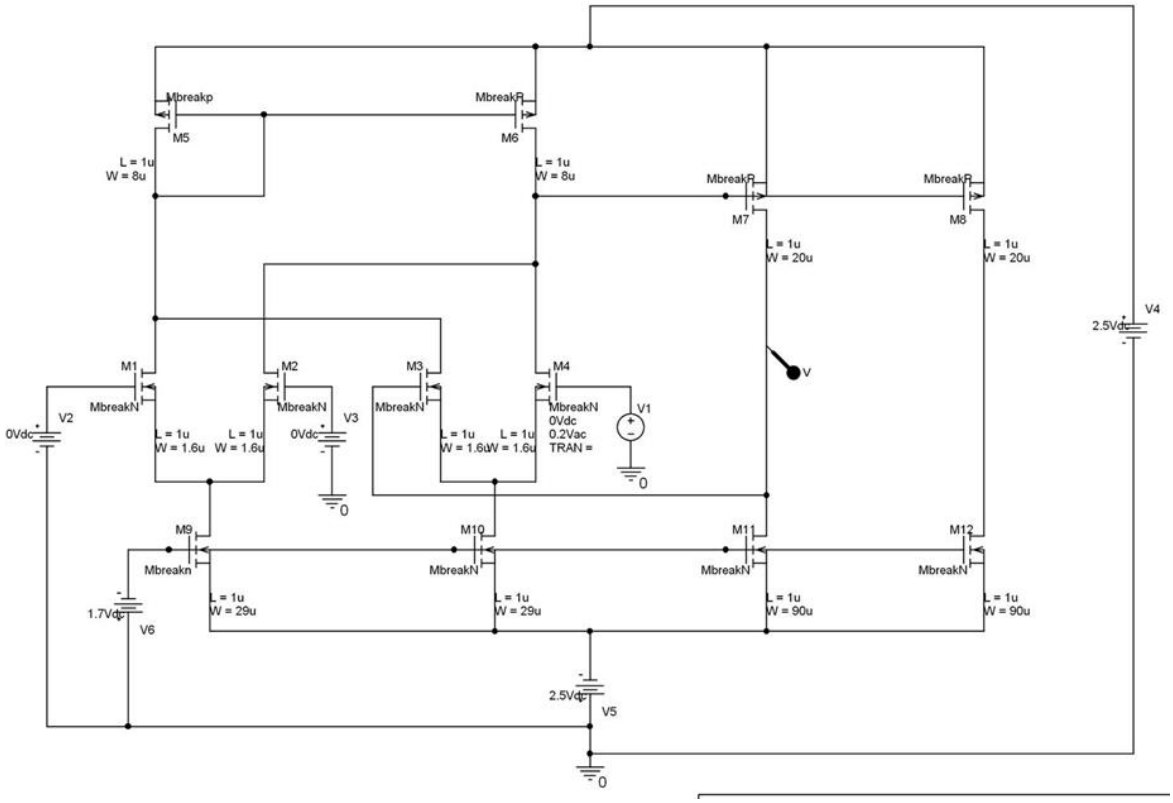

Figure:4.6 Pspice schematic of ddcc 2

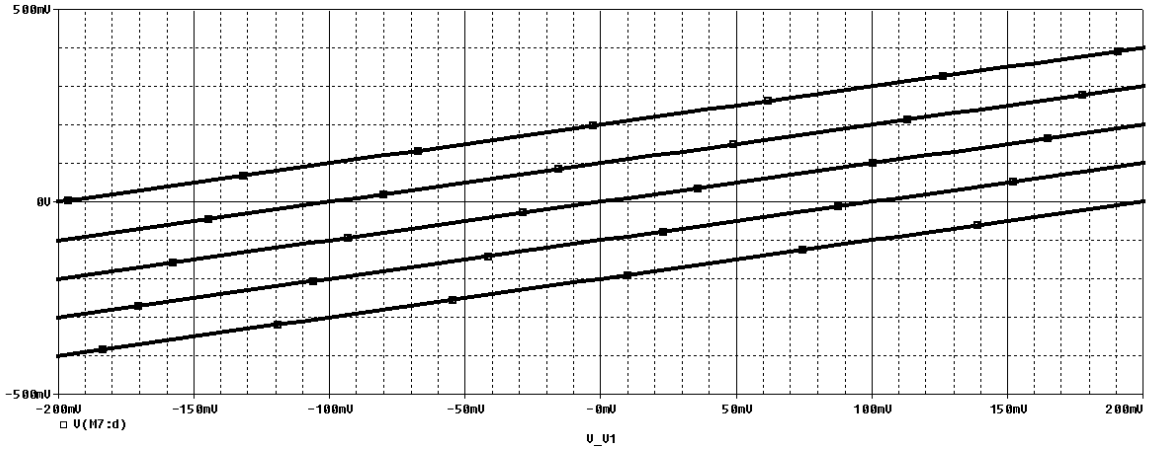

Figure:4.7 Dc characteristic

CHAPTER-5

REALIZATION OF CURRENT CONVEYOR BASED VLSI CIRCUITS

5.1 FULL WAVE RECTIFIER

In this paper, a new full-wave rectifier circuit using only two DDCCs is presented [9]. The proposed circuit uses a recently proposed current conveyor, named differential difference current conveyor (DDCC) [12]. The circuit is simple and suitable for IC implementation. The circuit also offers high-input and low-output impedance terminals, which is suitable for low impedance load. Simulation results verifying the theoretical analysis are also included

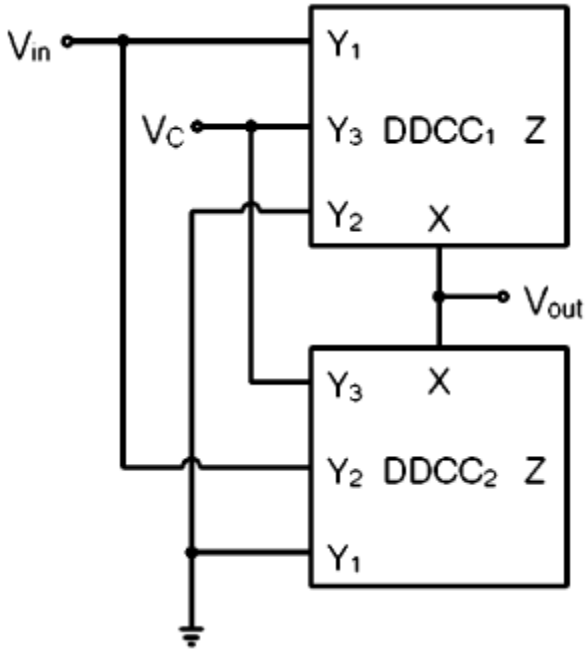

Figure: 5.1 Full wave rectifier

The electrical symbol of DDCC is shown in Figure 1. It was proposed in 1997 [5] and it enjoys the advantages of CCII and differential amplifier (DA) such as larger signal bandwidth, greater linearity, wider dynamic range, simple circuitry, low power consumption, high-input impedance. The DDCC has three voltage input terminals: Y Y and Y which have high input impedance. Terminal X is a low impedance current input terminal. There is a high impedance current output tenninal Z. The output current (IJ follow the input current through tenninal X. The voltage of X teoninal is related by the three

inputs voltage: Vx=Vyt -Vy2. The CMOS realization of the DDCC used in this paper for the proposed full-wave rectifier circuit is shown in Figure 2 [12].

Figure 3 shows the proposed full-wave rectifier circuit. The proposed circuit uses only two DDCCs. The positive output voltage of the DDCC is connected to the negative output voltage of the DDCC2. The full-wave operation is as follows: when Vin>O, the voltage Yin is followed by the DDCC to the voltage Vout at X terminal while the DDCC2 is turn-off. addition, when Vin<O, the voltage Yin is followed by the DDCC2 to the voltage Vout at X terminal while the DDCC is cut-off. From the operation of the proposed full-wave rectifier explained, the relations between the input voltage, Vin, and the output voltage, Vout, can be expressed as

Yin >0 ,Vout =Vin . DVCC1 -on

Yin <0 ,Vout= --Vin . DVCC2 –on

The complete output voltage of Figure 3 can be expressed as

Vout = mod (Vin)

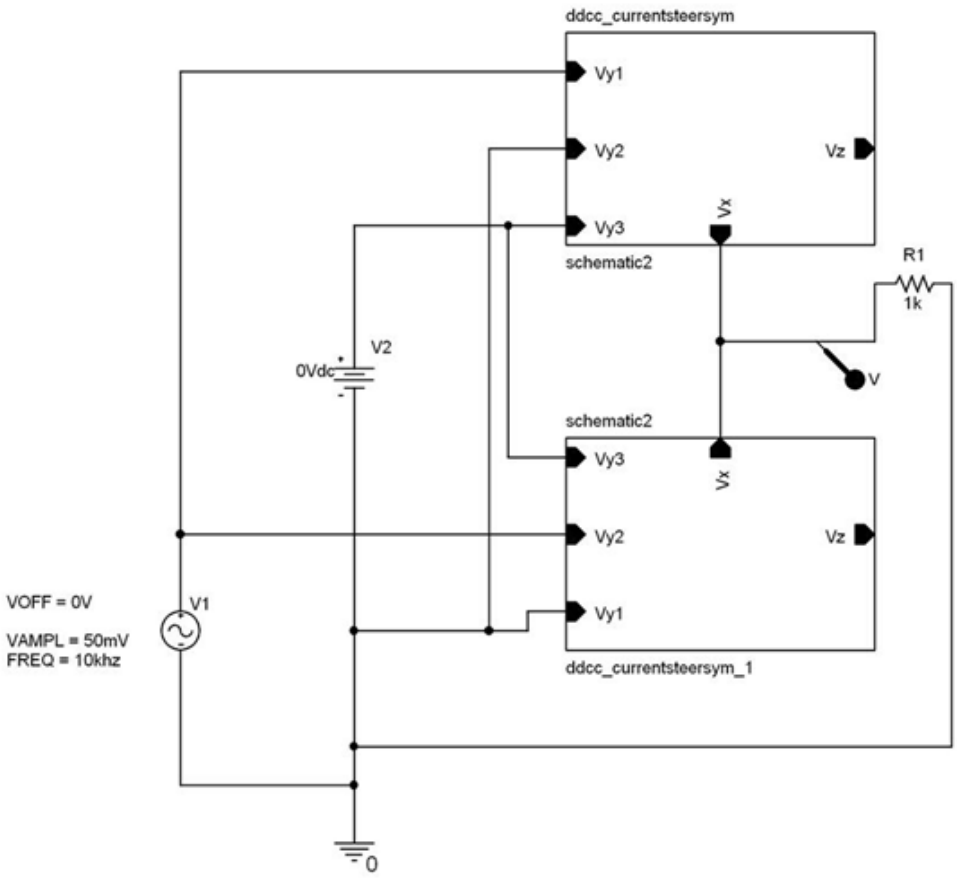

Figure: 5.2 Pspice schematic of fwr using ddcc 1

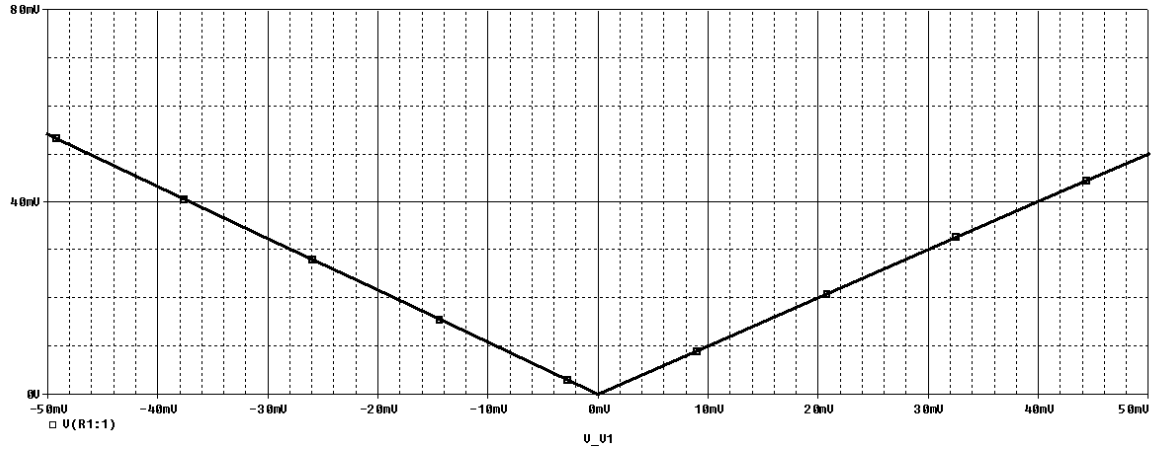

Figure: 5.3 Fwr dc characteristic using ddcc1

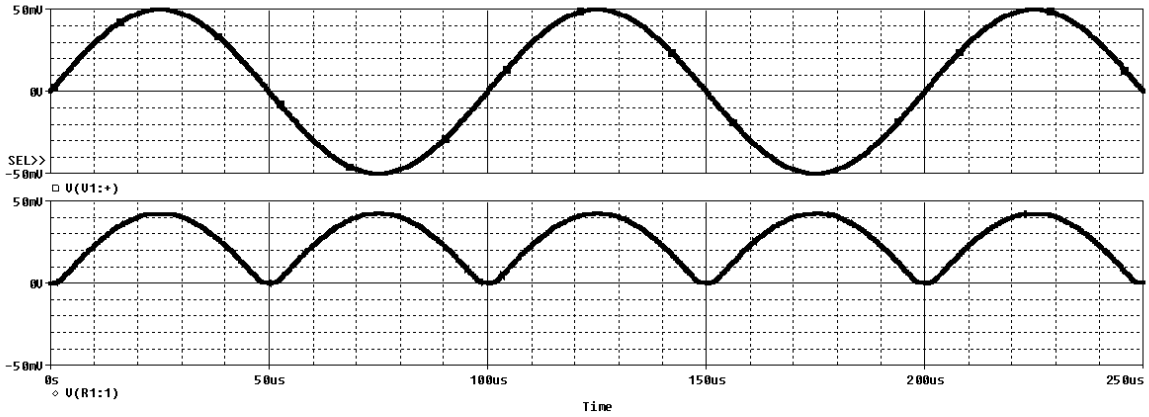

Figure: 5.4 Fwr ac characteristic using ddcc1

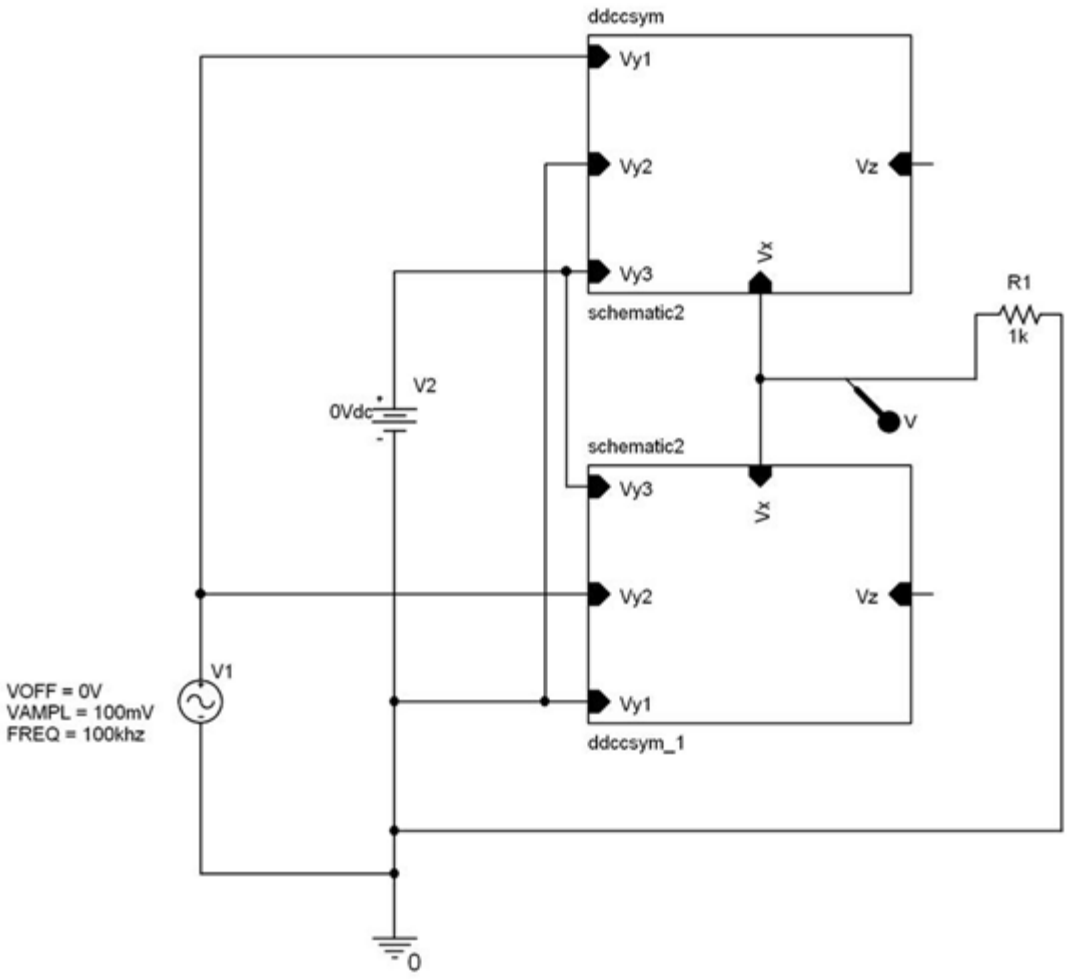

Figure: 5.5 Pspice schematic of fwr using ddcc 2

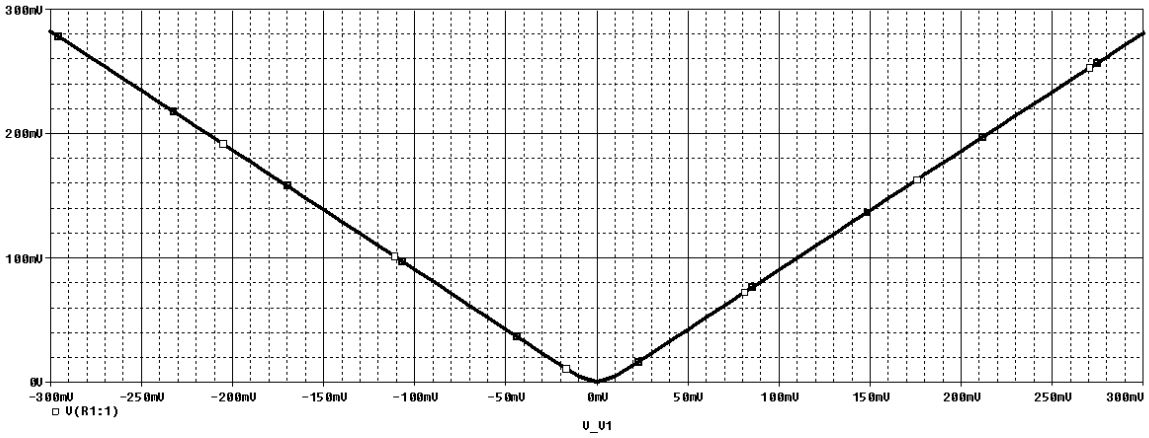

Figure: 5.6 Dc characteristic of fwr using ddcc2

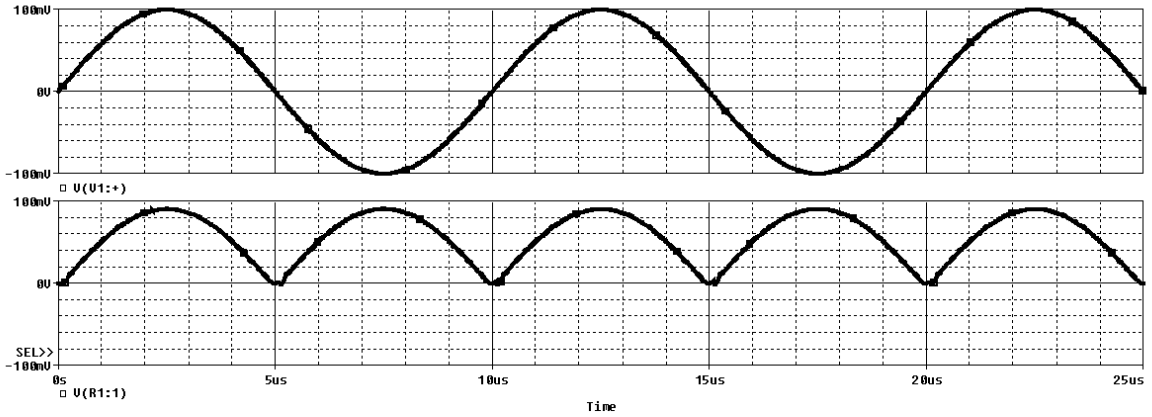

Figure: 5.7 ac characteristic of fwr using ddcc2

5.2 QUADRATURE OSCILLATOR

In this paper, a new voltage-mode quadrature oscillator based on DDCCs is presented [10]. The proposed circuit employs two DDCCs, two grounded capacitors, and two resistors. The proposed circuit enjoys low active and passive sensitivities. The use of grounded capacitors makes the proposed circuit suitable for integrated circuit implementation [9]. The theoretical results are verified by PSPICE simulation.

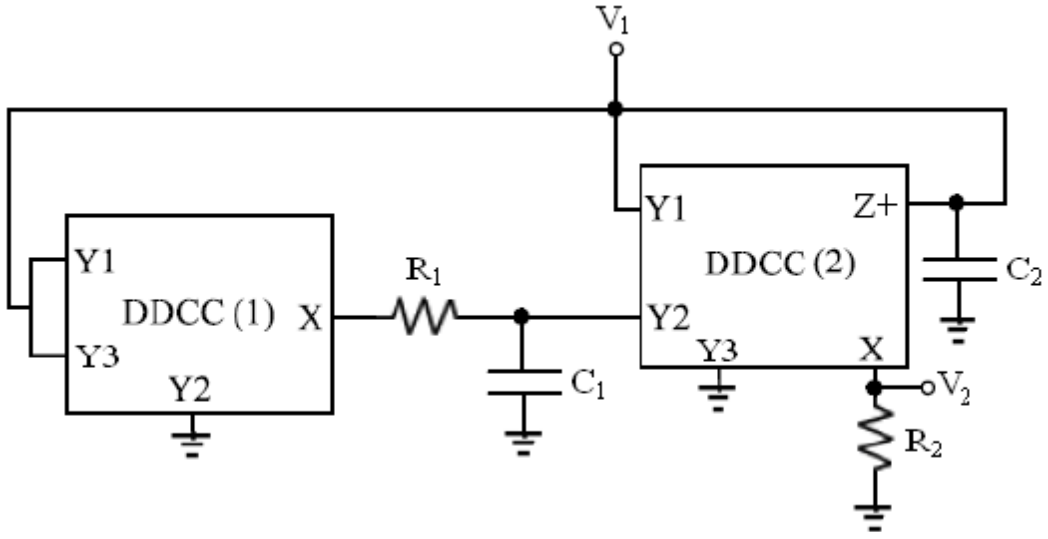

Figure: 5.8 Quadrature oscillator

The characteristic equation of the circuit can be expressed as

$$s^2 + \frac{s(C_2R_2 - C_1R_1)}{C_1C_2R_1R_2} + \frac{1}{C_1C_2R_1R_2} = 0$$

The oscillation frequency and oscillation condition can be obtained as:

$$\omega_0 = \frac{1}{\sqrt{C_1C_2R_1R_2}}$$

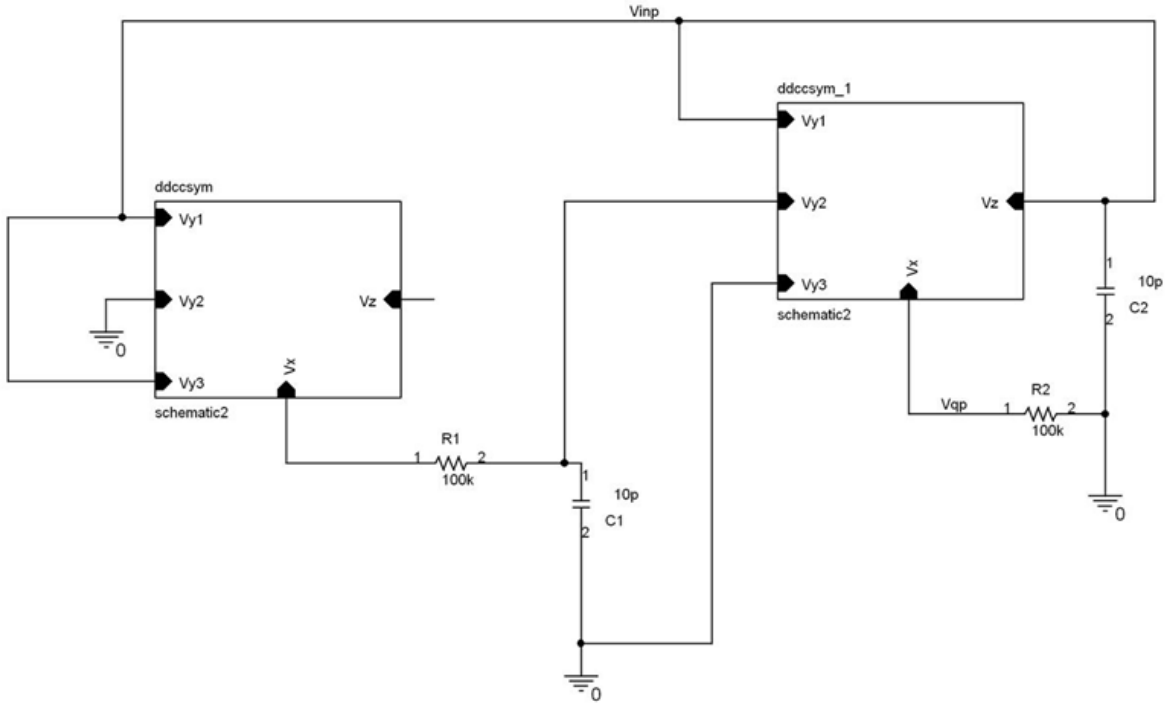

Figure: 5.9 Pspice schematic of oscillator using ddcc 1

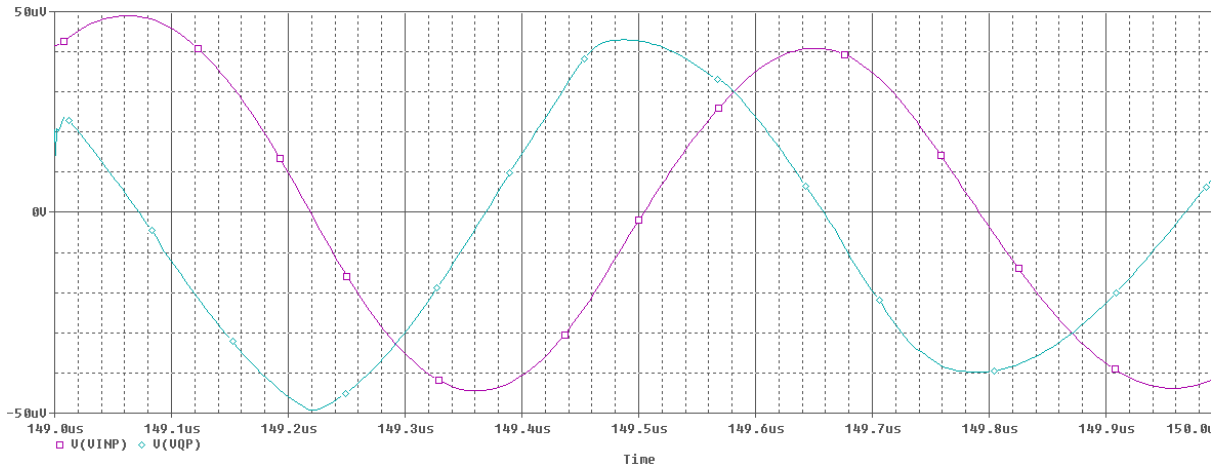

Figure: 5.10 VINP AND VQP of quadrature oscillator using ddcc1

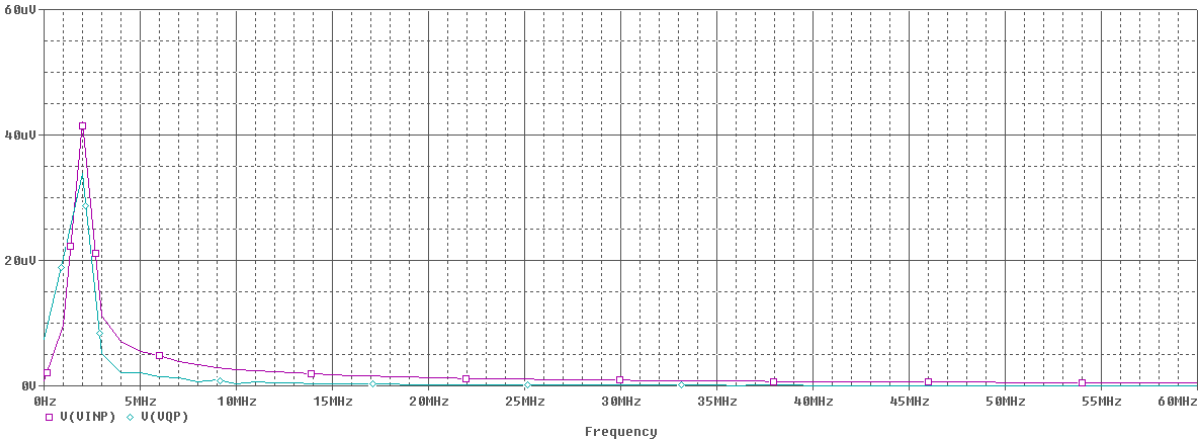

Figure: 5.11 FFT of vinp and vqp of quadrature oscillator showing same frequency using ddcc1

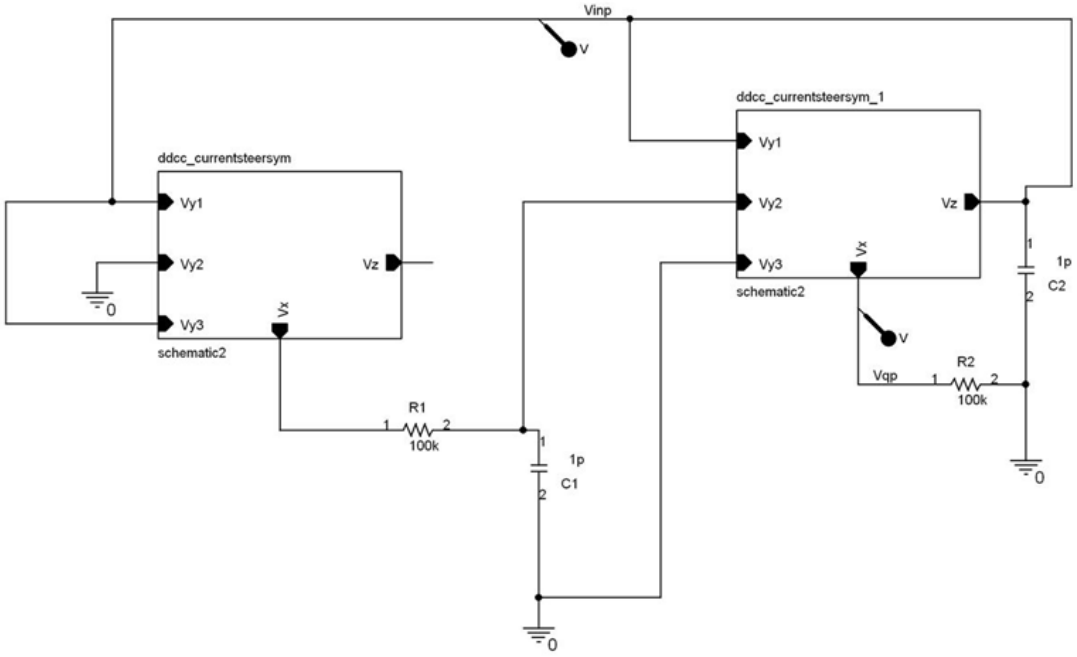

Figure: 5.12 Pspice schematic of quadrature oscillator using ddcc2

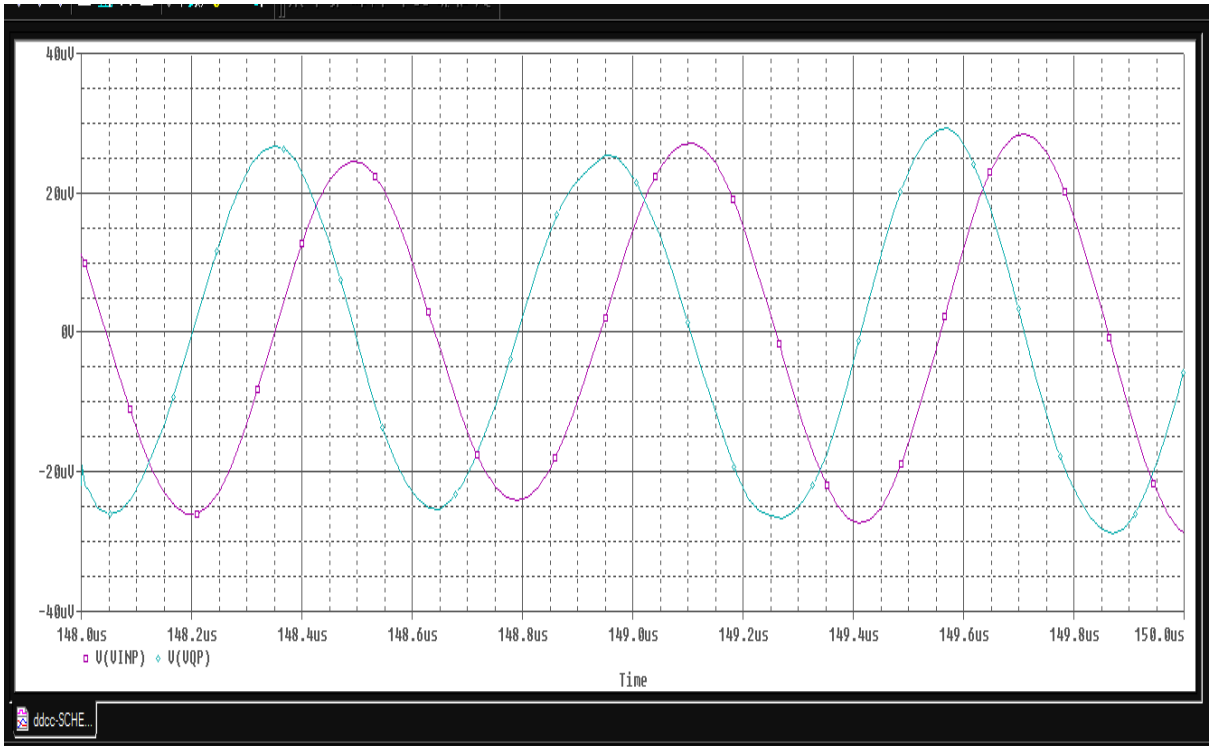

Figure: 5.13 VINP AND VQP of quadrature oscillator using ddcc2

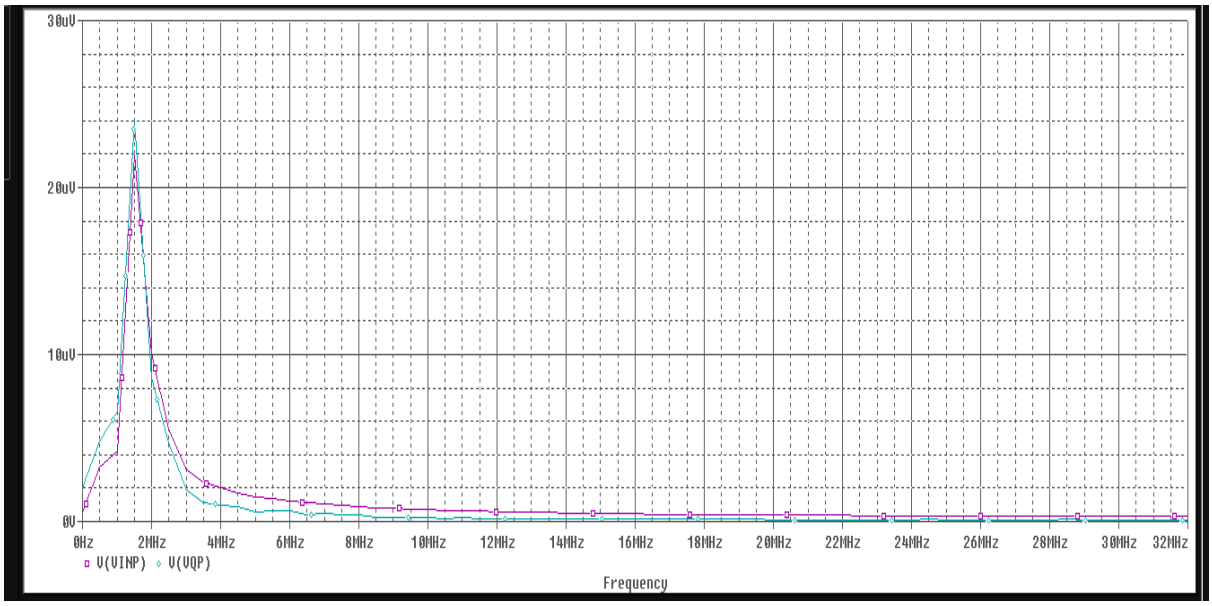

Figure: 5.14 FFT of vinp and vqp of quadrature oscillator showing same frequency using ddcc2

5.3 CURRENT MULTIPLIER AND DIVIDER

In this paper, a new current-mode one-quadrant log-antilog multiplier/divider based on DDCC is proposed [11]. The circuit employs one DDCC and four diodes. Since the addition and subtraction operation of voltage signals have been offered by DDCC, hence the proposed circuit is simple circuitry. Also, the circuit enjoys excellent temperature stability and very suitable for implementation in CMOS technology. The theoretical results are verified by PSPICE simulations.

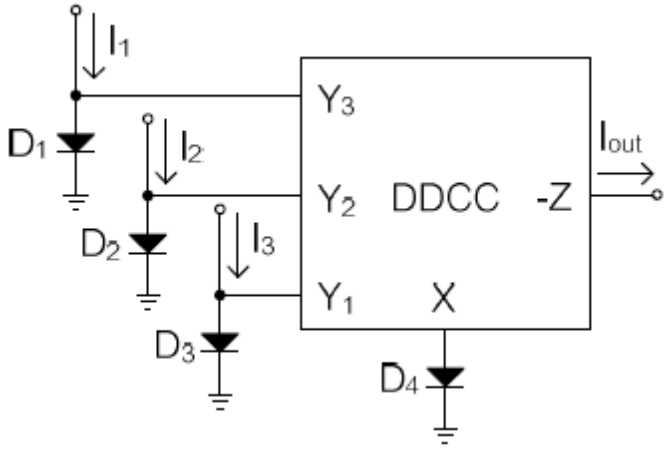

Figure: 5.15 Current-mode one-quadrant log-antilog multiplier/divider

The operation of the circuit can be explained as follows. If input currents (I1, I2, I3) are supplied, using the logarithm property of a forward bias p-n junction of diode [2], the voltages, VY1, VY2 and VY3, of DDCC can be obtained, respectively, as

$$V_{Y1} = V_T \ln\left(\frac{I_1}{I_S}\right)$$

$$V_{Y2} = V_T \ln\left(\frac{I_2}{I_S}\right)$$

$$V_{Y3} = V_T \ln\left(\frac{I_3}{I_S}\right)$$

where IS is the reverse saturation current and VT is the thermal voltage. Using equation (1), the voltage VX can be obtained as

$$V_X = V_T \ln\left(\frac{I_1}{I_S}\right) - V_T \ln\left(\frac{I_2}{I_S}\right) + V_T \ln\left(\frac{I_3}{I_S}\right)$$

Assume that diodes (D1, D2, D3, D4) are closely matched, the current output Iout can be expressed as

$$I_{out} = \frac{I_1 I_3}{I_2}$$

which means that the output current Iout is a multiplier/divider of the input signal currents I1, I2 and I3. It should be noted that the output current is also temperature independent.

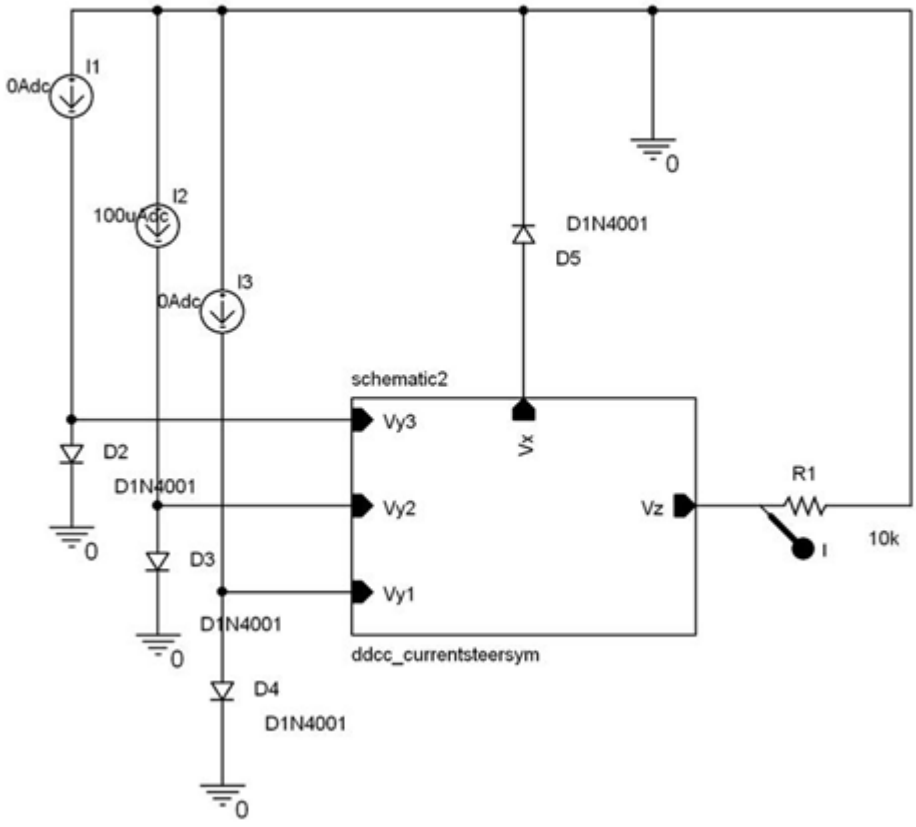

Figure: 5.16 Pspice schematic of multiplier/divider of ddcc1

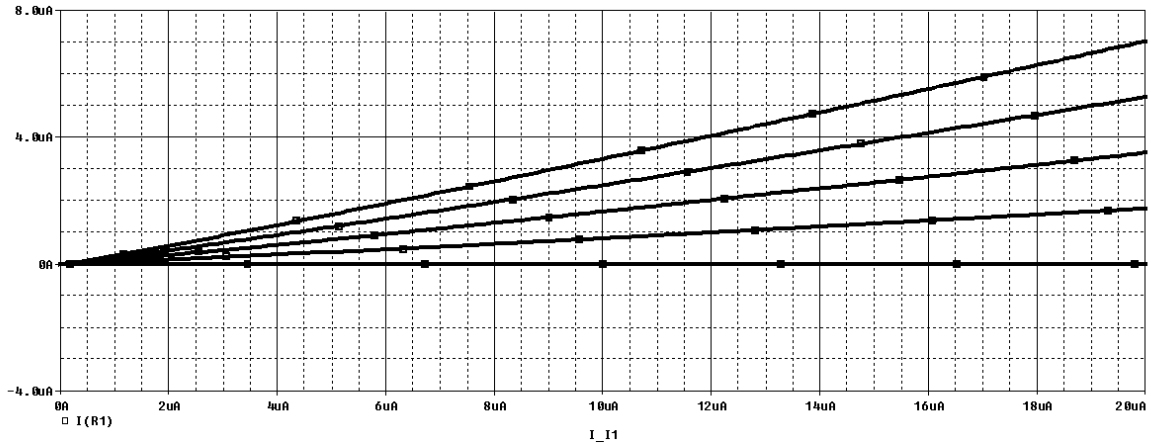

Figure: 5.17 Dc characteristic i1=0uA to 60uA, i2=100uA, i3=0,10,20,30,40uA

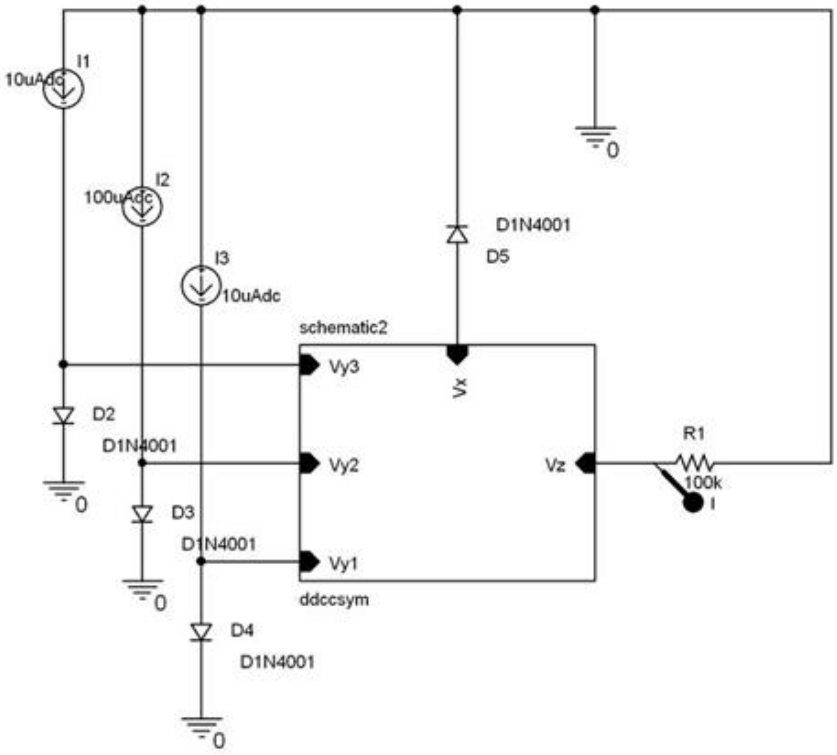

Figure: 5.18 Pspice schematic of multiplier/divider of ddcc2

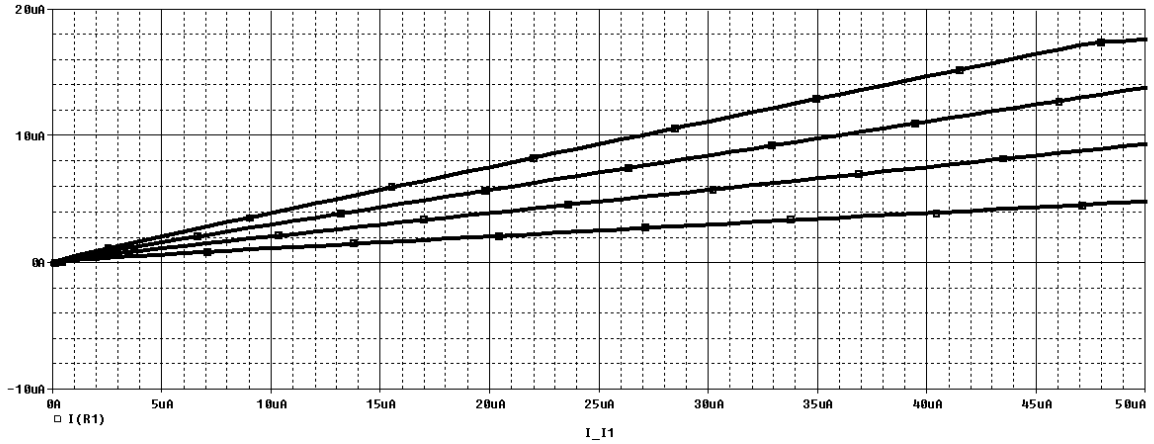

Figure: 5.19 Dc characteristic i1=0uA to 50uA, i2=100uA, i3=10,20,30,40uA

CHAPTER-5

CONCLUSION

This report describes the current conveyor used as a basic building block in a variety of electronic circuit in instrumentation and communication systems. In this report, some important blocks used in analog circuits have been studied. Besides it, the three existing realizations of current conveyors have been studied in detail. Two of these realizations of the current conveyer have been simulated using Spice (0.5 µm technology). Along with these, a few applications of the current conveyer has also been simulated. Today these systems are replacing the conventional Op-amp in so many applications such as active filters, analog signal processing, and converters. Spice simulation of the current conveyor blocks and their applications verifies its suitability as a building block in VLSI circuits. The need for low-voltage low-power circuits is immense in portable electronic equipments like laptop computers, pace makers, cell phones etc. Voltage Mode Circuits are rarely used in low-voltage circuits as the minimum bias voltages depend on the threshold voltages of the MOSFETs. From the restriction of DDCC, it lacks in tenability feature and requires the resistor connections.

CHAPTER-5

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