DESIGN OF AGC CIRCUITS FOR OSCILLATOR USING CURRENT CONVEYOR BASED TRANSLINEAR LOOPS

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This is certified that the dissertation entitled "**DESIGN OF AGC CIRCUITS FOR OSCILLATOR USING CURRENT CONVEYOR BASED TRANSLINEAR LOOPS"** is a work of **NIKHIL KAUSHIK** (University Roll No. – 2K11/VLS/14) is a student of Delhi Technological University. This work is completed under my direct supervision and guidance and forms a part of **MASTER OF TECHNOLOGY** in **VLSI DESIGN AND ENBEDDED SYSTEM** curriculum. He has completed his work with utmost sincerity and diligence.

The work embodied in this major project has not been submitted for the award of any other Institute / University for the award of any other degree to the best of my knowledge.

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ABSTRACT

With the increasing demand of portable and battery driven devices a low voltage operating devices has become necessary and for this current mode techniques are ideally suited. This thesis is focused on current conveyor based translinear(TL) loops in which a novel topology for TL loops comprising of CMOS second Generation Current Conveyors (CC-II) and diodes is studied. Using the same a new circuit of an integrator is implemented using log-domain principle. Further, three circuits for automatic gain control are proposed and implemented. All the proposed circuits are verified for the functionality using PSPICE and 0.18µm TSMC CMOS technology parameters.

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Chapter-1

Introduction and Thesis Outline

1.1 Introduction

Current mode circuits are gaining acceptance in variety of applications such as data acquisition and processing, testing, filter design and image sensory processing to name a few [1]. This is due to the many advantages offered by current mode circuits such as high speed, large bandwidth and ability to work under lower power supply voltage [2]. Another important consideration is that while voltage mode circuits require the use of complex techniques to lower power dissipation, current mode circuits can do the same in standard VLSI CMOS technology [2].

In the traditional circuit implementation where op-amp, MOSFET-C, transconductance-C or switched capacitors, there was a restriction on the bases of the supply voltage in attaining maximum dynamic range. Further, the use of linear resistors in a low-power environment requires a large silicon area for on-chip integration which makes this approach impractical.

TL circuits are the circuits that follow the dynamic translinear (DTL) circuit principle [3], which is considered as a generalization of the static TL (STL) principle formulated by Gilbert in 1975 [4]. Both static and dynamic TL circuits works on the inherent exponential transfer function, which is obtained from the relation between the collector current and base-emitter voltage of bipolar junction transistors (BJTs) [5] or between the drain current and gate-source voltage of a MOS transistor operating in its weak-inversion region [6]. In a MOS/CMOS based implementation of a TL circuit the current range where the exponential V-I characteristic can be used, thus restricting the choice and optimization of the operating point, is within the weak-inversion region.

Another fundamental limitation of MOS transistors operating in weak inversion is the poor matching of the threshold voltages which affect the distortion (and thus dynamic-range) performance of CMOS log-domain filters. Moreover, TL circuits implemented in CMOS technology operating in sub-threshold region suffer from low bandwidth limitations.

CCII-based translinear loops [7] open a new paradigm towards the design of static and dynamic TL circuits in CMOS technology.

Automatic gain control (AGC) is an adaptive system found in many electronic devices. The average of the output signal level is fed back to adjust the gain to an appropriate level for a range of input signal levels. An AGC is a closed-loop system that automatically adjusts the gain such that the output level stays within a desired range. As known, AGCs play a very important role in modern hearing aid devices and communication systems [8-9]. For example, without AGC the sound emitted from an AM radio receiver would vary to an extreme extent from a weak to a strong signal; the AGC effectively reduces the volume if the signal is strong and raises it when it is weak. Many published literatures have proposed different methods to design the AGC circuits [10-11]. However, most of the AGC circuits have been developed in voltage-mode configuration. In this thesis the work is presented on the current mode configuration to implement the AGC circuits.

1.2 Research Goals and Objectives

In the last decade, there has been much effort to reduce the supply voltage of analog CMOS systems. This is due to the command for portable and battery powered equipment. Since a low-voltage operating circuit becomes necessary, the current–mode technique is ideally suited for this proposes [12]. The purpose of this report is to present a realization of an AGC circuit functioning in current-mode.

The proposed AGC circuit which includes an integrator circuit has been conceived from the building blocks of multiplier and rectifier with low-pass filter circuits which had been proposed earlier in the research work available in literature[21]. All circuits can be realized using Current Conveyers. In addition, the gain of AGC is controlled by a reference current provided in the circuit. Consequently, the proposed circuit can be very appropriate for further fabricating into Integrated Circuit (IC) formed to employ in portable electronic equipment such as hearing aid instrument and wireless communication device. The simulation results are done through PSPICE.

1.3 Thesis Organisation

The thesis is organized as follows:

Chapter 2 presents the background of Translinear circuits. In this chapter the concept of Translinearity and Translinearity principle is studied. This chapter is further extended to the study of log-domain principle and √-domain principle.

Chapter 3 is a detailed study of current conveyors from the very basic current conveyor to the latest ones. All the three generations of current conveyors are studied namely CCI, CCII and CCIII.

Various CC based translinear circuits are studied and implemented in chapter 4. Circuits of multiplier and divider are implemented having TL loop as bases. Further an integrator circuit is proposed using log-domain principle and current conveyors.

Chapter 5 is dedicated to automatic gain control circuits. In this the principle and the use of AGC is studied. Further, three circuits for AGC are proposed and implemented.

Chapter 6 presents the conclusion and summarize the research work done in the thesis.

Chapter-2

Translinear Circuits

2.1 Introduction

A translinear circuit is a circuit that carries out its function using the translinear principle. These are current-mode circuits that can be made using transistors which obeys an exponential current-voltage characteristic which includes BJTs and CMOS transistors in weak inversion.

The word translinear (TL) was invented by Barrie Gilbert in 1975 to describe circuits that used the exponential current-voltage relation of BJTs. By using this exponential relationship, this class of circuits can implement multiplication, amplification and power-law relationships. When Barrie Gilbert described this class of circuits he also described the translinear principle (TLP) which made the analysis of these circuits possible in a way that were not allowed in the previous view towards BJTs as linear current amplifiers. TLP was later extended to include other elements that obey an exponential current-voltage relationship (such as CMOS transistors in weak inversion).

The TLP has been used in a variety of circuits including vector arithmetic circuits, current conveyors, current-mode operational amplifiers, and RMS-DC converters. It has been in use since the 1960s (by Gilbert), but was not formalized until 1975 [4]. In the 1980s, Evert Seevinck's work helped to create a systematic process for translinear circuit design. In 1990 Seevinck invented a circuit he called a *companding* current-mode integrator that was effectively a first-order log-domain filter. A version of this was generalized in 1993 by Douglas Frey [5] and the connection between this class of filters and TL circuits was made most explicit in the late 90s work of Jan Mulder [3] where they describe the dynamic translinear principle. More work by Seevinck led to synthesis techniques for extremely low-power TL circuits. More recent work in the field has led to the voltage-translinear principle, multiple-input translinear element networks, and field-programmable analog arrays (FPAAs).

2.2 Translinearity

Basically Translinearity could be considered as Transconductance which is linear with respect to voltage or current. So, what can be the devices can have transconductance linear with respect to voltage or current? Think of it as a synthesis procedure, so, if one has to call for a device what should be its

properties and characteristics. Its relation between current and voltage could be given as:

$$I_0 = f(V_i)$$

$$\text{Transconductance,} \quad g_m = \partial I_o / \partial V_i$$

Where I_0 is output current and V_i is input voltage.

If g_m is linear with respect to current,

$$g_m = \frac{\partial I_o}{\partial V_i} = kI_0$$

$$\text{so,} \quad I_0 = e^{kV_i}$$

which represents the characteristics for BJT.

$$I_c = I_s e^{V_{be}/V_{Th}} \quad \text{or} \quad V_{be} = V_t \ln \frac{I_c}{I_s}$$

Transconductance, $\frac{\partial I_c}{\partial V_{be}} = \frac{I_s}{V_t} e^{(V_{be}/V_t)} = \frac{I_c}{V_t}$

Similarly, if g_m is linear with respect to voltage,

$$g_m = \partial I_o / \partial V_i = kV_i$$

$$\text{so,} \quad I_o = kV_i^2 + k_0.$$

Which represents the characteristics for FET.

$$I_D = \frac{KW}{2L}(V_{gs} - V_{Th})^2$$

Transconductance, $\frac{\partial I_D}{\partial V_{gs}} = \frac{KW}{L}(V_{gs} - V_{Th})$

where every term has standard meanings.

2.3 The Translinear Principle

2.3.1 In BJT Translinear Circuits

The translinear principle is that in a closed loop containing an even number of translinear elements (TEs) with an equal number of them arranged clockwise and counter-clockwise, the product of the currents through the clockwise TEs equals the product of the currents through the counter-clockwise TEs or

$$\prod_{CW} I_n = \prod_{ACW} I_n$$

The principle applies where a number of forward biased base-emitter junctions (Vbe) are connected in continuous loops. The transistors in the loop can be considered as clockwise (CW) or anticlockwise (ACW) depending upon the direction of current in the junction. The transistor could be npn or pnp, but there must be the conditions that has to be satisfied: (i) the number of CW npn junctions should be equal to the number of ACW npn junctions, and (ii) the number of CW pnp junctions should be equal to the number of ACW pnp junctions. To satisfy these conditions there has to an even number of Vbe junctions in the loop.

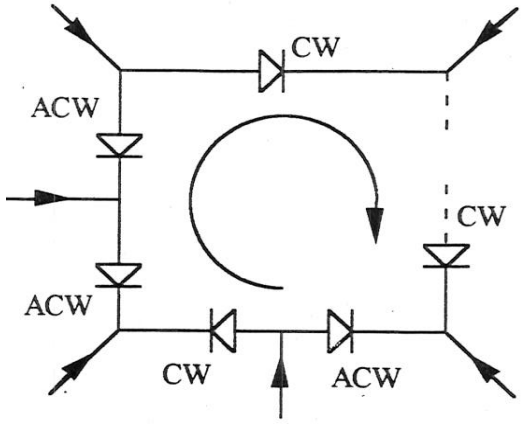

Figure 2.1: Loop with j npn Vbe and k pnp Vbe junction in each direction

Consider a loop in which there are j npn Vbe junctions in each direction and k pnp Vbe junctions in each direction. By applying the KVL in the loop ensures that the sum of CW voltages in loop is equal to the sum of ACW voltages in the loop.

$$\sum_{CW_j} V_{be_j} + \sum_{CW_k} V_{eb_k} = \sum_{ACW_j} V_{be_j} + \sum_{ACW_k} V_{eb_k}$$

$$\sum_{CW_j} V_{Th} \ln \frac{I_{c_j}}{I_{sn}} + \sum_{CW_k} V_{Th} \ln \frac{I_{c_k}}{I_{sp}} = \sum_{ACW_j} V_{Th} \ln \frac{I_{c_j}}{I_{sn}} + \sum_{ACW_k} V_{Th} \ln \frac{I_{c_k}}{I_{sp}}$$

Icj and Ick represents the collector current associated with each Vbe junction in the loop. The currents Isn and Isp represents the reverse saturation current in npn and pnp transistors respectively. These currents can be represented in terms of there current densities (Isn = JsnAj and Isp = JspAp).

$$\sum_{CW_j} \ln \frac{I_{c_j}}{J_{sn}A_j} + \sum_{CW_k} \ln \frac{I_{c_k}}{J_{sp}A_p} = \sum_{ACW_j} \ln \frac{I_{c_j}}{J_{sn}A_j} + \sum_{ACW_k} \ln \frac{I_{c_k}}{J_{sp}A_p}$$

$$\prod_{CW_{j,k}} \frac{I_{c_j} I_{c_k}}{J_{sn}^{j} A_j J_{sp}^{k} A_k} = \prod_{ACW_{j,k}} \frac{I_{c_j} I_{c_k}}{J_{sn}^{j} A_j J_{sp}^{k} A_k}$$

Assuming good transistor matching Js terms cancels out of both sides, such that

$$\prod_{CW_{j,k}} \frac{I_{c_j} I_{c_k}}{A_j A_k} = \prod_{ACW_{j,k}} \frac{I_{c_j} I_{c_k}}{A_j A_k}$$

If, j+k = m, i.e. there are total 2m junctions in the loop.

$$\prod_{CW_m} \frac{I_{c_m}}{A_m} = \prod_{ACW_m} \frac{I_{c_m}}{A_m}$$

The above equation is statement for bipolar translinear principle, i.e., in a translinear loop, the product of the clockwise junction current densities is equal to the product of the anticlockwise junction current densities. Because of this, voltage is the log of the signal and addition in the log domain is like multiplication of the original signal (i.e. log(a) + log(b) = log(ab)).

2.3.2 In MOS Translinear Circuits

The transconductance of MOS in strong inversion is linearly related to the increase in gate-source voltage above the threshold. Considering as above a loop of CW and ACW MOS transistors, which satisfies: (i) all transistors working in strong inversion and saturation, (ii) the number of CW NMOS is equal to the number of ACW NMOS, and (iii) the number of CW PMOS is equal to the number of ACW PMOS.

Consider as above, in each direction of the loop there are j NMOS and k PMOS transistors. Applying KVL across the loop:

$$\sum_{CW_j} V_{gs_j} + \sum_{CW_k} V_{sg_k} = \sum_{ACW_j} V_{gs_j} + \sum_{ACW_k} V_{sg_k}$$

$$\sum_{CW_{j,k}} \left[V_{Th_{n_j}} + V_{Th_{p_k}} + \sqrt{\frac{I_{D_j}}{K_n (W/L)_j}} + \sqrt{\frac{I_{D_k}}{K_p (W/L)_k}} \right] = \sum_{ACW_{j,k}} \left[V_{Th_{n_j}} + V_{Th_{p_k}} + \sqrt{\frac{I_{D_j}}{K_n (W/L)_j}} + \sqrt{\frac{I_{D_k}}{K_p (W/L)_k}} \right]$$

After cancelling the threshold voltage terms on both sides:

$$\sum_{CW_{j,k}} \left[\sqrt{\frac{I_{D_j}}{K_n (W/L)_j}} + \sqrt{\frac{I_{D_k}}{K_p (W/L)_k}} \right] = \sum_{ACW_{j,k}} \left[\sqrt{\frac{I_{D_j}}{K_n (W/L)_j}} + \sqrt{\frac{I_{D_k}}{K_p (W/L)_k}} \right]$$

The above equation is a statement of the MOS translinear principle. The process dependent terms Kn and Kp cannot be cancelled out even with even number of PMOS and NMOS transistors in each direction, because its summation not multiplication. However, if loop contains just one type of device then equation could be written as:

$$\sum_{CW_j} \sqrt{\frac{I_{D_j}}{(W/L)_j}} = \sum_{ACW_j} \sqrt{\frac{I_{D_j}}{(W/L)_j}}$$

2.4 Dynamic Translinear Principle

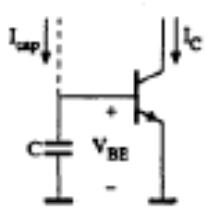

Figure 2.2: BJT Translinear Circuit

Translinear circuits are based on exponential law describing the bipolar and transistor or the MOS transistor in weak inversion, given by:

$$I_c = I_s e^{V_{BE}/V_{Th}}$$

Where all the symbols have there usual meanings.

The basis of the dynamic translinear circuits or log domain circuits, are the capacitor currents as shown in figure 2.2 which can be derived by time derivative of above equation.

$$I_{cap} = C V_{Th} \frac{\dot{I_c}}{I_c}$$

Where *C* is the capacitance value and dot shows the time derivative.

The equation represents a non linear relation between I_c and I_{cap}. On multiplying both sides of equation by I_c a direct relation can be achieved. The dynamic

translinear principle thus states "*the time derivative of a current* is *equivalent to a product of currents".* This product can be implemented using translinear principle. As there is a key role or translinear principle or its preferably known as "Dynamic translinear principle"[13].

2.5 √- Domain Principle

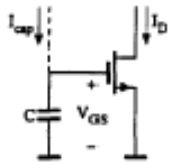

Figure 2.3: FET translinear Circuit

In analogy with the dynamic translinear principle, the √-domain principle is based on the large signal behaviour of the MOS transistor operating in strong inversion, given by:

$$I_D = \frac{\beta}{2}(V_{GS} - V_{Th})^2$$

Where all symbols have their usual meaning. Here as well the current I_{cap} can be derived by time derivative of above equation of I_d. In terms of drain current I_d the capacitor current I_{cap} is given by:

$$I_{cap} = \frac{C}{\sqrt{2\beta I_D}}\dot{I}_D$$

This equation can also be shown in a batter way:

$$\frac{C}{\sqrt{2\beta}}\dot{I}_D = \sqrt{I_D}I_{cap}$$

Thus √- domain principle can be written as "*The derivative of a current is equivalent to the product of the square root of that current and a capacitance current"*[14].

Chapter-3

Current Conveyors

3.1 Introduction

THE current-conveyor, published in 1968 [15], represented the first building block intended for current signal processing. In 1970 appeared the enhanced version of the current-conveyor: the second-generation current-conveyor CCII [16]. They used high quality PNP - NPN transistors of a like polarity and match each other but difference in current gain reduced the circuit accuracy. This is due to the base current error. The other current conveyor was devised in 1984 by G. Wilson [5] where another current-mirror configuration; known as Wilson current mirror was employed. It consists of an operational amplifier and external PNP transistors. A second generation current conveyor (CCII) was presented in 1990 using an operational amplifier and external CMOS transistors [17]. Both circuits were subject to the OP-AMP performance and again to the transistor mismatching. During that time, research societies started to notice that the voltage-mode operational amplifier is not necessarily the best solution to all analogue circuit design problems. New research findings regarding current-mode signal processing using current-conveyors were presented. Furthermore, a commercial product became available: the current-feedback operational amplifier [2, 18]. The high slew rate and wide bandwidth of this amplifier resulted in its popularity in video amplifier applications.

The current conveyor is receiving considerable attention as they offer analog designers some significant advantages over the conventional op-amp. These advantages can be pointed out as follows:

- Improve AC performance with better linearity.
- Wider and nearly constant bandwidth independent of closed loop gain.
- Relatively High slew rate (typically 2000V/?s).
- Flexibility of driving current or voltage signal output at its two separate nodes, hence suitable for current and voltage mode devices.
- Reduced supply voltage of integrated circuits.
- Accurate port transfer ratios equal to unity hence employed in low sensitivity design.
- Requirement of smaller number of passive components to perform a specific function.

In 1988 the principle of a MOS current copier was presented [19], which enabled analogue circuit designers to design different Current Conveyors using only MOS-transistors. Therefore, apart from above advantages following are the driving force behind the development of MOS Current Conveyor:

- Analog VLSI addresses almost all real world problems and finds exciting new information processing applications in variety of areas such as integrated sensors, image processing, speech recognition, hand writing recognition etc [2]. The need for low-voltage low-power circuits is immense in portable electronic equipments like laptop computers, pace makers, cell phones etc. Voltage Mode Circuits are rarely used in low-voltage circuits as the minimum bias voltages depend on the threshold voltages of the MOSFETs. However, in current mode circuits (CMCs), the currents decide the circuit operation and enable the design of the systems that can operate over wide dynamic range.
- MOS-transistors in particular are more suitable for processing currents rather than voltages because the output signal is current both in common-source and common-gate amplifier configurations. Common-drain amplifier configuration is almost useless at low supply voltages because of the bulk-effect present in typical CMOS-processes.
- MOS current-mirrors are more accurate and less sensitive to process variation.

Therefore,

MOS-transistor circuits should be simplified by using current signals in preference to voltage signals. For this reason, integrated current-mode system realizations are closer to the transistor level than the conventional voltage-mode realizations.

When signals are widely distributed as voltages, the parasitic capacitances are charged and discharged with the full voltage swing, which limits the speed and increases the power consumption of voltage-mode circuits. Current-mode circuits cannot avoid nodes with high voltage swing either but these are usually local nodes with less parasitic capacitances. Therefore, it is possible to reach higher speed and lower dynamic power consumption with current-mode circuit techniques. Current-mode interconnection circuits in particular show promising performance.

3.2 BASIC CURRENT CONVEYOR

A CC is a three or more port (X, Y, Z) network. Whose input-output relationship is given by:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & A & 0 \\ B & R_X & 0 \\ 0 & C & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix}$$

where A, B, C assume a value either 1, 0 or – 1 and RX is the intrinsic resistance offered by the port X to the input currents. For an ideal CC VX = VY and the input resistance (RX) at port X is zero. But in practical CCs, RX is a nonzero positive value.

The commonly used block representation of a CC is shown in Figure 3.1, where X and Y are the input terminals and Z is the output terminal.

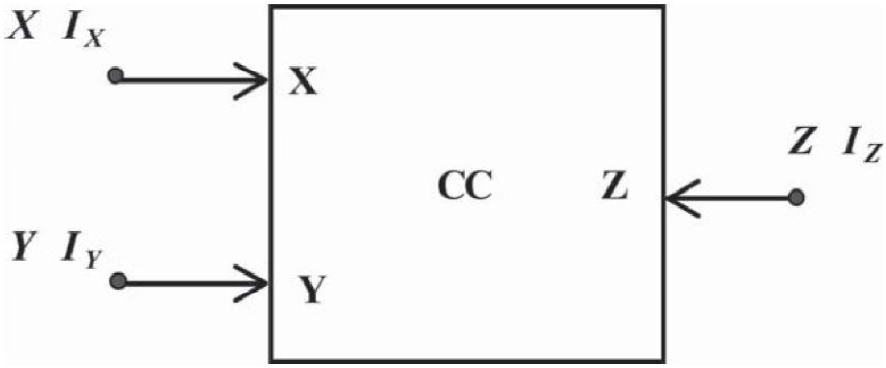

Figure 3.1: General Current Conveyor Symbol

3.3 First Generation Current- Conveyor CCI

The first generation current conveyor CCI forces both the currents and the voltages in ports X and Y to be equal and a replica of the currents is mirrored (or conveyed) to the output port Z. Port Y is used as input for voltage signals and it should not load the input voltage source by drawing current. But, in some applications, it is desirable to draw currents from the input voltage source. When A = 1, port Y draws a current equal to the current injected at port X and the configuration is termed as CCI. Figure 3.2 presents a simple MOS implementation of the first generation current-conveyor CCI. In this circuit, the NMOS transistors

M1 and M2 form a current mirror that forces the drain currents of the PMOS transistors M3 and M4 to be equal and hence the voltages at the terminals X and Y are forced to be identical.

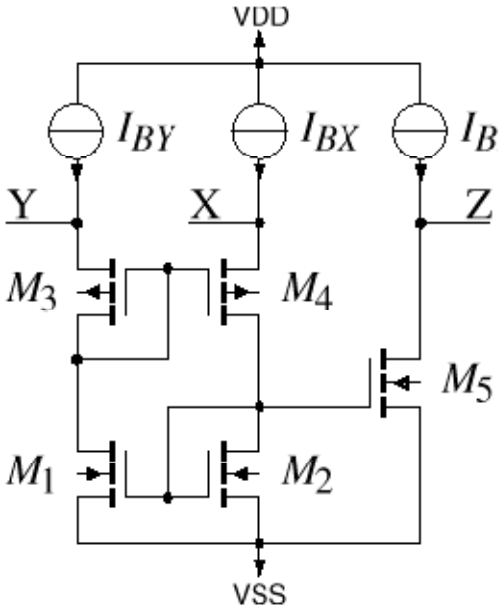

Figure 3.2: simple MOS implementation of the first generation current-conveyor CCI

Because of this low impedance at the input terminal CCI circuit can be used as an accurate current amplifier. In addition, the DC-voltage level at the current input X can be easily set to a desired value by the voltage at the Y-terminal and input voltage-to-current conversion is easier. It can also be used as a negative impedance converter (NIC), if the Y terminal is terminated with a grounded resistance R.

The impedance at the terminal X equals.

$$Z_X\Big|_{Z_Y=R} \approx -R.$$

3.4 Second Generation Current Conveyor CCII

In many applications, only one of the virtual grounds in terminals X and Y of the first generation current-conveyor is used and the unused terminal must be grounded or otherwise connected to a suitable potential. This grounding must be done carefully since a poorly grounded input terminal may cause unwanted negative impedance at the other input terminal. Moreover, for many applications a

high impedance input terminal is preferable. For these reasons, the second generation current-conveyor was developed. It has one high and one low impedance input rather than the two low impedance inputs of the CCI [16].

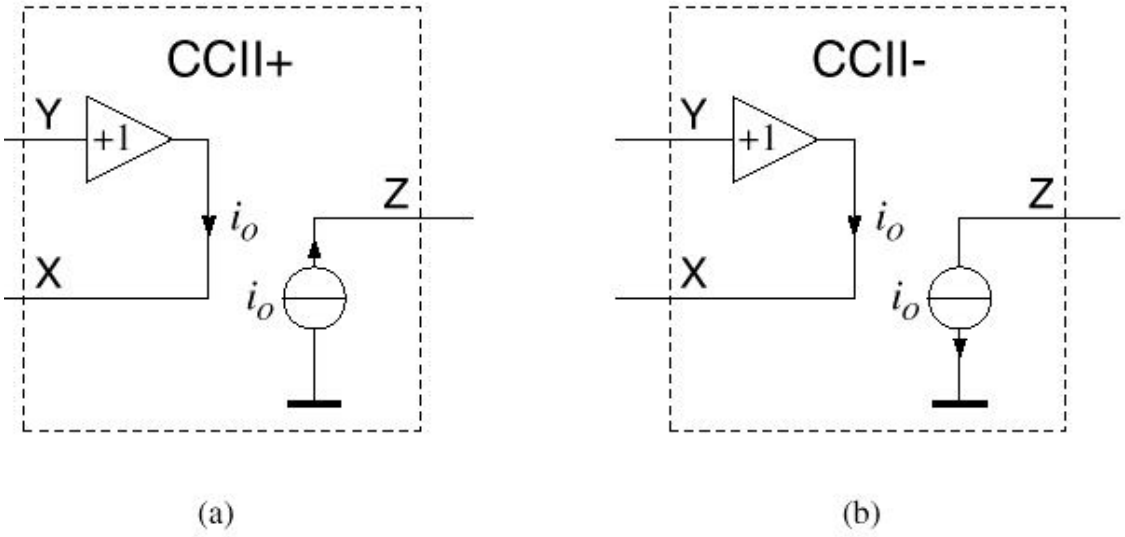

Figure 3.3: The principle of the second generation current conveyors.

(a) The positive conveyor CCII+, iz = ix.

(b) The negative conveyor CCII-, iz =- ix.

This current-conveyor differs from the first generation conveyor in that the terminal Y is a high impedance port, i.e. there is no current flowing into Y(A = 0). The Y-terminal of the second generation current- conveyor is a voltage input and the Z-terminal is a current output, the X-terminal can be used both as a voltage output and as a current input. Therefore, this conveyor can easily be used to process both current and voltage signals unlike the first generation current-conveyor or the operational amplifier.

A further enhancement to the second generation current-conveyor is that there are two types of conveyors: in the positive current-conveyor CCII+, the currents ix and iz have the same direction as in a current- mirror and in the negative current-conveyor CCII-the currents ix and iz have opposite direction as in a current buffer. The second-generation current conveyor is in principle a voltage-follower with a voltage input, Y, and a voltage output, X, and a current follower (or current-inverter) with a current input X and a current output Z connected together (Figure 3.3). The negative second-generation current-conveyor CCII- can also be considered an idealised MOS transistor, where the currents iy =ig =0 and iz =id = - ix = - is and the voltages vx = vs = vy = vg. An ideal MOS transistor is one that has a zero threshold voltage Vt and zero channel length modulation and

operates in the saturation region regardless of the drain-source voltage (positive or negative).

3.5 Third Generation Current Conveyor CCIII

Current-conveyor III was proposed in 1995 [20]. The operation of the third generation current-conveyor CCIII is similar to that of the first order current-conveyor CCI, with the exception that the currents in ports X and Y flow in opposite directions (A= -1). As the input current flows into the Y-terminal and out from the X-terminal, the CCIII has high input impedance with common-mode current signals, i.e. identical currents are fed both to Y- and X-terminals. Therefore common-mode currents can push the input terminals out from the proper operation range. Therefore this conveyor is used as current probing.

Chapter-4

CC BASED TRANSLINEAR CIRCUIT

4.1 Introduction

In a MOS/CMOS based implementation of a TL circuit the current range where the exponential V-I characteristic can be used, is typically limited to three decades compared to more than six decades for a BJT, thus restricting the choice and optimization of the operating point within the weak-inversion region.

Another fundamental limitation of MOS transistors operating in weak inversion is the poor matching of the threshold voltages which affect the distortion (and thus dynamic-range) performance of CMOS log-domain filters. Moreover, TL circuits implemented in CMOS technology operating in sub-threshold region suffer from low bandwidth limitations.

CCII-based translinear loops open a new paradigm towards the design of static and dynamic TL circuits in CMOS technology[21].

4.2 Translinear (TL) Loop

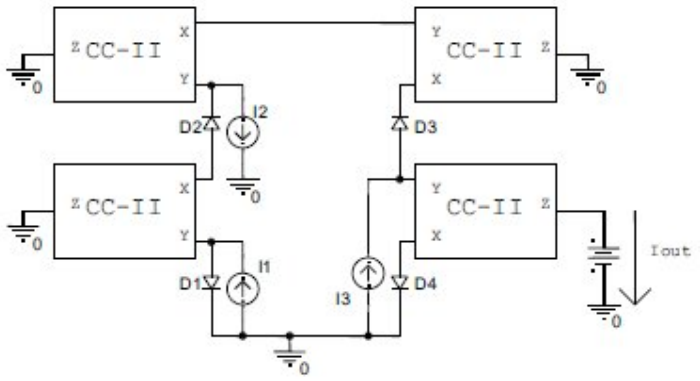

Figure 4.1: The Translinear loop using Current Conveyors[21]

The CC-II based TL loop is shown in Fig. 4.1. This technique allows decoupling of the exponential behaviour and gain, where CC-II at the output provides the gain,

whereas the diodes (also implemented in CMOS technology) take care of the exponentiation. An alternate topology with diodes D2 and D3 reversed is also possible but that requires higher voltage supplies. Using the I-V relationship of the diodes and the voltage tracking properties of the CC-II, the loop formed by the diodes D1 - D4 gives,

$$I_{D1}*I_{D3} = I_{D2}*I_{D4} \qquad ...(3.1)$$

where I_{Dx} is the current through diode Dx.

The above equation shows the multiplier/divider behaviour of the circuit in Figure4.1. Cascading more CCs and diodes can expand the TL loop further as shown in Figure 4.2. An expansion where the diodes are connected in toggled manner (alternate diodes in opposite direction) does not require any increase in the supply voltages. For such a loop, the generalized equation is given by

$$\prod_{k=1}^{3,5,\ldots} I_{D_k} = \prod_{j=2}^{4,6,\ldots} I_{D_j}$$

where I_{Dx} is the current through diode Dx.

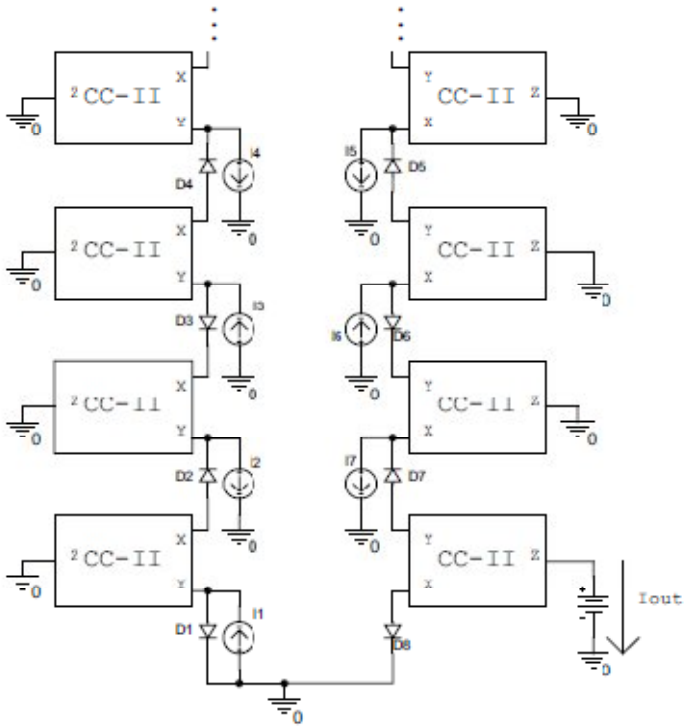

Figure 4.2: The Extended TL loop using Current Conveyors[21]

4.3 Integrator

Linear and nonlinear functions (differential equations) can be implemented by DTL circuits. As an example, a lossy integrator is implemented as shown in Fig. 7(a). This design is not meant for optimization with respect to the number of current conveyors used, however, the generalization of the CC-II based TL loop is proved for DTL circuits. The Transfer function of the integrator can be derived as follows. For the TL loop in Fig. 4.3 and using Eqn. 3.1, we get,

$$I_{in} * I_3 = I_{out} * (I_2 + I_c)$$

the current through a capacitor depends upon the time derivative of the voltage across it, therefore, we get,

$$I_2 I_{out} + C V_{Th} I_{out} \left(\frac{\dot{I}_{out}}{I_{out}} \right) = I_{in} I_3$$

where V_{Th} is Thermal voltage and I^* denotes time derivative of I_{in} in time domain,or, in s-domain,

$$\frac{I_{out}}{I_{in}} \approx \frac{I_3}{I_3 + sCV_{Th}}$$

The equation shows that the circuit in Figure 4.3 behaves as a lossy integrator with corner frequency (ω_c) given by,

$$\omega_c = I_2 / CV_{Th}$$

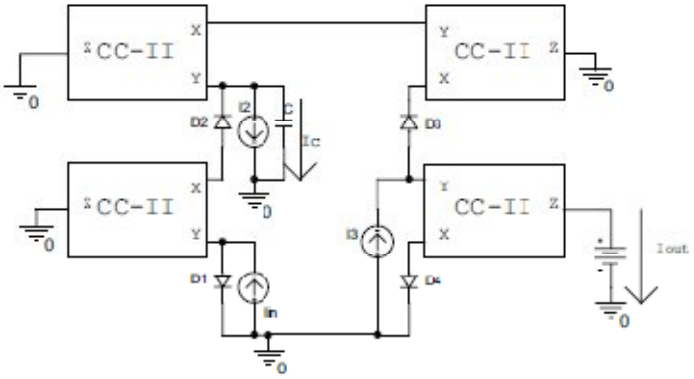

Figure 4.3: The Integrator formed using the proposed topology[21]

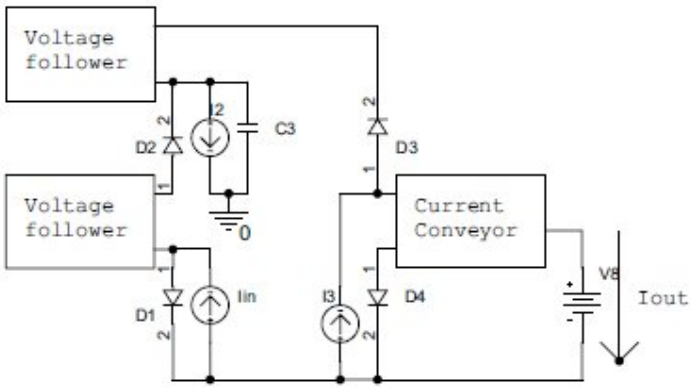

Figure 4.4: The Optimized Integrator

The circuit shown in Fig. 4.3 can be optimized as shown in Fig. 4.4 to save silicon area as well as the power dissipation. This design does not change the output function or any other performance characteristics circuit, however in this case, we do not have any generality.

A Biquadratic filter is also formed to demonstrate the application of the loop in filter design. The filter is formed using an Integrator-Integrator topology as shown in Fig. 4.5.

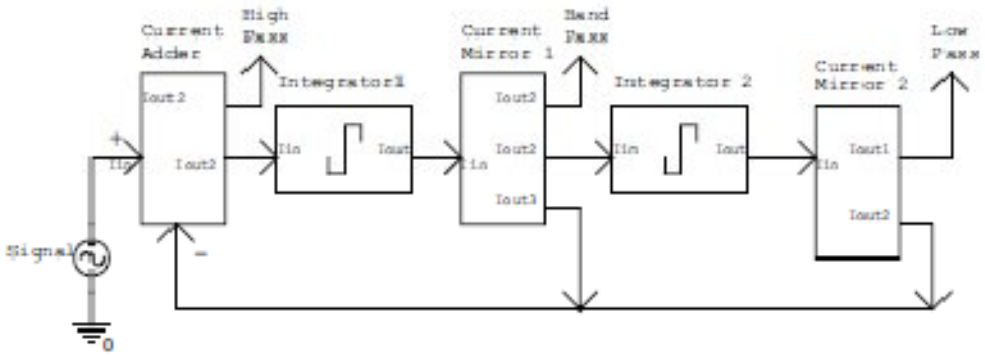

Figure 4.5: The Integrator-Integrator topology[21]

The integrators were realized with the help of the CC-II TL loop as shown in Fig. 4.3 and cascaded with the help of simple mirrors. The expressions for Low Pass, High Pass and Band Pass Transfer functions, Center Frequency (W_o) and Quality

Factor (Q) are shown in Table 1. From the table, it can be easily inferred that the capacitor tuning as well as the current tuning can control all these parameters.

Table 4.1. Transfer functions of the Biquad

High-Pass	$\frac{s^2 + (a+b)s + ab}{s^2 + (W_o/Q)s + W_o^2}$
Band - Pass	$\frac{s + b}{s^2 + (W_o/Q)s + W_o^2}$
Low – Pass	$\frac{1}{s^2 + (W_o/Q)s + W_o^2}$
Center Frequency (W_o)	$\sqrt{\frac{I_3(I_{12}+I_{13}) + I_2 I_{12}}{C_1 C_2 V_t^2}}$
Quality Factor (Q)	$\frac{\sqrt{C_1 C_2 \{I_3(I_{12}+I_{13}) + I_2 I_{12}\}}}{I_2 C_2 + I_{12} C_1 + I_3 C_2}$

As shown in Table 4.1,

$$a = \frac{I_2}{C_1 V_t}, b = \frac{I_{12}}{C_2 V_t}, \Lambda = \frac{I_3}{C_1 V_t}, B = \frac{I_{13}}{C_1 V_t}$$

and I2, I3 are currents through diodes D2 and D3 in Integrator-1 (as shown in Fig. 4.3 whereas I12 and I13 are similar currents in Integrator-2 (as shown in Fig. 4.5).

4.4 Proposed Integrator Circuit

We have studied in chapter-2, the log domain principle or dynamic translinear principle, which is applicable on BJT or MOS in weak inversion, and √- domain principle, based on large signal behaviour of MOS. With the growth in technology and need for lower power circuits things has shifted to MOS in place of BJT but there are following limitation of MOS-TLC:

- BJT offers product relation whereas MOS provides sum of roots relation making circuit complex.
- BJT follows exponential law over a wide current range, whereas range of MOS for ideal square law is limited.

- Another limitation of MOS transistors operating in weak inversion is the poor matching of the threshold voltages which affect the performance of CMOS log-domain filters.
- TL circuits implemented in CMOS technology operating in sub-threshold region suffer from low bandwidth limitations.

So, a circuit has been proposed to implement log domain principle with MOS by using *Current Conveyors*.

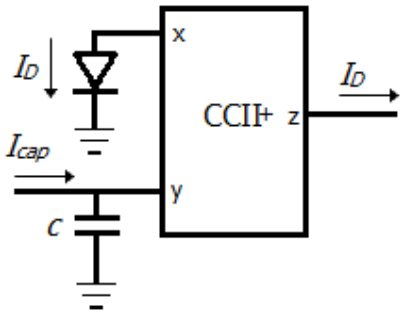

Figure 4.6: Current Conveyor based translinear circuit.

In the figure 4.6 the CCII at the output provides the gain, whereas the diodes (also implemented in CMOS technology) take care of the exponentiation. Hence we can have a similar relation as that of BJT exponential function:

$$I_{cap} = CV_{Th}\frac{\dot{I_D}}{I_D} \qquad \ldots(3.2)$$

This relation can be used for the implementation of integrator. In general any integrator can be described by a general differential equation:

$$\dot{y} = x$$

Where, dot represents the differentiation w.r.t. dimensionless time τ and y and x represents the output and input signals. This dimensionless equation has to be converted into an equation with proper dimensions so that log-domain principle is applicable. Therefore, y and x are converted into currents I_{out} and I_{in} respectively.

Second, the dimensionless time τ has to be transformed to the time t with dimension (s). In this transformation, the term CV_{Th} has to be introduced. A possible time transformation is:

$$t = \frac{CV_{Th}}{Io_1}\tau$$

where Io_1 is DC bias current. After these transformations, the differential equation describing the integrator reads:

$$CV_{Th}\dot{I}_{out} = Io_1 I_{in}$$

From the above equation the term $\dot{I}_{out}$ can be eliminated by using log domain principle. The term $\dot{I}_{out}$ is replaced by the product of terms I_{out} and I_{cap}. By using equation (3.2) and replacing I_D with I_{out} the expression can be written as:

$$I_{cap} I_{out} = Io_1 I_{in}$$

The overall block schematic of this integrator can be implemented as shown in figure.

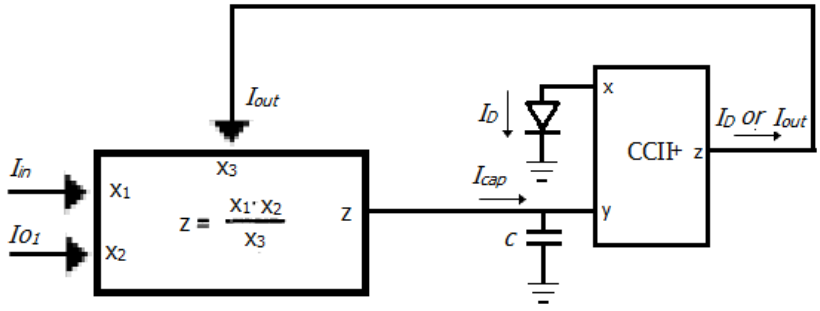

Figure 4.7: Proposed Integrator using CCII translinear circuit.

4.5 Simulation Results

In this section all the simulations were carried out in ORCAD PSPICE with circuit implementation using 0.18µm CMOS technology.

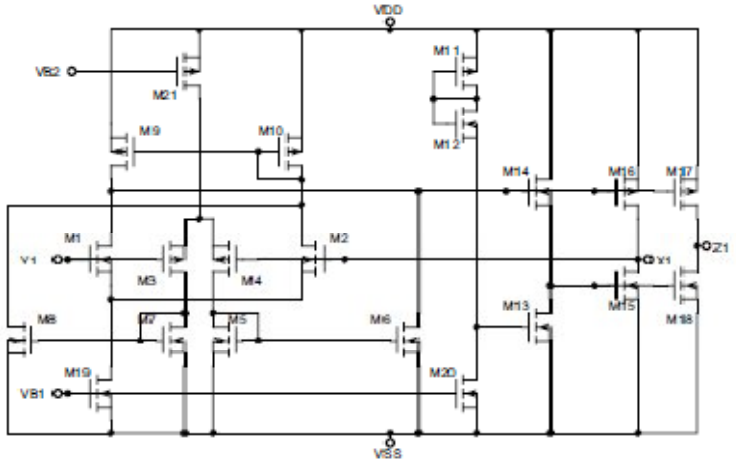

Figure 4.8: The CCII circuit used [22]

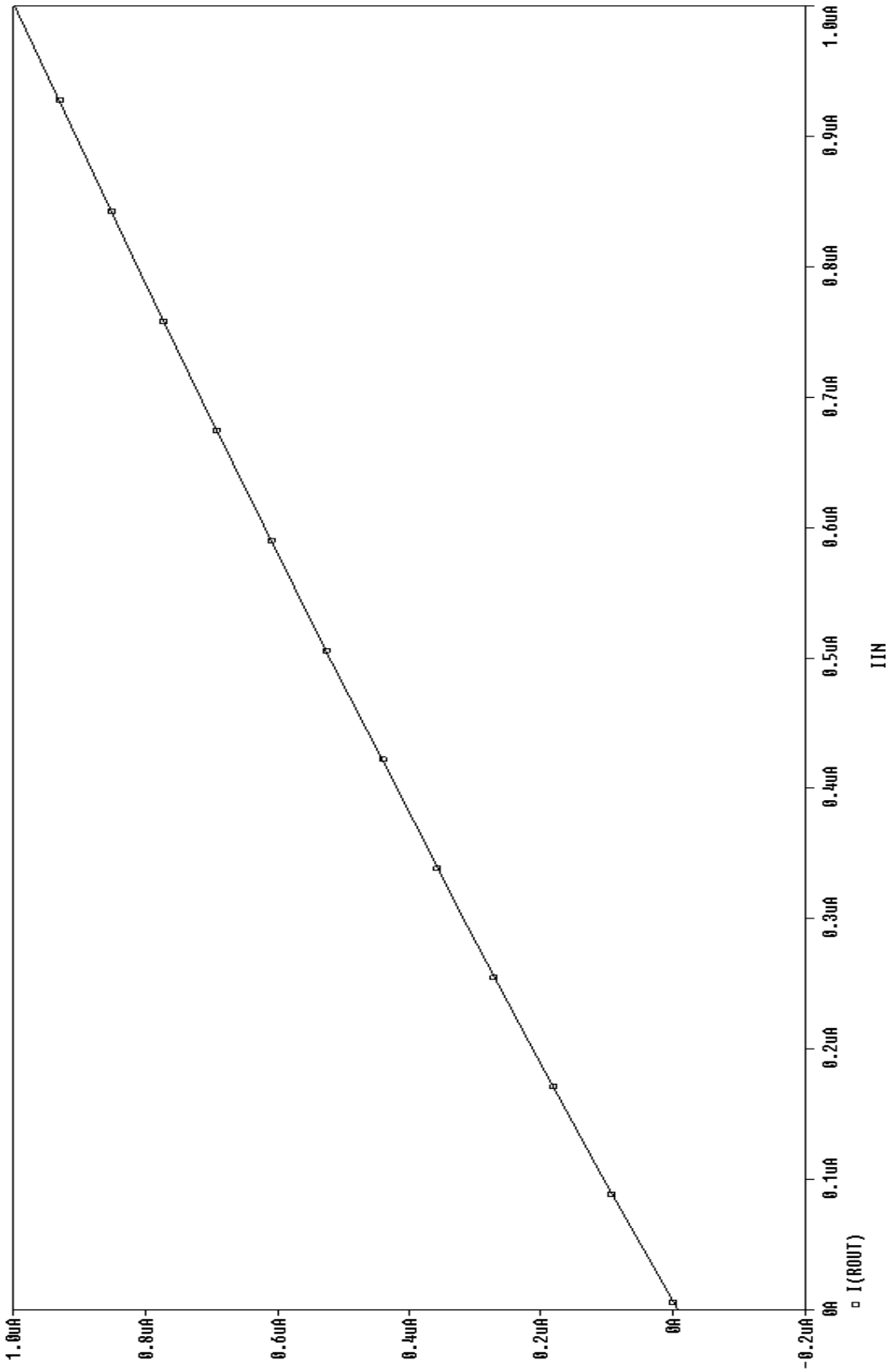

Figure 4.9: The Multiplier output response

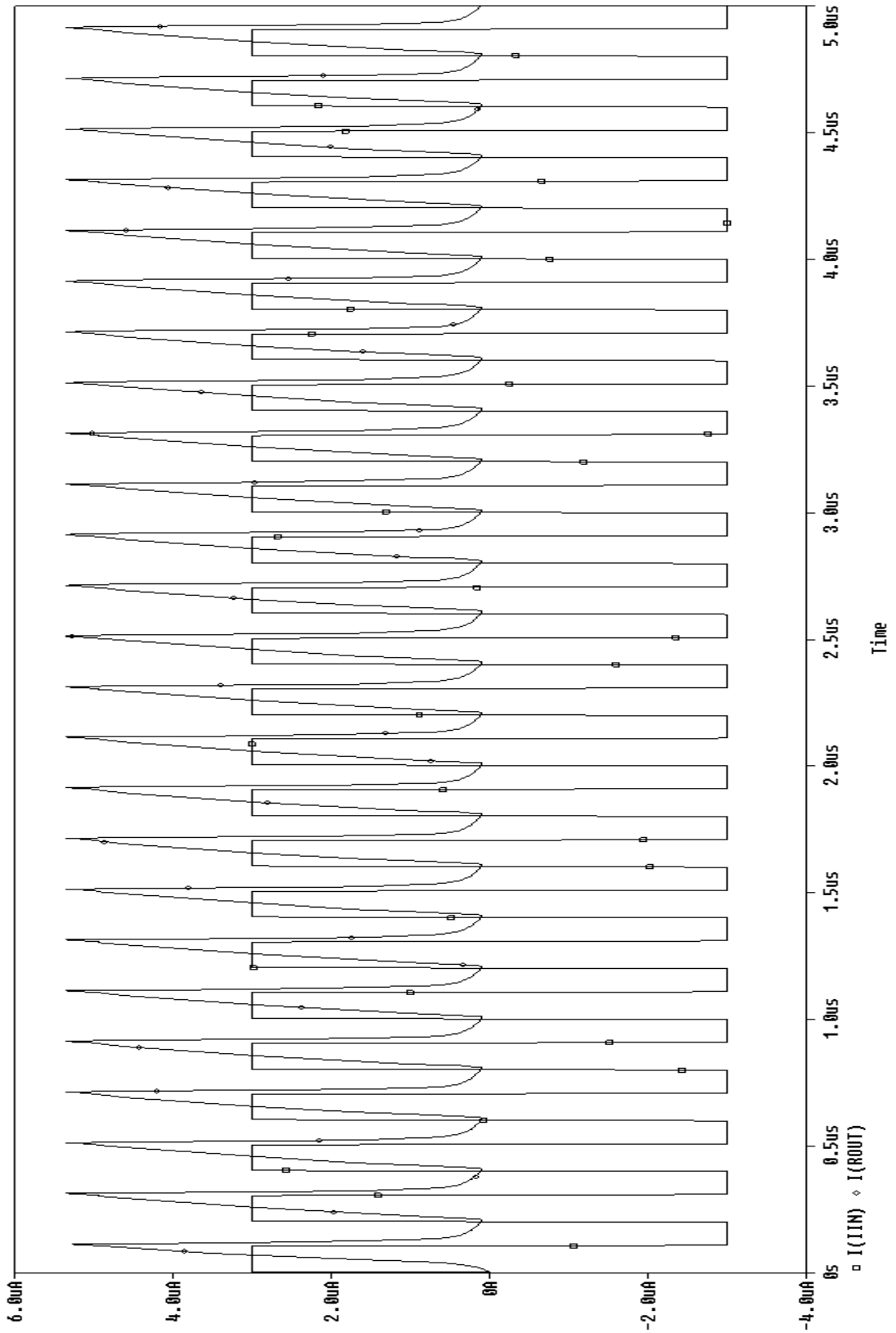

Figure 4.10: The Transient response for proposed integrator

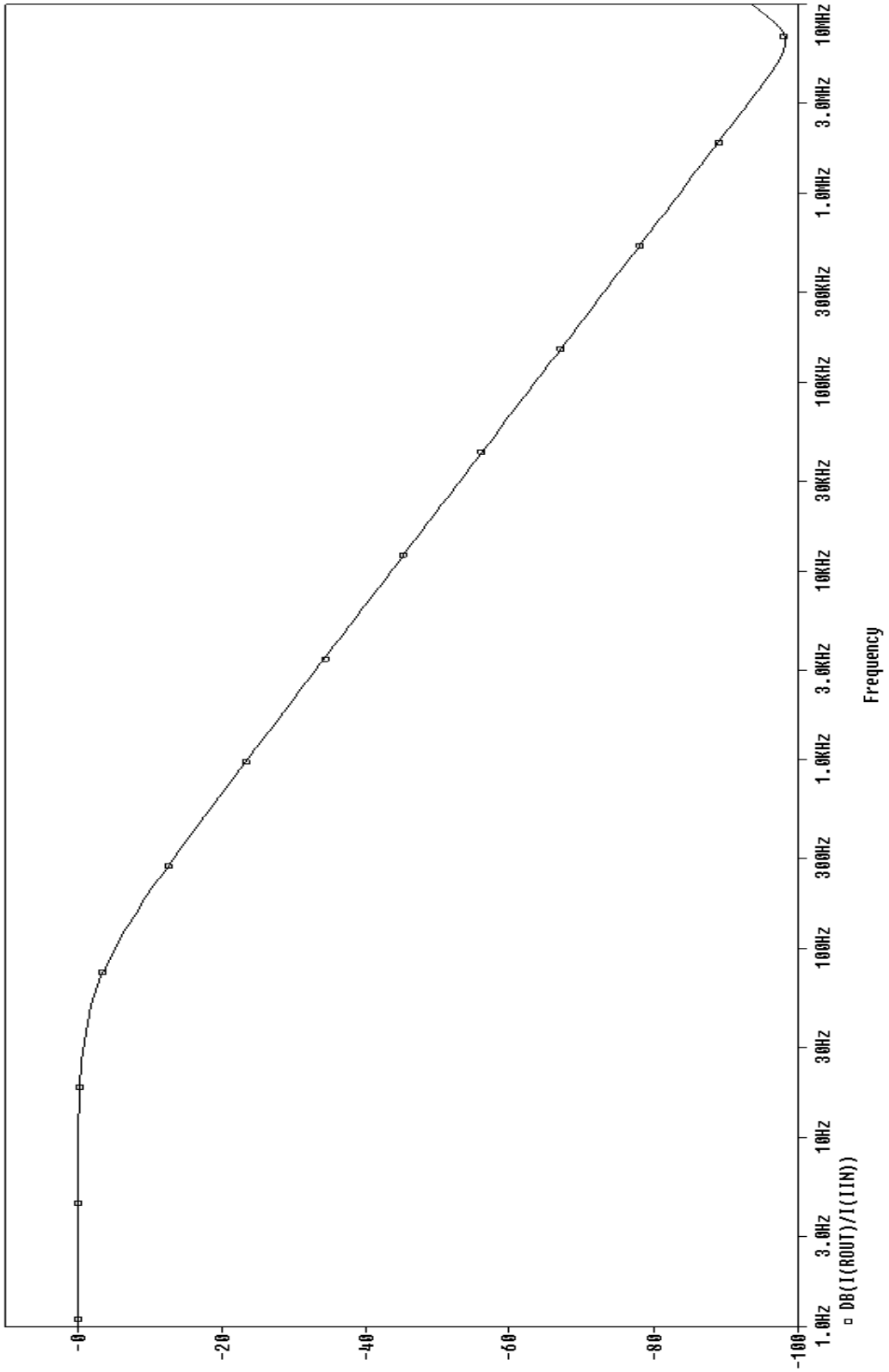

Figure 4.11: Frequency response in DB of proposed integrator

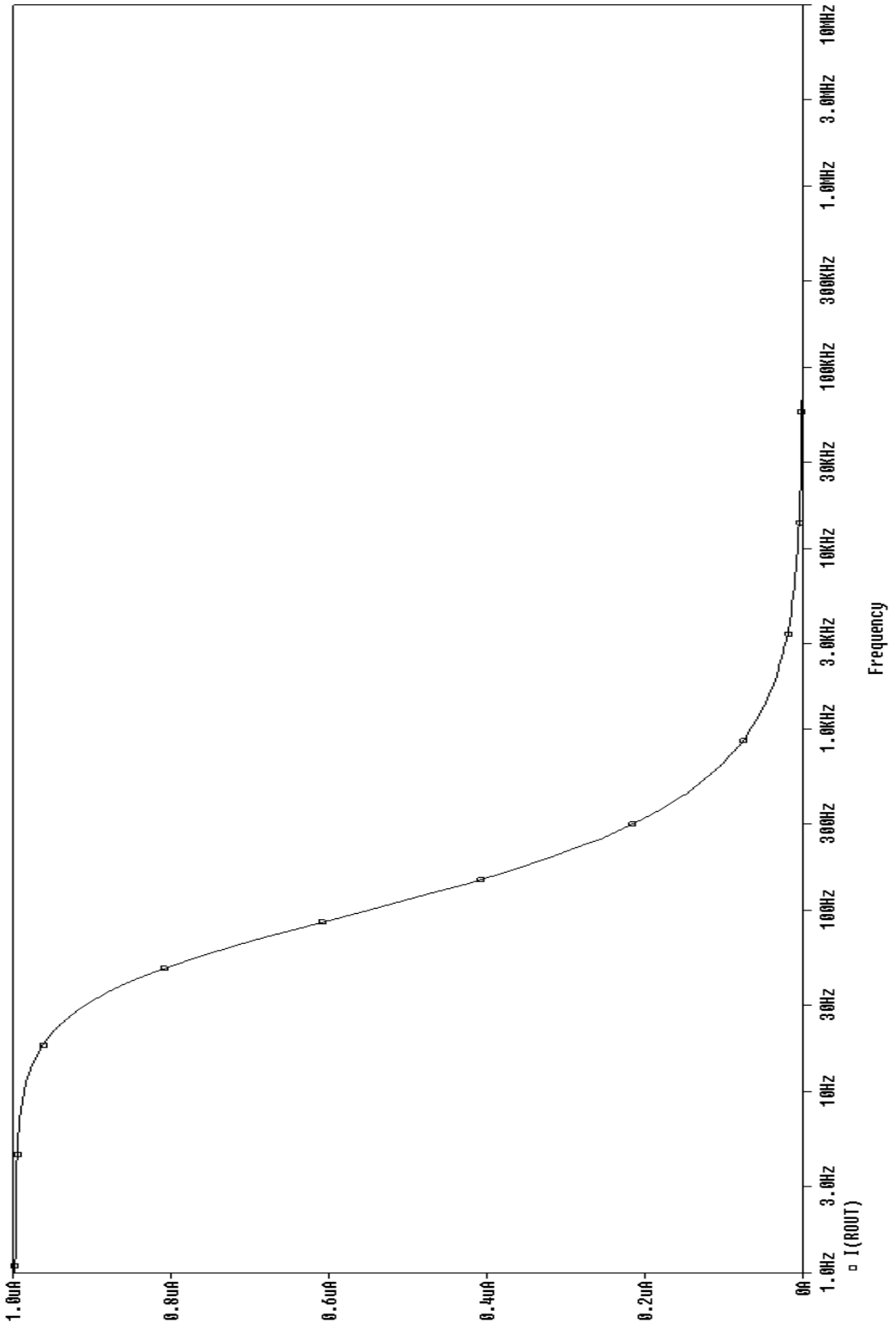

Figure 4.12: The frequency response of proposed integrator

Chapter-5

AGC

5.1 Introduction

Automatic gain control (AGC) is an adaptive system found in many electronic devices. The average of the output signal level is fed back to adjust the gain to an appropriate level for a range of input signal levels. An AGC is a closed-loop system that automatically adjusts the gain such that the output level stays within a desired range. As known, AGCs play a very important role in modern hearing aid devices and communication systems. For example, without AGC the sound emitted from an AM radio receiver would vary to an extreme extent from a weak to a strong signal; the AGC effectively reduces the volume if the signal is strong and raises it when it is weaker. Many published literatures have proposed different methods to design the AGC circuits. However, most of the AGCs work in voltage-mode. As a result, there are some restrictions in such: high supply voltage and power consumption, narrow frequency response, narrow dynamic range, complicated circuit details and absence of electronic control.

5.2 Proposed Circuit AGC1

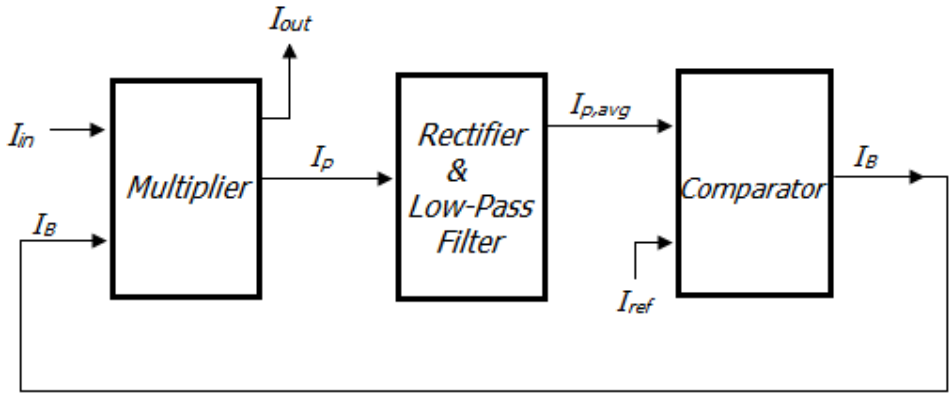

Figure 5.1: The proposed circuit of AGC1

The proposed AGC scheme can be found in Fig. 5.1. It consists of the multiplier whose gain can be adjusted by an input bias current. The current-mode precision

rectifier is employed to convert the output sinusoidal current to a positive half wave. Subsequently, this signal will be applied to current-mode first-order low pass filter to change it to a DC current level. After that, the DC current is compared to a reference current. The output current of comparator is used as multiplier control current to control the gain of the current multiplier.

The circuits used for the multiplier(fig. 5.2), rectifier(fig. 5.3) and comparator(fig. 5.4) are as follows.

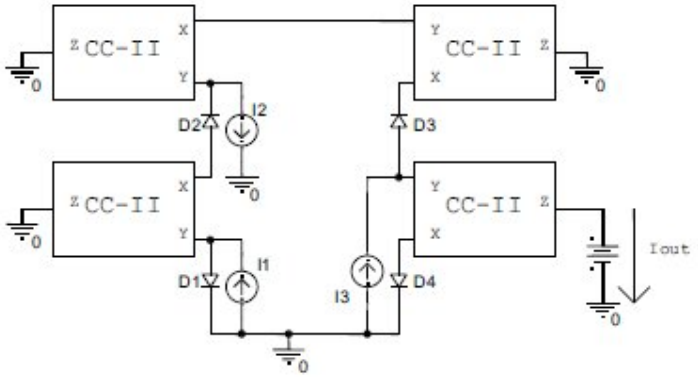

Figure 5.2: The Multiplier

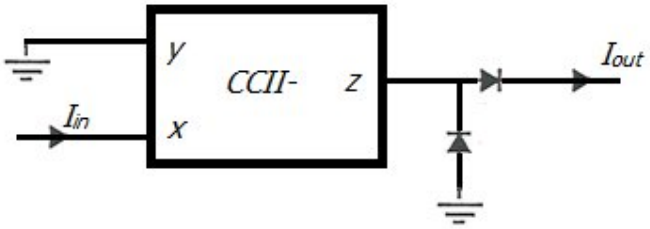

Figure 5.3: Half wave precision Rectifier

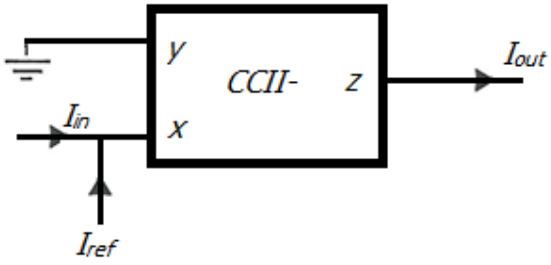

Figure 5.4: Comparator

The output response of this automatic gain control circuit is as shown in the figure 5.5 and 5.6. The circuits are set as to give an output response fixed at 1uAmp.

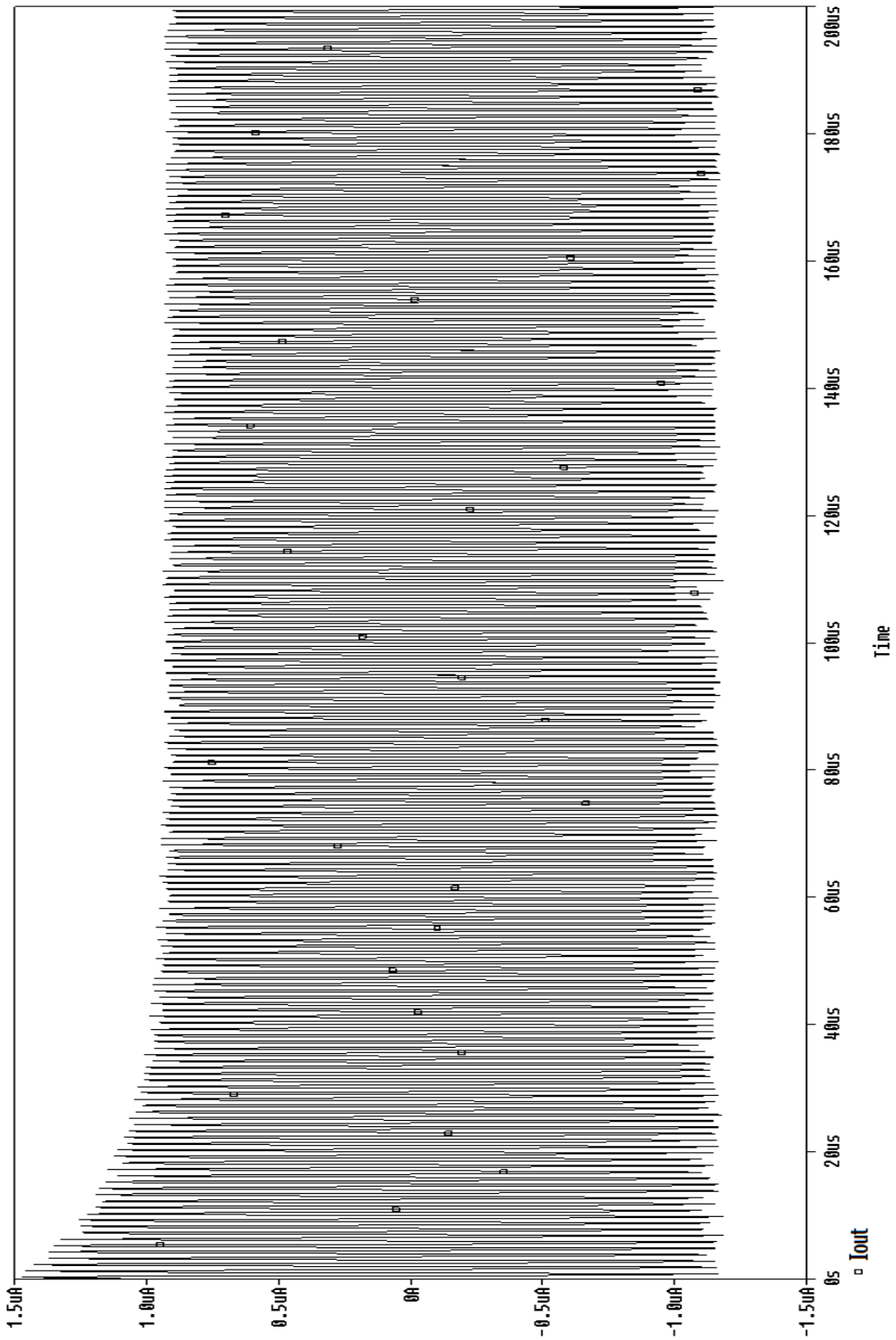

Figure 5.5: The output current of AGC1 when input current is increased

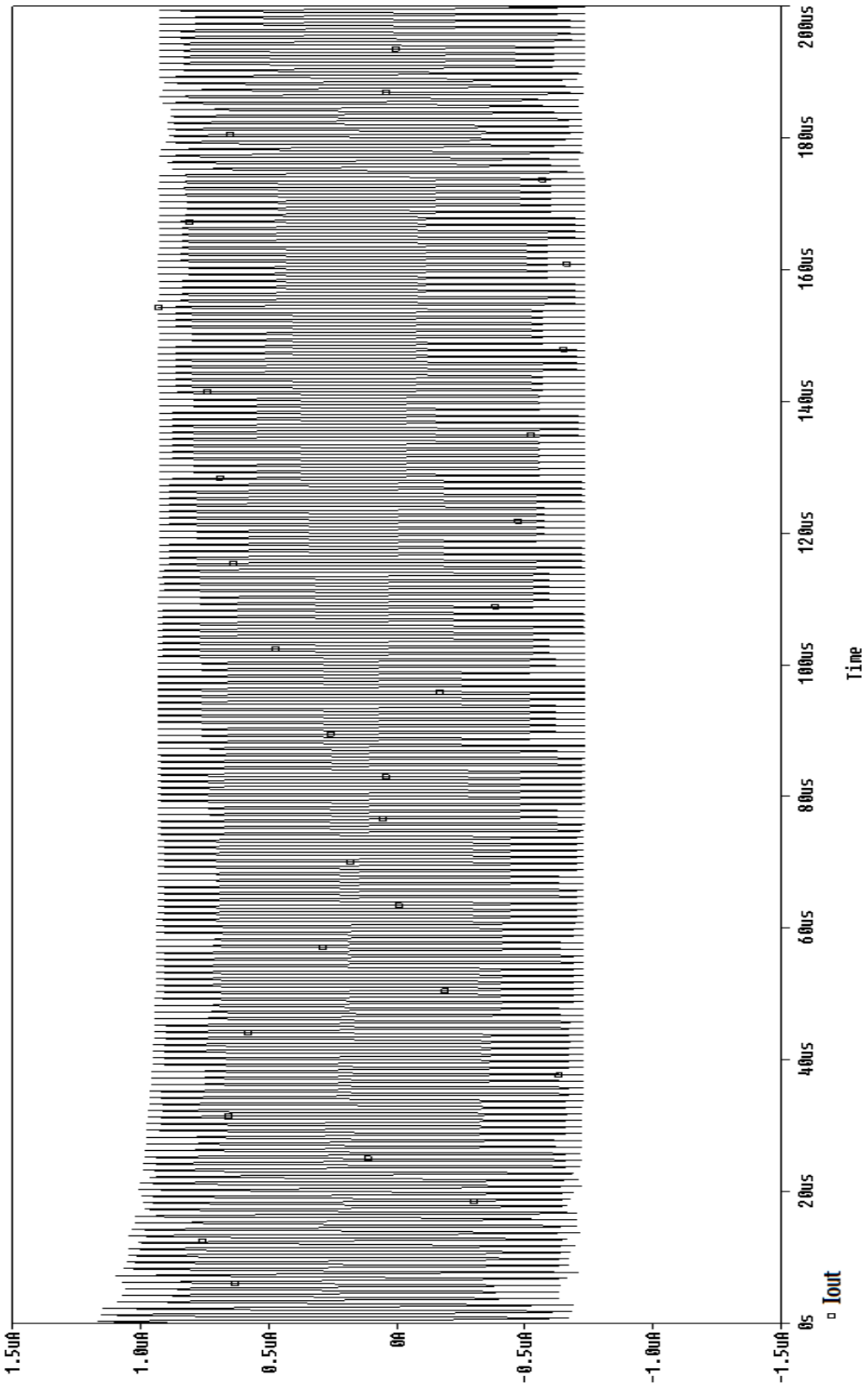

Figure 5.6: The output current of AGC1 when input current is decreased

The multiplier circuit consists of the only forward biased diodes, hence the circuits only entertains the +ve half of the circuit. To avoid that an additional D.C. biasing is required in the circuit such that on application of input the diodes are all forward biased, which is removed from the circuit after multiplier action is done. But still it can be seen from the waveform that this circuit is able to modulate only the +ve half of the waveform, which turns out to be a drawback for the circuit. This drawback is removed in the next proposed circuit.

5.3 Proposed Circuit AGC2

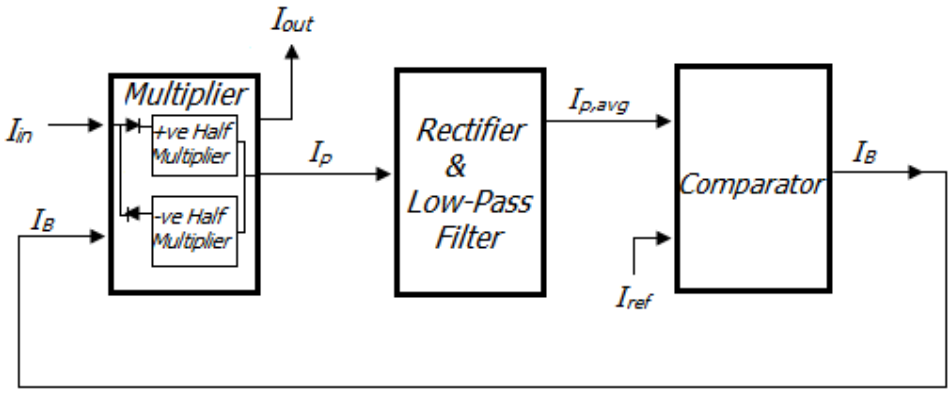

Figure 5.7: The proposed circuit of AGC2

The proposed AGC scheme found in Fig. 1 consists of two multipliers whose gain can be adjusted by an input bias current. The +ve half multiplier is responsible for processing the +ve half of the waveform while the –ve half multiplier prcesses the –ve half of the waveform. This helps removing the drawbacks of the previous circuit. The current-mode precision rectifier is employed to convert the output sinusoidal current to a positive half wave. Subsequently, this signal will be applied to current-mode first-order low pass filter to change it to a DC current level. After that, the DC current is compared to a reference current. The output current of comparator is used as multiplier control current to control the gain of the current multiplier.

The output waveform of the circuit is shown in figure 5.8.

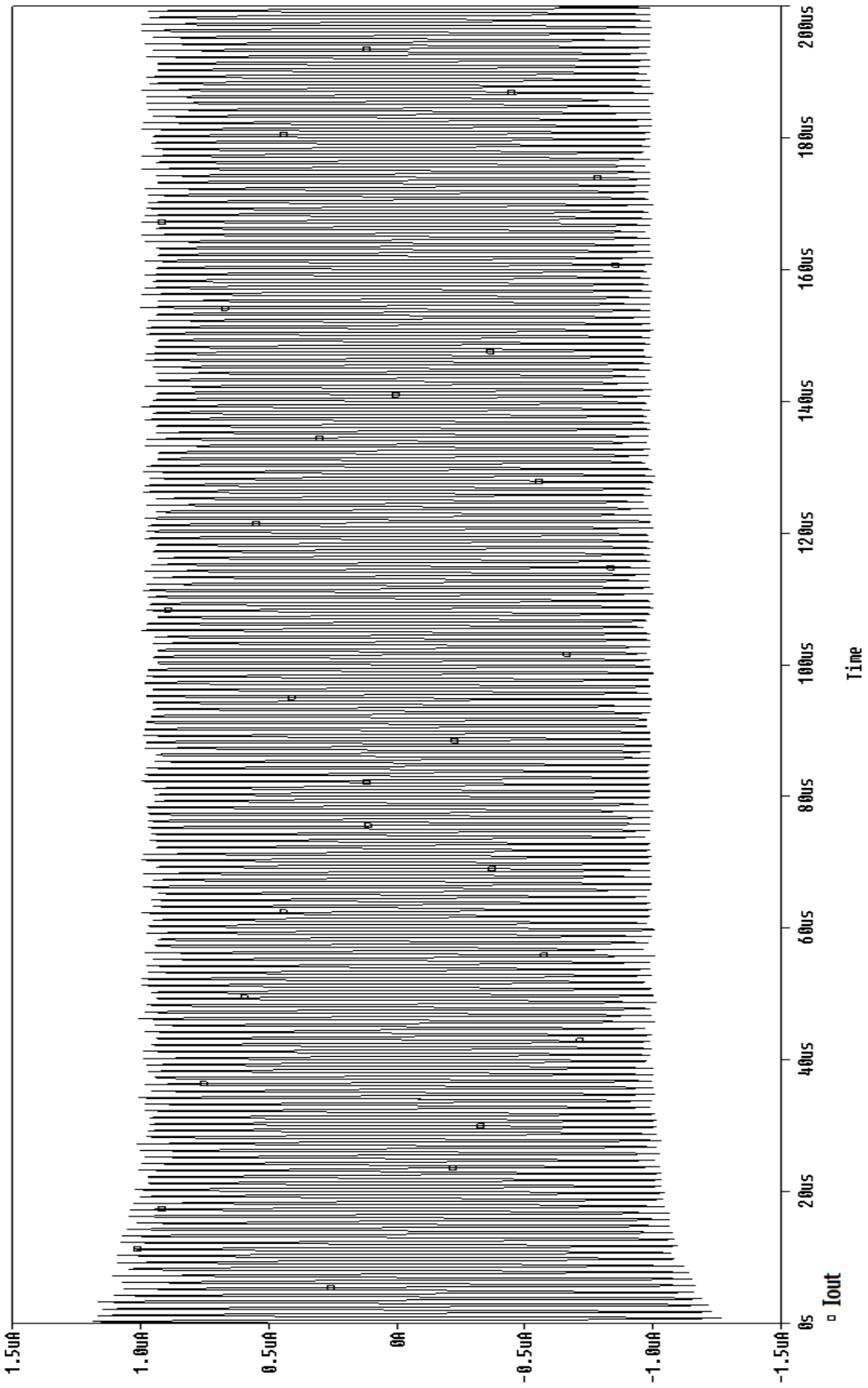

Figure 5.8: The output current of AGC2 when input current is increased

5.4 Proposed Circuit AGC3

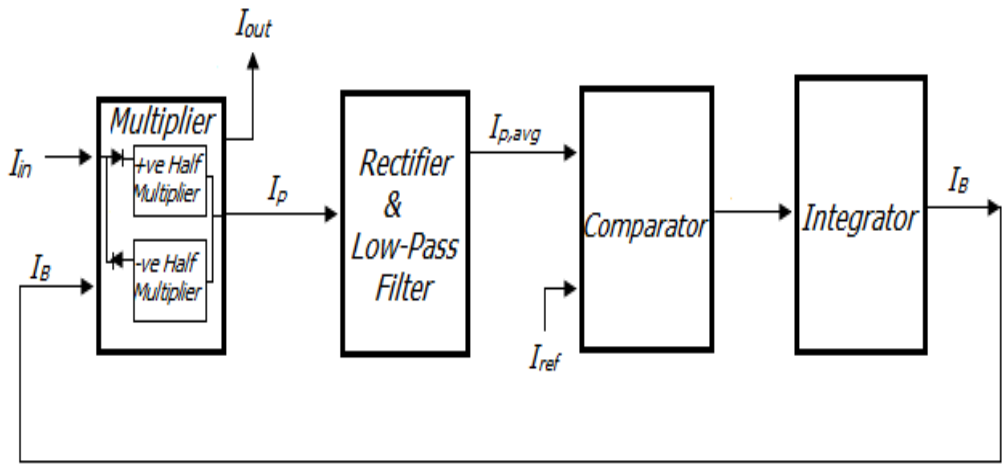

Figure 5.9: The proposed circuit of AGC3

The proposed AGC scheme found in Fig. 5.9 consists of two multipliers whose gain can be adjusted by an input bias current. The +ve half multiplier is responsible for processing the +ve half of the waveform while the –ve half multiplier prcesses the –ve half of the waveform. This helps removing the drawbacks of the previous circuit. The current-mode precision rectifier is employed to convert the output sinusoidal current to a positive half wave. Subsequently, this signal will be applied to current-mode first-order low pass filter to change it to a DC current level. After that, the DC current is compared to a reference current, the remaining current is employed as input current of integrator which is the major difference for the previous circuits. The output current of integrator is used as multiplier control current to control the gain of the current multiplier.

The output waveform of the circuit is shown in figure below.

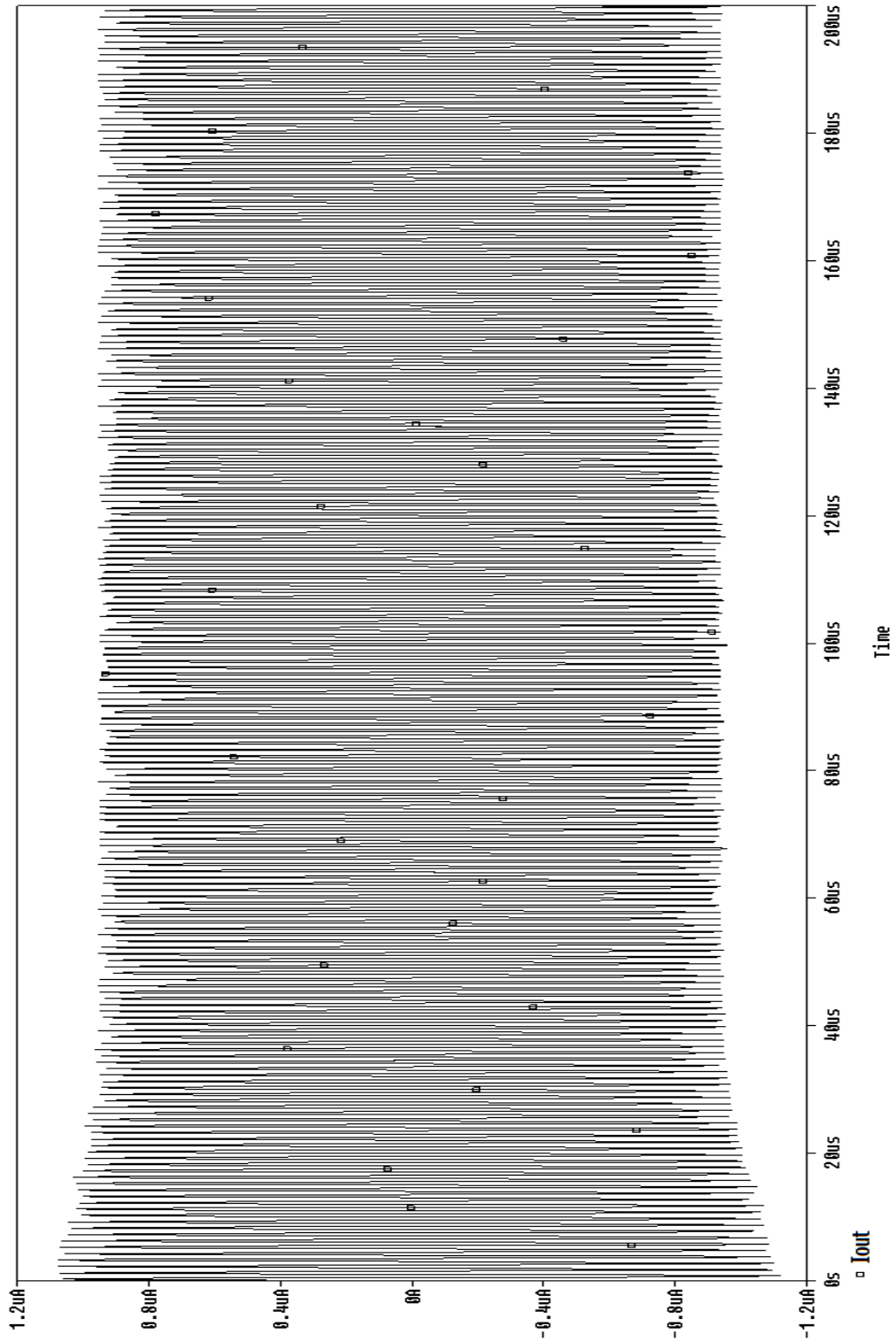

Figure 5.10: The output current of AGC2 when input current is increased

This circuits shown shows a batter control range over the input variations as compared to AGC1 and AGC2.

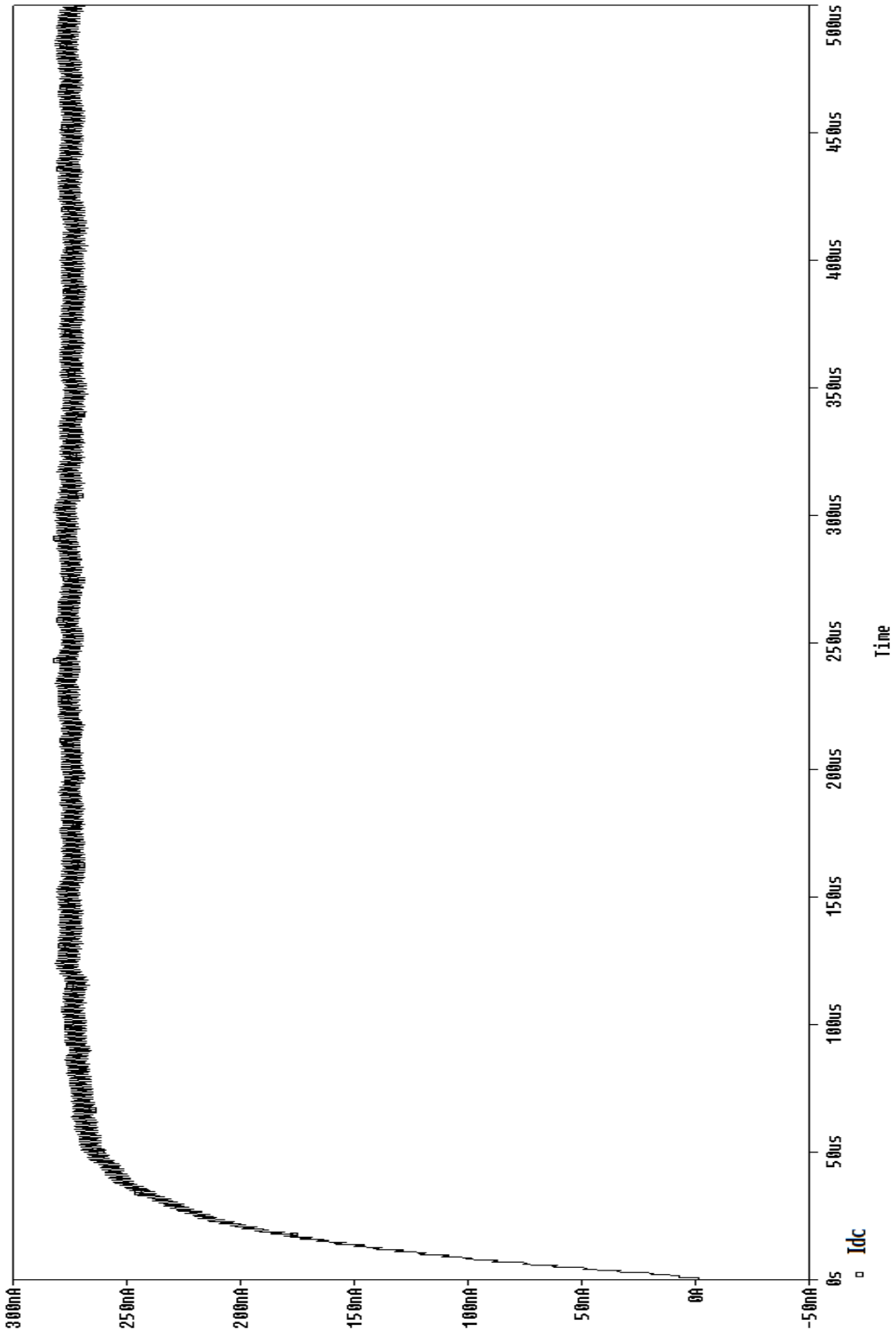

Figure 5.11: The output of the rectifier and low pass filter

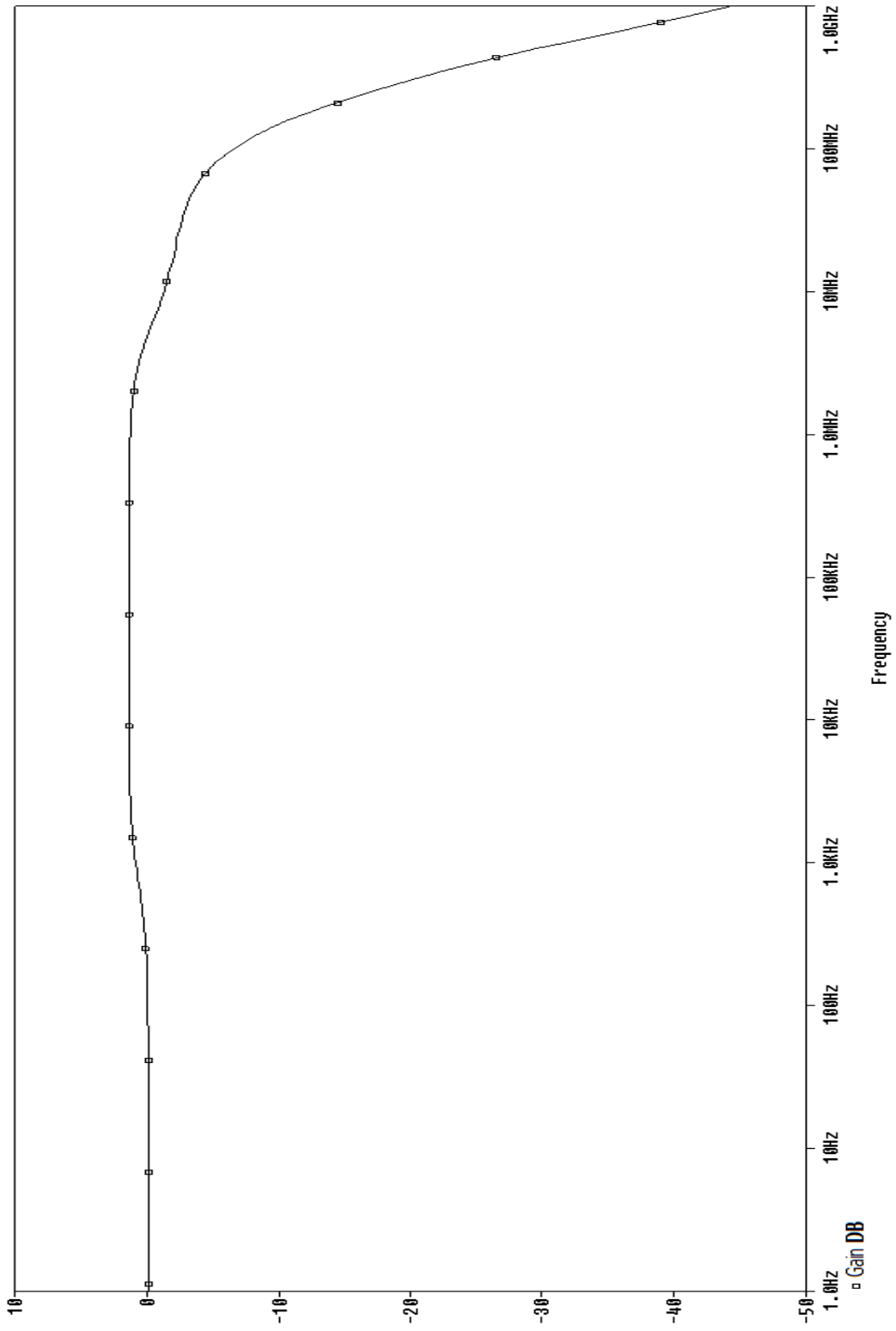

Figure 5.12:The frequency response proposed AGC Circuits

Chapter-6

Conclusion

In this thesis, A design technique for implementing STL and DTL circuits using CMOS CC-II based TL loops has been studied. This technique makes use of the exponential property of the diodes and the current conveying and voltage following properties of the CC-II. The operating range of the loop is bound by the bandwidth of the CC architecture and also the CMOS technology used. Using wider bandwidth CCs and shorter channel processes, the performance can be improved significantly. The power required is also very low which makes this technique highly suitable for low power filter design.

A new integrator topology is introduced which is implemented using current conveyor as a translinear element. This integrator exploits the log domain principle even working with the MOS transistors in strong inversion region.

Three new AGC circuits has been proposed. The first one is a single multiplier circuit with a comparator output as its biasing current. This circuit is able to control the gain of the +ve envelop of the input waveform only. The second AGC is a double multiplier circuit with comparator output as there biasing current. This circuit overcome the drawbacks of the first circuit. The third circuit is an enhanced version of the second with a double multiplier and an integrator after the comparator whose output is used as the biasing current. This circuit shows a much stable response and the current range of the circuit has also increased.

All the circuits are implemented using 0.18um technology and simulated using Pspice.

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