LOW POWER, HIGH SPEED CURRENT CONVEYOR BASED CURRENT COMPARATOR IN PIPELINED ADC

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CERTIFICATE

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I wish him success in all his endeavours.

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ABSTRACT

A current mode technique for the design of flash ADCs is presented. The current mode technique allows the necessary voltage swing for a given dynamic range to be reduced while at the same time eliminating the need of large capacitors on which to store charge. This thesis presents a flash ADC (Analog to Digital Converter) modules comprising of Current Mirror Circuits, Comparator Circuits and Encoder Circuit. A CCII network and positive feedback properties based novel approach of designing Current Comparator Circuit has been employed, which gives reduction in response time and hence increases the bandwidth. This makes the structure suitable for wide band applications. The presented ADC's comparator structure uses the thermometer code for conversion of analog signal to digital one. The circuit has been simulated using the PSPICE simulator for 180nm CMOS technology with 1.8V supply to get satisfactory output.

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CHAPTER 1: INTRODUCTION

1.1 Motivation

From past few decades, towards real time signal processing more importance is being given. As most physical variables are analogue in nature and can take on any value within a continuous range of values e.g. temperature, audio signals, speed, hence the systems are design for interfacing real world signals (analogue signals) with the digital one, as digital circuits has many advantages over the analog signals namely robustness, noise immunity, low bandwidth, easily encrypted, secure, low cost etc. Minimization in power consumption in these devices can be achieved by moving towards smaller feature size processes. Analog current mode techniques are used widely due to high speed, low power application VLSI CMOS technologies. The information processed by lumped electric networks can be represented by either the nodal voltages or branch currents of the networks. The former are referred to as voltage-mode circuits whereas the latter are known as current-mode circuits. Together, they provide a complete characterization of the behavior of the networks. The main advantage of using current mode technique is because the non linear characteristics exhibited by most FETs, a small change in input voltage results in much larger change in the output current. Hence dynamic range of current mode technique is larger than voltage mode circuits for fixed voltage; secondly they are much faster compared to voltage mode circuits, as parasitic capacitances will not affect the operating speed by significant amount. It is thus desirable to push the analog/digital boundary closer to the real world, where the system can take better advantage of the high speed digital circuit. The circuit which is used to convert analog signal (continuous) into digital (discrete), is called ADC (Analog to Digital Converter). It is a mixed signal device that provides an output that represents input voltage or current level. The basic structure of ADC is shown in figure 1.1.

V1>V2 = +Vref = logic 1

V1<V2 = -Vref = logic 0

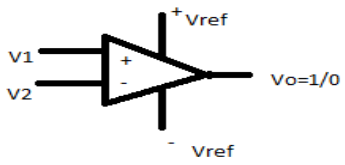


Fig 1.1. ADC Design

Nowadays high-speed devices like high-speed ADCs, operational amplifiers became of great importance and for these high- speed applications, a major thrust is given towards low power methodologies. The performance limiting blocks in such ADCs are typically inter stage gain amplifiers and comparators in which comparators are the most important. Therefore, the various design issues related to speed, gain, power dissipation, offset and resolution are of paramount importance. Dynamic comparators are being used in today's ADCs extensively because these comparators are high speed, having zero static power consumption and provide full-swing digital level output voltage in shorter time duration but consume more power dissipation and give high input-referred offset voltage.

1.2 Thesis Organization

The thesis provides a flash ADC design using the current conveyor (CCII) based current comparator for high speed applications. As CCII based technique of comparator design provide short propagation delay, power dissipation and precision. The thesis has been organized as follows:

Chapter 1 gives the introduction about motivation and organization of thesis.

Chapter 2 provides Literature Survey for ADC's components namely current mirror, current comparator and encoder circuits.

Chapter 3 introduces the ADC's conceptual and conventional design.

Chapter 4 discussed the proposed FLASH ADC design.

Chapter 5 provides post layout simulation results.

Chapter 6 conclusion and future scope.

CHAPTER 2:

LITERATURE SURVEY

2.1 Current mirror

Current mirror are the basic building blocks of almost all analog and mixed mode structures. Hence characteristics of these current mirrors decide their performance. Depending upon the characteristics of the input output ports, several implementations for the current mirrors are available. A current mirror reverses the direction of current injected into the low impedance input port and allows its true or scaled version to flow into high impedance output port. However the direction of output current can also be reversed. Current mirrors can be used as either active load or as biasing networks. The use of current mirrors in biasing structures results in better insensitivity to the variations in power supply and temperature. For high performance system, current mirror circuit must possess the following characteristics:-

- Current transfer ratio, which is precisely set by the (W/L) ratios, independent of temperature.
- Very high output impedance (high $R_{out\ and}$ low C_{out}). As a result, the output current is independent of output voltages.
- Low input resistance (R_{in}).

Almost all the analog circuit structures whether they operate as current mode devices or voltage mode devices, use current mirror in their design. Namely:-

- Operational amplifiers.
- Operational trans-conductance amplifier.

- Operational trans-resistance amplifier.
- Current feedback amplifier.
- Current conveyor.
- Digital to analog converters.
- Analog to digital converters.

The basic current mirror can be implemented using MOSFET transistors, as shown in Figure 2.1.1. Transistor M_1 is operating in the saturation or active mode, and so is M_2. In this setup, the output current I_{OUT} is directly related to $I_{REF.}$

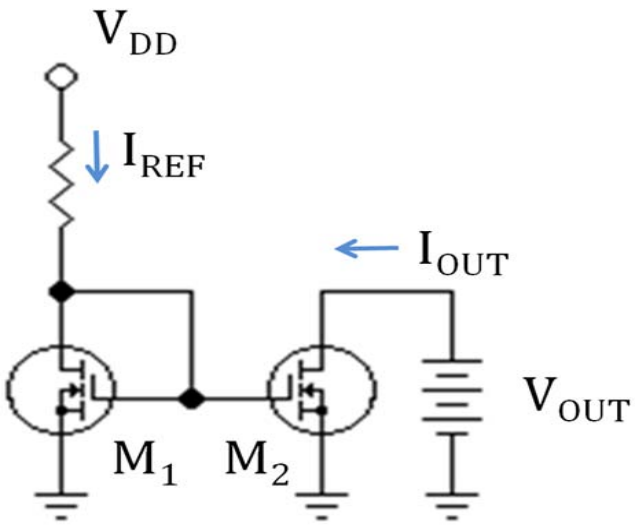


Fig.2.1. simple current mirror

The drain current of a MOSFET I_D is a function of both the gate-source voltage and the drain-to-gate voltage of the MOSFET given by $I_D = f(V_{GS}, V_{DG})$, a relationship derived from the functionality of the MOSFET device. In the case of transistor M_1 of the mirror, $I_D = I_{REF}$. Reference current I_{REF} is a known current, and can be provided by a resistor as shown, or by a "threshold-referenced" or "self-biased" current source to ensure that it is constant, independent of voltage supply variations. Using $V_{DG}=0$ for transistor M_1, the drain current in M_1 is $I_D = f(V_{GS},V_{DG}=0)$, so we find: $f(V_{GS}, 0) = I_{REF}$, implicitly determining the value of V_{GS}. Thus I_{REF}

sets the value of V_{GS}. The circuit in the diagram forces the same V_{GS} to apply to transistor M_2. If M_2 is also biased with zero V_{DG} and provided transistors M_1 and M_2 have good matching of their properties, such as channel length, width, threshold voltage etc., the relationship I_{OUT} = f (V_{GS},V_{DG}=0) applies, thus setting I_{OUT} = I_{REF}; that is, the output current is the same as the reference current when V_{DG}=0 for the output transistor, and both transistors are matched.

The drain-to-source voltage can be expressed as V_{DS}=V_{DG} +V_{GS}. With this substitution, the Shichman-Hodges model provides an approximate form for function f (V_{GS},V_{DG}):[2]

$$I_d = f\ (V_{GS}, V_{DG}) = \tfrac{1}{2}K_p\left(\tfrac{W}{L}\right)(V_{GS} - V_{th})^2(1 + \lambda V_{DS})$$
$$= \tfrac{1}{2}K_p\left(\tfrac{W}{L}\right)(V_{GS} - V_{th})^2\,(1 + \lambda(V_{DG} + V_{GS}))$$

where, K_p is a technology related constant associated with the transistor, W/L is the width to length ratio of the transistor, V_{GS} is the gate-source voltage, V_{th} is the threshold voltage, λ is the channel length modulation constant, and V_{DS} is the drain source voltage.

Output resistance:-

Because of channel-length modulation, the mirror has a finite output (or Norton) resistance given by the r_o of the output transistor, namely (see channel length modulation):

$$R_N = r_o = \frac{1/\lambda + V_{DS}}{I_D} = \frac{V_A + V_{DS}}{I_D},$$

where λ = channel-length modulation parameter and V_{DS} = drain-to-source bias.

The main sources of non- idealities in the current mirror characteristics include:-

- Channel length modulation
- Threshold voltage offset between input and output transistors.
- Imperfect geometrical matching.

2.2 Current Conveyor

A current conveyor is an abstraction for a three terminal analogue electronic device. It is a form of electronic amplifier with unity gain. There are three versions of generations of the idealized device, CCI, CCII and CCIII. When configured with other circuit elements, real current conveyors can perform many analogue signal processing functions, in a similar manner to the way op-amps and the ideal concept of the op-amp are used.

When Sedra and Smith first introduced the current conveyor in 1968, it was not clear what the benefits of the concept would be. The idea of the op-amp had been well known since the 1940s and integrated circuit manufacturers were better able to capitalize on this widespread knowledge within the electronics industry. Monolithic current conveyor implementations were not introduced and the op-amp became widely implemented. Since the early 2000s, implementations of the current conveyor concept, especially within larger VLSI projects such as mobile phones, have proved worthwhile.

Advantages

Current conveyors can provide better gain-bandwidth products than comparable op-amps, under both small and large signal conditions. In instrumentation amplifiers, their gain does not depend on the matching of pairs of external components, only on the absolute value of a single circuit element.

The first current conveyor (CCI)

The CCI is a three-terminal device with the terminals designated *X*, *Y*, and *Z*. The potential at *X* equals whatever voltage is applied to *Y*. Whatever current flows into *Y* also flows into *X*, and is mirrored at *Z* with a high output impedance, as a variable constant current source. In sub-type

CCI+, current into *Y* produces current into *Z*; in a CCI-, current into *Y* results in an equivalent current flowing *out* of *Z*.

Second generation current conveyor (CCII)

In a more versatile later design, no current flows through terminal *Y*. The ideal CCII can be seen as an ideal transistor, with perfected characteristics. No current flows into the gate or base which is represented by *Y*. There is no base-emitter or gate-source voltage drop, so the emitter or source voltage (at *X*) follows the voltage at *Y*. The gate or base has an infinite input impedance (*Y*), while the emitter or source has a zero input impedance (*X*). Any current out of the emitter or source (*X*) is reflected at the collector or drain (*Z*) as a current in, but with an infinite output impedance. Because of this reversal of sense between *X* and *Z* currents, this ideal bipolar or field-effect transistor represents a CCII. If current flowing out of *X* resulted in the same high-impedance current flowing *out* of *Z*, it would be a CCII+.

2.3 Current Comparator

An instrument for determining the ratio of two currents, based on Ampère's laws. The application of the current comparator, unlike the voltage ratio transformer, is not limited to alternating currents but can be used with direct currents as well.

The current comparator is based on Ampere's circuital law, which states that the integral of the magnetizing force around a closed path is equal to the sum of the currents which are linked with that path. Thus, if two currents are passed through a toroid by two windings of known numbers of turns, and the integral of the magnetizing force around the toroid is equal to zero, the current ratio is exactly equal to the inverse of the turns ratio. Widespread interest in "affordable-anywhere-anytime" wireless communication and computation has created a critical need for low power low voltage analog and digital integrated circuits. Not only do we want our system to run faster, but we also want them to run on little or no power. Comparators are the second most widely used current mode component after current mirrors. They have always been, and are still, an important building block in electronic system. A critical design aspect for comparator is good

tradeoff between sensitivity, speed and power consumption. Speed, in fact, can usually be increased at the expense of higher power consumption, while sensitivity requires high gain and hence low bias current, which leads to a slower time response.

For alternating-current comparators, the ampere-turn unbalance is given by the voltage at the terminals of a uniformly distributed detection winding on a magnetic core. Direct-current comparators use two magnetic cores which are modulated by alternating current in such a way that the dc ampere-turn unbalance is indicated by the presence of even harmonics in the voltage. Neither method is an exact measure of the integral of the magnetizing force, and various design features are added to overcome this deficiency. The most important of these are the magnetic shields, which are configured as hollow toroids. They protect the magnetic core and detection winding from the leakage fluxes of the current-carrying windings and ambient magnetic fields, and they are responsible for an improvement in accuracy of about three orders of magnitude. The copper shields supplement this action at higher frequencies and also provide mechanical protection for the magnetic steels.

Applications of the ac comparator include current and voltage transformer calibration, measurement of losses in large capacitors, inductive reactors and power transformers, resistance measurement, and the calibration of active and reactive power and energy meters. Further, the current comparator, like the current transformer, has the advantage of being applicable to measurements involving high-voltage, high-power circuits as well as being the basis for very accurate high-current-transconductance amplifiers. Figure 2.2 shows basic single input current comparator circuit.

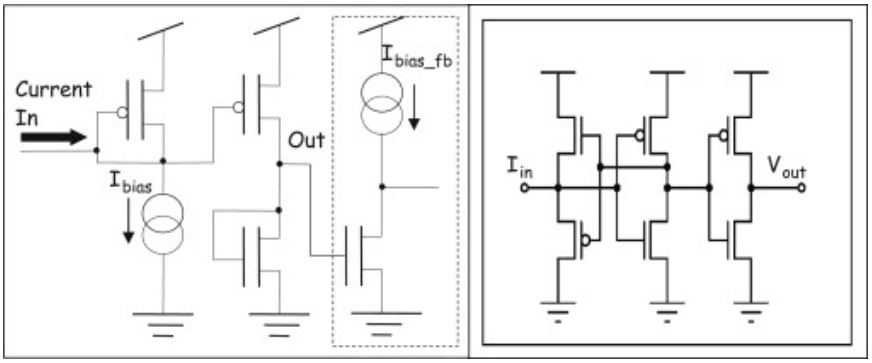


Fig. 2.2 single input current comparator circuit

The current comparator circuits are the basic building block in non linear analog signal processing circuits and A/D converter. Current mode circuits are widely used due to low power dissipation, large bandwidth, wide dynamic range and low voltage applications. The main function of current comparator circuit is to distinguish the two currents and provide the output either positive or negative in digital form. The ideal current comparator has zero delay, infinite transimpedance in transition region and zero offset. Many comparator circuits are designed each having its own operation applications. The simplest and high speed structure is presented by Traff in 1992. However some more power efficient, speedy structures are also presented at later stage. The simplest Traff's structure of current comparator is shown below in figure 2.3.

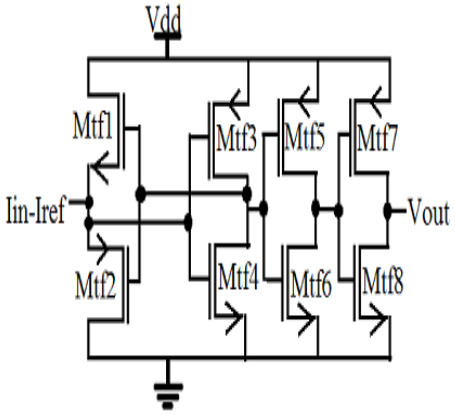


Fig.2.3.Traff comparator

2.4 Encoder

An encoder is a device, circuit, transducer, software program, algorithm or person that converts information from one format or code to another, for the purposes of standardization, speed, secrecy, security, or saving space by shrinking size. An encoder has 2^n input lines and only one of which is activated at a time and produces an n bit output code, depending on which input is activated. It is a combinational circuit. In normal encoder one of the input line is high and its corresponding binary is available at output. With general diagram of encoder as shown in figure

2.4, there are M inputs and N outputs. Encoders are used to convert codes to binary such as octal to binary, Hex to binary. The truth table for 4X2 encoder is shown below in Table 2.1.

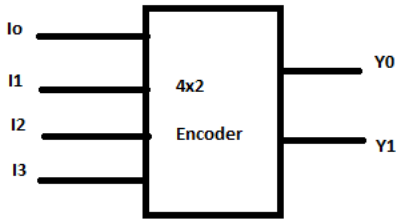


Fig. 2.4. 4X2 Encoder

2^n: n

Input output

I_0	I_1	I_2	I_3	Y_0	Y_1
1	0	0	0	0	0
0	1	0	0	0	1
0	0	1	0	1	0
0	0	0	1	1	1

Table 2.1. Truth table of 4X2 encoder

OUTPUTS:- $Y_0 = I_2+I_3$

$Y_1 = I_1+I_3$

CHAPTER 3:-

ADC's COMPARISION

What is ADC

An electronic integrated circuit which transforms a signal from analog (continuous) to digital (discrete) form. Analog signals are directly measurable quantities. Digital signals only have two states. For digital computer, we refer to binary states, 0 and 1.

Why ADC is needed

Microprocessors can only perform complex processing on digitized signals. When signals are in digital form they are less susceptible to the deleterious effects of additive noise. ADC Provides a link between the analog world of transducers and the digital world of signal processing and data handling.

ADC Process

2 steps:-

- Sampling and Holding (S/H)
- Quantizing and Encoding (Q/E)

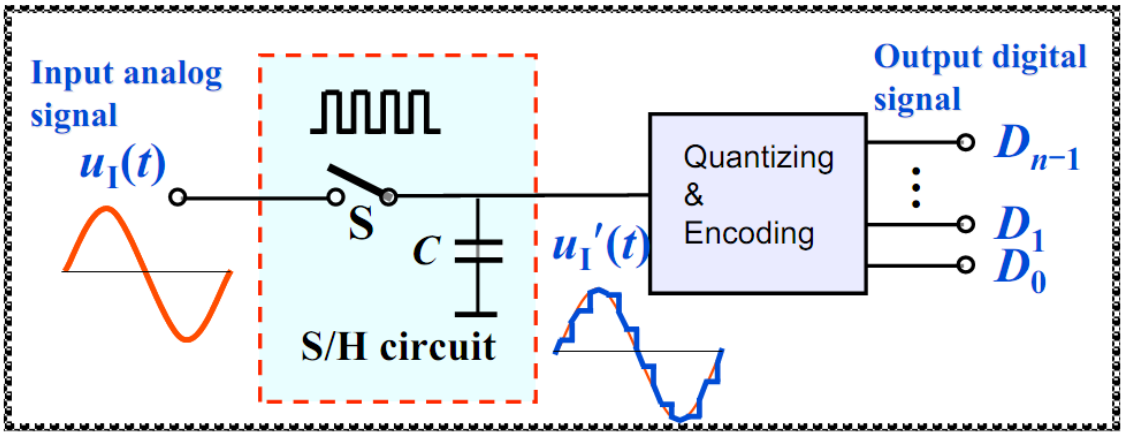


Fig 3.1 ADC process

Sampling And Holding

Holding signal benefits the accuracy of the A/D conversion.

Minimum sampling rate should be at least twice the highest data frequency of the analog signal.

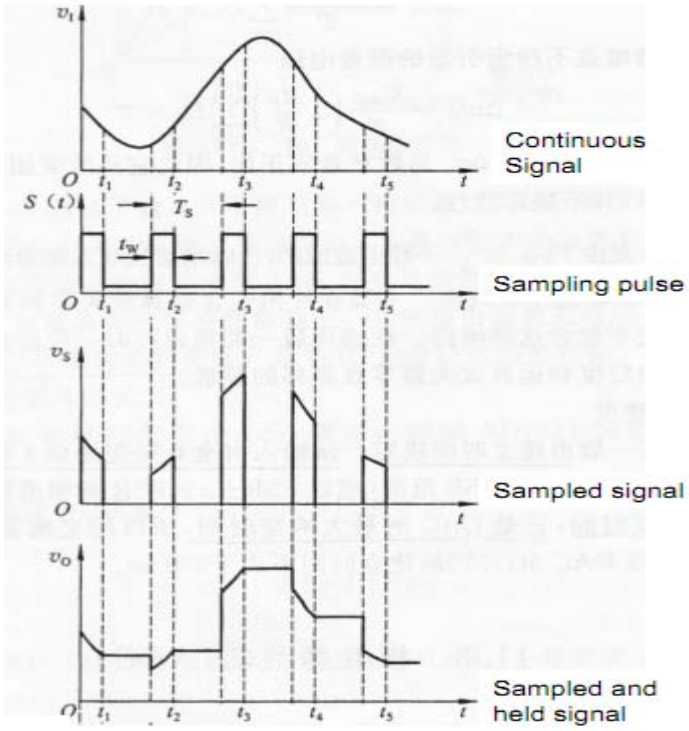


Fig 3.2 sampling and holding

Quantizing and Encoding

- **Resolution:**

  The smallest change in analog signal that will result in a change in the digital output.

$$\Delta V = \frac{V_r}{2^N}$$

  ΔV = Resolution

  V = Reference voltage range

  N = Number of bits in digital output.

  2^N= Number of states.

- **Quantizing:**

  Partitioning the reference signal range into a number of discrete quanta, then matching the input signal to the correct quantum.

- **Encoding:**

  Assigning a unique digital code to each quantum, then allocating the digital code to the input signal.

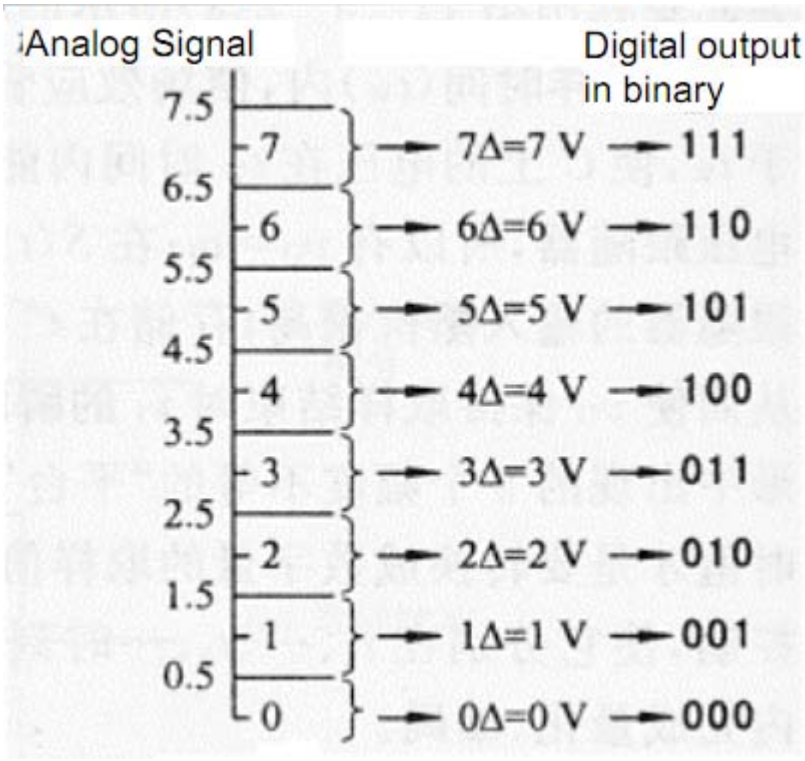


Fig 3.3 Quantizing and Encoding

An analog-to-digital converter (abbreviated ADC, A/D or A to D) is a device that converts the input continuous physical quantity to a digital number that represents the quantity's amplitude. The conversion involves quantization of the input, so it introduces a small amount of error. The inverse operation is performed by a digital-to-analog converter (DAC). Instead of doing a single conversion, an ADC often performs the conversions ("samples" the input) periodically. The result is a sequence of digital values that have converted a continuous-time and continuous-amplitude analog signal to a discrete-time and discrete-amplitude digital signal.

An ADC may also provide an isolated measurement such as an electronic device that converts an input analog voltage or current to a digital number proportional to the magnitude of the voltage or current. However, some non-electronic or only partially electronic devices, such as rotary encoders, can also be considered ADCs.

Resolution

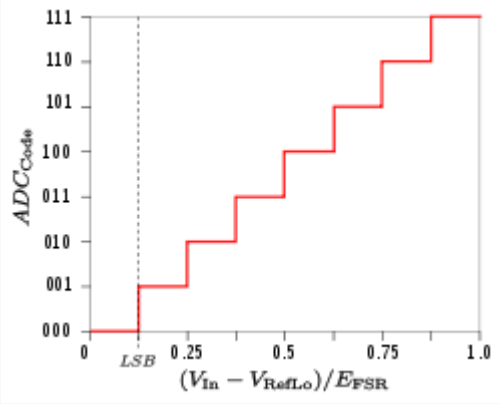


Fig. 3.4. An 8-level ADC coding scheme.

The resolution of the converter indicates the number of discrete values it can produce over the range of analog values. The values are usually stored electronically in binary form, so the resolution is usually expressed in bits. In consequence, the number of discrete values available, or "levels", is a power of two. For example, an ADC with a resolution of 8 bits can encode an analog input to one in 256 different levels, since $2^8 = 256$. The values can represent the ranges from 0 to 255 (i.e. unsigned integer) or from −128 to 127 (i.e. signed integer), depending on the application.

Resolution can also be defined electrically, and expressed in volts. The minimum change in voltage required to guarantee a change in the output code level is called the least significant bit (LSB) voltage. The resolution Q of the ADC is equal to the LSB voltage. The voltage resolution of an ADC is equal to its overall voltage measurement range divided by the number of discrete values:

$$Q = \frac{E_{\text{FSR}}}{2^M - 1},$$

where M is the ADC's resolution in bits and E_{FSR} is the full scale voltage range (also called 'span').

E_{FSR} is given by

$$E_{\mathrm{FSR}} = V_{\mathrm{RefHi}} - V_{\mathrm{RefLow}},$$

where V_{RefHi} and V_{RefLow} are the upper and lower extremes, respectively, of the voltages that can be coded.

Normally, the number of voltage intervals is given by

$$N = 2^M - 1,$$

where M is the ADC's resolution in bits. That is, one voltage interval is assigned in between two consecutive code levels.

In practice, the useful resolution of a converter is limited by the best signal-to-noise ratio (SNR) that can be achieved for a digitized signal. An ADC can resolve a signal to only a certain number of bits of resolution, called the effective number of bits (ENOB). One effective bit of resolution changes the signal-to-noise ratio of the digitized signal by 6 dB, if the resolution is limited by the ADC. If a preamplifier has been used prior to A/D conversion, the noise introduced by the amplifier can be an important contributing factor towards the overall SNR.

➢ Response type

Most ADCs are linear types. The term *linear* implies that the range of input values has a linear relationship with the output value.

Some early converters had a *logarithmic* response to directly implement A-law or μ-law coding. These encodings are now achieved by using a higher-resolution linear ADC (e.g. 12 or 16 bits) and mapping its output to the 8-bit coded values.

➢ Accuracy

An ADC has several sources of errors. Quantization error and (assuming the ADC is intended to be linear) non-linearity are intrinsic to any analog-to-digital conversion. There is also a so-called *aperture error* which is due to a clock jitter and is revealed when digitizing a time-variant signal (not a constant value).

These errors are measured in a unit called the least significant bit (LSB). In the above example of an eight-bit ADC, an error of one LSB is 1/256 of the full signal range, or about 0.4%.

➢ Quantization error

Quantization error (or quantization noise) is the difference between the original signal and the digitized signal. Hence, the magnitude of the quantization error at the sampling instant is between zero and half of one LSB. Quantization error is due to the finite resolution of the digital representation of the signal, and is an unavoidable imperfection in all types of ADCs.

➢ Non-linearity

All ADCs suffer from non-linearity errors caused by their physical imperfections, causing their output to deviate from a linear function (or some other function, in the case of a deliberately non-linear ADC) of their input. These errors can sometimes be mitigated by calibration, or prevented by testing.

Important parameters for linearity are integral non-linearity (INL) and differential non-linearity (DNL). These non-linearities reduce the dynamic range of the signals that can be digitized by the ADC, also reducing the effective resolution of the ADC.

➢ Aperture error

Imagine digitizing a sine wave $x(t) = A\sin(2\pi f_0 t)$. Provided that the actual sampling time *uncertainty* due to the *clock jitter* is Δt, the error caused by this phenomenon can be estimated as $E_{ap} \leq |x'(t)\Delta t| \leq 2A\pi f_0 \Delta t$.

The error is zero for DC, small at low frequencies, but significant when high frequencies have high amplitudes. This effect can be ignored if it is drowned out by the *quantizing*

error. Jitter requirements can be calculated using the following formula: $\Delta t < \frac{1}{2^q \pi f_0}$, where q is the number of ADC bits.

Types of A/D Converters

1. **Dual slope A/D Converter**
2. **Successive approximation A/D Converter**
3. **Flash A/D Converter**
4. **Delta-Sigma A/D Converter**

➢ Dual Slope A/D Converter

Fundamental components:-

1. Integrator
2. Electronically Controlled Switches
3. Counter
4. Clock
5. Control Logic
6. Comparator

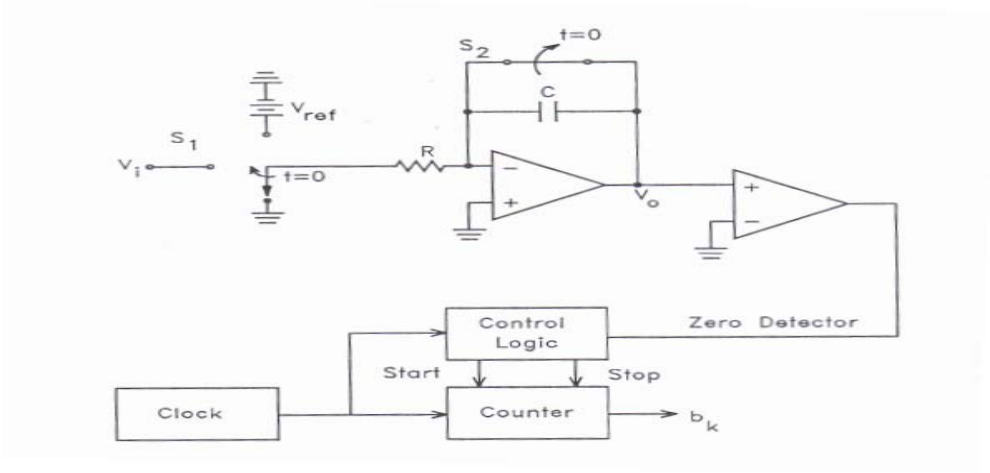


Fig 3.5 Dual slope A/D converter

A dual-slope ADC (DS-ADC) integrates an unknown input voltage (VIN) for a fixed amount of time (TINT), then "de-integrates" (TDEINT) using a known reference voltage (VREF) for a variable amount of time.

The key advantage of this architecture over the single-slope is that the final conversion result is insensitive to errors in the component values. That is, any error introduced by a component value during the integrate cycle will be cancelled out during the de-integrate phase.

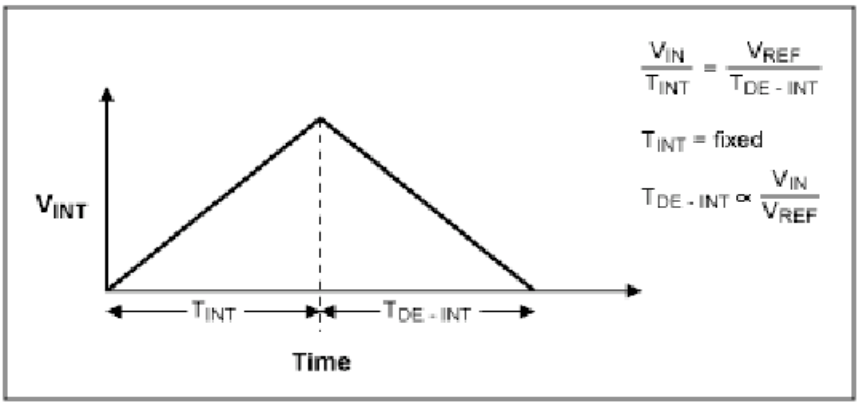


Fig 3.6 Integration and De integration of V_{in}

At t<0, S1 is set to ground, S2 is closed, and counter=0. At t=0 a conversion begins and S2 is open, and S1 is set so the input to the integrator is Vin. S1 is held for TINT which is a constant

predetermined time interval. When S1 is set the counter begins to count clock pulses, the counter resets to zero after TINT Vout of integrator at t=TINT is VINTINT/RC is linearly proportional to VIN. At t=TINT S1 is set so -Vref is the input to the integrator which has the voltage VINTINT/RC stored in it. The integrator voltage then drops linearly with a slope -Vref/RC. A compartor is used to determine when the output voltage of the integrator crosses zero. When it is zero the digitized output value is the state of the counter.

PROS:-

1. Conversion result is insensitive to errors in the component values.
2. Fewer adverse affects from “noise”.
3. High Accuracy.

CONS:-

1. Slow
2. Accuracy is dependent on the use of precision external components.
3. Cost

➢ Flash A/D Converter

Fundamental Components (For N bit Flash A/D)

1. 2N-1 Comparators
2. 2N Resistors
3. Control Logic

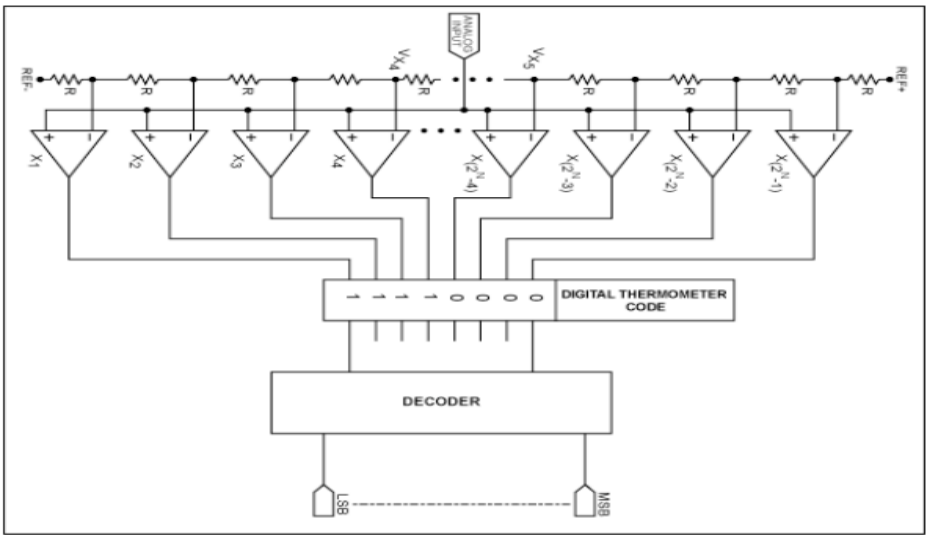


Fig 3.7 Flash ADC

Uses the 2N resistors to form a ladder voltage divider, which divides the reference voltage into 2N equal intervals. Uses the 2N-1 comparators to determine in which of these 2N voltage intervals the input voltage Vin lies. The Combinational logic then translates the information provided by the output of the comparators. This ADC does not require a clock so the conversion time is essentially set by the settling time of the comparators and the propagation time of the combinational logic.

PROS:-

1. Very Fast (Fastest)
2. Very simple operational theory
3. Speed is only limited by gate and comparator propagation delay

CONS:-

1. Expensive
2. Prone to produce glitches in the output.

3. Each additional bit of resolution requires twice the Comparator.

➢ SIGMA-DELTA A/D Converter

Main Components:-

1. Resistors
2. Capacitor
3. Comparators
4. Control Logic
5. DAC

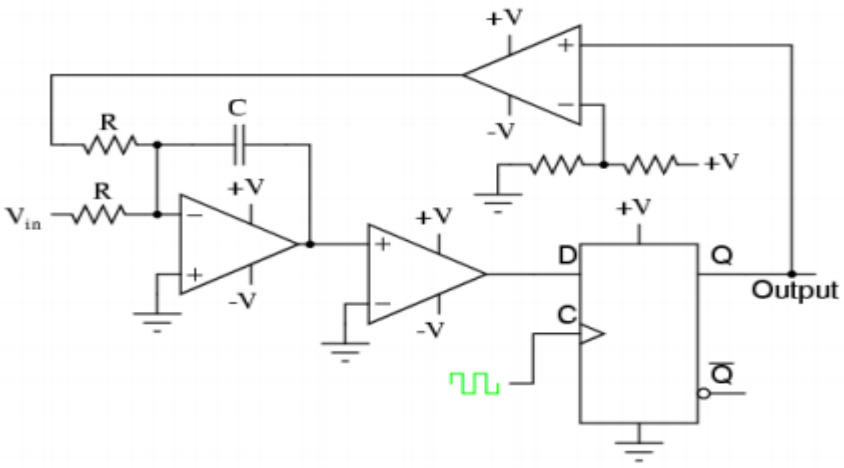


Fig 3.8 Sigma- Delta A/D converter

Input is over sampled, and goes to integrator. The integration is then compared to ground. Iterates and produces a serial bit stream. Output is a serial bit stream with # of 1's proportional to Vin.

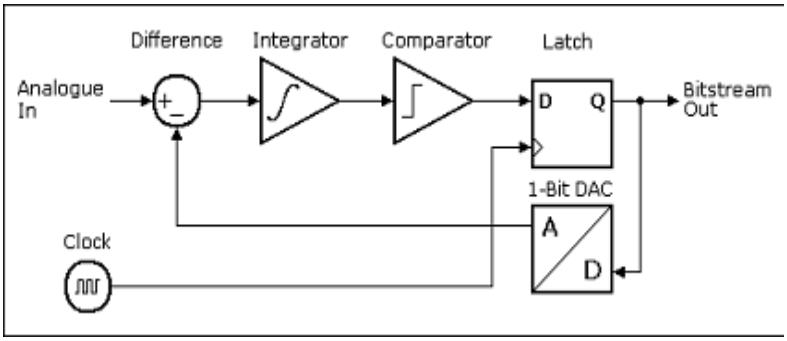


Fig 3.9 Process flow of Sigma Delta A/D converter

PROS:-

1. High Resolution
2. No need for precision components

With this arrangement the sigma-delta modulator automatically adjusts its output to ensure that the average error at the quantizer output is zero. The integrator value is the sum of all past values of the error, so whenever there is a non-zero error value the integrator value just keeps building until the error is once again forced to zero.

CONS:-

1. Slow due to over sampling
2. Only good for low bandwidth

➢ Successive Approximation ADC Circuit

- Uses a n-bit DAC to compare DAC and original analog results.
- Uses Successive Approximation Register (SAR) supplies an approximate digital code to DAC of Vin.
- Comparison changes digital output to bring it closer to the input value.
- Uses Closed-Loop Feedback Conversion.

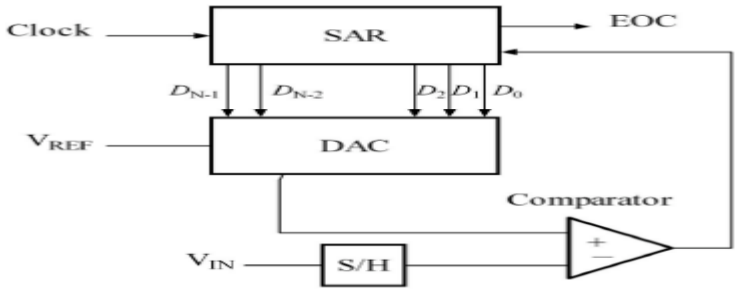


Fig 3.10 Successive Approximation A/D converter

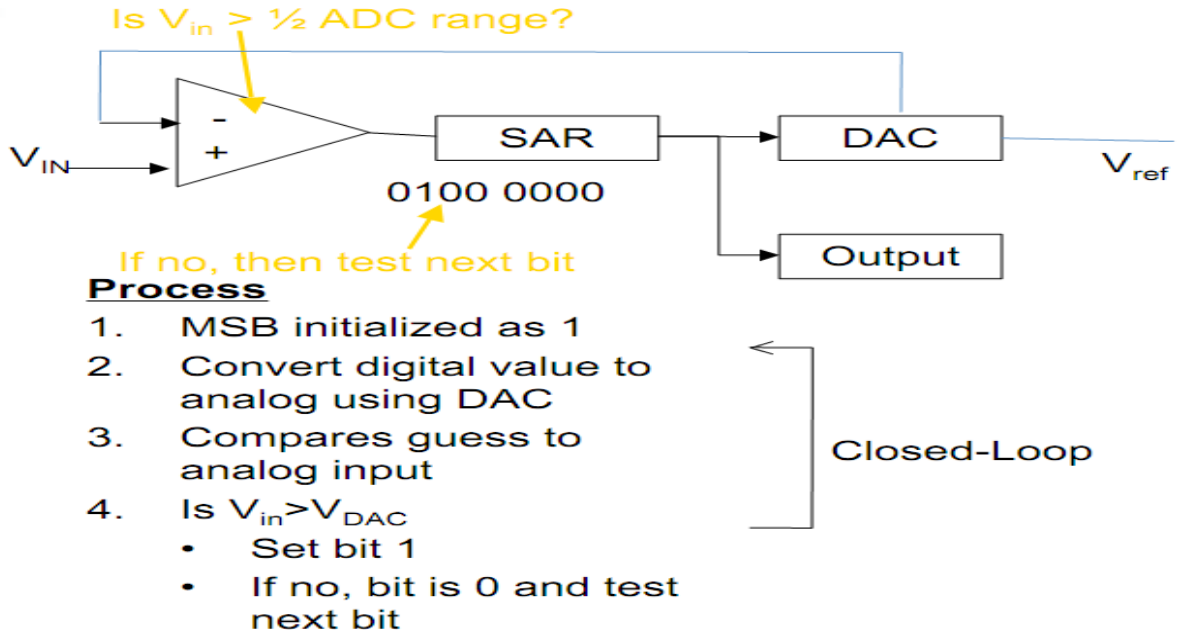


Fig 3.11 Process flow of Successive Approximation ADC

PROS:-

1. Capable of high speed and reliable
2. Medium accuracy compared to other ADC types
3. Good tradeoff between speed and cost
4. Capable of outputting the binary number in serial (one bit at a time) format

CONS:-

1. Higher resolution successive approximation ADC's will be slower
2. Speed limited to ~5Msps

Output

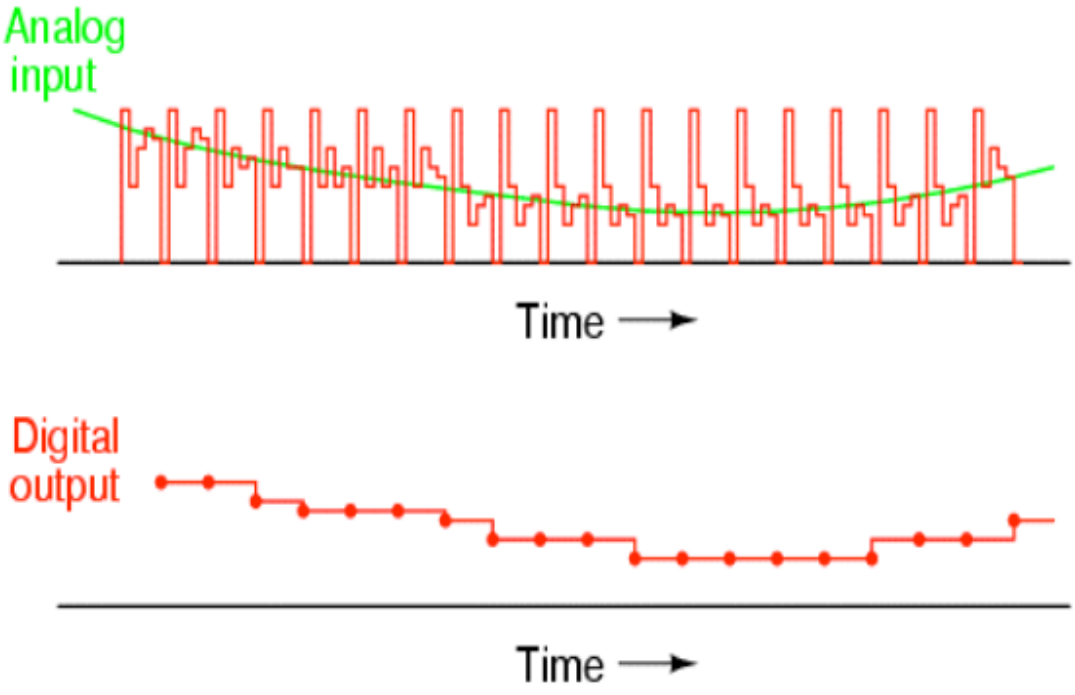


Fig 3.12 Analog to Digital Conversion

ADC Types Comparison

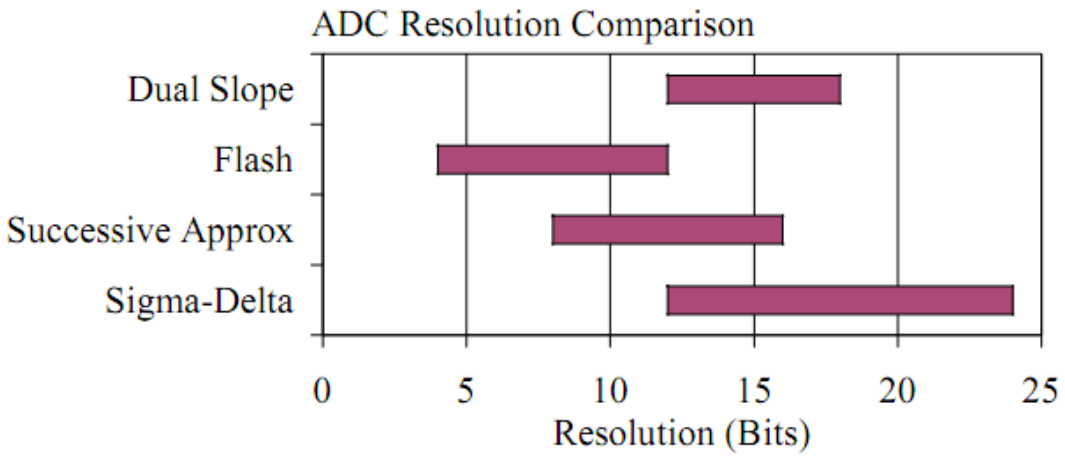


Fig 3.13 Different ADC's Resolution Comparison

Type	Speed (relative)	Cost (relative)
Dual Slope	Slow	Med
Flash	Very Fast	High
Successive Appox	Medium – Fast	Low
Sigma-Delta	Slow	Low

Table 3.1 comparison of ADC's on basis of speed and cost

Pipelined ADC

The pipelined analog-to-digital converter (ADC) has become the most popular ADC architecture for sampling rates from a few megasamples per second (Msps) up to 100Msps+. Resolutions range from eight bits at the faster sample rates up to 16 bits at the lower rates. These resolutions and sampling rates cover a wide range of applications, including CCD imaging, ultrasonic medical imaging, digital receivers, base stations, digital video (for example, HDTV), xDSL, cable modems,fast Ethernet.

Applications with lower sampling rates are still the domain of the successive approximation register (SAR) and integrating architectures, and more recently, oversampling/sigma-delta ADCs. The highest sampling rates (a few hundred Msps or higher) are still obtained using flash ADCs. Nonetheless, pipelined ADCs of various forms have improved greatly in speed, resolution, dynamic performance, and low power in recent years.

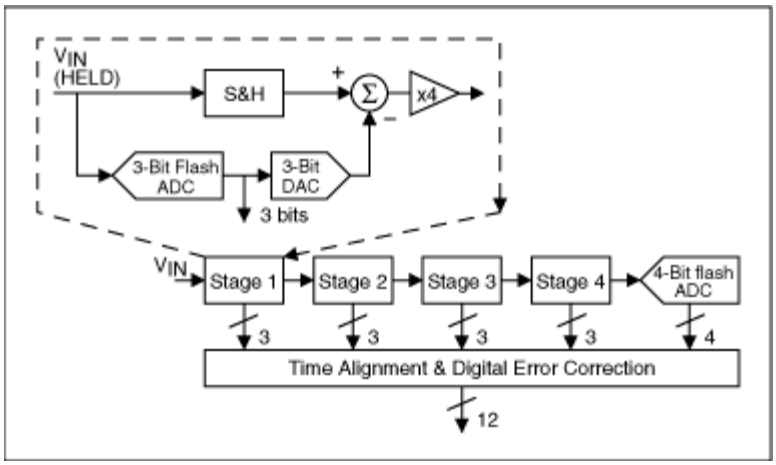


Fig 3.14 Pipelined ADC

When all the building blocks are clubbed together we can get the whole pipelined Analog-Digital Converter. The block diagram of the pipelined Analog-Digital converter is shown in figure 2 so when all the building blocks are connected together then we get a 10 bit 15 MSPS pipelined Analog-Digital converter.

The input goes to the track and hold circuit which samples the input at CLK1 and then holds the value for the rest of the clock cycle. At CLK2, the comparator becomes operational and makes a decision based on the input that it gets from the track and hold circuit. At CLK3 the residue amplifier gets the input and makes the decision by CLK5. The flip flops store the output of the comparator at CLK3 till the next clock cycle. The clocks are shown in figure 39. A voltage buffer is placed between each multiplying DAC so as to reduce the load seen by the previous stage and hence properly propagate the residue generated in each stage. If the residue generated is not correct then the decision made by the comparator would also be a wrong one. An error in residue at an initial stage would make it propagate through the further stages multiplying the error by 2 each time.

CHAPTER 4:-

PROPOSED ADC STRUCTURE

The Flash ADC requires two currents at the input, one being the input current (I_{in}) to be digitized and other being a set of references (I_{ref}), one each for the current comparators, to be compared with the input current. For a 2-bit Flash ADC, 2^2-1=3 current comparators are required and hence 3 reference currents need to be generated. The values of reference currents are computed as follows:

If input current, I_{in}, is in the range (I_1-I_2), then a step Δ is calculated as-

$$\Delta = \frac{(I2 - I1)}{2^n - 1}$$

Then, reference currents are computed as

$$Irefi = \Delta . i \qquad (1)$$

(where i=1,2,…..2^n-1).

Each of the current comparator compares Iin with a designated value of Iref, as computed in (1) and produces an output 0 or 1 based on the magnitude of I_{in}-I_{refi}. This constitutes a code called thermometer code. In the next step, this thermometer code is converted into the corresponding binary code using a suitably sized Thermometer to binary encoder. The generalized ADC structure is shown in figure 4.1.

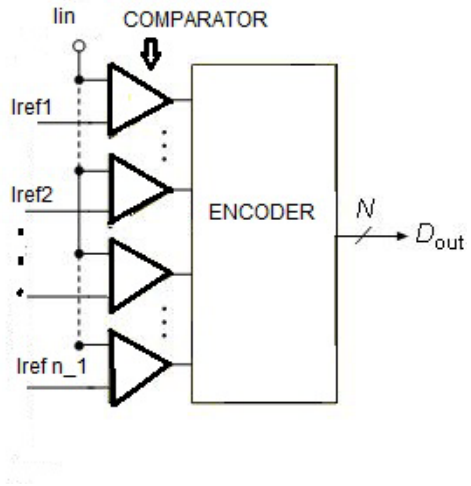


Fig. 4.1 Generalized ADC structure

The architecture of proposed ADC, as shown in figure 4.2, consists of three sections, as stated above. The 1st section consists of the combination of current mirror circuit that provides differenced output current to produce the input signal at three stages. This structure is based on the difference between input current (I_{IN}) and the reference current (I_{ref}).The output current of this stage is fed to input of comparator circuit. The comparator circuit compares the input current with internal current to produce the output voltage. The output of the comparator circuit is transferred to the encoder circuit to produce the digital output that is desired. Each part is discussed below separately:-

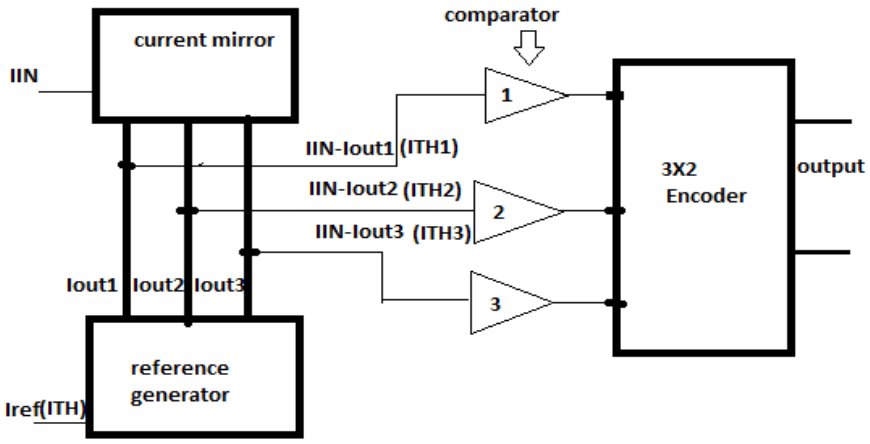


Fig. 4.2. Proposed Flash ADC module

A. Mirror circuit:-

Current mirror circuit is the combination of P channel and N channel MOSFETS, for providing constant currents at output that are summed up in the analogue fashion, trio circuit in which input current (I_{IN}) is applied to drain of transistor M1 that is copied to M2 transistor. There is combination of transistors M4 and M5 to provide DC reference current that is copied to M3 transistor to give I_{TH} that is compared with I_{IN}. Based on I_{IN} and I_{TH} comparison transistor operating region are decided.

If $I_{IN} < I_{TH}$

V_{DS} to be LOW(0), when threshold current is exceeded.

We have to force V_{DS} to low so that gate will be turn off. Aspect ratio of transistor plays important role here.

As the input current I_{in} is to be compared with I_{ref} by each of the current comparators, it is required to generate replicas of I_{in} and progressively increasing values of I_{ref} as per (1). This is achieved by employing current mirrors. The basic current mirror circuit consists of two matched back to back MOS Transistors, such that they have same gate to source voltage, shown in figure 4.3. Transistor Mn1 is enhancement type MOS. As $V_{gs1}=V_{gs2}$ and $V_{gd}=0$, the transistor Mn1 in saturation mode. The drain of Mn2 is connected to load circuit. The load circuit typically involves more additional stages of MOSFETs. When the transistor Mn2 is in saturation the circuit will act as current mirror (DC current source). The current I always goes into Mn2 transistor, such that the circuit act as sink circuit.

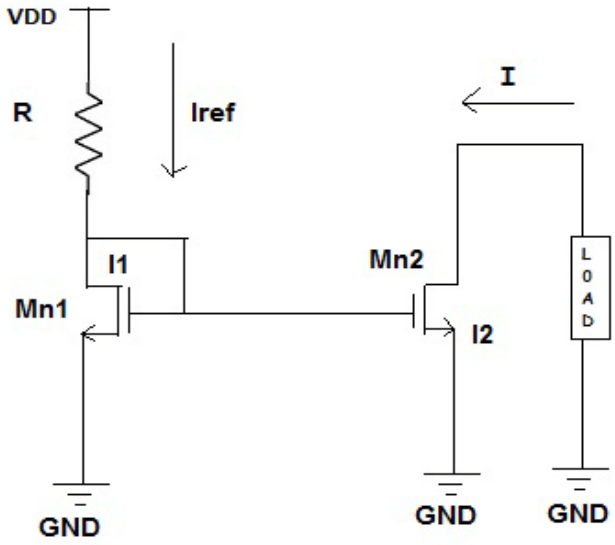


Fig. 4.3. Current mirror circuit

Our implementation of 2-bit ADC requires Iin and three values of Iref to be compared to Iin. This is achieved with the help of a current mirror trio circuit as shown in Fig. 4.4. In this circuit input current (I_{IN}) is applied to drain of transistor Mn1 that is copied to Mn2 transistor. There is combination of transistors Mp1 and Mn5 to provide DC reference current that is copied to Mp2 transistor that is compared with I_{IN}.

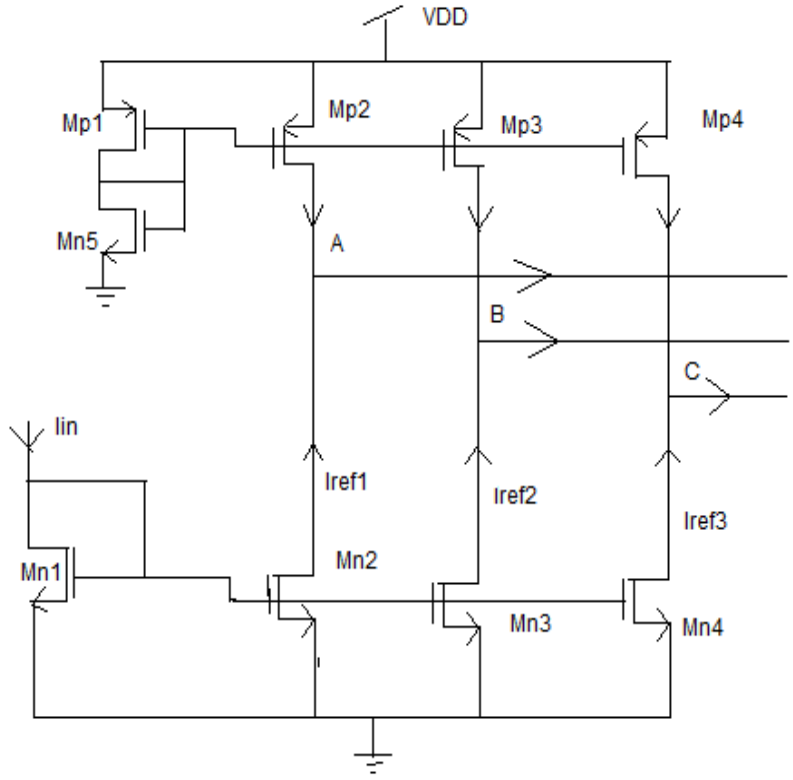


Fig. 4.4. Trio circuit for current mirror

We have to force V_{DS} to low so that gate will be turn off. Aspect ratio of transistor plays important role here. By varying the aspect ratios of transistors of Mp2, Mp3, Mp4 different ratio of reference current (I_{ref}) can be obtained that is provided by the NMOS transistors.

B. Current Comparator

The current comparison is based on circuital laws, which state that the integral of the magnetizing force around a closed path is equal to the sum of the currents which are linked with that path. There should be low input impedance, low power dissipation and short propagation delay for efficient structure design. The current comparator circuits are the basic building block in non linear analog signal processing circuits and A/D converter. The main function of current

comparator circuit is to distinguish the two currents and provide the output either positive or negative in digital form. The ideal current comparator has zero delay, infinite transimpedance in transition region and zero offset. Many comparator circuits are designed each having its own operation applications. However, there is still scope for improved and more efficient structures satisfying the basic performance criteria expected out of a current comparator.

We have employed a CCII (current conveyor) based current comparator. A current conveyor is a three terminal analogue electronic device which can perform many analogue signal processing functions, in a similar manner to the way op-amps. There are many current conveyor structures are implemented, the basic structure has three nodes X,Y,Z. the input is applied to Y terminal, the same is appear at X terminal, infinite input impedance at Y terminal, with no current flows into y terminal, the voltage that is appeared at X terminal is copied to Z terminal. There will be voltage follower at Y terminal and current follower at Z terminal. The ideal structure of current conveyor (CCII) is shown below in figure 4.5.

$$I_Y = I_X ;$$
$$V_X = V_Y$$
$$I_Z = +/- I_X$$

Ideally at X terminal input impedance should be low (0), and at Y and Z terminal it should be infinite, for non ideal circuit it has current gain($\alpha(s)$) and voltage gain ($\beta(s)$).

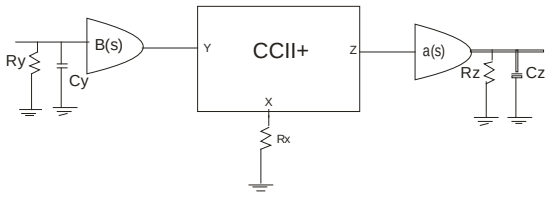


Fig. 4.5. Practical current conveyor circuit (CCII)

Matrix representation of same is given below. The modular diagram of CCII based comparator is shown below, figure 4.6.

$$\begin{pmatrix} I_x \\ V_X \\ I_Z \end{pmatrix} = \begin{pmatrix} 1/(R_Y//C_Y) & 0 & 0 \\ \beta(s) & R_X & 0 \\ 0 & +/-\alpha(s) & 1/(R_Z//C_Z) \end{pmatrix} \begin{pmatrix} V_Y \\ I_X \\ V_Z \end{pmatrix}$$

Matrix for CCII module

Current mode circuits have used quite regularly due to their wide dynamic range, low voltage operation, wide bandwidth and low power dissipation properties. Comparator is an important part of many analog integrated circuits. Current comparators are used broadly in high data conversion especially in analog to digital converter (ADC). Traff proposed the first current mode comparator. The design is based on the combination of two inverters with positive feedback. Compared with voltage mode comparators the most important drawback of this comparator is the response time of the circuit which restricts the input frequency range. Since then, many new design ideas have been developed in order to improve the above shortcoming as well as other properties such as power consumption, offset consideration and wider input dynamic range.

Palmisano and Palumbo have utilized an offset compensation circuit in order to reduce the offset current due to process mismatch. The application of compensation capacitors that are employed in the circuit deteriorate the switching time of the comparator. Cembrano et al. used a nonlinear negative feedback method to achieve high-speed for low current and high accuracy. Others have exploited different circuit ideas such as resistive feedback network, negative feedback structure and emphasis on a larger loop-gain. Banks and Toumazou reported a power efficient comparator where, advanced positive feedback network is used to improve the circuit characteristics. A lack of comparable time response with respect to the voltage mode comparators is observed in all the previous treatment of the current mode comparator circuits.

As shown in Fig, CCII is used as the input stage of the proposed new current comparator due to the low input impedance at node X and the inherent current to voltage conversion property of the CCII circuit. A wide number of CCII topologies in different classes such as A, B or AB are implemented in CMOS technology In realization of CCIIs, designers exploit different techniques to reach the unity value for a and b, the voltage and current gain, respectively. Current mirror and differentials pair through a feedback connection are used broadly in recent CCIIs. The

requirement of low impedance terminal at node X and due to the obvious advantages of differential pair, this configuration of CCII is used. The need for ‘‘rail-to-rail’’ current conveyor makes it easier to select one topology that link two differential pair in parallel. Fig. shows the complete current comparator (CC-CCII) circuit schematic. It is obvious that transistors M9, M11, and M10, M12 have the same transconductance as referenced in paper presented by R. Chavoshisani, O. Hashemipour, “A High speed current coveyor based current comparator”, in: Microelectronics Journals at ELSEVIER(2010).

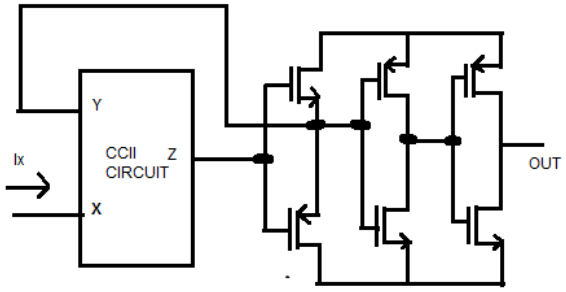


Fig. 4.6. CCII based Current Comparator

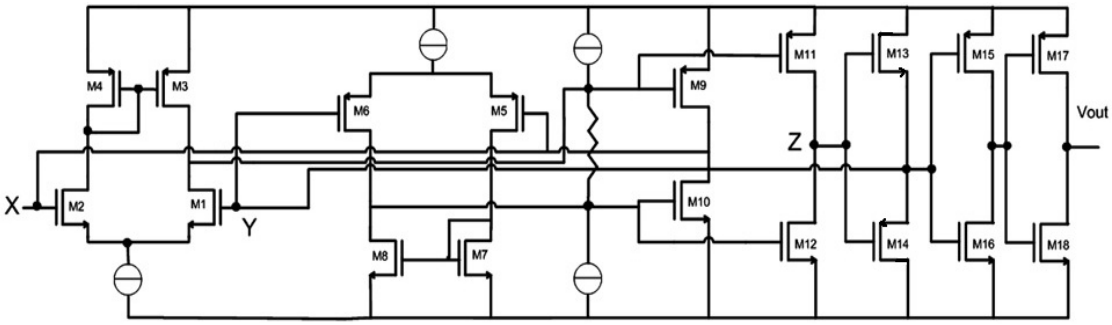


Fig 4.7 single input current comparator

C. Encoder

The results of current comparison need to be encoded to produce the binary code at the output. A basic encoder has 2^n input lines and only one of which is activated at a time and

produces an n bit output code, depending on which input is activated. With general diagram of encoder as shown in figure 4.7, there are M inputs and N outputs. For our 2-bit ADC, there are 3 comparators whose outputs are to be encoded to produce a 2-bit binary output. Hence, we employ a simple 3X2 CMOS encoder. The truth table for this encoder is shown below in Table 4.1. The MOS circuit is given below in figure 4.8, having 12 transistors, however the circuit is also designed using Pass Transistor Logic.

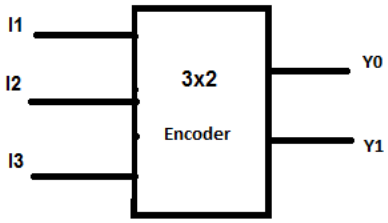


Fig. 4.8. 3X2 Encoder

I_0	I_1	I_2	I_3	Y_0	Y_1
0	1	0	0	0	1
0	0	1	0	1	0
0	0	0	1	1	1

Table 4.1. Truth table of 3X2 encoder

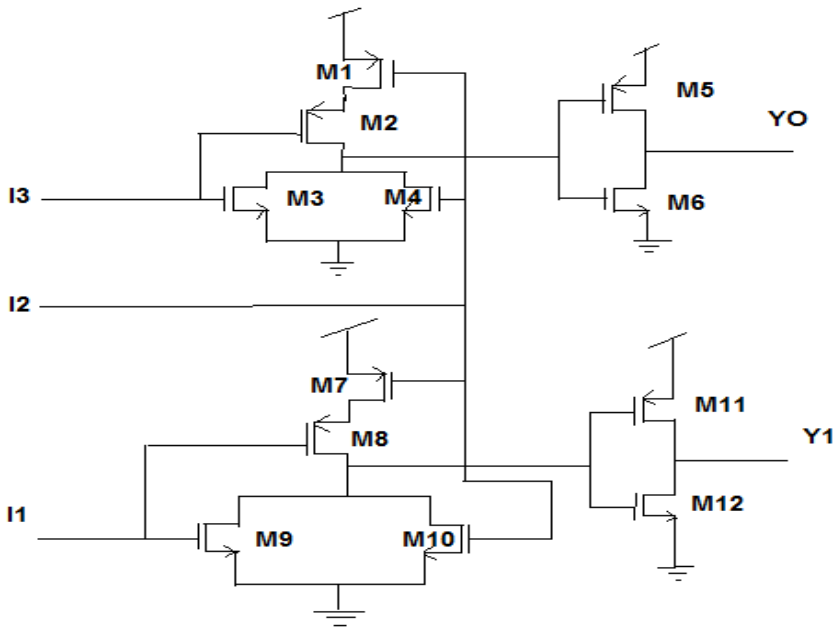


Fig. 4.9. Encoder (MOS Design)

OUTPUTS:- $Y_0 = I_2+I_3$

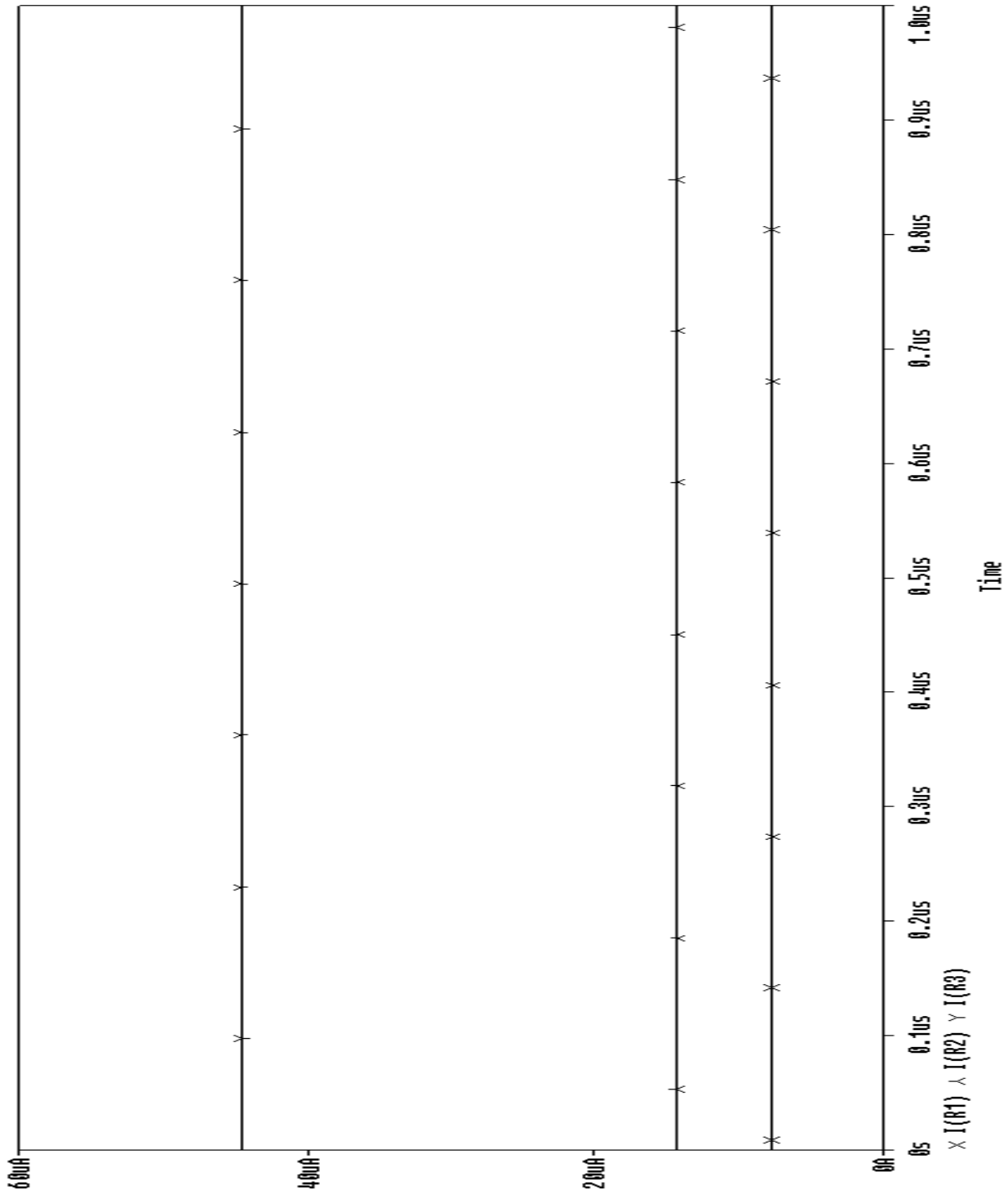
$Y_1 = I_1+I_3$

CHAPTER 5:- SIMULATION

The structure of proposed flash ADC shown in figure 4.2 (basic modular structure of Flash ADC) comprises of figure 4.4 (current mirror), 4.7 (CCII based current comparator) and 4.8(encoder) has been simulated. The proposed Flash ADC's components are simulated using Pspice simulator for 0.18µm technology and 1.8V supply voltage.

The output simulation results are shown in proceeding pages. The output for current mirror circuit is carried out to get the three different input sequences as discussed in previous chapter. The mirror circuit provides the different output values of current based on the different W/L ratios that is subtraction of I_{in}-I_{ref}, for providing an input signal for comparator. The range of comparator is 20uA, which means the comparator is active high after 20uA. Hence the input to the comparator that is generated by current mirror circuit is such that current up to 20uA is treated as logic 0 and above 20uA as logic 1. The output from comparator circuit provides two levels 0 and 1.8V treated as logic 0 and logic 1 as shown in simulation results. The output from comparator circuit is fed to the Encoder to provide the output result based on the input signal. The comparator circuit provides the low power consumption and low power supply in comparison to previous comparator circuits. The propagation delay of the comparator circuit reduced to 0.5ns in comparison to Traff comparator circuit's and Tang comparator circuit's 10 and 11 nsec respectively. The power consumption is also reduced from previous comparator circuits. The output shows the good response for all circuits to provide the low power circuit designing constraint.

The circuit of encode is simulated for three cases, ignoring the case in which we get both outputs as 0 logic as stated in CHAPTER 4, also shows satisfactory response.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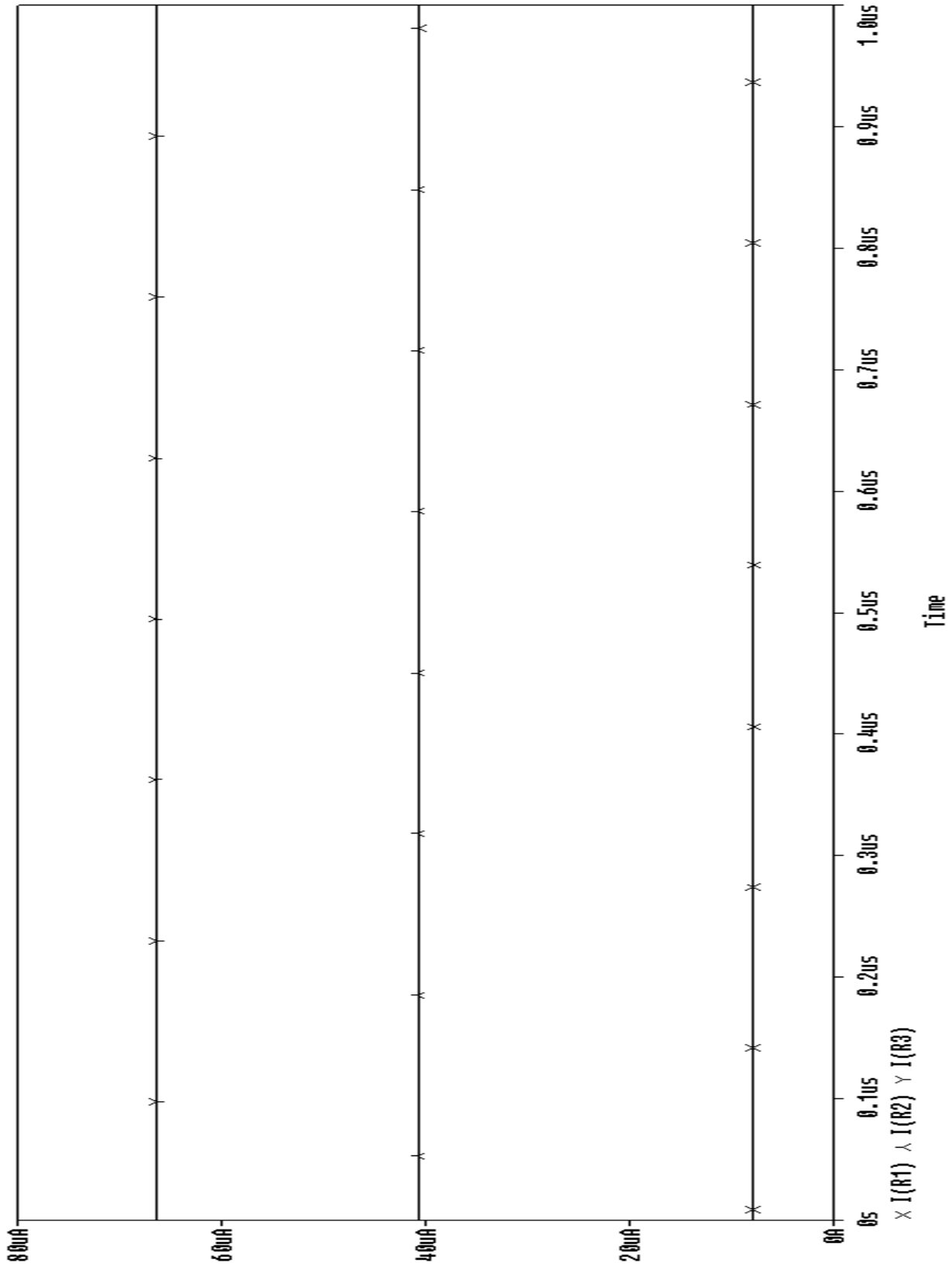
40uA
20uA
0A
0s
0.1us
0.2us
0.3us
0.4us
0.5us
0.6us
0.7us
0.8us
0.9us
1.0us
Time
I(R1)
I(R2)
I(R3)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60uA
40uA
20uA
0A
0s
0.1us
0.2us
0.3us
0.4us
0.5us
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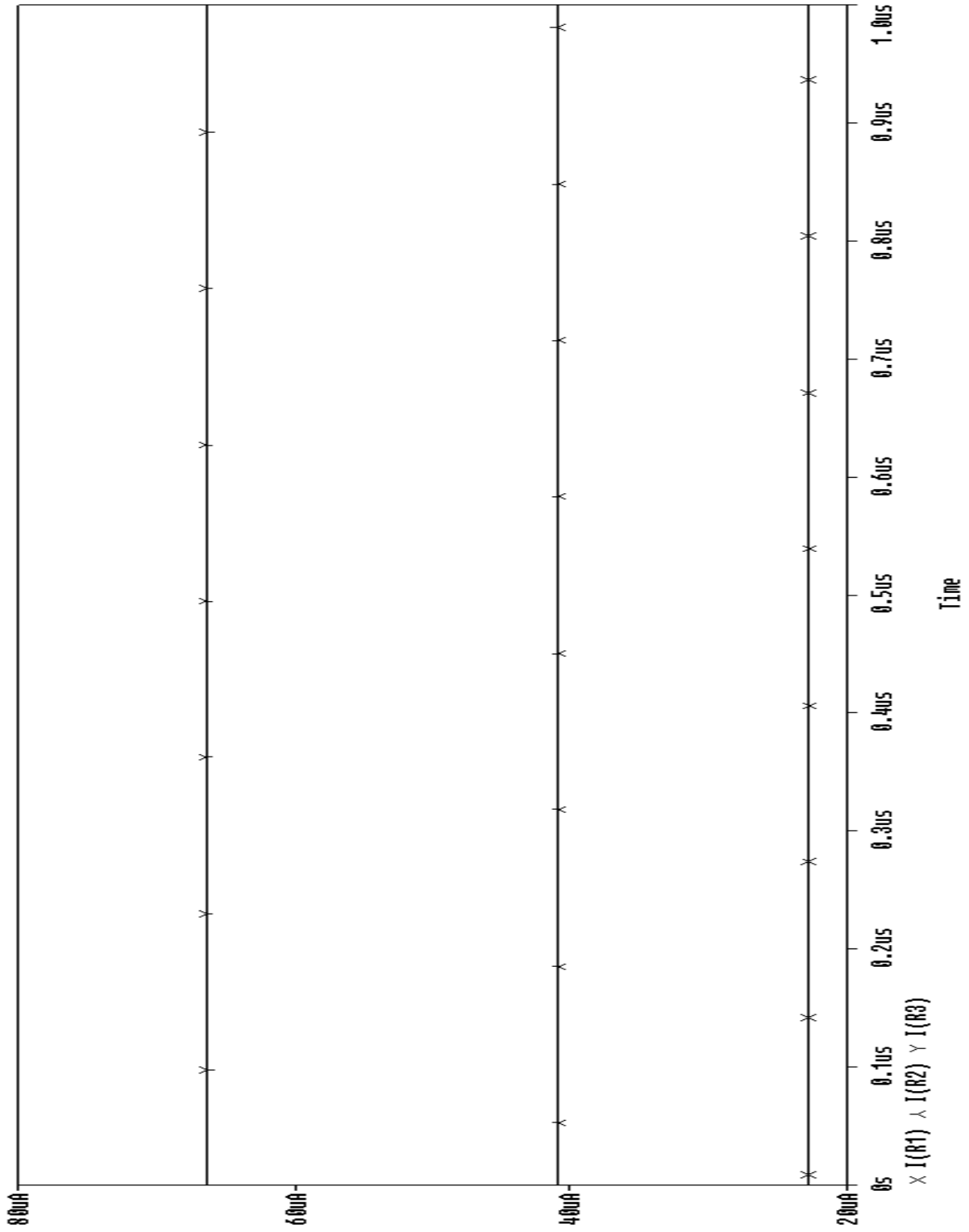
0.7us
0.8us
0.9us
1.0us
Time
I(R1)
I(R2)
I(R3)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60uA
40uA
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0s
0.1us
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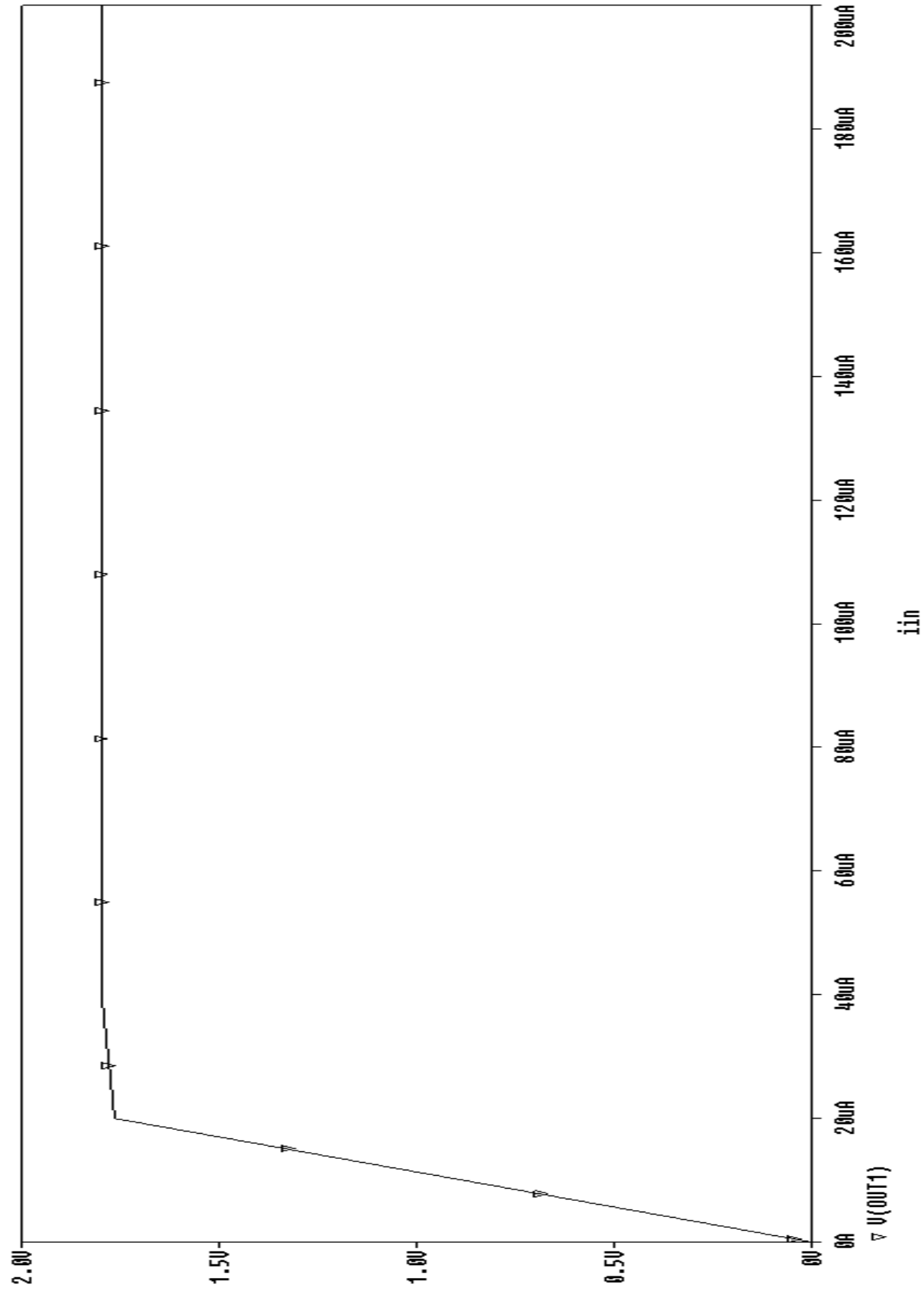
0.7us
0.8us
0.9us
1.0us
Time
I(R1)
I(R2)
I(R3)


2.0V
1.5V
1.0V
0.5V
0V
0A
20uA
40uA
60uA
80uA
100uA
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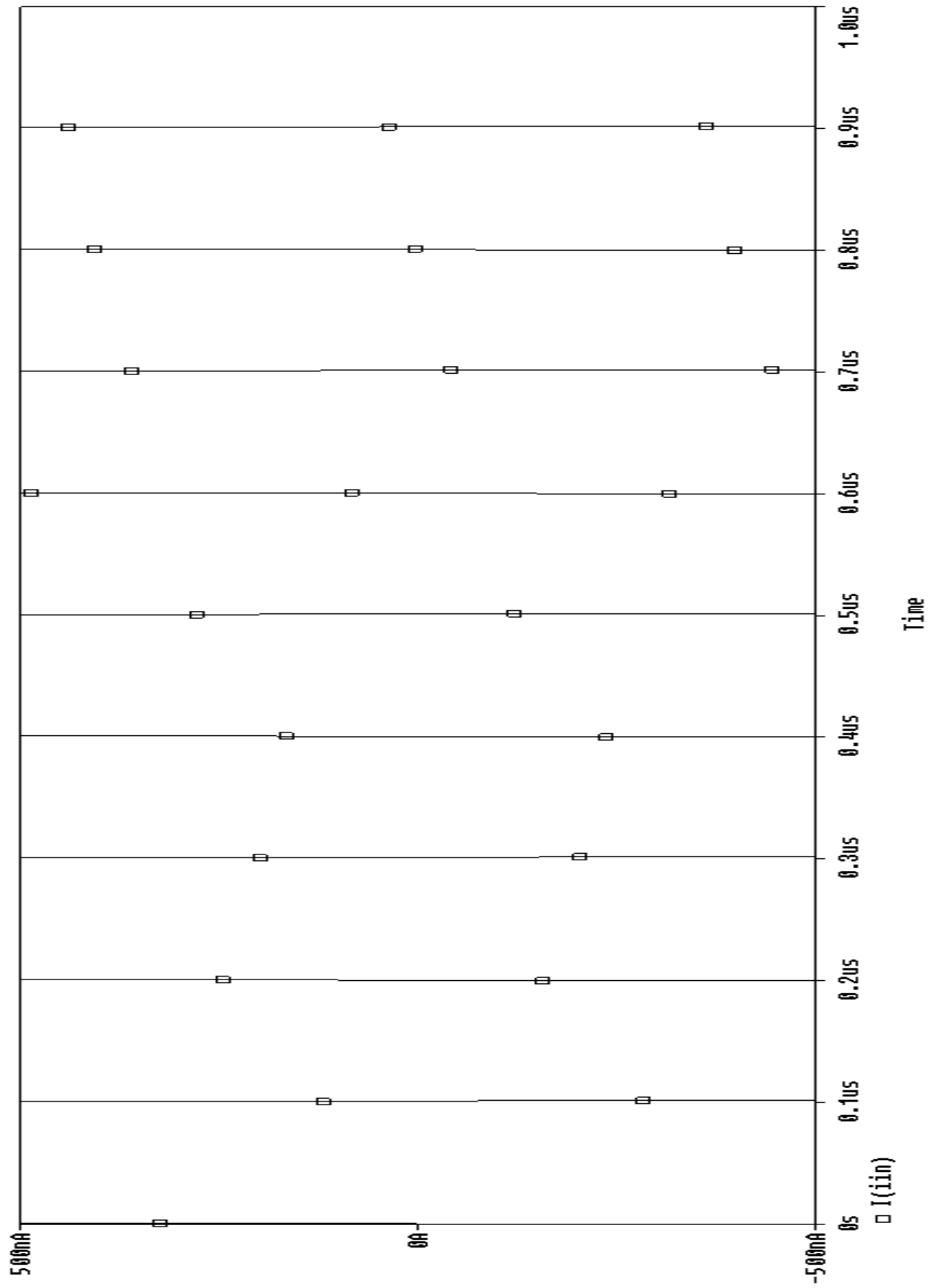
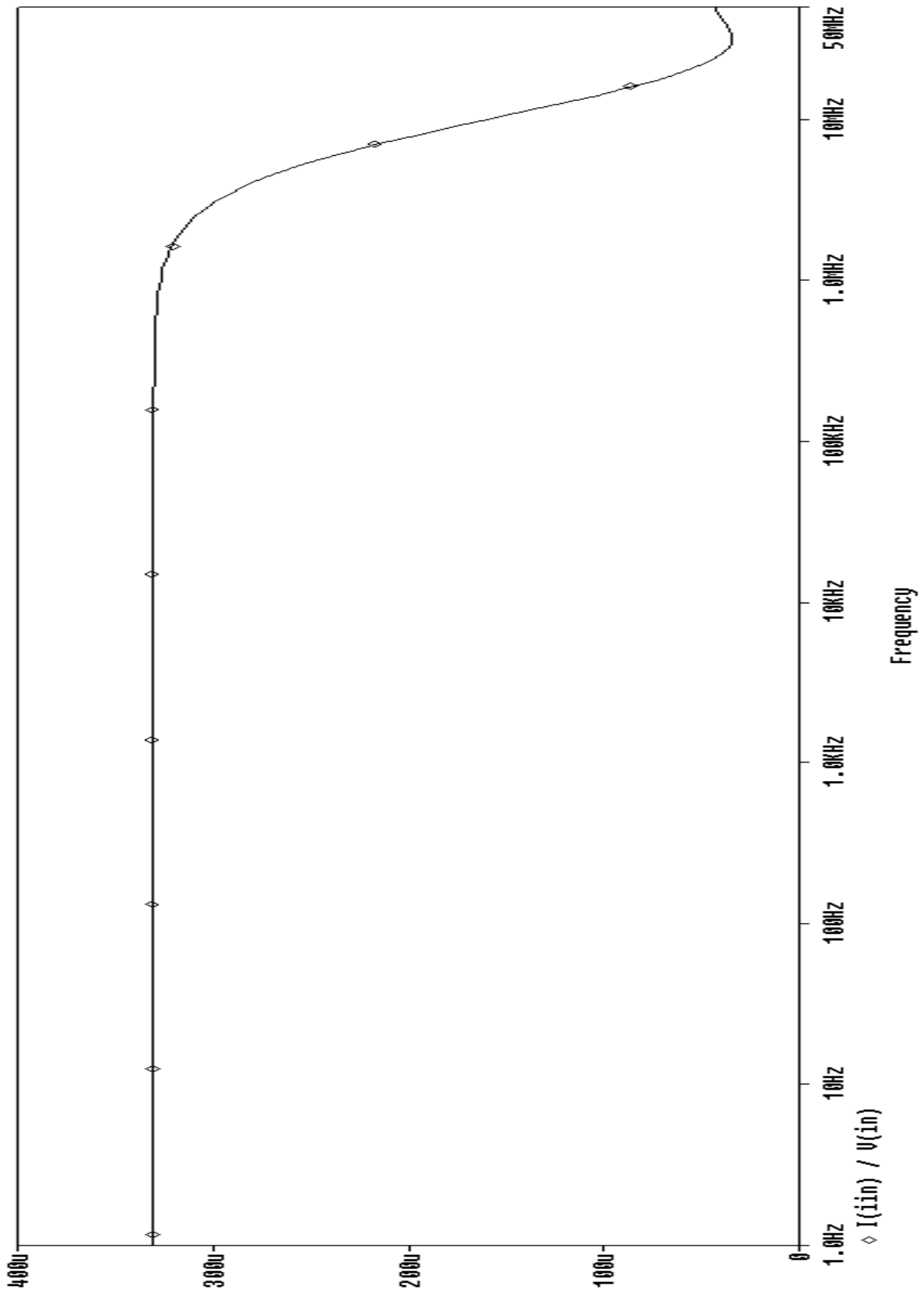
200uA
Iin
V(OUT1)


500nA
0A
-500nA
0s
0.1us
0.2us
0.3us
0.4us
0.5us
0.6us
0.7us
0.8us
0.9us
1.0us
Time
I(iin)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300u
200u
100u
0
1.0Hz
10Hz
100Hz
1.0KHz
10KHz
100KHz
1.0MHz
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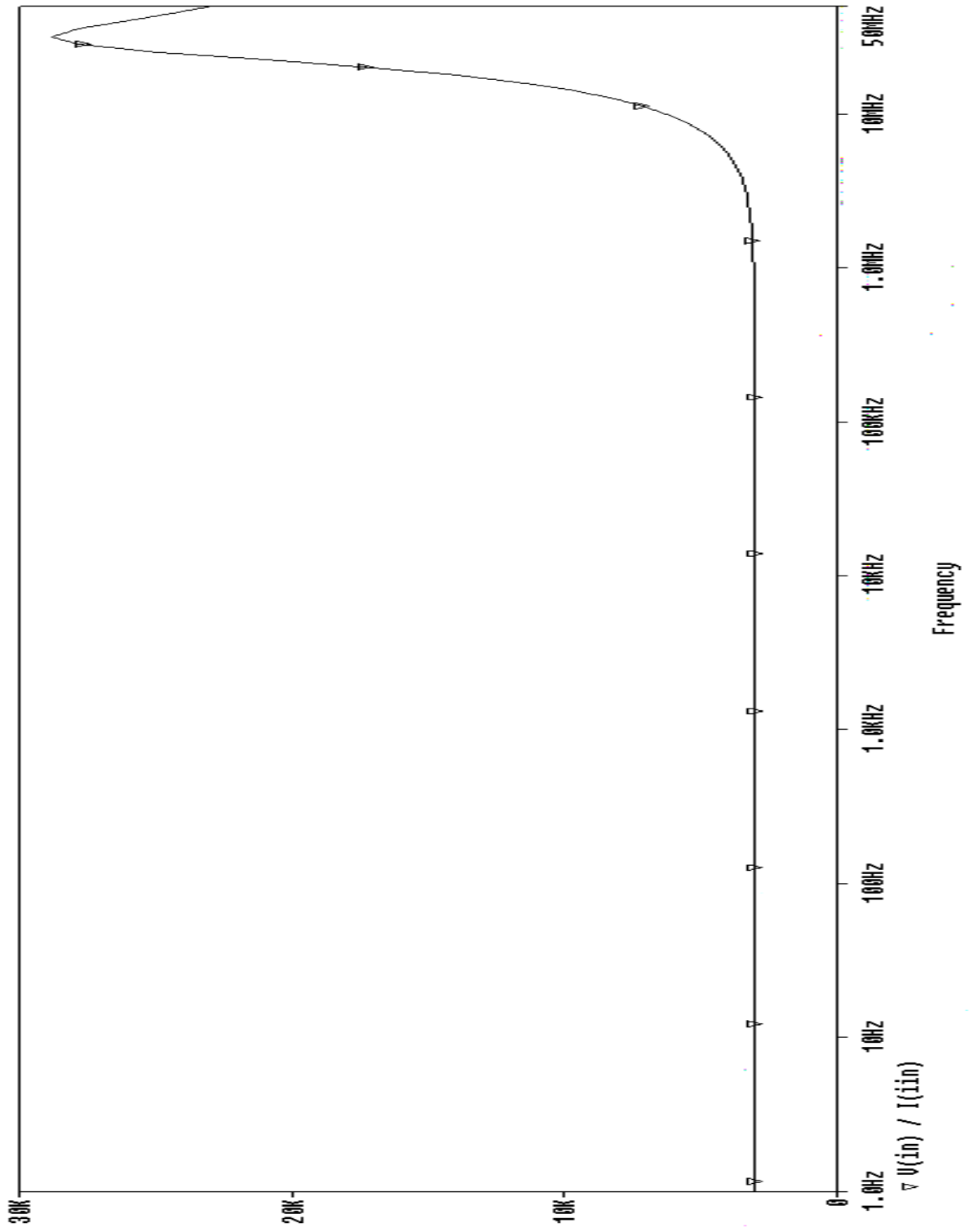
Frequency
◇ I(iin) / V(in)


30K
20K
10K
0
1.0Hz
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100Hz
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100KHz
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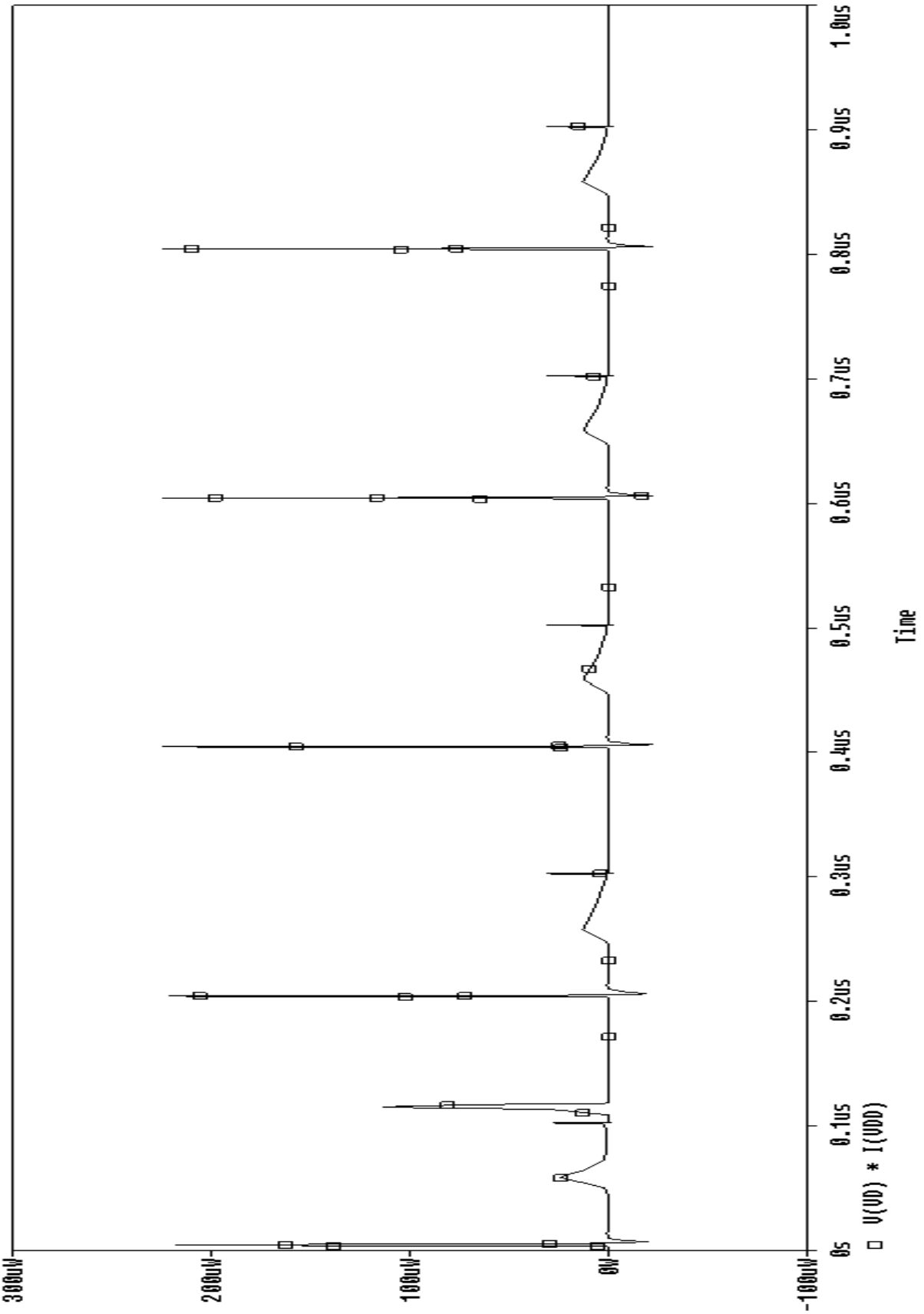
10MHz
50MHz
V(in) / I(iin)
Frequency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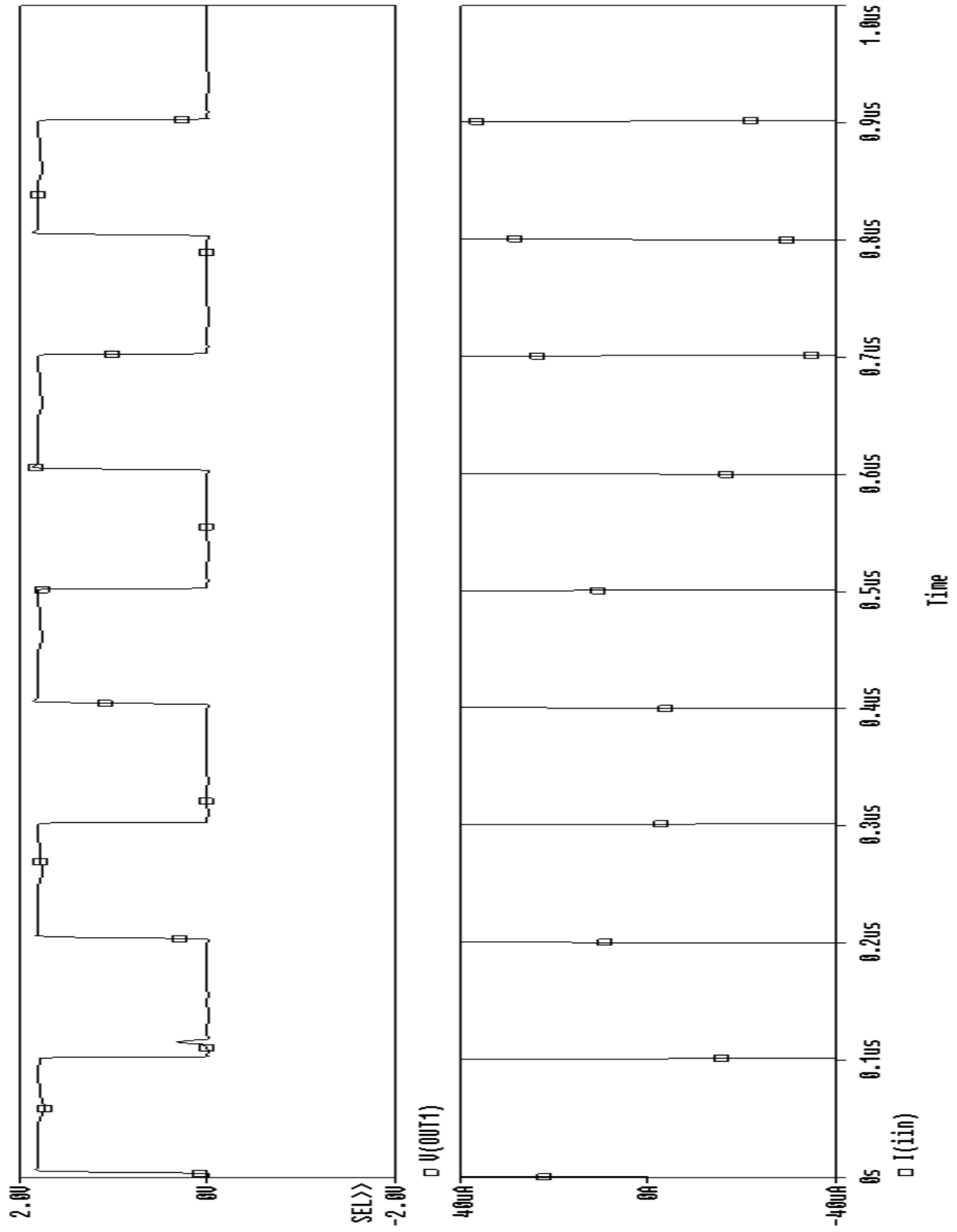
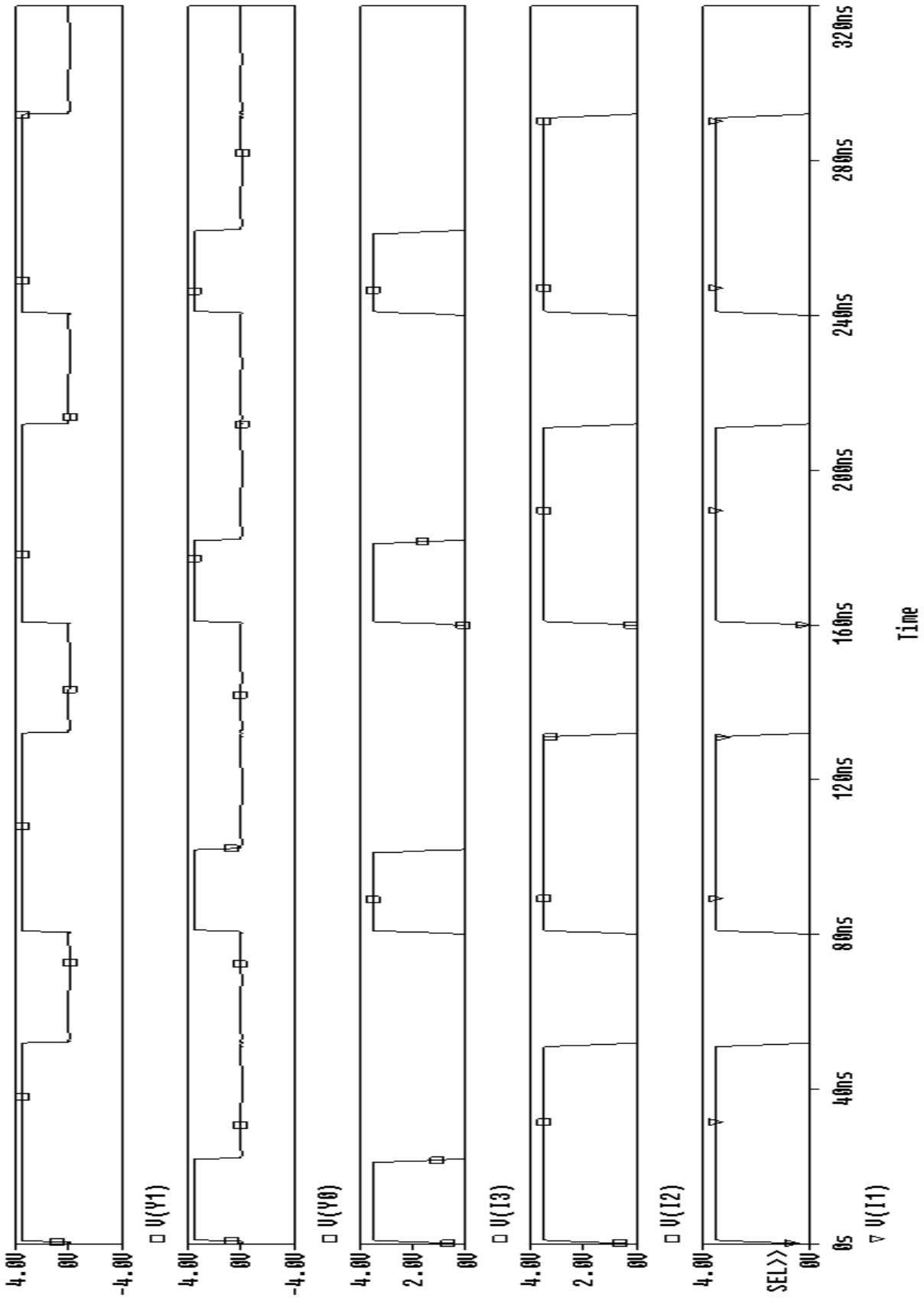
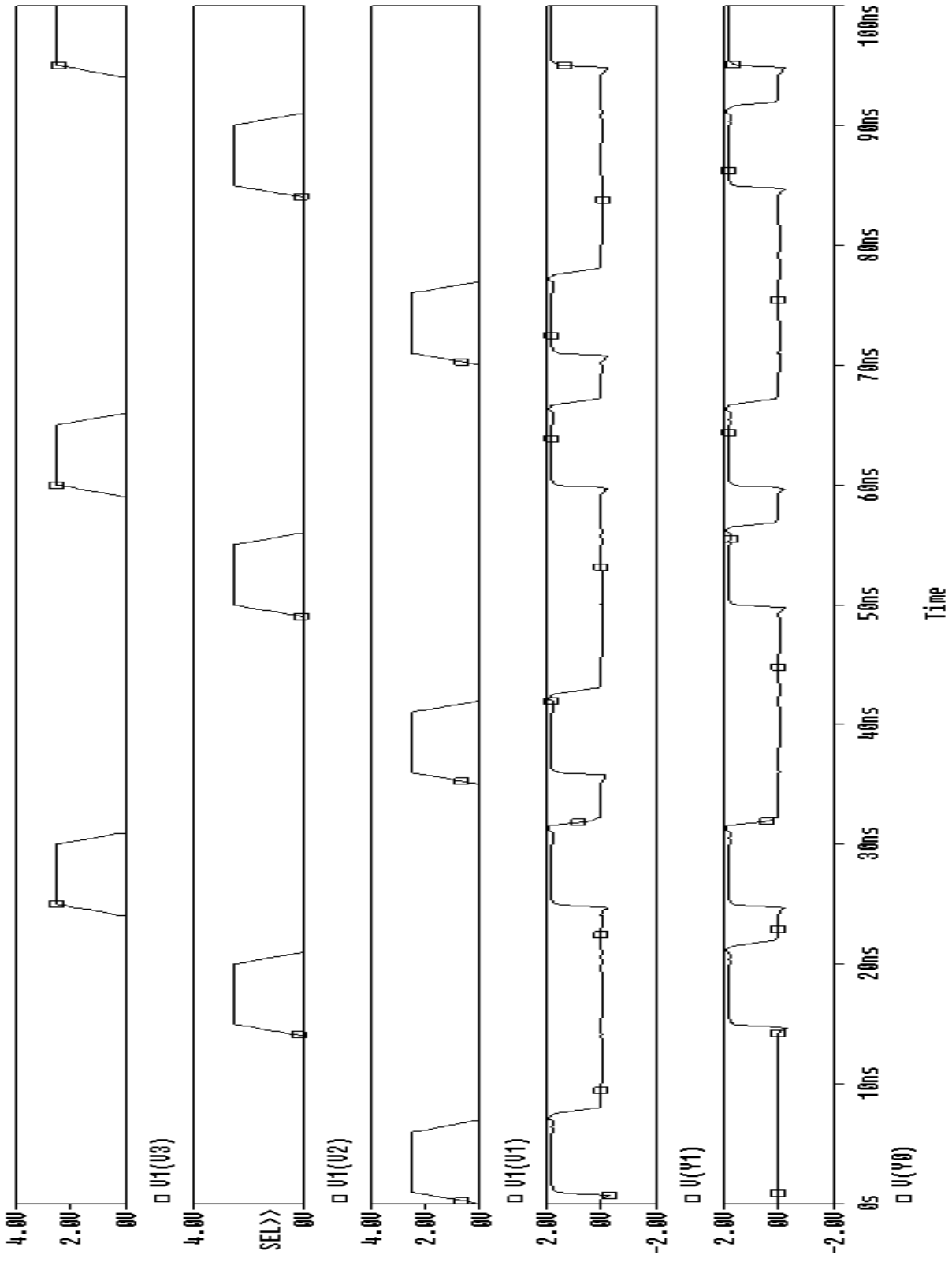
200uW
100uW
0W
-100uW
0s
0.1us
0.2us
0.3us
0.4us
0.5us
0.6us
0.7us
0.8us
0.9us
1.0us
Time
V(VD) * I(VDD)


2.0V
0V
SEL>>
-2.0V
V(OUT1)
40uA
0A
-40uA
I(iin)
0s
0.1us
0.2us
0.3us
0.4us
0.5us
0.6us
0.7us
0.8us
0.9us
1.0us
Time


4.0V
0V
-4.0V
V(V1)
4.0V
0V
-4.0V
V(V0)
4.0V
2.0V
0V
V(I3)
4.0V
2.0V
0V
V(I2)
4.0V
SEL>>
0V
V(I1)
0s
40ns
80ns
120ns
160ns
200ns
240ns
280ns
320ns
Time


4.0U
2.0U
0U
V1(U3)
4.0U
SEL>>
0U
V1(U2)
4.0U
2.0U
0U
V1(U1)
2.0U
0U
-2.0U
V(Y1)
2.0U
0U
-2.0U
0s
10ns
20ns
30ns
40ns
50ns
60ns
70ns
80ns
90ns
100ns
Time
V(Y0)

CHAPTER 6:-

CONCLUSION and FUTURE SCOPE

The comparator circuits for high speed ADCs have been investigated. The designs are mainly optimized for low propagation time, minimal input resolution and minimal circuit area. The comparator circuit topology with CC II circuit has been implemented, propagation time is reduced and power consumption is also reduced. The power consumption is reduced to about 160uW. The mirror trio circuit also implemented to provide the input signal to comparator circuit, which provides the excellent response. The scalability of this ADC design in terms of applicability to newer CMOS technologies using current conveyor increases the speed and decreasing power dissipation.

The circuit modules presented in the thesis used for designing different ADC structure for high speed, low power consumption namely flash ADC, Algorithmic ADC, folding and complementing structure of ADC's. However the encoder circuit MOS design concept used in the thesis can be change with pass transistor logic to increase the speed more. The ADCs can be ported to even smaller CMOS technologies to achieve even higher speed. For example the PMOS transistors are replaced by the resistors, the circuit operation is possible with lower supply voltage.

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APPENDIX

Model parameters --- LEVEL 7

.MODEL NMOS NMOS (LEVEL = 7

+TNOM =27	TOX=4.1E-9	
+XJ =1E-7	NCH =2.3549E17	VTH0= 0.3750766
+K1= 0.5842025	K2 =1.245202E-3	K3 =1E-3
+K3B =0.0295587	W0 =1E-7	NLX =1.597846E-7
+DVT0W =0	DVT1W =0	DVT2W =0
+DVT0=1.3022984	DVT1 =0.1021873	DVT2 =7.631374E-3
+U0 =296.8451012	UA=-1.179955E-9	UB =2.32616E-18
+UC= 7.593301E-11	VSAT =1.747147E5	A0 =2
+AGS =0.452647	B0=5.506962E-8	B1 =2.640458E-6
+KETA =-6.860244E-3	A1 =7.885522E-4	A2=0.3119338
+RDSW =105	PRWG =0.4826	PRWB =-0.2
+WR =1	WINT =4.410779E-9	LINT =2.045919E-8
+XL =0	XW=-1E-8	DWG =-2.610453E-9
+DWB =-4.344942E-9	VOFF =-0.0948017	NFACTOR =2.1860065
+CIT =0	CDSC =2.4E-4	CDSCD =0
+CDSCB =0	ETA0 =1.991317E-3	ETAB =6.028975E-5
+DSUB =0.0217897	PCLM =1.7062594	PDIBLC1=0.2320546
+PDIBLC2 =1.670588E-3	PDIBLCB =-0.1	DROUT =0.8388608
+PSCBE1 =1.904263E10	PSCBE2 =1.546939E-8	PVAG =0
+DELTA =0.01	RSH =7.1	MOBMOD =1
+PRT =0	UTE =-1.5	KT1 =-0.11
+KT1L =0	KT2 =0.022	UA1=4.31E-9
+UB1 =-7.61E-18	UC1 =-5.6E-11	AT = 3.3E4
+WL =0	WLN =1	WW =0

+WWN =1	WWL= 0	LL =0
+LLN =1	LW =0	LWN =1
+LWL =0	CAPMOD =2	XPART =0.5
+CGDO =6.7E-10	CGSO =6.7E-10	CGBO =1E-12
+CJ =9.550345E-4	PB =0.8	MJ = 0.3762949
+CJSW =2.083251E-10	PBSW =0.8	MJSW =0.1269477
+CJSWG =3.3E-10	PBSWG =0.8	MJSWG =0.1269477
+CF =0	PVTH0 =-2.369258E-3	PRDSW =-1.2091688
+PK2 =1.845284E-3	WKETA =-2.040084E-3	LKETA =-1.266704E-3
+PU0 = 1.0932981	PUA =-2.56934E-11	PUB =0
+PVSAT =2E3	PETA0=1E-4	PKETA =-3.350276E-3

)

.MODEL PMOS PMOS (LEVEL = 7

+TNOM =27	TOX=4.1E-9	
+XJ =1E-7	NCH =2.3549E17	VTH0= -0.3936726
+K1= 0.5750728	K2 =-0.0235926	K3 =0.1590089
+K3B =4.2687016	W0 =1E-6	NLX =1.033999E-7
+DVT0W =0	DVT1W =0	DVT2W =0
+DVT0=0.5560978	DVT1 =0.24790116	DVT2 =0.1
+U0 =112.5106786	UA=1.45072E-9	UB =1.195045E-21
+UC= 1E-10	VSAT =1.168535E5	A0 =1.7211984
+AGS =0.3806925	B0=4.296252E-7	B1 =1.288698E-6
+KETA =-0.0201833	A1 =0.2328472	A2=0.3
+RDSW =198.748329	PRWG =0.5	PRWB =-0.4971827
+WR =1	WINT =0	LINT =2.943206E-8
+XL =0	XW=-1E-8	DWG =-1.949253E-8
+DWB =-2.824041E-9	VOFF =-0.0979832	NFACTOR =1.9624066
+CIT =0	CDSC =2.4E-4	CDSCD =0
+CDSCB =0	ETA0 =7.282772E-4	ETAB =-3.818572E-4

+DSUB =1.518344E-3	PCLM =1.4728931	PDIBLC1=2.138043E-3
+PDIBLC2 =-9.966066E-6	PDIBLCB =-1E-3	DROUT =4.276128E-4
+PSCBE1 =4.8501167E10	PSCBE2 =5E-10	PVAG =0
+DELTA =0.01	RSH =8.2	MOBMOD =1
+PRT =0	UTE =-1.5	KT1 =-0.11
+KT1L =0	KT2 =0.022	UA1=4.31E-9
+UB1 =-7.61E-18	UC1 =-5.6E-11	AT = 3.3E4
+WL =0	WLN =1	WW =0
+WWN =1	WWL= 0	LL =0
+LLN =1	LW =0	LWN =1
+LWL =0	CAPMOD =2	XPART =0.5
+CGDO =7.47E-10	CGSO =7.47E-10	CGBO =1E-12
+CJ =9.550345E-4	PB =0.8560642	MJ = 0.4146818
+CJSW =2.046463E-10	PBSW =0.9123142	MJSW =0.316175
+CJSWG =4.22E-10	PBSWG =0.9123142	MJSWG =0.316175
+CF =0	PVTH0 =-8.456598E-4	PRDSW =8.4838247
+PK2 =1.338191E-3	WKETA =0.0246885	LKETA =-2.016897E-3
+PU0 = 1.5089586	PUA =-5.51646E-11	PUB =1E-21
+PVSAT =50	PETA0=1E-4	PKETA =-3.316832E-3

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