MODELING OF PHOTONIC CRYSTAL BASED LOGIC GATES AND OPTICAL DEVICES

A THESIS
Submitted to the Delhi Technological University
For the Award of the Degree of

DOCTOR OF PHILOSOPHY
IN
APPLIED PHYSICS

By

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DEPARTMENT OF APPLIED PHYSICS
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DELHI-110042 (INDIA)
OCTOBER 2016

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DECLARATION

This is to certify that this thesis entitled "**MODELING OF PHOTONIC CRYSTAL BASED LOGIC GATES AND OPTICAL DEVICES**", being submitted for the award of degree of Doctor of Philosophy to the Delhi Technological University, (Formerly Delhi College of Engineering) India, embodies the original research work carried out by me under the guidance of Dr. Yogita Kalra and Prof. Ravindra Kumar Sinha, Department of Applied Physics, Delhi Technological University, India. The results obtained in this thesis have not been submitted in part or in full to any other University or Institute for the award of any degree or diploma.

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DEDICATED

To

Lord Krishna

&

My Parents

Who have been my sources of Inspiration

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ABSTRACT

Recently, light guidance in photonic crystal structures has become one of the most fascinating technologies for the design and development of various optoelectronic devices. These structures provide an interesting platform for building the photonic circuitry due to their unique possibilities of molding the flow of light. Analogous to the electronic band gap in atomic crystals, photonic crystals exhibit photonic band gap, which is a wavelength range over which electromagnetic radiations are inhibited. The density of photon states in the photonic band gap region goes to zero. The two dimensional (2D) photonic crystals have attracted considerable attention due to their on-chip applications and the comparative ease of fabrication. They are periodic along a plane and extruded in the third dimension i.e. they include either periodically arranged dielectric rods in air or equally spaced air holes in a dielectric block.

This thesis addresses the design of all optical photonic crystal (PhC) devices and circuits. In this thesis, some novel designs of all optical logic gates have been presented. The two dimensional PhC composed of hexagonal array of silicon rods in air has been used for devising ultra compact photonic crystal waveguide based AND optical logic gate. Further, the AND optical logic gates have been designed in the PhC consisting of hexagonal array of air holes in silicon with the material waveguide as well as with the air waveguide. The proposed gates are operational at a wavelength of 1.55μm as also indicated by their spectral response.

Further, all-optical logic gates such as AND, OR, NOT, NAND, NOR, XOR, XNOR have been designed by introducing an appropriate initial phase difference between the input waveguides and the reference waveguide in the photonic crystal air bridge structure working for single polarization. However, these structures are mechanically unstable and require specific polarization leading to their unsuitability for on-chip integration. To overcome these problems, polarization independent all-optical logic gates have been designed on silicon on insulator (SOI) substrate. The contrast ratio, response period and bit rate have been calculated for all the proposed designs. These devices have

high switching rates as they require low power consumption of about micro watts and response time less than few pico seconds. Moreover, these devices are easier to fabricate and could be a strong candidate for future polarization independent all optical integrated circuits.

Another unique property of the photonic crystal structures is their ability to slow down the group velocity of light due to the strong light matter interaction. Slow light in slotted photonic crystal waveguide with slow down factor of 18.50 and its application as an optical buffer without the use of nonlinear material has been investigated in the thesis. The structure has been analysed for its application as time and wavelength division de-multiplexer.

Complete photonic band gap is exhibited by a few specifically designed photonic crystal structures only. A photonic crystal with honey comb lattice arrangement of air holes of two different radii on SOI substrate exhibits complete photonic band gap for a narrow range of frequencies. This feature has been exploited to design a polarization beam splitter. The characteristics of the proposed polarization beam splitter such as extinction ratio, insertion loss, excess loss, coupling loss and degree of polarization indicate the separation of two polarizations.

Hence, a suitably tailored photonic crystal structure can have a broad spectrum of applications ranging from the development of all-optical logic families to slow light photonic devices and polarization splitters, operational at a wavelength of 1.55 μm.

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AHS	Air Holes in Silicon
CAD	Computer Aided Design
CW	Continuous Wave
DBP	Delay Bandwidth Product
FDTD	Finite Difference Time Domain
FEM	Finite Element Method
GVD	Group Velocity Dispersion
IL	Insertion Loss
MZI	Mach-Zehnder Interferometer
NDBP	Normalized Delay Bandwidth Product
PhCs	Photonic crystals
PBG	Photonic Band Gap
PWE	Plane Wave Expansion
PML	Perfectly Matched Layer
PhCW	Photonic crystal waveguide
SOI	Silicon – on – Insulator
Si	Silicon
SPhCW	Slotted Photonic crystal waveguide
SRA	Silicon Rods in Air
SOA	Semiconductor Optical Amplifier

SiO_2	Silica
S	Slow Down Factor
TDM	Time Division De-Multiplexer
TE	Transverse Electric
TM	Transverse Magnetic
T	Transmittance
WDM	Wavelength Division De-Multiplexer
1D	One Dimensional
2D	Two Dimensional
3D	Three Dimensional

CHAPTER 1
Introduction

1.1 Introduction

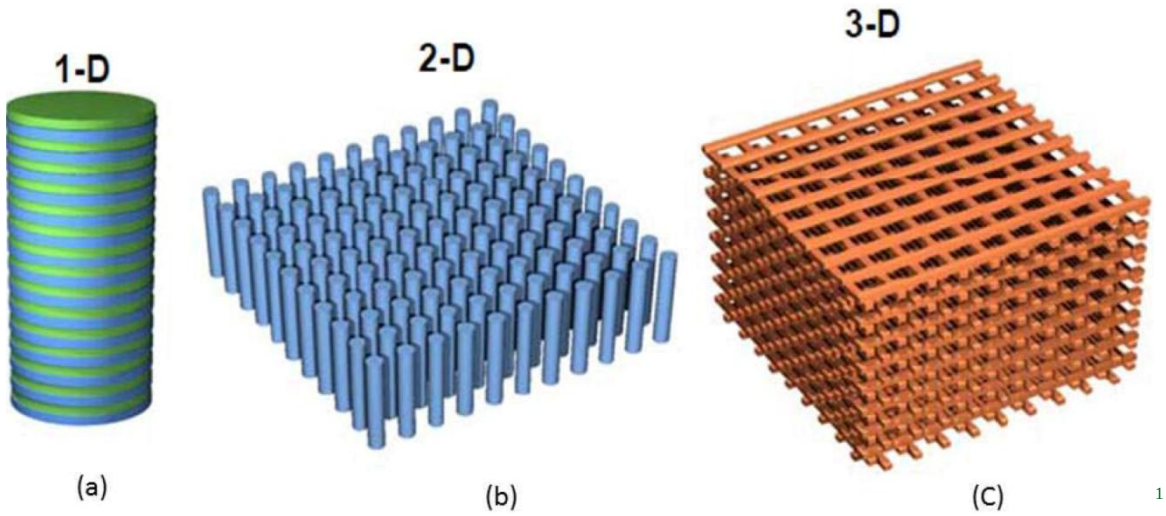
Photonics technology has become an attractive alternative to the electronic technology due to their several advantages over their counterparts. This includes larger bandwidth, high transmission, manipulation and storage of data using photons, low power consumption and reduced energy losses. The on-chip and chip-to-chip optical devices based on so called photonic crystals (PhCs) and quasi crystals pave a way towards faster signal processing. These highly periodic structures can be used to operate at the desired frequencies leading to the conception of all optical logic gates, switches, filters and transistors. The on-chip optical communication provides a path for transfer of information from one part of the microchip to another end by means of light propagation through optical waveguides, which in turn has improved the speed of optical communication. The highly developed micro and nano fabrication technology has now enabled the design and development of ultra compact on chip silicon integrated optical devices. In addition, a good progress has been made in the development of new technologies and techniques for producing controllable optical waveguides with slow group velocity. This also offers a robust platform for developing applications based on slow light techniques. The development of the subject and how it has convincingly become the platform of the present day technology has been briefly discussed below.

1.2 Literature review

1.2.1 Photonic crystals

Firstly, Lord Rayleigh in 1887 studied the propagation of electromagnetic waves in periodic media called as one dimensional (1D) photonic crystals. These structures exhibit a narrow band gap prohibiting light to propagate through the planes. About a century later, the designing of PhCs was proposed by Eli Yablonovitch and Sajeev John in 1987 [1, 2].

Photonic crystals [3] are the materials with refractive index periodicity that affect the propagation of electromagnetic waves in the same way as periodic potential in semiconductors affect the motion of electrons defined by allowed and forbidden energy bands. Depending on the periodicity they are categorized as one dimensional (1D), two dimensional (2D) and three dimensional (3D) PhCs as shown in figures 1.1(a), (b) and (c) respectively.



[1]

Fig. 1.1 Types of photonic crystals

1D PhCs [4, 5] are alternating stacks of dielectric constants along the propagation direction and are useful in wide range of applications such as high reflection mirrors, stop band filters, anti reflecting coatings and cavities for distributed feedback lasers. A 2D PhCs are periodic array of dielectric constants along two directions while homogenous and infinite in a direction perpendicular to the plane of periodicity. A good example of 2D PhC is periodically arranged air holes in homogenous medium and dielectric rods in air. The 3D PhCs consist of regular periodicity of dielectric constants in all the three directions. PhCs also exist in nature, such as pattern on the wings of blue Morpho butterfly, feathers of peacock, fur of sea mouse and also occur in hard minerals (opals). Due to the difficulty in fabrication of 3D PhC structures more attention has been drawn on the development of 2D PhC slab structures. 2D PhCs are believed to be of great importance in integrated devices

[1] Image: http://www.intechopen.com/books/advances-in-photonic-crystals/photonic-crystal-ring-resonator-based-optical-filters

with nanoscale features due to the existence of the photonic bandgap and easily available fabrication techniques. Photonic bandgap (PBG) is a band of frequencies within which light is prohibited from propagating inside the PhC. The band gap analysis and propagation of light in PhCs have been calculated by solving the Master equation [3] which is obtained by four Maxwell's equations in isotropic linear dielectric medium i.e.

$$\vec{\nabla} \bullet \vec{B} = 0 \tag{1.1}$$

$$\vec{\nabla} \bullet \vec{D} = \rho \tag{1.2}$$

$$\vec{\nabla} \times \vec{E} = -\frac{\partial \vec{B}}{\partial t} \tag{1.3}$$

$$\vec{\nabla} \times \vec{H} = \frac{\partial \vec{D}}{\partial t} + \vec{J} \tag{1.4}$$

and the constitutive relations

$$\vec{J} = \sigma \vec{E} \tag{1.5}$$

$$\vec{D} = \varepsilon \vec{E} \tag{1.6}$$

$$\vec{B} = \mu \vec{H} \tag{1.7}$$

where, $\vec{E}$ is the macroscopic electric field, $\vec{H}$ is the magnetic field, ρ is the free charge density, $\vec{J}$ is current density, $\varepsilon = \varepsilon_0 \varepsilon_r$ is the permittivity in isotropic medium (where ε_0 is the permittivity of vacuum and ε_r is the relative permittivity), and $\mu = \mu_0 \mu_r$, is the permeability (where μ_0 is the permeability in vacuum and μ_r is the relative permeability). The materials used in this work are non-magnetic insulators i.e. $\rho = 0$, $\vec{J} = 0$ and $\sigma = 0$, therefore equations (1.3) and (1.4) can be written as

$$\vec{\nabla} \times \vec{E}(r,t) = -\frac{\partial}{\partial t}\left[\mu_0 \vec{H}(r,t) \right] \tag{1.8}$$

$$\vec{\nabla}\times\vec{H}(r,t)=\frac{\partial}{\partial t}\left[\varepsilon_0\varepsilon_r(r)\vec{E}(r,t)\right] \tag{1.9}$$

On taking curl of equation (1.9) and substituting the time derivative of equation (1.8) into it, equation (1.9) becomes:

$$\vec{\nabla}\times\left[\frac{1}{\varepsilon_0\varepsilon_r(r)}\vec{\nabla}\times\vec{H}(r,t)\right]=-\frac{\partial^2}{\partial t^2}\mu_0\vec{H}(r,t) \tag{1.10}$$

The magnetic field in terms of harmonic modes can be written as:

$$\vec{H}(r,t)=\vec{H}(r)e^{-i\omega t} \tag{1.11}$$

Using equation (1.11), equation (1.10) becomes:

$$\vec{\nabla}\times\left[\frac{1}{\varepsilon_0\varepsilon_r(r)}\vec{\nabla}\times\vec{H}(r)\right]=\left(\frac{\omega}{c}\right)^2\vec{H}(r) \tag{1.12}$$

where, $c=\left[\frac{1}{\sqrt{\varepsilon_0\mu_0}}\right]$ is the speed of light in vacuum. Equation (1.12) is known as the master equation in terms of the magnetic field. The electric field can be calculated from

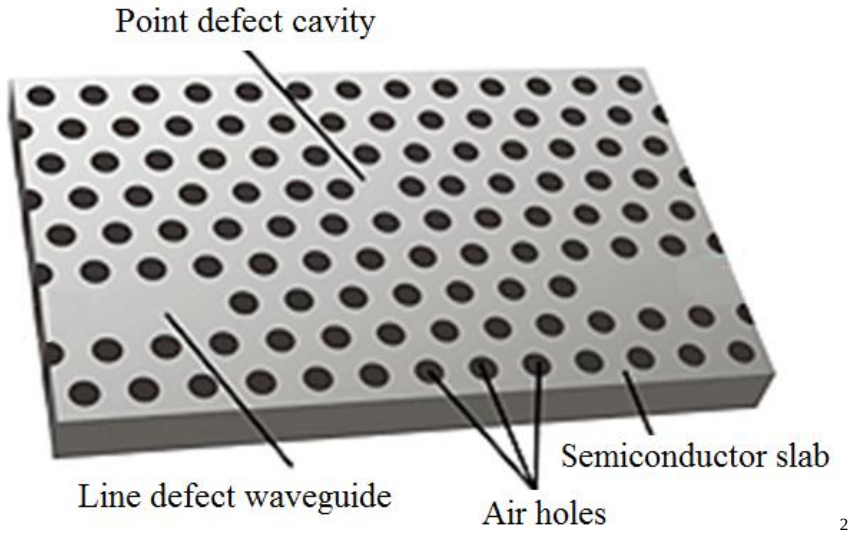
$$\vec{E}(r)=\frac{i}{\omega\varepsilon_0\varepsilon_r}\vec{\nabla}\times\vec{H}(r) \tag{1.13}$$

The master equation can be analogously written in terms of electric field as:

$$\vec{\nabla}\times\vec{\nabla}\times\vec{E}(r)=\left(\frac{\omega}{c}\right)^2\varepsilon_0\varepsilon_r(r)\vec{E}(r) \tag{1.14}$$

2D PhCs are of much interest not only due to the presence of photonic band gaps but due to the possibility of creation of localized defect states within the band gap region. The structural defects are classified as point defects i.e. cavity and extended defects/line defects i.e. waveguide [6-7] as shown in figure 1.2. The point defects can be created by locally modifying the refractive index, by changing the size of the patterns, by displacing one of the periodic patterns or by inserting a different pattern. The waveguides are alignment of identical point defects which are regularly spaced along the desired direction. Line defects

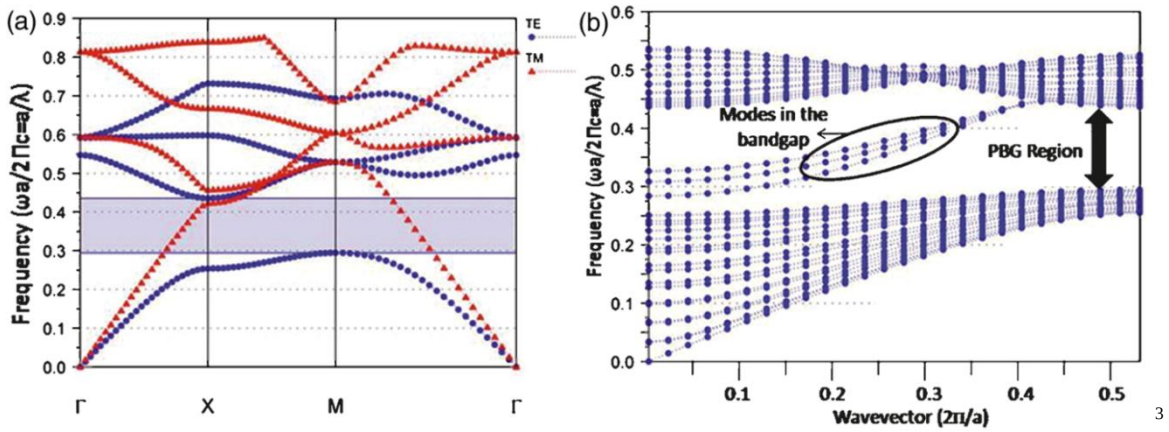
are sometimes called as defect doping (i.e. acceptor doping and donor doping) similar to impurity doping of semiconductors. In acceptor doping, the effective index at the lattice site is reduced either by replacing some higher index material with a lower index material or by increasing the size of air holes in a slab whereas, in donor doping the effective index at a lattice site is increased either by replacing some low index material with higher index material or by reducing the size of air holes in slab. These defect sites create defect associated photon states or defect modes in the band gap region as shown in figure 1.3. These defect modes are analogous to the impurity or dopant states between the conduction band and valence band of the semiconductor. A light wave with defect mode frequency does not leak out in the surrounding periodic medium and propagates inside the photonic crystal waveguide as shown in figure 1.4. The loss in the waveguide depends on its width approximately as 1/ (width) [2].



[2]

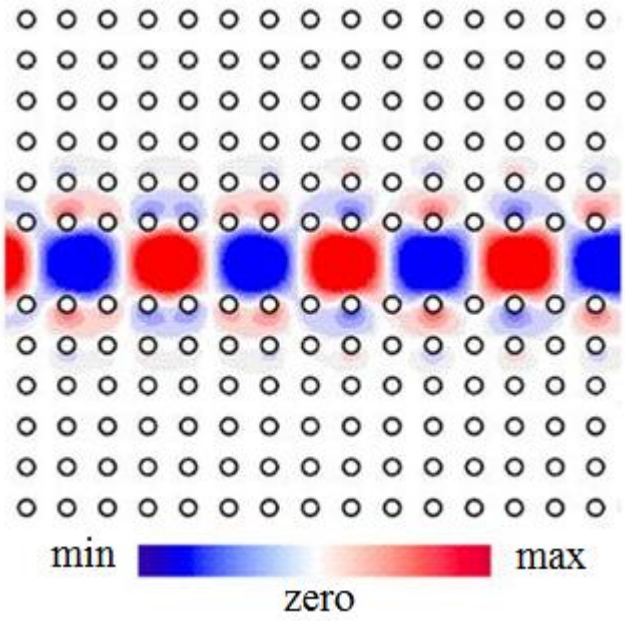
Fig.1.2 Schematic representation of point defect and line defect in photonic crystal

[2] Image : https://www.ntt-review.jp/archive/ntttechnical.php?contents=ntr201108ra1.html



[3]

Fig. 1.3 Dispersion relation showing defect mode within the band gap range



[4]

Fig. 1.4 Schematic filed distribution showing propagation of defect mode in photonic crystal waveguide

Basically, two types of 2D PhCs exist, one of which consist of disconnected dielectric cylinders and the other one is formed by air pores drilled in the dielectric matrix as shown in figure 1.5. These are symmetrical 2D PhC slab structures in which light is confined in the horizontal direction due to photonic band gap effect and in the vertical

[3] Image: http://nanophotonics.spiedigitallibrary.org/article.aspx?articleid=1226536

[4] Image: https://nanohub.org/resources/19417/watch?resid=19419

direction by total internal reflection due to the changes in the refractive index at the surface. The symmetrical structures are mechanically unstable from the fabrication point of view. An asymmetrical 2D PhC slab structure i.e. silicon on insulator (SOI) structure provides a new platform for planar integrated optics. In 2D PhC slab structures the propagating modes have been chosen with respect to the light line. The modes which lie below the light line are ideally not subject to propagation losses whereas the modes above the light line are called as leaky radiation modes and offer the propagation losses in the vertical direction.

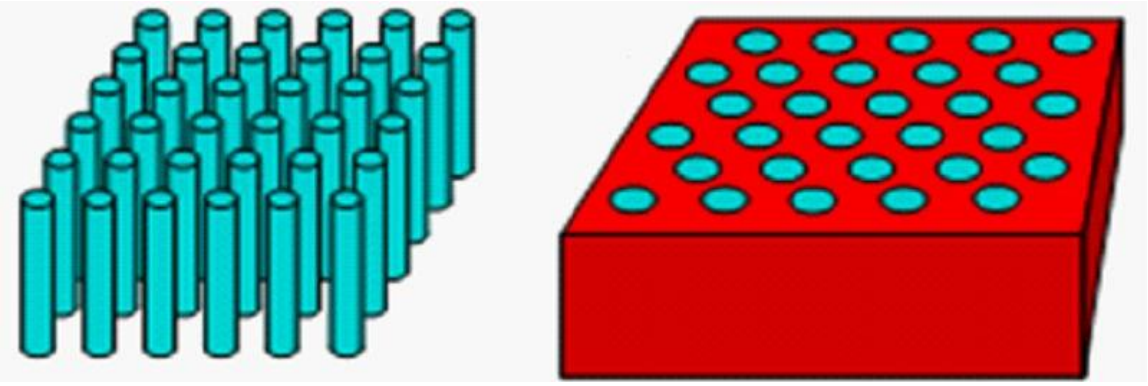
 [5]

Fig. 1.5 Schematic representation of (a) dielectric cylinders in air and (b) air holes in dielectric medium

2D PhCs could be developed into a direct continuation of planar integrated optics on employing the semi-infinite slab structures. These structures offer a tremendous advantage in terms of realization of compact optical devices as compared to the current status. These structures are assumed to be finite along the vertical direction and infinite along the horizontal directions. These PBG structures offer a wide variety of applications such as polarisers, splitters, multiplexers and de-multiplexers, couplers, resonators, lasers, modulators and logical devices [8-13].

[5] Image: http://www.intechopen.com/books/advances-in-photonic-crystals/photonic-crystal-ring-resonator-based-optical-filters

1.2.2 Optical logic gates

In recent years various techniques have been employed to design optical logic gates which are classified into two groups, one is band gap based and another is non band gap based. Band gap based logic gates have been designed using interferometers [14], modulators [11], filters [15], waveguides [16], multiplexers/de-multiplexers [17] and lasers [12], whereas non band gap based logic gates have been designed on the concept of self collimation effect [18] and dispersive prisms [19] that utilize the anisotropic dispersion exhibited by the photonic crystals. The main goal of designing and manufacturing optical logic gates is to increase the operational bandwidth, decrease power consumption, improve response time between the ON and OFF state, increase the contrast ratio between the high and low logical levels and integrate them to create all-optical logic circuits. Recently, photonic crystal based logic gates have received considerable attention to create optical processors because of the reduction in the size of the optical logic gate to the order of wavelength. Optical logic gates have low power consumption of about few microwatts and high switching speed with response time less than a few picoseconds. Optical logic gates have great influence in all-optical signal processors, optical computers and in high speed communication networks due to their numerous applications such as switching, computing, buffering, data encoding, signal regeneration, address recognition, data encryption/decryption, parity checking and de-multiplexing. The switching speed in optical logic gates is only limited by the speed of light passing through it.

1.2.3 Slow light

The ultra high speed for the efficient data transmission between two points is advantageous but requires the control of optical signals in the time domain, which is a difficult task and to overcome this problem slow light technology has now been investigated as a new means. Recently engineers have been developing information networks for all-optical signal processing that avoid electro optic conversions and provide solutions for the loop holes in present mechanical approaches. The control on the group velocity of light with much faster response speed could be useful in the design of optical buffers and in various types of time domain processing techniques such as multiplexing, retiming and performing convolution integrals [20]. Control over group velocity improves the phase control in array

beam shapers and interferometric modulators. It is also helpful in compressing optical signals and optical energy in space. Recently, photonic crystal structures are being considered as promising candidates for generation of slow light, as they are compatible with on-chip integration and room temperature operations. They also provide wide bandwidth and dispersion free propagation [21-24]. A delay bandwidth product (DBP) which is defined as the extent up to which group velocity of light is reduced within the required bandwidth range below the light line is a desirable property for dispersion compensated slow light devices. Slow light in PhCs is motivated by the fact that it can be achieved by changing the structural parameters alone. The nearly flat band region in the dispersion diagram can be used to achieve slow light in photonic crystal structures. This can be obtained by various ways such as by chirping the waveguide properties, by changing the waveguide width, by changing the holes size and shape, by infiltrating holes with dielectric materials and by adjusting the position of the holes adjacent to the PhC waveguide. Some of these techniques may lead to multimode operation and others are difficult to control during on chip fabrication processes. However, the photonic crystal structures with low group velocity, low group velocity dispersion (GVD) and broad bandwidth [21, 25] can find applications in optical buffer (for storage of data) as well as time and wavelength division de-multiplexing (TDM and WDM) [26].

1.3 Methods of fabrication

The fabrication methods [27, 28] play an important role in the study and practical applications of PhCs. Due to the unavailability of natural PhCs for their commercial use, several attempts have been made for the design and fabrication of the artificially structured materials which show the properties of PhCs. Various techniques have been proposed to fabricate high quality PhCs which have revolutionized the optical integrated circuits. The templates for PhCs have been created using wide variety of methods such as 1D PhCs and can be fabricated using molecular beam epitaxy method, chemical vapor deposition method, pulsed layer deposition method, spin coating method and sol gel method. The 2D PhCs and 3D PhCs are more complicated in terms of fabrication and require expensive micro fabrication technologies such as laser holography lithography, self-assembly of colloidal particles and direct laser writing, etc. A number of techniques are available for

colloidal assembly fabrication and widely used techniques are gravity sedimentation and cell method introduced by Xia and co-workers [29, 30] which is useful for fabrication of polystyrene PhCs in water. The two photon lithography technique for the fabrication of 3D PhCs such as logpile type PhC utilizes the fact that certain materials are sensitive to two photon excitation to trigger chemical and physical changes in the material structure. The electron beam lithography is relatively a complicated method that enables one to create on chip PhCs with extremely high resolution. It uses a focused beam of electrons to drill holes in a given substrate. The beam position and intensity is computer controlled and are too focused to specific areas to get the desired pattern. After the exposition the samples are accompanied by etching procedures to get the final crystalline structure. The holographic method utilizes the concept of multiple beam interference technique in which initial laser beam is split into several beams and is allowed to overlap at angles predetermined by the desired periodicity. The holographic method can also be used to fabricate electrically switchable polymer-dispersed liquid crystal photonic band gap materials. In holographic method highly periodic structures can be fabricated in a single laser exposure, thus avoiding step by step fabrication process.

1.4 Outline of the thesis

The main focus of this thesis is to design and characterize all optical devices based on the photonic crystal waveguides. These devices include the design of optical logic gates, optical buffers and delay lines, and polarization splitter. This thesis also includes generation of slow light in slotted photonic crystal waveguide and its applications. The thesis is divided into seven chapters as per the following layout.

Chapter 1 defines the literature review about photonic crystals and how they are useful in the design of optical devices. Further, the design of all the proposed devices in the present thesis have been formulated using certain computation methods as discussed below:

1.4.1 Computational methods

Recently research has been oriented in a more focused way towards the analysis of distinct characteristics of photonic crystal for the optoelectronics. The analysis of PhCs require

computer capabilities through the computer aided design (CAD) that can provide exact, fast and efficient solutions of Master equations shown above. The solution of most practical and complex structures requires efficient numerical methods such as Plane Wave Expansion (PWE) Method, Finite Difference Time Domain (FDTD) Method and Finite Element Method (FEM).

Here, the basic principle behind different numerical methods used for the theoretical analysis of the structures presented in this thesis work has been discussed.

1.4.1.1 Plane Wave Expansion (PWE) Method

Plane Wave Expansion (PWE) method is a computational technique based on Fourier expansion of electromagnetic fields and dielectric function. PWE is an efficient method for obtaining the band structures of photonic crystals. PWE expansions are rigorous solutions and well suited for the model solutions of Maxwell's equations over an inhomogeneous or periodic geometry. This method solves Maxwell's equations by formulating an Eigen value problem out of the Master equation which gives rise to a set of Eigen values 'ωa/2πc' for each value of 'k' i.e. optical modes solved in wave vector space or reciprocal space. In this thesis work the dispersion relations for periodic as well as for non periodic structures i.e. cavities and waveguides have been calculated using RSoft Bandsolve Software [31] by implementing a supercell of specific dimension.

1.4.1.2 Finite Difference Time Domain (FDTD) Method

Finite Difference Time Domain (FDTD) method is a robust, flexible, efficient, versatile, easy to understand, easy to implement and user friendly technique used to solve Maxwell's equations in time domain. This method solves Maxwell's equations by discretizing the equation via central differences in time and space and is based on Yee's mesh. It calculates the E and H field components at points on a grid with grid points spaced apart by Δx, Δy, and Δz. Further E and H field components are then interlaced in all the three spatial dimensions and time is broken up into discrete steps of Δt. The FDTD grid consists of electric and magnetic field nodes separated from each other by half space step i.e. electric field values computed at integer time steps (i.e. $t = n\Delta t$) and magnetic field values at half integer time steps (i.e. $t = (n+1/2)\Delta t$, where n is an integer representing the computation step). This method results into six equations that can be used to compute the field at a

given mesh point. Then the equations are iteratively solved in a leapfrog manner, alternating between computing the E and H fields at subsequent Δt/2 intervals. FDTD is suitable to obtain the transmission and reflection coefficients. It is a useful tool to understand the wave propagation through photonic crystal structures on calculating their band structures. The band structure is calculated by Fourier transform of the time dependent field to the frequency domain. This method is flexible in terms of geometry of the device i.e. it can solve electromagnetic fields in 2D and 3D respectively. FDTD simulations in this thesis have been carried out using RSoft Full Wave software.

1.4.1.3 Finite Element Method (FEM)

The Finite Element Method (FEM) is a versatile numerical technique in which domain of the problem is discretized into small elements. This method includes meshing or segmentation of the complicated device geometries into finite number of sub regions or elements of triangular or rectangular shapes such that the dielectric is homogenous in each element. There are many types of finite element methods for vector wave analyses, such as FEM using longitudinal electromagnetic field components (Ez and Hz), FEM using the three electric or magnetic field components and FEM using transverse electromagnetic field components. FEM is also effective for the calculation of effective index i.e. n_{eff} of the slab structures and analysis of waveguides of arbitrary cross section and dielectric in-homogeneity. FEM is applicable to the complicated domain structures and to problems in which electromagnetic fields are localized. This technique has become popular in electromagnetic because of its desirable features like geometrical adaptability and low memory requirements. In the present thesis, FEM simulations have been carried out to calculate the effective index of the photonic crystal slabs using RSoft FemSIM software.

The above mentioned computational/ numerical techniques have been used to design and analyse the various devices proposed in this thesis.

Chapter 2 proposes the design of optical logic AND gate based on three structures, one of which is a hexagonal lattice with silicon (Si) rods in air with air waveguide. The other two structures consist of air holes in Si, one with air waveguide and another with material waveguide. All the designs for the realization of AND optical logic gate is a line defect induced symmetric Y-branch waveguide. The plane wave expansion method and

finite difference time domain method have been used to design and analyze the logic behaviour. The performance of the three structures has been compared on the basis of their response time and bit rate.

Chapter 3 describes the design of all optical logic gates based on concept of interference of various inputs in 2D PhC composed of triangular lattice of air holes in Si. All the optical logic operations can be achieved if an appropriate initial phase is introduced between the input beams so that they may interfere constructively or destructively. The results show that the proposed structure could really function as all optical logic gates. The truth table as well as the performance of the device has been analyzed.

Chapter 4 reports the design and analysis of polarization independent all optical logic gates on SOI platform. The polarization independent all optical logic gates have been designed in 2 D honeycomb lattices with two different air holes exhibiting complete photonic band gap i.e. for both TE and TM modes in the same frequency range in the optical communication window. The performance of the proposed gates has been analysed.

Chapter 5 describes slow light effect in slotted PhC waveguide (SPhCW). A SPhCW is a waveguide in which light is confined in the low index region as compared to the conventional PhC waveguide where light is confined in the high index region. PhC structure consists of a hexagonal arrangement of elliptical air holes on a SOI substrate. A slotted waveguide has been created in the W1 waveguide so as to show the slow light effect. The SPhCW structure confines the light in an air slot as compared to the normal material waveguide which results into lower absorption losses. The structure has low group velocity and low group velocity dispersion with a wide normalized bandwidth range. Due to the large value of normalized delay bandwidth product equal to 0.634, it can be used as an optical buffer for the storage of large amount of data. The structure has also been analyzed for its applications as both time and wavelength division de-multiplexer.

Chapter 6 reports a design of polarization beam splitter based on the phenomenon of photonic crystal direction coupler. The design consists of honeycomb lattice arrangement of air holes of different radii in SOI substrate exhibiting complete photonic band gap. The coupling characteristics such as extinction ratio, insertion loss, excess loss, coupling ratio and degree of polarization of the proposed design have been obtained. The

extinction ratio for TE and TM polarizations is found out to be 24.56 and 28.29 dB, respectively at a wavelength of 1.55 μm. The degree of polarization for TE and TM polarizations are 99.29% and 99.70% which indicates the proper splitting of the two polarizations.

Chapter 7, summarizes and concludes the research work done in the previous chapters and describes the future scope of the research work carried out in the thesis.

CHAPTER 2

Design of optical logic AND gates in Y shaped photonic crystal waveguides[1]

2.1 Introduction

As mentioned in the previous chapter, photonic crystals (PhCs) have emerged as a versatile platform to construct nanoscale optical devices and are useful in the field of optical communication due to certain unique properties such as compactness, high speed, low power consumption and better confinement. Recently all optical logic gates have received much attention for their applications in real time optical processing and information communications [32-43], because all optical signal processing can handle large bandwidth signals, large information flows and have no need of electrical to optical conversion. In recent years, interest has been grown in the design and development of optical logic gates based on different schemes such as using nonlinear effects in optical fibers [44-48] and in waveguides [49-51], but most of these work suffer from certain limitations such as big size, low speed and difficult to perform chip-scale integration. Thus photonic crystal based all optical logic gates are considered as key elements in future photonic integrated circuits as logic gates are capable of performing many logic functions and have many applications in optical communication, photonic microprocessors, optical signal processors and optical instrumentation and such optical devices have attracted significant research in recent years. Most of the recent research work is based on material rods assembled in air with air

[1] Part of the results reported in this chapter has been published in the paper: "Realization of AND gate in Y shaped photonic crystal waveguide", Optics Communications, 298–299, pp. 227–231, 2013. http://dx.doi.org/10.1016/j.optcom.2013.02.014

[1] Part of the results reported in this chapter has been published in the SPIE conference proceedings: Design of Photonic Crystal Architecture for Optical Logic AND Gates', SPIE Optics +Photonic 2013 (Photonic Fiber and Crystal Devices: Advances in Materials and Innovations in Device Applications VII), August 25-29, 2013. San Diego USA: SPIE, pp. 88470X. http://dx.doi.org/10.1117/12.2023855

cladding on both sides [52-55] i.e. the PhC structures are freely suspended in air. These air-bridge structures having air cladding on both sides are mechanically unstable from practical perspective as well as they are not suitable for future integrated circuits [8, 56] and large scale integration. Structures with solid support are more realistic and suitable. To the best of our knowledge, a few optical logic gates have been proposed in two dimensional photonic crystal structures (2D PhC) composed of air holes in silicon (Si). In this chapter, we report the design of optical logic AND gate based on three structures, one of which is a hexagonal lattice with silicon (Si) rods in air (SRA) with air waveguide, another is the hexagonal lattice arrangement of air holes in silicon (AHS) with material waveguide and third one is the air holes in silicon with air waveguide. Optical AND gate has many applications, such as, AND logic gate is used to perform address recognition, packet-header modification, and data-integrity verification. AND gate also serves as a sampling gate in optical sampling oscilloscopes owing to their ultrafast operation compared to the traditional electrical methods. The proposed structures for the realization of AND logic gate is a line defect induced symmetric Y-branch waveguide. Earlier many applications have been realized on Y- shaped waveguide, such as, de-multiplexer [10, 57] and XOR logic gate [58]. The simulation results show that the proposed all optical photonic crystal waveguide structures could really function as AND logic gates. By appropriately choosing the size and the interaction length of the central rod in SRA structure and the size of the air hole at the centre of the Y shaped waveguide in AHS structure with material waveguide and AHS structure with air waveguide, the optimal performance for the proposed AND logic gates have been achieved.

2.2 Design and analysis of AND logic gates

AND logic gates on the platform of 2D PhC have been designed. The proposed structures consist of 15a ×15a arrangement of triangular lattices where ‘a’ denotes the lattice constant. The refractive index of Si has been taken as, n_{si} = 3.5. The selection of lattice constant and radius of rods/holes is based on the fact that the band gap exists for the wavelength of 1.55μm. In the proposed structures three waveguides have been considered. AND gate encompasses of two input signals and an output signal. The input signals are coming from the left lower and upper waveguides indicated as input port A and input port

B. Output signals are obtained from the right port of the horizontal waveguide indicated as output port Y. Due to the symmetric and linear waveguide structure, the input signal launched into either of the input waveguides gets distributed into the other two waveguides. Further, some part of the input signal is back reflected due to the presence of the central hole in the designed structure. However, when the input signal is launched into both the input waveguides, the two input signals interfere at the meeting point to yield the final output. The output for AND gate is logically '1' if and only if both of the input values are 1 otherwise it is logically 0. The transmittance (T) defined as the ratio of output intensity obtained from the output waveguide to the incident intensity at the input waveguides, i.e. $T = I_{out} / I_{in}$ has been calculated for all the proposed structures. The contrast ratio has also been calculated for all the proposed designs, i.e. Contrast Ratio= $10\log(P_1 / P_0)\ (dB)$, where P_1 represents power for logic-1 and P_0 represents power for logic-0. The response time [59-60] for the proposed logic gate structures has also been calculated. In the end comparison study among all the proposed designs for AND gate has been done.

2.2.1 AND logic gate based on AHS with material waveguide

2.2.1.1 Model and Operating principle

Firstly, all-optical AND logic gate using two dimensional triangular lattice of air holes in silicon with material waveguide has been designed as shown in figure 2.1. The radius of air holes is r = 0.4a, where 'a = 0.47μm' is the lattice constant in the considered PhC structure, whose photonic band gap has been calculated using the plane wave expansion (PWE) method.

A photonic band gap is defined as the gap between upper air band and lower dielectric band where electromagnetic modes are absent. The PWE method used to obtain the photonic band gap solves the eigen value equation of the designed structure formulated from the master equation as mentioned in chapter 1. It generates a set of eigen frequencies for a set of wave vectors which result into the dispersion relation. Figure 2.2 shows the dispersion band diagram of the designed structure in terms of normalized frequency and wave vector. Figure 2.2 shows a set of normalized frequency range (i.e. a/λ= 0.2440-

0.4038) between the lower and upper eigen modes for which the propagation of light is completely forbidden. This range of normalized frequency corresponds to the wavelength range 1.166 μm - 1.926 μm for transverse electric modes. To design the optical logic gate, linear waveguide has been created in the proposed structure in which light signal of frequency lying within the band gap range can propagate.

In the schematic indicated in figure 2.1 symmetric Y- shaped linear waveguide is formed and a hole is introduced at the centre of the three waveguides. For AND gate the radius of the central hole is optimized in such a way that for a single input signal as well as for both the input signals maximum power is obtained at the output port. Optimization of the structure is also carried out for increasing transmittance from output waveguide with respect to the wavelength.

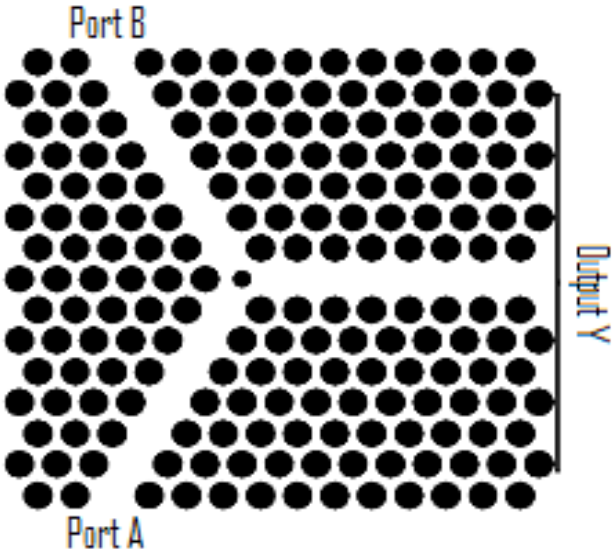


Figure 2.1 Schematic of all-optical AND logic gate based on AHS structure with material waveguide

The spectral response of proposed AND gate for TE like polarization of incident light from single input port and for both the input ports has been shown in figures 2.3 and 2.4. In figure 2.3, transmittance has been shown with respect to the wavelength when incident light is launched at one of the two input ports. Similarly, figure 2.4 represent transmittance with respect to the wavelength of incident light launched at both the input ports. The contrast ratio has been calculated for the proposed structure as shown in figure

2.5. Figure 2.5 shows the variation of contrast ratio with respect to the wavelength. Figures 2.3, 2.4 and 2.5 clearly show that the optimized structure can be best worked out at the normalized operating wavelength of 1.55μm which lies in optical communication range.

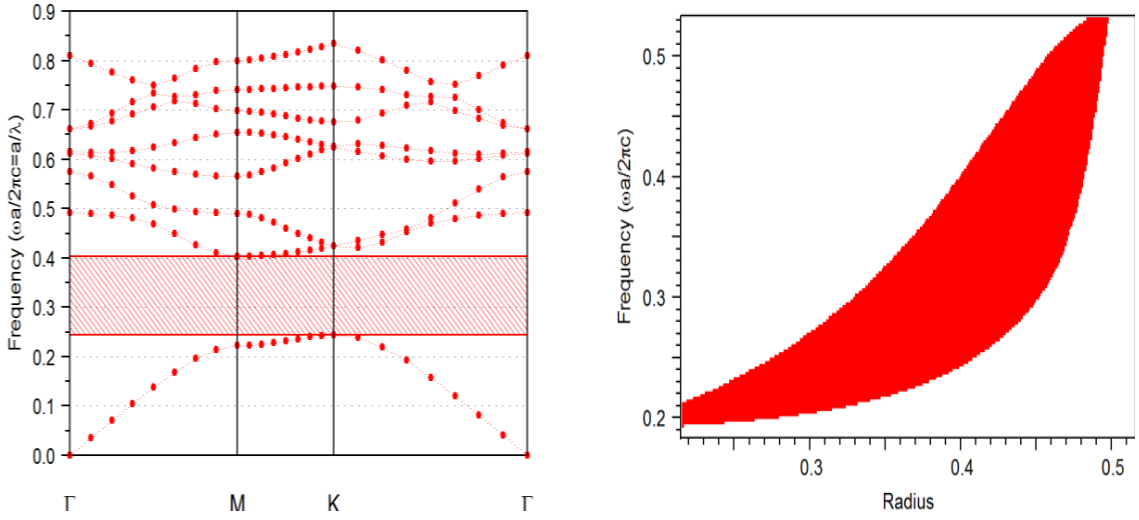


Figure 2.2 Band gap of the photonic crystal structure composed of air holes in silicon with material waveguide

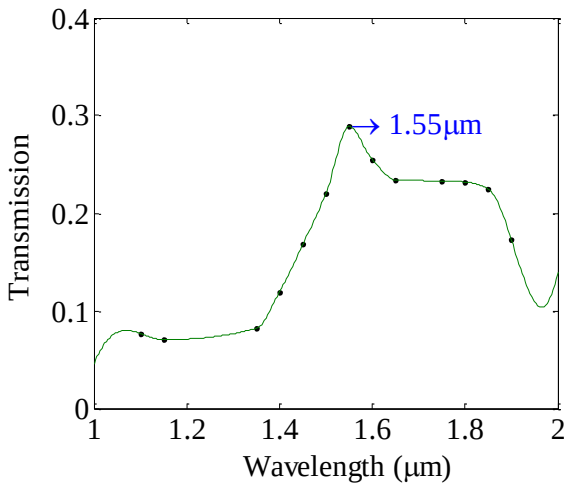


Figure 2.3 Variation of transmittance with wavelength from the output waveguide for the single input signal for TE like polarization of incident light

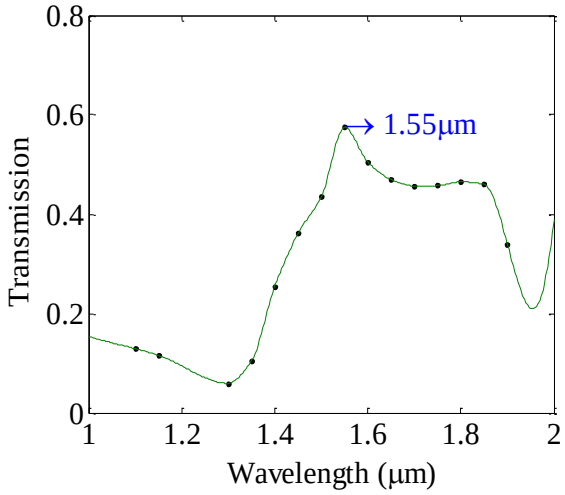


Figure 2.4 Variation of transmittance with wavelength from the output waveguide for both the input signals for TE like polarization of incident light

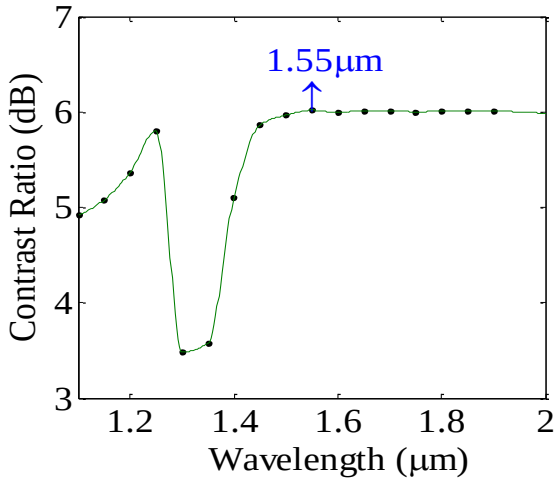


Figure 2.5 Contrast ratio versus the normalized operating wavelength

2.2.1.2 Optimization of the radius of the air hole at the centre of the three waveguides

To obtain the optimized value of the radius of the air hole at the centre of three waveguides, the radius of all the other air holes has been taken as r = 0.4a. The radius of central air hole has been scanned when one of the input signals as well as both the input signals are 1. Figure 2.6 indicates that, as the radius of central air hole increases, the output power increases to a maximum value for both the input signals as well as for the single input signal. From the figure 2.6 it is evident that as the value of radius is increased beyond 0.25a power at the output port goes on decreasing. Hence, the radius of air hole at the centre has been taken as r_c = 0.25a.

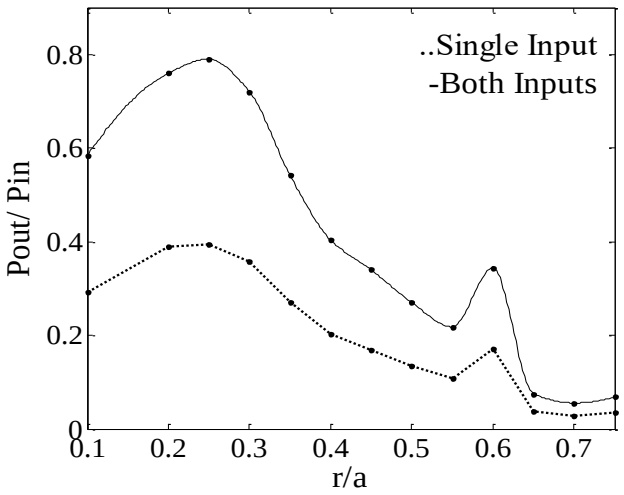


Figure 2.6 Power transmittance versus normalized radius of the central air hole at the centre of the three material waveguides in AHS structure

2.2.1.3 Results and discussion for AHS with material waveguide based AND optical logic gate

The proposed optimized structure with optimized parameters, r_c = 0.25a and r = 0.4a has been simulated using finite difference time domain method and the input ports have been excited by continuous wave sources with power P_a. For simulation and optimization of the structure as shown in figure 2.1, FDTD method with perfectly matched boundary conditions has been employed to absorb waves and avoid reflections at the boundaries. The magnetic field polarization of the wave has been chosen to be parallel to the y-axis, which is the axis of air holes in Si and the wave propagates in the (x, z) plane. Convergence of the simulations has been done according to the given rule, i.e. $\Delta x < \lambda/10$ and $\Delta z < \lambda/10$ where x and z axes are the horizontal and vertical direction coordinates and the axis of holes is along y direction. The space grid and the time grid have been chosen such that the structure meets the requirement of courant condition which is given by the equation $c\Delta t < 1/\sqrt{\Delta x^{-2} + \Delta z^{-2}}$, where c is the speed of light in medium. Firstly, we have applied continuous wave signal at port A and B separately and then simultaneously at both the input ports A and B with power P_a. It has been found out that output power is 0.395 P_a for separate excitation with power P_a at input port A as well as for separate excitation at input port B. For simultaneous excitation with power P_a at both input ports A and B the output power obtained is 1.580 P_a. Thus the system performs as an AND gate as summarised in table 2.1.

Table 2.1 Truth table for AND logic gate based on AHS structure with material waveguide, where output Y is in terms of input power P_a

AND GATE			
Input A	Input B	Logic output	Output Y
0	0	0	0
0	1	0	0.395 P_a
1	0	0	0.395 P_a
1	1	1	1.580 P_a

Table 2.1 shows the truth table for the proposed optical AND logic gate based on AHS structure with material waveguide. From figure 2.5 it has been found that the contrast ratio between logic-1 output power and logic-0 output power is 6.017dB at the normalized operating wavelength λ=1.55μm which lies in the optical communication range. The field distribution at steady state for all combinations has been shown in figure 2.7, which exhibits the operation of the proposed structure of an AND gate.

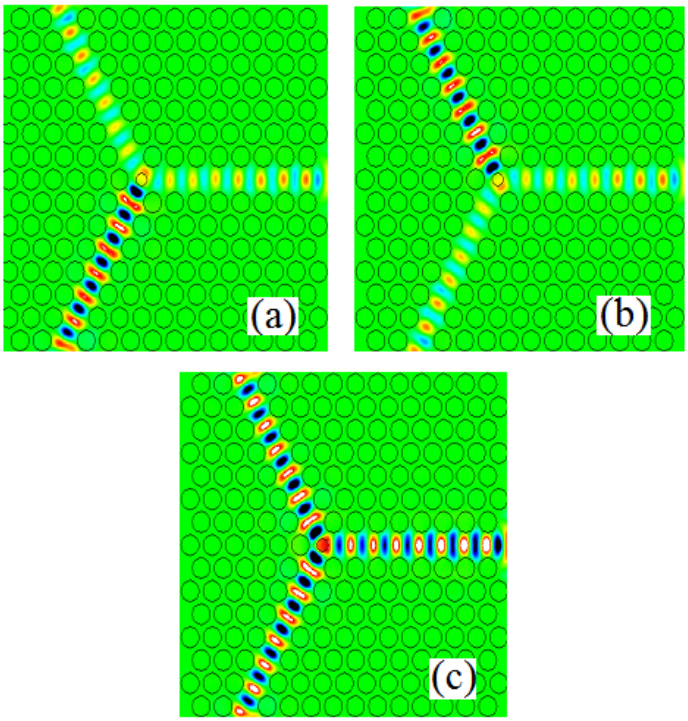


Figure 2.7 Field distributions at steady state of the AND logic gate based on AHS structure with material waveguide for (a) A=1, B=0 (b) A=0, B=1 (c) A=1, B=1

The response time of the optimized optical AND logic gate has been determined using the time evolving curve of the output power [60] as shown in figure 2.8. Figure 2.8 shows that the time for the output power to reach from 0 to 90% of the average output power (P_{av}) in the final steady state is ct=54.1μm or t=0.63 ps. The time 't' consists of two parts one of which is time due to transmission delay i.e. t_1=0.330 ps and another is the time for the output power to climb from 0.1% P_{av} to 90% P_{av} is found to be t_2 =0.301 ps. As the system operates on linear material, hence it is expected that the falling time from average output power i.e. P_{av} to 10% P_{av} is approximately equal to t_2. Thus a narrow pulse with a width of $2t_2$=0.602 ps can be produced. Hence, the response period of the signal is

obtained to be 1.204 ps, i.e. the proposed AND logic gate can operate at a bit rate of 0.830 Tbits/s.

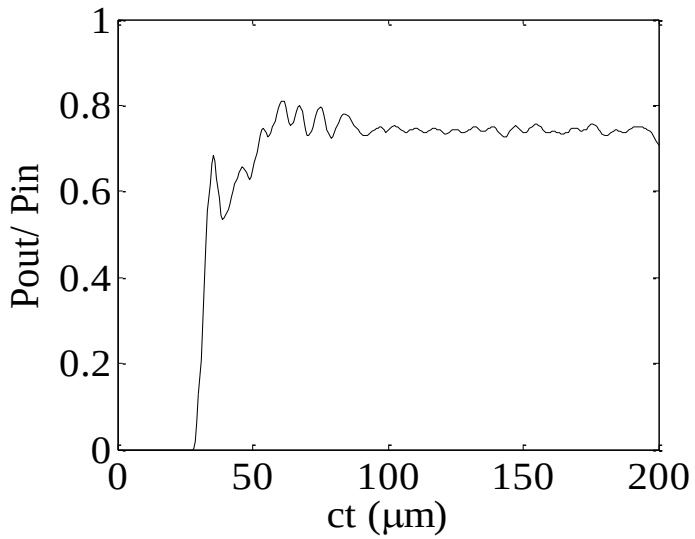


Figure 2.8 Time evolving curve of the output power for AHS structure with material waveguide

2.2.2 AND logic gate based on AHS with air waveguide

2.2.2.1 Model and Operating principle

The second type of AND gate has been designed using triangular lattice of air holes in Si with air waveguides as shown in figure 2.9. The lattice constant, 'a = 0.47μm' and radius of air holes, r = 0.4a has been chosen so that a large band gap for a wavelength range of 1.166μm-1.924μm for TE polarization is obtained as shown in figure 2.10.

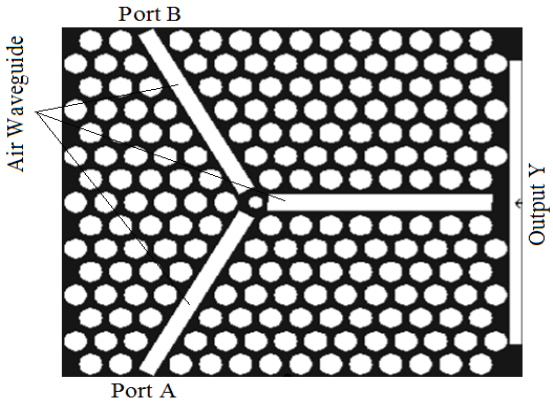


Figure 2.9 Schematic of all-optical AND logic gate for air holes in silicon with air waveguide

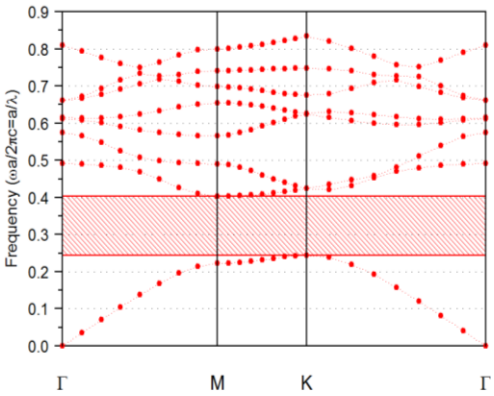


Figure 2.10 Band gap of the photonic crystal structure composed of air holes in silicon with air waveguide

In the proposed design three air waveguides have been created and a hole has been introduced at the centre of the waveguides as shown in figure 2.9. The spectral response has also been calculated for AHS structure with air waveguide as done for the AHS structure with material waveguide. The spectral response for the proposed AND gate for TE like polarization of incident light for single input as well as for both the inputs for AHS structure has been shown in Figures 2.11 and 2.12, respectively. Figures 2.11 and 2.12 clearly show that the optimized structure can be best worked out at the normalised operating wavelength λ=1.55μm.

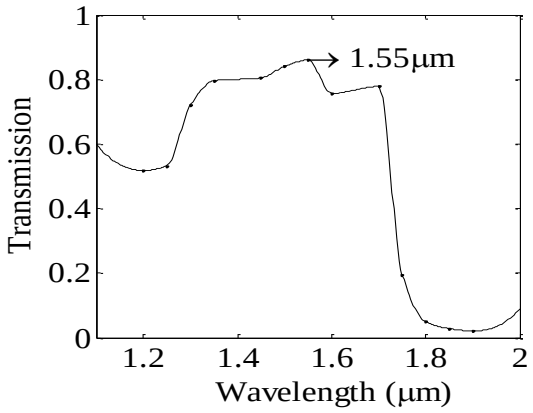


Figure 2.11 Variation of transmittance with wavelength from the output waveguide for the single input signal for TE like polarization of incident light

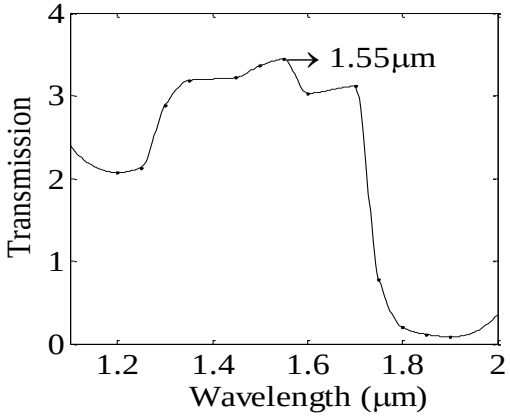


Figure 2.12 Variation of transmittance with wavelength from the output waveguide for both the input signals for TE like polarization of incident light

2.2.2.2 Optimization of the radius of the air hole at the centre of the three air waveguides

The radius of the air hole at the centre of the three waveguides has been optimized in such a way that for a single input launch as well as for both the input launches, maximum power is obtained at the output port. To optimize the radius of the central air hole, the radius of all the other air holes is initially set equal to 0.4a and then the ratio of output power to the input power has been calculated at different values of the radius of the central air hole as shown in figure 2.13. For AHS structure with air waveguide, the radius of central air hole in the Y shaped air waveguides has been optimized to be r_c = 0.25a.

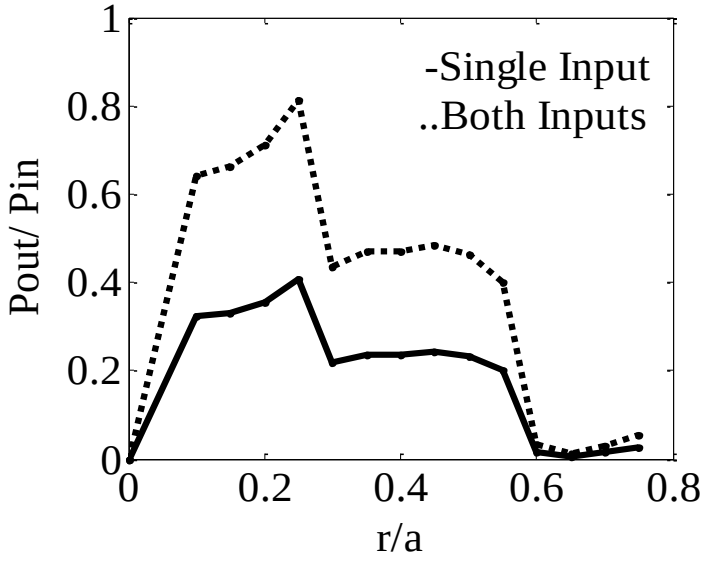


Figure 2.13 Power transmittance versus the normalized radius for air hole at the centre of the three air waveguides in AHS structure

2.2.2.3 Results and Discussion for AHS with air waveguide based AND optical logic gate

In the optimized structure, initially continuous wave signal has been launched at input port A and B separately and then simultaneously at both the input ports A and B with power P_a. It has been found that the output power obtained is 0.406 P_a for separate excitation with power P_a at input port A as well as for separate excitation at input port B. For simultaneous excitation with power P_a at both input ports A and B the output power obtained is 1.624 P_a. Thus the system performs as an AND optical logic gate as summarised in table 2.2. Table 2.2 shows the truth table for the proposed optical AND logic gate based on AHS structure with air waveguide. The contrast ratio between logic-1 output power and logic-0 output power is 3.003dB at the normalized operating wavelength of λ=1.55μm. The field distribution at steady state for all combinations has been shown in figure 2.14 which exhibits the operation of the proposed structure of an AND gate.

Table 2.2 Truth table for AND logic gate based on AHS structure with air waveguide, where output Y is in terms of input power P_a

AND GATE			
Input A	Input B	Logic output	Output Y
0	0	0	0
0	1	0	0.406 P_a
1	0	0	0.406 P_a
1	1	1	1.624 P_a

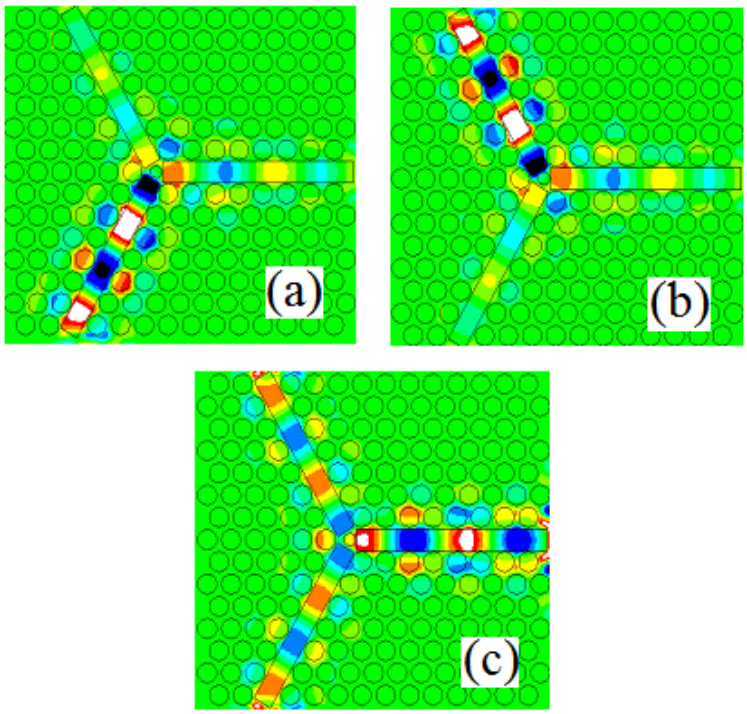


Figure 2.14 Field distributions at steady state of the AND logic gate based on AHS structure with air waveguide for (a) A=1, B=0 (b) A=0, B=1 (c) A=1, B=1

The response time of the optimized AHS structure with air waveguide has been calculated by plotting the time evolving curve of the output power as done for the AHS structure with material waveguide. From figure 2.15, it has been concluded that the time for the output power to reach from 0 to 90% of the average output power (P_{av}) in the final steady state is ct=53.1μm or t=0.17 ps. The time 't' consists of two parts one of which is time due to transmission delay i.e. t_1=0.03 ps and another is the time for the output power

to climb from 0.1% P_{av} to 90% P_{av} is found to be t_2 =0.14 ps. As the system operates on linear material, hence it is expected that the falling time from average output power (P_{av}) to 10% P_{av} is approximately equal to t_2. Thus a narrow pulse with a width of $2t_2$=0.28 ps can be produced. Hence, the switching period of the signal is obtained to be 0.56 ps, i.e. the proposed AND logic gate can operate at a bit rate of 1.785 Tbits/s.

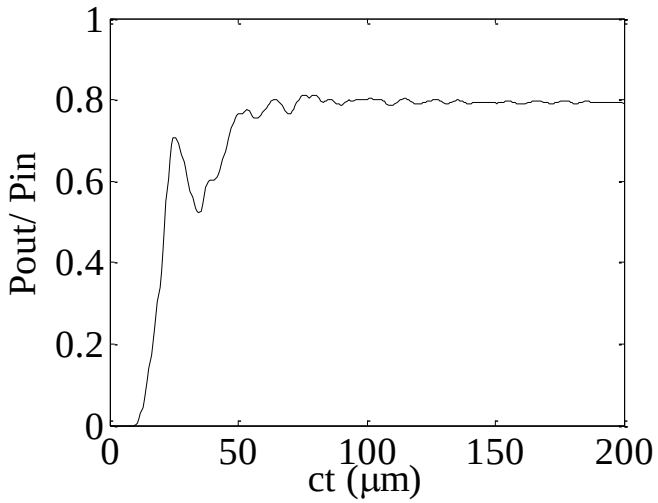


Figure 2.15 Time evolving curve of the output power for AHS structure with air waveguide

2.2.3 AND logic gate based on SRA structure with air waveguides

2.2.3.1 Model and Operating principle

Lastly, the optical logic AND gate using triangular lattice of Si rods in air has been designed as shown in figure 2.16. The radius of Si rods has been taken as r = 0.18a, where 'a = 0.56μm' is the lattice constant. According to the band diagram as shown in figure 2.17 of the designed structure calculated using plane wave expansion (PWE) method, light with wavelength range of 1.177μm - 1.933μm for TM modes cannot pass through the uniform PhC structure and thus is completely reflected. In the schematic diagram shown in figure 2.16 symmetric Y- shaped waveguide is formed and a rod is introduced at the centre of the three waveguides. For the proposed structure the transmittance has been calculated. The spectral response for the proposed AND gate for TM like polarization of incident light for single input as well as for both the inputs has been shown in Figures 2.18 (a) and 2.18 (b), respectively. Figures 2.18 (a) and 2.18 (b) clearly indicate that the optimized structure can be best worked out at the normalized operating wavelength of λ=1.55μm.

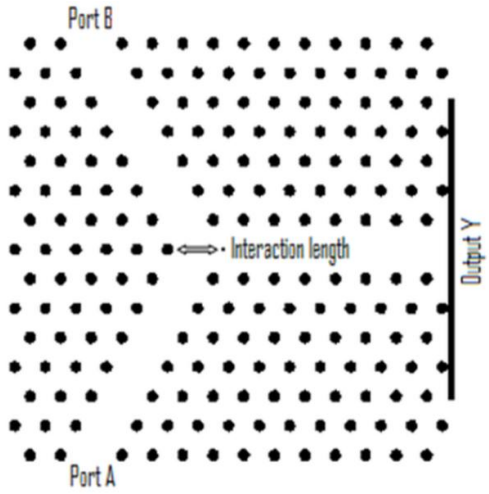


Figure 2.16 Schematic of all-optical AND logic gate for Si rods in air

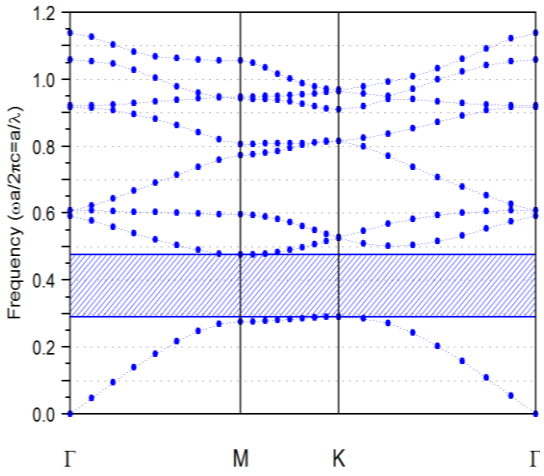


Figure 2.17 Band gap of the photonic crystal structure composed of Si rods in air

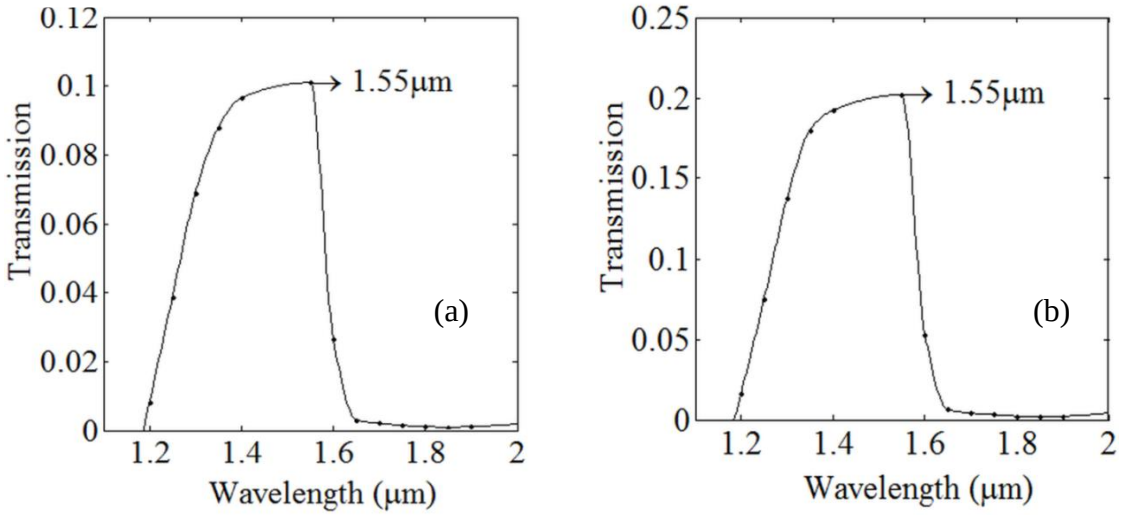


Figure 2.18 Variation of transmittance with wavelength from the output waveguide for (a) the single input signal for TM like polarization of incident light and (b) for both the input signals for TM like polarization of incident light

2.2.3.2 Optimization of the radius of the Si rod at the centre of the three air waveguides

The radius and the interaction length of the central rod has been optimized in such a way that for a single input launch as well as for both the input launches maximum power has been obtained at the output port. To optimize the radius of the central rod, the radius of all

other rods is initially set equal to 0.18*a* and then the ratio of output power to the input power has been calculated at different values of the radius of the central rod as shown in figure 2.19. Similarly the interaction length of the central rod has been optimized (shown in figure 2.20) while keeping the radius of all the other rods as 0.18*a* and the radius of the central rod as 0.05*a*. Hence, after the optimization, the radius (r_c) and interaction length (L) of the central rod has been taken as r_c = 0.05a and L = 1.875a, respectively, where 'a' is the lattice constant.

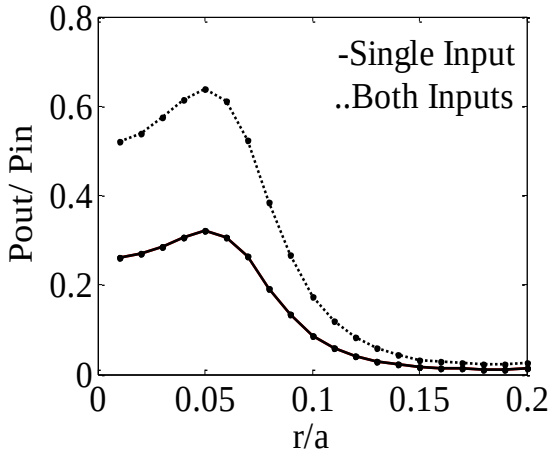


Figure 2.19 Power transmittance versus the normalized radius of the central rod

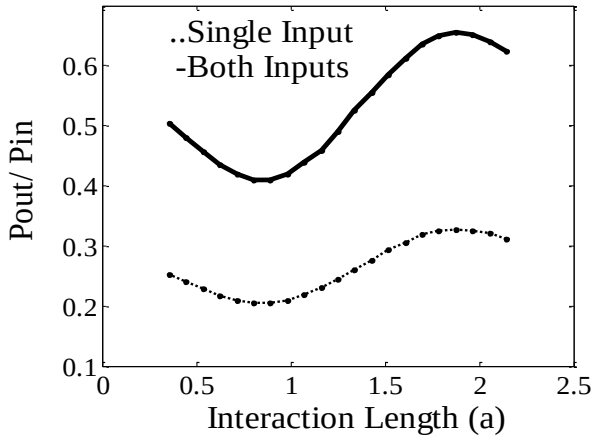


Figure 2.20 Power transmittance versus the normalized interaction length of the central rod

2.2.3.3 Results and discussion for SRA structure

After the optimization of the designed structure to work as an AND gate, results have been realized for single input launch as well as for both input launches with power P_a. It has been found that the output power is 0.328 P_a for separate excitation with power P_a at input port A as well as for separate excitation at input port B. The power obtained at the output port is 1.310 P_a for simultaneous excitation with power P_a at both input ports A and B. Thus the system performs as an AND optical logic gate as summarised in table 2.3. Table 2.3 shows the truth table for the proposed optical AND logic gate based on SRA structure with air waveguide. The contrast ratio between logic-1 output power and logic-0 output power is 3.009dB at the normalized operating wavelength of λ=1.55μm. The field distribution at steady state for all combinations has been shown in figure 2.21, which exhibits the operation of the proposed structure as an AND optical logic gate.

Table 2.3 Truth table for AND logic gate based on SRA structure where output Y is in terms of input power P_a

AND GATE			
Input A	Input B	Logic output	Output Y
0	0	0	0
0	1	0	0.328 P_a
1	0	0	0.328 P_a
1	1	1	1.310 P_a

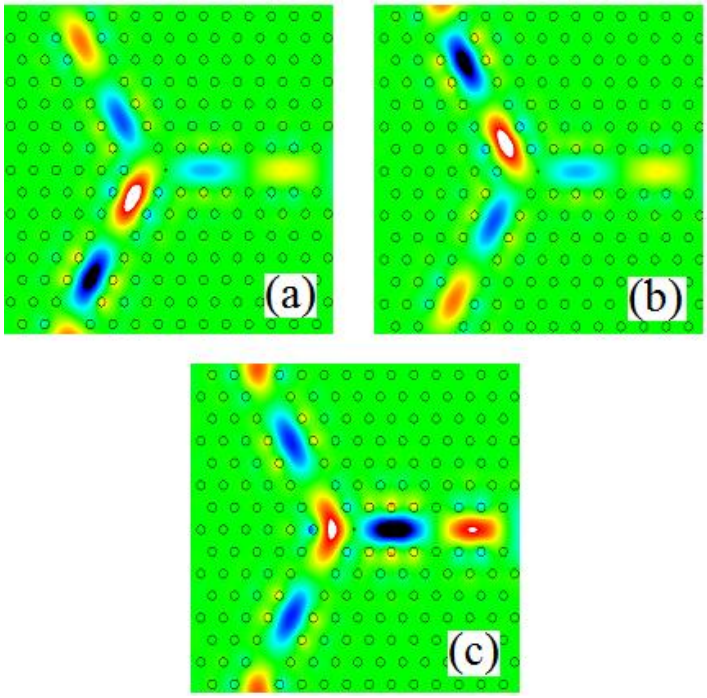


Figure 2.21 Field distributions at steady state of the AND logic gate based on SRA structure for (a) A=1, B=0 (b) A=0, B=1 (c) A=1, B=1

The response time for the designed structure has also been calculated in a similar manner as done in for AHS structures. The response time of the optimized structure has been calculated by plotting the time evolving curve of the output power as shown in figure 2.22. From figure 2.22, it has been concluded that the time (t) for the output power to climb from 0 to 90% of the average output power (P_a) in the final steady state consists of two parts one of which is the time due to transmission delay i.e. t_1 = 0.05 ps and another is t_2 = 0.124 ps i.e. the time for the output power to climb from 0.1% P_a to 90% P_a. Hence

from figure 2.22, ct = 52.1μm or t = 0.17ps. For linear materials, it has been expected that the falling time from P_a to 10% P_a is approximately same i.e. equal to t_2. So, a narrow pulse of width $2t_2$ = 0.248 ps for the proposed AND logic gate can be produced. The switching period of the signal is 0.496 ps when the OFF and ON time are same and the proposed AND gate can operate at a bit rate of 2.016 Tbit/s.

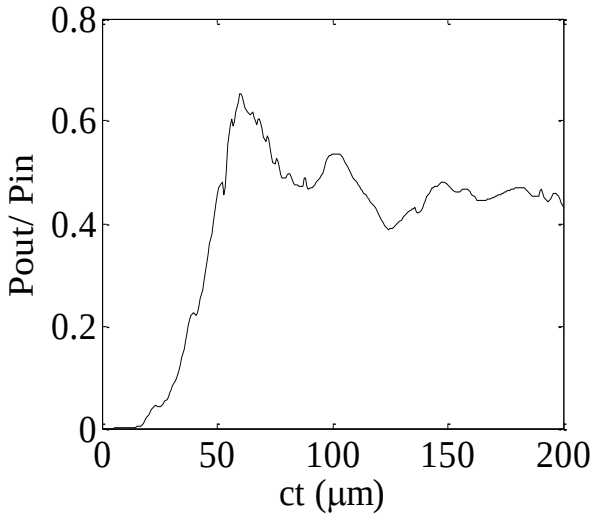


Figure 2.22 Time evolving curve of the output power for SRA structure

The redistribution of energy takes place in the designed structures. It has been observed that when input signal is launched into either of the input waveguides then 20% of energy is reflected back to the input waveguide due to the presence of a hole/rod at the centre of the three waveguides whereas remaining 80% gets distributed among the two other waveguides. However, when both input signals are launched into the input waveguides then 80% of the total energy is obtained at the output port and rest 20% is reflected back to the input waveguides. Hence, the overall energy remains conserved. Further, it has been concluded that the logic operation is purely linear.

2.3 Comparison study of AND optical logic gates

After the designing of AND optical logic gate using three structures, a comparison between the three designs has been done. The results of all the three designs have been mentioned in table 2.4 for the comparison. From table 2.4 it has been concluded that the best structure in terms of response period and bit rate is SRA structure with air waveguide, whereas in terms of contrast ratio the best structure is AHS structure with material waveguide. But

both the structures have their own draw backs such as SRA structure is a freely suspended structure and is mechanically unstable from practical perspective and not suitable for future integrated circuits, whereas AHS structure with material waveguide have material loss due to which the values of bit rate and response time are less. Hence, AHS structure with air waveguide is best suitable structure which overcomes the material losses as the waveguide is air instead of Si and is suitable from the fabrication point of view.

Table 2.4 Comparison between three structures

Results	SRA with air waveguide	AHS with air waveguide	AHS with material waveguide
Contrast ratio (dB)	3.003	3.009	6.017
Response time (ps)	0.496	0.560	1.204
Bit rate (Tbit/s)	2.016	1.785	0.830

2.4 Conclusion

In this chapter, the designs for all optical AND logic gates employing (i) air holes in silicon with material waveguide, (ii) air holes in silicon with air waveguide and (iii) silicon rods in air with air waveguide based on Y-shaped photonic crystal architecture have been proposed. The device performance has been analysed by PWE method and FDTD method. The method of determining the operating parameters has been explained and the optimized parameters are obtained for achieving high contrast ratio. A comparison study has been done among all the designs to work out the best design for optical AND logic gate. In this chapter, the designs of the AND optical logic gates are based on linear characteristics of the material and hence it can operate at very low powers. It is expected that such designs will help in realizing devices and components for broad band optical communication systems and networks. The proposed structures could be the strong candidate for future photonic crystal based all optical logic gates.

CHAPTER 3

Realization of all-optical logic gates in photonic crystal waveguide[2]

3.1 Introduction

In chapter 2, different designs for AND optical logic gates have been demonstrated and it has been studied that the logic gates play a basic, critical and important part in modern electronics and integrated circuits, due to their importance in addressing, switching, encryption, data encoding, signal regeneration, header recognition and contention resolution. In recent years different schemes have been demonstrated for the designing of all optical logic gates based on linear optical effects such as, interferometry [61], semiconductor optical amplifier (SOA) [62] and Mach-Zehnder interferometer (MZI) [63] and nonlinear processes which include electro-optical effect [64,65], thermal-optical effect [66], two-photon absorption [67] and third-order nonlinear effect [43,53]. Logic gates are capable of performing many logic functions and have numerous applications in optical communication, such as, AND logic gate is used to perform address recognition, packet-header modification, and data-integrity verification and also serves as a sampling gate in optical sampling oscilloscopes. XOR gate can perform functions like comparison of data patterns for address recognition, packet switching, data encryption/decryption, parity checking and optical generation of pseudorandom patterns. NOT gate can be used as inverter or switch and XNOR logic gate is used to realize the threshold detector functionality.

In this chapter, we have proposed the design of all optical logic gates based on two dimensional photonic crystals composed of triangular lattice of air holes in Si. Earlier

[2] Part of the results reported in this chapter has been published in the paper: "Design of all optical logic gates in photonic crystal waveguides", Optik 126, pp. 950–955, 2015. http://dx.doi.org/10.1016/j.ijleo.2015.03.003

various logic gate designs have been proposed which consist of Si rods in air [52, 68-70] but those designs are not practical from the point of view of sustainability and fabrication. Photonic crystal composed of air holes in silicon is a more practical structure and has been used in the design of optical logic gates [71, 72] and nano photonic devices [8,10]. The proposed optical logic gates are based on the phenomenon of optical interference effect and are designed in two dimensional photonic crystal waveguides composed of air holes in silicon. The designed waveguides are linear in nature and the overall energy remains conserved. The simulation results show that the proposed all optical photonic crystal waveguide structure could really function as all optical logic gates. By appropriately choosing the size of the air hole at the centre of the four PhC waveguides, the optimal performance in terms of response time, bit rate and contrast ratio for the proposed optical logic gates has been obtained.

3.2 Structure design and operating principle of all-optical logic gates

The design for all optical logic gates based on the platform of 2D PhC has been proposed. The proposed two dimensional photonic crystal structure, as shown in figure 3.1 consists of 15a ×15a two dimensional triangular lattice composed of air holes in silicon having refractive index, n=3.5. The radius (r) of air holes is 0.3a, where, ‘a’ is the lattice constant equal to 0.352μm. According to the band diagram of the bulk PhC as shown in figure 3.2, light with wavelength range of 1.291μm-1.715μm for TE modes cannot pass through the uniform PhC structure. Four waveguides have been created in the proposed design, out of which two waveguides have been considered as input ports indicated as port A and port B. As shown in figure 3.1, one port has been indicated as reference port R which is used to create phase difference between input signals resulting into constructive or destructive interference. Output signals are obtained from the right port indicated as output port Y.

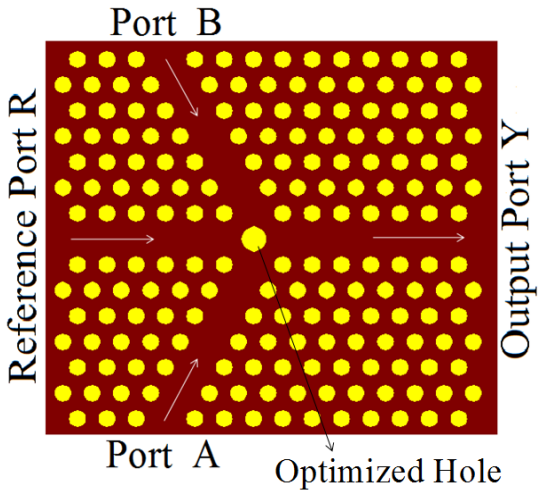


Figure 3.1 Schematic representation of all-optical logic gates

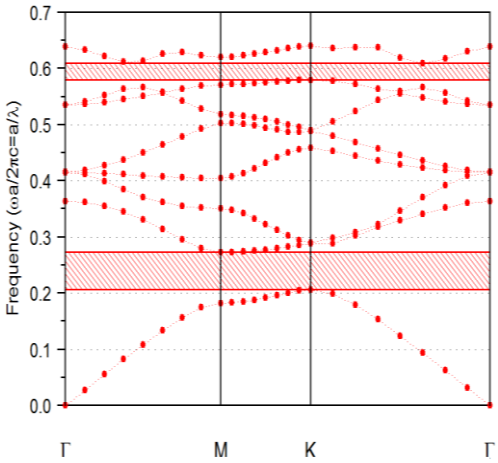


Figure 3.2 Band gap of the photonic crystal structure composed of air holes in silicon

Further, a hole has been introduced at the centre of the four waveguides. For the design of all optical logic gates the radius of the central hole is optimized in such a way that for a single input (along with reference signal) as well as both the inputs (along with the reference signal) maximum power is obtained at the output port Y. The transmittance (T) has been calculated for the proposed structure. The spectral response of proposed logic gates for TE like polarization of incident light from single input port (along with reference signal) as well as for both the input ports (along with the reference signal) has also been shown in figures 3.3 and 3.4. Figure 3.3 shows the transmittance with respect to the wavelength when the incident light is launched at one of the two input ports along with the reference signal having same phase angle as that of the input signal. Similarly, figure 3.4 represents the transmittance with respect to the wavelength of incident light launched at both the input ports along with the reference signal having same phase angle as that of the input signals. The contrast ratio has also been calculated for all optical logic gates. Figure 3.5 shows the defect modes that exist within the band gap range. From figures 3.3, 3.4 and 3.5, it has predicted that the optimized structure can be best worked out at the normalized operating wavelength of 1.55μm which lies in optical communication range. For the proposed structure, the response time has also been calculated from the time evolution curve as mentioned in [59, 60].

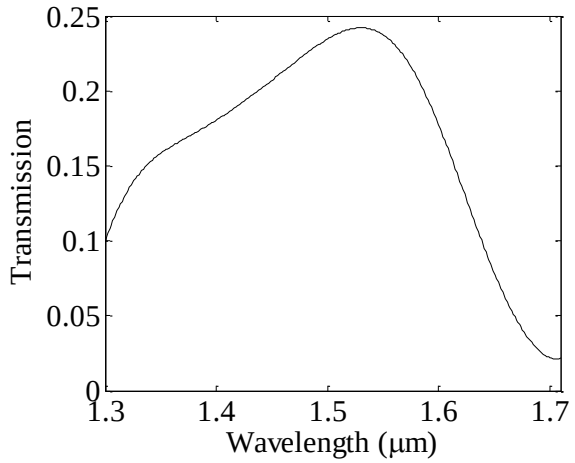


Figure 3.3 Variation of transmittance with wavelength from the output waveguide for the single input signal along with the reference signal for TE like polarization of incident light

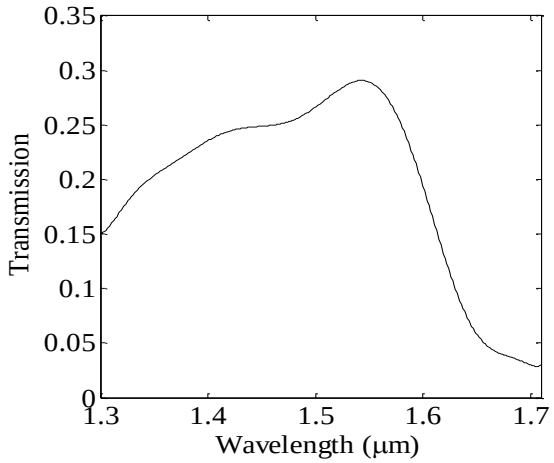


Figure 3.4 Variation of transmittance with wavelength from the output waveguide for both the input signals along with the reference signal for TE like polarization of incident light

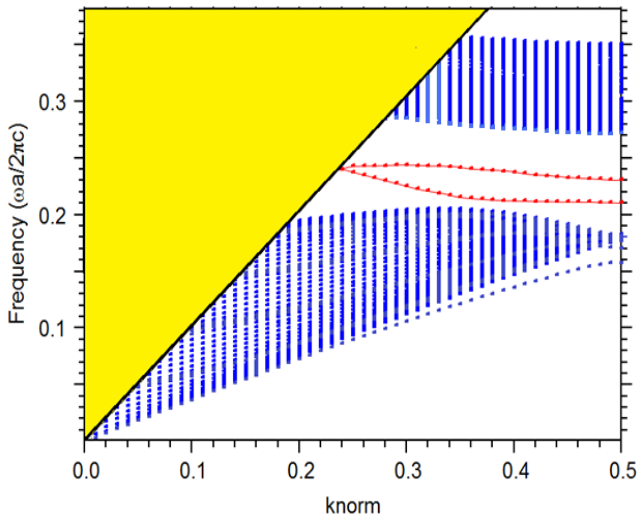


Figure 3.5 Dispersion relation for all the four involved PhC waveguides. The black solid line corresponds to the light line and the red dotted lines inside the band gap region correspond to the respective guided modes for TE polarization in all the waveguides.

3.3 Optimization of the radius of the hole at the centre of the four waveguides

The radius of central hole has been optimized when one of the input signals as well as both the input signals, along with the reference signal are unity and has zero phase difference. From the optimization curve for the radius of the central hole as shown in figure 3.6, it has been observed that as the radius of the central hole increases, the output power increases to a maximum value and then decreases for both the input signals as well as for the single input signal along with the reference signal. Hence, the optimized radius of the air hole at the centre of four waveguides has been taken as $r_c = 0.44a$.

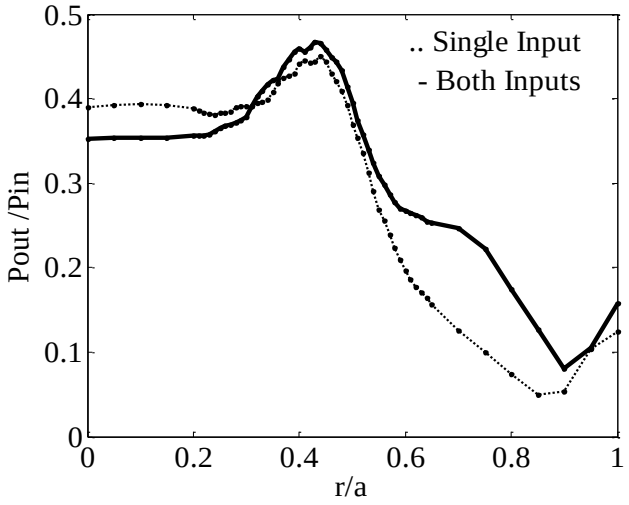


Figure 3.6 Normalized power transmittance versus the normalized radius of the central hole at the centre of the four PhC waveguides

3.4 Results and discussion

After the optimization of the proposed structure to operate as all optical logic gates, results have been realized using FDTD method with perfectly matched layer (PML). The input ports A, B and reference port (R) for single input launch as well as for both input launches have been excited by continuous wave (CW) signal with power P_o. Reference signal has been used to optimize the logic output of all the logic gate combinations. For the realization of all the logic gates the radius of central hole has been taken as $r_c = 0.44a$ and the radius of all the other holes as $r = 0.3a$.

3.4.1 For AND gate

Firstly the function of optical logic AND gate has been demonstrated using the initial values of the optimized parameters i.e. r_c = 0.44a and r = 0.3a. The AND gate encompasses of two input signals, a reference signal and an output signal. The AND logic gate operates as follows: (i) when input port A is launched with light having phase angle $\phi = 0^0$ and reference port with light having phase angle $\phi = 180^0$ then logic '0' is obtained at the output port Y. (ii) similarly, when input port B is launched with light having phase angle $\phi = 0^0$ and reference port with light having phase angle $\phi = 180^0$ then also logic '0' is obtained at the output port Y. (iii) when both the input ports A and B are excited with light signals having phase angle $\phi = 0^0$ and reference port with light also having phase angle $\phi = 0^0$ then logic '1' is obtained at the output port Y. The results are summarized in table 3.1 and field distributions for all possible combinations have been shown in figure 3.7. It has been predicted that the AND gate can operate at a wavelength of 1.55μm and the calculated value of contrast ratio is found to be 8.76 dB.

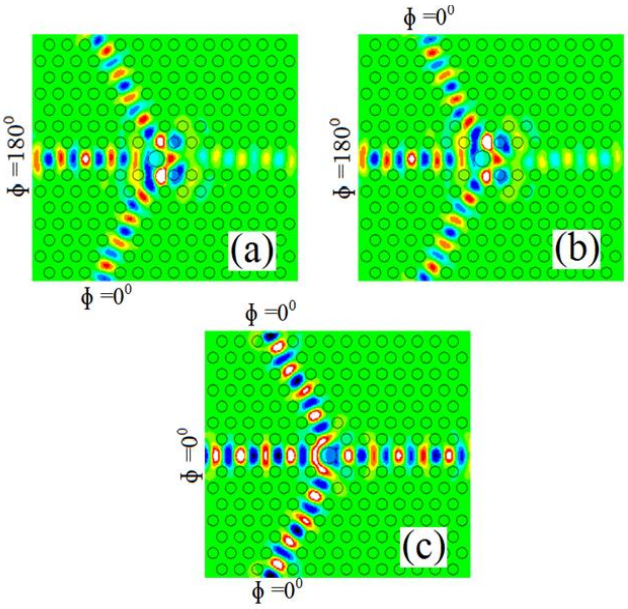


Figure 3.7 Field distributions at steady state of the AND logic gate for (a) A=1, B=0, R=1 (b) A=0, B=1, R=1 (c) A=1, B=1, R=1

Table 3.1 Truth table for AND logic gate where output Y is in terms of input power P_o

AND GATE				
Input A ($\phi = 0^0$)	Input B ($\phi = 0^0$)	Reference signal (R)	Logic output	Output Y
0	0	0	0	0
0	1	1($\phi = 180^0$)	0	0.1719 P_o
1	0	1($\phi = 180^0$)	0	0.1719 P_o
1	1	1($\phi = 0^0$)	1	0.4663 P_o

3.4.2 For OR gate

After the optimization of all the required parameters OR gate has been demonstrated. For OR gate the output is '0' if and only if both the input values are '0' otherwise output values are '1'. The operation of OR gate is as follows: (i) when input port A is launched with light having phase angle $\phi = 0^0$ and reference port with light also having phase angle $\phi = 0^0$ then logic '1' is obtained at the output port Y. (ii) similarly, when input port B is launched with light having phase angle $\phi = 0^0$ and reference port with light also having phase angle $\phi = 0^0$ then also logic '1' is obtained at the output port Y. (iii) when both the input ports A and B are excited with light signals having phase angle $\phi = 0^0$ and reference port with light also having phase angle $\phi = 0^0$ then logic '1' is obtained at the output port Y. The presence of same phase angle between the input signals and reference signal leads to the constructive interference, which helps to satisfy the logic output of the OR gate. The field distribution at steady state as shown in figure 3.8 and truth table 3.2 clearly show that the proposed structure can function as an OR logic gate.

Table 3.2: Truth table for OR logic gate where output Y is in terms of input power P_o

OR GATE				
Input A ($\phi = 0^0$)	Input B ($\phi = 0^0$)	Reference signal (R)	Logic output	Output Y
0	0	0	0	0
0	1	1($\phi = 0^0$)	1	0.4497 P_o
1	0	1($\phi = 0^0$)	1	0.4497 P_o
1	1	1($\phi = 0^0$)	1	0.4663 P_o

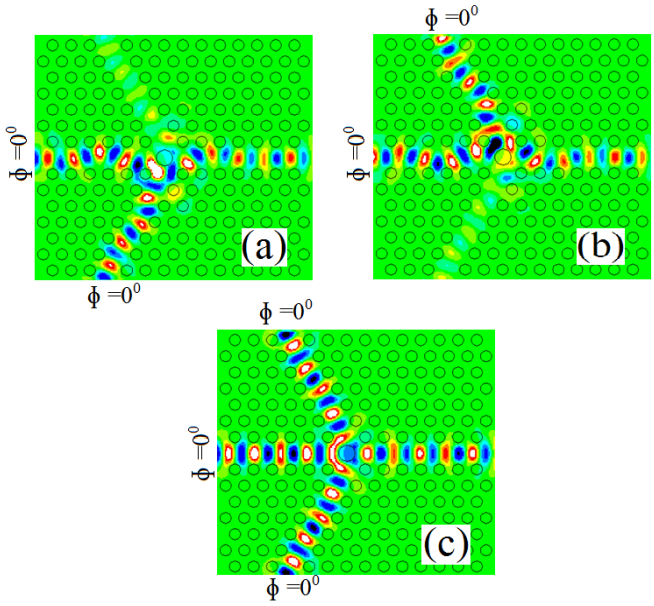


Figure 3.8 Field distributions at steady state of the OR logic gate for (a) A=1, B=0, R=1 (b) A=0, B=1, R=1 (c) A=1, B=1, R=1

3.4.3 For XOR gate

The output in XOR logic gate is logically '1' if only one of the two inputs is high (1) and logically '0' if both the inputs are high (1) or low (0). The working of XOR logic gate has been explained as follows: (i) when none of the input signals has been launched at the input ports A and B along with the zero signal at the reference port R, the output obtained at the output port Y is logically '0'. (ii) When any of the input ports A and B has been launched

with a signal having phase angle $\phi = 0^0$ along with the reference signal having same phase angle $\phi = 0^0$ then the output obtained at the output port Y is logically '1'. (iii) When both the input ports have been excited with the light signal having phase angle $\phi = 0^0$ and reference port with the light having phase angle $\phi = 180^0$ output obtained at the output port is logically '0'. The simulation figure 3.9 and the logic output values mentioned in table 3.3 show that the proposed structure could operate as XOR logic gate. The calculated value of contrast ratio for XOR logic gate has been found to be 8.49 dB.

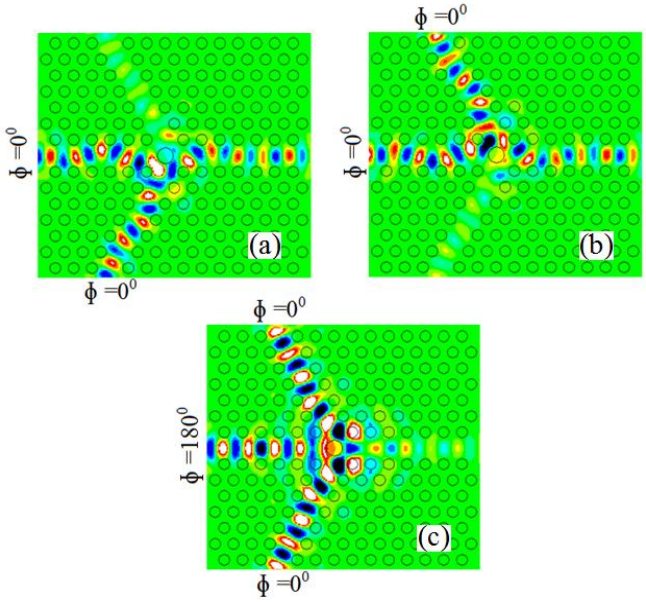


Figure 3.9 Field distributions at steady state of the XOR logic gate for (a) A=1, B=0, R=1 (b) A=0, B=1, R=1 (c) A=1, B=1, R=1

Table 3.3: Truth table for XOR logic gate where output Y is in terms of input power P_o

XOR GATE				
Input A ($\phi = 0^0$)	Input B ($\phi = 0^0$)	Reference signal (R)	Logic output	Output Y
0	0	0	0	0
0	1	1($\phi = 0^0$)	1	0.4497 P_o
1	0	1($\phi = 0^0$)	1	0.4497 P_o
1	1	1($\phi = 180^0$)	0	0.0905 P_o

3.4.4 For NOT gate

The NOT gate design is like an inverter in which output is inverse of the input. In the proposed structure one input has been taken at the input port A, and a reference port R. When input signal is launched at the input port A with phase angle $\phi = 0^0$ and a reference signal with phase angle $\phi = 180^0$ then the output obtained at the output port Y is logically '0' and logically '1' when no input signal is launched at the input port but only reference signal is launched with phase angle $\phi = 180^0$. The contrast ratio for NOT gate is 5.42 dB. The table 3.4 and field distribution as shown in figure 3.10 clearly indicate that the proposed structure can be used as a NOT gate.

Table 3.4: Truth table for NOT logic gate where output Y is in terms of input power P_o

NOT GATE			
Input A ($\phi = 0^0$)	Reference signal (R)	Logic output	Output Y
0	1($\phi = 180^0$)	1	0.5429 P_o
1	1($\phi = 180^0$)	0	0.1719 P_o

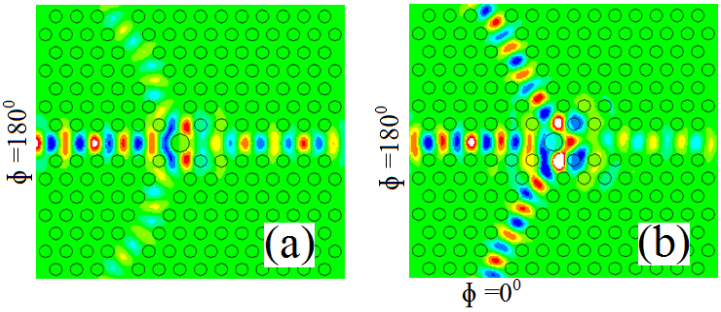


Figure 3.10 Field distributions at steady state of the NOT logic gate for (a) A=1, R=1 (b) A=0, R=1

3.4.5 For NAND gate

NAND gate is the inverse of the AND gate where logic output values are inverse of the AND logic output values. In NAND logic gate output is logically '1' if light is launched at either of the two inputs or zero input is launched at both the inputs and it is logically '0' when both the input values are launched along with the reference signal. The working of

NAND gate has been explained as follows: (i) When reference signal is launched at the reference port R with phase angle $\phi = 0^0$ and none of the signal is launched at the input ports, or signal with phase $\phi = 0^0$ is launched at either of the input ports A and B, then logic '1' is obtained at the output port Y. (ii) When light with phase $\phi = 0^0$ is launched at both the input ports A and B and reference port R is launched with the signal having phase angle $\phi = 180^0$ then logic '0'is obtained at the output port Y. The results have been summarized in table 3.5 where output values are expressed in terms of input power P_o. The contrast ratio for NAND gate has been obtained to be 9.59 dB. The simulation results shown in figure 3.11 and truth table 3.5 clearly indicate that the structure could really behave as NAND logic gate.

Table 3.5: Truth table for NAND logic gate where output Y is in terms of input power P_o

NAND GATE				
Input A ($\phi = 0^0$)	Input B ($\phi = 0^0$)	Reference signal (R)	Logic output	Output Y
0	0	1($\phi = 0^0$)	1	0.5429 P_o
0	1	1($\phi = 0^0$)	1	0.4497 P_o
1	0	1($\phi = 0^0$)	1	0.4497 P_o
1	1	1($\phi = 180^0$)	0	0.0905 P_o

3.4.6 For NOR gate

NOR logic gate is logically inverse of the OR logic gate where output is '1' when both the inputs are '0'. The operation of NOR logic gate has been demonstrated as follows: (i) when no signal is launched at the input ports A and B and only reference port has been excited with the input signal having phase angle $\phi = 180^0$, logic output '1' is obtained at the output port Y. (ii) When either of the two input ports or both the input ports have been excited with light having phase angle $\phi = 0^0$ along with the reference signal having phase angle $\phi = 180^0$ output obtained at the output port Y is logically '0'. The contrast ratio for NOR

logic gate has been found to be 5.42dB. The results for the NOR gate have been mentioned in the table 3.6 and shown in figure 3.12. From the table 3.6 and field distribution shown in figure 3.12 indicate that the proposed structure could really work as NOR logic gate.

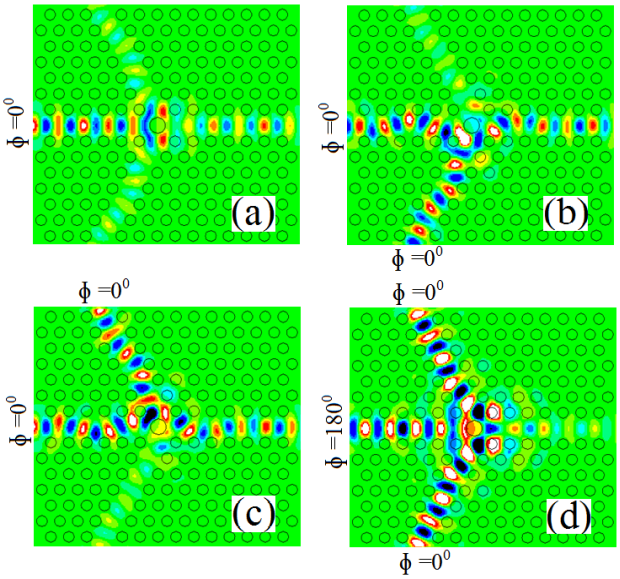


Figure 3.11 Field distributions at steady state of the NAND logic gate for (a) A=0, B=0, R=1 (b) A=1, B=0, R=1 (c) A=0, B=1, R=1 (d) A=1, B=1, R=1

Table 3.6: Truth table for NOR logic gate where output Y is in terms of input power P_o

NOR GATE				
Input A ($\phi = 0^0$)	Input B ($\phi = 0^0$)	Reference signal (R)	Logic output	Output Y
0	0	1($\phi = 180^0$)	1	0.5429 P_o
0	1	1($\phi = 180^0$)	0	0.1719 P_o
1	0	1($\phi = 180^0$)	0	0.1719 P_o
1	1	1($\phi = 180^0$)	0	0.0905 P_o

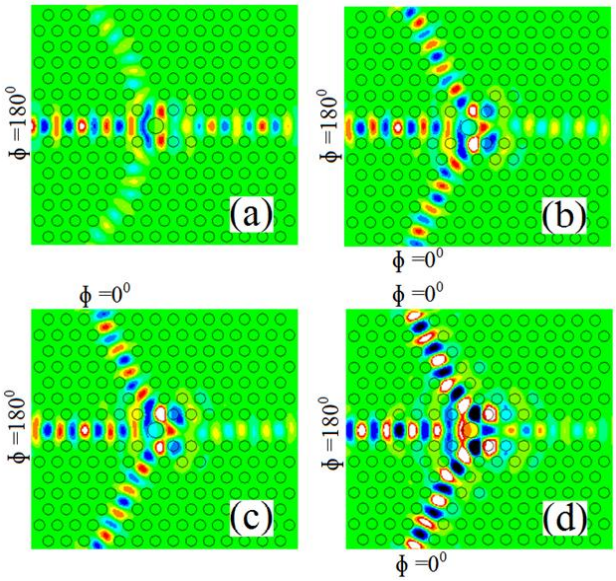


Figure 3.12 Field distributions at steady state of the NOR logic gate for (a) A=0, B=0, R=1 (b) A=1, B=0, R=1 (c) A=0, B=1, R=1 (d) A=1, B=1, R=1

3.4.7 For XNOR gate

XNOR logic gate is logically inverse of the XOR logic gate, where output is '1' if both the input values are same and '0' if both input values are different. The function of XNOR logic gate is as follows: (i) when both the input ports are either excited with the signal having phase angle $\phi = 0^0$ or not excited with any signal but reference signal has been launched at the reference port R with light having phase angle $\phi = 0^0$, then output obtained at the output port Y is logically '1'. (ii) When either of the input ports has been launched with the input signal having phase angle $\phi = 0^0$ along with the reference signal having phase angle $\phi = 180^0$, then output obtained at the output port is logically '0'. The contrast ratio for XNOR logic gate has been calculated to be 5.42 dB. The field distribution at steady state as shown in figure 3.13 and output values shown in table 3.7 clearly indicate that the proposed structure can be used to operate as a XNOR logic gate.

Hence, the realization of all optical logic gates in a single designed structure, exhibit the mutual dependence of the angle between the input beams. On the basis of the dependence of angle variation of the input beams, different logic operations with the desired output values have been successfully realised.

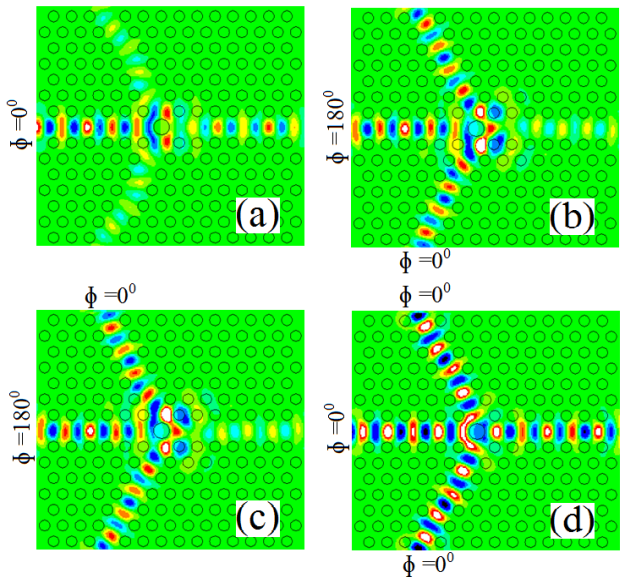


Figure 3.13 Field distributions at steady state of the XNOR logic gate for (a) A=0, B=0, R=1 (b) A=1, B=0, R=1 (c) A=0, B=1, R=1 (d) A=1, B=1, R=1

Table 3.7: Truth table for XNOR logic gate where output Y is in terms of input power P_o

XNOR GATE				
Input A ($\phi = 0^0$)	Input B ($\phi = 0^0$)	Reference signal (R)	Logic output	Output Y
0	0	1($\phi = 0^0$)	1	0.5429 P_o
0	1	1($\phi = 180^0$)	0	0.1719 P_o
1	0	1($\phi = 180^0$)	0	0.1719 P_o
1	1	1($\phi = 0^0$)	1	0.4663 P_o

3.5 Response Time

The response time has been calculated for the proposed design using the time evolution curve as shown in figure 3.14. From figure 3.14, it has been concluded that the time taken to climb output power from 0 to 90% of the average output power i.e. P_{av} in the final steady state is ct=35.9μm or t=0.419 ps and it consists of two parts one of which is the time due to transmission delay i.e. t_1 =0.163 ps and another t_2=0.256 ps is the time for the output

power to climb from 0.1% P_{av} to 90% P_{av}. Since the system operates on linear materials it has been expected that the falling time from average output power i.e. P_{av} to 10% P_{av} is approximately equal to t_2. Hence, a narrow pulse of width of $2t_2$=0.512 ps can be produced. Hence it has been predicted that the proposed structure has a response period of 1.024 ps and can operate at a bit rate of 0.976 Tbit/s.

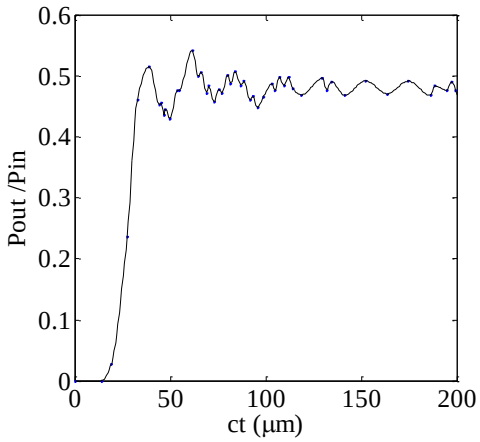


Figure 3.14 Time evolution curve of the output power

3.6 Conclusion

In this chapter, the design for all optical logic gates on a single structure based on optical interference effect in two dimensional PhC waveguides has been proposed. The performance of the proposed PhC structure has been analyzed by PWE method and transmission and optimization characteristics have been obtained using FDTD method. The method of determining the operating parameters has been explained and the optimized parameters have been obtained for achieving the contrast ratio for all optical logic gates. The proposed all optical logic gates can operate at very low powers and it is expected that the proposed structure can be effectively used for the design of all optical integrated circuits.

CHAPTER 4

Polarization independent all-optical logic gates in silicon-on-insulator photonic crystal[3]

4.1 Introduction

In chapter 2 and 3, the design of AND optical logic gate and all optical logic gates, which have emerged as an important part of optoelectronic and integrated devices, have been demonstrated using 2D PhC structure. The 2D PhC slab structures have attracted wide attention due to their ease of fabrication as compared to three dimensional structures. The 2D PhC structures provide versatile platform for on-chip device design and present an alternative to the existing electronic circuitry. In general, these 2D PhC structures are operational for only one specific polarization that limits the light coupling to localized optical modes and extraction of light from the slab. However, polarization independent wave guiding in 2D PhC structures with complete photonic band gap (i.e. photonic band gap for both TE and TM mode) may overcome this limitation [8, 73-75]. Only single polarization based logic gates have been reported so far [13, 43, 64, 72 and 76]. Optical logic gates on SOI platform lead to certain applications like the ultrafast operation of the devices as compared to the traditional electronic devices, data-integrity verification, packet header modification etc. The reported optical logic gates are 2D structures operational for single polarization [53, 65, 69, 71 and 77].

In this chapter, we propose the design of polarization independent AND optical logic gate and all optical logic gates in silicon-on-insulator (SOI) platform based on the light beam interference effect. The structure for AND gate consists of symmetric Y branch

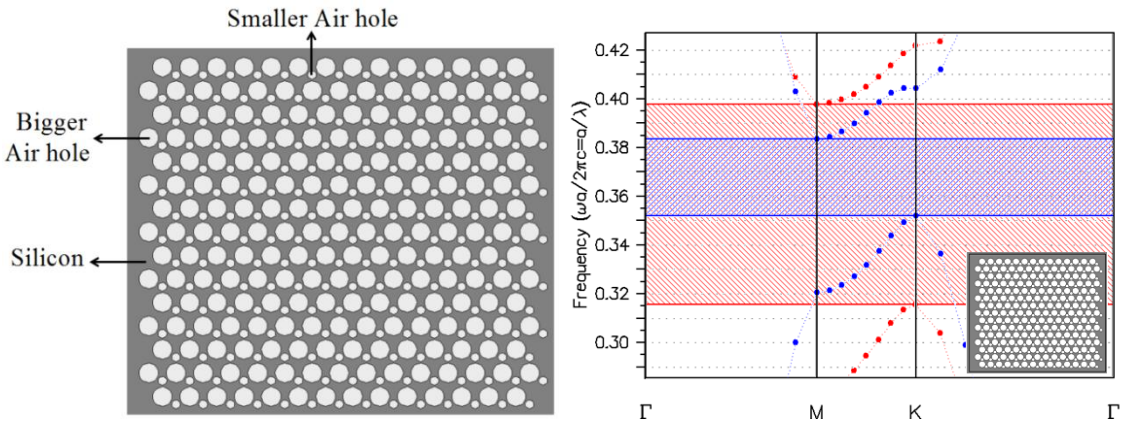
[3] Part of the results reported in this chapter has been published in the paper: "Design and analysis of polarization independent all-optical logic gates in silicon-on-insulator photonic crystal", Optics Communication, 374, pp. 148–15, 2016. http:// dx.doi.org/10.1016/j.optcom.2016.04.037

waveguide so that light beams interfere constructively whereas for all optical logic gates one additional reference waveguide has been created. The light beams interfere either constructively or destructively for both the polarizations based on the phase angle of the light beam launched at reference waveguide. Phase angle of the input light beam can be varied as demonstrated by Tobias Birr et al [78]. The proposed design consists of honey comb lattice arrangement with two different air holes in SOI substrate. The honey comb arrangement on SOI platform has been chosen because this arrangement supports both the polarizations. The honey comb structure of such type can be easily implemented on SOI substrate using recently available technology. The structure has been optimized for both the polarizations (TE and TM mode) at 1.55μm wavelength. The contrast ratio, bit rate and response time have been calculated for TE and TM modes separately and it has been found that the proposed designs behave as AND optical logic gate and all optical logic gates. The calculated results i.e. response period and bit rate are improved than that reported in the previous papers [60, 71, 77]. All the designed structures show linear behaviour and obey the principle of the energy conservation.

4.2 Device design, optimization and simulation results

The design for AND optical logic gate and all optical logic gates constructed on SOI substrate has been presented. The proposed design consists of honey comb lattice of air holes of two different radii in silicon slab as shown in figure 4.1 (a). The radii of two different air holes have been chosen, so as to achieve complete photonic band gap. The radii of two air holes has been taken as r_b = 0.36a (radius of bigger air hole) and r_s = 0.16a (radius of smaller air hole), where 'a = 570nm' is the lattice constant. The smaller air holes have been placed exactly at the centre of the bigger air holes. An asymmetrical Si ($n_{si} = 3.5$) slab of thickness 250nm has been taken which has air as upper cladding and silica ($n_{sio_2} = 1.45$) as lower cladding layer. The 3D calculations consume more time and memory, so, we have employed 2D analysis with effective index method. The effective index of the slab for TE and TM modes has been calculated to be n_{eff} (TE) = 2.89 and n_{eff} (TM) = 2.15 at 1.55μm wavelength, respectively using Finite Element Method (FEM) [75]. Using PWE method, it has been observed that there exists a complete photonic band

gap in the normalized frequency range of 0.3520 to 0.3836 (a/λ), as shown in figure 4.1 (b).



(a) (b)

Figure 4.1 (a) Schematic representation of honey comb photonic crystal (b) complete band gap for honey comb lattice arrangement where red curves correspond to the TE modes and blue curves correspond to the TM modes

4.2.1 For AND optical logic gate

4.2.1.1 Design

For AND optical logic gate three waveguides have been created in the proposed structure to act as input and output waveguides. The design consists of a Y branch photonic crystal waveguide having three arms out of which two behave as input ports (Input A and Input B) and the third one acts as an output port as shown in figure 4.2. The region on both sides of the waveguides has mirror image symmetry so that the maximum light remains confined within the waveguide region. Further, the output waveguide has been modified by addition of the extra air holes of smaller radii at the two boundaries of the output waveguide. A hole has been introduced at the centre of the three waveguides, which has been optimized for both the TE and TM modes. Due to the symmetric waveguide structure the light interferes constructively at the intersection of the three waveguides, when both the signals are launched simultaneously in both the input waveguides. As a result, the maximum value of power is obtained. However, there is branching of signals through the other path when either one of the two signals is present. As a result, low value of power is obtained in the

output waveguide. Thus, leading the proposed design to operate as an AND optical logic gate.

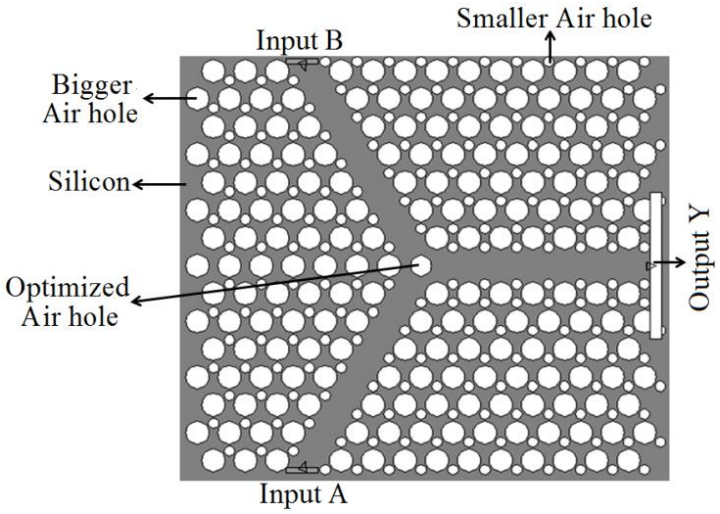


Figure 4.2 Schematic representation of AND optical logic gate

4.2.1.2 Optimization of the radius of the central hole for AND optical logic gate

The radius of the central hole has been optimized at the centre of the Y branch to enhance the performance of the proposed logic gate for both the TE and TM modes separately. Figure 4.3 shows the variation of ratio of output power to the input power (P_{out}/P_{in}) versus radius of the central hole for both the polarizations at single input signal and both input signals.

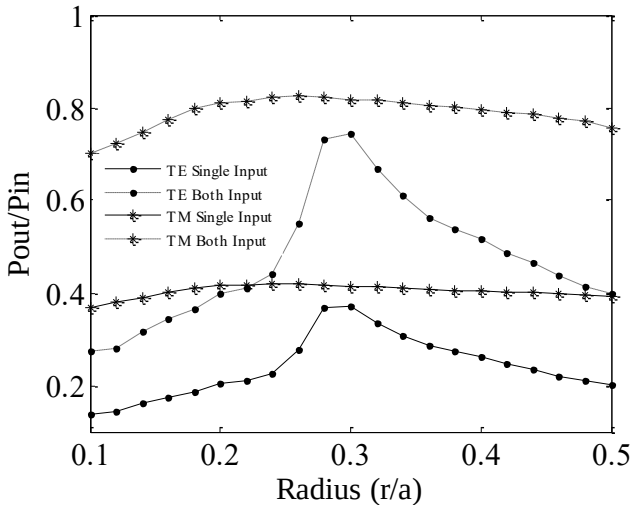


Figure 4.3 Power transmittance with radius of central hole both for TE and TM mode with respect to the single input and both inputs

For TE mode, it has been observed that as the radius of the central hole increases the ratio of output power to input power increases and then decreases whereas the variation remains same for TM mode. A common region has been chosen for optimization of the radius of central hole where output for single input as well as for both input signals is maximum for TE and TM polarizations. Hence, the optimized radius of the central hole has been taken as 0.30a.

4.2.1.3 Simulation results and discussion for AND gate

The optimized structure has been analyzed to perform as AND optical logic gate for both TE and TM modes using FDTD method. Both the TE polarized and TM polarized light has been launched at input ports A and B. When input power P_a is launched at input port A or at port B separately, then the power at output port remains low. When power is launched at both the ports A and B simultaneously, then maximum power is obtained at the output port for both TE and TM polarizations as mentioned in table 4.1. The results calculated in table 4.1 indicate that the design can work as AND optical logic gate for both TE and TM polarizations based on the phenomenon of interference. The contrast ratio for both TE and TM polarizations has been calculated and found to be 6 dB at 1.55μm wavelength as shown in figure 4.4. Figure 4.4 shows the variation of the contrast ratio for both the TE and TM polarizations in the entire range of complete photonic band gap.

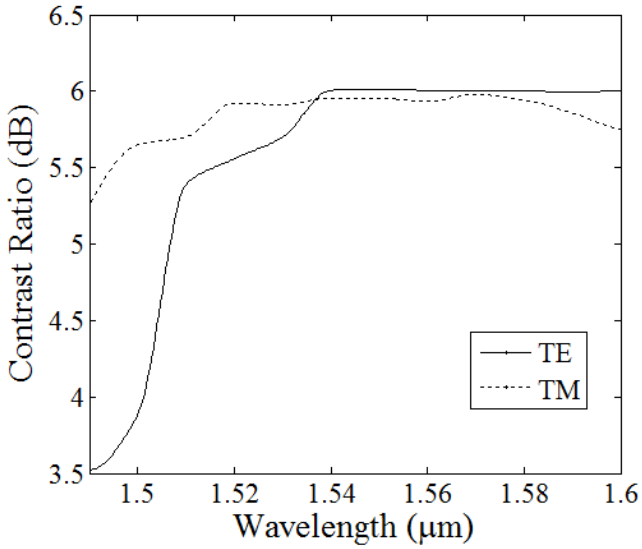


Figure 4.4 Contrast ratio for both TE and TM polarizations in the complete band gap range

Table 4.1 Truth table for AND optical logic gate for TE and TM polarizations at 1.55μm wavelength where output power Y is in terms of input power P_a

AND GATE				
Input A	Input B	Logic output	Output Y (TE)	Output Y (TM)
0	0	0	0	0
0	1	0	0.372 P_a	0.414 P_a
1	0	0	0.372 P_a	0.414 P_a
1	1	1	1.485 P_a	1.630 P_a

The response time which is defined as the switching time of the device between the OFF and ON state for both TE and TM polarizations has been determined using time evolving curve of the output power as shown in figure 4.5.

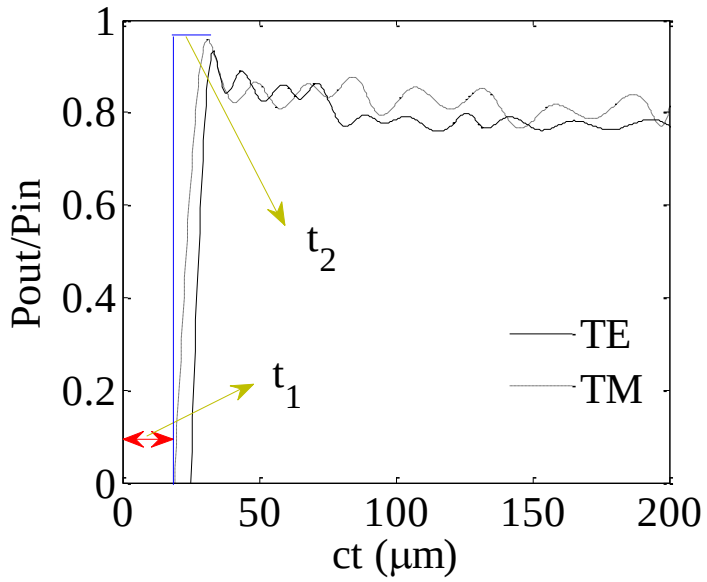


Figure 4.5 Response time in terms of time evolution of the output power for both TE and TM polarizations

For TE polarized mode, at steady-state, the time taken to reach output power from 0 to 90% of the average output power (P_{av}) is ct = 32.8μm or t = 0.316 ps, where 'c' is the speed of light in medium. This time consists of two parts one of which is the time due to transmission delay i.e. t_1 = 0.241 ps and another is the time taken by output power to climb from 0.1% to 90% of P_{av} i.e. t_2 = 0.075 ps. It has been expected that the falling time from P_{av} to 10% of P_{av} is approximately equal to t_2. Thus, a narrow pulse width of $2t_2$ = 0.150 ps

can be produced and hence the response time of 0.300 ps has been achieved if the ON and OFF time of the signal is same. Further, bit rate which is defined as the inverse of the response time has been calculated to be 3.33Tbit/s for TE polarized mode. Similarly, response period and bit rate has been calculated for TM polarized mode using figure 4.5. For TM polarized mode, ct = 30.3 μm or t = 0.27 ps, t_1 =0.136 ps, t_2 = 0.081 ps, $2t_2$ =0.162 ps and the response period of 0.324 ps and a bit rate of 3.09 Tbit/s have been obtained. Hence, we have achieved the improved values of bit rate and response period as reported earlier [60, 71, and 77]. The field distribution profiles at steady state for both TE and TM polarized modes as shown in figure 4.6 and the results mentioned in table 4.1 for both TE and TM polarizations at a wavelength of 1.55μm, indicate that the design behaves as AND optical logic gate.

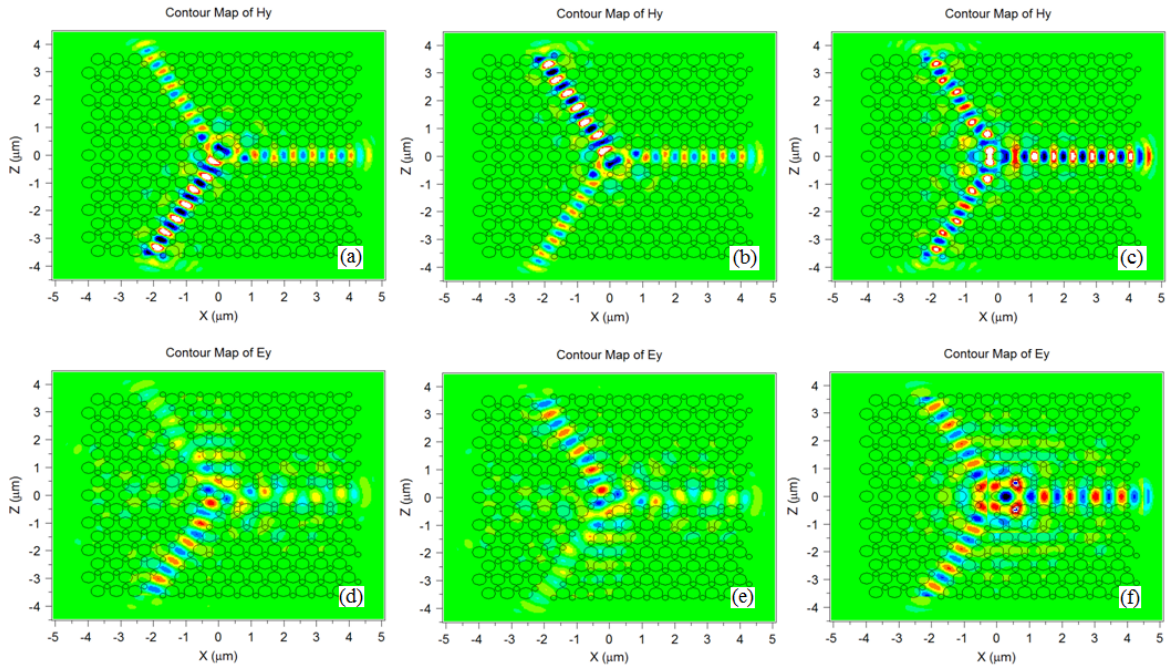


Figure 4.6 Field distributions at steady state of the AND logic gate at 1.55μm wavelength for TE polarization at (a) A=1, B=0 (b) A=0, B=1 (c) A=1, B=1 and for TM polarization at (d) A=1, B=0 (e) A=0, B=1 (f) A=1, B=1

4.2.2 For all optical logic gates

4.2.2.1 Device design

In the proposed design for all optical logic gates, four waveguides have been created out of which two behave as input ports (Input A and Input B) and the third one acts as a reference port (R) and fourth as an output port Y as shown in figure 4.7. The reference port with reference/control signal has been used to create phase difference between the input signals which results into constructive as well as destructive interference depending on the phase angle of the reference/control signal. In this structure also mirror image symmetry has been considered so that the maximum light remains confined within the waveguide region. A hole has been introduced at the centre of the four waveguides, which has been optimized for both the TE and TM polarized modes. The light interferes constructively at the intersection of the four waveguides as the addition of signals that are in-phase, when either of the input signals or both the input signals are launched simultaneously in both the input waveguides. As a result, maximum value of power is obtained. However, there is a destructive interference when signals are out of phase resulting into low value of power in the output waveguide. Thus, the proposed design can be used for the realization of all optical logic gates.

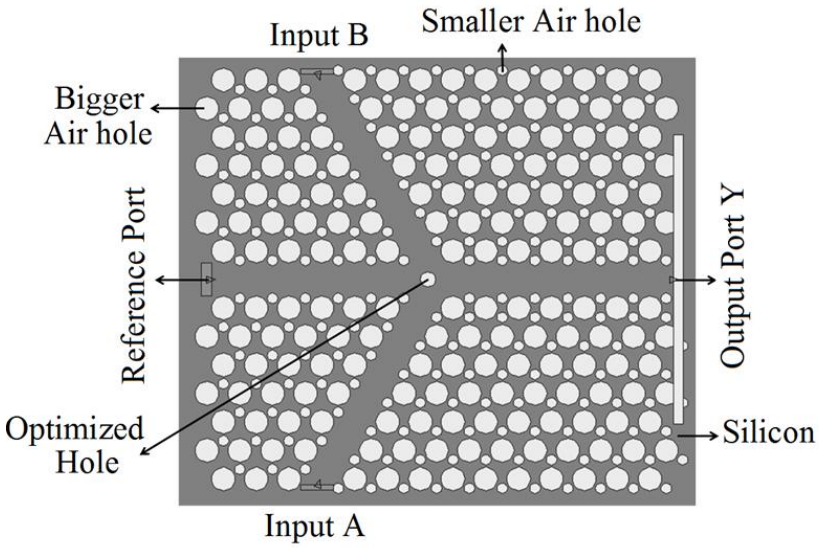


Figure 4.7 Schematic representation of all optical logic gates

4.2.2.2 Optimization of the radius of the central hole for all optical logic gates

The radius of the central hole has been optimized at the centre of the four waveguides to enhance the performance of the proposed design for both the TE and TM polarized modes separately. Figure 4.8 shows the variation of ratio of output power to the input power (P_{out}/P_{in}) versus radius of the central hole for both the polarizations at single input (along with the reference signal) and both input signals (along with the reference signal). For TE polarized mode, it has been observed that as the radius of the central hole increases the ratio of output power to input power increases and then decreases. For TM mode it increases first and then decreases for both inputs whereas it keeps on decreasing for single input. A common region has been chosen for the optimization of the radius of central hole where output for both input signals (along with the reference signal) crosses each other for TE and TM polarizations. Hence, the optimized radius of the central hole has been taken as 0.23a.

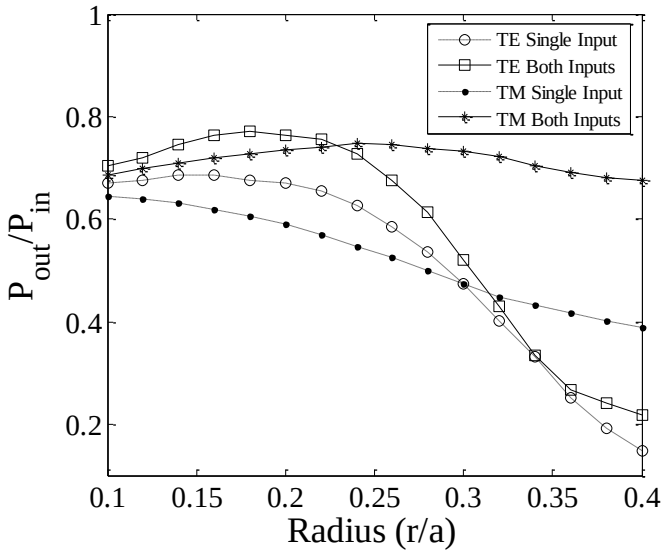


Figure 4.8 Power transmittance versus radius of central hole for all optical logic gates for both TE and TM polarized modes with respect to the single input and both inputs along with the reference/control signal

4.2.2.3 Results and discussion

The optimized structure has been analyzed to perform as AND, OR, NOT, NAND, NOR, XOR, XNOR all-optical logic gates for both TE and TM polarized modes using FDTD method. Both the TE polarized and TM polarized light has been launched at both the input

ports and reference port. The logic operations have been performed as follows: (i) when either of the input ports A and B or both the input ports A and B have been excited with light signal having phase angle $\varphi = 0^0$ and the reference port with reference/control signal having phase angle $\varphi = 0^0$ then logic 1 is obtained at the output port Y. (ii) when either of the input ports A and B or both the input ports A and B are excited with light signals having phase angle $\varphi = 0^0$ and reference port with control signal having phase angle $\varphi = \pi$ then logic 0 is obtained at the output port Y. (iii) when only the control signal at reference port with $\varphi = 0^0$ or $\varphi = \pi$ has been excited then maximum power is obtained at the output port as shown in figures 4.9 and 4.10. Figure 4.9 represents the field distribution pattern for TE polarized mode and figure 4.10 corresponds to the TM polarized mode. The logic behaviours have been analyzed at a wavelength of 1.55μm for both the TE and TM polarizations.

4.2.2.3.1 AND gate

The AND optical logic gate operation is as follows:

(i) A = 1, B = 0 at $\varphi = 0^0$ and R = 1 at $\varphi = \pi$, output Y = 0 due to destructive interference.

(ii) A = 0, B = 1 at $\varphi = 0^0$ and R = 1 at $\varphi = \pi$, output Y= 0.

(iii) A = 1, B = 1 at $\varphi = 0^0$ and R = 1 at $\varphi = 0^0$ then output Y = 1 due to constructive interference.

The results have been compared and summarized in table 4.2 for all possible combinations for both TE and TM polarizations. Figures 4.9(c), (d) and (e) show the field distribution for TE polarization. The field distribution for TM polarization has been shown in figures 4.10 (c), (d) and (e). The calculated value of contrast ratio is found to be 10 dB.

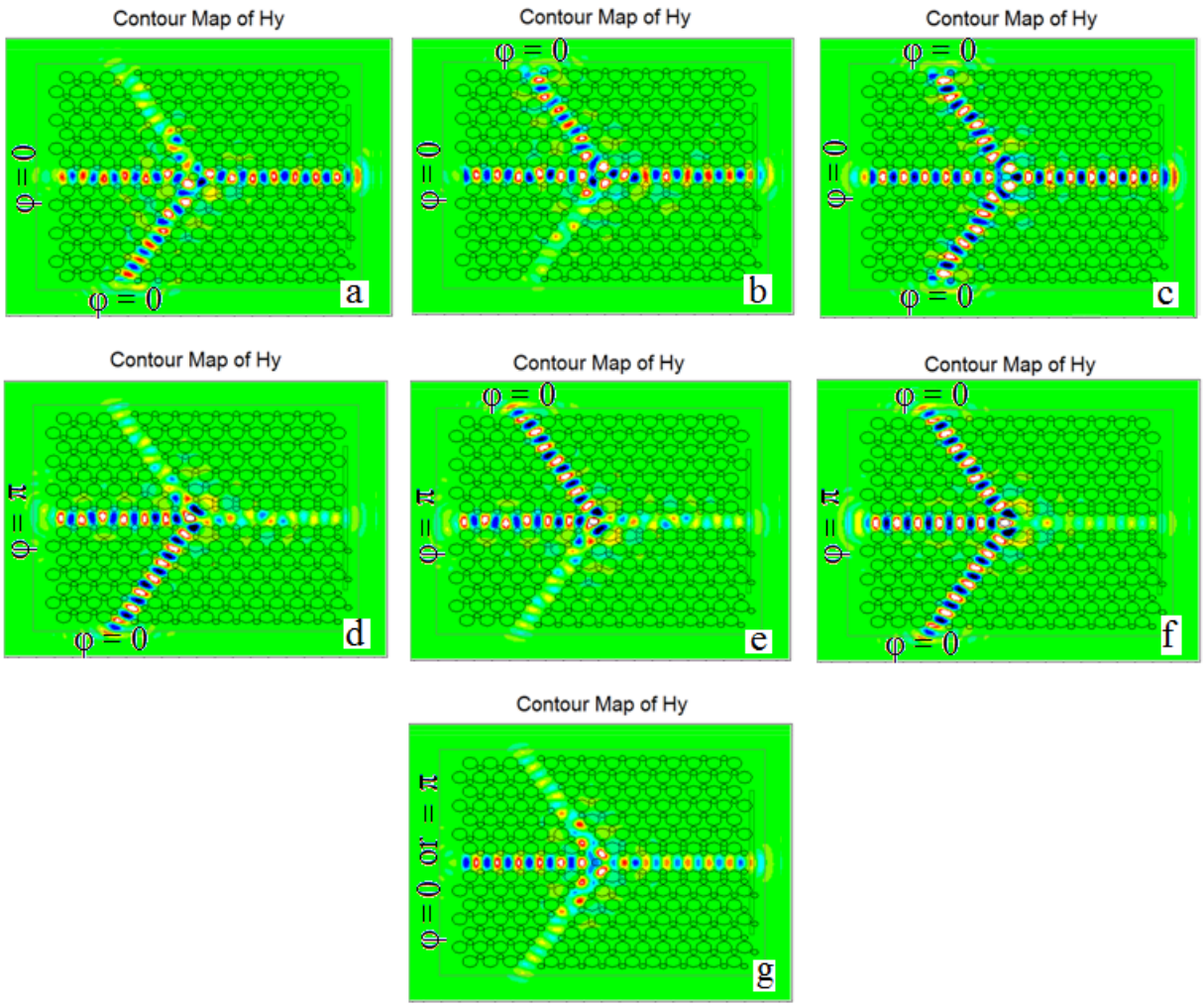


Figure 4.9 Field distributions at steady state for all optical logic gates at 1.55μm wavelength for TE like polarization at (a) A = 1, B = 0 at $\varphi = 0^0$, R = 1 at $\varphi = 0^0$ (b) A = 0, B = 1 at $\varphi = 0^0$, R = 1 at $\varphi = 0^0$ (c) A = 1, B = 1 at $\varphi = 0^0$, R = 1 at $\varphi = 0^0$ (d) A = 1, B = 0 at $\varphi = 0^0$, R = 1 at $\varphi = \pi$ (e) A = 0, B = 1 at $\varphi = 0^0$, R = 1 at $\varphi = \pi$ (f) A = 1, B = 1 at $\varphi = 0^0$, R = 1 at $\varphi = \pi$ (g) A = 0, B = 0, R = 1 at $\varphi = 0^0 or \pi$

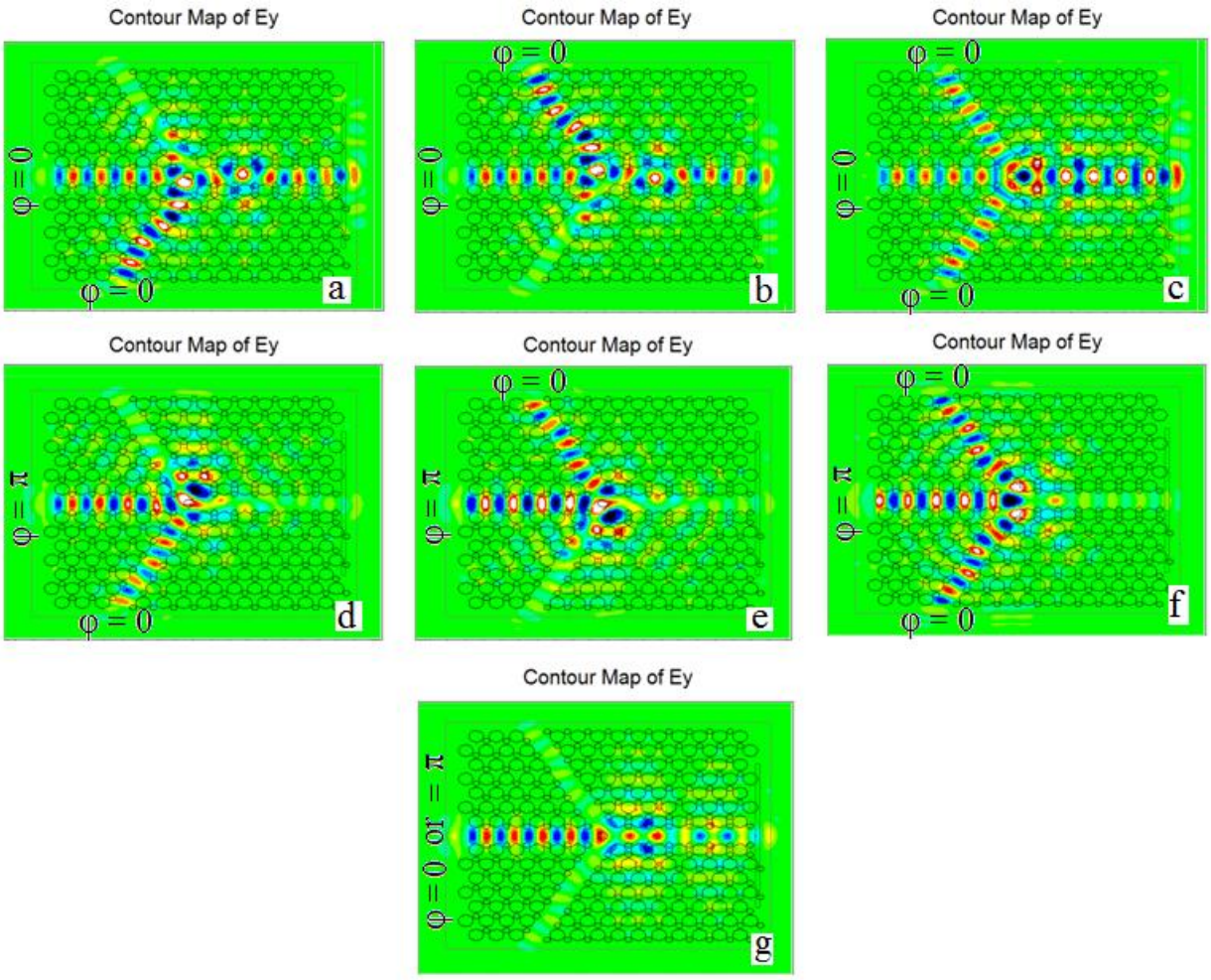


Figure 4.10 Field distributions at steady state for all optical logic gates at 1.55μm wavelength for TM like polarization at (a) A = 1, B = 0 at $\varphi = 0^0$, R = 1 at $\varphi = 0^0$ (b) A = 0, B = 1 at $\varphi = 0^0$, R = 1 at $\varphi = 0^0$ (c) A = 1, B = 1 at $\varphi = 0^0$, R = 1 at $\varphi = 0^0$ (d) A = 1, B = 0 at $\varphi = 0^0$, R = 1 at $\varphi = \pi$ (e) A = 0, B = 1 at $\varphi = 0^0$, R = 1 at $\varphi = \pi$ (f)) A = 1, B = 1 at $\varphi = 0^0$, R = 1 at $\varphi = \pi$ (g) A = 0, B = 0, R = 1 at $\varphi = 0^0 or \pi$

Table 4.2 Truth table for AND optical logic gate for TE and TM polarizations at 1.55μm wavelength where normalized output power Y is in terms of input power P_a

AND GATE					
Input A ($\varphi = 0^0$)	Input B ($\varphi = 0^0$)	Reference Signal (R)	Logic output	Normalized Output Y (TE)	Normalized Output Y (TM)
0	0	0	0	0	0
0	1	1($\varphi = \pi$)	0	0.1716 P_a	0.0902 P_a
1	0	1($\varphi = \pi$)	0	0.1722 P_a	0.0920 P_a
1	1	1($\varphi = 0^0$)	1	0.7448 P_a	0.7453 P_a

4.2.2.3.2 OR gate

The optimized structure can be operated as OR gate for both TE and TM polarizations and is explained as follows:

1. A = 1, B = 0, or A = 0, B = 1, at $\varphi = 0^0$ and R = 1 also at $\varphi = 0^0$, Y = 1 i.e. logic '1'is obtained at the output port Y due to the constructive interference.
2. A = 1, B = 1, at $\varphi = 0^0$ and reference port with reference/control signal R = 1 is also having phase angle $\varphi = 0^0$ then logic '1' is obtained at the output port Y due to the phase matching condition.

For the OR gate realization, the phase angle between the input signals and control signal has been taken as same which results into the constructive interference and satisfying the logic output of the OR gate. The field distribution at steady state for TE polarization has been shown in figures 4.9(a), (b), and (c) and for TM polarization in figures 4.10(a), (b) and (c). The results mentioned in table 4.3 clearly show that the proposed structure can function as OR optical logic gate.

Table 4.3 Truth table for OR optical logic gate for TE and TM polarizations at 1.55μm wavelength where normalized output power Y is in terms of input power P_a

OR GATE					
Input A ($\varphi = 0^0$)	Input B ($\varphi = 0^0$)	Reference Signal (R)	Logic output	Normalized Output Y (TE)	Normalized Output Y (TM)
0	0	0	0	0	0
0	1	1($\varphi = 0^0$)	1	0.6407 P_a	0.5629 P_a
1	0	1($\varphi = 0^0$)	1	0.6391 P_a	0.5572 P_a
1	1	1($\varphi = 0^0$)	1	0.7448 P_a	0.7453 P_a

4.2.2.3.3 NOT gate

In the proposed structure, for NOT gate one input has been taken at the input port A and other at the reference port as control signal. The switching from off to on state has been maintained by phase difference of π between the input signal and control signal. The output remains high when only control signal is present with phase angle of $\varphi = \pi$ i.e. A = 0, R = 1and is low when input signal and the control signal are out of phase i.e. A = 1 at $\varphi = 0^0$, R=1 at $\varphi = \pi$ as indicated in table 4.4 for both TE and TM polarizations at a wavelength of 1.55μm. The contrast ratio for NOT gate is found to be 6 dB. The table 4.4 and field distributions shown in figures 4.9(d), (g) for TE polarization and 4.10(d) and (g) for TM polarization clearly indicate that the proposed structure can be used as a NOT gate.

Table 4.4 Truth table for NOT optical logic gate for TE and TM polarizations at 1.55μm wavelength where normalized output power Y is in terms of input power P_a

NOT GATE				
Input A ($\varphi = 0^0$)	Reference Signal (R)	Logic output	Normalized Output Y (TE)	Normalized Output Y (TM)
0	1 ($\varphi = \pi$)	1	0.6562 P_a	0.4244 P_a
1	1 ($\varphi = \pi$)	0	0.1722 P_a	0.0920 P_a

4.2.2.3.4 NAND gate

The universal NAND gate is the inverse of the AND gate. The NAND gate optical logic behaviour for both the TE and TM polarizations has been explained as follows:

(i) When control signal is launched at the reference port with phase angle $\varphi = 0^0$ i.e. R = 1 and none of the signals is launched at the input ports, i.e. A = 0, B = 0 then the output obtained at the output port Y is logically '1'.

(ii) When either of the input ports have been excited with the input signals i.e. A = 1, B = 0 or A = 0, B = 1 with $\varphi = 0^0$ and control signal R = 1 with $\varphi = 0^0$ then also the output obtained is logically '1'.

(iii) A = 1, B = 1 with phase $\varphi = 0^0$ and reference port with control signal R = 1 with $\varphi = \pi$, then logic '0' is obtained at the output port Y.

The results have been summarized in table 4.5 and the simulations shown in figures 4.9(a), (b), (f) and (g) for TE polarization and figures 4.10 (a), (b), (f) and (g) for TM polarization clearly indicate that the structure could really behave as NAND optical logic gate. The contrast ratio for NAND gate is found to be 7 dB.

Table 4.5 Truth table for NAND optical logic gate for TE and TM polarizations at 1.55μm wavelength where normalized output power Y is in terms of input power P_a

NAND GATE					
Input A ($\varphi = 0^0$)	Input B ($\varphi = 0^0$)	Reference Signal (R)	Logic output	Normalized Output Y (TE)	Normalized Output Y (TM)
0	0	1($\varphi = 0^0$)	1	0.6562 P_a	0.4244 P_a
0	1	1($\varphi = 0^0$)	1	0.6407 P_a	0.5629 P_a
1	0	1($\varphi = 0^0$)	1	0.6391 P_a	0.5572 P_a
1	1	1($\varphi = 0^0$)	0	0.1236 P_a	0.1215 P_a

4.2.2.3.5 NOR gate

The inverse of OR gate leads to the universal NOR logic gate which can further be used to design other devices. The NOR logic operation is as follows:

(i) When only the control signal is applied at the reference port with phase angle $\varphi = \pi$ then only the output is logically in the ON state.

(ii) When the input signal is applied at either of the input ports or at both the input port with phase angle $\varphi = 0^0$ but control signal is applied at the reference port with phase angle $\varphi = \pi$ then the output at the output port is always zero i.e. in OFF state.

The logic output for both TE and TM polarizations have been compared in table 4.6 and can be easily verified from the simulation figures shown in figure 4.9 and 4.10. The contrast ratio for NOR gate has been found out to be 6.7 dB.

Table 4.6 Truth table for NOR optical logic gate for TE and TM polarizations at 1.55μm wavelength where normalized output power Y is in terms of input power P_a

NOR GATE					
Input A ($\varphi = 0^0$)	Input B ($\varphi = 0^0$)	Reference Signal (R)	Logic output	Normalized Output Y (TE)	Normalized Output Y (TM)
0	0	1($\varphi = \pi$)	1	0.6562 P_a	0.4244 P_a
0	1	1($\varphi = \pi$)	0	0.1716 P_a	0.0902 P_a
1	0	1($\varphi = \pi$)	0	0.1722 P_a	0.0920 P_a
1	1	1($\varphi = \pi$)	0	0.1236 P_a	0.1215 P_a

4.2.2.3.6 XOR gate

The output in XOR logic gate is logically ‘1’if only one of the two inputs is high (1) and logically ‘0’if both the inputs are high (1) or low (0). The working of XOR logic gate has been explained as follows:

(i) When one of the input signals is applied along with the control signal i.e. A = 1, B = 0, R = 1 or A = 0, B = 1, R = 1 with phase angle $\varphi = 0^0$ then the output is logically high.

(ii) The output is logically low when none of the input ports and reference port have been excited or both the input ports have been excited with the light signal having phase angle $\varphi = 0^0$ and reference port with the reference light signal having phase angle $\varphi = \pi$ i.e. A = 0, B = 0, R = 0 or A = 1, B = 1, R = 1.

The simulation figures 4.9(a), (b) and (f) for TE polarization and figures 4.10(a), (b) and (f) for TM polarization show that the proposed structure could really work as XOR logic gate. The truth table for TE and TM polarizations has been compared in table 4.7. The calculated value of contrast ratio for XOR logic gate has been found to be 5 dB.

Table 4.7 Truth table for XOR optical logic gate for TE and TM polarizations at 1.55μm wavelength where normalized output power Y is in terms of input power P_a

XOR GATE					
Input A ($\varphi = 0^0$)	Input B ($\varphi = 0^0$)	Reference Signal (R)	Logic output	Normalized Output Y (TE)	Normalized Output Y (TM)
0	0	0($\varphi = 0^0$)	0	0	0
0	1	1($\varphi = 0^0$)	1	0.6407 P_a	0.5629 P_a
1	0	1($\varphi = 0^0$)	1	0.6391 P_a	0.5572 P_a
1	1	1($\varphi = 0^0$)	0	0.1236 P_a	0.1215 P_a

4.2.2.3.7 XNOR gate

The XNOR optical logic gate is the inverse of the XOR optical logic gate and can be easily verified as mentioned in table 4.8 for both the polarizations. The contrast ratio has been calculated to be 9.1 dB. The field distributions shown in figures 4.9(c), (d), (e) and (g) for TE polarization and figures 4.10(c), (d), (e) and (g) for TM polarization proves that the proposed design can be efficiently used as XNOR optical logic gate.

Table 4.8 Truth table for XNOR optical logic gate for TE and TM polarizations at 1.55μm wavelength where normalized output power Y is in terms of input power P_a

XNOR GATE					
Input A ($\varphi = 0^0$)	Input B ($\varphi = 0^0$)	Reference Signal (R)	Logic output	Normalized Output Y (TE)	Normalized Output Y (TM)
0	0	1($\varphi = \pi$)	1	0.6562 P_a	0.4244 P_a
0	1	1($\varphi = \pi$)	0	0.1716 P_a	0.0902 P_a
1	0	1($\varphi = \pi$)	0	0.1722 P_a	0.0920 P_a
1	1	1($\varphi = \pi$)	1	0.7448 P_a	0.7453 P_a

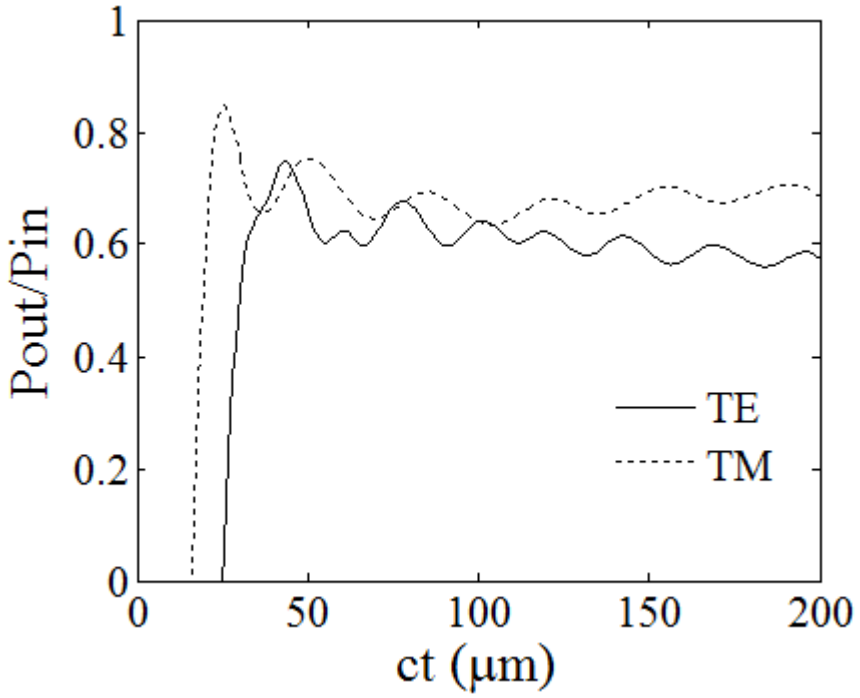


Figure 4.11 Response time in terms of time evolution of the output power for all optical logic gate design for both TE and TM polarizations

The response time of the all optical logic gate device for both TE and TM polarized modes has also been determined using time evolving curve of the output power as shown in figure 4.11. For TE mode, at steady-state, ct = 37.4μm or t = 0.360 ps, time due to transmission delay is t_1 = 0.245 ps and time taken by output power to climb from 0.1% to

90% of P_{av} is t_2 = 0.115 ps, a narrow pulse width of $2t_2$ = 0.230 ps. Thus, the response time of 0.460 ps has been achieved which leads to a bit rate of 2.17 Tbit/s. Similarly, for TM mode, ct = 32.0 μm or t = 0.230 ps, t_1 =0.114 ps, t_2 = 0.116 ps, $2t_2$ =0.232 ps and the response period of 0.464 ps and a bit rate of 2.15 Tbit/s have been obtained. Hence, we have achieved the improved values of bit rate and response period for both TE and TM modes at a wavelength of 1.55μm. The results indicate that the proposed designs behave as all-optical logic gates.

4.3 Conclusion

In this chapter, we have reported the design and performance characteristics of polarization independent AND optical logic gate in Y shaped and all optical logic gates in three port waveguide shaped honey comb photonic crystal which yields complete photonic band gap in the range of optical communication window around 1.55μm. The PWE and FDTD methods have been utilized to determine the optimized parameters. The contrast ratios for both TE and TM modes are comparable at 1.55μm wavelength which makes this suitable for c-band device design. The response time and bit rate have been calculated for the designs for both the polarizations. The proposed structures are easier to fabricate than alternating slabs conducive to TE and TM band gaps and hence could be a strong candidate for future polarization independent all optical integrated devices.

CHAPTER 5

Time and wavelength de-multiplexer in slotted photonic crystal waveguide on SOI platform[4]

5.1 Introduction

In the previous chapters, the design of all optical logic gates in various configurations have been proposed and analysed. To design all optical logic gates, the properties of photonic band gap and photonic band gap guidance in PhCs have been explored. However, these optimally structured PhCs can exhibit diverse features. One of the interesting properties exhibited by PhCs, that have gained considerable attention over the years, is the control they can exercise over the group velocity. This property can be utilised to attain slow light i.e. the reduction in group velocity. Slow light has attracted wide attention due to its diverse applications in optical sensors [79], time-domain processing of optical signals i.e. optical delay lines [80], spatial compression of optical energy [81], quantum computing, enhancement of light-matter interaction [82-85] and for the miniaturization of optoelectronic integrated circuits and devices [81, 86-89]. As mentioned in chapter 1, PhC line defect waveguide is one of the most suitable structures for realizing slow light effect. This is because such line defect structure operates at room temperature and has high potential for on-chip integration by modification of the initial PhC structure [90]. To design the novel slow light structures in PhC, the useful bandwidth is the frequency range of the propagating mode that lies below the silica light line. Low group velocity i.e. high group index and low group velocity dispersion with wide bandwidth are the novel properties for design and development of slow light effect in PhC. Slow light effect with

[4] Part of the results reported in this chapter has been published in the paper: "Slow light enabled time and wavelength division de-multiplexer in slotted photonic crystal waveguide", Journal of Nanophotonics, 9, pp. 093063-1, 2015. http://dx.doi.org/10.1117/1.JNP.9.093063

wide band width range and low GVD has been observed and reported in many experiments [91-92]. The slow light effect in PhC has been realised in many ways such as by infiltrating with dielectric material [93-94], by changing holes size and shape [95-98] and by adjusting the position of holes adjacent to the waveguide [99-102, 104].

Recently, slow light effect in slotted PhC waveguide has drawn considerable interest in which the light is confined in the low index region as compared to the conventional PhC waveguide where light is confined in the high index region. The confinement of light in low index slot waveguide with slow light can be useful in sensor applications, where the interaction of slow light and measuring samples is enhanced. Further, there is a strong possibility that slotted PhC based slow light in lower index waveguide will be applicable in the design of optical buffer. The slotted PhC waveguide has advantage over the high index guiding waveguide due to the confinement of light in the air slot as compared to the normal material waveguide. In slotted PhC waveguide, the material absorption losses are less as compared to the conventional material waveguide. It is expected that such slotted PhC waveguide in slow light region may find applications in the enhancement of linear and nonlinear effects.

In this chapter, the design of slotted SOI based PhC structure having periodic arrangement of elliptical air holes within the silicon substrate to enhance the slow light properties with low group velocity dispersion and large bandwidth range is reported. The basic schematic structure of the proposed design has been shown in figure 5.1. The PWE and FDTD method has been used to analyze the dispersion relation of the slotted waveguide based structure. The proposed slotted PhC waveguide structure has been analyzed for its application as an optical buffer. Further, the application of slotted time and wavelength division de-multiplexer has been explored. The calculated results show that the time delay between the two wavelengths in the slotted structure (1165 ps) is higher than that reported earlier (647 ps) [96].

5.2 Structure design

The design of slotted waveguide in a PhC structure composed of elliptical air holes laid on SOI substrate has been reported as shown in figure 5.1. To design the proposed structure,

initially we have assumed a hexagonal arrangement of circular air holes of radius 0.3a where, 'a=0.4182' is the lattice constant, embedded in a Si slab of SOI substrate. The refractive index of Si has been taken to be 3.5 with thickness 450 nm. The core guiding layer of Si is bonded onto lower cladding layer of silica (Sio_2) of thickness 3μm. Further, a W1 PhC channel waveguide along the Γ-K direction has been created by making a single line defect in the proposed PhC structure. Full 3-D calculation of the dispersion relation of photonic crystal waveguide (PhCW) is very time consuming, so 2-D analysis with effective refractive index method has been done, which is precise enough for estimating the slow light properties of PhCW. The effective refractive index for the proposed PhC has been calculated to be 3.25. Figure 5.2(a) shows the band diagram for the initial PhC structure consisting of circular air holes which shows a band gap in the normalized frequency region 0.2208-0.2883 for TE polarization.

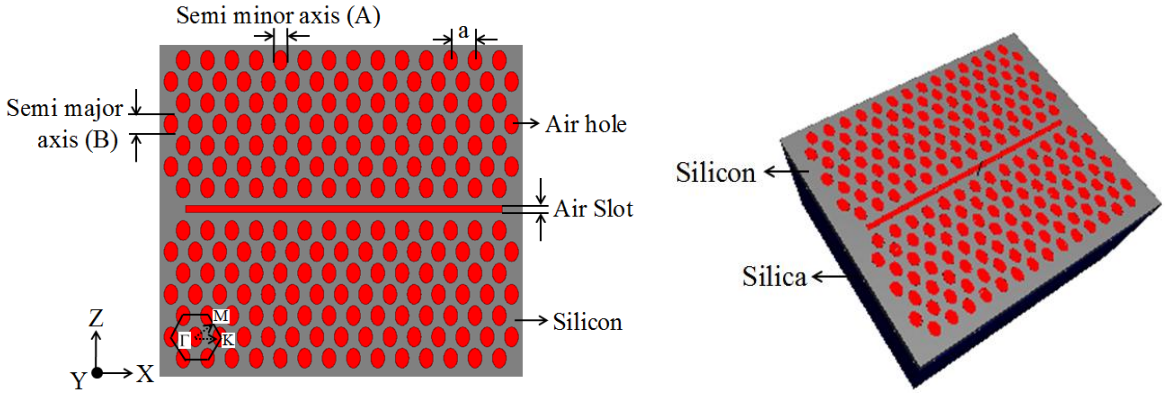
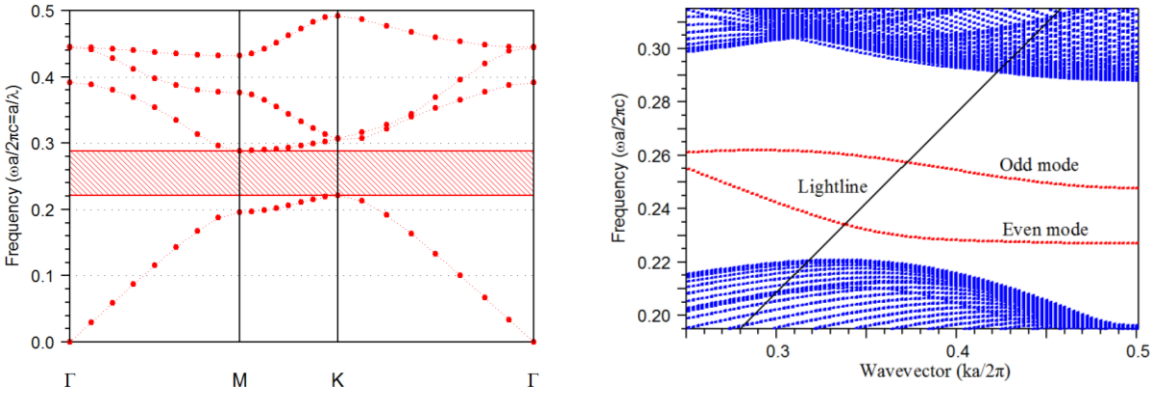


Figure 5.1 Schematic representation of the proposed optimized structure with an air slot and regular arrangement of elliptical air holes, where A and B correspond to the radius of semi-minor axis and semi-major axis

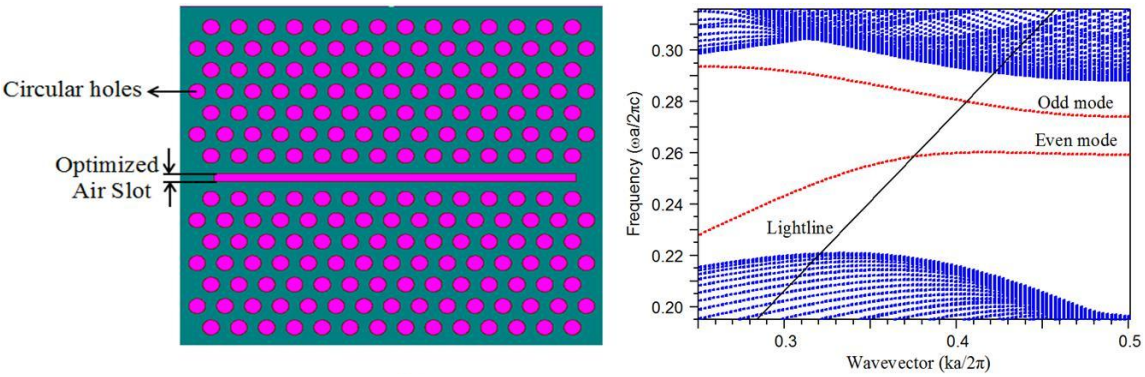
Further, the dispersion diagram for the W1 PhC waveguide has been shown in figure 5.2(b), that exhibits two guided modes existing below the silica light line. Then an air slot has been created in the W1 waveguide as shown in figure 5.3(a). Figure 5.3(b) depicts the dispersion diagram which shows the opposite behaviour of the two guided modes lying below the silica light line in comparison to the guided modes of the W1 PhCW as shown in figure 5.2(b). This opposite nature/behaviour shown by the guided modes of the slotted PhCW (SPhCW) is due to the lower effective index in the waveguide than that in the surrounding slab. This leads to the positive slope of the even guided mode

in the SPhCW as compared to the negative slope of the even mode in the W1 PhC waveguide.



(a) (b)

Figure 5.2 (a) Band gap for TE polarization (b) dispersion relation showing two modes (even and odd) below the light line lying within the band gap range for radius of air holes = 0.3a.



(a) (b)

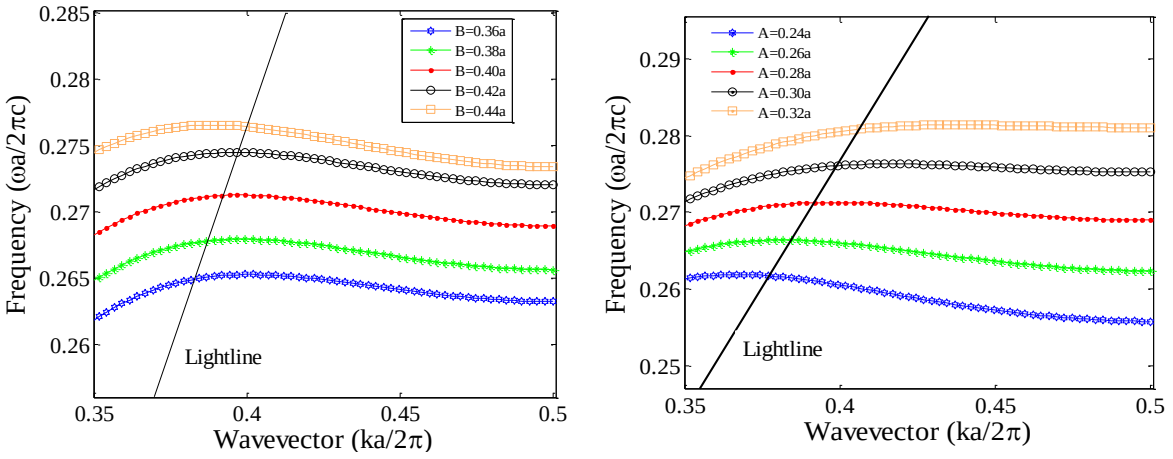
Figure 5.3 (a) Basic structure with optimized slot width in W1 PhC waveguide (b) dispersion relation showing two modes with flat band section below the light line for slotted waveguide of width s = 0.3a

Further, the width of slot in the W1 PhC waveguide has been optimized. It has been observed that as the slot width is increased, it gradually shifts the guided mode towards the higher frequency pushing it outside the band gap region. On the other hand, the decrease in the slot width pulls the mode towards the lower frequency pulling it outside the gap region. Hence, an optimum value of slot width i.e. s = 0.30a has been taken as it places the even guided mode well within the band gap region. Further, the group velocity and group

velocity dispersion (GVD) has been calculated to analyze the slow light effect in the basic structure. The calculations show that the group velocity is very low because of the flat dispersion curve, but the GVD parameter turns out to be of the order of 10^8 ps^2/km, which is large. The large value of GVD limits the achievable bandwidth for slow light transmission. Thus, the structure needs to be optimized in order to obtain low value of GVD required for the desired slow light effect.

5.3 Optimization of slotted structure

Various optimization techniques have been proposed to obtain the flat section of the dispersion curve i.e. the high group index and low GVD parameter. In most of the papers, the shape, size and position of the first two rows of air holes adjacent to the air slot have been chosen for modification. In this chapter, to optimize the structure, the circular air holes have been replaced by elliptical air holes in the originally considered structure in order to obtain flat section of the dispersion curve [103]. The semi minor axis (A) and semi major axis (B) of the elliptical air holes have been modified and its effect on the dispersion relation has been analyzed. Further, the even mode has been used for analysis of the slow light effect because most of the energy in the SPhCW's is concentrated in the even mode due to symmetric constraint caused by air holes. Figure 5.4(a) shows dispersion diagram for even guided mode when 'A' is fixed at 0.28a while 'B' is varied from 0.36a to 0.44a. From figure 5.4(a) it is evident that the dispersion curves shift toward the higher frequency as the value of 'B' is increased. Moreover, with the increase in 'B' the dispersion curve becomes flatter at the high wave vector values. Similarly, when the semi-major axis 'B' is fixed at 0.40a and semi-minor axis 'A' is varied from 0.24a to 0.32a, the dispersion curve again shifts towards the higher frequency, as shown in Fig. 5.4(b). Keeping in view, the variation observed in the dispersion curves due to the change of semi-major and semi-minor axes of the elliptical air holes , the final parameters of the structure have been taken as 'A=0.28a' and 'B=0.40a' with 's = 0.3a' . Figure 5.5 shows the dispersion curve representing the even mode for the optimized structure. The band diagram for the optimized structure does not show any variation as compared to the basic structure for TE polarization.



(a) (b)

Figure 5.4 Variation of dispersion curve of slot even mode (a) when semi minor axis A is fixed and semi major axis B is varied (b) when semi major axis B is fixed and semi minor axis A is varied.

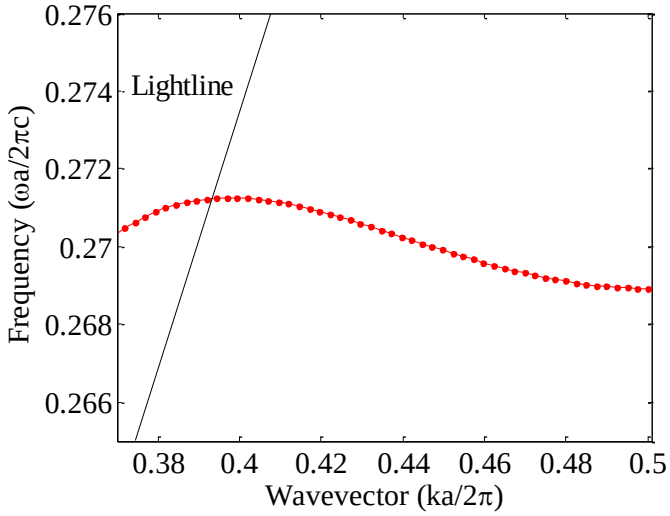


Figure 5.5 Dispersion relation representing the even mode for the optimized structure with values s=0.3a, A=0.28a and B=0.40a

5.4 Results and discussion

The key characteristic of a slow mode is its group velocity v_g, defined as the velocity with which the envelope of a short pulse propagates through space and calculated by the slope of the dispersion curve in the band structure diagram, i.e.

$$v_g = \frac{d\omega}{dk} \tag{5.1}$$

where, ω is the angular frequency and k is the wave propagation vector along the waveguide. For slow light devices, the two basic figures of merit commonly used to describe slow modes are the group index and slow down factor. The group index (n_g) is defined as the speed of the mode with respect to the speed of light in vacuum c i.e.

$$n_g = \frac{c}{v_g} = c\frac{dk}{d\omega} = \frac{d\left(ka/2\pi\right)}{d\left(\omega a/2\pi c\right)} \tag{5.2}$$

The slowdown factor S, is defined as the ratio of the phase velocity over the group velocity i.e.

$$S = \frac{v_p}{v_g} \tag{5.3}$$

The GVD parameter β is defined as the second-order derivative of the dispersion relation or derivative of the inverse group velocity with respect to angular frequency given by

$$\beta = \frac{d^2k}{d\omega^2} = \frac{1}{c}\frac{dn_g}{d\omega} = \frac{d}{d\omega}\left[\frac{1}{d\omega/dk}\right] = -\frac{1}{\left(d\omega/dk\right)^3}\frac{d^2\omega}{dk^2} = -\frac{1}{v_g{}^3}\frac{d^2\omega}{dk^2} \tag{5.4}$$

The equation 5.4 indicates the inverse relation of GVD parameter and group velocity. The increase of GVD (the decrease in group velocity) causes the spreading of the optical pulse. But the proposed structure has been optimized to exhibit low group velocity and low GVD parameter. Figure 5.6 shows the variation of group velocity and GVD parameter with respect to the normalized frequency for the slow slotted mode lying below the light line i.e. within the normalized frequency range of 0.2689-0.2713. The value of group velocity varies from 0.0017c to 0.0053c and GVD parameter lies in the range of 10^4 ps^2/km and has both negative and positive values. The flat section of the GVD curve has been considered as the extreme negative and positive values of GVD tend to seriously broaden the optical pulse width. Figure 5.6 shows that the flat section of GVD curve corresponds to the bandwidth range of $\Delta\nu = \frac{\Delta\omega}{2\pi}$ = 1.72 THz or Δλ=14nm. The maximum group velocity

(0.034c) and very low value of GVD (~ 1) have been achieved near the mid-frequency i.e. (ωa/2πc) = 0.2703. The very low GVD value has been obtained over the wide spectral bandwidth of 1.72 THz. Further, at 1.55μm, the slow down factor of S= 18.50 have been obtained.

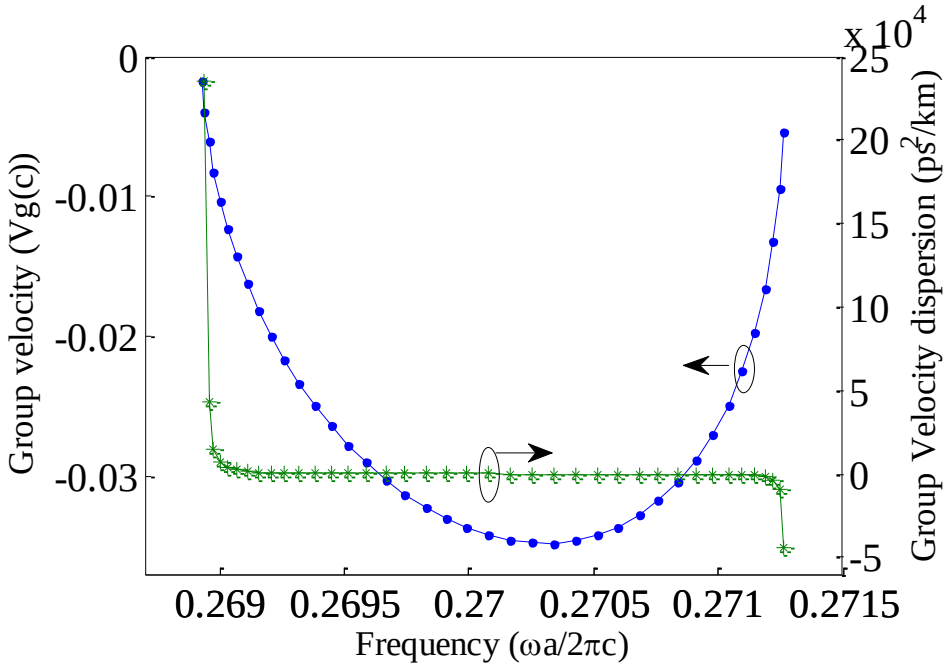


Figure 5.6 Variation of group velocity and group velocity dispersion with respect to the normalized frequency of the optimized structure

5.4.1 Applications

The optimized structure with both low group velocity and GVD has broad bandwidth and finds applications in optical buffer for storage of data and time and wavelength division de-multiplexing (TDM and WDM).

5.4.1.1 Optical Buffer

Another parameter namely the Delay Bandwidth Product (DBP) plays a significant role for the application of slow light in optical buffers. DBP represents number of bits that can be stored in a slow light device given by

$$DBP = T_d \bullet B \qquad (5.5)$$

where, T_d is the propagation time of a pulse in the waveguide and B is the bandwidth. For a particular length (L) of the waveguide and with minimum distortion of the propagating pulse, the upper limit on the DBP is given by

$$DBP = T_d \bullet B \le \frac{L}{\tilde{V}_g}\left(\frac{1}{4\pi L|\beta|}\right)^{1/2} \le \left(\frac{L}{4\pi}\right)^{1/2}\left(\frac{1}{\tilde{V}_g} \bullet \frac{1}{|\beta|^{1/2}}\right) \tag{5.6}$$

The equation 5.6 indicates that for a particular length of the structure, the DBP is inversely proportional to average group velocity and GVD parameter. Thus, to increase the value of DBP both the group velocity and GVD parameter should be less. The proposed SPhCW structure has been optimized to attain the upper limit of DBP. For normalized frequency ($\omega a/2\pi c$) = 0.2698 i.e. at a wavelength of 1.55μm, the value of average group velocity is 0.032c and GVD is 85.05 ps^2/km as calculated from figure 5.6. The calculated value of $\tilde{V}_g|\beta|^{1/2} = 0.29 cpskm^{1/2}$ is much less than that of $4.4 cpskm^{1/2}$ as reported in [105]. The observed value of $\tilde{V}_g|\beta|^{1/2} = 0.79 cpskm^{1/2}$ for the slowest velocity (0.0017c) achieved at normalized frequency ($\omega a/2\pi c$) = 0.2689 i.e at wavelength of 1.555μm is also less than that in reference [105,106]. Further to measure the buffering capacity, the normalized delay band width product (NDBP) has been calculated which is defined as

$$NDBP = n_g \bullet \frac{\tilde{\Delta\omega}}{\omega_0} \tag{5.7}$$

where, $\tilde{n}_g$ is the average group index in the frequency range Δω and can be calculated as

$$\tilde{n}_g = \int_{\omega_0 - \Delta\omega/2}^{\omega_0 + \Delta\omega/2} n_g(\omega)\frac{d\omega}{\Delta\omega} \tag{5.8}$$

where, ω_0 is the central normalized frequency. Figure 5.7 shows the variation of group velocity and group index with respect to the normalized frequency. From figure 5.7, the average group index has been obtained as $\tilde{n}_g$ = 71.24 and the NDBP has been calculated in the normalized bandwidth of $\Delta\omega/\omega_0$=0.0089 around central normalized frequency,

ω_0=0.2689 is 0.634. Despite the fact that in the proposed structure, light has been confined in the air slot, the value of NDBP is greater than that reported in the literature [105 - 107] where light propagates in the medium. Therefore, the proposed slotted waveguide based design can be used as an optical buffer without nonlinear effect.

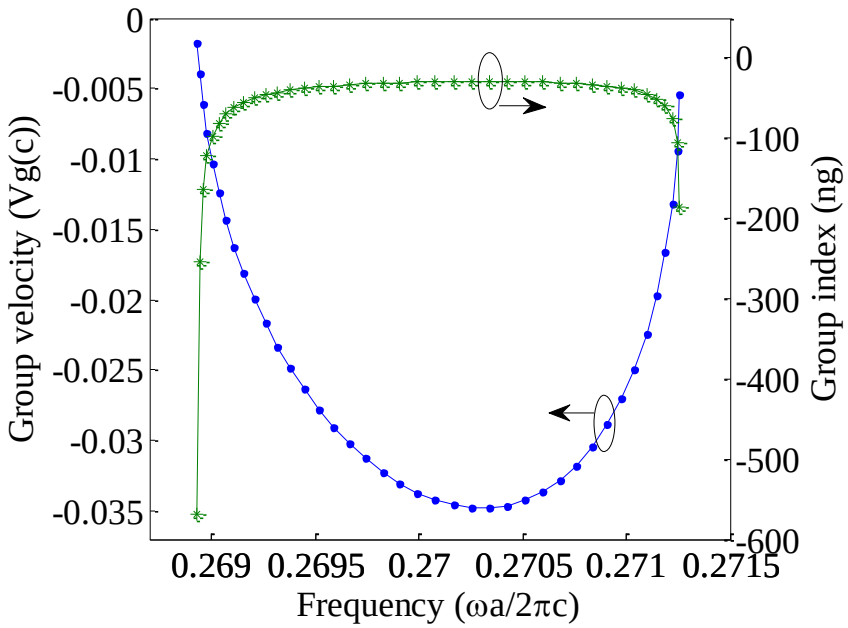


Figure 5.7 Variation of group velocity and group index with respect to the normalized frequency of the optimized structure

Similarly, figure 5.8 shows the variation of group velocity and GVD parameter with respect to the normalized frequency for the dispersion curve of odd mode lying below the light line. At a wavelength of 1.45µm, the group velocity and GVD parameter has been calculated to be 0.092c and 12.41 ps^2/km, which implies less distortion. Thus, the signal at a wavelength of 1.45µm travels three times faster than the signal at a wavelength of 1.55µm, where velocity is 0.032c. Since different wavelengths reach the output end at different times, this can be used in applications like TDM and WDM.

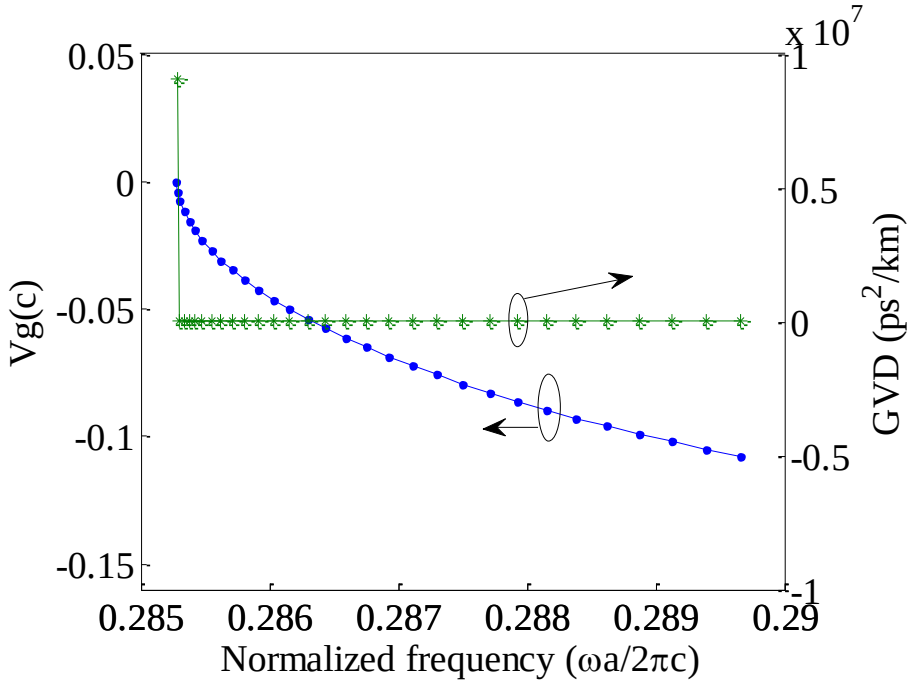


Figure 5.8 Variation of group velocity and group velocity dispersion with respect to the normalized frequency of the optimized structure

5.4.1.2 Time and wavelength division de-multiplexer

The optimized SOI based SPhCW structure has been investigated for its application as a (TDM and WDM). For the transmission length of 20a, the time delay between input and output peak at (ωa/2πc) = 0.2698 i.e. at a wavelength of 1.550μm has been calculated to be 0.87 ps which corresponds to the velocity of 0.032c as shown in figure 5.9. Similarly, for wavelength of 1.555μm at which slowest velocity has been achieved i.e. 0.0017c, the time delay has been calculated to be 16.40 ps. For a wavelength of 1.45μm the time delay has been found out to be 0.30 ps. Since different time delays have been achieved for different wavelengths, the proposed SPhCW structure can be used for both time and wavelength division de-multiplexer (figure 5.10).

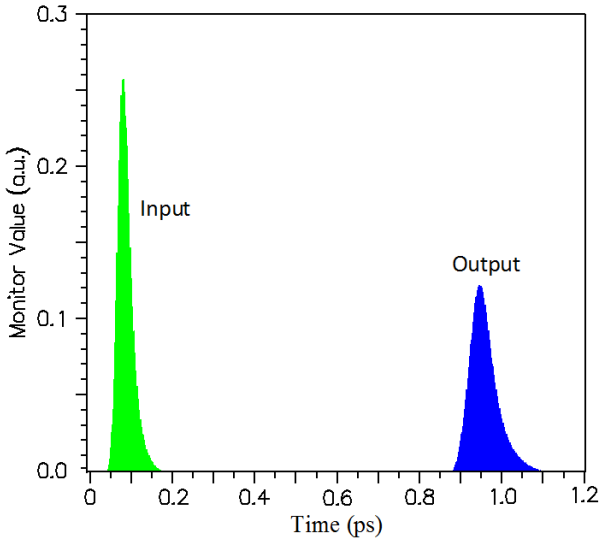


Figure 5.9 Time domain Gaussian optical pulse propagation in the slotted PhCW for λ=1.55µm

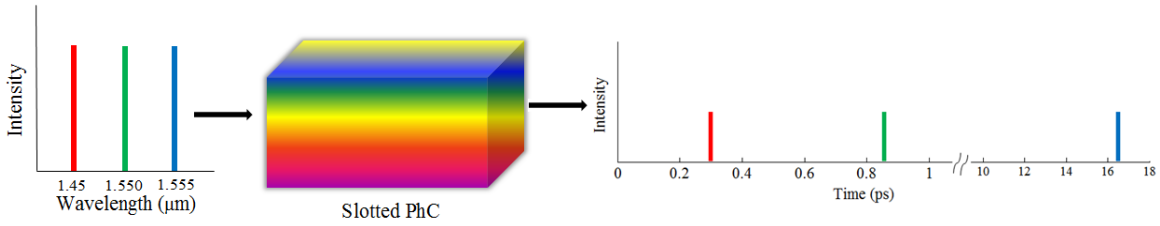


Figure 5.10 Schematic representation of pulse separation in slotted PhCW for time and wavelength division de-multiplexing at wavelength of 1.45µm, 1.550µm and 1.555µm

If we assume the device transmission length to be 600µm, the time delay for wavelength of 1.550µm and 1.555µm has been calculated and compared with the reported value in table 5.1. The improved time delay can be utilized for the effective de-multiplexing of the two wavelengths in the optical communication window and may find applications in the design and development of optical devices.

Table 5.1 Comparison of time delay between two wavelengths at transmission length of 600μm

Wavelength (μm)	Time delay (ps)	Difference in time delay	Reference
1.550	65	1165	Present work
1.555	1230		
1.550	57	647	[96]
1.555	704		

5.5 Conclusion

In this chapter, a new design of SPhCW on a SOI substrate with elliptical air holes in hexagonal arrangement has been reported. The low group velocity and low GVD with wide bandwidth range (0.0089) has been attained. The slow down factor of 18.50 shows the slow light behaviour in the optimized design. Though the light has been confined in the air slot, the high value of NDBP (0.634) has been achieved, which can be of high potential for the proposed waveguide to be used as an optical buffer without nonlinear effect. Also, the improved time delay of the waveguide finds application in the TDM and design of WDM devices in the optical communication window.

CHAPTER 6

Polarization splitter on silicon-on-insulator photonic crystal platform[5]

6.1 Introduction

In the previous chapters, it has been mentioned that photonic band gap guidance offers a platform for various applications. One of the important applications is PhC based polarization beam splitter. A polarization beam splitter is an important functional device in optical integrated circuits that splits the orthogonally polarized components of the guided waves. They have been widely used in many applications such as optical sensors [108], optical imaging [109], optical data storage [110] and optical communications [111]. Various types of polarization beam splitters have been implemented so far using Mach-Zehender interferometer [112], directional coupling [113-116], photonic crystal structures [8-9, 117], negative refraction [118], guided resonance [119], self collimation, photonic crystal ring resonators [120] and multimode interference [121-123]. Among these, some are relatively bigger and longer in size while others are relatively complex. Over the past decades, most of the proposed polarization beam splitters are based on two dimensional free standing photonic crystals [9, 117 and 124] which offer mass manufacturing possibilities due to their ultra small size, compactness and low loss. However, these polarization beam splitters have problems in mechanical stability. Recently developed 2D photonic crystals in silicon on insulator (SOI) platform provide a versatile platform for on chip device design as they provide higher mechanical stability and are easier to fabricate.

[5] Part of the results reported in this chapter has been published in the paper: "Complete photonic band gap based polarization splitter on silicon-on-insulator platform", Journal of Nanophotonics, 10(2), pp. 026023-1, 2016. http://dx.doi.org/10.1117/1.JNP.10.026023

In this chapter, a polarization beam splitter on SOI substrate based on photonic crystal directional coupler has been designed. The proposed design consists of honey comb lattice arrangement with two different air holes in SOI substrate as mentioned in chapter 4. The structure exhibits a complete photonic band gap for a range of wavelength that has been used for the design of the proposed polarization splitter. The characteristics of the polarization splitter have been analyzed by using the PWE method and the FDTD method. The coupling characteristics like extinction ratio, insertion loss, excess loss, coupling ratio and degree of polarization are enhanced as compared to the earlier reported results [125].

6.2 Structure design and analysis

A photonic crystal polarization beam splitter in SOI substrate has been designed as shown in figure 6.1. A honey comb lattice photonic crystal has been considered in order to obtain a complete photonic band gap. A honey comb lattice arrangement of air holes of two different radii on Si substrate of height 'h=0.25μm' has been chosen. The radius of larger and smaller air holes have been taken as R_b = 0.36a and R_s = 0.16a, respectively with lattice constant 'a =0.565μm'.

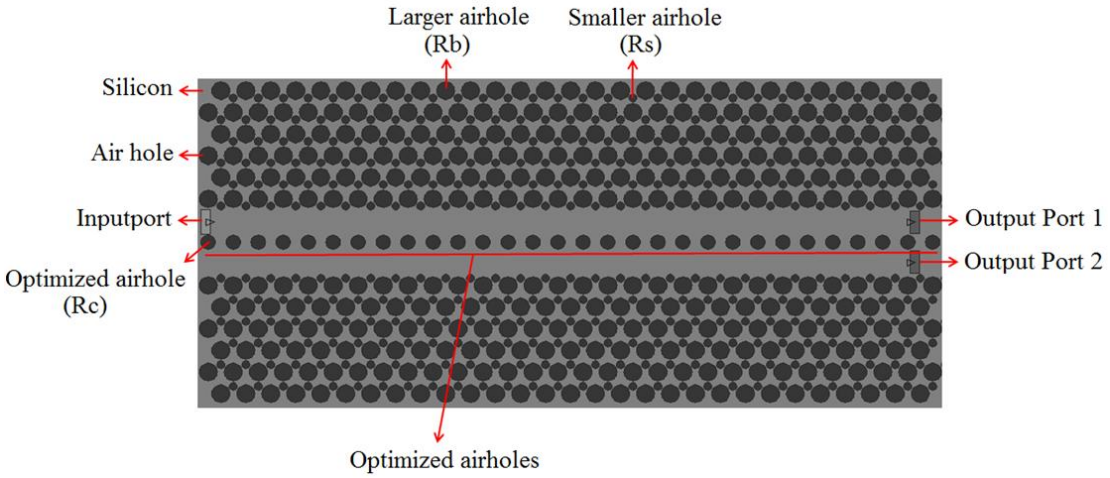


Figure 6.1 Schematic representation of the polarization splitter on SOI substrate where R_b and R_s represent the radius of the larger and smaller air holes and R_c represents the radius of the optimized air holes separating the two waveguides

The designed structure exhibits a complete photonic band gap within the normalized frequency range of 0.3520 – 0.3836 as shown in figure 6.2. The effective index

for TE mode and TM mode has been obtained to be n_{eff} (TE) = 2.89 and n_{eff} (TM) = 2.15 as calculated using FEM method [75]. Further, a waveguide directional coupler has been created in the proposed photonic crystal structure. To create a waveguide directional coupler, two closely spaced waveguides in the ΓK direction have been created and separated from each other by a row of air holes of radii (R_c). The radius R_c is smaller than the radius R_b and larger than the radius R_s.

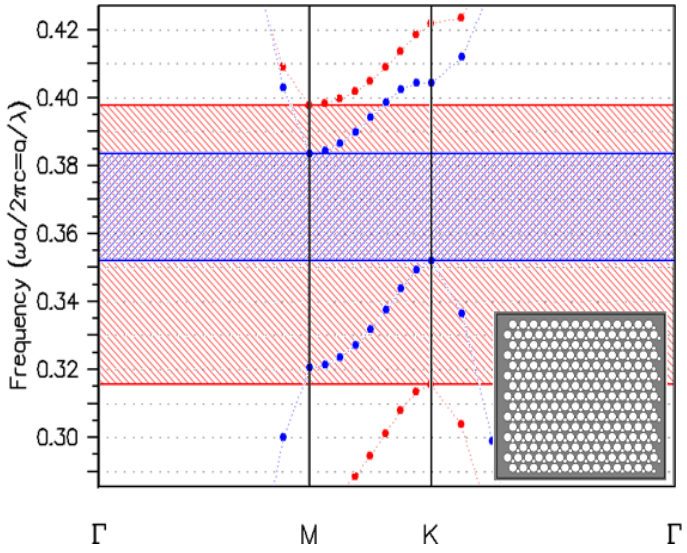


Figure 6.2 Photonic band diagram for the honey comb lattice arrangement, where red region corresponds to the TE polarization and blue region corresponds to the TM polarization

The dispersion diagrams for both TE and TM polarizations have been calculated using the PWE method. The variation of dispersion relation with the radius of the air holes separating the two waveguides for TE and TM polarizations has been shown in figures 6.3 and 6.4 respectively. From figure 6.4 it has been found that there are two modes for TM polarization i.e. one odd mode and one even mode whereas single mode is available for TE polarization as shown in figure 6.3. To design the proposed structure as a polarization splitter, a common frequency region has been chosen from the figures 6.3 and 6.4 where the defect modes for both TE and TM polarizations lie within the desired normalized frequency range.

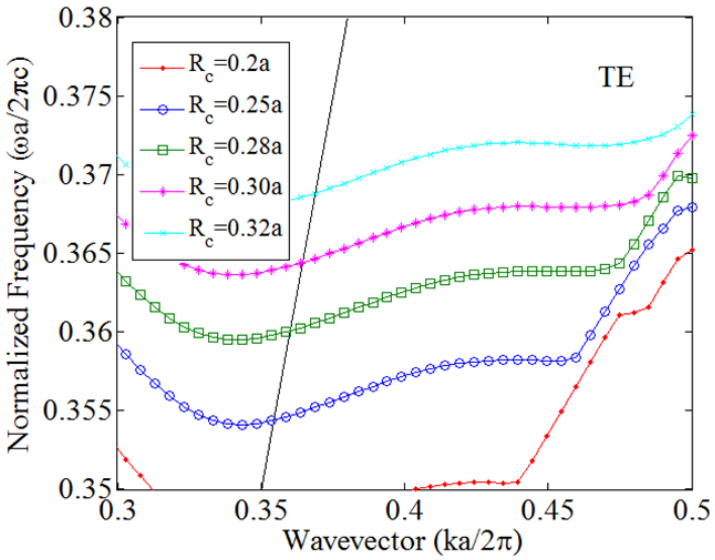


Figure 6.3 Dispersion relation of TE polarized modes with the radius of the central row of air holes separating the two waveguides

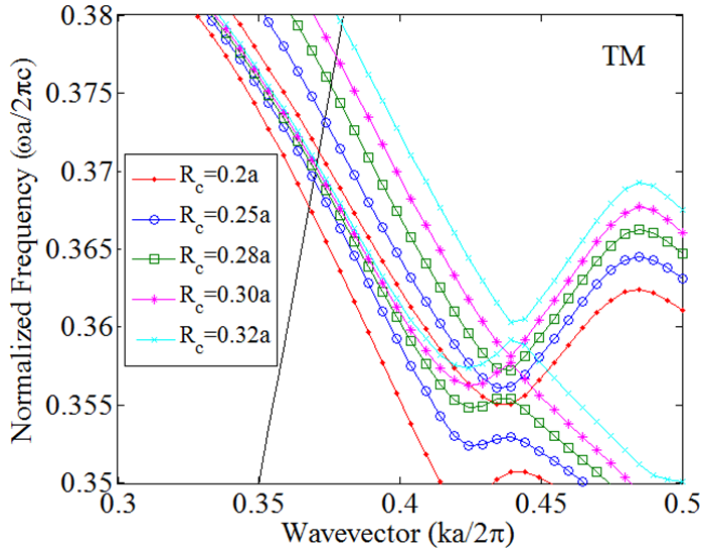


Figure 6.4 Dispersion relation of TM polarized modes with the radius of the central row of air holes separating the two waveguides

For different values of R_c only the normalized frequency range varies and not the performance of the proposed splitter. The figures 6.3 and 6.4 indicate that for radius R_c = 0.29a the defect mode for both TE and TM polarizations lie within a desired normalized frequency range of 0.3639 – 0.3651 as shown in figure 6.5. Figure 6.5 indicates that the structure exhibits a coupling region for TM polarization due to the presence of even and odd mode whereas no such region is exhibited for TE polarization which has only

one mode. The coupling length which is defined as $L = \frac{\pi}{|k_e - k_0|}$, where $k_e = 0.3873$ and $k_0 = 0.4108$ is the propagation constant of both the even and odd mode of the TM polarization respectively, has been calculated to be 12.02μm at R_c = 0.29a for a normalized frequency ωa/2πc = 0.3647 (i.e. at a wavelength of 1.55μm) using figure 6.5.

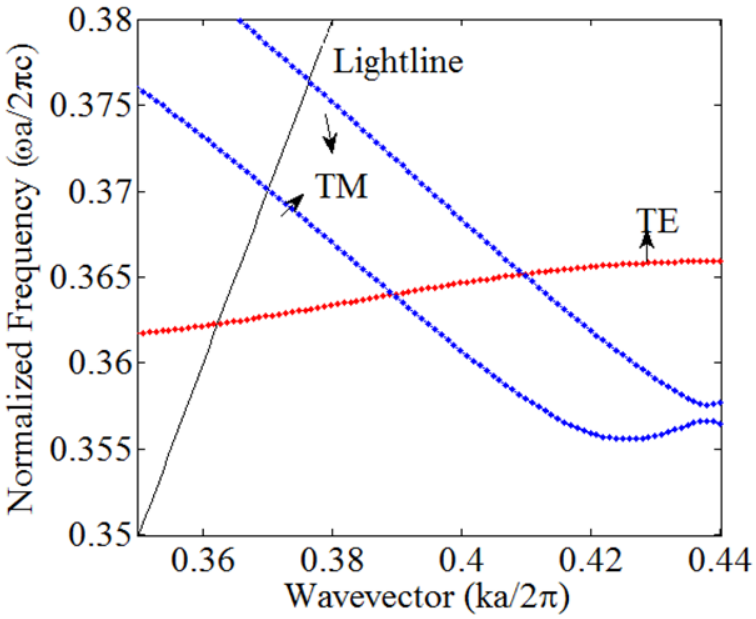


Figure 6.5 Dispersion relation at radius R_c = 0.29a of the central row of air holes separating the two waveguides for both the polarizations

The PWE results have also been verified using FDTD method. The variation of intensity in the proposed waveguide directional coupler has been obtained using the FDTD method as shown in figure 6.6 for both TE and TM polarizations. Figure 6.6 shows that at a distance of 12 μm, the wave/light with TM polarization couples to the another waveguide i.e. output port 2, whereas light with TE polarization continues to propagate in the same waveguide i.e. at the output port 1. Thus at a distance of 12 μm, a light with TM polarization is in cross state whereas the light with TE polarization remains in the bar state. Thus, the two polarizations can be separated at a distance of 12 μm.

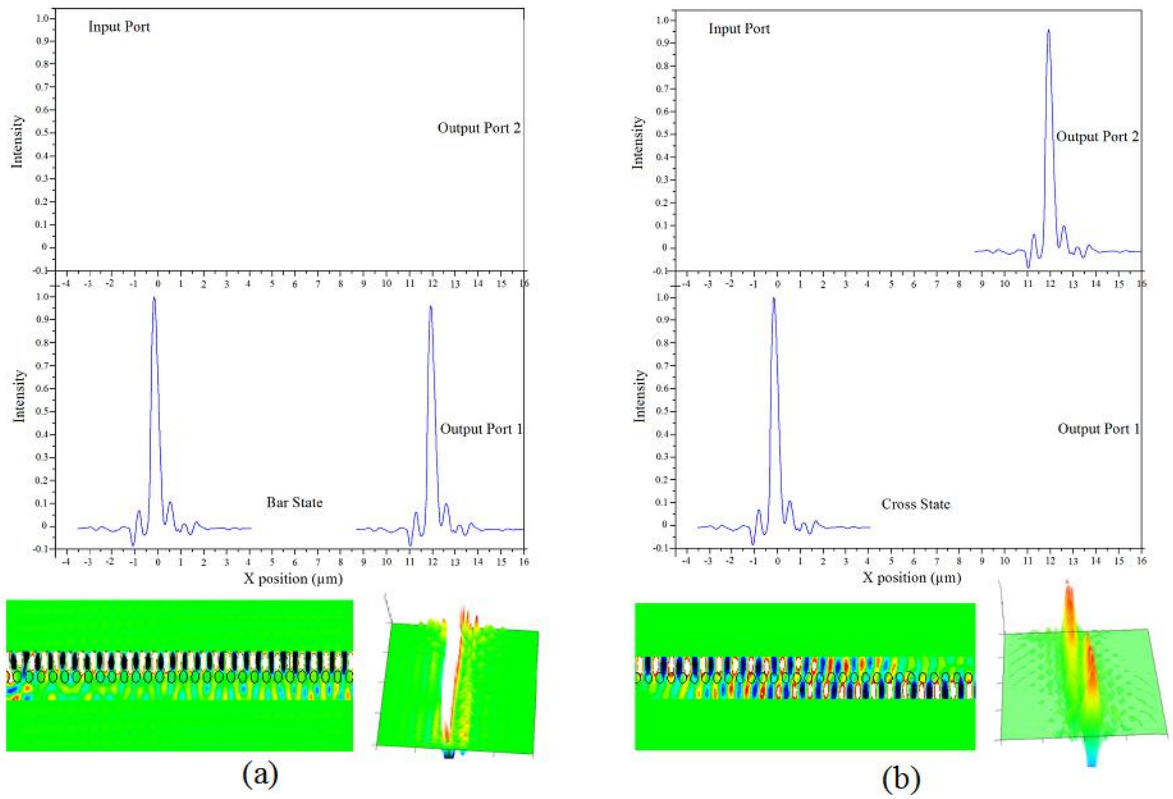


Figure 6.6 The intensity distribution at a distance of 12μm for (a) TE polarization and (b) TM polarization

6.3 Results and discussion

The proposed photonic crystal polarization splitter on SOI substrate can split the two polarizations at a distance of 12 μm as calculated using the PWE calculations and FDTD simulations at 1.55 μm. To further evaluate the performance of the polarization splitter, the intensity distribution obtained from the FDTD simulations has been analyzed for the calculation of extinction ratio, insertion loss, coupling ratio and excess loss. The extinction ratio for TE polarization and TM polarization has been calculated at a wavelength of 1.55μm which is defined as

$$ER_{TE} = 10\log_{10}\left(\frac{Power\ \ for\ TE\ \ at\ \ output\ \ 1}{Power\ \ for\ TE\ \ at\ \ output\ \ 2}\right) \tag{6.1}$$

$$ER_{TM} = 10\log_{10}\left(\frac{Power\ \ for\ TM\ \ at\ \ output\ \ 2}{Power\ \ for\ TM\ \ at\ \ output\ \ 1}\right) \tag{6.2}$$

The polarization splitter exhibits an extinction ratio of 24.56 dB for TE polarization (ER_{TE}) and 28.29 dB for TM polarization (ER_{TM}). The values of extinction ratio remain same within the desired wavelength range as shown in table 6.1. Hence, it has been concluded that the proposed design can work efficiently within the normalized bandwidth range as calculated by PWE method and FDTD method for both the polarizations.

Table 6.1 Comparison of the extinction ratio with wavelength for both TE and TM polarizations

Wavelength (μm)	ER_{TE} (dB)	ER_{TM} (dB)
1.5475	24.34	28.41
1.5485	24.45	28.35
1.5495	24.54	28.29
1.5505	24.58	28.30
1.5515	24.63	28.36
1.5525	24.67	28.33

The insertion loss (IL) defined as the ratio of input power to the output power in dB i.e.

$$IL = 10\log_{10}\left(\frac{Input\ Power}{Output\ Power}\right) \tag{6.3}$$

has been calculated to be 0.71 dB and 0.60 dB for TE and TM polarizations, respectively, at 1.55μm wavelength. Variation of insertion loss with wavelength for both TE and TM polarizations has been shown in table 6.2.

Table 6.2 Comparison of the insertion loss with wavelength for both TE and TM polarizations

Wavelength (μm)	IL_{TE} (dB)	IL_{TM} (dB)
1.5475	0.88	0.47
1.5485	0.77	0.54
1.5495	0.73	0.60
1.5505	0.64	0.59
1.5515	0.59	0.57
1.5525	0.55	0.56

The excess loss defined as the ratio of input power to the total output power in dB i.e.

$$EL = 10\log_{10}\left(\frac{Input\ Power}{Total\ output\ Power}\right) \tag{6.4}$$

for the proposed structure has been calculated to be -2.36 dB at a wavelength of 1.55μm. The comparison of excess loss with wavelength has been calculated and mentioned in table 6.3.

Table 6.3 Comparison of the excess loss with wavelength

Wavelength (μm)	EL (dB)
1.5475	-2.34
1.5485	-2.36
1.5495	-2.37
1.5505	-2.40
1.5515	-2.46
1.5525	-2.46

The corresponding coupling ratio defined as the ratio of optical power from one output port to the total output power, in percentage has been found to be 49.19% for TE polarization and 50.55% for TM polarization at a wavelength of 1.55μm. The degree of polarization P in each output port has also been calculated using the definition of P as

$$P = \frac{\left|P_{TE} - P_{TM}\right|}{\left|P_{TE} + P_{TM}\right|} \tag{6.5}$$

where, P_{TE} is the power for TE polarization and P_{TM} is the power for TM polarization. The degree of polarization for TE mode and TM mode has been calculated to be 99.29% and 99.70%, respectively. Thus, the optimized design can efficiently split the two polarizations at a distance of 12μm. Hence, the proposed design can be used as a polarization splitter for on chip integrated devices.

6.4 Conclusion

In this chapter, a novel design for the polarization beam splitter in silicon on insulator substrate consisting of honey comb lattice arrangement of air holes of different radii has been demonstrated. The proposed design is based on the concept of photonic crystal directional coupler exhibiting complete photonic band gap. The structure finds strong applications in the future on chip polarization splitters owing to its miniature size and easy fabrication capabilities using recent technologies.

CHAPTER 7
Conclusion and Future Scope

All optical data processing information in optical networks is an important research area during the last decades. All optical network elements eliminate the use of electronic to optical conversion because maximum communication networks use light pulses to be intensified, renewed and transformed into electronic signals and then again transformation into light signals. Recently, the demand of high bandwidth optical switches has rapidly increased due to the removal of multiple conversions of signals from an optical to electrical signal. The optical logic gates are key elements to realize all-optical functions. They have certain advantages over the electronic logic gates such as they are more compact, immune to short circuits, immune to electronic interference. They have low transmission loss, more band width and use more efficient parallel computing. Thus it is necessary to develop several designs of all-optical logic gates at the same platform without the implementation of complex electro-optic conversions.

In this thesis, different architectures have been proposed for all optical logic gates. Initially different schemes for an optical logic gate architecture have been proposed to perform AND logic gate. The proposed structures consist of three schemes one of which is silicon rods in air, and other two are air holes in silicon with air waveguide and air holes in silicon with material waveguide. The AND logic gates are simple and are implemented using hexagonal lattice arrangement in photonic crystal. The contrast ratio, response time and bit rate have also been analyzed for all the logic gates. The structures are simple and their potential for integration makes them an interesting approach in photonic computing and optical signal processing.

Another type of logic gates relies on the changes in phase difference between two input signals and reference signal. The light beams interfere either constructively or destructively based on the phase angle of the light beam launched at reference waveguide. Further, the use of polarization independent wave guidance in photonic crystals improves

the performance of all-optical logic gates. The technique of using combination of universal logic gates for the design of all-optical logic gates lead to the development of the prototype of the electronic logic gates.

This thesis also focuses on the achievement of slow light in slotted photonic crystal wave guide where light is confined in the low index region as compared to the conventional photonic crystal material waveguide. The slow light in slotted photonic crystal waveguide has strong possibility to be used as an optical buffer and optical storage devices without any material losses. The confinement of light in low index slot waveguide with slow light can be useful in sensor applications where there is an enhancement of interaction between slow light and measuring samples.

A simple and effective way towards the analysis of the design of polarization splitter based on the phenomenon of directional coupler in photonic crystal has also been demonstrated in the present thesis. It would be interesting to obtain high extinction ratios which provide the possibility of realizing polarization insensitive large scale integrated optoelectronic systems.

The optical logic gates presented in this thesis are extremely fast as compared to their electronic counterparts and hence can be used to manufacture optical computers having unimaginably high processing speed (~THz) which is only a dream with today's computer technology. A complete logic family can be developed in near future based on the proposed optical logic gates, which can further facilitate the development of all-optical signal processors. Therefore the need of optical to electronic signal conversion will come to an end and the data could be directly processed and transmitted. In light of work carried out in this thesis, following future work can be carried out:

- Design of all-optical flip flops on SOI platform using photonic crystals.
- Design and analysis of all optical transistors on SOI photonic crystal platform.
- Reversible logic gates can be designed on photonic crystal platform which shall have the ability to reduce the power dissipation which is the main requirement in low power VLSI design. They have wide applications in low power CMOS and optical information processing systems, DNA computing and quantum computation.

- A slotted waveguide is used as an antenna in microwave radar applications, which have no reflectors but emits light directly through the slots. So in near future slotted photonic crystal wave guide can also be used to design antennas for specific applications. Further, the device performance can be enhanced using slow light effect in metal based photonic crystal slotted waveguides.

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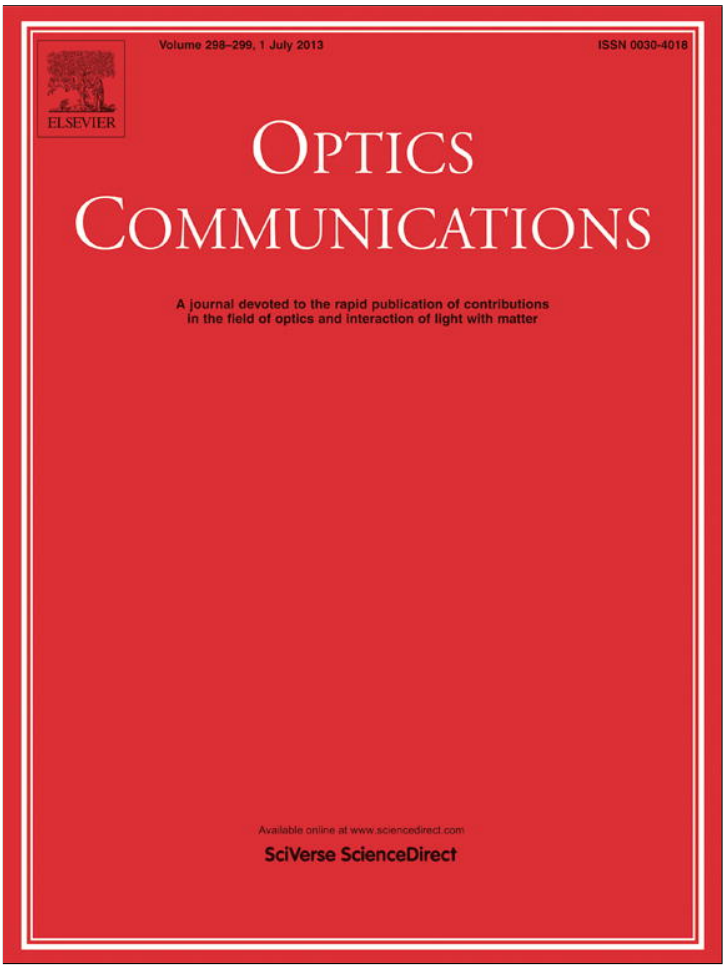

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Realization of AND gate in Y shaped photonic crystal waveguide

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ABSTRACT

We report the design of an AND optical logic gate based on two dimensional triangular lattice of air holes in Si. The proposed structure consists of Y-branch waveguide without nonlinear materials and optical amplifiers. The simulation results show that the proposed all optical structure could really function as an AND logic gate. This structure is favorable for large scale optical integration and can potentially be used in on-chip photonic logic integrated circuits.

1. Introduction

Photonic crystal (PhC) is a versatile platform to construct devices with dimensions of a few wavelengths of light being confined and have emerged as one of the most significant topic in the field of optical communication. They have some unique properties such as compactness, high speed, low power consumption and better confinement.

Recently all optical logic gates have received much attention for their applications in real time optical processing and information communications [1–12], because all optical signal processing can handle large bandwidth signals, large information flows and have no need of electrical to optical conversion. In recent years different schemes have been demonstrated for the designing of all optical logic gates using nonlinear effects in optical fibers [13–15] and in waveguides [16–18], but most of these works suffer from certain limitations such as big size, low speed and difficult to perform chip-scale integration. As logic gates are capable of performing many logic functions and have many applications in optical communication, photonic microprocessors, optical signal processors and optical instrumentation. Thus photonic crystal based all optical logic gates are considered as key elements in future photonic integrated circuits and such optical devices have attracted significant research in recent years. Most of the recent research work is based on material rods assembled in air with air cladding on both sides [19–22] i.e. the PhC structures are freely suspended in air. These air-bridge structures having air cladding on both sides are mechanically unstable from practical perspective as well as not suitable for future integrated circuits [23–24] and large scale integration. Structures with solid support are more realistic and suitable. To the best of our knowledge, no optical logic gates have been proposed in two dimensional photonic crystal structures (2D PhC) composed of air holes in silicon (Si). In this paper, we have proposed the design of AND logic gate based on two dimensional triangular lattice photonic crystals composed of air holes in Si with Y-shaped PhC waveguide. Optical AND gate has many applications, such as, AND logic gate is used to perform address recognition, packet-header modification, and data-integrity verification. AND gate also serves as a sampling gate in optical sampling oscilloscopes owing to their ultrafast operation compared to the traditional electrical methods. The structure proposed for the realization of AND logic gate is a line defect induced symmetric Y-branch waveguide. Earlier many applications have been realized on Y-shaped waveguide, such as, demultiplexer [25–26] and XOR logic gate [27]. The simulation results show that the proposed optical photonic crystal waveguide structure could really function as AND logic gate. By appropriately choosing the size of the holes at the center of the Y shaped waveguide the optimal performance for the proposed AND logic gate has been achieved.

2. Model and operating principle of AND logic gate

Fig. 1 shows the design of an all optical AND logic gate on the platform of 2D PhC. In the schematic indicated in Fig. 1 symmetric Y-shaped waveguide is formed and a hole is introduced at the

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center of the three waveguides. The proposed two dimensional photonic crystal structures consist of $15a \times 15a$ two dimensional triangular lattices. The refractive index of silicon (Si) is equal to $n=3.5$. The radius of air holes is ($r=0.4a$), where "a" is the lattice constant. According to the band diagram (shown in Fig. 2) of our proposed structure as calculated by the plane wave expansion (PWE) method, light with wavelengths between 1.166 μm and 1.926 μm for TE modes cannot pass through the uniform PhC structure and thus is completely reflected. In Fig. 1 the input signals are coming from the left lower and upper waveguides indicated as input port A and input port B. Output signals are obtained from the right port of the horizontal waveguide. AND gate encompasses of two input signals and an output signal. The output is logically "1" if and only if both of the input values are 1. For AND gate the radius of the central hole is optimized in such a way that for a single input as well as for both the inputs maximum power is obtained at the output port. Optimization of the structure is also carried out for increasing transmittance from output waveguide with wavelength. Transmittance (T) is defined as the ratio of output intensity obtained from the output waveguide to the incident intensity at the input waveguides, i.e. $T=I_{out}/I_{in}$. Fig. 3 shows the spectral response of proposed AND gate for TE like polarization of incident light from single input port and Fig. 4 for both the input ports. In Fig. 3, transmittance has been shown with respect to the wavelength when incident light is launched at one of the two input ports. Similarly Fig. 4 represents transmittance with respect to the wavelength of incident light launched at both the input ports. The contrast ratio

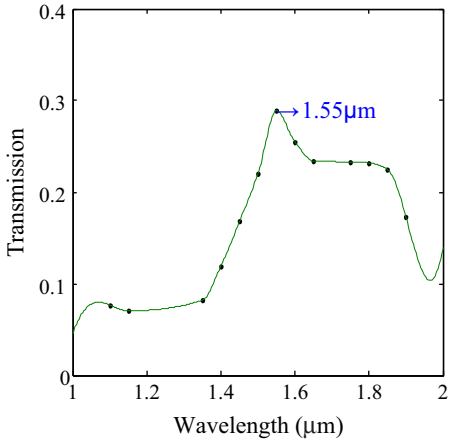

Fig. 3. Variation of transmittance with wavelength from the output waveguide for the single input signal for TE like polarization of incident light.

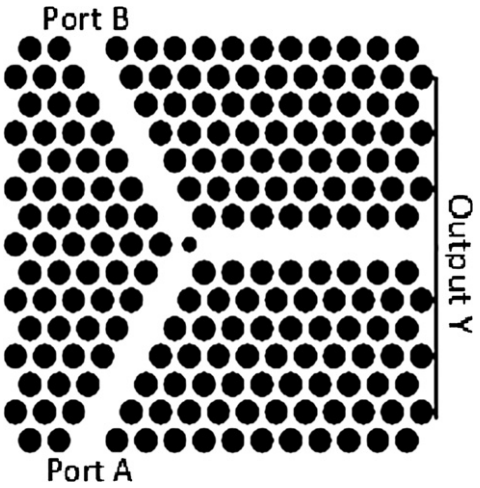

Fig. 1. Schematic of all-optical "AND" logic gate.

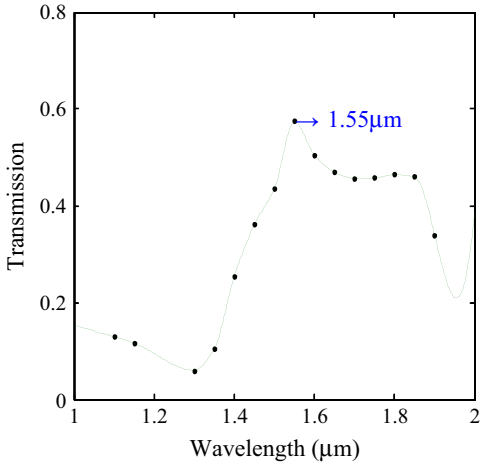

Fig. 4. Variation of transmittance with wavelength from the output waveguide for both the input signals for TE like polarization of incident light.

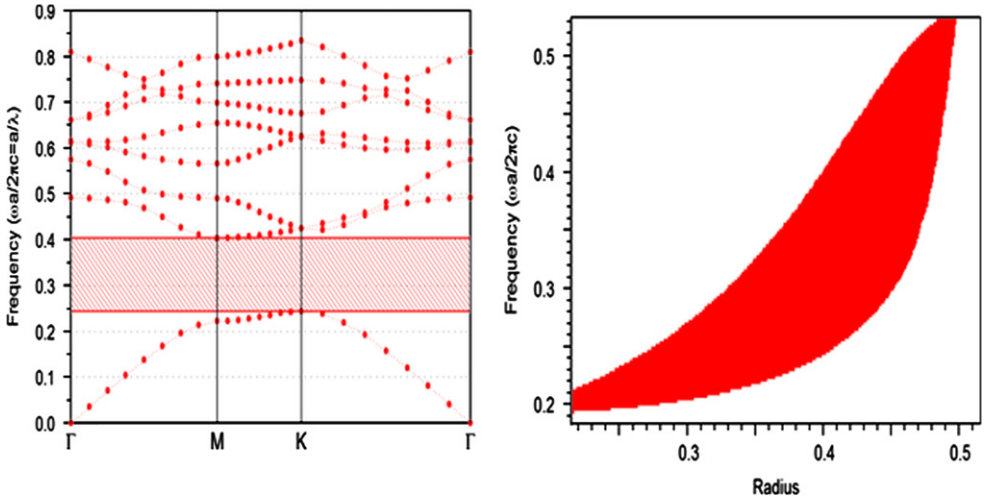

Fig. 2. Band gap structure of the photonic crystal layout.

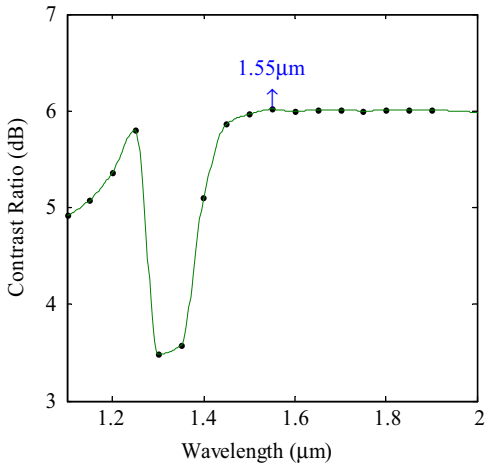

Fig. 5. Contrast ratio versus the normalized operating wavelength.

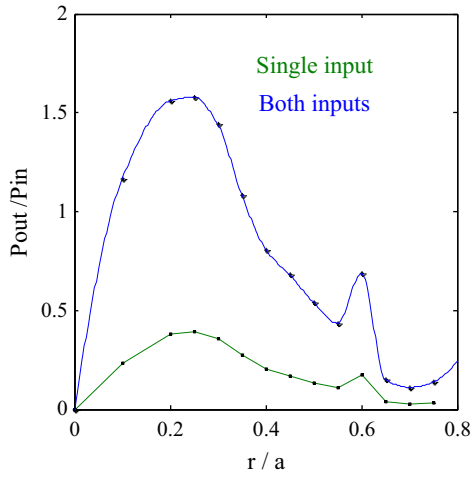

Fig. 6. Power transmittance versus the normalized radius of the central hole in the cavity.

Table 1
Truth table for AND logic gates where output Y is in terms of input power P_a

Input A	Input B	Logic output	Output Y
0	0	0	0
0	1	0	0.395 Pa
1	0	0	0.395 Pa
1	1	1	1.580 Pa

has also been calculated, i.e. Contrast ratio $= 10\log(P_1/P_0)$ dB, where P_1 represents power for logic-1 and P_0 represents power for logic-0. Fig. 5 shows the variation of contrast ratio with respect to the wavelength. Figs. 3–5 clearly show that the optimized structure can be best worked out at the normalized operating wavelength 1.55 μm which lies in optical communication range. The response time [28,29] for the proposed logic gate structure has also been calculated.

3. Optimization of the radius of the hole at the center of the three waveguides

To obtain the reasonable initial value of the radius of the hole at the center of waveguides, the radius of all the other holes except for the central hole has been taken as $r = 0.4a$. The radius of central hole has been scanned when one of the input signals as well as both the input signals are 1. Fig. 6 indicates that, as radius of central hole increases, the output power increases to a maximum value for both the input signals as well as for the single input signal. From Fig. 6 it is evident that as the value of radius is increased beyond $0.25a$ power at the output port goes on decreasing. Hence the radius of hole at the center is to be taken as $r_c = 0.25a$.

4. Results and discussion for AND gate

The proposed optimized structure ($r_c = 0.25a$ and $r = 0.4a$) has been simulated using the finite difference time domain (FDTD) method and the input ports have been excited by continuous wave sources with power P_a. For simulation and optimization of the structure shown in Fig. 1, the finite difference time domain method with perfectly matched boundary conditions has been employed to absorb waves and avoid reflections at the boundaries. The magnetic field polarization of the wave has been chosen to be parallel to the y-axis, which is the axis of air holes in Si and the wave propagates in the (x, z) plane. Convergence of the simulations has been done according to the given rule, i.e. $\Delta x < \lambda/10$ and $\Delta z < \lambda/10$ where x and z axes are the horizontal and vertical direction coordinates and the axis of holes is along y direction. The space grid and the time grid has been chosen such that the structure meets the requirement of courant condition which is given by the equation $c\Delta t < 1/\sqrt{\Delta x^{-2} + \Delta z^{-2}}$, where c is the speed of light in medium. We first apply continuous wave signal at ports A and B separately and then simultaneously at both the input ports A and B with power P_a. It has been found out that output power is $0.395P_a$ for separate excitation with power P_a at input port A as well as for separate excitation at input port B. For simultaneous excitation with power P_a at both input ports A and B the output power obtained is $1.580P_a$.Thus the system performs as an AND gate as summarized in Table 1. Table 1 shows the truth table for the proposed optical AND logic gate.

From Fig. 5 it has been found out that the contrast ratio between logic-1 output power and that for logic-0 is 6.017 dB at the normalized operating wavelength ($\lambda = 1.55$ μm) which lies in the optical communication range. The field distribution at steady state for all combinations has been shown in Fig. 7 which exhibits the operation of the proposed structure of an AND gate.

The response time of the proposed optimized optical AND logic gate has been determined using the time evolving curve of the output power similar to [29] and shown in Fig. 8.

From Fig. 8, it has been concluded that the time for the output power to reach from 0% to 90% of the average output power P_{av} in the final steady state is $ct = 54.1$ μm or $t = 0.63$ ps. The time "t" consists of two parts one of which is time due to transmission delay i.e. $t_1 = 0.330$ ps and another is the time for the output power to climb from 0.1% P_{av} to 90% P_{av} is found to be $t_2 = 0.301$ ps. As the system operates on linear material, hence it is expected that the falling time from average output power P_{av} to 10% P_{av} is approximately equal to t_2.Thus a narrow pulse with a width of $2t_2 = 0.602$ ps can be produced. Hence, the response period of the signal is obtained to be 1.204 ps, i.e. the proposed AND logic gate can operate at a bit rate of 0.830 Tbits/s.

5. Conclusion

In this paper we have proposed the design for all optical AND logic gate based on Y-shaped photonic crystal architecture. The device performance has been analyzed by PWE method and

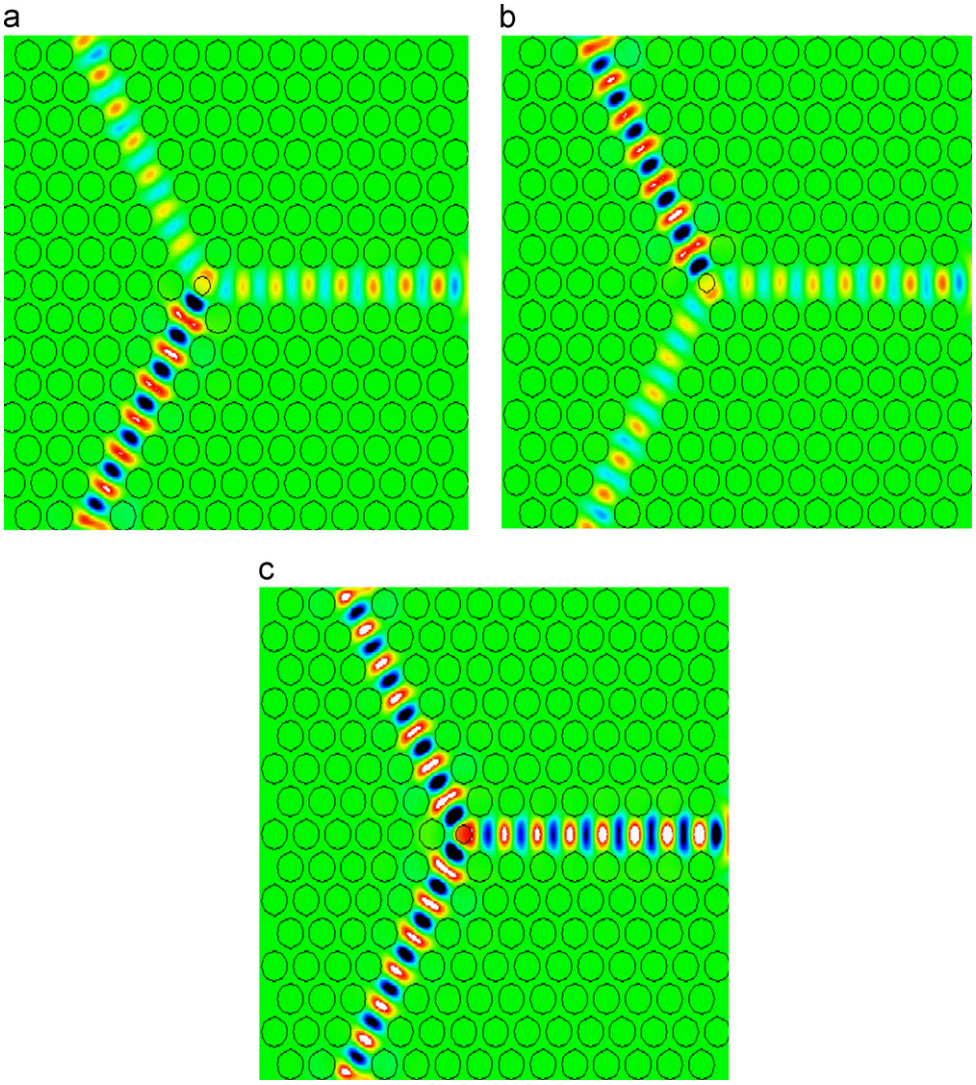

Fig. 7. Field distributions at steady state of the "AND" logic gate for (a) $A=1$, $B=0$; (b) $A=0$, $B=1$ and (c) $A=1$, $B=1$.

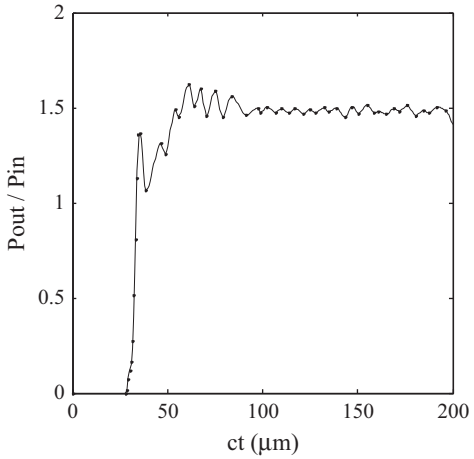

Fig. 8. Time evolving curve of the output power.

simulated using the FDTD method. The method of determining the operating parameters has been explained and the optimized parameters are obtained for achieving high contrast ratio. In this paper, the design of the AND logic gate is based on linear characteristics of the material and hence it can operate at very low powers. It is expected that such a design will help in realizing devices and components for broadband optical communication systems and networks. The proposed structure could be the strong candidate for future photonic crystal based all optical logic gates.

Acknowledgments

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Design of all optical logic gates in photonic crystal waveguides

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ABSTRACT

In this paper, we report the design of all optical logic gates based on two-dimensional photonic crystal (PhC) composed of triangular lattice of air holes in silicon (Si). The proposed structure has been simulated using finite difference time domain (FDTD) method and it has been shown that all optical logic operations can be achieved if an appropriate initial phase is introduced between the input beams so that they may interfere constructively or destructively. The optical logic gates designed in the proposed structure have a response period of 1.024 ps and can operate at a bit rate of 0.976 Tbit/s.

1. Introduction

Logic gates and devices play a basic, critical and important part in modern electronics and integrated circuits. Recently, all optical logic gates have received considerable attention for their applications in optical communication networks, due to their importance in addressing, switching, encryption, data encoding, signal regeneration, header recognition and contention resolution. In recent years different schemes have been demonstrated for the designing of all optical logic gates based on linear optical effects such as, interferometry [1], semiconductor optical amplifier (SOA) [2] and Mach-Zehnder interferometer (MZI) [3] and nonlinear processes which include electro-optical effect [4,5], thermal-optical effect [6], two-photon absorption [7] and third-order nonlinear effect [8,9]. Logic gates are capable of performing many logic functions and have numerous applications in optical communication, such as, AND logic gate is used to perform address recognition, packet-header modification, and data-integrity verification and also serves as a sampling gate in optical sampling oscilloscopes. XOR gate can perform functions like comparison of data patterns for address recognition, packet switching, data encryption/decryption, parity checking and optical generation of pseudorandom patterns. NOT gate can be used as inverter or switch and XNOR logic gate is used to realize the threshold detector functionality. In this paper, we have proposed the design of all optical logic gates based on two-dimensional photonic crystals composed of triangular lattice of air holes in Si. Till now many logic gate designs have been proposed which consist of Si rods in air [10–13] but those designs are not practical from the point of view of sustainability and fabrication. Photonic crystal composed of air holes in silicon is a more practical structure and has been used in the design of optical logic gates [14,15] and nano photonic devices [16,17]. The proposed optical logic gates are based on the phenomenon of optical interference effect and are designed in two dimensional photonic crystal waveguides composed of air holes in silicon. The simulation results show that the proposed all optical photonic crystal waveguide structure could really function as all optical logic gates. By appropriately choosing the size of the air hole at the center of the four PhC waveguides the optimal performance in terms of response time, bit rate and contrast ratio for the proposed optical logic gates has been obtained.

2. Design and operating principle of all optical logic gates

In this paper, the design for all optical logic gates has been proposed based on the platform of 2D PhC. The proposed two dimensional photonic crystal structure, as shown in Fig. 1 consists of $15a \times 15a$ two dimensional triangular lattice composed of air holes in silicon having refractive index $n = 3.5$. The radius (r) of air holes is $0.3a$, where, 'a' is the lattice constant equal to 0.352 μm. According to the band diagram of the bulk PhC as shown in Fig. 2, light with wavelength range of (1.291–1.715 μm) for TE modes cannot pass through the uniform PhC structure. In the proposed design four waveguides have been created, from which two of them are considered as input ports indicated as port A and port B. As shown in Fig. 1, one port has been indicated as reference port R which is used to create phase difference between input signals resulting into constructive or destructive interference. Output signals are obtained

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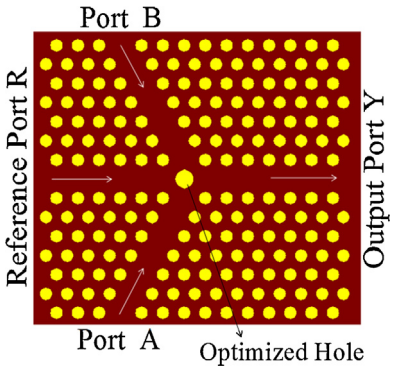

Fig. 1. Schematic representation of all-optical logic gates.

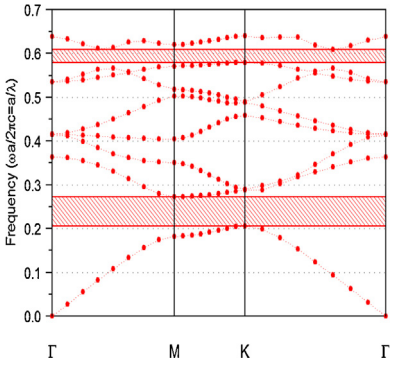

Fig. 2. Band gap structure of the photonic crystal layout.

from the right port indicated as output port Y. Further, in the proposed structure a hole has been introduced at the center of the four waveguides. For the design of all optical logic gates the radius of the central hole is optimized in such a way that for a single input (along with reference signal) as well as both the inputs (along with the reference signal) maximum power is obtained at the output port Y. For the proposed structure, transmittance (T) which is defined as $T = I_{out}/I_{in}$ has also been calculated, where 'I_{out}' is the intensity of light received at the output port Y and 'I_{in}' is the intensity of light launched at the input port. The spectral response of proposed logic gates for TE like polarization of incident light from single input port (with reference signal) as well as for both the input ports (with the reference signal) has been shown in Figs. 3 and 4. Fig. 3 shows the transmittance with respect to the wavelength when the incident light is launched at one of the two input ports with the reference signal having same phase with the input signal. Similarly, Fig. 4 represents the transmittance with respect to the wavelength of

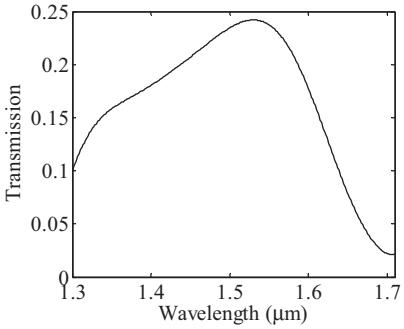

Fig. 3. Variation of transmittance with wavelength from the output waveguide for the single input signal along with the reference signal for TE like polarization of incident light.

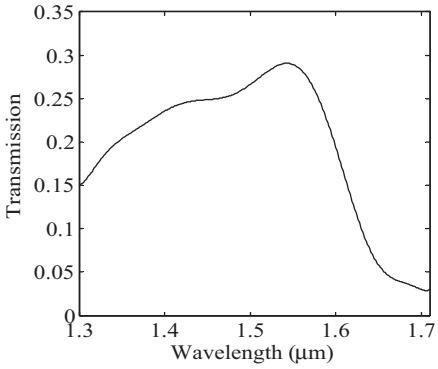

Fig. 4. Variation of transmittance with wavelength from the output waveguide for both the input signals along with the reference signal for TE like polarization of incident light.

incident light launched at both the input ports with the reference signal having same phase as that of the input signals. The contrast ratio defined as $10\log(P_1/P_0)$ (dB) has also been calculated for all optical logic gates, where P_1 represents the power for logic-1 and P_0 represents the power for logic-0. Fig. 5 shows the defect modes that exist within the band gap range. From Figs. 3–5 it has predicted that the optimized structure can be best worked out at the normalized operating wavelength of 1.55 μm which lies in optical communication range. The response time for the proposed structure has also been calculated and plotted [18,19].

3. Optimization of the radius of the hole at the center of the four waveguides

The radius of central hole has been optimized when one of the input signals as well as both the input signals, along with the reference signal are unity and has zero phase difference. From the optimization curve for the radius of the central hole as shown in Fig. 6, it has been observed that as the radius of the central hole increases, the output power increases to a maximum value and then decreases for both the input signals as well as for the single input signal along with the reference signal. Hence the optimized radius of the air hole at the center of four waveguides has been taken as $r_c = 0.44a$.

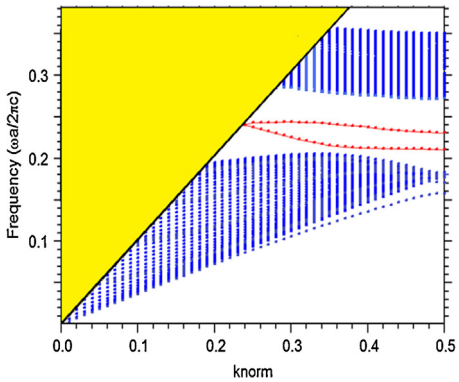

Fig. 5. Dispersion relation for all the four involved PhC waveguides. The black solid line corresponds to the light line and the red dotted lines inside the band gap region correspond to the respective guided modes for TE polarization in all the waveguides. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

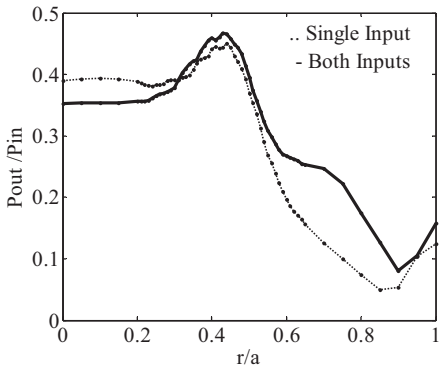

Fig. 6. Normalized power transmittance versus the normalized radius of the central hole in the four PhC waveguides.

4. Simulation and results

After the optimization of the proposed structure to work as all optical logic gates, results have been realized using FDTD method and perfectly matched layer (PML) has been applied to meet the requirements of the courant condition. The input ports A, B and reference port (R) for single input launch as well as for both input launches have been excited by continuous wave (CW) signal with power P_o. Reference signal has been used to optimize the logic output of all the logic gate combinations. For the realization of all the logic gates the radius of central hole has been taken as $r_c = 0.44a$ and the radius of all the other holes as $r = 0.3a$.

4.1. For AND gate

With initial value of $r_c = 0.44a$ and $r = 0.3a$, firstly the function of optical logic AND gate has been demonstrated. In the proposed structure AND gate encompasses of two input signals, a reference signal and an output signal. The AND logic gate operates as follows: (i) when input port A is launched with light having phase angle $\Phi = 0^\circ$ and reference port with light having phase angle $\Phi = 180^\circ$ then logic 0 is obtained at the output port Y. (ii) Similarly, when input port B is launched with light having phase angle $\Phi = 0^\circ$ and reference port with light having phase angle $\Phi = 180^\circ$ then also logic 0 is obtained at the output port Y. (iii) When both the input ports A and B are excited with light signal having phase angle $\Phi = 0^\circ$ and reference port with light also having phase angle $\Phi = 0^\circ$ then logic 1 is obtained at the output port Y. The results are summarized in Table 1 and field distributions for all possible combinations have been shown in Fig. 7. It has been predicted that the gate can operate at a wavelength of 1.55 μm and the calculated value of contrast ratio is found out to be 8.76 dB.

4.2. For OR gate

After the optimization of all the required parameters OR gate has been demonstrated. For OR gate the output is '0' if and only if both the input values are 0 otherwise output values are 1. The operation of OR gate is as follows: (i) when input port A is launched with light having phase angle $\Phi = 0^\circ$ and reference port with light also having phase angle $\Phi = 0^\circ$ then logic 1 is obtained at the output port Y. (ii) Similarly, when input port B is launched with light having phase angle $\Phi = 0^\circ$ and reference port with light having phase angle $\Phi = 0^\circ$ then also logic 1 is obtained at the output port Y. (iii) When both the input ports A and B are excited with light signal having phase angle $\Phi = 0^\circ$ and reference port with light also having phase angle $\Phi = 0^\circ$ then logic 1 is obtained at the output port Y. For the OR gate realization, the presence of same phase angle between the input signal and reference signal results into the constructive

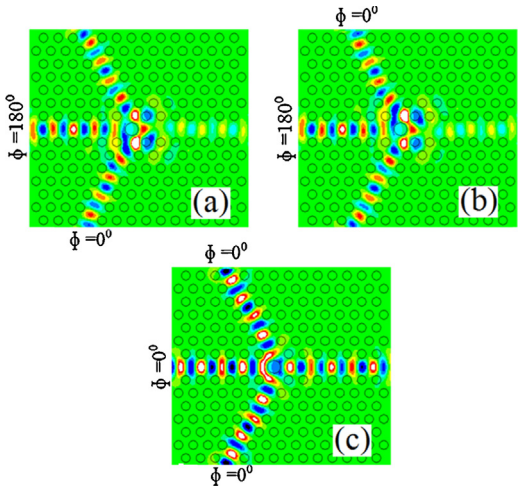

Fig. 7. Field distributions at steady state of the "AND" logic gate for (a) A = 1, B = 0, R = 1; (b) A = 0, B = 1, R = 1 and (c) A = 1, B = 1, R = 1.

interference which helps to satisfy the logic output of the OR gate. The field distribution at steady state as shown in Fig. 8 and Table 2 clearly shows that proposed structure can function as an OR logic gate.

4.3. For XOR gate

The output in XOR logic gate is logically "1" if only one of the two inputs is high (1) and logically "0" if both the inputs are high (1) or low (0). The working of XOR logic gate has been explained as follows: (i) when no signal has been launched at the input ports A and B along with the zero signal at the reference port R, output obtained at the port Y is logically "0". (ii) When any of the input ports A and B has been launched with a signal having phase angle $\Phi = 0^\circ$ along with the reference signal having same phase angle $\Phi = 0^\circ$ output obtained at the output port Y is logically "1". (iii) When both the input ports have been excited with the light signal having phase angle $\Phi = 0^\circ$ and reference port with the light having phase angle $\Phi = 180^\circ$ output obtained at the output port is logically "0". The simulation and logic output values shown in Fig. 9 and Table 3 show that the proposed structure could really work as XOR logic gate. The calculated value of contrast ratio for XOR logic gate has been found out to be 8.49 dB.

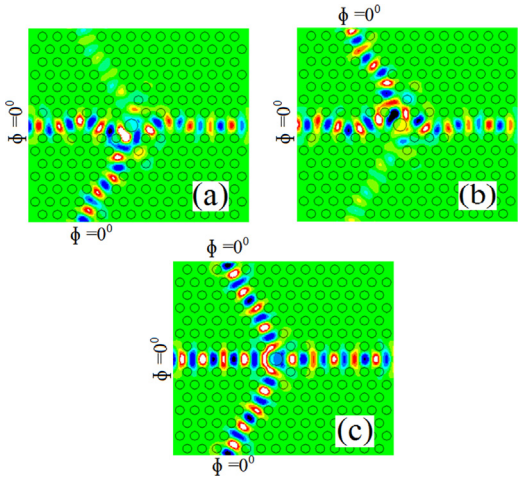

Fig. 8. Field distributions at steady state of the "OR" logic gate for (a) A = 1, B = 0, R = 1; (b) A = 0, B = 1, R = 1 and (c) A = 1, B = 1, R = 1.

Table 1
Truth table for AND logic gate where output Y is in terms of input power P_o.

AND gate				
Input A ($\Phi = 0^\circ$)	Input B ($\Phi = 0^\circ$)	Reference signal (R)	Logic output	Output Y
0	0	0	0	0
0	1	1 ($\Phi = 180^\circ$)	0	$0.17194P_o$
1	0	1 ($\Phi = 180^\circ$)	0	$0.17194P_o$
1	1	1 ($\Phi = 0^\circ$)	1	$0.46638P_o$

Table 2
Truth table for OR logic gate where output Y is in terms of input power P_o.

OR gate				
Input A ($\Phi = 0^\circ$)	Input B ($\Phi = 0^\circ$)	Reference signal (R)	Logic output	Output Y
0	0	0	0	0
0	1	1 ($\Phi = 0^\circ$)	1	$0.44975P_o$
1	0	1 ($\Phi = 0^\circ$)	1	$0.44975P_o$
1	1	1 ($\Phi = 0^\circ$)	1	$0.46638P_o$

Table 3
Truth table for XOR logic gate where output Y is in terms of input power P_o.

XOR gate				
Input A ($\Phi = 0^\circ$)	Input B ($\Phi = 0^\circ$)	Reference signal (R)	Logic output	Output Y
0	0	0	0	0
0	1	1 ($\Phi = 0^\circ$)	1	$0.44971P_o$
1	0	1 ($\Phi = 0^\circ$)	1	$0.44971P_o$
1	1	1 ($\Phi = 180^\circ$)	0	$0.09051P_o$

4.4. For NOT gate

The NOT gate design is like an inverter in which output is inverse of the input. In the proposed structure one input has been taken at the input port A and a reference signal. When input signal is launched at the input port A with phase angle $\Phi = 0^\circ$ and a reference signal with phase angle $\Phi = 180^\circ$ the output obtained at the output port Y is logically '0' and logically '1' when no input signal is launched at the input port but only reference signal is launched with phase angle $\Phi = 180^\circ$. The contrast ratio for NOT gate is 5.42 dB. The Table 4 and field distribution shown in Fig. 10 clearly indicates that the proposed structure can be used as a NOT gate.

4.5. For NAND gate

NAND gate is the inverse of the AND gate where logic output values are inverse of the AND logic output values. In NAND logic gate output is logically '1' if light is launched at any one of the two inputs or zero input launch from both the inputs and it is logically '0' when both the input values are launched along with the reference signal. The working of NAND gate has been explained as follows: (i) when reference signal is launched at the reference port R with phase angle $\Phi = 0^\circ$ and none of the signal is launched at the input ports, or signal with phase $\Phi = 0^\circ$ is launched at either of the input ports A and B, then logic '1' is obtained at the output port Y. (ii) When light with phase $\Phi = 0^\circ$ is launched at both the input ports A and B and reference port R is launched with the signal having phase angle $\Phi = 180^\circ$ then logic '0' is obtained at the output port Y. The results have been summarized in Table 5 where output values are expressed in terms of input power P_o. The contrast ratio for NAND gate is found out to be 9.59 dB. The simulation results shown in Fig. 11 clearly indicate that the structure could really behave as NAND logic gate.

4.6. For NOR gate

NOR logic gate is logically inverse of the OR logic gate where output is '1' when both the inputs are '0'. The operation of NOR logic gate has been demonstrated as follows: (i) when no signal is launched at the input ports A and B and only reference port has been excited with the input signal having phase angle $\Phi = 180^\circ$,

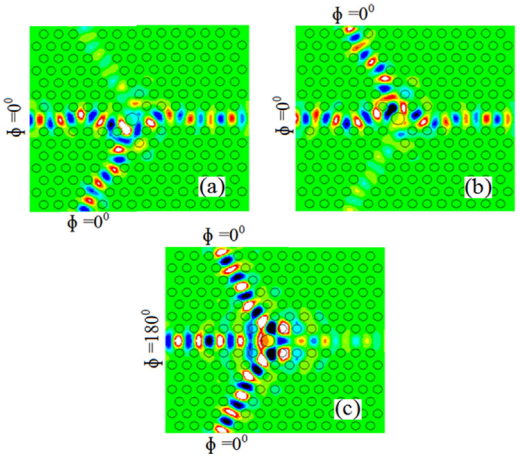

Fig. 9. Field distributions at steady state of the "XOR" logic gate for (a) A = 1, B = 0, R = 1; (b) A = 0, B = 1, R = 1 and (c) A = 1, B = 1, R = 1.

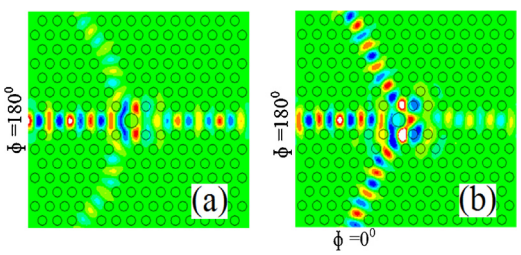

Fig. 10. Field distributions at steady state of the "NOT" logic gate for (a) A = 1, R = 1 and (b) A = 0, R = 1.

Table 4
Truth table for NOT logic gate where output Y is in terms of input power P_o.

NOT gate			
Input A ($\Phi = 0^\circ$)	Reference signal (R)	Logic output	Output Y
0	1 ($\Phi = 180^\circ$)	1	$0.5429P_o$
1	1 ($\Phi = 180^\circ$)	0	$0.1719P_o$

Table 5
Truth table for NAND logic gate where output Y is in terms of input power P_o.

NAND gate				
Input A ($\Phi = 0^\circ$)	Input B ($\Phi = 0^\circ$)	Reference signal (R)	Logic output	Output Y
0	0	1 ($\Phi = 0^\circ$)	1	$0.5429P_o$
0	1	1 ($\Phi = 0^\circ$)	1	$0.4497P_o$
1	0	1 ($\Phi = 0^\circ$)	1	$0.4497P_o$
1	1	1 ($\Phi = 180^\circ$)	0	$0.0905P_o$

Table 6
Truth table for NOR logic gate where output Y is in terms of input power P_o.

NOR gate				
Input A ($\Phi = 0^\circ$)	Input B ($\Phi = 0^\circ$)	Reference signal (R)	Logic output	Output Y
0	0	1 ($\Phi = 180^\circ$)	1	$0.5429P_o$
0	1	1 ($\Phi = 180^\circ$)	0	$0.1719P_o$
1	0	1 ($\Phi = 180^\circ$)	0	$0.1719P_o$
1	1	1 ($\Phi = 180^\circ$)	0	$0.0905P_o$

logic output "1" is obtained at the output port Y. (ii) When either of the two input ports or both the input ports have been excited with light having phase angle $\Phi = 0^\circ$ along with the reference input signal having phase angle $\Phi = 180^\circ$ output obtained at the output port Y is logically "0". The contrast ratio for NOR logic gate is found to be 5.42 dB. The results for the NOR gate have been shown in the Table 6 and Fig. 12. From the Table 6 and field distribution shown in Fig. 12 indicates that the proposed structure could really work as NOR logic gate.

4.7. For XNOR gate

XNOR logic gate is logically inverse of the XOR logic gate, where output is "1" if both the input values are same and "0" if both input values are different. The function of XNOR logic gate is as follows: (i) when both the input ports are either excited with the signal having phase angle $\Phi = 0^\circ$ or not excited with any signal but reference signal has been launched at the reference port R with light having phase angle $\Phi = 0^\circ$, then output obtained at the output port Y is logically "1". (ii) When either of the input ports has been launched with the input signal having phase angle $\Phi = 0^\circ$ along with the reference signal having phase angle $\Phi = 180^\circ$, then output obtained at the output port is logically "0". The contrast ratio for XNOR logic gate is obtained to be 5.42 dB. The field distribution at steady state as shown in Fig. 13 and output values shown in Table 7 clearly indicates that the proposed structure can be used to operate as a XNOR logic gate.

5. Response time

From Fig. 14, which represents the response time for the proposed structure, it has been concluded that the time taken to climb output power from 0 to 90% of the average output power P_{av} in the final steady state is $ct_1 = 35.9\,\mu m$ or $t_1 = 0.419$ ps and it consists of two parts one of which is the time due to transmission delay i.e. $t_{11} = 0.163$ ps and another $t_{12} = 0.256$ ps is the time for the

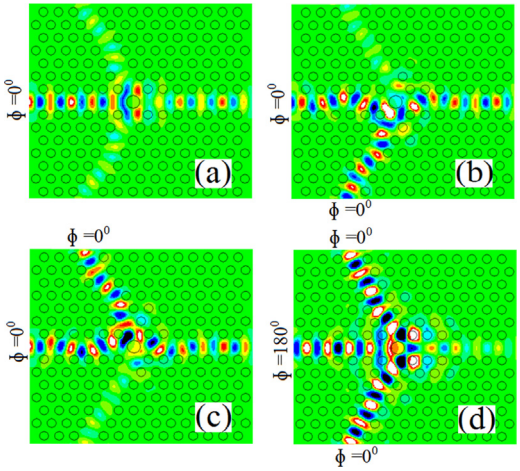

Fig. 11. Field distributions at steady state of the "NAND" logic gate for (a) A = 0, B = 0, R = 1; (b) A = 1, B = 0, R = 1; (c) A = 0, B = 1, R = 1 and (d) A = 1, B = 1, R = 1.

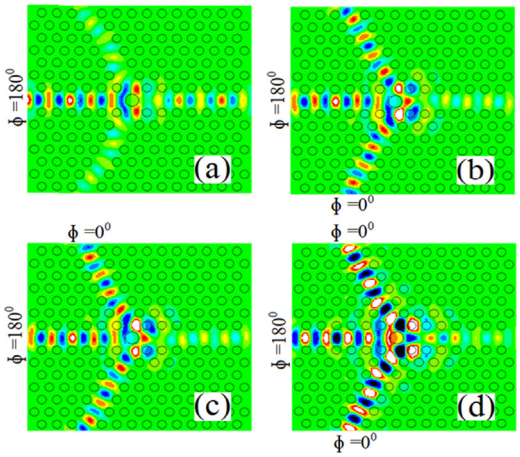

Fig. 12. Field distributions at steady state of the "NOR" logic gate for (a) A = 0, B = 0, R = 1; (b) A = 1, B = 0, R = 1; (c) A = 0, B = 1, R = 1 and (d) A = 1, B = 1, R = 1.

Table 7
Truth table for XNOR logic gate where output Y is in terms of input power P_o.

XNOR gate				
Input A ($\Phi = 0^\circ$)	Input B ($\Phi = 0^\circ$)	Reference signal (R)	Logic output	Output Y
0	0	1 ($\Phi = 0^\circ$)	1	$0.5429P_o$
0	1	1 ($\Phi = 180^\circ$)	0	$0.1719P_o$
1	0	1 ($\Phi = 180^\circ$)	0	$0.1719P_o$
1	1	1 ($\Phi = 0^\circ$)	1	$0.4663P_o$

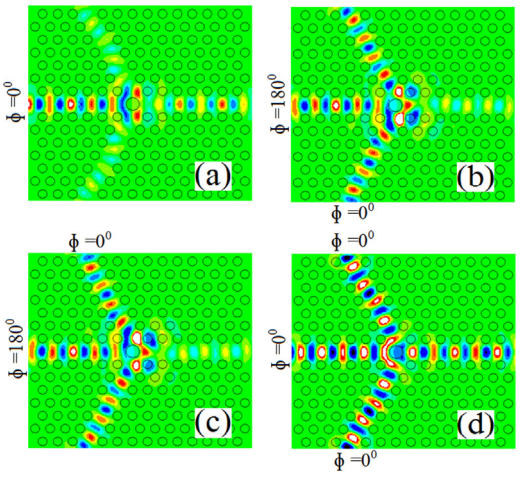

Fig. 13. Field distributions at steady state of the "XNOR" logic gate for (a) A = 0, B = 0, R = 1; (b) A = 1, B = 0, R = 1; (c) A = 0, B = 1, R = 1 and (d) A = 1, B = 1, R = 1.

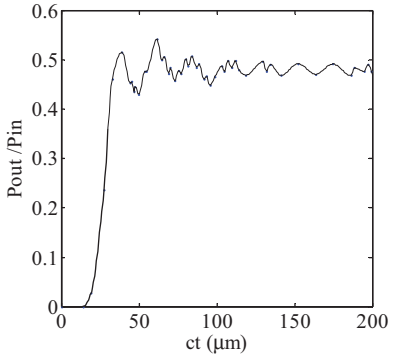

Fig. 14. Time evolution curve of the output power.

output power to climb from 0.1%P_{av} to 90%P_{av}. Since the system operates on linear materials it has been expected that the falling time from average output power P_{av} to 10% P_{av} is approximately equal to t_{12}. Hence, a narrow pulse of width of $2t_{12} = 0.512$ ps can be produced. Hence it has been predicted that the proposed structure has a response period of 1.024 ps and can operate at a bit rate of 0.976 Tbit/s.

6. Conclusion

In this paper, we have proposed the design for all optical logic gates based on optical interference effect in two-dimensional PhC waveguides. The performance of the proposed PhC structure has been analyzed by PWE method and transmission and optimization characteristics have been simulated using FDTD method. The method of determining the operating parameters has been explained and the optimized parameters have been obtained for achieving the contrast ratio for all optical logic gates. The design of the all optical logic gates can operate at very low powers and it is expected that the proposed structure can be effectively used for the design of all optical integrated circuits.

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Design and analysis of polarization independent all-optical logic gates in silicon-on-insulator photonic crystal

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ABSTRACT

In this paper, we have reported design and analysis of polarization independent all optical logic gates in silicon-on-insulator photonic crystal consisting of two dimensional honeycomb lattices with two different air holes exhibiting photonic band gap for both TE and TM mode in the optical communication window. The proposed structures perform as an AND optical logic gate and all the optical logic gates based on the phenomenon of interference. The response period and bit rate for TE and TM polarizations at a wavelength of 1.55 μm show improved results as reported earlier.

1. Introduction

In recent years various schemes have been employed for the designing of optical logic gates using optical fibers [1–5] and waveguides [6–8], but they have certain limitations like low speed, big size and difficult to perform on chip integration. Recently, two dimensional (2D) photonic crystal (PhC) slab structures have attracted wide attention due to their ease of fabrication as compared to three dimensional structures. The 2D PhC structures provide versatile platform for on-chip device design and present an alternative to the existing electronic circuitry. In general, these 2D PhC structures are operational for only one specific polarization that limits the light coupling to localized optical modes and extraction of light from the slab. However, polarization independent wave guiding in 2D PhC structures with complete photonic band gap (i.e. photonic band gap for both transverse electric (TE) and transverse magnetic (TM) mode) may overcome this limitation [9–12]. Optical switches and logic gates have emerged as an important part of optoelectronic and integrated devices and have several applications.

To our knowledge, only single polarization based logic gates have been reported so far [13–17]. Optical logic gates on SOI platform lead to certain applications like the ultrafast operation of the devices as compared to the traditional electronic devices, data-integrity verification, packet header modification etc. The reported optical logic gates are 2D structures operational for single polarization [18–22]. In this paper, we propose the design of polarization independent AND optical logic gate and all optical logic gates in silicon-on-insulator (SOI) platform based on the light beam interference effect. The structure for AND gate consists of symmetric Y branch waveguide so that light beams interfere constructively whereas for all optical logic gates one additional reference waveguide has been created. The light beams interfere either constructively or destructively for both the polarizations based on the phase angle of the light beam launched at reference waveguide. Phase angle of the input light beam can be varied as demonstrated by Birr et al. [23]. The proposed design consists of honey comb lattice arrangement with two different air holes in SOI substrate. The honey comb arrangement on SOI platform has been chosen because this arrangement supports both the polarizations. The honey comb structure of such type can be easily implemented on SOI substrate using recently available technology. The structure has been optimized for both the polarizations (TE and TM mode) at 1.55 μm wavelength. The contrast ratio and bit rate have been calculated for TE and TM modes separately and it has been found that the proposed designs behave as AND optical logic gate and all optical logic gates. The contrast ratio defined as $10\log(P_1/P_0)$ (dB) has been calculated for both TE and TM polarizations separately, where P_1 represents power for logic-1 and P_0 represents the power for logic-0 obtained at the output port. The response time [24,25] for both the polarizations has been

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evaluated using the finite difference time domain (FDTD) method. The calculated results i.e. response period and bit rate are improved than that reported in the previous papers [18,19,25].

2. Device design, optimization and simulation results

In this paper, the design for AND optical logic gate and all optical logic gates constructed on SOI substrate has been presented. The proposed design consists of honey comb lattice of air holes of two different radii in silicon slab as shown in Fig. 1(a). The radii of two different air holes have been chosen, so as to achieve complete photonic band gap. The radii of two air holes has been taken as $r_b=0.36a$ (radius of bigger air hole) and $r_s=0.16a$ (radius of smaller air hole), where '$a=570$ nm' is the lattice constant. The smaller air holes have been placed exactly at the center of the bigger air holes. An asymmetrical silicon ($n_{Si}=3.5$) slab of thickness 250 nm has been taken which has air as upper cladding and silica ($n_{Sio_2}=1.45$) as lower cladding layer. The 3D calculations consume more time and memory, so, we have employed 2D analysis with effective index method. The effective index of the slab for TE and TM modes has been calculated to be n_{eff} (TE)=2.89 and n_{eff} (TM)=2.15 at 1.55 μm wavelength, respectively using Finite Element Method (FEM) [12]. Using plane wave expansion (PWE) method, it has been observed that there exists a complete photonic band gap in the normalized frequency range of 0.3520–0.3836 (a/λ), as shown in Fig. 1(b).

2.1. For AND optical logic gate

2.1.1. Design

For AND optical logic gate three waveguides have been created in the proposed structure to act as input and output waveguides. The design consists of a Y branch photonic crystal waveguide having three arms out of which two behave as input ports (Input A and Input B) and the third one acts as an output port as shown in Fig. 2. The region on both sides of the waveguides has mirror image symmetry so that the maximum light remains confined within the waveguide region. Further, the output waveguide has been modified by addition of the extra air holes of smaller radii at the two boundaries of the output waveguide. A hole has been introduced at the center of the three waveguides, which has been optimized for both the TE and TM modes. Due to the symmetric waveguide structure the light interferes constructively at the intersection of the three waveguides, when both the signals are launched simultaneously in both the input waveguides. As a result, the maximum value of power is obtained. However, there is branching of signals through the other path when either one of the two signals is present. As a result, low value of power is obtained in the output waveguide. Thus, leading the proposed design to operate as an AND optical logic gate.

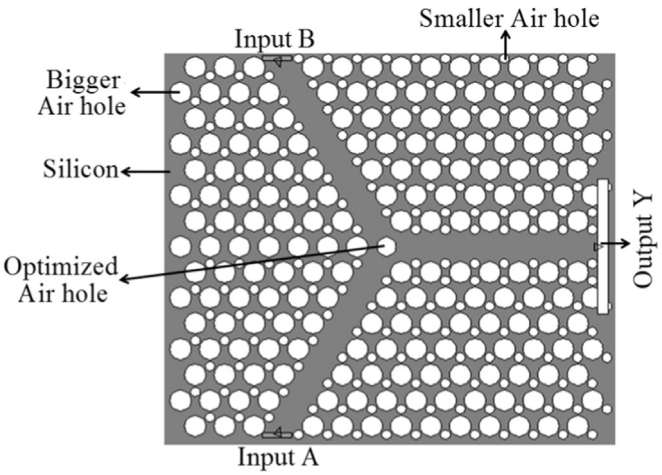

Fig. 2. Schematic representation of AND optical logic gate.

2.1.2. Optimization of the radius of the central hole for AND optical logic gate

The radius of the central hole has been optimized at the center of the Y branch to enhance the performance of the proposed logic gate for both the TE and TM modes separately. Fig. 3 shows the variation of ratio of output power to the input power (P_{out}/P_{in}) versus radius of the central hole for both the polarizations at single input and both input signals. For TE mode, it has been observed that as the radius of the central hole increases the ratio of output power to input power increases and then decreases whereas the variation remains same for TM mode. A common region has been chosen for optimization of the radius of central hole where output for single input as well as for both input signals is maximum for TE and TM polarizations. Hence, the optimized radius of the central hole has been taken as $0.30a$.

2.1.3. Simulation results and discussion for and gate

The optimized structure has been analyzed to perform as AND optical logic gate for both TE and TM modes using FDTD method.

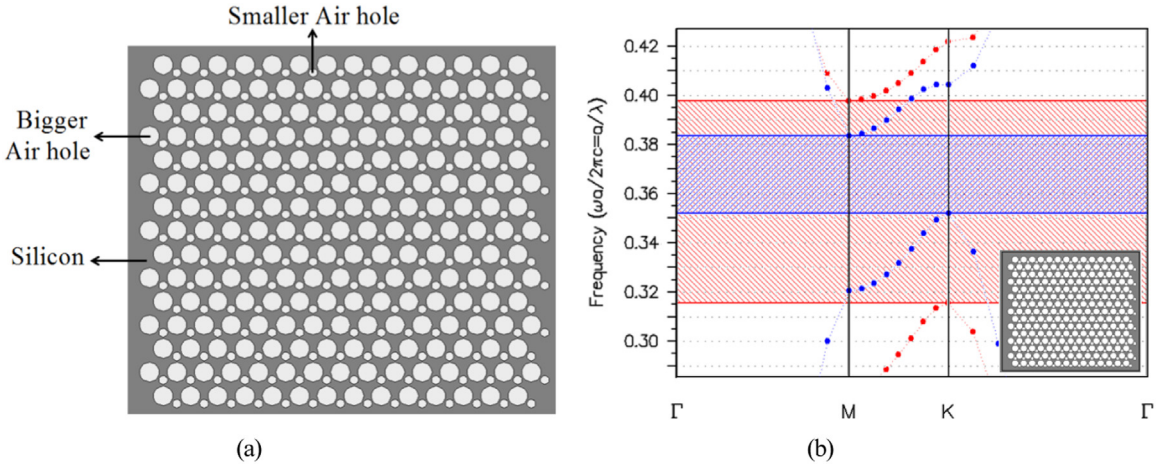

Fig. 1. (a) Schematic representation of honey comb photonic crystal (b) complete band gap for honey comb lattice arrangement where red curves correspond to the TE modes and blue curves correspond to the TM modes. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article).

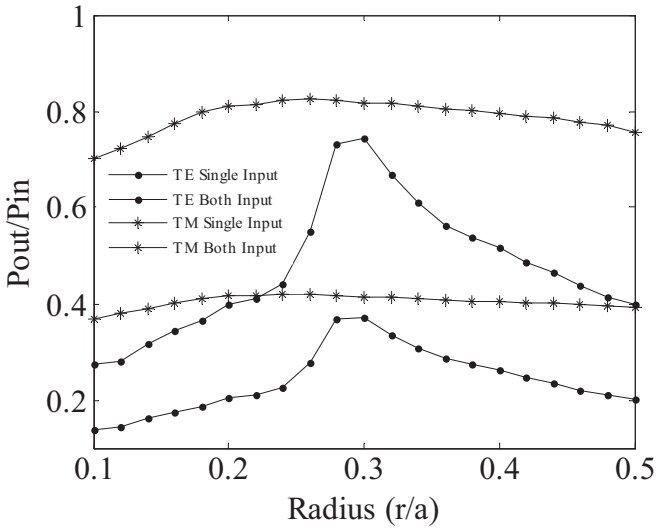

Fig. 3. Power transmittance with radius of central hole both for TE and TM mode with respect to the single input and both inputs.

Table 1
Truth table for AND optical logic gate for TE and TM polarizations at 1.55 μm wavelength where output power Y is in terms of input power P_a.

AND gate				
Input A	Input B	Logic output	Output Y (TE)	Output Y (TM)
0	0	0	0	0
0	1	0	0.372 P_a	0.414 P_a
1	0	0	0.372 P_a	0.414 P_a
1	1	1	1.485 P_a	1.630 P_a

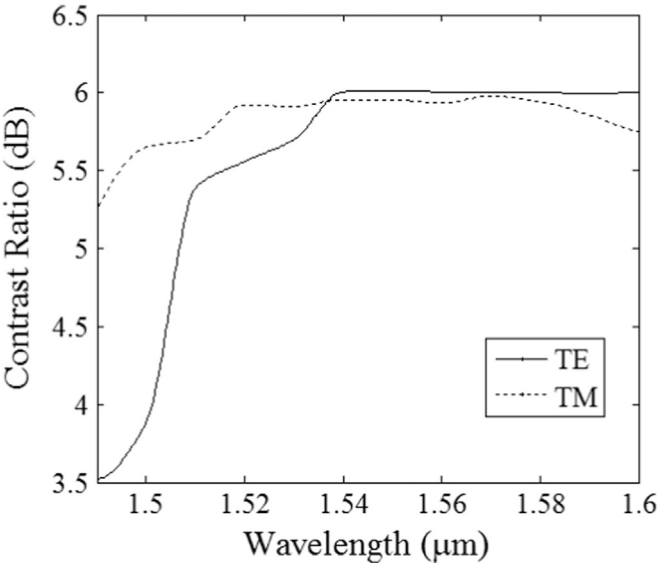

Fig. 4. Contrast ratio for both TE and TM polarizations in the complete band gap range.

Both the TE polarized and TM polarized light has been launched at input ports A and B. When input power P_a is launched at input port A or at port B separately, then the power at output port remains low. When power is launched at both the ports A and B simultaneously, then maximum power is obtained at the output port for both TE and TM polarizations as mentioned in Table 1. The results calculated in Table 1 indicate that the design can work as AND optical logic gate for both TE and TM polarizations based on

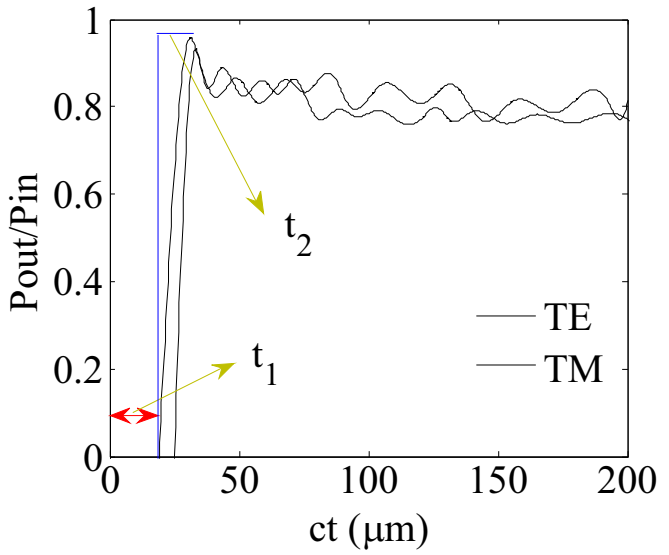

Fig. 5. Response time in terms of time evolution of the output power for both TE and TM polarizations.

the phenomenon of interference. The contrast ratio for both TE and TM polarizations has been calculated as the ratio of the power for logic-1 to the power for logic-0 i.e. Contrast Ratio = 10 $\log(P_1/P_0)$ (dB), where P_1 represents power for logic-1 and P_0 represents power for logic-0 and has been found out to be 6 dB at 1.55 μm wavelength as shown in Fig. 4. Fig. 4 shows the variation of the contrast ratio for both the TE and TM polarizations in the entire range of complete band gap. The response time which is defined as the switching time of the device between the OFF and ON state for both TE and TM polarizations has been determined using time evolving curve of the output power as shown in Fig. 5. For TE polarized mode, at steady-state, the time taken to reach output power from 0% to 90% of the average output power (P_{av}) is ct=32.8 μm or t=0.316 ps, where 'c' is the speed of light in medium. This time consists of two parts one of which is time due to transmission delay i.e. t_1=0.241 ps and another is time taken by output power to climb from 0.1% to 90% of P_{av} i.e. t_2=0.075 ps. It has been expected that the falling time from P_{av} to 10% of P_{av} is approximately equal to t_2. Thus, a narrow pulse width of $2t_2$ =0.150 ps can be produced and hence the response time of 0.300 ps has been achieved if the ON and OFF time of the signal is same. Further, bit rate which is defined as the inverse of the response time has been calculated to be 3.33 Tbit/s for TE polarized mode. Similarly, response period and bit rate has been calculated for TM polarized mode using Fig. 5. For TM polarized mode, ct=30.3 μm or t=0.27 ps, t_1=0.136 ps, t_2=0.081 ps, $2t_2$=0.162 ps and the response period of 0.324 ps and a bit rate of 3.09 Tbit/s have been obtained. Hence, we have achieved the improved values of bit rate and response period as reported earlier [18,19,25]. The field distribution profiles at steady state for both TE and TM polarized modes as shown in Fig. 6 and the results mentioned in Table 1 for both TE and TM polarizations at a wavelength of 1.55 μm, indicate that the design behaves as AND optical logic gate.

2.2. For all optical logic gates

2.2.1. Device design

In the proposed design for all optical logic gates, four waveguides have been created out of which two behave as input ports (Input A and Input B) and the third one acts as a reference port (R) and fourth as an output port Y as shown in Fig. 7. The reference port with reference/control signal has been used to create phase

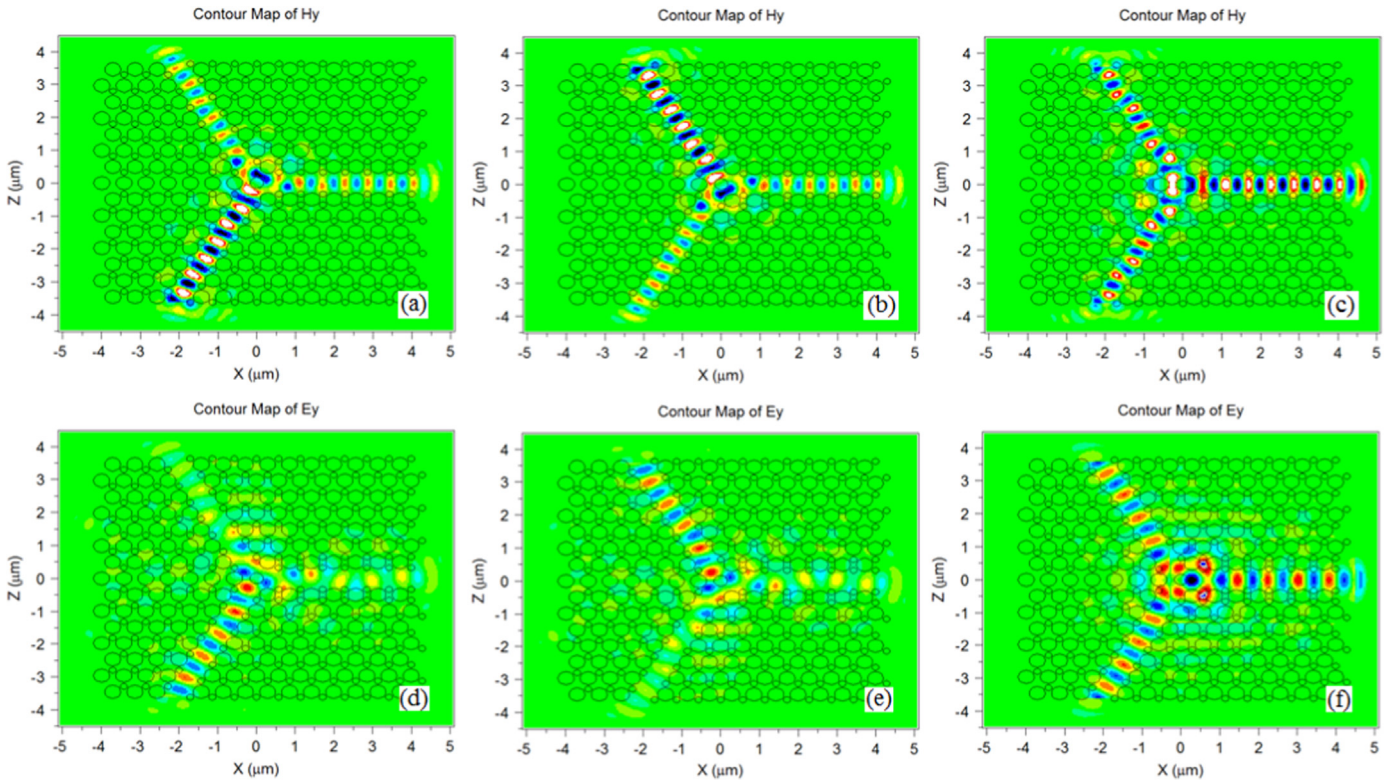

Fig. 6. Field distributions at steady state of the "AND" logic gate at 1.55 μm wavelength for TE polarization at (a) A=1, B=0 (b) A=0, B=1 (c) A=1, B=1 and for TM polarization at (d) A=1, B=0 (e) A=0, B=1 (f) A=1, B=1.

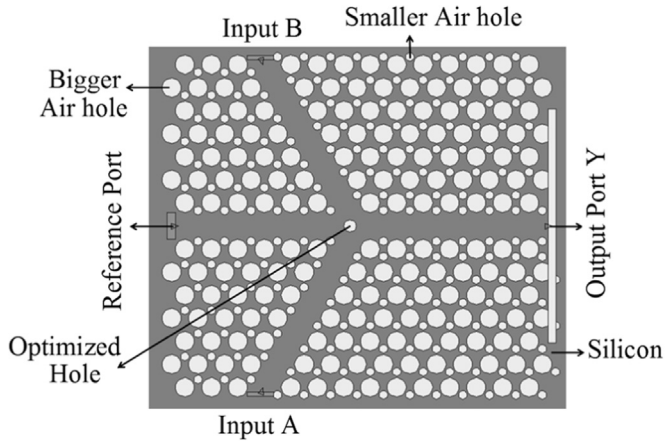

Fig. 7. Schematic representation of all optical logic gates.

difference between the input signals which results into constructive as well as destructive interference depending on the phase angle of the reference/control signal. In this structure also mirror image symmetry has been considered so that the maximum light remains confined within the waveguide region. A hole has been introduced at the center of the four waveguides, which has been optimized for both the TE and TM polarized modes. The light interferes constructively at the intersection of the four waveguides as the addition of signals that are in-phase, when either of the input signals or both the input signals are launched simultaneously in both the input waveguides. As a result, maximum value of power is obtained. However, there is a destructive interference when signals are out of phase resulting into low value of power in the output waveguide. Thus, the proposed design can be used for the realization of all optical logic gates.

2.2.2. Optimization of the radius of the central hole for all optical logic gates

The radius of the central hole has been optimized at the center of the four waveguides to enhance the performance of the proposed design for both the TE and TM polarized modes separately. Fig. 8 shows the variation of ratio of output power to the input power (P_{out}/P_{in}) versus radius of the central hole for both the polarizations at single input (along with the reference signal) and both input signals (along with the reference signal). For TE polarized mode, it has been observed that as the radius of the central

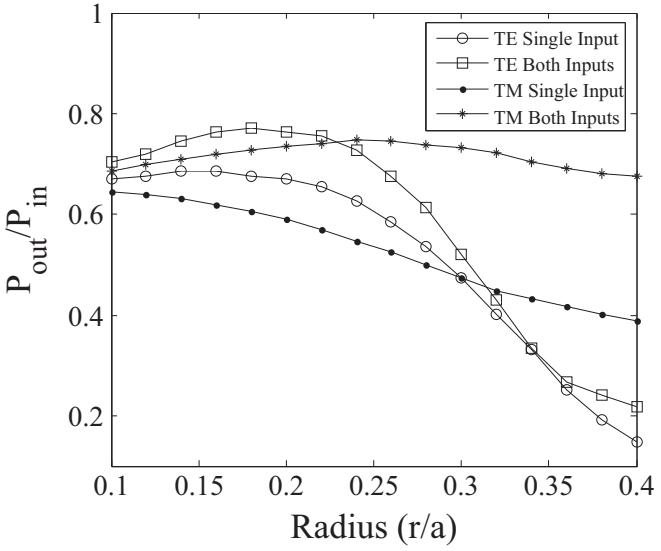

Fig. 8. Power transmittance with radius of central hole for all optical logic gates for both TE and TM polarized modes with respect to the single input and both inputs along with the reference/control signal.

hole increases the ratio of output power to input power increases and then decreases. For TM mode it increases first and then decreases for both inputs whereas it keeps on decreasing for single input. A common region has been chosen for the optimization of the radius of central hole where output for both input signals (along with the reference signal) crosses each other for TE and TM polarizations. Hence, the optimized radius of the central hole has been taken as 0.23*a*.

2.2.3. Results and discussion

The optimized structure has been analyzed to perform as AND, OR, NOT, NAND, NOR, XOR, XNOR all-optical logic gates for both TE and TM polarized modes using FDTD method. Both the TE polarized and TM polarized light has been launched at the input ports A and B and at reference port. The logic operations has been performed as follows: (i) when either of the input ports A and B or both the input ports A and B has been excited with light signal having phase angle $\varphi = 0^{\circ}$ and the reference port with reference/control signal having phase angle $\varphi = 0^{\circ}$ then logic 1 is obtained at the output port Y. (ii) when either input ports A and B or both the input ports A and B are excited with light signals having phase angle $\varphi = 0^{\circ}$ and reference port with control signal having phase angle $\varphi = \pi$ then logic 0 is obtained at the output port Y. (iii) When only the control signal at reference port with $\varphi = 0^{\circ}$ or $\varphi = \pi$ has been excited then maximum power is obtained at the output port as shown in Figs. 9 and 10. Fig. 9 represents the field distribution pattern for TE polarized mode and Fig. 10 corresponds to the TM polarized mode. The logic behaviors have been analyzed at a wavelength of 1.55 μm for both the TE and TM polarizations.

2.2.3.1. AND gate. The AND optical logic gate operations is as follows (i) when A=1, B=0 at $\varphi = 0^{\circ}$and R=1 at $\varphi = \pi$ then output Y=0 due to destructive interference. (ii) When A=0, B=1 at $\varphi = 0^{\circ}$ and R=1 at $\varphi = \pi$ the also output Y=0. (iii) When A=1, B=1 at $\varphi = 0^{\circ}$ and R=1 at $\varphi = 0^{\circ}$ then output Y=1 due to constructive interference. The results have been compared and summarized in Table 2 for all possible combinations for both TE and TM polarizations. Fig. 9(c)–(e) shows the field distribution for TE polarization. The field distribution for TM polarization has been shown in Fig. 10(c)–(e). The calculated value of contrast ratio is found out to be 10 dB.

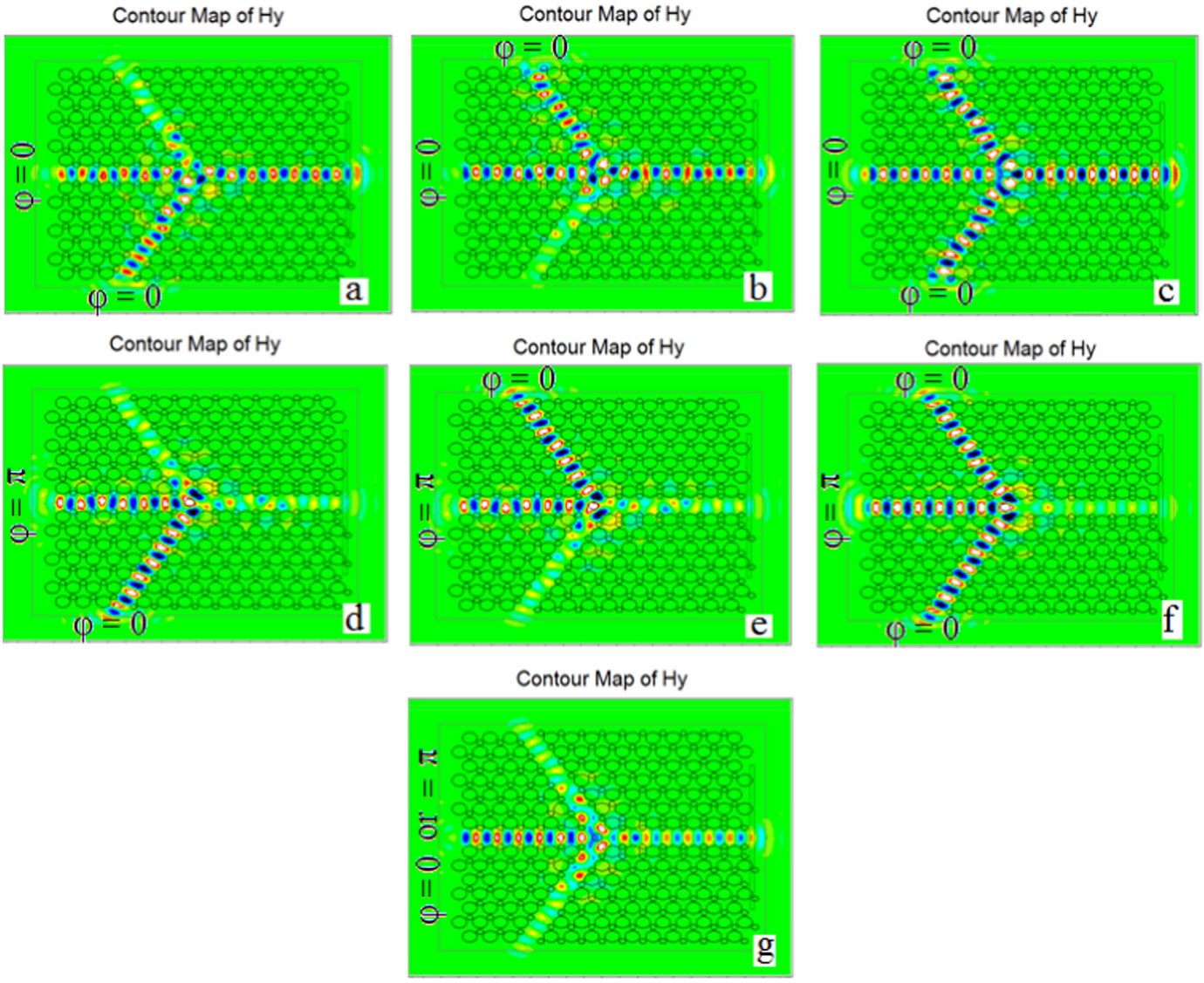

Fig. 9. Field distributions at steady state for all optical logic gates at 1.55 μm wavelength for TE like polarization at (a) A=1, B=0 at $\varphi = 0^{\circ}$, R=1 at $\varphi = 0^{\circ}$ (b) A=0, B=1 at $\varphi = 0^{\circ}$, R=1 at $\varphi = 0^{\circ}$ (c) A=1, B=1 at $\varphi = 0^{\circ}$, R=1 at $\varphi = 0^{\circ}$(d) A=1, B=0 at $\varphi = 0^{\circ}$, R=1 at $\varphi = \pi$ (e) A=0, B=1 at $\varphi = 0^{\circ}$, R=1 at $\varphi = \pi$ (f) A=1, B=1 at $\varphi = 0^{\circ}$, R=1 at $\varphi = \pi$ (g) A=0, B=0, R=1 at $\varphi = 0^{\circ}$ or π.

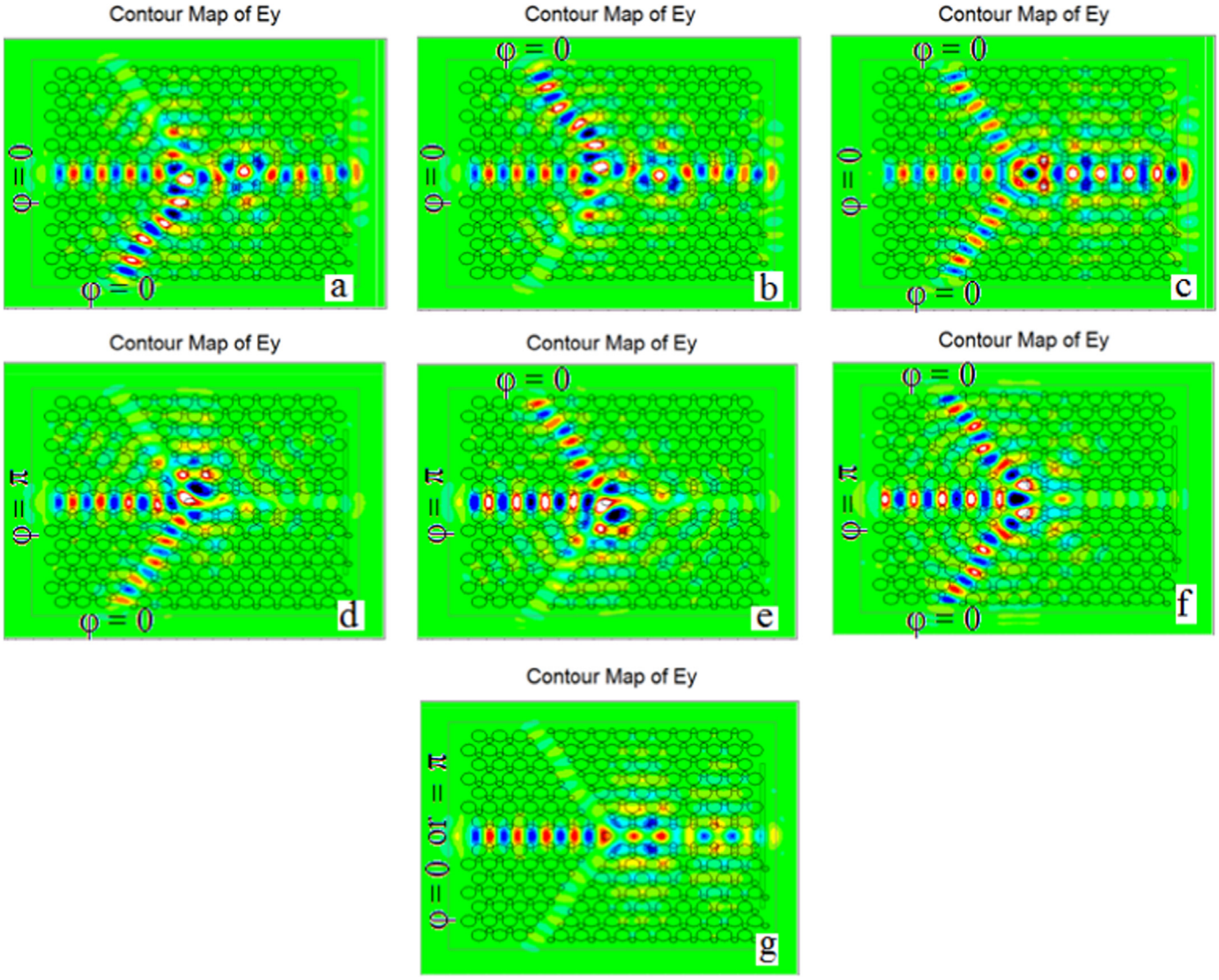

Fig. 10. Field distributions at steady state for all optical logic gates at 1.55 μm wavelength for TM like polarization at (a) A=1, B=0 at $\varphi = 0^{\circ}$, R=1 at $\varphi = 0^{\circ}$ (b) A=0, B=1 at $\varphi = 0^{\circ}$, R=1 at $\varphi = 0^{\circ}$ (c) A=1, B=1 at $\varphi = 0^{\circ}$, R=1 at $\varphi = 0^{\circ}$ (d) A=1, B=0 at $\varphi = 0^{\circ}$, R=1 at $\varphi = \pi$ (e) A=0, B=1 at $\varphi = 0^{\circ}$, R=1 at $\varphi = \pi$ (f) A=1, B=1 at $\varphi = 0^{\circ}$, R=1 at $\varphi = \pi$ (g) A=0, B=0, R=1 at $\varphi = 0^{\circ}$ or π.

Table 2
Truth table for AND optical logic gate for TE and TM polarizations at 1.55 μm wavelength where normalized output power Y is in terms of input power P_a.

AND gate					
Input A ($\varphi = 0^{\circ}$)	Input B ($\varphi = 0^{\circ}$)	Reference signal (R)	Logic output	Normalized output Y (TE)	Normalized output Y (TM)
0	0	0	0	0	0
0	1	1 ($\varphi = \pi$)	0	0.1716 P_a	0.0902 P_a
1	0	1 ($\varphi = \pi$)	0	0.1722 P_a	0.0920 P_a
1	1	1 ($\varphi = 0^{\circ}$)	1	0.7448 P_a	0.7453 P_a

Table 3
Truth table for OR optical logic gate for TE and TM polarizations at 1.55 μm wavelength where normalized output power Y is in terms of input power P_a.

OR gate					
Input A ($\varphi = 0^{\circ}$)	Input B ($\varphi = 0^{\circ}$)	Reference signal (R)	Logic output	Normalized output Y (TE)	Normalized output Y (TM)
0	0	0	0	0	0
0	1	1 ($\varphi = 0^{\circ}$)	1	0.6407 P_a	0.5629 P_a
1	0	1 ($\varphi = 0^{\circ}$)	1	0.6391 P_a	0.5572 P_a
1	1	1 ($\varphi = 0^{\circ}$)	1	0.7448 P_a	0.7453 P_a

2.2.3.2. OR gate. The optimized structure can be operated as OR gate for both TE and TM polarizations and explained as follows: (i) when A=1, B=0, or A=0, B=1, at $\varphi = 0^{\circ}$ and R=1 also at $\varphi = 0^{\circ}$ then Y=1 i.e. logic 1 is obtained at the output port Y due to the constructive interference. (ii) When A=1, B=1, at $\varphi = 0^{\circ}$ and reference port with reference/control signal R=1 is also having phase angle $\varphi = 0^{\circ}$ then logic 1 is obtained at the output port Y due to the phase matching condition. For the OR gate realization, the phase angle between the input signals and control signal has been taken as same which results into the constructive interference and satisfying the logic output of the OR gate. The field distribution at steady state for TE polarization has been shown in Fig. 9(a)–(c) and for TM polarization in Fig. 10(a)–(c). The results mentioned in Table 3 clearly shows that the proposed structure can function as OR optical logic gate.

Table 4
Truth table for NOT optical logic gate for TE and TM polarizations at 1.55 μm wavelength where normalized output power Y is in terms of input power P_a.

NOT gate				
Input A ($\varphi = 0^\circ$)	Reference signal (R)	Logic output	Normalized output Y (TE)	Normalized output Y (TM)
0	1 ($\varphi = \pi$)	1	0.6562 P_a	0.4244 P_a
1	1 ($\varphi = \pi$)	0	0.1722 P_a	0.0920 P_a

2.2.3.3. NOT gate. In the proposed structure, for NOT gate one input has been taken at the input port A and other at the reference port as control signal. The switching from off to on state has been maintained by phase difference of π between the input signal and control signal. The output remains high when only control signal is present with phase angle of $\varphi = \pi$ i.e. A=0, R=1and is low when input signal and the control signal are out of phase i.e. A=1 at $\varphi = 0^\circ$, R=1 at $\varphi = \pi$ as indicated in Table 4 for both TE and TM polarizations at a wavelength of 1.55 μm. The contrast ratio for NOT gate is 6 dB. The Table 4 and field distributions shown in Fig. 9 (d) and (g), 10(d) and (g) clearly indicate that the proposed structure can be used as a NOT gate.

2.2.3.4. NAND gate. The universal NAND gate is the inverse of the AND gate. The NAND gate optical logic behavior for both the TE and TM polarizations has been explained as follows: (i) When control signal is launched at the reference port with phase angle $\varphi = 0^\circ$ i.e. R=1 and none of the signals is launched at the input ports, i.e. A=0, B=0 then the output obtained at the output port Y is logically '1'. (ii) When either of the input ports have been excited with the input signals i.e. A=1, B=0 or A=0, B=1 with $\varphi = 0^\circ$ and control signal R=1 with $\varphi = 0^\circ$ then also the output obtained is logically '1'. (iii) When A=1, B=1 with phase $\varphi = 0^\circ$ and reference port with control signal R=1 with $\varphi = \pi$ then logic '0' is obtained at the output port Y. The results have been summarized in Table 5 and the simulations shown in Fig. 9(a), (b), (f) and (g) for TE polarization and Fig. 10(a), (b), (f) and (g) for TM polarization clearly indicate that the structure could really behave as NAND optical logic gate. The contrast ratio for NAND gate is found out to be 7 dB.

2.2.3.5. NOR gate. The inverse of OR gate leads to the universal NOR logic gate which can further be used to design other devices. The NOR logic operation is as follows (i) when only the control signal is applied at the reference port with phase angle $\varphi = \pi$ then only the output is logically in the ON state. (ii) When the input signal is applied at either of the input ports or at both the input port with phase angle $\varphi = 0^\circ$ but control signal is applied at the reference port with phase angle $\varphi = \pi$ then the output at the output port is always zero i.e. in OFF state. The logic output for both TE and TM polarizations have been compared in Table 6 and

Table 6
Truth table for NOR optical logic gate for TE and TM polarizations at 1.55 μm wavelength where normalized output power Y is in terms of input power P_a.

NOR gate					
Input A ($\varphi = 0^\circ$)	Input B ($\varphi = 0^\circ$)	Reference signal (R)	Logic output	Normalized output Y (TE)	Normalized output Y (TM)
0	0	1($\varphi = \pi$)	1	0.6562 P_a	0.4244 P_a
0	1	1($\varphi = \pi$)	0	0.1716 P_a	0.0902 P_a
1	0	1($\varphi = \pi$)	0	0.1722 P_a	0.0920 P_a
1	1	1($\varphi = \pi$)	0	0.1236 P_a	0.1215 P_a

can be easily verified from the simulation figures shown in Figs. 9 and 10.

2.2.3.6. XOR gate. The output in XOR logic gate is logically "1" if only one of the two inputs is high (1) and logically "0" if both the inputs are high (1) or low (0). The working of XOR logic gate has been explained as follows: (i) when one of the input signals is applied along with the control signal i.e. A=1, B=0, R=1 or A=0, B=1, R=1 with phase angle $\varphi = 0^\circ$ then the output is logically high. (ii) The output is logically low when none of the input ports and reference port have been excited or both the input ports have been excited with the light signal having phase angle $\varphi = 0^\circ$ and reference port with the reference light signal having phase angle $\varphi = \pi$ i.e. A=0, B=0, R=0 or A=1, B=1, R=1. The simulation Fig. 9 (a), (b) and (f) for TE polarization and Fig. 10(a), (b) and (f) for TM polarization show that the proposed structure could really work as XOR logic gate. The truth table for TE and TM polarizations has been compared in Table 7. The calculated value of contrast ratio for XOR logic gate has been found out to be 5 dB.

2.2.3.7. XNOR gate. The XNOR optical logic gate is inverse of the XOR optical logic gate and can be easily verified as mentioned in Table 8 for both the polarizations. The field distribution shown in Fig. 9(c)–(e) and (g) for TE polarization and Fig. 10(c)–(e) and (g) for TM polarization proves that the proposed design can be efficiently used as XNOR optical logic gate.

The response time of the all optical logic gate device for both TE and TM polarized modes has also been determined in a similar manner as done for AND optical logic gate design using time evolving curve of the output power as shown in Fig. 11. For TE mode, at steady-state, ct=37.4 μm or t=0.360 ps, time due to transmission delay is t_1=0.245 ps and time taken by output power to climb from 0.1% to 90% of P_{av} is t_2=0.115 ps, a narrow pulse width of $2t_2$=0.230 ps. Thus, the response time of 0.460 ps has been achieved which leads to a bit rate of 2.17 Tbit/s. Similarly, for TM mode, ct=32.0 μm or t=0.230 ps, t_1=0.114 ps, t_2=0.116 ps, $2t_2$ =0.232 ps and the response period of 0.464 ps and a bit rate of 2.15 Tbit/s have been obtained. Hence, we have achieved the

Table 5
Truth table for NAND optical logic gate for TE and TM polarizations at 1.55 μm wavelength where normalized output power Y is in terms of input power P_a.

NAND gate					
Input A ($\varphi = 0^\circ$)	Input B ($\varphi = 0^\circ$)	Reference signal (R)	Logic output	Normalized output Y (TE)	Normalized output Y (TM)
0	0	1 ($\varphi = 0^\circ$)	1	0.6562 P_a	0.4244 P_a
0	1	1 ($\varphi = 0^\circ$)	1	0.6407 P_a	0.5629 P_a
1	0	1 ($\varphi = 0^\circ$)	1	0.6391 P_a	0.5572 P_a
1	1	1 ($\varphi = \pi$)	0	0.1236 P_a	0.1215 P_a

Table 7
Truth table for XOR optical logic gate for TE and TM polarizations at 1.55 μm wavelength where normalized output power Y is in terms of input power P_a.

XOR gate					
Input A ($\varphi = 0^\circ$)	Input B ($\varphi = 0^\circ$)	Reference signal (R)	Logic output	Normalized output Y (TE)	Normalized output Y (TM)
0	0	0 ($\varphi = 0^\circ$)	0	0	0
0	1	1 ($\varphi = 0^\circ$)	1	0.6407 P_a	0.5629 P_a
1	0	1 ($\varphi = 0^\circ$)	1	0.6391 P_a	0.5572 P_a
1	1	1 ($\varphi = \pi$)	0	0.1236 P_a	0.1215 P_a

Table 8
Truth table for XNOR optical logic gate for TE and TM polarizations at 1.55 μm wavelength where normalized output power Y is in terms of input power P_a.

XNOR gate					
Input A ($\varphi = 0^\circ$)	Input B ($\varphi = 0^\circ$)	Reference signal (R)	Logic output	Normalized output Y (TE)	Normalized output Y (TM)
0	0	1 ($\varphi = \pi$)	1	0.6562 P_a	0.4244 P_a
0	1	1 ($\varphi = \pi$)	0	0.1716 P_a	0.0902 P_a
1	0	1 ($\varphi = \pi$)	0	0.1722 P_a	0.0920 P_a
1	1	1 ($\varphi = 0^\circ$)	1	0.7448 P_a	0.7453 P_a

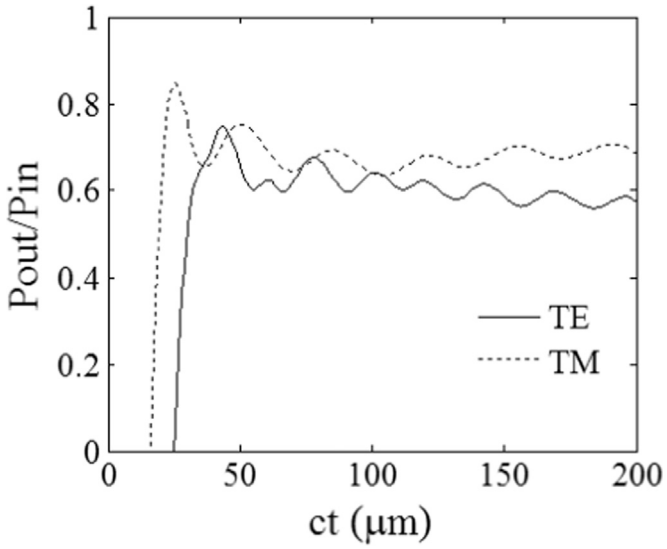

Fig. 11. Response time in terms of time evolution of the output power for all optical logic gate design for both TE and TM polarizations.

improved values of bit rate and response period for both TE and TM modes at a wavelength of 1.55 μm. The results indicate that the proposed design behaves as all-optical logic gates.

3. Conclusion

In this paper, we have reported the design and performance characteristics of polarization independent AND optical logic gate in Y shaped and all optical logic gates in three port waveguide shaped honey comb photonic crystal which yields complete photonic band gap in the range of optical communication window around 1.55 μm. The PWE and FDTD methods have been utilized to determine the optimized parameters. The contrast ratios for both TE and TM modes are comparable at 1.55 μm wavelength which makes this suitable for c-band device design. The response time and bit rate have been calculated for the designs for both the polarizations. The proposed structures are easier to fabricate than alternating slabs conducive to TE and TM band gaps and hence could be a strong candidate for future polarization independent all optical integrated devices.

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Slow light enabled time and wavelength division demultiplexer in slotted photonic crystal waveguide

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Slow light enabled time and wavelength division demultiplexer in slotted photonic crystal waveguide

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Abstract. We have proposed a design for slow light with ultraflat dispersion in a slotted photonic crystal waveguide consisting of a hexagonal arrangement of elliptical air holes on a silicon-on-insulator substrate. The proposed structure has low group velocity and low group velocity dispersion with a wide normalized bandwidth range of 0.0089. The proposed structure can be used as an optical buffer for the storage of a large amount of data due to the large value of the normalized delay bandwidth product equal to 0.634. An optimized structure for a slotted photonic crystal has been analyzed for its applications as both a time and wavelength division demultiplexer. Furthermore, the time delay between two adjacent wavelengths (1550 and 1555 nm) is more than that reported earlier. © *2015 Society of Photo-Optical Instrumentation Engineers (SPIE)* [DOI: 10.1117/1.JNP.9.093063]

Keywords: photonic crystal; slotted photonic crystal waveguide; demultiplexer; optical buffer.

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1 Introduction

Recently, slow light has attracted attention due to its wide applications in optical sensors,[1] time-domain processing of optical signal, i.e., optical delay lines,[2] spatial compression of optical energy,[3] quantum computing, enhancement of light–matter interaction,[4–7] and for the miniaturization of optoelectronic integrated circuits and devices.[8–12] Photonic crystal (PhC) line defect waveguide is one of the most suitable and attractive structures for realizing the slow light effect. This is because such a line defect structure operates at room temperature and has a high potential for on-chip integration by modifying the initial PhC structure.[13] To design novel slow light structures in PhC, the useful bandwidth is the frequency range of the propagating mode that lies below the silica light line. Low group velocity, i.e., high group index and low group velocity dispersion (GVD) with wide bandwidth are the novel properties for design and development of the slow light effect in PhC. The slow light effect with a wide bandwidth range and low GVD has been observed and reported in many experiments.[14,15] The realization of the slow light effect in PhC has been done in many ways, such as by infiltrating with dielectric material,[16,17] by changing holes' sizes and shapes,[18–21] and by adjusting the position of holes adjacent to the waveguide.[22–27]

Recently, the slow light effect in a slotted PhC waveguide (SPhCW) has drawn considerable attention. With this method, light is confined in the low index as compared to the conventional PhCW where light is confined in the high-index region. The confinement of light in the low-index slot waveguide with slow light can be useful in sensor applications where there is an enhancement of the interaction of slow light and measuring samples. Further, there is a strong possibility that SPhC based slow light in a lower-indexed waveguide will be applicable in the design of optical buffers. SPhCW has advantage over the high-index guiding waveguide due to the confinement of light in the air slot as compared to the normal material waveguide. In SPhCW, the material absorption losses are lower compared to the conventional material waveguide, as light is propagating in air rather than in a material medium.

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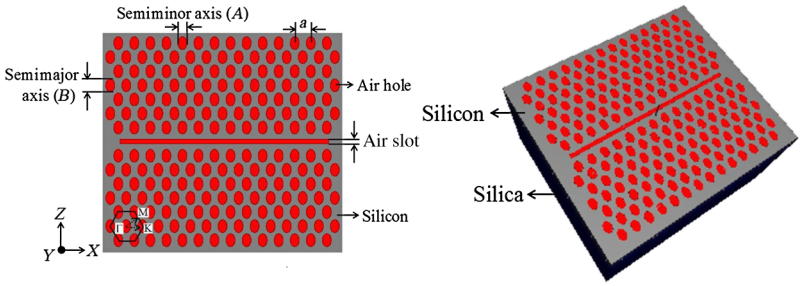

Fig. 1 Schematic representation of the proposed optimized structure with an air slot and regular arrangement of elliptical air holes, where *A* and *B* correspond to the radius of semiminor axis and semimajor axis.

In this paper, we report the design of slotted silicon on insulator (SOI) based PhC structures having a periodic arrangement of elliptical air holes within the silicon substrate to enhance the slow light properties with a low GVD and large bandwidth range. The basic schematic structure of the proposed design has been shown in Fig. 1. The plane wave expansion method and finite-difference time-domain method have been used to analyze the dispersion relation of the slotted waveguide based structure. The proposed structure, i.e., SPhCW, has been analyzed for its application as an optical buffer. Further, the application of a slotted time and wavelength division demultiplexer has been explored. The calculated results show that the time delay between the two adjacent wavelengths (1550 and 1555 nm) in the slotted structure (1165 ps) is higher than that reported earlier (647 ps).[19]

2 Structure Design

In this paper, we propose the design of a slotted waveguide in a PhC structure composed of elliptical air holes laid on an SOI substrate. To design the proposed structure, initially we have assumed a hexagonal arrangement of circular air holes of radius $0.3a$, where $a = 0.4182$ is the lattice constant, embedded in a silicon slab of the SOI substrate. The refractive index of silicon (Si) has been taken to be 3.5 with a thickness 450 nm. The core guiding layer of Si is bonded onto the lower cladding layer of silica (SiO_2) of thickness 3 μm. Further, a W1 PhC channel waveguide along the Γ-K direction has been created by making a single line defect in the proposed PhC structure. Full three-dimensional calculation of the dispersion relation of PhCW is very time consuming, so two-dimensional analysis with the effective refractive index method has been done, which is precise enough for estimating the slow light properties of PhCW. The effective refractive index for the proposed PhC has been calculated to be 3.25. Figure 2(a) shows the band diagram for the initial PhC structure consisting of circular air holes, which shows a band gap in the frequency region from 0.2208 to 0.2883 for TE polarization. Further, the dispersion diagram

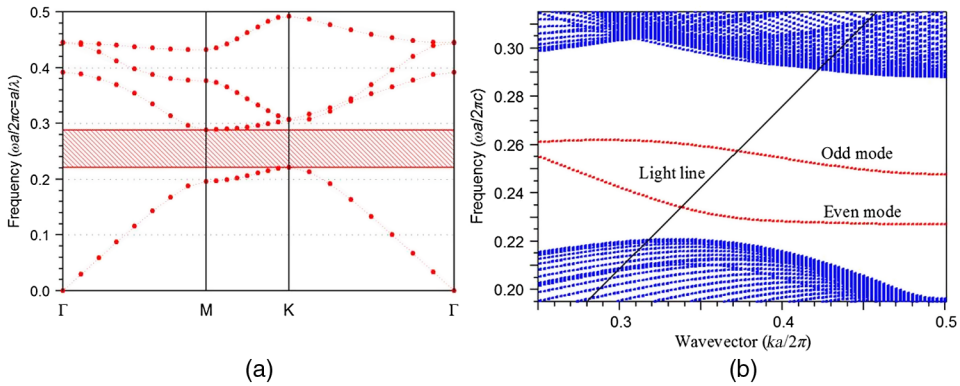

Fig. 2 (a) Band gap for TE polarization and (b) dispersion relation showing two modes (even and odd) below the light line lying within the band gap range for radius of air holes = $0.3a$.

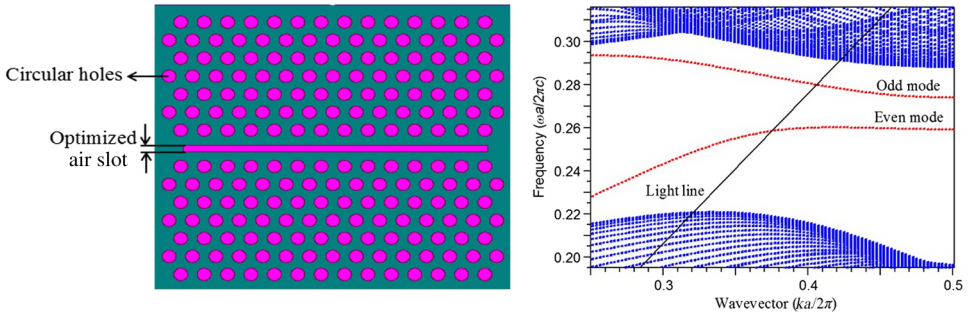

Fig. 3 (a) Basic structure with optimized slot width in W1 photonic crystal (PhC) waveguide and (b) dispersion relation showing two modes with flat band section below the light line for slotted waveguide of width $s = 0.3a$.

for the W1 PhCW has been shown in Fig. 2(b), which exhibits two guided modes existing below the silica light line. An air slot has been created in the W1 waveguide and its dispersion diagram has been obtained as shown in Fig. 3(b). Figure 3(b) also shows the opposite behavior of the two guided modes lying below the silica light line in comparison to the guided modes of the W1 PhCW as shown in Fig. 2(b). This opposite nature/behavior shown by the guided modes of SPhCW is due to the lower effective index in the waveguide than that in the surrounding slab. This leads to the positive slope of the even guided mode in the SPhCW as compared to the negative slope of the even mode in the W1 PhCW. Further, the width of the slot in the W1 PhCW has been optimized. To optimize the slot width, the variation of the guided even mode has been considered, and it has been observed that as the slot width is increased, it gradually shifts the guided mode toward the higher frequency pushing it outside the band gap region. On the other hand, the decrease in the slot width pulls the mode toward the lower frequency pulling it outside the gap region. Hence, an optimum value of slot width, i.e., $s = 0.30a$, has been taken as it places the even guided mode well within the band gap region. Figures 3(a) and 3(b) show the basic structure with an optimized slot width in the W1 PhCW and its dispersion curve. Further, the group velocity and GVD have been calculated to analyze the slow light effect in the basic structure. The calculations show that the group velocity is very low because of the flat dispersion curve, but the GVD turns out to be on the order of 10^8 $\mathrm{ps}^2/\mathrm{km}$, which is large. The large value of the GVD limits the achievable bandwidth for slow light transmission. Thus, the structure needs to be optimized in order to obtain the low value of GVD required for the desired slow light effect.

3 Optimization of Slotted Structure

Various optimization techniques have been proposed to obtain the flat section of the dispersion curve, i.e., the high group index and low GVD. In most of the papers, the shapes, sizes, and positions of the first two rows of air holes adjacent to the air slot have been chosen for modification. In this paper, to optimize the structure, the circular air holes have been replaced by elliptical air holes in the originally considered structure in order to obtain a flat section of the dispersion curve. The semiminor axis (A) and semimajor axis (B) of the elliptical air holes have been modified and their effect on the dispersion relation has been analyzed. Further, the even mode has been used for analysis of the slow light effect because most of the energy in the SPhCW is concentrated in the even mode due to the symmetric constraint caused by air holes. Figure 4(a) shows the dispersion diagram for the even guided mode when A is fixed at $0.28a$ while B is varied from $0.36a$ to $0.44a$. From Fig. 4(a), it is evident that the dispersion curves shift toward the higher frequency as the value of B is increased. Moreover, with the increase in B, the dispersion curve becomes flatter at the high wave vector values. Similarly, when the semimajor axis B is fixed at $0.40a$ and the semiminor axis A is varied from $0.24a$ to $0.32a$, the dispersion curve again shifts toward the higher frequency, as shown in Fig. 4(b). Keeping in view the variation observed in the dispersion curves due to the change of semimajor and semiminor axes of the elliptical air holes, the final parameters of the structure have been taken as $A = 0.28a$ and

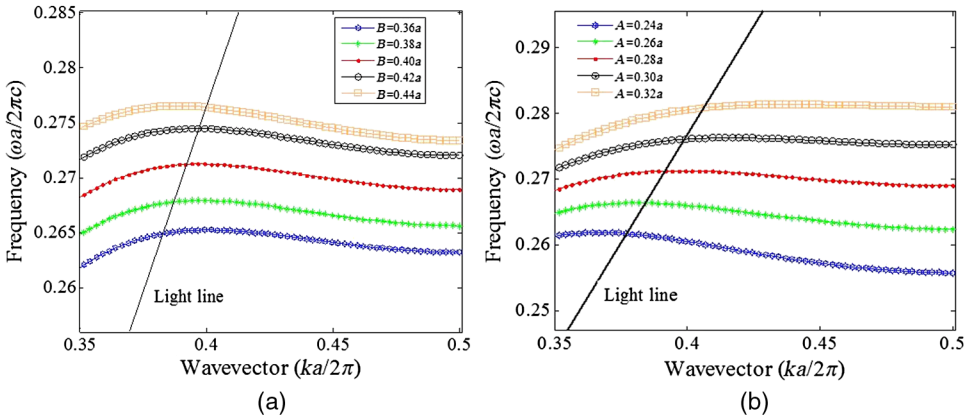

Fig. 4 Variation of dispersion curve of slot even mode (a) when semiminor axis A is fixed and semimajor axis B is varied and (b) when semimajor axis B is fixed and semiminor axis A is varied.

$B = 0.40a$ with $s = 0.3a$. Figure 5 shows the dispersion curve representing the even mode for the optimized structure. The band diagram for the optimized structure does not show any variation as compared to the basic structure for TE polarization.

4 Results and Discussion

The key characteristic of a slow mode is its group velocity (v_g), defined as the velocity with which the envelope of a short pulse propagates through space and calculated by the slope of the dispersion curve in the band structure diagram, i.e.,

$$v_g = \frac{d\omega}{dk}, \tag{1}$$

where ω is the angular frequency and k is the wave propagation vector along the waveguide. For slow light devices, the two basic figures of merit commonly used to describe slow modes are the group index and slowdown factor. The group index (n_g) is defined as the speed of the mode with respect to the speed of light in vacuum c, i.e.,

$$n_g = \frac{c}{v_g} = c\frac{dk}{d\omega} = \frac{d(ka/2\pi)}{d(\omega a/2\pi c)}. \tag{2}$$

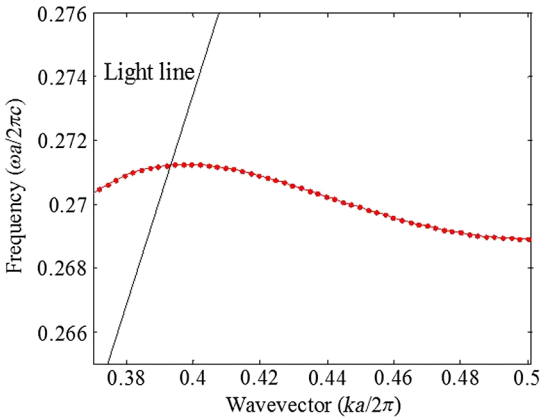

Fig. 5 Dispersion relation representing the even mode for the optimized structure with values $s = 0.3a$, $A = 0.28a$, and $B = 0.40a$.

The slowdown factor S is defined as the ratio of the phase velocity (v_p) over the group velocity, i.e.,

$$S = \frac{v_p}{v_g}. \tag{3}$$

The GVD (β) is defined as the second-order derivative of the dispersion relation or derivative of the inverse group velocity with respect to angular frequency given by

$$\beta = \frac{d^2k}{d\omega^2} = \frac{1}{c}\frac{dn_g}{d\omega} = \frac{d}{d\omega}\left[\frac{1}{d\omega/dk}\right] = -\frac{1}{(d\omega/dk)^3}\frac{d^2\omega}{dk^2} = -\frac{1}{v_g^3}\frac{d^2\omega}{dk^2}. \tag{4}$$

Equation (4) indicates the inverse relation of GVD and group velocity. The increase of GVD (the decrease in group velocity) causes the spreading of the optical pulse. But the proposed structure has been optimized to exhibit a low group velocity and low GVD. Figure 6 shows the variation of group velocity and GVD with respect to the normalized frequency for the slow slotted mode lying below the light line, i.e., within the normalized frequency range from 0.2689 to 0.2713. The value of the group velocity varies from $0.0017c$ to $0.0053c$, and GVD lies in the range of 10^4 ps^2/km and has both negative and positive values. The flat section of the GVD curve has been considered as the place where the extreme negative and positive values of GVD tend to seriously broaden the optical pulse width. Figure 6 shows that the flat section of GVD curve corresponds to the bandwidth range of $\Delta\nu = \Delta\omega/2\pi = 1.72$ THz or $\Delta\lambda = 14$ nm, where $\Delta\omega$ is the change in frequency and $\Delta\lambda$ is the change in wavelength. The maximum group velocity ($0.034c$) and very low value of GVD ($\sim$1) have been achieved near the mid-frequency, i.e., $(\omega a/2\pi c) = 0.2703$. The very low GVD value has been obtained over the wide spectral bandwidth of 1.72 THz. At 1550 nm, the slowdown factor of $S = 18.50$ has been obtained.

4.1 *Applications*

The optimized structure with both low group velocity and low GVD has a broad bandwidth and finds applications like optical buffers for storage of data and time and wavelength division demultiplexing (TDM and WDM).

4.1.1 *Optical buffer*

Another parameter, namely the delay bandwidth product (DBP), plays a significant role for the application of slow light in optical buffers. DBP represents the number of bits that can be stored in a slow light device given by

$$\mathrm{DBP} = T_d \cdot B, \tag{5}$$

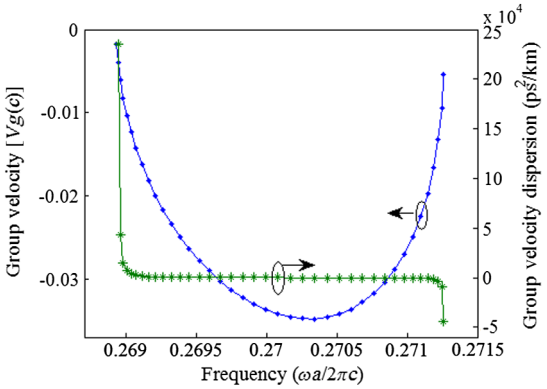

Fig. 6 Variation of group velocity and group velocity dispersion with respect to the normalized frequency of the optimized structure.

where T_d is the propagation time of a pulse in the waveguide and B is the bandwidth. For a particular length (L) of the waveguide and with minimum distortion of the propagating pulse, the upper limit on the DBP is given by[28]

$$\mathrm{DBP} = T_d \cdot B \le \frac{L}{\tilde{V}_g}\left(\frac{1}{4\pi L|\beta|}\right)^{1/2} \le \left(\frac{L}{4\pi}\right)^{1/2}\left(\frac{1}{\tilde{V}_g}\cdot\frac{1}{|\beta|^{1/2}}\right), \tag{6}$$

where $\tilde{V}_g$ is the average group velocity.

Equation (6) indicates that for a particular length of the structure, the DBP is inversely proportional to the average group velocity and GVD. Thus, to increase the value of DBP, both the average group velocity and GVD should be less. The proposed SPhCW structure has been optimized in order to obtain the maximum limit/value of DBP, which means that for our structure, the value of DBP is not higher than that reported earlier. For normalized frequency $(\omega a/2\pi c) = 0.2698$, i.e., at a wavelength of 1550 nm, the value of the average group velocity is $0.032c$ and the GVD is 85.05 $\mathrm{ps}^2/\mathrm{km}$ as calculated from Fig. 6. The calculated value of $\tilde{V}_g/|\beta|^{1/2} = 0.29\ \mathrm{cps\,km}^{1/2}$ is much less than that of $4.4\ \mathrm{cps\,km}^{1/2}$ as reported in Ref. 28. The observed value of $\tilde{V}_g/|\beta|^{1/2} = 0.79\ \mathrm{cps\,km}^{1/2}$ for the slowest velocity ($0.0017c$) achieved at normalized frequency $(\omega a/2\pi c) = 0.2689$, i.e., at wavelength of 1555 nm, is also less than that in Refs. 29 and 28. Further, to measure the buffering capacity, the normalized delay bandwidth product (NDBP) has been calculated, which is defined as

$$\mathrm{NDBP} = \tilde{n_g} \cdot \frac{\Delta\omega}{\omega_0}, \tag{7}$$

where $\tilde{n_g}$ is the average group index in the frequency range $\Delta\omega$ and can be calculated as

$$\tilde{n}_g = \int_{\omega_0-\Delta\omega/2}^{\omega_0+\Delta\omega/2} n_g(\omega)\frac{d\omega}{\Delta\omega}, \tag{8}$$

where ω_0 is the central normalized frequency. Figure 7 shows the variation of group velocity and group index with respect to the normalized frequency. From Fig. 7, the average group index has been obtained as $\tilde{n_g} = 71.24$ and the NDBP, calculated in the normalized bandwidth of $\Delta\omega/\omega_0 = 0.0089$ around central normalized frequency, $\omega_0 = 0.2689$, is 0.634. Despite the fact that in the proposed structure, light has been confined in the air slot, the value of NDBP is greater than that reported in the literature[30,29,28] where light propagates in the medium. Therefore, the proposed slotted waveguide based design can be used as an optical buffer without a nonlinear effect. In the proposed structure, light guidance is in the air, which does not show any nonlinear behavior unless very high values of power are employed.

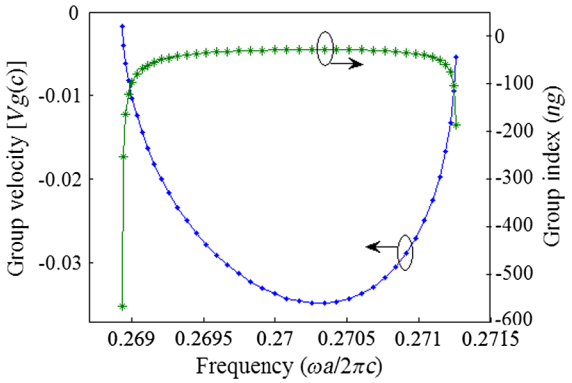

Fig. 7 Variation of group velocity and group index with respect to the normalized frequency of the optimized structure.

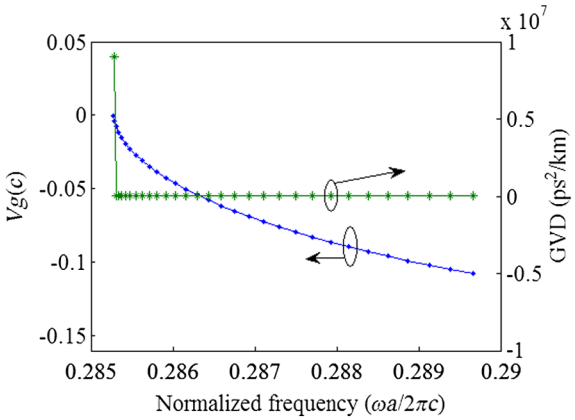

Fig. 8 Variation of group velocity and group velocity dispersion with respect to the normalized frequency of the optimized structure.

4.1.2 *Time and wavelength division demultiplexer*

Further, the optimized SOI based SPhCW structure has been investigated for its application as a TDM and WDM. For the applications of the proposed structure as TDM and WDM, the variations of group velocity and GVD with respect to the normalized frequency for the dispersion curve of odd mode lying below the light line have been plotted as shown in Fig. 8. At a wavelength of 1450 nm, the group velocity and GVD have been calculated to be $0.092c$ and 12.41 ps^2/km, which implies less distortion. However, at a wavelength of 1550 nm, the group velocity and GVD have been earlier calculated to be $0.032c$ and 85.05 ps^2/km.

Thus, the signal at a wavelength of 1450 nm travels three times faster than the signal at a wavelength of 1550 nm. Since different wavelengths reach the output end at different times, the proposed SOI based SPhCW structure can be used in applications like TDM and WDM.

For the transmission length of $20a$, the time delay between input and output peak at $(\omega a/2\pi c) = 0.2698$, i.e., at a wavelength of 1550 nm, has been calculated to be 0.87 ps, which corresponds to the velocity of $0.032c$ as shown in Fig. 9. Similarly, for a wavelength of 1555 nm at which slowest velocity has been achieved, i.e., $0.0017c$, the time delay has been calculated to be 16.40 ps. For a wavelength of 1450 nm, the time delay has been found out to be 0.30 ps. Since different time delays have been achieved for different wavelengths, the proposed SPhCW structure can be used as both a time and wavelength division demultiplexer (Fig. 10).

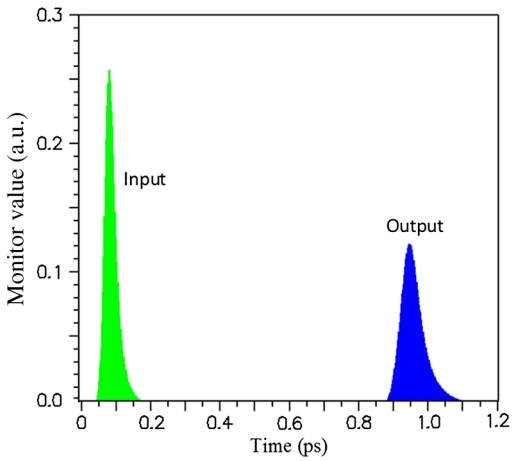

Fig. 9 Time-domain Gaussian optical pulse propagation in the slotted PhC waveguide (PhCW) for $\lambda = 1550$ nm.

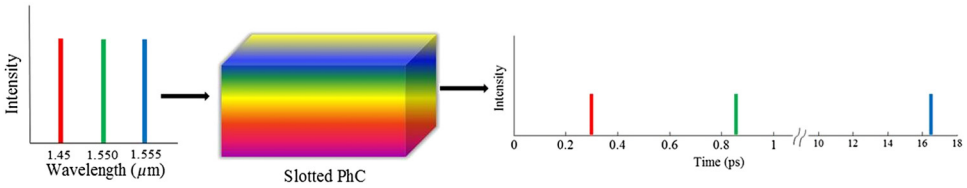

Fig. 10 Schematic representation of pulse separation in slotted PhCW for time and wavelength division demultiplexing at wavelengths of 1450, 1550, and 1555 nm.

Table 1 Comparison of time delay between two wavelengths at transmission length of 600 μm.

Wavelength (nm)	Time delay (ps)	Difference in time delay	Reference
1550	65	1165	Present work
1555	1230		
1550	57	647	19
1555	704		

If we assume the device transmission length to be 600 μm, the time delay for wavelengths of 1550 and 1555 nm has been calculated and compared with the reported value in Table 1. The improved time delay can be utilized for the effective demultiplexing of the two wavelengths in the optical communication window and may find applications in the design and development of optical devices.

The proposed device has significant practical uses in optical devices and will have certain types of losses. The losses in PhCW based optical devices are basically due to coupling, transmission, and deviation in hole size. In addition, the slow light in SPhCW may find coupling losses at the interface of fast and slow light regions, which could result in reflection at the interface of the coupling waveguide and SPhCW. The proposed structure has a transmission loss of 5.99 dB for a device length of 4.18 μm at a wavelength of 1550 nm, which has been obtained as the ratio of change in power to the input power, i.e.,

$$10 \log\left(\frac{P_{\text{out}} - P_{\text{in}}}{P_{\text{in}}}\right), \tag{9}$$

where P_{out} is the output power received at the output end and P_{in} is the input power launched at the input end.

5 Conclusion

In this paper, a new design of SPhCW on an SOI substrate with elliptical air holes in a hexagonal arrangement has been reported. The low group velocity and low GVD with a wide bandwidth range (0.0089) has been attained. The slowdown factor of 18.50 shows the slow light behavior in the optimized design. Though the light has been confined in the air slot, the high value of NDBP (0.634) has been achieved, which can be of great potential for the proposed waveguide to be used as an optical buffer without a nonlinear effect. Also, the improved time delay of the waveguide finds applications in the TDM and the design of WDM devices in the optical communication window.

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Complete photonic bandgap-based polarization splitter on silicon-on-insulator platform

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Complete photonic bandgap-based polarization splitter on silicon-on-insulator platform

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Abstract. We propose a design for a polarization beam splitter based on the phenomenon of a photonic crystal directional coupler. The design consists of a honeycomb lattice arrangement of air holes of different radii in a silicon-on-insulator substrate exhibiting a complete photonic bandgap. The results obtained by the finite-difference time domain method show that the extinction ratio for transverse electric (TE) and transverse magnetic (TM) polarizations is 24.56 and 28.29 dB, respectively, at a wavelength of 1.55 μm. The degree of polarization for TE polarization is 99.29% and for TM polarization is 99.70%. Hence, the proposed design can be efficiently used as a polarization splitter for on-chip integrated devices. © *2016 Society of Photo-Optical Instrumentation Engineers (SPIE)* [DOI: 10.1117/1.JNP.10.026023]

Keywords: photonic crystal; polarization splitter; directional coupler; silicon-on-insulator.

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1 Introduction

A polarization beam splitter is an important functional device in optical integrated circuits that split the orthogonally polarized components of the guided waves. They have been widely used in many applications, such as optical sensors,[1] optical imaging,[2] optical data storage,[3] and optical communications.[4] Various types of polarization beam splitters have been implemented so far using a Mach–Zehnder interferometer,[5] directional coupling,[6–9] photonic crystal structures,[10–12] negative refraction,[13] guided resonance,[14] self-collimation, photonic crystal ring resonators,[15] and multimode interference.[16–18] Among these, some are relatively bigger and longer in size, while others are relatively complex. Over the past decades, most of the proposed polarization beam splitters are based on two-dimensional (2-D) free-standing photonic crystals,[10,12,19] which offer mass manufacturing possibilities due to their ultrasmall size, compactness, and low loss. However, these polarization beam splitters have problems in their mechanical stability. Recently developed 2-D photonic crystals in the silicon-on-insulator (SOI) platform provide a versatile platform for on-chip device design as they provide higher mechanical stability and are easier to fabricate.

In this paper, we have proposed a design for polarization beam splitter on SOI substrate based on a photonic crystal directional coupler. The proposed design consists of a honeycomb lattice arrangement with two different air holes in the SOI substrate. The structure exhibits a complete photonic bandgap for a range of wavelength that has been used for the design of the proposed polarization splitter. The characteristics of the polarization splitter have been analyzed by using the plane wave expansion (PWE) method and the finite-difference time domain (FDTD) method using the commercial software RSoft Bandsolve and Fullwave version 9.0. The coupling characteristics such as extinction ratio, insertion loss (IL), excess loss, coupling ratio, and degree of polarization are enhanced as compared to the earlier reported results.[20]

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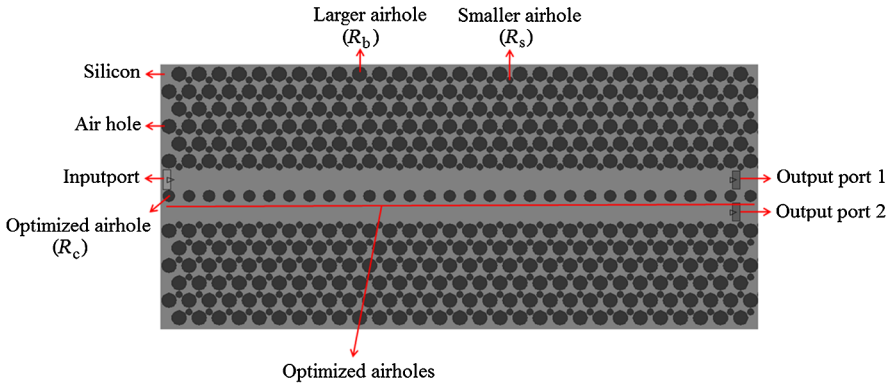

Fig. 1 Schematic representation of the polarization splitter on SOI substrate where R_b and R_s represent the radius of the larger and smaller air holes and R_c represents the radius of the optimized air holes separating the two waveguides.

2 Structure Design and Analysis

A photonic crystal polarization beam splitter in SOI substrate has been proposed as shown in Fig. 1. A honeycomb lattice photonic crystal has been considered in order to obtain a complete photonic bandgap. A honeycomb lattice arrangement of air holes of two different radii on silicon substrate of height $h = 0.25$ μm has been chosen. The radius of larger and smaller air holes has been taken as $R_b = 0.36a$ and $R_s = 0.16a$, respectively, with the lattice constant $a = 0.565$ μm. The proposed structure exhibits a complete photonic bandgap within the normalized frequency range of 0.3520 to 0.3836 as shown in Fig. 2. The effective index for transverse electric (TE) mode and transverse magnetic (TM) mode has been obtained to be n_{eff} (TE) $= 2.89$ and n_{eff} (TM) $= 2.15$ as calculated using the finite-element method.[21] Further, a waveguide directional coupler has been created in the proposed photonic crystal structure. To create a waveguide directional coupler, two closely spaced waveguides in the ΓK direction have been created and separated from each other by a row of air holes of radii (R_c). The radius R_c is smaller than the radius R_b and larger than the radius R_s. The dispersion diagrams for both TE and TM polarizations have been calculated using the PWE method. The variation of dispersion relation with the radius of the air holes separating the two waveguides for TE and TM polarizations has been shown in Figs. 3 and 4, respectively. From Fig. 4, it has been found that there are two modes for TM polarization, i.e., one odd mode and one even mode, whereas a single mode is available for TE polarization as shown in Fig. 3. To design the proposed structure as a polarization splitter, a common frequency

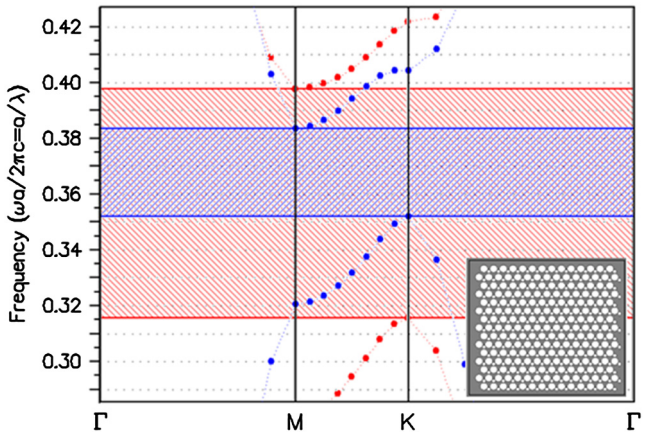

Fig. 2 Photonic band diagram for the honeycomb lattice arrangement, where the red region corresponds to the TE polarization and blue region corresponds to the TM polarization.

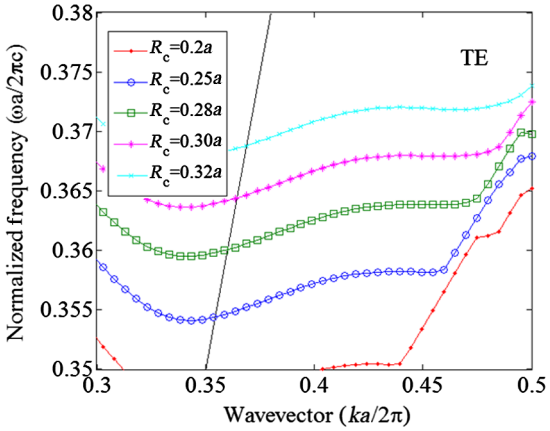

Fig. 3 Dispersion relation of TE polarized modes with the radius of the central row of air holes separating the two waveguides.

region has been chosen from Figs. 3 and 4, where the defect modes for both TE and TM polarizations lie within the desired normalized frequency range. For different values of R_c only, the normalized frequency range varies and not the performance of the proposed splitter. Figures 3 and 4 indicate that for radius $R_c = 0.29a$ the defect mode for both TE and TM polarizations lie within a desired normalized frequency range of 0.3639 to 0.3651 as shown in Fig. 5. Figure 5 indicates that the structure exhibits a coupling region for TM polarization due to the presence of even and odd modes, whereas no such region is exhibited for TE polarization, which has only one mode. The coupling length, which is defined as $L = \pi/|k_e - k_o|$, where $k_e = 0.3873$ and $k_o = 0.4108$ is the propagation constant of both the even and odd modes of the TM polarization, respectively, has been calculated to be 12.02 μm at $R_c = 0.29a$ for a normalized frequency $\omega a/2\pi c = 0.3647$ (i.e., at a wavelength of 1.55 μm) using Fig. 5.

This has also been verified using the FDTD method. The variation of intensity in the proposed waveguide directional coupler has been obtained using the FDTD method as shown in Fig. 6 for both TE and TM polarizations. Figure 6 shows that at a distance of 12 μm the wave/light with TM polarization couples to the another waveguide, i.e., output port 2, whereas light with TE polarization continues to propagate in the same waveguide, i.e., at the output port 1. Thus, at a distance of 12 μm, a light with TM polarization is in the cross state whereas the light with TE polarization remains in the bar state. Thus, the two polarizations can be separated at a distance of 12 μm.

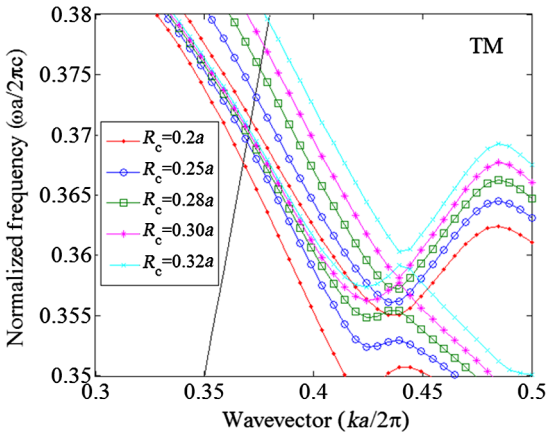

Fig. 4 Dispersion relation of TM polarized modes with the radius of the central row of air holes separating the two waveguides.

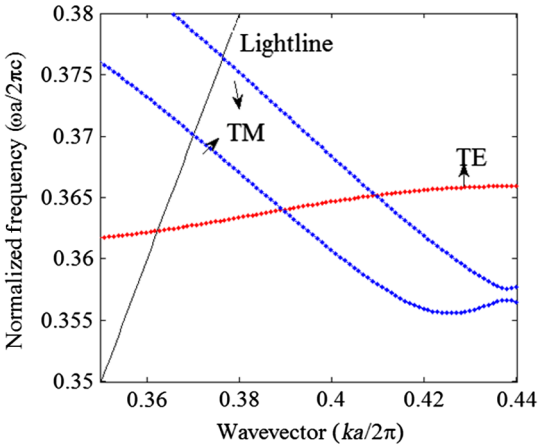

Fig. 5 Dispersion relation at radius $R_c = 0.29a$ of the central row of air holes separating the two waveguides for both the polarizations.

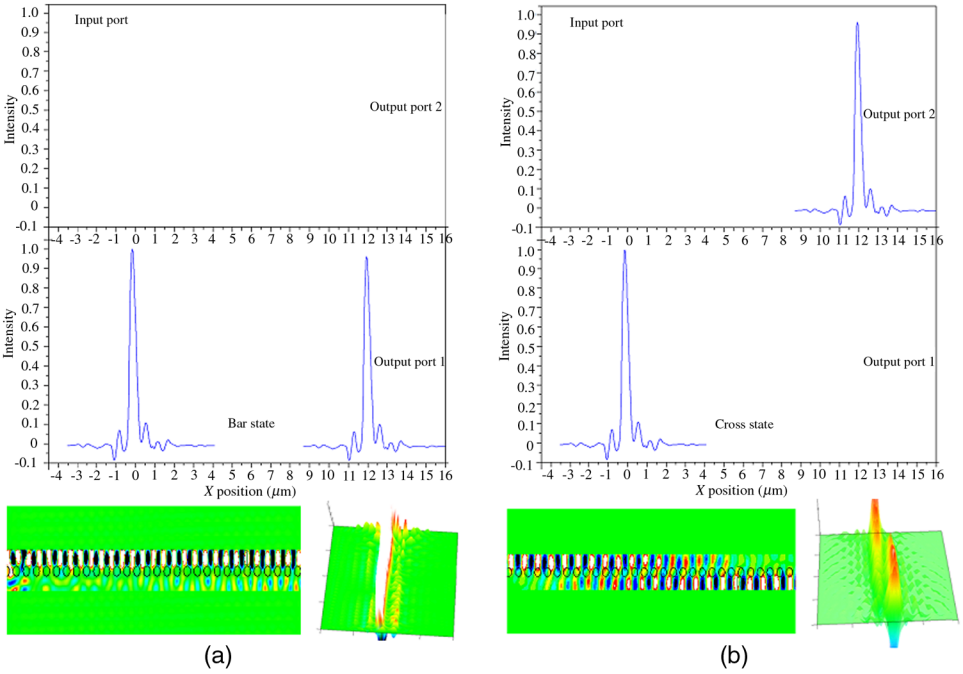

Fig. 6 The intensity distribution at a distance of 12 μm for (a) TE polarization and (b) TM polarization.

3 Results and Discussion

The proposed photonic crystal polarization splitter on SOI substrate can split the two polarizations at a distance of 12 μm as calculated using the PWE calculations and FDTD simulations at 1.55 μm. To further evaluate the performance of the polarization splitter, the intensity distribution obtained from the FDTD simulations has been analyzed for the calculation of extinction ratio, IL, coupling ratio, and excess loss. The extinction ratio for TE polarization and TM polarization has been calculated at a wavelength of 1.55 μm, which is defined as

$$\mathrm{ER_{TE}} = 10\log_{10}\left(\frac{\text{Power for TE at output 1}}{\text{Power for TE at output 2}}\right) \tag{1}$$

Table 1 Comparison of the extinction ratio with wavelength for both TE and TM polarizations.

Wavelength (μm)	ER_{TE} (dB)	ER_{TM} (dB)
1.5475	24.34	28.41
1.5485	24.45	28.35
1.5495	24.54	28.29
1.5505	24.58	28.30
1.5515	24.63	28.36
1.5525	24.67	28.33

$$\mathrm{ER_{TM}} = 10\log_{10}\left(\frac{\text{Power for TM at output 2}}{\text{Power for TM at output 1}}\right). \tag{2}$$

The polarization splitter exhibits an extinction ratio of 24.56 dB for TE polarization (ER_{TE}) and 28.29 dB for TM polarization (ER_{TM}). The values of extinction ratio remain the same within the desired wavelength range as shown in Table 1. Hence, it has been concluded that the proposed design can work efficiently within the normalized bandwidth range as calculated by the PWE method and FDTD method for both the polarizations.

The IL, defined as the ratio of input power to the output power in dB, i.e.,

$$\mathrm{IL} = 10\log_{10}\left(\frac{\text{Input Power}}{\text{Output Power}}\right) \tag{3}$$

has been calculated to be 0.71 and 0.60 dB for TE and TM polarizations, respectively, at 1.55-μm wavelength. Variation of IL with wavelength for both TE and TM polarizations has been shown in Table 2.

The excess loss, defined as the ratio of input power to the total output power in dB, i.e.,

$$\mathrm{EL} = 10\log_{10}\left(\frac{\text{Input Power}}{\text{Total output Power}}\right) \tag{4}$$

for the proposed structure has been calculated to be -2.36 dB at a wavelength of 1.55 μm. The comparison of excess loss with wavelength has been calculated and given in Table 3.

The corresponding coupling ratio, defined as the ratio of optical power from one output port to the total output power, in percentage, has been found to be 49.19% for TE polarization and

Table 2 Comparison of the IL with wavelength for both TE and TM polarizations.

Wavelength (μm)	IL_{TE} (dB)	IL_{TM} (dB)
1.5475	0.88	0.47
1.5485	0.77	0.54
1.5495	0.73	0.60
1.5505	0.64	0.59
1.5515	0.59	0.57
1.5525	0.55	0.56

Table 3 Comparison of the excess loss with wavelength

Wavelength (μm)	EL (dB)
1.5475	−2.34
1.5485	−2.36
1.5495	−2.37
1.5505	−2.40
1.5515	−2.46
1.5525	−2.46

50.55% for TM polarization at a wavelength of 1.55 μm. The degree of polarization P in each output port has also been calculated using the definition of P as

$$P = \frac{|P_{\mathrm{TE}} - P_{\mathrm{TM}}|}{|P_{\mathrm{TE}} + P_{\mathrm{TM}}|}, \tag{5}$$

where P_{TE} is the power for TE polarization and P_{TM} is the power for TM polarization. The degree of polarization for TE mode and TM mode has been calculated to be 99.29% and 99.70%, respectively. Thus, the optimized design can efficiently split the two polarizations at a distance of 12 μm. Hence, the proposed design can be used as a polarization splitter for on-chip integrated devices.

4 Conclusion

In this paper, we have demonstrated a design for the polarization beam splitter in SOI substrate consisting of a honeycomb lattice arrangement of air holes of different radii. The proposed design is based on the concept of a photonic crystal directional coupler exhibiting complete photonic bandgap. The structure should find various applications in the future on-chip polarization splitters owing to its miniature size and easy fabrication capabilities using modern technologies.

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