CHAPTER-1 →

INTRODUCTION

1. Introduction

This dissertation presents Voltage Differencing Buffered Amplifier (VDBA) and its applications. Voltage Differencing Buffered Amplifier is an active building block which can play an important role in Analog Signal Processing applications. A lot of active devices have been proposed till now by the researchers and the research is a never ending procedure, hence a lot of active devices may still be proposed in the near future. Since the overall work of this study is focused on use of active device VDBA in signal processing, we have started with the definition of signal processing.

2. Signal Processing

Signal processing is an area of system engineering, electrical engineering and applied mathematics that deals with operations on or analysis of signals, or measurements of time-varying or spatially varying physical quantities. Signals of interest can include sound, electromagnetic radiation, images, and sensor data, for example biological data such as electrocardiograms, control signals ,telecommunication transmission signals, and many others**.** Amplifiers, Filters, Integrators, Differentiators and Oscillators etc. are main means of signal processing.

It can be classified into two broad categories: (i) Analog Signal Processing (ii) Digital Signal Processing.

2.1 Analog Signal Processing is any signal processing conducted on analog signals by analog means. "Analog" indicates something that is mathematically represented as a set of continuous values. This differs from "digital" which uses a series of discrete quantities to represent signal. Analog values are typically represented as a voltage, electric current or electric charge around components in the electronic devices. An error or noise affecting such physical quantities will result in a corresponding error in the signals represented by such physical quantities.

Examples of analog signal processing include crossover filters in loudspeakers, "bass", "treble" and "volume" controls on stereos, and "tint" controls on TVs. Common analog processing elements include capacitors, resistors, inductors and transistors

2.2 Digital signal processing is the mathematical manipulation of an information signal to modify or improve it in some way. It is characterized by the representation of discrete time, discrete frequency, or other discrete domain signals by a sequence of numbers or

symbols and the processing of these signals. Digital signal processing and analog signal processing are subfields of signal processing. DSP includes subfields like: audio and speech signal processing, sonar and radar signal processing, sensor array processing, spectral estimation, statistical signal processing, digital image processing, signal processing for communications, control of systems, biomedical signal processing, seismic data processing, etc.

The goal of DSP is usually to measure, filter and/or compress continuous real-world analog signals. The first step is usually to convert the signal from an analog to a digital form, by sampling and then digitizing it using an analog-to-digital converter (ADC), which turns the analog signal into a stream of numbers. However, often, the required output signal is another analog output signal, which requires a digital-to-analog converter (DAC). Even if this process is more complex than analog processing and has a discrete value range, the application of computational power to digital signal processing allows for many advantages over analog processing in many applications, such as error detection and correction in transmission as well as data compression

3. Active & Passive Devices used in Signal Processing

3.1 Active Devices

An **active device** is any type of circuit component with the ability to electrically control electron flow (electricity controlling electricity). In order for a circuit to be properly called electronic, it must contain at least one active device. In any Analog Signal Processing circuit the core is built around some active building block .This active building block can be a discrete transistor, a FET/MOSFET (the earlier active building blocks included vacuum tubes etc) or an integrated circuit amplifier like IC 741(Voltage Operational Amplifier) IC 3080(Operational Trans-conductance Amplifier) or IC AD844(Current Feedback Amplifier) etc.

Nowadays with the rapidly going advancements in the semiconductor technologies a trend is emerging wherein different active building blocks to be integrated on the chip along with some passive components so as to be application specific integrated circuits (ASICs) are being introduced. Such devices include Current Conveyors, Derivatives of Current Conveyors, Operational Trans-resistance Amplifier,

Current Differencing Buffered Amplifiers, and Current Differencing Trans-conductance Amplifiers etc.

All active devices control the flow of electrons through them. Devices utilizing a static voltage as the controlling signal are called voltage-controlled devices and the devices utilizing current as controlling signal are called current controlled devices. For the record, vacuum tubes are voltage-controlled devices while transistors are made as either voltage-controlled or current controlled types.

All active devices include in their circuit behavioral diagram one or more of the four types of controlled sources given below.

3.1.1. Voltage Controlled Voltage Source (VCVS)

It is an element with output voltage controlled by input voltage as shown in fig1

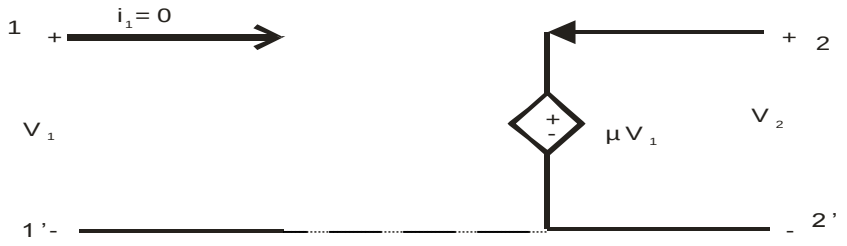

Fig1: Voltage Controlled Voltage Source

Here port-2 is a voltage source whose voltage depends on the voltage across the open circuit of port-1.

The defining equations of VCVS are

v_2=μv_1, i_1=0, R_i =∞ R_o=0…… (1)

The constant μ is a scalar quantity and is called a voltage gain.

3.1.2. Voltage Controlled Current Source (VCCS)

It is an element with output current controlled by input voltage as shown in fig2

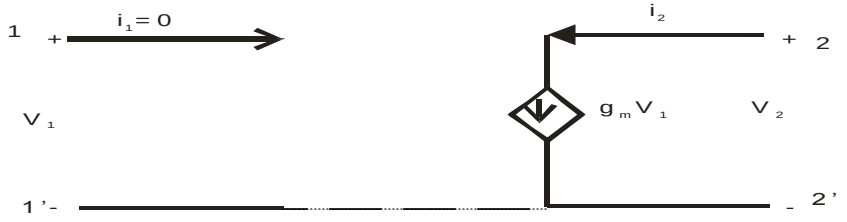

Fig2: Voltage Controlled Current Source

Here port-2 is a current source whose current depends on the voltage across the open circuit of port-1.

The defining equations of VCCS are

i_1=0, i_2=$g_m v_1$. R_i=∞, R_o=0…….. (2)

The constant g_m is called trans-conductance.

3.1.3. Current Controlled Current Source (CCCS)

It is an element with output current controlled by input current as shown in fig3

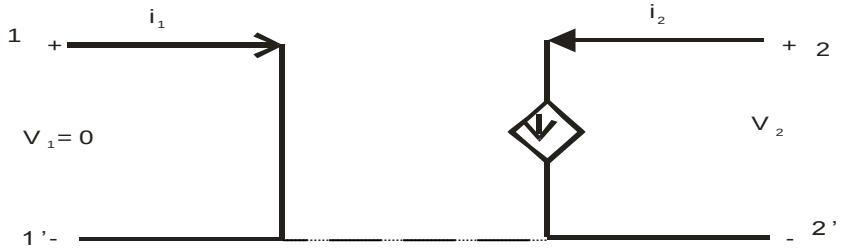

Fig3: Current Controlled Current Source

Here port-2 is a current source whose current depends on the current through the short circuit of port-1.

The defining equations of CCCS are

v_1=0, i_2=αi_1, R_i=0, R_o=∞…….. (3)

The scalar α is known as current gain

3.1.4. Current Controlled Voltage Source (CCVS)

The CCVS is an element with output voltage controlled by input current as shown in fig4

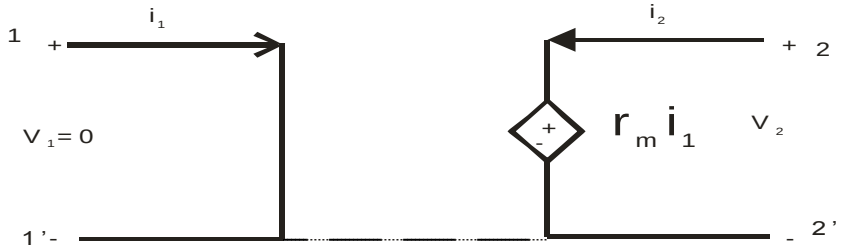

Fig4: Current Controlled Voltage Source

Here port-2 is a voltage source whose voltage depends on the current through the short circuit of port-1.

The defining equations of CCVS are

v_1=0, v_2=$r_m i_1$, R_i=0, R_o=∞…….. (4)

The scalar r_m is called trans-resistance.

3.2 Passive Devices

Components incapable of controlling current by means of another electrical signal are called passive devices. Resistors, capacitors, inductors, transformers, and even diodes are all considered passive devices.

Passive devices are the resistors, capacitors, and inductors required to build electronic hardware. They always have a gain less than one. A combination of passive components can multiply a signal by values less than one, they can shift the phase of a signal, and they can reject a signal because it is not made up of the correct frequencies, they can control complex circuits, but they cannot multiply by more than one because they lack gain. The passive inductor when used for low frequency applications presents different kind of challenges to the Analog signal processing engineer. It is quite bulky and has a very low quality factor and is unsuitable for microminiaturization and is seldom used as such in analog signal processing applications. Instead simulated inductor can be realized with the help of controlled sources and RC elements. In fact a very large body of literature on realization of simulated inductors using different types of active building blocks and RC elements exist.

4. Current-mode versus Voltage-mode Signal Processing

The applications of analog signal processing have followed two trends: (i) voltage mode (ii) current mode. In case of voltage mode circuits the signals representing the information being processed are in the form of electric voltages whereas in case of current mode circuits the signals representing the information being processed, are in the form of electric currents .This definition of current mode and voltage mode circuits is not highly precise because every circuit node has an associated voltage and every branch an associated current, and it is a matter of definition which ones represent signals and which ones do not. However most of literature available on signal processing uses this definition. There are indeed performance differences between published voltage mode and current mode circuits. The reason for this is that voltage-mode and current-mode circuits are often built with different design techniques. Voltage mode circuits often use higher loop gains than current mode circuits. Electronic filters are very often used as building blocks of almost all electronic appliances. Requirements for integration lead to

the active RC filter design techniques. First active filters were designated in voltage mode operation and they used Op-Amps as their active elements. As integration density was being increased, supply voltage was being decreased. Also demand for processing of signals at higher frequencies appeared. However constant gain bandwidth product of Op-Amps limits their usage from point of view of frequency range. Solution to this problem was found in current mode. The current transmission within the circuit is not limited so much due to parasitic properties. Traditional differential voltage amplifiers belong to voltage mode circuits. Their dynamic range is smaller and power cost is larger In contrast to the conventional voltage- mode, the current- mode circuits can exhibit under certain conditions-among other things-higher bandwidth and better signal linearity. Since they are designed for lower voltage swings, smaller supply voltages can be used.

A research monograph on Analog IC design using current mode approach has been presented in [1].Various developments in the field of current mode circuit techniques have been surveyed in it. Due to the advances made in integrated circuit(IC) technology during the last two decades, circuit designers have quite often exploited the potential of current-mode analog techniques for evolving elegant and efficient solutions to several circuit design problems. Some of the advantages which the circuit designers using the current-mode approach have exploited include

(i) Higher frequency range
(ii) Lower Power consumption
(iii) Simplified circuit topologies
(iv) Improved Linearity
(v) Better Accuracy etc.

It may be mentioned here that all of the above advantages are not present in all current-mode circuits. A critique of the current-mode circuit design approach has been presented in [2] wherein it has been opinioned that the terminology current-mode should not be used for all analog circuit design.

5. Trends in the development of Signal Processing

The objective of this dissertation is the simulation and analysis of Voltage Differencing Buffered Amplifier (VDBA) and its applications in analog signal processing. The circuit principle of VDBA block was first proposed by Biolek, Senani, Biolkova and Kolka in [3]. In [3] an excellent survey of various active building blocks proposed by different research groups till 2007-2008 has been presented. This paper has very systematically outlined the developments of these blocks and proposed many other active building blocks possessing special features suitable for different signal processing applications. Since the VDBA block has been realized with OTAs and differential amplifiers, it is worthwhile to present some of the significant points presented in [3] in the following. The initial set of active elements for analog signal processing is currently evolving in two directions. The first direction is represented by modifying the basic elements such as VFA (Voltage Feedback Amplifier), OTA (Operational Tran conductance Amplifier), and particularly current conveyors (CC). The important motivations for such modifications consist in the effort to increase the application potential of the element. Simultaneously, this element should have a simple internal structure in order to retain low power consumption and high-speed operation.

The second direction of the evolution of the active elements is characterized by the appearance of entirely new elements which extend the original VFA-CFA-OTA-CC set. The current conveyor (CC) is the basic building block of a number of contemporary applications both in the current and the mixed modes. The principle of the current conveyor of the first generation was published in 1968 by Sedra and Smith [4]. In 1970, today's widely used second generation CCII was introduced in [5] and in 1995 the third generation [6]. However, initially during that time, the current conveyor did not find many applications because its advantages compared to the classical Op-Amp were not widely appreciated and any IC implementation of current conveyors was not available commercially. An IC CC, namely PA630, was introduced by Wadsworth [7] in1989 and about the same time AD844 IC was introduced [8].

Ever since their introduction, current conveyors have proved to be functionally flexible and versatile, rapidly gaining acceptance as both a theoretical and practical building block. However it is only in the last ten to twenty years that high performance

implementations have emerged, to enable conveyors now to challenge successfully traditional voltage operational circuits in areas such as active filters, oscillators and amplifiers. In addition, a number of novel circuit functions and topologies have been explored on the broader front of current-mode analogue circuits in, opening up wider area of interest. When configured with other circuit elements real conveyors can perform many analogue signal processing functions, in a similar manner to the way Op-Amps and the ideal concept of Op-Amp are used.

The CCII proves to be a versatile building block that can be used to implement a variety of high performance circuits which are simple to construct. The CCII has a disadvantage that only one of the input terminals has high input impedance. This disadvantage becomes evident when the CCII is required to handle differential signals, as in the case of instrumentation amplifier. The design of such an amplifier requires two or more CCIIs. The DVCC [9] is a novel building block specially defines to handle differential signals. A lot of devices emerged from extension of CCIIs.

Op-Amp is the well known and extremely useful device also available commercially for last four to five decades. Over time, the Op-Amp internal structure has been modified and two basic Op-Amp types –Voltage Feedback Amplifier (VFA) and Current Feedback Amplifier (CFA) [10] have been outlined. However the well known input-output behavior of the ideal Op-Amp in the linear regime is still the same.

OTA (Operational Trans-conductance Amplifier) [11] belongs to the most widespread active elements for on- chip implementation of fast frequency filters. It acts as a voltage-controlled current source with the possibility of electronic adjustment of trans-conductance g_m. Another building block for current- and mixed-mode signal processing, the conventional Trans-impedance Operational Amplifier (TOA) [1], is a combination of the CCII and the voltage buffer amplifier. The well known CFA has an identical internal structure. In a popular CFA from Analog Devices Inc., namely AD844, the z-terminal of the internal CCII+ is brought out which provides more flexibility in its use in several applications [12]. However, in CFAs from other manufacturers [10], the z terminal of the internal CCII is not led out of the device in order to maximize the parasitic trans-impedance and thus the bandwidth. In slower applications, where higher stability is required, the VFAs can be used.

In 1992 a new circuit element called OTRA (Operational Trans-resistance Amplifier) was introduced [13]. In 1999 CDBA (Current Differencing Buffered Amplifier) was introduced [14]. CDBA is also known as DCVC (Differential Current Voltage Conveyor). CDBA, a generalization of OTRA, is a universal element for filter design, primarily for voltage mode operation. CDBA contains the so called CDU (Current Differencing Unit) and the voltage unity gain buffer. Basically CDU is a current conveyor of the MDCC type. It has two low impedance terminals p and n. The difference of currents I_p and I_n flows out of the z terminal and the corresponding voltage drop on the external impedance is copied by the buffer to the w output. That is why the additional impedances are necessary for implementing the feedbacks from the voltage output to the current inputs. It is inconvenient from the point of view of simplicity and low power consumption.

In [15] the CDTA (Current Differencing Trans-conductance Amplifier) active element was described for the first time. The input part of the CDTA is formed –much like for the CDBA-by the CDU. It is followed by the multiple outputs OTA. In principle, CDTA applications do not require the use of external resistors, which are substituted by the internal trans-conductors.

In [3] an analysis of the state of art of active elements for analog signal processing has been presented which support-in contrast to the conventional operational amplifiers-not only the voltage-mode but also the current- and mixed-mode operations. A methodology has been proposed which generates a number of fundamentally new active elements with their potential utilization in various areas of signal processing.

6. Organization of the Dissertation

In this chapter we have presented a general introduction to signal processing, various generic devices used in analog signal processing, voltage and current mode approaches of signal processing. The chapter also included a brief qualitative description of some of the important active building blocks used for analog signal processing.

The Chapter-2 chapter presents the symbolic representation and terminal equations of some of the important active building blocks introduced for analog signal processing during the last two decades.

The Chapter-3 presents a CMOS Voltage Differencing Buffered Amplifier (VDBA) and its characterization.

Chapter-4 presents general signal processing applications of VDBA. PSpice simulations have been presented to verify the workability of these circuits.

Chapter-5 presents a KHN type voltage mod biquad in which VDBA has been used as the active building block.

Chapter-6 presents the summary of the work presented in this dissertation and scope for future work on this topic.

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CHAPTER-2 ⟶

ACTIVE BUILDING BLOCKS

AT A GLANCE

2. Introduction

In the previous chapter we had presented a qualitative description of some of the active building blocks introduced in the domain of analog signal processing during the last two decades. In this chapter we present the symbols, terminal equations and general features of some of those popular active building blocks. We have also included current conveyors and their important derivatives, operational trans-conductance amplifiers and current feedback amplifiers in this chapter, though these blocks were introduced in late sixties, seventies and eighties respectively, because the basic concept underlying most of other blocks draws heartily from these blocks.

2.1 Current Conveyors: Current conveying is the concept in which current is conveyed between two ports at extremely different impedance level. A current conveyor is an abstraction for a three terminal analogue electronic device. There are three versions of generations of the idealized device known as CCI, CCII and CCIII.

The general block representation of CC is shown in fig5

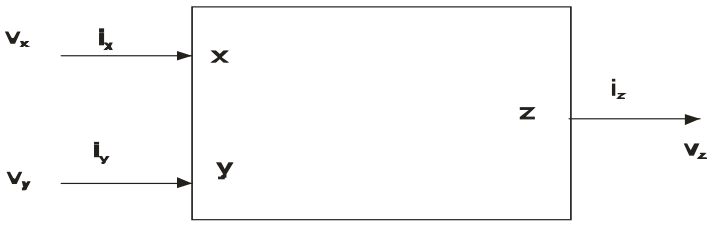

Fig5: Current Conveyor General Block Diagram

2.1.1 The First Generation CCI

The first generation current conveyor was introduced by Sedra and Smith [1].

This is an implementation of a 3 port network and can be described by the following terminal relationships

$$i_y = i_x, v_x = v_y, i_z = i_x \quad \ldots\ldots(1)$$

Using hybrid parameters, we may denote the above terminal relationships in matrix notation

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \quad \text{..... (2)}$$

If the circuit is examined between inputs port x and output port z, it can be considered as a dual to the idealized emitter follower

2.1.2 The Second Generation CCII

To increase the versatility of the current conveyor, a second version in which no current flows in terminal y was introduced in 1970[2].

The terminal relationships in the CCII are given as follows

$$i_y = 0, v_x = v_y, i_z = \pm i_x \quad \text{..... (3)}$$

Using hybrid parameter representation, the above terminal relationships may be denoted in matrix form

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \quad \text{..... (4)}$$

Terminal y exhibits infinite input impedance. Voltage at x follows that applied to y thus exhibits zero input impedance. The current supplied to x is conveyed to the high impedance output terminal z where it is supplied with either positive or negative polarity representing CCII+ or CCII-All currents and voltages in equations (1) and (2) are instantaneous quantities rather than incremental values. This property requires that any implementation of the current conveyor should be directly coupled, should have no offset, and should exhibit linear ideal operation over a wide signal range. CCII is a main current mode circuit. The filters, amplifiers and A/D convertors based on CCII have been proposed. CCII has two shortages: (i) the lack of programmability (ii) larger voltage tracking error from y terminal to x terminal because of the parasitic resistor of x terminal

2.1.3 The Third Generation Current Conveyor(CCIII)

It is defined from the general equations that describe the first and second generation conveyors. It was introduced by Fabre in 1995[3].

The terminal relationships are given below

$$i_y = -i_x, v_x = v_y, i_z = \pm i_x \quad \text{..... (5)}$$

Using hybrid parameter representation, the above terminal relationships may be denoted in matrix form

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \quad \text{..... (6)}$$

The main features of the CCIII are

(i)Low gain errors (high accuracy)

(ii)High linearity

(iii)Wide frequency response

In addition high output resistance at z terminal of the CCIII is required to enable easy cascadability without need for additional active elements in applications. Unfortunately, because of the limited linearity and low output resistance of the basic current mirrors used in the structure of the conventional CCIII [3], its DC and AC performances are low. CCIIIs can be used as active elements for the design of frequency filters.

In [4] Wadsworth introduced a current conveyor topology and monolithic implementation using Current Conveyors. An introduction to commercially available Current Conveyors was given in [5]. Later on a number of active building blocks were introduced using blocks of current conveyors, known as derivatives of current conveyors.

2.2 Differential Voltage Current Conveyor (DVCC)

The differential voltage current conveyor (DVCC) is an extension of the second generation current conveyor (CCII) introduced by Sedra and Smith [2]. It was first proposed in 1997[6]. The CCII proves to be a versatile building block that can be used to implement a variety of high-performance circuits which are simple to construct. The CCII has a disadvantage that only one of the input terminals has high input impedance (the y terminal). The disadvantage becomes evident when the CCII is required to handle differential signals, as in the case of an instrumentation amplifier. The design of such an amplifier requires two or more CCIIs.

DVCC is a novel building block which provides two high –impedance terminals to handle differential input voltage signals. The DVCC is a five-port building block which is defined by the following terminal relationships.

$$V_X = V_{Y1} - V_{Y2}, I_{Y1} = 0, I_{Y2} = 0, I_Z = \pm I_X \quad \text{..... (7)}$$

The general block representation of DVCC is shown in fig6

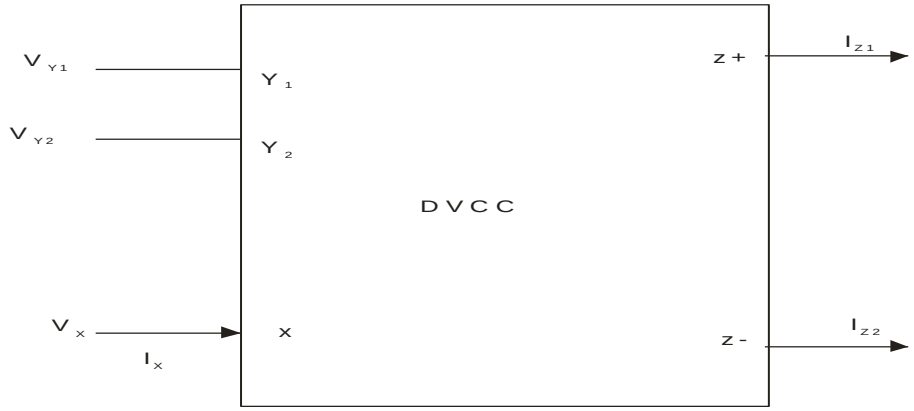

Fig6: DVCC Block Diagram

The terminal relationships may also be represented by the following matrix- equation

$$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Z1} \\ I_{Z2} \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_{Z1} \\ V_{Z2} \end{bmatrix} \quad \text{..... (8)}$$

2.3 Multiple Output Current Conveyors (MOCC)

Traditional differential voltage amplifiers belong to voltage-mode circuits. Their dynamic range is smaller and power cost is larger. Lately current mode (CM) circuits have been receiving significant attention because of their wide bandwidth, greater linearity, wider dynamic range, simple circuitry and low power consumption. Second generation current conveyor (CCII) is a main CM circuit. The filters, amplifiers and A/D convertors based on CCIIs have been developed. However, CCII have two shortages (i) the lack of programmability; (ii) larger voltage tracking error from Y terminal to X terminal because of parasitic resistor of X terminal. In 1995 Fabre proposed a second generation current controlled conveyor (CCIII) constructed by bipolar transistors [7]. The CCIII has

electronic programmability as well as a smaller voltage tracking from Y to X terminal. The current mode filters, oscillators and amplifiers have been developed. A CMOS differential second generation current controlled conveyor with multiple outputs has been implemented in [8]

Circuit Symbol of MO-DCCCII and its port characteristic

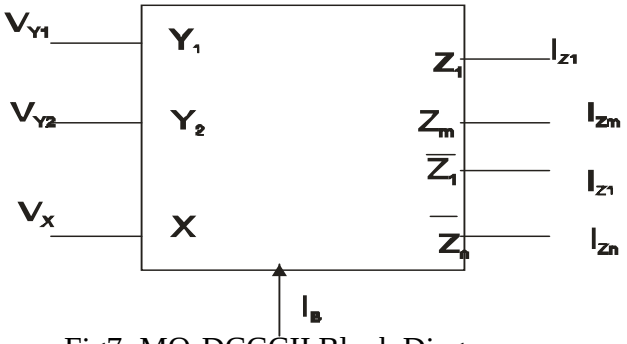

Fig7: MO-DCCCII Block Diagram

Y_1 and Y_2 terminals are two differential voltage inputs and they posses high input impedance. X is called voltage -tracking terminal. $Z_1 \, to \, Z_m$ are non-inverting current outputs, and $\bar{Z}_1 \, to \, \bar{Z}_n$ are inverting current outputs. I_B is bias current, by which the voltage relation between X terminal and Y_1, Y_2 terminals is adjusted. So it has electronic programmability.

The port characteristic of MO-DCCCII is given as the following equations

$$V_X = (V_{Y1} - V_{Y2}) + I_X R_X \quad \text{..... (9)}$$

$$I_{Y1} = I_{Y2} = 0, I_{Z1} = I_{Z2} = ...I_{Zm} = -I_{\bar{Z}1} = ...I_X \quad \text{.....(10)}$$

Where R_X is an internal resistor of X terminal and it is a function of I_B

2.4 Fully Differential Second Generation Current Conveyor (FDCCII)

One of the standard techniques to extend the dynamic range of analog blocks is to use fully differential signal processing. In 2000 a new active element called Fully Differential current conveyor (FDCCII) was proposed [9]. It can extend the dynamic range over one order of magnitude through the cancellation of even harmonics, as well as the suppression of all undesirable common mode signals.

The FDCC is an eight-terminal analog building block shown symbolically as below

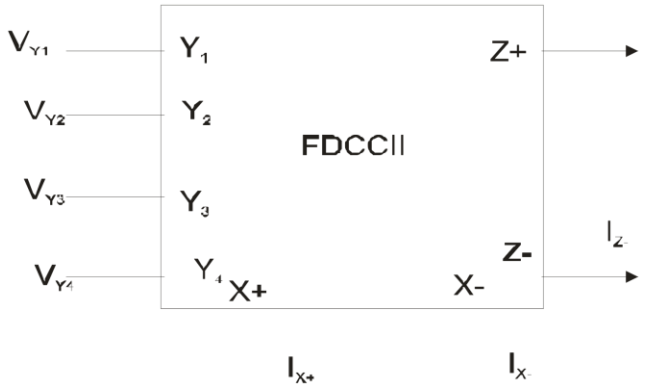

Fig8: FDCCII Block Diagram

The describing equation of FDCCII is given below

$$\begin{bmatrix} V_{X+} \\ V_{X-} \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 & -1 & 1 & 0 \\ 0 & 0 & -1 & 1 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{X+} \\ I_{X-} \\ V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ V_{Y4} \end{bmatrix} \quad \text{.....(11)}$$

It is the point to be noticed that V_{X+}=-V_{X-} if V_{Y3}=V_{Y4}=0

2.5 Differential Difference Current Conveyor(DDCC):

The DDCC [10] is a versatile building block for implementing differential and floating input circuits. Furthermore, the other current conveyors such as CCI, CCII, CCIII, and DVCC can be easily implemented by using DDCC.

The DDCC is a six-port building block as shown below

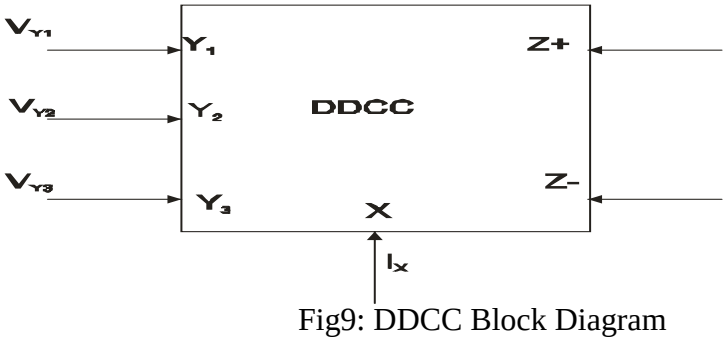

Fig9: DDCC Block Diagram

It has three voltage input terminals: Y_1, Y_2 and Y_3,which have high input impedance. Terminal X is a low impedance current input terminal. There are two high impedance current output terminals: Z_1 and Z_2

. The input output characteristics of the DDCC is defined as

$$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ \vdots V_{Z+} \\ V_{Z-} \end{bmatrix} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (12)$$

$$I_{Y1} = I_{Y2} = I_{Y3} = 0, V_X = V_{Y1} - V_{Y2} + V_{Y3}, I_Z = \pm I_X \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (13)$$

Where the plus and minus sign indicate whether the conveyor is configured as an inverting or non-inverting circuit termed DDCC- or DDCC+. The DDCC is very flexible in implementing floating input circuits and impedance conversion circuits.

2.6 Operational Trans-conductance Amplifier (OTA)

(CA3080A)

An OTA is a voltage controlled current source, more specifically the term 'operational' comes from the fact that it takes the difference of two voltages as the input for the current conversion. The ideal transfer characteristic is therefore

$$I_o = g_m(V_+ - V_-), \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (20)$$

Where V_+ and V_- are voltages on non-inverting and inverting input terminal of OTA. The block-diagram of OTA is shown in figure10

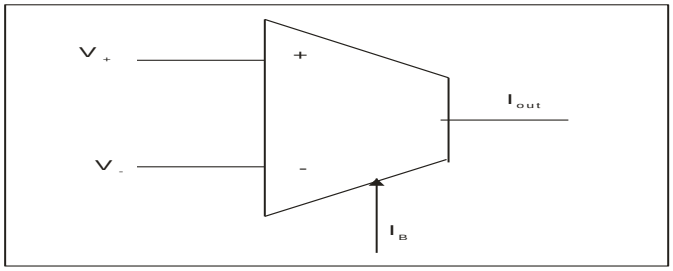

Fig10: OTA Block-Diagram

The trans-conductance is taken such as bellow

$$g_m = \sqrt[2]{(\mu_n C_{ox} \frac{W}{L} I_b)} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (21)$$

$$g_m = \frac{I_C}{2V_T} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (22)$$

Whereμ_n,C_{ox}, W/L and I_b are the electron mobility of NMOS, gate oxide capacitance per unit area, transistor aspect ratio and bias current of the OTA, respectively. In above equation, it can observe that the trans-conductance g_m is adjustable by a supplied bias current I_b.Characteristics of ideal OTA Input impedance (Z_{in}) =∞, Output Impedance (Z_0) =∞, Bandwidth = ∞ . .

2.7 Operational Trans-resistance Amplifier (OTRA)

The Operational Trans-resistance Amplifier [11] is a three terminal analog building block with a describing matrix in the form:

$$\begin{bmatrix} V_+ \\ V_- \\ V_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{bmatrix} \begin{bmatrix} I_+ \\ I_- \\ I_o \end{bmatrix} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (23)$$

Both the input and output terminals are characterized by low impedance, thereby eliminating response limitations incurred by capacitive time constants. The input terminals are virtually grounded leading to circuits that are insensitive to the stray capacitances.[12]. Current mode circuits using the OTRA as the active element suffer from using a large number of active elements [12]. [11] Implements voltage-mode signal processing operations using the OTRA that benefits from the current processing capabilities at the input terminals, thus reducing the number of OTRAs and keeping compatibility with the existing signal processing circuits.

OTRA is commercially available from several manufacturers under the name current differencing or Norton Amplifier.

2.8 Current Feedback Amplifier(CFA)

Among the various current-mode active building blocks, the current feedback operational amplifier (CFOA) is a very important device.CFA was developed to improve the finite gain-bandwidth product of the conventional voltage feedback amplifier. It can provide not only a constant bandwidth independent of closed loop gain but also a high slew rate capability. Usage of CFA as a basic building block in active filter design is highly

beneficial on account of these factors. The applications and advantages in realizing active filter transfer functions using current feedback amplifiers have received great attention because the amplifier enjoys the features of constant bandwidth independent of closed-loop gain and high slew rate, besides having low output impedance. The two main features of the CFA are improved slew rate and decoupling of closed loop of bandwidth and gain for low to medium values of gain [13, 15]. Thus, it is advantageous to use CFA as a basic building block in the accomplishment of various analog signal processing tasks.

CFA is an operational trans-impedance amplifier and is internally a CCII+ followed by a voltage follower. Presently the CFA is commercially available as IC AD844 [16, 17]]. It can be employed to realize filters, amplifiers, oscillators, inductors and simulators etc. [17].Although the CFA has better performance in case of slew rate and bandwidth there are some limitations too. These are input offset voltage, input offset current, common mode input range, common mode rejection ratio, power supply rejection ratio and open loop gain. VFAs are generally used for precision and general purpose applications while CFAs are used in high frequency applications.

Conventionally, the electrical characteristics for applications of the CFAs cannot be adjusted by electronic methods, which this means that they cannot be controlled by currents and/or voltages. Although, they can be achieved by passive element adjustments, the electronic control method is being more popular more than those by passive elements (i.e. resistors and capacitors) due to it can be easily adapted to automatic or microcontroller-based controls. In addition, the CFA cannot be controlled by the parasitic resistance at current input port so when it is used in a circuit, it must unavoidably require some external passive components, especially the resistors. This makes it not appropriate for IC implementation due to occupying more chip area, high power dissipation and cannot be electronic controllable. If it is employed for an off-the-shelf design, the circuit description is composed of a large number of external passive elements. Thus, a modified-version CFA whose parasitic resistance at current input port can be controlled by an input bias current, called current controlled current feedback amplifier (CC-CFA***),*** was proposed by Siripruchyanun, Chanapromma, Silapan, and Jaikla [18]. To reduce offset phenomenon, a BiCMOS technology was used for realizing

the proposed element. In addition, the voltage follower was also developed to reduce the offset output current and voltage. The CFA properties can be shown in the following equation

$$\begin{bmatrix} I_y \\ V_X \\ I_Z \\ V_w \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} I_x \\ V_y \\ V_z \\ V_w \end{bmatrix} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (14)$$

The symbol and the equivalent circuit of the CFA are illustrated in Fig. **11** (a) and (b), respectively. A circuit implementation of CFA can be achieved by using second-generation current conveyor (CCII) as input stage, followed by a buffered amplifier

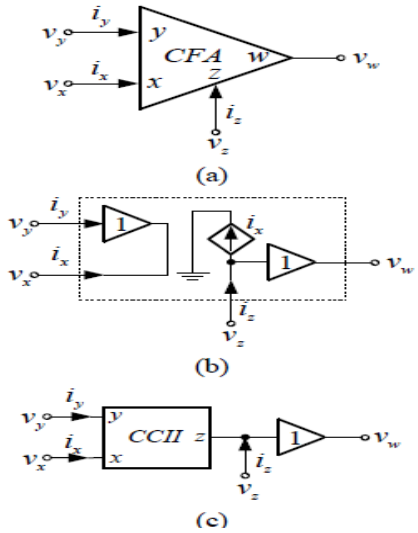

Figure11: CFA (a) Symbol (b) Equivalent circuit (c) Element implementation

Basic Concept of CC-CFA

CC-CFA properties are similar to the conventional CFA, except that the CC-CFA has finite input resistance *Rx* at the *x* input terminal. This parasitic resistance can be controlled by the bias current I_B as shown in the following equation

$$\begin{bmatrix} I_y \\ V_X \\ I_Z \\ V_w \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ R_x & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} I_x \\ V_y \\ V_z \\ V_w \end{bmatrix} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (15)$$

Where, $R_x = \frac{V_T}{2I_B}$

V_T is the thermal voltage, which is 26mV at room temperature.

The symbol and equivalent circuit of the CC-CFA are illustrated in Fig. **12**(a) and (b) respectively. In similar, we can realize the CC-CFA by using second-generation current controlled current conveyor (CCCII) as input stage, followed by a buffered amplifier as illustrated in Fig. **2**(viii).(c)

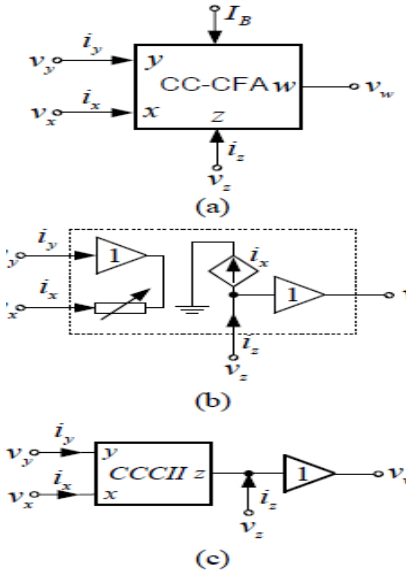

Figure 12: CC-CFA (a) Symbol (b) Equivalent circuit (c) Element implementation

2.9 Current Differencing Buffered Amplifier (CDBA)

Current differencing buffered amplifier (CDBA) was introduced by Acar and Ozoguz to provide further possibilities in the circuit synthesis and to simplify the implementation [19, 20]. The CDBA can offer such as high-slew rate, wide bandwidth and simple implementation for internally grounded input terminals [21]. Since the CDBA can be considered as a collection of current and voltage-mode unity gain cells, it has large dynamic range and quite wide bandwidth similar to its current-mode counterparts such as, current feedback operational amplifiers (CFAs) and second generation current conveyors (CCIIs). Many applications based on CDBA were reported in the literature. Many applications of CDBA have demonstrated that the CDBA is a versatile active building block for voltage-mode and current-mode signal processing applications.

Circuit Description of CDBA

CDBA is a multi- terminal active component with two inputs and two outputs. It is derived from current feedback amplifier (CFA) which is commercially available as AD844.The circuit symbol and equivalent of CDBA are shown in fig13

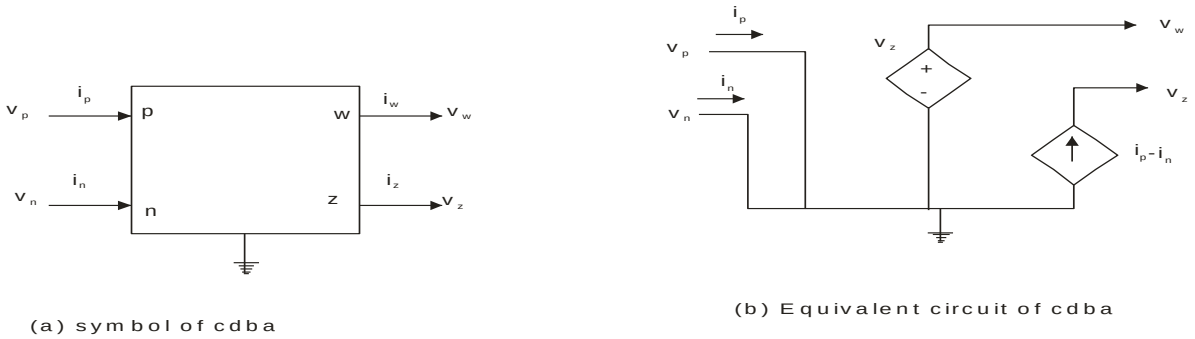

Fig13: Symbol & Equivalent Circuit of CDBA

In the circuit symbol shown in fig13 p and n are input terminals and w and z are output terminals. The equivalent circuit of CDBA involves dependent voltage and current sources. The terminal characteristics of CDBA can be modeled as follows

$$\begin{bmatrix} i_z \\ v_w \\ v_p \\ v_n \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 & -1 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_z \\ i_w \\ i_p \\ i_n \end{bmatrix} \quad \text{.....(16)}$$

According to the above model current through z-terminal follows the difference of the currents through p-terminal and n-terminal, and hence we name z-terminal as current output. We also name p-terminal as positive (non-inverting) input and n-terminal as negative (inverting) input. Moreover the voltage of w-terminal follows the voltage of z-terminal. Hence we name w-terminal as voltage output.

Fig.14 shows the implementation of CDBA using Current Feedback Amplifiers.

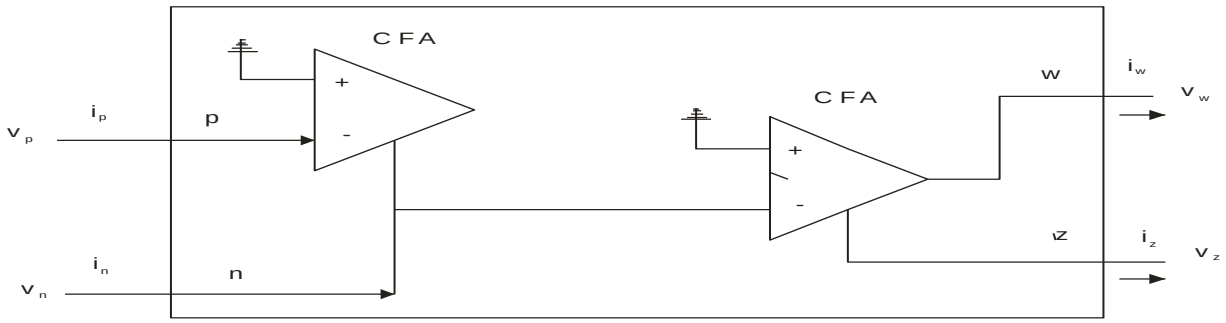

Fig14 CDBA using CFAs

. CDBA contains the so-called CDU (Current Differencing Unit) and the voltage unity-gain buffer. Basically, CDU is a current conveyor of the MDCC type: It has two low-impedance terminals, *p* and *n*. The difference of currents $I_P$and I_N flows out of the *z* terminal and the corresponding voltage drop on the external impedance is copied by the buffer to the *w* output. That is why the additional impedances are necessary for implementing the feedbacks from the voltage output to the current inputs. It is inconvenient from the point of view of simplicity and low power consumption. Another drawback is the impossibility of direct electronic control of circuit parameters such as that for the OTA-based applications. This problem is solved via two different approaches, the CC-CDBA (Current Controlled CDBA) and DC-CDBA (Digitally Controlled CDBA)

2.9.1 Current Controlled CDBA , CC-CDBA

CDBA offers advantage of high impedance current output as well as a buffered voltage output. The finite parasitic resistance at the two input ports of the CDBA (P and N) can be used as an advantage if made controllable. In 2003 Maheshwari and Khan proposed the current controlled CDBA [22], in which the parasitic resistances are current-controlled using mixed trans-linear input loops and current mirrors.

Already discussed CDBA is characterized by the following port relationship

$$V_P = V_N = 0, \quad I_Z = I_P - I_N, \quad V_W = V_Z \qquad \ldots\ldots\ldots\ldots (17)$$

Here the two input terminals (P and N) offer a finite parasitic resistance. These parasitic resistances can be current-controlled in a CCCDBA whose symbol is shown in Figure15

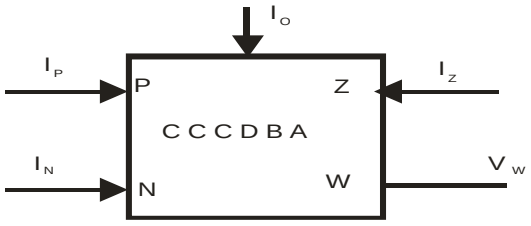

Fig15: CC-CDBA

The circuit implementation of Figure 15 consists of mixed trans-linear loops [23].

2.9.2 Digitally Controlled CDBA, DC-CDBA

In 2008 a low voltage digitally controlled CDBA, DC-CDBA, realized by interconnecting a current differencing circuit, a current division network (CDN), and a unity-gain voltage amplifier was proposed[24]. The novel CDN circuit was also proposed in order to provide the digital control of the current gain of the DC-CDBA.

Circuit Descriptions

The DC-CDBA is a versatile analog building block, described symbolically as shown in Fig.16 and mathematically by the following matrix equation.

$$\begin{bmatrix} I_z \\ V_w \\ V_p \\ V_n \end{bmatrix} = \begin{bmatrix} 0 & 0 & \alpha & -\alpha \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_z \\ i_w \\ i_p \\ i_n \end{bmatrix} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (18)$$

Where α is the current gain that is controlled digitally. According to eq. (18), this device consists of three stages as shown in Fig. 16. The input stage is a current differencing circuit to provide the difference of the input currents (i_p and i_n) through the terminals *p* and *n* into the x-terminal current (i_x). The second stage is a CDN, which is based on the linear current division principle. At this stage, the current *ix* is copied to the z-terminal and is digitally controlled by the current gain parameter α. The last stage is simply a voltage buffer, since the voltage at the w-terminal follows the voltage of the z-terminal.

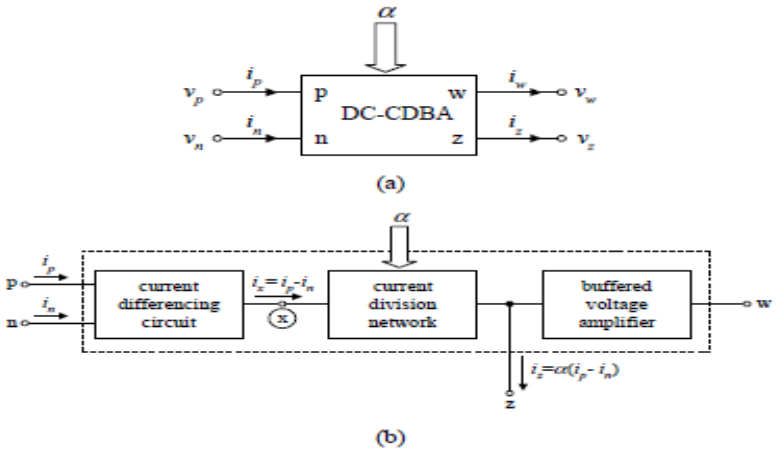

Fig 16 (a) Circuit Symbol (b) Block diagram of DC-CDBA

2.10 Current Differencing Trans-conductance Amplifier (CDTA)

A new active element with two current inputs and two kinds of current output, namely the Current- Differencing Trans-conductance Amplifier (CDTA) was proposed by Dalibor Biolek [25] and the element is a synthesis of the known CDBA (Current-Differencing Buffered Amplifier) and OTA (Operational Trans-conductance Amplifier) elements to facilitate the realization of current-mode analog filters.

A simple model of ideal CDTA element is in Fig.17 Analogously to the CDBA, it has difference current inputs *p* and *n*. The difference of these currents flows from terminal *z* into an outside load. The voltage across the *z* terminal is transferred by a trans-conductance *g* to a current that is taken out as a current pair to the *x* terminals. This last element part is the familiar trans-conductance operational amplifier (OTA). In general, the trans-conductance is controllable electronically through an auxiliary port that is not shown in Fig. 17

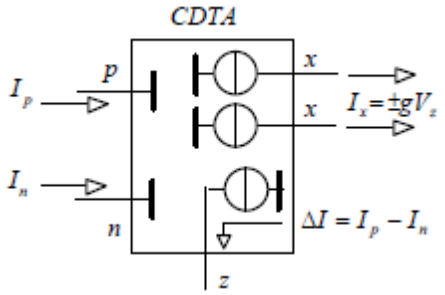

Fig 17: Behavioral model of CDTA

The pair of output currents from the *x* terminals, shown in Fig.17 may have three combinations of directions:

1. Both currents can flow out.
2. The currents have different directions.
3. Both currents flow inside the CDTA element.

Accordingly we can mark them as CDTA++, CDTA+-, and CDTA-- elements. It is suitable to mark the current directions in the circuit symbol by the signs + (outside) and – (inside) as shown in Fig.18

The symbol of CDTA is in Fig.18 (a**)** Also in Fig.18 (b) is given a possible implementation of CDTA using the familiar CCII+ and OTA components.

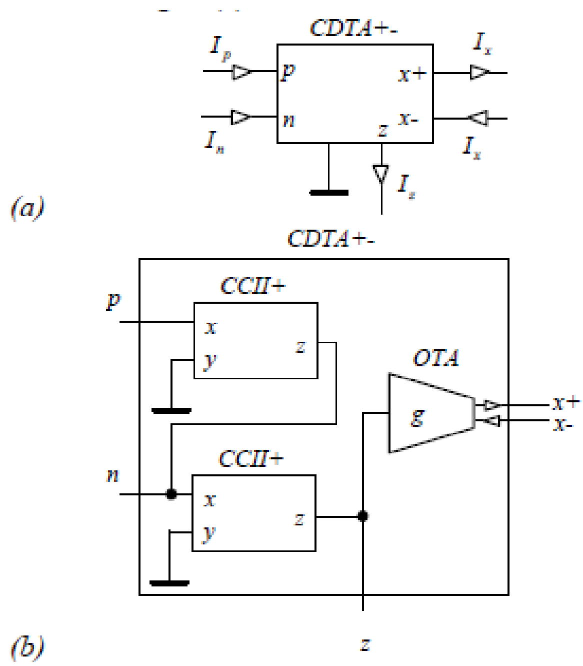

Figure18: (a) Symbol of the CDTA element, (b) its implementation by current conveyors and by OTA with double current output.

Marking the voltages of *p*, *n*, *x*, and *z* terminals in Fig.18 (a) with symbols, and

, then for the CDTA+- element the following equations are true:

$$\begin{bmatrix} I_z \\ I_{x+} \\ I_{x-} \\ V_P \\ V_n \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 1 & -1 \\ g & 0 & 0 & 0 & 0 \\ -g & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_z \\ V_{x+} \\ V_{x-} \\ I_P \\ I_n \end{bmatrix} \qquad (18)$$

The CDTA element proposed by Dalibor Biolek enables an easy implementation of multiple-input current integrators. That is why it seems to be a promising building block of current-mode filters. Compared with CDBA, the CDTA element is less universal in the sense that – to avoid all additional current-to-voltage-to-current conversions- it does not enable setting the summing coefficients simply by means of outside *R* and *C* components. The voltage mode prototypes provide more design freedom. The CDTA is a universal active building block for implementing many signal processing functions including sinusoidal oscillators

2.11 ZC-CDTA

The modified CDTA was proposed by D. Biolek, A.U¨. Keskin, V. Biolkova [26.] Its schematic symbol is shown in fig19 .It has a pair of low-impedance current inputs p and n, and an auxiliary terminal z, whose outgoing current is the difference of input currents. In addition to the CDTA, a copy of the z-terminal current is also available at the ZC high-impedance terminal. Therefore this modified CDTA element is called **ZC-CDTA** (Z Copy CDTA).

Similar to the CDTA, this element provides a pair of x-terminals whose currents are equal in magnitude, but flow in opposite directions, and the product of trans-conductance (gm) and voltage at the z-terminal determines their magnitudes. The circuit equations of the ZC-CDTA are as follows

$$\begin{bmatrix} V_p \\ V_n \\ I_z \\ I_{zc} \\ I_{x+} \\ I_{x-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & g_m & 0 & 0 & 0 \\ 0 & 0 & -g_m & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ V_z \\ V_{zc} \\ V_{x+} \\ V_{x-} \end{bmatrix} \quad \text{.....(19)}$$

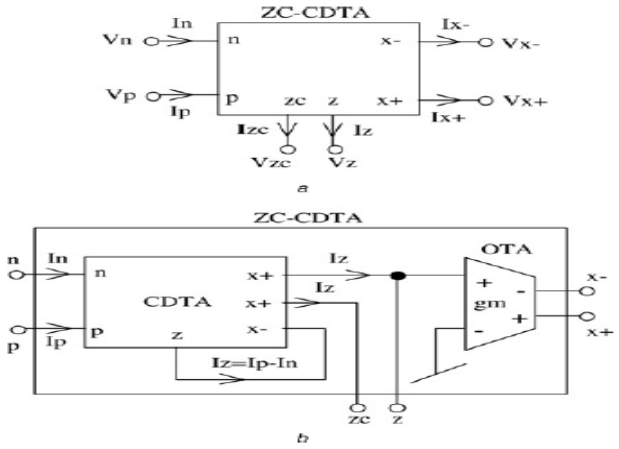

Fig 19: (a) Symbol of ZC-CDTA (b) ZC-CDTA implementation based on CDTA and OTA

2.12 Current Conveyor Trans-conductance Amplifier (CCTA)

The CCTA (Current Conveyor Trans-conductance Amplifier) is the newly designed type of analog block proposed by Roman Prokop, Vladislav Musil in 2005**,** [27] that was inspired by trans-impedance amplifier (current feedback amplifier which is built from CCII conveyor followed by voltage buffer). CCTA is designed for usage mostly in current mode circuits but it is also good choice in case of hybrid (voltage-current) circuits. Behavioral model of the CCTA is shown in Fig.20 The CCTA consists from two basic blocks. The input is represented by the current conveyor CCIII that is followed by double output trans-conductance amplifier (OTA).

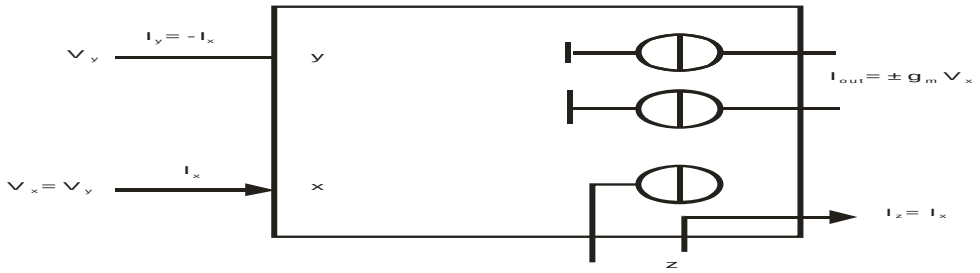

Figure 20: Behavioral model of CCTA,

The input behavior is mostly given by properties of the CCIII conveyor that is described below. Conveyor output current flows out of the CCTA terminal "z" into an outside load. The voltage across the z-terminal is converted through a trans-conductance gm into a two output currents with opposite polarity. The trans-conductance can be either fixed or given by external component or controlled electronically from an auxiliary terminal as well. The CCTA may be reasonably useful, for example, in current sensing applications. In fact, if a current, at a generic point into a network, has to be sensed, the current "probe" should be able to make flow a current with very low series impedance while the sensed current can be further processed (amplified, filtered etc.).The CCTA is brought in as the new convenient element for current mode signal processing, which should be very convenient for several applications, e.g. sensor output signals processing. CCTA is supposed for usage mostly in current mode circuits but it is also good choice in case of voltage mode and/or hybrid (voltage-current) circuits (e.g. V/I converters). This modern active device is a newly designed type of analog block that was inspired by trans-impedance amplifier (current feedback amplifier which is basically built from CCII).

2.13 Differential Voltage CCTA (DVCCTA)

It is well known that DVCC has some advantages, especially for applications demanding differential and floating inputs, over CCII or CCCII owing to two high input impedance terminals for DVCC compared to one high input impedance terminal for CCII or CCCII. However, DVCC does not have a powerful inbuilt tuning property in contrast to CCCII. Recently proposed active building block namely differential voltage current conveyor trans-conductance amplifier (DVCCTA) [28] has DVCC as input block and is followed by TA. The DVCCTA has all the good properties of CCTA or CCCCTA including the possibility of inbuilt tuning of the parameters of the signal processing circuits to be implemented and also all the versatile and special properties of DVCC such as easy implementation of differential and floating input circuits. However, the same may be implemented using separate DVCC and OTA analog building blocks, but it will be more convenient and useful, if DVCCTA is implemented in monolithic chip which will result in compact implementation of signal processing circuits and systems.

The DVCCTA is based on DVCC [8] and consists of differential amplifier as input, current mirrors and trans-conductance amplifier. The port relationships of the proposed DVCCTA as shown in Fig. 21 can be characterized by the following matrix:

$$\begin{bmatrix} I_{y1} \\ I_{y2} \\ V_x \\ I_{z+} \\ I_{z-} \\ I_{o-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & -g_m & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{y1} \\ V_{y2} \\ I_x \\ V_{z+} \\ V_{z-} \\ V_{o-} \end{bmatrix}$$

Where g_m is trans-conductance of the DVCCTA

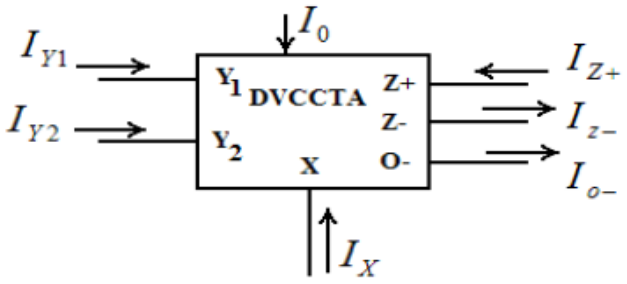

Fig .21: Circuit symbol of DVCCTA

2.14 Voltage Differencing Trans-conductance Amplifier (VDTA)

VDTA can be compared with CDTA, the previously introduced active element. In CDTA, differential input current (I_P,I_N) flows over the Z terminal. The voltage drop at the terminal Z is transferred to current at the terminal X by a trans-conductance gain. In VDTA, differential input voltage (V_{PN},V_{VN}) is transferred to current at the terminal Z by first trans-conductance gain and the voltage drop at the terminal Z is transferred to current at the terminals X+ and X- (negative of X+) by second trans-conductance gain. Both trans-conductance are electronically controllable by external bias currents. Compared to other active blocks discussed so far, the advantageous feature of VDTA is that this new element exhibits two different values of trans-conductance's so that several applications such as biquad filters, oscillator, inductance and FDNR (frequency dependent negative resistor) simulator can be realized with a single active block employing one or two capacitors. Another important feature, this block can be used easily at trans conductance mode applications owing to input terminals is voltage and output terminals is current.

Circuit Description

The circuit symbol of the proposed active element, VDTA, is shown in Fig.22 where V_P and V_N are input terminals and Z, X+ and X- are output terminals. All terminals exhibit high impedance values. Using standard notation, the terminals relationship of an ideal VDTA can be characterized by:

$$\begin{bmatrix} I_z \\ I_{x-} \\ I_{x-} \end{bmatrix} = \begin{bmatrix} g_{m1} & -g_{m1} & 0 \\ 0 & 0 & g_{m2} \\ 0 & 0 & -g_{m2} \end{bmatrix} \begin{bmatrix} V_{VP} \\ V_{VN} \\ V_Z \end{bmatrix}$$

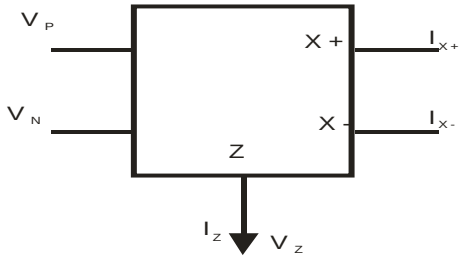

Fig 22:.The circuit symbol of VDTA

Consequently, the above describing-equations, the input stage and output stage can be simply implemented by floating current sources. According to input terminals, an output current at Z terminal is generated. The intermediate voltage of Z terminal is converted to output currents.

2.15 Current Follower Trans-conductance Amplifier (CFTA)

This new active element was introduced by Norbert Herencsar, Yaroslavl Koton, Kamil Vrba, and Ibo Lattenberg in 2008[29]. The element is a combination of the Current Follower (CF) and the Balanced Output Trans-conductance Amplifier (BOTA). The ideal behavioral model of the CFTA element is shown in Fig. 23 The element is a combination of the Current Follower (CF), which is the input part of the designed element, and the Balanced Output Trans-conductance Amplifier (BOTA) [30-31], which forms the output part of the element. The schematic symbol of the CFTA element is shown in Fig. 23**(**b)

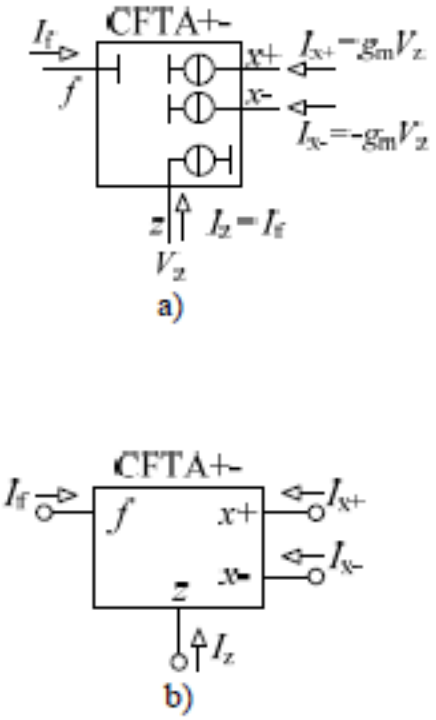

Fig 23: (a) Behavioral model of CFTA+ element (b) Schematic symbol of CFTA+

The element has been defined in compliance with network convention i.e. all currents are flowing into the circuit. The element has one low impedance current input *f*. Current from the terminal *f* is transferred by the Current Follower to auxiliary terminal *z*. The voltage

V_Z on this terminal is transformed into current using the trans-conductanceg_m, which flows into output terminals *x*+ and *x*-.

Relations between the individual terminals of the CFTA+- element can be described in matrix form as follows:

2.16 Conclusion

In the present chapter we have discussed the port relationships and specific features of important active building blocks introduced during the last two decades. It is observed that most of the derivative blocks have added to the flexibility of the basic active building blocks.

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CHAPTER-3 →

VDBA & ITS CMOS REALIZATION

3.1 Introduction

In the previous chapter the port relationships and the general features of some important voltage-mode and current-mode active building blocks was presented. In the present chapter we discuss the Voltage Differencing Buffered Amplifier (VDBA), its circuit implementation and characterization

In [1], Biolek, Senani, Biolkova and Kolka have proposed a variety of current mode active building blocks. The circuit principle of Voltage Differencing Buffered Amplifier (VDBA) has been proposed therein. It is proposed as an alternative to the existing CDBA (Current Differencing Buffered Amplifier). The differences between VDBA and CDBA are that the VDBA inputs are voltages whereas for the CDBA, inputs are currents.

The proposed schematic symbol of the VDBA is shown below

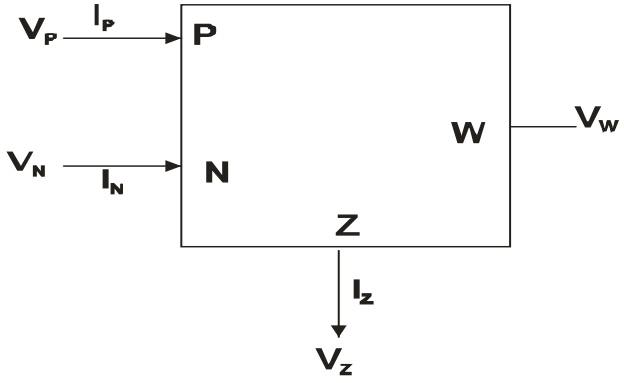


Fig24: VDBA Block

In the figure shown above P and N are input terminals while Z and W are output terminals. Current entering into both the input terminals is zero thus VDBA block has high impedance input terminals. Differential input voltage $(V_P - V_N)$ is transferred into current I_Z at Z terminal by a trans-conductance gain g_m.

3.2 The VDBA Model

The VDBA model can also be described in the form of a matrix as given below

$$\begin{bmatrix} I_p \\ I_N \\ I_Z \\ V_W \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ g_m & -g_m & 0 \\ 0 & 0 & \alpha \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \end{bmatrix}$$

I_P=Current entering into input terminal P, which is zero. Thus input terminal P is a high impedance terminal

I_N=Current entering into input terminal N, which is zero. Thus input terminal N is a high impedance terminal

I_Z=$g_m(V_P\text{-}V_N)$. This is a high impedance current output terminal

V_P=Input voltage applied at P terminal.

V_N=Input voltage applied at N terminal

V_Z=When the current through Z terminal is passed through a passive element than a voltage appears at Z terminal.

V_W=The voltage at the output terminal W

g_m=This is called transconductane. Transconductane is defined as the ratio of output current to input voltage voltage. This transconductane is controlled by an additional biasing current or biasing voltage which is not shown in the schematic symbol of the VDBA.

α: This is called voltage ratio of the VDBA. The voltage at Z terminal is transferred to voltage at W terminal in a different impedance level by this voltage ratio. The relationship between voltage at Z terminal and voltage at W terminal is given in terms of this voltage ratio α.

V_W=αV_Z. The value of α is 1 ideally but it is found to be less than 1 practically. The difference is expressed in terms of voltage tracking error.

$\alpha = 1 - \varepsilon_v$Here ε_v is the voltage tracking error. The magnitude of tracking error is much less than unity.

3.3 CMOS Implementation of VDBA

A CMOS implementation of VDBA proposed in [1], shown in figure25 was given in [2].

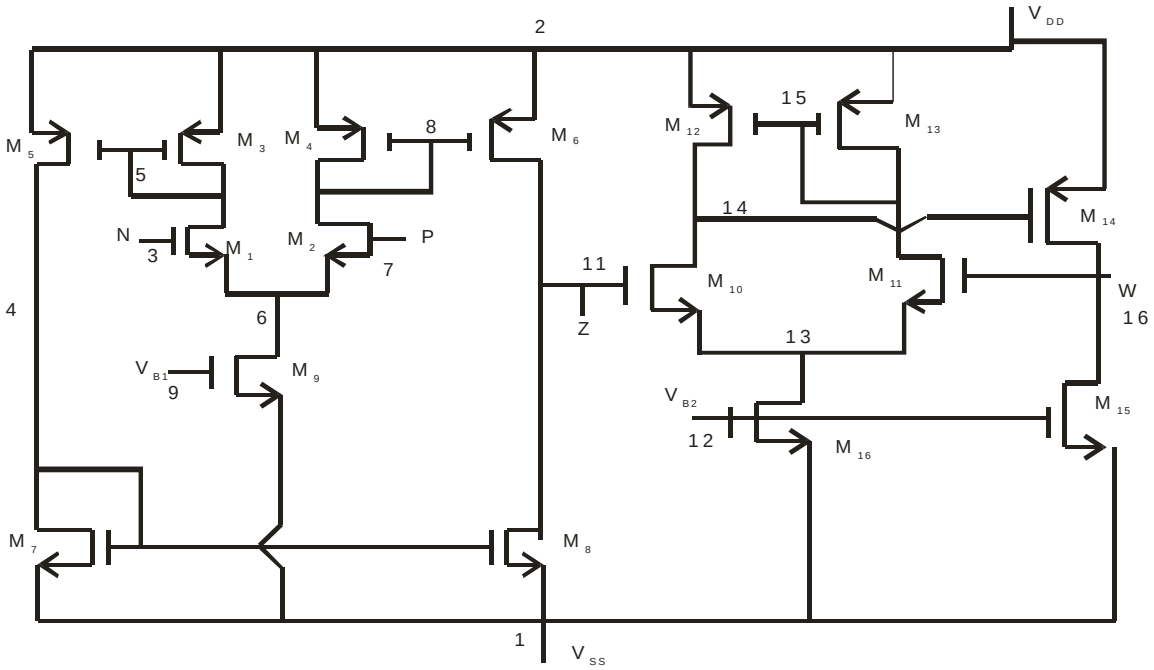


Fig25: CMOS Implementation of VDBA

Fig25 shows the complete schematic of the VDBA circuit. This schematic is based on the use of the OTA circuit (M_{1}_M_{9}) [3] and the voltage buffer circuit (M_{10}-M_{16}) [4].

The input stage of the VDBA is composed of the differential input OTA. The voltage buffer is connected to the OTA current output. The operational trans-conductance amplifier (OTA) is an amplifier whose differential input voltage produces an output current is a voltage controlled current source (VCCS). There is usually an additional input for current to control the amplifiers' trans-conductance. The OTA is similar to a standard operational amplifier in that it has a high impedance differential input stage and is suitable for negative feedback. A buffer amplifier (sometimes, simply called a buffer) is one that provides electrical impedance transformation from one circuit to another.

3.4 Simulation using PSPICE

Consider the circuit shown in fig25, here; we have assigned a number to each node for PSpice programming purposes. Now we see that we can easily separate the circuit into two blocks: OTA and Buffer.

Table No.1:

Transistors Aspect Ratios for the VDBA

Transistors	W(µm)	L(µm)
M_1-M_4,M_{10},M_{11},M_{15},M_{16}	7	0.35
M_5,M_6	21	0.7
M_7,M_8	7	0.7
M_9	3.5	0.7
M_{12}-M_{14}	14	0.35

Power Supply Connection

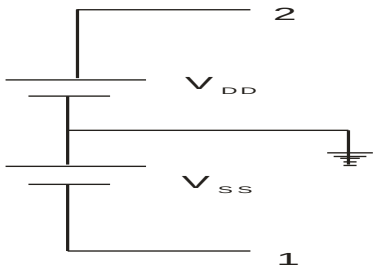


Fig26: Power Supply Connection Diagram

V_{DD}=-V_{SS}

Model Parameters: For all of the PSpice simulations explained in this report we have used the 0.35UM TSMC CMOS parameters which are available in appendix.

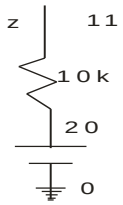
Dummy Source: In Pspice programming, a dummy voltage source (0V) is used to measure the current through a terminal**.** In all our simulations explained in this report we have used V_x as a dummy voltage source. Current through the dummy source is indicated by I (V_x)

3.4.1 Simulation of OTA stage only

Consider the OTA stage of the nodal diagram shown in fig25

V_P=V_{in}, V_N=0, I_Z= g_m(V_P-V_N) =$g_m V_{in}$.

The value of $g_m$depends upon the bias voltage V_{B1}applied at node 9. Now we apply 1V input voltage at P terminal and terminal N is grounded. We take initially the bias voltage V_{B1}=-0.44V. A dummy voltage source and a resistor of 10kΩ is connected as shown below



Observation1:

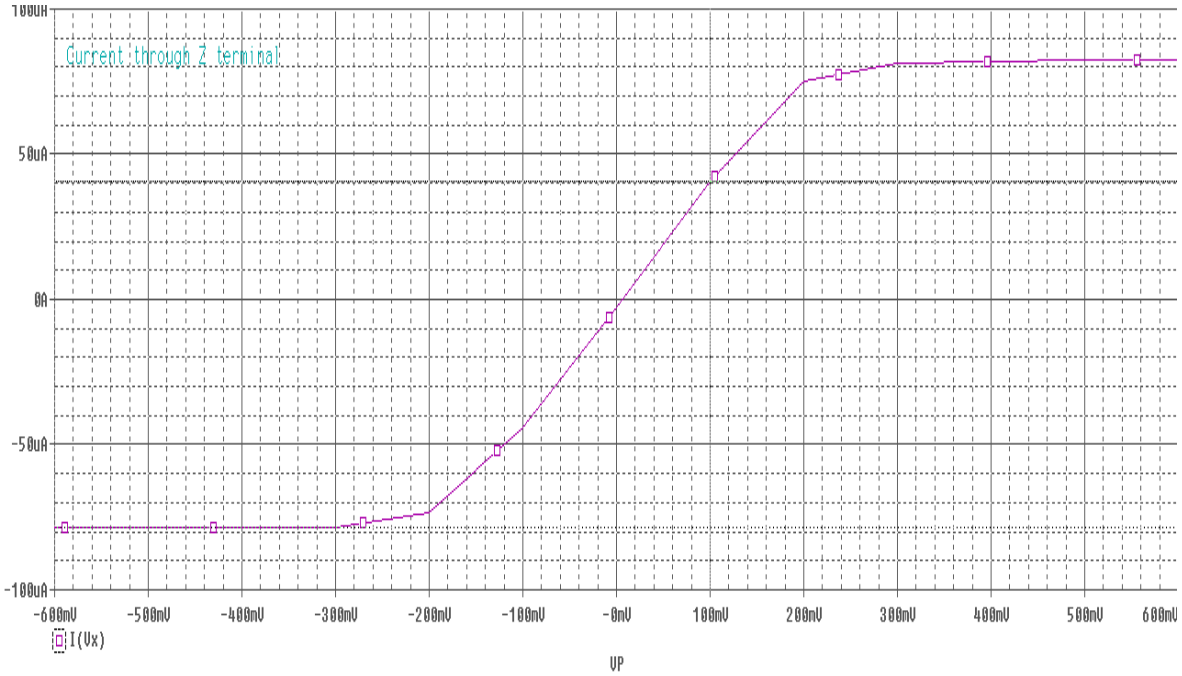


Fig27: Variation of $I_Z$with input voltage at P terminal

From the simulation result obtained in fig27 we see that the current through the Z terminal has a linear relationship with the input voltage (between the ranges -0.2V to 0.2V). Beyond this limit of input voltage the output current saturates. Now by varying the input bias voltage we can vary the trans-conductanceg_m.

The values of $g_m$obtained for different values of $V_{B1}$are shown in table no.-2

TABLE No-2

Variation of Trans-conductance g_m with bias voltage V_{B1}

V_{B1}(V)	$g_m(\frac{mA}{V})$	V_{B1}(V)	$g_m(\frac{mA}{V})$
-0.60	505.70	-0.40	675.32
-0.58	524.26	-0.38	690.75
-0.52	577.47	-0.36	705.98
-0.48	611.20	-0.34	721.00
-0.44	643.7	-0.30	783.23

From the table shown above we observe that the value of trans-conductance is totally controlled by the bias voltage. If we increase the bias voltage then trans-conductance starts reducing up to a certain limit below which it comes into saturation. If we decrease the bias voltage then trans-conductance starts increasing up to a certain limit and then becomes saturated.

Use of Bias Current instead of Bias Voltage: We have observed the effect of bias voltage on trans-conductance. It is not necessary to use voltage for biasing; we can also use biasing current for varying trans-conductance. We measured the current flowing between the nodes 1 and 6 in the figure 3(iv). We got it around 200µA. So we place a current source of 200µA (known as bias current) in place of M_9 as shown below

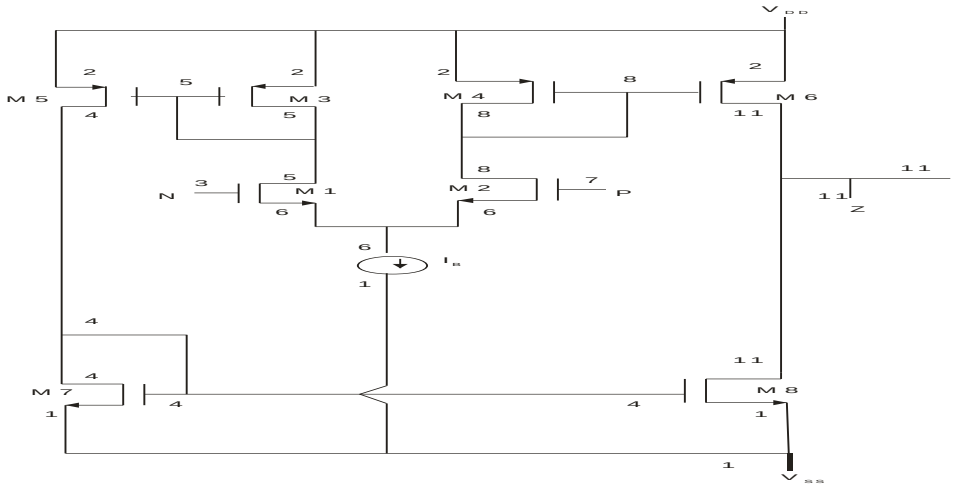


Fig28: Use of Bias Current instead of Bias Voltage

TABLE No.-3

Variation of Trans-conductance with Bias Current

I_B(µA)	$g_m(\frac{\mu A}{V})$	I_B(µA)	$g_m(\frac{\mu A}{V})$
170	518.23	220	583.70
180	532.32	240	606.69
190	545.88	260	628.88
200	558.94	280	649.96
210	575.15	300	669.18

3.4.2 Simulation of complete VDBA Block

If V_{DD}=-V_{SS}=1.75V, V_{B1}=-0.12V, V_{B2}=-0.14V

For above taken values of power supplies and bias voltages the value of trans-conductance comes to be around 521$\frac{\mu A}{V}$

Observation 2:

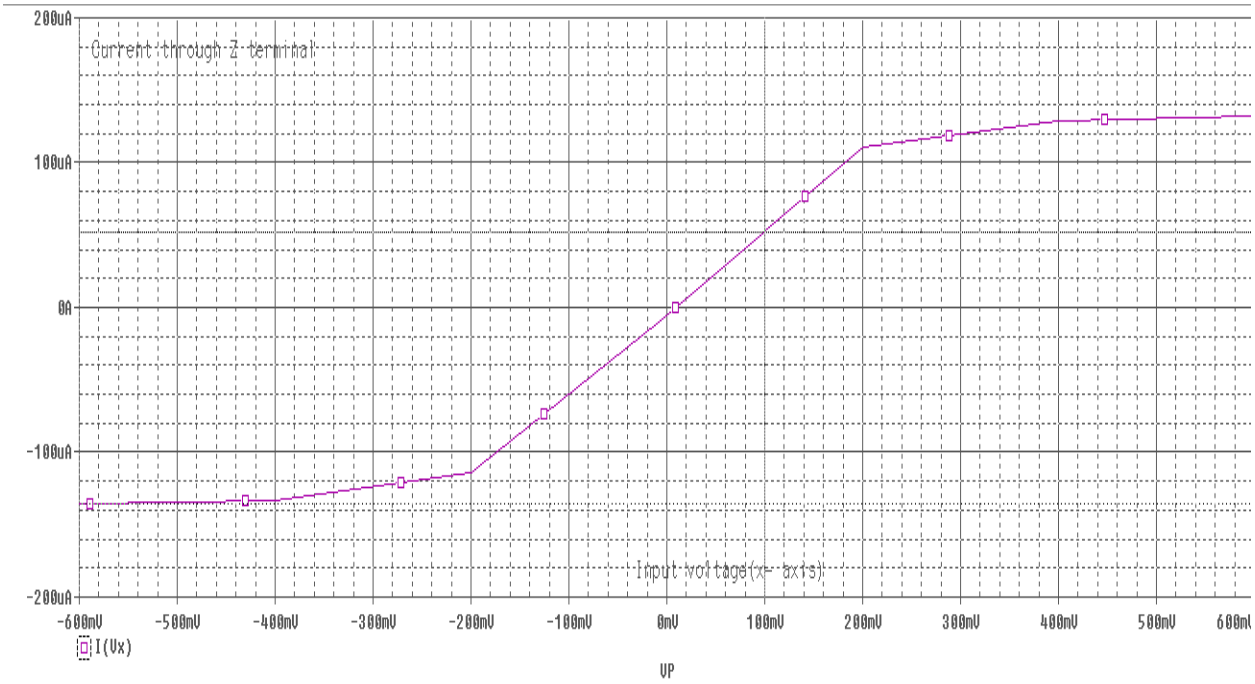


Fig 29: Variation of current through Z terminal with Voltage at P terminal

The above plot shows the variation of current through Z terminal against the Input voltage.

Now we find that if we make a table of values of trans-conductance for different values bias voltages or bias currents we find that the table is same as that obtained for OTA stage only. We now keep V_{B1}fix and vary V_{B2}only. The following table no.4 is obtained.

TABLE No.-4

Variation of g_m with V_{B2}

$V_{B2}(V)$	$g_m(\frac{\mu A}{V})$	$V_{B2}(V)$	$g_m(\frac{\mu A}{V})$
0.12	**520.82**	**0.20**	**520.82**
0.14	**520.82**	**0.22**	**520.82**
0.16	**520.82**	**0.24**	**520.82**
0.18	**520.82**	**0.28**	**520.82**

From the table no.4 we observe that bias voltage used in the Buffer stage of VDBA has no effect on the trans-conductance

3.4.3 Simulation of Buffer Stage

A buffer amplifier (sometimes simply called a buffer) is one that provides electrical impedance from one circuit to another. This buffer stage is the main difference between a VDBA and an OTA.

Now we have to verify the relationship between voltage at Z terminal and voltage at W terminal. The voltage at Z terminal is the voltage at node11 and voltage at W is the voltage at node 16.

V_W=αV_Z; α is the voltage ratio of VDBA and α=1-ε_v; Here ε_v is the voltage tracking error.

The value of α comes to be 0.868 for this particular observation. The voltage tracking error is 1-0.868=0.132

Observation 3:

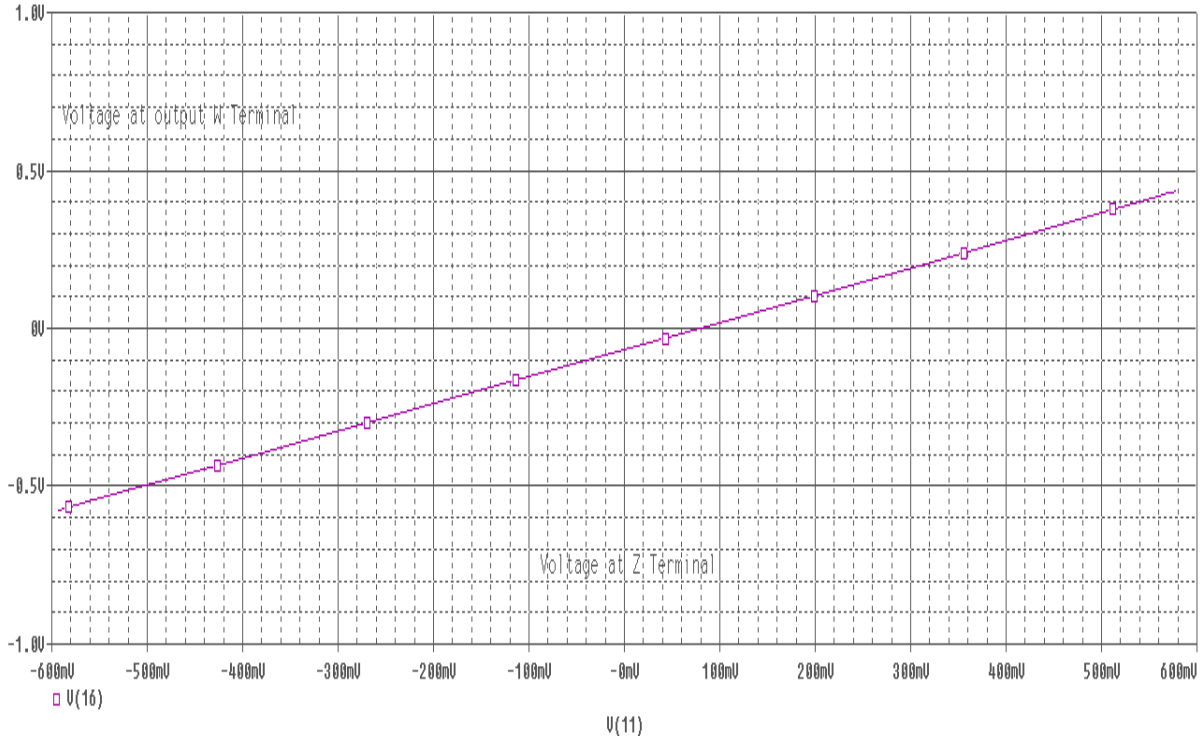


Fig 30: Variation of voltage at W terminal with voltage at Z terminal

Effect of V_{B1} and V_{B2} on α:

The value of α is independent of the biasing used in OTA stage. It depends on the biasing used in Buffer stage only**.** Thus α depends only onV_{B2}. It increases with increasing value of bias voltage V_{B2}

Parasitic Effect

In electrical networks, a **parasitic element** is a circuit element (resistance, inductance or capacitance) that is possessed by an electrical component but which it is not desirable for it to have for its intended purpose. For instance, a resistor is designed to possess resistance, but will also possess unwanted capacitance. The supply voltage $V_{DD} = -V_{SS} = 1.75V$ and $V_{B_1} = -0.44V, V_{B_2} = -0.9V$ .Simulation results show that this choice yields the trans-conductance value of $g_m = 653\frac{\mu A}{V}$ and parasitic impedance of $R_{zp} = 298k\Omega, C_{zp} = 0.42\,pF$ parasitic parallel and capacitances at Z terminal and parasitic series resistance of 12kΩ at W terminal respectively

3.5 Conclusion

The difference between VDBA and CDBA are that CDBA inputs are current while VDBA inputs are voltage. Besides, VDBA can be compared with Op-Amp. Both of them have the same properties such as high input and low output impedances. Differential input voltage is transferred to current at the terminal Z by trans-conductance gain and the voltage drop at the terminal Z is mirrored in different impedance region, that is, terminal W. The main difference between VDBA and a traditional voltage Op-Amp lies in the fact that the open loop gain of the Op-Amp is fixed, whereas in VDBA it can be controlled by controlling g_m and α, thus making electronic tenability of various signal processing circuits using VDBA possible. In the present chapter a CMOS implementation of VDBA proposed in [2] has been characterized in PSPICE. Parasitic impedance associated with device has been calculated. Furthermore; VDBA still enjoys features of trans-conductance such as value of trans-conductance can be adjusted electronically. Besides, difference between VDBA and OTA is that VDBA has low output impedance that is more suitable than voltage-mode circuit because loading effect is completely eliminated.

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CHAPTER-4

APPLICATIONS OF VDBA

4.1 Introduction

In the previous chapter we had presented a CMOS implementation of VDBA and its characterization in PSpice. In the present chapter we have used the CMOS implementation given in [1] to present some basic applications of VDBA given below

(i) Basic Inverting Amplifier
(ii) Basic Non Inverting Amplifier
(iii) A voltage Sumer Circuit
(iv) Integrator
(v) First Order Low Pass Filter
(vi) First Order High Pass Filter
(vii) Second Order Biquad Filters

The simplest application of VDBA is to build inverting and non inverting amplifiers. Both the amplifiers contain a single VDBA. A lossless as well as lossy integrator has also been explained. Both the integrators contain single VDBA along with a passive capacitor. Two voltage mode biquad filters proposed in [1] have also being explained. Both of these circuits contain two VDBAs, two or three passive components and have three-inputs single output. The first proposed biquad filter contains two VDBAs and two capacitors and generates all filter functions(low pass(LP), band pass(BP), high pass(HP), band stop(BS) and all pass(AP),but this topology needs inverting type input voltage signal for the employed AP filters. The second proposed biquad filter employs two VDBAs, two capacitors and a resistor and realizes the all filter functions without the use of inverting input terminals. Furthermore, quality factor can be adjusted with resistor as independent natural frequency..

4.2 Basic Inverting Amplifier

To build an inverting amplifier using VDBA, we consider the block showing inverting amplifier using OTA

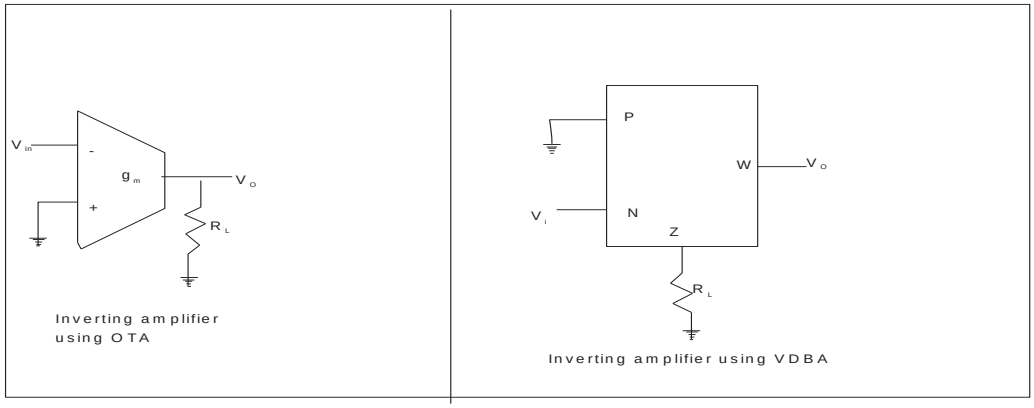


Fig31: Inverting amplifier using VDBA

The current through Z terminal of VDBA is given by

$$I_{Z=}g_m(V_P\text{-}V_N)=\text{-}g_mV_i \quad \text{..... (1)}$$

The voltage drop at the Z terminal

$$V_Z=I_ZR_L=\text{-}g_mR_LV_i \quad \text{..... (2)}$$

The output voltage is given by $V_O=V_W=\alpha V_Z=\text{-}g_m\alpha R_LV_i$ ..... (3)

4.2.1 Simulation Results

Consider the circuit shown in fig31; the following values have been used

$V_{DD}=-V_{SS}=1.5V$, $V_{B1}=-0.56, V_{B2}=-0.16V$, R=1KΩ

Terminal P is grounded and a 1V DC input voltage at N is sweep between -0.6V to 0.6V in the steps of 0.1V. The plot of current through Z terminal versus input voltage applied at N terminal is shown in fig32 and plot of voltage at W terminal versus voltage at Z terminal is shown in fig33. The values of trans-conductance $g_m=740\frac{\mu A}{V}$ and voltage ratio α=0.83. The transient response of the Inverting amplifier when a sinusoidal input of amplitude 0.5Vand frequency 50Hz is applied is shown in fig34. We observe that output is also sinusoidal with amplitude αg_mR times of input voltage.

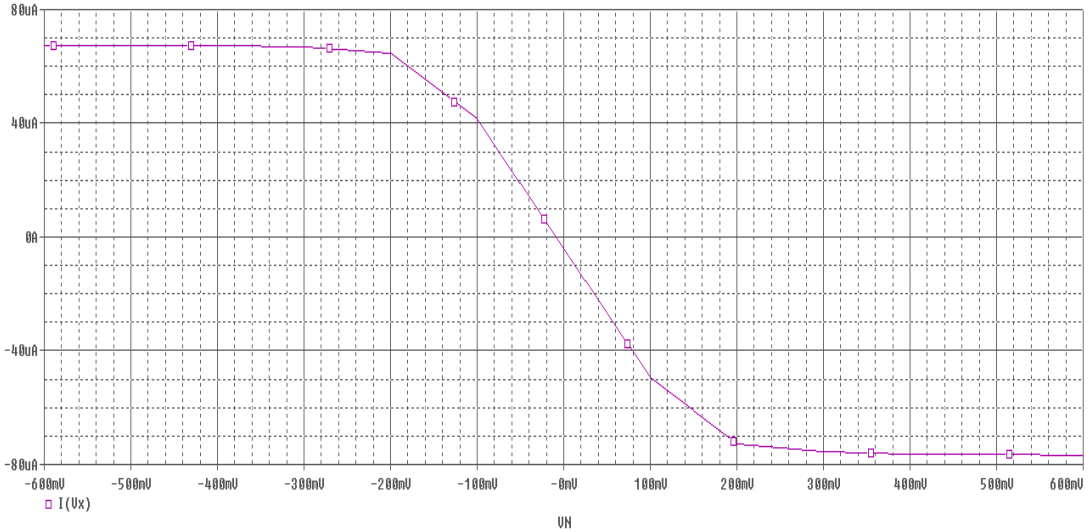


Fig32: Plot of current through Z terminal versus input voltage in Inverting amplifier

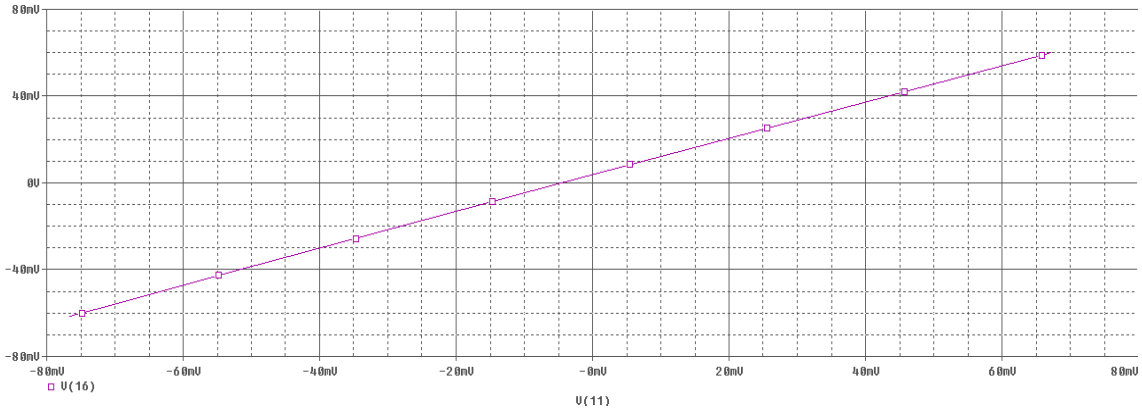


Fig33: Plot of voltage at W terminal versus voltage at Z terminal in Inverting amplifier

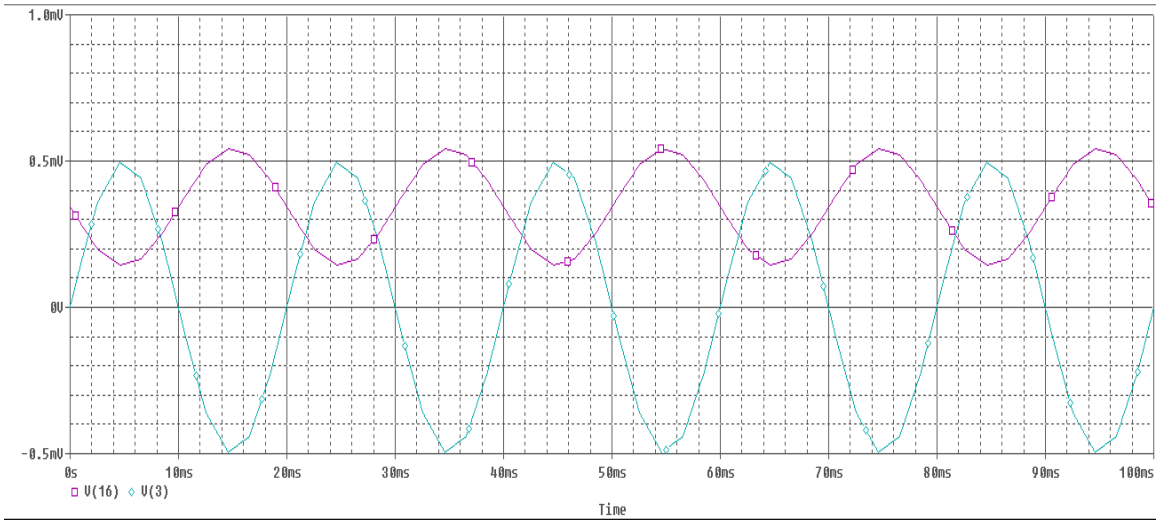


Fig34: Transient response of inverting amplifier

4.3 Basic Non- Inverting Amplifier using VDBA

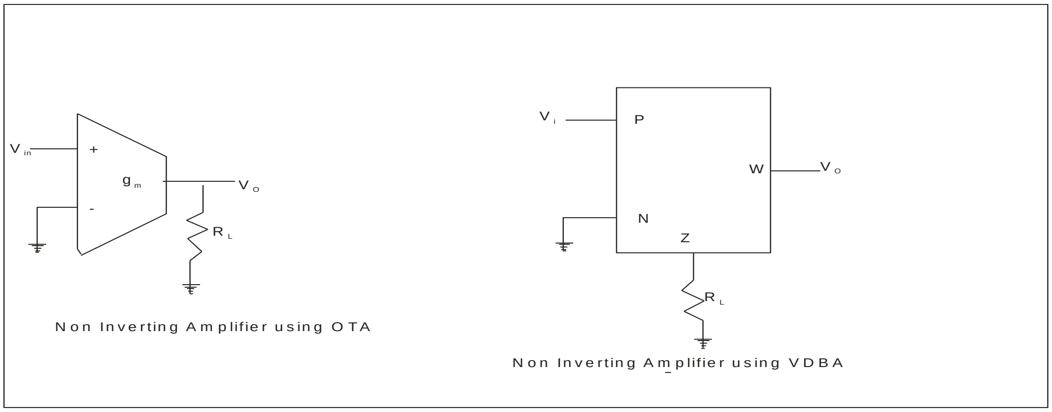


Fig35: Non-Inverting amplifier using VDBA

The current through Z terminal of VDBA is given by

$I_{Z}=g_m(V_P\text{-}V_N)= g_m V_i$ …………………………………………….. (4)

The voltage drop at the Z terminal

$V_Z=I_Z R_L=g_m R_L V_i$ ……………………………………………….. (5)

The output voltage is given by $V_O=V_W=\alpha V_Z=g_m \alpha R_L V_i$ ……………………… (6)

The output of non inverting configuration using VDBA is given by the equation

$V_O=\alpha g_m R_L V_i$

4.3.1 Simulation Results

Consider the circuit shown in fig35; the following values have been used

$V_{DD}=-V_{SS}=1.5V$, $V_{B1}=-0.56, V_{B2}=-0.16V$, R=1KΩ

Terminal N is grounded and a 1V DC input voltage at P is sweep between -0.6V to 0.6V in the steps of 0.1V. The plot of current through Z terminal versus input voltage applied at P terminal is shown in fig36 and plot of voltage at W terminal versus voltage at Z terminal is shown in fig37. The values of trans-conductance $g_m=740\frac{\mu A}{V}$ and voltage ratio α=0.83. The transient response of the Non- inverting amplifier when a sinusoidal input of amplitude 0.1Vand frequency 50Hz is applied is shown in fig38

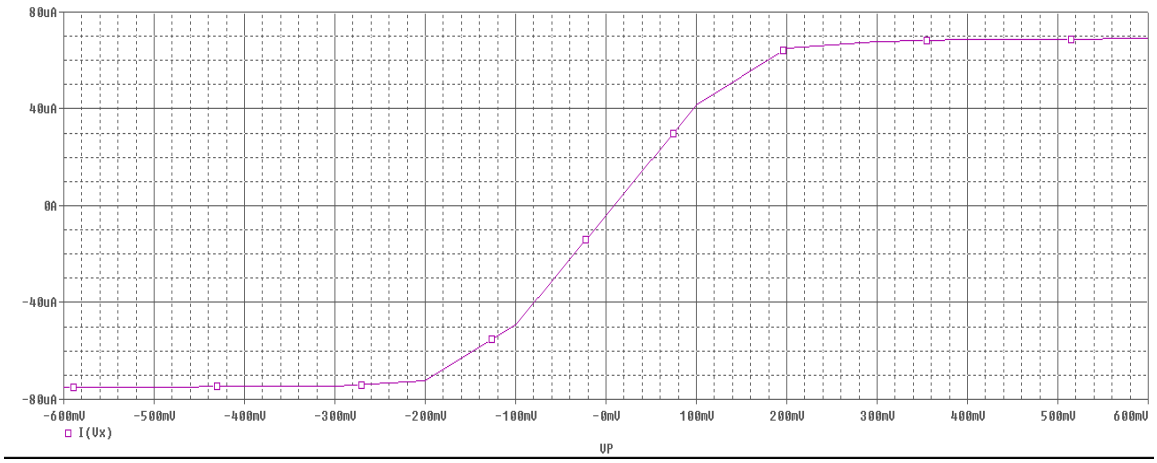


Fig36: Plot of current through Z terminal versus input voltage in Inverting amplifier

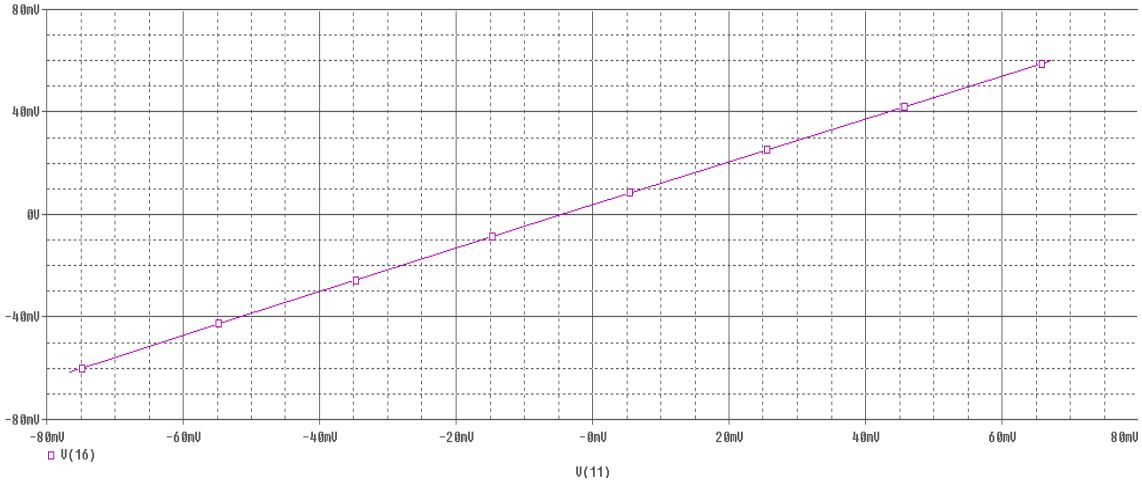


Fig37: Plot of voltage at W terminal versus voltage at Z terminal

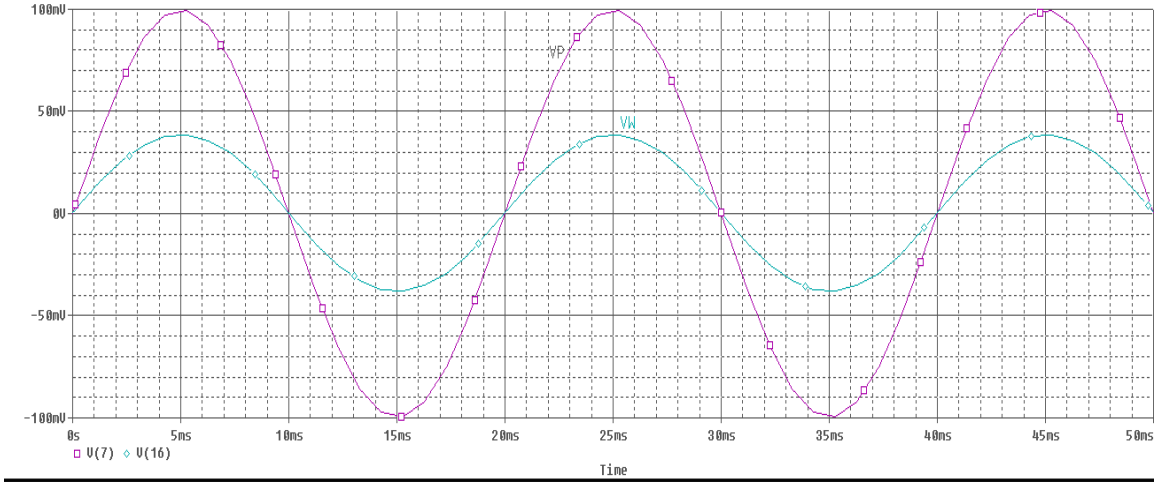


Fig38: Transient response of Non-inverting amplifier

4.4 Voltage Summer Circuit using VDBA

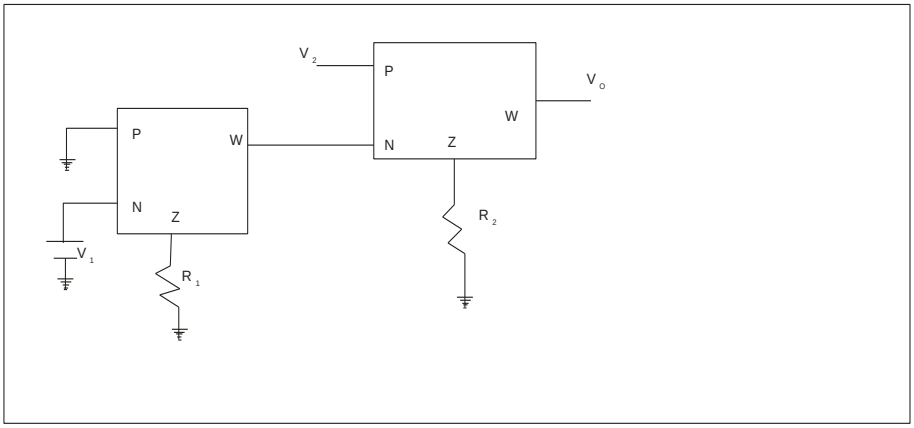


Fig39: Voltage Sumer Circuit using VDBA

Considering that input $V_1$is applied to the first VDBA and input V_2 is applied to the second VDBA. The current flowing out through the first VDBA is

$$I_{z_1} = g_{m_1}(V_P - V_N) = -g_{m_1}V_1 \quad \text{.....(4)}$$

The voltage at Z terminal of first VDBA is

$$V_{z_1} = I_{Z_1}R_1 = -g_{m_1}R_1V_1 \quad \text{..... (5)}$$

The output voltage at the W terminal of first VDBA is

$$V_{W_1} = \alpha_1 V_{Z_1} = -\alpha_1 g_{m_1}R_1V_1 \quad \text{..... (6)}$$

Now considering the second VDBA, the current flowing out of Z terminal

$$I_{Z_2} = g_{m_2}(V_2 - V_{W_1}) \quad \text{..... (7)}$$

The voltage at Z terminal

$$V_{Z_2} = g_{m_2}R_2(V_2 - V_{W_1}) \quad \text{..... (8)}$$

The output voltage at W terminal of second VDBA is

$$V_O = \alpha_2 V_{Z_2} = \alpha_2 g_{m_2}R_2(V_2 - V_{W_1}) = \alpha_2 g_{m_2}R_2(V_2 + \alpha_1 g_{m_1}R_1V_1) \quad \text{.....(9)}$$

Thus the output expression of the above summer circuit can be written as

$$V_O = \alpha_1\alpha_2 g_{m1}g_{m2}R_1R_2V_1 + \alpha_2 g_{m2}R_2V_2 \quad \text{..... (10)}$$

The output is a linear combination of both the inputs

4.5 Implementing an Integrator using VDBA

An integrator is an important device in analog signal devices. Integrator can be implemented using almost all active devices.

Consider the block shown below in fig40

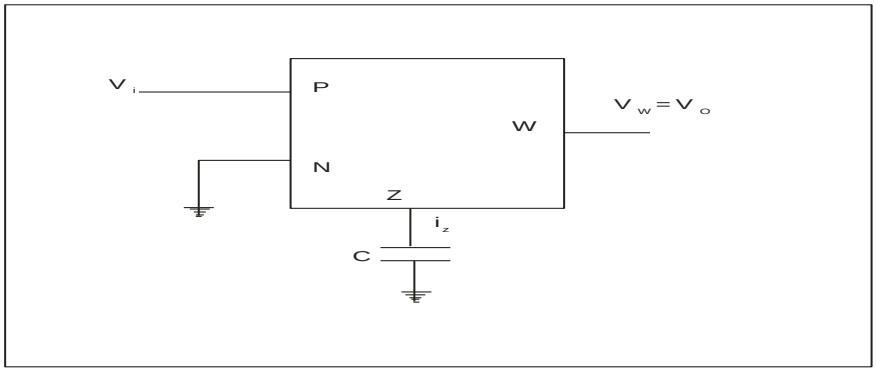


Fig40: Integrator using VDBA

The current flowing through the z-terminal

$i_{z=}g_m(V_P\text{-}V_N)=g_mV_i$

$$v_Z = \frac{1}{C}\int i_z dt$$

$$V_Z(s) = \frac{1}{sC} I_Z = \frac{g_m}{sC} V_i(s)$$

$$V_O(s) = V_W(s) = \alpha V_Z(s) = \frac{\alpha g_m}{sC} V_i(s)$$

$\frac{V_O(s)}{V_i(s)} = \frac{\alpha g_m}{sC}$ This is the transfer function of the stated integrator.

4.5.1 Simulation Results

The integrator circuit given in fig40 was simulated using PSpice where we have used the CMOS VDBA whose details have been given in previous chapter. The integrator was simulated with the following values; C=5µF, g_m=696.77 and α=0.79 and the simulation result when a square wave of amplitude 1V is applied at input terminal P is shown in fig 41.The time response of the circuit when an input pulse of amplitude 1V and frequency 1 KHz is given in fig42. The ac response when applied an AC input of amplitude 0.5V is shown in fig43

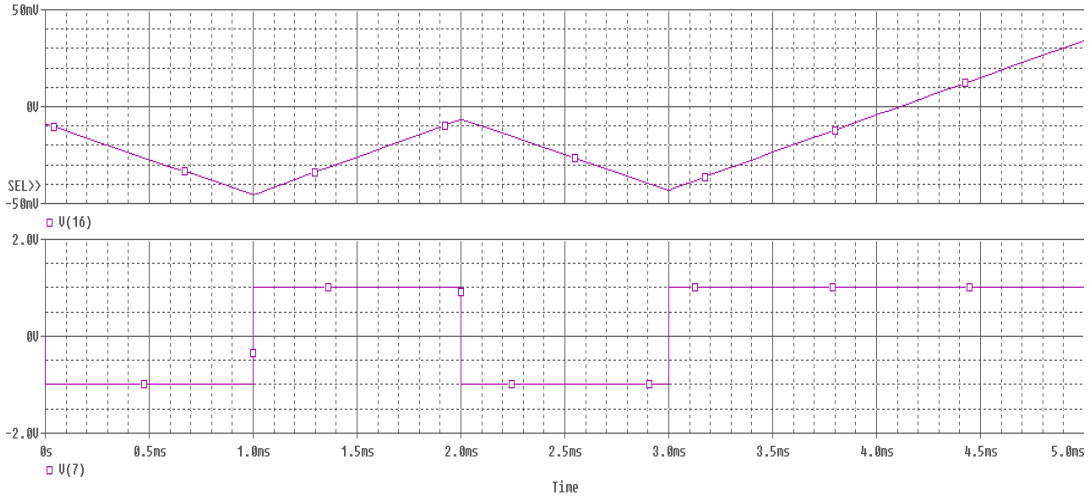


Fig41: Simulation of Integrator circuit

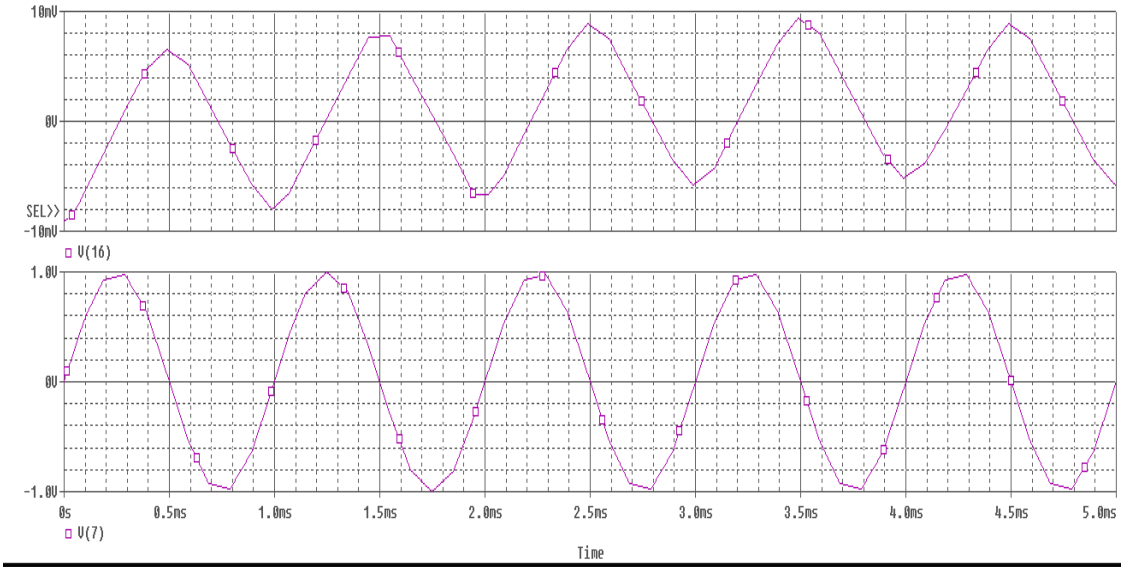


Fig42: Transient Response of Integrator Circuit

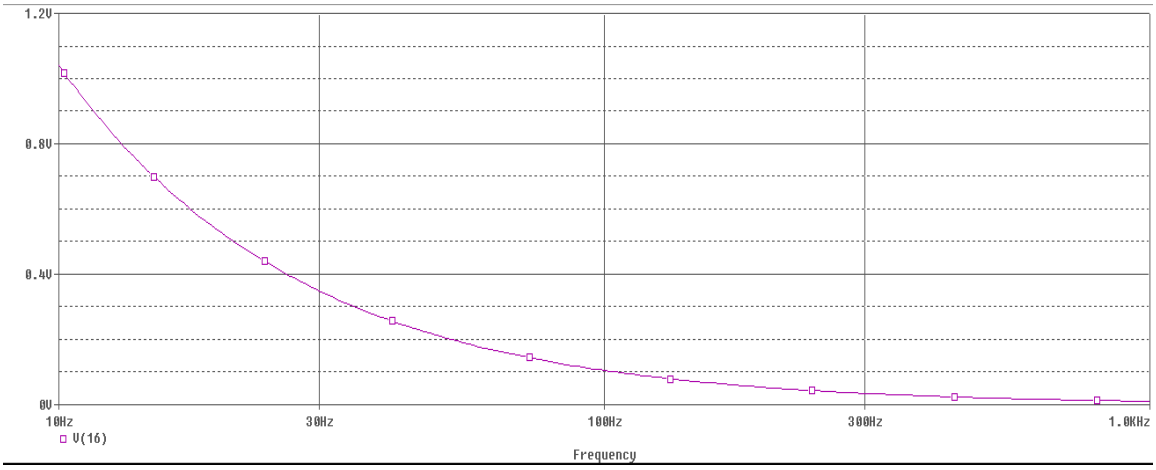


Fig43: AC response of Integrator

4.6 A First order Low Pass Filter using VDBA

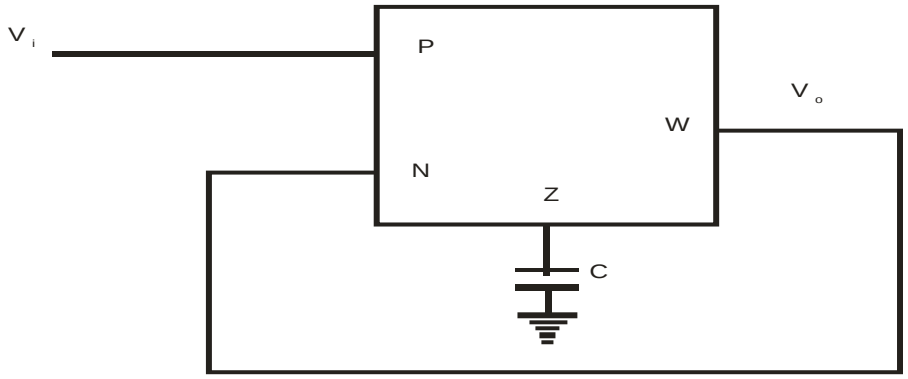


Fig44: First order Low Pass Filter using VDBA

For the LPF circuit shown the first order transfer function is given as

$\frac{V_o(s)}{V_i(s)} = \frac{\frac{\alpha g_m}{C}}{s + \frac{\alpha g_m}{C}} = \frac{a_0}{s + \omega_0}$. Where ω_0 represents the cut off frequency or $3\,dB$ frequency of the first order low pass filter circuit shown in fig44

Thus cut off frequency is $\frac{\alpha g_m}{C}$ and the dc gain is 1.

4.6.1 Simulation Results

The first order Low Pass Filter circuit shown in fig44 was simulated in PSpice using CMOS VDBA. The following values were used:

$$V_{B1} = V_{B2} = -0.16V, gm = 722.77\frac{\mu A}{V}, \alpha = 0.847, C = 100\,pF$$

$$f_0 = \frac{\alpha g_m}{2\pi C} = \frac{0.85*722.77*10^{-6}}{2*3.14*100*10^{-12}} = 0.98*10^6 = 0.98MHz$$

The ac response of the low pass filter circuit for an ac input of amplitude 1V is shown in fig45.From the simulation result obtained in fig45 we observed that cut off frequency is 1.09MHz. This small difference in cut off frequency is due to the fact that we have not considered the parasitic effect in our calculations.

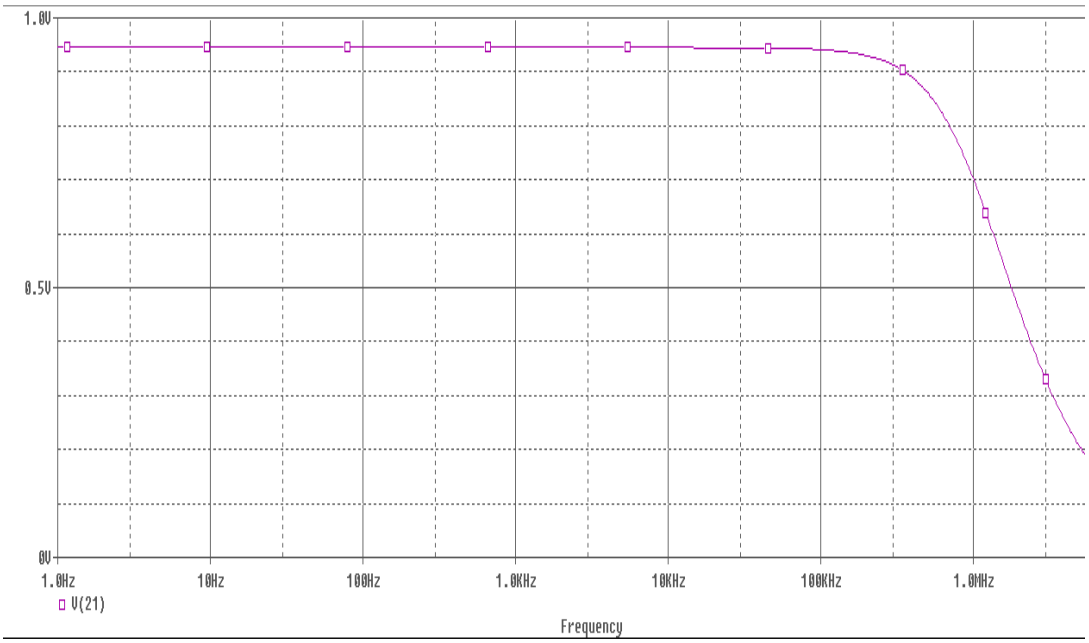


Fig45: AC response of First Order Low Pass Filter

The transient analysis of the low pass filter circuit was also performed using the same VDBA. We applied a sinusoidal input with amplitude 0.1V and frequency 0.5MHz and observed the waveforms at input node (20) and output node (21) as shown below in fig46

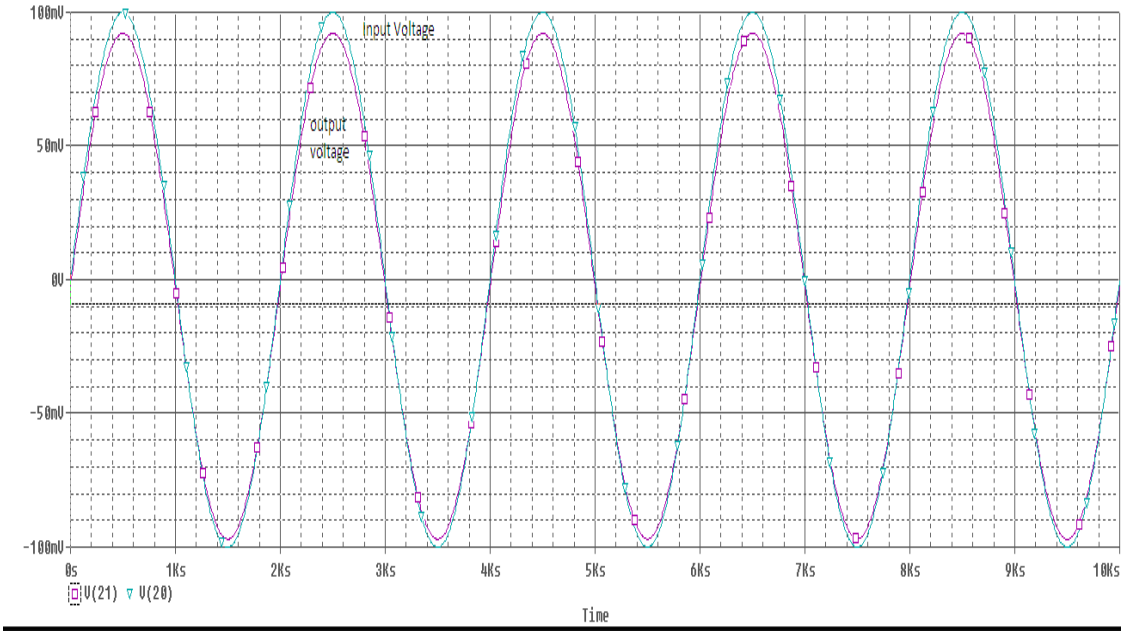


Fig46: Transient response of first order low pass filter

4.7 A First order High Pass Filter using VDBA

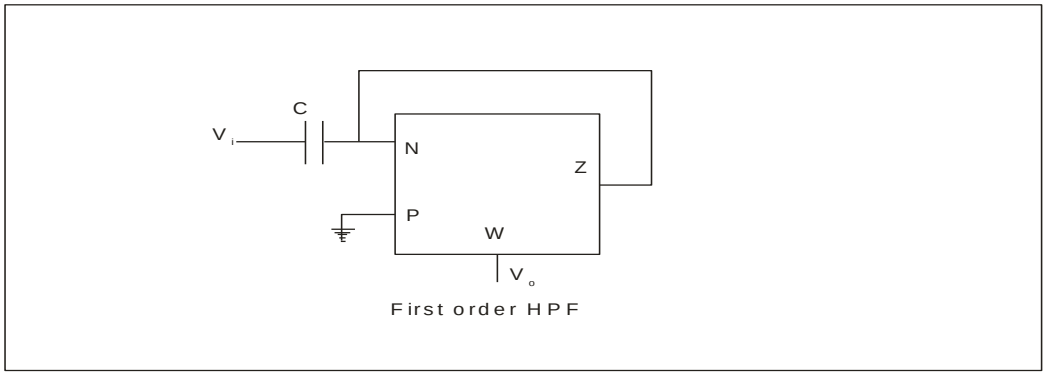


Fig47: First order High Pass Filter using VDBA

The transfer function of the above high pass filter circuit may be written as

$$\frac{V_o(s)}{V_i(s)} = \frac{\alpha sC}{sC + g_m} = \frac{\alpha s}{s + \frac{g_m}{C}} = \frac{a_1 s}{s + \omega_0}$$

Where ω_0 is the off frequency and $a_1$is the high frequency gain. Thus the expression for cut off frequency is $\frac{gm}{C}$ while the high frequency gain is α.

4.7.1 Simulation Results

For simulation of high pass filter circuit shown in fig47 the following values were taken

$$V_{DD} = -V_{ss} = 1.5V, V_{B1} = -0.16V, V_{B2} = -0.14V, C = 100\,pF, gm = 721\frac{\mu A}{V}, \alpha = 0.85$$

The value of cut off frequency is $f_0 = \frac{g_m}{2\pi C} = \frac{721}{2*3.14*100*10^{-12}} = 1.14MHz$

The ac response of the high pass circuit when an ac input signal of amplitude 0.5V was applied is shown in figure48. The observed cut off frequency is 1.07MHz.

The transient response, when sinusoidal input of amplitude 0.5V and frequency 10Hz is shown below in fig49

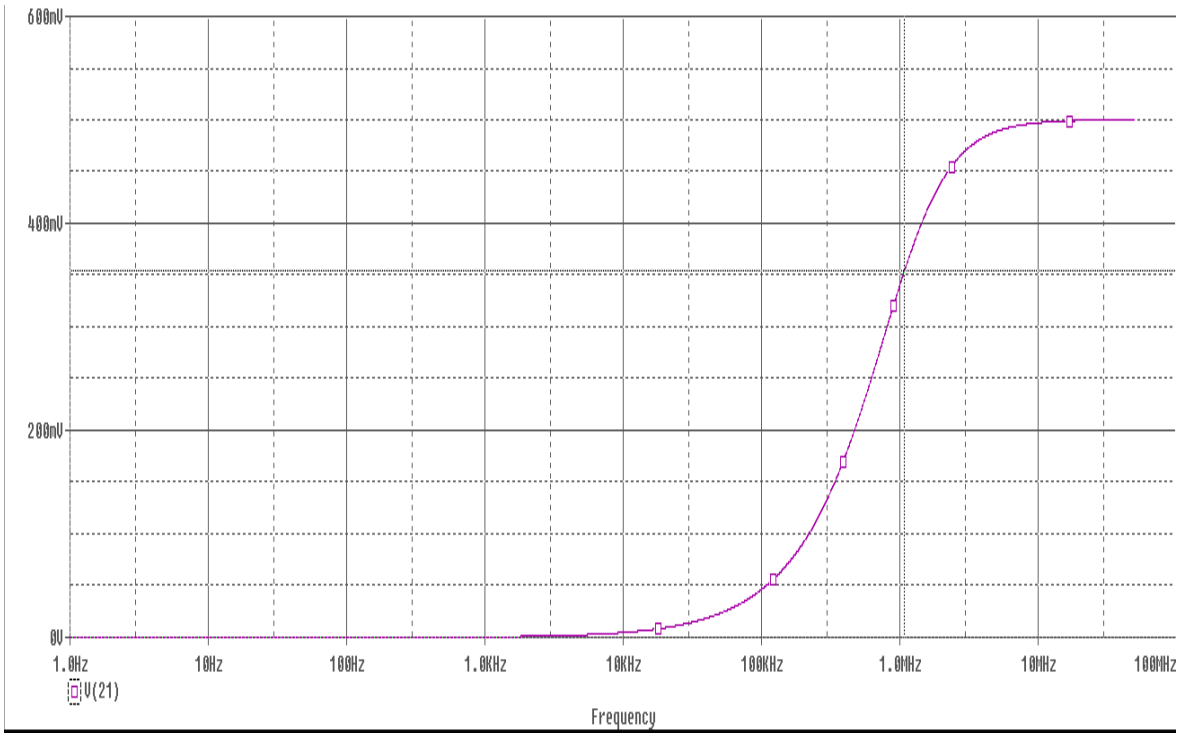


Fig48: AC response of First order High Pass Filter using VDBA

Fig49: Transient response of first order High Pass Filter using VDBA

4.8 Second Order Biquad Filter Structures

In this section present two structures proposed in [2], for biquad filters. These biquad filter contains two VDBAs and two capacitors and generates all filter functions low pass ,band pass, high pass, band stop and all pass, but this topology needs inverting type input voltage signal for the employed AP filters. The second proposed biquad filter employs two VDBAs, two capacitors and a resistor and realizes the all filter functions without the use of inverting input terminals. Furthermore quality factor can be adjusted with resistor as natural frequency.

4.8.1 First Biquad Structure [2]

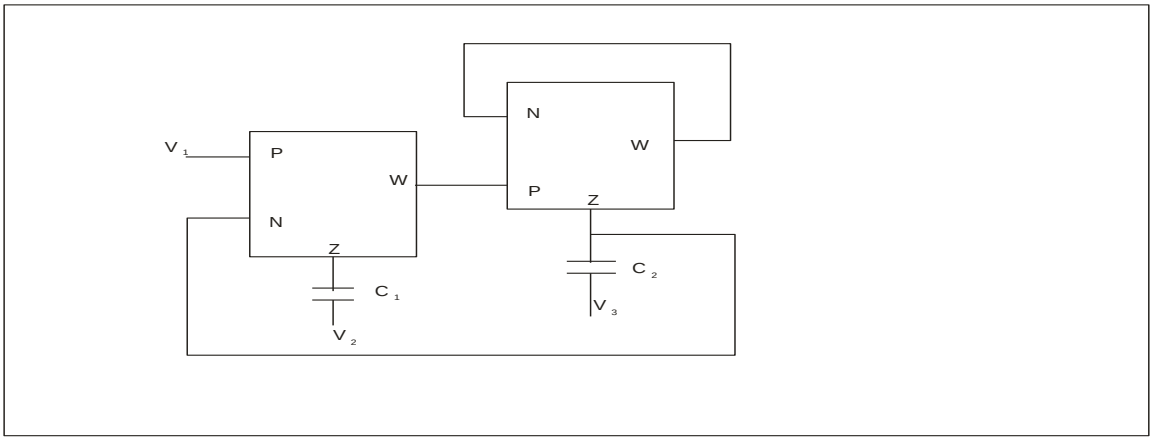


Fig50: First Biquad structure

The first proposed circuit that can be used as three inputs-single output voltage-mode filters is shown in the above figure. The node analysis of circuit yields the following voltage transfer function.

$$V_o = \frac{V_3 s^3 C_1 C_2 \alpha_2 + V_2 s g_{m_2} C_1 \alpha_1 \alpha_2 + V_1 g_{m_1} g_{m_2} \alpha_1 \alpha_2}{s^2 C_1 C_2 + s g_{m_2} C_1 \alpha_2 + g_{m_1} g_{m_2} \alpha_1}$$

Depending on the voltage status of V_1, V_2 *and* V_3 in the numerator of above equation , one of the following five filter functions are realized.

(i) LPF: $V_2 = V_3 = 0, V_1 = V_{IN}$

(ii) BPF: $V_1 = V_3 = 0, V_2 = V_{IN}$

(iii) HPF: $V_1 = V_2 = 0, V_3 = V_{IN}$

(iv) BSF: $V_2 = 0, V_1 = V_3 = V_{IN}$

(v) APF: $V_1 = V_3 = -V_2$

The pole frequency (ω_0) and Quality factor(Q) of the first proposed biquad filter are given as follows;

$$\omega_0 = \sqrt{\frac{g_{m_1} g_{m_2} \alpha_1}{C_1 C_2}}, Q = \frac{1}{\alpha_2}\sqrt{\frac{g_{m_1} C_2 \alpha_1}{g_{m_2} C_1}}$$

4.8.1.1 Low Pass Filter Using first proposed BIQUAD

The circuit for second order Low Pass Filter is shown below

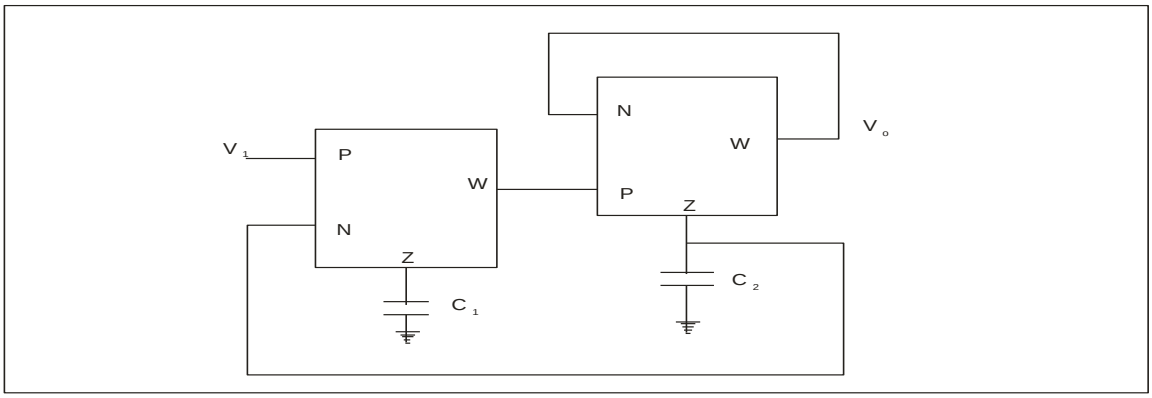


Fig51: Second order Low Pass Filter structure

The output of the circuit shown in fig4 (XX) may be written as

$V_o = \frac{V_i g_{m_1} g_{m_2} \alpha_1 \alpha_2}{s^2 C_1 C_2 + s g_{m_2} C_1 \alpha_2 + g_{m_1} g_{m_2} \alpha_1}$. The cut off frequency is $f_0 = \frac{1}{2\pi}\sqrt{\frac{g_{m1} g_{m2} \alpha_1}{C_1 C_2}}$

The dc gain is α_2

4.8.1.1. A Simulation Results

Two VDBAs have been used in the implementation of second order low pass filter.

Taking trans-conductance and voltage ratio of each is same: $g_{m1} = g_{m2} = 721\frac{\mu A}{V}$,

$\alpha_1 = \alpha_2 = 0.85$

When an ac input of amplitude 0.5V was applied, the output at dc frequency

$V_o = 0.5*0.84 = 442mV$, $V_{o3dB} = 0.5*0.84*0.707 = 282mV$

The cut off frequency is $f_0 = \frac{1}{2\pi}\sqrt{\frac{721*721*10^{-12}*.84}{100*100*10^{-12}}} = 1.06MHz$

The observed cut off frequency was 1.4MHz.

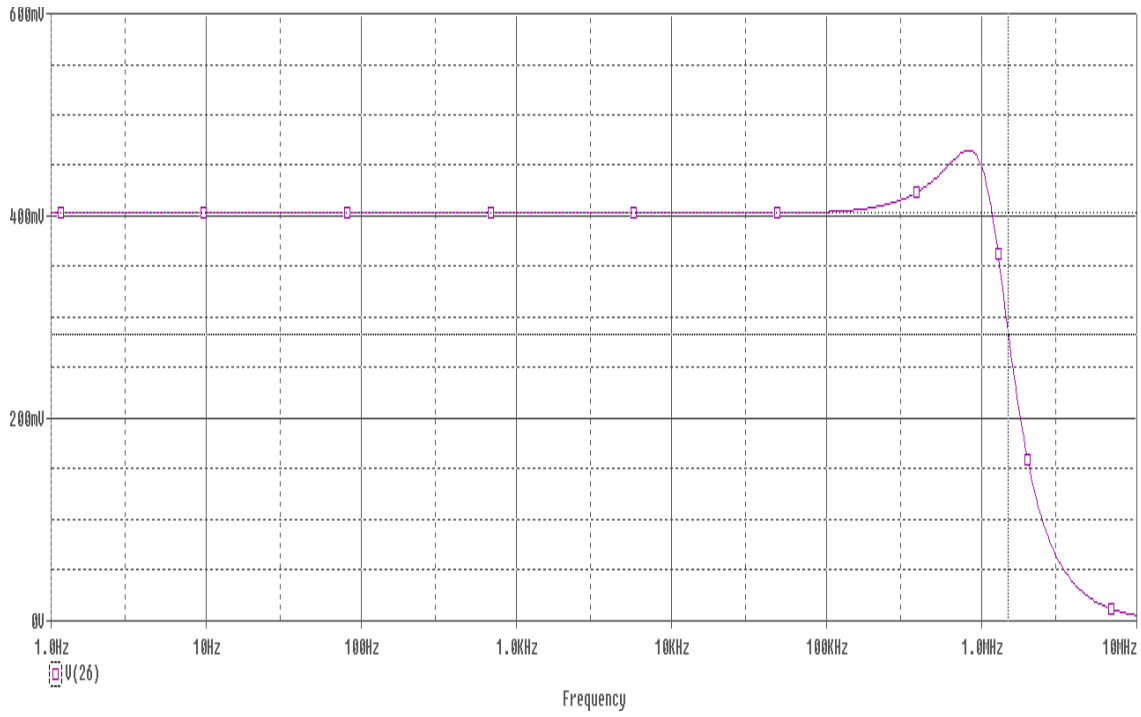


Fig52: AC response of 2nd order Low Pass Filter

The transient response of the circuit when an input signal of amplitude 0.5V and frequency 0.5MHz was applied is shown below in fig53. The output signal is also sinusoidal with amplitude 0.4V. All the signals of frequency below the cut off may get passed through this low pass filter circuit.

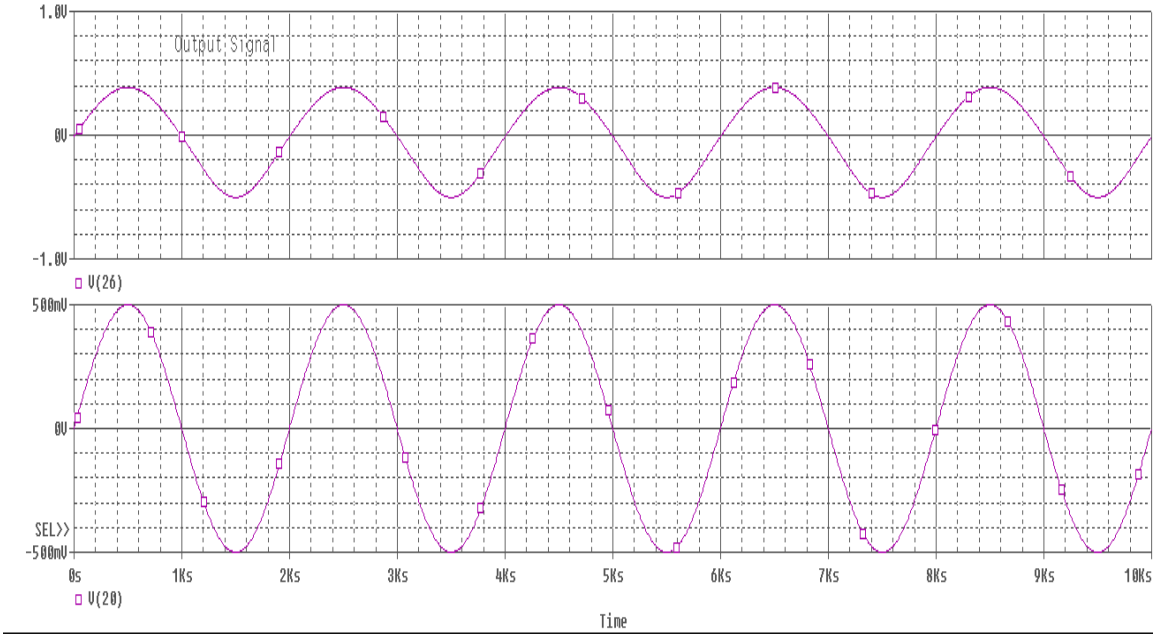


Fig53: Transient response for input frequency less than cut off

Now we applied a sinusoidal input of amplitude 0.5V and frequency 2MHz (more than cut off frequency) and observed the transient response as shown in fig54

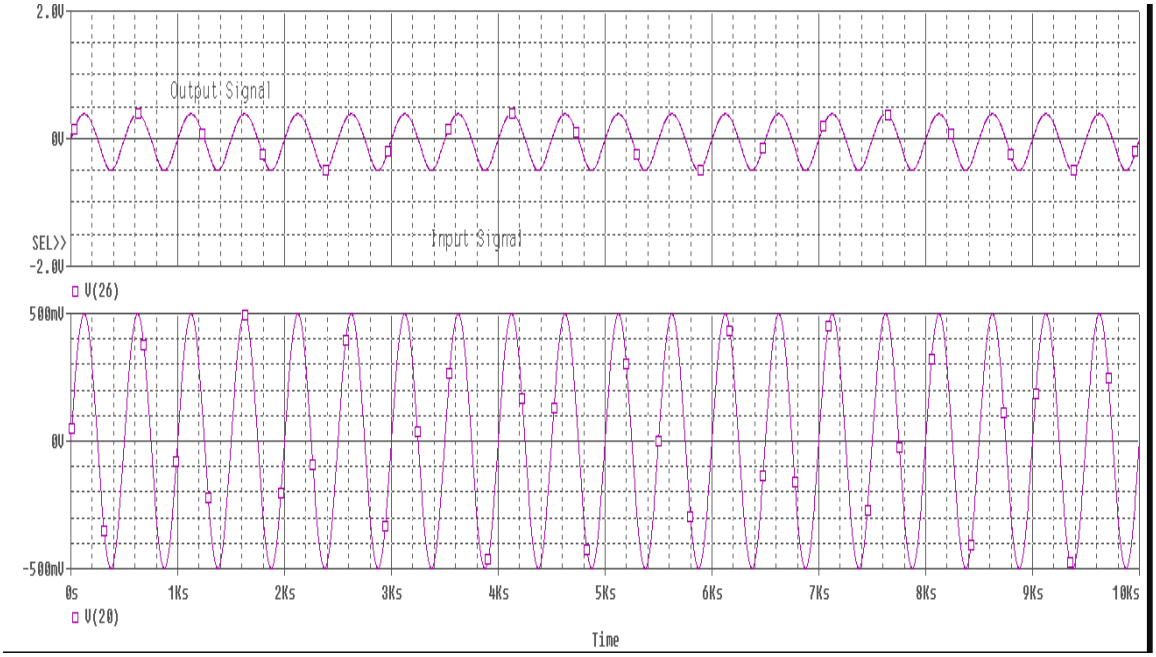


Fig54: Transient response for input frequency more than cut off

We observed that input signals of frequency more than cut off are not passed without attenuation. The amplitude of output signal was observed 0.1V for an ac input of 0.5V.Hence we can conclude that the given circuit is performing well as a low pass filter.

4.8.1.2 Band Pass Filter using first proposed BIQUAD

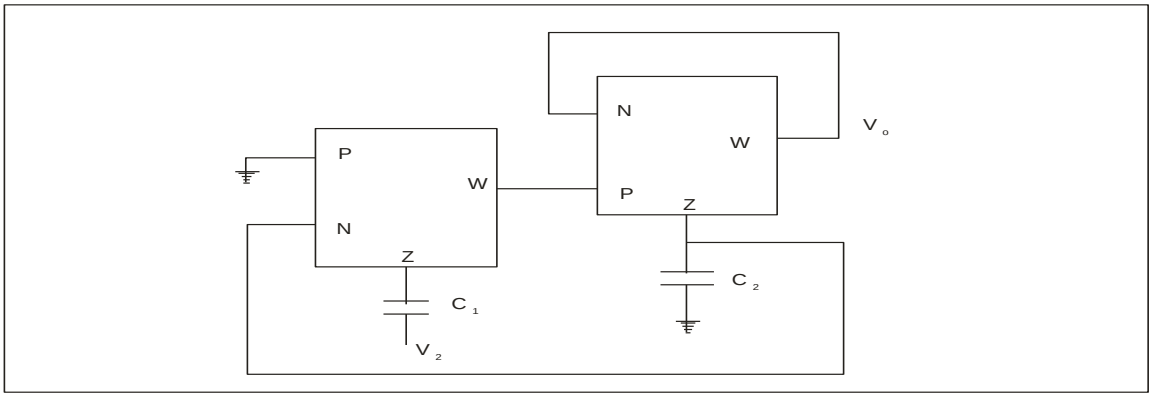


Fig55: Second order Band Pass Filter Structure

The output of the band pass circuit shown above is written as

$$V_o = \frac{g_{m2}C_1\alpha_1\alpha_2 sV_{in}}{s^2C_1C_2 + sg_{m2}C_1\alpha_2 + g_{m1}g_{m2}\alpha_1}.$$

The magnitude response peaks at $\omega = \omega_0$. Thus the center frequency of the band pass filter is equal to the pole frequency $\omega_0 = \sqrt{\frac{g_{m1}g_{m2}\alpha_1}{C_1C_2}}$

4.8.1.2. A Simulation Results

The second order band pass circuit shown in figure 55 was simulated in PSpice with the following values

$V_{DD} = -V_{SS} = 1.5V, C_1 = C_2 = 100pF$, The VDBA used in the simulation had the following values: $V_{B1} = -0.16V, V_{B2} = -0.14V, g_{m1} = g_{m2} = 721\frac{\mu A}{V}, \alpha_1 = \alpha_2 = 0.84$

For the above chosen values, the pole frequency comes to be

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{721*721*10^{-12}*0.84}{100*100*10^{-24}}} = 1.05MHz$$

The ac response of band pass circuit was obtained by applying an ac input of amplitude 0.5V, which is shown below in fig56

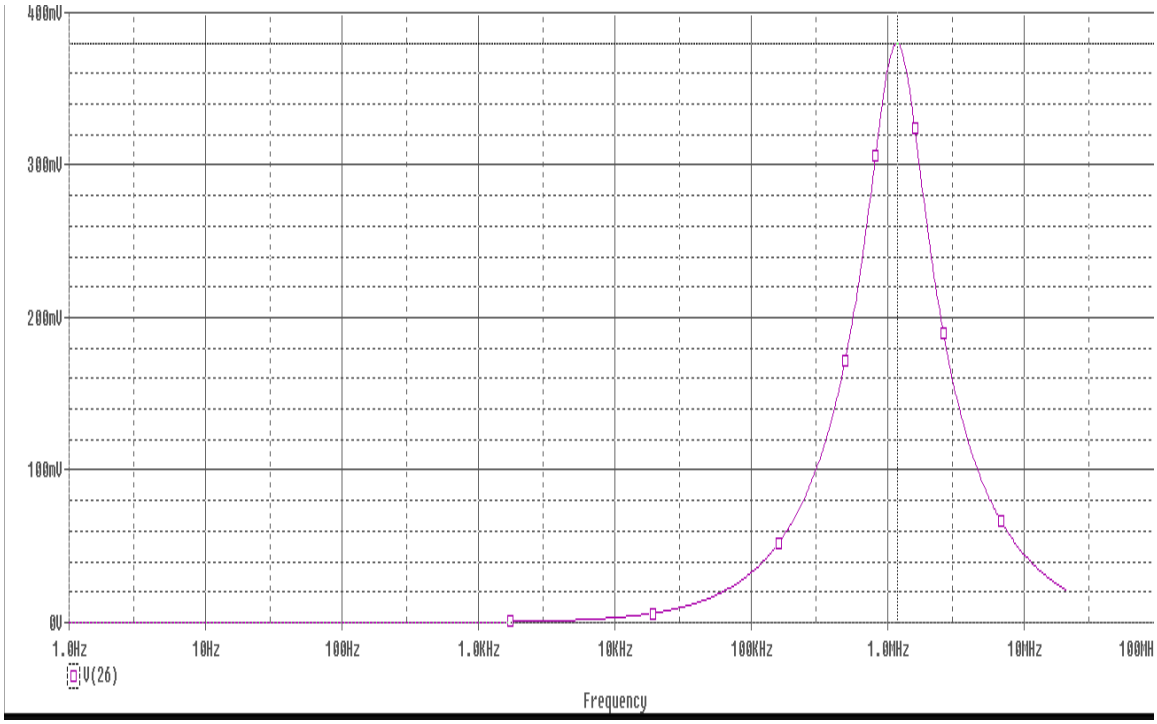


Fig56: AC response of the circuit shown in fig55

From the ac response obtained for second order band pass circuit we found that the magnitude peak occurs at 1.14MHz frequency,

4.8.1.3 Band Stop Filter using first proposed BIQUAD

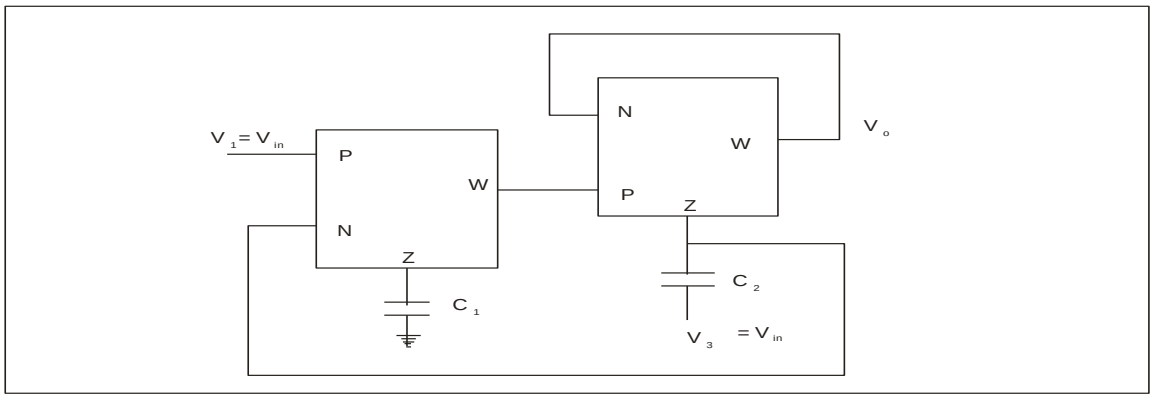


Fig57: Band Stop Filter Structure

The output of the band stop circuit shown above is given as

$$V_o = \frac{V_{in}(s2C1C2\alpha 2 + gm1gm2\alpha 1\alpha 2)}{s^2C_1C_2 + sg_{m2}C_1\alpha_2 + g_{m1}g_{m2}\alpha_1}$$

4.8.1.3. A Simulation Results

The simulation of the band stop circuit was performed in PSpice using the following values

$$V_{DD} = -V_{SS} = 1.5V, V_{B1} = -0.16V, V_{B2} = -0.14V, g_{m1} = g_{m2} = 721\frac{\mu A}{V}, \alpha_1 = \alpha_2 = 0.84, C_1 = C_2 = 100\,pF$$

The ac response of the band stop circuit when two ac signals V_1 and $V_3$of amplitude 0.5V each were applied, is shown below in fig58

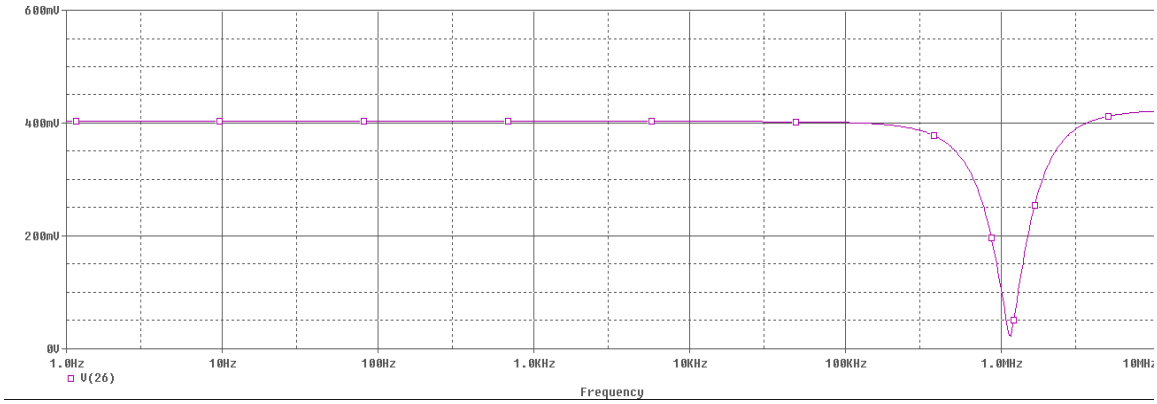


Fig58: AC response of Band stop filter

4.8.1.4 High Pass Filter using First proposed Biquad

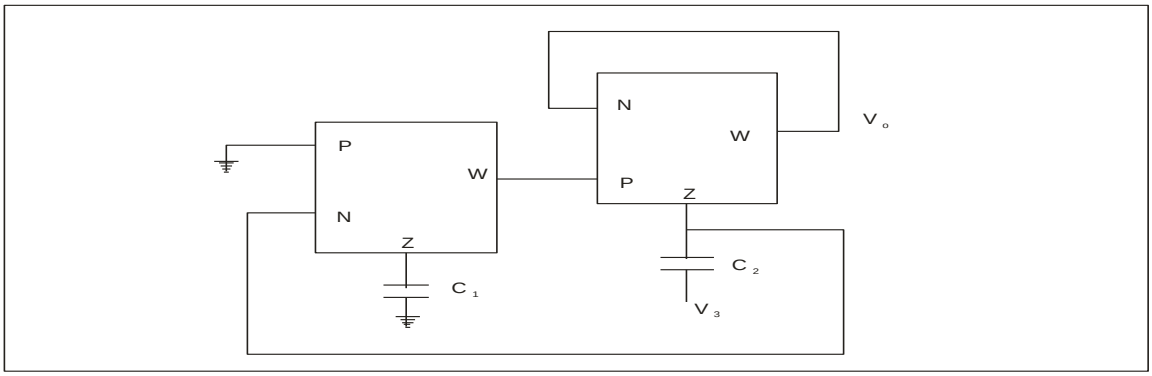


Fig59: Second Order High Pass Filter structure

The output of the second order high pass circuit shown above is given below

$$V_o = \frac{V_3 s^3 C_1 C_2 \alpha_2}{s^2 C_1 C_2 + s g_{m2} C_1 \alpha_2 + g_{m1} g_{m2} \alpha_1}$$

The cut off frequency is given by $f_0 = \frac{1}{2\pi}\sqrt{\frac{g_{m1} g_{m2} \alpha_1}{C_1 C_2}}$

4.8.1.4. A Simulation Results

For the simulation of the high pass circuit shown above in PSpice, the following values were used

$$V_{DD} = -V_{SS} = 1.5V, V_{B1} = -0.16V, V_{B2} = -0.14V,$$

$$g_{m1} = g_{m2} = 721\frac{\mu A}{V}, \alpha_1 = 0.84, \alpha_2 = 0.84, C_1 = C_2 = 100\,pF$$

From above chosen values the cut off frequency

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{721*721*10^{-12}*0.84}{100*100*10^{-24}}} = 1.05MHz$$

The ac response of the high pass circuit obtained, when applied an ac input signal of amplitude 0.5V is shown in fig60. The observed cut off frequency is 0.94MHz. .

The transient response of the circuit shown in fig59 when input signals of amplitude 0.5V and 1 KHz was applied is given in fig61

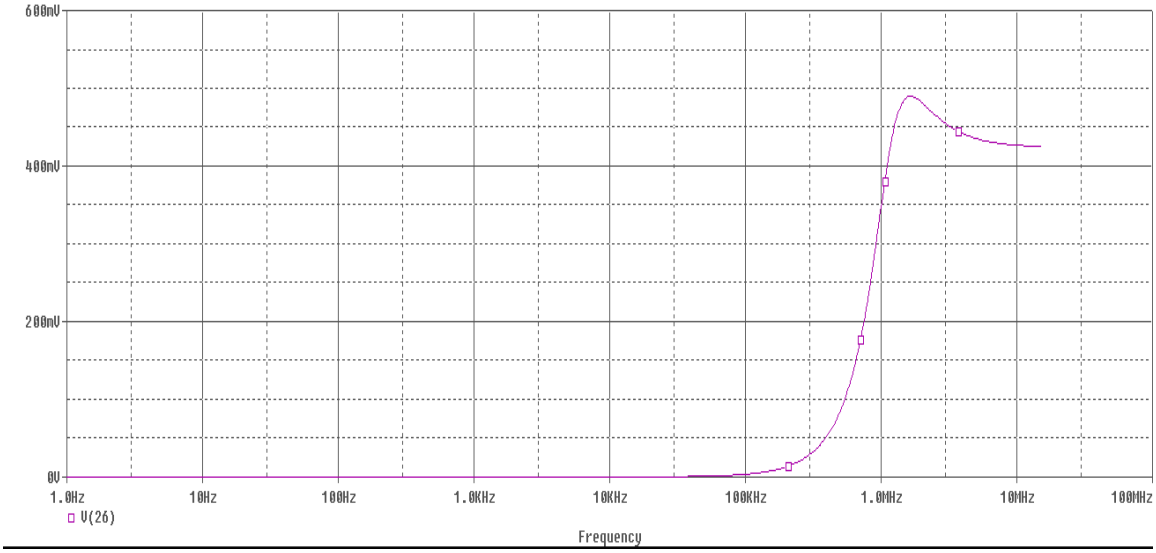


Fig60: AC response of circuit shown 2nd order HPF

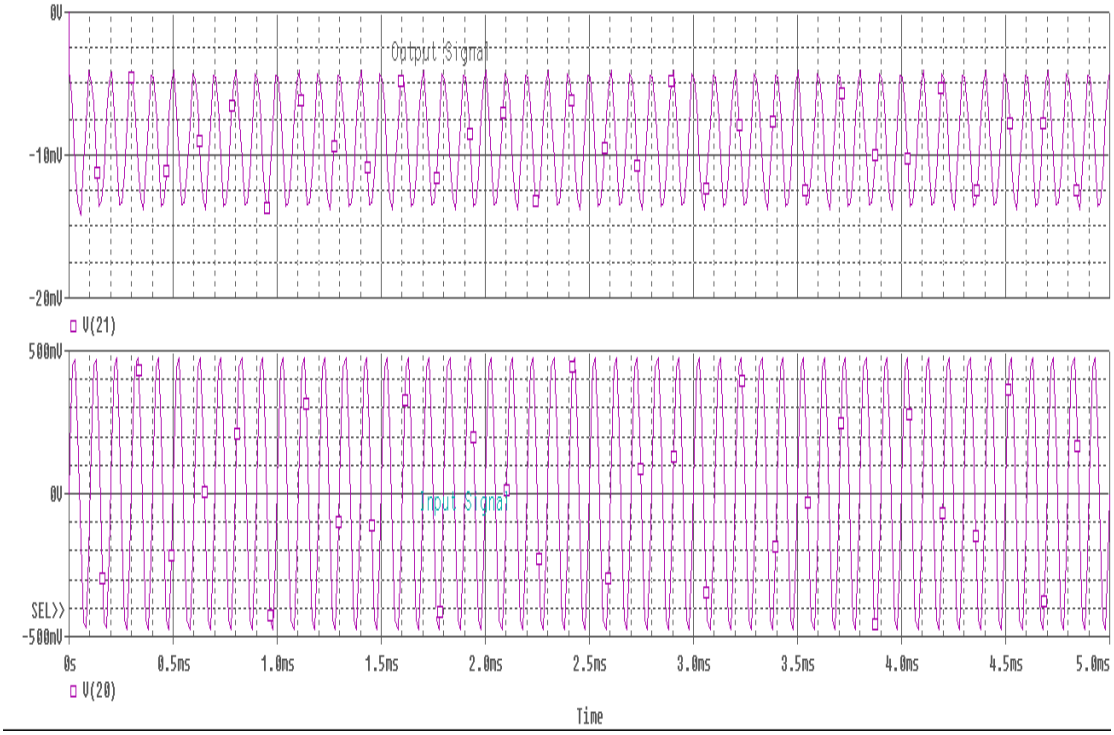


Fig61: Transient response of 2nd order HPF

4.8.2 Second Proposed Biquad [2]

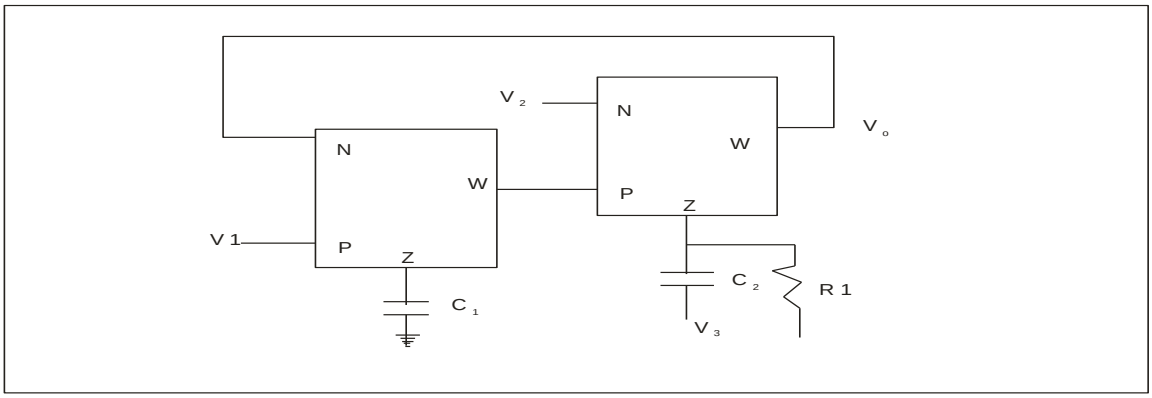


Fig62: Second Biquad Structure

The second proposed biquad filter is shown in above figure. Its transfer function can be given as

$$V_o = \frac{V_3 s^2 C_1 C_2 \alpha_2 - V_2 s C_1 g_{m_2} \alpha_2 + V_1 g_{m_1} g_{m_2} \alpha_1 \alpha_2}{s^2 C_1 C_2 + \frac{s C_1}{R_1} + g_{m_1} g_{m_2} \alpha_1 \alpha_2}$$

It can be seen from the above equation that the proposed filter can be used to obtain five types of filters, those are summarized as;

(i) LPF: $V_2 = V_3 = 0, V_1 = V_{IN}$

(ii) BPF: $V_1 = V_3 = 0, V_2 = V_{IN}$

(iii) HPF: $V_1 = V_2 = 0, V_3 = V_{IN}$

(iv) BSF: $V_2 = 0, V_1 = V_3 = V_{IN}$

(v) APF: $V_1 = V_3 = V_2 = V_{IN}$

The pole frequency (ω_0) and Quality factor (Q) of the second proposed biquad filter are given as follows

$\omega_0 = \sqrt{\frac{g_{m_1} g_{m_2} \alpha_1 \alpha_2}{C_1 C_2}}$, $Q = R_1 \sqrt{\frac{g_{m_1} g_{m_2} C_2 \alpha_1 \alpha_2}{C_1}}$ Clearly Q can be tuned by different resistor values as independent natural frequency.

4.8.2.1 Low Pass Filter using second proposed Biquad

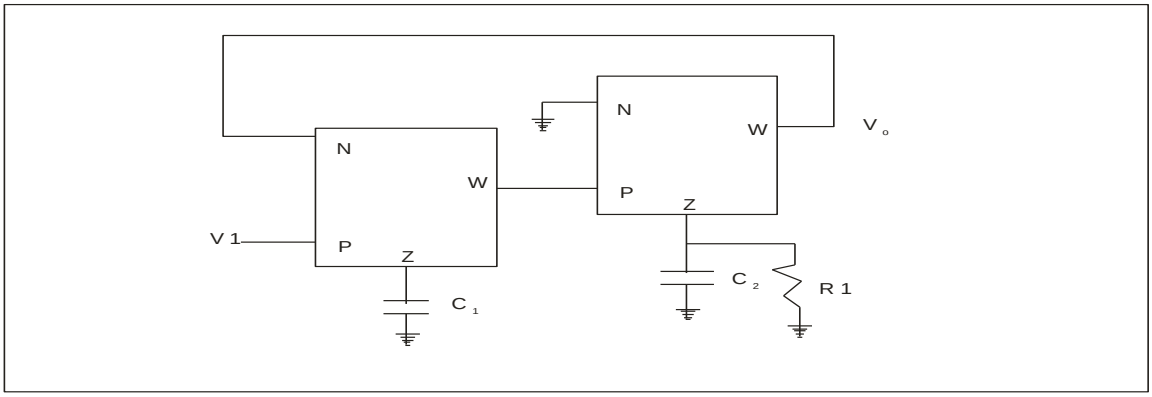


Fig63: Second Order Low Pass Filter Structure

The output of the low pass circuit shown above is written as

$$V_o = \frac{V_1 g_{m1} g_{m2} \alpha_1 \alpha_2}{s^2 C_1 C_2 + \frac{s C_1}{R_1} + g_{m1} g_{m2} \alpha_1 \alpha_2}$$ Where the cut off frequency $f_0 = \frac{1}{2\pi}\sqrt{\frac{g_{m1} g_{m2} \alpha_1 \alpha_2}{C_1 C_2}}$

4.8.2.1. A Simulation Results

For the simulation of the low pass circuit shown above in PSpice, the following values were used

$$V_{DD} = -V_{SS} = 1.5V, V_{B1} = -0.16V, V_{B2} = -0.14V,$$
$$g_{m1} = g_{m2} = 721\frac{\mu A}{V}, \alpha_1 = 0.84, \alpha_2 = 0.84, C_1 = C_2 = 100\,pF$$

From the above chosen values, the cut off frequency is

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{721*721*10^{-12}*0.84*0.84}{100*100*10^{-24}}} = 0.96MHz$$

The ac response of the low pass circuit, when an ac input of amplitude 1V was applied is shown in fig63. The transient response of the circuit when an input signal of amplitude 1V and frequency 1 KHz was applied is shown below in fig64

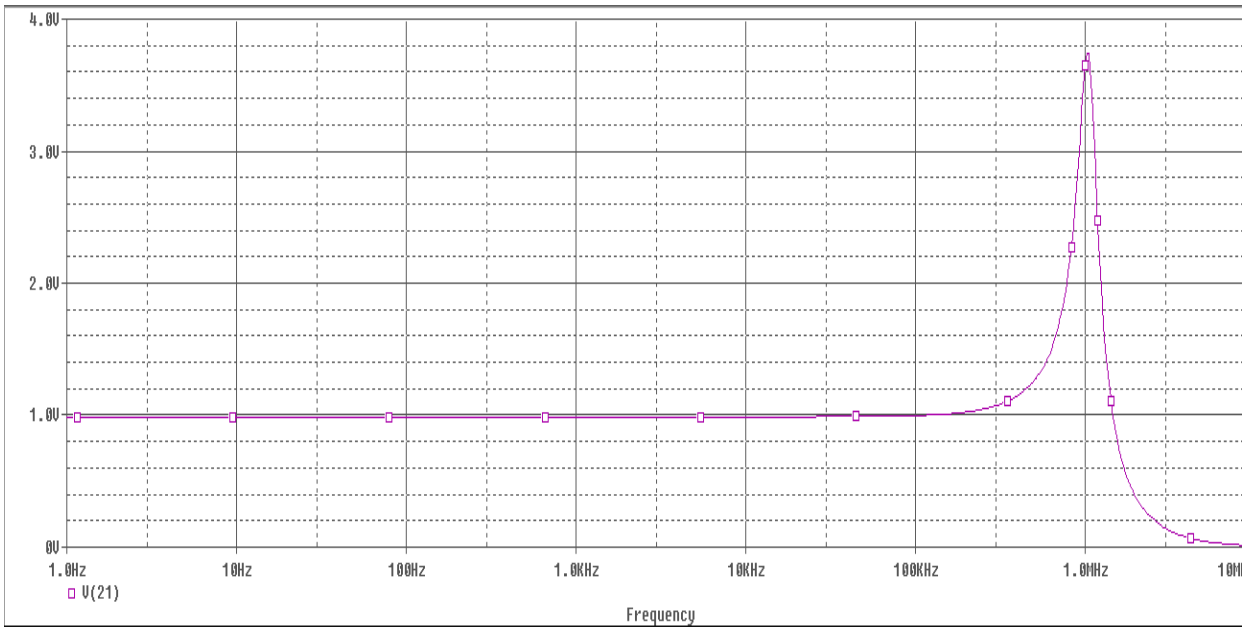


Fig64: AC response of 2^{nd} order LPF using second biquad

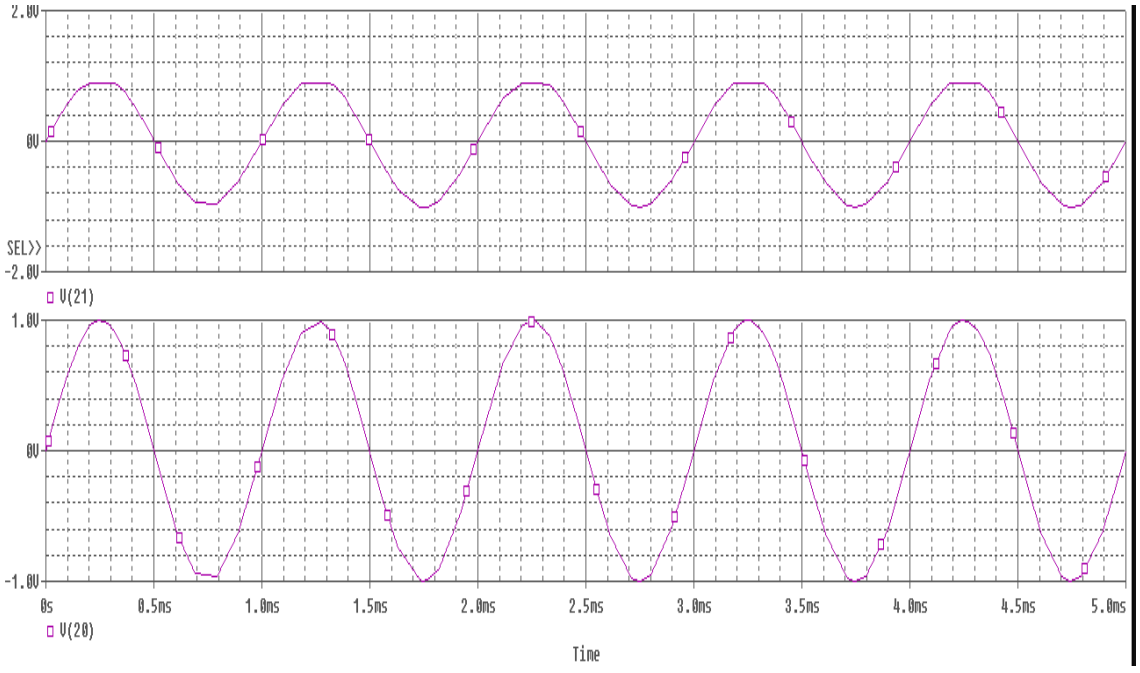


Fig65: Transient response of 2nd order LPF using second biquad

4.8.2.2 Band Pass Filter using second proposed Biquad

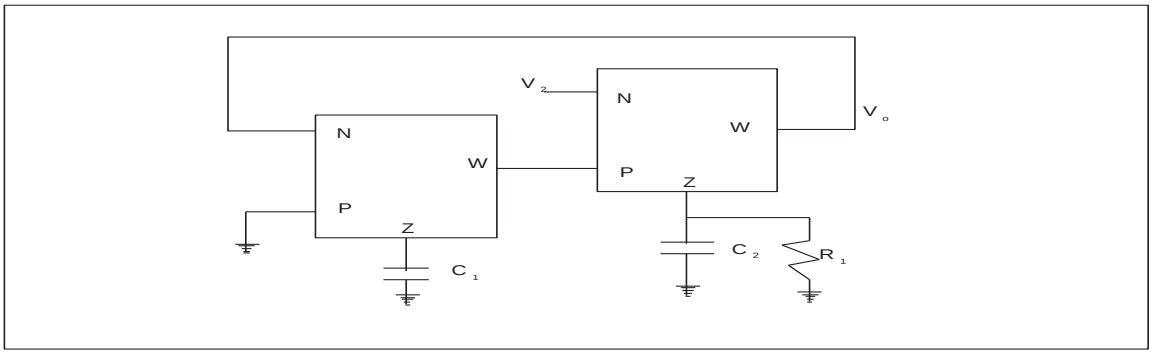


Fig66: Second Order Band Pass Filter Structure

4.8.2.2. A Simulation Results

The band pass circuit shown in fig66 was simulated in PSpice using the values

$V_{DD} = -V_{SS} = 1.5V, C_1 = C_2 = 100\,pF$, The VDBA used in the simulation had the following values: $V_{B1} = -0.16V, V_{B2} = -0.14V, g_{m1} = g_{m2} = 721\frac{\mu A}{V}, \alpha_1 = \alpha_2 = 0.84$

AC response was obtained by applying an ac signal of 0.5V which is shown in fig67

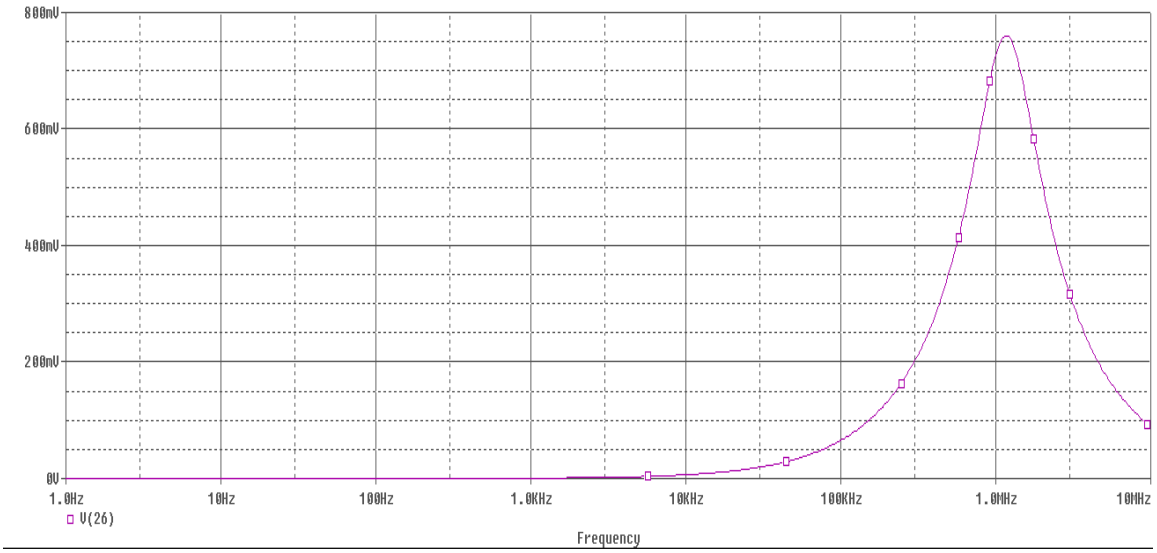


Fig67: AC response of circuit shown in fig66

4.8.2.3 Band Stop Filter using second proposed BIQUAD

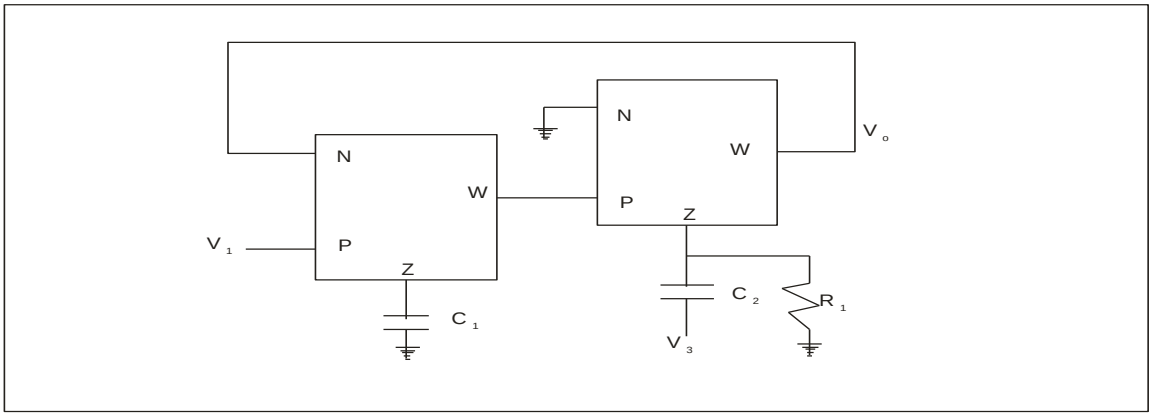


Fig66: Band Stop Filter Structure

4.8.2.3. A Simulation Results

The simulation of the band stop circuit was performed in PSpice using the following values

$$V_{DD} = -V_{SS} = 1.5V, V_{B1} = -0.16V, V_{B2} = -0.14V, g_{m1} = g_{m2} = 721\frac{\mu A}{V}, \alpha_1 = \alpha_2 = 0.84, C_1 = C_2 = 100\,pF$$

The ac response of the band stop circuit when two ac signals V_1 and $V_3$of amplitude 0.5V each were applied, is shown below in fig67

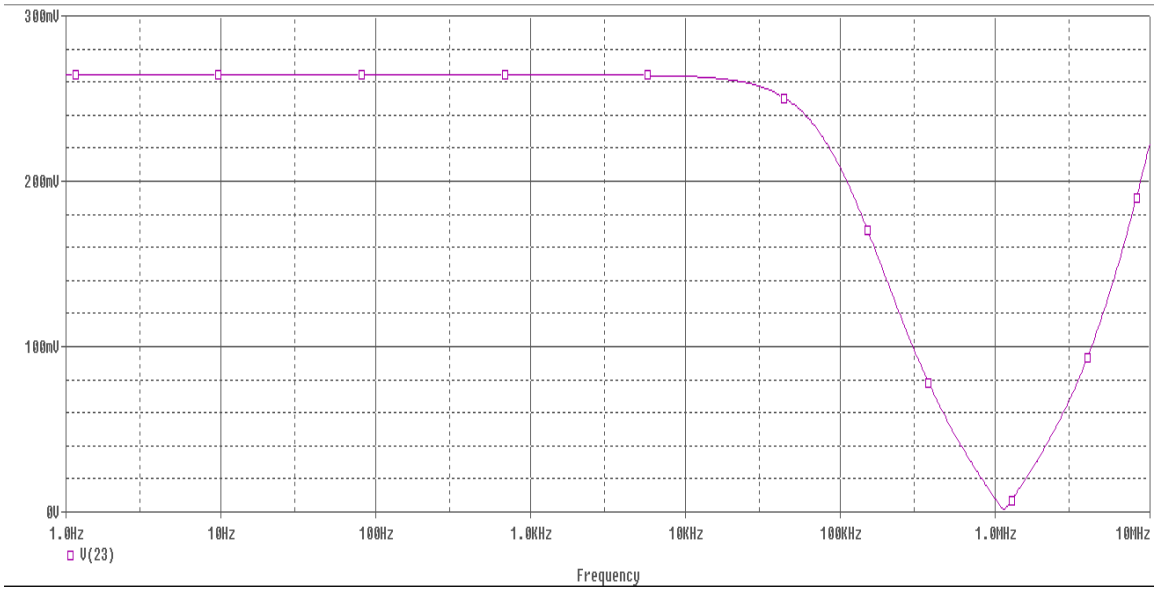


Fig67: AC response of the circuit shown in fig66

4.8.2.4 High Pass Filter using second proposed BIQUAD

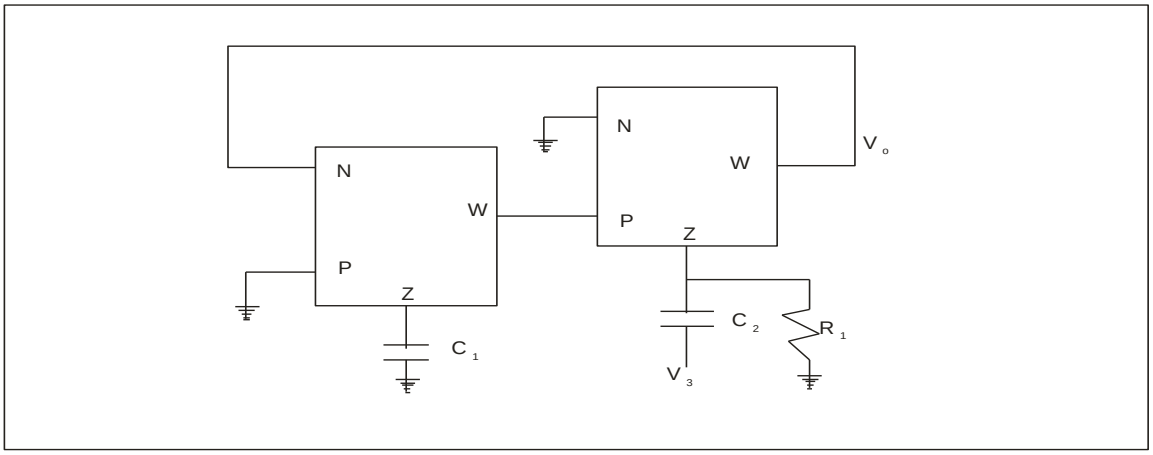


Fig68: High Pass Filter Structure

4.8.2.4. A Simulation Results

For the simulation of the high pass circuit shown above in PSpice, the following values were used

$$V_{DD} = -V_{SS} = 1.5V, V_{B1} = -0.16V, V_{B2} = -0.14V,$$

$$g_{m1} = g_{m2} = 721\frac{\mu A}{V}, \alpha_1 = 0.84, \alpha_2 = 0.84, C_1 = C_2 = 100\,pF$$

From above chosen values the cut off frequency

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{721*721*10^{-12}*0.84}{100*100*10^{-24}}} = 1.05MHz$$

The ac response of the high pass circuit obtained, when applied an ac input signal of amplitude 0.5V is shown in fig69. The observed cut off frequency is 0.94MHz. .

The transient response of the circuit shown in fig68 when input signals of amplitude 0.5V and frequencies 1 KHz and 1 MHz applied is shown in fig70

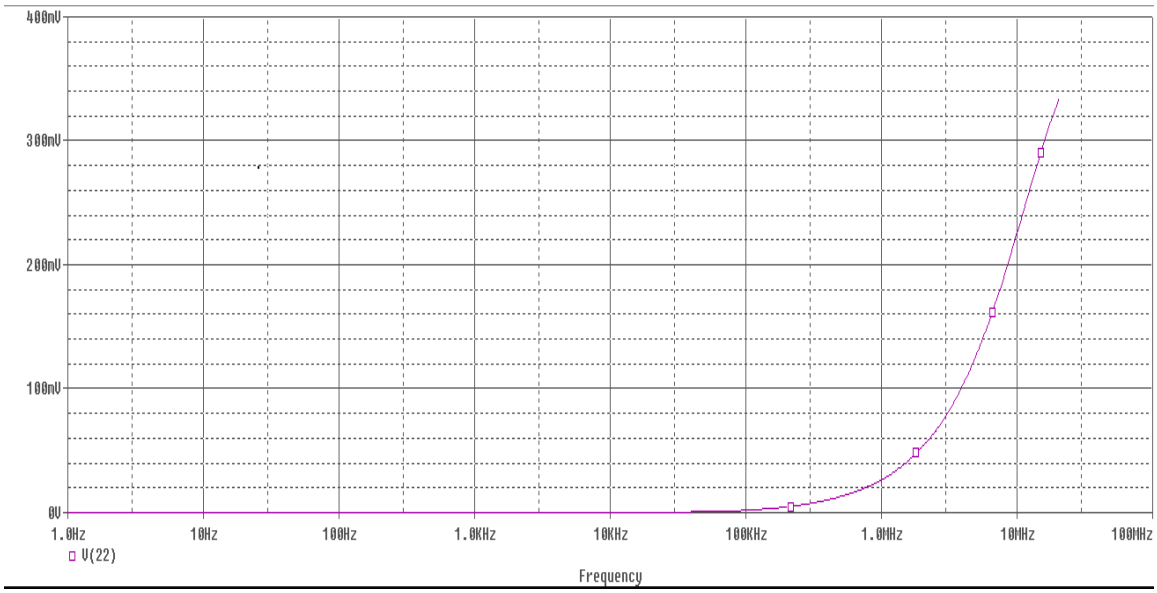
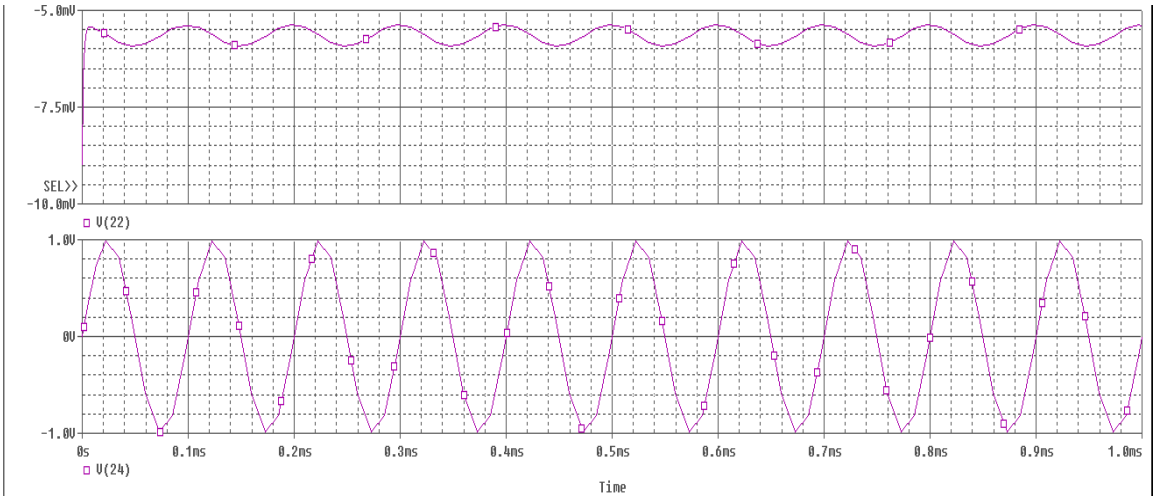
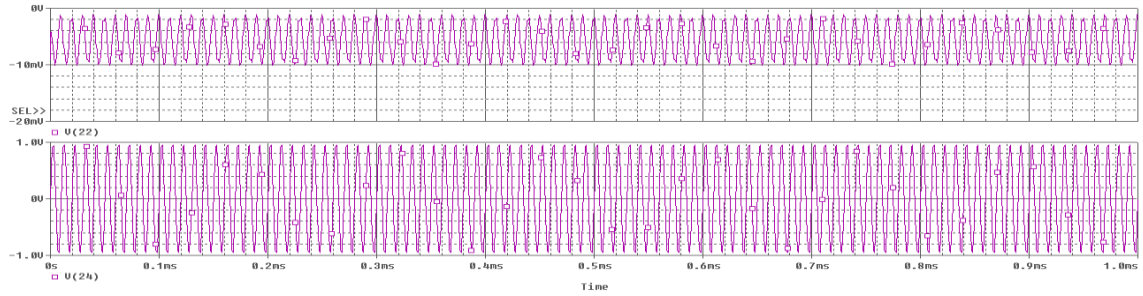


Fig69: AC response of circuit shown in fig68



(a)



(b)

Fig70: Transient response of the circuit shown in fig68

4.9 Conclusion

In this chapter simple applications of VDBA were presented**.** The basic amplifiers, summer, integrator and filter applications are the most important and essential of any new active device. The two proposed voltage- mode biquad filters were verified. Both filter circuits realize all filter configurations and natural frequency can be tuned electronically with bias voltage. Furthermore quality factor of the second proposed filter can be adjusted to resistor as independent natural frequency.

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CHAPTER-5 →

KHN BIQUAD USING VDBA

5. Introduction

In the previous chapter we have presented some applications of VDBA in signal processing. In this chapter we present a VDBA based KHN type biquad. A vest amount of literature is available on KHN type biquads using all kinds of active building blocks.. We have referred only the works presented in [1]-[5]. For simulation purpose we have used CMOS implementation of [6].

5.1 Biquads using two Integrator loop

Biquad filters can be realized with two integrators in a loop. Such a biquad circuit is more popularly referred to KHN Biquad, named after the inventors, Kerwin, Huelsman and New Comb. A KHN Biquad is characterized by the following features.

(i) It is single input multiple output type structure

(ii) There is simultaneous availability of the generic filtering functions namely Low Pass, High Pass and Band Pass, Band Elimination and All Pass.

(iii) By adding Low Pass and High Pass responses a Band Elimination response may be obtained. Similarly by adding Low Pass, High Pass and inverting Band Pass, the All Pass response can be obtained. It may be mentioned here that one may require additional devices for carrying out these additions.

(iv) The most important feature of the KHN Biquad is the ability to tune the various parameters of the biquad namely the gain, bandwidth, quality factor and the pole frequency independently.

The general second order (or biquadrates) filter transfer function is usually expressed in the standard form

$T(s) = \dfrac{a_2 s^2 + a_1 s + a_0}{s^2 + (\dfrac{\omega_0}{Q})s + \omega_0{}^2}$, ω_0 is known as the pole frequency and Q is known as the pole quality factor.

5.2 General KHN Biquad block

Fig71 shows the general KHN Block Diagram

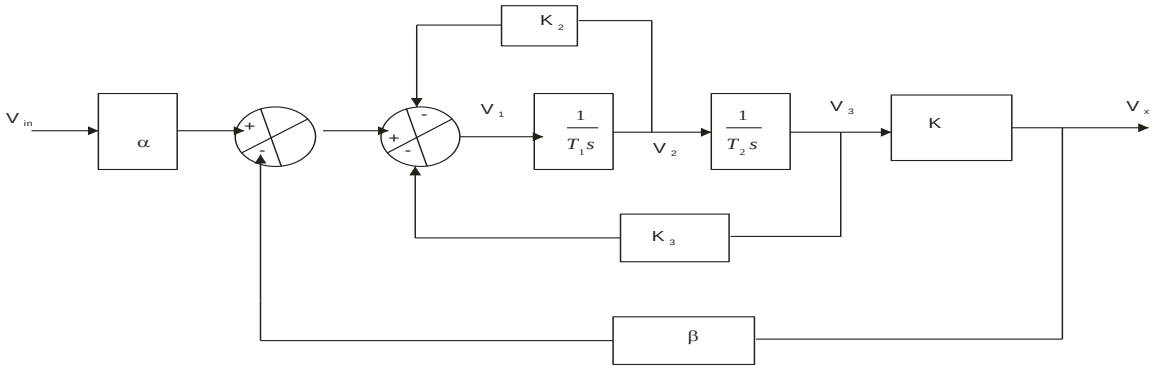


Fig71: General KHN Block

$$V_1 = \alpha V_{in} - \beta V_x - K_2 V_2 - K_3 V_3 \quad \text{..... (1)}$$

$$V_2 = \tfrac{1}{T_1 s} V_1 \ldots V_3 = \frac{V_2}{T_2 s} = \frac{V_1}{T_1 T_2 s^2} \quad \text{..... (2)}$$

$$V_3 = \frac{V_2}{T_2 s} = \frac{V_1}{T_1 T_2 s^2} \quad \text{..... (3)}$$

$$Vx = KV_3 = \frac{KV_1}{T_1 T_2 s^2} \quad \text{..... (4)}$$

Substituting values of (2),(3) and (4) in equation (1), we get

$$V_1 = \alpha Vin - \frac{\beta K V_1}{T_1 T_2 s^2} - \frac{K_2 V_1}{T_1 s} - \frac{K_3 V_1}{T_1 T_2 s^2} \quad \text{..... (5)}$$

$$V_1[1 + \frac{\beta K}{T_1 T_2 s^2} + \frac{K_2}{T_1 s} + \frac{K_3}{T_1 T_2 s^2}] = \alpha Vin \quad \text{..... (6)}$$

$$V_1[T_1 T_2 s^2 + \beta K + K_2 T_2 s + K_3] = T_1 T_2 s^2 \alpha V_{in} \quad \text{..... (7)}$$

$$V_1 = \frac{\alpha T_1 T_2 s^2 Vin}{[T_1 T_2 s^2 + K_2 T_2 s + (K_3 + \beta K)]}$$

This is the transfer function of high pass filter.

$$V_2 = \frac{\alpha T_2 s Vin}{[T_1 T_2 s^2 + K_2 T_2 s + (K_3 + \beta K)]}$$

This is the transfer function of band pass filter

$$V_3 = \frac{\alpha Vin}{[T_1 T_2 s^2 + K_2 T_2 s + (K_3 + \beta K)]}$$

This is the transfer function of low pass filter. Thus we obtain three filter functions simultaneously using a single block diagram.

5.3 KHN Biquad using VDBAs

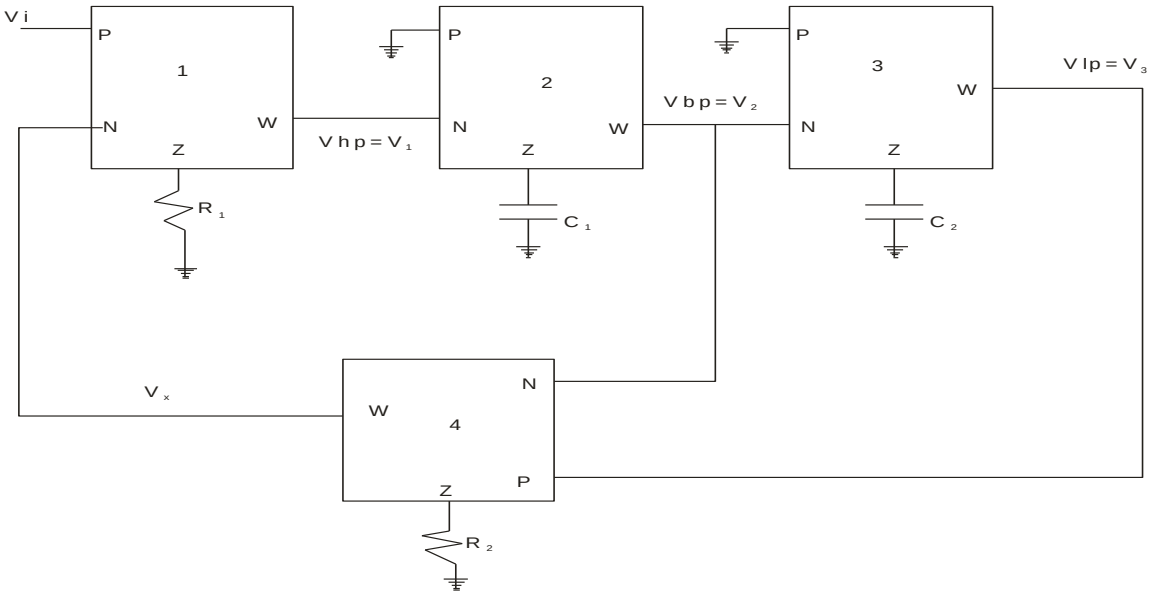
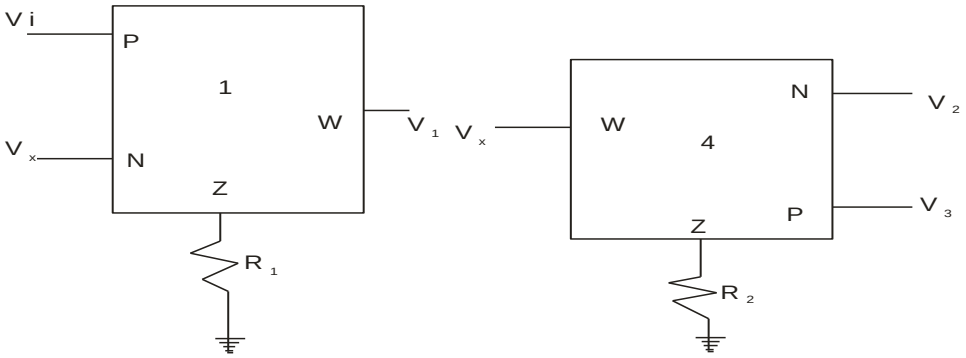


Fig72 KHN Biquad using VDBA blocks



$$V_1 = g_{m_1}\alpha_1 R_1 (V_i - V_x)$$

……. (8)

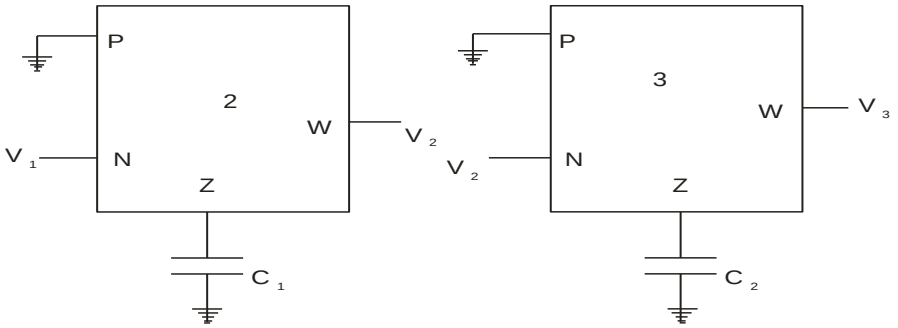
$$V_x = g_{m_4}\alpha_4 R_2 (V_3 - V_2)$$

…….... (9)

From equations (8) and (9), we get

$$V_1 = g_{m_1}\alpha_1 R_1 V_i - g_{m_1}\alpha_1 R_1 V_x = g_{m_1}\alpha_1 R_1 V_i - g_{m_1}\alpha_1 R_1 g_{m_4}\alpha_4 R_2 (V_3 - V_2)$$

$$= g_{m_1}\alpha_1 R_1 V_i - g_{m_1} g_{m_4}\alpha_1\alpha_4 R_1 R_2 V_3 + g_{m_1} g_{m_4}\alpha_1\alpha_4 R_1 R_2 V_2 \text{ …….. (10)}$$



$$V_2 = -\frac{g_{m_2}\alpha_2 V_1}{sC_1} \text{ …….. (11)}$$

$$V_3 = -\frac{g_{m_3}\alpha_3 V_2}{sC_2}$$

…… (12)

From equations (11) and (12)

$$V_3 = -\frac{g_{m_3}\alpha_3}{sC_2}\left(-\frac{g_{m_2}\alpha_2 V_1}{sC_1}\right) = \frac{g_{m_3} g_{m_2}\alpha_3\alpha_2 V_1}{s^2 C_1 C_2} \text{ ……... (13)}$$

Now substituting equations (11) and (13) into (10), we get

$$V_1 = \frac{g_{m_1}\alpha_1 R_1 C_1 C_2 s^2 V_{in}}{s^2 C_1 C_2 + g_{m_1} g_{m_2} g_{m_4}\alpha_1\alpha_2\alpha_4 R_1 R_2 C_2 s + g_{m_1} g_{m_2} g_{m_3} g_{m_4}\alpha_1\alpha_2\alpha_3\alpha_4 R_1 R_2}$$

$$= \frac{g_{m_1}\alpha_1 R_1 s^2 V_{in}}{s^2 + \frac{g_{m_1}g_{m_2}g_{m_4}\alpha_1\alpha_2\alpha_4 R_1 R_2 s}{C_1} + \frac{g_{m_1}g_{m_2}g_{m_3}g_{m_4}\alpha_1\alpha_2\alpha_3\alpha_4 R_1 R_2}{C_1 C_2}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (14)$$

Equation (14) represents a High Pass Filter transfer function.

No using equations (11) and (14) we get

$$V_2 = -\frac{g_{m_2}\alpha_2 V_1}{sC_1} = \frac{\frac{g_{m_1}g_{m_2}\alpha_1\alpha_2 R_1}{C_1} sV_{in}}{s^2 + \frac{g_{m_1}g_{m_2}g_{m_4}\alpha_1\alpha_2\alpha_4 R_1 R_2 s}{C_1} + \frac{g_{m_1}g_{m_2}g_{m_3}g_{m_4}\alpha_1\alpha_2\alpha_3\alpha_4 R_1 R_2}{C_1 C_2}} \quad \ldots\ldots (15)$$

Thus equation (15) represents a Band Pass Filter Transfer function.

Now using equations (12) and (15) we get

$$V_3 = -\frac{g_{m_3}\alpha_3 V_2}{sC_2} = \frac{\frac{g_{m_1}g_{m_2}g_{m_3}\alpha_1\alpha_2\alpha_3 R_1}{C_1 C_2} V_{in}}{s^2 + \frac{g_{m_1}g_{m_2}g_{m_4}\alpha_1\alpha_2\alpha_4 R_1 R_2 s}{C_1} + \frac{g_{m_1}g_{m_2}g_{m_3}g_{m_4}\alpha_1\alpha_2\alpha_3\alpha_4 R_1 R_2}{C_1 C_2}} \quad \ldots\ldots (16)$$

Thus equation (16) represents a Low Pass Filter transfer function.

We know that the general second order transfer function of a high pass filter is written as

$$V_o = \frac{Ks^2}{s^2 + s(\frac{\omega_0}{Q}) + \omega_0{}^2} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (17)$$

Where K represents high frequency gain, ω_0 represents pole frequency and Q represents quality factor. By comparing equations (14), (15), and (16) with (17) we can get values of pole frequency and quality factor. Also from these equations we observe that pole frequency; gain and quality factor can be adjusted by varying trans-conductance and voltage ratios of different VDBAs. The values of trans- conductance gain and voltage ratio is controlled by bias voltages and hence we can control the gain, pole frequency and

quality factor by bias voltages. The external resistances and capacitances can also control the three parameters.

Filter	ω_0	$\frac{\omega_0}{Q}$	**K**
HPF	$\sqrt{\frac{g_{m1}g_{m2}g_{m3}g_{m4}\alpha_1\alpha_2\alpha_3\alpha_4R_1R_2}{C_1C_2}}$	$\frac{g_{m1}g_{m2}g_{m4}\alpha_1\alpha_2\alpha_4R_1R_2}{C_1}$	$g_{m1}\alpha_1R_1$
BPF	$\sqrt{\frac{g_{m1}g_{m2}g_{m3}g_{m4}\alpha_1\alpha_2\alpha_3\alpha_4R_1R_2}{C_1C_2}}$	$\frac{g_{m1}g_{m2}g_{m4}\alpha_1\alpha_2\alpha_4R_1R_2}{C_1}$	$\frac{1}{g_{m4}\alpha_4R_2}$
LPF	$\sqrt{\frac{g_{m1}g_{m2}g_{m3}g_{m4}\alpha_1\alpha_2\alpha_3\alpha_4R_1R_2}{C_1C_2}}$	$\frac{g_{m1}g_{m2}g_{m4}\alpha_1\alpha_2\alpha_4R_1R_2}{C_1}$	$\frac{1}{g_{m4}\alpha_4R_2}$

It is thus seen that bandwidth and pole frequency can be tuned independently while the specifications on the gain parameter can be met either as upper bound or lower bound.

Now consider that if all of the four VDBAs are same then we can assume that

$g_{m_1} = g_{m_2} = g_{m3} = g_{m_4} = g_m, \alpha_1\alpha_2\alpha_3\alpha_4 = \alpha$ and we also take $R_1 = R_2 = R, C_1 = C_2 = C$

$$V_1 = \frac{g_m\alpha Rs^2}{s2 + \frac{{g_m}^3\alpha^3R^3s}{C} + \frac{{g_m}^4\alpha^4R^2}{C^2}}Vin \quad \text{..... (18)}$$

Now comparing equations (17) and (18) we get the following values

$$\omega_0 = \frac{{g_m}^2\alpha^2R}{C}, Q = \frac{1}{g_m\alpha R}, \; K = g_m\alpha R$$

5.4 Simulation of KHN Biquad

The proposed KHN Biquad using four VDBAs was simulated using 0.35µm TSMC CMOS process. The result of simulations of VDBA has been given in chapter-3. For simulation we have used the following values:

$$V_{DD} = -V_{SS} = 1.5V, V_{B1} = -0.16V, V_{B2} = -0.14V,$$
$$g_{m1} = g_{m2} = g_{m3} = g_{m4} = 721\frac{\mu A}{V}, \alpha_1 = \alpha_2 = \alpha_3 = \alpha_4 = 0.84,$$
$$C_1 = C_2 = 200\,pF, R_1 = R_2 = 20K\Omega$$

The observation shown below shows the result of simulation of proposed KHN Biquad. The node 27 represents a low pass filter response, node 25 represents a band pass filter response and node 23 represents a high pass filter responses. All of these responses are available simultaneously. The given KHN Biquad was designed for operating frequency 2MHz

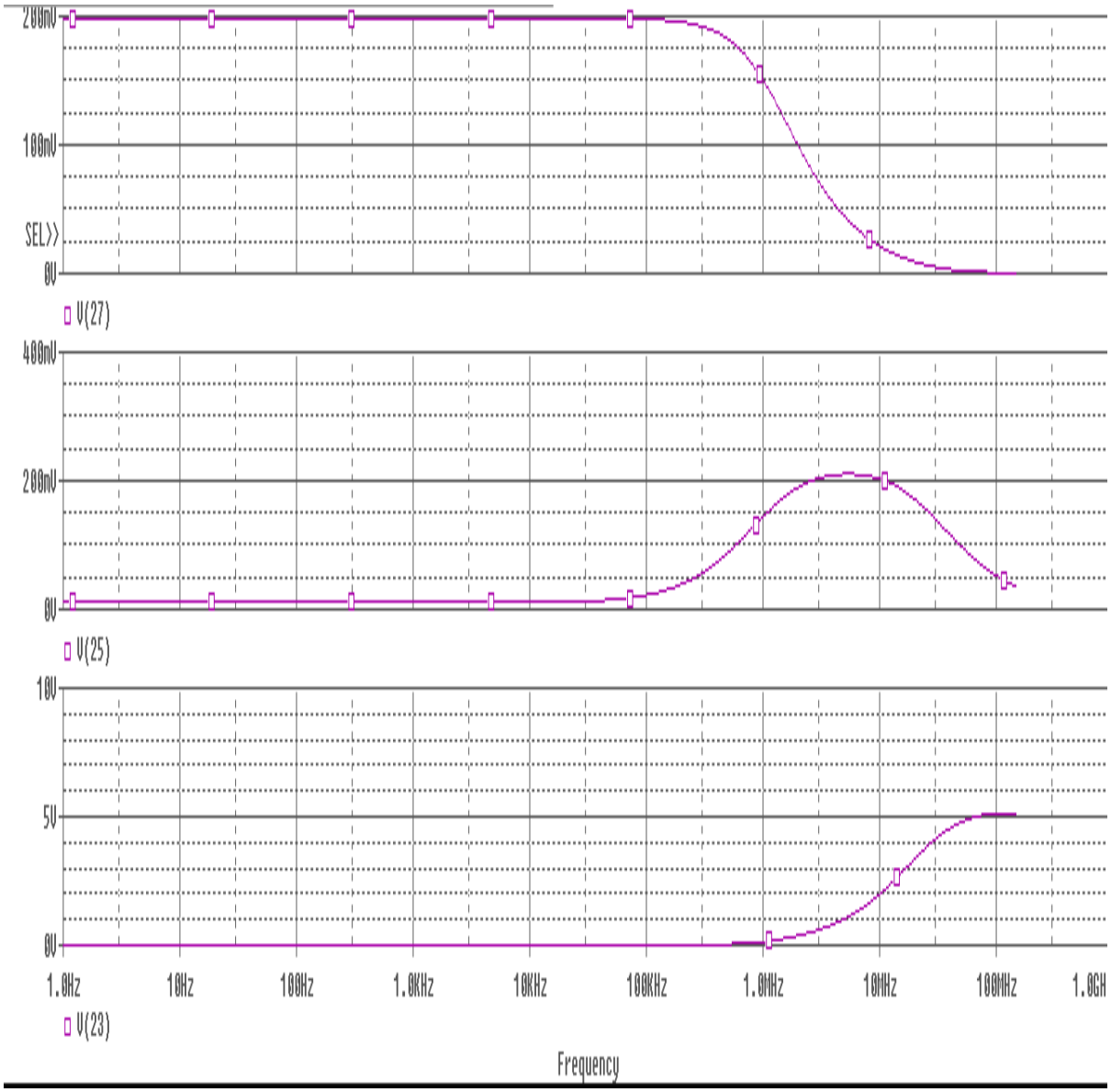


Fig73: AC response of KHN Biquad

The ac response of the low pass section of the proposed KHN is shown in fig74. The ac response was obtained by applying an ac signal of 0.5V. The transient response which is shown in fig75 was also obtained for the same by applying a sinusoidal signal of 0.1V and 1 KHz frequency.

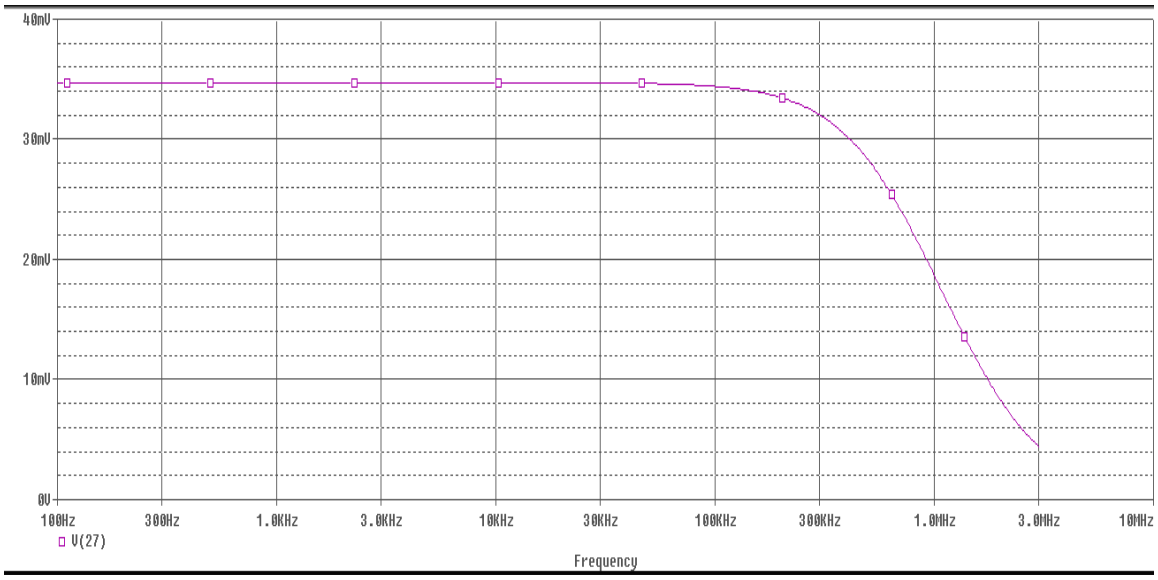


Fig74: AC responses of low pass section of KHN

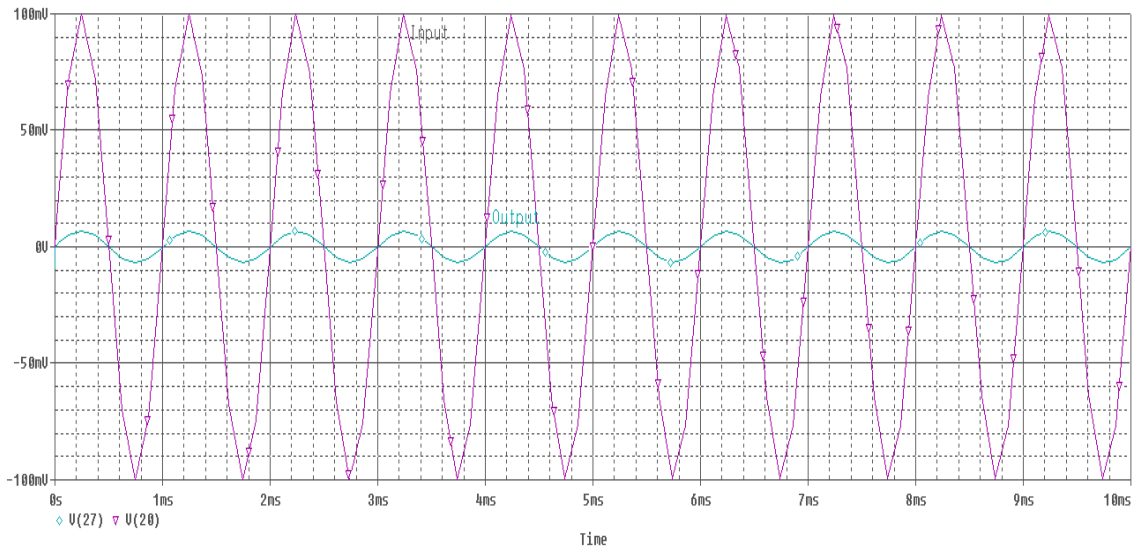


Fig75: Transient responses of low pass section of KHN

5.5 Conclusion

In the present chapter we have presented a voltage mode filter based on two integrator loop. The realized filter has properties similar to the classical KHN biquad. Analytical results showing the development has been presented. PSPICE simulations have confirmed the workability of the presented circuit.

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CHAPTER-6 ⟶

CONCLUSION & FUTURE SCOPE

1. Conclusion and Future Scope

The main objective of this dissertation was to study a new active building block called VDBA (Voltage Differencing Buffered Amplifier) which was proposed as an alternative to the existing CDBA (Current Differencing Buffered Amplifier), its CMOS realization, some of its applications and to study some of the already proposed applications.

VDBA can also be compared with voltage operational amplifier. Both of them have the same properties such as high input and low output impedances. Differential input voltage is transferred to current at the terminal z by trans-conductance gain and the voltage drop at the terminal z is mirrored in different impedance region, that is, terminal w. However, VDBA provides properties of current mode circuit such as greater bandwidth, lower power consumption, higher slew rate and wider linearity compared to Op-Amp. Furthermore, VDBA enjoys the features electronic tenability as the gain of the trans-conductance stage can be varied by changing the bias voltage (current).

The simplest application of VDBA is to build inverting and non inverting amplifiers. Both the amplifiers contain a single VDBA. A lossless as well as lossy integrator has also been explained. Both the integrators contain single VDBA along with a passive capacitor. Two voltage mode biquad filters have also being explained. Both of these circuits contain two VDBAs, two or three passive components and have three-inputs single output. The first proposed biquad filter contains two VDBAs and two capacitors and generates all filter functions(low pass(LP), band pass(BP), high pass(HP), band stop(BS) and all pass(AP),but this topology needs inverting type input voltage signal for the employed AP filters. The second proposed biquad filter employs two VDBAs, two capacitors and a resistor and realizes the all filter functions without the use of inverting input terminals. Furthermore, quality factor can be adjusted with resistor as independent natural frequency.

A state variable filter is a type of active filter. Any LTI system can be described as a state-space model, with n state variables for an nth-order system. A state variable filter realizes the state-space model directly. The instantaneous output voltage of one of the integrators in KHN corresponds to one of the state-space model's state

variables. We have used the basic two integrator loop topology to realize a biquad filter which used the VDBA based integrators and amplifiers.

VDBA is a recently proposed active building block and its applications in various signal processing functions are being explored currently by different researchers. Some of the areas in which the work presented in this dissertation can be extended are given below:

i) Realization of single resistance controlled oscillators in which the frequency of oscillation can be controlled electronically

ii) Realization of instrumentation amplifierswith very high electronically controllable CMRR

iii) CMOS and Bipolar realization of VDBA.

Thus there is enough scope of extending the work presented in this dissertation.

APPENDIX

0.35µmTSMC CMOS PROCESS

```
.MODEL NMOS1 NMOS (LEVEL=3 TOX=7.9E-9 NSUB=1E17
+GAMMA=0.5827871 PHI=0.7 VTO=0.5445549 DELTA=0
+UO=436.256147 ETA=0 THETA=0.1749684 KP=2.055786E-4
+VMAX=8.309444E4 KAPPA=0.2574081 RSH=0.0559398
+NFS=1E12 TPG=1 XJ=3E-7 LD=3.162278E-11 WD=7.046724E-8
+CGDO=2.82E-10 CGSO=2.82E-10 CGBO=1E-10 CJ=1E-3
+PB=0.9758533 MJ=0.3448504 CJSW=3.777852E-10
+MJSW=0.3508721)

.MODEL PMOS1 PMOS(LEVEL=3 TOX=7.9E-9 NSUB=1E17
+GAMMA=0.4083894 PHI=0.7 VTO=0.7140674 DELTA=0
+UO=212.231980 ETA=9.999762E-4 THETA=0.2020774
+ KP=6.733755E-5 VMAX=1.181551E5 KAPPA=1.5
+ RSH=30.0712458 NFS=1E12 TPG=1 XJ=2E-7 LD=5.00000E-13
+ WD=1.249872E-7 CGDO=3.09E-10 CGSO=3.09E-10
+CGBO=1E-10 CJ=1.419508E-3 PB=0.8152753 MJ=0.5
+CJSW=4.813504E-10 MJSW=0.5)
```

First Order Transfer Functions

S.N	Type of Filter	Transfer Function
1	Low Pass Filter	$\frac{a_0}{s+\omega_0}$
2	High Pass Filter	$\frac{a_1 s}{s+\omega_0}$
3	General	$\frac{a_1 s + a_0}{s+\omega_0}$
4	All Pass	$-a_1 \frac{s-\omega_0}{s+\omega_0}$, $a_1 > 0$

Second Order Transfer Functions

S.N	**Type of Filter**	**Transfer Function**
1	Low Pass Filter	$\frac{a_0}{s^2+s\frac{\omega_0}{Q}+{\omega_0}^2}$, DC Gain=$\frac{a_0}{{\omega_0}^2}$
2	High Pass Filter	$\frac{a_2 s^2}{s^2+s\frac{\omega_0}{Q}+{\omega_0}^2}$, High Frequency Gain=$a_2$
3	Band Pass Filter	$\frac{a_1 s}{s^2+s\frac{\omega_0}{Q}+{\omega_0}^2}$, Center frequency gain=$\frac{a_1 Q}{\omega_0}$
4	All Pass Filter	$a_2 \frac{s^2-s\frac{\omega_0}{Q}+{\omega_0}^2}{s^2+s\frac{\omega_0}{Q}+{\omega_0}^2}$, Flat gain=a_2