A DISSERTATION

On

Current Mode ADC using Current Differencing Transconductance Amplifier

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I wish him success in all his endeavours.

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ABSTRACT

This dissertation presents the implementation of a two bit flash analog-to-digital converter based on current-mode technique. The analog-to-digital converter presented here employs three current differencing transconductance amplifier (CDTA) based comparator ,a current mirror and a priority encoder. The advantages of current -mode technique are higher speed, lower power dissipation, and simple division of reference current based on current mirror. The new method allows effective and simple high-speed A/D conversion where the input is a current signal and the output is a digital voltage signal. By using this technique we have reduced the power dissipation and response time. This current mode method is highly accurate. The circuit has been simulated using the PSPICE simulator for .18 μ m CMOS technology with 1.8V supply to get satisfactory output.

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CHAPTER 1

Introduction

1.1 Background

The evolution of modern applications of analog signal processing has followed the trends of current mode processing, where signals representing the information being processed, are in the form of electric currents.

The need for low-voltage low power circuits is immense in portable electronic equipments. During the last few decades, the current mode processing has emerged as low voltage design technique for analog design and has become a viable alternative because of its inherent advantages over voltage mode circuits. In voltage mode circuits the minimum bias voltages depend on the threshold voltages of the MOSFETs whereas in current mode circuits the current decides the circuit operation and enables the design of system that can operate over wide dynamic range. Higher bandwidth, very low operating voltage, greater linearity, higher slew rate low power consumption, and simple architecture as compared to voltage mode circuits are the key advantages offered by current mode processing .

Due to the advantages offered by current mode processing it is becoming an alternative design technique for the development of high performance analog circuits and systems. The maturity of current mode signal processing is seen from the development of systems based on the current mode approach. A wide spectrum of applications includes important areas such as data acquisition and processing, testing, filter design, general analog interfacing and image sensory processing.

Advances in current mode processing has given way to the development of variety of current processing active analog building blocks (ABB) and current differencing transconductance amplifier (CDTA) is one such ABB.

With the development of current-mode applications, the mixed-mode circuits are also analyzed because of the necessity of optimizing the interface between the sub-blocks, which are working in different modes.

Current comparator is an essential building block of a current mode analog to digital converter (ADC) which compares two input currents and gives a corresponding binary output voltage.The design of current mode comparator is a relatively new area of research and the range of application of current mode comparators is very wide. The comparator is then used in current mode flash ADC converter which has characteristics of high speed, high resolution, and low power dissipation.

1.2 Research Goals

The focus of this thesis is to present the design and implementation of Current Mode Analog to Digital Converter using CDTA and evaluate the performance characteristics of the proposed design.

The current comparator is designed using CDTA.This current comparator along with current mirror and priority encoder, is further used in implementation of a 2-bit Flash type ADC. The performance characteristics of the ADC are evaluated. The workability of the proposed design is verified through SPICE simulations.

1.3 Thesis Organization

In this thesis design of a CDTA based current mode analog to digital converter is presented.The organization of the proposed work is presented in this section.

Chapter 2 presents the background of current comparator and realization of CDTA block. This CDTA block is further used to design a current comparator. The CDTA and the curent comparator are also simulated to get a qualitative idea of their performance. Then the proposed current comparator presented and their behavior is discussed.

Chapter 3 current mirror are discussed. Current mirror are common analog circuit which are a basic part of many application like data converters, current adder/subtractor , biasing circuits etc. For conceptual purpose, the simple current mirror is explained and latter the regulated cascade current which is reported to have good current mirroring capabilities. The design of purposed current mirror is simulated.

Chapter 4 The design and implementation of priority encoder is explained . The Priority encoder circuit is implemented and its transient analysis is performed to check the operation.

Chapter5 Common analog to digital converter architectures are discussed followed by description of area speed efficient ADC architecture. Then the purposed Analog to digital converter is implemented and simulation were carried out to measure its performance.

Chapter 6 Presents the conclusions and summarizes the research work done in the thesis .

Chapter 2

Current Comparators using CDTA

2.1 Introduction

Current comparator perform comparison between two input currents and give binary output voltage depending on which input current is greater . One of the two input currents is a constant and is known as the reference current. Current comparators play an important role in current mode function generation, data converters etc. The advantage of current mode circuits are such as larger dynamic range, higher signal bandwidth, greater linearity, simpler circuitry, low power consumption, higher slew rate.

Current comparators also lead to reduction in circuit area. This is because many sensors outputs signal in the form of current and a current comparator eliminates the need for current to voltage converter. Because of its advantages the current comparator is a key element of analog and mixed signal processing

2.2 Basic Concepts

The current comparator accepts two input currents (Iin1 and Iin2) and provides an output signal (voltage or current) which in binary form represents the case where Iin1>Iin2 than the output is 1 in Iin1<Iin2 represent the output is 0.

The functionality of current comparator can be represented as:

$$V_{out} = \begin{pmatrix} 1, I_{in1}(t) > I_{in2}(t) \\ 0, I_{in1}(t) < I_{in2}(t) \end{pmatrix} \qquad (2.1)$$

This representation of the comparator acts as a transimpedance structure. Fig.2.1 shows the ideal current comparator transfer characteristics for voltage codification. EOL and EOH in this figure

denote the boundary values for the output logical states meaning that has two states 0 or 1. The x-axis Iin denotes the input difference current[1].

Fig.2.1 shows the ideal current comparator transfer characteristics for voltage codification. EOL and EOH in this figure denote the boundary values for the output logical states; Fig.2.2 shows the ideal comparator transient response. These figures illustrate the ideal current comparator features: **a)** infinite transimpedance in the transition region; **b)** zero offset; and **c)** zero delay. Also, to reduce loading errors due to finite output resistance of the driving source, the input voltage of an ideal current comparator should be kept constant for the full range of input current. Finally, all these characteristics should hold true for the largest possible input current range[1].

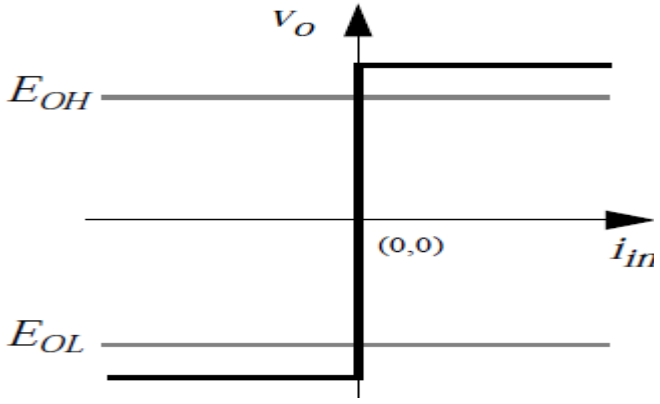

Fig.2.1 Ideal current comparator operation: Transfer characteristics

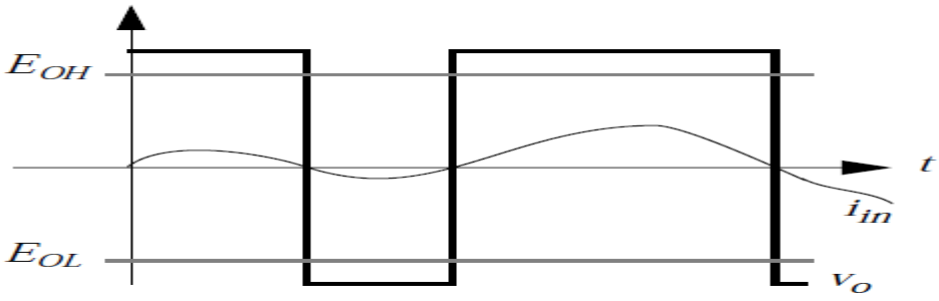

Fig.2.2 Ideal current comparator operation: Transient response

Practical circuit performance deviates from these ideal features, and is characterized by a set of static and dynamic specification parameters, among which the most significant for design are:

- Offset (Ios), defined as the input current required to annul the output voltage,
- Gain error(Δ) or static resolution, defined as the input increase needed to drive the output voltage from EOL to EOH; any input level larger than static resolution is called an overdrive,
- Resolution time (TR), defined as the time required for the output to change from 0 up to EOH (or down to EOL).
- Response time (TD), defined as the time required for the output to change between the two logical states.

2.3 CDTA based current comparator

In this work the current comparator has been designed using CDTA block. This requires an understanding of CDTA block. This section presents the terminal characteristics of a CDTA block which is followed by its CMOS realization presented in [3]. The CMOS realization of CDTA [2] is used for further implementation of CDTA based current comparator.

2.3.1 Current Differencing Transconductance Amplifier (CDTA)

CDTA is a five terminal current-mode active building block[3]. It can be also seen as a current operational amplifier if the intermediate z terminal is not taken outside. Its symbol is in Fig. 2.5 and defining equations are given below .

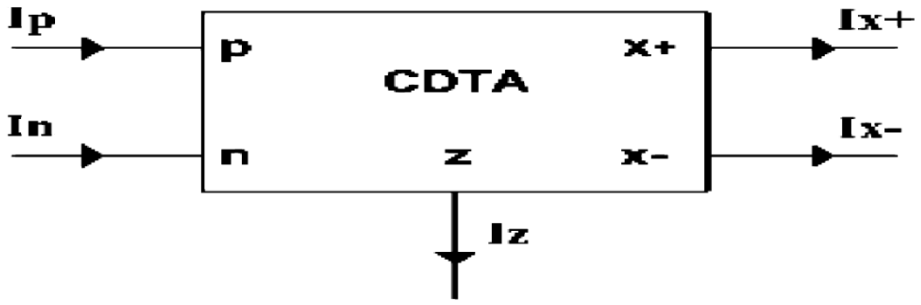

Fig. 2.3 Symbol of the CDTA element

$$V_p = V_n = 0 \tag{2.2}$$

$$I_z = I_p - I_n \tag{2.3}$$

$$I_x = g_m V_z = g_m Z_z I_z \tag{2.4}$$

The proposed symbol of CDTA is in Fig. 2 .3 is given a possible implementation of CDTA. Marking the voltages of *p*, *n*, *x*, and *z* terminals in Fig. 2 .3 with symbols *Vp*, *Vn*, *Vx*, and *Vz*, then for the CDTA+- element the following equations are true:

$$\begin{bmatrix} I_z \\ I_{x+} \\ I_{x-} \\ V_p \\ V_n \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 1 & -1 \\ g & 0 & 0 & 0 & 0 \\ -g & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_z \\ V_{x+} \\ V_{x-} \\ I_p \\ I_n \end{bmatrix} \tag{2.5}$$

Differential input current flows over the z terminal. Usually,an external impedance is connected to this node and the voltage over this impedance is converted to the output currents by the output transconductors with transconductance g for the positive output and $-g$ for the negative output. Intermediate z terminal of the CDTA can be very handy if a circuit is to be designed with all grounded passive elements which is good in view of process-dependent realization issues. Since input differential current flows over that z terminal it is possible to use one or more than one grounded passive elements to convert this differential current to voltage which seems a very promising method to obtain compact designs.

CMOS realization of CDTA[6]

Current Differencing Transconductance Amplifier is realize using 27 MOS transistor. In CDTA structure each mos have different W/L aspect ratio. In MOS structure of CDTA we use ± 1.8 V supply voltage . cdta have five node p,n,z,x+, and x-, p and n terminal are the input terminal on this terminal we apply current. On z terminal we get the difference of current of p and n terminals . The x terminal saturates at the supply voltage of this circuit . Fig.2.4 represent the MOS structure of CDTA.

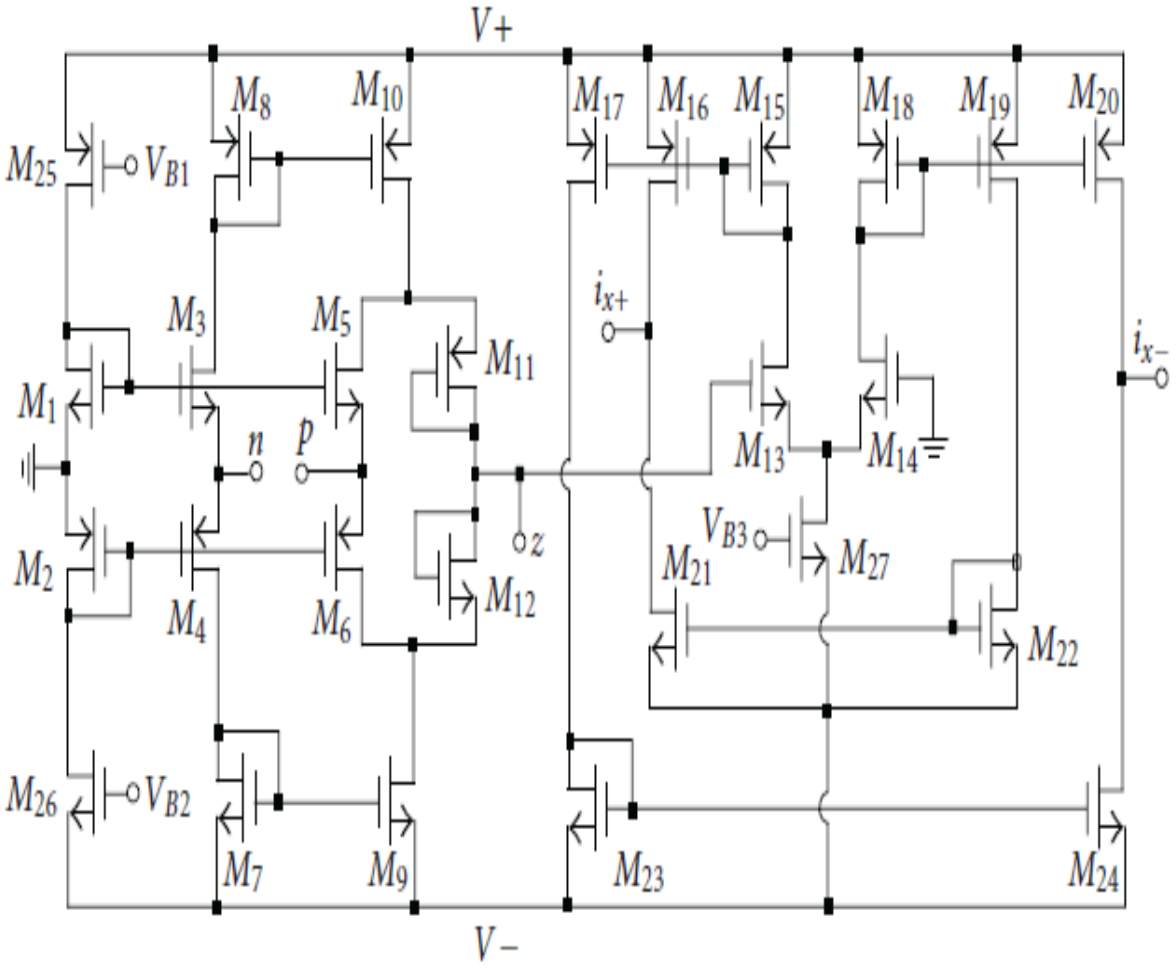

Fig.2.4 CMOS-based CDTA.

Aspect ratios of the Of the MOS transistor used in CDTA block shown in Fig. 2.4 are listed in table 2.1

Table 2.1 Aspect ratio MOS transistors in CDTA

MOS transistors	Aspect ratio (W/L)
*M*1, *M*3, *M*5, *M*7, *M*9, *M*12, *M*21, *M*22, *M*23, *M*24, *M*26	27/1.8
*M*2, *M*4, *M*6, *M*8, *M*10, *M*11, *M*13, *M*14, *M*25, *M*27	*72*/1.8
*M*15, *M*16, *M*17, *M*18, *M*19, *M*20	63/1.8

2.3.2 CDTA based comparator

The current comparator circuits are the basic building block in non linear analog signal processing circuits and A/D converter. The main function of current comparator circuit is to distinguish the two currents and provide the output either positive or negative in digital form. The ideal current comparator has zero delay, infinite transimpedance in transition region and zero offset. Many comparator circuits are designed each having its own operation applications. However, there is still scope for improved and more efficient structures satisfying the basic performance criteria expected out of a current comparator.

We have employed a CDTA(Current Differencing Transconductance Amplifier) based current comparator. A Current Differencing Transconductance Amplifier is a five terminal anologue electronic device which can perform many analogue signal processing functions, in a similar manner as the op-amps. There are many current conveyor structures are implemented, the basic structure has five nodes p ,n, z, x+, and x-. In CDTA we basically apply current at terminal p and n. At node z it give the difference of current Ip and In. At node z we got current Iz. At x terminal we got a current of gmIz. At x terminal give a saturated voltage.

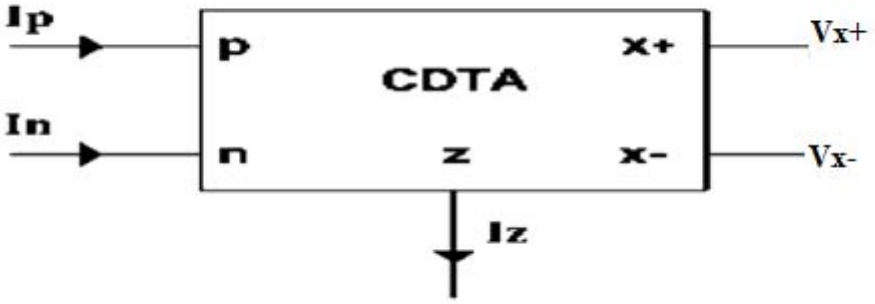

Fig.2.5 CDTA Comparator

When we apply a input current at the p and n. It give the diffence of signal at point z if the difference is positive than it give a positive voltage at point x+, if it is negative then it give a negative voltage.

$$I_z = I_p - I_n \tag{2.6}$$

$$Vx^+ = \pm Vsat \tag{2.7}$$

This Vx+ voltage used as the priority encoder input. This voltage act as like as digital input for the priority encoder.

2.4 Simulation Result

All simulation presented in this section were carried out in PSPICE with circuit implemented using 0.18µm CMOS technology at power supply voltage of 1.8V. The CDTA circuit work as a comparator. The current to be compared is given in p and n terminal of CDTA comparator shown in Fig. 2.5 z terminal gives the output current. If current at z terminal is positive, the output will be +Vsat at x+ terminal and If it is negative, the output will be –Vsat at x+ terminal.

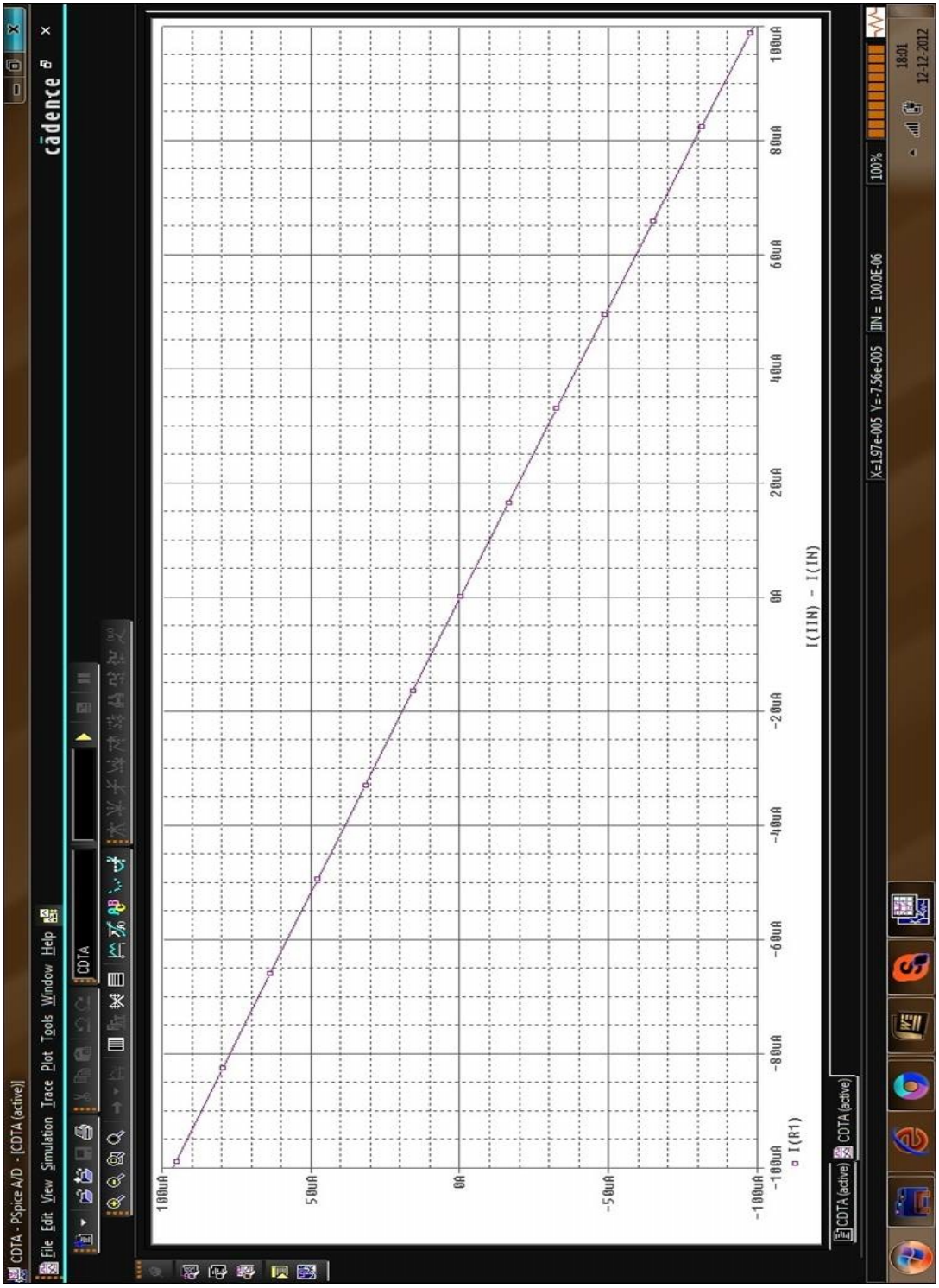

Fig. 2.6 CDTA circuit DC analysis

This is CDTA circuit characterstic that give the difference of (Ip-In) on Iz terminal. The range of cdta circuit is 100µA to – 100µA. The Iz current is ploted on Y axis .

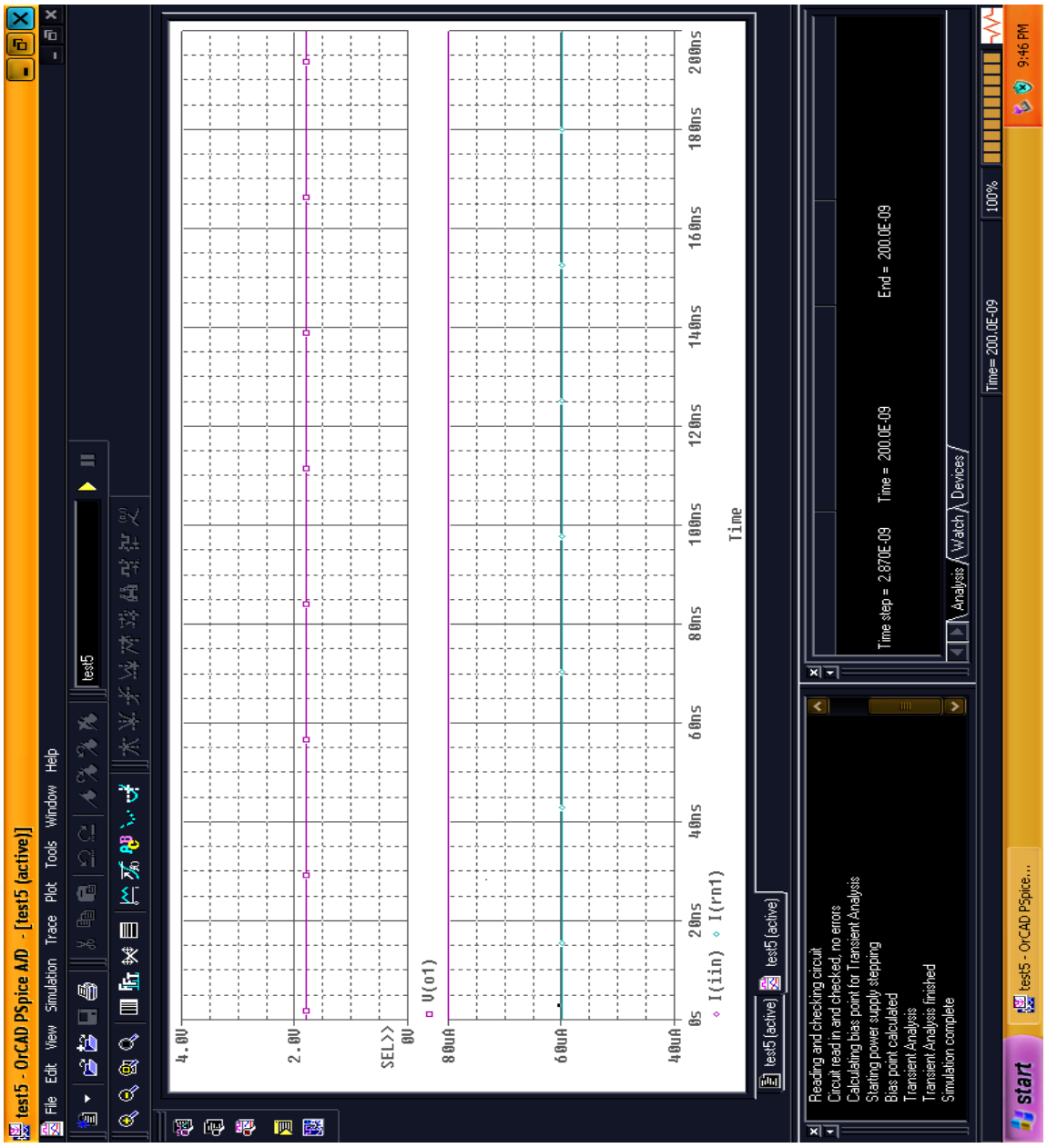

Fig.2.7 CDTA Circuit as Comparator Transient Analysis for logic 1

Simulation result with Ip=80µA, In=60µA.We get a high logic output. The output voltage is +1.8V.

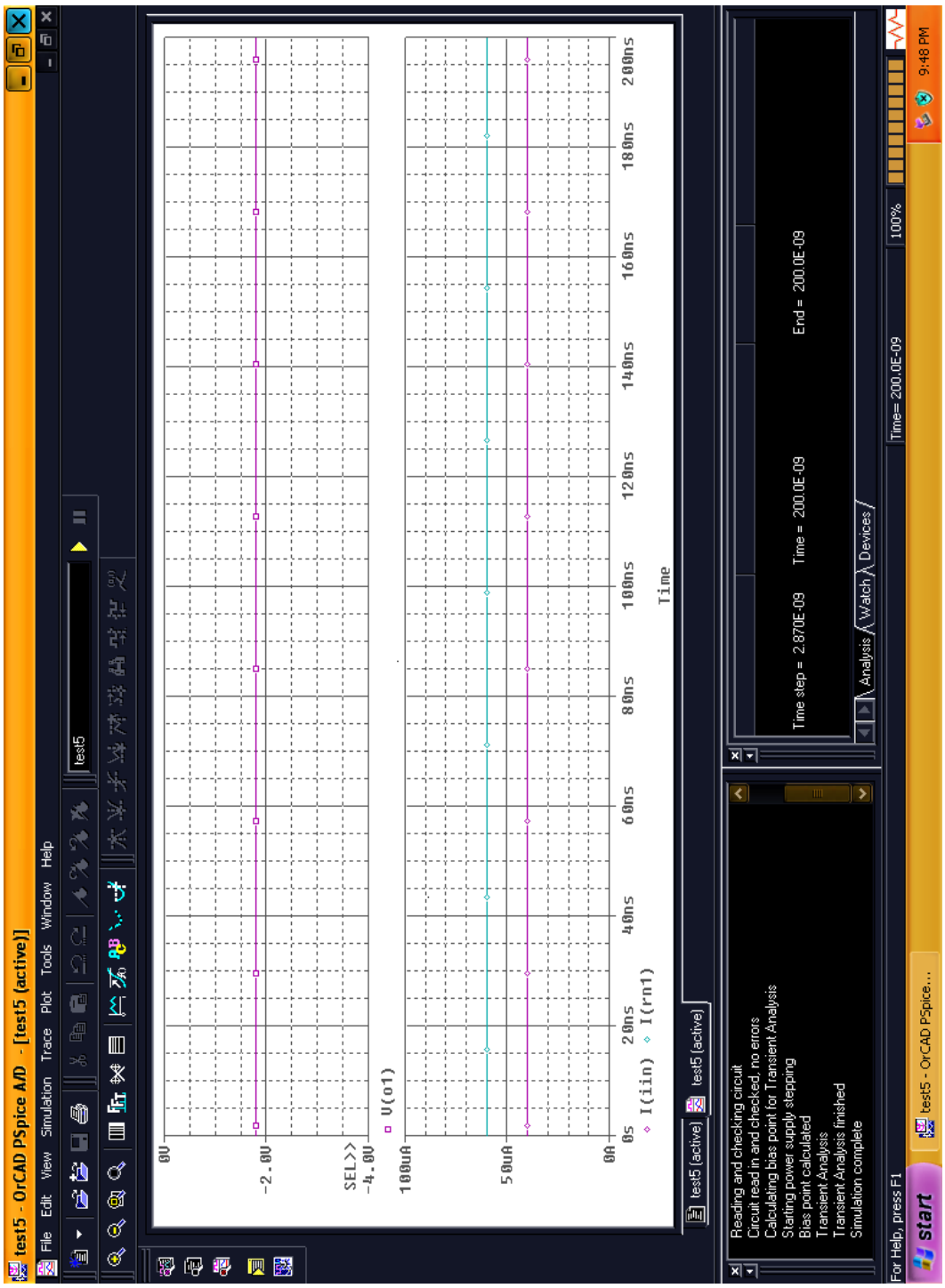

Fig.2.8 CDTA Circuit as Comparator Transient Analysis for logic 0

Simulation result with Ip=80µA, In=60µA.We get a high logic output. The output voltage is +1.8V.

Chapter 3

Current Mirrors

3.1 Introduction

In this chapter we discuss the current mirror circuit as they are an important part of current mode Analog to Digital convertor, which will be presented in chapter 5.

A two terminal circuit whose output current is independent of the output terminal voltage and depends only on the input current is called current mirror. Generally, it is used to generate a replica of given reference current. If necessary, it can also amplify or attenuate the reference current. A current mirror can be thought as a current controlled current source. Ideally, the output impedance of a current source/sink should be infinite and capable of generating or drawing a constant current over a wide range of voltages. However, finite value of output resistance and a limited output voltage required to keep device in saturation will ultimately limit the performance of the current mirror. Current mirror is used for biasing, loading, current amplification etc. Current mirrors are employed in many applications such as operational amplifiers, analog to digital and digital to analog converters.

Fig. 3.1 shows the symbols of current mirror circuits in which arrow is used to designate the direction of the current flow on the input side. The ratio 1: K represents the current gain of the mirror circuit. [4]

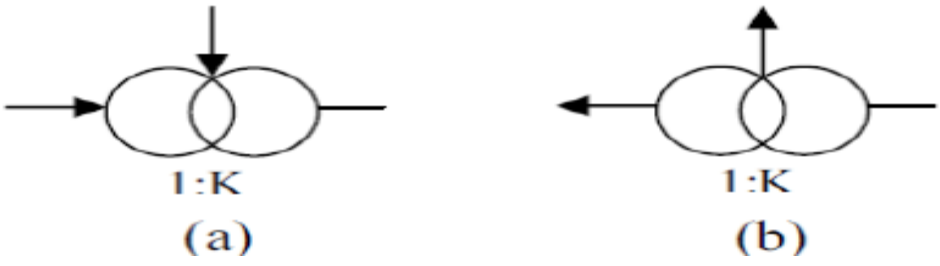

Fig. 3.1 Current Mirror Symbols (a) NMOS Current Mirror (b) PMOS Current Mirror

Current mirrors mimic the performance of an ideal current source. Therefore their designs must fulfill the following requirements. [4]

1.Input impedance should be zero.

2.Output impedance should be infinite.

3.Output current should be constant over wide swing of voltage

4.Accurate copy of input current.

3.2 Topologies of current mirror

3.2.1 Basic Current Mirror

3.2.2 Double Cascode Current Mirror

3.2.3 Triple Cascode Current Mirror

3.2.1 Basic Current Mirror

Fig.3. 2 shows the basic current mirror. A current flows through M1 corresponding to VGS1. Since VGS1 = VGS2, ideally the same current, or a multiple of the current in M1, flows through M2. If the MOSFETs are of the same size, the same drain current flows in each MOSFET, provided M2 stays in the saturation region[4]. The current through M1 can be given by,

$$I_{D1} = \frac{\beta_1}{2}(V_{GS1} - V_{THN})^2 \qquad (3.1)$$

The output current, assuming M2 in saturation is given by

$$I_{D2} = I_0 = \frac{\beta_2}{2}(V_{GS2} - V_{THN})^2 \qquad (3.2)$$

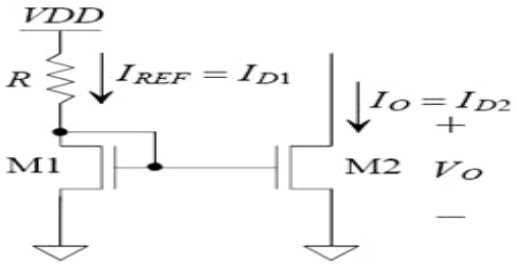

Fig. 3.2 Basic Current Mirror

Since VGS1=VGS2, the ratio of the drain currents is

$$\frac{I_{D2}}{I_{D1}} = \frac{\beta_2}{\beta_1} = \frac{\frac{W_2}{L_2}}{\frac{W_1}{L_1}} \qquad (3.3)$$

The desired output current can be obtained by adjusting W/L ratios of two devices.[4] Here it is required that M2 remains in saturation. Therefore the minimum output voltage across the current mirror is given by Vmin=VDS(SAT)=VGS-VTHN. The output resistance of current mirror is equal to output resistance of M2.

$$r_0 = \frac{1}{\lambda I_0} \qquad (3.4)$$

3.2.2Double Cascode Current Mirror

Double cascode configuration is used to increase the output resistance of a current source or sink. Fig.3. 3 shows schematic diagram for this configuration. If we define ΔV as excess gate-source voltage, the gate voltage of M4 is 2(ΔV+VTHN) and source voltage is ΔV+VTHN. The minimum voltage across the current sink is limited by the requirement that M4 remains in the saturation region. VDS4 ≥ VGS4 -VTHN or VD4 ≥ 2ΔV+VTHN [3]. This minimum voltage across the cascode current mirror is significantly larger than the minimum voltage across the basic current mirror.

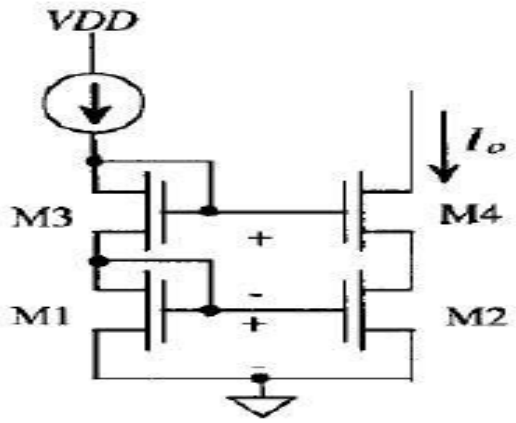

Fig.3. 3 Double Cascode Current Mirror

3.2.3 Triple Cascode Current Mirror

Output impedance can be further increased by adding one more stage to double cascode configuration [4]. Triple cascode configuration is shown in fig.3.4.

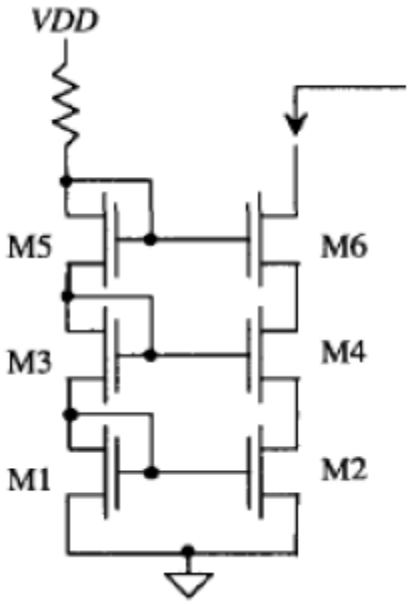

Fig.3.4 Triple Cascode Current Mirror

3.3 Current Mirror Structure used

In our current mode Analog to digital converter we require a three input current which is to be compared with the reference current.In our thesis basic simple current mirror configuration. As the input current I_{in} is to be compared with I_{ref} by each of the current comparators, it is required to generate replicas of I_{in} and progressively increasing values of I_{ref} as per proposed ADC structure.. This is achieved by using this current mirror circuit as shown in figure . In this current mirror circuit we generate a three o/p current I_{r1}, I_{r2},and I_{r3} and using one input current I_{in}. These output current is compare with the Iref current using CDTA based current comparator. The proposed current mirror circuit is shown in Fig.3.5.

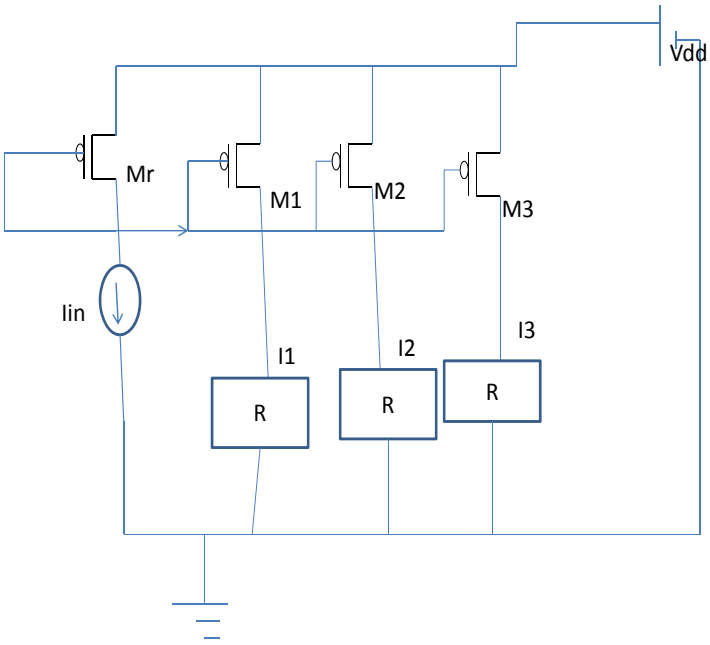

Fig.3.5 Current mirror structure

In aspect ratio of (5/1) is used for all the transistor in current mirror

3.4 Simulation Result

The simulation were carried out in PSPICE with circuit implemented using 0.18µm CMOS technology at power supply voltage of 1.8V. The output of current mirror i.e., replica of I_{in} is used as reference current for comparator.

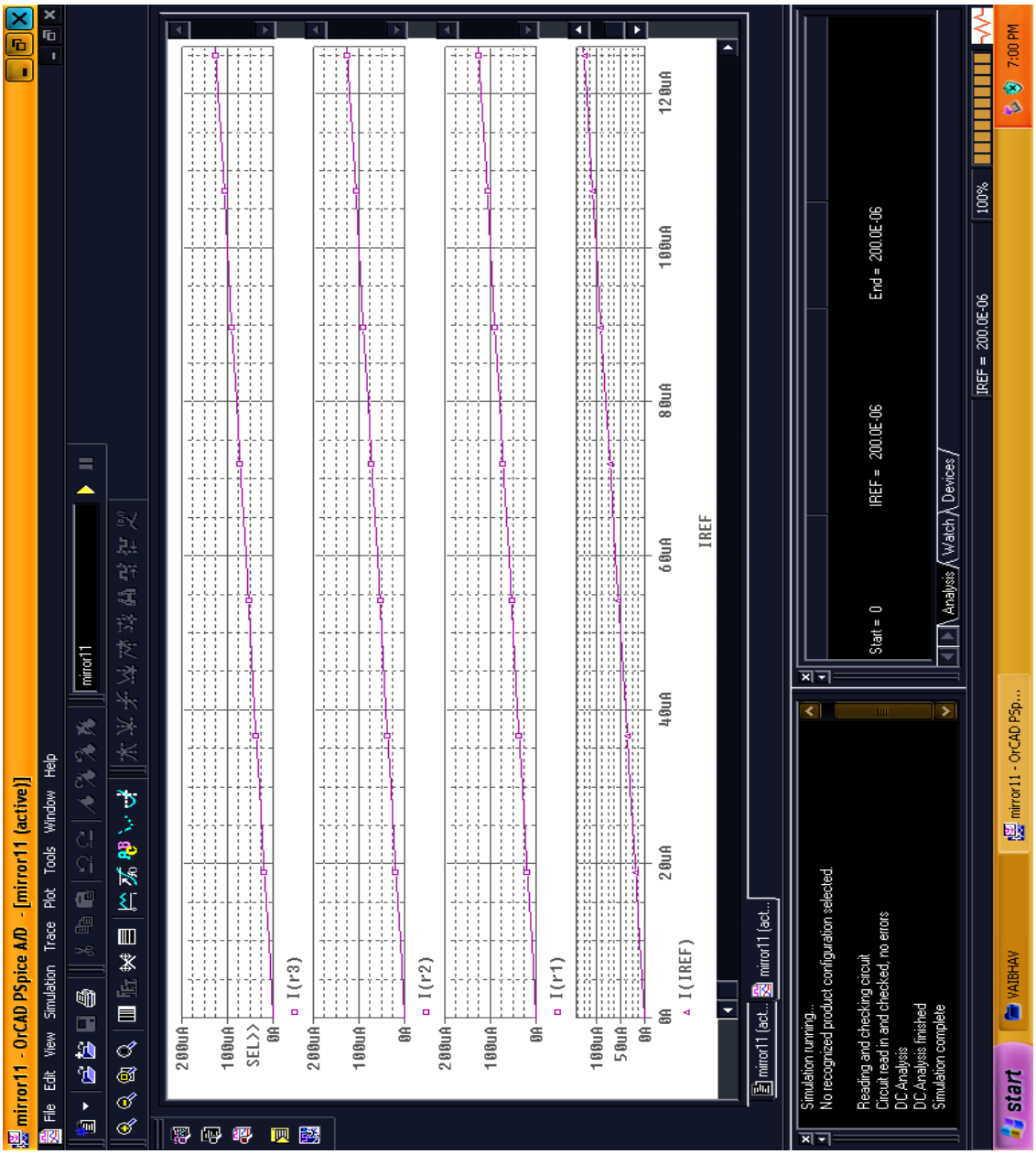

Fig 3.6 DC Analysis of current mirror circuit

I_{in} is the input current and I_{r1} ,I_{r2},and I_{r3} are the replica produced by the current mirror circuit.

Chapter 4

Priority Encoder

4.1 Introduction

In this chapter, we discuss priority encoder circuit as they are a part of analog to digital converter, Encoder circuit is used for binarization . The encoder circuit is designed for 2 bit ADC to produce 2 bit binary output.

An priority encoder is a circuit that convert information from one format or code to another. This is done due to requirement of standardization, security, speed or compression. The priority encoder can be realized various ways. Here a logic realization of ckt is selected.

4.2 Priority Encoder Circuit

The priority encoder circuit here works as a code converter converting comparator output to its binary equivalent. The structure of a 3 to 2 priority encoder is shown in Fig. 4.1. The truth table of the encoder is shown in table4.1

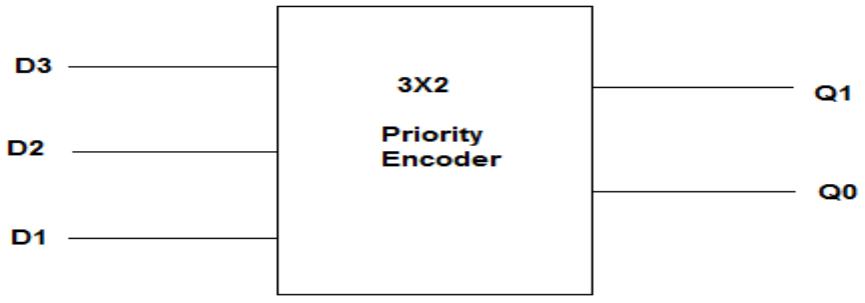

Fig. 4.1 priority encoder block diagram

Table 4.1Truth table of priority encoder

D_3	D_2	D_1	D_0	Q_1	Q_0
1	0	0	0	1	1
0	1	0	0	1	0
0	0	1	0	0	1

In this priority encoder D3 given highest priority as compared to D2 and D1. Where D2 have highest priority as compared to D1.The table show the output of priority encoder. The proposed priority encoder circuit is shown in given Fig.4.2

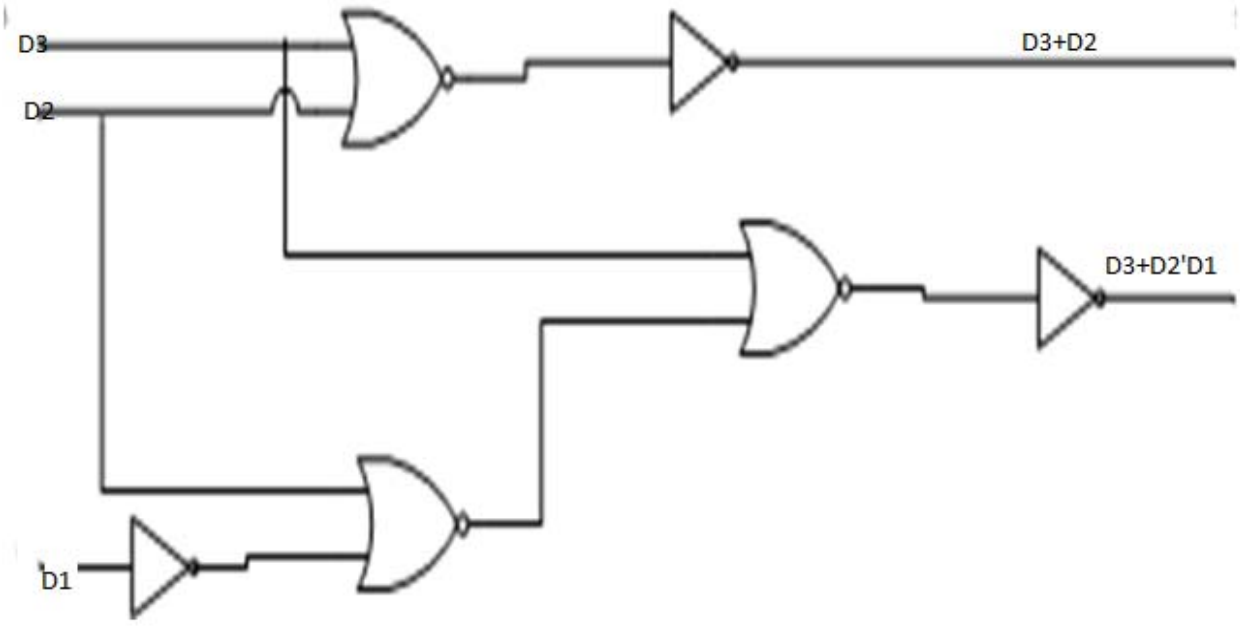

Fig. 4.2 Priority Encoder ckt. using logic gates

Minimizing the truth table using K map

$$Q0 = D3 + D2'D1 \qquad (4.1)$$

$$Q1 = D3 + D2 \qquad (4.2)$$

Equation (4.1) and (4.2) can be realized using Nor and Not gates as shown in Fig. 4.2

4.3 Simulation Results

In this section, the result of the transient analysis of the priority encoder is presented .The priority encoder is implemented using 0.18μm CMOS technology in PSPICE. The transient analysis ensures that highest priority for D3, then D2 and then D1.

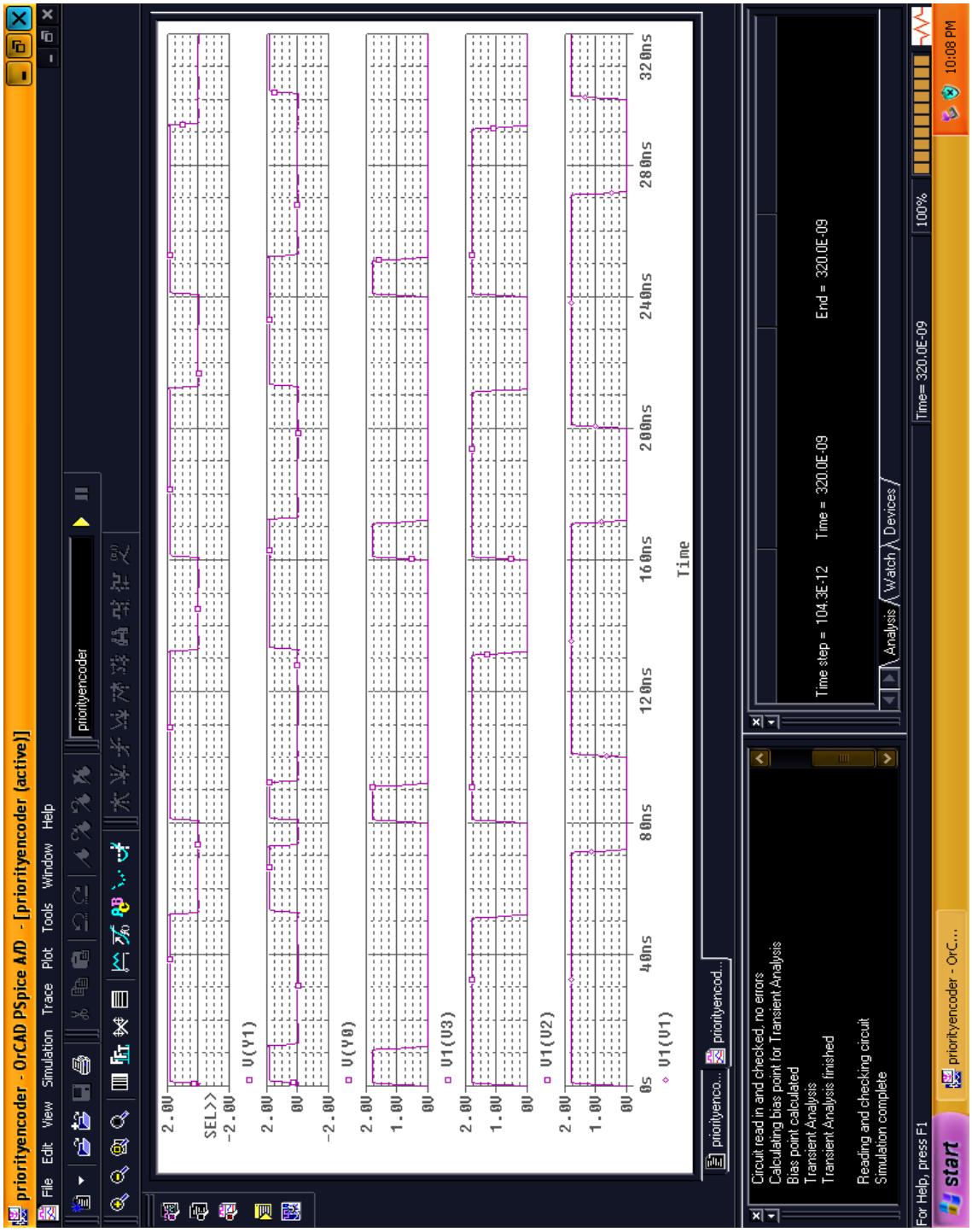

Fig. 4.3 Transient Analysis of priority encoder

Chapter 5

Analog to Digital Converter

5.1 Introduction

In this chapter the design of current mode 2 bit flash ADC using CDTA based current comparator is presented. An ADC is a circuit that accepts continuous infinite valued signal as the input, sample and quantizes it to output a digital signal. The ADC is designed and various parameters like Integral non linearity (INL) and Differential non linearity offset error resolution and SNR are calculated.

A current mode ADC has the following functional block:

1) Current Comparators using CDTA
2) Current Mirrors
3) Priority Encoder

The design and implementation of all the three components is presented in the previous chapters. In this chapter we present their integration into single circuit and the calculation of the parameters of ADC.

Section 5.2 describes the structures of different types of ADCs and their advantages and disadvantages are also presented. In section 5.3 we discuss the proposed current mode ADC structure. Section 5.4 presents the simulation result of proposed ADC. In section 5.5 parameters of ADC are calculated.

5.2 Types of ADC

Various ADC structures are as given below:

Successive-Approximation ADCs

Integrating ADCs: Dual Slope

Flash A/D Converter

SIGMA-DELTA A/D Converter

Pipelined ADC

5.2.1 Successive-Approximation ADCs

The basic successive approximation ADC is shown in Figure 5.1 It performs conversions on command [2]. On the assertion of the convert start command, the sample-and-hold (SHA) is placed in the hold mode, and all the bits of the successive approximation register (SAR) are reset to "0" except the MSB which is set to "1." The SAR output drives the internal DAC. If the DAC output is greater than the analog input, this bit in the SAR is reset, otherwise it is left set. The next most significant bit is then set to "1." If the DAC output is greater than the analog input, this bit in the SAR is reset, otherwise it is left set. If the output is less than analog input then MSB is same and next significant bit set to 1 The process is repeated with each bit in turn. When all the bits have been set, tested, and reset or not as appropriate, the contents of the SAR correspond to the value of the analog input, and the conversion is complete. These bit "tests" can form the basis of a serial output version SAR-based ADC.

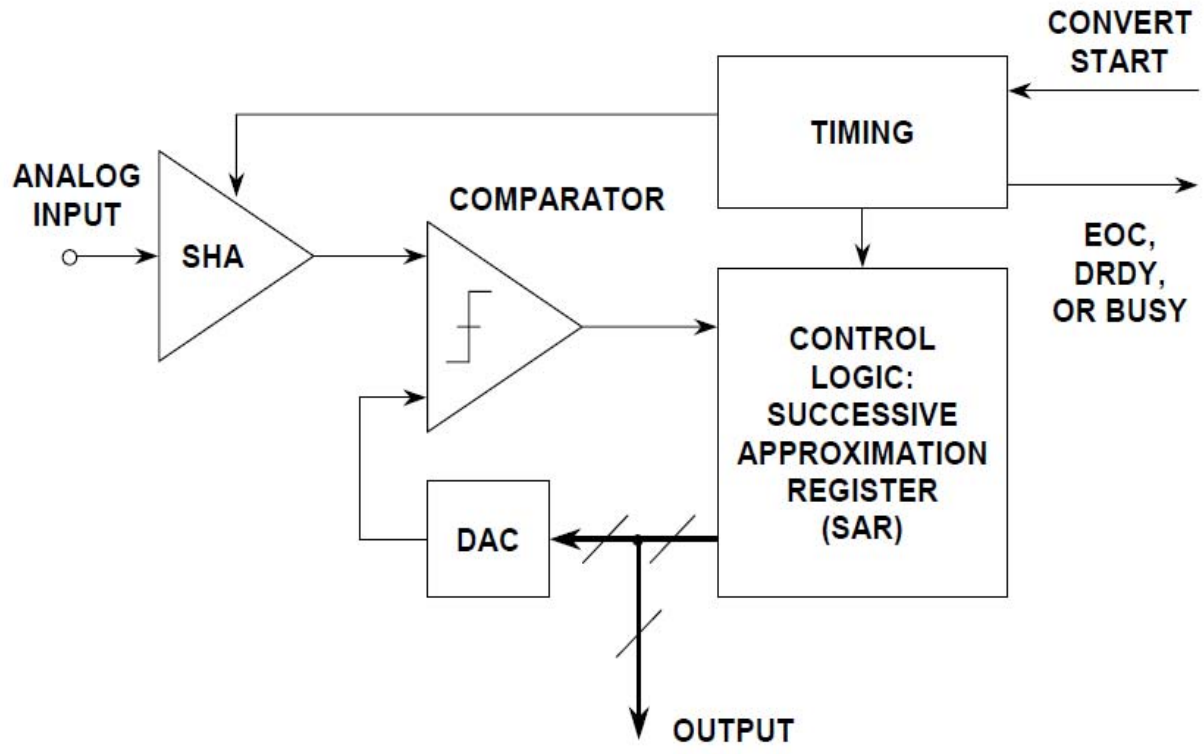

Fig.5.1 Successive-Approximation ADC

Advantage:-

1. Capable of high speed and reliable
2. Medium accuracy compared to other ADC types
3. Good tradeoff between speed and cost
4. Capable of outputting the binary number in serial (one bit at a time) format

Disadvantage:-

1. Higher resolution successive approximation ADC's will be slower

Speed limited to ~5Msps

5.2.2 Integrating ADCs: Dual Slope

The fundamental component of integrating dual slop ADC is Integrator, Electronically Controlled Switches, Counter, Clock, Control Logic, Comparator. These are the basic block for integrating dual slop comparator.

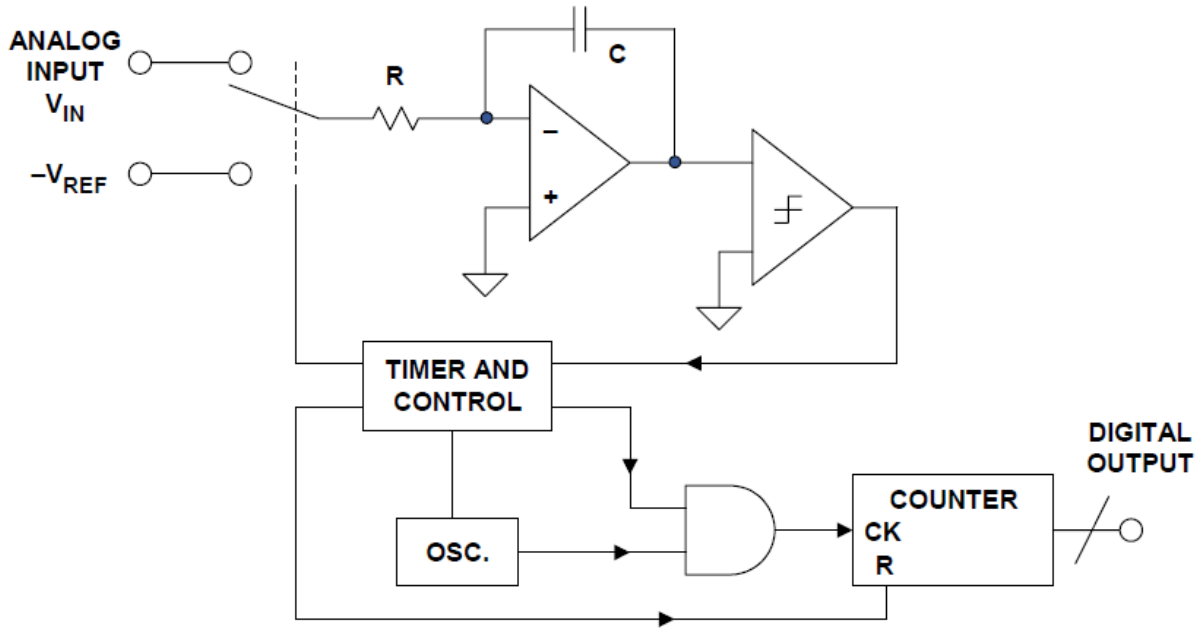

Fig 5.2 Dual slope A/D converter

An integrating A/D converter basically consists of an integrator and a counter. In this type of ADC no sample-and-hold is used, instead the output is an average of the input signal over a certain time period. First, the signal is integrated in a capacitor over a constant time period. Next, the capacitor is discharged at a constant rate and the counter measures the time it takes for the capacitor to discharge. The measured time is proportional to the signal amplitude if the signal is constant. For a time varying signal the measured time is proportional to the mean value of the signal during the measuring time. This kind of A/D converter can be made with high accuracy, but is quite slow. The integrating ADCs have a very simple structure which means that they are cheap, and the power consumption is low. Another advantage with the integrating ADC is that the integration time can be matched to reject for instance 50 Hz disturbances by integrating over an integer multiple of the disturbance period. Integrating A/D converters are used to measure slowly varying signals and DC signals. An integrating ADC typically has an integration time of around 1 ms up to 10 s, and the precision varies between 5 and 30 bits. Typical applications are digital multimeters and other applications where the information is presented on a display.

Advantage:-

1. Conversion result is insensitive to errors in the component values.
2. Fewer adverse affects from “noise”.
3. High Accuracy.

Disadvantage:-

1. Slow
2. Accuracy is dependent on the use of precision external components.
3. Cost

5.2.3 Flash A/D Converter

The fundamental component of Flash type Adc is comparator, resistor control logic, priority encoder.For N bit ADC we require $2^N - 1$ comparator and 2^N resistors.

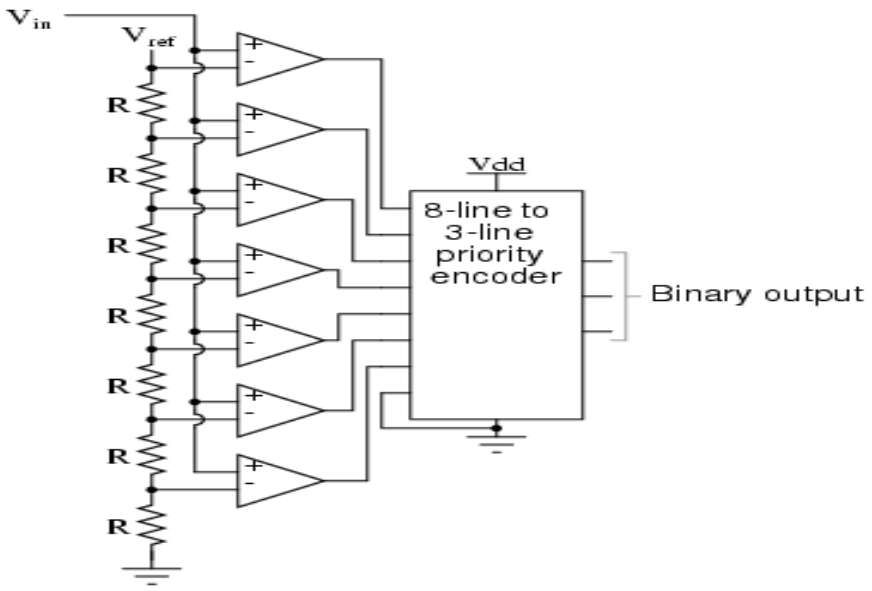

Fig 5.3 Flash ADC

Uses the 2^N resistors to form a ladder voltage divider, which divides the reference voltage into 2^N equal intervals. Uses the $2^N - 1$ comparators to determine in which of these 2^N voltage intervals the input voltage Vin lies. The Combinational logic then translates the information provided by the output of the comparators. This ADC does not require a clock so the conversion time is essentially set by the settling time of the comparators and the propagation time of the combinational logic.

Advantage:-

1. Very Fast (Fastest)
2. Very simple operational theory
3. Speed is only limited by gate and comparator propagation delay

Disadvantage:-

1. Expensive
2. Prone to produce glitches in the output.
3. Each additional bit of resolution requires twice the Comparator.

5.2.4 SIGMA-DELTA A/D Converter

The sigma-delta architecture takes a fundamentally different approach from the rest of the architectures [2]. Sigma-delta converters offer high resolution, high integration, and low cost, making them a good ADC choice for applications such as process control and weighing scales. Considerably less work has been done on Sigma-delta ADCs as compared to other architectures.

In its most basic form, a sigma-delta converter consists of an integrator, a comparator, and a single-bit DAC, as shown in Fig 5.4. The output of the DAC is subtracted from the input signal. The resulting signal is then integrated, and the integrator output voltage is converted to a single-bit digital output by the comparator. The resulting bit becomes the input to the DAC, and the DAC's output is subtracted from the ADC input signal, etc. This closed-loop process is carried out at a very high "oversampled" rate. The digital data coming from the ADC is a stream of ones and zeros, and the value of the signal is proportional to the density of digital ones coming from the comparator. This bit stream data is then digitally filtered and decimated to result in a binary-format output.

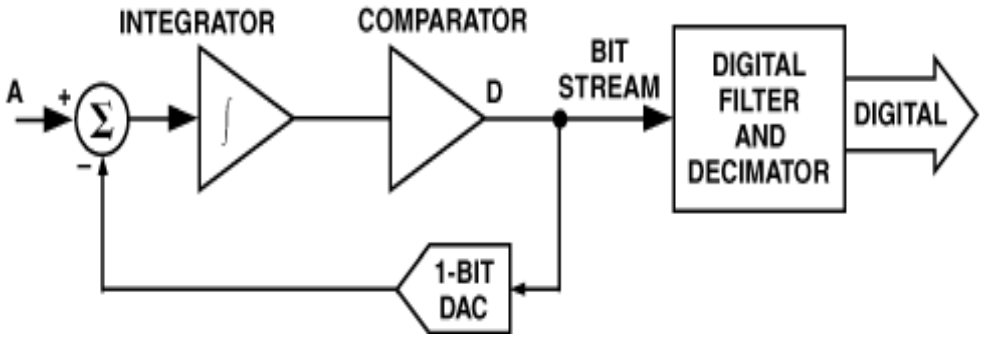

Fig 5.4 Sigma-delta ADC architecture

Advantage:-

1. High Resolution
2. No need for precision components

Disadvantage:-

1. Slow due to over sampling
2. Only good for low bandwidth

5.2.5 Pipelined ADC

The pipelined (or pipelined-flash) architecture, shown in Fig. 2.14, effectively overcomes the limitations of the flash architecture [2]. A pipelined converter divides the conversion task into several consecutive stages Each of these stages consists of a sample and hold circuit, an m-bit ADC (e.g. a flash converter), and an m-bit Digital to Analog converter (DAC). First the sample and hold circuit of the first stage acquires the signal. The m-bit flash converter then converts the sampled signal to digital data. The conversion result forms the most significant bit of the digital output. This same digital output is fed into the DAC, and its output is subtracted from the original sampled signal. The residual analog signal is then amplified and sent on to the next stage in the pipeline to be sampled and converted as it was in the first stage. This process is repeated through as many stages as are necessary to achieve the desired resolution. In principle, a pipelined converter with p pipelined stages, each with an *m*-bit flash converter, can produce a high-speed ADC with a resolution of n = *p***m* bits using $p*(2^m-1)$ comparators.

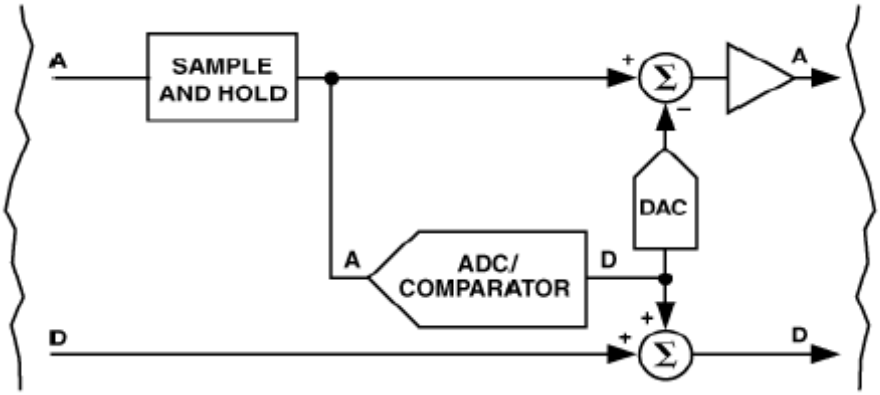

Fig.5.5 A Single Pipelined Converter Stage

Target applications for pipeline ADCs include communication systems, in which total harmonic distortion (THD), spurious-free dynamic range (SFDR), and other frequency-domain specifications are significant; CCD-based imaging systems, in which favorable time-domain specifications for noise, bandwidth, and fast transient response guarantee quick settling; and data-acquisition systems, in which time and frequency domain characteristics are both important. Fast and accurate N-bit conversions can be accomplished using at least two or more steps of pipelining.

5.3 Proposed ADC Structure

A 2 bit flash type ADC requires three comparators, a current mirror and a priority encoder. Fig.5.6 shows the proposed ADC structure.

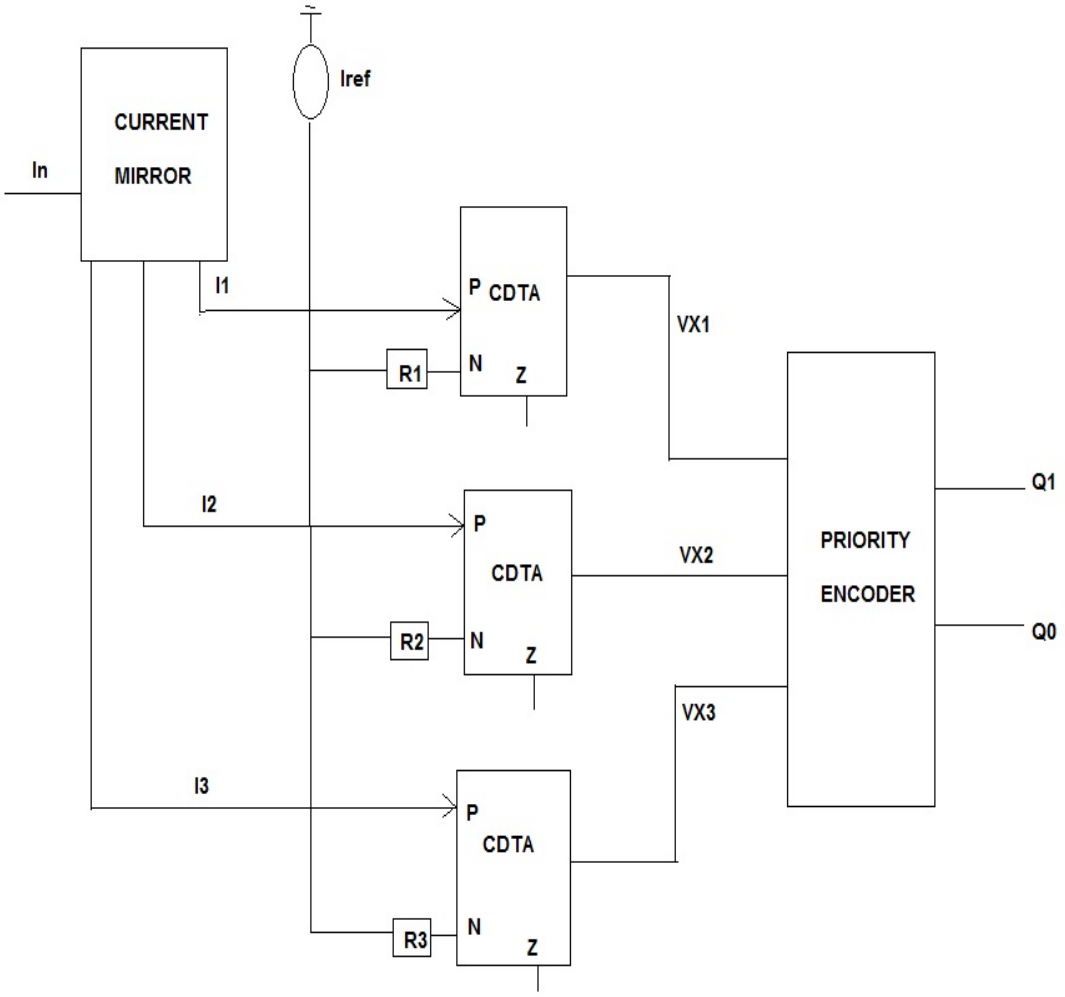

Fig. 5.6 Proposed Flash ADC module

In this ADC basically an input current I_{in} is given which can be converted into Digital. I_{in} is compared with the reference current. Our proposed ADC uses three current comparators and for all the three comparators one input is driven by the reference current and other terminal is given current I_{in} . This I_{in} current is replicated by current mirror circuit. Each current comparator compares the two currents and generates a voltage of + Vsat or –Vsat. The outputs of the comparators are used as inputs to priority encoder and priority encoder generate its binary value.

5.4 Simulation Results

In this section, transient analysis of the priority encoder is presented .The priority encoder is implemented in 0.18µm CMOS technology in PSPICE. The 2- Bit ADC is designed to function in the range of 0-100µA and has a step size of 20µA. The comparator reference currents Iref1, Iref2 and Iref3 were set as 20µA, 40µA and 60µA respectively.

To verify the correctness of the circuit transient analysis input, with a ramp input varying 0-70µA is done. The result are shown in fig.5.7.

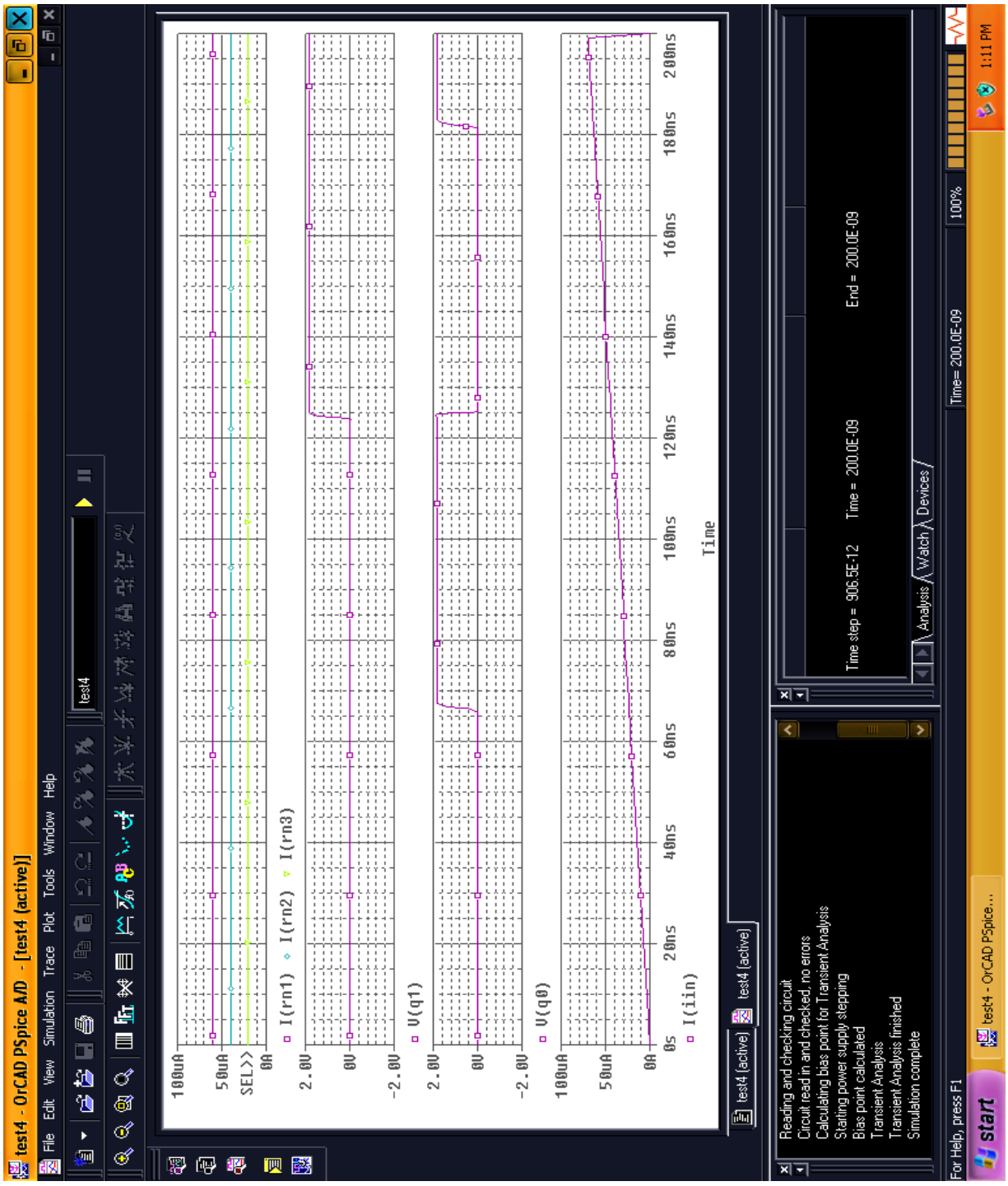

Fig. 5.7 Transient Analysis of ADC

5.5 Parameter Calculation of ADC

In our proposed ADC we take a 2 bit analog to digital converter. So we use three comparators. Reference point for comparator one is 20uA, comparator two is 40uA, and comparator three is 60uA.

Resolution

The resolution of the converter indicates the number of discrete values it can produce over the range of analog values.

$$\text{ADC current resolution} = \frac{60\mu A - 0}{2^2 - 1} = \frac{60\mu A}{3} = 20\mu A \qquad (5.1)$$

Step size is 20μA. Ideally first transition occur when input is equal to 20μA, then Analog to digital converter generate a code word of 01(1),when input is equal to 40μA, then adc generate a codeword of 10(2), and when input is equal to 60μA then adc generate a codeword 11(3).Fig. 5.9 explain the ideal characteristic of ADC.

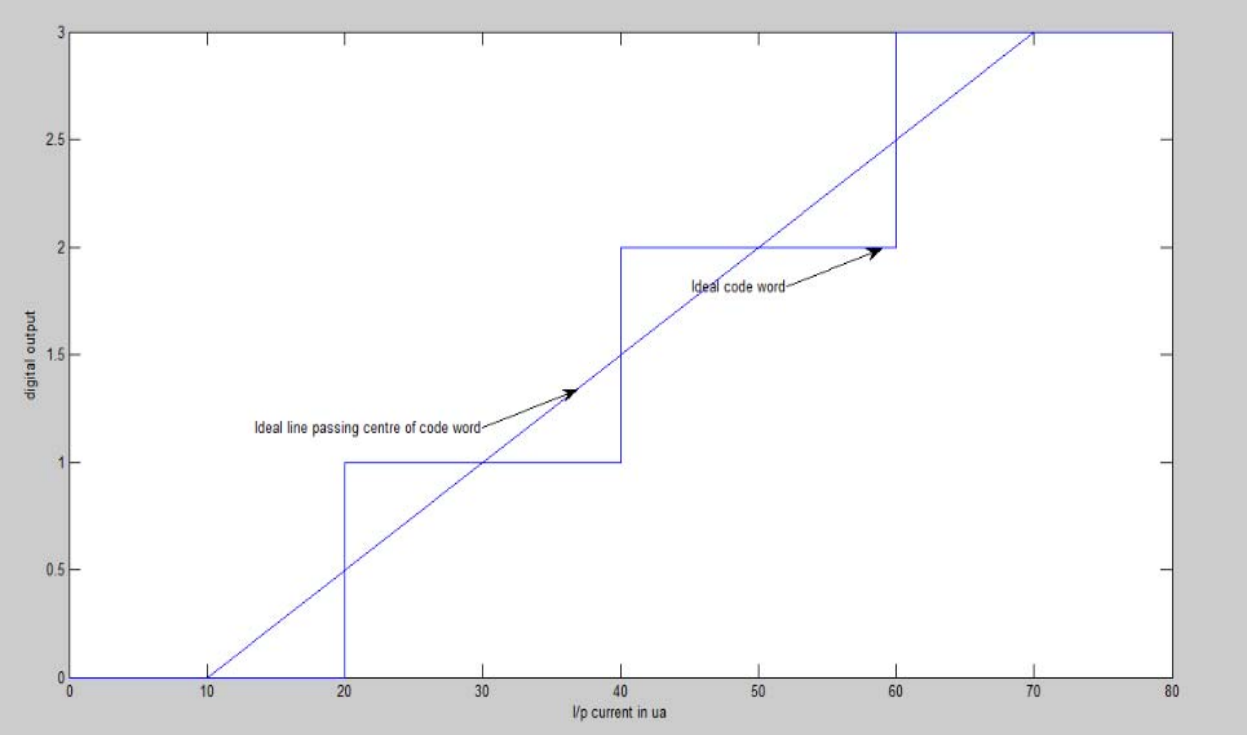

Fig.5.8 Ideal analog-to-digital converter characteristic

Offset Error

Offset error is the deviation in the A/D converter's behavior at zero. The First transition should be at LSB but in actual case the first transition occur at greater than LSB. As shown in Fig. The size of LSB is 20µA. But the first transition occur at 22µA. The offset error is 2µA which is equivalent to 0.1 LSB.

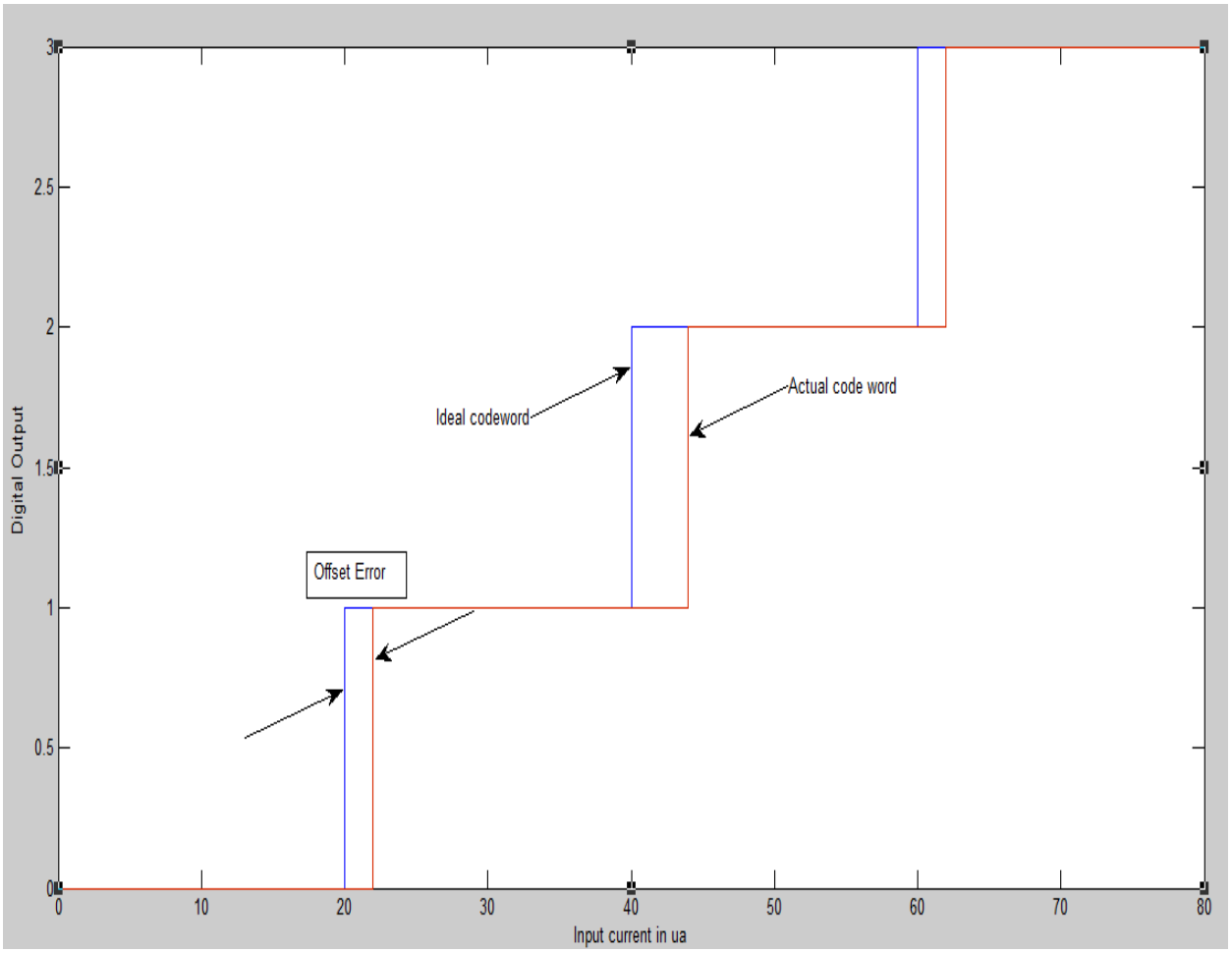

Fig.5.9 offset error

Differential Nonlinearity

Differential nonlinearity (DNL) is the deviation of the code transition widths from the idealwidth of 1 LSB. All code widths in the ideal A/D converter are 1 LSB wide, so the DNL would be zero everywhere. Calculation of DNL as shown in Fig.5.10

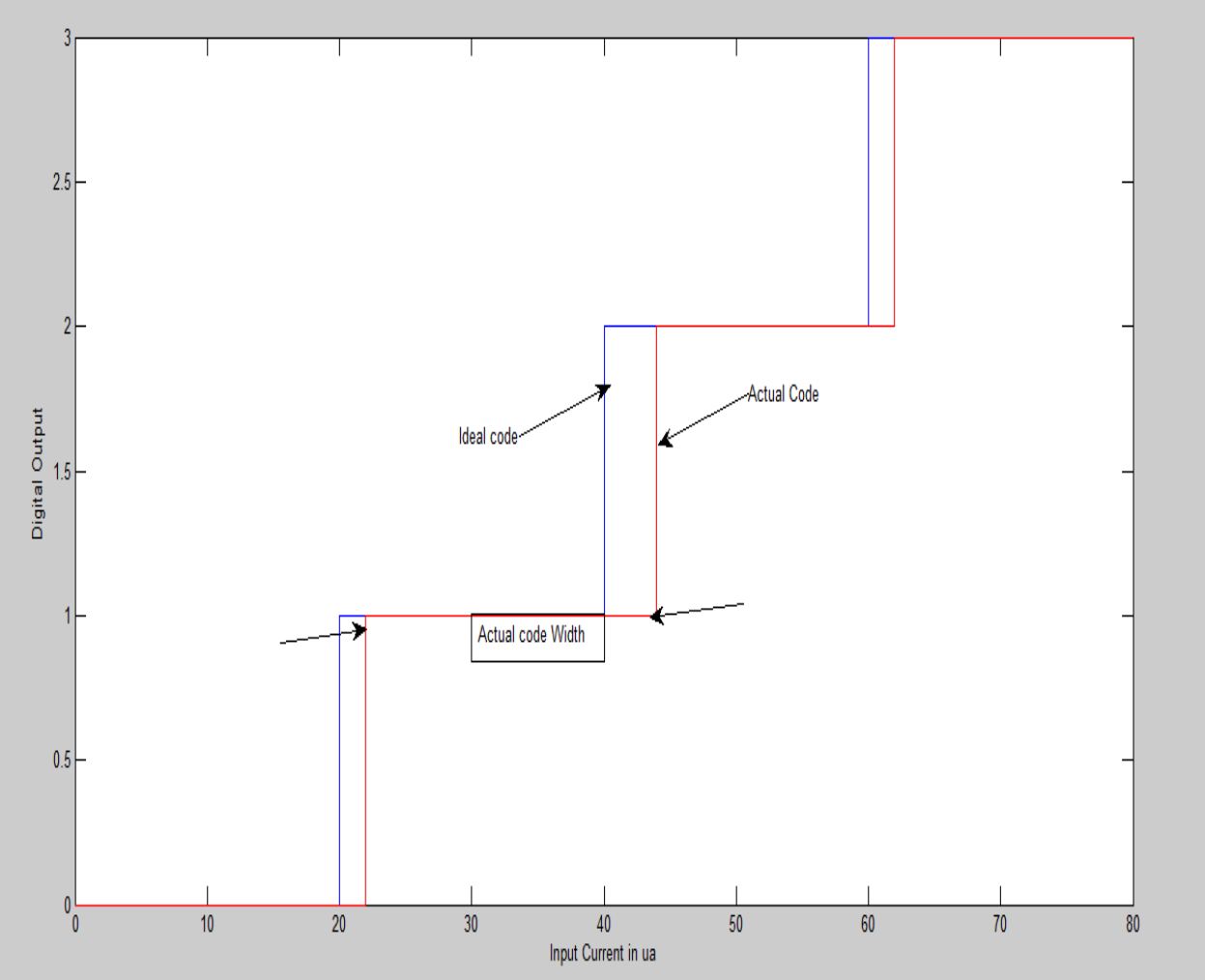

Fig.5.10 Ideal and Practical output of ADC

$$DNL = \frac{ActualCodeWidth - LSB}{LSB} \qquad (5.2)$$

In our ADC the DNL for 1 = (22-20)/20= 0.1 LSB

The DNL for 2 = (18-20)/20= -0.1 LSB

For proper working of analog to digital converter the DNL value should be as small as possible. The proposed ADC DNL value is approximately 0.1 LSB. Therefore there is not missing code word in the design.

Integral Nonlinearity

Integral nonlinearity (INL) is the distance of the code centers in the A/D converter characteristic

from the ideal line. If all code centers land on the ideal line, the INL is zero everywhere.

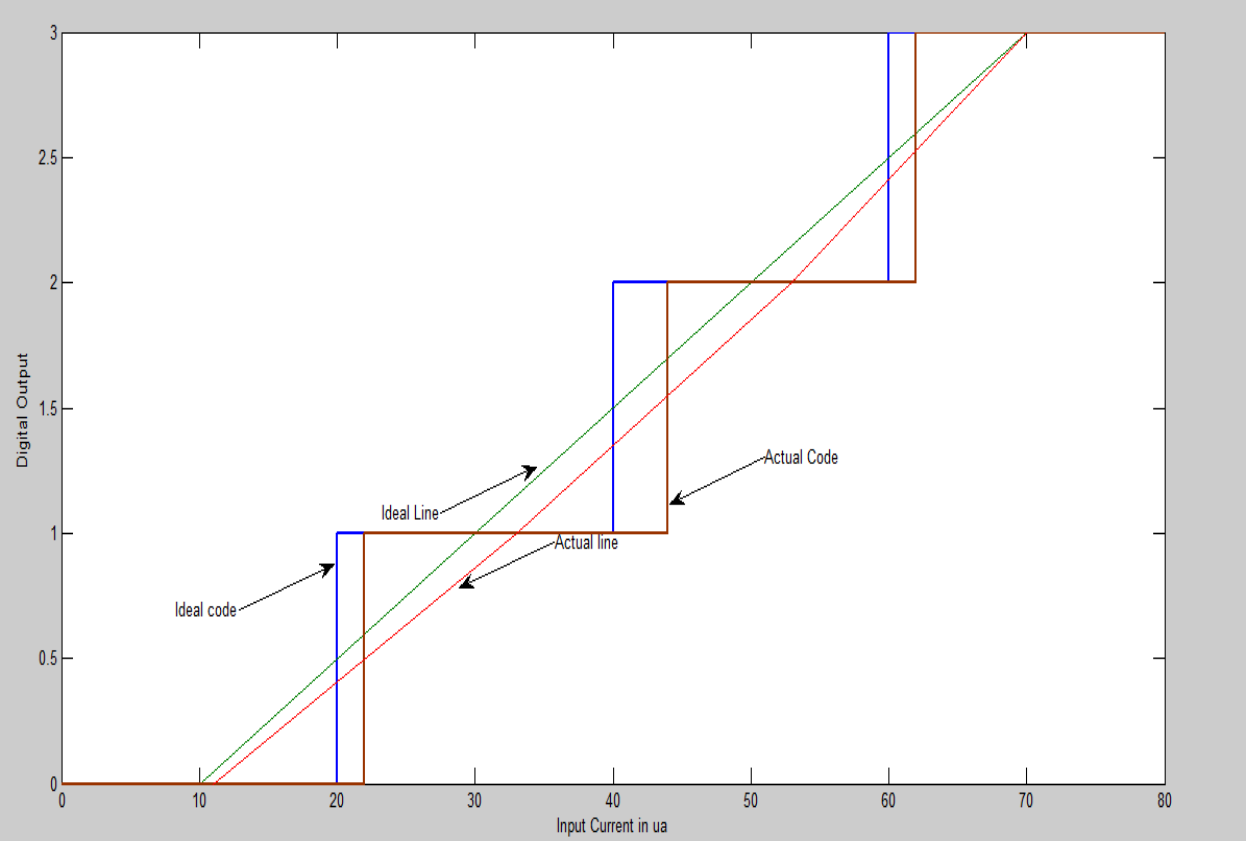

Fig.5.11 Observed output for INL calculation

As Shown in Fig.5.11 the distance between ideal line and actual line is represent the Integral linearity in our ADC the maximum Distance between the ideal line or actual line is 0.1LSB.

INL can be written as for kth code

$$INL(k) = \frac{\sum_{i=0}^{k-1} w_i - kLSB}{LSB} \qquad (5.3)$$

Where w_i is the width of code word if we assume all w_i are in LSB then

$$INL(k) = \sum_{i=0}^{k-1} w_i - k \qquad (5.4)$$

INL for k+1 code word is

$$INL(k+1) = \sum_{i=0}^{k} w_i - k \qquad (5.5)$$

Subtracting eg(5.4) from (5.5) to we get

$$INL(k+1) - INL(k) = w_k - 1 = DNL \qquad (5.6)$$

So we can say that INL is running sum of DNL.

ADC Response Time

Response time is defined as the amount time take output signal from low to high, high to low . We have get the response time of the Flash type Analog to Digital converter equal to 1.5ns

Power Dissipation

The simulated power dissipation of the designed flash type Analog to Digital convertor is observed to be 18.7mW.

CHAPTER 6

Conclusion & Future Scope

In this Dissertation flash type current mode analog to digital convertor has been designed. A 2-bit current mode ADC has been implemented in 0.18µm CMOS technology. The designs are mainly optimized for low power dissipation, accuracy and low response time. In this ADC maximum value of Differential Non Linearity value is 0.1 LSB and hence not a code word lost in this ADC. The response time of a ADC is 1.5ns. The power dissipation of a analog to digital converter reduced upto 18.7mw.

The circuit modules presented in the thesis used for designing different ADC structure for high speed, low power consumption namely flash ADC, Algorithmic ADC, folding and complementing structure of ADC's. However the priority encoder circuit MOS design concept used in the thesis can be change with pass transistor logic to increase the speed more and reduced the size. The ADCs can be ported to even smaller CMOS technologies to achieve even higher speed and low power dissipation.

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Appendix

Model parameters --- LEVEL 7

.MODEL NMOS NMOS (LEVEL = 7

+TNOM =27	TOX=4.1E-9	
+XJ =1E-7	NCH =2.3549E17	VTH0= 0.3750766
+K1= 0.5842025	K2 =1.245202E-3	K3 =1E-3
+K3B =0.0295587	W0 =1E-7	NLX =1.597846E-7
+DVT0W =0	DVT1W =0	DVT2W =0
+DVT0=1.3022984	DVT1 =0.1021873	DVT2 =7.631374E-3
+U0 =296.8451012	UA=-1.179955E-9	UB =2.32616E-18
+UC= 7.593301E-11	VSAT =1.747147E5	A0 =2
+AGS =0.452647	B0=5.506962E-8	B1 =2.640458E-6
+KETA =-6.860244E-3	A1 =7.885522E-4	A2=0.3119338
+RDSW =105	PRWG =0.4826	PRWB =-0.2
+WR =1	WINT =4.410779E-9	LINT =2.045919E-8
+XL =0	XW=-1E-8	DWG =-2.610453E-9
+DWB =-4.344942E-9	VOFF =-0.0948017	NFACTOR =2.1860065
+CIT =0	CDSC =2.4E-4	CDSCD =0
+CDSCB =0	ETA0 =1.991317E-3	ETAB =6.028975E-5
+DSUB =0.0217897	PCLM =1.7062594	PDIBLC1=0.2320546
+PDIBLC2 =1.670588E-3	PDIBLCB =-0.1	DROUT =0.8388608
+PSCBE1 =1.904263E10	PSCBE2 =1.546939E-8	PVAG =0
+DELTA =0.01	RSH =7.1	MOBMOD =1
+PRT =0	UTE =-1.5	KT1 =-0.11

+KT1L =0	KT2 =0.022	UA1=4.31E-9
+UB1 =-7.61E-18	UC1 =-5.6E-11	AT = 3.3E4
+WL =0	WLN =1	WW =0
+WWN =1	WWL= 0	LL =0
+LLN =1	LW =0	LWN =1
+LWL =0	CAPMOD =2	XPART =0.5
+CGDO =6.7E-10	CGSO =6.7E-10	CGBO =1E-12
+CJ =9.550345E-4	PB =0.8	MJ = 0.3762949
+CJSW =2.083251E-10	PBSW =0.8	MJSW =0.1269477
+CJSWG =3.3E-10	PBSWG =0.8	MJSWG =0.1269477
+CF =0	PVTH0 =-2.369258E-3	PRDSW =-1.2091688
+PK2 =1.845284E-3	WKETA =-2.040084E-3	LKETA =-1.266704E-3
+PU0 = 1.0932981	PUA =-2.56934E-11	PUB =0
+PVSAT =2E3	PETA0=1E-4	PKETA =-3.350276E-3

)

.MODEL PMOS PMOS (LEVEL = 7

+TNOM =27	TOX=4.1E-9	
+XJ =1E-7	NCH =2.3549E17	VTH0= -0.3936726
+K1= 0.5750728	K2 =-0.0235926	K3 =0.1590089
+K3B =4.2687016	W0 =1E-6	NLX =1.033999E-7
+DVT0W =0	DVT1W =0	DVT2W =0
+DVT0=0.5560978	DVT1 =0.24790116	DVT2 =0.1
+U0 =112.5106786	UA=1.45072E-9	UB =1.195045E-21
+UC= 1E-10	VSAT =1.168535E5	A0 =1.7211984
+AGS =0.3806925	B0=4.296252E-7	B1 =1.288698E-6
+KETA =-0.0201833	A1 =0.2328472	A2=0.3
+RDSW =198.748329	PRWG =0.5	PRWB =-0.4971827
+WR =1	WINT =0	LINT =2.943206E-8
+XL =0	XW=-1E-8	DWG =-1.949253E-8

+DWB =-2.824041E-9	VOFF =-0.0979832	NFACTOR =1.9624066
+CIT =0	CDSC =2.4E-4	CDSCD =0
+CDSCB =0	ETA0 =7.282772E-4	ETAB =-3.818572E-4
+DSUB =1.518344E-3	PCLM =1.4728931	PDIBLC1=2.138043E-3
+PDIBLC2 =-9.966066E-6	PDIBLCB =-1E-3	DROUT =4.276128E-4
+PSCBE1 =4.8501167E10	PSCBE2 =5E-10	PVAG =0
+DELTA =0.01	RSH =8.2	MOBMOD =1
+PRT =0	UTE =-1.5	KT1 =-0.11
+KT1L =0	KT2 =0.022	UA1=4.31E-9
+UB1 =-7.61E-18	UC1 =-5.6E-11	AT = 3.3E4
+WL =0	WLN =1	WW =0
+WWN =1	WWL= 0	LL =0
+LLN =1	LW =0	LWN =1
+LWL =0	CAPMOD =2	XPART =0.5
+CGDO =7.47E-10	CGSO =7.47E-10	CGBO =1E-12
+CJ =9.550345E-4	PB =0.8560642	MJ = 0.4146818
+CJSW =2.046463E-10	PBSW =0.9123142	MJSW =0.316175
+CJSWG =4.22E-10	PBSWG =0.9123142	MJSWG =0.316175
+CF =0	PVTH0 =-8.456598E-4	PRDSW =8.4838247
+PK2 =1.338191E-3	WKETA =0.0246885	LKETA =-2.016897E-3
+PU0 = 1.5089586	PUA =-5.51646E-11	PUB =1E-21
+PVSAT =50	PETA0=1E-4	PKETA =-3.316832E-3

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