Chapter 1

INTRODUCTION

The major driving force for the semiconductor industry, the device contacted gate pitch (Lpitch) is scaled down by a factor of 0.7 every technology node [1]. Reasonable questions to ask are: Will the MOSFET scaling be stopped? Is there a way to extend the silicon technology roadmap? After silicon technology, or as a complement to silicon technology, is there any potential technology that may be used? The last few years witnessed a dramatic increase in nanotechnology research, especially the nano electronics. These technologies vary in their maturity, as illustrated by Figure 1.2. The exciting opportunity is to design complex electronic circuits using the cutting-edge silicon technology and/or the novel nanometer-scale transistors in the future.

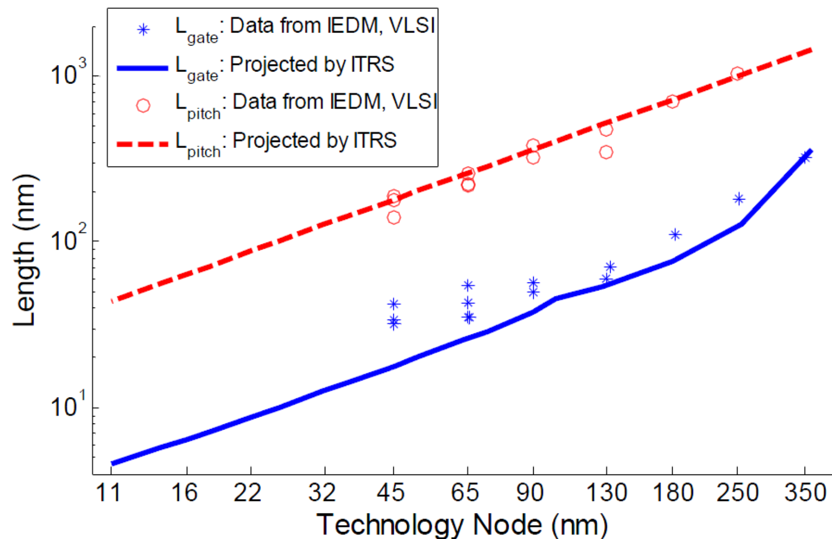


Figure 1.1: The physical gate length (Lgate) and the contacted gate pitch (Lpitch) of the fabricated devices (denoted by symbols) and projected by ITRS (denoted by lines).

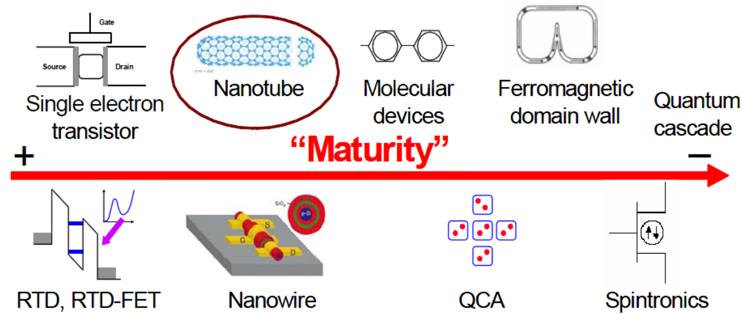


Figure 1.2: The novel nanoelectronic technologies in order of their maturity.

Carbon nanotubes (CNTs) are at the forefront of these new materials because of the unique mechanical and electronic properties. Carbon nanotube field effect transistor (CNTFET or CNFET) is the most promising technology to extend or complement traditional silicon technology due to three reasons: First, the operation principle and the device structure are similar to CMOS devices; we can reuse the established CMOS design infrastructure. Second, we can reuse CMOS fabrication process. And the most important reason is that CNTFET has the best experimentally demonstrated device current carrying ability to date [2,3].

The thesis is organized as follows:

Chapter 2: It describes the basic of carbon nanotube. In this chapter, firstly we will understand the bonding structure and fundamentals of the tube. Later is the summary of fundamental parameter definition and their relationship. It also explains the basics of energy band and tube conductivity dependency.

Chapter 3: This chapter is a brief literature survey of Carbon nanotube FET (CNFET).

Chapter 4: The complete device model of CNFET is divided into two parts. First part is the intrinsic channel behavior of the tube conductivity including some nonidealities, will be explained in this chapter.

Chapter 5: In this chapter, we will see the rest part of device model. Here, two different six and four capacitor model has been discussed, though the four capacitor model is implemented. We will also see the device behavior and performance via HSPICE simulations. A brief comparison between CMOS and CNFET has also been demonstrated here.

Chapter 6: This chapter is about the brief introduction of HSPICE and the useful tool (mathematical as well as simulation), that will be very helpful in the analog behavioral modeling of the device. Also, we will briefly overview the library files to understand the mechanics of the device design.

Chapter 7: In this chapter, we are going to implement some digital and analog application. In digital applications, gates like NAND and NOR is implement. The EXOR gate based on pass transistor design is implemented, so that the gate as well as the pass transistor performance could be demonstrated using CNTFET.

Chapter 2

THE CARBON NANOTUBE

Carbon nanotubes (**CNTs**) are allotropes of carbon with a cylindrical nanostructure. Nanotubes have been constructed with length-to-diameter ratio of up to 132,000,000:1 [4], significantly larger than for any other material. These cylindrical carbon molecules have unusual properties, which are valuable for nanotechnology, electronics, optics and other fields of materials science and technology. In particular, owing to their extraordinary thermal conductivity and mechanical and electrical properties, carbon nanotubes find applications as additives to various structural materials. Nanotubes are members of the fullerene structural family. Their name is derived from their long, hollow structure with the walls formed by one-atom-thick sheets of carbon, called graphene. These sheets are rolled at specific and discrete ("chiral") angles, and the combination of the rolling angle and radius decides the nanotube properties; for example, whether the individual nanotube shell is a metal or semiconductor. Nanotubes are categorized as single-walled nanotubes(SWNTs) and multi-walled nanotubes (MWNTs).

2.1 Atomic Bonding and Structure

Carbon atom has an electron configuration of 1s2 2s2 2p2 in its ground state. In graphene, sp2 hybridization occurs through covalent bonding of the two outermost shells. A carbon atom in graphene assembles in a single-sheet hexagonal lattice. The inter-carbon-atom distance within the hexagonal lattice (d) is approximately 1.44 Å, and the angle between carbon-carbon bonds (σ-bond) is 120 degrees. The lattice constant (a) is given by $\sqrt{3}$ d =2.49 Å. The 2p electrons from all the atoms on a lattice form a delocalized π-orbital between the two adjacent sheets. The inter-layer spacing between the multiple sheets in graphene is about 3.35 Å. The weak electrostatic interactions between the sheets make it possible to assume the electrical characteristics of the graphite sheets are independent each other.

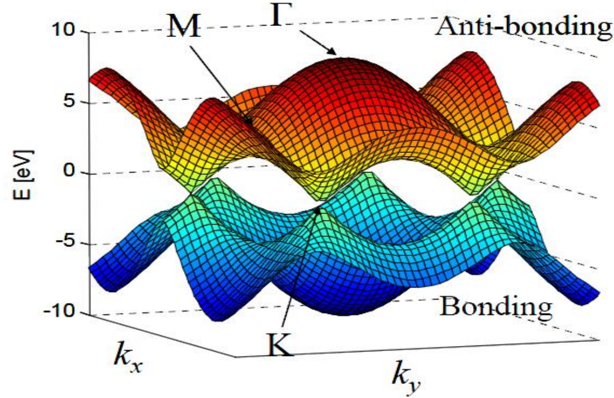


Figure 2.1: E-k dispersion relation for graphene, calculated using a nearest-neighbour tight-binding model. The three high-symmetry points are indicated by capital letters.

The dispersion relation for graphene, obtained by the Slater-Koster tight-binding scheme, considering only the π-orbital, is given by,

$$E_{g2D}(k_x,k_y) = \pm\sqrt{1+4\cos\left(\frac{\sqrt{3}k_x a}{2}\right)\cos\left(\frac{\sqrt{3}k_y a}{2}\right)+4\cos^2\left(\frac{k_y a}{2}\right)} \qquad (2.1)$$

Where (k_x, k_y) are wave vectors, V_π is the transfer integral (or the nearest-neighbour parameters). Figure 2.1 illustrates the band structure calculated with the above equation. The high-symmetry points are indicated by capital letters. *K*-points are degenerate, indicating the zero-bandgap (semi-metallic) characteristic of graphene sheet.

A single-walled carbon nanotube (SWCNT) can be visualized as a sheet of graphite which is rolled up and joined together along a wrapping vector $C_h = n_1.\bar{a}_1 + n_2.\bar{a}_2$, where [$\bar{a}_1$, $\bar{a}_2$] are lattice unit vectors as shown by Figure 2.2, and the indices (n_1, n_2) are positive integers that specify the chirality of the tube [5]. The length of C_h is thus the circumference of the CNT, which is given by,

$$C_h = a\sqrt{n_1^2 + n_2^2 + n_1 n_2} \qquad (2.2)$$

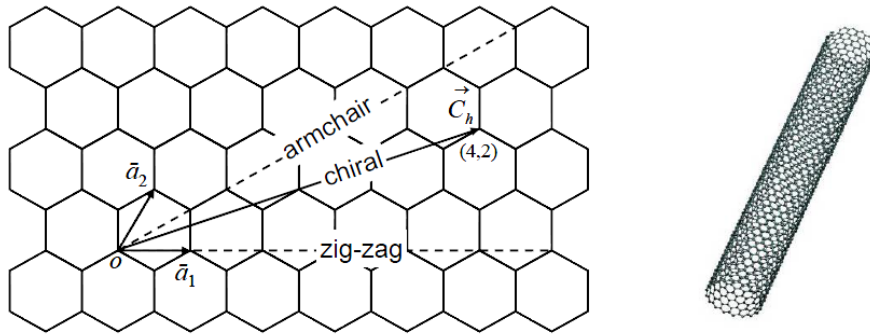


Figure 2.2: Unrolled graphite sheet and the rolled carbon nanotube lattice structure.

Single-walled CNTs are classified into one of their groups (Figure 2.2), depends on the chiral number (n_1, n_2): (1) armchair ($n_1 = n_2$), (2) zigzag ($n_1 = 0$ or $n_2 = 0$), and (3) chiral (all other indices). Figure 2.3 can give more easier look on the classification [5]. The diameter of the CNT is given by the formula $DCNT = C_h / \pi$. The typical diameters of CNTs are about several nanometers. Due to the small diameter of CNT, the quantization of wave vector in the circumferential direction occurs. A general analytic *E-k* dispersion relation for CNT is obtained by applying periodic boundary conditions in the circumferential direction to the 2D graphite sheet *E-k* dispersion relation. Pictorially, the dispersion of CNT is obtained by taking slices of the surface in Figure 2.1 with each cut determined by the circumferential quantization.

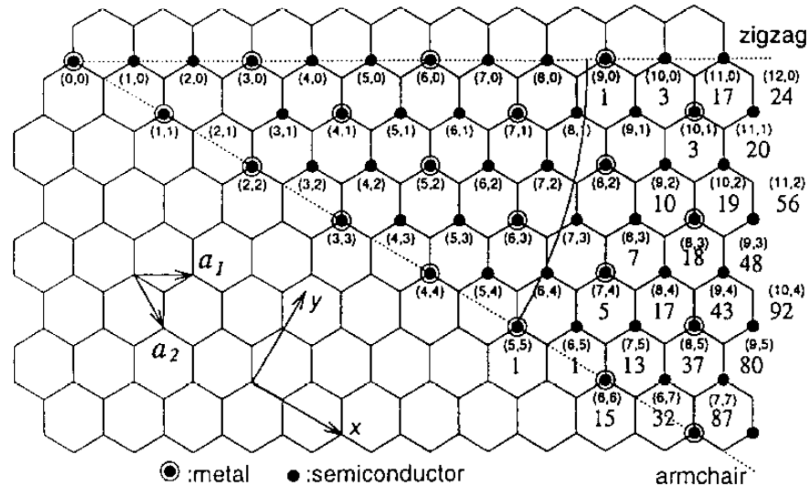


Figure 2.3: The 2D graphene sheet with different chiralities.

2.2 Fundamental Parameters and Relationship for CNT

This section summarizes the fundamental parameters for the CNT, to give the basic relations governing these parameters [5], and list typical numerical values for these parameters.

In the theoretical carbon nanotube literature, the focus is on single-wall tubules, cylindrical in shape with caps at each ends as shown in Figure 2.4, such that the two caps can be joined together to form a fullerene. The cylindrical portions of the tubules consist of a single graphene sheet that is shaped to form the cylinder. Recent discoveries of method help to make it possible to test the predictions of the theoretical calculations.

It is convenient to specify a general carbon nanotubule in terms of the tubule diameter d and the chiral angle θ. The chiral vector C_h is defined in table 2.1in terms of the integers (n_1,n_2) and the basis

vector a_1 and a_2 of the honeycomb lattice, which are also given in the table in terms of rectangular coordinates. The length L of the chiral vector C_h is directly related to the tubule diameter d. the chiral angle θ between the C_h direction and the zigzag direction of the honeycomb lattice $(n_1,0)$ is related in related in table 2.1 to the integers (n_1,n_2).

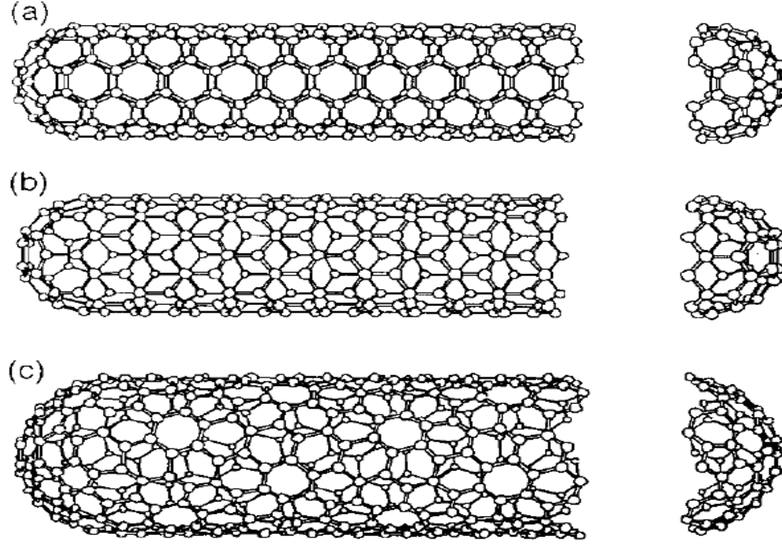


Figure 2.4: fullerene-derived tubules.

Table 2.1: parameters of carbon nanotube

symbol	name	Formula	value
a_{C-C}	carbon-carbon distance		1.421 Å (graphite)
a	length of unit vector	$\sqrt{3}\ a_{C-C}$	2.46 Å
a_1, a_2	unit vectors	$(\frac{\sqrt{3}}{2},\frac{1}{2})a,(\frac{\sqrt{3}}{2},-\frac{1}{2})a$	in (x,y) coordinate
b_1,b_2	reciprocal lattice vectors	$(\frac{1}{\sqrt{3}},1)\frac{2\pi}{a},(\frac{1}{\sqrt{3}},-1)\frac{2\pi}{a}$	in (x,y) coordinate
C_h	chiral vector	$C_h = n_1a_1 + n_2a_2 \equiv (n_1, n_2)$	n_1,n_2 integers
L	circumference of nanotube	$L = \|C_h\| = a\sqrt{n_1^2 + n_2^2 + n_1n_2}$	$0 \leq \|n_2\| \leq n_1$
d	diameter of nanotube	$d = \frac{L}{\pi} = \frac{a\sqrt{n_1^2 + n_2^2 + n_1n_2}}{\pi}$	
θ	chiral angle	$\sin\theta = \frac{\sqrt{3}n_2}{2\sqrt{n_1^2 + n_2^2 + n_1n_2}}$	$0 \leq \|\theta\| \leq 30^\circ$
		$\cos\theta = \frac{2n_1 + n_2}{2\sqrt{n_1^2 + n_2^2 + n_1n_2}}$	
		$\tan\theta = \frac{\sqrt{3}n_2}{2n_1 + n_2}$	
D	highest common divisor of(n1,n2)		
D_R	highest common divisor of (2n1+n2,2n2+n1)	$D_R = \begin{Bmatrix} D & \text{if } n1-n2 \text{ not multiple of } 3D \\ 3D & \text{if } n1-n2 \text{ a multiple of } 3D. \end{Bmatrix}$	

T	translational vector of 1D unit cell	$T = t_1 a_1 + t_2 a_2 \equiv (t_1, t_2)$	t_1, t_2 integer
		$t_1 = \frac{2n_2 + n_1}{D_R}$	
		$t_2 = -\frac{2n_1 + n_2}{D_R}$	
N	number of hexagons per 1D unit cell	$N = \frac{2(n_1^2 + n_2^2 + n_1 n_2)}{D_R}$	$2N \equiv n_C / unit\ cell$
R	symmetry vector	$\boldsymbol{R} = pa_1 + qa_2$	p,q:integers
		$D = n_2 p - n_1 q, 0 \le p \le n_1 / D, 0 \le q \le n_2 / D$	
M	number of 2 π revolutions	$M = \left[(2n_1 + n_2)p + (2n_2 + n_1)q\right] / D_R$	M: integer
		$N\boldsymbol{R} = MC_h + DT$	
R	basic symmetry operation	$R = (\psi / \tau)$	
Ψ	relation operation	$\psi = 2\pi \frac{M}{N}, \left(\chi = \frac{\psi L}{2\pi}\right)$	Ψ in radians
τ	translation operation	$\tau = \frac{DT}{N}$	χ, τ :length

These parameters will be used in chapter 3 in the understanding and physical modeling of CNTFET. To be compatible with the quasi 1D structure of CNT, we convert the (k_x, k_y) coordinate to (k_t, m), where the wave vector k_t is in the direction of transport, and m is quantization number in the circumferential direction. Analytically, the dispersion of CNT is given by the formula [5],

$$E_{CNT}(k_t, m) = \pm V_\pi \sqrt{1 + 4\cos t_1 \cos t_2 + 4\cos^2 t_2} \qquad (2.3)$$

Where the parameters are given by

$$t_1 = \frac{\sqrt{3}a}{4}\frac{n_2 - n_1}{n} k_t + \frac{\pi}{2}\frac{n_1 + 3n_2}{n^2} m$$

$$t_2 = \frac{\sqrt{3}a}{4}\frac{n_2 + n_1}{n} k_t + \frac{\pi}{2}\frac{3n_1 - n_2}{n^2} m$$

$$n^2 = n_1^2 + n_2^2 + n_1 n_2 \qquad (2.4)$$

$$-\frac{\pi D_R}{\sqrt{3}a.n} < k_t < \frac{\pi D_R}{\sqrt{3}a.n}$$

$$m = 0 : \frac{2n}{D_R} - 1$$

2.3 Electrical Conductivity and Density of States in CNT

In terms of the electrical conductivity, SWCNT is either metallic (when $|n_1 - n_2|$ is a multiple of 3) with zero band gap or semiconducting with finite band gap. The band structure for both metallic CNTs

and semiconducting CNTs are illustrated by figure 2.5, using both armchair SWCNTs (single walled carbon nanotubes) and zigzag SWCNTs as examples. To be accurate, achiral armchair SWCNTs (n_1=n_2) and zigzag SWCNTs ($n_1n_2 = 0$) are metallic, and the others ($|n_1-n_2|$ is a multiple of 3 but $n_1 \neq n_2$ and $n_1n_2 \neq 0$) are quasi-metallic with small band gap, calculated with equations (2.3, 2.4).

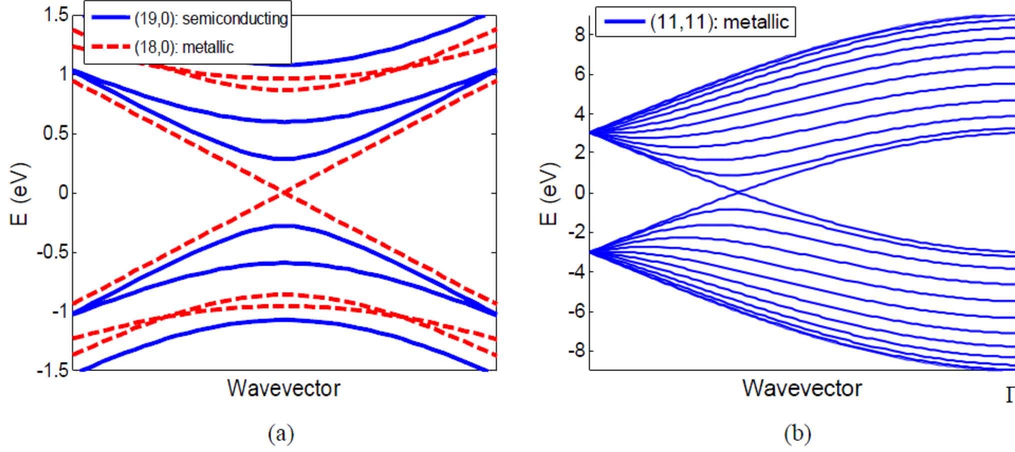


Figure 2.5: Energy dispersion relation for (a) (19,0), (18,0) zigzag CNTs, and (b) (11,11) armchair CNT.

The density of states (DOS) can be obtained as,

$$g(E) = \frac{2}{\pi}\int \left|\frac{\partial E_{CNT}}{\partial k_t}\right|^{-1} dE_{CNT} \tag{2.5}$$

proposes an universal expression to describe CNT band structure and the density of states, which are valid for the energy range $E_{CNT} << V\pi$ [6] . Figure 2.6 shows the DOS for (19,0) and (18,0) SWCNT with similar diameter (~ 1.5 nm).

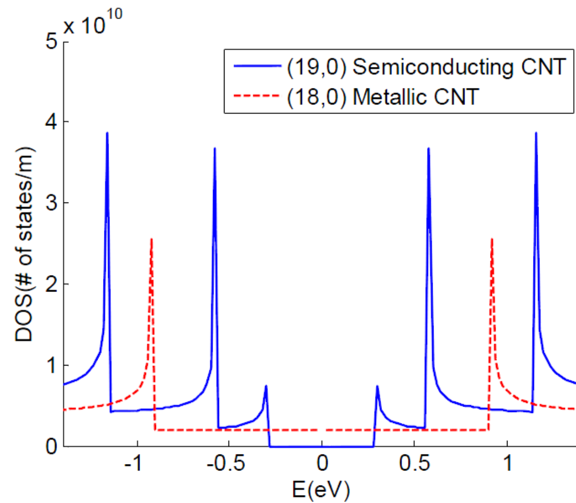


Figure 2.6:The density of states for (19,0) semiconducting and (18,0) metallic CNT

The electrons in CNT are confined within the atomic plane of graphene. Due to the quasi-1D structure of CNT, the motion of the electrons in the nanotubes is strictly restricted. Electrons may only move freely along the tube axis direction. As a result, all wide angle scatterings are prohibited. Only forward scattering and backscattering due to electron-phonon interactions are possible for the carriers in nanotubes. The experimentally observed ultra-long elastic scattering mean-free-path (MFP) [2, 3, 7] (~ 1 μm) implies ballistic or near-ballistic carrier transport. High mobility, typical in the range of 10^3 ~ 10^4 $cm^2/V \cdot s$ which are derived from conductance experiments in transistors, has been reported by a variety of studies [8, 9]. Theoretical study also predicts a mobility of ~ 10^4 $cm^2/V \cdot s$ for semiconducting CNTs [10]. The current carrying capacity of multi-walled CNTs are demonstrated to be more than 10^9 A/ cm^2, about 3 orders higher than the maximum current carrying capacity of copper which is limited by the electron migration effect, without performance degradation during operation well above room temperature [11]. The superior carrier transport and conduction characteristic makes CNTs desirable for nanoelectronics applications, e.g. interconnect and nanoscale devices.

Now at the end and of this chapter, we have understood some of important the basics of carbon nanotube such as the parameters to define the CNT structure, bonding model and the energy bands and density of states. In the coming chapters we will use the parameters to characterize the carbon nanotube field effect transistor (CNFET or CNTFET) and understand its modeling.

Chapter 3

THE CNTFET- A Literature Survey

The operation principle of carbon nanotube field-effect transistor (CNTFET) is similar to that of traditional silicon devices. This three (or four) terminal device consists of a semiconducting nanotube, acting as conducting channel, bridging the source and drain contacts. The device is turned on or off electrostatically via the gate. The quasi-1D device structure provides better gate electrostatic control over the channel region than 3D device (e.g. bulk CMOS) and 2D device (e.g. fully depleted SOI) structures [12].

In terms of the device operation mechanism, CNFET can be categorized as either Schottky Barrier (SB) controlled FET (SB-CNFET) or MOSFET-like FET [2, 3, 13]. The conductivity of SB-CNFET is governed by the majority carriers tunneling through the SBs at the end contacts. The on-current and thereby device performance of SB-CNFET is determined by the contact resistance due to the presence of tunneling barriers at both or one of the source and drain contacts, instead of the channel conductance, as shown by Figure 3.1(a). The SBs at source/drain contacts are due to the Fermi-level alignment at the metal-semiconductor interface. Both the height and the width of the SBs, and therefore the conductivity, are modulated by the gate electrostatically. SB-CNFET shows ambipolar transport behavior [14]. The work function induced barriers at the end contacts can be made to enhance either electron or hole transport. Thus both the device polarity (n-type FET or p-type FET) and the device bias point can be adjusted by choosing the appropriate work function of source/drain contacts [15]. On the other hand, MOSFET like CNFET exhibits unipolar behavior by suppressing either electron (pFET) or hole (nFET) transport with heavily doped source/drain. The non-tunneling potential barrier in the channel region, and thereby the conductivity, is modulated by the gate-source bias (Figure 3.1(b)).

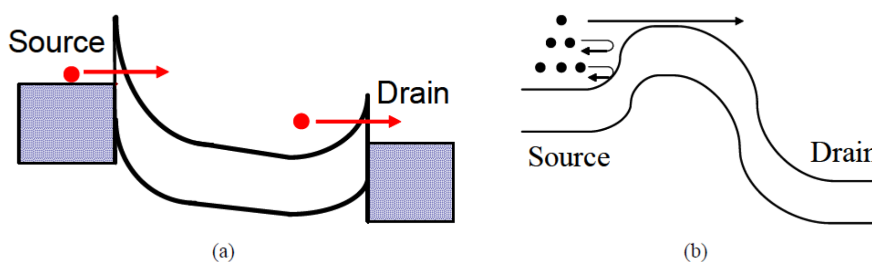


Figure 3.1: The energy band diagram for (a) SB-CNFET, and (b) MOSFET-like CNFET.

The first fabricated CNFET devices with Au or Pt source/drain metal contacts were reported in 1998 [16, 17]. The gate dielectric material was a thick SiO2 layer. A highly doped Si back gate was used to control the conductivity. The Al_2O_3 gate dielectric was introduced to improve the gate controllability over the channel region. The front gate device structure, by placing the gate electrode over the thin gate oxide that covers CNT, was used to further improve the channel electrostatics. Better gate electrostatics was achieved by using high-k, e.g. HfO_2, gate dielectric material [13]. The source/drain contacts using a variety of metals (Ti, Ni, Al, Pd, …) were fabricated to study the effect of the work function difference between the metal contacts and CNT on device conductivity. Ti source/drain metallization was reported to be efficient on reducing the contact resistance [14]. The device fabricated with Pd source/drain metal contact, Al gate electrode, and HfO2 gate dielectric was reported to achieve excellent dc characteristics. Logic circuits with field-effect transistors based on single carbon nanotubes have been demonstrated in the past few years. In 2001, demonstrated one-, two-, and three transistor circuits that exhibit a range of digital logic operations, including an inverter, a logic NOR, a static random-access memory (SRAM) cell, and an three-stage ac ring oscillator operating at 5 Hz. A five-stage CMOS type nanotube ring oscillator using palladium p-type gates and aluminum n-type gates was reported in 2006. Owing to the compact device/circuit design, this ring oscillator works at a frequency of 72 MHz Regarding RF analog application using CNFET, the first demonstration of ac gain in a single-walled carbon nanotube common-source amplifier was reported in 2006. The low frequency gain was ~ 11.3 dB, and the unity-gain frequency was about 560 kHz which was mostly limited by the parasitic load capacitance.

While the CNT synthesis / fabrication technique and the performance of CNFET devices and circuits have been significantly improved since the first fabricated device in 1998, CNFETs is still premature for very large scale integrated (VLSI) circuits design and commercial use. In order for CNFET to develop into a technology, first, we need tools to enable circuit design and performance benchmarking.

Efforts have been made in recent years on modeling semiconducting CNFET for digital logic applications and CNT for interconnects in order to evaluate the potential performance at the device level. This thesis will mostly focus on the device applications of CNT. A numerical model was reported in [18] to evaluate the dc current of SB-CNFET. The model reported in [19] predicts the dc performance of short channel SB-CNFET. Though good dc current can be achieved by SB-CNFET with the self-aligned structure, its ac performance is going to be poor due to the proximity of the gate electrode to the source/drain metal. The ambipolar behavior of SBCNFET also makes it undesirable for complementary logic design. Considering both the fabrication feasibility [20] and superior device performance of MOSFET-like CNFET as compared to SB-CNFET, we will focus on MOSFET-like CNFETs. To

evaluate the device/circuit performance as well as the performance dependence on device/geometry parameters, the requirements for a good device model include:

(1) Good scalability.

(2) Physics-based, or at least semi-physics based.

(3) Reasonable accuracy for both large signal and small signal analysis.

(4) Acceptable run time.

The reported compact models to date [21, 22] used one or more lumped static gate capacitances and assumed an ideal ballistic transport channel. These simplifications make it questionable when evaluating the transient response and device dynamic performance. The integral function used in [23] requires intensive calculation efforts and thereby makes it difficult to implement in circuit simulators, e.g. HSPICE [24]. The model in [22] improves the run time significantly by using a polynomial fitting approach. This methodology dilutes the physical meaning of the device model and makes evaluating CNFET performance with different device parameters (e.g. CNT chiralities, gate oxide thickness) inconvenient. The reported models to date [21, 22, 23] used a simple coaxial or planer gate structure that differs from the typical realistic CNFET gate structure that consists of high-k gate oxide on top of SiO2 insulating bulk [13]. For a CNFET with multiple parallel CNTs [3], these published models cannot examine the multiple CNT-to-CNT screening effect on both the driving current and the effective gate capacitance [25]. All the reported device models assumed CNFET devices with perfect and ideal CNT channel. Compared to the intrinsic performance of CNFET predicted by theoretical studies [23], the actual device and circuit level performance is mostly limited by various parasitic and process induced imperfections. The device parasitics and/or non-idealities include, but are not limited to: the channel length dependence of current drive, the finite scattering mean free path, the source/drain series resistance, the source/drain contacts (SBs) resistance, the geometry dependence of the gate to channel capacitance, and the interconnect wiring capacitance. To evaluate CNFET device/circuit performance with improved accuracy, a CNFET device model with a more complete circuit-compatible structure and also incorporating the typical device/circuit non-idealities is necessary. A good balance between the simulation run-time and accuracy is desired.

The circuit macro level performance is not only limited by the performance of one single device, but also limited by the device performance variations which are significant for nanometer scale devices. There are a variety of device parameter variations and imperfections caused by today's CNT synthesis/fabrication technique: (1) CNT diameter and chirality control; (2) Doping level control; (3) The probability of a CNT to be metallic; (4) Directed-CNT-growth. A reasonable question to ask is: considering these imperfections, what can be gained at the circuit-level using CNFET technology compared to cutting-edge Si CMOS?

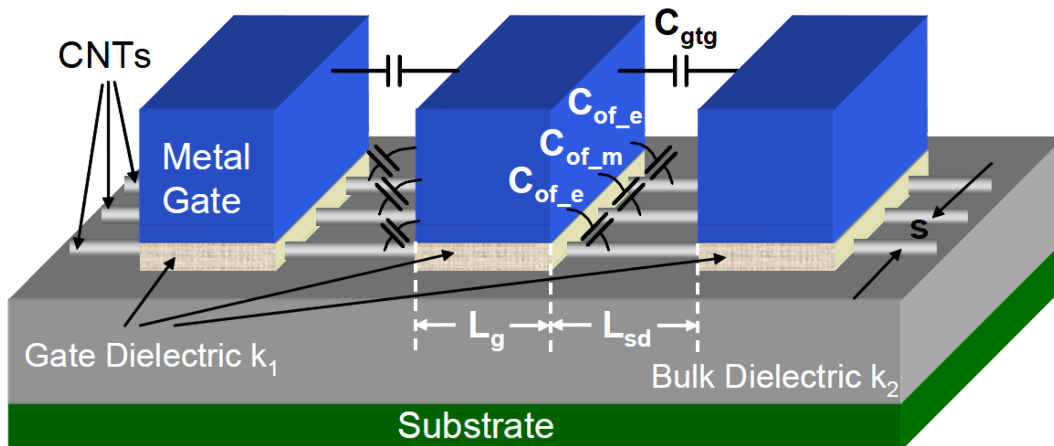
Chapter 4

COMPACT MODEL FOR INTRINSIC CHANNEL REGION OF CNFET

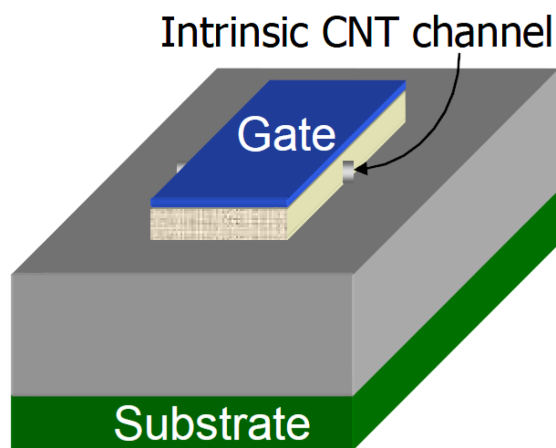
As one of the promising new transistors, carbon-nanotube field-effect transistor (CNFET) avoids most of the fundamental limitations for traditional silicon MOSFETs. With ultra-long (~1μm) mean free path (MFP) for elastic scattering, a ballistic or near-ballistic transport can be obtained with an intrinsic carbon nanotube (CNT) under low voltage bias to achieve the ultimate device performance [7]. The quasi 1D structure provides better electrostatic control over the channel region than 3-D device (e.g., bulk CMOS) and 2D device (e.g., fully depleted SOI) structures [26]. Efforts have been made in recent years on modeling semiconducting CNFET for digital logic applications and CNT for interconnects, in order to evaluate the potential performance at the device level [21,27,28]. The reported compact models to date used one or more lumped static gate capacitances and an ideal ballistic transport model. These simplifications make it questionable when evaluating the transient response and device dynamic performance. The integral function [27,28] used in and requires intensive calculation efforts and thereby makes it difficult to implement in circuit simulators, e.g., HSPICE [24]. The polynomial fitting approach used in improves the runtime significantly [21], but it makes the evaluation of the CNTFET performance with different device parameters inconvenient. The simple coaxial or planer gate structures utilized in differ from the typical realistic CNFET gate structure that consists of high-k gate oxide on top of the SiO2 insulating bulk. For a CNFET with multiple parallel CNTs [2], these published models cannot examine the multiple CNT-to-CNT screening effects on both the driving current and the effective gate capacitance. To evaluate the CNFET circuit performance with an improved accuracy, a CNTFET device model with a more complete circuit-compatible structure and also incorporating the typical device/circuit nonidealities is necessary.

4.1 Device Structure

A typical layout of a MOSFET-like CNFET device is illustrated in Figure 4.1(a). One or multiple devices can be fabricated along a single CNT, and multiple CNTs may be placed under the same gate in order to improve the drive current. The CNT channel region is undoped, and the other regions are heavily



(a)



(b)

Figure 4.1: (a) The 3-D device structure of CNFETs with multiple channels, high-*k* gate dielectric material, and the related parasitic gate capacitances. In this example, three CNFETs are fabricated along one single CNT. The channel region of CNTs is un-doped, and the other regions of CNTs are heavily doped. (b) The 3D device structure of CNTFET that is modeled in this chapter, only with the intrinsic channel region.

acting as both the source/drain extension region and/or interconnects between two adjacent devices (un-contacted source-gate/gate-drain configurations). In order to account for the screening by the adjacent CNTs for the device with multiple CNTs, the nanotubes under the gate are grouped into (1) the two CNTs at the edges; (2) the other CNTs in the middle. The CNTs in each group are treated identically [25].

This chapter describes the modeling of one single intrinsic channel of CNFET, as shown in Figure 4.1(b), which is a starting point towards the complete device model reported in Chapter 5. For

MOSFET-like CNFET, since pFET behavior is similar to nFET, we will only describe the equations for nFET in this chapter, though we implemented both nFET and pFET for the SPICE simulations.

From the circuit point of view, the input / output signals can be defined as either current or potential, and the outputs (current or potential) are just the responses to the inputs (current or potential). The potential can be either electrostatic potential or chemical potential (referred as the “Fermi level” in the following). For macro scale circuits/devices, potential usually means electrostatic potential because the Fermi level profile follows the electrostatic potential profile around the contacts which are usually the input/output ports. For a 1-D quantum wire with two contacts (source and drain), the source Fermi level µs and the drain Fermi level μ_d will be split apart with finite drain bias (V_{ds}) due to the finite density of states (DOS) [29]. Thus it becomes ambiguous to describe 1-D device behavior with electrostatic potential only, especially for the devices that are connected serially without an intermediate reservoir of electrons provided by a metal contact. In this work, we use both the Fermi level and the surface (electrostatic) potential to describe CNFET device behavior.

4.2 Model of the Intrinsic Channel Region

This part models the intrinsic channel region of CNFET with a near-ballistic transport and without any parasitic capacitance and parasitic resistance. The equivalent circuit model is shown as Figure 4.2. Figure 4.2(a) is the equivalent circuit implemented with HSPICE [24], and Figure 4.2(b) and (c) is the other two possible implementations for the trans-capacitance network, which will be discussed in the coming section.

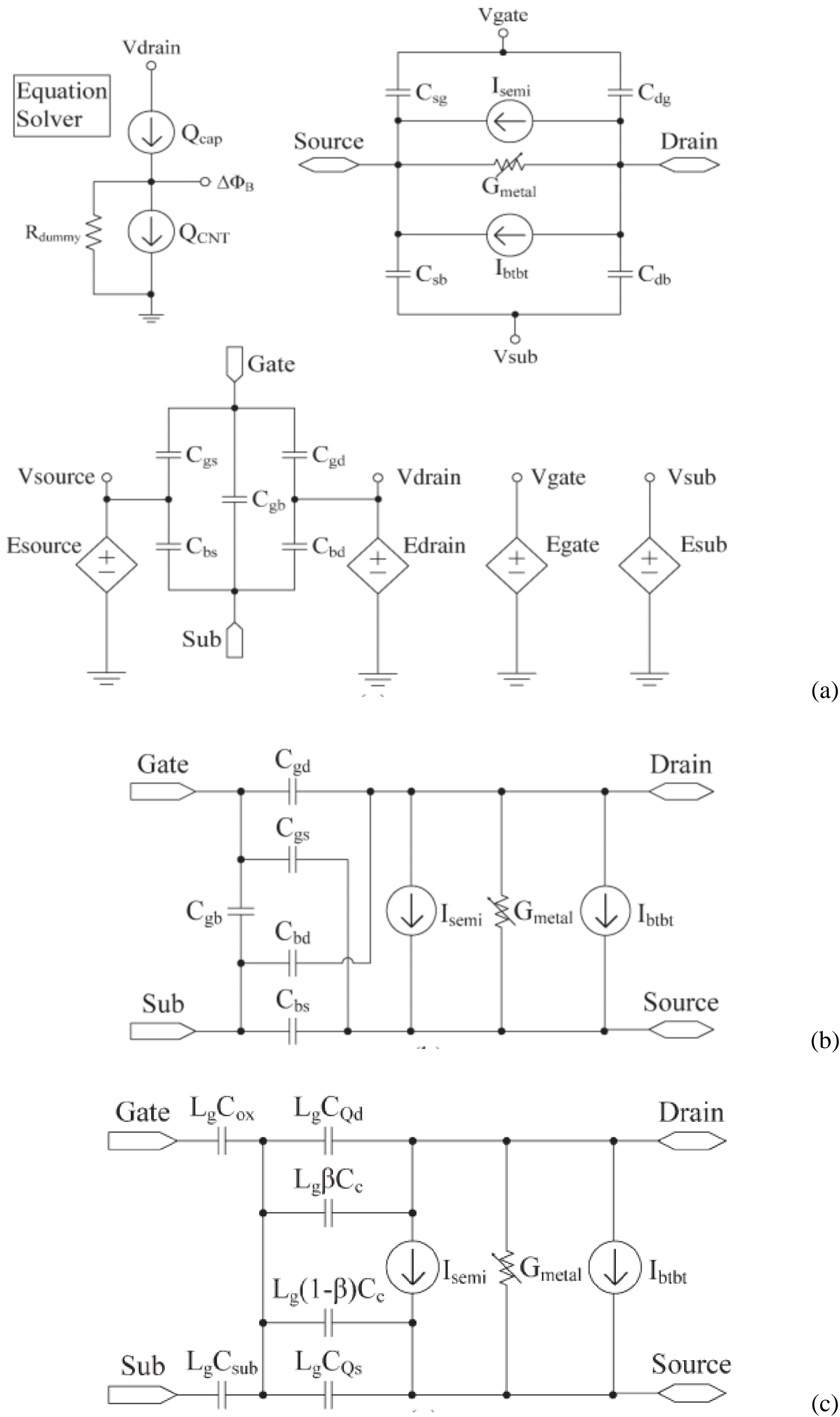


Figure 4.2: Equivalent circuit model for the intrinsic channel region of CNFET. (a) Nine-capacitor model, assuming that the carrier distribution along the channel is uniform. Exxx is the voltage-controlled voltage source, and the potential of Vxxx is equal to the controlling voltage source. R_{dummy} is a large-value (>1e15) resistor to keep the circuit stable. (b) Five-capacitor model and (c) six-capacitor model, assuming that all the carriers from +k branches are assigned to the source and that all the carriers from −k branches are assigned to the drain.

The Fermi-level profiles and the energy-band diagram in the channel region with a ballistic transport are shown in fig .The potential differences $\mu_s - \mu'_s$ and $\mu_d - \mu'_d$ are determined by both the applied bias and the property of the source/drain extension regions. We will treat the nonballistic transport and the potential drop at the source/drain extension region and the contacts in the complete device model. We assume near-ballistic transport and ideal (reflectionless) contacts in this chapter, i.e., $eV_{DS} \approx \mu_d - \mu_s$; thus, $\mu_s(\mu_d)$ remains almost constant in the source-channel (drain-channel) region Figure 4.3(a).

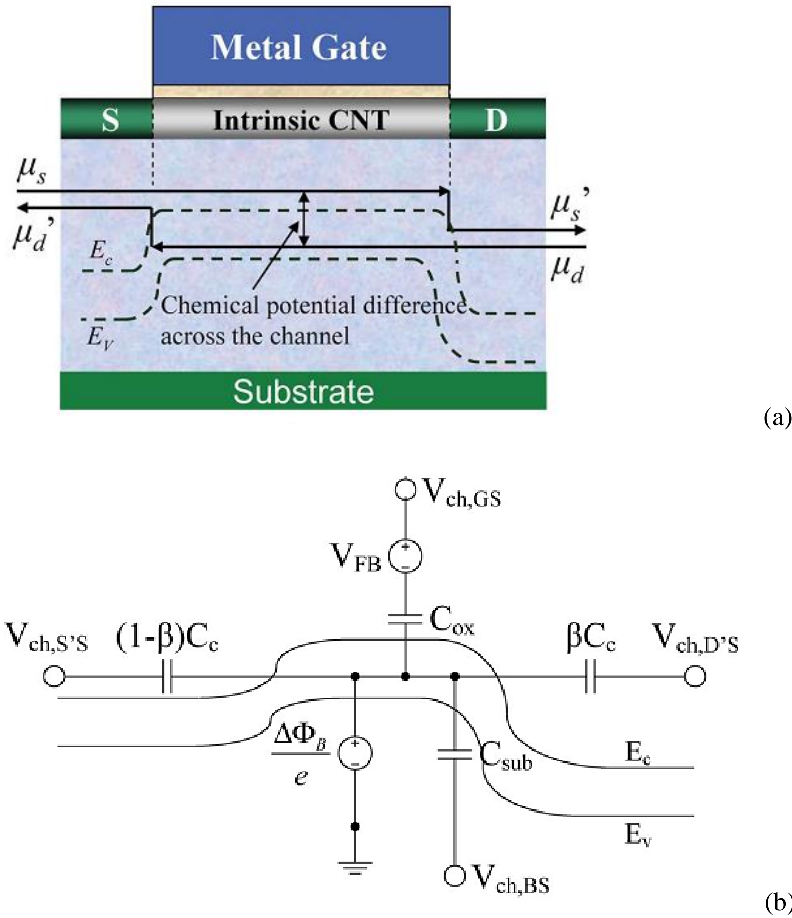


Figure 4.3(a): Ideal CNFET with ballistic (intrinsic) channel. Superposed are the Fermi-level profiles (solid arrows) from source to drain and the energy-band diagram (dashed lines) with bias $V_{DS}=(\mu_d - \mu_s)/e$. (b) Electrostatic capacitor model used to calculate the channel surface-potential change $\Delta\Phi_B$ before and after gate /source /drain /substrate bias. All the node potentials are referred to the input source Fermi level. Superposed is the energy-band diagram (only the first subband shown) from the external source nodes to the external drain node D'.

4.3 Current Sources

The single-walled CNT (SWCNT) is treated as a quasi-1D quantum wire in this chapter. For SWCNT with chiralities (n_1,n_2), the diameter (D_{CNT})is given by (a=2.49 Å is the lattice constant) [5].

SWCNTs can be grouped as either metallic or semiconducting nanotubes. For SWCNT with a finite length (Lg) and a finite diameter (D_{CNT}), applying the Born–von Karman boundary condition on both the circumferential direction and axial (channel length) directions, the E–k dispersion relation is quantized into discrete substates. We denote (m, l) as the lth substate at the mth subband, k_m as the wavenumber of the mth subband in the circumferential direction, and k_l as the wavenumber of the lth substate in the current-flow direction [5]. We define the subbands with positive band gap as "semiconducting subbands," and the subbands with zero or negative band gap as "metallic subbands." Thus, the band structure of metallic nanotubes can be treated as a summation of the metallic and semiconducting subbands.

$$D_{CNT} = \frac{a\sqrt{n_1^{\ 2} + n_2^{\ 2} + n_1 n_2}}{\pi} \qquad (4.1)$$

The wavenumbers related with semiconducting subbands are given by [29]

$$k_m = \frac{2\pi}{a\sqrt{n_1^{\ 2} + n_2^{\ 2} + n_1 n_2}}.\lambda \qquad (4.2a)$$

$$\lambda = \begin{cases} \frac{6m-3(-1)^m}{12}, & m=1,2,........;\mathrm{mod}(n_1-n_2,3)\neq 0. \\ m, & m=0,1,.........;\mathrm{mo}(n_1-n_2,3)=0. \end{cases} \qquad (4.2b)$$

$$k_l = \frac{2\pi}{L_g} l, \qquad l = 0,1,2,..... \qquad (4.2c)$$

m=0 is reserved for the metallic subband. k_l approaches the continuous values for large L_g. Around the Fermi point with carrier energy $E_{m,l} << V_\pi$(~3.033 eV, the carbon π–π bond energy in the tight bonding model), CNT $E-k$ dispersion relation can be approximated as

$$E_{m,l} \approx \frac{\sqrt{3}}{2} aV\pi\sqrt{k_m^2 + k_l^2} \qquad (4.3)$$

We consider three current sources in the CNFET model: 1) the thermionic current contributed by the semiconducting subbands (I_{semi}) with the classical band theory; 2) the current contributed by the metallic subbands(I_{metal}); and 3) the leakage current (I_{btbt})caused by the band-to-band tunneling (BTBT) mechanism through the semiconducting subbands.

4.3.1 Thermionic Current Contributed by Semiconducting Subbands

For semiconducting subbands, we only consider the electron current for the nFET because the hole current is sup-pressed by the n-type heavily doped source/drain. The current contributed by the substate *(m,l)* is given by

$$J_{m,l}(V_{xs}, \Delta\Phi_B) = 2env_F \qquad (4.4)$$

Where V_{xs} is the potential difference between the node x and the source. The Fermi velocity $v_F=1/\hbar\cdot\partial E/\partial k_l$. The factor of two is due to electron spin degeneracy, e is the unit electronic charge, and n is the number of electrons that occupy the substate *(m, l)*, which is given by

$$n = \frac{f_{FD}(E_{m,l} + eV_{xs} - \Delta\Phi_B)}{Lg} \qquad (4.5a)$$

$$f_{FD} = \frac{1}{1+e^{E/kT}} \qquad (4.5b)$$

Where $\Delta\Phi_B$ is the channel surface-potential change with gate/drain bias, $f_{FD}(E)$ is the Fermi–Dirac distribution function, k is the Boltzmann constant, T is the temperature in kelvin, and $E_{m,1}$ is the carrier energy at the substate (m, l).

With (4.4) and (4.5), we obtain

$$J_{m,l}(V_{xs}, \Delta\Phi_B) = \frac{2e}{h}\frac{\sqrt{3}a\pi V_\pi}{L_g}\frac{k_l}{\sqrt{k_m^2 + k_l^2}}\frac{1}{1+e^{(E_{m,l}+eVxs-\Delta\Phi_B)/kT}} \qquad (4.6)$$

The total current contributed by all substates is equal to the current flowing from the drain to the source (+k branch) minus the current flowing from the source to the drain (−k branch)

$$I_{semi}(V_{ch,DS}, V_{ch,GS}) = 2\sum_{\substack{k_m \\ m=1}}^{M}\sum_{\substack{k_l \\ l=1}}^{L}\left[T_{LR}J_{m,l}(0, \Delta\Phi_B)|_{+k} - T_{RL}J_{m,l}(V_{ch,DS}, \Delta\Phi_B)|_{-k}\right] \qquad (4.7)$$

Where $V_{ch,DS}$ and $V_{ch,GS}$ denote the Fermi potential differences near the source side within the channel, the factor of two is due to the double degeneracy of the subband, and M and L are the numbers of subbands and substates, respectively.

For typical devices with appropriate diameter range(D_{CNT}<3nm) and short gate length ($Lg \leq 100$ nm), only the first two or three subbands and the first 10–15 substates have a significant impact on the current using a sub-1-V power supply. Including more subbands should be done with more caution due to two limitations: (1) The band-structure model used in this chapter requires $E_{m,l} << V_{\pi}$, and (2) the complex phonon modes at high energy level. For long-channel devices (Lg>100 *nm*), one can either approximate the current for short device equation 4.7 by setting Lg=100 nm in equations (4.2c), (4.5a), and (4.6) or use the long-channel model introduced in equation 4.14 in the succeeding part of this part. T_{LR} and T_{RL} are the transmission probability of the carriers at the substate *(m,l)* in $+k$ and $-k$ branches, respectively. We consider three typical scattering mechanisms in the channel region: 1) acoustic phonon scattering (near-elastic process [27]); 2) optical phonon scattering (inelastic process [30]); and 3) elastic scattering [30]. The elastic-scattering probability is assumed to be independent of the carrier energy and will be treated in the complete device modeling in coming chapter. Both the acoustic and optical phonon scatterings depend on the carrier energy. Only intraband scatterings are considered in this chapter. Random-angle scatterings are suppressed and only back and forward scatterings can occur in a 1D quantum wire due to the Pauli's exclusion principle and the confined k-space [5]. A scattering event from the substate (m, l_1) in +/−k branch to the substate (m,l_2) in −/+k branch can occur only if the two conditions are satisfied: 1) The substate (m, l_1) is filled with electrons, and 2) the substate (m, l_2)is empty so that it can accept the scattered carrier from (m,l_1). Assuming that the optical phonon-scattering MFP (λop∼15 nm) and the acoustic phonon-scattering MFP (λap∼500 nm [2]) are constant if both conditions are met, we normalize the effective acoustic phonon-scattering MFP (l_{ap}) and the effective optical phonon-scattering MFP(l_{op})of the semiconducting subbands to the available target empty states

$$l_{ap}(V_{xs},m,l) = \frac{\lambda_{ap} D_o}{D(E_{m,l})\left[1 - f_{FD}\left(E_{m,l} - \Delta\Phi_B + eV_{xs}\right)\right]} \quad (4.8a)$$

$$l_{op}(V_{xs},m,l) = \frac{\lambda_{op} D_o}{D(E_{m,l} - \hbar\Omega)\left[1 - f_{FD}\left(E_{m,l} - \hbar\Omega - \Delta\Phi_B + eV_{xs}\right)\right]} \quad (4.8b)$$

Where $\hbar\Omega$(~0.16 eV [2]) is the optical phonon energy that a carrier attains before an optical phonon scattering can occur.

Optical phonon scattering becomes more significant at high $V_{ch,DSbias}$. Do is a constant $8/(3\pi V_{\pi} \cdot d)$, where d is the carbon–carbon bond distance, which is about 0.144 nm. $D(E)$ is the CNT universal DOS which is valid in the range $E_{m,l} << V_{\pi}$.

$$D(E)=\begin{cases} D_0.E/\sqrt{E^2-E_{m,0}^2}, & E>E_{m,0} \\ 0, & E\le E_{m,0}. \end{cases} \quad (4.9)$$

The effective phonon-scattering MFP is in the form of

$$\frac{1}{l_{eff}(V_{xs},m,l)}=\frac{1}{l_{ap}(V_{xs},m,l)}+\frac{1}{l_{op}(V_{xs},m,l)} \quad (4.10)$$

It is reasonable to assume that the phonon backscattered carriers are not likely to be backscattered again due to the energy loss and/or the occupied states. Thus, the transmission probabilities in equation 4.7 are given by

$$T_{LR}=\frac{l_{eff}(V_{ch,DS},m,l)}{l_{eff}(V_{ch,DS},m,l)+L_g} \quad (4.11a)$$

$$T_{RL}=\frac{l_{eff}(0,m,l)}{l_{eff}(0,m,l)+L_g} \quad (4.11b)$$

The key parameter for evaluating CNFET current is $\Delta\Phi_B$, which is the channel surface-potential change in response to the changes in the gate and source/drain bias. As shown in Figure 4.3(b), there are three electrostatic coupling capacitors, assuming that the channel material is with an infinite DOS: the capacitance (C_{ox}) between the gate and channel, the capacitance (C_{sub}) between the channel and substrate, and the capacitance (C_c)between the channel and external drain (D')/source (S'). $\Delta\Phi_B$ is dynamically affected by the drain bias. βC_c is a fitting parameter that describes this effect due to the two mechanisms: 1) the surface-potential lowering due to the electrostatic coupling between the channel region and the external drain electrode through fringing electric field, and 2) the surface-potential lowering due to nonuniform channel surface-potential profile caused by the drain-induced barrier-lowering effect. Operationally, the parameters C_c and β are chosen to fit the subthreshold slope and the measured short-channel effect. For a semiconducting channel with a finite DOS, the channel surface potential $\Delta\Phi_B$ changes with the gate bias at a rate $\Delta\Phi_B/\Delta V_{GS}<1$, a phenomenon known as the effect of quantum capacitance. We calculate $\Delta\Phi_B$ using the charge conservation equations

$$Q_{cap}=Q_{CNT} \quad (4.12a)$$

$$Q_{cap}=C_{ox}\left(V_{ch,GS}-V_{FB}\right)+C_{sub}V_{ch,BS}+\beta C_c V_{ch,DS}+\left(1-\beta\right)C_c V_{ch,s's}-\left(C_{ox}+C_{sub}+C_c\right)\frac{\Delta\Phi_B}{e}$$

(4.12b)

$$Q_{CNT} = \frac{4e}{L_g} \sum_{\substack{k_m \\ m=m_0}}^{M} \sum_{\substack{k_l \\ l=0}}^{L} \left[\frac{1}{1+e^{\left(E_{m,l}-\Delta\Phi_B\right)/KT}} + \frac{1}{1+e^{\left(E_{m,l}-\Delta\Phi_B+eV_{DS}\right)/KT}} \right] \quad (4.12c)$$

$$m_0 = \begin{cases} 1, & \mathrm{mod}(n_1 - n_2, 3) \neq 0 \\ 0, & \mathrm{mod}(n_1 - n_2, 3) = 0. \end{cases} \quad (4.12d)$$

The factor of four includes both the spin degeneracy and the double degeneracy of the subband. V_{FB} is the flat-band voltage, and V_{BS} is the potential difference between the substrate and source. Q_{cap} is the charge induced by the electrodes, and Q_{CNT} is the total charge induced on the SWCNT surface. We solve iteratively using a construct in HSPICE [Fig. 4.2(a)].

The front-gate capacitance C_{ox} is modeled as a planar-gate structure with high-k*gate* dielectric on top of the SiO2 insulating layer (Figure 4.1). For the device with multiple SWCNTs in parallel, Cox is grouped into the capacitance between the gate and SWCNT at the two ends *(Cox_e)* and the capacitance between the gate and SWCNT in the middle *(Cox_m)* [20]. For SWCNT of 1.5 nm in diameter with 4*nm*-thick HfO_2 (k_1=16) and 5*nm* inter-CNT spacing, *Cox_e=246* aF/µm, and *Cox_m=186* aF/µm. The substrate-to-gate capacitance C_{sub} can either be calculated similarly if a double-gate device is desired or be calculated with the simple equation $C_{sub} = 2\pi k_2 \varepsilon 0/ln(2H_{sub}/r)$.

For a long-channel device (*Lg>>100 nm*), the wavenumber k_l can be represented as a continuous variable. By replacing the inner summation with the integral function and assuming $T_{LR}=T_{RL}=T_m$, can be simplified as

$$I_{semi}(V_{ch,DS}, V_{ch,GS}) \approx \frac{4e^2}{h} \sum_{\substack{k_m \\ m=1}}^{M} \left[V_{ch,DS} + \frac{KT}{e} \ln\left(\frac{1+e^{\left(E_{m,0}-\Delta\Phi_B\right)/KT}}{1+e^{\left(E_{m,0}-\Delta\Phi_B+eV_{ch,DS}\right)/KT}} \right) \right] \quad (4.13)$$

The previous equations utilize the approximated SWCNT band structure which is valid in the range $E_{m,l}>> V_\pi$. A more accurate model can be obtained by replacing the simplified band structure with the tight binding model at the cost of the more intensive calculations (approximately three times) or an exact analytical form valid only for achiral CNTs. Little difference is found for both the E–k relationship and the current drive in low-energy range. The chirality difference for SWCNTs with the same diameter can also be ignored, for our purpose, in the range where the carrier energy is less than 1.0*eV*.

4.3.2 Current Contributed by Metallic Subbands

For metallic subbands of metallic nanotubes, the current includes both the electron and hole currents

$$I_{metal} = 2(1-m_0)T_{metal}\sum_{\substack{k_l \\ l=1}}^{L}\left[J_{ele_0,l} + J_{hole_0,l}\right] \tag{4.14a}$$

$$J_{ele_0,l} = \frac{2e}{h}\frac{\sqrt{3}a\pi V_\pi}{L_g}(f_{FD}(E_{0,l} - \Delta\Phi_B) - f_{FD}(E_{0,l} + eV_{ch,DS} - \Delta\Phi_B)) \tag{4.14b}$$

$$J_{hole_0,l} = \frac{2e}{h}\frac{\sqrt{3}a\pi V_\pi}{L_g}(f_{FD}(-E_{0,l} - \Delta\Phi_B) - f_{FD}(-E_{0,l} + eV_{ch,DS} - \Delta\Phi_B)) \tag{4.14c}$$

The transmission probability T_{metal} is given by,

$$T_{metal} = \frac{\lambda_{ap}\lambda_{op}}{\lambda_{ap}\lambda_{op} + (\lambda_{ap} + \lambda_{op}).L_g} \tag{4.15}$$

If the summation function is replaced with an integral, can be simplified to

$$I_{metal} = (1-m_0)\frac{4e^2}{h}T_{metal}V_{ch,DS} \tag{4.16}$$

Thus, I_{metal} is independent of the channel surface-potential change $\Delta\Phi_B$ as expected because the DOS of metallic CNT is independent of the carrier energy. For metallic CNTs of less than 3 nm in diameter, the half band gap of the first semiconducting subband is larger than 0.43*eV*. Considering the large quantum capacitance of metallic CNT and the typical gate electrostatic capacitance discussed in Section following, the semiconducting subbands in a metallic CNT are not likely to be populated in and thereby contribute to the current with sub-1-V power supply.

4.3.3 Band to Band Tunneling Current

In the sub-threshold region, especially with negative gate bias (nFET), the band-to-band tunneling (BTBT) current from drain to source becomes significant. We include a voltage controlled

current source I_{btbt} in the device model in order to evaluate the device sub-threshold behavior and the static power consumption.

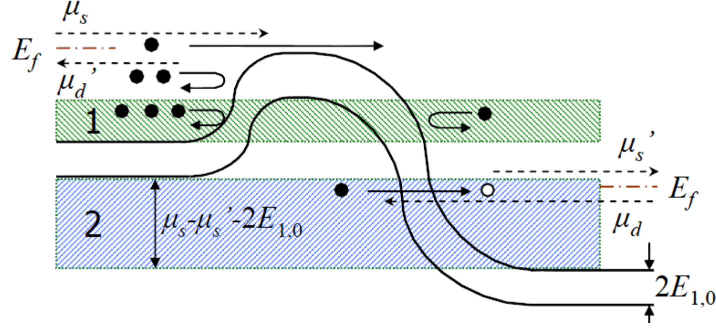


Figure 4.4: Energy-band diagrams (only the first subband is shown) and the associated Fermi levels at the source/drain side for NFET with moderate gate/drain bias. There are two possible tunneling regions: regions 1and 2, which are shaded on the plot. We only consider the tunneling through region 2 in this chapter.

As shown in Figure 4.3, there are two possible tunneling regions: the "n" shape region 1 and the "L" shape region 2. With $V_{ch,DS} > E1,0$, the tunneling through the drain junction in region 1 causes holes (electrons) pile up in the nFET (pFET) channel region because the source junction prohibits the holes (electrons) from escaping away. The hole (electron) pile up results in surface potential lowering and thereby a higher current and worse subthreshold behavior [32]. This mechanism depends on the drain junction electrical field and thereby the doping profile. A gradual drain junction doping profile helps relieve this effect by spreading the potential drop over a longer distance. Little such effect is observed for well-tempered devices. To simplify the modeling, we ignore this effect in this work. Because the tunneling through the source junction in region 1 is prohibited, we only consider the BTBT current through the drain junction in region 2. There are two prerequisites for tunneling to occur in region 2: First, the conduction band at the drain side is below the valance band at source side, i.e $Vch,DS > 2Em,0$ where $Em,0$ is the half band gap of the mth sub-band; and second, there are enough empty states at the drain side to accept the carriers that tunnel from the source/channel region. Assuming ballistic transport for the tunneling process, the BTBT current is approximated by the BTBT tunneling probability (Tbtbt) times the maximum possible tunneling current integrating from the conduction band at drain side up to the valance band at source side,

$$I_{btbt} \approx \sum_{\substack{k_m \\ m=1}}^{M} T_{btbt} \frac{4e}{h} \int_{E_{m,0}-E_f}^{V_{ch,DS}-E_{m,0}-E_f} \left(1 - f_{FD}(E)\right).dE \tag{4.17}$$

Ef is the Fermi level of the doped source/drain nanotube in units of eV. Applying the Fermi-Dirac function from equation 4.5b in the above equation, we obtain,

$$I_{btbt} = \frac{4e}{h} kT. \sum_{\substack{k_m \\ m=1}}^{M} \left[T_{btbt} \ln \left(\frac{1+e^{\left(E_{ch,DS}-E_{m,0}-E_f\right)/kT}}{1+e^{\left(E_{m,0}-E_f\right)/kT}} \right) . \frac{\max\left(eV_{ch,DS}-2E_{m,0},0\right)}{eV_{ch,DS}-2E_{m,0}} \right] \quad (4.18)$$

Following the work of Kane [24,25], the WKB-like transmission coefficient is given by,

$$I_{btbt} \approx \frac{\pi^2}{9} \exp\left(-\frac{\pi m^{*(1/2)}\left(\eta_m 2E_{m,0}\right)}{2^{3/2} e.\hbar.F} \right) \quad (4.19)$$

The "perpendicular energy" part in [25] is ignored in this case because the motion of the carriers in 1-D quantum wire is confined along the channel direction. $2E_{m,0}$ is the band gap, and η_m is a fitting parameter, set to 0.5 in this work, which represents the band gap narrowing effect under high electrical field [26,27]. m^* is the effective electron mass, defined as $\hbar^2/(\partial E_{m,l}/\partial k_l^2)$. Applying equation (4.3) and approximating the effective mass near the bottom of the sub-bands, we obtain,

$$m^* \approx \frac{2\hbar k_m}{\sqrt{3}.a.V_\pi} \quad (4.20)$$

m^* is about $0.05m_o$ and $0.10m_o$ for the carriers in the 1st and the 2nd (semiconducting) subband, respectively, where m_o is the electron rest mass. F is the electrical field triggering the tunneling process near the drain side junction; we normalize the total potential drop across the channel-drain junction to a fitting parameter, l_{relax}, assuming the potential difference relaxes over the distance l_{relax},

$$F = \frac{V_{ch,DS} + E_f - \Delta\Phi_B}{l_{relax}} \quad (4.21)$$

l_{relax} affects both BTBT current slope and its magnitude. The default value is set to 40 *nm* to match the BTBT current slope vs. V_{gs} of MOSFET-like CNFET in [2].

4.4 Transcapacitance network

To model the intrinsic ac response of CNFET device, we use a controlled transcapacitance array among the four electrodes (G,S,D and B) with the Meyer capacitor model [28]. C_{IJ} is the mathematically derived transcapacitance per unit gate length *(Lg)* between the nodes i and j, which is defined as $|\partial Q_I/\partial V_J|$. The actual transcapacitance in the channel region is $C_{ij} = C_{IJ}.L_g$ [Figure 4.2(a)].

First, we consider the source/drain capacitance with respect to the gate/substrate voltage variation. There are two methods to assign the charges in the channel region to the source and the drain: 1) Assuming a near-ballistic transport in the channel, the carrier distribution along the channel should be almost uniform, i.e., $Q_{s,\mathrm{ch}} \approx Q_{d,\mathrm{ch}} = Q_{\mathrm{cap}}/2 = Q_{\mathrm{CNT}}/2$. 2) All the carriers from $+k$ branches are assigned to the source, and all the carriers from $-k$ branches are assigned to the drain. The first approach is more

reasonable in representing the physical meaning of the capacitor (a carrier reservoir which does not distinguish where the carriers come from), whereas it may result in $C_{ij} \neq C_{ji}$. We first discuss the former (charge separation) approach which results in the equivalent circuit model in Figure 4.2(a). All the carriers in both the channel region and the source/drain nodes [Fig. 4.3(b)] come from the (external) source and drain electrodes; thus $Q_S = L_g \cdot (Q_{\text{cap}}/2 + (1-\beta)C_c \cdot \Delta\Phi_B)$, and $Q_D = L_g \cdot (Q_{\text{cap}}/2 + \beta C_c(\Delta\Phi_B - V_{\text{DS}}))$. We denote the total electrostatic coupling capacitance per unit length between the channel and other electrodes as $C_{\text{tot}} = C_{\text{ox}} + C_{\text{sub}} + C_c$. Taking the partial derivative of Q_S and Q_D over V_G, we obtain

$$C_{sg} = \frac{L_g}{2}\left(C_{ox} - \frac{1}{e}\frac{C_{tot} - 2(1-\beta)C_c}{\partial V_G / \partial \Delta\Phi_B}\right) \tag{4.23a}$$

$$C_{gd} = \frac{L_g}{2}\left(C_{ox} - \frac{1}{e}\frac{C_{tot} - 2\beta C_c}{\partial V_G / \partial \Delta\Phi_B}\right) \tag{4.23b}$$

where $\partial V_G / \partial \Delta\Phi_B$ can be calculated by equating $\partial Q_{cap} / \partial \Delta\Phi_B$ and $\partial Q_{CNT} / \partial \Delta\Phi_B$ with fixed $V_{ch,S}$, $V_{ch,D}$, and V_B using (4.12b) and (4.12c).

$$\frac{\partial V_G}{\partial \Delta\Phi_B} = \frac{1}{EC_{ox}}\left(C_{tot} + C_{Qs} + C_{Qd}\right) \tag{4.24a}$$

$$C_{Qs} = \frac{4e^2}{L_g.kT}\sum_{\substack{k_m \\ m=0}}^{M}\sum_{\substack{k_l \\ l=0}}^{L}\left[\frac{e^{(E_{m,l}-\Delta\Phi_B)/kT}}{\left(1+e^{(E_{m,l}-\Delta\Phi_B)/kT}\right)^2}\right] \tag{4.24b}$$

$$C_{Qd} = \frac{4e^2}{L_g.kT}\sum_{\substack{k_m \\ m=0}}^{M}\sum_{\substack{k_l \\ l=0}}^{L}\left[\frac{e^{(E_{m,l}-\Delta\Phi_B+eV_{ch,DS})/kT}}{\left(1+e^{(E_{m,l}-\Delta\Phi_B+eV_{ch,DS})/kT}\right)^2}\right] \tag{4.24c}$$

We define C_{Qs} and C_{Qd} as the quantum capacitance due to the carriers from source ($+k$ branch) and drain ($-k$ branch), respectively. With small gate bias ($E_{m,0}<\Delta\Phi_B$), $\partial V_G/\partial\Delta\Phi_B \approx C_{\text{tot}}/(eC_{\text{ox}})$; thus, the channel acts as a linear voltage divider which has little dependence on quantum capacitance. With large gate bias ($E_{m,0}< \Delta\Phi_B$), $\partial V_G/\partial\Delta\Phi_B > C_{\text{tot}}/(eC_{\text{ox}})$; therefore, the surface potential will be limited by the quantum capacitance. With (23) and (24), we obtain

$$C_{sg} = \frac{L_g C_{ox}}{2}\frac{C_{Qs} + C_{Qd} + 2(1-\beta)C_c}{C_{tot} + C_{Qs} + C_{Qd}} \tag{4.25a}$$

$$C_{dg} = \frac{L_g C_{ox}}{2}\frac{C_{Qs} + C_{Qd} + 2\beta C_c}{C_{tot} + C_{Qs} + C_{Qd}} \tag{4.25b}$$

We can follow a similar approach to calculate the capacitance C_{sb} and C_{db} as $C_{\text{sb}} = C_{\text{sg}} \cdot (C_{\text{sub}}/C_{\text{ox}})$ and $C_{\text{db}} = C_{\text{dg}} \cdot (C_{\text{sub}}/C_{\text{ox}})$, respectively. The charges accumulated on the gate and substrate (back gate) electrodes

are given by $Q_G = L_g \cdot C_{ox} \cdot (V_{GS} - V_{FB} - \Delta\Phi_B)$ and $Q_B = L_g \cdot C_{sub} \cdot (V_{BS} - \Delta\Phi_B)$, respectively. With a similar approach, the coupling capacitance between the gate and the substrate is derived as

$$C_{bg} = C_{gb} = \frac{L_g C_{sub} C_{ox}}{C_{tot} + C_{Qs} + C_{Qd}} \tag{2.26}$$

Next, we consider the gate/substrate capacitance due to source/drain voltage variation. With similar approach as the earlier one, we obtain

$$C_{gs} = \frac{L_g C_{ox} \left[C_{Qs} + (1-\beta) C_c \right]}{C_{tot} + C_{Qs} + C_{Qd}} \tag{4.27a}$$

$$C_{gd} = \frac{L_g C_{ox} \left[C_{Qd} + \beta C_c \right]}{C_{tot} + C_{Qs} + C_{Qd}} \tag{4.27a}$$

$$C_{bs} = C_{gs} \frac{C_{sub}}{C_{ox}} \tag{4.27c}$$

$$C_{bd} = C_{gd} \frac{C_{sub}}{C_{ox}} \tag{4.27d}$$

The earlier equations give the values of the nine capacitors in Figure 4.2(a). If we use the second channel charge-separation approach (+k carriers for source and −k carriers for drain), reciprocality is guaranteed, and Csg = Cgs, Cdg = Cgd, Csb = Cbs, and Cdb = Cbd; thus, the gate-capacitance network can be simply represented by the five-capacitor model in Fig. 4.2(b), or by the six-capacitor model, as shown in Figure 4.2(c), which shows explicitly the electrostatic and quantum capacitances with the same transfer function as the five-capacitor model.

This chapter presented a circuit-compatible compact model of the intrinsic channel region of MOSFET-like SWCNFETs including some channel region nonidealities. Comparison with a more accurate device model using the tight binding band-structure model shows that this model is valid for CNFET with a wide range of chiralities and diameters. This model uses a substate summation approach, instead of the integral, to calculate the parameters. This approach makes the modeling methodology described in this chapter to be generally applicable to other 1-D devices, e.g., silicon nanowire FET, and requires less computation efforts, thereby making it more compatible with a circuit simulator. The complete dynamic gate-capacitance network makes the model suitable for both small- (analog) and large signal (digital) applications. This model serves as a starting point toward the complete CNFET-device model, including the device/circuit-level nonidealities and multiple CNTs, which is reported in the next chapter.

Chapter 5

COMPLETE DEVICE MODEL AND CIRCUIT PERFORMANCE

In addition to the nonidealities included in the chapter 4, this chapter includes the elastic scattering in the channel region, the resistive source/drain (S/D), the Schottky-barrier resistance, and the parasitic gate capacitances. More than one nanotube per device can be modeled. Compared to silicon technology, the CNFETs show much better device performance based on the intrinsic *CV/I* gate-delay metric (six times for nFET and 14 times for pFET) than the MOSFET device at the 32-nm node, even with device nonidealities. This large speed improvement is significantly degraded (by a factor of five to eight) by interconnect capacitance in a real circuit environment. We performed circuit-performance comparison with all the standard digital library cells between CMOS random logic and CNFET random logic with HSPICE simulation. Compared to CMOS circuits, the CNFET circuits with one to ten carbon nanotubes per device is about two to ten times faster, the energy consumption per cycle is about seven to two times lower, and the energy-delay product is about 15–20 times lower, considering the realistic layout pattern and the interconnect wiring capacitance.

5.1 Circuit Topology

A MOSFET-like CNFET device structure (Figure 4.1a) is used for the modeling and this chapter because of both the fabrication feasibility and superior device performance of the MOSFET-like CNFET as compared to the Schottky Barrier (SB)-controlled FET. The complete CNFET device model is implemented hierarchically in three levels (Figure 5.1). Device nonidealities are included hierarchically at each level. Level 1, denoted as CNFET_L1, models the intrinsic behavior of MOSFET like CNFET. The model at this level is similar to the device level models such as those in [27] and [28]. The second level, denoted as CNFET_L2, includes the device nonidealities: the capacitance and resistance of the doped S/D CNT region, as well as the possible SB resistances of S/D contacts. The first two levels deal with only one CNT under the gate. The top level, denoted as CNFET_L3, models the interface between the CNFET device and the CNFET circuits. This level deals with multiple CNTs per device and includes the parasitic gate capacitance and screening due to the adjacent CNTs. This chapter presents the second- and third-level model as an extension to the first-level model CNFET_L1 in chapter 4.

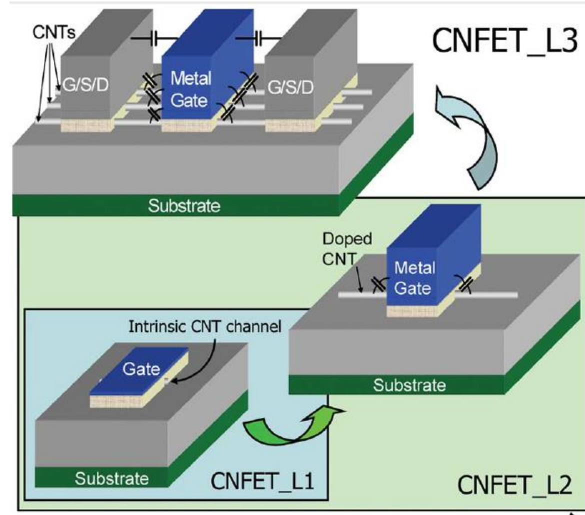
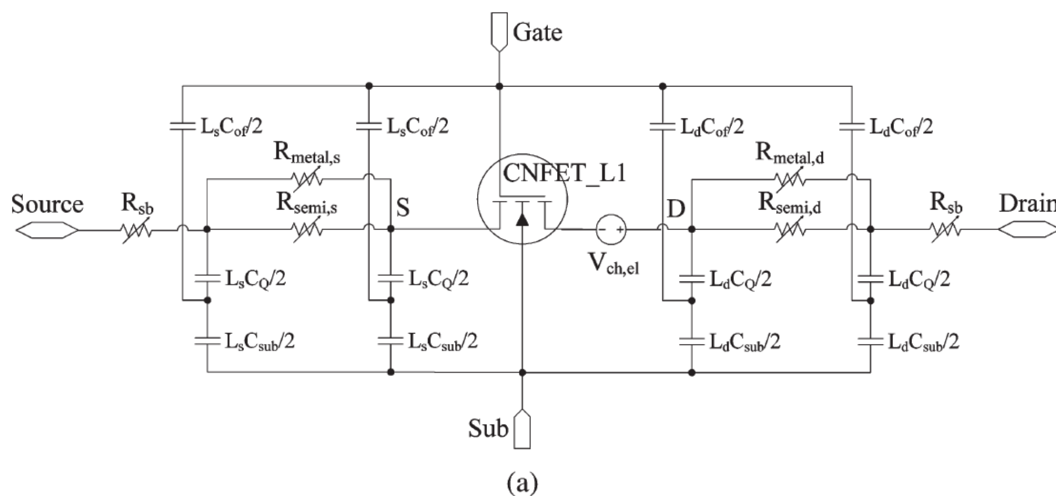


Figure 5.1: Complete CNFET device model is implemented with hierarchical three levels. Level 1, CNFET_L1, models the intrinsic behavior of CNFET. The second level, CNFET_L2, includes the device nonidealities. The first two levels deal with only one CNT under the gate. The top level, CNFET_L3, models the interface between the CNFET device and CNFET circuits. This level deals with multiple CNTs per device and includes the parasitic gate capacitance and screening due to adjacent CNTs.

5.2 Device Model- The Second Level

As an extension to the first-level CNFET model CNFET_L1 of the intrinsic channel region in chapter 4, this level models the device nonidealities, including the elastic scattering in the channel region, the quantum/series resistance and the parasitic capacitance of the doped S/D region, as well as the SB resistance at the interface between the doped CNT and the S/D metal contacts. The equivalent circuit diagram is shown in Figure 5.2.



(a)

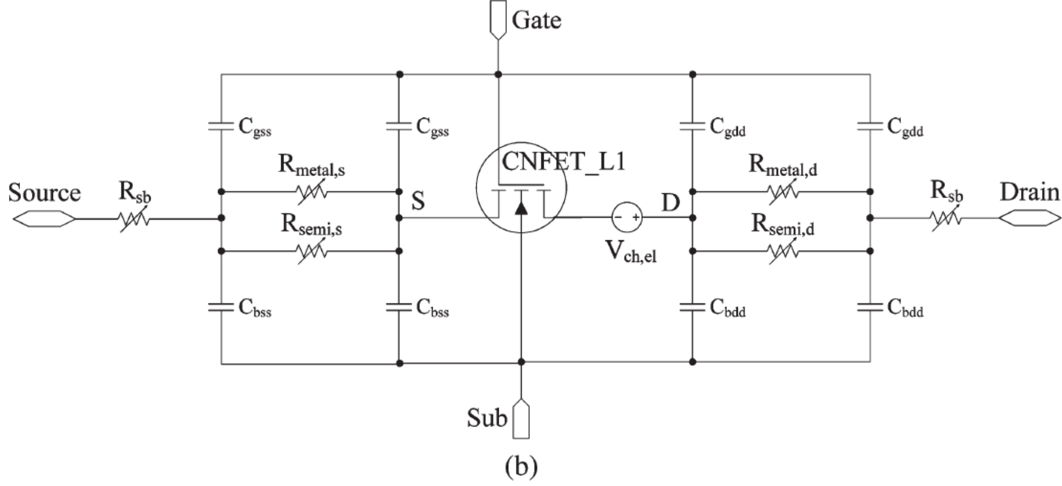


Figure 5.2: Second-level equivalent circuit model CNFET_L2 for CNFET.

(a) The six-capacitor model and (b) the four-capacitor model.

5.2.1 Channel Resistance

We consider three typical scattering mechanisms in the channel region: 1) acoustic phonon scattering (near elastic process [33]); 2) optical phonon scattering (inelastic process [33]); and 3) elastic scattering. Both the acoustic phonon scattering and optical phonon scattering are treated in the first-level device modeling [30]. The elastic-scattering rate and thereby the MFP are assumed to be independent of the carrier energy. We include the elastic scattering in this chapter in a computationally efficient way. Although the elastic-scattering MFP of the intrinsic CNT can be longer than 1 μm, the fabricated CNTs often contain nonideal scattering centers (e.g., defects) which may degrade the MFP significantly and, in turn, cause additional potential drop along the channel region. The total potential drop (V_{DS}) across the channel region is a summation of the potential drop ($V_{\mathrm{ch,DS}}$) due to the channel quantum resistance $R_{\mathrm{ch},c}$ and the potential drop ($V_{\mathrm{ch,el}}$) over the channel resistance $R_{\mathrm{ch,el}}$ due to the elastic scattering (Figure 5.3), i.e., $V_{\mathrm{DS}} = V_{\mathrm{ch,DS}} + V_{\mathrm{ch,el}}$, $V_{\mathrm{ch,DS}} = I_{\mathrm{DS}}R_{\mathrm{ch},c}$, and $V_{\mathrm{ch,el}} = I_{\mathrm{DS}}R_{\mathrm{ch,el}}$. $R_{\mathrm{ch,el}}$ is equal to $(1 - T_{\mathrm{ch}})/T_{\mathrm{ch}} \cdot R_{\mathrm{ch},c}$, where T_{ch} is the transmission probability in the channel region, $T_{\mathrm{ch}} = l_{\mathrm{eff}}/(L_g + l_{\mathrm{eff}})$, and L_g and l_{eff} are the channel length and the effective elastic-scattering MFP, respectively. We further assume that MFP l_{eff} is linearly proportional to the nanotube's diameter, i.e., $l_{\mathrm{eff}} = D_{\mathrm{CNT}}/(1.5\ \mathrm{nm}) \cdot \lambda_{\mathrm{eff}}$, where D_{CNT} is the CNT diameter, and λ_{eff} (~200 nm [31]) is the elastic-scattering MFP for 1.5 nm in diameter CNT. With the aforementioned equations, we can represent the potential drop over $R_{\mathrm{ch,el}}$ as

$$V_{ch,el} = \frac{L_g}{L_g + \frac{D_{CNT}}{1.5nm}.\lambda_{eff}} V_{DS} \tag{5.1}$$

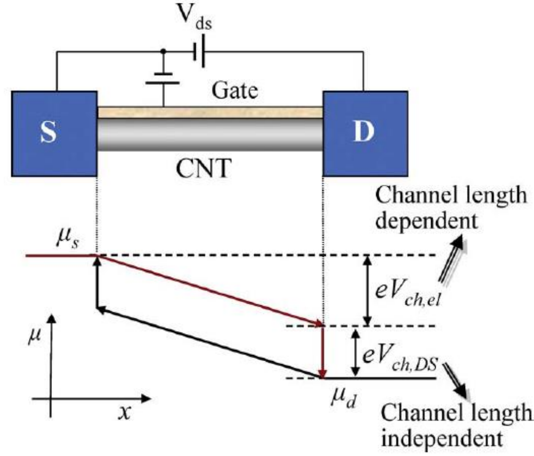


Figure 5.3: Fermi-level profile for 1-D device with series resistance (finite MFP along CNT). The Fermi-level profile is approximated as a linear function of the position along the channel.

Representing the effect of the channel resistance due to elastic scattering as a voltage-controlled voltage source $V_{\mathrm{ch,el}}$ (Figure 5.2) can avoid calculating $R_{\mathrm{ch,el}}$ directly, thereby simplifying the computation.

5.2.2 Doped S/D CNT

The heavily doped nanotube regions of the CNFET act as both the S/D extension region and the local interconnect between two adjacent devices. π model is used to represent the equivalent circuit of the doped S/D region (Figure 5.2).

Resistance: First, we discuss the model for the resistance of the doped CNT region. Similar to the channel region, the CNT can be either metallic or semiconducting. The S/D resistance is modeled as two paralleled resistors: $R_{\mathrm{semi},s}$ ($R_{\mathrm{semi},d}$) due to the semiconducting subbands and $R_{\mathrm{metal},s}$ ($R_{\mathrm{metal},d}$) due to the metallic subbands of the metallic nanotubes. We consider two typical cases for device connectivity: 1) The drain of one CNFET is connected to the source of another CNFET, i.e., the doped CNT acts as interconnect between two devices in series [Figure 5.4(a)] without a metal contact in between, and 2) the S/D of one CNFET is connected to the metal contact, e.g., at the output node [Fig. 4(b)]. For the first case, the two segment doped nanotubes should be the same as one continuous doped nanotube in the model, i.e., the potential profile along the two segments is continuous [Fig. 4(a)]. Furthermore, we describe the device intrinsic behavior with S/D input Fermi levels (μs, μd) as mentioned earlier, whereas the input source Fermi level μs of one device is connected to the output source Fermi level μ_s of another device [Figure 5.4]. Thus, it is needed to convert the output port of the equivalent circuit model from μd to μ_s for this case. For the second case, the ideal metal contact is an electron reservoir that has infinite density of state (DOS) and acts as an infinite scattering center so that there is an additional

potential drop across the boundary between the doped CNT and the metal contact (called the quantum contact resistance) due to mode mismatch [Fig. 4(b)]. The device model is able to handle both cases correctly as described next. We define two parameters S_{out} (D_{out}) representing the S/D connectivity: they are equal to 0 if source (drain) is connected to the doped CNT; otherwise, they are equal to 1. Consider the Fermi-level profiles for both cases in Figure 5.4. Now we obtain the total effective resistance of the doped S/D region [30].

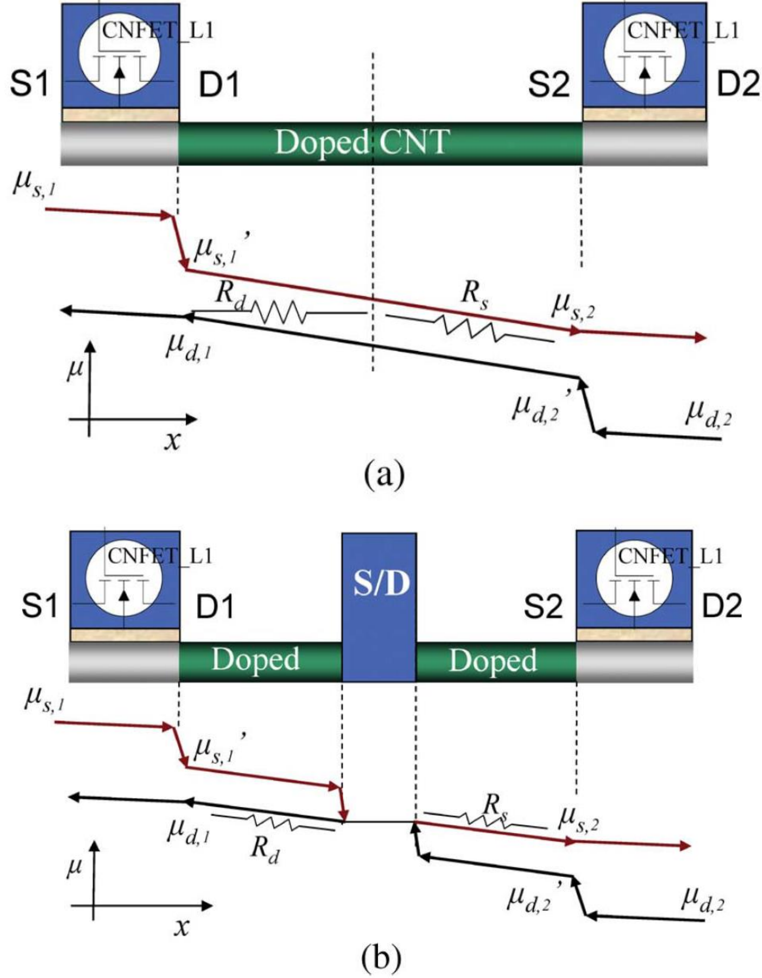


Figure 5.4: Related Fermi-level profiles for (a) two CNFETs that are connected with a doped CNT and (b) two CNFETs that are connected by an ideal metal contact (without considering the SBs between the CNT and metal interface).Superposed are the equivalent S/D resistors.

$$R_{x,s} = L_s / (\lambda_{sd} G_{x,c}) \tag{5.2a}$$

$$R_{x,d} = \eta_{deff} / G_{x,c} \tag{5.2b}$$

$$\eta_{deff} = \begin{cases} (L_d - \lambda_{sd}) / \lambda_{sd}, & D_{out} = 0 \\ L_d / \lambda_{sd}, & D_{out} = 1 \end{cases} \quad (5.2c)$$

The subscript x denotes either "semi" or "metal". L_s and L_d are the lengths of the doped source and drain regions, respectively. λ_{sd} is the impurity scattering MFP, assumed a constant with a default value of 15 nm, which is a pessimistic estimation, for degenerately doped nanotubes. A longer MFP, 20–50 nm, can be derived from the work in [20] with charge-transfer doping. $G_{x,c}$ is the quantum conductance of doped CNT. $G_{x,c}$ depends on CNT diameter, the doping level (E_f), and the S/D Fermi-level difference ($eV_c = |\mu_s - \mu_d|$). $G_{x,c}$ expression is mentioned in [30], for semiconducting subband given as

$$G_{semi,c}(V_c) = \frac{4e^2}{h} \sum_{\substack{k_m \\ m=1}}^{2} \left[1 + \frac{kT}{eV_c} \ln \left(\frac{1 + e^{(E_{m,0} - E_f - \Delta\Phi_B)/kT}}{1 + e^{(E_{m,0} - E_f - \Delta\Phi_B + eV_c)/kT}} \right) \right] \quad (5.3)$$

With small drain bias ($V_c < E_f - E_{1,0} + \Delta\Phi_{s,\max}$), $G_{\text{semi},c}$ can be approximated as a constant, $G_{\text{semi},c} \approx 4e^2/(m \cdot h)$, where m is the number of subbands below E_f . With large drain bias ($V_c > E_f - E_{1,0} + \Delta\Phi_{s,\max}$), e.g., in the saturation region, the maximum surface-potential change referred to μs will be pinned at $\Delta\Phi_{s,\max}$, and the drain Fermi level will be pushed below the first subband, which causes a rapid increase in resistance. Therefore, the S/D resistance increases with an increasing current (drain bias). On the other hand, the quantum conductance of the metallic subbands is almost independent of bias because the DOS is constant,

$$G_{metal,c} = (1 - m_0) \frac{4e^2}{h} \quad (5.4)$$

where $m0 = 0$ if $\text{mod}(n_1 - n_2, 3) = 0$ with (n_1, n_2) CNT; otherwise, it is equal to 1. The internal parameter V_c is related to the circuit parameter $V_{\text{series},s}$ or $V_{\text{series},d}$ (the potential drop over the series resistor at the source or drain side, respectively) by equation $V_c = V_{\text{series},d} / \eta_{\text{deff}} = V_{\text{series},s} \lambda_{\text{sd}} / L_s$. With the aforementioned equations, we are ready to calculate the S/D resistance as voltage-controlled resistors ($R_{\text{semi},s}$, $R_{\text{semi},d}$, $R_{\text{metal},s}$, and $R_{\text{metal},d}$).

Capacitance: Similar to the channel region in chapter 4, there are two implementations for the extrinsic capacitor network: 1) the six capacitor model that consists of the electrostatic capacitance and quantum capacitance [Figure 5.2(a)] or 2) the four-capacitor model with four transcapacitances [Figure 5.2(b)]. The two implementations are equivalent in terms of ac response. The four equivalent capacitances can be expressed in terms of the six physical capacitors in Fig. 2(a) by

$$C_{gzz} = \frac{L_z . C_{of} C_Q}{2(C_Q + C_{of} + C_{sub})} \quad (5.5a)$$

$$C_{bzz} = \frac{L_z . C_{sub} C_Q}{2(C_Q + C_{of} + C_{sub})} \quad (5.5b)$$

The subscript "z" denotes either "s" or "d"; thus L_z is the length of either source or drain. C_Q is the quantum capacitance of the doped S/D region. For the channel region, we need to model C_Q accurately because the gate capacitance (C_{ox}) is comparable with C_Q. However, for the heavily doped CNT region, C_Q (~400 aF/µm per subband) is typically much larger than the electrostatic capacitance (C_E) between CNT and ground (typically100aF/µm). Thus, we approximate C_Q to the first order as $C_Q = \left[\Theta(E_f - E_{1,0}) + \Theta(E_f - E_{2,0})\right] \times 400 aF / \mu m$ where Θ (x) is a step function that is equal to 1 if x > 0; otherwise, it is equal to 0. For multiple CNTs per gate, the gate outer-fringe capacitances (C_{of}) are grouped into the fringe capacitance between the gate and S/D CNT at the two edges (C_{of_e}) and into the fringe capacitance between the gate and S/D CNT in the middle (C_{of_m}) in this chapter, as described in [25].

SB Resistance: SB may exist at the interface between CNT and metal contact [34] and in CNT hetero-junctions between metallic and semiconducting CNTs . In this chapter, we use a simplified model to describe SB resistance between doped CNT and metallic electrode to include some signature effects of SB on device performance. We made the following simplifying assumptions in this model: 1) The doped CNT region is long enough so that there is no surface-potential modification due to the quantum confinement within a short CNT; 2) dipole effects are ignored; 3) there are no pinning effects [35]; and 4) the depletion profile is steep. Figure 5.5(a) shows an example of the potential profile of SB at the source side. In this simple model, we only consider tunneling through the first subband, assuming that the carriers injecting from the metal contact can redistribute over all the subbands near the contact region. The potential barriers seen by the carriers at the metal contact side (Φ_1) and the doped CNT side (Φ_2) are given by

$$\Phi_1 = \Phi_M - \Phi_C + E_{1,0} \quad (5.6a)$$

$$\Phi_2 = \begin{cases} \Phi_1 + \left|V_{sb,s}\right| + \Delta\Phi_s, & Source-SB \\ \Phi_1 - \left|V_{sb,d}\right| - V_c + \Delta\Phi_s, & Drain-SB \end{cases} \quad (5.6b)$$

$V_{sb,s}$ and $V_{sb,d}$ are the potential drops over the equivalent SB resistor at the source and drain sides, respectively, from the equivalent circuit point of view. Φ_M and Φ_C are the metal and CNT work functions, respectively. With positive bias V_{DS} and V_{GS}, the carriers of the source side see a higher SB,

whereas the carriers of the drain side see a lower SB. With doping level E_f , the normalized volume doping density is

$$N_D = \frac{32E_{1,0}^2}{3\pi^2 V_\pi^3 d^3}\sqrt{E_f^2 - E_{1,0}^2} \quad (5.7)$$

The depletion length is then approximately

$$W_d = \sqrt{\frac{2k_2\varepsilon_0}{eN_D}V_{bi}} \quad (5.9a)$$

Where

$$V_{bi} = E_f - E_{1,0} + \Phi_2 \quad (5.9b)$$

V_{bi} is the build in potential with an applied bias. For low doping level (< 2 × 10−4), the depletion width for CNT is micrometers or so, precluding a nanoscale device [23]. At high doping (> 10−3), the length scale becomes small enough so that the contact is essentially ohmic through tunneling. The conduction-band potential profile is

$$E_C(x) = \frac{eN_D(W_d - x)^2}{2k_2\varepsilon_0} + E_{1,0} - E_f - \Phi_1 + \Phi_2 \quad (5.10)$$

We approximate the potential profile with a triangular potential profile with the same classical turning points, 0,W_1 (before bias), and W_2 (after bias) shown in the Figure 5.5(a).

$$W_1 = \sqrt{\frac{2k_2\varepsilon_0}{eN_D}}\left(\sqrt{V_{bi}} - \sqrt{E_f - E_{1,0} + \Phi_1 - \Phi_2}\right) \quad (5.11a)$$

$$W_2 = \sqrt{\frac{2k_2\varepsilon_0}{eN_D}}\left(\sqrt{V_{bi}} - \sqrt{E_f - E_{1,0}}\right) \quad (5.11b)$$

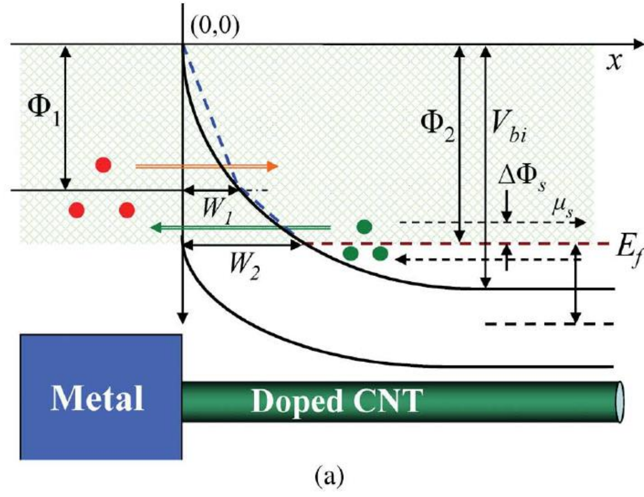
Using the Wentzel–Kramer–Brillouin approximation, we obtain the tunneling probability through a triangular potential barrier with height *v* and width *w*

$$\ln T \cong -2\int_0^w |k(x)|dx = -\frac{2\sqrt{2m}\times w\sqrt{v}}{3\hbar} - \frac{4w}{9r}\sqrt{\frac{2v}{E_{1,0}}} \quad (5.12)$$

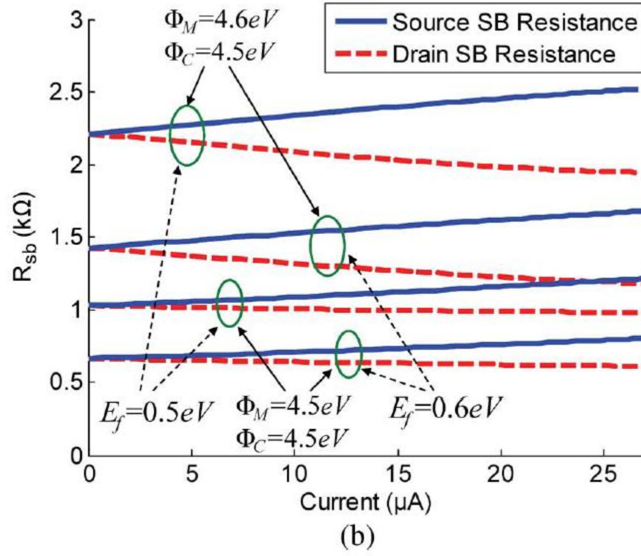
The average transmission probability through the first subband is approximately

$$T_{SB} \approx \frac{\int_{\Phi_1}^{\Phi_2} T\,dE}{\Phi_2 - \Phi_1} \approx \frac{2}{3(\Phi_2 - \Phi_1)\tau^{2/3}}\left[\Gamma\left(\frac{3}{2}, \tau.\Phi_1^{3/2}\right) - \Gamma\left(\frac{3}{2}, \tau.\Phi_2^{3/2}\right)\right] \quad (5.13a)$$

$$\tau \approx \frac{4\sqrt{2}W_2}{9r\sqrt{E_{1,0}.\Phi_2}} \quad (5.13b)$$



(a)



(b)

Figure 5.5: (a) The energy band diagram for the contacted metal and doped CNT with bias. The potential barrier in the tunneling region (shaded area) is approximated as a triangle potential barrier. (b) SB resistances as functions of the current, with different metal/CNT work functions and different CNT doping levels. Both smaller barrier height and higher CNT doping level help to reduce SB resistance significantly.

The potential barrier height Φ2 and thickness W_2 depend on the bias. With high degenerate doping which is satisfied in this chapter, to improve runtime, the prior equation can be approximated with

$$T_{SB} \approx 0.5 \times \left(\exp(-\tau.\Phi_1^{3/2}) + \exp(-\tau.\Phi_2^{3/2}) \right) \tag{5.14}$$

The equivalent SB series resistance is then given by

$$R_{sb} = \frac{1}{G_{semi,c}} \left(\frac{1}{T_{SB}} - 1 \right) \left(1 - X_{out} \right) \tag{5.15}$$

The symbol "X" denotes either "S" (source-side SB) or "D" (drain-side SB), which are defined as either 0 or 1 in previous section. The SB resistance is modeled as a voltage controlled resistor (Figure 5.2). The equations in this section are highly simplified and only valid for the heavily doped CNT, i.e., $E_f > E_{1,0}$; otherwise, the performance of CNFET will be heavily limited by S/D resistance which is out of the. With this model, we can observe that the source (drain) SB resistance increases (decreases) with an increased S/D current (increased V_{DS} and V_{GS}) due to the increased (reduced) SB seen by the carriers tunneling from the doped CNT to the metal contact shown in Figure 5.5(b). With high doping (~0.8%) and $\Phi_M = \Phi_C = 4.5$ eV, the SB resistance can be suppressed to a small value (< 1 kΩ) compared with the typical device resistance (~40 kΩ); thus, it can be ignored in most applications if this high level of doping can be achieved experimentally.

5.3 Device Model-The Third Level

This level is the top level of the device model, which allows for multiple CNTs for each device (Fig. 5.6). Consider the case where there are NCNTs under the gate. The CNTs are grouped into 1) a number of *min(N,2)* CNTs at the two edges and 2) the other *(N-min(N, 2))* CNTs in the middle. The direct coupling capacitance (Cgsub) between the gate and the substrate is simply expressed as $C_{gsub} \approx 2\pi L_g k_2 \varepsilon_0 / \ln(4H_{sub} / H_{gate})$, where Hsub is the insulating bulk thickness, and Hgate is the gate height. Cgsub is about 1 aF, about one-third of the gate intrinsic capacitance, assuming a 10-µm-thick SiO2 bulk, a 64-nm gate height and a 32-nm channel length, and an infinitely large substrate.

5.4 Gate and Interconnect Parasitic Capacitances

To be compatible with the CMOS process, we assume that the CNFET circuits use the same conventional metal interconnect technology (the feature size is defined by photolithography) as that for silicon technology. Consider the layout in Figure 5.1; the parasitic gate capacitance between the gate and the adjacent gate/S/D contacts per unit length is given by (5.15) in [25]. For devices at 32-*nm* node (L_{sd} = 32 *nm*, L_g= 32 *nm*, H_{gate}= 64 *nm*, and k_2 = 3.9), Cgtg is about 110 *aF/µm* for one side (each gate has two sides). Thus, C_{gtg} of such a device with 32-nm gate width is about 11 *aF* (including the Miller effect), which is more than twice larger than the intrinsic gate capacitance (~ 4 aF per CNT channel). Therefore, it is very important to include the extrinsic parasitic capacitances for ac performance evaluation.

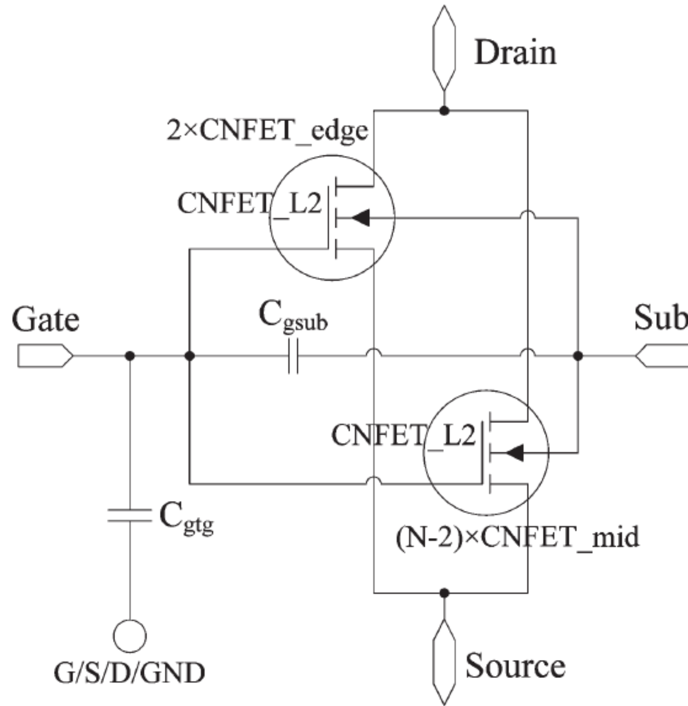


Figure 5.6:. Third-level equivalent circuit model CNFET_L3 for CNFET. There are N nanotubes under the gate. These CNTs are grouped into 1) a number of min(N, 2) CNTs at the two edges and 2) the other N − min(N, 2) CNTs in the middle. All CNTs in each group are treated identically. Cgtg is the parasitic gate coupling capacitance connected between the gate and the S/D/ground or the gate of the adjacent devices, according to the device layout.

5.5 CNFET Device and Circuit Performance

In this section, we compare our model with experimental data and use the model to project circuit performance of CNFET circuits. The aforementioned model is implemented in HSPICE. Both the dc and ac performances evaluated with the device model match well with the experimental data. The observable 10% mismatch between the simulation and the experimental data may due to two reasons: 1) this model uses a simplified band structure. This may introduce inaccuracy for the DOS, which will affect the transconductance. 2) We assume a linear potential profile in both the channel region and the S/D region, which may not be accurate enough for the fabricated device. Next, we evaluate the CNFET device and circuit performance at the 32-nm node with a 0.9-V power supply for high-performance logic. All CNTs are assumed to be (19, 0) semiconducting CNTs with 1.5-nm diameter and 0.6-eV (~0.8%) S/D

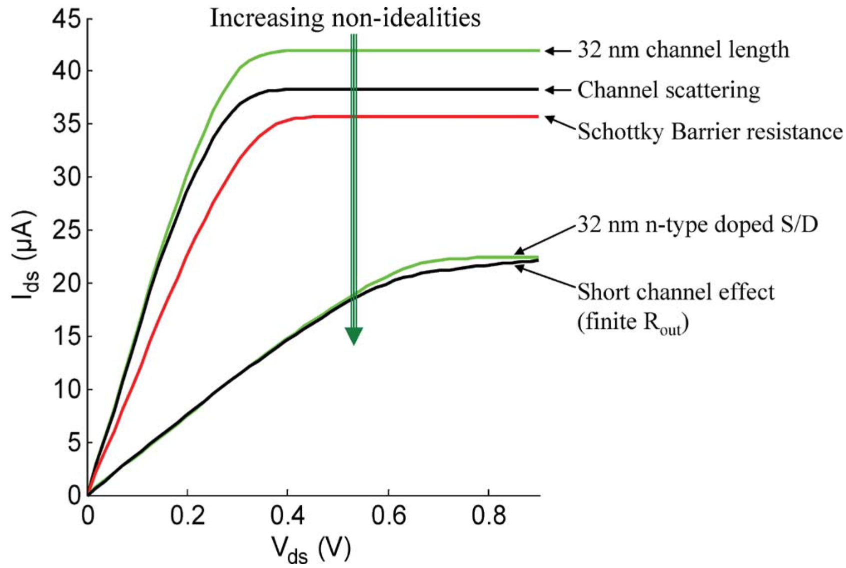
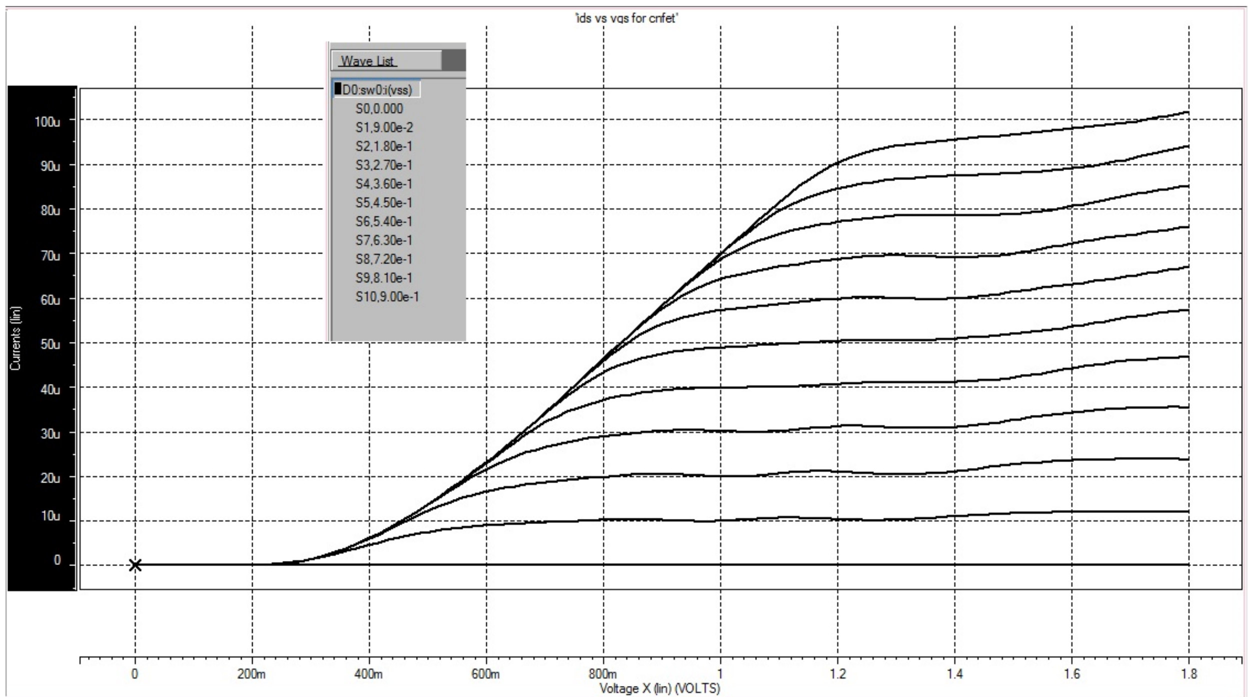
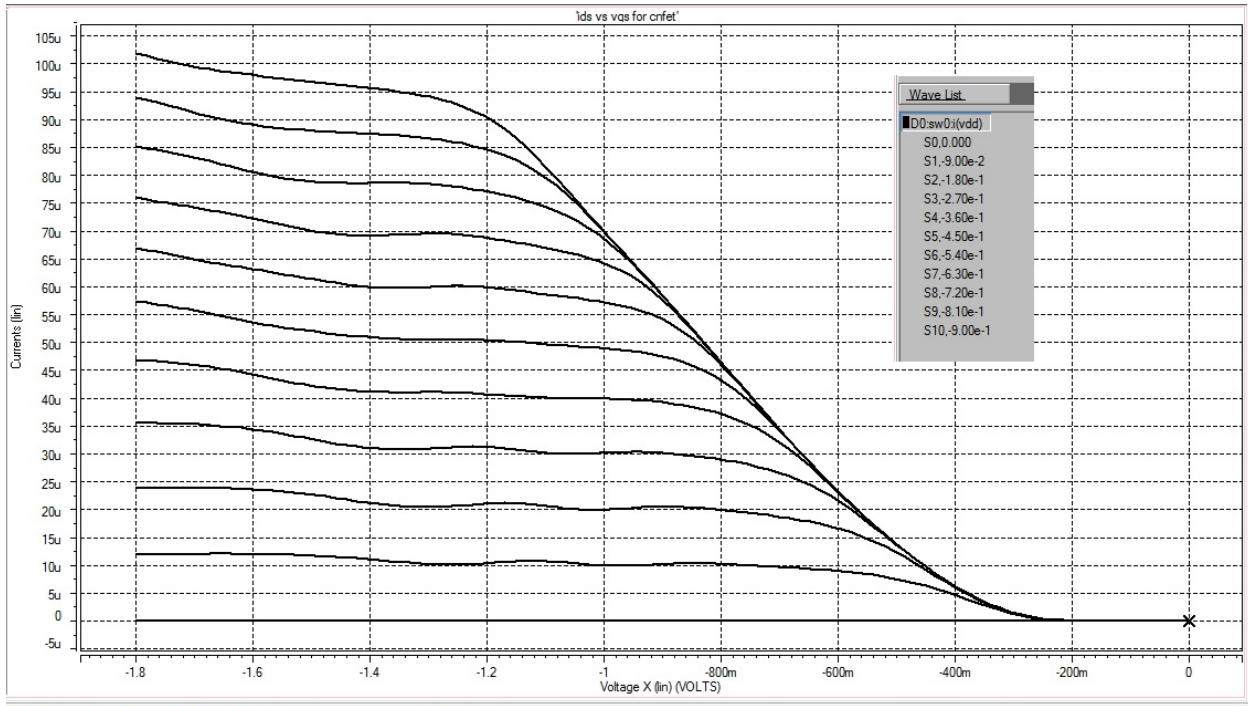


Figure 5.7: Drain current at (Vgs = 0.9 V, VFB = 0 V) for (19, 0) chiralityCNFETs with incremental device nonidealities. The front-gate dielectric is a3-nm-thick HfO2, and the insulating bulk is a 10-ìm-thick SiO2. The metaland CNT work functions are 4.6 and 4.5 eV, respectively.

doping level3 unless otherwise specified. The gate dielectric is a 3-nm-thick HfO2 (dielectric constant k1 = 16) on top of 10-μm-thick SiO2. The metal work function is assumed to be the same as the CNT work function (4.5 eV). Fig. 8 shows the device current in the presence of nonidealities. The ballistic current of a 32-nm-gate-length CNFET is about 42 μA. The scattering in the channel region decreases the ON-current by about 10%.



(a)



(b)

Figure 5.8: Device performance HSPICE simulation - (a) NCNFET and (b) PCNFET, with multitubule channel and supply range for 0 to 1.8 V

(Even though the device is designed to perform in sub-1 volt range)

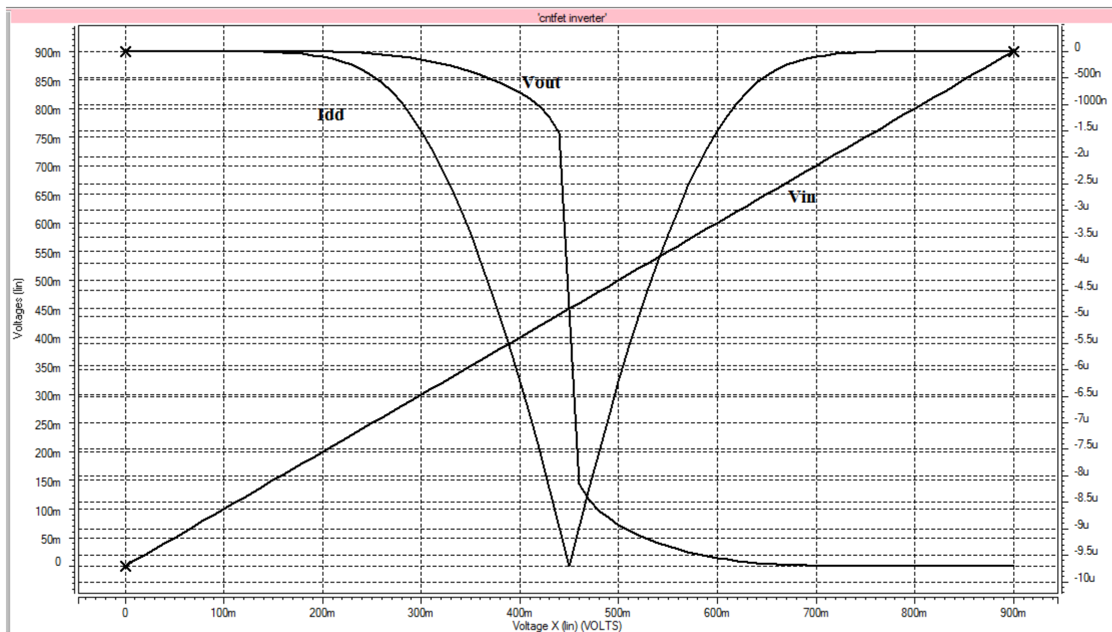


Figure 5.9: CNFET inverter simulation in HSPICE with Vdd=0.9V

with maximum instantaneous power dissipation of 8.73µw and also introduce 13.6ps delay

Table 5.1: performance of CNFET over MOS

$L_{channel}$=18nm	Gate C_{eff}	I_{off}(nA/fF)	I_{on}(mA/fF)	I_{on}/I_{off}	CNFET/MOS
nMOS	1.1fF/µm	383	1.2	3.1x103	N/A
nCNFET	3.6aF/FET	383	7.2	1.9x104	6
pMOS	1.1fF/µm	253	0.5	2.1x103	N/A
pCNFET	3.6aF/FET	253	7.1	2.8x104	14

The SB resistance further reduces the ON-current by another 5%. The largest current-drive detractor is the S/D series resistance due to the heavily doped CNTs, which reduces the ON-current to 22 μA. Compared to silicon bulk CMOS technology (benchmarked with the BSIM4 predictive model [36]), the CNFET shows better single device performance based on the intrinsic *CV/I* gate-delay metric (six times for nFET and 14 times for pFET) than the MOSFET (where *C* is the intrinsic gate capacitance) in the 32-nm node, even with device nonidealities (Table 5.2). The device-performance improvement (six times for nFET) is smaller than the value (approximately 13 times) reported in [30] because the current is degraded by about a factor of two due to the S/D extension resistance and SB resistance, considering the actual device layout.

Chapter 6

HSPICE AND ANALOG BEHAVOUR MODELLING OF CNTFET

This chapter is about the behavioural modeling of CNTFET in HSPICE. At first we will see the basics of HSPICE toolbar, used in modeling of the device. Thereafter we will go through the library file briefly to have an idea of the device model. Though, the complete program is not mentioned in this chapter but it has been implemented thoroughly.

6.1 HSPICE Introduction

HSPICE is an analog circuit simulator copyright ©2007 of SYNOPSYS, Inc. (similar to Berkeley's SPICE-3) capable of performing transient, steady state, and frequency domain analyses. Existing SPICE decks created for SPICE- 3 can be easily modified to run under HSPICE, or can be rewritten to take advantage of features not available in SPICE-3. HSPICE generally has better convergence than SPICE-3 and, because it is a commercial product (from Meta-Software), is better supported. It also allows hierarchical node naming, circuit optimization, input, output, and behavioral algebraics for parameterized cells, and interactive waveform viewing with MetaWaves.

6.1.1 Installation of setup

This section will introduce few steps to install (only in all versions of Microsoft windows above XP) the set of SYNOPSYS version 2008.03, used for simulation in this thesis:

1. Install Hspice V-2008.03
2. Copy HSPICERF.EXE from crack directory to ..\Bin directory
3. Copy the license files from Crack directory to C:\Flexlm
4. Modify the environment variable "LM_LICENSE_FILE" to point to the license file. For example: C:\Flexlm\Hspice_2007-09.lic

6.1.2 Running simulations

For running the programming the spice codes in HSPICE the following steps are to be followed:

1. Write the netlist for the required circuit in notepad.

2. Save the notepad with extension **.sp**.
3. Copy the netlist file in a common folder wherever the library files for the CNTFET are.
4. Run the installed setup of **Hspui A 2008.03** from the start menu.
5. Open the netlist file from the **Hspui A 2008.03** window and load (Figure 6.1).

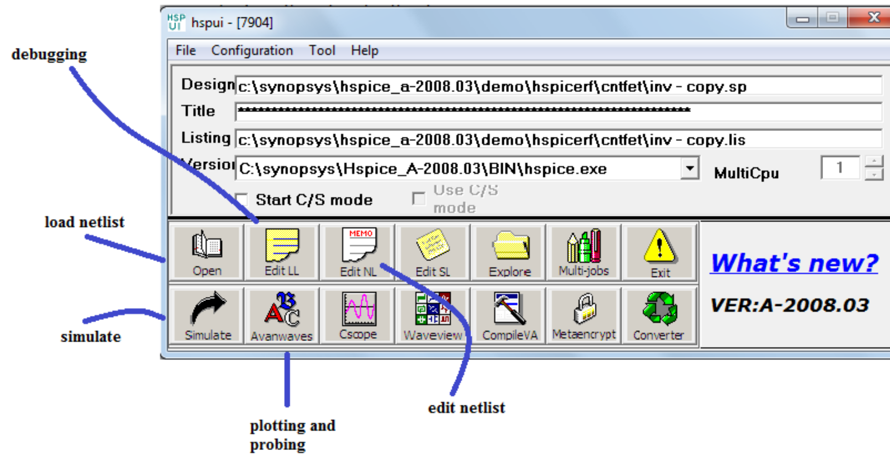


Figure 6.1: Simulation of netlist.

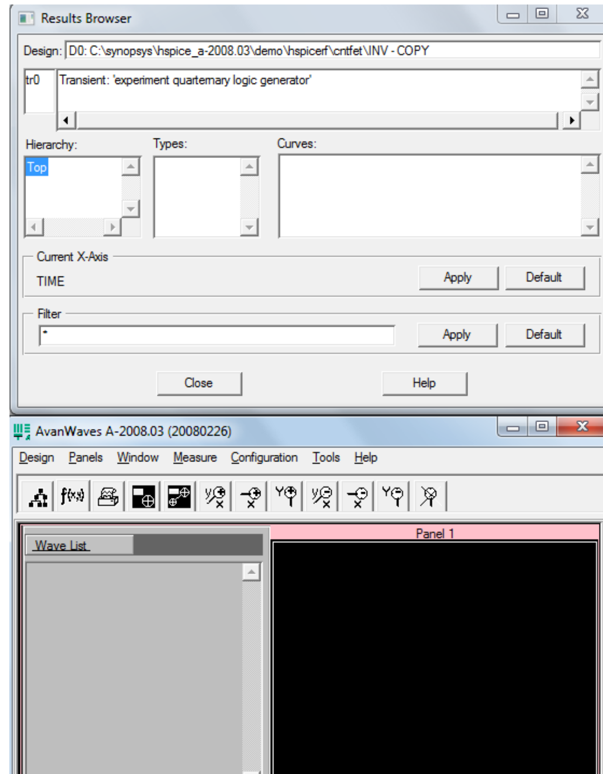


Figure 6.2: Avanwave window for curve generation.

6. Simulate the netlist.
7. For debugging the simulation (if required), click the button of **Edit LL,** which is next to the **Open** button.
8. For further editing of netlist, click on the **Edit NL**.
9. After successful simulation, click on the button **Avanwaves** to view the required and regarded graphs.
10. Go to the **Result Browser** window of the opened **Avanwaves**. Select the analysis by double clicking.
11. Select the **Hierarchy**, then select the **Types** and then select the **Curves** of the respective required simulation. Double click to view the curve in **Avanwaves** window.

6.2 HSPICE basics

HSPICE stores the simulation results requested in an output listing file and, if **.option post** is specified, a graph data file. When **post** is specified, the complete circuit solution (either steady state, time, or frequency domain) is stored. The results for any node voltage or branch current can then be viewed or plotted using MetaWaves. If you are converting a SPICE-3 input file to HSPICE format, it is only necessary that you add the line **.option post** somewhere in your file and put **.end** at the end (make sure to hit <cr> after the **.end** statement to form a complete line). However, if you wish to take advantage of some of the unique features of HSPICE you will need to refer to a copy of the *HSPICE USERS MANUAL.* HSPICE also has specific file naming conventions to indicate the function of each file. All of the files associated with a particular design reside in one directory and are named by catenating the design name and a particular suffix. Both HSPICE and MetaWaves extract the design name from the input file and use it to form the output files.

6.3 HSPICE Input File Structure

The basic structure of an input netlist file consists of one main program and one or more optional submodules. The submodule (preceded by the **.ALTER** statement) can be used to easily alter and re-simulate an input netlist file with different options, netlist, analysis statements, and test vectors. Several high level call statements can be used to restructure the input netlist file modules. These are the **.INCLUDE**, **.LIB** and **.DEL LIB** statements. Using these statements, netlists, model parameters, test vectors, analysis, and option macros can be called into a file from either library files or other files. The input netlist file can also call an external data file. The external data file contains parameterized data for element sources and models. The basic elements of an input netlist file are:

Table 6.1: basics of HSPICE netlist

TITLE	implicit first line; becomes input netlist file title
** or $*	comments to describe the circuit
.options	set conditions for simulatin
ANALYSIS AND TEMPERATURE	statements to set sweep variables
PRINT/PLOT/GRAPH	statements to sset print, plot and graph variables
.IC	sets input state, also can be put in subcircuits
SOURCES	Sets input stimulus
NETLIST	Circuit description
<.PROTECT>	Turns off output printback
.LIB libraries	Include .MODEL or .MACRO libraries
.INCLUDE libraries	Include .MODEL or .MACRO libraries
<.UNPROTECT>	Restores output printback
.ALTER	Sequence for worst case corners analysis
.DELETE LIB	Removes previous library selection
.LIB	Adds a new library case
.ALTER	Sequence for in-line case analysis
.END	Terminates any ALTERs and the simulation

6.4 Algebraic Expressions

Any parameter defined in the netlist can be replaced by an algebraic expression with single quoted strings. These expressions can then be used as output variables in the .PLOT, .PRINT, and .GRAPH statements. The algebraic expressions greatly expand the user's options in creating an input netlist file. Important features of algebraic expressions are:

Scaling or changing of element and model parameters

Parameterization

.PARAM x=5

Algebra

.PARAM x='y+3'

Functions

*.PARAM rho(leff,weff)='x*leff*weff-2u'*

Hierarchical subcircuit algebraic parameter passing

.subckt inv in out wp=10u wn=5u qbar-ic=vdd

.ic qbar=qbar-ic

…

.ends

Algebra in elements

R1 1 0 r='abs(v(1)/i(m1))+10'

Algebra in .MEASURE statements

.MEAS vmax MAX V(1)

.MEAS imax MAX I (q2)

.MEAS ivmax PARAM= ' vmax imax'*

Algebra in output statements

.print conductance=PAR(' i (ml)/v(22 ')

In addition to simple arithmetic operations (+, -, *,/), HSPICE also accepts the following quoted string functions:

Table 6.2: String functions

sin(x)	pow(x,y)	max(x,x)
cos(x)	sinh(x)	sqrt(x)
tan(x)	abs(x)	db(x)
atan(x)	cosh(x)	log10(x)
exp(x)	min(x,x)	
log(x)	tanh(x)	

6.5 Library Composition for Behavioral Model for CNTFET

Global parameters: *PARAMETERS.lib* [37]

```
.PROTECT

.PARAM q=1.60e-19              $ Electronic charge
+      Vpi=3.033               $ The carbon PI-PI bond energy
+      d=0.144e-9              $ The carbon PI-PI bond distance
+      a=0.2495e-9             $ The carbon atom distance
+      pi=3.1416               $ PI, constant
+      h=6.63e-14              $ Planck constant,X1e20
+      h_ba=1.0552e-14         $ h_bar, X1e20
+      k=8.617e-5              $ Boltzmann constant
+      epso=8.85e-12           $ Dielectric constant in vacuum

.PARAM Cgsub=30e-12            $ Metal gate (W) to Substrate fringe capacitance per unit length, approximated
                               $as 30af/um,
                               $ with 10um thick SiO2 default 30e-12
+      Cgabove=27e-12          $ W local interconnect to M1 coupling capacitance, 500nm apart, infinite large
                               $plane
                               $ default 27e-12
+      Cc_cnt=26e-12           $ The coupling capacitance between CNTs with 2Fs=6.4nm, about 26pF/m
+      Ccabove=15e-12          $ Coupling capacitance between CNT and the above M1 layer, 500nm apart,
                               default 15e-12
```

```
+    Cc_gate=78e-12              $ The coupling capacitance between gates with 2F=64nm, about 78pF/m,
                                 $W=32nm, H=64nm,
                                 $ contact spacing 32nm default 78e-12
+    Ctot='Cgsub+Cgabove+Cc_gate+Cc_gate'   $ total coupling capacitance for gate region

+        Cint='0*Cc_cnt+0.5*(20e-12+Ccabove)'     $ total coupling capacitance for source/drain region CNT,
                                 redefined $within models


+    Coeff1_Cgsd=0e-12           $ The slope for Cg_sd vs. Lsd, H=64nm, Klowk=2, contact spacing 32nm,
                                 valid $for 10nm<Lsd<100nm
+    Coeff2_Cgsd=0e-18           $ The intersection of Cg_sd vs. Lsd, H=64nm, Klowk=2, contact spacing
                                 32nm, $valid for 10nm<Lsd<100nm

+    Rsub=1                      $ Substrate resistance, set to zero for the ideal case
+    Klowk=2                     $ The dielectric constant of low-k material
+    Ksub=4                      $ The dielectric constant of SiO2
***Kox is Kgate
+    Kox=16                      $ The dielectric constant of high-K gate oxide

+    Ld_par=15e-9                $ Length of the drain CNT, 1 MFP of OP scattering, to calculate parasitic
                                 $diffusion capacitance
+    Rcnt=3.3e3                  $ n+ CNT resistance due to finite modes, 3.3K for 0.7eV doped n+CNT
+    FacR=0.4                    $ The factor of Rus/Rcnt

+    Efo=0.66                    $ The n+/p+ doped CNT fermi level (eV), 0.66eV for 1% doping level, 0.6eV
                                 for 0.8% doping level
+    lambda_op=15e-9             $ The Optical Phonon backscattering mean-free-path in Matallic CNT,15nm
+    lambda_ap=500e-9            $ The Acoustic Phonon backscattering mean-free-path in Matallic CNT, 500nm
+    photon=0.16                 $ The photon energy, typical value 0.16eV
+    L_channel=32e-9             $ CNFET printed/physical channel length, assume 32nm for 32nm node
                                 $technology
+    L_sd=16e-9                  $ n+CNT source/drain full length, 32nm, from gate edge to S/D metal contact
                                 $edge
+    L_relax=40e-9               $ delta_Vds relaxation range at drain side, fitting parameter
+    sub_pitch=6.4e-9            $ Sublithography full pitch, 6.4nm
+    de_fac=4                    $ the factor to calculate the number of electrons in CNT

+    Lgmax=100e-9                $ The maximum channel length to calculate current for short channel device

+    coeffj='4*q*q/h/1e-20'      $ The coefficient of current component, 4 is due to both spin degeneracy and
                                 $mode degeneracy
+    Coeff_Cc='pi*Klowk*epso'  $ The coefficient of the coupling capacitance between adjacent CNTs
+    kT='k*(TEMP+273)'           $ The KT constant
+    Rus='Rcnt*FacR'             $ Source side contact resistance
+    Rud='Rcnt*(1-FacR)'         $ Drain side contact resistance

+    Ccsd=0                      $ The coupling capacitance between channel region and source/drain islands
+    CoupleRatio=0.0             $ The percentage of coupling capacitance between channel and drain out of the
                                 $total fringe capacitance Ccsd
+    Leff=15e-9                  $ The mean free path in p+/n+ doped CNT, estimated as 15nm
+    Lceff=200e-9                $ The mean free path in intrinsic CNT, estimated as 200nm
+    phi_M=4.5                   $ Metal work function default=4.6
+    phi_S=4.5            $ CNT work function

.UNPROTECT
```

Model Description : CNFET.lib

```
* N-CNFET Level 1 Sub-circuit Definition
.SUBCKT NCNFET_L1 Drain Gate Source Sub CoupleNode Lg=L_channel Lgeff=Lceff Lss=L_sd
Ldd=L_sd Efi=Efo Kgate=Kox Tox=4e-9 Csub=20e-12 Ccsd=0 CoupleRatio=0 Vfbn=0 GF=0 Pitch=20e-9
n1=19 n2=0 CNTPos=1

…….. parameter definition……….

* start of device model

* The voltage controlled current source

GCNT Drain Source CUR='JFET(V(Drain,Source),photon,V(phib,Gnd))'
GBTBT Drain Source CUR='J_btbt(V(Drain,Source),I(GCNT),V(phib,Gnd))'

* Gate to Source/Drain/Sub capacitance

Csg Source Gate 'abs((Ci-(Ci+Csub_tot)/Vg_to_phib(V(Vdrain),V(Vsource),V(phib,Gnd)))*Lg/2)'
Cdg Drain Gate 'abs((Ci-(Ci+Csub_tot)/Vg_to_phib(V(Vdrain),V(Vsource),V(phib,Gnd)))*Lg/2)'
Cbg Gate mid2 'abs(Csub_tot/Vg_to_phib(V(Vdrain),V(Vsource),V(phib,Gnd))*Lg)'

Cgs Gate Source 'abs(Ci*(1-
Vs_to_vg(V(Vdrain),V(Vsource),V(phib,Gnd))/Vg_to_phib(V(Vdrain),V(Vsource),V(phib,Gnd)))*Lg)'
Cgd Gate Drain
'abs(charge_vds(V(Vdrain),V(Vsource),V(phib,Gnd))/Vg_to_phib(V(Vdrain),V(Vsource),V(phib,Gnd))*Lg)'

Csb Source Sub 'abs((Csub_tot-
(Ci+Csub_tot)/Vg_to_phib(V(Vdrain),V(Vsource),V(phib,Gnd))*Csub_tot/Ci)*Lg/2)'
Cdb Drain Sub 'abs((Csub_tot-
(Ci+Csub_tot)/Vg_to_phib(V(Vdrain),V(Vsource),V(phib,Gnd))*Csub_tot/Ci)*Lg/2)'

Cdj Drain Gnd 'abs(Cdj(V(Drain,Source),photon,V(phib,Gnd))*Ld_par)'

* The coupling capacitance between metal Gate stack and doped S/D carbon nanotube
Cgss Gate Source '(Coeff1_Cgsd*Lss+Coeff2_Cgsd)*GF*Cratio'
Cgdd Gate Drain '(Coeff1_Cgsd*Ldd+Coeff2_Cgsd)*GF*Cratio'

* Substrate resistance

Rsub mid2 Sub 'Rsub'

Edrain Vdrain Gnd VCVS Drain Gnd 1
Egate Vgate Gnd VCVS Gate Gnd 1
Esource Vsource Gnd VCVS Source Gnd 1
Esub VsubM Gnd VCVS Sub Gnd 1

.ENDS NCNFET_L1
```

NOTE – For PCNFET, the last four controlled source will be change (regarding polarity and voltage shift just like empirical models), can be stated as

```
Edrain   Vdrain    Gnd   VCVS   Drain     Gnd   -1
Egate    Vgate     Gnd   VCVS   Gate      Gnd   -1
Esource  Vsource   Gnd   VCVS   Source    Gnd   -1
Esub     VsubM     Gnd   VCVS   Sub       Gnd   -1
Evdd     VddM      Gnd   VCVS   Drain     Gnd    1
EVgg     VggM      Gnd   VCVS   Gate      Gnd    1
EVss     VssM      Gnd   VCVS   Source    Gnd    1
EVbb     VbbM      Gnd   VCVS   Sub       Gnd    1
```

Chapter 7

APPLICATIONS OF THE MODELLED CNTFET

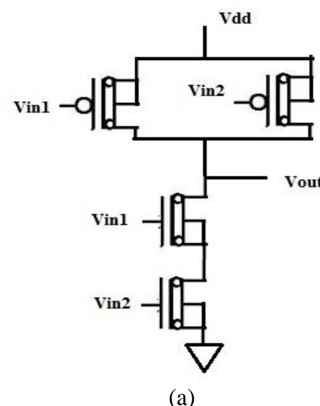
In this chapter, we are going to talk about the applications of the CNTFET device that has been designed in this thesis as a part of the project. The default model setting (chapter 5) will be used to implement the applications, discussed in this chapter. First, some of the digital application like NAND, NOR and EXOR will be implement. Then, as a part of analog application design, we are going to present a precision full wave rectifier base on differential difference current conveyor, where MOS circuit has been replaced by CNTFET. We will also see the improvement in the circuit performance comparatively CMOS designs.

7.1 Digital applications

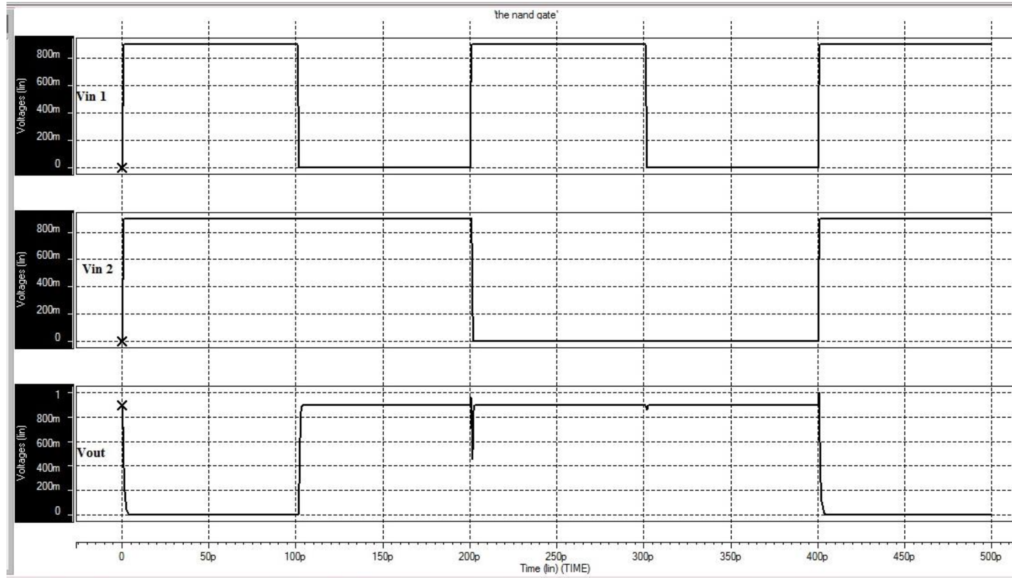
Few of the digital gate are implemented with the CNTFET device, are given below. First of all we will view the basics (Figure 7.1).

Figure 7.1- Symbol for nCNTFET (a) and pCNTFET (b).

NAND Gate:



(a)



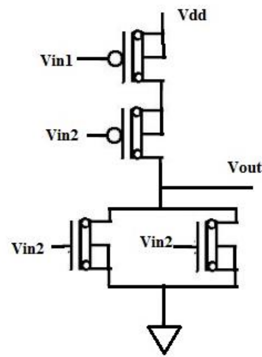
(b)

Figure 7.2: (a) NAND gate schematics and (b) circuit performance

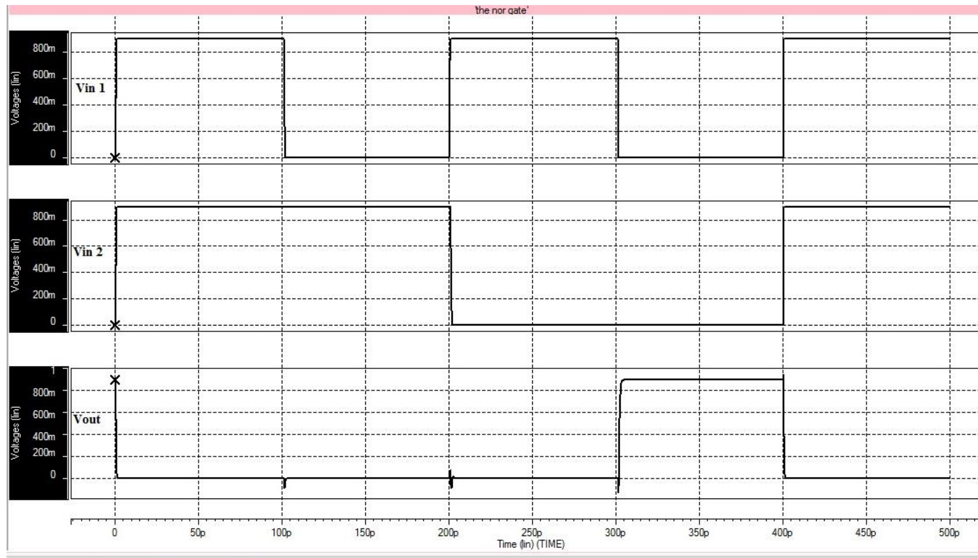
Table 7.1: NAND Gate performance

Max gate delay	13.6 ps
Average power dissipation	1.2µw

NOR Gate:



(a)



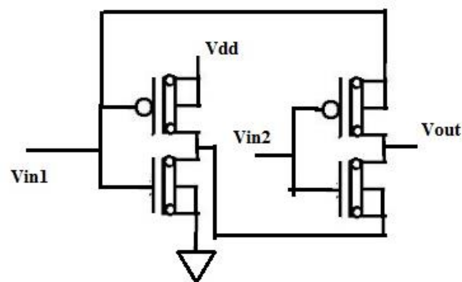
(b)

Figure 7.3: (a) NOR gate schematics and (b) circuit performance

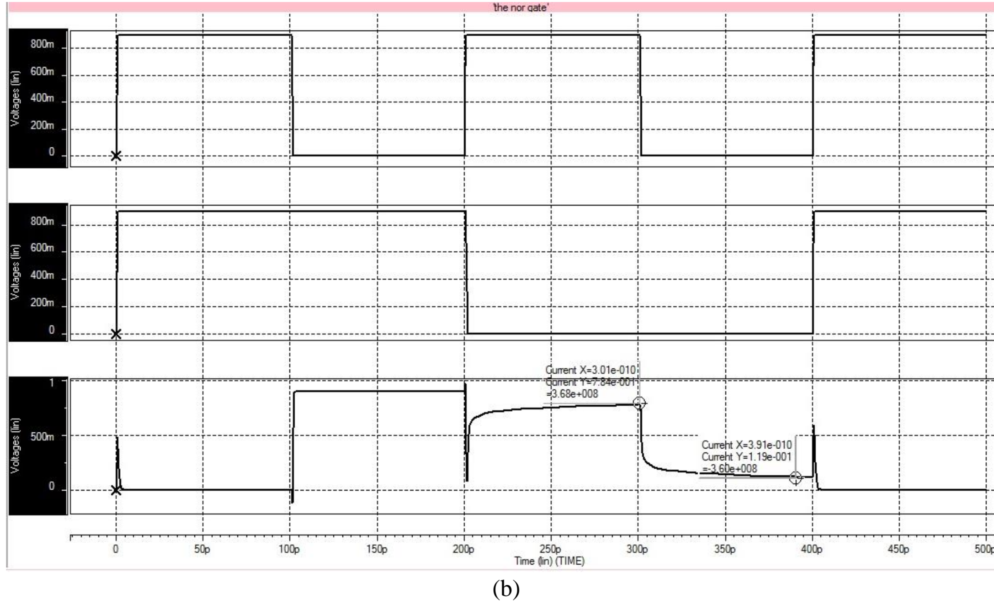
Table 7.2: NOR Gate performance

Max gate delay	13.6 ps
Average power dissipation	1.2μw

EXOR Gate: This logic circuit has been designed with pass transistor circuitry to show the pass transistor performance using PCNFET and NCNFET. As we know that PMOS cannot pass full zero logic and appends $V_{t,p}$ and similarly NMOS cannot pass full high logic and reduce it to V_{DD}-$V_{t,n}$. Hence Figure 7.4(a) can be consider for such performance including the EXOR logic performance.



(a)



(b)

Figure 7.4: (a) EXOR gate schematics and (b) circuit performance with *Vt,p=-0.119 V* and *Vt,n=0.116 V* approximately

Table 7.2: EXOR Gate with pass transistor performance

Max gate delay	15.8 ps
Average power dissipation	1.89µw

7.2 Analog Application

7.2.1 DDCC

The electrical symbol of differential difference current conveyor (DDCC) [8] is shown in Figure 7.5(a). It has three voltage input terminals: Y1, Y2and Y3, which have high input impedance. Terminal X is a low impedance current input terminal. There is a high impedance current output terminal Z. . The input-output characteristics of ideal DDCC are described in Figure 7.5(b). the circuit diagram for the DDCC device(CNTFET Technology based) is shown in fig-4 where pCNTFET and nCNTFET can be replace by pMOS and nMOS respectivily for MOS based device implentation.

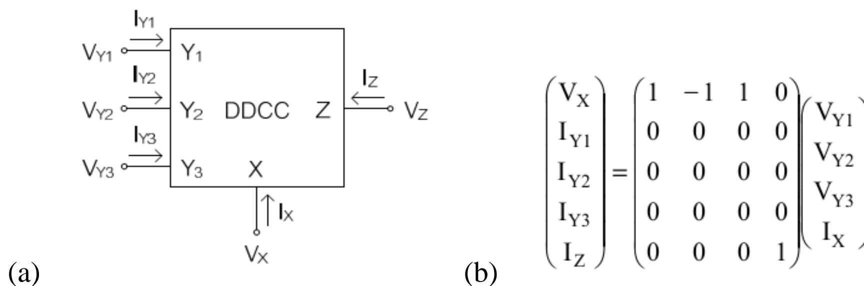


Figure 7.5: DDCC ciruit symbol(a) and characteristics(b)

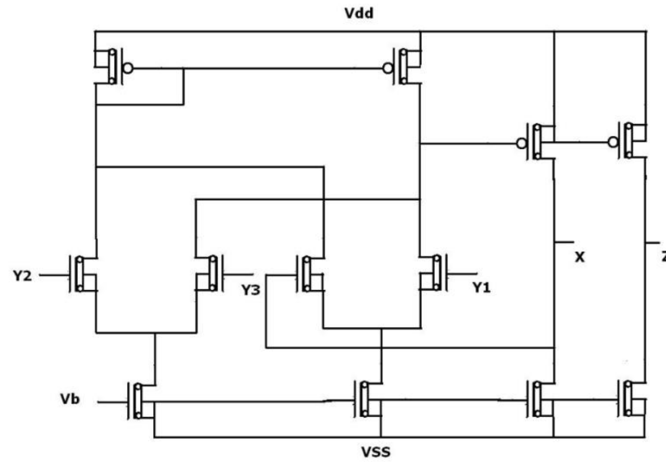


Figure 7.6: Circuit diagram of DDCC

The characteristics of the DDCC device can be view in Figure 7.7 where V_x vs. V_y1has been indicated with parametric analysis with respect to V_{y2}.

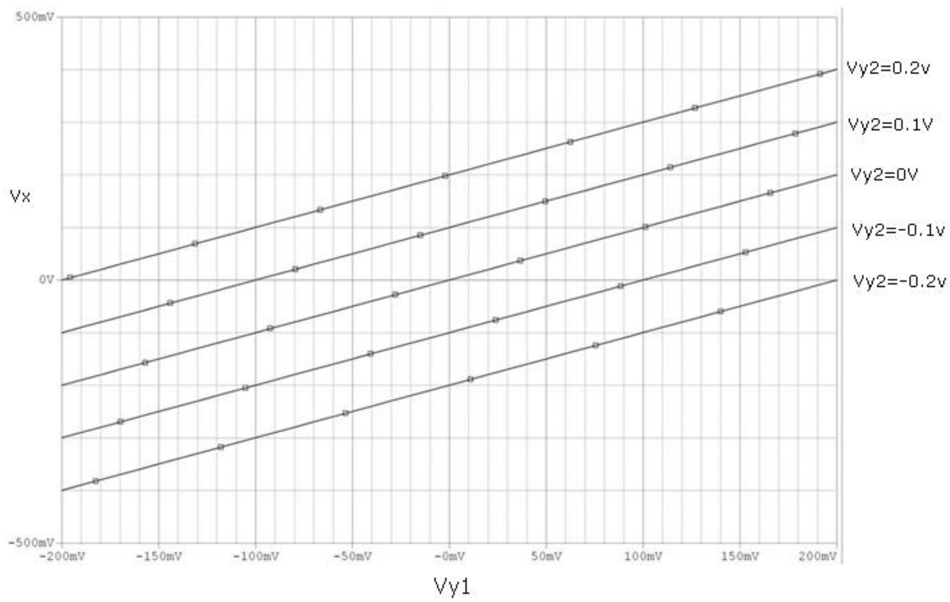
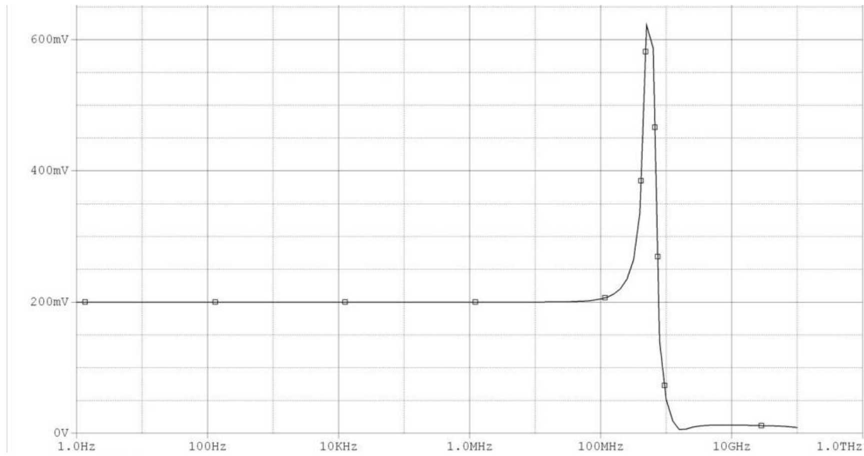
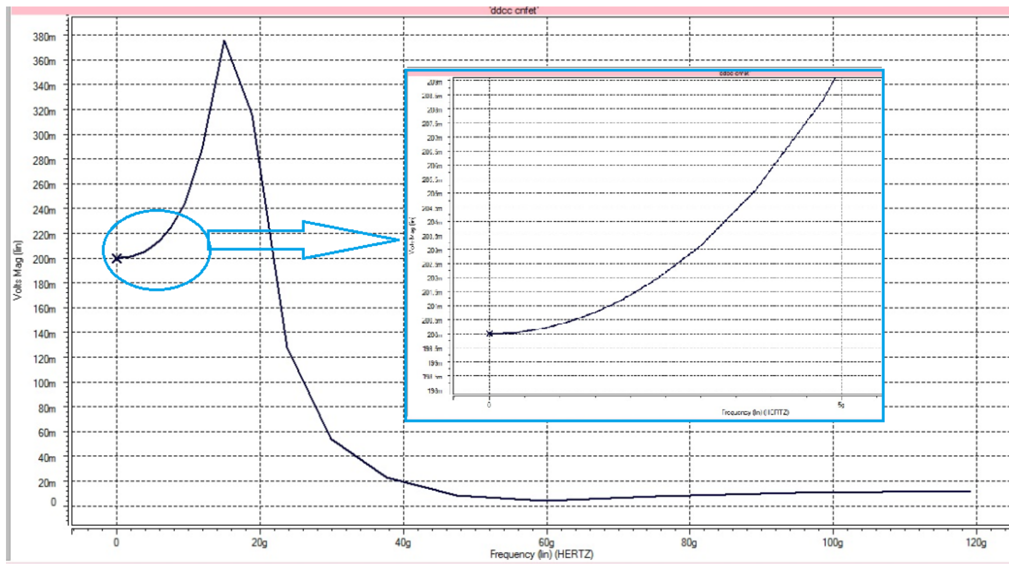


Figure 7.7: Input-output characteristics of DDCC



(a)



(b)

Figure 7.8: AC characteristics of the DDCC (a) using MOS (350nm) technology having voltage consistencyof 4.5% for 200mV, upto 100MHz and (b)using CNTFET having voltage consistencyof 4.5% for 200mV, upto 5GHz.

In the Figure 7.8 even though the response of the CNTFET based DDCC device doesn't have good high frequency response but upto 5 GHz it has a good voltage consistency comparitively the CMOS (350nm) technology.

7.2.2 Circuit Realization of Precision Full Wave rectifier

The full-wave rectifier circuit is shown Figure 7.9. This circuit uses only two DDCCs[4].The positive output voltage of the DDCC1 is connected to the negative output voltage of the DDCC2.

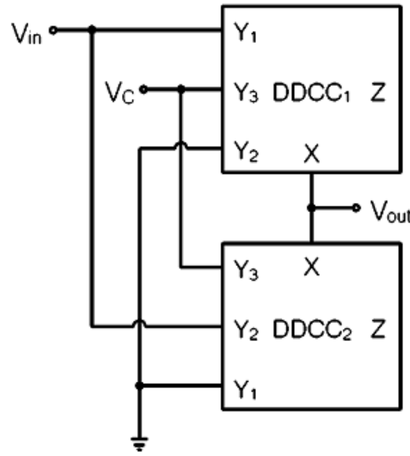


Figure 7.9. Full wave Rectifier circuit

The full-wave operation is as follows:

When Vin>0, the voltage Vin is followed by the DDCC1 to the voltage Vout at X terminal while the DDCC2 is tum-off. In addition, whenVin<0, the voltage Vin is followed by the DDCC2 to the voltage Vout at X terminal while the DDCC1 is cut-off .From the operation of the given full-wave rectifier explained.,the relations between the input voltageVin, and the output voltageVout, can be expressed as

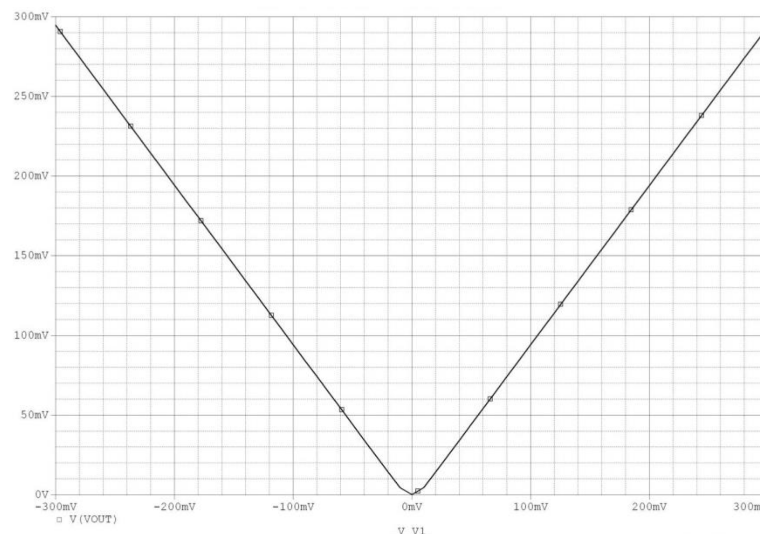
$V_{in} > 0$; $V_{out}=V_{in}$: $DDCC_1$= on

$V_{in} < 0$; $V_{out}= -V_{in}$: $DDCC_2$=on

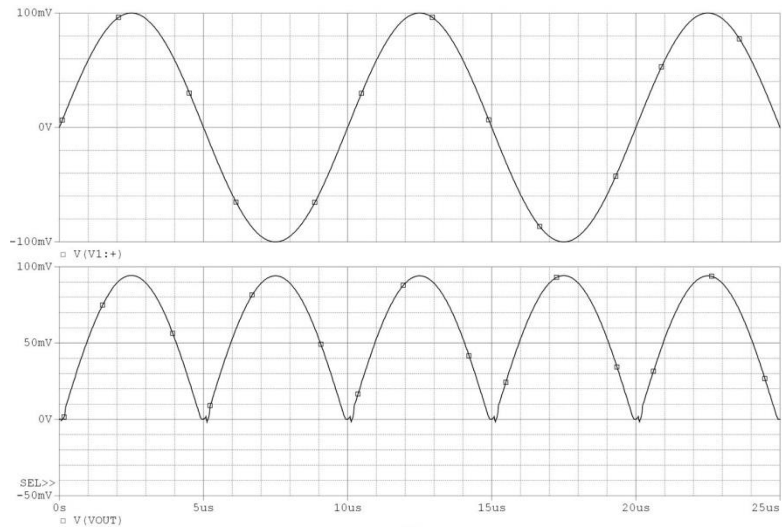
The complete output voltage of Fig.4 can be expressed as

$V_{out}= | V_{in}|$

Therefore, the given circuit provides the full-wave rectification[39]. Vc is auxiliary voltage. The circuit performance is shown in Figure 7.10.



(a)



(b)

Figure 7.10: Precision full-wave rectifier response (a) and (b)

From above it is obvious that this rectifier can rectify any signal as low as 5 mv whereas for conventional rectifiers like full-wave rectifier[40][41] the minimum applied voltage should be above the Knee voltage of the semiconductor material being used (which is 0.7 V for silicon and 0.3v for germanium). This is a significant advantage of this circuit.

Chapter 8

CONCLUSION AND FUTURE SCOPE

CONCLUSION

This thesis describes a body of work on modeling, understanding, and performance evaluation and prediction for nanoscale devices and circuits, including both CMOS technology beyond the 45 nm node and carbon nanotube field effect transistors (CNFETs), with the aim of guiding nanoscale device and circuit design. This thesis covers: device performance metric definition, extending the silicon CMOS technology roadmap by selective footprint scaling, 1-D FET gate capacitance modeling, CNFET device modeling, CNFET device / circuit / system performance prediction, performance comparison between CNFET and CMOS technology, and CNFET device some applications in digital and analog domain. The analog application part of this thesis is published in International Journal of Engineering and science in Research Inventy (ISBN: 2319-6483, ISSN: 2278-4721, Vol. 2, Issue 1 (January 2013), PP 40-47).

After nearly half a century of evolution since 1960's, the 45 nm CMOS technology has been announced in 2007. Silicon technology is believed to be able to solve its impending scalability problems and extend the roadmap beyond 22 nm node, based on the efforts of the semiconductor industry. As a new technology first conceived in 1998, CNT-based devices have demonstrated attractive material and device level performance compared to conventional CMOS technology in a short time. Though today's CNT based device and circuit performances cannot compete with the well-developed CMOS technology, CNT still remains an attractive material for nanoelectronics devices, interconnects, owing to the near-ballistic transport, high current capability, nanometer scale, and low-cost synthesis technique. It should not be surprising that CNFET technology and CMOS technology will cross and/or join together at some point in the future.

FUTURE SCOPE

An assumption has been taken in this thesis, that the sizes of various device structures (e.g. contact sizes, overlay spacing) can be arbitrarily reduced using yet-to-be developed process technologies. The extended scaling path requires tight pitch patterning, tight overlay tolerances, and a short gate height processes. All these are potential yield limiters. More studies on the effect of these assumptions on yield should be carried out to verify the concept of device footprint scaling from the

manufacturability point of view. Novel nanofabrication techniques, such as self-assembly and low-*k* spacer, are needed to realize the substantial benefits offered by L_{pitch} scaling and parasitic engineering. Additionally, packaging and/or architectural solutions are also required to mitigate the increased power density due to the smaller device footprint. Future work on device/circuit performance optimization may further consider the effects of stress-dependent carrier mobility, low-*k* isolation dielectric (low-*k* STI), simultaneous optimization of footprint, and device width.

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Appendix A

A BRIEF SPECIFICATION OF CNTFET DEVICE MODEL

A1. DEVICE LIMITATIONS

The current version is implemented with HSPICE (ver. 2008.03) Marco model. This model is designed for unipolar behavior CMOS-like CNFET device. The minimum channel length (~10 nm) is restricted by the complex quantum mechanisms which are not implemented in this model. In principle, this model has no limitation on the maximum gate length of CNFET. For gate length longer than 100 nm, the device is treated as long channel device. The transition from the short channel model (10 nm < Lg < 100 nm) to the long channel model (Lg > 100 nm) is continuous and is automatically handled by the model.

A2. FUNCTION CALLING AND PARAMETERS

The usage of this model is similar to that of the CMOS models. The local parameters can be set up for every single device. The syntax to call device models is as below:

NCNFET

XCNT Drain Gate Source Sub NCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9 Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3

PCNFET

XCNT Drain Gate Source Sub PCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9 Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3

Table A.1: definition and default values of local parameter

Local Parameter	Description	Default Value
Lch	Physical channel length. This model may not be valid for channel length below 10 nm where other quantum mechanical effects may need to be considered.	32 nm (Set by global parameter L_channel)
Lgeff	The mean free path in the (intrinsic) channel region due to non-ideal elastic scattering.	200 nm (Set by global parameter Lceff)
Lss	The length of doped source side extension region (CNT)	32 nm (Set by global parameter L_sd)
Ldd	The length of doped drain side extension region (CNT)	32 nm (Set by global parameter L_sd)
Efi	The Fermi level of the doped S/D tube	0.6 eV (Set by global parameter Efo)
Kgate	The dielectric constant of high-k front gate dielectric material (planer gate)	16 (Set by global parameter Kox)
Tox	The thickness of high-k front gate dielectric material (planer gate)	4 nm
Csub	The coupling capacitance between channel region and substrate (back gate)	20 pF/m (assume 10 µm thick SiO2)
Csd	The coupling capacitance between channel region and source/drain region	0 pF/m (Set by global parameter Ccsd)
CcdBeta	The percentage of coupling capacitance between channel and drain region out of Ccsd	0 pF/m (Set by global parameter CoupleRatio)
Vfbn, Vfb	Flat band voltage for nFET, pFET, respectively	0eV
Dout	Describe the property of the drain side output: 1: the drain output is connected to another CNFET directly 0: the drain output is connected to metal contact	0
Sout	Describe the property of the source side output: 1: the source output is connected to another CNFET directly 0: the source output is connected to metal contact	0
Pitch	The distance between the center of two adjacent tubes under the same gate. This parameter is used to include the screening effects. It is also useful to change the Gate-Tube coupling capacitance in case Tox and Kgate are fixed.	20 nm
Wgate	The width of metal gate. This parameter is used to include interconnect capacitance, approximated as 0.213 fF/µm	6.4 nm (set by global parameter sub_pitch)
CNPOS	The position of CNT under the gate (unique for model file 'CNFET_nonBalistic_single_CNT.lib': 1: the tube is at the two ends 0: the tube is in the middle	1
Mul	The number of tubes under the same gate.	1

Table A.1: definition and default values of major/global parameters

Global Parameter	Description	Default Value
Klowk	The dielectric constant of low-k oxide material	2
Ksub	The dielectric constant of back gate (substrate) dielectric material	4
Kox	The dielectric constant of high-k gate oxide material	16
Ld_par	Fitting parameter. The length of the drain CNT, to calculate parasitic diffusion capacitance at drain side junction.	15 nm
Efo	The Fermi level of n+/p+ doped source/drain tube. This parameter is internally limited to be above the first conduction band.	0.6 eV (~0.8% doping level)
Lambda_op	The Optical Phonon backscattering mean-freepath in Matallic CNT	15 nm
Lambda_ap	The Acoustic Phonon backscattering mean-freepath in Matallic CNT	500 nm
Photon	The optical phonon energy	0.16 eV
L_channel	Physical gate length	32 nm
L_sd	The length of doped source/drain extension tube.	32 nm
L_relax	Fitting parameter. Carrier relaxation range at drain side, used to match BTBT current.	40 nm
Sub_pitch	Sublithography full pitch	6.4 nm
Ccsd	The coupling capacitance between channel region and source/drain region.	0pF/m
CoupleRatio	The percentage of coupling capacitance between channel and drain region out of Ccsd.	0
Lceff	The mean free path in intrinsic CNT	200 nm
Leff	The mean free path in P+/n+ doped CNT	15 nm
fai_M	The work function of Source/Drain metal Contact	4.6 eV
fai_S	CNT work function	4.5 eV

Appendix B

LIST OF PUBLICATIONS

1. "CNTFET Technology Based Precision Full-Wave Rectifier Using DDCC" by Gavendra Singh, Umesh Kumar, Rajeev Ranjan.
   International Journal of Engineering and Science
   ISBN: 2319-6483, ISSN: 2278-4721, Vol. 2, Issue 1
   (January 2013), PP 40-47.

2. "Patch Antenna Array Fault Modeling and Its Monitoring" by Umesh Kumar, Rajiv Kapoor.
   IOSR Journal of Electronics and Communication Engineering (IOSR-JECE)
   ISSN: 2278-2834, ISBN: 2278-8735. Volume 3, Issue 4 (Sep-Oct. 2012), PP 06-11
   DOI **"10.9790/2834-0340611".**

3. "CMOS Body Driven Quaternary Logic Generator" by Umesh Kumar, Rajiv Kapoor
   IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)
   ISSN: 2319 – 4200, ISBN No. : 2319 – 4197 Volume 1, Issue 1 (Sep-Oct. 2012), PP 46-50
   DOI **"10.9790/4200-0114650".**

4. "Fiction Supporting Decelerated Expansion of the Universe" by Umesh Kumar.
   IOSR Journal of Applied Physics (IOSR-JAP)
   ISSN: 2278-4861. Volume 2, Issue 1 (Sep-Oct. 2012), PP 41-42
   DOI **"10.9790/4861-0214142".**