CERTIFICATE

This is to certify that the dissertation entitled "**A NUMERICALLY EFFICIENT IMPROVED CHANNEL LENGTH ANALOG BEHAVIOURAL MODEL OF CNTFET AND APPLICATIONS**" is the work of Mr. Umesh Kumar (Roll No.: 10/VLSI/2k11), a student of M.Tech. (VLSI Design and Embedded System) in Delhi Technological University (Formerly DCE). This work is completed under my direct supervision and guidance and forms a part of Master of Technology (Electronics and Communication) course and curriculum. He has completed her work with utmost sincerity and diligence.

The work embodied in this major project has not been submitted to any other Institute/University for the award of any other degree to the best of my knowledge.

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DECLARATION

I, hereby, declare that all the information in this document has been obtained and presented in accordance with academic rules and ethical conduct. This report is my own, unaided work. I have fully cited and referenced all material and results that are not original to this work. It is being submitted for the degree of master of technology in engineering at the Delhi Technological University. It has not been submitted before any degree or examination in other university.

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To my teachers and my parents……

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ABSTRACT

Ever since the 0.35 μm node, the gate length of MOSFET has entered the deepsubmicron region. 65 nm technologies becomes the mainstream since 2006, and 45 nm technology has been announced in 2007. As CMOS continues to scale deeper into the nanoscale, various device non-idealities cause the I-V characteristics to be substantially different from well-tempered MOSFETs.

It becomes more difficult to further improve device/circuit performance by reducing the physical gate length. The discrepancy between the fabricated physical gate length and the ITRS projected gate length becomes larger as the technology advances. Recognizing that the device structure has been scaled from 3-D (bulk CMOS), quasi 2-D (partially depleted SOI), 2-D (fully depleted SOI), quasi 1-D (nanowire FET, FINFET, tri-gate FET), to 1-D (CNFET) for better channel electrostatics, it is important and necessary to model the behavior of 1-D device with the aim of guiding 1-D device and circuit design.

This thesis describes a body of work on modeling, implementation and understanding for nanoscale devices, carbon nanotube field effect transistors (CNFETs), with the aim of making the device model more numerically efficient and improving the channel length, as well as enhancing the accuracy of channel current by introducing the band to band tunneling current (I_{btbt}). This work will also lead to the nanoscale device based circuit design in the field of analog and digital domain applications. Analog behavior modeling carbon nanotube FET has been implemented using HSPICE. Later part of the thesis is implementation of digital logic gates as digital domain application and implementation of precision full wave rectifier using differential difference current conveyor (DDCC) as analog domain application.

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