CHAPTER 1

INTRODUCTION

1.1 MOTIVATION

Since the beginning of electronics, the need of new active devices has always been very important. It has driven to the birth of transistors which have been used, then, in amplifiers, impedance converters, filters, etc. In particular, the voltage operational amplifier has rapidly become the main analog block and has dominated the market since the advent of the first analog integrated circuits. Presently, the situations changing because there is a new impulse towards these called current mode circuits, which are able to overcome the limitation of a constant gain-bandwidth product and trade-off between speed and bandwidth, so that performance is improved in terms of low-voltage characteristics and of slew-rate and bandwidth. Many topologies for current conveyor have been presented by eminent researchers. I derived motivation for my work from these works on current conveyor towards having a comparative analysis of these topologies based on their various parametric values.

1.2 VOLTAGE AND CURRENT MODES

One procedure for finding alternative, preferably simpler, circuit realizations is to use current signals rather than voltage signals for signal processing. MOS-transistors in particular are more suitable for processing currents rather than a voltage because the output signal is current both in common-source and common-gate amplifier configurations and common-drain amplifier configuration is almost useless at low supply voltages because of the bulk-effect present in typical CMOS-processes. Moreover, MOS current-mirrors are more accurate and less sensitive to process variation than bipolar current-mirrors because with the latter the base currents limit the accuracy. Therefore, at the very least, MOS-transistor circuits should be simplified by using current signals in preference to voltage signals. For this reason, integrated current-mode system realizations are closer to the transistor level than the conventional voltage-mode realizations and therefore simpler circuits and systems should result. When signals are widely distributed as

voltages, the parasitic capacitances are charged and discharged with the full voltage swing, which limits the speed and increases the power consumption of voltage-mode circuits. Current-mode circuits cannot avoid nodes with high voltage swing either but these are usually local nodes with less parasitic capacitances[3]. Therefore, it is possible to reach higher speed and lower dynamic power consumption with current-mode circuit techniques. Current-mode interconnection circuits in particular show promising performance.

1.3 CURRENT-MODE DESIGN

The current-mode design technique is a good alternative for the high performance analog circuit design as it offers voltage independent high bandwidth. In current-mode design, the stress is more on the current levels for the operation of the circuits and the voltage levels at various nodes are immaterial[1]. In voltage-mode circuits (VMCs), such as operational amplifiers (op amp), the performance of the circuit is determined in terms of voltage levels at various nodes including the input and the output nodes. But all these circuits suffer from the following disadvantages:

- Output voltage cannot change instantly when there is a sudden change in the input voltage due to stray and other circuit capacitances.
- Bandwidth of the op amp based circuits is usually low because of finite unity gain bandwidth.
- Slew rate is dependent on the time constants associated with the circuit.
- Circuits do not have high voltage swings.
- Require higher supply voltages for better signal-to-noise ratio.

Therefore, VMCs are not suitable for high frequency applications. When signals are widely distributed as voltages, the parasitic capacitances are charged and discharged with the full voltage swing, which limits the speed and increases the power consumption of voltage-mode circuits. Current-mode circuits cannot avoid nodes with high voltage swing either but these are usually local nodes with less parasitic capacitances. Therefore, it is possible to achieve higher speed and lower dynamic power consumption with current-mode circuit techniques.

When the signal is conveyed as a current, the voltages in MOS transistor circuits are proportional to the square root of the signal, if the devices are assumed to be operating in saturation region. Therefore, a compression of voltage signal swing and a reduction of supply voltage are possible. This feature is utilized in log domain filters, switched current filters and in non-linear current-mode circuits. However, as a result of the device mismatches, this non-linear operation may generate an excessive amount of distortion and cannot be used for the applications where high linearity is required[2]. Thus, linearization techniques are utilized in current-mode circuits to reduce the nonlinearity of the transistor transconductance and in this case the voltage signal swing is also not reduced.

Current conveyor:

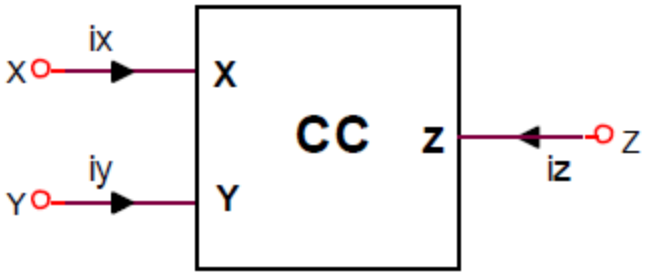

Fig1-1: Current conveyor block diagram

With the reduction in the supply voltage and device threshold voltage of CMOS technology, the performance of CMOS voltage-mode circuits has greatly affected which results in a reduced dynamic range, an increased propagation delay and reduced low noise margins. The influence of supply voltage reduction on the performance of current-mode circuits, however, is less severe as compared with that of voltage-mode circuits. This is because the design emphasis of current-mode circuits is on branch currents rather than nodal voltages. The usefulness of CMOS current-mode circuits in overcoming the difficulties arising from the reduction of the supply voltage and the increase in the operation speed has received an increasing attention from the industry.
Current conveyors were introduced in the late sixties, early seventies by Smith and Sedra [4].

They were considered to be used as controlled voltage and current sources, impedance converters and inverters, etc., but also as function generators, amplifiers, filters, etc., in current processing circuits mainly for instrumentation and measurement applications.
In the first years of their appearance the performance of current conveyors was severally limited by the available technologies, which did not allow well-matched devices on fabricated chips. Since the technologies have improved in the eighties, the current conveyors gained the attention of many analog designers. Today the current conveyors have developed to very useful building blocks of analog electronics. They are parts of a number of very often used circuits, like active filters, trans impedance and ‘current feedback' operational amplifiers, voltage and current operational amplifiers and other more, and their main application areas are in high-speed, high-frequency circuits for both voltage and current signal processing.

Current Conveyors represent the emerging class of high performance analog circuit design based on current-mode approach. They have simple structure, wide bandwidth and capability to operate at low voltages. Current conveyors are unity gain active elements exhibiting higher linearity, wider dynamic range and better high frequency performance.

These circuits can give large bandwidths and are suitable for low-voltage applications. Current feedback amplifiers, Operational floating Conveyors, Current Conveyors (CCs) etc. are the popular current mode circuits structures and most widely used structure among them is the CCII structure.

REFERENCES

[1] Giuseppe Ferri & Nicola C.Guerrini "Low Voltage Low power CMOS current conveyors"

[2] Issa Eldbib " Low Voltage Current-Conveyors Design Techniques"

[3] Ahmed M. Soliman "Current-Mode Universal Filters Using Current Conveyors: Classification and review".

[4] K. C. Smith and A. Sedra, "The current conveyor-A new circuit building block," Proc. IEEE (Letters), vol. 56, pp. 136B-1369A, ugust 1968

CHAPTER 2
LITERATURE SURVEY

The demand for electronic circuits with extremely low supply voltages and power consumption is important in development of microelectronic technologies. Electronically tunable analog filter are useful in many applications, such as telecommunication, multimedia and consumer electronics. Medical electronics etc. are important subsystems in such systems. Among the existing realization method of continuous-time domain integrated analog filters circuit, CCII topology is most useful one and it offer good performances with lower power consumption and high frequency operation. In many applications, additional requirements appear, particularly the extreme speed or the accuracy of signal processing. Simultaneous fulfillment of the above demands is problematic. CMOS technology, using the CCII as the active element can achieve a considerable improvement in amplifier speed, accuracy and bandwidth, overcoming the finite gain–bandwidth product associated with operational amplifiers. Extensive literature survey shows that a lot of work has been done on current mode logic devices using the current conveyors. The analog integrated circuit design in current mode is receiving increased attention due to some potential performance features like wide bandwidth, less circuit complexity, wide dynamic range, low power consumption, and high operating speed[4]. The current mode approach has emerged as an alternate method besides the traditional voltage mode circuits. The current mode active elements are appropriate to operate with signals in current or voltage or mixed mode and are gaining acceptance as building blocks in high-performance circuit designs.

2.1 CURRENT CONVEYORS

The concept of the current-conveyor was earliest introduced in 1968 and then modified to a second-generation current-conveyor in 1970s . The current-conveyor is considered as a general building block as with the operational amplifier. Because of the operational amplifier idea has been current since the late 1940s, it is tuff to get any other same concept widely accepted. However, OpAmps do not perform good in applications where a current output waveform is needed and resultantly there is an application area for current-conveyor circuits[3]. Since current-

conveyors perform without any global feedback, a different high frequency behavior compared to OpAmps circuits results.

2.1.1 CLASSIFICATION OF CCs

There are many schemes for classification of CCs. Very common techniques in them are formed on the characteristics of X, Y and Z ports. Current conveyors have too classified same to power amplifiers based on current that flow.

2.1.1.1 Port Y based classification

Port Y acts as input for voltage waveforms and it does not load the input voltage excitation by drawing the current. But in some circuits, it is needed to draw currents from the input voltage excitation. When port Y draws a current same to the current entered at port X, A = 1 this topology is termed as First generation current conveyor.

When port Y draws no current (A = 0), it is Second generation current conveyor.

Similarly, when this current similar to the current entered at port X but of opposite sign, the topology is termed as Third generation current conveyor for which A = −1.

- **First Generation Current Conveyors – CCI**

Current-conveyors are three-port structures having ports X, Y and Z as shown below:

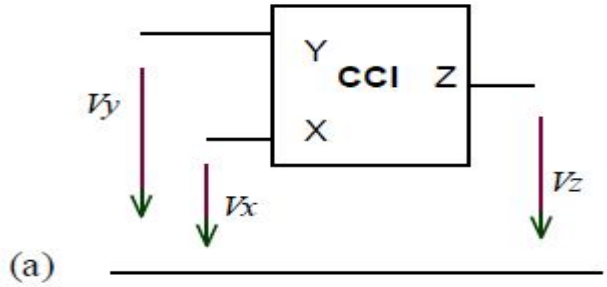

Figure 2-1: First generation current-conveyor symbol.

The impedance level at different ports of first generation current conveyor is listed in **table 2.1** below:

CCI PORTS	IMPEDENCE LEVEL
X	Low (ideally zero)
Y	Low (ideally zero)
Z	High (ideally infinite)

The network of the first generation current-conveyor CCI has been formulated in a matrix form as follows :

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix}$$

The first generation current conveyor CCI forces both the currents and the voltages in ports X and Y to be equal and a replica of the currents is mirrored (or conveyed) to the output port Z.

- **Second Generation Current Conveyor – CCII**

For many applications a high impedance input terminal is preferable and to increase the versatility of the current conveyor, which no current flows in terminal Y. It has one high and one low impedance input instead of the two low impedance inputs of the CCI . This building block has since proven be more useful than CCI. CCII can be described by following matrix:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix}$$

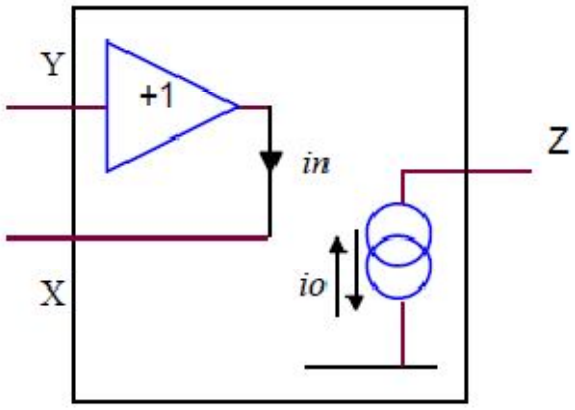

Figure 2-2: The principle of the second generation current conveyor.

The current flowing into (CCII+) or out of (CCII-) the Z node is proportional to the current flowing into the X node.

The second-generation current-conveyor is a principle of voltage-follower with a voltage input Y node and a voltage output X node, and a current-follower (or current-inverter) with a current input X and a current output Z.

The impedance level at various ports of second generation current conveyor is shown in the **table 2.2** below .Impedance at input and output ports of current conveyors plays an important role in determining its characteristics

CCI PORTS	**IMPEDENCE LEVEL**
X	Low (ideally zero)
Y	High (ideally infinite)
Z	High (ideally infinite)

CCII has proven to be by far the more useful of the current conveyor family types. Wide range of applications was published. It is very suitable building block for design of the active-RC filters or number of special admittance converters. In the last decade the numbers of high-speed and wide-range op amps are based on current conveyor structure. And also for low voltage applications CCII is starting to be very powerful building block.

- **Third Generation Current Conveyor – CCIII**

Third generation current-conveyor CCIII is defined in a matrix form as follows. This type is similar to CCI, there is opposite current transfer between X and Y terminal. Matrix described this CC type is following:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix}$$

The input current comes into the Y-port and out from the X-port, one can consider that a differential current input could be formed with this amplifier. However, the CCIII has high input impedance with common-mode current waveforms, i.e. similar currents are given both to Y- and X-ports[2]. Therefore common-mode currents can force the input ports out from the proper operational range. This CC can be used as an active current wave probe.

2.1.1.2 Port X based classification

For voltage signals, port Y perform as input port and now the port X serves as output terminal. The output voltage at terminal X can either have identical polarity as of the input voltage (VY) , in this case current conveyor is called as non-inverting CC. or that of opposite polarity , are termed as inverting CCs . The inverting second generation current conveyor „positive‟ (ICCII+), has the following port relation between terminal voltages and currents:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ -1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix}$$

2.1.1.3 Port Z based classification

Port Z is the current output port and usually, the magnitude of the output current at port Z equals to the magnitude of the current injected into port X. In some cases, however, this amplitude may be scaled version (generally up scaled) of the input current and also the direction of the current may be same or opposite to that of the current in port X. CC with positive current output is termed as CC+ and with negative output currents as CC− [10].

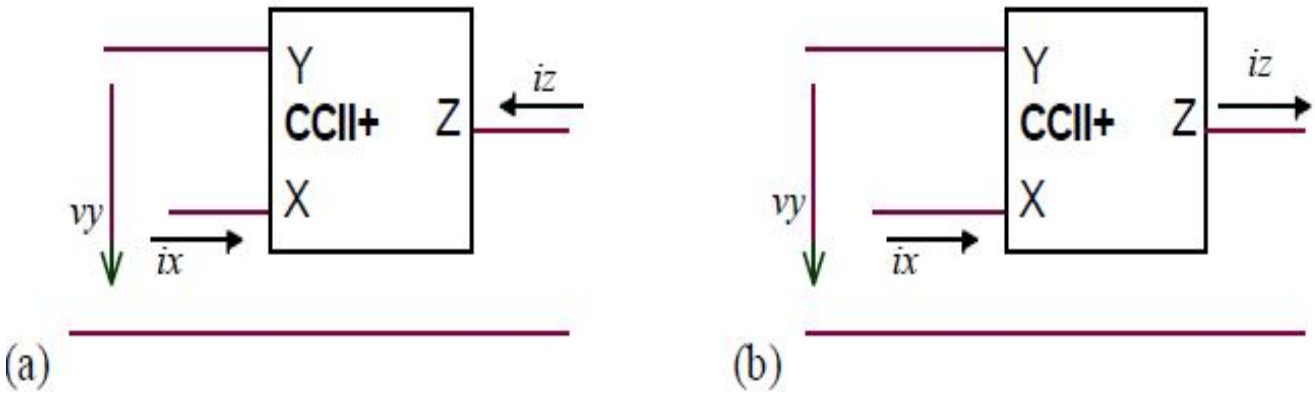

Fig: 2-3 Positive and negative CCII basic blocks.

A Current conveyor can have two or more output ports, which can independently sink or source currents. Such a Current conveyor is known as multi port Current conveyor. A multi port Current conveyor with both types of output ports (positive as well as negative), is known as composite port CCII.

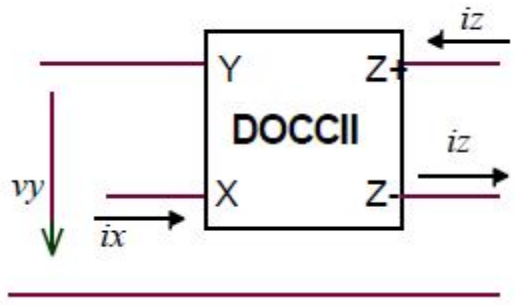

Figure 2-4: Dual output CCII basic block

2.1.2 CCII APPLICATIONS

Due of the different voltage and current inputs both the voltage and current amplifiers can easily be formed with the second-generation CC and the gain can be adjusted by resistor ratios as in OpAmp circuits. Signal processing in CC circuits is based on voltage-to-current and current-to-voltage conversions and on waveform buffering by voltage and current buffers[1]. Because there is typically no feedback in the current-conveyor circuits, wide bandwidth operation without any slewing at large signal amplitudes can be obtained. The conventional applications of CCs are:

- Amplifier circuits
- Oscillator circuits
- Analog filters
- Wave shaping circuits
- Analog computer designing etc.

Low-voltage and low-power structures of CCs are particularly suitable in the design of voltage and power starved systems.

2.1.2.1 Current Output Amplifier

The CCII can easily be used to configure the current output amplifiers, as shown in Figure below. Current amplifier can be performed through the use of a CCII , the input current is converted into an input voltage, applied to Y node. The X node voltage obtained in this way forces, into R2, a current which flows from high impedance Z node.

$$\frac{I_{out}}{I_{in}} = \frac{R_1}{R_2}$$

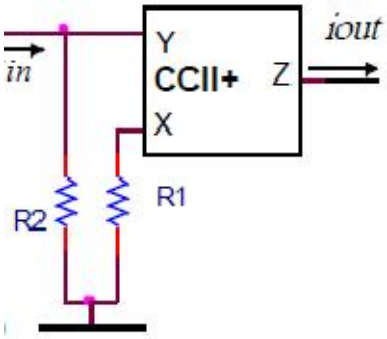

Fig 2-5 (a) current amplifier.

V-I converter Figure (b) is an important circuit block in current code amplifier design.

$$Iz = g.Vy$$

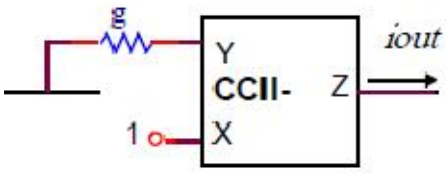

Fig 2-5 (b) V-I converter.

Current integrator is presented in Figure (c)

$$I_{out} = \frac{I_{in}}{sCR}$$

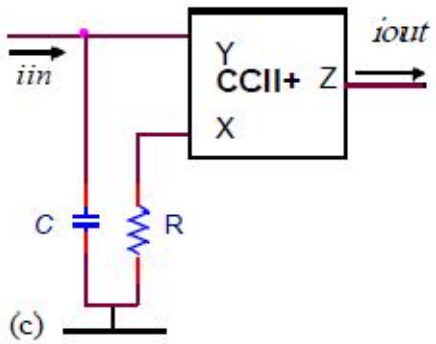

Fig 2-5 (c) Current integrator

Current differentiator is obtained, as pictured in Figure d

$$I_{out} = sCR.I_{in}$$

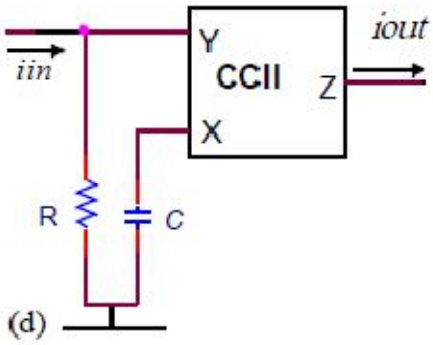

Fig 2-5 (d) Current differentiator

2.1.2.2 Voltage Amplifiers

Voltage amplification can be obtained by adding a voltage buffer to the VCCS[6] .

The voltage amplifier shown in Figure (a) is implemented through the use of two CCII blocks. The second CCII performs the buffering operation, so it can be avoided either when R2 resistance considered the load or with less value than load resistance.

$$V_{out} = V_{in} \cdot \frac{R_2}{R_1}$$

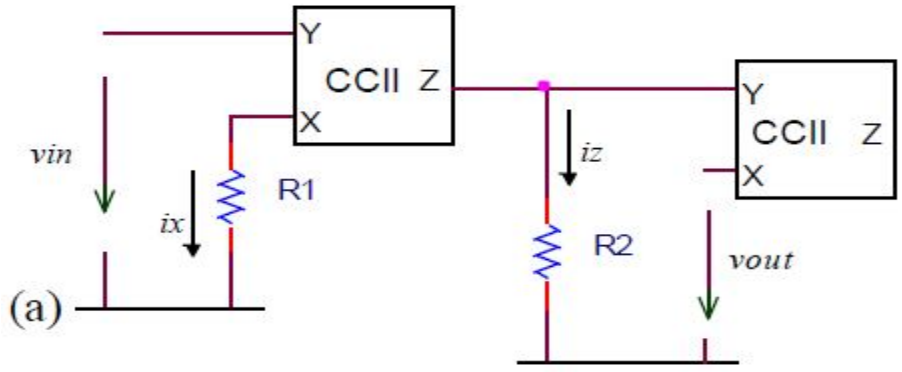

Fig 2-6 (a) voltage amplifier

Voltage integrator is depicted in Figure (b) The second current conveyor ensures again the voltage buffer operation at the output.

$$V_{out} = \frac{V_{in}}{sCR}$$

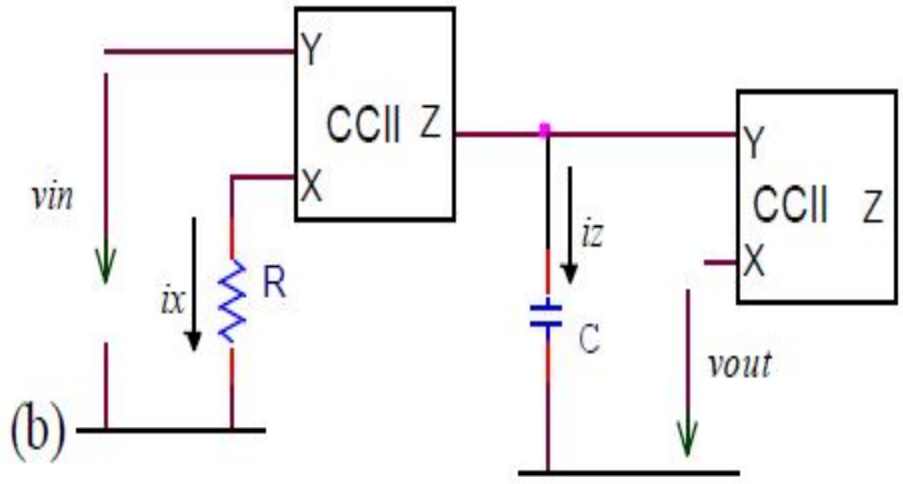

Fig 2-6 (b) voltage integrator.

Voltage differentiator, also the passive elements can be swept to reach the design Figure(c)

$$V_{out} = sCR.V_{in}$$

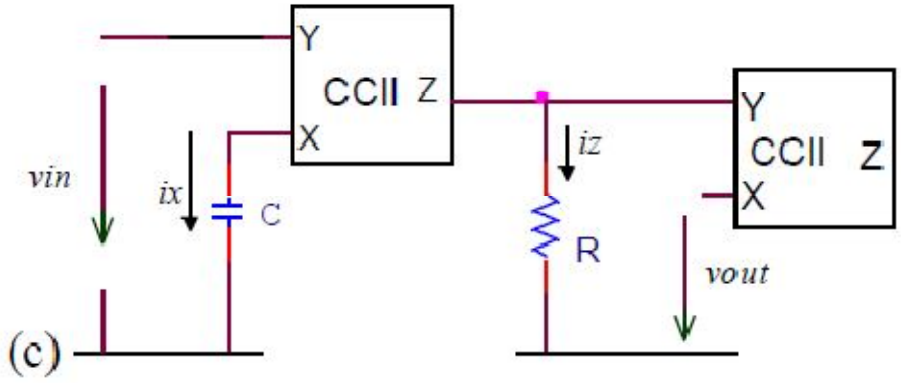

Fig 2-6 (c) voltage differentiator.

2.1.2.3 Oscillators

Current conveyor (CCII) has attracted the attention of researchers in the field of oscillators due to its distinct advantages over operational amplifier. This is attributed to their larger signal bandwidth, greater linearity, wider dynamic range, simple circuitry and low power dissipation.

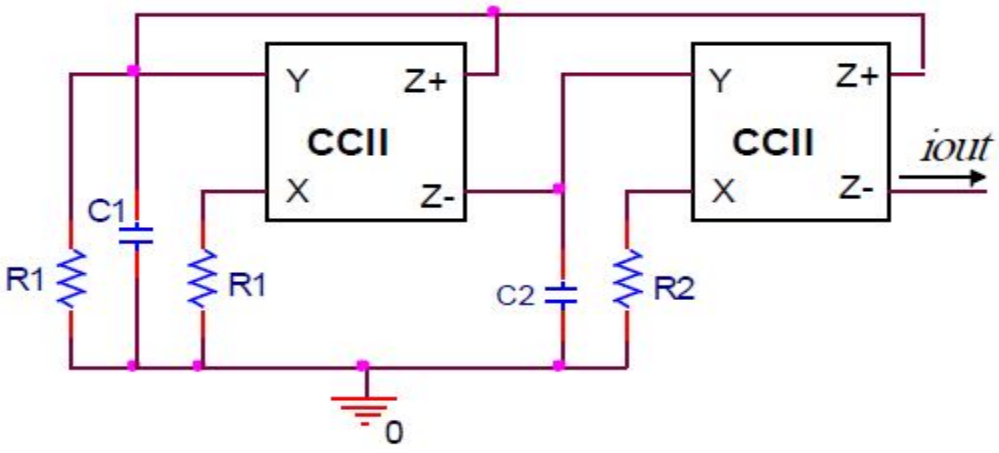

Fig 2-7: CCII-based oscillators

Here only two CCII blocks are needed Figure .The design equation for this oscillator is the following:

Oscillation frequency $(\omega_o) = \frac{1}{\sqrt{C_1 C_2 R_1 R_2}}$

2.1.2.4 Filters

This is also a very important application of CCII block as better results are obtained by filters using CCII. [4]Operational amplifier based filter topologies can be converted to a current conveyor based circuits. An example of this is the Sallen-Key SAB (single OpAmp biquad) filter which is converted to a CCII- based current-mode filter structure.

However, in the voltage-mode circuit, the OpAmp serves as a voltage follower and, as a result; its circuit element is a current follower. For the reason a second generation CC can by used as a substitute for the OpAmp in a very limited number of applications.

There has been great interest in proposing active filters using second generation current conveyors (CCIIs) to realize current transfer functions. This type of filter will be referred to as a current-mode filter. There are two types of current-mode filters. The first type has one or more inputs and a single output . The other type has one input and realizes the three well-known types of transfer functions at three different outputs. Also, by adding the high-pass output current to the low-pass one a notch response will be realizable without adding any extra CCIIs. The all-pass response is realizable by adding the three output currents provided that the band-pass polarity is opposite to both the low-pass and high-pass polarities.

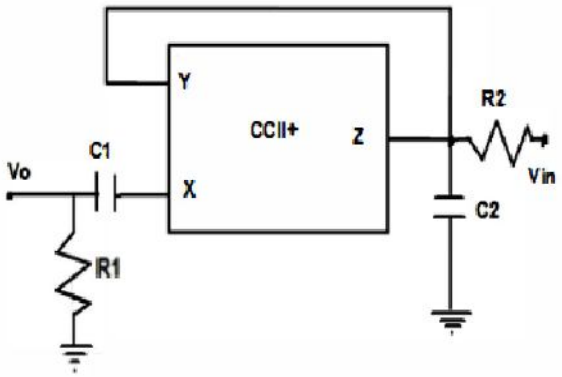

Fig 2-8 (a): CCII+ based Low pass filter[5]

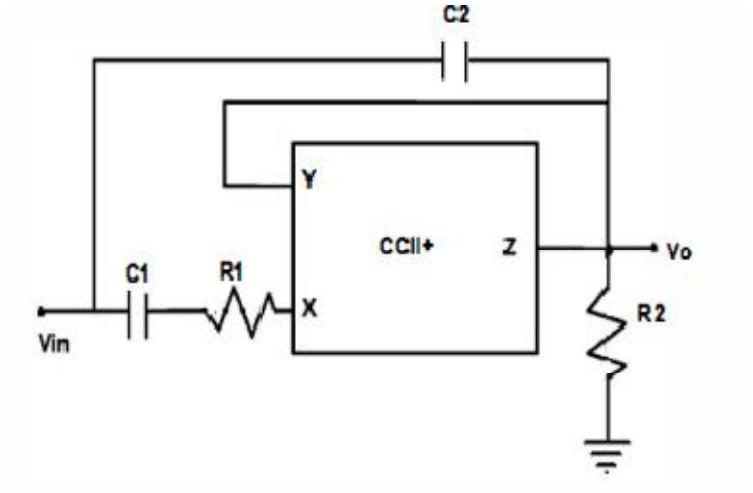

Fig 2-8(b): CCII+ based high pass filter

In switched-current signal processing, antialiasing and post smoothing lowpass filters are needed and also current-mode circuits need to interface with voltage- mode circuits. It would be therefore desirable to have a single circuit which can perform both filtering and interfacing (rather than two separate circuits) to reduce the system complexity, power, size and cost. For this purpose, a voltage to current lowpass filter suitable for use at the input of a switched-current circuit has been developed using a single dual output CCII.

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[2] Issa Eldbib " Low Voltage Current-Conveyors Design Techniques"

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[5] Garima Varshney, Neeta Pandey, Raj Eshwari Pandey, Asok Bhattacharyya "Performance Comparison Of Filter Circuits Based On Two Different Current Conveyor Topologies"

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CHAPTER 3

SECOND GENERATION CURRENT CONVEYOR

AND PARASITIC ELEMENTS

Due to voltage follower property between ports Y and X and current follower property between port X and Z , current conveyor can be used to realize electronic function operating in current mode as well as voltage mode. Several implementations have been described to implement this building block[1].

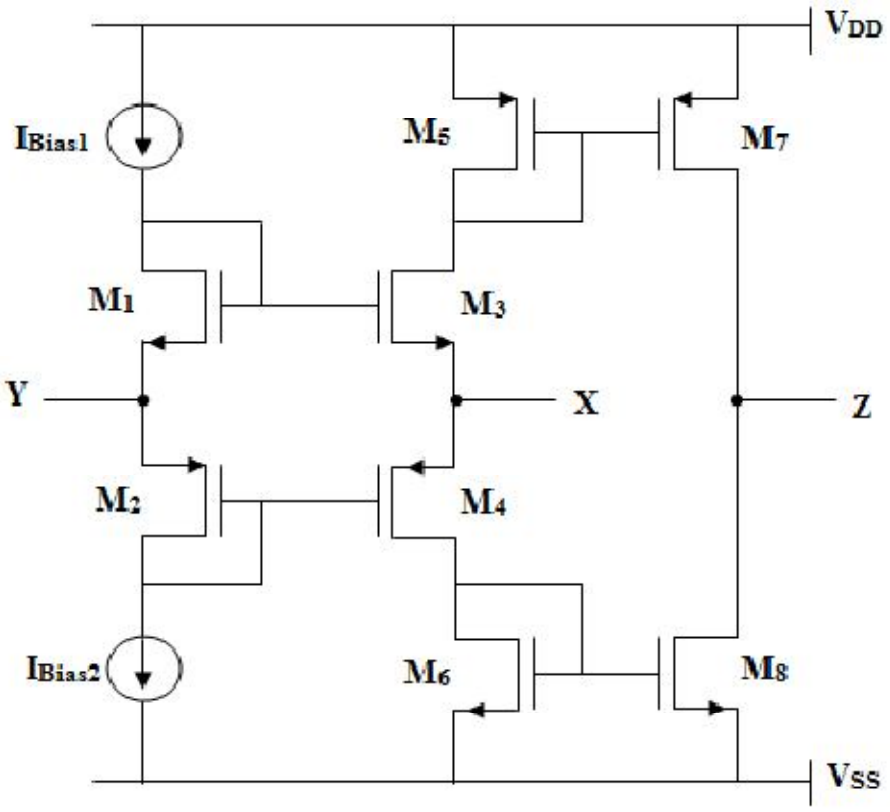

Fig 3-1:Single output Translinear CCII

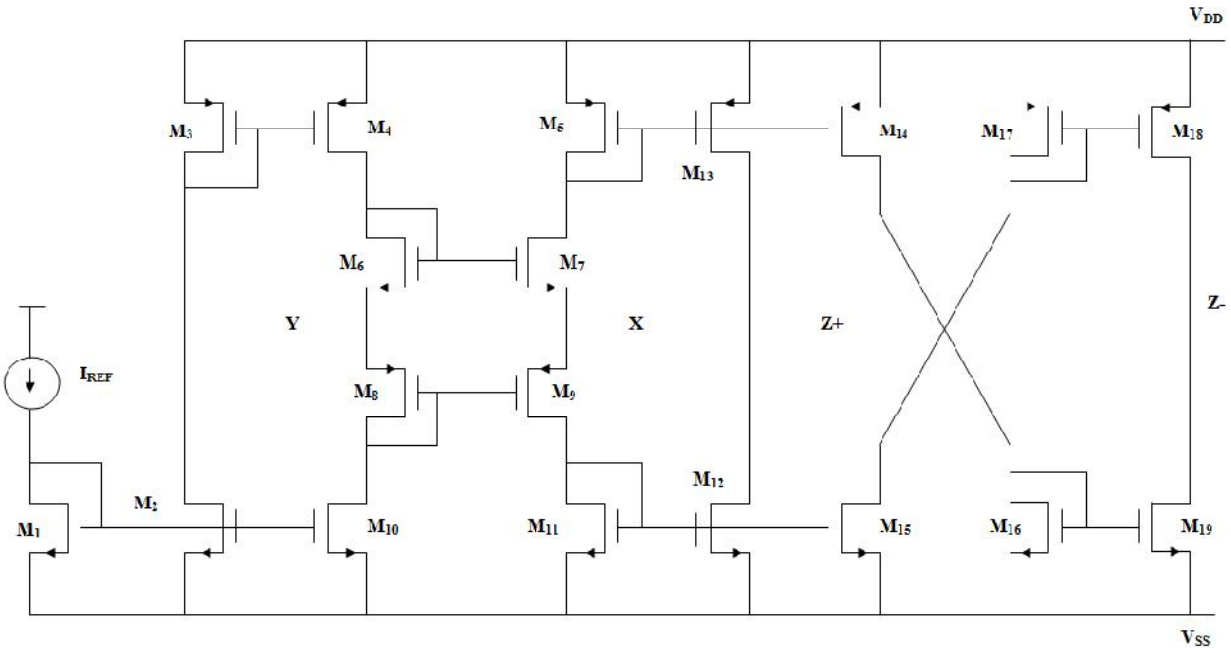

Fig 3-2:Double output Translinear CCII

Above figures show the basic implementation of CCII in translinear form. The two circuits use a mixed translinear loop[3] DC biased by the two current sources I_o to get a high input impedance at terminal Y. For CCII+ two complementary current mirrors allow to replicate on terminal Z the input current flowing through port X .The circuits which have been used for various simulations were implemented with minor changes from the forms given in above figures. Particular attention has been given when designing the input terminal Y to increase the input impedance at port Y[1].

3.1 IDEAL CCII:

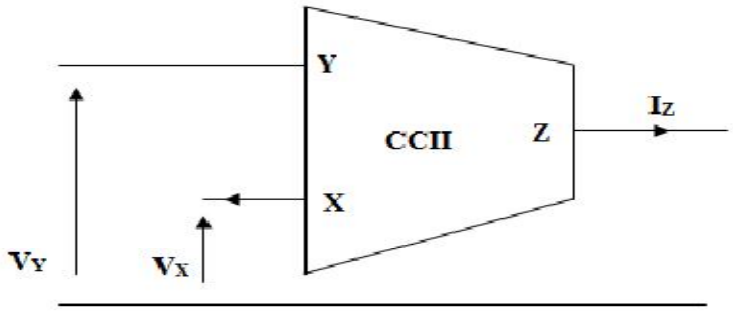

Fig3-3: Ideal CCII

Impedance Level of Ports for Ideal CCII **Table 3.1:**

CCII PORTS	**IMPEDENCE LEVEL**
X	Low (ideally zero)
Y	High (ideally infinite)
Z	High (ideally infinite)

3.2 REAL CONVEYOR AND ITS PARASITIC ELEMENTS:

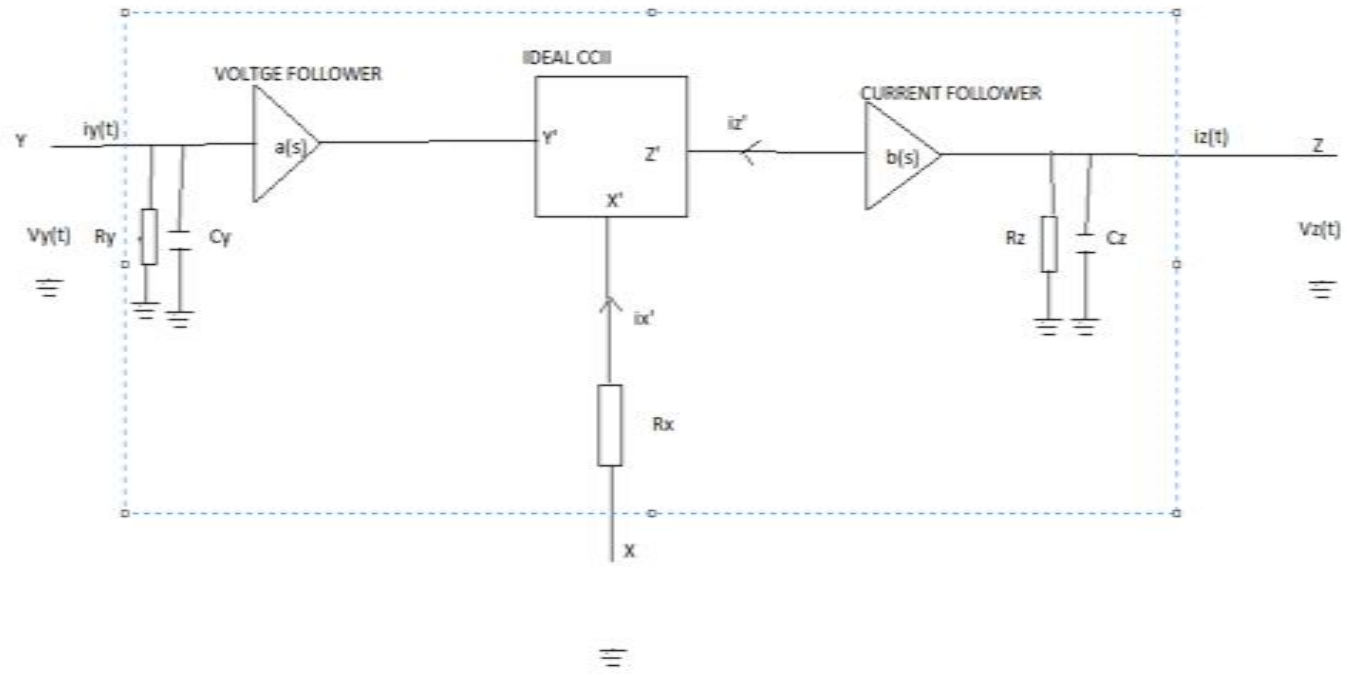

Fig 3-4. THE REAL CCII (i.e. its parasitic and the ideal CCII)

The ideal conveyor as [1]general equation allows only an approximate analysis of circuit implemented from CCIIs.When possibilities of an electronic function will have to be determined and notebaly its performance at frequencies above Mhz range,it will necessary to be considered as a simplified circuit for CCII. But this must be relatively close to the real CCII.this model will have to include the different parasitic impedances of circuit as well as the possible variations according to frequency , of the voltage and current transfers[1].

Above figure represent the [1]common equivalent circuit that will be used to show the behavior of real conveyors. The CCII is represented by dotted lines. The circuit contains an ideal CCII defined by relationship:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix}$$

- Between respectively each port Y and Z and the ground , the circuit contains a parallel equivalent parasitic impedance R_y and R_z.
- R_x is the output resistance of the equivalent thevenin generator seen from port X.
- β(s) and α(s) are respectively the voltage and current transfers of the conveyor that will generally be described by the following first order functions[2] :

Voltage transfer function:

$$\beta\,(s) = \frac{\beta o}{1} + \left(\frac{s}{\omega_\beta}\right)$$

Current transfer function:

$$\alpha\,(s) = \frac{\alpha_0}{1} + \left(\frac{s}{\omega_\alpha}\right)$$

- β_o and α_o are the values of these transfer functions at low frequencies.

- Values of β_o and α_o are close to unity.
- W_β and W_α represent their corresponding poles.

The matrix equation of ideal CCII thus modified for real CCII[4] and it becomes:

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 1/(R_y \,//\, C_y) & 0 & 0 \\ \beta(s) & R_x & 0 \\ 0 & +\alpha(s) & 1/(R_z \,//\, C_z) \end{bmatrix} \times \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix}$$

3.3 DETERMINATION OF PARAMETERS OF REAL CCII:

Determination of voltage transfer function:

- $\beta(s) = V_x / V_y$ is [1]the voltage transfer function of the conveyor. It has to be determined as a function of the frequency. An infinite R_L connected at X , the conveyor being driven on Y by a voltage generator with zero output resistance, and with output Z grounded.

Determination of current transfer function:

- $\alpha(s) = I_z / I_x$ [1]is the current transfer function of the conveyor. It has to be determined with an input current applied on port X.The current I_z is then the current that flows through port Z which is grounded; port Y being also grounded.

Determination of Y port parameters:

- The values for R_y and C_y will be determined with port X loaded with infinite impedance[1]; port Z grounded. The input voltage in this case applied at Y from a generator with zero output resistance.

Then the variation according to the frequency of the current I_y that goes into conveyor allows to determine the evolution of the input impedance:

$$Z_y = (R_y // C_y) = V_y / I_y .$$

R_y is the value of the impedance at low frequency.

The value C_y is then deduced from the -3 DB cutoff frequency f_y of Z_y;

$$C_Y = \frac{1}{2\pi} f_Y R_Y$$

Determination of X port parameters:

- The value of R_x is determined with outputs Y and Z grounded. When an input current I_x is applied on port X, the resulting voltage V_x allows to determine R_X[1]:

$$R_X = \frac{V_X}{I_X}.$$

Determination of Z port parameters:

- The values for R_z and C_z that constitute output port impedance of the current generator on port Z will be determined for the conveyor driven by a current I_x on X with port Y grounded[1] .Then the voltage V_z which results at port Z loaded by infinite impedance , allows to determine R_z at low frequency:

$$R_z = \frac{V_z}{I_X} .$$

R_z is the value of the impedance at low frequency.

The value C_z is then deduced from the -3 DB cutoff frequency f_z ;

$$C_Z = \frac{1}{2\pi} f_Z R_Z.$$

3.4 ANALYSIS OF CCII CHARACTERITICS:

- **DC ANALYSIS:**

  The dc analysis of the CCII is performed in order to observe:

  - Voltage transfer characteristics between ports Y and X.
  - Current transfer characteristics between ports X and Z+, Z-.

  For voltage transfer characteristics, a varying voltage source is applied at port Y and corresponding output is taken at port X. The input voltage is varied along X axis and from the figure below it can be seen that output follows the input for a range of -0.5v to 0.5v i.e. 1V.

  During this analysis, the port Z was at ground terminal.

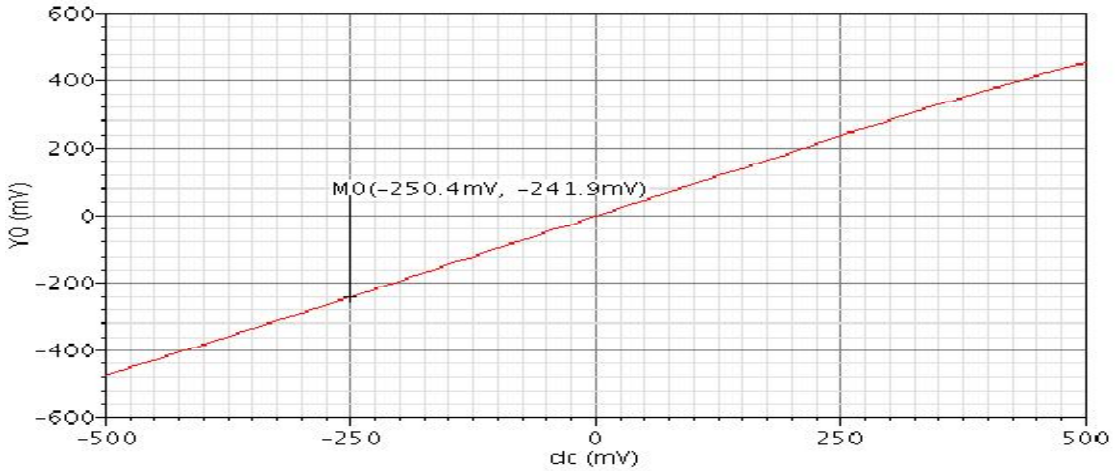

Fig 3-5(a) : dc voltage characteristic at port X

For current transfer characteristics, a varying current source is applied at port X and corresponding output is taken at ports Z+ and Z-. The input current is varied from 50µA to +50µA and the desired output current characteristics are shown in figures and during this analysis, the port Y was at ground terminal.

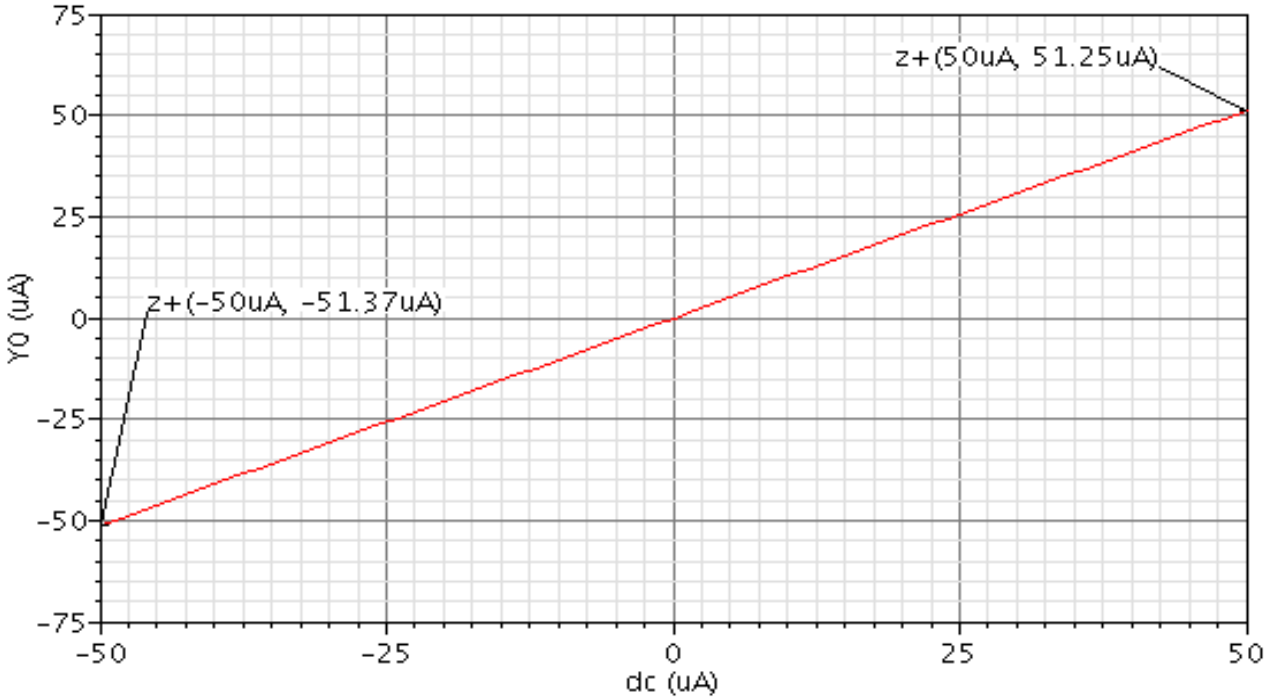

Fig 3-5(b): dc current characteristic at port Z+

- **TRANSIENT ANALYSIS:**

Transient analysis of the CCII is performed in order to examine the voltage transfer characteristics between ports Y and X with respect to time. It is performed by applying voltage source at port Y:

- By applying an AC voltage source of amplitude 0.4V peak-to-peak and having frequency 100 MHz at port Y ; its transient response is shown in figure.

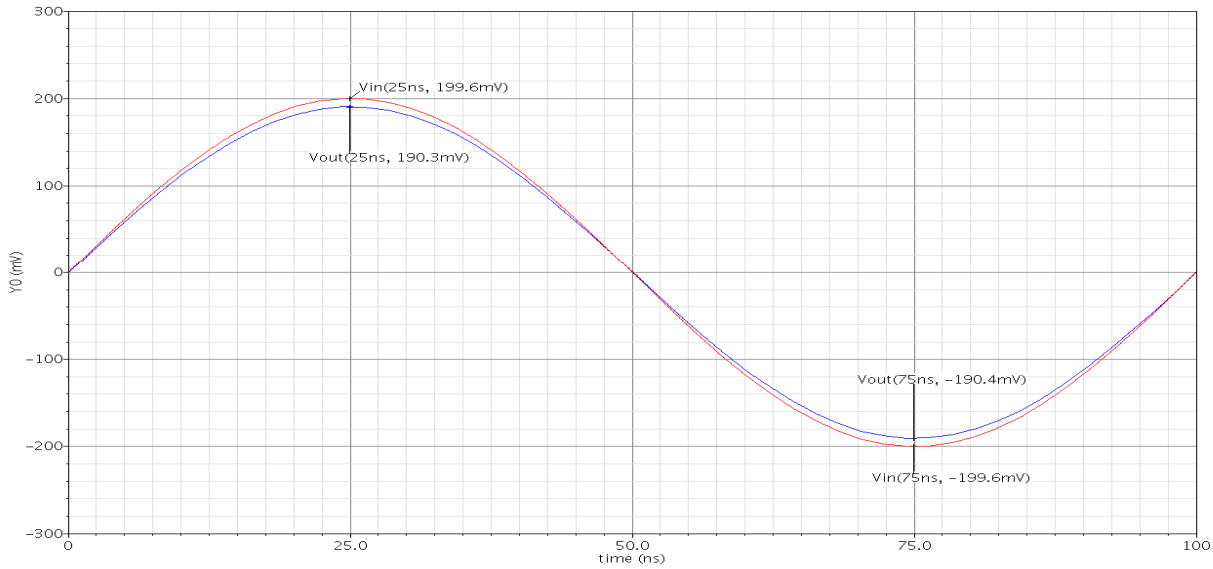

Fig 3-6: Voltage transient characteristics by applying a sine wave.

Offset value:

It can be seen from the figure that output follows the input correctly and an offset is found between input and output. This type of characteristics validates the performance of CCII as voltage follower between ports Y and X. The output offset voltage can be minimized by increasing the width of the transistors that forming the translinear loop. But this increase in the width of transistors increases the capacitances associated with these transistors and this reduces the voltage transfer bandwidth.

- **AC ANALYSIS**

For a typical CCII frequency response (AC analysis in PSPICE) of the voltage gain at port X is shown in figure below.

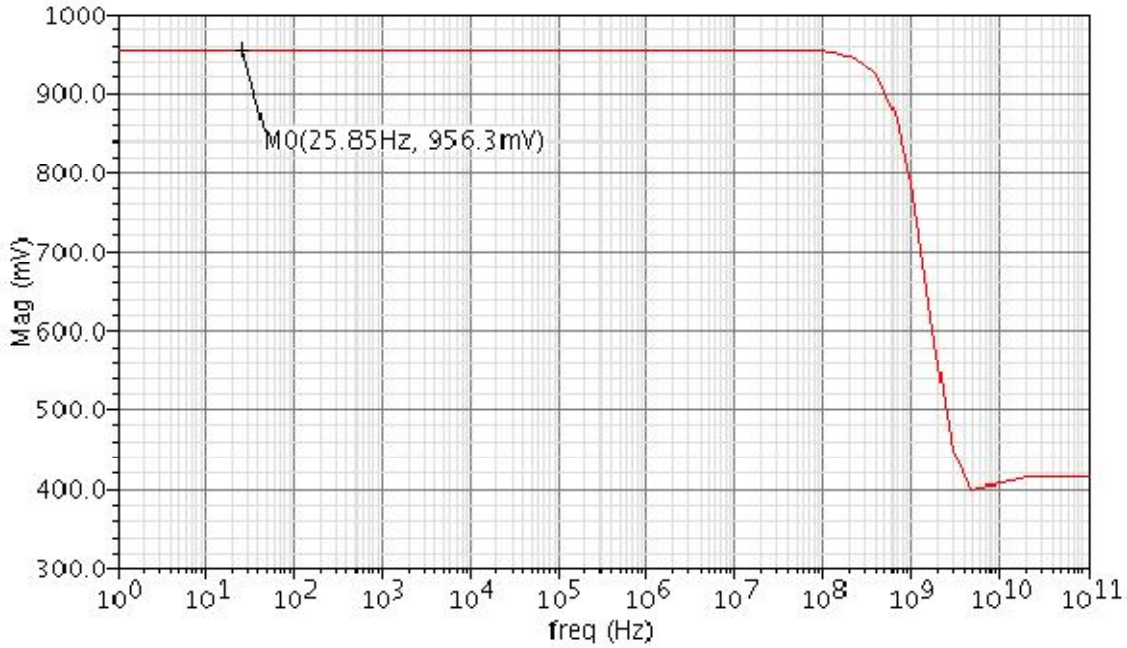

Fig 3-7 : Frequency response of voltage gain at port X.

Similarly current gain at port Z whose ideal value is unity shows frequency limitation at Ghz frequency range.

W_α and W_β are thus defined at 3DB frequency in current and voltage AC analysis curve respectively[5].

REFERENCES

[1] Alain Fabre. "On the frequency limitations of the circuits based on second generation current conveyors", Analog Integrated Circuits and Signal Processing, 03/1995

[2] Ahmed M. Soliman "Current-Mode Universal Filters Using Current Conveyors: Classification and review".

[3] Garima Varshney, Neeta Pandey, Raj Eshwari Pandey, Asok Bhattacharyya "Performance Comparison Of Filter Circuits Based On Two Different Current Conveyor Topologies"

[4] Giuseppe Ferri & Nicola C.Guerrini "Low Voltage Low power CMOS current conveyors"

[5] Saddam Husain & Shahabuddin Ali RR Institute of Modern Technology, BBD University, Lucknow "Current Conveyors and their Analog & Digital Applications"

CHAPTER 4

TRANSLINEAR LOOP BASED CCII

Translinear CCII structure performs the following two functions:

- Voltage following action from port Y to port X
- Current following action from port X to port Z.

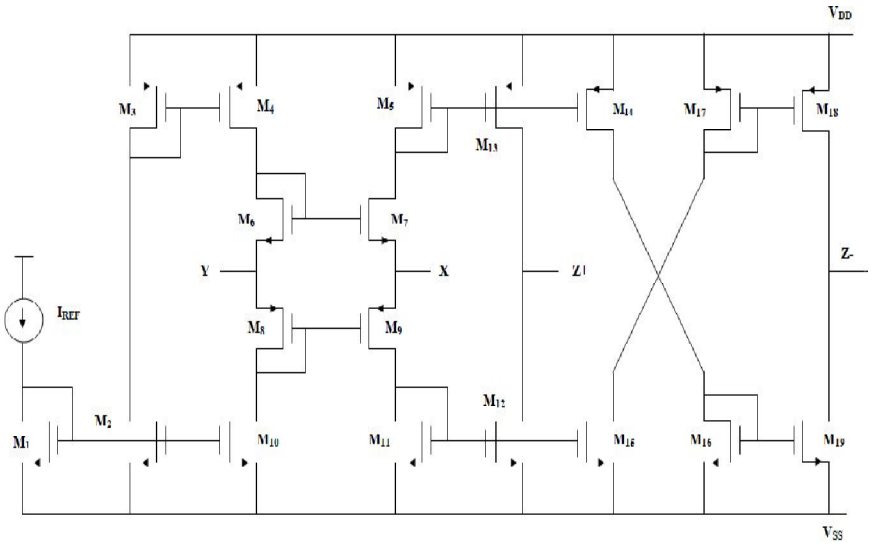

Fig 4-1: Translinear Second Generation Current Conveyor

4.1 SUB CIRCUITS OF TRANSLINEAR CCII:

The circuit comprises of four different blocks:

- Transistors M6-M9 form the translinear loop whose role is to provide equal voltage in both X and Y ports[2]. This input cell presents high impedance at the input port Y and a low impedance at the output port X.

- Transistors M4 and M10 allow the mixed loop to be biased by the dc current Io.

• Transistors (M11, M12) and (M5, M13) form the NMOS and PMOS current mirrors which supply the current being supplied at port X to the port Z+, which is at a high impedance level.

• The cross coupled structure formed by transistors M14-M16 convey the same current but in inverting mode to the output port Z-, which is also at high impedance level.

The biasing current of the circuit plays an important role in determining the power consumption and the resistance at port X. So it is set to 50µ in order to meet the desired specifications.

4.1.1 Typical parameters values for a translinear CCII+ :

-Voltage gain(β_o) = 0.999
-current gain(α_o) = 1.18
-3 db frequency(for voltage output) = 1.03 Ghz
-X port impedance = 4.5KΩ
-Z port impedance = 577 KΩ
-Output Offset V = 0.473mv
- Output Offset I = -3.3µa

4.1.2 MOS translinear loop:

The term "translinear" was first introduced by Gilbert in 1975, which emphasizes on the fact that trans-conductance (g_m) is linear with current for the case of BJT transistor and also for MOS transistor operating in weak inversion. However, when transconductance is linear with the voltage instead of the current as:

$$G_M = \frac{di}{dv} = bv$$

where b is a scaling factor, then it leads to an another class of translinear circuits that can

be implemented with the quasi quadratic law of the MOS transistor.

The input cell comprises of transistors M6-M9 form the translinear loop[2] and is shown in figure. This cell is the main core of the circuit as it provides equal voltages at ports X and Y, thus provide the voltage following action. This input cell presents high input impedance at the input port Y and a low impedance at output port X.

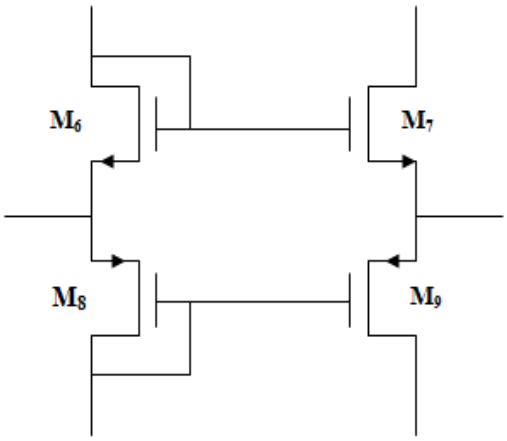

Fig 4-2: Mixed Translinear Loop.

In order to maximize the voltage gain, the transconductance of the transistors M7 and M9 must be high . So for a given bias current I0 and length of transistor, the g_m can only be increased by increasing the width of the transistors. Therefore, in order to maximize the voltage gain, the width of the transistors forming the translinear loop is kept large while designing the circuit[4].

4.1.3 Current mirror:

The current mirror is one of the main building blocks of analog circuit design. For high performance applications, the accuracy and output impedance are the most important parameters to determine the performance of the current mirror. It is widely used in the biasing or the loading elements. The current variations due to the supply and the temperature can be reduced by using current mirror as the biasing elements. Ideal CM has zero input and infinite output resistance, which implies that input voltage does not vary with input currents and output currents are independent of applied output voltage. However, the practical CMs have non zero input and finite output resistances and thus do not copy the current properly. Therefore, special design approach has to be taken while designing CMs in order to ensure proper mirroring of current[3].

The design of current sources in analog circuits is based on copying currents from a reference with the assumption that one precisely defined current source is already available. Two identical MOS devices that have equal gate-to-source voltages and operate in saturation carry equal currents.

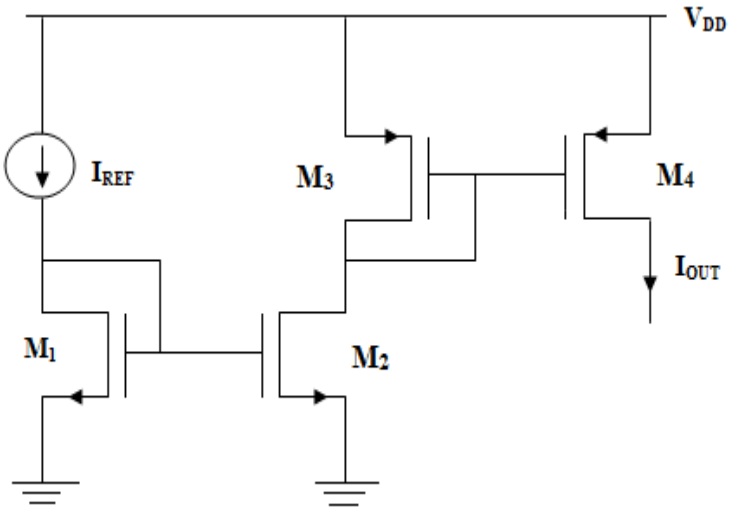

Fig 4-3: Two Stage Current Mirror

Two stage Current Mirror is shown in figure above. In order to calculate the relationship between I_{OUT} and I_{REF}, all the transistors are assumed to be in saturation region and channel length modulation effect is neglected. Different drain current equations for this circuit are given as:

$$I_{D2} = I_{REF} \times \left[\frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1}\right]$$

$$I_{D4} = I_{D3} \times \left[\frac{\left(\frac{W}{L}\right)_4}{\left(\frac{W}{L}\right)_3}\right]$$

$$|I_{D3}| = |I_{D2}|$$

Thus $$I_{D4} = \alpha\beta I_{REF}$$

The current mirrors should have desirable characteristics:

a) Current transfer ratio must be precisely set by the (W/L) ratio and it should be independent of temperature.

b) Very high output resistance (high R_{out}) so that the output current is independent of output voltage.

c) Low input resistance (Low R_{in}).

d) Low input and output compliance voltages.

4.2 SIMULATION RESULT FOR TRANSLINEAR LOOP BASED CCII+ :

Simulation results for CCII+ are obtained at 2.5V supply and 0.35 µm technology.

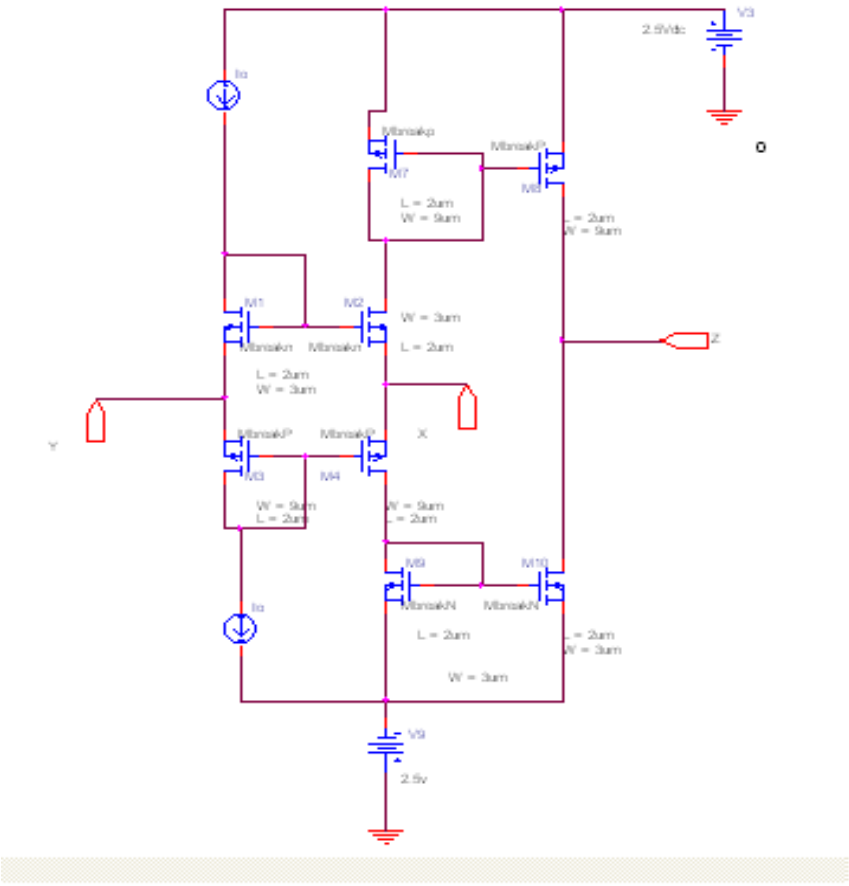

Fig4-4: Schematic Diagram of translinear loop based CCII+

❖ **DC ANALYSIS:**

DC voltage characteristics:

For voltage transfer characteristics, a varying voltage source is applied at port Y and corresponding output is taken at port X[1]. The input voltage is varied along X axis and from the figure below it can be seen that output follows the input for a range of -0.5v to 0.5v . During this analysis, the port Z was at ground terminal.

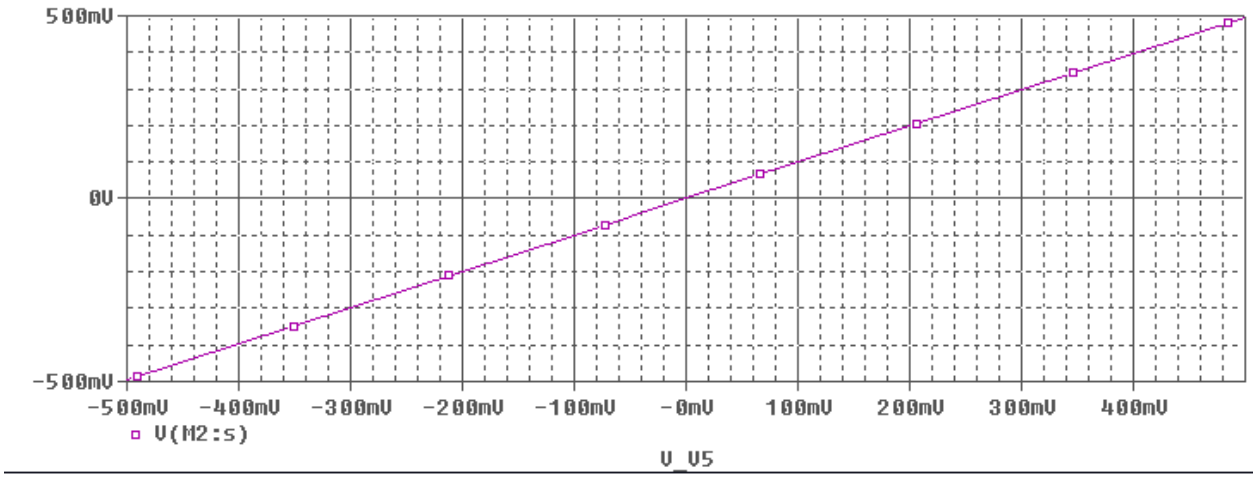

Fig 4-5(a): DC voltage transfer plot.

DC current characteristics:

For current transfer characteristics, a varying current source is applied at port X and corresponding output is taken at ports Z. The input current is varied from 50µA to +50µA and the desired output current characteristics are shown in figures below and during this analysis, the port Y was at ground terminal.

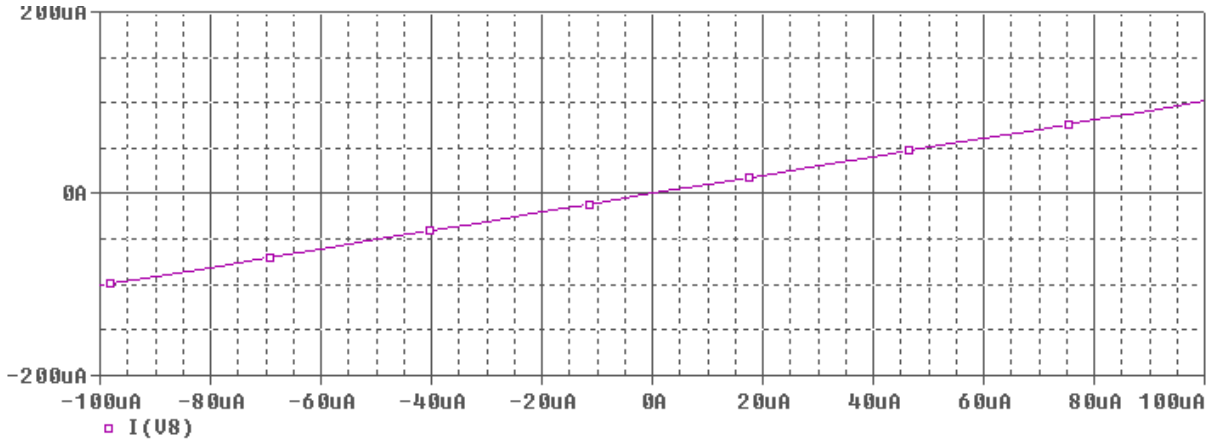

Fig 4-5(b): DC current transfer plot.

- **AC ANALYSIS:**

AC voltage characteristics:

The frequency response of the voltage gain at port X is shown in figure below:

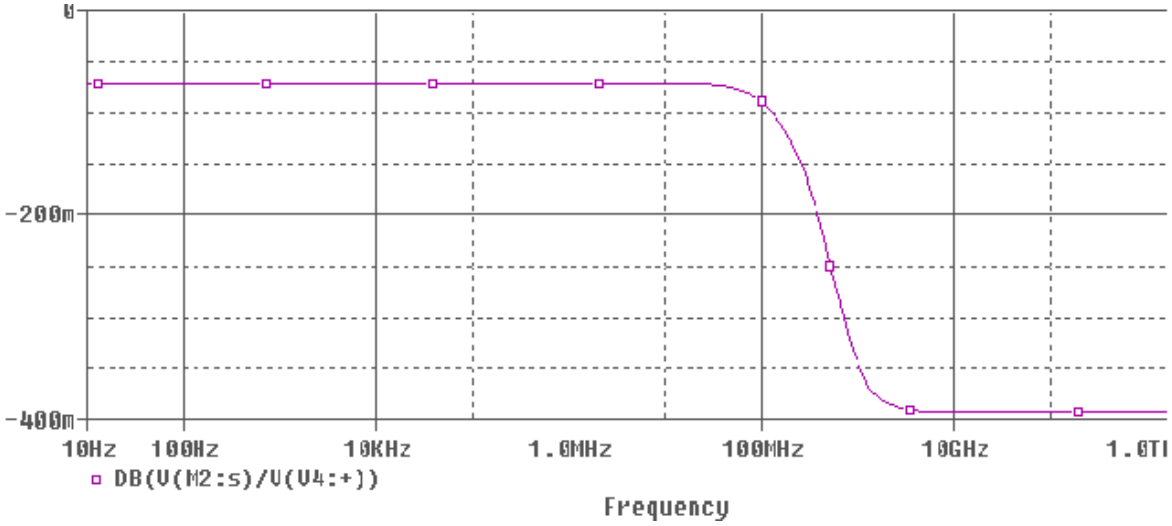

Fig 4-6(a): AC voltage plot at port X.

β (s) = V_x/ V_y : The voltage transfer function of the conveyor determined as a function of the frequency[1]. Its steady value comes out to be 0.991

The 3 db frequency (ω_β) of above AC voltage curve at port X comes out to be a very large value.

AC current characteristics:

The frequency response of the current gain at port Z is shown in figure below:

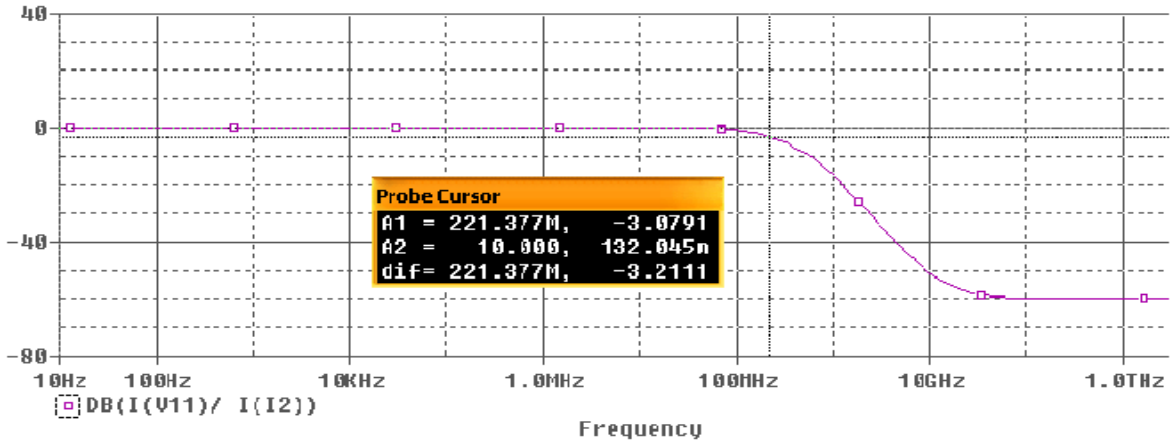

Fig 4-6(b): AC current plot at port Z.

α (s) = I_Z/ I_X : The current transfer function of the conveyor determined as a function of the frequency[1]. Its steady value comes out to be 1.015

The 3 db frequency (ω_α) of above AC current plot at port Z comes out to be 221.37Mhz.

❖ **PARASITIC IMPEDANCES:**

- R_y and C_y : R_y is the value of the Y port impedance at low frequency.
  The value C_y is then deduced from the -3 DB cutoff frequency f_y of Z_y;

$$C_Y = \frac{1}{2\pi} f_Y R_Y$$

  The R_y value comes out to be 3.74TΩ and the C_y value comes out to be 0.028pf.
- $R_X = V_X / I_X$; value comes out to be 4.03 KΩ.
- R_z and C_z i.e. output port impedance of port Z .

$$R_z = \frac{V_z}{I_X} .$$

  R_z is the value of the impedance at low frequency.

The value C_z is then deduced from the -3 DB cutoff frequency f_z;

$$C_Z = \frac{1}{2\pi} f_Z R_Z.$$

The R_z value comes out to be 3.956MΩ and the C_z value comes out to be .0021pf.

❖ TRANSIENT ANALYSIS:

By applying an AC voltage source having frequency 100 MHz at port Y its transient response is shown in figure below:

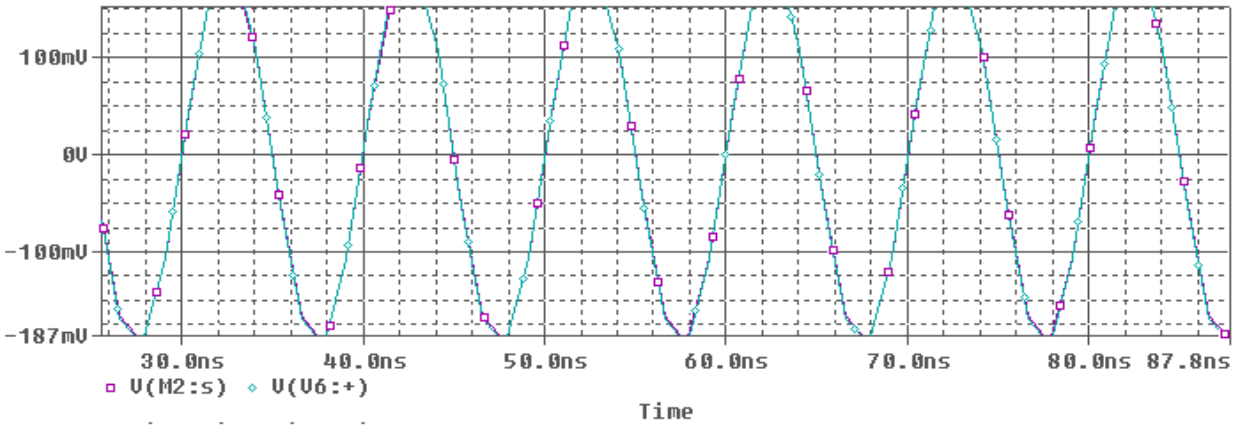

Fig 4-7: Output Voltage transient plot.

Thus the output offset voltage value comes out to be 1.1mv which is calculated by above transient plot.

Similarly, by applying current sinusoidal input, the output offset current value comes out to be 2μa which is calculated by current plot.

- **Power dissipation:** By observing output simulation file in PSPICE ; power dissipation of above circuit comes out to be 7.53×10^{-04}watt.

❖ 4.1 PARAMETERS TABLE FOR TRANSLINEAR LOOP BASED CCII+:

PARAMETER	VALUE
β_o	0.991
α_o	1.015
ω_β	Very large
ω_α	221.37Mhz.
R_y	3.74TΩ
C_y	0.028pf.
R_x	4.03 KΩ.
R_z	3.956MΩ
C_z	.0021pf
Offset V	1.1mv
Offset I	2μa
Power dissipation	7.53×10^{-04}watt

REFERENCES

[1] Alain Fabre. "On the frequency limitations of the circuits based on second generation current conveyors", Analog Integrated Circuits and Signal Processing, 03/1995

[2] Garima Varshney, Neeta Pandey, Raj Eshwari Pandey , Asok Bhattacharyya “Performance Comparison Of Filter Circuits Based On Two Different Current Conveyor Topologies”

[3] Giuseppe Ferri & Nicola C.Guerrini “Low Voltage Low power CMOS current conveyors”

[4] H . Barthelemy, M . Fillaud, S . Bourdel, and J . Gaubert, "CMOS inverters based positive second generation current conveyor," Analog Integr. Circ Sig Process pp. 1 4 1-146, 2007.

CHAPTER 5

DIFFERENTIAL AMPLIFIER BASED CCII OR SURAKAMPONTORN'S CCII

5.1 Differential pair based CCII :

In literature, a large number of current conveyors utilizing a differential pair which realizes through a feedback connection the input voltage buffer .

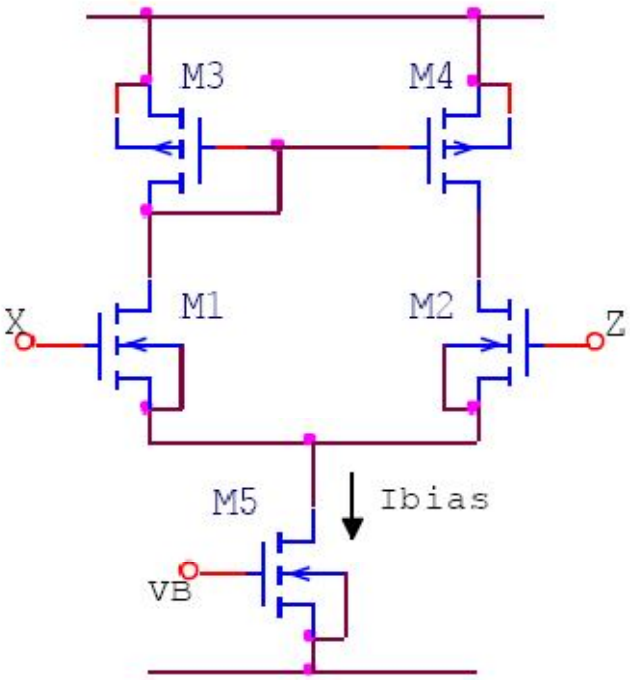

Fig 5-1 :Differential pair

For LV LP applications, a special attention to the supply values of current sources, it is fundamental to guarantee signal dynamic and a constant bias current independent from supply voltage. The choice of biasing current is one of the important keys to power consumption[5], differential pair transistor sizes, and X node parasitic impedance, after implement the current source have to set M1-M4 sizes.

There are lot of developments of Second Generation Current Conveyors (CCII) that are realized by the use of a differential amplifier (diff-amp) as a circuit building block. One of the first CMOS-based promising techniques that uses differential amplifier to implement CCII is proposed by Surakampontorn is detailed in this chapter.

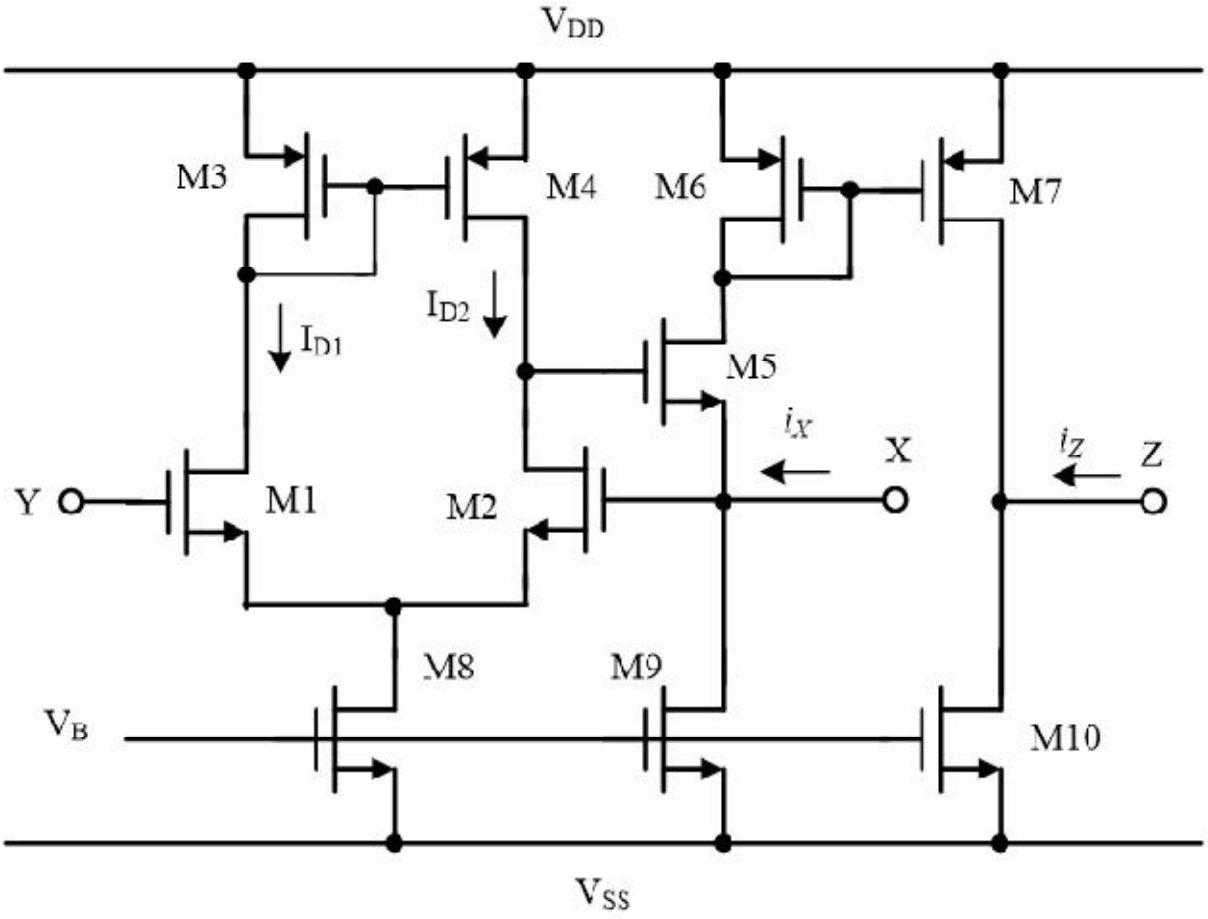

Fig 5-2: Surakampontorn CCII[2]

Above Fig. shows the circuit diagram of the first possible solution of CMOS-based CCII that was proposed by Surakampontorn . In fact, this is a CMOS-based version of the bi-polar based voltage to current converter circuit .

5.2 SUB CIRCUIT :

Diff-amp:

The circuit is operated in class A. Transistors M1, M2 and M8 form as a diff-amp[2].

Current mirror:

The current mirror M3-M4 forces the drain currents $I_{d1} = I_{d2}$, the gate source voltages of transistors M1 and M2 are equaled, or $Vgs_1 = Vgs_2$.

This means that the diff-amp functions as a voltage follower, then forces $V_Y = V_X$.

Transistor M5, which is connected in the form of a source follower, functions as a current follower stage and also provides a low-output resistance at port X[3]**.** Transistor M5 and current mirror M6-M7 are used to sense the current flowing from port X to port Z. If the source and drain currents of M5 are equaled and the current gain of the current mirror M6-M7 is equaled to 1, then $i_Z = i_X$**..** Therefore, the circuit realizes CCII +

The value of parasitic impedance at port X or R_X is quite low and the impedance at port Z is high, as required by the current conveyor characteristics.

Applications of differential amplifier based CCII:

The CCII of the above Fig. has been employed as basic building blocks to realize CCII-based analog signal processing circuits in many different ways.

For example:

active capacitance multipliers, V-I scalar circuits , and low-sensitivity biquadratic filters[4].The CCII has also been constructed as current followers to realize a multiple output active filter based on current follower. Using the CCII Fig. a new circuit cell which is the combination of the CCII+ and CCII-was used to simulate resistively terminated LC ladder filters .

5.2.1 Typical parameters values for SURAKAMPONTORN'S CCII+ :

-Voltage gain(β_o) = 0.9938

-current gain(α_o) = 1.0037

-3 db frequency(for voltage output) = 776 Mhz

-X port impedance = 5.9Ω

-Z port impedance = more than 100KΩ

-Output Offset V = -4.52mv to 2.27mv

- Output Offset I = -1.04μa to 0.006 μa

-Input voltage range = -0.73 to 0.2 V

-Input current range = -100 μa to 100 μa

5.3 SIMULATION RESULT FOR SURAKAMPONTORN'S CCII+ :

Simulation results for CCII+ are obtained at 1.5V supply and 0.50 μm technology.

For ac analysis source voltage is 100mv and source current of 100 μa. is taken.

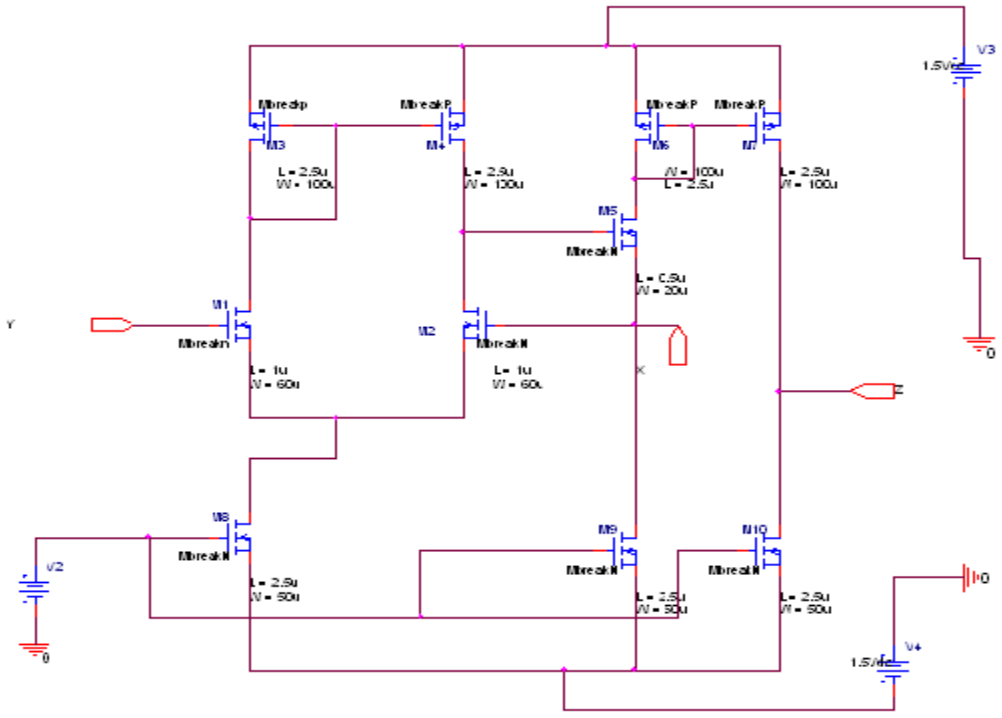

Fig 5-3: SCHEMATIC DIAGRAM OF SURAKAMPONTORN'S CCII+

TRANSISTOR ASPECT RATIOS:

Transistor	**W (μm)/L (μm)**
M1, M2	60/1
M3, M4	100/2.5
M5	20/0.5
M6, M7	100/2.5
M8, M9, M10	50/2.5

- **DC ANALYSIS:**

DC voltage characteristics:

For voltage transfer characteristics, a varying voltage source is applied at port Y and corresponding output is taken at port X. The input voltage is varied along X axis and from the figure below it can be seen that output follows the input for a range of -0.5v to 0.5v .

During this analysis, the port Z was at ground terminal.

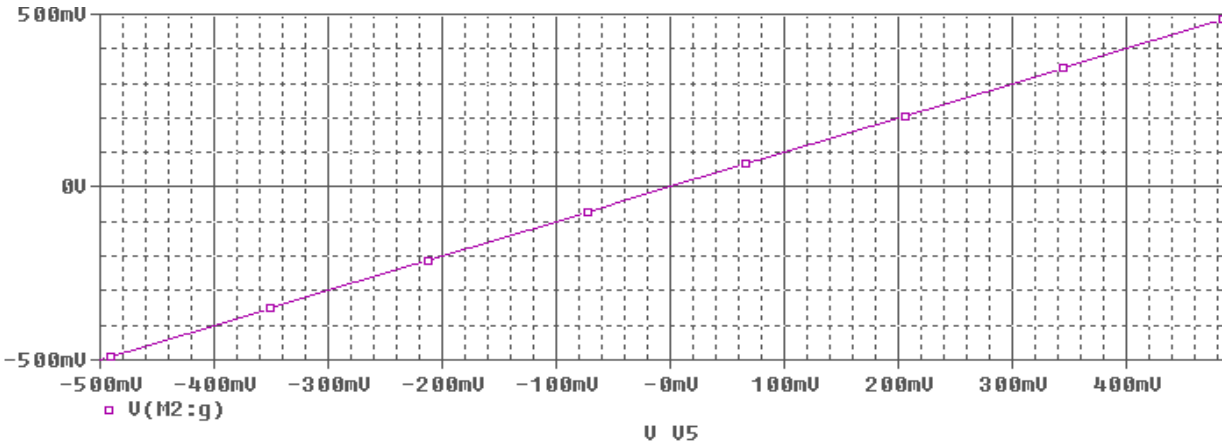

Fig 5-4(a): DC voltage transfer plot.

DC current characteristics:

For current transfer characteristics, a varying current source is applied at port X and corresponding output is taken at ports Z. The input current is varied from -30µA to +30µA and the desired output current characteristics are shown in figures below and during this analysis, the port Y was at ground terminal.

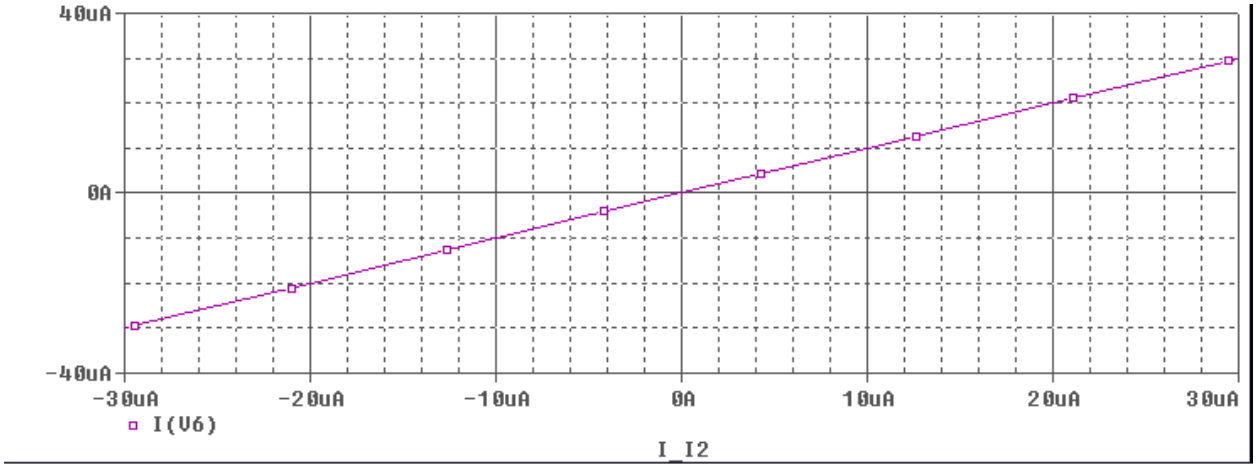

Fig 5-4(b): DC current transfer plot.

- **AC ANALYSIS:**

AC voltage characteristics:

The frequency response of the voltage gain at port X is shown in figure below:

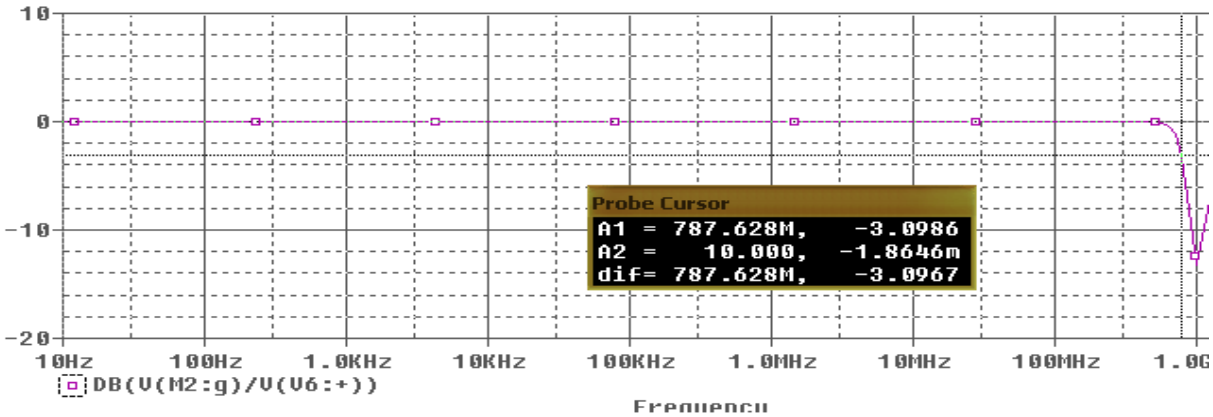

Fig 5-5(a): AC voltage plot at port X.

β (s) = V_x/ V_y : The voltage transfer function of the conveyor determined as a function of the frequency[1]. Its steady value comes out to be 0.999

The 3 db frequency (ω_β) of above AC voltage curve at port X comes out to be 787.62Mhz

AC current characteristics:

The frequency response of the current gain at port Z is shown in figure below:

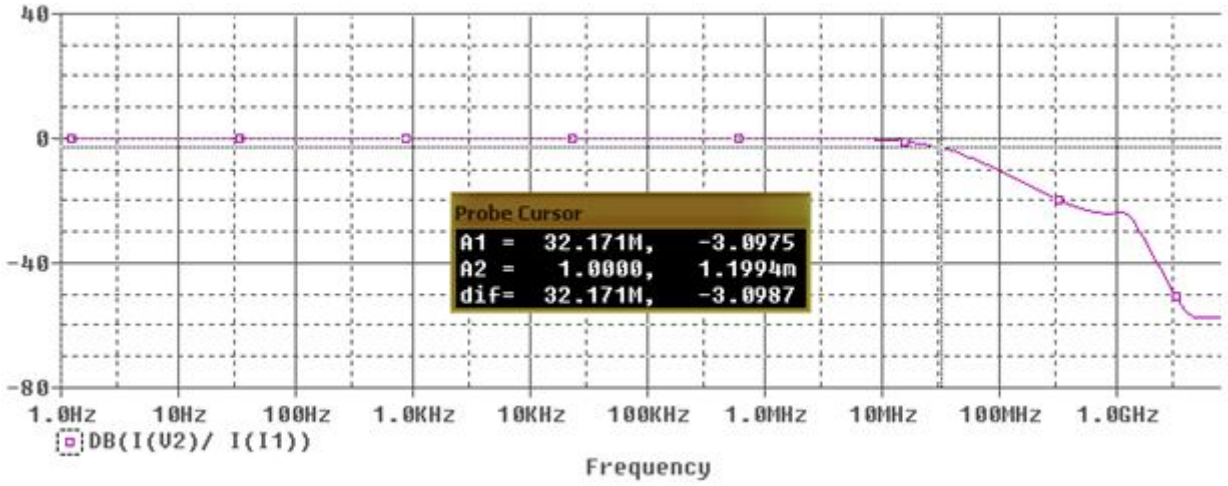

Fig 5-5(b): AC current plot at port Z.

α (s) = I_Z/ I_X : The current transfer function of the conveyor determined as a function of the frequency[1]. Its steady value comes out to be 1.0001

The 3 db frequency (ω_α) of above AC current plot at port Z comes out to be 32.17Mhz.

❖ **PARASITIC IMPEDANCES:**

- R_y and C_y : R_y is the value of the Y port impedance at low frequency.

  The value C_y is then deduced from the -3 DB cutoff frequency f_y of Z_y;

  $$C_Y = \frac{1}{2\pi} f_Y R_Y$$

  The R_y value comes out to be 1.8TΩ and the C_y value comes out to be 0.0058pf.
- $R_X = V_X / I_X$; value comes out to be 0.5Ω.

- R_z and C_z i.e. output port impedance of port Z .

$$R_z = \frac{V_z}{I_X}$$

R_z is the value of the impedance at low frequency.

The value C_z is then deduced from the -3 DB cutoff frequency f_z;

$$C_Z = \frac{1}{2\pi} f_Z R_Z$$

The R_z value comes out to be 14.01MΩ and the C_z value comes out to be .0341pf.

❖ TRANSIENT ANALYSIS:

By applying an AC voltage source having frequency 100 MHz at port Y its transient response is shown in figure below:

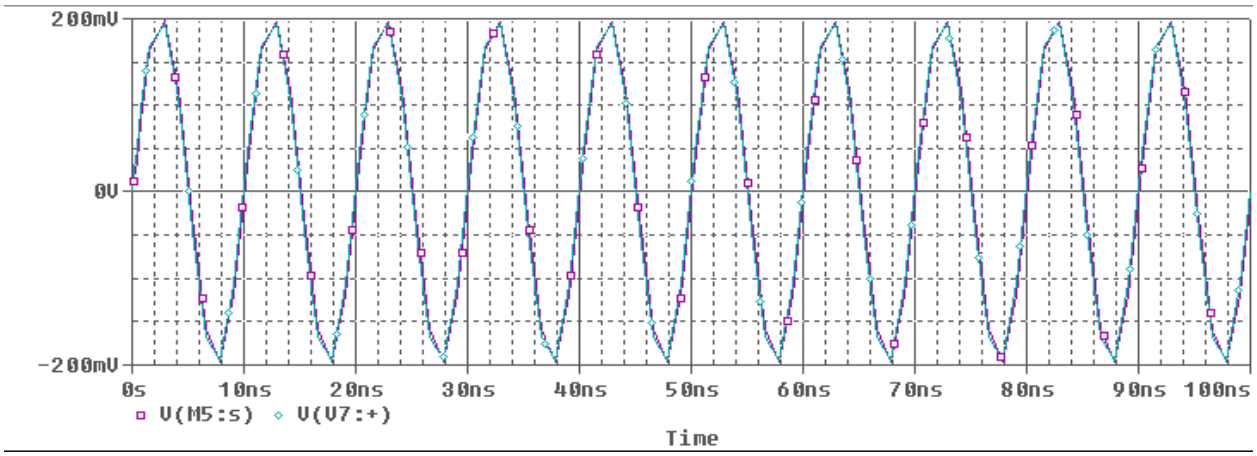

Fig 5-6: Output Voltage transient plot.

Thus the output offset voltage value comes out to be 2.5mv which is calculated by above transient plot.

Similarly, by applying current sinusoidal input, the output offset current value comes out to be 9μa which is calculated by current plot.

- **Power dissipation:** By observing output simulation file in PSPICE ; power dissipation of above circuit comes out to be 3.05×10^{-04}watt.

❖ 5.1 PARAMETERS TABLE FOR DIFFERENTIAL AMPLIFIER BASED CCII:

PARAMETER	VALUE
β_o	0.999
α_o	1.0001
ω_β	787.62Mhz
ω_α	32.17Mhz.
R_y	1.8TΩ
C_y	0.0058pf.
R_x	0.5Ω.
R_z	14.01MΩ
C_z	.0341pf
Offset V	2.5mv
Offset I	9μa
Power dissipation	3.05×10^{-04}watt

REFERENCES

[1] Alain Fabre. "On the frequency limitations of the circuits based on second generation current conveyors", Analog Integrated Circuits and Signal Processing, 03/1995

[2] Wanlop Surakampontorn and Khanittha Kaewdang “Development of Differential Amplifier Based the Second Generation Current Conveyors”

[3] Wanlop Surakampontorn, Member, ZEEE, Vanchai Riewruja, Kiattisak Kumwachara, and Kobchai Dejhan “Accurate CMOS-based Current Convevors” IEEE transactions on instrumentation and measurement, vol. 40. no. 4. august 1991

[4] WESSAM S. HASSANEIN, INAS A. AWAD AND AHMED M. SOLIMAN “New Wide Band Low Power CMOS Current Conveyors” Electronics and Communication Engineering Department, Cairo University, Egypt

[5] Giuseppe Ferri & Nicola C.Guerrini “Low Voltage Low power CMOS current conveyors”

CHAPTER 6

WIDE BAND CMOS CURRENT CONVEYOR

In this chapter a new wide band CMOS CCII detailed[3] . Its voltage follower section is based on a cascade of two voltage followers. The first one is the flipped voltage follower; Unfortunately, this voltage follower while standing alone suffers from a large voltage offset. By cascading another voltage follower to this one, this voltage offset is cancelled. Another advantage of the wide band CCII is that the voltage following is independent of the mismatches between the transistors. This is not the case in the differential pair based CCII realizations which are affected by any mis-matches in the differential pair transistors. The current following stage of the wide band CCII is made up of class-A branches and resembles that of Surakampontorn CCII .One more advantage of the wide band CCII is that it achieves wider voltage and current transfer bandwidths [4]while keeping all other parameters as accurate as Surakampontorn CCII.

6.1 Wide Band CCII:

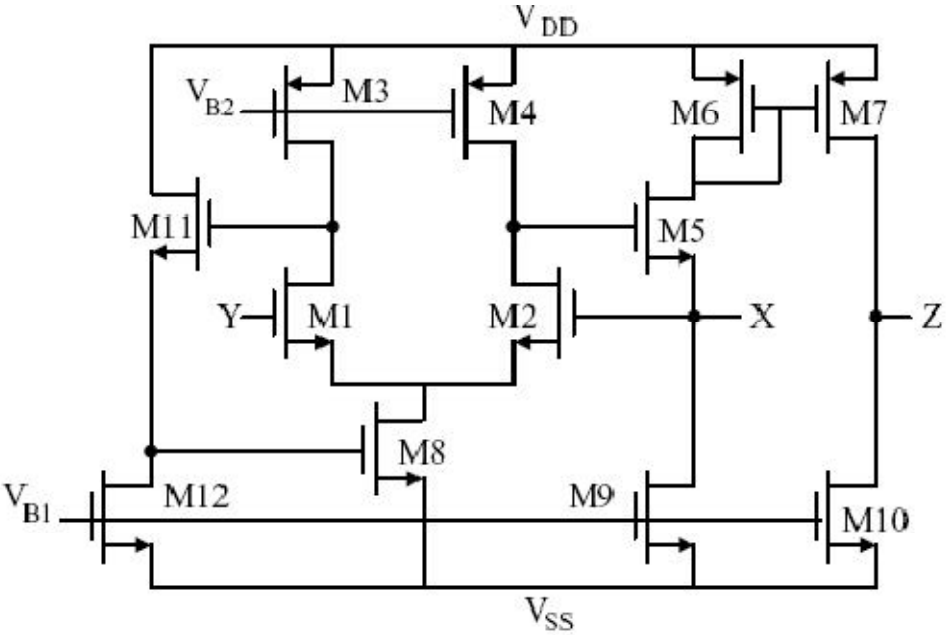

Fig.6-1 : The wide band CCII. [3]

6.1.1 Sub Circuit Description:

The CMOS realization of the wide band CCII is shown in above Fig.

- The groups of the transistors (M1 and M2), (M3 and M4), (M6 and M7) as well as (M9 andM10) are matched.

Assuming that all the transistors operate in their saturation regions, the operation of the circuit can be explained as follows:

- **Current source:**

  M3, M4, M9, M10 and M12 serve as DC current sources holding equal currents of I_B.

- **Differential pair:**

  The circuit utilizes a differential pair (M1 andM2) to transfer V_Y to V_X . The voltage transfer occurs because the source terminals of M1 andM2 are at the same potential and they are biased by equal currents I_B.

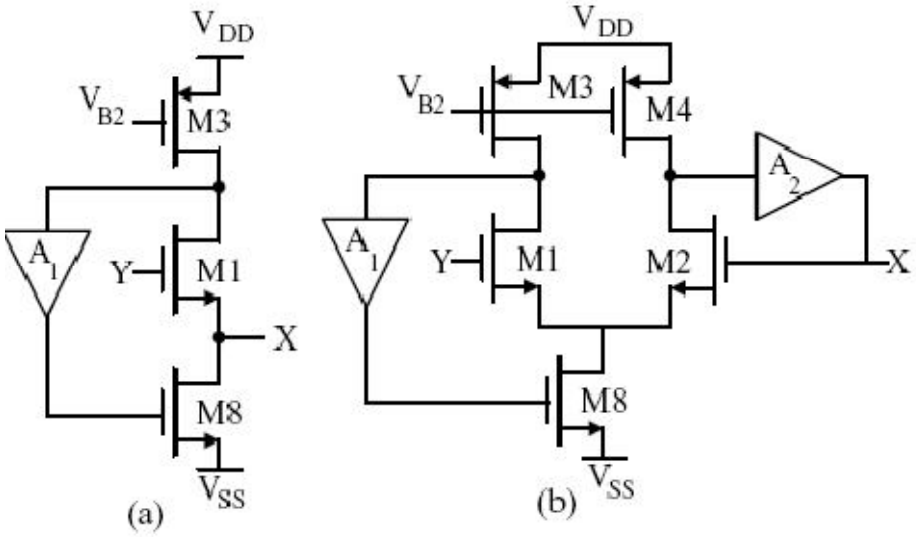

Fig.6-2 (a) The flipped voltage follower. (b) The modified voltage follower.

The idea can be explained as follows. Figure (a) shows the flipped voltage follower.

The circuit exhibits low input resistance at node *X*. However, there is a large voltage offset[5] between the *Y* and *X* terminals that slightly exceeds one threshold voltage. This large offset can be compensated by adding another voltage follower in cascade as shown in Fig.(b).
A class-A CCII based on the voltage buffer shown in Fig.(b) is presented in wide band CCII.

- The gain *A*1 is taken unity and is implemented by the source follower transistor M11.
- Similarly, the gain *A*2 is taken unity and is implemented by the source follower transistor M5.

A current mirror comprising M6 and M7 is added to convey the *X* terminal current to the *Z* terminal.

It can be seen that the voltage transfer gain is very close to unity and independent of the mismatches between M1 and M2[2]. However, when equal currents are used to bias M3 and M4, the matching between M1 and M2 is necessary to cancel the DC voltage offset between the *Y* and the *X* terminals.

6.1.2 Typical parameters values for WIDE BAND CCII+ :

-Voltage gain(β_o) = 0.9938
-current gain(α_o) = 1.0037
-3 db frequency(for voltage output) = 1150 Mhz
-X port impedance = 5.9Ω
-Output Offset V = -5.8mv to 2.54mv
- Output Offset I = -1.04μa to 0.023 μa
-Input voltage range = -0.63 to 0.25 V
-Input current range = -100 μa to 100 μa

6.2 SIMULATION RESULT FOR WIDE BAND CCII+ :

Simulation results for CCII+ are obtained at 1.5V supply and 0.50 µm technology.

For ac analysis source voltage is 100mv and source current of 100 µa. is taken.

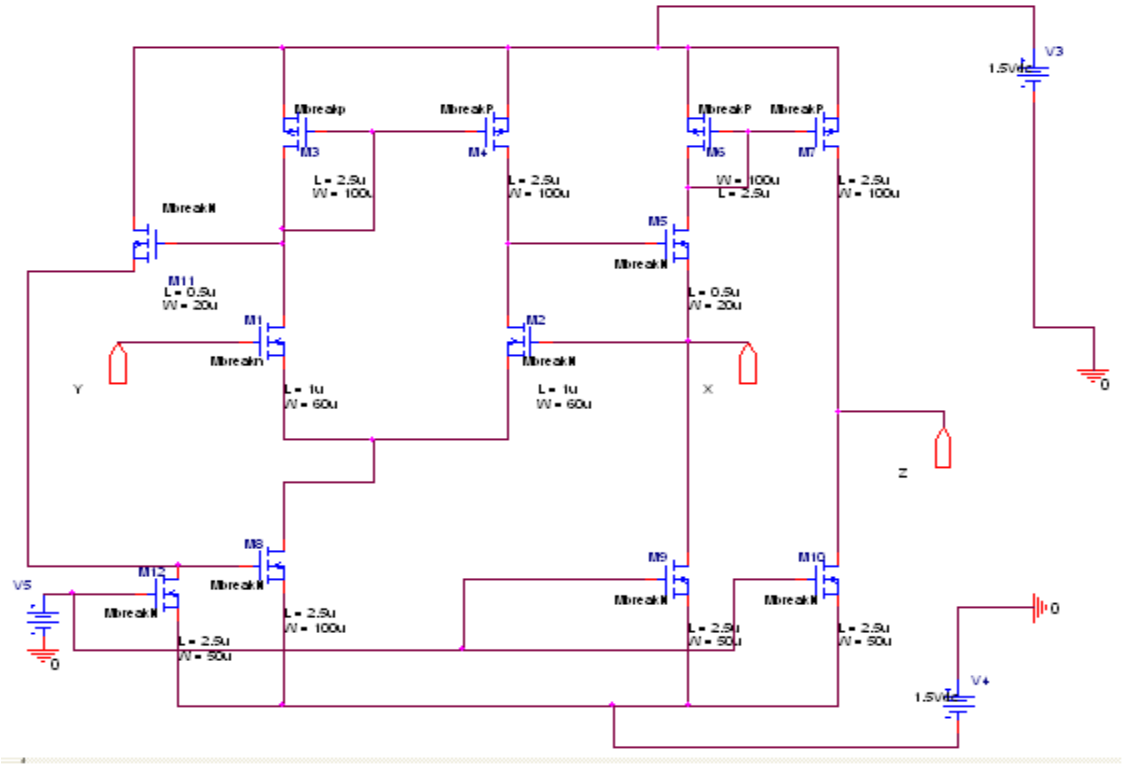

Fig 6-3: SCHEMATIC DIAGRAM OF WIDE BAND CCII+

Transistor aspect ratios:

Transistor	**W (μm)/L (μm)**
M1, M2	60/1
M3, M4	100/2.5
M5, M11	20/0.5
M6, M7	100/2.5
M8	100/2.5
M9, M10, M12	50/2.5

❖ **DC ANALYSIS:**

DC voltage characteristics:

For voltage transfer characteristics, a varying voltage source is applied at port Y and corresponding output is taken at port X. The input voltage is varied along X axis and from the figure below it can be seen that output follows the input for a range of -0.5v to 0.5v .

During this analysis, the port Z was at ground terminal.

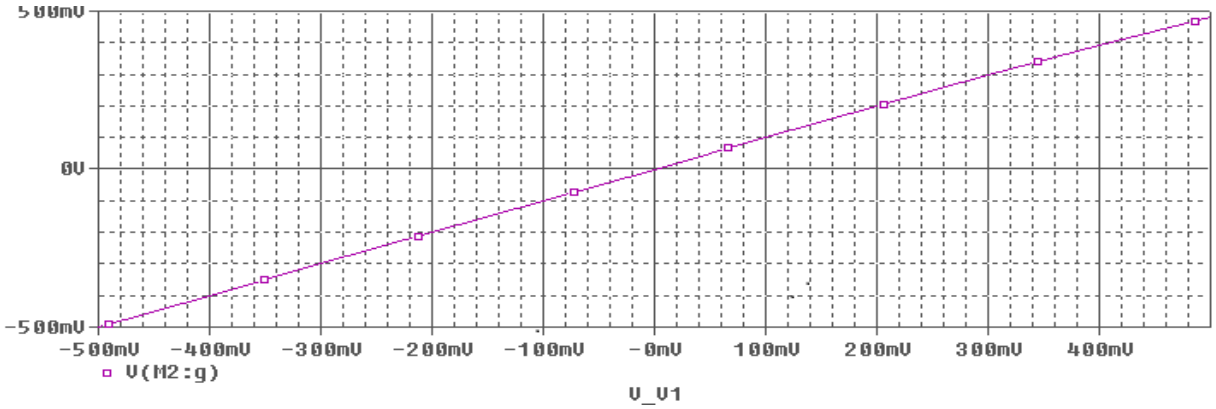

Fig 6-4(a): DC voltage transfer plot.

DC current characteristics:

For current transfer characteristics, a varying current source is applied at port X and corresponding output is taken at ports Z. The input current is varied from -20µA to +20µA and the desired output current characteristics are shown in figures below and during this analysis, the port Y was at ground terminal.

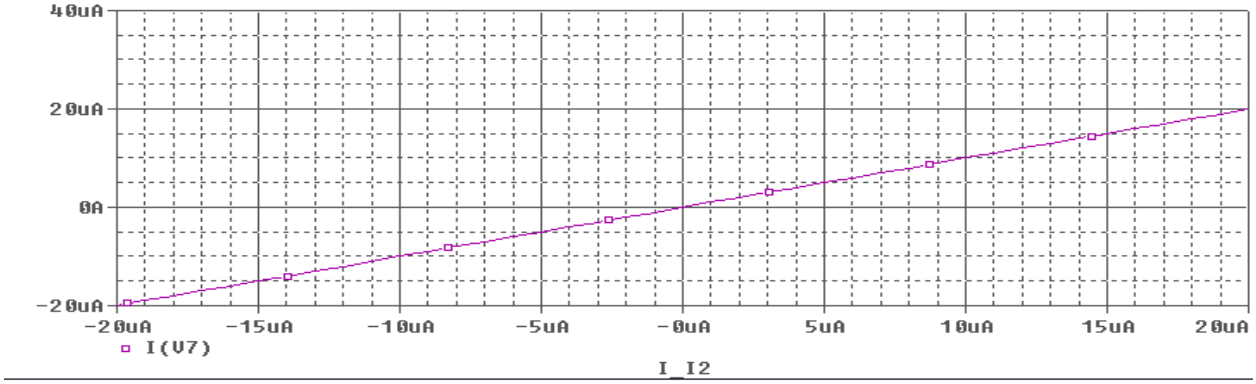

Fig 6-4(b) : DC current transfer plot.

❖ **AC ANALYSIS:**

AC voltage characteristics:

The frequency response of the voltage gain at port X is shown in figure below:

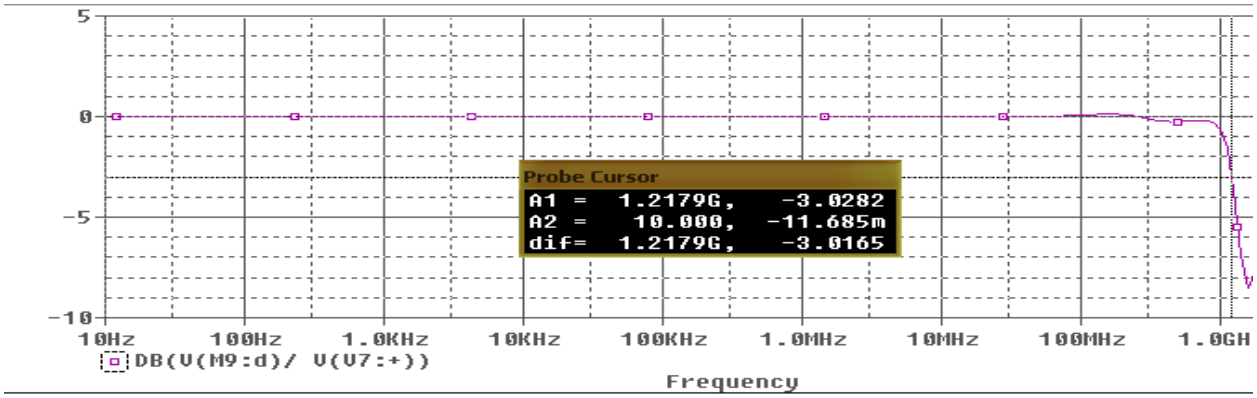

Fig 6-5(a): AC voltage plot at port X.

β (s) = V_x/ V_y : The voltage transfer function of the conveyor determined as a function of the frequency[1]. Its steady value comes out to be 0.9987

The 3 db frequency (ω_β) of above AC voltage curve at port X comes out to be 1217Mhz

AC current characteristics:

The frequency response of the current gain at port Z is shown in figure below:

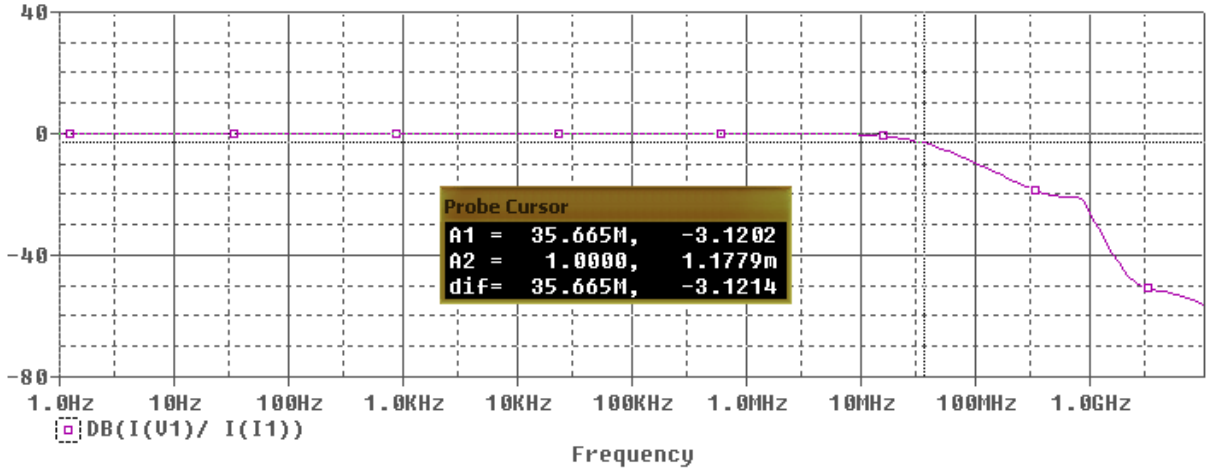

Fig 6-5(b): AC current plot at port Z.

α (s) = I_Z/ I_X : The current transfer function of the conveyor determined as a function of the frequency[1]. Its steady value comes out to be 1.0001

The 3 db frequency (ω_α) of above AC current plot at port Z comes out to be 35.66Mhz.

- **PARASITIC IMPEDANCES:**

- R_y and C_y : R_y is the value of the Y port impedance at low frequency.

  The value C_y is then deduced from the -3 DB cutoff frequency f_y of Z_y;

  $$C_Y = \frac{1}{2\pi} f_Y R_Y$$

  The R_y value comes out to be 1.8TΩ and the C_y value comes out to be 0.0058pf.

- $R_X = V_X / I_X$; value comes out to be 2.8Ω.

- R_z and C_z i.e. output port impedance of port Z .

  $$R_z = \frac{V_z}{I_X}$$

  R_z is the value of the impedance at low frequency.

  The value C_z is then deduced from the -3 DB cutoff frequency f_z ;

  $$C_Z = \frac{1}{2\pi} f_Z R_Z$$

  The R_z value comes out to be 18.5MΩ and the C_z value comes out to be .03412pf.

❖ **TRANSIENT ANALYSIS:**

By applying an AC voltage source having frequency 100 MHz at port Y its transient response is shown in figure below:

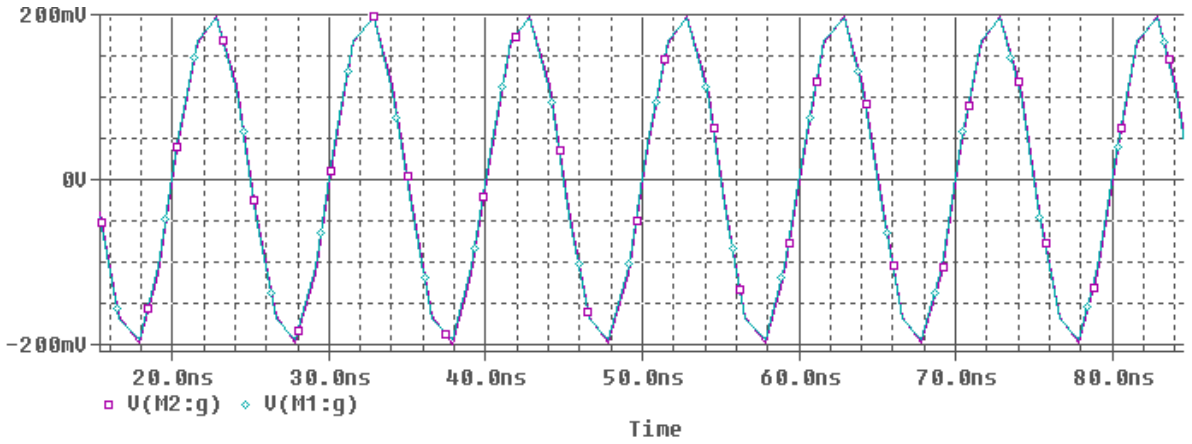

Fig 6-6: Output Voltage transient plot.

Thus the output offset voltage value comes out to be 2.2mv which is calculated by above transient plot.

Similarly, by applying current sinusoidal input, the output offset current value comes out to be 4µa which is calculated by current plot.

- **Power dissipation:** By observing output simulation file in PSPICE ; power dissipation of above circuit comes out to be 1.15×10^{-03}watt.

❖ 6.1 PARAMETERS TABLE FOR WIDE BAND CCII:

PARAMETER	VALUE
β_o	0.9987
α_o	1.0001
ω_β	1217Mhz
ω_α	35.66Mhz.
R_y	1.8TΩ
C_y	0.0058pf.
R_x	2.8Ω.
R_z	18.5MΩ
C_z	.03412pf
Offset V	2.2mv
Offset I	4μa
Power dissipation	1.15×10^{-03}watt

REFERENCES

[1] Alain Fabre. "On the frequency limitations of the circuits based on second generation current conveyors", Analog Integrated Circuits and Signal Processing, 03/1995

[2] Wanlop Surakampontorn and Khanittha Kaewdang“Development of Differential Amplifier Based the Second Generation Current Conveyors”

[3] WESSAM S. HASSANEIN, INAS A. AWAD AND AHMED M. SOLIMAN “New Wide Band Low Power CMOS Current Conveyors” Electronics and Communication Engineering Department, Cairo University, Egypt

[4] A.M. Ismail and A.M. Soliman, “Wideband CMOS current conveyor.” Electronics Letters, vol. 34, no. 25, pp. 2368–2369, 1998.

[5] Ahmed M. Soliman “Current-Mode Universal Filters Using Current Conveyors: Classification and Review”

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CHAPTER 7

FLIPPED VOLTAGE FOLLOWER BASED CCII

7.1 FLIPPED VOLTAGE FOLLOWER(FVF):

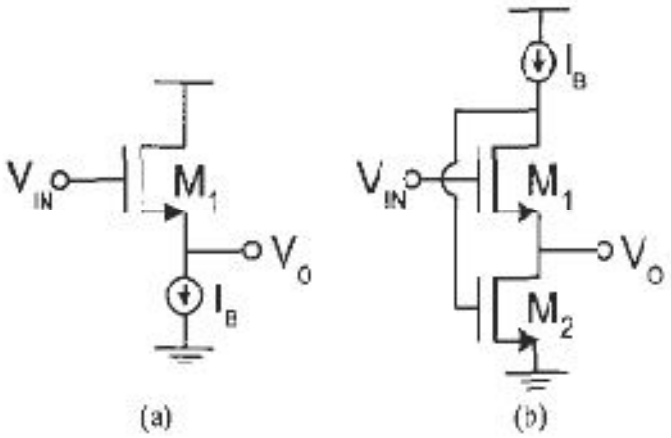

Fig7-1: (a)Common Drain Amplifier(b)Flipped Voltage Follower

The basic structure of NMOS FVF[2] (flipped voltage follower) is shown in fig above.

It is the modified version of classical voltage drain amplifier (also known as voltage follower) shown in fig(a). Feedback in the FVF allows to bias transistor *M,* from a node different than the output one, so that the drain current remains constant regardless of the output current, and therefore (neglecting second-order effects) its V_{GS} also becomes constant. So,large and small signal voltage gains are very close to I_B **,** even for resistive loads. This is in opposite to the voltage follower of Fig.(a), where drain current in M_1**,** depends on the output current and makes the voltage gain less than 1 and strongly dependent on the load resistance. Feedback in the FVF allows getting an output resistance very low[5]. It is approximately given by: where the small signal parameters g_m and r_o have their usual meanings. This resistance is typically in the range of tens of ohms, As on sequence, the FVF can sink huge currents.

The R_{out} is given by:

$$R_{OUT} = \frac{1}{G_M(M_1)G_M(M_2)R_O\ (M_2)}$$

7.2 LOW VOLTAGE CURRENT MIRRORS:

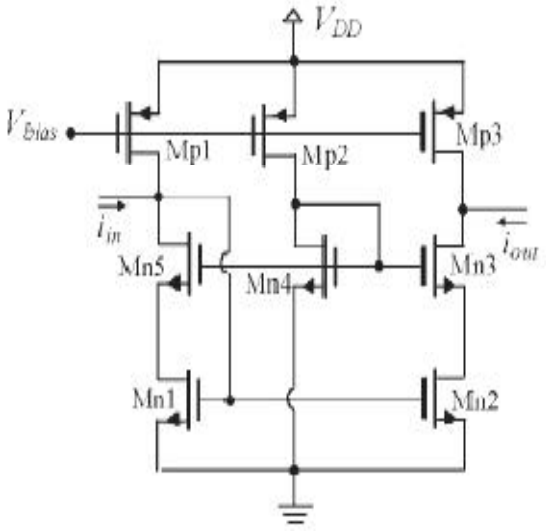

Fig 7-2 : FVF based current mirror

One of the most widely used current mirror topologies in low voltage signal processing is the conventional cascode current mirror[4] shown in fig with reference to the voltage restrictions the minimum supply voltage requirement is given by :

$$V_{DDMIN} = V_{TH}(M_{N1}) + V_{DSSAT}(M_{P1})$$

The minimum voltage across the wide-swing current source is one threshold voltage drop less than the regular cascode , while the output resistance is the same, that is, $g_m r_o^2$ Note that the body effect has been neglected in it[3].

7.3 CCII BASED ON FVF BASED CURRENT MIRROR:

One of the most widely used current mirror topologies in low voltage signal processing is the conventional cascode current mirror. The problem with the cascode mirror is higher voltage headroom[2]. That can be reduced by connecting gate of Mn1 to drain of Mn5 which reduces the headroom by Amount V_{TH} .The current mirror can be converted in to second generation current conveyor CCII by connecting Mn6 and Mn7 as current sink load.With reference to the voltage restrictions the minimum supply voltage requirement is given by[2]:

$$V_{DDMIN} = V_{TH}(M_{N1}) + V_{DSSAT}(M_{P1}) + V_{DS}(M_{N6})$$

Where $V_{TH}(Mn_1)$is the threshold voltage of the diode connected transistor Mn_1 and $VDS_{SAT}(Mp_1)$.

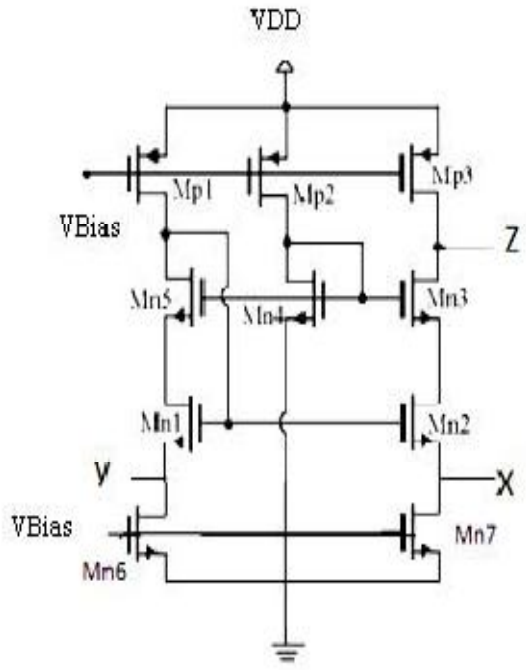

Fig 7-3: Flipped voltage current mirror based CCII.

W/L RATIO OF TRANSISTORS:

Transistor	**W/L**
Mp1-Mp3	200/1
Mn1- Mn5	400/1
Mn6-Mn7	300/3

7.3.1 Typical parameters values for Flipped Voltage Follower based CCII+ :

-Voltage gain(β_o) = 1.8

-current gain(α_o) = 1.1

-X port impedance = 14kΩ

-Z port impedance = 15kΩ

-Output Offset V = 350mv

-Power dissipation = 1.05×10^{-04}watt

-THD = 11%@100Mhz

7.4 SIMULATION RESULT FOR FLIPPED VOLTAGE FOLLOWER BASED CCII+ :

Simulation results for CCII+ are obtained at 1.5V supply and 0.50 µm technology.

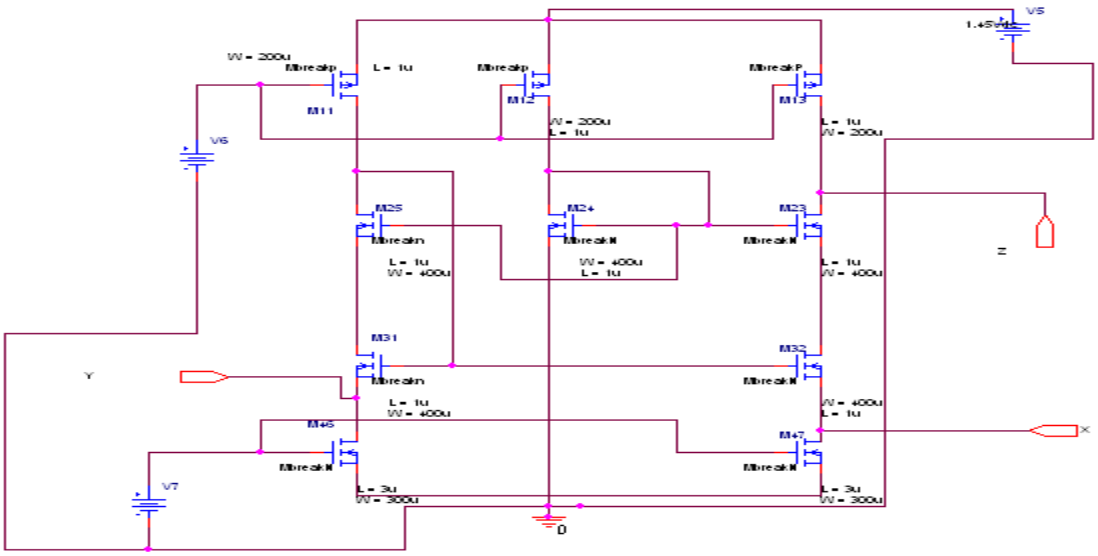

Fig 7-4 : Schematic Diagram of FVF based CCII+

❖ **DC ANALYSIS:**

DC voltage characteristics:

For voltage transfer characteristics, a varying voltage source is applied at port Y and corresponding output is taken at port X. The input voltage is varied along X axis and from the figure below it can be seen that output follows the input for a range of -0.5v to 0.5v . During this analysis, the port Z was at ground terminal.

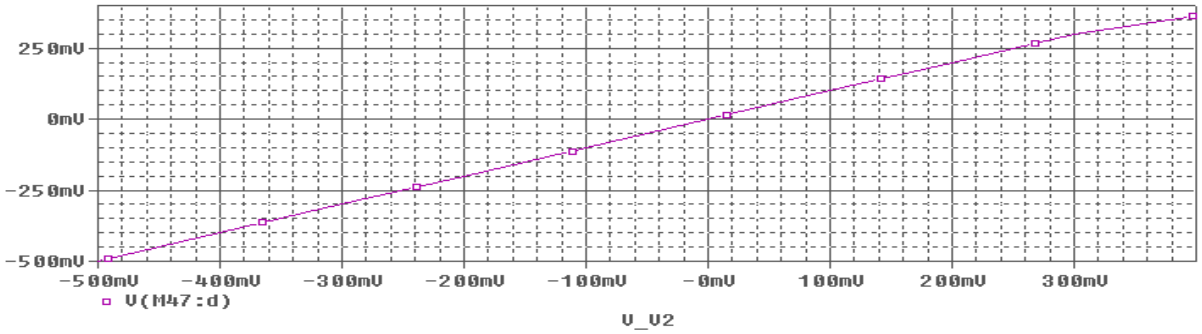

Fig 7-5(a): DC voltage transfer plot.

DC current characteristics:

For current transfer characteristics, a varying current source is applied at port X and corresponding output is taken at ports Z. The input current is varied from -50µA to +50µA and the desired output current characteristics are shown in figures below and during this analysis, the port Y was at ground terminal.

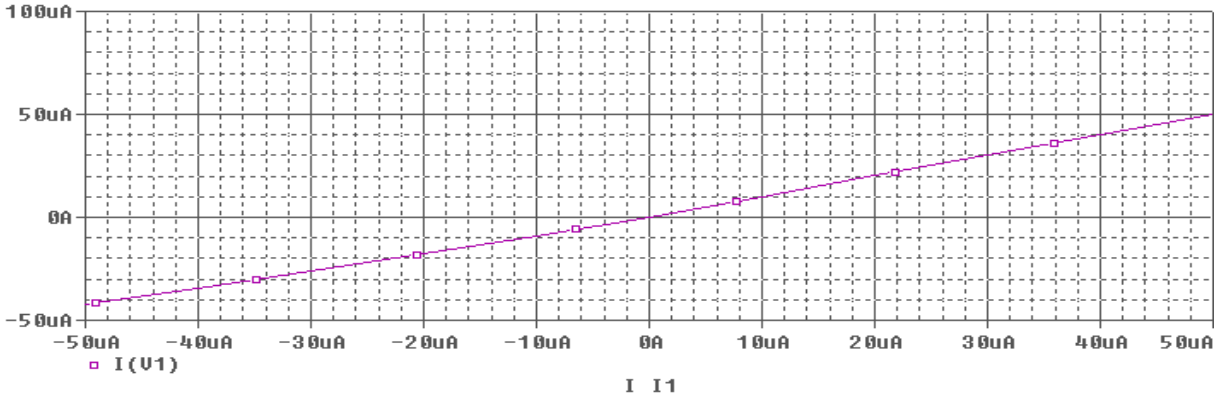

Fig 7-5(b): DC current transfer plot.

❖ **AC ANALYSIS:**

AC voltage characteristics:

The frequency response of the voltage gain at port X is shown in figure below:

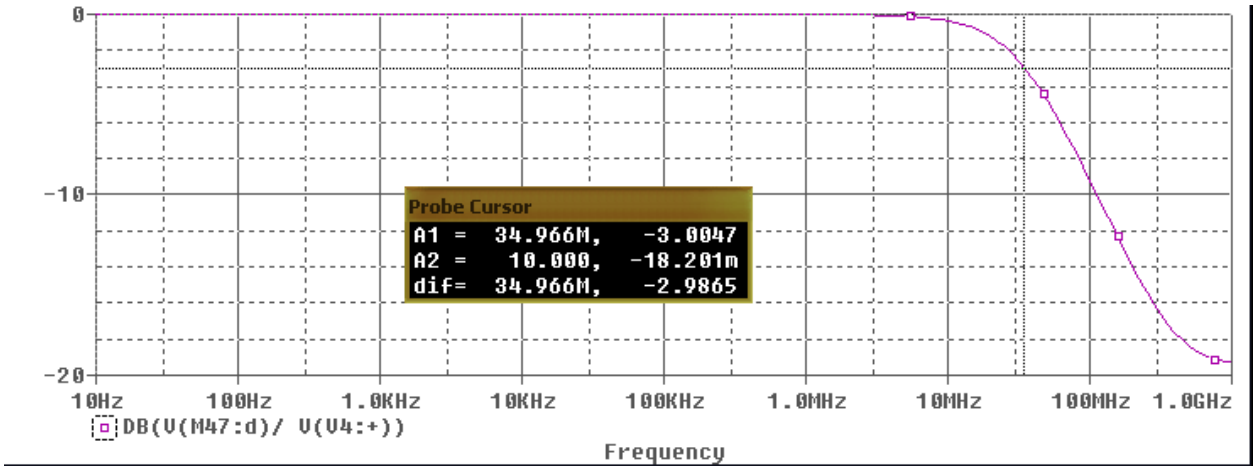

Fig 7-6(a): AC voltage plot at port X.

β (s) = V_x/ V_y : The voltage transfer function of the conveyor determined as a function of the frequency[1]. Its steady value comes out to be 0.9981

The 3 db frequency (ω_β) of above AC voltage curve at port X comes out to be 34.96Mhz

AC current characteristics:

The frequency response of the current gain at port Z is shown in figure below:

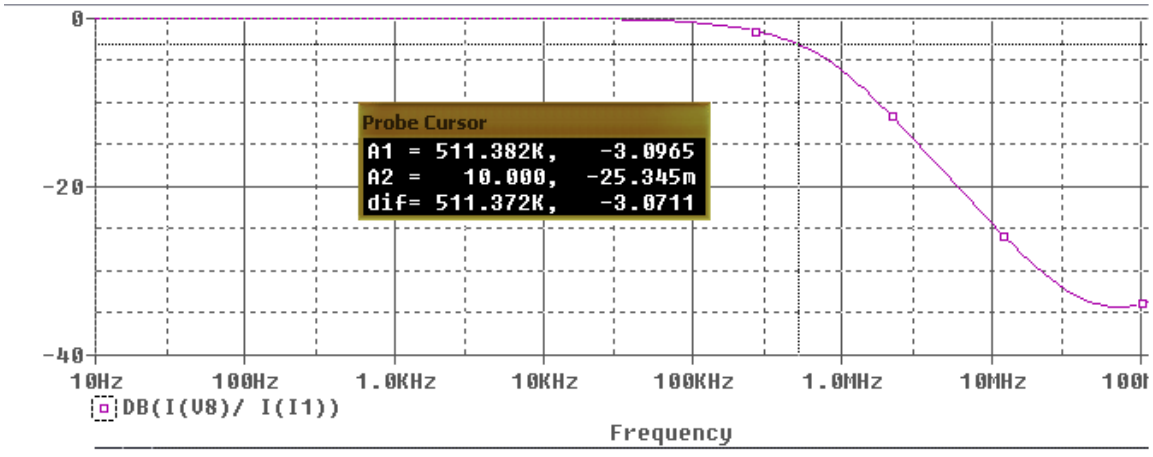

Fig 7-6(b) : AC current plot at port Z.

α (s) = I_Z/ I_X : The current transfer function of the conveyor determined as a function of the frequency[1]. Its steady value comes out to be 1.02

The 3 db frequency (ω_α) of above AC current plot at port Z comes out to be 511.38Khz.

❖ **PARASITIC IMPEDANCES:**

- R_y and C_y : R_y is the value of the Y port impedance at low frequency.

  The value C_y is then deduced from the -3 DB cutoff frequency f_y of Z_y;

  $$C_Y = \frac{1}{2\pi} f_Y R_Y$$

  The R_y value comes out to be 5.93MΩ. and the C_y value comes out to be 0.741 pf.
- $R_X = V_X / I_X$, value comes out to be 22.5KΩ.
- R_z and C_z i.e. output port impedance of port Z .

  $$R_z = \frac{V_z}{I_X}$$

  R_z is the value of the impedance at low frequency.

  The value C_z is then deduced from the -3 DB cutoff frequency f_z ;

  $$C_Z = \frac{1}{2\pi} f_Z R_Z.$$

  The R_z value comes out to be 54KΩ and the C_z value comes out to be 8.823pf.

❖ **TRANSIENT ANALYSIS:**

By applying an AC voltage source having frequency 100 MHz at port Y its transient response is shown in figure below:

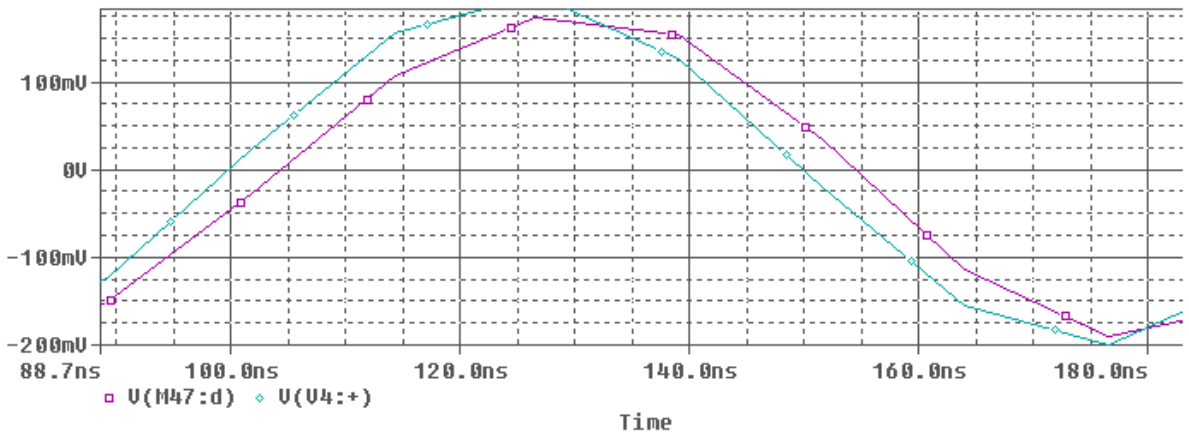

Fig 7-7: Output Voltage transient plot.

Thus the output offset voltage value comes out to be 50mv which is calculated by above transient plot.

- **Power dissipation:** By observing output simulation file in PSPICE ; power dissipation of above circuit comes out to be 1.16×10^{-07}watt.

❖ 7.1 PARAMETERS TABLE FOR FVF BASED CCII:

PARAMETER	VALUE
β_o	0.9981
α_o	1.02
ω_β	34.966Mhz
ω_α	511.38Khz
R_y	5.93MΩ
C_y	0.741pf.
R_x	22.5KΩ.
R_z	54KΩ
C_z	8.823pf
Offset V	50mv
Power dissipation	1.16×10^{-07}watt

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CHAPTER 8

FILTER DESIGNING USING CCII TOPOLOGIES

8.1 FILTER THEORY

8.1.1 Low-pass filter

A low-pass filter is a filter that passes low-frequency signals and attenuates signals with frequencies higher than the cutoff frequency. The actual amount of attenuation for each frequency varies depending on specific filter design. It is sometimes called a high-cut filter in audio applications. A low-pass filter is the opposite of a high-pass filter. A band-pass filter is a combination of a low-pass and a high-pass.

Low-pass filters exist in many different forms, including electronic circuits, anti-aliasing filters for conditioning signals prior to analog-to-digital conversion, digital filters for smoothing sets of data, acoustic barriers, blurring of images, and so on. The moving average operation used in fields such as finance is a particular kind of low-pass filter, and can be analyzed with the same signal processing techniques as are used for other low-pass filters. Low-pass filters provide a smoother form of a signal, removing the short-term fluctuations, and leaving the longer-term trend.

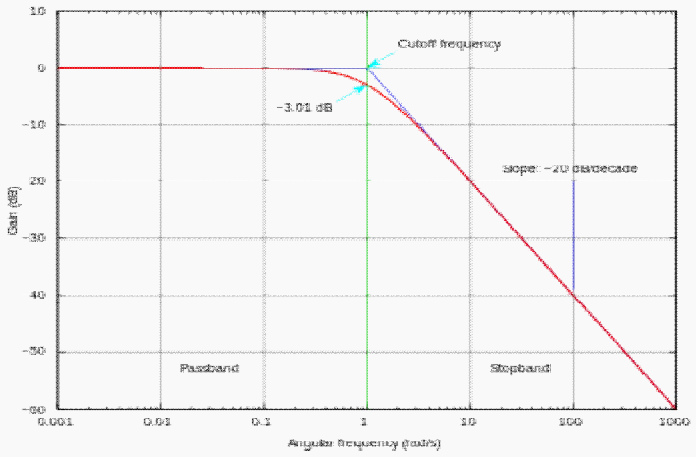

FIG 8-1:The gain-magnitude frequency response of a first-order (one-pole) low-pass filter[6]

Power gain is shown in decibels (i.e., a 3 dB decline reflects an additional half-power attenuation).Angular frequency is shown on a logarithmic scale in units of radians per second.

There are many different types of filter circuits, with different responses to changing frequency. The frequency response of a filter is generally represented using a Bode plot, and the filter is characterized by its cutoff frequency and rate of frequency roll off. In all cases, at the cutoff frequency, the filter attenuates the input power by half or 3 dB. So the order of the filter determines the amount of additional attenuation for frequencies higher than the cutoff frequency.A second-order filter attenuates higher frequencies more steeply. The Bode plot for this type of filter resembles that of a first-order filter, except that it falls off more quickly. For example, a second-order Butterworth filter reduces the signal amplitude to one fourth its original level every time the frequency doubles. Third- and higher-order filters are defined similarly. In general, the final rate of power rolloff for an order-n all-pole filter is $6n$ dB per octave (i.e., $20n$ dB per decade) [4].

8.1.2 High-pass filter

A high-pass filter (HPF) is an electronic filter that passes high-frequency signals but attenuates signals with frequencies lower than the cutoff frequency. The actual amount of attenuation for each frequency varies from filter to filter. A high-pass filter is usually modeled as a linear time-invariant system. It is sometimes called a low-cut filter or bass-cut filter. High-pass filters have many uses, such as blocking DC from circuitry sensitive to non-zero average voltages or RF devices. They can also be used in conjunction with a low-pass filter to make a bandpass filter.

8.1.3 Band-pass filter

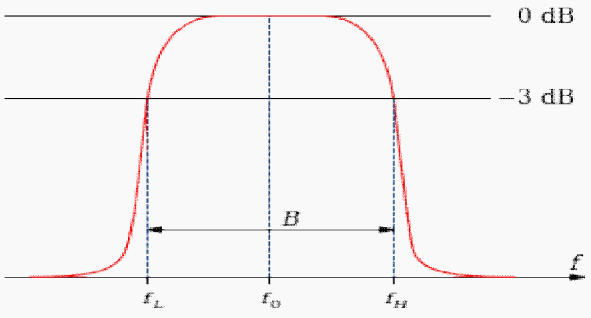

FIG 8-2: Magnitude transfer function versus frequency for a band-pass filter.

A band-pass filter is a device that passes frequencies within a certain range and rejects frequencies outside that range.An example of an analogue electronic band-pass filter is an RLC circuit (a resistor–inductor–capacitor circuit). These filters can also be created by combining a low-pass filter with a high-pass filter.

An ideal bandpass filter would have a completely flat passband and would completely attenuate all frequencies outside the passband. Additionally, the transition out of the passband would be instantaneous in frequency. In practice, no bandpass filter is ideal. The filter does not attenuate all frequencies outside the desired frequency range completely; in particular, there is a region just outside the intended passband where frequencies are attenuated, but not rejected. This is known as the filter roll-off, and it is usually expressed in dB of attenuation per octave or decade of frequency[1]. Generally, the design of a filter seeks to make the roll-off as narrow as possible, thus allowing the filter to perform as close as possible to its intended design. Often, this is achieved at the expense of pass-band or stop-band ripple.

The bandwidth of the filter is simply the difference between the upper and lower cutoff frequencies. The shape factor is the ratio of bandwidths measured using two different attenuation values to determine the cutoff frequency, e.g., a shape factor of 2:1 at 30/3 dB means the bandwidth measured between frequencies at 30 dB attenuation is twice that measured between frequencies at 3 dB attenuation.

A band-pass filter can be characterised by its Q-factor. The Q-factor is the inverse of the fractional bandwidth. A high-Q filter will have a narrow passband and a low-Q filter will have a wide passband. These are respectively referred to as narrow-band and wide-band filters.

8.1.4 All-pass filter

An all-pass filter is a signal processing filter that passes all frequencies equally in gain, but changes the phase relationship between various frequencies. It does this by varying its phase shift as a function of frequency. Generally, the filter is described by the frequency at which the phase shift crosses 90° (i.e., when the input and output signals go into quadrature – when there is a quarter wavelength of delay between them).

They are generally used to compensate for other undesired phase shifts that arise in the system, or for mixing with an unshifted version of the original to implement a notch comb filter.

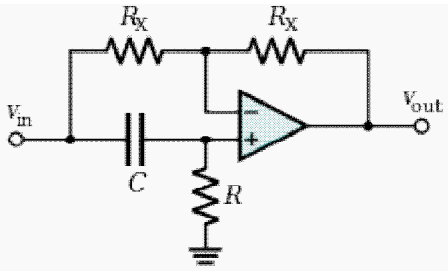

Figure 8-3: Schematic of an Op Amp all-pass filter[6]

The operational amplifier circuit shown in Figure 1 implements an active all-pass filter with the transfer function

$$H(s) = \frac{(sRC - 1)}{(sRC + 1)}$$

8.2 LOW PASS FILTER DESIGN USING CCII+ TOPOLOGIES

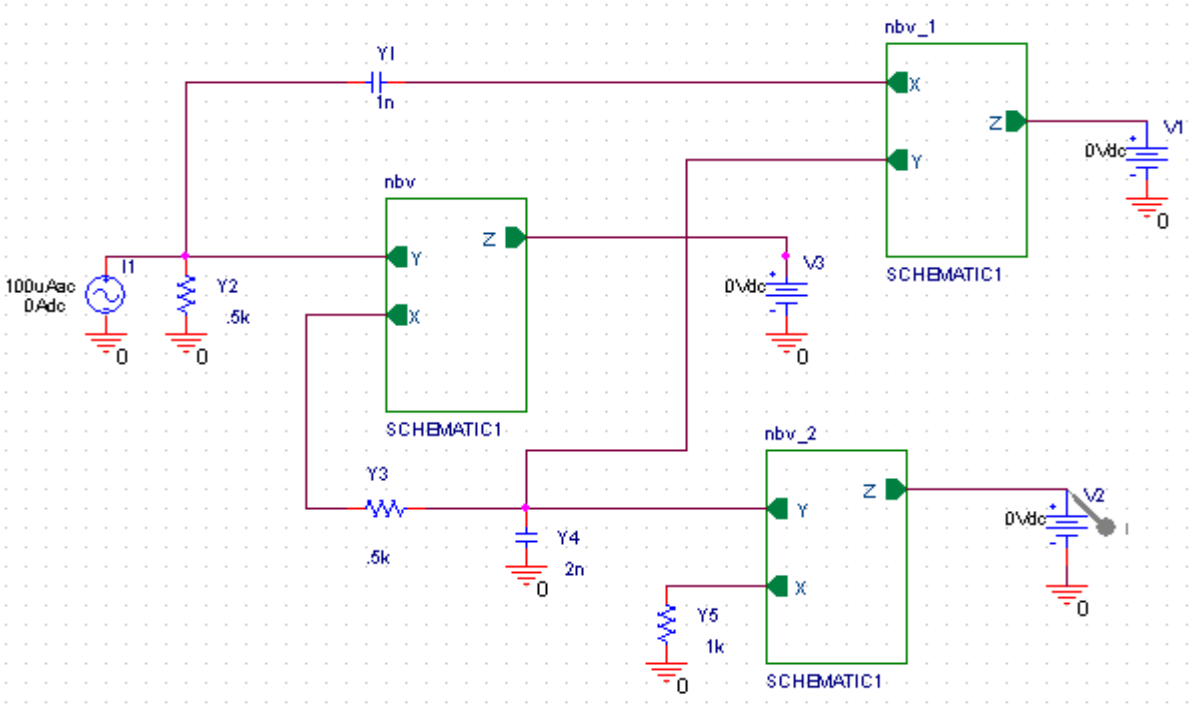

FIG 8-4: LOW PASS FILTER CIRCUIT USING CCII[3]

The circuit in this section is shown in Fig. above employs two capacitors plus three resistors circuit, which is better than the circuit which employs three capacitors plus two resistors.

Although this circuit uses three resistors plus two capacitors it still suffers from having no independent control on the filter Q.

Transfer function for above LPF is:

$$\frac{I(v_2)}{I(I_1)} = \frac{G_3 G_5}{S^2 C_1 C_4 + S C_4 G_2 + G_2 G_3}$$

Thus, $$\omega_0 = \sqrt{\frac{G_3 G_2}{C_1 C_4}}$$

$$Dc\ Gain(K).\ {\omega_0}^2 = \frac{G_3 G_5}{C_1 C_4}$$

8.3 SIMULATION RESULTS:

For an ac source of 100ua ; the simulation results are:

DIFFERENTIAL AMPLIFIER BASED CCII

For C_1=1n; C_4=2n; R_3=0.5k R_2=0.5k and R_5=1k

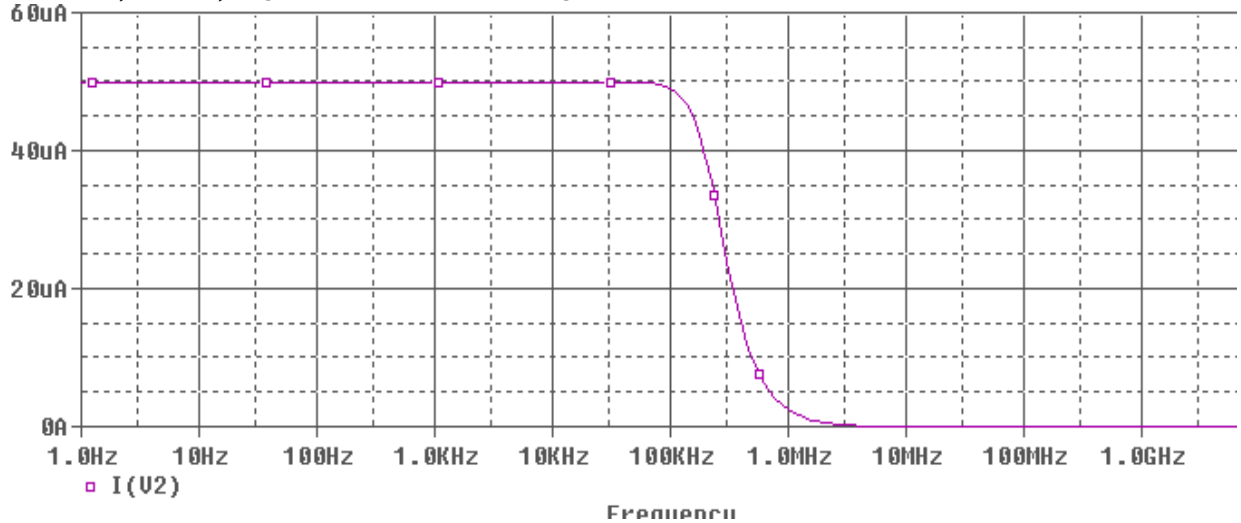

FIG 8-5: LOW PASS FILTER OUTPUT FOR DIFFERNTIAL AMPLIFIER BASED CCII

RESULT TABLE:

PARAMETER	PSPICE PLOT VALUE	THEORATICAL VALUE
3 db cutoff	225.546 khz	225.079 khz
Dc Gain(k)	0.49965	0.5
Power dissipation	9.16×10^{-04}watt	
THD	7.526%	
MOS used	10	

WIDE BAND CCII

For C_1=1n; C_4=2n; R_3=0.5k R_2=0.5k and R_5=1k

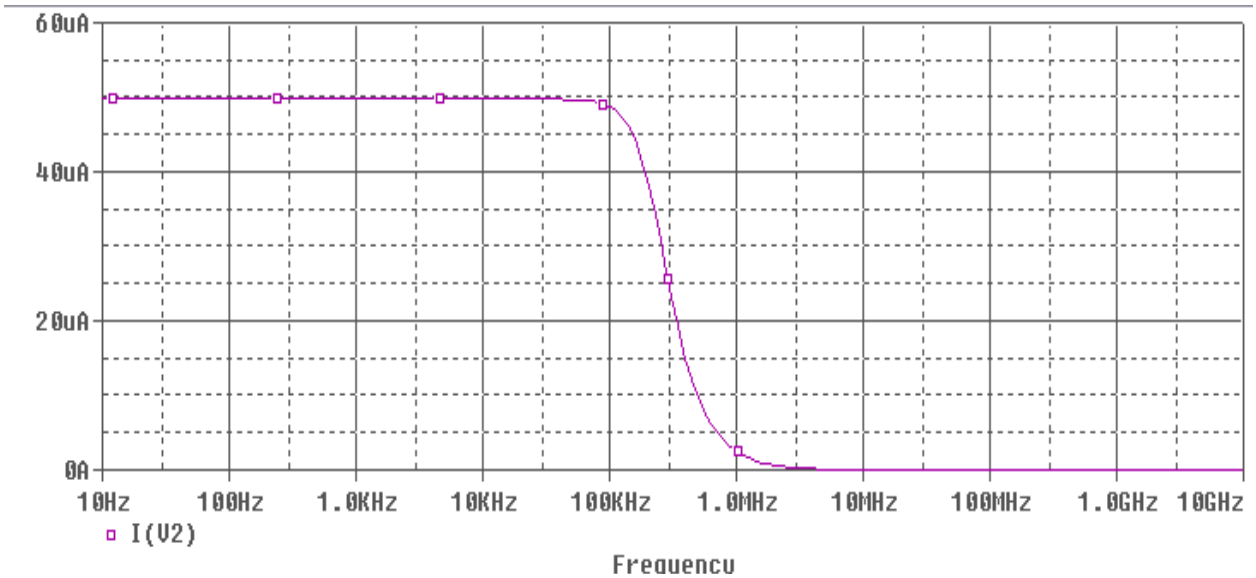

FIG 8-6: LOW PASS FILTER OUTPUT FOR WIDE BAND CCII

RESULT TABLE:

PARAMETER	PSPICE PLOT VALUE	THEORATICAL VALUE
3 db cutoff	223.102 khz	225.079 khz
Dc Gain(k)	0.4976	0.5
Power dissipation	3.72×10^{-03}watt	
THD	5.491%	
MOS used	12	

TRANSLINEAR LOOP BASED CCII

For C_1=0.1n; C_4=0.05n; R_3=10k R_2=10k and R_5=1k[5]

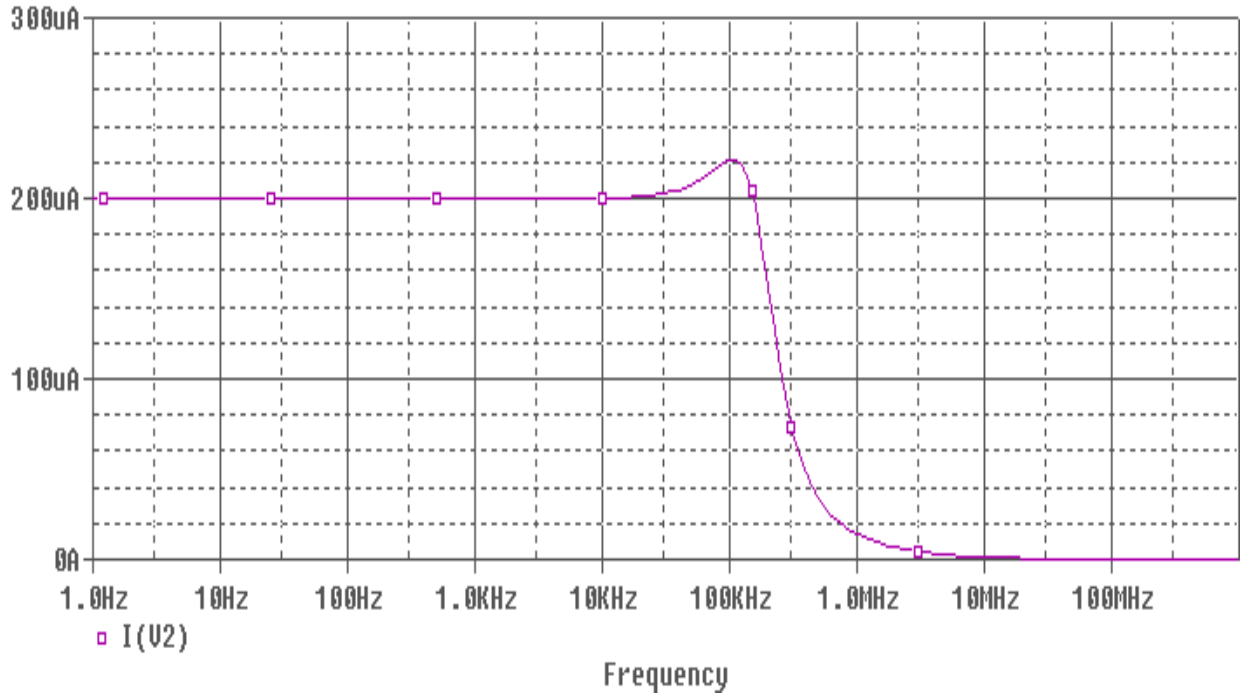

FIG 8-7: LOW PASS FILTER OUTPUT FOR TRANSLINEAR CCII

RESULT TABLE:

PARAMETER	PSPICE PLOT VALUE	THEORATICAL VALUE
3 db cutoff	219.477 khz	225.079 khz
Dc Gain(k)	1.9966	2
Power dissipation	2.61×10^{-03}watt	
THD	0.956%	
MOS used	8	

FLIPPED VOLTAGE FOLLOWER BASED CCII

For C_1=1.414n; C_2=1.414n; R_1=0.5k R_2=0.5k

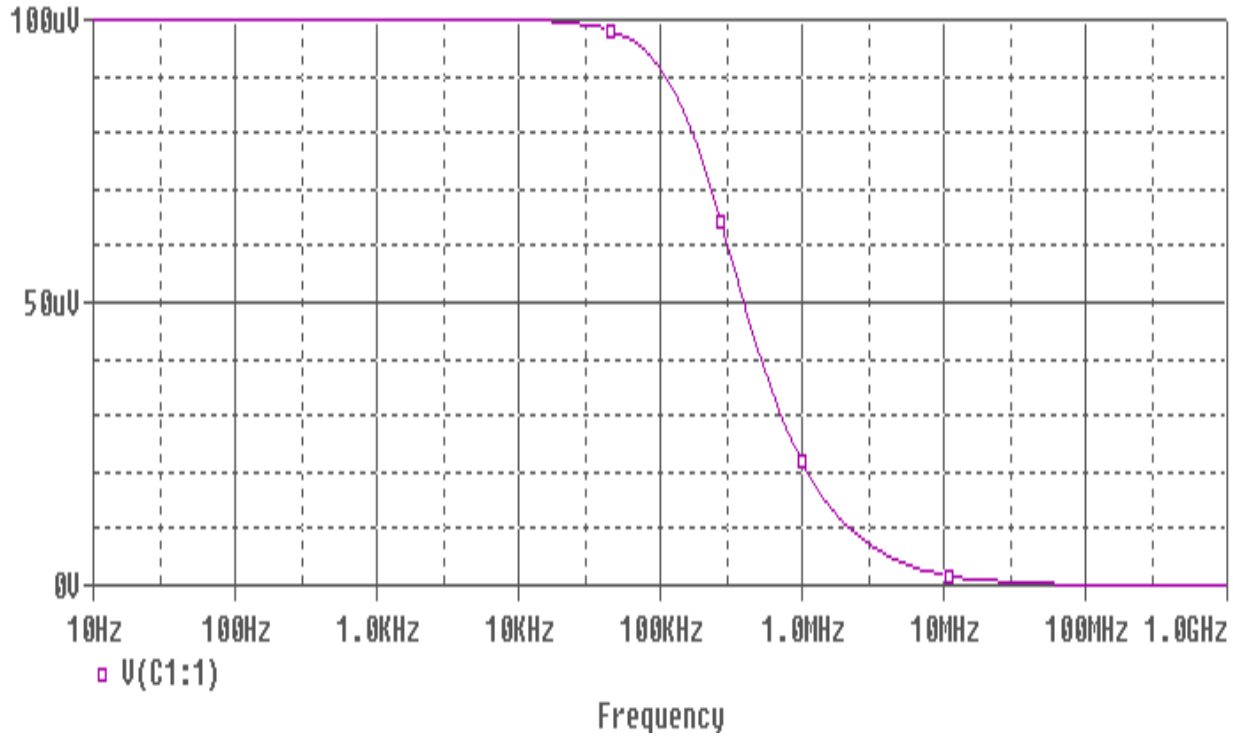

FIG 8-8: LOW PASS FILTER OUTPUT FOR FLIPPED VOLTAGE CCII

RESULT TABLE:

PARAMETER	PSPICE PLOT VALUE	THEORATICAL VALUE
3 db cutoff	223.567 khz	225.079 khz
Dc Gain(k)	0.9994	1
Power dissipation	1.77×10^{-06}watt	
THD	6.2265%	
MOS used	10	

8.4 COMPARISON TABLE FOR FILTER OUTPUT:

PARAMETER	DIFFERNTIAL PAIR BASED CCII	WIDE BAND CCII	TRANSLINEAR LOOP BASED CCII	FLIPPED VOLTAGE CCII
3 db cutoff	225.546 khz	223.102 khz	219.477 khz	223.567 khz
Dc Gain(k)	0.49965(0.5)	0.4976(0.5)	1.9966(2)	0.9994(1)
Power dissipation	9.16×10^{-04}watt	3.72×10^{-03}watt	2.61×10^{-03}watt	1.77×10^{06}watt
THD	7.526%	5.491%	0.956%	6.2265%
MOS used	10	12	8	10

8.5 COMPARISON TABLE FOR PARAMETERS OF VARIOUS TOPOLOGIES:

PARAMETER	DIFFERNTIAL PAIR CCII	WIDE BAND CCII	FLIPPED VOLTAGE CCII	TRANSLINEAR CCII
β_o	0.999	0.9987	0.9981	0.991
α_o	1.0001	1.0001	1.02	1.015
ω_β	787.62Mhz	1217Mhz	34.966Mhz	Very large
ω_α	32.17Mhz.	35.66Mhz.	511.38Khz	221.37Mhz.
R_y	1.8TΩ	1.8TΩ	5.93MΩ	3.74TΩ
C_y	0.0058pf.	0.0058pf.	0.741pf.	0.028pf.
R_x	0.5Ω.	2.8Ω.	22.5KΩ.	4.03 KΩ.
R_z	14.01MΩ	18.5MΩ	54KΩ	3.956MΩ
C_z	.0341pf	.03412pf	8.823pf	.0021pf
Offset V	2.5mv	2.2mv	50mv	1.1mv
Powerdissipation	3.05×10^{-04}watt	1.15×10^{-03}watt	1.16×10^{-07}watt	7.53×10^{-04}watt
MOS used	10	12	10	8

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9. CONCLUSION AND FUTURE PROSPECTIVE

The current conveyor used as a basic building block in a variety of electronic circuit in instrumentation and communication systems. Some important topologies used for second generation current conveyor have been studied. Each topology has been studied from very basic of its construction and simulated also. The four prominent topologies of second generation current conveyors have been studied in detail. All of these topologies of the current conveyer have been simulated using Spice (0.5 µm technology). AC, DC and transient analysis of each topology is done and their various parameters are studied in order to have a faithful design. Low pass Filter is also designed using these topologies and it has been found that for better cut off frequency stability differential pair based CCII; for higher bandwidth operation modified differential pair i.e. wide band CCII; for using lower number of transistor & low distortion translinear CCII and for having lower power dissipation & better gain flipped voltage based CCII should be preferred. Certainly by doing more study of above topologies such as by involving compensating techniques etc. and by involving remaining topologies of current conveyors more robust view can be generated which will surely help in designing all type of high order circuits using current conveyors. Today these systems are replacing the conventional Op-amp in so many applications such as active filters, analog signal processing, and converters. Spice simulation of the current conveyor blocks and their applications verifies its suitability as a building block in VLSI circuits.