TCAD ANALYSIS OF HOT CARRIER RELIABILITY AND THERMAL BEHAVIOUR OF TRANSPARENT GATE RECESSED CHANNEL MOSFET

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by

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CERTIFICATE

This is certified that the thesis titled "TCAD ANALYSIS OF HOT CARRIER RELIABILITY AND THERMAL BEHAVIOUR OF TRANSPARENT GATE RECESSED CHANNEL MOSFET" is being submitted by me (Ajay Kumar–2K12/NST/01) towards partial fulfilment for the award of Master of Technology degree in Nanoscience & Technology in Delhi Technological University. This work is original and has not been submitted in part or fully to any other University or institute for the award of any degree or diploma.

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ABSTRACT

TCAD ANALYSIS OF HOT CARRIER RELIABILITY AND THERMAL BEHAVIOUR OF TRANSPARENT GATE RECESSED CHANNEL MOSFET

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In this thesis, a novel device structure called Transparent Gate Recessed Channel MOSFET (TGRC-MOSFET) is proposed to alleviate the hot carrier effects for the advanced nanometer process. TGRC-MOSFET involving a recessed channel and incorporates Indium Tin Oxide as a transparent gate. TCAD analysis shows that performance of TGRC-MOSFET surpasses Conventional Recessed Channel (CRC)-MOSFET in terms of high I_{ON}/I_{OFF} ratio and better carrier transport efficiency in compare to Conventional Recessed Channel (CRC) MOSFET. This simulation divulges the reduction in hot-carrier-effects metrics like electron velocity, electron temperature, potential, and electron mobility. All the simulations have been done using DEVEDIT-3D and ATLAS device simulator. The work proposes the novel design for reduction in hot carrier and low power switching application.

In thermal analysis of a novel design Transparent Gate Recessed Channel MOSFET (TGRC-MOSFET) at 300K. TGRC- MOSFET involves a recessed channel and incorporates Indium Tin Oxide as a transparent gate. Simulation results show that performance of TGRC-MOSFET surpasses Conventional Recessed Channel (CRC)-MOSFET in terms of heat capacity, heat conductivity, lattice temperature and total heat power in comparison to CRC-MOSFET. All the simulations have been done using DEVEDIT-3D AND ATLAS device simulator. Indium tin oxide (ITO or tin-doped indium oxide) is a solid solution of indium oxide (In_2O_3) and tin oxide (SnO_2). It is transparent and colourless in thin layers. Because of its two key properties, i.e. electrical conductivity and optical transparency, indium tin oxide is used as one of the most widely used transparent conducting oxides. Also, the In_2O_3 phase itself contributes free electron for electrical conductivity. Furthermore, with the reduction in transistor size, intrinsic self-heating effects have become unfavourable in low power applications. As the issue of heat becomes increasingly important in sub-micron MOSFETs, it becomes increasingly more important to accurately measure and model its thermal parameters to fully characterize its thermal performance.

High heat capacity of TGRC-MOSFET device is favourable for high power applications as compared to CRC MOSFET. Furthermore, low thermal conductivity of a device, finding application as heat insulation. TGRC-MOSFET has lower thermal conductivity as shown in fig. 3. In addition, there is reduction in hot electron (HE) injection gate current and impact ionization (II) substrate current in TGRC-MOSFET compared to CRC MOSFET which improves the device speed performance and hence reduced the power dissipation as it is evident from results respectively. Since, there is appreciable reduction in electric field at the drain side in TGRC-MOSFET in comparison to CRC-MOSFET which results in lower leakage current.

The noise assessment of Novel Transparent Gate Recessed Channel MOSFET has been investigated based on the simulated result from ATLAS device simulation. TCAD simulation results show TGRC-MOSFET divulges Conventional Recessed Channel (CRC)-MOSFET in terms of reduction in noise figure, noise conductance and parasitic capacitances. It also achieves higher optimum source impedance for high performance applications where noise immunity is a key factor. Here we accentuate our focus on Transparent Gate architecture incorporation onto the Conventional Recessed Channel MOSFET for superior noise performance of scaled MOS devices. Intensive TCAD device simulations have been performed to probe the internal transport conditions of CRC MOSFET and TGRC-MOSFET,

and substantial interpretation is given to the internal behaviours observed in all the devices investigated. TCAD simulation reveals the deterioration in minimum noise figure, noise conductance and parasitic capacitances. It also achieves higher optimum source impedance. This work presents a TGRC-MOSFET device which is reliable for RF applications and CMOS technology for the designing of multi-gigahertz communication circuits.

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CHAPTER 1

INTRODUCTION

1.1 CONVENTIONAL MOSFET

Having studied the junction diode, which is the most basic two-terminal semiconductor device, we now turn our attention to three-terminal semiconductor devices. Three-terminal devices are far more useful than two-terminal ones because they can be used in a multitude of applications, ranging from signal amplification to digital logic and memory [1]. The basic principle involved is the use of the voltage between two terminals to control the current flowing in the third terminal. In this way a three-terminal device can be used to realize a controlled source, which as we have learned is the basis for amplifier design. Also, in the extreme, the control signal can be used to cause the current in the third terminal to change from zero to a large value, thus allowing the device to act as a switch. The switch is the basis for the realization of the logic inverter, the basic element of digital circuits [2]. There are two major types of three-terminal semiconductor devices: the metal-oxide semiconductor field-effect transistor (MOSFET) and bipolar junction transistor (BJT). Although each of the two transistor types offers unique features and areas of application, the MOSFET has become by far the most widely used electronic device, especially in the design of integrated circuits (ICs), which are entire circuits fabricated on a single silicon chip. Compared to BJTs, MOSFETs can be made quite small (i.e., requiring a small area on the silicon IC chip), and their manufacturing process is relatively simple. Also, their operation requires comparatively little power. Furthermore, circuit designers have found ingenious ways to implement digital and analog functions utilizing MOSFETs almost exclusively [3]. All of these properties have made it possible to pack large numbers of MOSFETs (as many as 2 billion!) on a single IC chip to implement very sophisticated, very-large-scale-integrated (VLSI) digital circuits such as those for memory and microprocessors. Analog circuits such as amplifiers and filters can also be implemented in MOS technology, albeit in smaller, less-dense chips. Also, both

analog and digital functions are increasingly being implemented on the same IC chip, in what is known as mixed-signal design. The objective of this chapter is to develop in the reader a high degree of familiarity with the MOSFET: its physical structure and operation, terminal characteristics, circuit models, and basic circuit applications. Although discrete MOS transistors exist, and the material studied in this chapter will enable the reader to design discrete MOS circuits, our

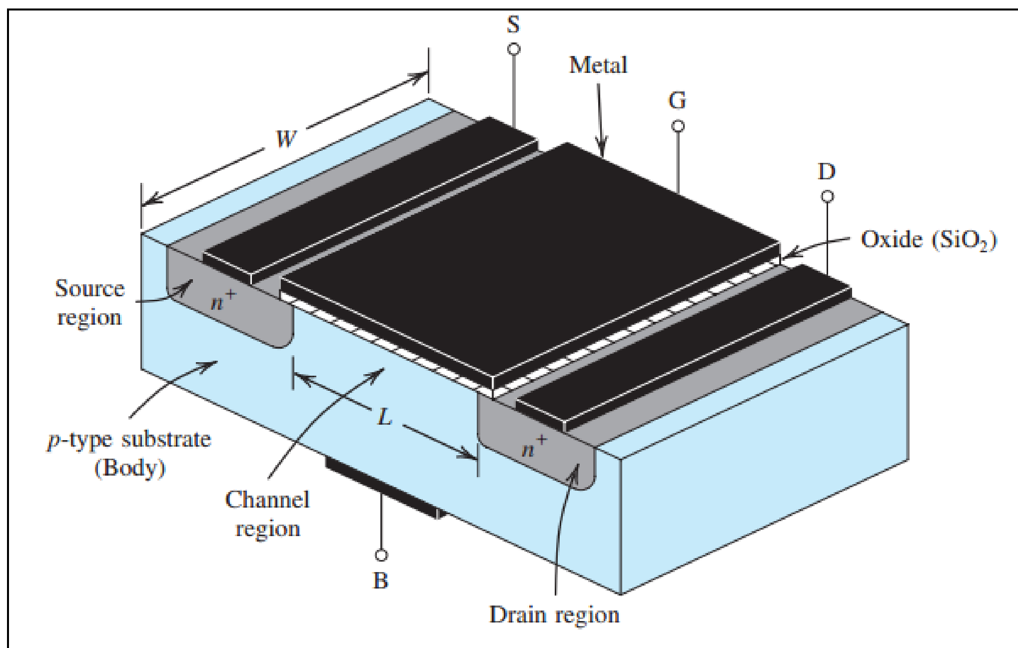

Fig. 1.1 Schematic structure of Conventional MOSFET [4].

study of the MOSFET is strongly influenced by the fact that most of its applications are in integrated-circuit design [1]. The high voltage power MOSFETs that are available today are N-channel, enhancement-mode, double diffused, Metal Oxide-Silicon, Field Effect Transistors. They perform the same function as NPN, bipolar junction transistors except the former are voltage controlled in contrast to the current controlled bi-polar devices. Today MOSFETs owe their ever-increasing popularity to their high input impedance and to the fact that being a majority carrier device, they do not suffer from minority carrier storage time effects, thermal runaway, or second breakdown [5].

1.2 NEED OF RECESSED CHANNEL MOSFETS

As mentioned, the supply voltage also scales down with device scaling, however, it cannot follow the speed of channel length reduction. Therefore, the maximum electric field for a minimum size MOS transistor rises to the tens of Volts/µm level. The carriers in the device are accelerated by this electric field and acquire excessive kinetic energy. These high energy carriers are called "hot carriers" because they have effective temperatures of several thousands of carrier temperatures. The hot-carriers occur at the drain junction where the electric field is highest in a MOS device. To lose this excessive kinetic energy from scattering, the carrier needs to travel tens of nanometers which is of the order of half the channel length of the smallest devices currently in mass production. This effect is also called velocity overshoot because the carriers travel at higher velocity than the scatter-limited saturation velocity. Therefore the carrier distribution along the channel is changed and more carriers are injected from the source. The high energy carriers also cause excess noise because of these high carrier temperatures and field modification along the channel. Moreover, the conventional planar MOSFETs also face the drawbacks of increase in the sub-threshold swing due to high doping and increase in series resistance due to the shallow junction. Recent experimental studies on sub-100 nm MOSFET's [6-7] attempted to overcome the drawbacks faced by conventional planar MOSFET's, such as the increase in sub-threshold swing due to high doping and the increase in series resistance due to the shallow junction. High transconductance and excellent sub-threshold swing were attained by low-temperature operation and silicon-on-insulator structures, respectively. However, the problems of short channel effects were not fully addressed. The quickening pace of MOSFET scaling is accelerating the introduction of new technologies to extend CMOS beyond the 65 nm node. These technologies include both new materials and advanced MOSFET structures.

1.2.1. RECESSED CHANNEL MOSFET PERFORMANCE

Recessed Channel (RC) MOSFET, as shown in Fig.1.2 is considered as a promising device for suppressing short channel effects and hot carrier effects because structures with shallow junctions or even negative junctions can be fabricated without any increase in the series resistance. These MOSFETs are, hence, good candidates for use in sub-100 nm regime. The optimization of the structure and technology is, however, important to obtain better gate

control and hence, high drain current. The geometry of the device retained for the scaling of MOSFET down to the sub-100 nm range should not require too many additional and expensive process steps. This eliminates, for the moment, original structures as gate-all-around transistors [8], although very good performances in term of short-channel effects and current drive capabilities were demonstrated, due to the excellent control of the gate on the channel. In a review of the technology requirements for sub-100 nm MOSFET's, Fiegna et al. reported different conventional structures with uniform, buried or epitaxial channel and also single and double gate SOI devices, but overlooked the investigation of structures with elevated source and drain. These device architectures have recently attracted much attention for their low sensitivity to the short-channel effects and hot carrier effects [9-11].

Φ

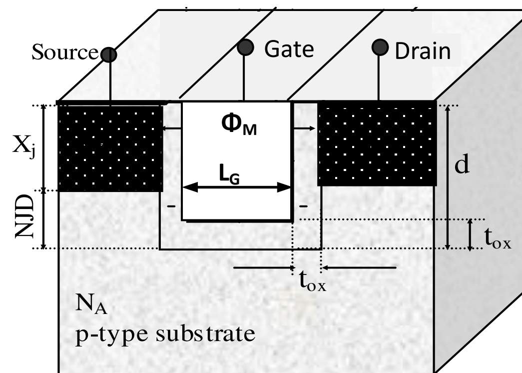

Fig.1.2. Schematic cross-sectional view of Conventional Recessed Channel MOSFET. **[12]**

The "corner effect" or the potential barrier formed at each concave corner is found to be responsible for suppressing the short-channel effects, hot-carrier effects and punch-through. It is also responsible for the degradation of current capability [13]. The higher the potential barriers are, the larger the energy needed to surmount the potential barriers for carriers, so the threshold voltage is increased and the carrier velocity is reduced with the increase of the concave corner, which will bring about hot carrier-effect immunity and driving capability degradation.

When the carriers move to the drain electrode, they not only have to surmount the potential barriers formed at the two concave corners, but also have to change their moving direction. And the electric field at the region near the source is smaller in Recessed Channel than that in planar devices. Therefore the impact ionization generation rate is far smaller than that in planar devices. Low impact ionization rate brings small substrate and gate current consequentially, which means hot-carrier-effect immunity in Recessed Channel MOS devices is better than that in planar devices. Furthermore, as the concave corner increases, the hot-carrier effect is strongly suppressed due to noticeable corner effect. Carriers lose more energy when surmount the two potential barriers and their velocity becomes lower, therefore the hot-carrier effect is low [12]. As the negative junction depth (NJD) increases, the potential barriers increase, and the potential in the channel becomes lower. Besides that, as the negative junction depth increases, the flat portion of the channel shortens. Hence, the path in which carriers are accelerated is shortened and the energy gained by the carriers is lowered, so the probability of becoming the hot carrier becomes smaller and the hot-carrier-effect immunity is better. Studies by Chaujar et.al [14-15], Appenzeller et.al [16] prove that the capability of the hot-carrier-effect immunity in recessed channel MOSFET is intensely influenced by geometric structure. Due to the geometric structure, the electric field distribution and the corner effect in Recessed Channel MOSFETs are influenced strongly, so do the transportation of carriers and the hot-carrier-effect immunity.

The shape and dimensions of the gate of MOSFET transistors are generally the only device parameters controllable by the integrated-circuit design engineer once the process parameters have been specified. Typically the designer utilizes the rectangular-shaped gate whenever possible. This approach is commonplace since the rectangular geometry is convenient for layout, component density can be high, and good models for this device have been developed. Nonrectangular devices are (eg., trapezoidal, "L"-shaped, "V"-shaped, etc.), however, used occasionally [17-18]. These devices are particularly useful when it is of paramount importance to fit a given amount of circuitry into a predetermined region on the die or when extreme device lengths or widths are required. Unfortunately, utilization of these nonrectangular MOSFET's is limited by the unavailability of suitable device models. This dissertation, is hence, focused on the rectangular gate geometry recessed channel MOSFETs. This work can, thus, guide us to optimize the Recessed Channel (RC) structure and to obtain the most satisfactory hot-carrier reliability. It is clear that one potential barrier is formed at each concave corner for RC MOSFET. However, there is only one barrier observed in planar

devices [13]. The formation of these barriers is the basic reason for improvement in the shift of threshold voltage with a decrease in channel length in RC MOSFET. With increase of drain bias voltage, the surface potential distribution is affected directly by drain voltage using depleted area causing the potential in the channel to distort intensely; and the only potential barrier present in planar MOSFETs disappears. On the contrary, the potential barrier near drain decreases just a little and in addition, these two barriers also exist. Thus the effect of drain electric field on channel is diminished in these devices and the DIBL (Drain-Induced Barrier Lowering) is suppressed. In a planar device, the main reason for short channel effects (such as shift of threshold voltage, punch-through, DIBL etc.) is attributed to the severe impact of drain voltage on electric field in the channel; and as a result, the drain area potential extends to the source region [19]. In RC devices, however, the effect of drain voltage is almost shielded by the two barriers formed at each concave corner and the short channel effects are, hence, suppressed effectively. Because of the emergence of corner effect, the threshold voltage roll-off with the shortness of channel length is removed completely in RC MOSFETs even in sub-100 nm regions. It is possible to eliminate this threshold voltage shift against channel length variation by taking advantage of the corner effect. A number of structural parameters, such as the concave corner, junction depths, concave sidewall structure, and the channel doping concentration can be used to adjust the threshold voltage in RC MOSFET's, while only the channel doping concentration can be used in conventional planar MOSFET's. In addition, although the gate length of the conventional MOSFET is longer than the effective channel length due to the lateral diffusion of the source/drain regions, the gate length of the RC MOSFET is shorter than the effective channel length because the junction depths are less than the groove depth. Therefore, RC structure lends itself to higher packing density. This MOSFET design, thus, proves its efficacy for high performance applications where device and hot carrier reliability is a major concern.

For the fabrication feasibility of Recessed Channel MOSFET structure, several integration schemes have been suggested such as plasma etching and LOCOS isolation [20], reactive ion etching and LOCOS isolation technique [21], shallow trench isolation (STI) where gate oxide films were produced with a conventional furnace and the oxide films for gate electrode was deposited by LP-CVD at 850˚C [22] and Self-Aligned Chemical Mechanical Polishing (CMP), where, the self-aligned process was defined by the groove etching and polysilicon CMP steps [23].

In order to overcome the shortcomings associated with Recessed Channel MOSFET such as driving current degradation, poor carrier transport efficiency and reduced gate controllability over the channel, Gate Dielectric Engineering and Gate Electrode Workfunction Engineering are carried out in order to overcome these drawbacks and enhance the device performance. The next section outlined the manifestation of these engineering schemes for betterment of the device characteristics and improved reliability and further, extends the lifespan of conventionally scaled MOSFET device. Hence a novel structure introduced, called Transparent Gate Recessed Channel (TGRC) MOSFET. In this device a transparent conducting material is introduced in place of Aluminium gate. By using of transparent conducting material and replacing gate material, transport efficiency, gate controllability, electron velocity, electric field, electron temperature and thermal parameters have been improved.

1.3 TRANSPARENT GATE RECESSED CHANNEL (TGRC) MOSFET

Transparent Gate Recessed Channel MOSFET consists of gate which is made of transparent conducting material Indium Tin Oxide (ITO) as shown in Fig 1. Indium tin oxide (ITO or tin-doped indium oxide) is a solid solution of indium oxide (In_2O_3) and tin oxide (SnO_2). It is transparent and colorless in thin layers. Indium tin oxide is one of the most widely used transparent conducting oxides because of its two chief properties, its electrical conductivity and optical transparency, as well as the ease with which it can be deposited as a thin film. By using ITO, we improve I_{ON} which causes the decrease in device power consumption. The In_2O_3 phase itself contributes free electron for electrical conductivity [24].

When Tin (Sn) is diffused, then some of the oxygen vacancies may be created by SnO_2 which creates free electrons to enhance the concentration of carriers and hence increase conductivity and decrease the resistivity with temperature. In the presence of indium tin oxide in TGRC-MOSFET which is effectively acting as a parallel oxide with SiO_2 and hence effective permittivity is increased which eventually leads to increase in input impedance. It also decreases parasitic capacitances.

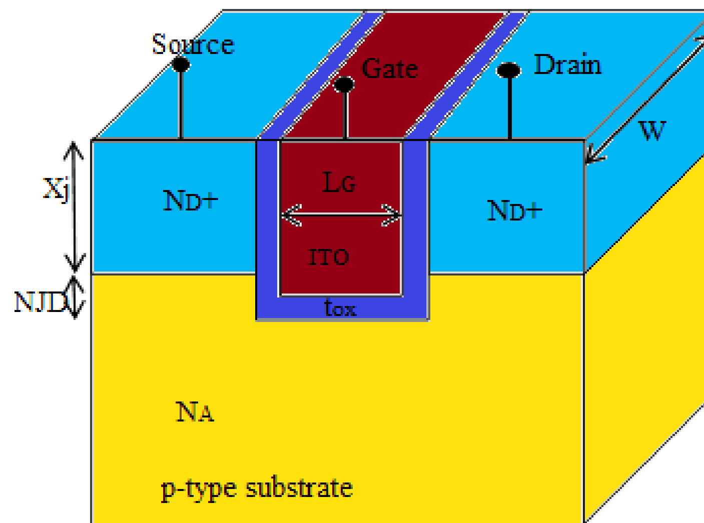

Fig.1.3 Schematic structure of Transparent Gate Recessed Channel (TGRC) MOSFET.

Hasten in semiconductor manufacturing techniques and more and more demand for high speed and more complicated Integrated Circuits (ICs) have driven the associated Metal Oxide Semiconductor Field Effect Transistor (MOSFET) sizes close to their physical limits. On the other hand, it is difficult to scale-down the supply voltage used to perform these ICs consistently due to compatibility problem with earlier generation circuits, power, noise margin and delay requirements, and not scaling the threshold voltage and sub-threshold slope.

While the successive increase in internal electric fields in aggressively scaled MOSFETs comes with the additional ameliorate of increased carrier velocities, and hence increased switching speed, it also presents higher reliability complications for the long period of operation of these devices.

As devices are scaled down, the benefits of higher electric fields saturate while the associated reliability problems get worse. The presence of large electric fields in MOSFETs implies the presence of high energy carriers, referred as “hot-carriers”, in such devices [25]. The presence of this kind of mobile carriers in the oxide creates some physical damages which may change device characteristics for a long time. The aggregation of damage can ultimately be the reason of circuit failure . The aggregation damage of the hot carrier results in deterioration in device behavior [19,26]. The need of superior performance of ICs has led to the scaling of MOSFETs down to 30 nm and below.

Design parameters of CRC-MOSFET & TGRC-MOSFET device designs	
Channel Length (L_G)	30nm
Device Width	200nm
Groove Depth	38nm
Source/Drain Junction Depth	30nm
Negative Junction Depth (NJD)	10nm
Substrate Doping (N_A)	$1x10^{16}$ cm^{-3}
Source/Drain Doping (N_D^+)	$1x10^{19}$ cm^{-3}
Physical Oxide Thickness (t_{ox})	2nm
Permittivity of SiO_2	$\varepsilon_{ox} = 3.9$
Gate to Source Voltage (V_{gs})	0.7V
Drain to Source Voltage (V_{ds})	0.5V
Work function for TGRC-MOSFET (Φ_{ITO})	4.7 eV
Work function for CRC-MOSFET (Φ_M)	4.1 eV

Table 1.1 Design parameters of CRC-MOSFET & TGRC-MOSFET device designs

The hot-carrier dilapidation becomes a stringent limitation to the reliability of 100-nm devices and VLSI packing density [27]. Under the influence of high lateral fields in short-channel MOSFETs, carriers in the channel and pinch-off regions of the transistor reach non-equilibrium energy distributions. The generation of these hot-carriers is the primary source of several reliability problems. Hot-carriers can acquire sufficient energy to surmount the energy barrier at the Si-SiO_2 interface or tunnel into the oxide.

From the last several decades, the hot carrier reliability performance in a MOS device has been studied since MOS device is scaled and suffered from hot carrier effect which also pervert analog circuit desideratum. When we scaled the device, the ameliorates of higher electric fields impregnate while associated reliability problems get worse. When electric field

will be large in MOSFETs, then carrier will have high energy and these carriers are hot carriers. To abate these hot-carrier effects in CRC-MOSFET, instead of metallic gate we are using Indium Tin Oxide.

1.4 ATLAS-DEVICE SIMULATOR

ATLAS provides general capabilities for physically-based two (2D) and three-dimensional (3D) simulation of semiconductor devices. ATLAS is designed to be used with the VWF INTERACTIVETOOLS. The VWF INTERACTIVE TOOLS are DECKBUILD, TONYPLOT, DEVEDIT, MASKVIEWS, and OPTIMIZER. See their respective manuals on how to use these products. ATLAS is supplied with numerous examples that can be accessed through DECKBUILD. These examples demonstrate most of ATLAS's capabilities. The input files that are provided with the examples are an excellent starting point for developing your own input files [29].

There are different physical models which are used in device simulation. These are:

1.4.1 MOBILITY MODELS

Electrons and holes are accelerated by electric fields, but lose momentum as a result of various scattering processes. These scattering mechanisms include lattice vibrations (phonons), impurity ions, other carriers, surfaces, and other material imperfections. Since the effects of all of these microscopic phenomena are lumped into the macroscopic mobilities introduced by the transport equations these mobilities are therefore functions of the local electric field, lattice temperature, doping concentration, and so on. Mobility modelling is normally divided into: (i) low-field behavior, (ii) high field behavior, (iii) bulk semiconductor regions and (iv) inversion layers [29].

The value of this mobility is dependent upon phonon and impurity scattering. Both of which act to decrease the low-field mobility. The high electric field behavior shows that the carrier mobility declines with electric field because the carriers that gain energy can take part in a wider range of scattering processes. The mean drift velocity no longer increases linearly with increasing electric field, but rises more slowly. Eventually, the velocity doesn't increase any more with increasing field but saturates at a constant velocity. Impurity scattering is relatively insignificant for energetic carriers, and so μsat is primarily a function of the lattice

temperature. Modeling mobility in bulk material involves: (i) characterizing μ_{n0} and μ_{p0} as a function of doping and lattice temperature, (ii) characterizing μsat as a function of lattice temperature, and (iii) describing the transition between the low-field mobility and saturated velocity regions. Modeling carrier mobilities in inversion layers introduces additional complications. Carriers in inversion layers are subject to surface scattering, extreme carrier-carrier scattering, and quantum mechanical size quantization effects. These effects must be accounted for in order to perform accurate simulation of MOS devices. The transverse electric field is often used as a parameter that indicates the strength of inversion layer phenomena. You can define multiple non-conflicting mobility models simultaneously. You also need to know which models are over-riding when conflicting models are defined [29].

1.4.2 Carrier Generation-Recombination Models

Carrier generation-recombination is the process through which the semiconductor material attempts to return to equilibrium after being disturbed from it. If we consider a homogeneously doped semiconductor with carrier concentrations n and p to the equilibrium concentrations n_0 and p_0 then at equilibrium a steady state balance exists according to:

$$n_0\, p_0 = n_i^2$$

Semiconductors, however, are under continual excitation whereby n and p are disturbed from their equilibrium states: n_0 and p_0. For instance, light shining on the surface of a p-type semiconductor causes generation of electron-hole pairs, disturbing greatly the minority carrier concentration. A net recombination results which attempts to return the semiconductor to equilibrium. The processes responsible for generation-recombination are known to fall into six main categories:

- phonon transitions
- photon transitions
- Auger transitions
- surface recombination
- impact ionization
- tunnelling

In addition to generation-recombination within the bulk of the semiconductor, electrons or holes may recombine or be generated at interfaces. The rate of surface recombination may be

even greater than within the bulk. The standard method is to model interface recombination in a similar manner as the bulk generation-recombination rate [29].

1.4.3 IMPACT IONIZATION MODELS

In any space charge region with a sufficiently high reverse bias, the electric field will be high enough to accelerate free carriers up to a point where they will have acquired sufficient energy to generate more free carriers when in collision with the atoms of the crystal. In order to acquire sufficient energy, two principle conditions must be met. First, the electric field must be sufficiently high. Then, the distance between the collisions of the free carrier must be enough to allow acceleration to a sufficiently high velocity. In other words, the carrier must gain the ionization energy E_i between collisions. If the generation rate of these free carriers is sufficiently high this process will eventually lead to avalanche breakdown. The general impact ionization process is described by-

$$G = \alpha_n \left|\vec{J}\right|_n + \alpha_p \left|\vec{J}\right|_p$$

Here, G is the local generation rate of electron-hole pairs, $\alpha_{n,p}$ are the ionization coefficient for electrons and holes and $J_{n,p}$ are their current densities. The ionization coefficient represents the number of electron-hole pairs generated by a carrier per unit distance travelled. The accurate calculation of this parameter has been researched because it is vital if the effects related to impact ionization, such as substrate current and device breakdown, are to be simulated. These models can be classified into two main types: local and non-local models. The former assume that ionization at any particular point within the device is a function only of the electric field at that position. Non-local models, however, perform a more rigorous approach by taking into account the energy that the carrier gains [29].

1.4.4 GATE CURRENT MODELS

In devices that have a metal-insulator-semiconductor (MIS) formation, the conductance of the insulating film would ideally be considered as zero. But, for the sub 0.5um generation of MOS devices there is now considerable conductance being measured on the gate contacts.

This gate current has resulted in two major consequences, one negative and one positive. On the negative side, the gate current is responsible for the degradation in device operating

characteristics with time. This reliability issue is important because the lifetime of electronic parts has to be guaranteed. You can simulate reliability within the Silvaco suite of tools for device level reliability which are described in a later chapter [29].

On the positive side, the existence of this gate current has caused the proliferation of the nonvolatile memory market. These devices use the existence of gate current to program and erase the charge on a "floating" contact. This concept has resulted in a variety of different devices such as FLASH, FLOTOX, and EEPROM. All such devices rely on the physics of the gate current process for their existence. There are a variety of different conduction mechanisms within an insulating layer, but in the case of non-volatile memory, only two mechanism are relevant: Fowler-Nordheim tunneling and hot carrier injection. Models for these two injection processes are described in the following sections. In the case of hot electron injection, two models are available: the lucky electron model and the Concannon gate current model [29].

1.4.5 DEVICE LEVEL RELIABILITY MODELING

The Hansch Reliability Model can be used to simulate MOS transistor degradation under stress conditions. The causes of device characteristic degradation are the hot electron (hole) injection into gate oxide, and the trapping of electron (hole) charge on the effective interface acceptor (donor) like traps. The model calculates hot electron (hole) injection current according to the lucky electron model. The arbitrary position-dependent distributions of acceptor and donor-like traps are specified on the oxide-semiconductor interface with corresponding capture cross sections. The device degradation is calculated as a function of stress time by performing transient calculations. The trap rate equation is solved on every time-step and thus the trapped electron (hole) concentration is calculated [29].

The results of stress simulation can be used to calculate the characteristics of the degraded device (the shift of the threshold voltage, transconductance degradation, and so on). You can view the distribution of traps, hot electron (hole) current density, and trapped electron (hole) distribution by using TONYPLOT.

ATLAS simulations use two input files. The first input file is a text file that contains commands for ATLAS to execute. The second input file is a structure file that defines the structure that will be simulated. ATLAS produces three types of output files. The first type of output file is the run-time output, which gives you the progress and the error and warning

messages as the simulation proceeds. The second type of output file is the log file, which stores all terminal voltages and currents from the device analysis. The third type of output file is the solution file, which stores 2D and 3D data relating to the values of solution variables within the device at a given bias point. The ATLAS tool supports calculation of various AC parameters like Hybrid (H), Admittance(Y), Impedance (Z), Scattering(S) etc. The gain analysis can also be done as a part of small signal analysis. AC sinusoidal small-signal analysis should be performed after solving for a DC condition. The full Newton method must be used for this analysis. Frequency range of interest, device width and the method for ac analysis has to be selected. A direct parameter is included which is robust for all range of frequencies. The gate terminal is selected as input port where ac bias will be applied, while drain terminal is selected as output port indicating that device works in common source configuration.

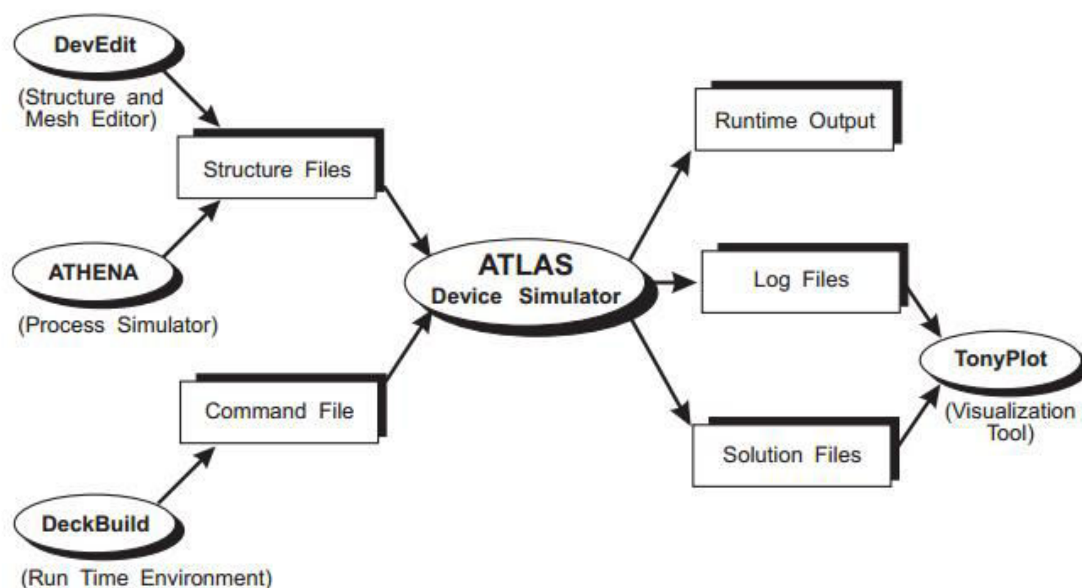

Fig.1.4 Processing of ATLAS Device Simulation **[28]**

1.4.6 SPECIFYING THE INITIAL MESH

The first statement must be:

MESH SPACE.MULT=<VALUE>

This is followed by a series of X.MESH and Y.MESH statements.

X.MESH LOCATION=<VALUE> SPACING=<VALUE>

Y.MESH LOCATION=<VALUE> SPACING=<VALUE>

.

The SPACE.MULT parameter value is used as a scaling factor for the mesh created by the X.MESH and Y.MESH statements. The default value is 1. Values greater than 1 will create a globally coarser mesh for fast simulation. Values less than 1 will create a globally finer mesh for increased accuracy. The X.MESH and Y.MESH statements are used to specify the locations in microns of vertical and horizontal lines, respectively, together with the vertical or horizontal spacing associated with that line. You must specify at least two mesh lines for each direction. ATLAS automatically inserts any new lines required to allow for gradual transitions in the spacing values between any adjacent lines. The X.MESH and Y.MESH statements must be listed in the order of increasing x and y. Both negative and positive values of x and y are allowed [29].

1.4.7 SPECIFYING REGIONS & MATERIALS

Once the mesh is specified, every part of it must be assigned a material type. This is done with REGION statements. For example:

REGION number=<integer> <material_type> <position parameters>

Region numbers must start at 1 and are increased for each subsequent region statement. You can have up to 200 different regions in ATLAS. A large number of materials is available. If a composition-dependent material type is defined, the x and y composition fractions can also be specified in the REGION statement.

The position parameters are specified in microns using the X.MIN, X.MAX, Y.MIN, and Y.MAX parameters. If the position parameters of a new statement overlap those of a previous REGION statement, the overlapped area is assigned as the material type of the new region. Make sure that materials are assigned to all mesh points in the structure. If this isn't done, error messages will appear and ATLAS won't run successfully [29].

1.4.8 SPECIFYING ELECTRODES

Once you have specified the regions and materials, define at least one electrode that contacts a semiconductor material. This is done with the ELECTRODE statement. For example:

ELECTRODE NAME=<electrode name> <position_parameters>

You can specify up to 50 electrodes. The position parameters are specified in microns using the X.MIN, X.MAX, Y.MIN, and Y.MAX parameters. Multiple electrode statements may have the same electrode name. Nodes that are associated with the same electrode name are treated as being electrically connected. Some shortcuts can be used when defining the location of an electrode. If no Y coordinate parameters are specified, the electrode is assumed to be located on the top of the structure [29].

You also can use the RIGHT, LEFT, TOP, and BOTTOM parameters to define the location. For example:

ELECTRODE NAME=SOURCE LEFT LENGTH=0.5

specifies the source electrode starts at the top left corner of the structure and extends to the right for the distance LENGTH.

1.4.9 SPECIFYING DOPING

You can specify analytical doping distributions or have ATLAS read in profiles that come from either process simulation or experiment. You specify the doping using the DOPING statement. For example:

DOPING <distribution_type> <dopant_type> <position_parameters>

1.4.10 ANALYTICAL DOPING PROFILES

Analytical doping profiles can have uniform, gaussian, or complementary error function forms. The parameters defining the analytical distribution are specified in the DOPING statement. Two examples are shown below with their combined effect :

DOPING UNIFORM CONCENTRATION=1E16 N.TYPE REGION=1

DOPING GAUSSIAN CONCENTRATION=1E18 CHARACTERISTIC=0.05 P.TYPE \
X.LEFT=0.0 X.RIGHT=1.0 PEAK=0.1

The first DOPING statement specifies a uniform n-type doping density of 10^16 cm-3 in the region that was previously labelled as region #1. The position parameters X.MIN, X.MAX, Y.MIN, and Y.MAX can be used instead of a region number [29].

1.5 SYNTAX AND PARAMETERS OF ATLAS

1.5.1 THE ORDER OF ATLAS COMMANDS

The order in which statements occur in an ATLAS input file is important. There are five groups of statements that must occur in the correct order (see Figure 1). Otherwise, an error message will appear which may cause incorrect operation or termination of the program. For example, if the material parameters or models are set in the wrong order, then they may not be used in the calculations. The order of statements within the mesh definition, structural definition, and solution groups is also important. Otherwise, it may also cause incorrect operation or termination of the program[29].

Group	*Statements*
1. Structure Specification	MESH REGION ELECTRODE DOPING
2. Material Models Specification	MATERIAL MODELS CONTACT INTERFACE
3. Numerical Method Selection	METHOD
4. Solution Specification	LOG SOLVE LOAD SAVE
5. Results Analysis	EXTRACT TONYPLOT

***Fig.1.5 ATLAS Command Groups with the Primary Statements in each Group* [26].**

1.5.2 TYPES OF PARAMETERS

Parameter	**Description**	**Value Req.**	**Example**
Character	Any character string	Yes	INFILE=NMOS.DOP
Integer	Any whole number	Yes	REGION=2
Logical	A true or false condition	No	GAUSSIAN
Real	Any real number	Yes	X.MIN=0.52

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CHAPTER 2

TRANSPARENT CONDUCTING OXIDES-AN OVERVIEW

2.1. INTRODUCTION

Transparent conducting oxides (TCOs) are electrical conductive materials with comparably low absorption of electromagnetic waves within the visible region of the spectrum. They are usually prepared with thin film technologies and used in opto-electrical apparatus such as solar cells, displays, opto-electrical interfaces and circuitries. Here, based on a modern database-system, aspects of up-to-date material selections and applications for transparent conducting oxides are sketched, and references for detailed information are given. As n-type TCOs are of special importance for thin film solar cell production, indium-tin oxide (ITO) and the reasonably priced aluminium-doped zinc oxide (ZnO:Al), are discussed with view on preparation, characterization and special occurrences. For completion, the recently frequently mentioned typical p-type delafossite TCOs are described as well, providing a variety of references, as a detailed discussion is not reasonable within an overview publication [1].

TCOs are electrical conductive materials with a comparably low absorption of light. They are usually prepared with thin film technologies and used in opto-electrical devices such as solar cells, displays, opto-electrical interfaces and circuitries. Glass fibres are nearly lossless conductors of light, but electrical insulators; silicon and compound semiconductors are

wavelength dependent optical resistors (generating mobile electrons), but dopant dependent electrical conductors. Transparent conducting oxides are highly flexible intermediate states with both these characteristics. Their conductivity can be tuned from insulating via semiconducting to conducting as well as their transparency adjusted. As they can be produced as n-type and p-type conductive, they open a wide range of power saving opto-electrical circuitries and technological applications. A still valuable overview of transparent conductive oxides is given in [2], basics to material physics of TCOs are discussed in [3], some structural investigation of TCOs was made e.g., in [4], preparation of TCOs was discussed in [5] and substitutes for the most popular transparent conducting oxide, namely ITO are listed in [6]. Here, based on a modern database-system, aspects of up-to-date material selections and applications for transparent conducting oxides are sketched, and references for detailed information are given. As n-type TCOs are of special importance for thin film solar cell production, ITO and the reasonably priced aluminium-doped zinc oxide (ZnO:Al) are discussed with view on preparation, characterization and special occurrences. For completion, the recently frequently mentioned typical p-type delafossite TCOs are described as well, providing a variety of references, as a detailed discussion is not reasonable within an overview publication.

As transparent conducting oxides are usually compound semiconductors—where the non-metal part is oxygen—they are discussed along their metal elements. Metals were used as compound materials or dopants (with just a few per cent content).

2.2 TRANSPARENT CONDUCTING OXIDES (TCOS)

2.2.1 TCOS IN GENERAL

In TCOs, the non-metal part, B, consists of oxygen. In combination with different metals or metal-combinations, A, they lead to compound semiconductors, Ay Bz, with different opto-electrical characteristics. These opto-electrical characteristics can be changed by doping, Ay Bz:D (D = dopant), with metals, metalloids or non-metals. Hence, metals can be part of the compound semiconductor itself, A, or can be a dopant, D. Scanning the periodic table of elements, with a view on the utilization of metals for TCOs, results in Table 1 (regarding just the 2nd and 3rd period, exclusively aluminium).

Period of the PE	Compound semiconductor	Dopant	Preparation	Characterization	Reference
2	NiO	Li	Pulsed Laser Deposition (different Li-concentr.)	?	[6]
			No TCO-Layers with Be		
3	ZnO	Na, Al	Sol-gel, Annealing	SEM, Photoluminescence	[7–9]
	Cr_2O_3	Mg, N	Spray Pyrolysis	?	[10]
	$CuCrO_2$ (Delafossite)	Mg	Sol-gel Technique	?	[11]
	$Mg_{1-x}Zn_xO$	In	Pulsed Laser Deposition (different substrates)	X-ray diffraction, HRTEM	[12]
	$Mg_{1-x}Zn_xO$	Al	Radio Frequency Magnetron Sputtering (different substrates)	?	[13]
	$Mg_{12}Al_{14}O_{33}$ ("Mayenite") Al		?	?	[14]

Table 1.Published results regarding transparent conducting oxide (TCO)-layers, containing metallic elements e.g., from the 2nd and 3rd period of the periodic table of the elements (PE, excluding aluminum), including examples for the later discussed ZnO's and delafaossites (mayenites)—research with the web of knowledge using "TCO < name of element > oxide".

Outstanding good optical characteristics have been provided by tin-, indium- and zinc oxides (A = tin, indium, zinc). Well known is, for example, indium tin oxide (ITO), and the doping of zinc oxide with less than 5% aluminium (ZnO:Al). Moreover, doped delafossite and mayenite compounds are of upcoming interest (see Table 1). A variety of preparation and characterization methods was applied to investigate their different chemical structures and physical characteristics. These shall be briefly discussed.

2.2.2 Indium Tin Oxide (ITO)

ITO is a solid solution of indium (III) oxide (In_2O_3) and tin(IV) oxide (SnO_2), with typically 90%wtIn_2O_3, 10%wtSnO2. It is transparent and colorless as a thin film and yellowish to grey as bulk material. Indium tin oxide is the most widely used transparent conducting oxide (TCO [15]) because of its two key properties, its electrical conductivity and optical transparency. ITO thin films are still deposited with ion assisted plasma evaporation [17], (low temperature) electron beam evaporation, direct current (DC), pulsed DC (PDC), high

power pulsed magnetron sputtering (HPPMS), radio frequency (RF) magnetron sputtering, thermal evaporation or pulsed laser deposition (PLD). Post process thermal annealing steps are discussed for the example in [17], oxygen-plasma treatments in and the influence of acids and bases on ITO thin films in. Investigations were made on electrical, optical and structural properties of this ternary compound semiconductor. According to structural investigations, the focus was set on the border between amorphous and crystal phases [18] and the growth mechanisms (Volmer-Weber, Frank-van der Merwe). Band structure and work function are analysed in.

2.2.3 ALUMINIUM DOPED ZINC OXIDE (ZnO:Al)

Transparent conducting, aluminum doped zinc oxide thin films (AlxZnyOz, ZnO:Al) contain about 2%wtaluminum and can be produced with spray pyrolysis, sol gel technology, electro deposition, vapour phase deposition, magnetron DC sputtering, magnetron RF sputtering or a combination of both the sputter deposition methods. Moreover, high quality deposition methods using thermal plasmas, (low pressure (LP), metal organic (MO), plasma enhanced (PE)) chemical vapour deposition (CVD), electron beam evaporation, pulsed laser deposition and atomic layer deposition can be applied [19].

The underlying substrate—crystalline, amorphous or organic—may have an influence on the grown structure and the opto-electronic properties of the thin film [20], independent of the used deposition method. For example, in the case of solar cell production, an ultra-thin CdS buffer layer is usually the basis for ZnO:Al deposition. Even if the substrate is identical, the layer thickness (deposition time, position upon the substrate) itself influences the physical values of the deposited thin film [21]. A variation of the physical values from the grown thin films can also be reached by changing process parameters, as temperature or pressure, or by additions to the process gas, as oxygen or hydrogen. Commonly, pure zinc oxides are n-doped with aluminium. Alternatively, n-doping can be done with metals such as copper, Cu, silver, Ag, gallium, Ga, magnesium, Mg, cadmium, Cd, indium, In, tin, Sn, scandium, Sc, yttrium, Y, cobalt, Co, manganese, Mn, chrome, Cr, and boron, B. p-Doping of ZnO is technologically difficult, but apart from nitrogen, N, phosphorus, P, seems to be an adequate dopant [22]. The opto-electronic properties of these TCO thin films can be changed by post process thermal annealing in an inert gas or reactive gas atmosphere. Especially surface and interface states can be influenced. The deterioration of ZnO:Al thin films is discussed in [23].

2.2.4 DELAFOSSITE AND MAYENITE TYPE TRANSPARENT CONDUCTING OXIDES

Commonly, ITO- and ZnO-based TCO thin films are n-doped, as p-doping has been shown to be technologically more difficult. Fortunately, for delafossite compound semiconductors this is vice versa. They typically show TCO properties with semiconducting p-type characteristics. Delafossites, CuxAyOz, are commonly ternary material combinations of copper, Cu, one (or more) further metal(s), A, (aboriginal iron, A = Fe) and oxygen, O. Copper may be replaced by silver, palladium or platinum. As further metal, A, iron, cobalt or chrome (without doping hardly transparent) may be used as well as elements of the 2nd group of the periodic table of the elements—strontium, barium—or the 3rd group—aluminium, gallium, indium, scandium, yttrium, lanthanum.

Moreover, other lanthanides such as praseodymium, neodymium samarium and europium have been applied [24], in order to get ternary semiconductor compounds. Quaternary semiconductors as for example the Sb-based $CuA_2/3Sb1/3O_2$(A = Mn, Co, Ni, Zn, Mg), respectively $AgA_2/3Sb1/3O_2$(A = Ni, Zn) or the Cr-based $CuCr1{-}xAxO_2$(A = Mg, Ca, Al) delafossites have been investigated. Ag-Cu and Rh-Mg replacements were for example studied in the quaternary structure Cu1−xAgxRh1−y $MgyO_2$. Oxygen off-stoichiometry, $CuxAyO_{2+d}$, has been examined. Oxy-sulphide delafossite type TCOs, CuxAyOzSα, were sputtered (CuLa1−xOS:Srx, x = 0%–5%) or already existing delafossite-oxide films, $Cu_2In_2O_5$, sulfurized to $CuInS_2$, by annealing in H_2S [25]. Delafossites have been grown from a melt by a slow cooling-method in air.

They were deposited using low temperature hydro/solvothermal processes, the sol-gel technology and the spray pyrolysis technique. Moreover, advanced methods such as (direct current (DC), radio frequency (RF)) magnetron sputtering of prefabricated targets, with varying temperature, pressure, oxygen flow or sputter energies, pulsed laser deposition, with varying temperature and pressure [26], thermal evaporation, e-beam evaporation technique, and (low-pressure (LP), metal-organic (MO)) chemical vapor deposition (CVD) were applied. Annealing in N_2, O_2, air or argon was examined, showing for example a reduction in CuO resp. spinel $CuCr_2O_4$ fraction and formation of highly crystalline films with single-phase delafossite $CuCrO_2$structure. The CuA III O_2 group shows increasing band gap from A III= Al, Ga, to In. The largest gap $CuInO_2$can be doped both n- and p-type but not the smaller

gaps $CuAlO_2$ and $CuGaO_2$ [27]. Therefore, doping $CuInO_2$ with Ca results in p-type, doping with Sn inn-type semiconducting TCO thin films.

Bidirectional doping is possible for $CuFeO_2$, too (p-type: Mg, n-type: Sn). In addition, the electronic structure of $CuAO_2$(A = Al, Ga, Y) was discussed in and its luminescent properties in. Defect analyses have been made with the screened-hybrid density functional theory. Additional p-doping is usually performed with Ca, Mg or occasionally with K, in order to increase the conductivity resulting in e.g., $CuInO_2$:Ca, $Cu_2In_2O_5$:Ca, $CuYO_2$:Ca, $CuCrO_2$:Mg, CuScO2:Mg or Cu_2SrO_2:K. N-type doping of delafossite. TCO thin films is normally done with Sn, e.g., $CuInO_2$:Sn or $AgInO_2$:Sn.

Further discussion on doping of delafossite TCOs is shown in. Because of the structural anisotropy of the $CuAlO_2$-crystal, anisotropic electrical conductivity was detected in. Ohmic contacts between $CuInO_2$and Cu are reported in. The crystal structures and chemistries are by far the best investigated topics in delafossite (semi)conductor research and systematically discussed in; the according temperature dependency is shown in [28].

2.3 SUMMARY

Based on a modern database-system aspects of up-to-date material selections and applications for transparent conducting oxides have been sketched; references for detailed information have been given for the interested reader. As n-type TCOs are of special importance for thin film solar cell production, indium-tin oxide (ITO) and the reasonably priced aluminium-doped zinc oxide (ZnO:Al) have been discussed with view on preparation, characterization and special occurrences. For completion, typical p-type delafossite TCOs have been described the same way, providing a variety of references, as a detailed discussion is not reasonable within an overview-publication. Moreover, absolutely unusual, novel TCO materials have been discussed and their presence and development in the world of science pointed out. Trends have been shown.

As transparent conducting oxides are usually compound semiconductors—where the non-metal part is oxygen—they have been discussed along their metal elements. Metals were used as compound materials or dopants (with just a few per cent content).

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CHAPTER 3

TRANSPARENT GATE RECESSED CHANNEL MOSFET FOR IMPROVED HOT CARRIER RELIABILITY APPLICATIONS

3.1. INTRODUCTION

A novel device structure called Transparent Gate Recessed Channel MOSFET (TGRC-MOSFET) is proposed to alleviate the hot carrier effects for the advanced nanometer process. TGRC-MOSFET involves a recessed channel and incorporates Indium Tin Oxide as a transparent gate. TCAD analysis shows that the performance of TGRC-MOSFET surpasses Conventional Recessed Channel (CRC)-MOSFET in terms of high I_{ON}/I_{OFF} ratio and better carrier transport efficiency as compared to Conventional Recessed Channel (CRC) MOSFET.

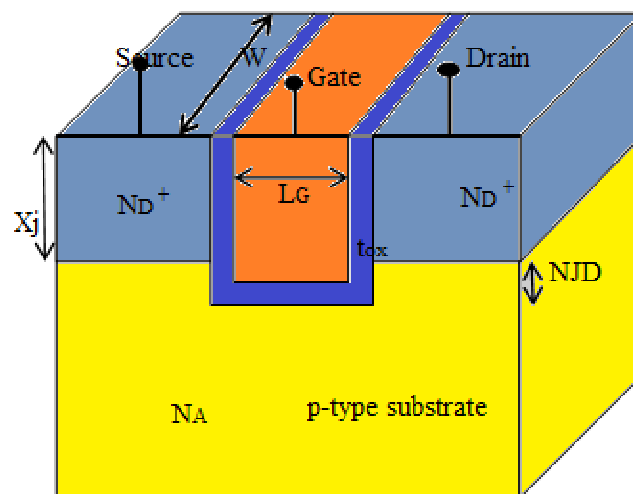


Fig. 3.1 Schematic structure of Transparent Gate Recessed Channel MOSFET.

This simulation divulges the reduction in hot-carrier-effects metrics like electron velocity, electron temperature, potential, and electron mobility. All the simulations have been done using DEVEDIT-3D and ATLAS device simulator. The need of superior performance of ICs has led to the scaling of MOSFETs down to 30 nm and below. The hot-carrier dilapidation becomes a stringent limitation to the reliability of 100-nm devices and VLSI packing density [1-2].

To abate these hot-carrier effects in CRC-MOSFET, instead of metallic gate we are using Indium Tin Oxide. Indium tin oxide (ITO or tin-doped indium oxide) is a solid solution of indium oxide (In_2O_3) and tin oxide (SnO_2). It is transparent and colorless in thin layers. Indium tin oxide is one of the most widely used transparent conducting oxides because of its two chief properties, its electrical conductivity and optical transparency, as well as the ease with which it can be deposited as a thin film. By using ITO, we improve I_{ON} which causes the decrease in device power consumption. The In_2O_3 phase itself contributes free electron for electrical conductivity [3].

3.2 Simulation Results Of Transparent Gate Recessed Channel MOSFET

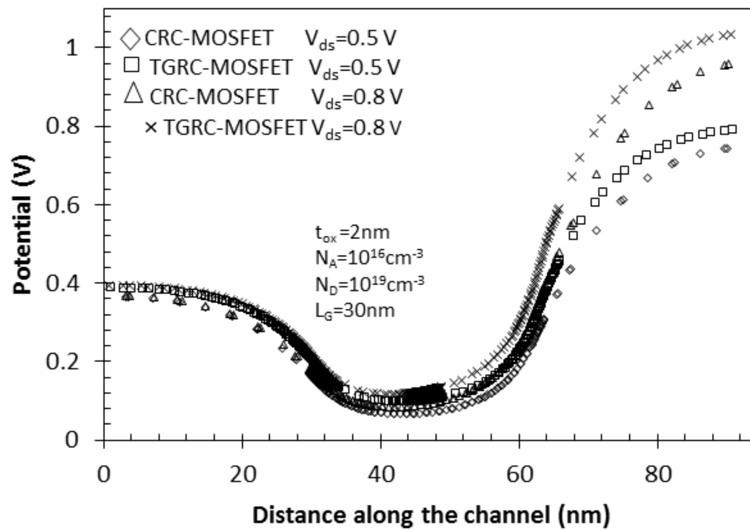
The present analysis is carried out for a channel length, L_G=30nm, uniformly doped source/drain, N_D with doping density of $1x10^{19}$ cm^{-3}, p type substrate doping, N_A with a doping density of $1x10^{16}$ cm^{-3}, SiO_2 thickness, t_{ox}=2.0 nm. The gate work function (Φ_{ITO}) is 4.7 eV.

3.2.1 Potential

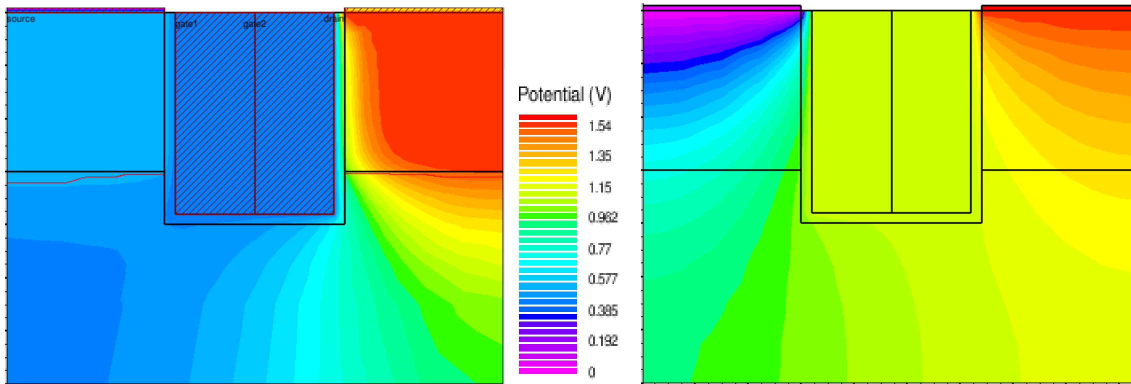
Fig.3.2 (a) shows the variation of surface potential along the channel for CRC-MOSFET and TGRC-MOSFET at two different drain voltages V_{ds}=0.5 V and 0.8 V. Fig.3.2 (b) and Fig.3.2 (c) shows the surface potential profile for TGRC-MOSFET and CRC-MOSFET respectively. It is clearly evident from surface potential profiles that potential at drain side in TGRC-MOSFET is higher in compare to CRC-MOSFET.

Fig.3.3 and Fig.3.4 shows the conduction band and valence band energy profiles along the channel length for CRC-MOSFET and TGRC-MOSFET. The lowering of barrier potential at source side indicates that the DIBL (Drain Induced Barrier Lowering) effect is less observed in this device, as it is evident from Fig.3.2.(a) The improvement in DIBL effect is more in

case TGRC-MOSFET, as it incorporates the non-stationary effects such as velocity overshoots. This minimum potential shift towards the source is higher in the TGRC-MOSFET design as compared to CRC-MOSFET and thus, lowers the potential barrier for electrons flow from source to drain, accounting for better gate controllability over the channel.



(a)



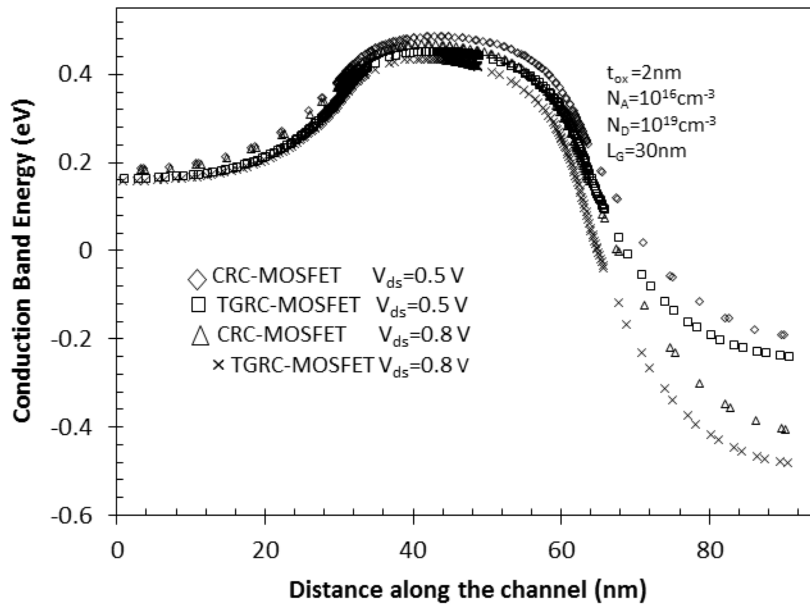
(b) **(c)**

Fig.3.2 (a) Surface potential as a function of position along the channel for CRC- MOSFET and TGRC-MOSFET at V_{ds}=0.5 V and V_{ds}=0.8 V. Surface potential profile for (b) TGRC-MOSFET (c) CRC-MOSFET.

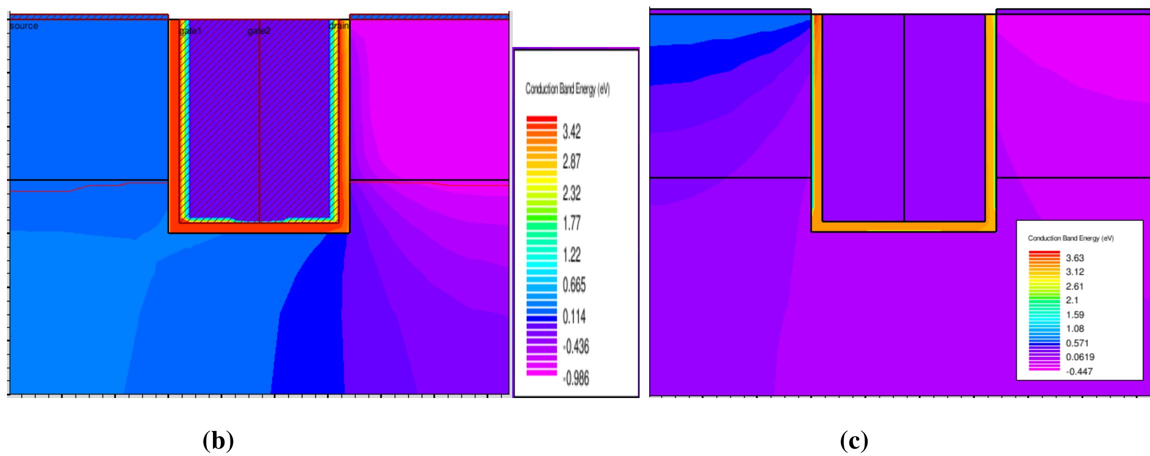
Fig.3.2 (a) also reflects a shift in the position of minimum surface potential towards the source, as L_G is reduced; thereby shifting the step potential profile towards the source resulting in a further reduction in DIBL. It also depicts the electric field distribution along the

channel for different value of gate lengths L_G, keeping the total gate length constant. As L_G reduces, the peak electric field position moves towards the source, thereby enhancing the carrier transport efficiency and hence the switching speed of the device [4].

3.2.2 Conduction Band Energy



(a)



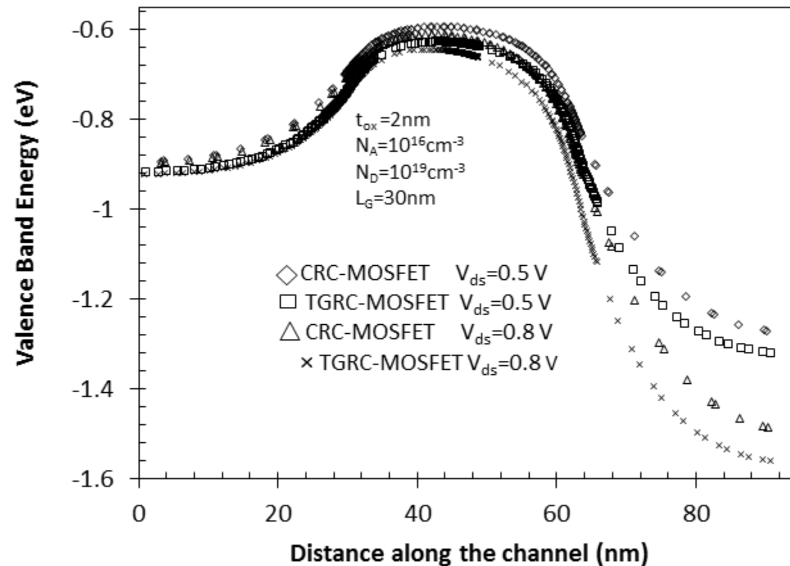
(b) **(c)**

Fig.3.3 (a) Conduction band energy as a function of position along the Channel for CRC- MOSFET and TGRC-MOSFET at V_{ds}=0.5 V and V_{ds}=0.8 V. Conduction Band Energy profile for (b) TGRC-MOSFET (c) CRC-MOSFET

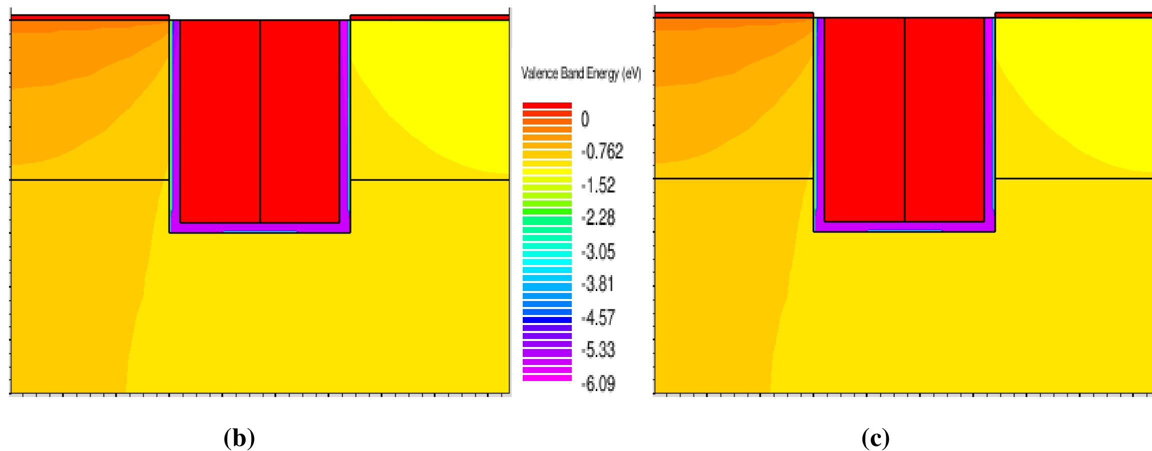
The results clearly depict that the benefit of transparent material gate, which is mainly associated with the screening of the channel region under gate transparent conducting

material from drain bias variations, depreciates at lower channel lengths due to the limit in resolution of the potential difference induced by the transparent gate. But this depreciation in the DIBL effect is significantly lower in the proposed TGRC-MOSFET in comparison to its CRC-MOSFET counterpart where the DIBL deterioration is appreciably higher as is clear from fig.3.2 (a).

3.2.3 VALENCE BAND ENERGY



(a)



(b) **(c)**

Fig.3.4 (a) Valance band energy as a function of position along the channel for CRC- MOSFET and TGRC-MOSFET at V_{ds}=0.5 V and V_{ds}=0.8 V. Valence Band Energy profile for (b) TGRC-MOSFET (c) CRC-MOSFET.

The improvement in DIBL effect is due to the step in conduction band energy profile in the channel region, which is resulting from transparent gate. DIBL is more pronounced

inconventional MOSFET, which is calculated from the difference of conduction band energy between V_{ds} of 0.8 and 0.5 V.

3.2.4 DRAIN INDUCED BARRIER LOWERING

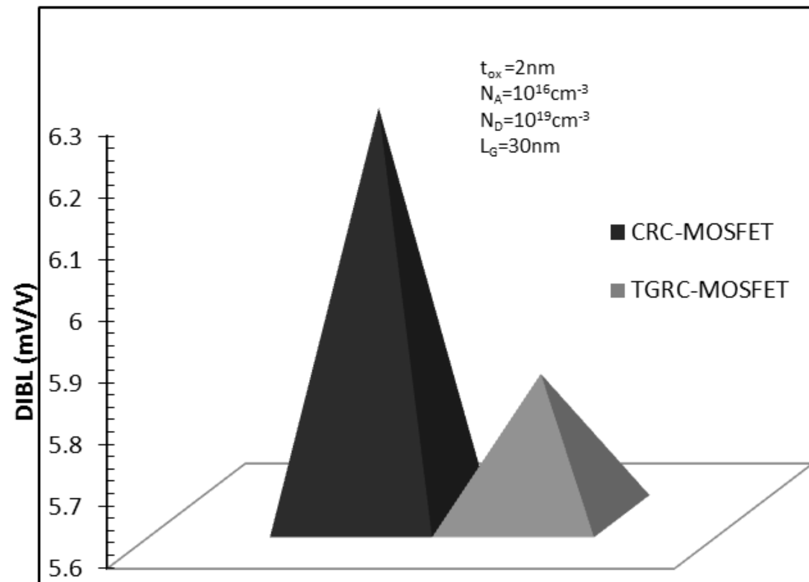
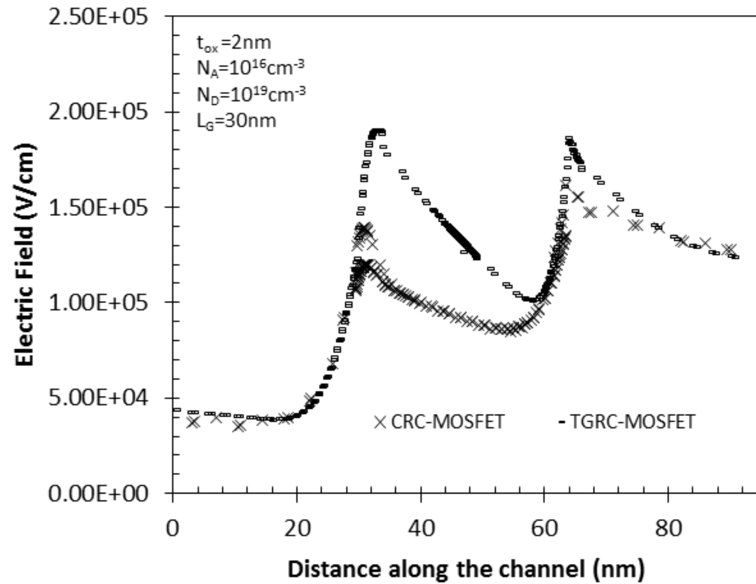


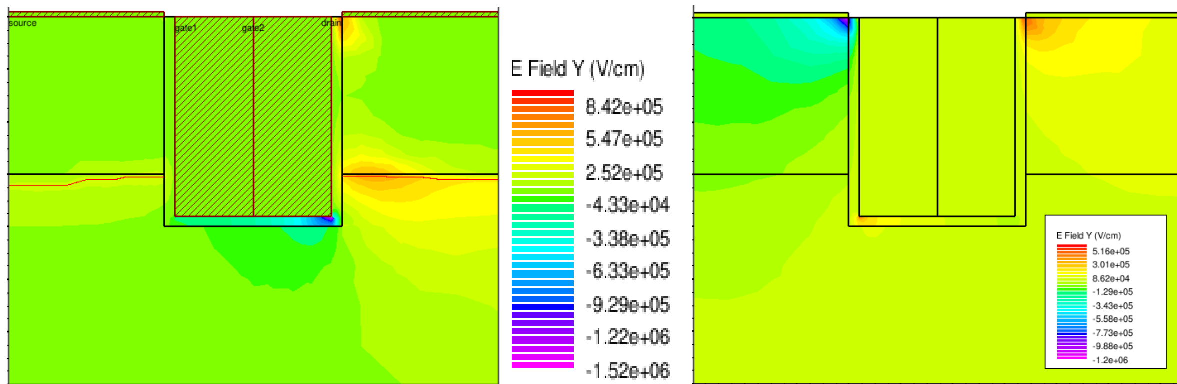
Fig.3.5 Drain Induced Barrier Lowering (DIBL) for CRC- MOSFET and TGRC-MOSFET at V_{ds}=0.5 V and V_{ds}=0.8V.

Fig.3.5 Drain Induced Barrier Lowering (DIBL) for CRC- MOSFET and TGRC-MOSFET at V_{ds}=0.5 V and V_{ds}=0.8 V. It is clearly evident that DIBL in TGRC-MOSFET is lower than CRC-MOSFET. In short-channel MOS transistors, it is known that the depletion-layer widths associated with source and drain junctions become comparable to channel length such that the potential distribution under the gate is described by a two dimensional function. The threshold voltage is strongly dependent on the potential distribution function and it tends to decrease with decreasing channel length. For submicron transistors, the threshold voltage is known to decrease linearly with the increase of drain voltage [5-7]. The main mechanism which reduces the threshold voltage is the decrease of the potential barrier in the depletion region under the gate due to the drain voltage. This effect is known as Drain Induced Barrier Lowering (DIBL).

3.2.5 ELECTRIC FIELD



(a)



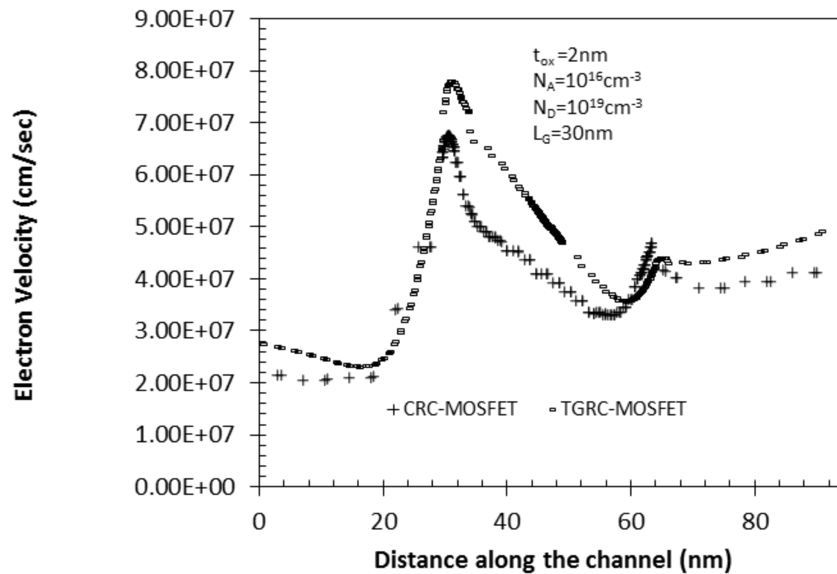
(b) **(c)**

Fig.3.6 (a) Electric field as a function of position along the channel for CRC- MOSFET and TGRC-MOSFET at L_G=30 nm, V_{ds}=0.5 V and V_{gs}=0.7 V. Electric Field profile for (b) TGRC-MOSFET (c) CRC-MOSFET.

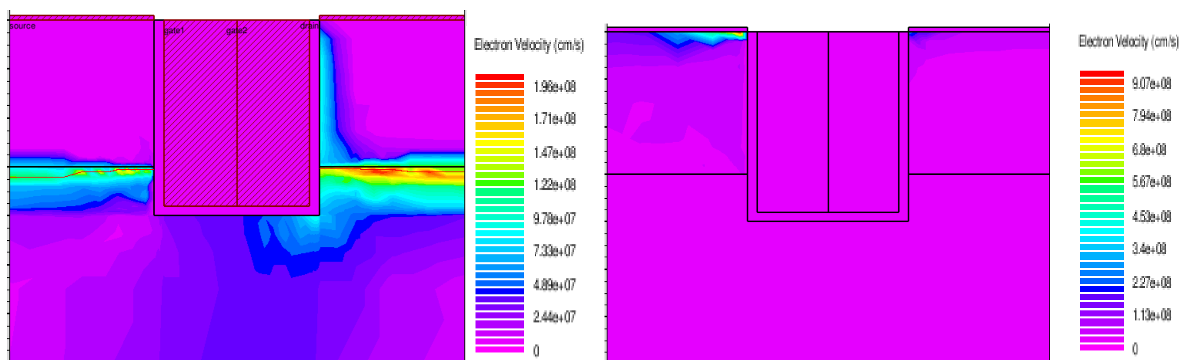
Fig. 3.6 (a) shows the variation of electric field along the channel. It can be seen that in the TGRC-MOSFET, the electric field peak near the source side is higher compared to drain side. The reduction in electric field at the drain end can be interpreted as a reduction in hot carrier effects, lower impact ionization and higher breakdown voltage. Electric field at source side is 2.00E+05 in TGRC-MOSFET and 1.50E+05 in CRC-MOSFET, and 1.80E+05 in TGRC-

MOSFET and 1.60E+05 in CRC-MOSFET at drain side. It shows the improved property in TGRC-MOSFET. Fig.3.6 (b) shows the electric field profile in TGRC-MOSFET and Fig.3.6 (c) shows electric field profile in CRC-MOSFET. Electric field profiles clearly depict that electric field at source side in TGRC-MOSFET is higher than CRC-MOSFET.

3.2.6 ELECTRON VELOCITY



(a)



(b) **(c)**

Fig.3.7 (a) Electron Velocity as a function of position along the channel for CRC- MOSFET and TGRC-MOSFET at V_{ds}=0.5 V and V_{gs}=0.7V. Electron Velocity profile for (b) TGRC-MOSFET (c) CRC-MOSFET.

Fig. 3.7 (a) shows the variation of electron velocity of TGRC-MOSFET and CRC-MOSFET along the channel. Here the electron velocity is more at source side in TGRC-MOSFET in

compare to CRC-MOSFET. As fig. 3.7 (a) shows electron velocity at drain side is lower in TGRC-MOSFET in comparison to CRC-MOSFET which reduces hot carrier effects.

Electron velocity at source side 8.00E+07 cm/sec in TGRC-MOSFET and 6.50E+07 cm/sec in CRC-MOSFET while at drain side 4.00E+07 cm/sec in TGRC-MOSFET and 4.50E+07 cm/sec in CRC-MOSFET. High electron velocity near the source manifests itself in the form of improved carrier transport efficiency. It is seen from fig.3.7(a) that in the TGRC-MOSFET structure, the electron velocity near the source end is higher and hence a higher drain current is achievable, in comparison to the conventional CRC-MOSFET, where the electron velocity near the source end is much less [4].

Furthermore the TGRC-MOSFET structure, electron velocity near the drain end is lower in comparison to the CRC-MOSFET structure. Hence, the GEWE-RC structure is less susceptible to hot electron effects. However, on decreasing the groove depth, the reduction in the corner potential barriers causes the carrier velocity to increase resulting in improved carrier transport efficiency and reduced hot electron effects. Excellent hot carrier effect immunity, exhibited by TGRC-MOSFET, is demonstrated in fig.3.7 (a). Further, increasing the drain bias significantly enhances the temperature rise in the CRC-MOSFET design, thereby adding to the hot carrier effects. The TGRC-MOSFET design, thus, provides excellent hot carrier effect immunity [8].

3.2.7 ON CURRENT

Fig.3.8 shows high ON current in TGRC-MOSFET in comparison to CRC-MOSFET which favours its pertinence in switching applications as compared to CRC-MOSFET. In Indium Tin Oxide, In_2O_3 contributes many free electrons which increases the electrical conductivity and decreases the resistivity. As a result, the electron velocity near the source side is higher in TGRC-MOSFET which magnifies the source carrier injection in to the channel. Thus, the trans- conductance and drive current of TGRC-MOSFET will be more than CRC-MOSFET [9-10]. ON current is 1.20E-05 Ampere in TGRC-MOSFET and 8.50E-06 Ampere in CRC-MOSFET which indicates that TGRC-MOSFET is more suitable for switching applications.

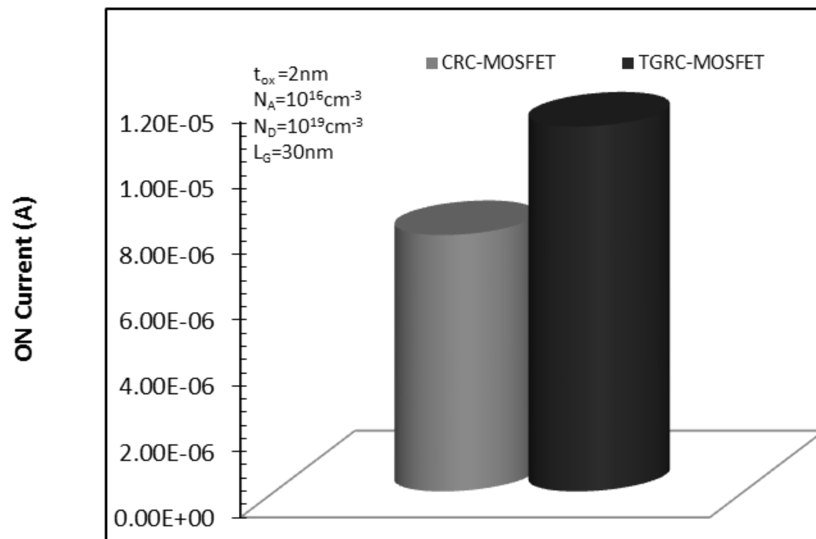
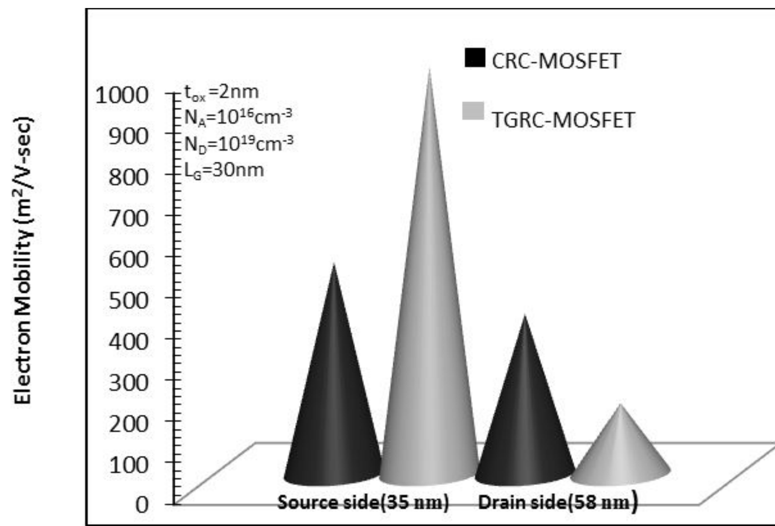


Fig.3.8 ON Current for CRC- MOSFET and TGRC-MOSFET at V_{ds}=0.5 V and V_{gs}=0.7V.

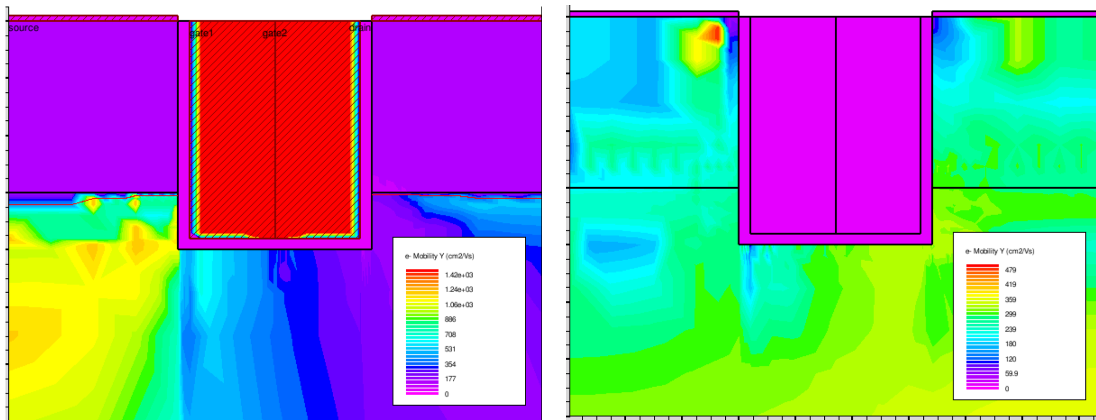
3.2.8 ELECTRON MOBILITY

Fig.3.9 (a) shows the variation of electron mobility of TGRC-MOSFET and CRC-MOSFET along the channel. Here the electron mobility is high at source side in TGRC-MOSFET in comparison to CRC-MOSFET. Fig. shows that electron mobility at drain side is higher in TGRC-MOSFET in compare to CRC-MOSFET which reduces hot carrier effects. The mobility of charge carriers in ITO thin films is largely stimulated by four scattering mechanisms: lattice scattering, ionized impurity scattering, neutral impurity scattering, and grain boundary scattering [11].

In Indium Tin Oxide, Tin Oxide creates more electrons, thereby increasing the carrier concentration and hence decreasing the mobility at drain side and increasing at source side. It is clearly evident from Fig.3.9 (b) and Fig.3.9 (c) which shows electron mobility profile for TGRC-MOSFET and CRC-MOSFET respectively, that electron mobility more in drain side and less in source side. Fig.3.9 (a) also shows that maximum value at source side is 1000 m^2/V-sec in TGRC-MOSFET and 600m^2/V-sec in CRC-MOSFET while at drain side, 400K m^2/V-sec in TGRC-MOSFET and 200m^2/V-sec in CRC-MOSFET.



(a)



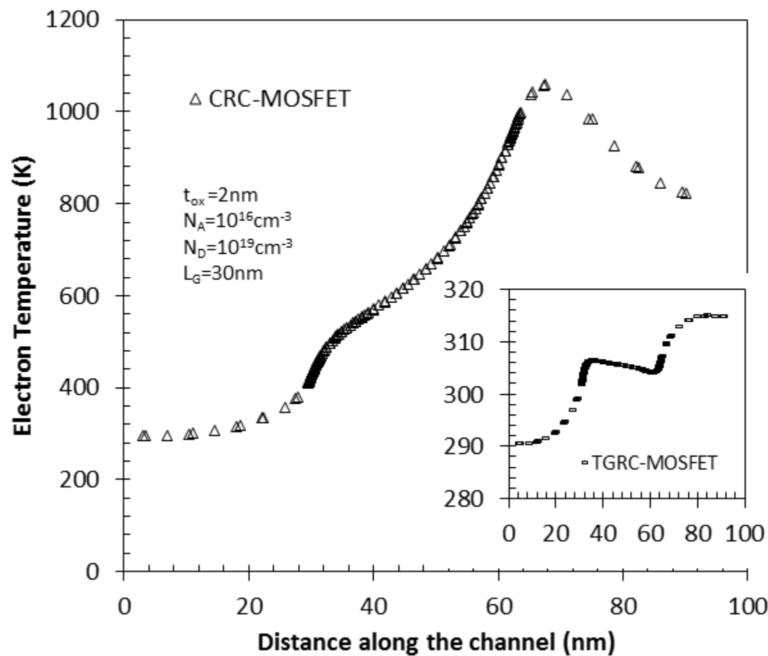
(b) **(c)**

Fig.3.9 (a) Electron mobility of TGRC-MOSFET and conventional RC-MOSFET at 35 nm and 58 nm along the channel at V_{ds}=0.5 V and V_{gs}=0.7 V. Electron Mobility profile for (b) TGRC-MOSFET (c) CRC-MOSFET.

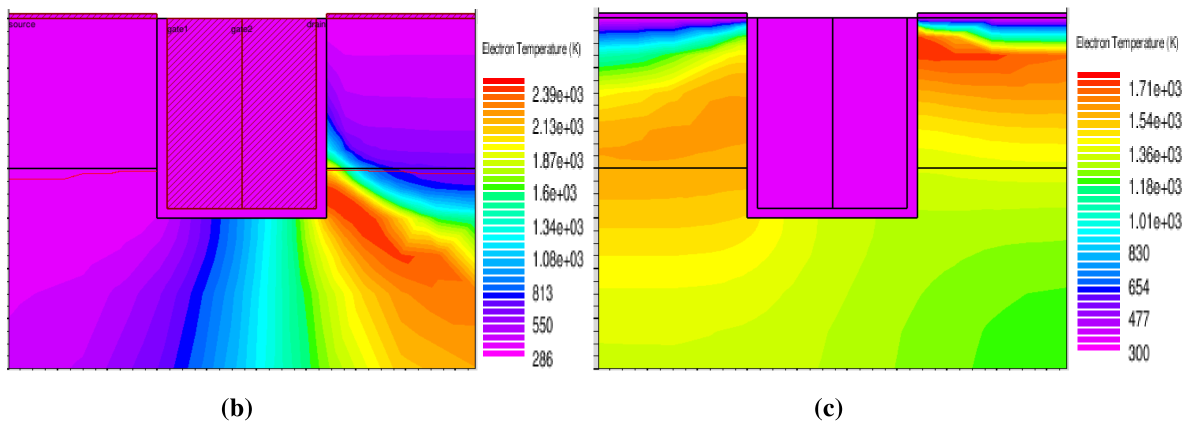
3.2.9 ELECTRON TEMPERATURE

Fig.3.10 (a) shows the variation of electron temperature across the channel length of MOSFET. High electron temperature at the drain side in CRC-MOSFET ostentation that hot carrier effect is less pronounced as compared to TGRC-MOSFET. When we use ITO as a transparent conducting material, mobility and carrier concentration is directly dependent

upon temperature. When carrier concentration increases and mobility decreases, then the increase in electron temperature is less in TGRC-MOSFET compared to CRC-MOSFET. Increase in electron temperature may cause the device damage and hot-carrier degraded performance. Maximum temperature at drain side in CRC-MOSFET is 1100K and 300K in TGRC-MOSFET as shown in Fig.3.10 (a).



(a)



(b) **(c)**

Fig.3.10 (a) Electron Temperature as a function of position along the channel for) for CRC- MOSFET and TGRC-MOSFET at V_{ds}=0.5 V and V_{gs}=0.7V. Electron Temperature profile for (b) TGRC-MOSFET (c) CRC-MOSFET.

The degradation MOSFET's due to hot-carrier (HC) injection into the gate oxide during the application of high drain voltages is most frequently evaluated by monitoring changes in the

transfer characteristics $I_D(V_G)$ or, simply, in the threshold voltage V_T or transconductance g_m [12]. However, there are other characteristics of the MOSFET which are modified by an electrical stress and thus can be used to characterize and better understand HC-induced degradation [13-14]. Fig.3.10 (b) shows the electron temperature profile in TGRC-MOSFET and Fig.3.10 (c) shows the electron temperature profile in CRC-MOSFET. It is clearly evident from potential profile that electron temperature in TGRC-MOSFET is very less in compare to CRC-MOSFET.

3.3 SUMMARY

Here we accentuate our focus on Transparent Gate architecture incorporation onto the Conventional Recessed Chanel MOSFET for improved hot-carrier reliability of scaled MOS devices. Intensive 3-D TCAD device simulations have been performed to probe the internal transport conditions of CRC MOSFET and TGRC-MOSFET, and substantial interpretation is given to the internal behaviours observed in all the devices investigated. TCAD simulation reveals the improvement in hot-carrier effects metrics such as electron velocity, potential, electron mobility and electron temperature. This work presents a TGRC-MOSFET device which is reliable for high performance application in CMOS technology.

3.4. REFERENCES

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CHAPTER 4

THERMAL BEHAVIOR OF NOVEL TRANSPARENT GATE RECESSED CHANNEL (TGRC) MOSFET: TCAD ANALYSIS

4.1. INTRODUCTION

Here we investigate the thermal analysis of Transparent Gate Recessed Channel (TGRC) MOSFET at 300K using ATLAS device simulation software. The behaviour of this device in different thermal applications such as heat sink and thermal insulation in comparison with Conventional Recessed Channel (CRC) MOSFET. Moreover, TCAD simulation shows reduction of electron temperature, heat conductivity, impact ionization substrate current and Hot Electron (HE) gate current. Short-channel effects (SCEs) result in many problems such as increases in power consumption and leakage current [1]. Hot-electron degradation is another unenviable effect of short-channel devices [2, 4]. As the scaling of transistors penetrates into the submicron regime, the electric field grows and causes electrons and holes to gain high kinetic energy, referred to as “hot carriers”. The presence of such mobile carriers in the oxides triggers numerous physical damage processes that can drastically change the device characteristics over long periods. The accumulation of damage can eventually cause the circuit to fail as key parameters such as threshold voltage shift due to such damage. The accumulation of damage resulting degradation in device behavior due to hot carrier injection is called “hot carrier degradation” [2-4].

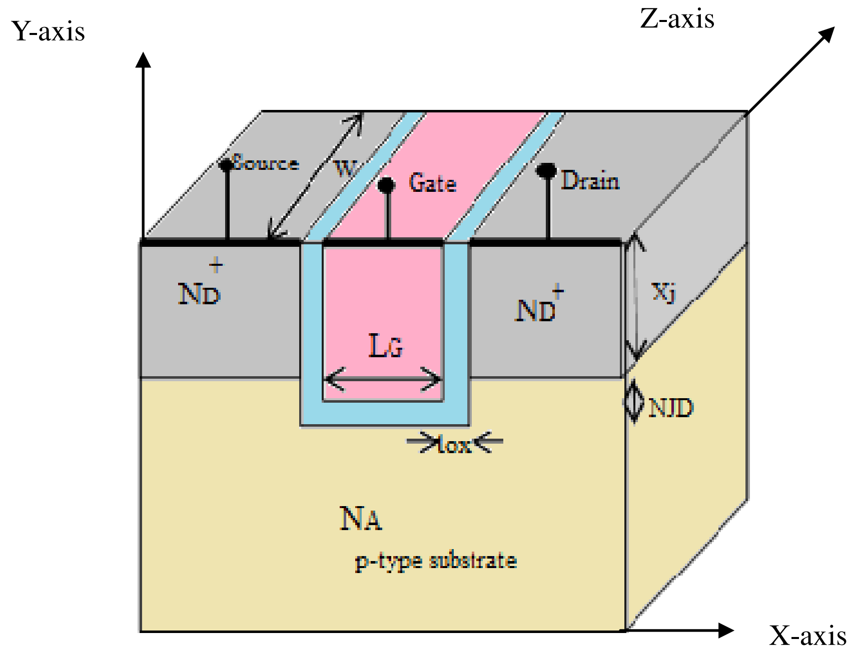

Fig.4.1 Schematic structure of Transparent Gate Recessed Channel MOSFET.

Design parameters: Gate Length L_G= 30 nm, Source/Drain junction depth (Xj) = 30 nm, Substrate doping (N_A) = 1 × 10^{16} cm^{-3}, source/drain doping, N_D^+= 1 × 10^{19} cm^{-3}, oxide thickness (t_{ox}) = 2 nm, ε_{ox}= 3.9, thermal contact temperature = 300 K, Negative Junction Depth (NJD) = 10 nm, V_{gs} = 0.7 V, V_{ds}= 0.5V. Gate workfunction of TRC-MOSFET (Φ_{ITO}) = 4.7 eV.

It is thus increasingly essential to analyse the thermal behaviour in terms of hot-electron-injected gate current, impact-ionization substrate current and temperature near the drain end for their impact on the overall chip performance [6]. Apart from the intricacy of designing devices at these sub-µm scales, the two issues of power dissipation and heat removal are supreme concerns, which have already limited the clock speed. Understanding thermal transport at the device level is increasingly important as future technology evolves toward devices with larger internal thermal resistances and higher heat generation per unit volume. However, the self-heating of thin and short SOI devices stands as a very serious problem. As the film becomes thinner, the heat path through the source/drain regions is squeezed which increases the thermal resistance and makes the transistor body temperature rise. Self-heating is responsible for performance degradation in SOI MOSFETs: mobility and threshold voltage lowering, increase in leakage current and sub-threshold swing, etc. [7–12]. As the issue of heat becomes increasingly important in deep-submicron MOSFETs, it is necessary to be able

to accurately measure and model the thermal parameters of MOSFET to fully characterize its thermal performance.

4.2 SIMULATION RESULTS OF TRANSPARENT GATE RECESSED CHANNEL MOSFET

4.2.1 HEAT CAPACITY

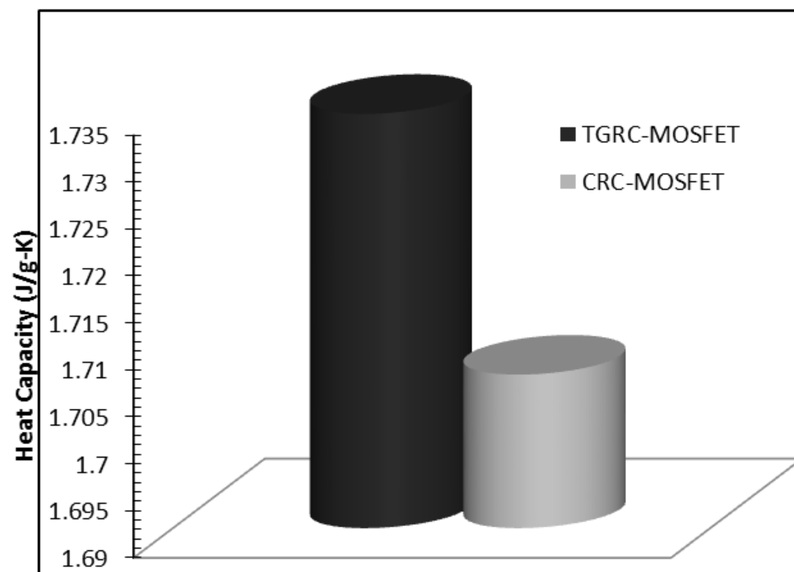

Fig.4.3 Heat Capacity of TGRC-MOSFET & CRC-MOSFET

Heat capacity or thermal capacity is the amount of heat energy required to change the temperature of a body by a given amount. Fig.4.3 shows the comparison of heat capacity of TGRC-MOSFET and CRC-MOSFET at a point along the channel. It clearly evident from Fig.4.3 that heat capacity of TGRC-MOSFET is higher than CRC-MOSFET, which favours its application in high temperature where less temperature change of a device is required when a large amount of heat is provided by surroundings.

Fig.4.4 shows the variation of heat capacity at different temperatures and it is evident that with the increase in temperature, heat capacity also increases. Heat capacity at 300K of TGRC-MOSFET is higher than heat capacity of CRC-MOSFET at 300K. When we increase temperature to 400K and 500K then heat capacity also increases. It indicates that TGRC-

MOSFET can be uses for high temperature applications. In TGRC-MOSFET, when impact ionization will occur near the drain end then increase in temperature due to hot electron will be less because increased in temperature very less in transparent conducting oxide thus the heat capacity increases.

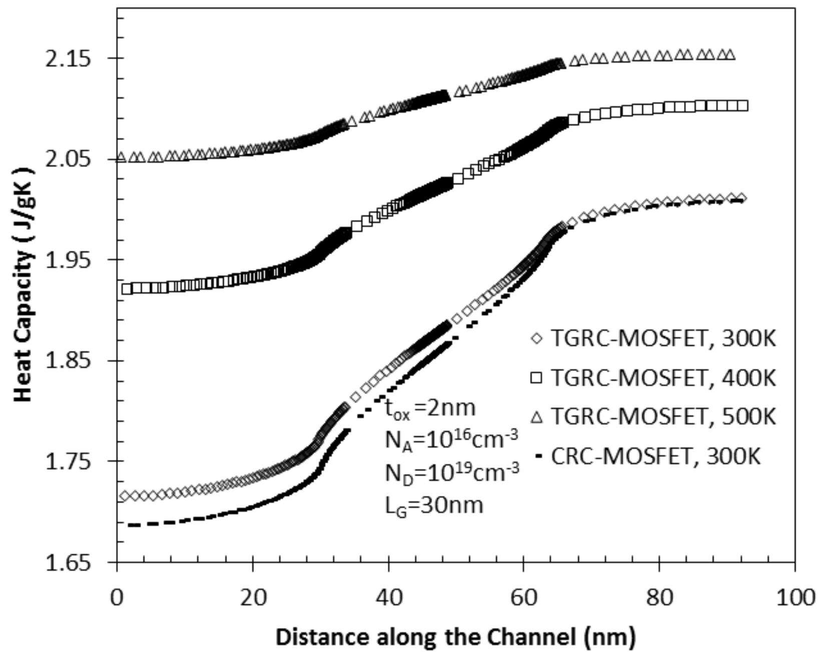

Fig.4.4 Heat capacity variation along the channel at 300K,400K,500K of TGRC-MOSFET and at 300K of CRC-MOSFET.

4.2.2 HEAT CONDUCTIVITY

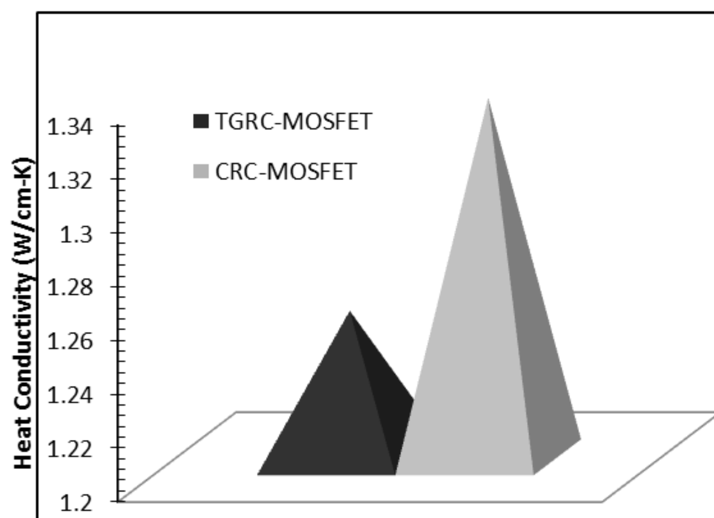

Fig.4.5 Heat Conductivity of TGRC-MOSFET & CRC-MOSFET.

Thermal conductivity is one of the most important parameter determining the efficiency of those semiconductors devices used in thermoelectric energy conversion. It is the property of a material to conduct heat. TGRC-MOSFET has low thermal conductivity in comparison to CRC-MOSFET. Lower thermal conductivity of a device, finding application as heat insulation. High and low thermal conductivity allows heat sink and heat insulation applications respectively. Effect of temperature in a transparent material is lower in comparison to normal metal because in transparent conducting oxide, flow of heat remains less with increase in charge concentration. Thus heat conductivity is low in TGRC-MOSFET.

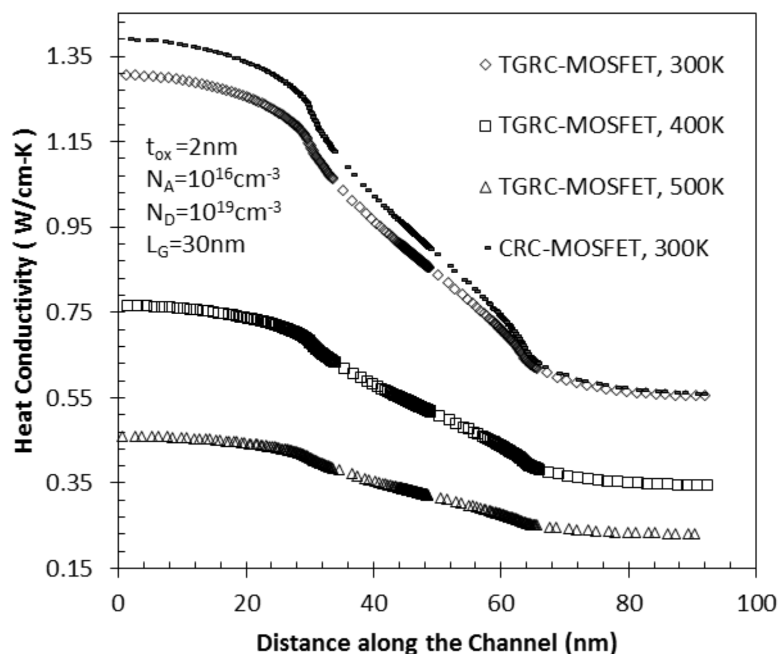

Fig.4.6 Heat Conductivity variation along the channel at 300K,400K,500K of TGRC-MOSFET and at 300K of CRC-MOSFET.

Fig.4.6 shows the variation of heat conductivity at different temperatures and it is evident that with the increase in temperature, heat capacity is decreasing. Heat conductivity at 300K of TGRC-MOSFET is lower than heat conductivity of CRC-MOSFET at 300K. When we increase temperature at 400K and 500K then heat conductivity is decreases. In any transparent conducting oxides number of free electrons is created which increase the carrier concentration and decreases the heat conductivity. Indium Tin Oxide is one of the transparent conducting materials in which more number of electrons are generated but thermal

conductivity is decreases with the increase of temperature. In TGRC-MOSFET thermal conductivity is decreases more with corresponding increasing of temperature.

4.2.3 HOT-ELECTRON INJECTED GATE CURRENT

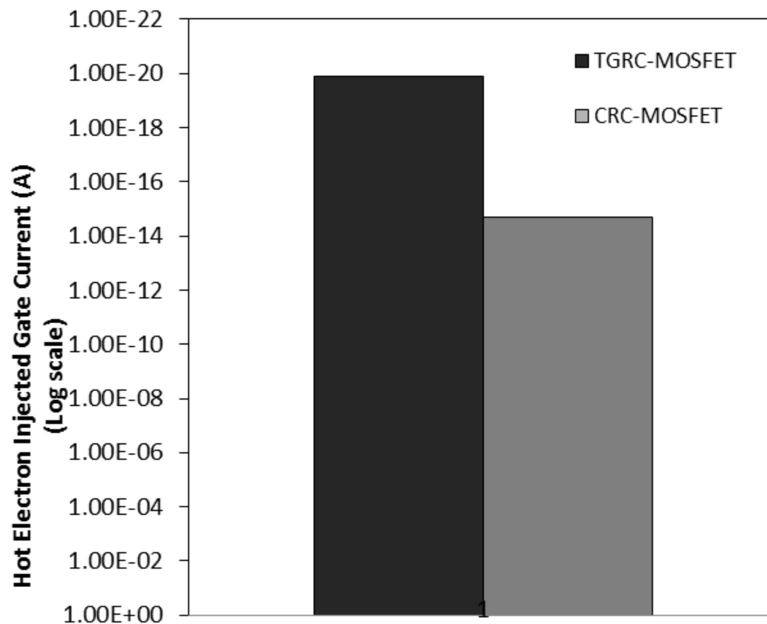

Fig.4.7 Hot Electron Injected Gate Current of TGRC-MOSFET & CRC-MOSFET

Whenever reduces the channel length is reduced keeping the supply voltage constant, the maximum electric field experienced by the carriers in the channel region near the drain end increased. As the carrier move from the source to drain, they can acquire more kinetic energy in the high field region of the drain junction so as to cause impact ionization. Some of them can even surmount the Si-SiO_2 interface barrier and enter in to the oxide. These high energy carriers that are no longer in thermal equilibrium with the lattice, and have energy higher than the thermal energy, are called hot-carriers [13]. Because these hot carriers gate current is induced, the device performance is degraded. In TGRC-MOSFET, hot-electron injected gate current is reduced in comparison to CRC-MOSFET as shown in Fig.4.7, which improves the performance of the device. In transparent conducting material, concentration of charge carriers increases then these increased charge carriers only contributed to improves drain current and very less number of charge carriers surmounted Si-SiO_2 interface because thermal effect on charge carriers in transparent conducting oxide is very less. It reveals that the gate

current induced by these hot carriers is reduces in transparent gate. ITO is a transparent conducting material which reduces these hot carriers thus hot-electron injected gate current is reduces in TGRC-MOSFET.

4.2.4 IMPACT IONIZATION SUBSTRATE CURRENT

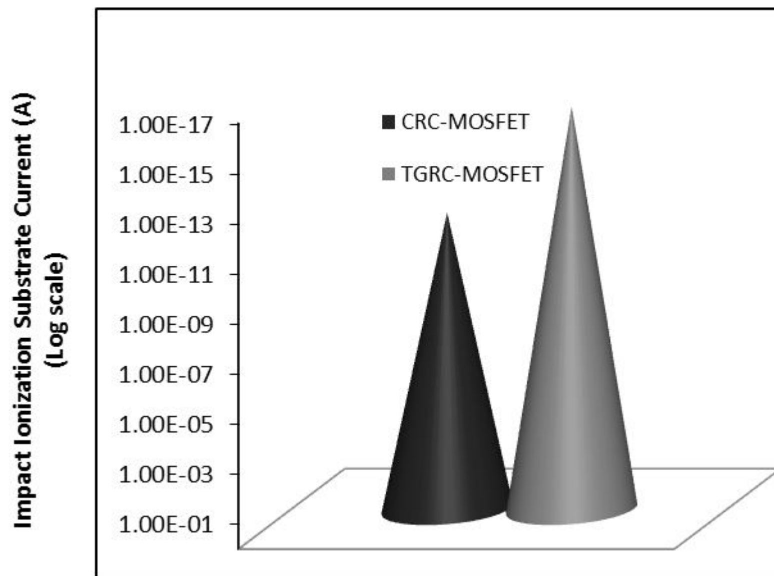

Fig.4.8 Impact Ionization Substrate Current of TGRC-MOSFET & CRC-MOSFET

When the impact ionization occurs, a primary hot-carrier will generate a secondary electron-hole pair. While the electron continue to constitute drain-to-source current, the secondary holes generated by the impact ionization drift through the substrate to the sub-contact resulting in a so called the substrate current. For better performance of a device, substrate current should be as less as possible [13]. From Fig.4.8 it is evident that impact ionization substrate current in TGRC-MOSFET is less than CRC-MOSFET which shows that thermally generated electrons are very less in TGRC-MOSFET as compared to CRC-MOSFET. In ITO, when indium oxide defused with tin, some of oxygen vacancies could be created by SnO_2 which gives free electrons, hence carrier concentration increases. When carrier concentration increases then due to impact ionization electron-hole pair generated and all these charge carriers contributed for current in device and very less number of holes come down at substrate and generates less substrate current. If substrate current is less, then the drain current will increase which increases switching speed of the device. The generation of hole current due to impact ionization leads to a significant increase in substrate current. Substrate

current thus provides a good monitor to the heating of the channel carriers and to the electric field in the drain region. Furthermore, when the MOS devices are scaled down to sub-50 nm or even lower, the substrate current increases due to deteriorated hot-carrier effects [6].

4.2.5 TOTAL HEAT POWER

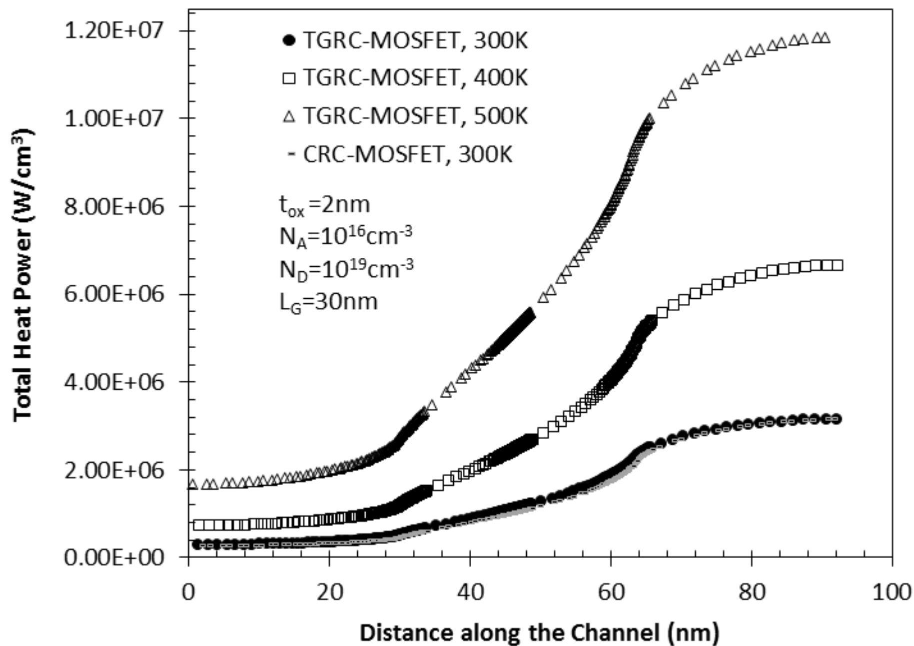

Fig.4.9 Variation of Total Heat Power along the channel at 300K,400K,500K of TGRC-MOSFET and at 300K of CRC-MOSFET.

Total heat power TGRC-MOSFET increases with temperature as compared to CRC-MOSFET as shown in Fig.4.9. It is also evident from the figure that as the temperature rises from 300K to 400K and 500K, and then the total heat power also increases because transparent materials have very good heat power. By using ITO, we improve I_{ON} which causes the decrease in device power consumption. The In_2O_3 phase itself contributes free electron for electrical conductivity [14]. In transparent material charge carriers acquire high energy at very low temperature thus these electron have more heat power compare to normal metal thus the total heat power in improves in TGRC-MOSFET as compare to CRC-MOSFET.

4.2.6 ELECTRON TEMPERATURE

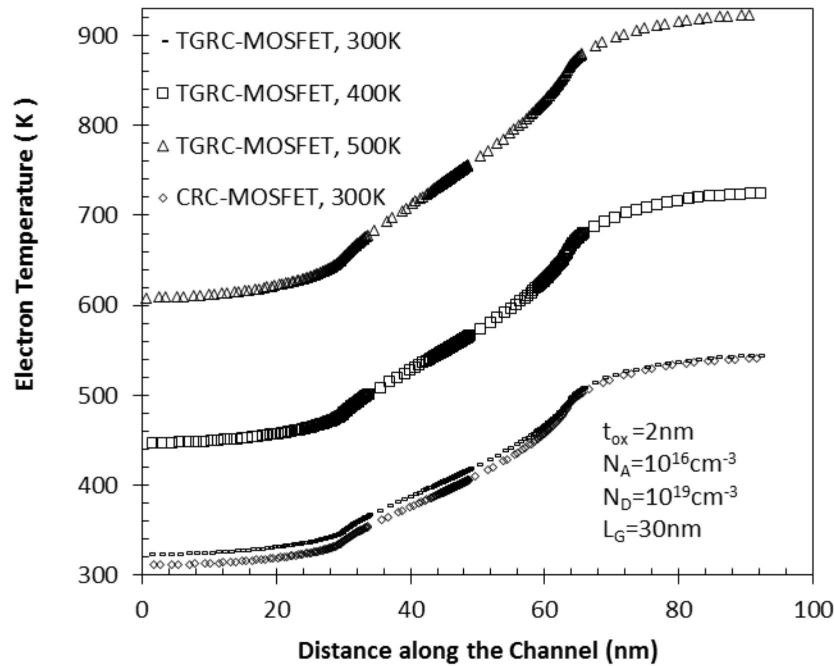

Fig.4.10 Variation of Electron Temperature along the channel at 300K,400K,500K of TGRC-MOSFET and at 300K of CRC-MOSFET.

Fig.4.10 predicts the variation of electron temperature along the channel length from source to drain for TGRC-MOSFET and CRC-MOSFET at different temperatures. As is clear from the results, an appreciable reduction in electron temperature for TGRC-MOSFET at the drain side is observed which is due to reduction in electric field at the drain side. This in turn reduces the leakage current and hence improves hot carrier immunity in comparison to CRC-MOSFET.

4.3 SUMMARY

Here we confer the thermal analysis of a novel design Transparent Gate Recessed Channel MOSFET (TGRC-MOSFET) at different temperatures. Simulation results show that performance of TGRC-MOSFET surpasses Conventional Recessed Channel (CRC)-MOSFET in terms of heat capacity, heat conductivity, lattice temperature and total heat power in comparison to CRC-MOSFET. Simulations results show there is a trade-off between TGRC-MOSFET and CRC-MOSFET for thermal applications.

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CHAPTER 5

NOISE ANALYSIS OF TRANSPARENT GATE RECESSED CHANNEL (TGRC) MOSFET

5.1. INTRODUCTION

Noise analysis is very important in many analog and RF receiver circuit design since the received signals are very weak. In case of differential amplifiers the noise appear as common mode signal and hence is rejected. However a single stage amplifier is the contribution of various circuit elements to noise must be taken into consideration. Resistors, MOSFETs and Diodes are the common sources of noise in analog circuits. In order to perform noise analysis we need to have accurate noise models for various elements used in the design. Since noise voltages and currents are small in magnitude, their influence on the circuit can be obtained through small signal analysis of the circuit. As a result, the noise voltages and currents can be added to the small signal model of the circuit. There are several different kinds of noise sources that can be found in semiconductor devices. Perhaps the most important is the Thermal Noise. Thermal noise results from random motion of charge carriers within a conductor or a semiconductor due to the presence of scattering centres. The noise in a MOSFET arises from thermal noise due to channel resistance and flicker noise component due carrier trapping at the oxide interface [1].

Scaling-down of MOS devices improves RF performance characterstics. On the other hand, it is difficult to scaledown the supply voltage used to perform these ICs consistently due to compatibility problem with earlier generation circiuts, noise margin, power and delay requirements, but not scaling of subthresold slope and thresold voltage [2]. While the successive increase in internal electric fields in aggressively scaled MOSFETs comes with the additional ameliorate of increased carrier velocities, and hence increased switching speed, it

also presents higher reliability complications for the long period of operation of these devices [3]. As the size and signal levels of a MOSFET is scale-down, the low frequency noise (LFN) properties become more important and the LNF is higher than the signals[4-5]. To abate the noise effects in CRC-MOSFET, instead of metallic gate we are using Indium Tin Oxide. Indium tin oxide (ITO or tin-doped indium oxide) is a solid solution of indium -oxide (In_2O_3) and tin oxide (SnO_2). It is transparent and colorless in thin layers. Indium tin oxide is one of the most widely used transparent conducting oxides because of its two chief properties, its electrical conductivity and optical transparency, as well as the ease with which it can be deposited as a thin film.. The In_2O_3 phase itself contributes free electron for electrical conductivity [6-8]. When Tin (Sn) is diffused, then some of the oxygen vacancies may be created by SnO_2 which creates free electrons to enhance the concentration of carriers and hence increase conductivity and decrease the resistivity with temperature. As the device scale-down, parasitic capacitances are arises. These parasitic capacitances degrade the device performance. By using TGRC-MOSFET parasitic capacitances have been reduced.

5.2. DEVICE STRUCTURE & PARAMETERS

The simulation device structure i.e. Transparent Gate Recessed Channel MOSFET consists of gate which is made by transparent conducting material Indium Tin Oxide (ITO) as shown in Fig 5.1.

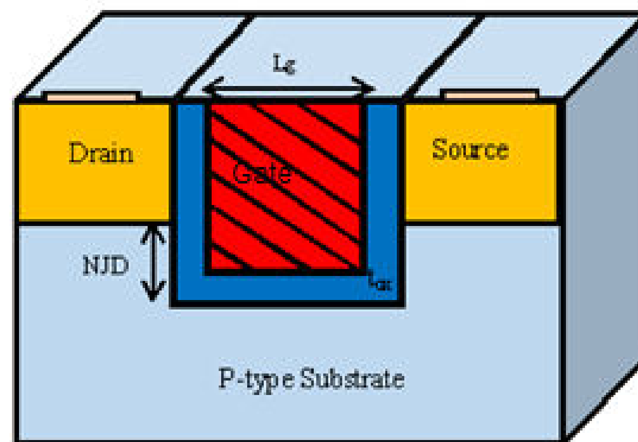

Fig.5.1 Schematic structure of Transparent Gate Recessed Channel (TGRC) MOSFET.

The total gate length is 30 nm and thickness of oxide is 2.0 nm. In this case, substrate doping is p-type with concentration of $1\times10^{17}cm^{-3}$; source and drain are n-type with uniform doping profiles is $1\times10^{19}cm^{-3}$. Groove depth is 38 nm and source/drain junction depth is 30 nm. Here we had taken negative junction depth 10 nm. Gate to source and drain to source voltage is 0.7

V. Workfuntion is taken for transparent material is 4.7 eV in TGRC-MOSFET and 4.1 eV for metal in CRC-MOSFET. All simulations have been performed using ATLAS device simulator. In gate electrode, we are replacing metal gate by transparent conducting material ITO, but source electrode and drain electrodes are remain metal. Bias voltage V_{gs}=0.7 V and V_{ds}=0.7 V are applied. Activated models comprise the inversion layer Lombardi CVT mobility model with the Auger recombination model and Shockley-Read –Hall (SRH) for minority carrier recombination. After that we enable the hydrodynamic energy transport model which also comprises the continuity equations, energy balance equations of the carriers, momentum transport equations and Poisson's equation [9].

5.3 COMPUTER SIMULATION RESULTS OF TRANSPARENT GATE RECESSED CHANNEL MOSFET

5.3.1 MINIMUM NOISE FIGURE

The present analysis is carried out for a channel length, L_G=30nm, uniformly doped source/drain, N_D with doping density of 1×10^{19} cm^{-3}, p type substrate doping, N_A with a doping density of 1×10^{17} cm^{-3}, SiO_2 thickness, t_{ox}=2.0 nm. The gate work function (Φ_{ITO}) is 4.7 eV.

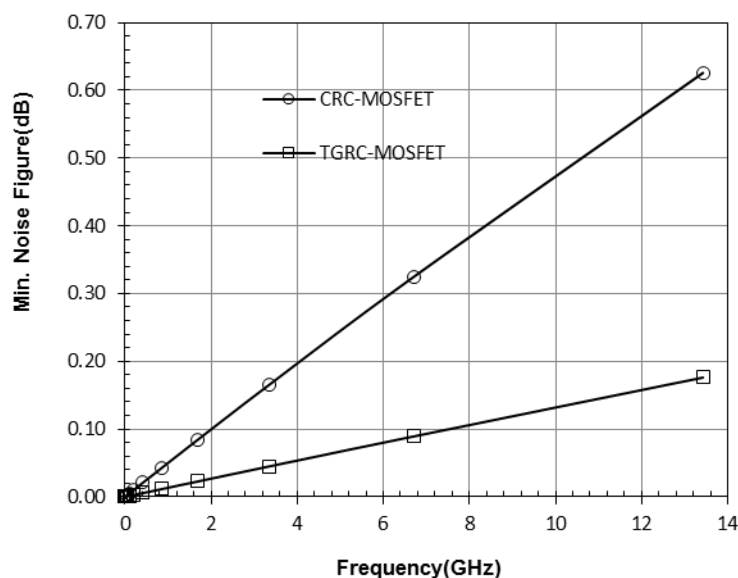

Fig.5.2: Minimum noise figure for CRC- MOSFET and TGRC-MOSFET.

Noise figure is generally used as a measure of an amplifer's RF performance. Fig.5.2. shows the minimum noise figure for CRC-MOSFET and TGRC-MOSFET at different frequencies. When frequency increases from 100 Hz to 10 GHz, minium noise figure decreses in TGRC-MOSEFT compared to CRC-MOSFET.

At higher frequencies the value of NF min for both the devices is almost the same. This observation can be mainly attributed to the work function difference of the gates in the GEWE-RC architecture, due to which a step-potential is introduced in the channel. There exists a screening of the channel region from the drain induced variations due to which the number of carriers entering the channel remains comparatively less varied [10]. Also, the vertical electric field is reduced due to which the trapping of the carriers near the Si-SiO2reduces, which results in the improved carrier transport efficiency.

5.3.2 OPTIMUM SOURCE IMPEDANCE (Z_0)

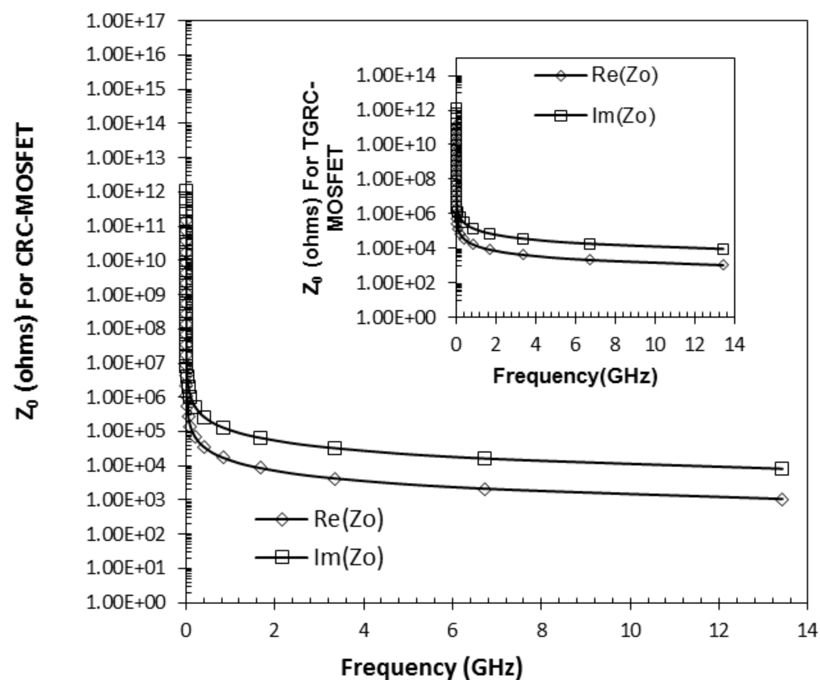

Fig.5.3: Optimum source impedance Z_0 for CRC- MOSFET and TGRC-MOSFET.

Fig.5.3. predicts the behavior of optimum source impedance ($Z_{OPT}=R_{OPT}+jX_{OPT}$) with respect to frequency. When the frequency increases, optimum impedance decreases in CRC-

MOSFET while it is maximum at low frequencies. As evident from Fig.5.3, the optimum source impedance in TGRC-MOSFET is slightly higher than CRC-MOSFET because of the presence of indium tin oxide in TGRC-MOSFET which is effectively acting as a parallel oxide with SiO_2 and hence effective permittivity is increased which eventually leads to increase in input impedance. This high impedance of TGRC-MOSFET also helps in reduction of electrostatic charges, which basically comes in to existence with scale-down of oxide [11]. As the oxide thickness is being continuously shrunk due to the scaling of the MOSFET, the MOSFET should have a large source impedance to avoid destruction by electrostatic charges. In the Fig.5.3 it can be vividly seen that optimum impedance for TGRC MOSFET is much higher than that of the CRC-MOSFET.

5.3.3 PARASITIC CAPACITANCES

Fig.5.4. show the parasitic capacitances for CRC-MOSFET and TGRC-MOSFET and it is clearly divulged that reduced parasitic capacitances are observed in TGRC-MOSFET as compared to CRC-MOSFET. In addition, for better performance of a device in microwave-communication, parasitic capacitances should be as small as possible.

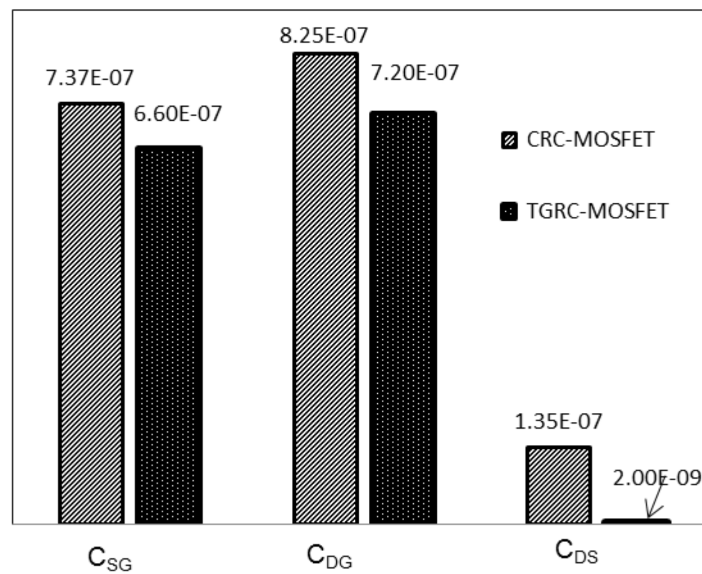

Fig.5.4: Parasitic capacitance (fF) of source to gate (C_{SG}), drain to gate (C_{DG}) and drain to source (C_{DS}) for CRC- MOSFET and TGRC-MOSFET.

Local stress on the radio-frequency (RF) performance of the transistor and parasitic capacitances are investigated in 30-nm CMOS technology [12]. Parasitic capacitances and

resistance put upper limit on the speed of a transistor [13]. Parasitic capacitance is the cause of delay in logic-cell. When one logic cell drives another, the parasitic input capacitance of the driven cell becomes the load capacitance of the driven cell [14]. Fig.5.4 shows that the parasitic capacitances in TGRC-MOSFET are less than the CRC-MOSFET. The ITO-SiO_2 forms a MOS capacitor with ITO serving as metallic gate electrode at GHz frequencies and SiO_2 forming the gate insulator [15].

5.3.4 NOISE CONDUCTANCE

Noise conductance in TGRC-MOSFET is less as compare to CRC-MOSFET as shown in Fig.5.5. In the RF applications of a MOS device noise, conductance should be low as much as possible. In TGRC-MOSFET noise conductance is low because in transparent conducting material mobility is decreases with increase of concentration of charge carriers due to increase in temperature.

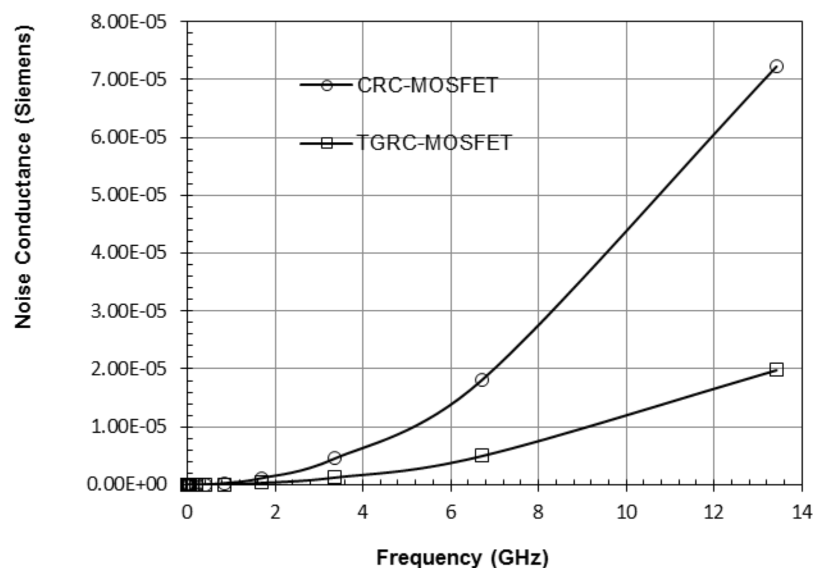

***Fig.5.5: Noise conductance for CRC- MOSFET and TGRC-MOSFET**.*

Further, in the RF applications of a MOS device, noise conductance should be as low as possible. In a MOS device, noise conductance increases due to thermally generated charge carriers. In TGRC-MOSFET, noise conductance is low because in transparent conducting material, oxygen vacancies created by oxides give more free electrons and hence, mobility decreases with increase in the concentration of charge carriers, leading to lesser number of thermally generated charge carriers as is shown in Fig.5.5 [16].

Spectral density of a noise current generator is measured in conductance units at a specified frequency. It can be seen from Fig.5.5 that the noise conductance for TGRC-MOSFET is less than that of CRC-MOSFET. This can be mainly attributed to the lower DIBL in the TGRC structure incorporated along with RC in GEWE-RC MOSFET.

5.4 SUMMARY

The noise assessment of Novel Transparent Gate Recessed Channel MOSFET has been investigated based on the simulated result from ATLAS device simulation. TCAD simulation results show TGRC-MOSFET divulges Conventional Recessed Channel (CRC)-MOSFET in terms of reduction in noise figure, noise conductance and parasitic capacitances. It also achieves higher optimum source impedance for high performance applications where noise immunity is a key factor. Here we accentuate our focus on Transparent Gate architecture incorporation onto the Conventional Recessed Channel MOSFET for superior noise performance of scaled MOS devices. Intensive TCAD device simulations have been performed to probe the internal transport conditions of CRC MOSFET and TGRC-MOSFET, and substantial interpretation is given to the internal behaviors observed in all the devices investigated. TCAD simulation reveals the deterioration in minimum noise figure, noise conductance and parasitic capacitances. It also achieves higher optimum source impedance. This work presents a TGRC-MOSFET device which is reliable for RF applications and CMOS technology for the designing of multi-gigahertz communication circuits.

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CHAPTER 6

CONCLUSION, PERSPECTIVE & FUTURE RESEARCH

6.1. SUMMARY OF CONTRIBUTIONS

The MOSFETs that are available today perform the same function as bipolar transistors except the former are voltage controlled in contrast to the current controlled bipolar devices. Today MOSFETs owe their ever-increasing popularity to their high input impedance and to the fact that being a majority carrier device, they do not suffer from minority carrier storage time effects, thermal runaway, or second breakdown. As the future size of semiconductor device has been pushed in to smaller dimensions, the problem of physical device modelling has been become increasingly more difficult and various short channel effects become more significant which can no longer be neglected. Among all the major short channel effects which affect the device characteristics most are punch-through, drain induced barrier lowering (DIBL) and threshold voltage roll-off. These effects are mainly comes in to the existence because of drain potential extension in to the source region, resulting the barrier lowering [1].

In order to reduce these short channel effects, a recessed channel structure can be taken as a potential candidate who not only reduce the impact of drain potential over the channel but also improves the gate control because of its negative junctions which can be fabricated without any increase in series resistance. The other advantages of this structure is the high packing density due to the large effective channel length with respect to gate length because the junction depth are less than the groove depth which reduces the impact of short channel

effects even at shorter gate lengths [2]. While the successive increase in internal electric fields in aggressively scaled MOSFETs comes with the additional ameliorate of increased carrier velocities, and hence increased switching speed, it also presents higher reliability complications for the long period of operation of these devices. As devices are scaled down, the benefits of higher electric fields saturate while the associated reliability problems get worse. The presence of large electric fields in MOSFETs implies the presence of high energy carriers, referred as “hot-carriers”, in such devices. The presence of this kind of mobile carriers in the oxide creates some physical damages which may change device characteristics for a long time. The aggregation of damage can ultimately be the reason of circuit failure . The aggrigation damage of the hot carrier results in deterioration in device behavior. The need of superior performance of ICs has led to the scaling of MOSFETs down to 30 nm and below [3].

Moreover, as a result of scale-down process, hot carriers effects have also become one of the serious problems. A fraction of these electrons trapped in the gate oxide which may produce net trapped charge that can reason of local shift in threshold voltage and hence, need to be minimized. Furthermore, the structure, i.e. TGRC-MOSFET, considered in this study consists of two potential barrier forms at the corner which plays the most important role in the improvement of shift in threshold voltage but on the other side, electron requires more energy to surmount these barriers which in turn results in reduced carrier transport efficiency of the device. Thus in order to mitigate hot electron effect and to increase carrier transport efficiency transparent gate architecture has been implemented on to the present device. Transparent Gate Recessed Channel MOSFET consists of gate which is made by transparent conducting material Indium Tin Oxide (ITO). Indium tin oxide (ITO or tin-doped indium oxide) is a solid solution of indium oxide (In_2O_3) and tin oxide (SnO_2) [4]. It is transparent and colourless in thin layers. Indium tin oxide is one of the most widely used transparent conducting oxides because of its two chief properties, its electrical conductivity and optical transparency, as well as the ease with which it can be deposited as a thin film. By using ITO, we improve I_{ON} which causes the decrease in device power consumption. The In_2O_3 phase itself contributes free electron for electrical conductivity [5].

In the present thesis, an attempt has been made to address the issue such as short channel length, hot carrier effects, punchthrough and degradation in current drive related with the various level device structure presented in the dissertation for sub-100 nm regime. Moreover, in order to help the TCAD engineer to advice accurate computer simulation, and develop

improved device design for mixed-mode applications, the thesis accounted for the several aspects of mixed mode performance; hot carrier reliability and thermal behaviour; noise analysis; transparent gate recessed channel MOSFET. This chapter summarizes the contribution of this thesis and finally comes potential areas for future research work have been identified and listed later.

Chapter-1 provides brief overview of MOSFET and need of MOSFET and then the introduction of CRC-MOSFET. Hence it sets the background for the present work. *Chapter-2* gives overview of different transparent oxides. They are usually prepared with thin film technologies and used in opto-electrical apparatus such as solar cells, displays, opto-electrical interfaces and circuitries. Transparent conducting oxides are highly flexible intermediate states with both these characteristics. Their conductivity can be tuned from insulating via semiconducting to conducting as well as their transparency adjusted.

Chapter-3 present a novel device structure called Transparent Gate Recessed Channel MOSFET (TGRC-MOSFET) to alleviate the hot carrier effects for the advanced nanometer process. TGRC-MOSFET involves a recessed channel and incorporates Indium Tin Oxide as a transparent gate. TCAD analysis shows that the performance of TGRC-MOSFET surpasses CRC-MOSFET in terms of high I_{ON}/I_{OFF} ratio and better carrier transport efficiency as compared to CRC-MOSFET. This simulation divulges the reduction in hot-carrier-effects metrics like electron velocity, electron temperature, potential, and electron mobility.

All the simulations have been done using DEVEDIT-3D and ATLAS device simulator. Here we accentuate our focus on Transparent Gate architecture incorporation onto the Conventional Recessed Chanel MOSFET for improved hot-carrier reliability of scaled MOS devices. Intensive 3-D TCAD device simulations have been performed to probe the internal transport conditions of CRC MOSFET and TGRC-MOSFET, and substantial interpretation is given to the internal behaviours observed in all the devices investigated. TCAD simulation reveals the deterioration in hot-carrier effects metrics such as electron velocity, potential, electron mobility and electron temperature. This work presents a TGRC-MOSFET device which is reliable for high performance application in CMOS technology.

Chapter-4 represents thermal analysis of novel design TGRC-MOSFET at 300K. Simulation results show that the performance of TGRC-MOSFET surpasses CRC-MOSFET in terms of heat capacity, heat conductivity, lattice temperature and total heat power in comparison to CRC-MOSFET. Indium tin oxide (ITO or tin-doped indium oxide) is a solid

solution of indium oxide (In_2O_3) and tin oxide (SnO_2). It is transparent and colourless in thin layers. Because of its two key properties, i.e. electrical conductivity and optical transparency, indium tin oxide is used as one of the most widely used transparent conducting oxides. Also, the In_2O_3 phase itself contributes free electron for electrical conductivity. Furthermore, with the reduction in transistor size, intrinsic self-heating effects have become unfavourable in low power applications. As the issue of heat becomes increasingly important in sub-micron MOSFETs, it becomes increasingly more important to accurately measure and model its thermal parameters to fully characterize its thermal performance.

Chapter-5 represents noise analysis of TGRC-MOSFET. Here we accentuate our focus on noise performance of TGRC-MOSFET over rather scaled MOS devices. Intensive TCAD device simulations have been performed to probe the internal transport conditions of CRC MOSFET and TGRC-MOSFET, and substantial interpretation is given to the internal behaviours observed in all the devices investigated. TCAD simulation reveals the improvement in minimum noise figure, noise conductance and parasitic capacitances. It also achieves higher optimum source impedance. This work presents a TGRC-MOSFET device which is reliable for RF applications and CMOS technology for the designing of multi-gigahertz communication circuits.

6.2. RECOMMENDATION FOR FUTURE WORK

Replacing the gate metal with transparent conducting material (ITO) improves device efficiency and reduces short channel effects hence it has future in photovoltaic applications such as solar cell, flat panel display etc. Furthermore, linearity performance and high frequency RF analysis of TGRC-MOSFET can also be done.

This work can be further extended by performing analytical modelling of TGRC-MOSFET in terms of threshold voltage, drain current etc. to verify the simulated results as described in this dissertation. In addition, hot-carrier and thermal analysis can also be extended by performing parameter variation such as gate length, negative junction depth, oxide thickness etc. Moreover the effect of interface trap charges present mainly near the drain side can also be studied to analyse device reliability.

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