DESIGN OF SINGLE PHASE AND THREE PHASE CASCADED MULTI LEVEL INVERTERS

DISSERTATION
SUBMITTED PARTIAL FULFILLMENT OF THE
REQUIREMENTS
FOR THE AWARD OF THE DEGREE
OF

MASTER OF TECHNOLOGY
IN
CONTROL AND INSTRUMENTATION

Submitted by

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CANDIDATE DECLARATION

I, BHOGESWARA RAO ANGARA, Roll No. 2K13/C&I/03 student of M. Tech. (CONTROL AND INSTRUMENTATION), hereby declare that the dissertation/project titled **"Design of Single phase and Three phase Cascaded Multilevel Inverters"** under the supervision of Dr. Madan Mohan Tripathi, Department of Electrical Engineering, Delhi Technological University in partial fulfillment of the requirement for the award of the degree of Master of Technology has not been submitted elsewhere for the award of any Degree.

Place: Delhi

Date: 25.06.2015

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CERTIFICATE

This is to certify that the dissertation/Project entitled **"Design of Single phase and Three phase Cascaded Multilevel Inverters"** being submitted by Bhogeswara Rao Angara in partial fulfillment of the requirements for the degree of Master of Technology in Control and Instrumentation at DTU is an authentic record of the work carried out by him under my supervision and guidance.

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ACKNOWLEDGEMENT

I am highly grateful to the Department of Electrical Engineering, Delhi Technological University (DTU) for providing this opportunity to carry out the project work.

The constant guidance and encouragement received from Dr. M. M. TRIPATHI of Department of Electrical Engineering, DTU, has been of great help in carrying my present work and is acknowledged with reverential thanks.

I would like to express my thankfulness to PROF. MADHUSHUDAN SINGH and Dr. DHEERAJ JOSHI for providing the laboratory and other facilities to carry out the project work. Again, the help rendered by DR. M. M. TRIPATHI, for the literature, and for experimentation is greatly acknowledged.

Finally, I would like to expresses gratitude to other faculty members of Electrical Engineering Department, DTU for their intellectual support throughout the course of this work.

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ABSTRACT

Multilevel Inverters (MLI) have received significant attention in recent times. Reduced distortion, better output power quality, minimum switching losses, reduced switching stress make multilevel architecture suitable for a variety of applications. Till date multilevel inverters are widely used in UPS (un-interruptible power supply), renewable energy systems, medium voltage industrial (induction motor) drives and many more. An extensive study and research is being carried out to design multilevel inverters for advanced industrial applications as well as efficient utilization and storage of renewable energy. A variety of control mechanisms (PI, Fuzzy, Hysteresis bands etc.) and switching/modulation techniques (SPWM, SVM, Selective harmonic elimination, wavelet modulation) have been proposed and demonstrated across the world. Our work deals with design and analysis of various control techniques for single phase and three phase MLI.

In our work we demonstrated multilevel inverter systems following Generalized Proportional Integral (GPI) control mechanism. The design of the system is based on cascade H-bridge architecture. The cascade H-bridge architecture eliminates the problems observed with other architectures such as Diode Clamped and Flying Capacitor. We designed a single phase MLI and also a three phase MLI.

Feedback is an important facet in the design of closed loop systems. Typical feedback in an inverter would be voltage or current or both. In our work we designed MLI using current feedback and voltage feedback independently. Each model is designed for a 7-level inverter following single phase and three phase. The switching scheme for these designs follows SPWM (Sinusoidal Pulse Width Modulation) technique. This makes the system less complex and easy to implement.

Major limitation on the design of cascaded MLI is the number of switches required. To resolve this limitation and a novel design method was proposed. The proposed technique based on H-bridge. This design also reduces the number of DC voltage sources, each having different magnitudes of voltage and number of power electronic switches.

This proposed model has been designed for 7-level, 9-level, 15-level and 31-level inverters. All the multilevel systems are simulated using MATLAB Simulink. The loads for single phase MLI are taken as R-L load. The MLI design for reduced power electronic devices (switches, DC voltage Sources) is simulated for R-L load. The Total Harmonic Distortion for each system has also been studied from simulation results.

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LIST OF ABBREVIATIONS

PWM	- Pulse Width Modulation
SPWM	-Sinusoidal Pulse Width Modulation
UPS	-Un Interruptible Power Supply
HVDC	-High Voltage Direct Current
FACTS	- Flexible AC Transmission
THD	-Total Harmonic Distortion
FFT	-Fast Fourier Transform
DC	-Direct Current
VS	-Voltage Source
VSI	-Voltage Source Inverter
CSI	-Current Source Inverter
IGBT	-Insulated Gate Bipolar Transistor
IGCT	-Insulated Gate Commutated Thyristor
GTO	- Gate Turn-off Thyristor
EMC	-electromagnetic compatibility
SVM	-Space Vector Modulation
WM	-Wavelet Modulation
PI	-Proportional Integral
GPI	-Generalized Proportional Integral

NPC	- Neutral point clamped converter
FCMLI	-Flying Capacitor Multilevel Inverters
DCMLI	-Diode clamped Multilevel Inverters
CMLI	-Cascade Multilevel Inverters
SHE	-Selective Harmonic Elimination
DSP	-Digital Signal Processor
FPGA	-Field Programmable Gate Array

CHAPTER 1

INTRODUCTION

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INTRODUCTION

Power electronics are playing a vital role in efficient electrical energy from source to load i.e. conversion of electrical energy from one form to another in an efficient and robust manner for proper utilisation. There are tremendous applications of power electronics in the area of industrial fields, energetics, residential appliances, commercial and business fields, telecommunications, medicines, aeronautics, military domain and electric utility systems.

Power electronic devices are drawing more attention in recent days especially in power systems. They offer better flexibility and power flow control making them efficient for small scale to large scale power systems. The gate pulses and firing angle play a vital role in design, development and implementation of these power systems.

The power electronic devices are primarily controlled by using gate pulses or controlling gate signal. An efficient power system requires a better switching scheme design. If the

switching scheme is poor, it degrades the output power quality. Several parameters should be taken into account for the design. Important factors to be considered are Root Mean Square (RMS) values of output current and voltage, harmonic distortion, losses due to switches (ON/OFF time of switches), peak values of current and voltage, average values of current and voltage and practical implementation of the system.

A variety of components are involved in the design of power electronic systems. Few such components are MOSFET, IGBT, DIODE, Thyristor, GTO, SMPS etc. Firing angle of these components controls the state of these components and hence the power electronic systems.

For the past three decades, enormous research and development is being done and has found many applications in various fields. Inverters are used to convert DC power to AC power at desired frequency and voltage. Inverters are used in many applications such as un-interruptible power supply (UPS), Medium voltage Industrial (induction motor) drives, ship propulsion Induction heating high voltage direct current (HVDC) power transmission, wind

Energy System or grid connected photovoltaic system ([1]-[2]), railway locomotives, active filters, and applications of power system for example flexible AC transmission (FACTS).

1.1. Classical Inverters

Classical inverters can be built by connecting devices in series. Typical classical inverters are efficient for low power applications but fail to satisfy high power applications. Classical inverters exhibit various drawbacks such as

a. High DC voltage across each switch in OFF state
b. Static sharing
c. Dynamic sharing
d. May damage motor insulation due to large step voltage (Two level output)
e. Higher distortion

Despite these drawbacks classical inverters offer the following advantages

a. Design involves standard Pulse width modulation technique
b. Less number of power electronic components
c. High reliability
d. Adding devices in series is easier resulting in redundancy of system

1.2. Multilevel Inverters

Total harmonic distortion (THD) [3] is an important parameter associated with every inverter (including multi-level) and is ideally desired to be almost zero. Multi-level cascaded inverter reduces the total harmonic distortion, switching stress on devices, electromagnetic compatibility (EMC) and produce high power ratings of the output current and voltage. All these applications use devices MOSFET's, Insulated Gate Bipolar Transistor (IGBT), Insulated Gate Commutated Thyristor (IGCT), Gate Turn-off Thyristor (GTO) etc.

Multilevel cascaded inverters [4] are used mainly to achieve quality improvement of output voltage signal [5]. Typical cascaded multi-level inverter needs 'n' DC sources to generate (2n+1) levels of output for each phase. Consequently, a five level inverter generates five output voltage levels with two DC voltage sources and a seven level Inverter generates seven output voltage levels with three DC voltage sources.

Multiple DC voltage sources can be designed using active elements like batteries, capacitors, any renewable energy voltage sources. Although high output voltages can be made possible by power semiconductor switches, the rated voltages depend only on the connected DC sources. Different multilevel cascaded inverter topologies have been developed such as cascaded H-bridges inverter with diode clamped multilevel inverter, separate DC sources and flying capacitor multilevel inverter etc.

1.3. Modulation Techniques

There exist different modulation techniques available to generate control pulses such as

a. Sinusoidal Pulse Width Modulation (SPWM) [6]
b. Space Vector Modulation (SVM)
c. Wavelet Modulation (WM)
d. Selective Harmonic Elimination
e. Harmonic orientation of pulse width modulation

1.4. Controllers

A variety of feedback controls and switching techniques are available to reduce the total harmonic distortion in cascaded multi-level inverter with unequal DC voltage sources. Proportional Integral (PI) controller technique [7] is widely used to regulate DC signal since it can reduce the steady state error. In proportional integral controller the integral term improves the tracking by reducing the instantaneous error between the actual and reference signal and hence improves the system stability, reduces the offset and yields faster response. It is used in the control of flow, level and pressure etc.

Other control methods available for inverters include systems based on hysteresis bands (higher efficiency, low cost), Pulse Width Modulation (PWM) controller [8] (higher efficiency, more reliable and prolong battery drain of time) and fuzzy controller (easy to implement and flexible), GPI (Generalized Proportional plus Integral) controller [9] (an efficient solution for robustness problem).

CHAPTER 2

LITERATURE SURVEY

CHAPTER 2

LITERATURE SURVEY

2.1. Inverters:

The inverters are power conditioning device that converts from DC (voltage or current) to AC (voltage or current) at desired frequency and amplitude. The DC sources are battery bank, capacitors etc. Based on input DC source there are two types of inverters namely voltage source inverter (VSI) and current source inverter (CSI).

2.1.1. Voltage Source Inverter (VSI):

If the input DC source is voltage source then the inverter is voltage source inverter (VSI).The output voltage is constant mostly irrespective of load, because of this property of voltage source inverters are mostly used in industrial applications such as power systems, adjustable induction motor drives.

2.1.2. Current Source Inverter(CSI):

In this type of inverter the output is AC current waveform. i.e. If the input is DC current source and it is generating ac output current wave form. These inverters are mostly used in medium voltage applications. Using these inverters, the high quality wave form is obtained.

2.2. Single phase inverter (VSI):

Dual polarity voltage (positive and negative) with one directional current flow can be obtained using single phase inverter. The two arms of single phase inverter consist of two switches each with antiparallel diodes across each switch for reverse current discharge. The schematic of single phase full bridge inverter is shown in Figure 2.1. The switches are S1, S2, S3, S4. The switches in each arm can't be operate in same mode simultaneously. The dead beat time is required to avoid short circuiting. By implementing different switching time of switches, the output voltage can shift from one level to another level. The switching states of single phase inverter are shown in TABLE 2.1. The switching scheme for single phase inverter can be implemented by using PWM.

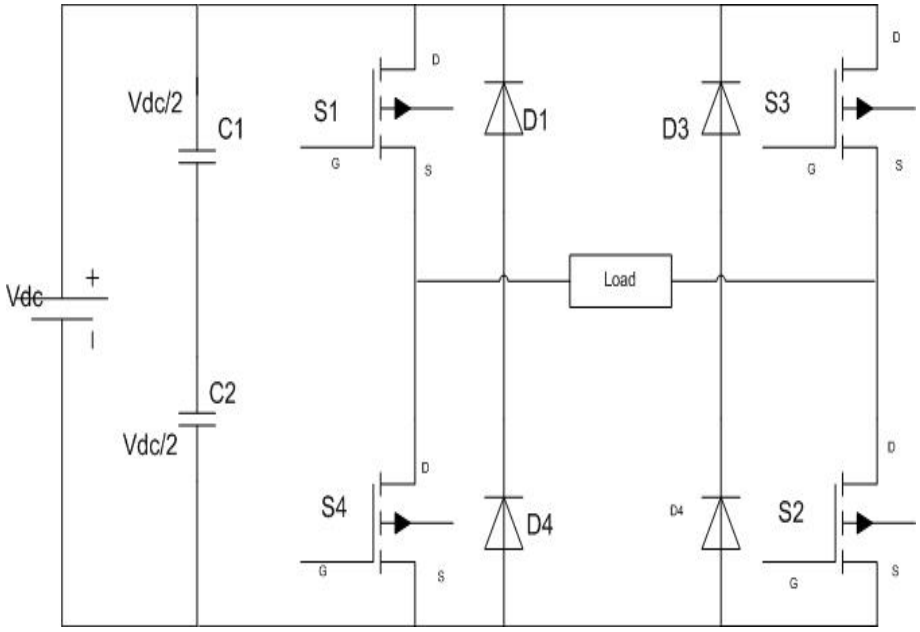

Figure.2.1 Single Phase voltage source (Full wave Bridge) Inverter.

TABLE 2.1

Switching scheme for single phase inverter

S1	S2	S3	S4	V_A	V_B	V_{AB}
ON	OFF	OFF	ON	$+V_s/2$	$-V_s/2$	$+V_s$
OFF	ON	ON	OFF	$+V_s/2$	$+V_s/2$	$-V_s$
ON	OFF	ON	OFF	$+V_s/2$	$-V_s/2$	0
OFF	ON	OFF	ON	$-V_s/2$	$+V_s/2$	0

2.3. Three Phase Inverter:

Three phase systems are used widely across the world. Most of the available power transmission systems follow three phase AC design. Typically components include three phase generators, electrical loads, and as well as transmission lines. In a three phase system constant power is available at the load. This makes three phase systems preferable over a single phase systems.

Generally three phase inverters are used for high and medium power applications. Three phase inverters can be designed with three single phase half bridge (half bridge contains two controlled switches in series) are connected in parallel. Also, three single phase full bridges to be connected in parallel with separate DC sources can form three phase inverter. The different models of three phase inverter are shown in Figure.2.2, and Figure.2.3.

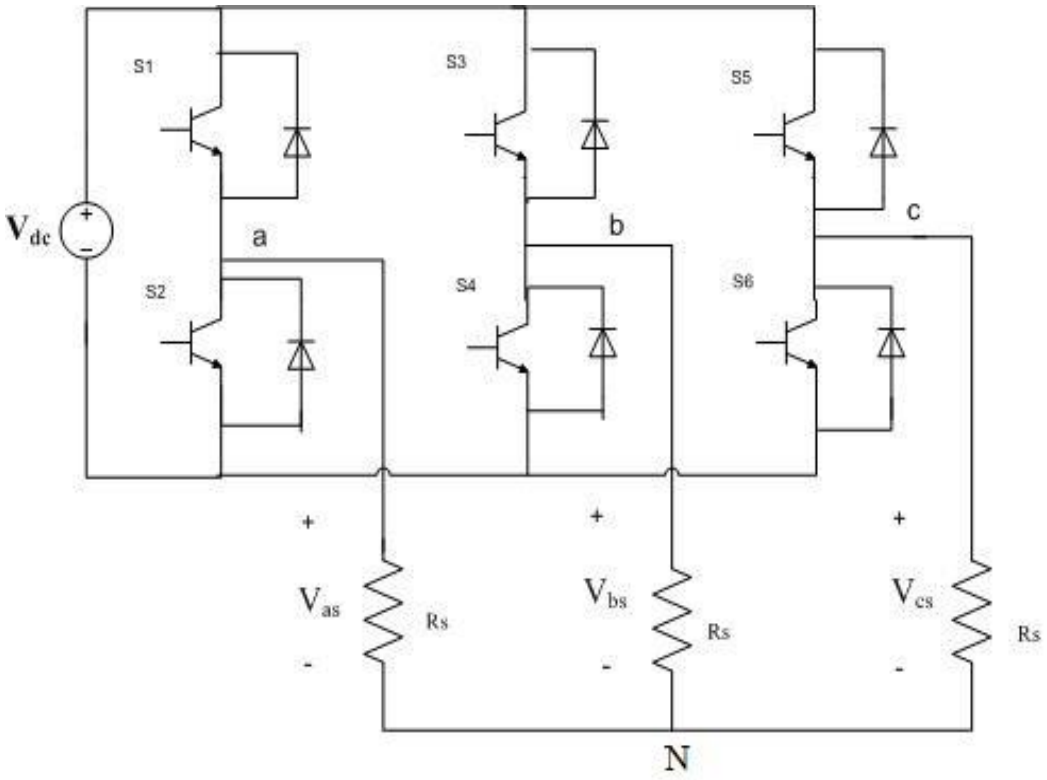

Figure.2.2 Three Phase voltage source Inverter with single phase half bridges.

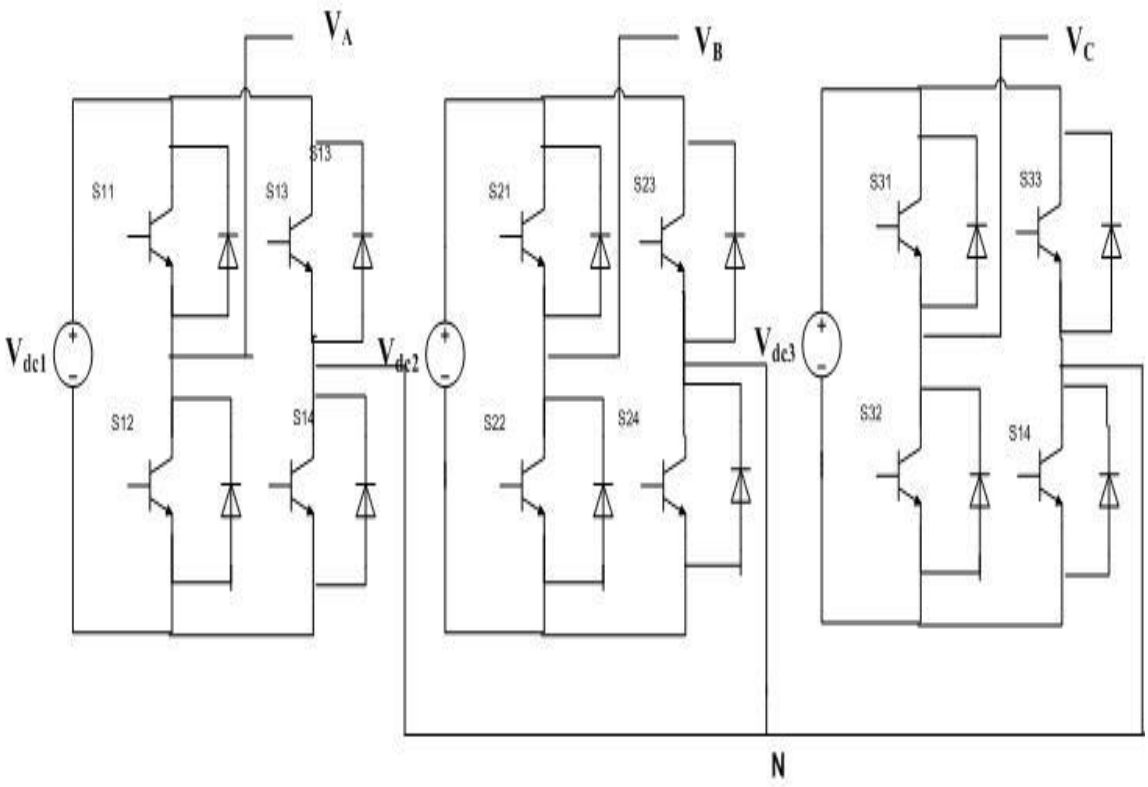

Figure.2.3 Three Phase voltage source Inverter with separate DC source.

2.4. Multilevel Inverter:

Multilevel converters are being used for variety of applications and also are commercially available in the markets. The growing demand of these devices attracted researchers and industries. An in-depth study is being done on various parameters of multilevel converter systems across the world. Researchers are trying to improve the performance of multilevel systems especially in terms of energy efficiency, power density, complexity, accuracy and reliability. Multilevel inverters produce output voltage in the form of stepped [10 - 11].

Advantages:

A Multilevel inverter has many advantages over a classical inverters or conventional 2-level inverter that uses pulse width modulation with very high carrier or switching frequency. These are following attractive features of multilevel inverters.

a. **Switching Frequency:**

Operation at fundamental switching and higher switching frequency pulse width modulation (PWM) is possible by using multilevel inverters.

b. **Input current:**

The current drawn by multilevel inverter usually exhibits low distortion.

c. **Staircase waveform quality:**

Multilevel inverters can reduce the switching stress or dv/dt stress; hence there is reduction of Electromagnetic compatibility (EMC) problem.

d. **Common mode voltage:**

By using multilevel converters, the obtained common mode voltages are smaller; therefore the stress can be reduced. With modern modulation schemes, common mode voltage can be eliminated further [12].

Disadvantages:

Despite various advantages discussed above multilevel inverters or converters have the following disadvantages

a. Several power semiconductor switches required.
b. High cost
c. Complex design

2.4.1. Types of Multilevel inverters:

There are primarily three types of multilevel inverter structures namely

a. Cascade Multilevel Inverters (C-MLI)
b. Flying Capacitor Multilevel Inverters (FC-MLI)
c. Diode clamped Multilevel Inverters (DC-MLI)

2.4.1.1. Cascade Multilevel Inverter/Cascaded H-bridge inverter:

The cascade H-Bridge inverter is a H-Bridges connected in a series or cascade of H-Bridges [13]. The number of DC sources required to produce a (2n+1) output phase voltage levels in a three phase multilevel cascade inverter is given by the relation.

$$M = 2n + 1 \quad (2.1)$$

Where M = Number of voltage levels and n = no of DC sources. Phase voltage is the sum of voltages of each H-bridge cell

$$V_{an} = V_{dc1} + V_{dc2} + V_{dc3} + \text{----------} + V_{dcm} + V_{dcn} \quad (2.2)$$

Figure.2.4 illustrates the structure of multilevel cascaded H-bridge inverter for single phase. Each single phase H-bridge or full bridge contains separate DC source. A five level cascaded multilevel inverter generates five output voltage levels (V_{dc}, $2V_{dc}$, 0, $-V_{dc}$, $-2V_{dc}$) with two DC separate voltage sources and a seven level cascaded multilevel inverter produces seven output voltage levels (V_{dc}, $2V_{dc}$, $3V_{dc}$, 0, $-V_{dc}$, $-2V_{dc}$, $-3V_{dc}$) with three separate DC voltage sources for each phase of three phase inverter. Each single phase full bridge contains four switches, S11, S12, S13,S14 are produces three different output voltage levels such as V_{dc}, 0, $-V_{dc}$. $+V_{dc}$ output voltage level can be obtained, when the switches S11 and S14 are turn on, similarly $-V_{dc}$ output voltage level can be obtained by turning on switches S12 and S13. In other cases of switching the output voltage level is zero.

Figure.2.5 stepped wave form shows the example for 11- level single phase inverter which contains five different separated DC sources and five full bridges. The output voltage is given by

$$V_{n5} = V_{n1} + V_{n2} + V_{n3} + V_{n4} + V_{n5} \quad (2.3)$$

The Fourier transform for the wave form shown in Fig.2.5 is follows

$$H\ (m) = \frac{4}{m\pi}\left[\cos(m\theta_1) + \cos(m\theta_2) + \cdots + \cos(m\theta_s)\right. \quad (2.4)$$

Where m = 1, 3, 5, 7, ...

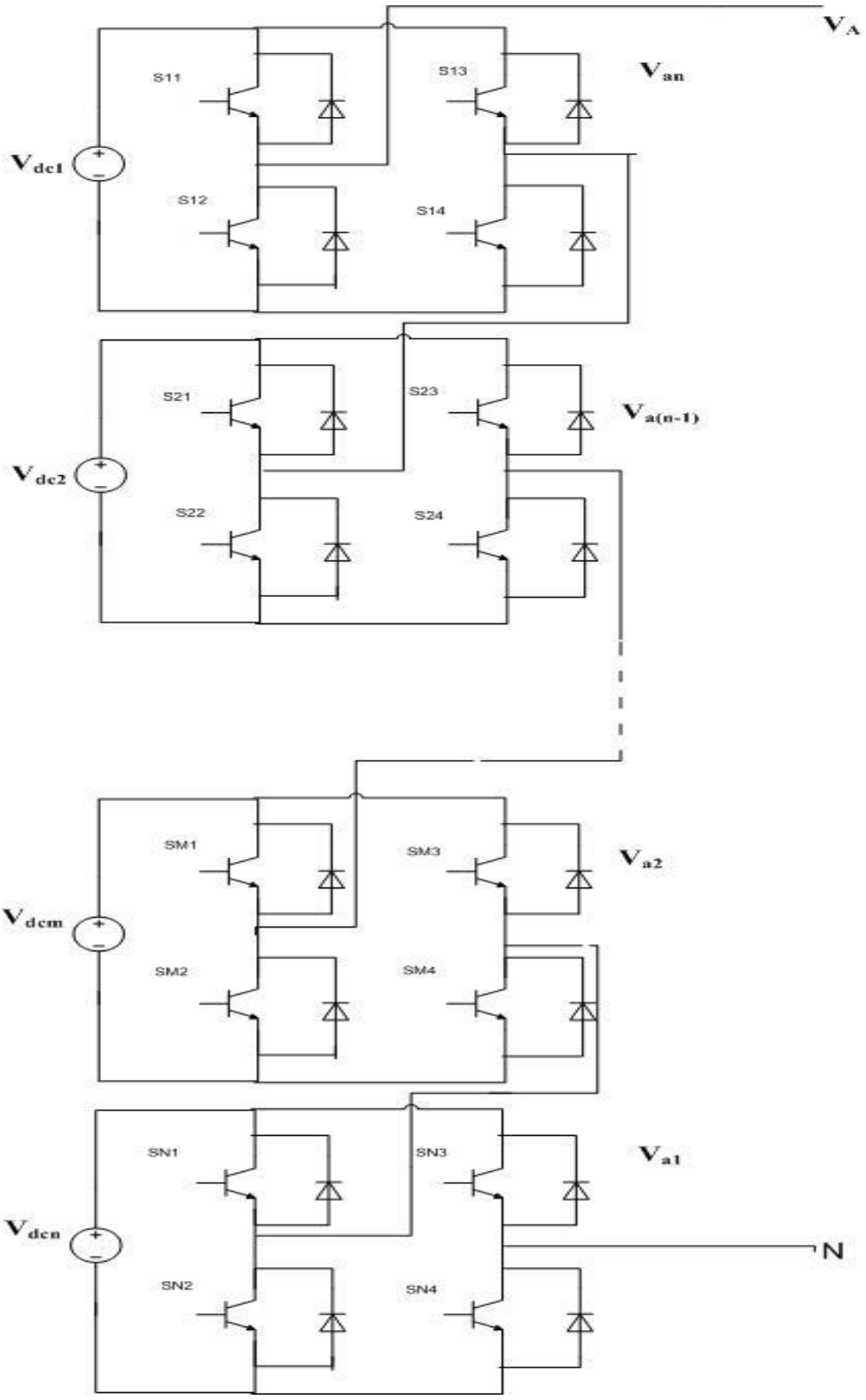

Figure.2.4 Structure of multilevel cascaded H-bridge inverter for single phase.

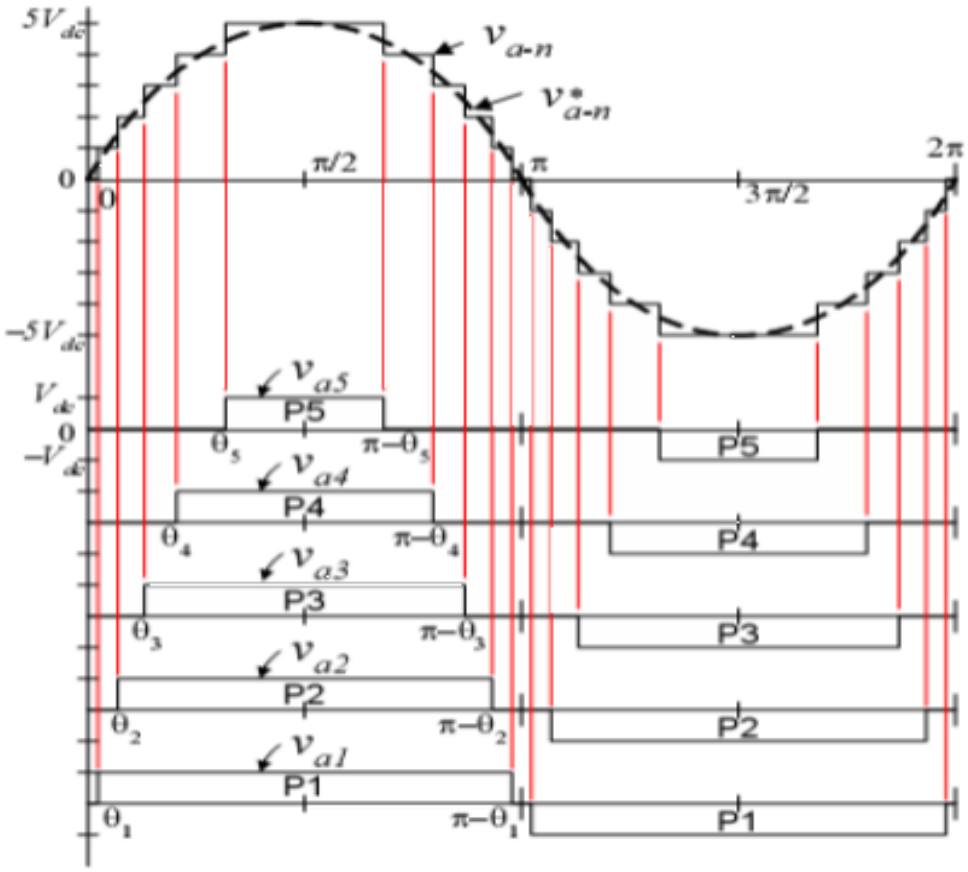

Figure.2.5 11-level inverter output voltage waveform with five separate DC sources.

Advantages:

- Electrical shocks are reduced.
- No extra requirement of clamping diodes hence number of components decreases.
- These inverters are scalable, good circuit layout due to the series structure.
- Switching redundancy is feasible

Disadvantages:

- Due to availability of separate DC voltage sources these inverters are restricted to certain applications.

2.4.1.2. Flying Capacitor Multilevel Inverter (FC-MLI):

This is also called as Capacitor-Clamped multilevel inverter [14]. Flying capacitor multilevel inverter topology permits high flexibility in output waveform and also allows balancing voltage across flying capacitors.

The Figure.2.6 shows the general structure of m-level flying capacitor or capacitor clamped based multilevel inverter which produces m-level output voltage waveform. The requirement voltages for the capacitors are different. This type of multilevel inverter structure demands more number of flying capacitors per phase. Due to large number of capacitors the design becomes bulky and complex. Simple five level flying capacitor multilevel inverter is shown in Figure.2.7 and the switching pattern for five level inverter is shown in TABLE 2.2

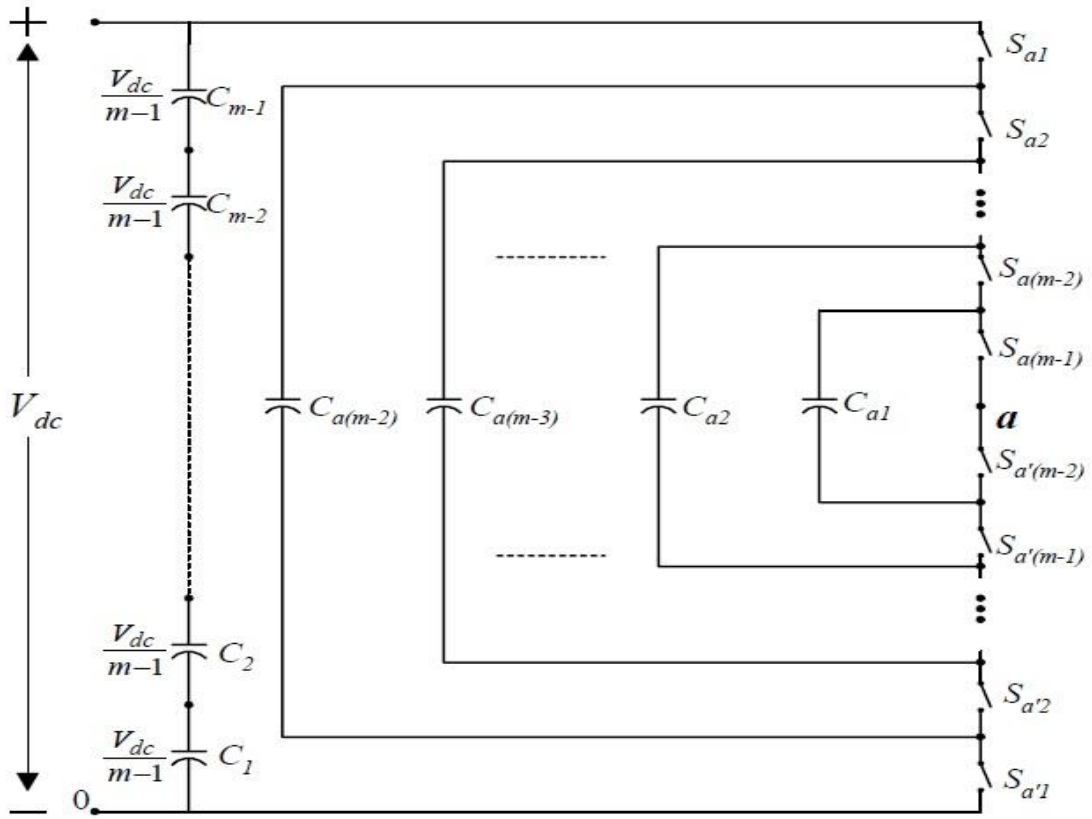

Figure.2.6 m-level Flying Capacitor multilevel inverter.

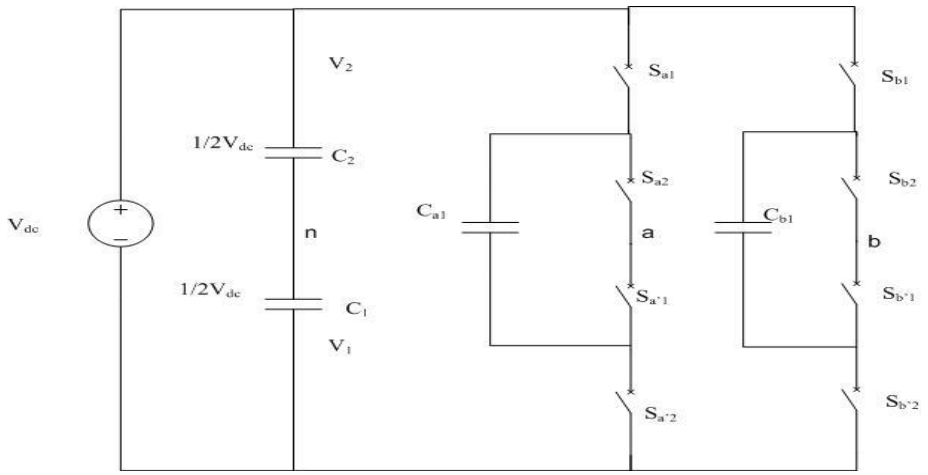

Figure.2.7 A five level flying Capacitor multilevel inverter.

TABLE 2.2

Switching scheme for flying capacitor or clamped capacitor multilevel inverter

S_{a1}	S_{a2}	$S_{a'2}$	$S_{a'1}$	S_{b1}	S_{b2}	$S_{b'2}$	$S_{b'1}$	V_{ab}
0	0	1	1	1	1	0	0	$-V_{dc}$
0	0	1	1	0	1	0	1	$-\frac{1}{2}V_{dc}$
0	1	0	1	1	1	0	0	$-\frac{1}{2}V_{dc}$
0	1	0	1	1	1	0	0	$-\frac{1}{2}V_{dc}$
1	1	0	0	1	1	0	0	0
0	0	1	1	0	0	1	1	0
0	1	0	1	0	0	1	1	$\frac{1}{2}V_{dc}$
1	1	0	0	0	1	0	1	$\frac{1}{2}V_{dc}$
1	0	1	0	0	0	1	1	$\frac{1}{2}V_{dc}$
1	1	0	0	0	0	1	1	V_{dc}

The advantages and disadvantages of the flying capacitor multilevel inverters is as follows

Advantages:

- Total Harmonic Distortion is reduced.
- Reactive power as well as real power flow can be controlled.
- Flexible switching redundancy.
- Greater m allows

Disadvantages:

- Due to large number of capacitors design is bulky and increases the cost.
- Switching control becomes complex.
- Efficiency reduces for real power transmission.

2.4.1.3. Diode Clamped Multilevel Inverter (DC-MLI):

Diode clamped inverter, also known as Neutral point clamped converter (NPC) [15] at basic level, consists of a combination of switches, diodes and capacitors. The two switches are arranged in series with capacitors and diodes in parallel such that the higher dc voltage is divided into lower steps by the capacitors. This configuration can result in five level output *(-V_{dc} to +V_{dc})* for a given DC input V_{dc}. The output voltage is controlled by the combination of switches in the network. The schematic for five level diode clamped inverter is shown in Figure 2.8, and switching scheme for this design is shown in TABLE 2.3. The 5-level system is just the simplest one and higher levels (3-phase-6-level) have also been already implemented.

Higher levels of systems require more number of diodes per phase. It was observed that series inclusion of diodes is impractical for higher level design and hence cannot be implemented. Also, the capacitor voltage is often imbalanced which makes this model less efficient for higher level outputs. One way to overcome the voltage imbalance is to add resistors in series with each capacitor. Although this improves the performance, the NPC system yet has several drawbacks.

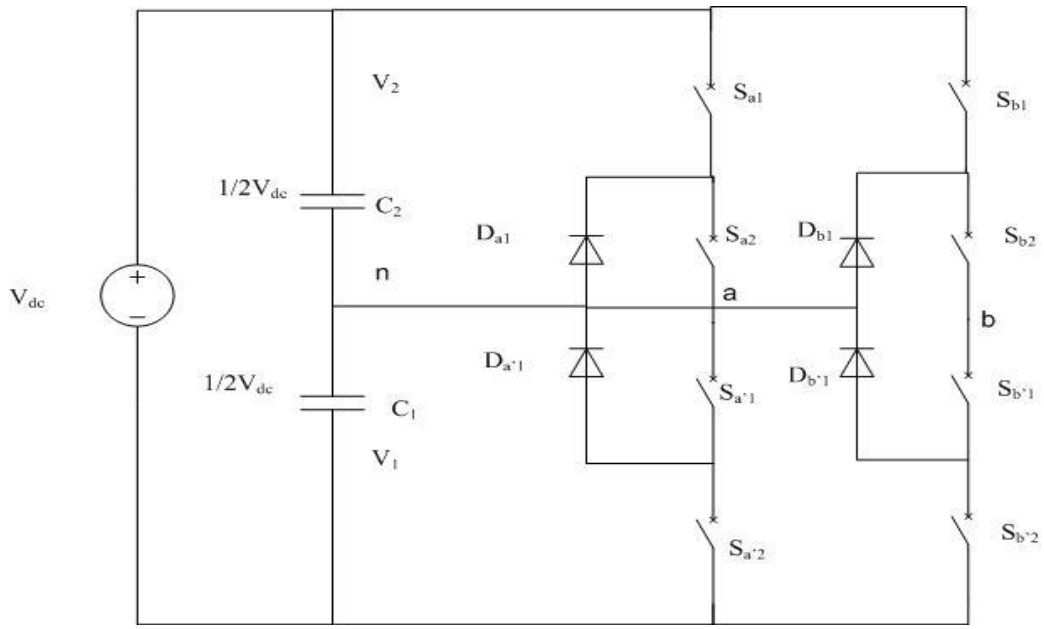

Figure.2.8 A five level Diode Clamping multilevel inverter.

TABLE 2.3

Switching scheme for Diode Clamped multilevel inverter

S_{a1}	S_{a2}	$S_{a'2}$	$S_{a'1}$	S_{b1}	S_{b2}	$S_{b'2}$	$S_{b'1}$	V_{ab}
0	0	1	1	1	1	0	0	$-V_{dc}$
0	0	1	1	0	1	1	0	$-\frac{1}{2}V_{dc}$
1	1	0	0	1	1	0	0	0
0	0	1	1	0	0	1	1	0
0	1	1	0	0	0	1	1	$\frac{1}{2}V_{dc}$
1	1	0	0	0	0	1	1	V_{dc}

Advantages:

- Harmonic distortion reduces merely by increasing the number of levels.
- Efficiency can be high for operation at fundamental frequency of switching.
- The design model is relatively simple.
- DC voltage across each phase is same.

Besides these advantages, diode clamped inverter systems exhibit several disadvantages.

Disadvantages:

- Number of diodes required increases nonlinearly with required levels of output.
- Voltage imbalance disturbs the performance of system.
- Current rating varies for each switch due to different duty cycles of operation.

2.5. Importance of Cascade multilevel inverter:

There are different structures of multilevel inverters namely diode clamped multilevel inverters, cascaded multilevel inverter, flying capacitor multilevel inverters and other structures available. Among these different structures of multilevel inverters, cascade multilevel inverters are producing high output voltage levels, high output power levels and high reliability due to property of modular topology. The structure obtained by adding single phase inverters are in series is cascade multilevel inverters. This structure of multilevel inverters can reach medium output power and voltage level easily using advanced low voltage components. If the number of components (power electronic components) is more, the system becomes less reliable [16] (number of elements is indirectly proportional to reliability). The comparisons of three different structures of multilevel inverter are shown in TABLE 2.4. It is inferred that Cascade multilevel inverter requires less number of components and hence cascade multilevel inverter systems are high reliable and flexible.

TABLE 2.4

Comparison of Multilevel inverter topologies

Type of converter	Diode Clamped Multilevel inverter	Flying Capacitor Multilevel inverter	Cascade Multilevel inverter
Main Diodes	(n - 1)* 2	(n - 1)* 2	(n - 1)* 2
Main Switching	(n - 1)* 2	(n - 1)* 2	(n - 1)* 2
Clamping Diodes	(n - 1)* (n - 1)	0	0
Balancing Capacitors	0	(n - 1)* (n - 1)	0
DC bus Capacitors	(n - 1)	(n - 1)	(n - 1)/2

2.6. Applications of Cascade multilevel inverters:

Cascade multilevel inverter requires more number of separate DC sources then also these inverters are mostly used in various applications.

a. Electric Vehicles traction motor drives:

For Electric vehicles traction motor drives applications [17], cascade inverters are most suitable. These inverters are produces output voltage almost sinusoidal with low electromagnetic compatibility (EMC) and also low voltage ripples.

b. LNG Plant

c. STATCOM

d. Pumps and Fans

2.7. Modulation Technique for Multilevel Inverters:

There are several modulation techniques available to control multilevel inverters such as Sinusoidal Pulse Width Modulation (SPWM) [18], Space Vector Modulation (SVM), Selective Harmonic Elimination (SHE), Wavelet Modulation (WM) and others. In this work multilevel inverters are controlled by Sinusoidal Pulse Width Modulation (SPWM).

Now a days in practical applications pulse width modulation (PWM) inverters are mostly used in power electronic applications. PWM inverters are producing DC to AC voltages of variable frequency and variable magnitude. PWM inverters are used in ac motor loads to adjust speed. These PWM pulses can be generated by using analog and digital design. By using 555 timer, Microcontroller, DSP (Digital Signal Processor) processor [19-20] and FPGA (Field Programmable Gate Array) we can generate PWM pulses. There are several PWM techniques available such as Sinusoidal Pulse Width Modulation (SPWM), Space Vector Modulation (SVM), Wavelet Modulation and Selective Harmonic Elimination. In this work we designed multilevel cascaded inverter using sinusoidal pulse width modulation technique. This is also called as natural sampling i.e. amplitudes of modulating wave (sine wave) is compared with high frequency carrier wave (triangular wave) to generate PWM signals. The ratio of amplitude of modulating waveform to the amplitude of carrier waveform is known as modulation index. The SPWM technique achieves low power consumption, higher efficiency, good power handling capability and easy to implement using today's digital microcontrollers, microprocessors and FPGA.

Sinusoidal Pulse Width Modulation (SPWM):

The multiple pulses are produced in this modulation technique and each pulse width varies with respect to magnitude of sine wave. These gating signals or control signals can be obtained by comparing triangular signal having high frequency with desired frequency sinusoidal signal. The number of gating pulses per half cycle based upon the ratio of frequency of the reference (sinusoidal) signal to the carrier or triangular signal (f_c). The ratio of peak amplitude of control (modulating sine wave) signal to the peak amplitude of carrier signal is modulation index (m_a).

Figure 2.9 shows the generation of gating pulses with different modulation index. Modulation index controls the RMS voltage of output waveform. The RMS value of output voltage is given by

$$V_o = V_s \left[\sum_{m=1}^{2q} \frac{2t_{on}}{T} \right]^{1/2} \tag{2.5}$$

Where t_{on} = Width of mth pulse.

The amplitude modulation index is given by

$$m_a = \frac{V_m}{V_{car}} \tag{2.6}$$

Where V_m = peak amplitude of modulating signal or control signal

V_{car} = peak amplitude of high frequency carrier signal.

Modulation ratio for frequency is

$$m_f = \frac{f_{car}}{f_m} \tag{2.7}$$

Where f_m = frequency of sinusoidal signal

f_{car} = frequency of triangular signal

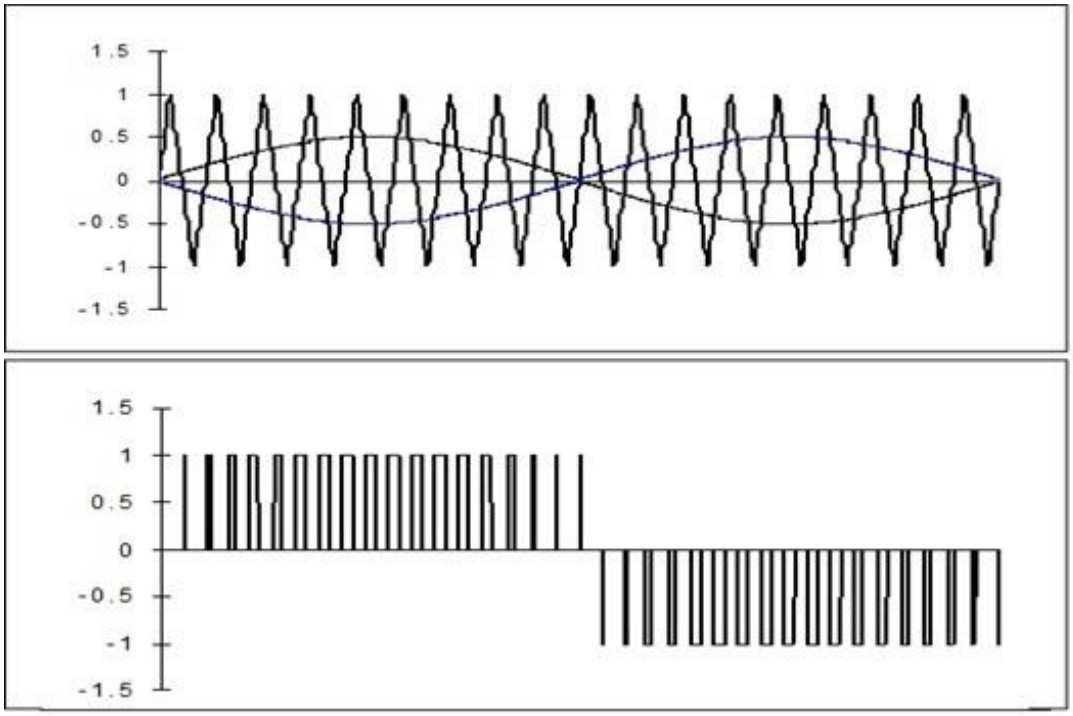

Fig.2.9 PWM signal generation with modulation index (m_a) < 1.

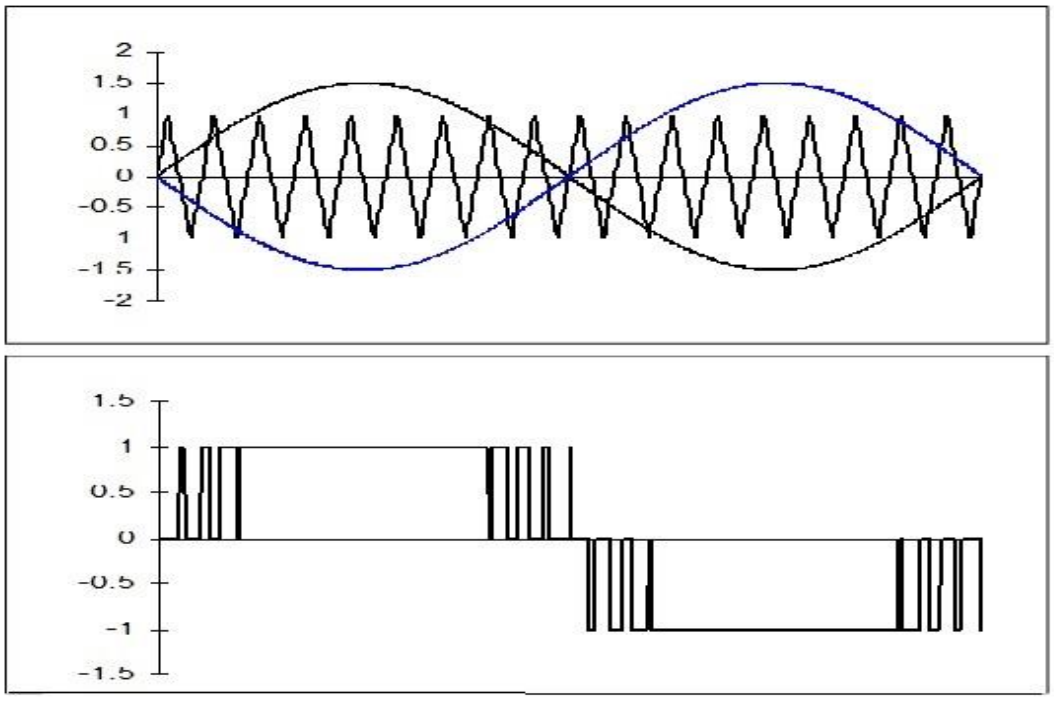

Fig.2.10 PWM signal generation with modulation index (m_a) > 1.

Advantages:

- Lower Switching losses.
- Low power loss since no voltage drop across when switch is turn ON and also there is no practical current when switch is in OFF state hence reduces power loss.
- Easy to implement.
- Also works with digital controls due to their turn ON/OFF nature.

Applications:

- Low power HVDC transmission
- Active filters
- UPS (Uninterruptible power supplies)
- In AC motors as adjustable speed drives
- Renewable energy applications
- STATCOM, DSTACTCOM, UPFC.

CHAPTER 3

GPI CONTROLLER

CHAPTER 3

GPI CONTROLLER

3.1. Generalized Proportional Integral Tracking Controller with output voltage as feedback

GPI controller is robust [21] hence, in this work; we have used a GPI controller with output voltage as a feedback for cascade multi-level Inverter. GPI voltage controller helps to maintain the desired voltage level at the load by tracking the reference voltage. In most of the applications multilevel cascade inverters are subjected to unexpectedly nonlinear loads [22], [23] due to this the output voltage is not constant across the load. The Generalized Proportional Integral Voltage Controller has the ability to resolve the robustness difficulty. These controllers have been used in many applications such as voltage/power converters (DC to DC) [24], [25] in different manners and stabilization around a constant required reference [26]. Figure.3.1 shows the five level cascaded single phase inverter with LC filter and Figure.3.2 shows the equivalent model for five level inverter.

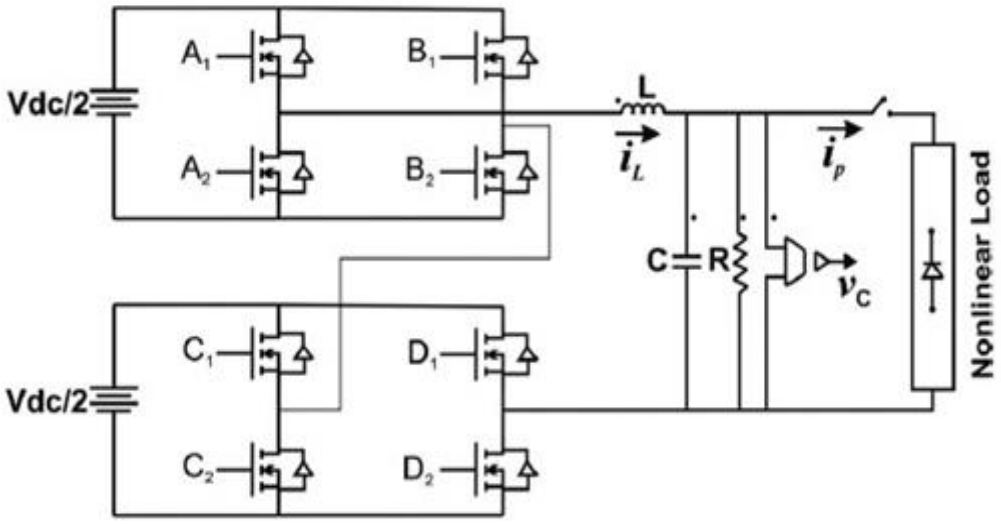

Figure.3.1 Five level inverter with LC filter.

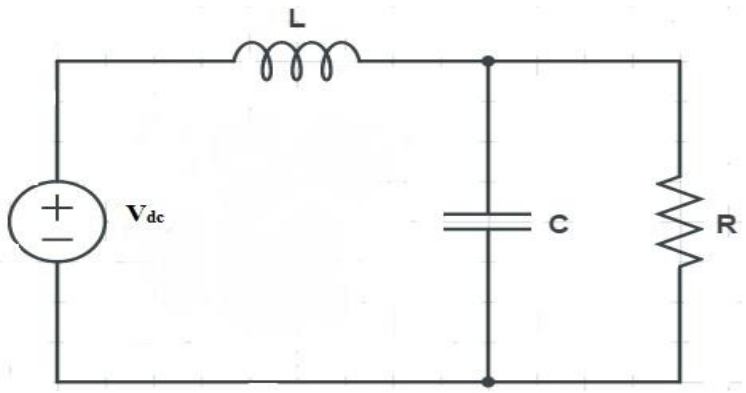

Figure.3.2 Equivalent model of inverter.

The mathematical model of the cascaded multi-level inverter can be given by [27]:

$$L\frac{di}{dt} = -v_o + V_{dc}\,u_{av} \tag{3.1}$$

$$C\frac{dv}{dt} = i_L - \frac{1}{R}v_0 \tag{3.2}$$

Where, i is the current through the inductor, v_o is voltage across capacitor and u is denotes control input taking discrete values between [-1 1] [28]. L, C represent Inductor and Capacitor respectively which act as a low pass filter. R denotes load resistance. Schematic of a five level inverter with R, L, C is shown in Figure 3.1. Higher levels can be designed using the similar modules by increasing the number of sources.

The control method is based on the state average model of the inverter with control input u replaced with a signal u_{avg} ; where, u_{avg} is a continuous signal in time and it takes the values between -1 to 1. The average model of the inverter is flat i.e., control signal can be expressible in terms of flat output, denoted by F , and this output is equal to voltage across capacitor.

$$i_L = C\frac{dF}{dt} + \frac{1}{R}F \tag{3.3}$$

$$u_{avg} = \frac{LC}{V_{dc}}\left(\frac{d^2F}{dt^2}\right) + \frac{L}{RV_{dc}}\left(\frac{dF}{dt}\right) + \frac{1}{V_{dc}}F \tag{3.4}$$

$$v_o = F \tag{3.5}$$

On integrating Eq(3.1), we get

$$i_L\ (\mathrm{t})\ =\ i_L\ (0)\ +\ \frac{1}{L}\int_0^t [V_{dc}\,u_{avg}(\beta) -\ v_o\,(\beta)\ ]\ d\ \beta \tag{3.6}$$

$$\hat{\imath}_L(\mathrm{t}) =\ \frac{1}{L}\ \int_0^t [V_{dc}\,u_{avg}(\beta) -\ v_o\,(\beta)\ ]\ d\ \beta \tag{3.7}$$

$$\dot{F} = \dot{v} \tag{3.8}$$

$$\hat{\dot{F}} = \frac{1}{C}\ \hat{\imath}\ -\ \frac{1}{RC} \tag{3.9}$$

$$= \frac{1}{LC}\ \int_0^t [V_{dc}\,u_{avg}(\beta) -\ v_o\ (\beta)\ ]\ d\ \beta - \frac{1}{RC} \tag{3.10}$$

$$F =\ \hat{\dot{F}} +\ \dot{F}_0 \tag{3.11}$$

Where $\dot{F}$ denotes unknown initial rate of change of voltage. Consider a sinusoidal signal with known constant amplitude A_m and constant known frequency ω_n *i.e.* $v^*_o(t) = A_m \sin(\omega_n t)$ it is desired to have the output capacitor voltage $v_o(t)$ of the inverter track the signal with small tracking error independent of the time varying load current.

GPI feedback control law is given by

$$u_{avg} = \frac{LC}{V_{dc}}\,v(t)\ +\ \frac{L}{RV_{dc}}\ \hat{\dot{F}} + \frac{1}{V_{dc}}\ F \tag{3.12}$$

Where

$$v(t) = \ddot{F}^*(t) - z_3\ \left[\hat{\dot{F}}\ (t) -\ \dot{F}^*(t)\right] -\ z_2[F(t) -\ F^*\ (t)]$$

$$- z_1\ \int_0^t [\,F(\beta) -\ F^*(\beta)]\ d\beta - z_0 \int_0^t \int_0^\sigma [F(\Omega) -\ F^*(\Omega)]\ d\Omega \tag{3.13}$$

$$F^*(t) = A_m \sin\,(\omega_n\,t),$$

$$\dot{F}^*(t) = A_m\,\omega_n\,\cos\,(\omega_n\,t),$$

$$\ddot{F}^*(t) = -\ A_m\,\omega_n^2\,\sin^{\,2}(\omega_n\,t) \tag{3.14}$$

$$u_{av}{}^{*}(t) = \frac{LA_m\,\omega_n}{RV_{dc}}\,cos\,(\omega n\,t) + \frac{A_m}{V_{dc}}\,[1 - LC\omega_n^2]sin\,(\omega_n\,t) \tag{3.15}$$

After some fundamental operations, one obtains

$$u_{av}{}^{*}(t) = \sqrt{[\left(\frac{LA_m\,\omega_n}{RV_{dc}}\right)^2 + \left(\frac{A_m}{V_{dc}}\,[1 - LC\omega_n^2]\right)^2\,]}\,sin(\omega n\,t\,+\,\alpha) \tag{3.16}$$

$$\alpha = \arctan\,(\frac{L\omega_n}{R(1 - LC\omega_n^2)}) \tag{3.17}$$

Equation (3.16) gives the relation between the magnitude A_m and frequency of the required output voltage. The condition is

$$A_m \leq \frac{V_{dc}}{\sqrt{\left(\frac{L}{R}\right)^2\,\omega_n^2 + \,(1 - LC\omega_n^2)^{\,2}}} \tag{3.18}$$

Let $e = F(t) - F^{*}(t)$ represents tracking error. The closed loop system is formed from equations (12) and (4).Error dynamics given by

$$e^4 + \,z_3\,e^3 + \,z_2\ddot{e} + \,z_1\dot{e} + \,z_o e\, = \,-\frac{1}{C}\,\frac{d^3}{dt^3}\,i(t) \tag{3.19}$$

If z_3, z_2, z_1, z_0 are the coefficients of the linear dynamics of above equation are chosen such that the polynomial in the complex variable s can be given by:

$$e(s) = s^4 + \,z_3 s^3 + \,z_2 s^2 + \,z_1 s + \,z_0 \tag{3.20}$$

The desired Hurwitz polynomial can then be written as:

$$p_d\,(s) = (s^2 + \,2\xi\omega_n s + \,\omega_n^2)^2 \tag{3.21}$$

And the gains of GPI controller will be given by:

$$Z_3 = 4\xi\omega_n \tag{3.22}$$

$$Z_2 = 4\xi^2\omega_n^2 + 2\omega_n^2 \tag{3.23}$$

$$Z_1 = 4\xi\omega_n^3 \tag{3.24}$$

$$Z_0 = \omega_n^4 \tag{3.25}$$

The pole location of the above characteristic polynomial sufficiently far in left – half complex plane in order to reduce effects of nonlinear load in the closed loop. The roots were located at $(-2812 - 2525.52j)^2$ and $(-2812 + 2525.52j)^2$.

3.2. Simulation results

3.2.1. Single Phase Inverter

Design Parameters are given below in TABLE 3.1.

TABLE 3.1

Parameters used for Simulink Design using GPI controller

Parameter	Value
Voltage(V_{dc})	120V
Capacitance	10 µF
Inductance(L)	3 mH
Carrier Frequency(F_C)	2. 4 KHz
Cut off Frequency	900 Hz
Modulation Frequency	50 Hz
Damping Ratio(ξ)	0.750
Damping Frequency	3750
z_0	11250
z_1	59765625
z_2	1.58e11
z_3	1.9755e14

The Simulink model for seven level Single Phase Inverter is shown in Figure 3.3 and that of the GPI voltage controller in Figure 3.4. Seven level single phase inverter consists of three H-Brides and three equal magnitudes of DC voltage sources.

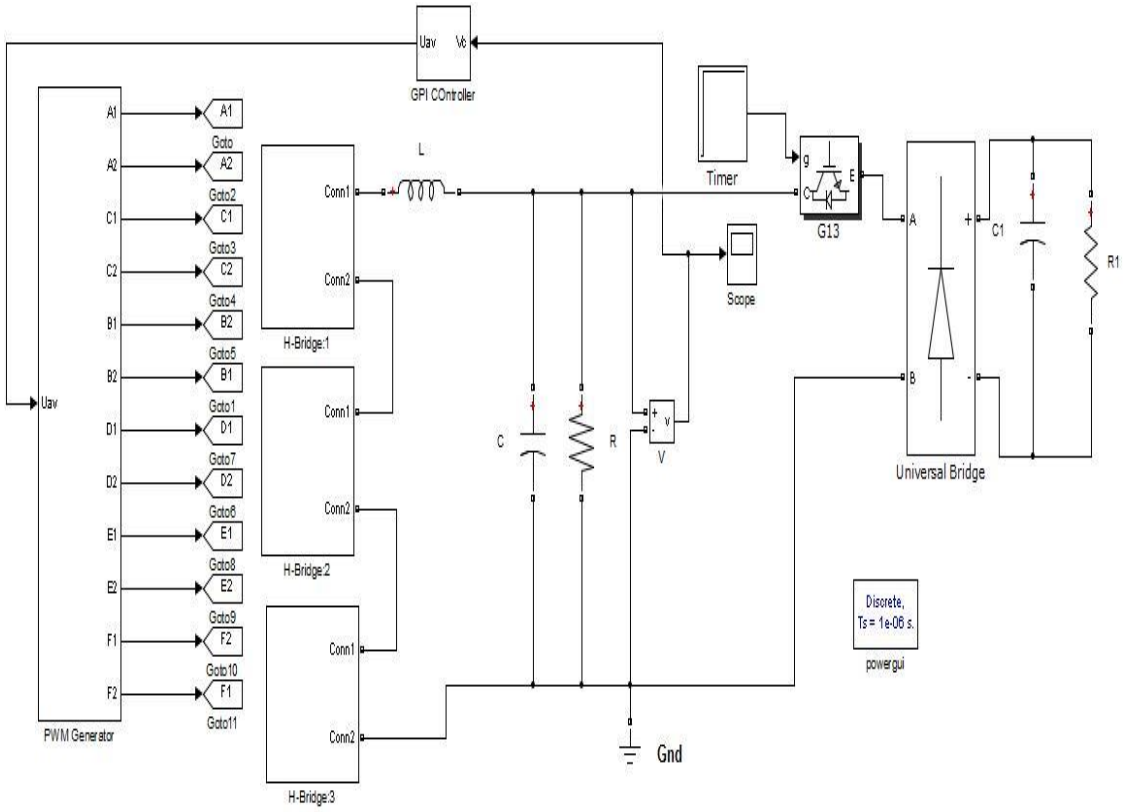

Figure.3.3 Simulink Model for seven level Single Phase Inverter with GPI voltage controller.

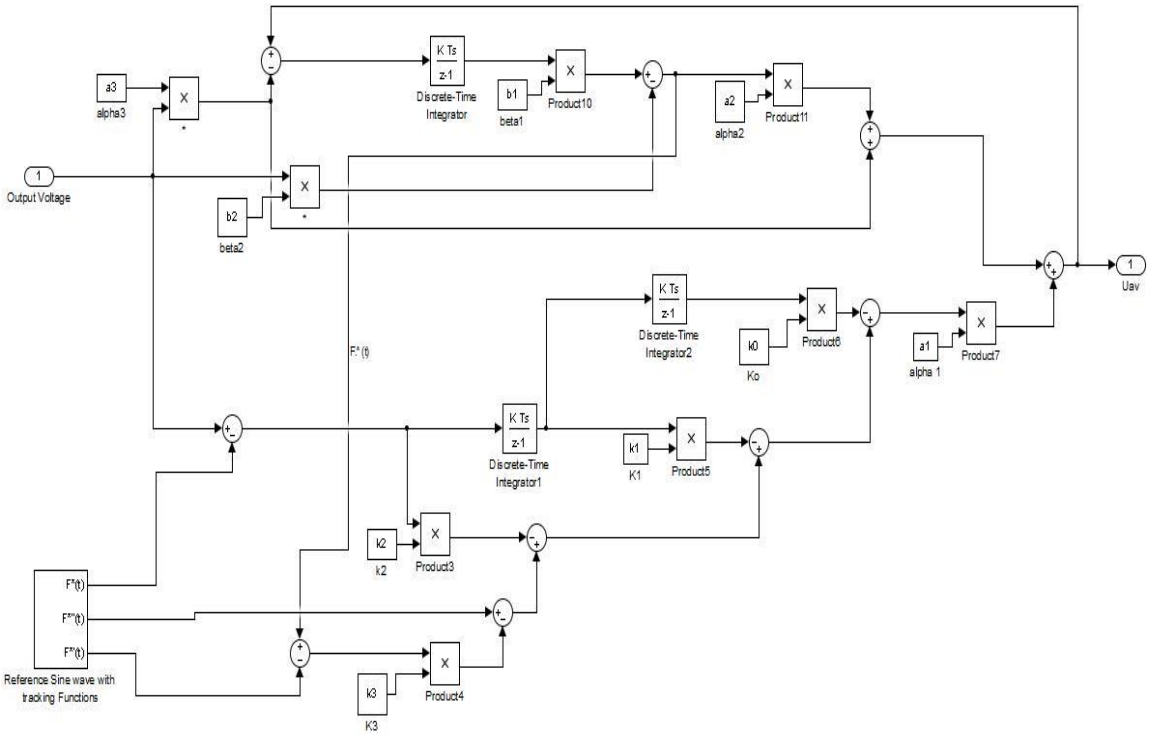

Figure.3.4 Simulink model of GPI voltage controller.

The control signal, u_{avg} is compared with triangular wave having frequency 2.4 KHz to generate switching signal with delay for seven level Inverter. For seven level single phase cascade multilevel inverter requires 12 gating signals to produce seven output voltage levels. The gating pulses generated by using Sinusoidal Pulse Width Modulation technique (SPWM). Control signal u_{avg} is compared with six triangular signals each phase shifted by 60^0. The matlab Simulink model for SPWM generation is shown in Figure.3.5.

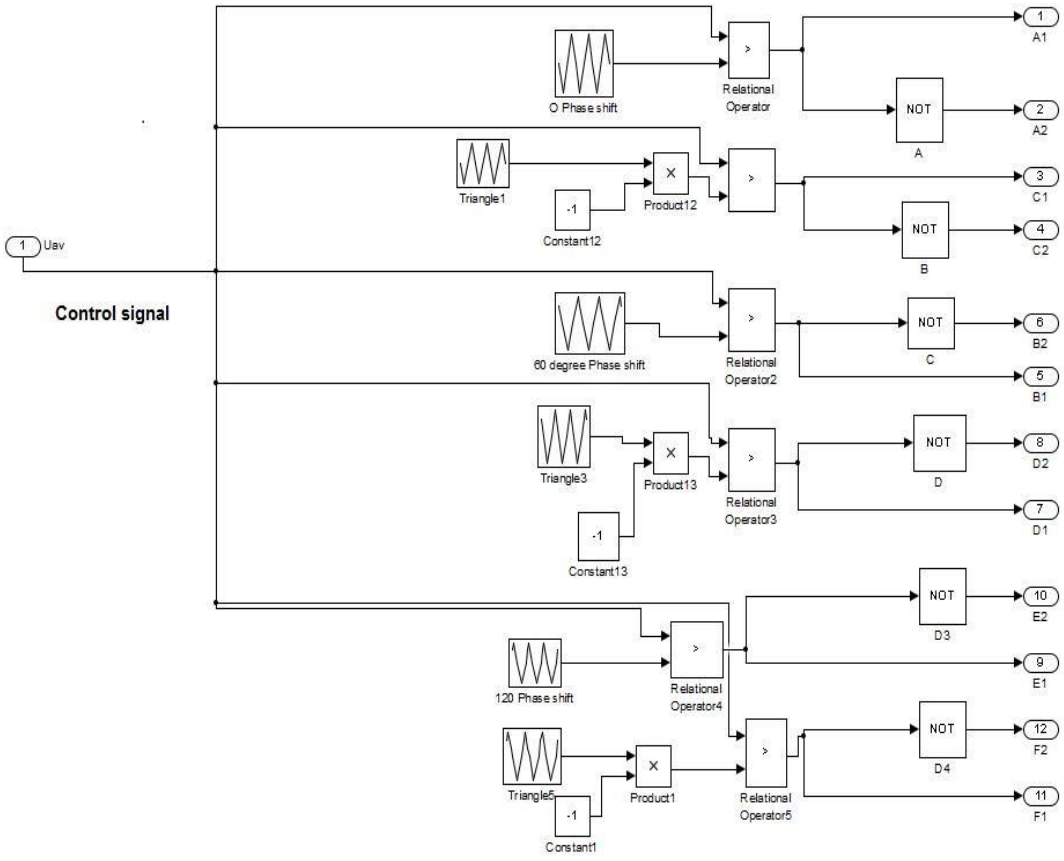

Figure.3.5 Matlab Simulink model for SPWM generation.

3.2.2. R-Load:

Load resistance (R_L) = 75Ω

The generated PWM signals (A1, A2, C1, and C2) are shown in Figure.3.6. The simulation results and FFT analysis of output voltage with and without filter and current for seven level single phase inverter are shown in Figure.3.7, Figure.3.8 respectively.

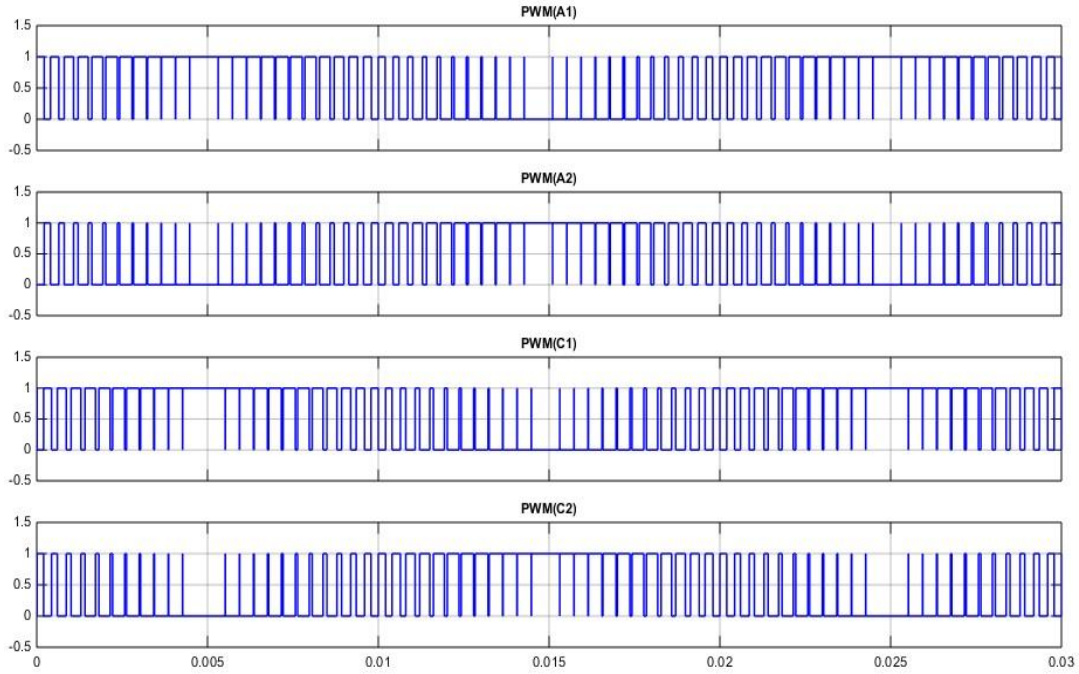

Figure.3.6 SPWM signals.

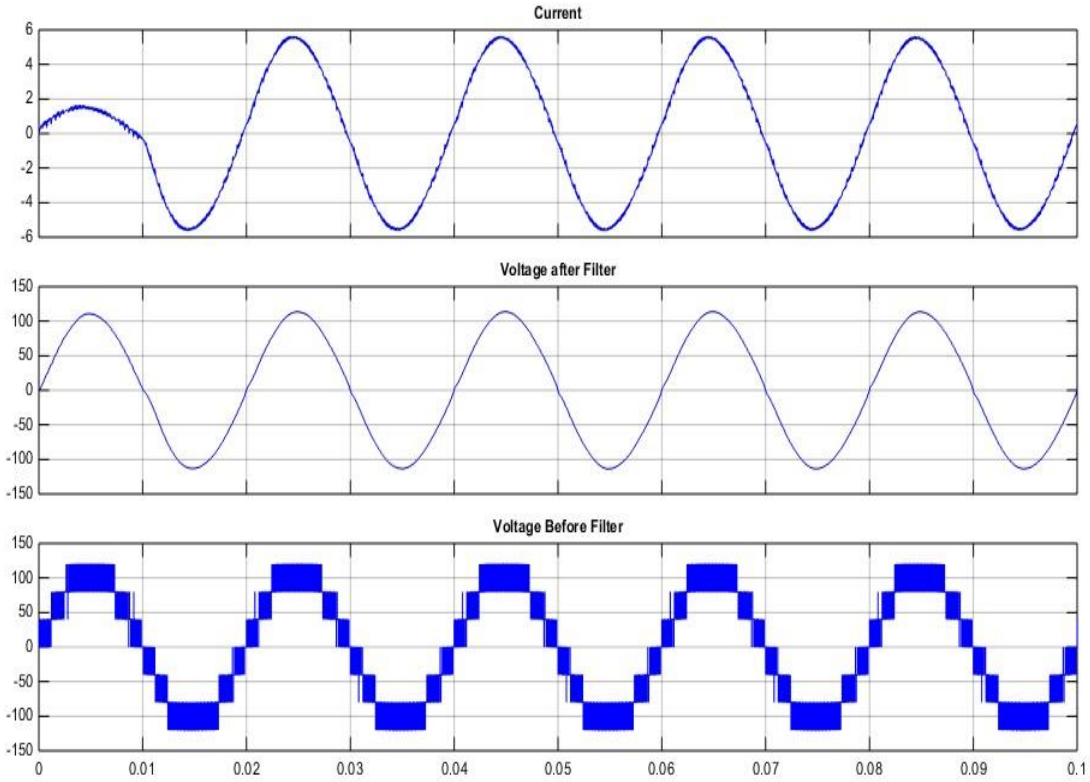

Figure.3.7 Current and voltage (with and without filter) waveforms for seven level single phase inverter with resistive load using GPI voltage controller.

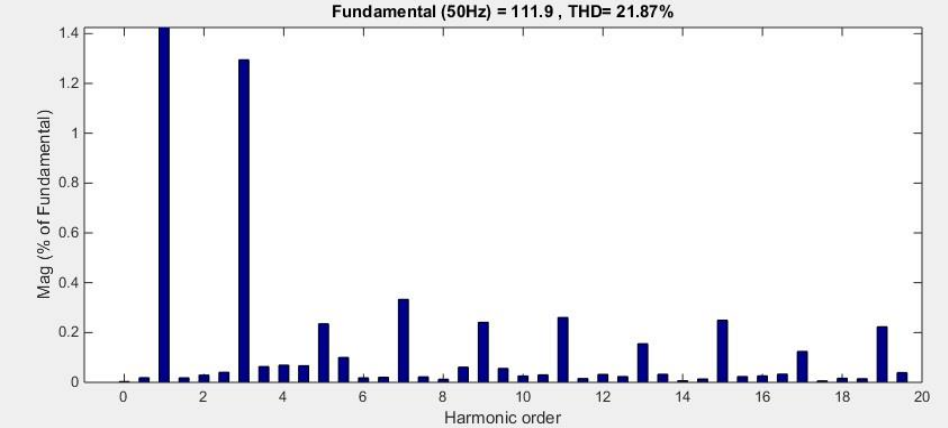

Figure.3.8 (a)

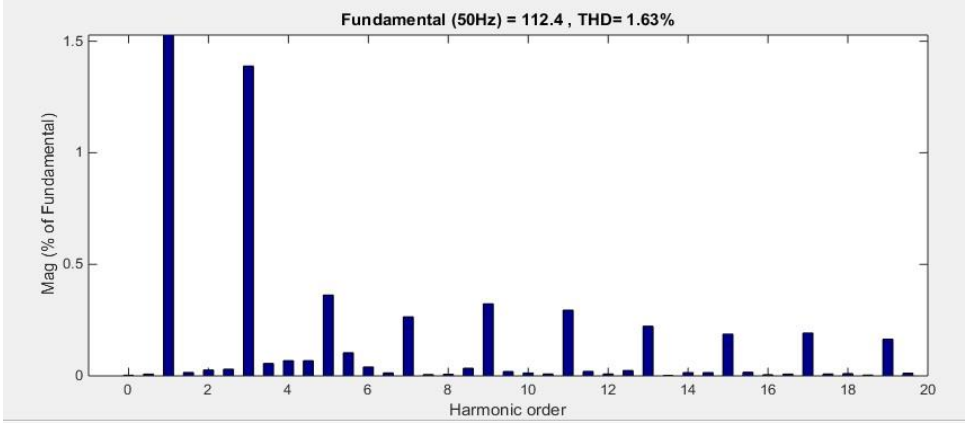

Figure.3.8 (b)

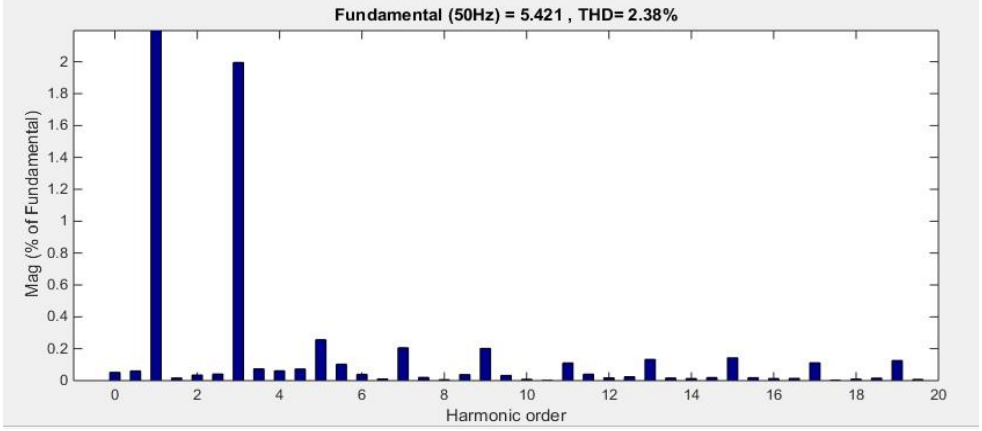

Figure.3.8 (c)

Figure.3.8 FFT Spectra of seven level single phase inverter with R-load using GPI voltage controller (a) Output voltage without filter (b) output voltage with filter (c) Output current.

3.2.3. R-L load:

Load resistance (R_L) = 75Ω

Load Inductance (L) = 200mH

The simulation results and FFT analysis of output voltage with and without filter and current for seven level single phase inverter are shown in Figure.3.9, Figure.3.10 respectively.

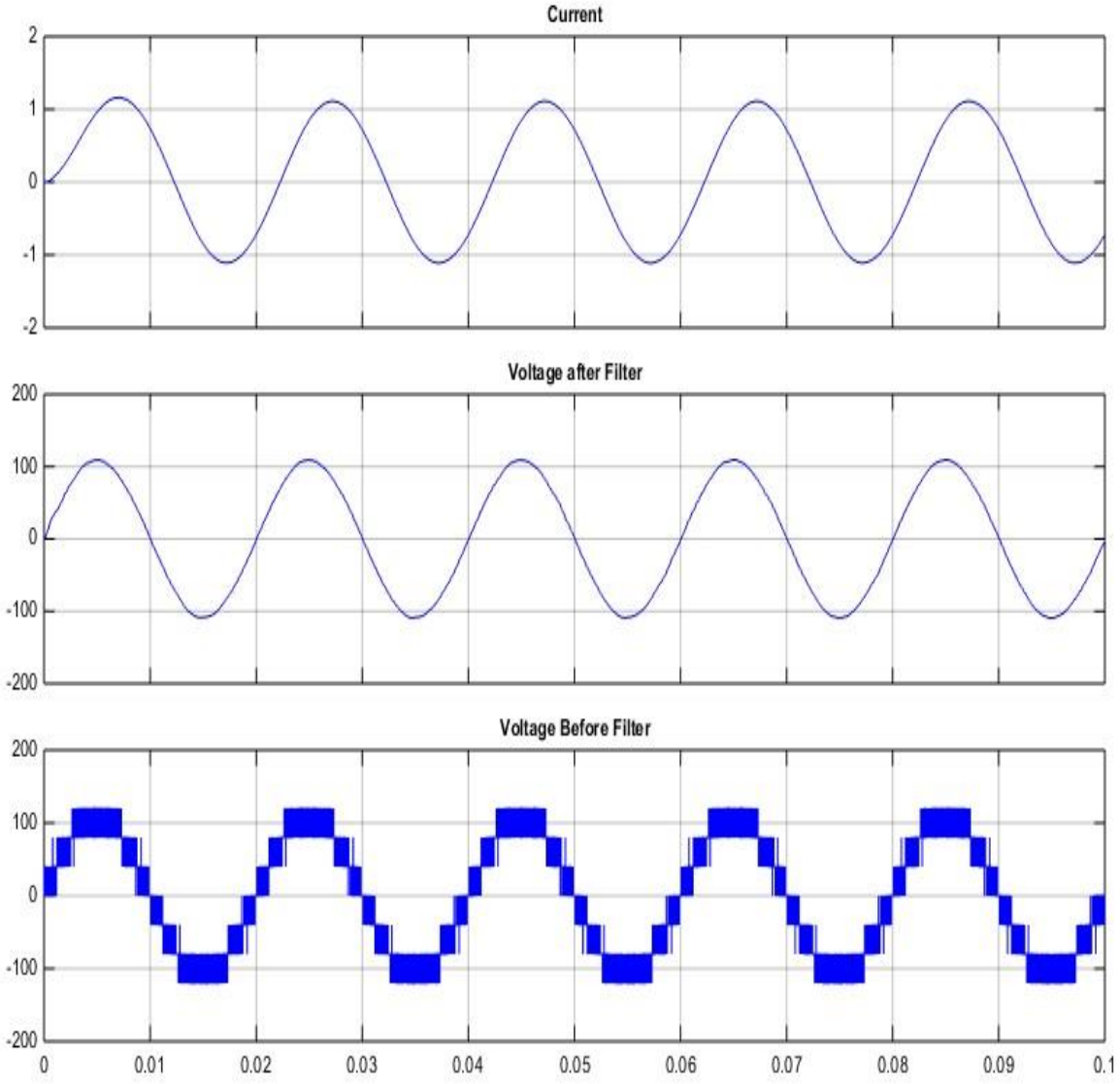

Figure.3.9 Current and voltage (with and without filter) waveforms for seven level single phase inverter with R-L load using GPI voltage controller.

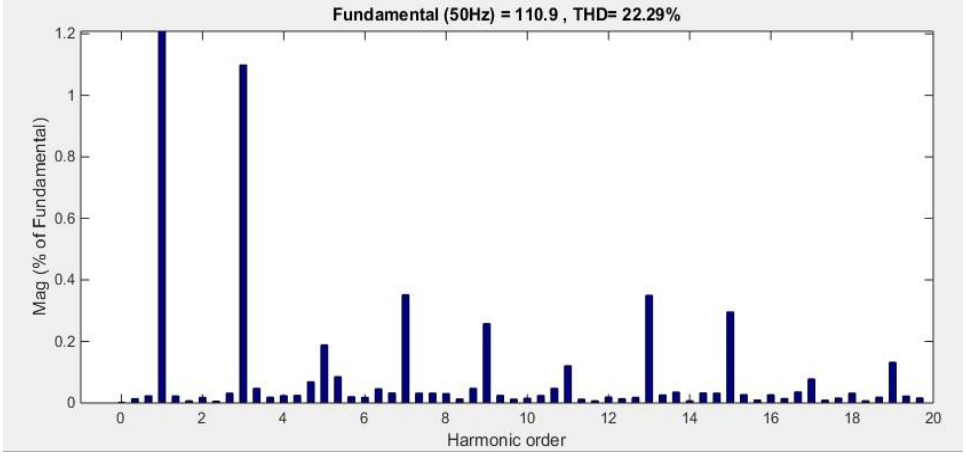

Figure.3.10 (a)

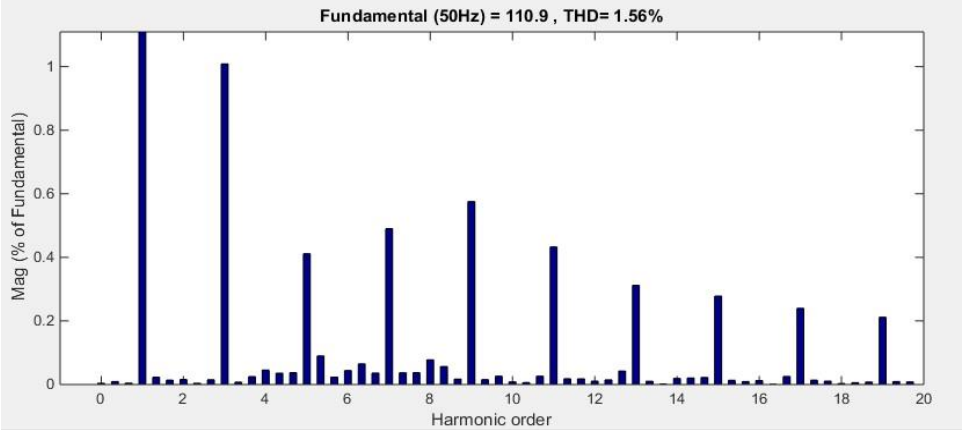

Figure.3.10 (b)

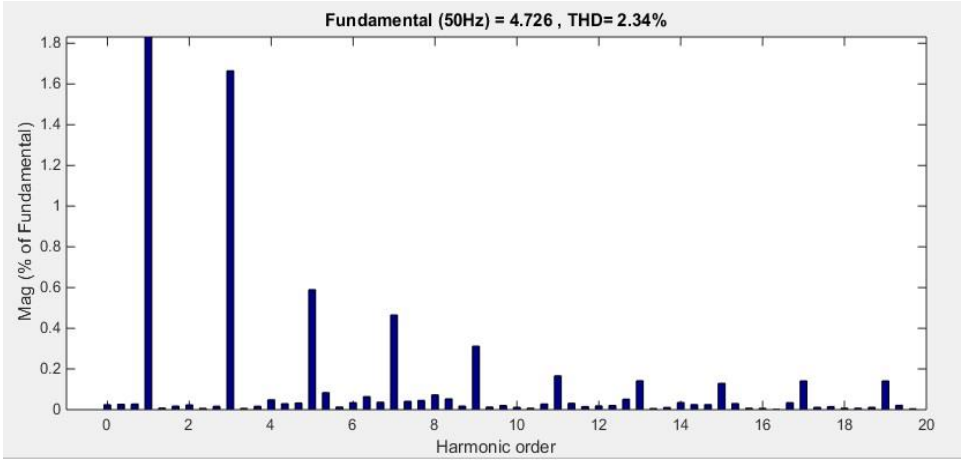

Figure.3.10 (c)

Figure.3.10 FFT Spectra of seven level single phase inverter with R-L load using GPI voltage controller (a) Output voltage without filter (b) output voltage with filter (c) Output current.

3.4. Three Phase Inverter:

The Simulink model of three phase seven level inverter with separated DC sources is shown in Figure 3.11. Each phase consists of three H-Bridges and three equal values of DC voltage sources. The Simulation results and FFT analysis of seven level three phase inverter are shown in Figure 3.12 and Figure 3.13 respectively.

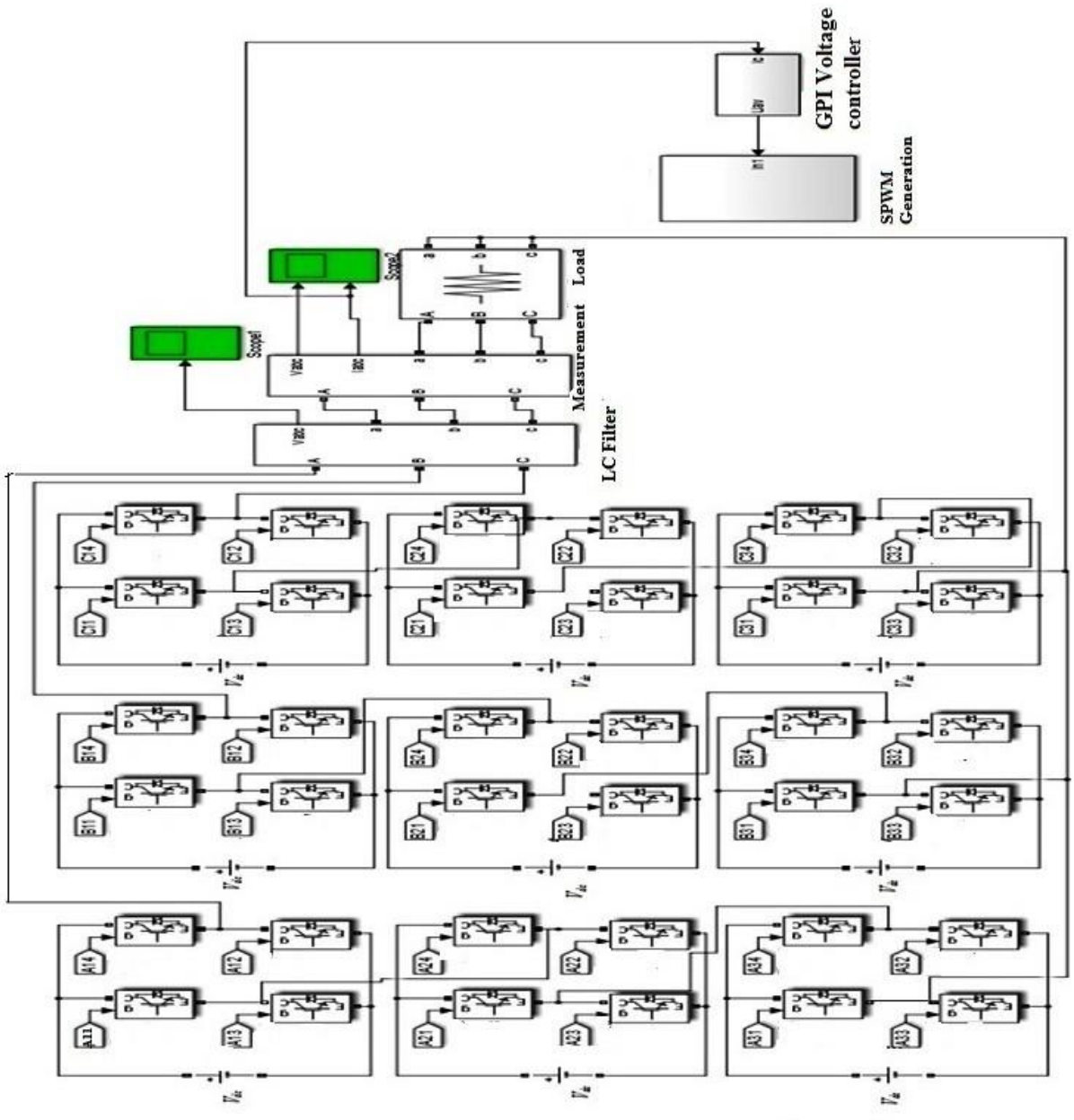

Figure.3.11 Simulink Model for seven level three phase inverter with GPI voltage controller.

The simulation results of output voltage with and without filter and current for seven level three phase inverter with resistive load are shown in Figure.3.9, Figure.3.10 respectively.

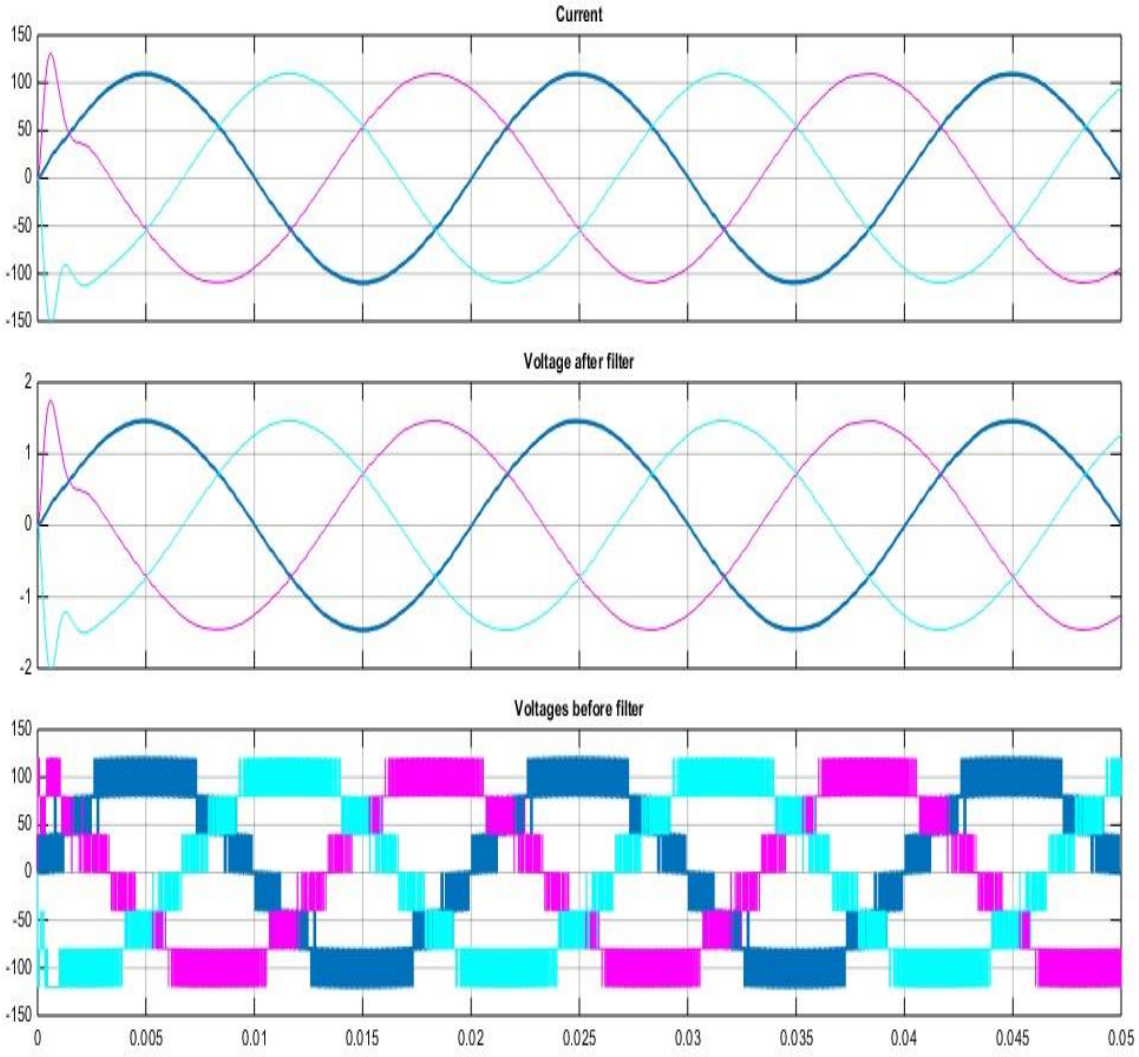

Figure.3.12 Current and voltage (with and without filter) waveforms for seven level three phase inverter with resistive load using GPI voltage controller.

The FFT analysis of output voltage and output current for three phase seven level inverter are shown in Figure.3.13, and it shows the THD of voltage and current for one phase of three phase seven level inverter. The remaining phases exhibit same THD.

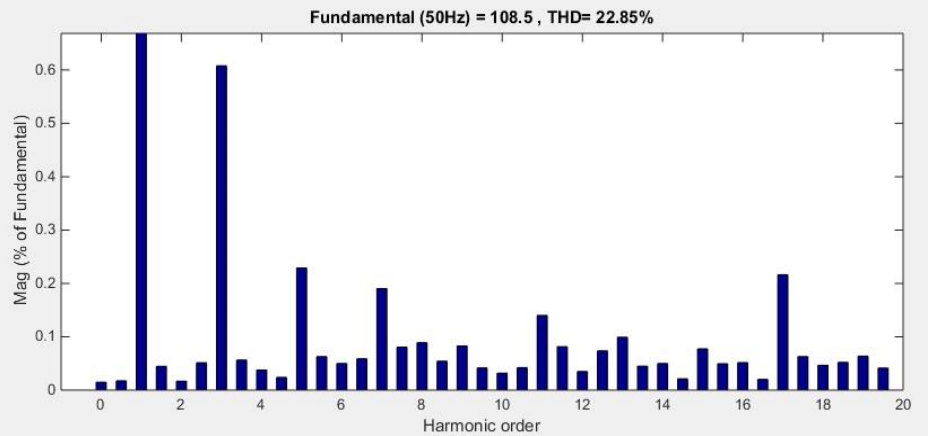

Figure.3.13 (a)

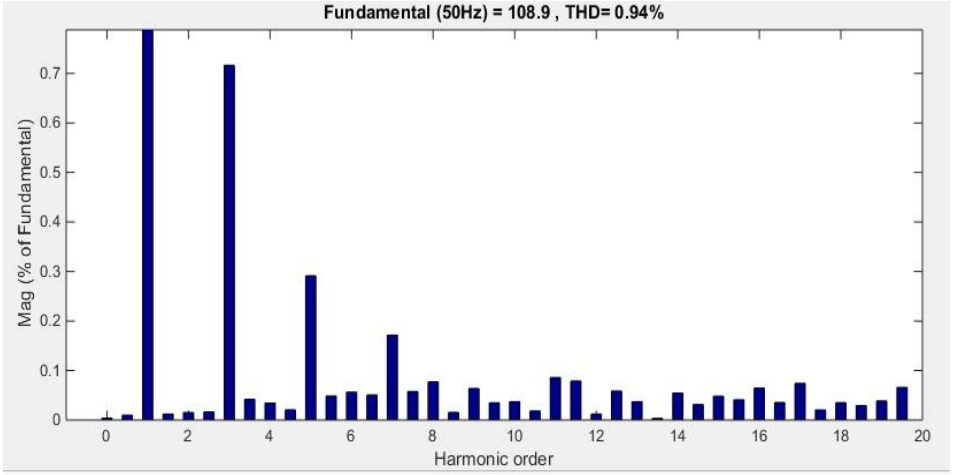

Figure.3.13 (b)

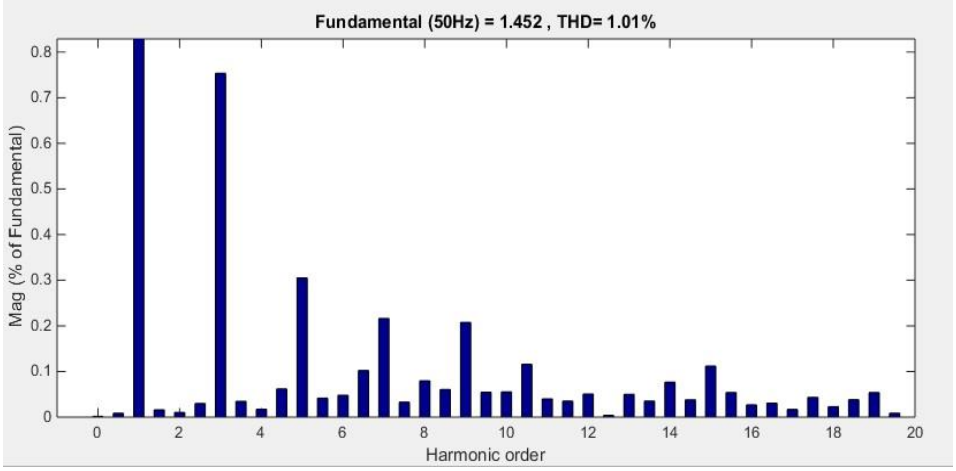

Figure.3.13 (c)

Figure.3.13 FFT Spectra of seven level three phase inverter with resistive load (a) Output voltage without filter (b) output voltage with filter (c) Output current.

3.4. Generalized Proportional Integral Tracking Controller with output current as feedback

GPI controller is robust hence, in this work; we have used a GPI controller with output current as a feedback for cascade multi-level Inverter. GPI current controller helps to maintain the desired current level at the load by tracking the reference current signal.

The mathematical model of the cascaded multilevel single phase inverter is given by

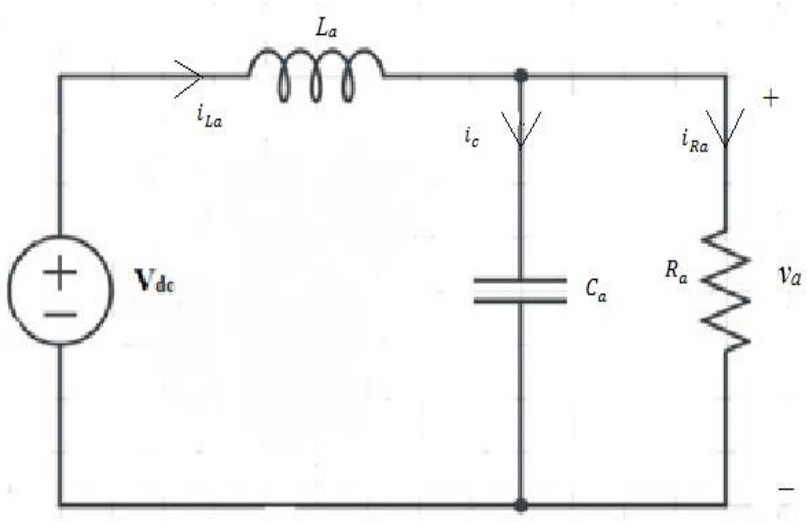

Figure.3.14 Equivalent circuit for single phase inverter.

Applying KVL and KCL to the above circuit

$$L_a \frac{di_a}{dt} = -v_a + V_{dc}u_{ai} \tag{3.26}$$

$$C_a \frac{dv_a}{dt} = i_{La} - \frac{1}{R_a} v_a \tag{3.27}$$

$$V_{c1} = i_{Ra}R_a \tag{3.28}$$

Where i_a is the current through the inductor, v_a is voltage across capacitor and u_{ai} is denotes control input taking discrete values between [-1 1]. L_a, C_a represent Inductor and Capacitor respectively which act as a low pass filter. R_a denotes load resistance.

The control method is based on the state average model of the inverter with control input u replaced with a signal u_{ai} ; where, u_{ai} is a continuous signal in time and it takes the values between -1 to 1.

$$i_{La} = C_a \frac{dV_{ca}}{dt} + \frac{1}{R_a} v_{ca} \tag{3.29}$$

$$i_{La} = i_{Ra} + R_a Ca \frac{di_{Ra}}{dt} \tag{3.30}$$

$$V_{dc} u_{ai} = \frac{L_a R_a Ca}{V_{dc}} \left(\frac{d^2 i_{Ra}}{dt^2}\right) + \frac{L_a}{V_{dc}} \left(\frac{di_{Ra}}{dt}\right) + \frac{R_a}{V_{dc}} i_{Ra} \tag{3.31}$$

The average model of the inverter is flat i.e., control signal can be expressible in terms of flat output, denoted by I , and this output is equal to current through the load resistance R_a.

$$u_{ai}(t) = \frac{L_a Ca}{V_{dc}} \left(\frac{d^2 I}{dt^2}\right) + \frac{L_a}{R_a V_{dc}} \left(\frac{dI}{dt}\right) + \frac{1}{V_{dc}} I \tag{3.32}$$

$$i_{Ra} = I \tag{3.33}$$

$$V_{dc} u_{ai} = \frac{L_a R_a Ca}{V_{dc}} \left(\frac{d^2 i_{Ra}}{dt^2}\right) + \frac{L_a}{V_{dc}} \left(\frac{di_{Ra}}{dt}\right) + \frac{R_a}{V_{dc}} i_{Ra} \tag{3.31}$$

On integrating Eq(3.26), we get

$$i_{La}\,(\mathrm{t}) = i_{La}\,(0) + \frac{1}{L_a} \int_0^t [V_{dc}\, u_{ai}(\beta) - v_{Ca}\,(\beta)\,]\, d\,\beta \tag{3.32}$$

$$\hat{\imath}_{La}(\mathrm{t}) = \frac{1}{L_a} \int_0^t [V_{dc}\, u_{ai}(\beta) - v_{Ca}\,(\beta)\,]\, d\,\beta \tag{3.32}$$

$$\dot{I} = i_{Ra} \tag{3.33}$$

$$\hat{I} = \frac{1}{R_a C_a} [\hat{\imath}_{La} - i_{Ra}] \tag{3.34}$$

$$= \frac{1}{L_a R_a Ca} \int_0^t [V_{dc}\, u_{ai}(\beta) - i_{Ra}\, R_a] d\beta - \frac{1}{R_a Ca}\, i_{R_a} \tag{3.35}$$

$$\dot{I} = \hat{\dot{I}} + \dot{I}_0 \tag{3.36}$$

Where $\dot{I}$ denotes unknown initial rate of change of current. Consider a sinusoidal signal with known constant amplitude A_m and constant known frequency ω_n *i.e.* $I_{Ra}^*(t) = A_m \sin(\omega_n * t)$. It is desired to have the output current of the inverter track the signal with small tracking error independent of the time varying load current.

GPI feedback control law is given by

$$u_{ai}(t) = \frac{L_a Ca}{V_{dc}}\, i(t) + \frac{L_a}{R_a V_{dc}} \hat{I} + \frac{1}{V_{dc}}\, I \tag{3.38}$$

Where

$$i(t) = \ddot{I}^*(t) - s_3 \left[\hat{I}(t) - \dot{I}^*(t) \right] - s_2 [I(t) - I^*(t)] - s_1 \int_0^t [I(\beta) - I^*(\beta)]\, d\beta - s_0 \int_0^t \int_0^\sigma [I(\Omega) - I^*(\Omega)] d\Omega \tag{3.39}$$

$$I^*(t) = A_m \sin(\omega_n t),$$

$$\ddot{I}^*(t) = -A_m \omega_n^2 \sin(\omega_n t)$$

$$\dot{I}^*(t) = A_m \omega_n \cos(\omega_n t) \tag{3.40}$$

Let $e = I(t) - I^*(t)$ represents tracking error. The closed loop system is formed from equations (12) and (4).Error dynamics given by

$$e^4 + k_3 e^3 + k_2 \ddot{e} + k_1 \dot{e} + k_o e = -\frac{1}{C_a} \frac{d^3}{dt^3}\, i_{Ra}(t) \tag{3.41}$$

If k_3, k_2, k_1, k_0 are the coefficients of the linear dynamics of above equation are chosen such that the polynomial in the complex variable s can be given by:

$$e(s) = s^4 + k_3 s^3 + k_2 s^2 + k_1 s + k_0 \quad (3.42)$$

The desired Hurwitz polynomial can then be written as:

$$p_d(s) = (s^2 + 2\xi\omega_n s + \omega_n^2)^2 \quad (3.43)$$

And the gains of GPI controller will be given by:

$$s_3 = 4\xi\omega_n \quad (3.44)$$

$$s_2 = 4\xi^2\omega_n^2 + 2\omega_n^2 \quad (3.45)$$

$$s_1 = 4\xi\omega_n^2 \quad (3.46)$$

$$s_0 = \omega_n^4 \quad (3.47)$$

The pole location of the above characteristic polynomial sufficiently far in left half complex plane in order to reduce effects of nonlinear load in the closed loop. The roots were located at $(-2812 - 2525.52j)^2$ and $(-2812 + 2525.52j)^2$.

3.5. Simulation results

3.5.1. Single Phase Inverter

The Simulink model for GPI current controller is shown in Figure.3.15. The output load current has taken as feedback.

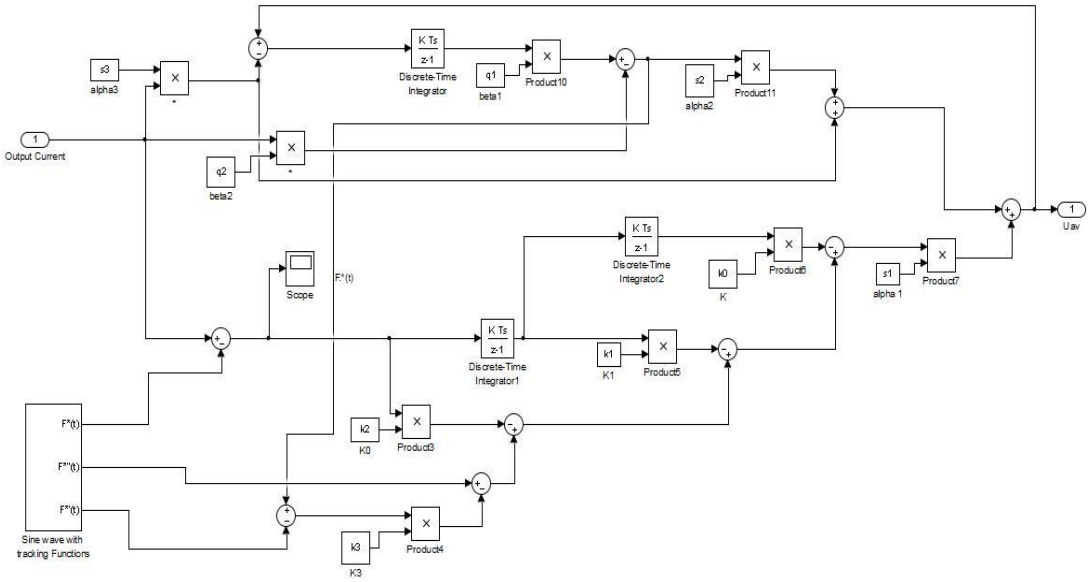

Figure.3.15 Simulink model of GPI current Controller.

3.5.2. R-Load:

Load resistance (R_L) = 75Ω

The simulation results and FFT analysis of output voltage with and without filter and current for seven level single phase inverter are shown in Figure.3.16, Figure.3.17 respectively.

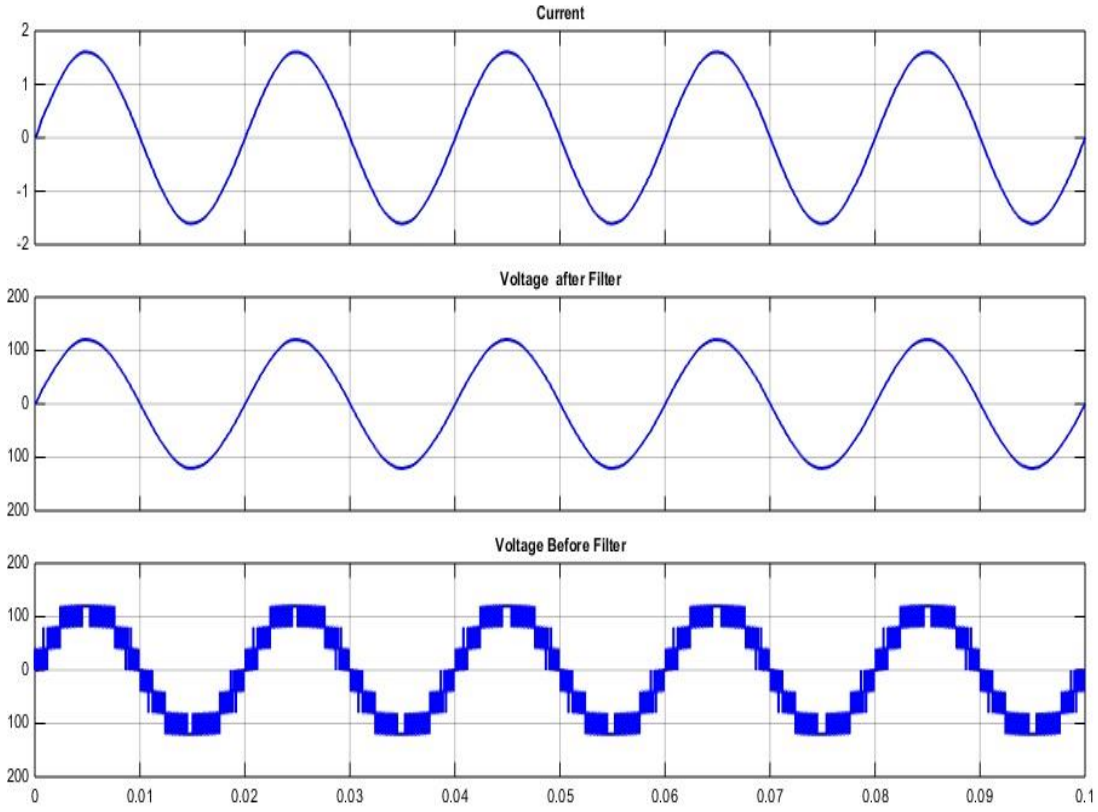

Figure.3.16 Current and voltage (with and without filter) waveforms for seven level single phase inverter with resistive load using GPI current controller.

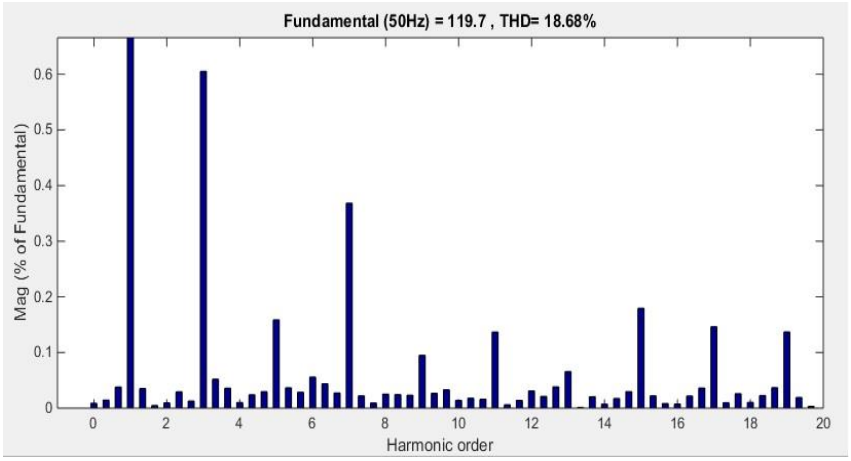

Figure.3.17 (a)

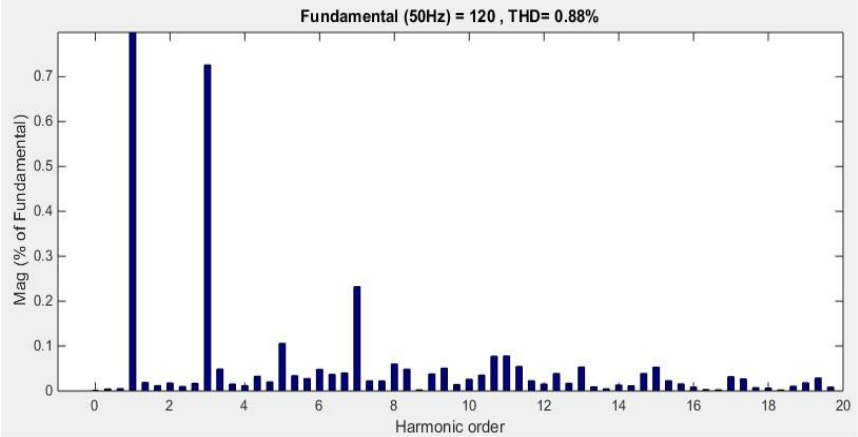

Figure.3.17 (b)

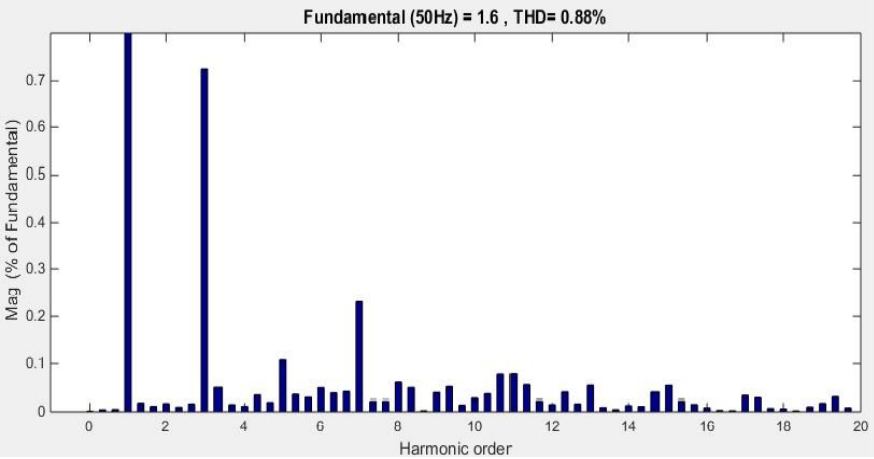

Figure.3.17 (c)

Figure.3.17 FFT Spectra of seven level single phase inverter with resistive load using GPI current controller (a) Output voltage without filter (b) output voltage with filter (c) Output current.

3.5.3. R-L load:

Load resistance (R_L) = 75Ω

Load Inductance (L) = 150mH

The simulation results and FFT analysis of output voltage with and without filter and current for seven level single phase inverter are shown in Figure.3.18, Figure.3.19 respectively.

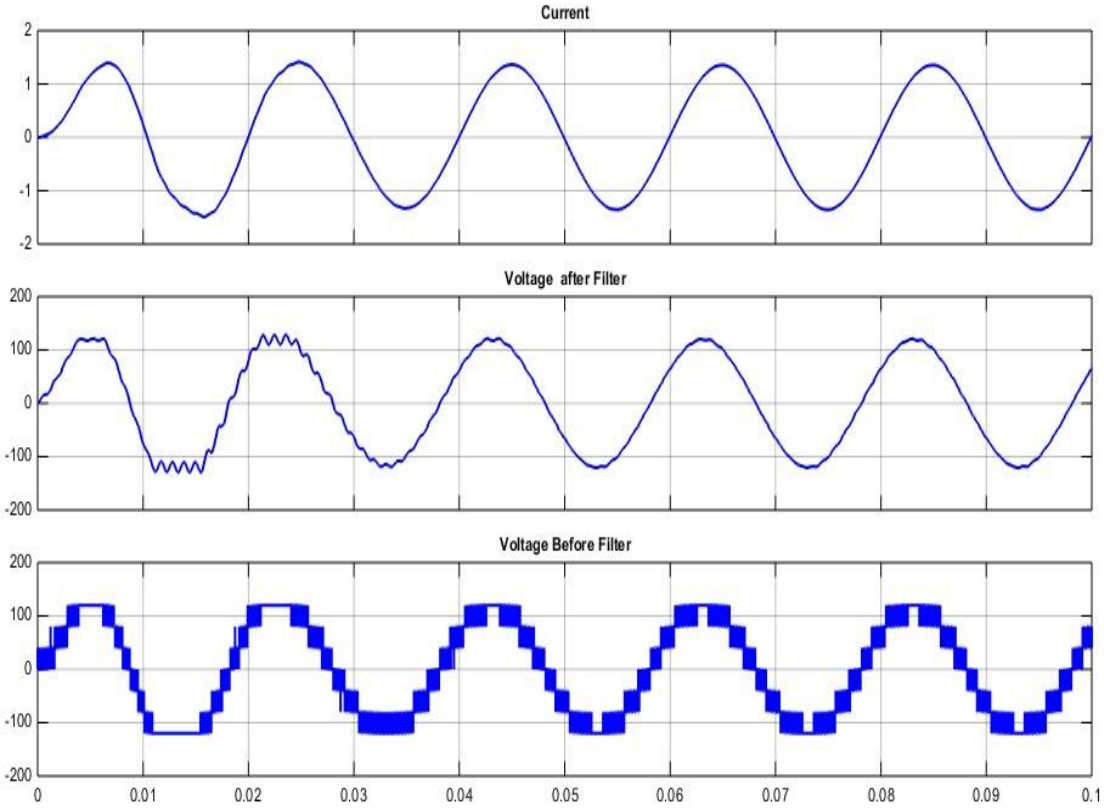

Figure.3.18 Current and voltage (with and without filter) waveforms for seven level single phase inverter with R-L load using GPI current controller.

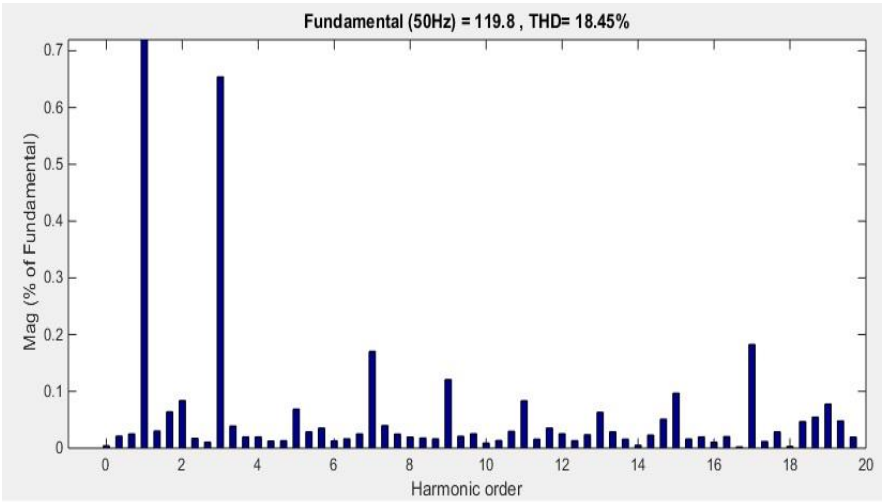

Figure.3.19 (a)

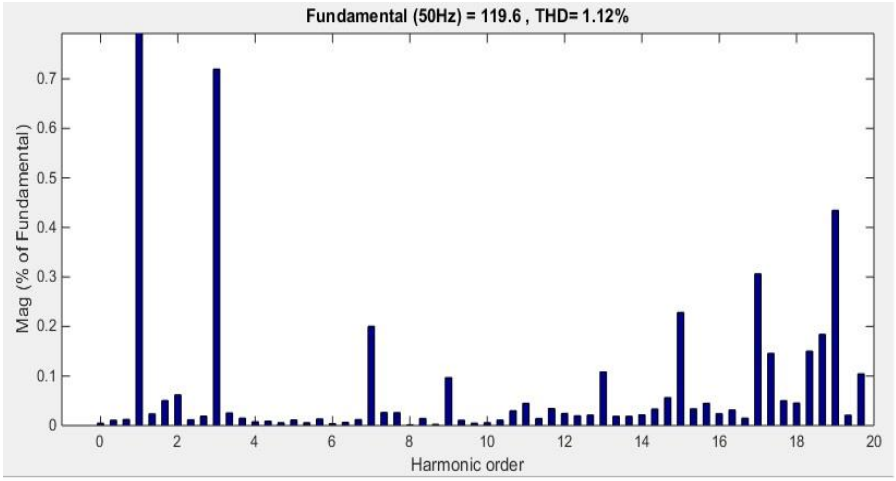

Figure.3.19 (b)

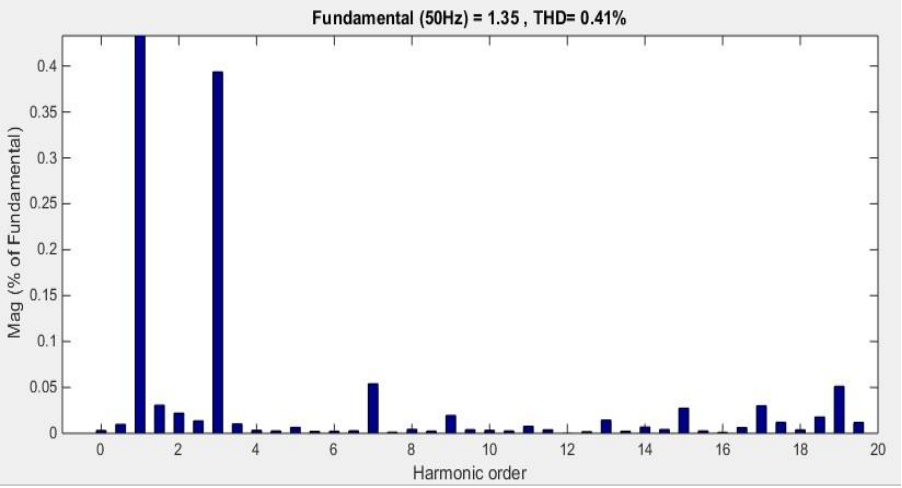

Figure.3.19 (c)

Figure.3.19 FFT Spectra of seven level single phase inverter with R-L load using GPI current controller (a) Output voltage without filter (b) output voltage with filter (c) Output current.

3.6. Three Phase Inverter

The simulation results of output voltage with and without filter and current for seven level three phase inverter with resistive load are shown in Figure.3.20, Figure.3.21 respectively.

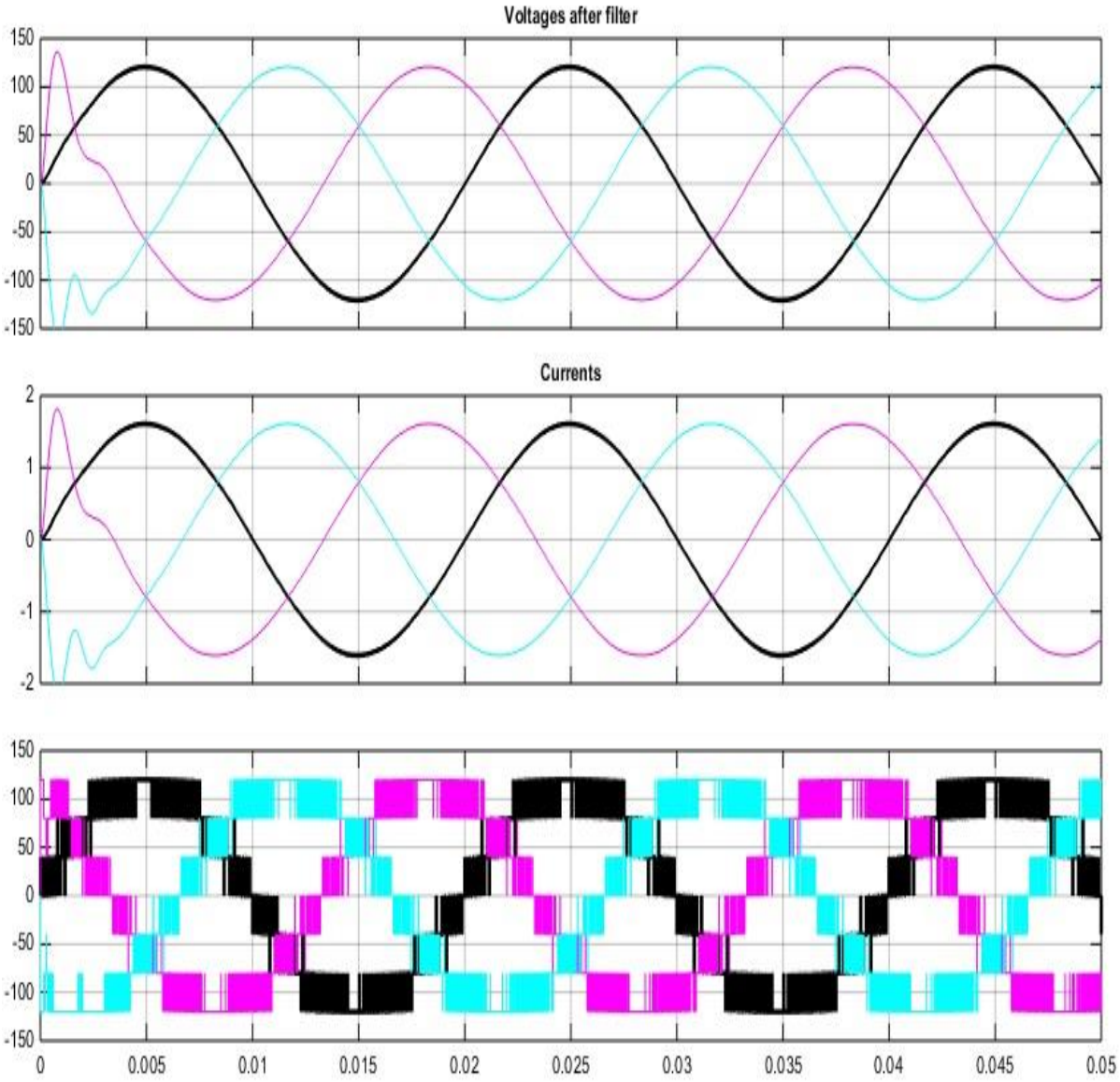

Figure.3.20 Current and voltage (with and without filter) waveforms for seven level three phase inverter with resistive load using GPI current controller.

The FFT analysis of output voltage and output current for three phase seven level inverter are shown in Figure.3.21, and it shows the THD of voltage and current for one phase of three phase seven level inverter. The remaining phases exhibit same THD.

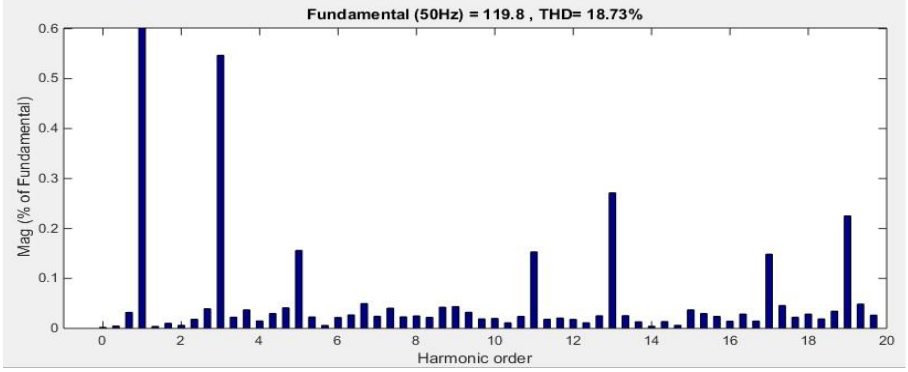

Figure.3.21 (a)

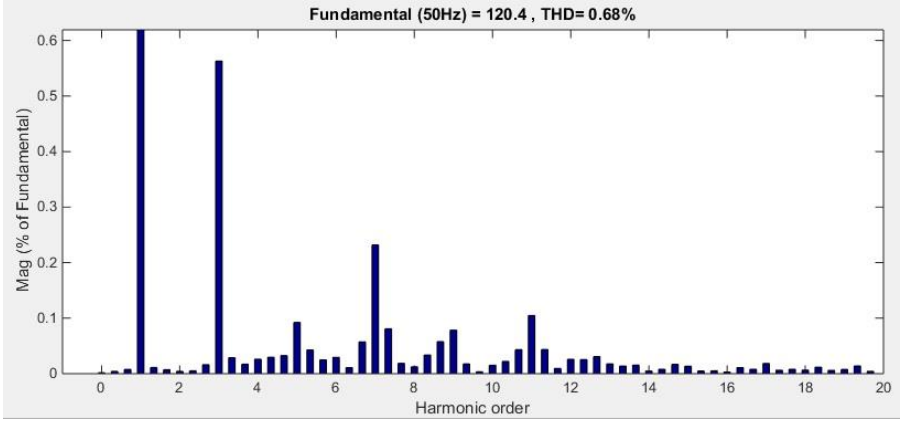

Figure.3.21 (b)

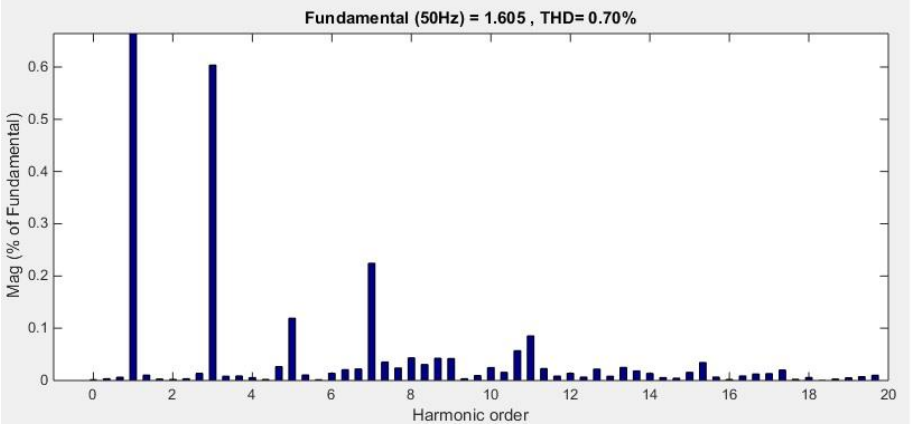

Figure.3.21 (c)

Figure.3.21 FFT Spectra of seven level three phase inverter with resistive load using GPI current controller (a) Output voltage without filter (b) output voltage with filter (c) Output current.

3.7. Discussions:

From the above simulation results the THD values for voltage and current are shown in TABLE 3.2. The designed single phase and three phase inverters are produces seven level of output voltage. From the table.3.2 it is observed that in each case the THD of voltage with filter and current is less than 3.0% and also GPI current controller gives less distortion than GPI voltage controller.

TABLE 3.2

THD of multilevel inverter using GPI controller

Controller	Multilevel inverter	Load	THD_v(%) without filter	THD_v(%) with filter	THD_i(%)
GPI voltage Controller	Single Phase	R Load	21.87	1.65	2.38
		R-L Load	22.29	1.56	2.34
	Three Phase	R Load	22.85	0.94	1.01
GPI current Controller	Single Phase	R Load	18.68	0.88	0.88
		R-L Load	18.45	1.12	0.41
	Three Phase	R Load	18.73	0.68	0.70

CHAPTER 4

Cascaded multilevel inverter with reduced number of power electronic components

CHAPTER 4

Cascaded multilevel inverter with reduced number of power electronic components

Depending on the DC voltage source magnitude, the cascade multilevel inverters can be divided into two groups such as Asymmetric design and symmetric design. In the symmetric design [29], the DC voltage source magnitude is equal for all single phase H-bridges and in asymmetric model [30] the magnitudes of DC source voltages are unequal for all single phase H-bridges.

4.1. Seven level inverter:

The design of seven level cascade inverter [31] consists of two unequal magnitudes of DC voltage sources (V_1, V_2) and six power electronic switches (S_1, S_2 , S_3 , S_4 , S_a, S_b). The switches S_a, S_b cannot be turn on simultaneously to avoid short circuits. The schematic model for 7- level inverter with reduced number of power electronic switches and DC voltage sources is shown in Figure.4.1.

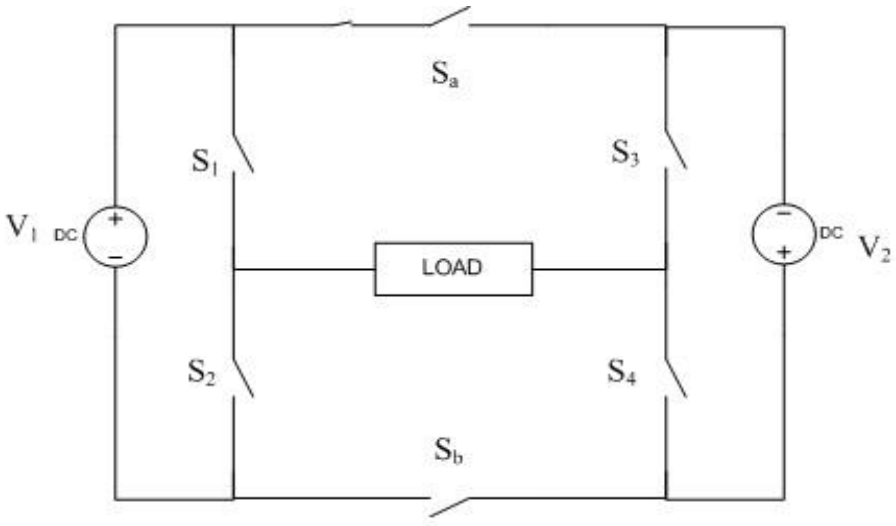

Figure.4.1 Seven level single phase inverter with new topology.

The values of DC voltage sources of 7-level cascade inverter are

$$V_1 = V_{dc} \tag{4.1}$$

$$V_2 = 2V_{dc} \tag{4.2}$$

From these DC voltage sources the designed 7-level inverter can produce seven output voltage levels such as 0, V_{dc}, + $2V_{dc}$, + $3V_{dc}$, -V_{dc}, - $2V_{dc}$, -$3V_{dc}$.

The switching scheme for proposed 7-level cascade inverter is shown in TABLE 4.1

TABLE 4.1

Output voltages of the seven level single phase inverter

Serial No	S_1	S_2	S_3	S_4	S_a	S_b	V_0
1	1	0	0	1	0	1	V_1
2	0	1	1	0	0	1	V_2
3	1	0	1	0	0	1	$(V_1 + V_2)$
4	0	1	0	1	0	1	0
5	0	1	1	0	1	0	$- V_1$
6	1	0	0	1	1	0	$-V_2$
7	0	1	0	1	1	0	$-(V_1 + V_2)$

4.2. 9- level, 13-level and 15-level inverters:

The 9-level, 13-level and 15-level inverters have been developed from the seven level inverter as shown in Figure.4.2 and Figure.4.3 respectively. The 9-level inverter topology consists of three DC voltage sources and 8 switches. The 13-level, 15-level inverter design

comprises of Three DC voltage sources and ten power switches. The same design is generating 9-level, 11-lvel, 13-level and 15-level output voltages with different magnitudes of DC voltage sources. The magnitudes of DC voltage sources and output voltage levels are shown in TABLE 4.2 below and switching topology of 15-level inverter is shown in TABLE 4.3 respectively.

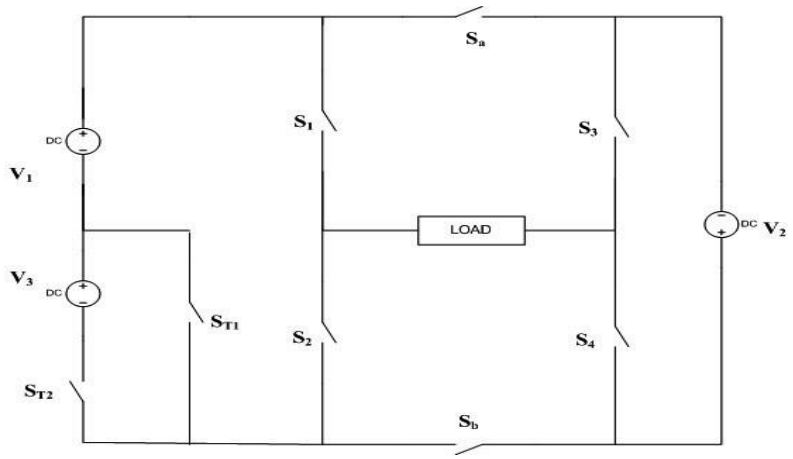

Figure.4.2 Nine level inverter new topology.

TABLE 4.2

The magnitudes of DC voltage sources

Voltage source	9-level	11-level	13-level	15-level
V_1	V_{dc}	V_{dc}	V_{dc}	V_{dc}
V_2	$2V_{dc}$	$2V_{dc}$	$2V_{dc}$	$2V_{dc}$
V_3	V_{dc}	$2V_{dc}$	$3V_{dc}$	$4V_{dc}$

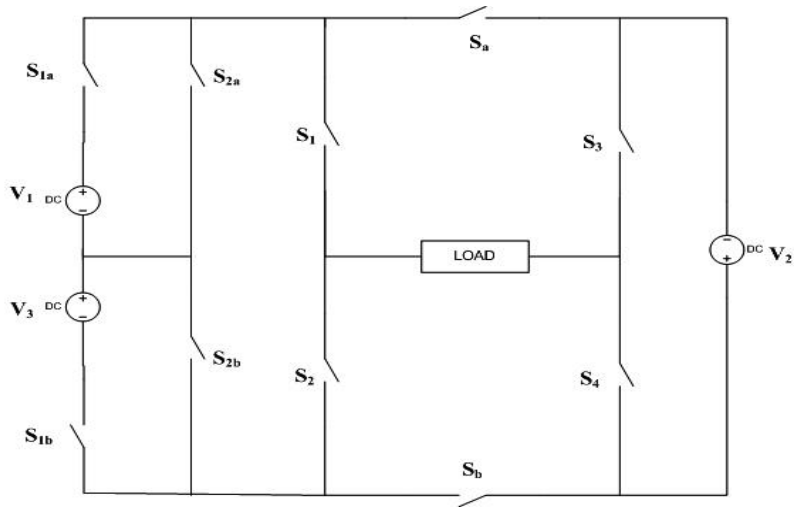

Figure.4.3 Proposed multilevel inverter (13 and 15 levels).

TABLE 4.3

Switching scheme of 15-level inverter

No	S_1	S_2	S_3	S_4	S_a	S_b	S_{1a}	S_{2a}	S_{1b}	S_{2b}	Output Voltage
1	0	1	0	1	0	1	0	0	0	1	0
2	1	0	0	1	0	1	1	0	0	1	V_1
3	0	1	1	0	0	1	0	0	0	0	V_2
4	1	0	1	0	0	1	1	0	0	1	$(V_2+ V_1)$
5	1	0	0	1	0	1	0	1	1	0	V_3
6	1	0	0	1	0	1	1	0	1	0	$(V_3+ V_1)$
7	1	0	1	0	0	1	0	1	1	0	$(V_2+ V_3)$
8	1	0	1	0	0	1	1	0	1	0	$(V_2 + V_1 + V_3)$
9	0	1	1	0	1	0	1	0	0	1	$-V_1$
10	1	0	0	1	1	0	0	0	0	0	$-V_2$
11	0	1	0	1	1	0	1	0	0	1	$-(V_2+ V_1)$
12	0	1	1	0	1	0	0	1	1	0	$-V_3$
13	0	1	1	0	1	0	1	0	1	0	$-(V_3 + V_1)$
14	0	1	0	1	1	0	0	1	1	0	$-(V_2 + V_3)$
15	0	1	0	1	1	0	1	0	1	0	$-(V_2 + V_1 + V_3)$

4.3. 31- Level Inverter:

The different topology for 31 level single phase inverter is shown in Figure.4.4 and the switching pattern is shown in TABLE 4.4. This inverter structure consists of four unequal magnitudes of DC voltage sources and ten power electronic switches. Other topologies require more number of power electronic switches and DC sources compare with above topology. The switches (S_1, S_2), (S_3, S_4), (S_5, S_6), (S_7, S_8) and (S_a, S_b) will not be turn-on simultaneously since if the power switches of these combination turn on simultaneously the DC voltage sources will be short circuited. To avoid short circuit the power switches will not be turn-on at the same time.

For this 31-level inverter topology the values of the number of power switches (M_{switch}), maximum output voltage (V_{max}), number of DC sources (M_{source}), voltage steps (M_{step}) are calculated as follows

$$M_{switch} = 4m + 2 \tag{4.3}$$

$$M_{source} = 2m \tag{4.4}$$

$$M_{step} = 2^{2m+1} - 1 \tag{4.5}$$

$$V_{max} = V_{L,m} + V_{R,m} \tag{4.6}$$

Where m represents the number of DC voltage sources on each leg.

The values of DC voltage sources of 31-level cascade inverter are

$$V_1 = 5V_{dc} \tag{4.7}$$

$$V_2 = V_{dc} \tag{4.8}$$

$$V_3 = 2V_{dc} \tag{4.9}$$

$$V_4 = 10V_{dc} \tag{4.10}$$

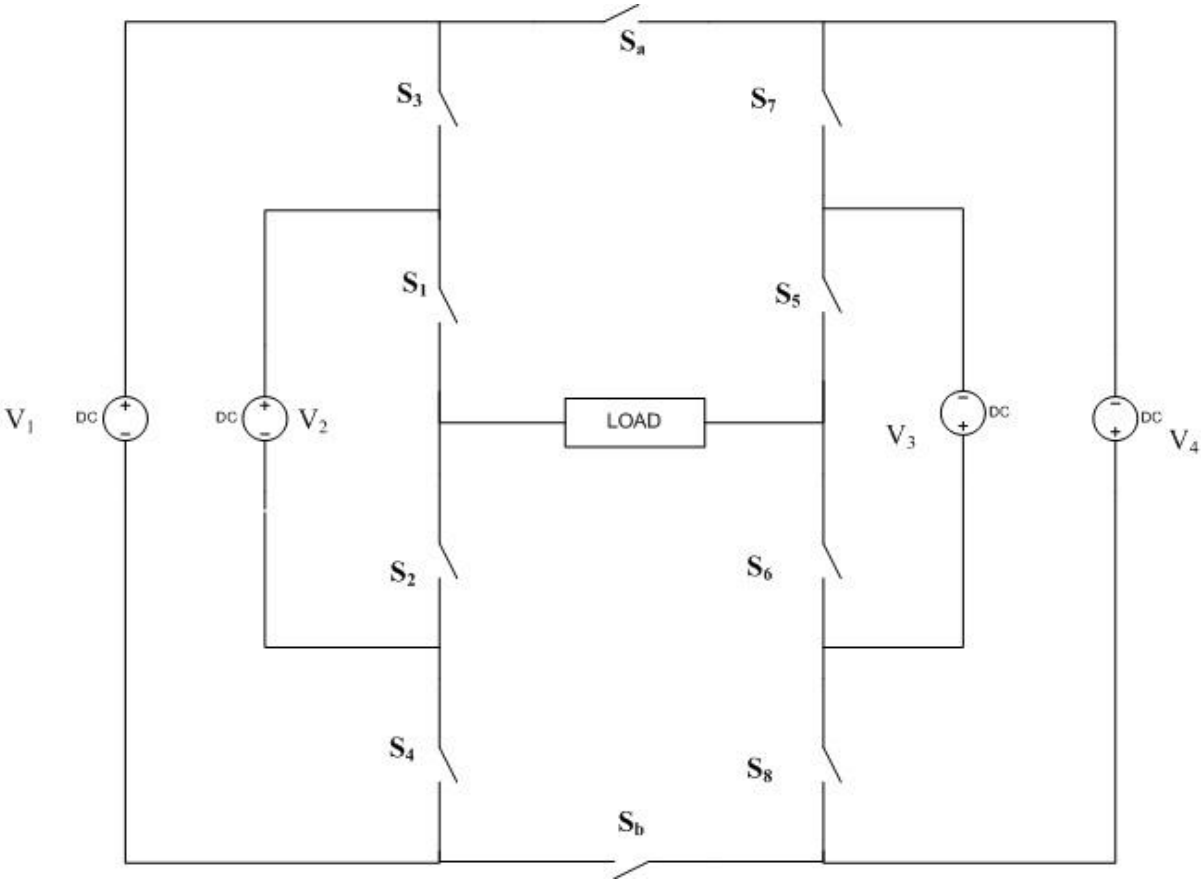

Figure.4.4 31-level inverter topology.

TABLE 4.4

Switching topology for 31-level inverter

No	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_a	S_b	V_0
1	1	0	1	0	1	0	1	0	0	1	$V_1 + V_4$
2	1	0	1	0	0	1	1	0	0	1	$V_4 + V_1 – V_2$
3	0	1	1	0	1	0	1	0	0	1	$V_4 + V_1 – V_3$
4	0	1	1	0	0	1	1	0	0	1	$V_1 + V_4 - V_2 - V_3$
5	1	0	1	0	1	0	0	1	0	1	$V_4 + V_2$
6	1	0	1	0	0	1	0	1	0	1	V_4
7	0	1	1	0	1	0	0	1	0	1	$V_2 - V_3 + V_4$

No	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_a	S_b	V_0
8	0	1	1	0	0	1	0	1	0	1	$V_4 - V_3$
9	1	0	0	1	1	0	1	0	0	1	$V_1 + V_3$
10	1	0	0	1	0	1	1	0	0	1	$V_1 + V_3 - V_2$
11	0	1	0	1	1	0	1	0	0	1	V_1
12	0	1	0	1	0	1	1	0	0	1	$V_1 - V_2$
13	1	0	0	1	1	0	0	1	0	1	$V_2 + V_3$
14	1	0	0	1	0	1	0	1	0	1	V_3
15	0	1	0	1	1	0	0	1	0	1	V_2
16	0	1	0	1	0	1	0	1	0	1	0
17	1	0	1	0	0	1	1	0	1	0	$- V_2$
18	0	1	1	0	1	0	1	0	1	0	$- V_3$
19	0	1	1	0	0	1	1	0	1	0	$- (V_2 + V_3)$
20	1	0	1	0	1	0	0	1	1	0	$- (V_1 - V_2)$
21	1	0	1	0	0	1	0	1	1	0	$- V_1$
22	0	1	1	0	1	0	0	1	1	0	$- (V_1 + V_3 - V_2)$
23	0	1	1	0	0	1	0	1	1	0	$- (V_1 + V_3)$
24	1	0	0	1	1	0	1	0	1	0	$- (V_4 - V_3)$
25	1	0	0	1	0	1	1	0	1	0	$- (V_2 - V_3 + V_4)$
26	0	1	0	1	1	0	1	0	1	0	$- V_4$
27	0	1	0	1	0	1	1	0	1	0	$- (V_4 + V_2)$
28	1	0	0	1	1	0	0	1	1	0	$- (V_1 + V_4 - V_2 - V_3)$
29	1	0	0	1	0	1	0	1	1	0	$- (V_4 + V_1 - V_3)$
30	0	1	0	1	1	0	0	1	1	0	$- (V_4 + V_1 - V_2)$
31	0	1	0	1	0	1	0	1	1	0	$- (V_1 + V_4)$

4.4. Simulation Results:

Load Resistance = 45 Ω and 75Ω

Load Inductance = 55mH and 60mH.

4.4.1. Seven level Inverter:

The Simulink model for 7-level inverter is shown in Figure.4.5 and the design parameters for 7-level inverter are given below

$V_1 = 30\,V$

$V_2 = 60\,V$

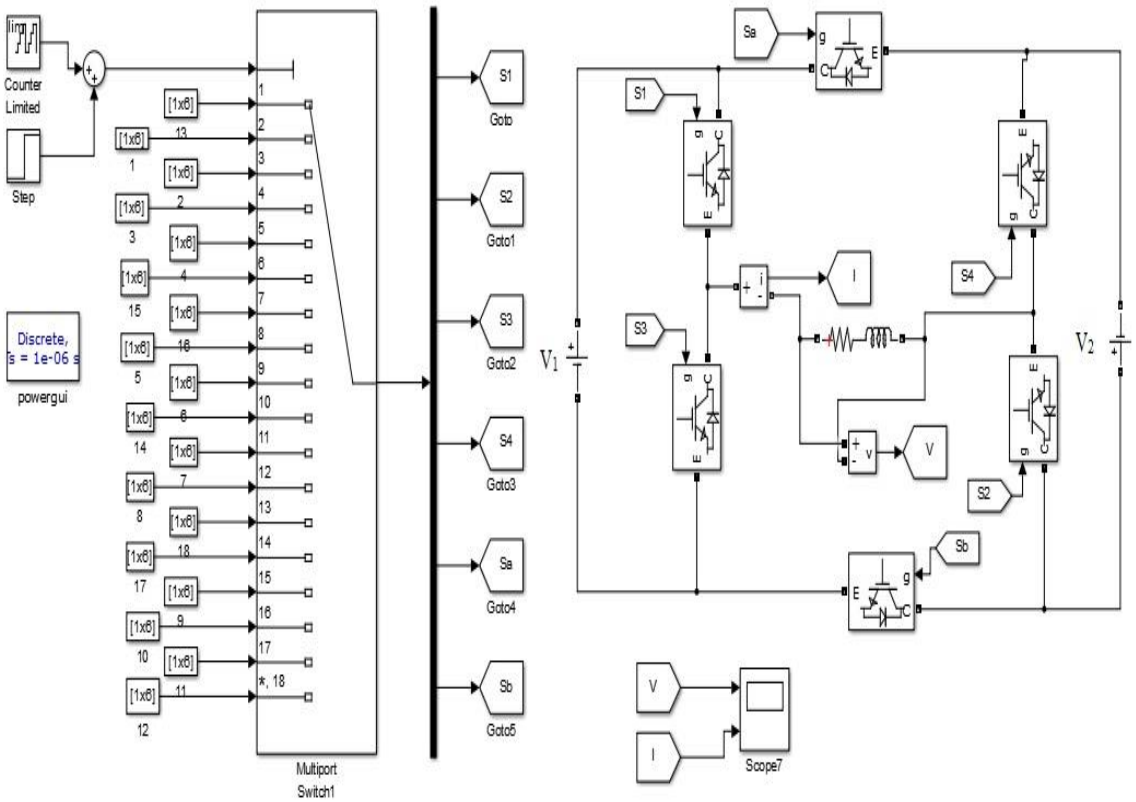

Figure.4.5 Simulink model of seven level inverter with new topology.

The simulation of output voltage and current waveforms for 7-level inverter are shown in Figure.4.6 and FFT analysis is shown in Figure.4.7 respectively.

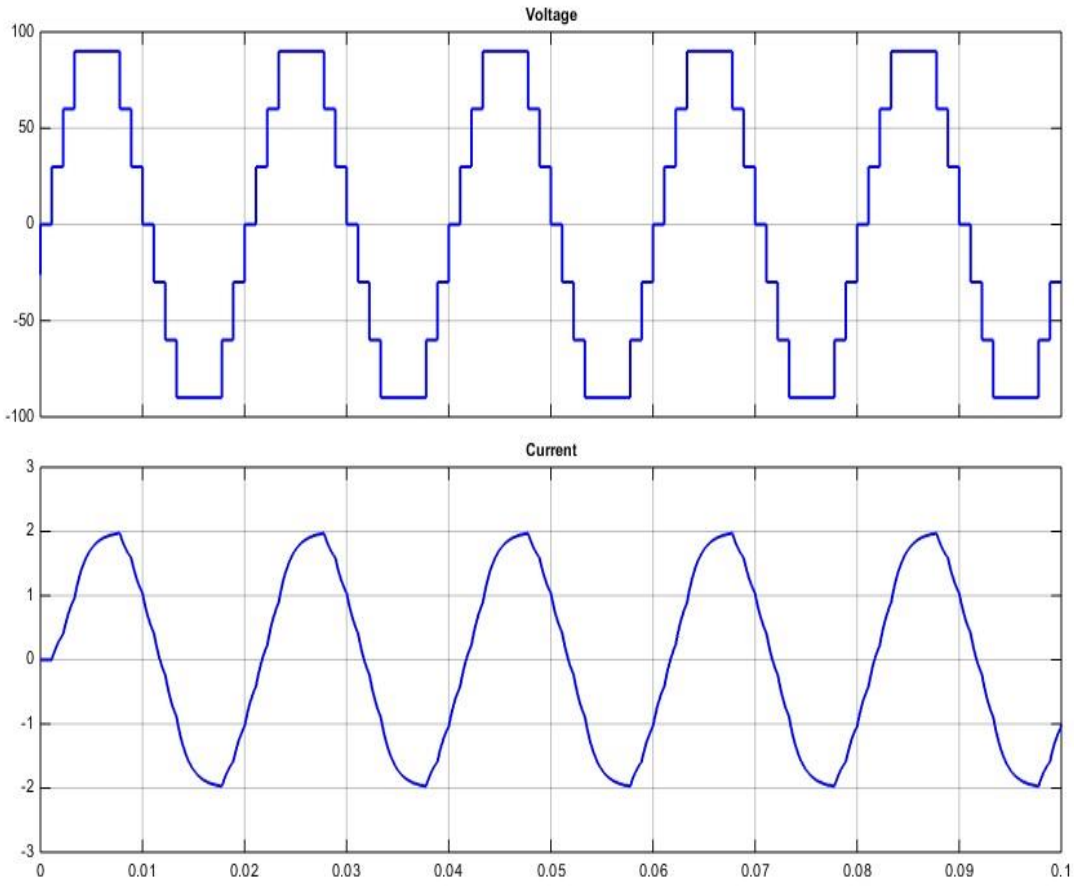

Figure.4.6 Output voltage and current of seven level inverter.

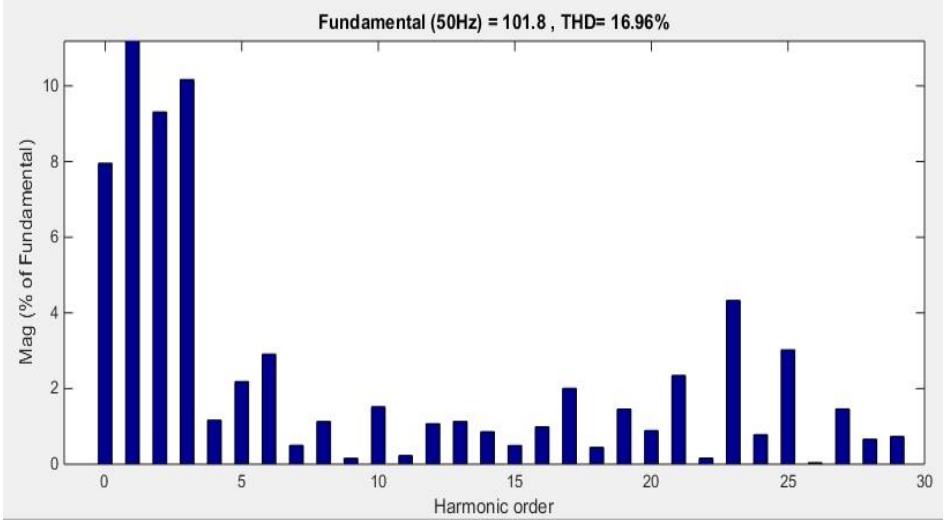

Figure.4.7 (a)

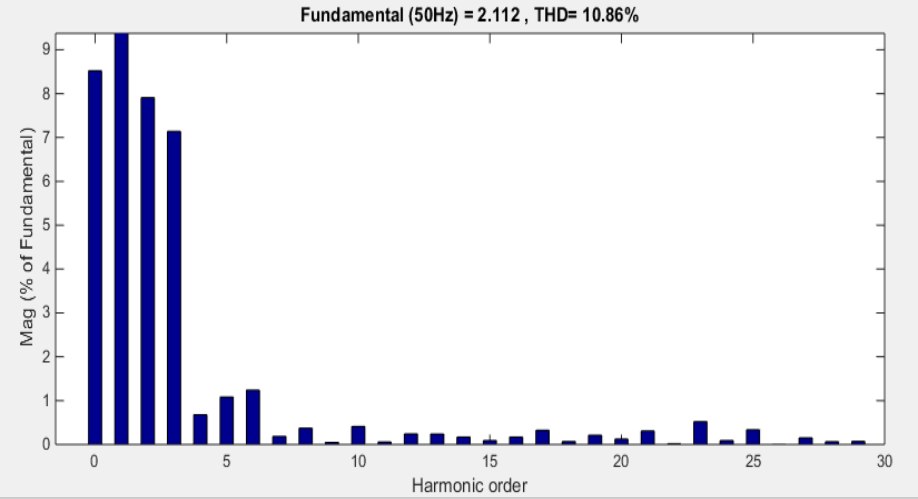

Figure.4.7 (b)

Figure.4.7 FFT Spectra of seven level single phase inverter with new topology

(a) Voltage (b) Current.

4.4.2. 9-level Inverter:

The Simulink model for 9-level inverter is shown in Figure.4.8 and the design parameters for 9-level inverter are given below

$V_1 = 30V$

$V_2 = 60V$

$V_3 = 30V$

The simulation results and FFT analysis of output voltage with and without filter and current for 9-level inverter are shown in Figure.4.9, Figure.4.10 respectively.

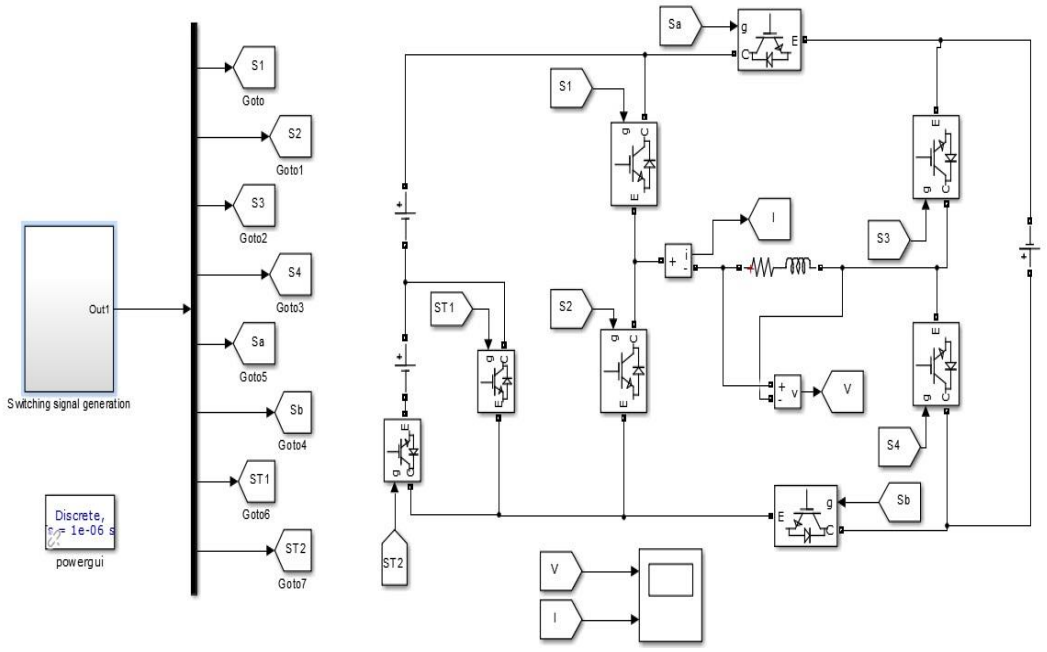

Figure.4.8 Matlab Simulink model for 9-level inverter.

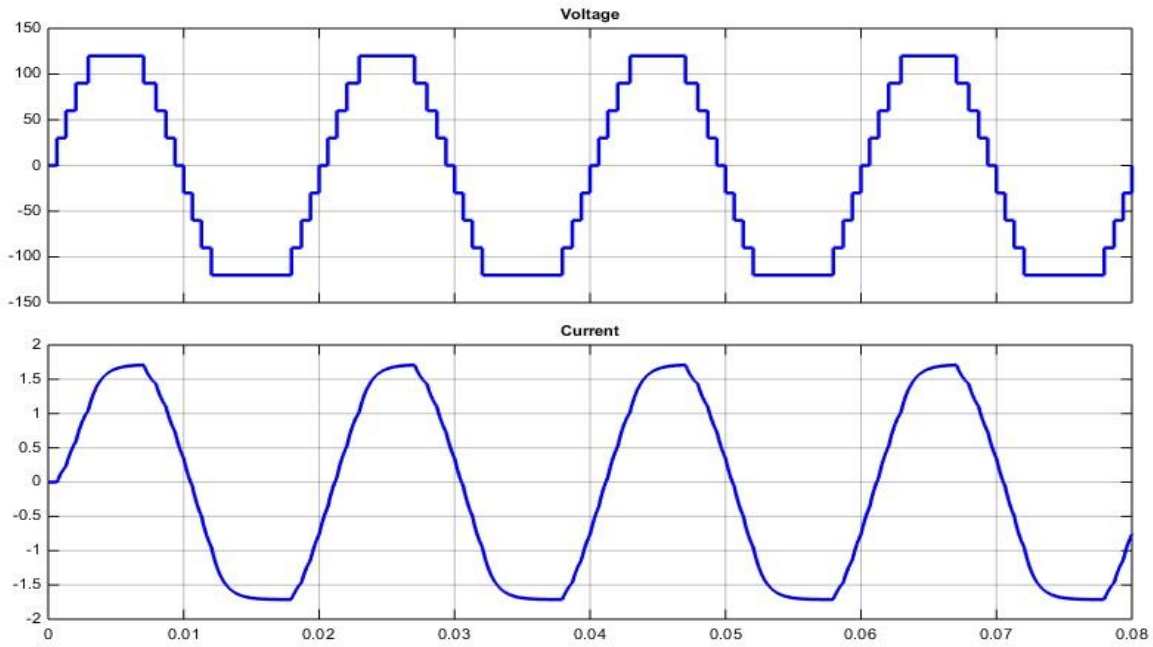

Figure.4.9 Output voltage and current of 9-level inverter.

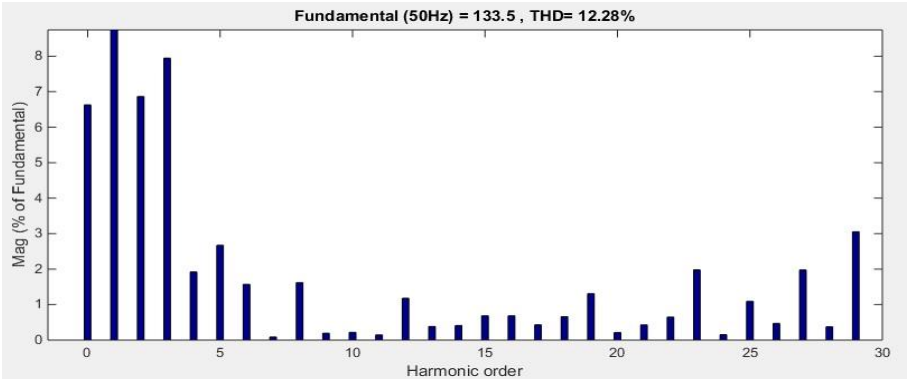

Figure.4.10 (1)

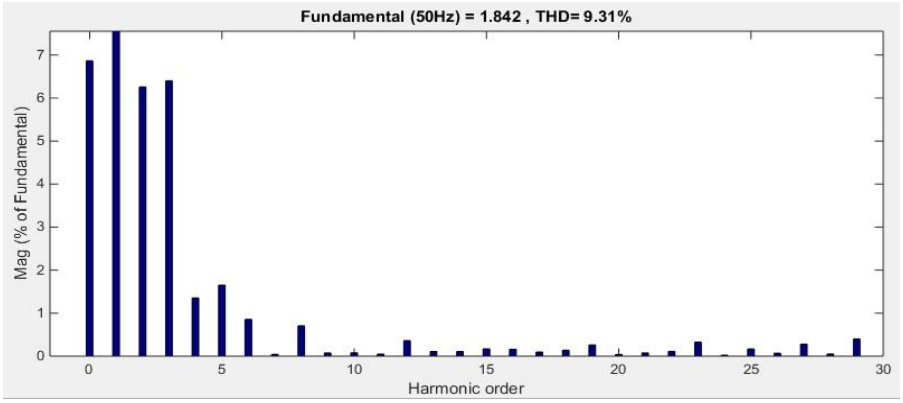

Figure.4.10 (2)

Figure.4.10 FFT spectrum of 9-level inverter (a) voltage (b) current.

4.4.3. 15-level inverters:

The Simulink model for 13-level as well as 15-level inverter is shown in Figure.4.11.

The DC voltage source magnitudes for 15-level inverter are given below and the simulation results and FFT analysis of output voltage with and without filter and current for 15-level inverter are shown in Figure.4.12, Figure.4.13 respectively.

$V_1 = 15V$

$V_2 = 30V$

$V_3 = 60V$

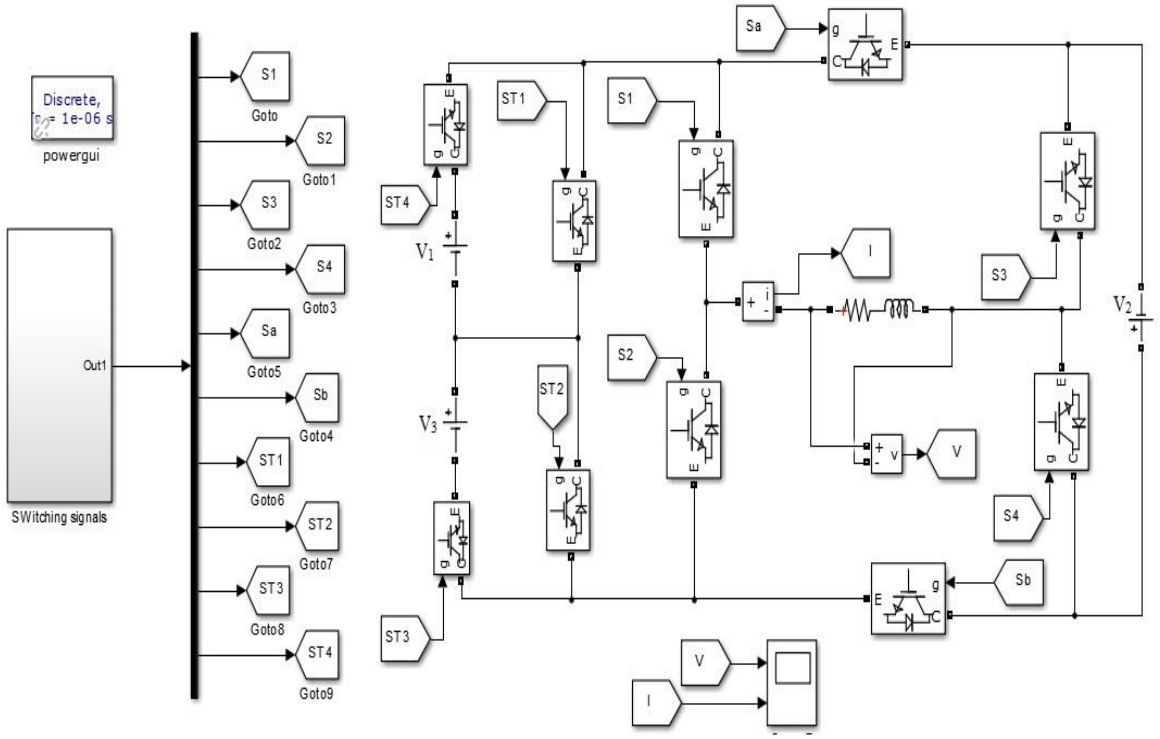

Figure.4.11 Matlab Simulink model for 15-level inverter

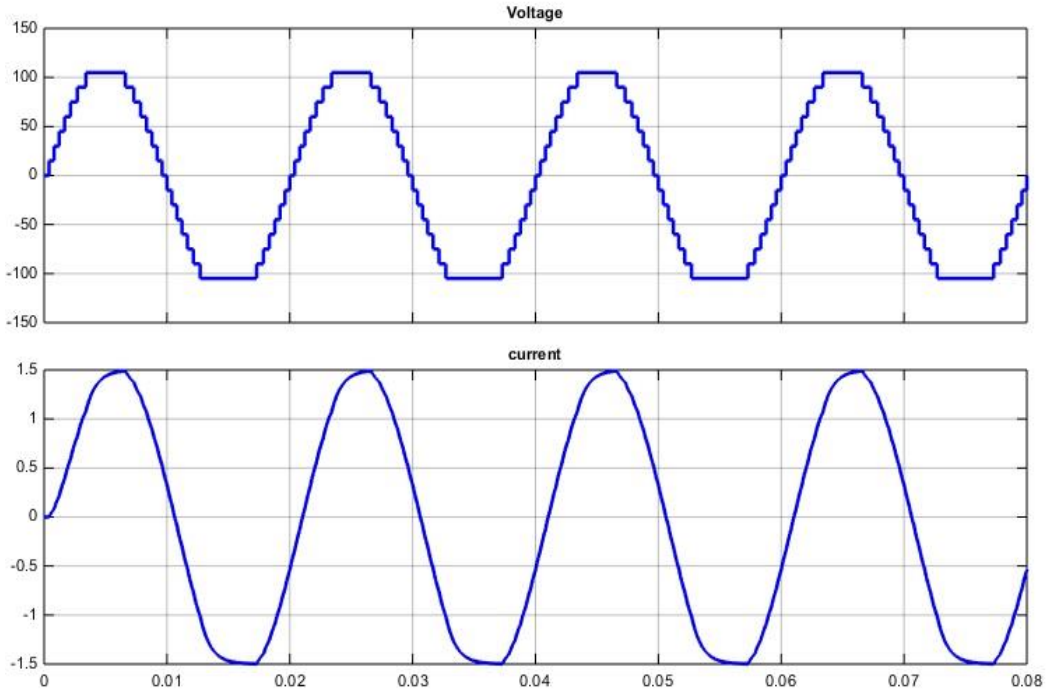

Figure.4.12 Output voltage and current of 15-level inverter.

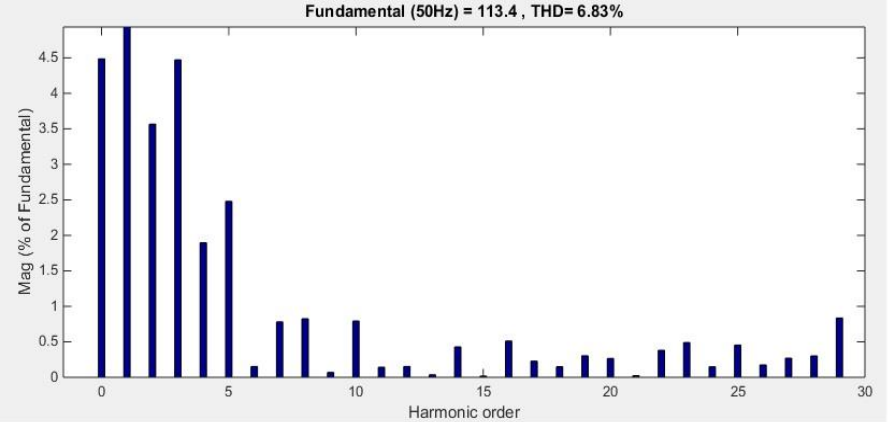

Figure.4.13 (a)

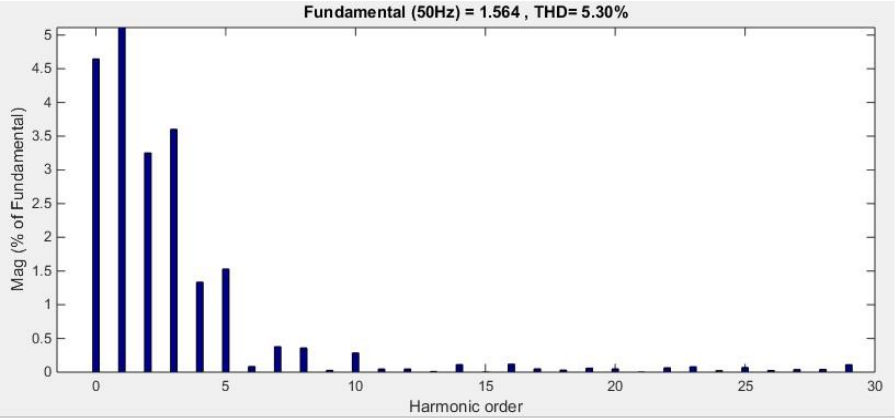

Figure.4.13 (b)

Figure.4.13 FFT spectrum of 15-level inverter (a) voltage (b) current.

4.4.4. 31-level Inverter:

The values of DC voltage sources of 31-level cascade inverter are

$V_1 = 75\ V$

$V_2 = 15\ V$

$V_3 = 30\ V$

$V_4 = 150\ V$

The simulation of output voltage and current waveforms for 31-level inverter are shown in Figure.4.14 and FFT analysis of output voltage and current is shown in Figure.4.15.

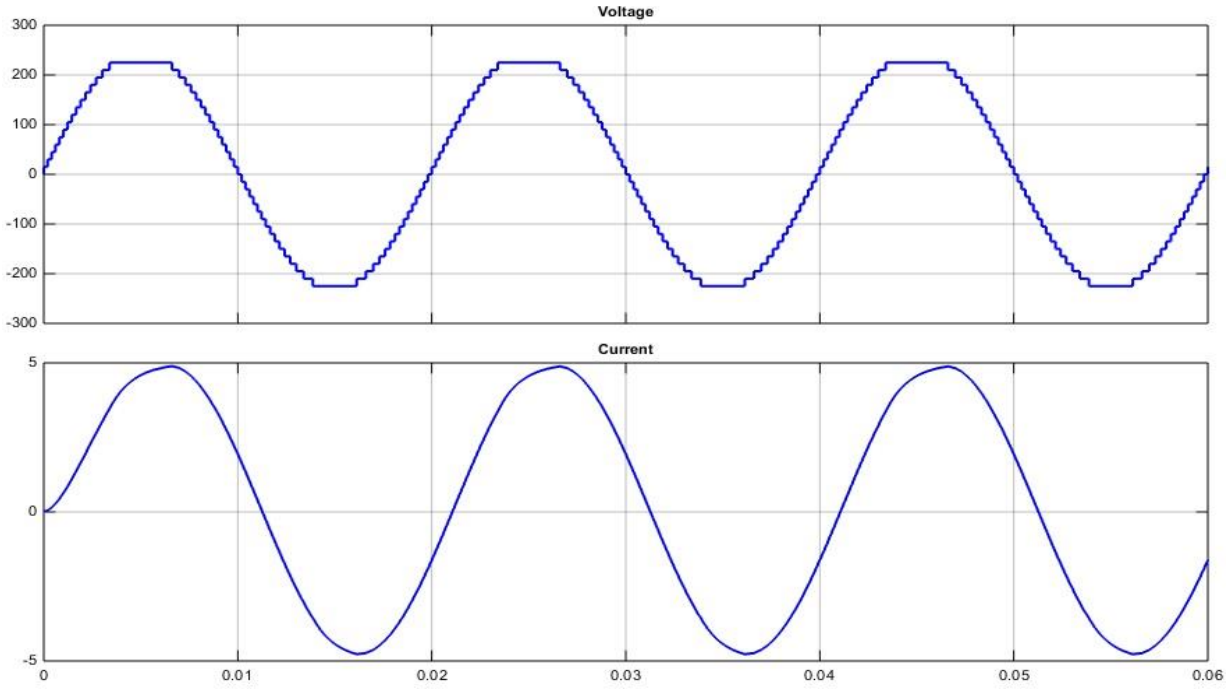

Figure.4.14 Output voltage and current of 31- level inverter.

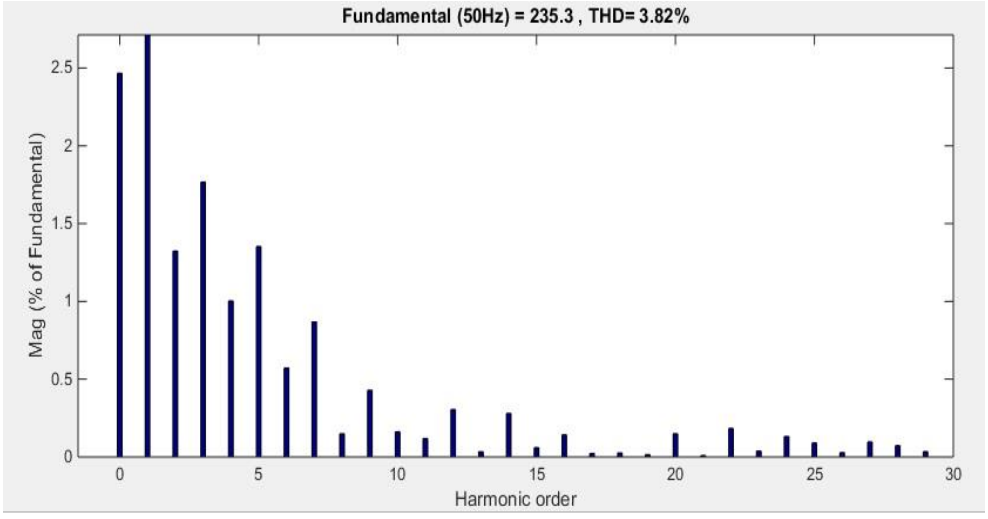

Figure.4.15 (a)

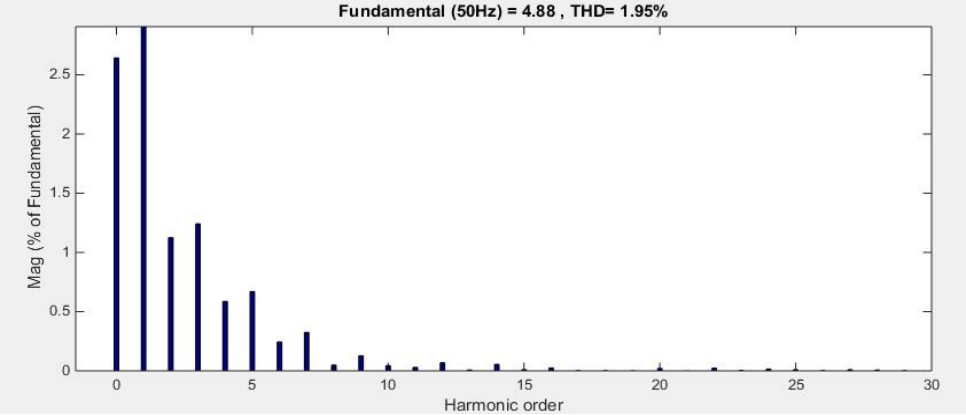

Figure 4.15 (b)

Figure.4.15 FFT Spectra of 31- level single phase inverter with new topology

(a) Voltage (b) Current

4.5. Discussions:

The comparisons of conventional cascaded multilevel inverter and proposed multilevel inverters with respect to number of DC voltage sources and switches shown in TABLE 4.5.

TABLE 4.5

Comparison of cascaded conventional and proposed multilevel inverters

Level	**Conventional cascaded multilevel inverter**		**Proposed multilevel inverter**	
	No of DC voltage sources	**No of switches**	**No of DC voltage sources**	**No of switches**
7-level	3	12	2	6
9-level	4	16	3	8
13-level	6	24	3	10
15-level	7	28	3	10
31-level	15	60	4	10

THD values of current, voltage of 7-level, 9-level, 13-level, 15-level and 31-level Inverters are shown in below TABLE 4.6.

TABLE 4.6

THD of multilevel Inverters

Level	**THD_v (%)**	**THD_i (%)**
7-level	16.96	10.86
9-level	12.28	9.31
15-level	6.83	5.30
31-level	3.82	1.95

From different levels of simulation it is observed that by increasing number of levels THD can be decreased. Due to the less number of power electronic switches and number of DC voltage sources the total cost of the inverter decreases and also switching losses decreases.

CHAPTER 5

CONCLUSION

CHAPTER 5

CONCLUSION

In this work various architectures for multilevel inverters have been presented. We have designed MLI with 7-level output voltage. The design initially proposed for single phase inverter. Further it was extended to three phase as well. Thus the design is suitable for any DC to AC converter applications. We have considered pure resistive load for three phase MLI. The load for single phase MLI was taken to be pure resistive and reactive (R-L) load individually. We have designed MLI following GPI (Generalized Proportional and Integral) controller. The feedback signal was primarily taken as voltage signal. Since current feedback has some potential applications we have designed MLI having current feedback as well. The Total Harmonic Distortion (THD) in each of the cases observed using simulation results. An FFT spectrum was generated in each simulation which shows the harmonic order or THD.

For a seven level three phase R-load the THD_i and THD_v were found to be 1.01% and 0.94%, while the same for a single phase system was found to be 2.38% and 1.65% respectively with voltage feedback. For a seven level three phase R-load the THD_i and THD_v were found to be 0.70% and 0.68%, while the same for a single phase system was found to be 0.88% and 0.88% respectively with current feedback. With an R-L load the single phase seven level MLI showed THD_i and THD_v values of 2.34% and 1.56% respectively under voltage feedback. The same design with current feedback showed THD_i and THD_v values of 1.12% and 0.41% respectively.

In all these designs the THD was found to be less than 5%. This suggests 7- level inverter with GPI controller delivers output power with better quality.

Traditional architecture of multilevel inverter requires numerous power electronic components. As a solution to this, we have also designed MLI based on novel H-bridge structure. This model resulted in the reduction of switching elements as well as DC voltage sources required. For a seven level MLI, six switches and DC voltage sources are sufficient which is less compared to the conventional system using twelve switches and three sources. Using the same model we have also demonstrated 9-level inverter with three DC sources and eight switches, 15-level inverter with three DC source and ten switches and 31-level inverter with ten switches and four DC voltage sources. In 31-level inverter the THD found to be less than 5%, making the system compact yet efficient.

CHAPTER 6

FUTURE SCOPE

CHAPTER 6

FUTURE SCOPE

In our work we presented seven level inverter systems. We have designed MLI with GPI controller for resistive and reactive (R-L) loads. The design can be extended to drive various motors such as induction motor, railway traction etc. We have demonstrated inverters with single and three phases. Further a multi-phase inverter can also be designed following similar or slightly modified architecture. We chose current and voltage signal separately as feedback signals for generating switching pulses using SPWM technique. Using combination of these feedback signals we may obtained better output power quality. In addition other modulation techniques such as Selective harmonic elimination, wavelet modulation etc. for switching based on desired application.

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PUBLICATIONS

Communicated:

1. Bhogeswara Rao Angara, M.M.Tripathi "Design of Single phase multi-level cascade inverter using GPI controller", IEEE International Conference on Advances in Computing and Communication Engineering (ICACCE 2015)be held during 1st and 2nd May, 2015, TULA's Institute, Dehradun **(Accepted).**

2. Bhogeswara Rao Angara, M.M.Tripathi "'Novel design of cascaded multilevel inverter with reduced number of components" in IET power electronics 2015.

3. Bhogeswara Rao Angara, M.M.Tripathi "Design of GPI Controller for Current Feedback Multilevel Cascaded Inverter" in IEEE INDICON conference 2015.