# CURRENT DIFFERENCING DIFFERENTIAL OUTPUT BUFFERED AMPLIFIER (CDDOBA) AND ITS APPLICCTIONS IN SIGNAL PROCESSING

A

DISSERTATION
SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE AWARD OF THE DEGREE OF

**MASTER OF TECHNOLOGY**
IN
**CONTROL AND INSTRUMENTATION**
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SUBMITTED BY:
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UNDER THE SUPERVISION OF

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**JULY,2016**

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## Candidate's Declaration

I, **Arshdeep Kaur**, Roll No. **2K14/C&I/18** student of **M. Tech. (Control and Instrumentation)**, hereby declare that the dissertation titled **"Current Differencing Differential Output Buffered Amplifier (CDDOBA) And Its Applications In Signal Processing"** under the supervision of **Prof. Pragati Kumar**, in partial fulfilment of the requirement for the award of the degree of Master of Technology has not been submitted elsewhere for the award of any degree.

I hereby solemnly and sincerely affirm that the entire particular stated above by me are true and correct to the best of my knowledge and belief.

Place: Delhi **Arshdeep Kaur**

Date: **2K14/C&I/18**

# DEPARTMENT OF ELECTRICAL ENGINEERING

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# Certificate

This is to certify that the dissertation entitled **"Current Differencing Differential Output Buffered Amplifier (CDDOBA) And Its Applications In Signal Processing"** submitted by **Arshdeep Kaur** in completion of major project dissertation for Master of Technology degree in **Control and Instrumentation** at Delhi Technological is an authentic work carried out by him under my supervision and guidance.

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

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# ABSTRACT

In the present dissertation implementation of new active building block Current differencing differential output buffer amplifier (CDDOBA) using IC AD844 has been presented. CDDOBA is a new active building block with two input p and n terminal and two output, +w and -w terminal. CDDOBA can be well thought-out as a collection of inverting and non inverting current mode and inverting and non inverting voltage mode unity-gain cells. Recent advancements in current mode signal processing and advantages of current mode signal processing over voltage mode are briefly described in the second chapter. In this dissertation detailed description of the architecture of CDDOBA and PSPICE simulation of CDDOBA realized with IC AD844 is presented. General first order filters, voltage mode amplifier and differentiator and integrator circuits have been presented as application examples in order to demonstrate the performance of the CDDOBA. The PSPICE simulation results for frequency response are incorporated to verify the theory. A new Biquad filter, employing one CDDOBA as active element and four resistors and four capacitors is proposed.

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# CHAPTER 1

# INTRODUCTION

## 1.1 Introduction

This dissertation deals with CDDOBA and its applications in signal processing. The domain of analog signal processing has seen many developments since the introduction of integrated circuit operational amplifiers which used to dominate the signal processing space. Though the IC op-amp was developed nearly half a century ago very little improvement in the architecture of the operational amplifier had taken place. This may be attributed partly to the fact that semiconductor manufacturing industry was being optimised for mass production of digital integrated circuits in which mostly unipolar transistors were used. Any improvement in the architecture required good quality PNP/PMOS transistors also. But during the last couple of decades major advances have taken place in semiconductor manufacturing processes and high quality CMOS transistors are now available to the analog circuit designer and this has led to development of alternative active building blocks. With the development of alternative building blocks the term current mode signal processing has become very popular. In simple terms, current mode means a signal processing environment in which input and output variables are current rather than voltages. Current mode circuits are generally characterised by

- Low voltage swings
- Higher speed
- Simple architecture etc.

Therefore current mode technique is progressively being acknowledged as a way to overcome the limitations of conventional opamp and to realize high speed systems [1].

In the last few decade new current mode building blocks [2] like Current-feedback opamps(CFOA), second generation current conveyors(CCII+ and CCII-) [3], differential voltage current conveyor (DVCC), third generation current conveyor(CCIII), electronically controlled current-conveyor (ECCII),voltage differencing buffer amplifier(VDBA), current differencing buffer amplifier(CDBA), etc have received lot of attention due to their dynamic range and wide bandwidth[4]. Recently, a new active building block namely, current differencing differential output buffered amplifier (CDDOBA), was introduced to offer

additional possibilities in signal processing [5]. The CDDOBA can offer high-slew rate, eliminate parasitic impedance, offer wide bandwidth and has a simple implementation. Since this element contains unity gain current differencing unit and a voltage buffer with complimentary outputs, this would be suitable for implementation of current and voltage mode signal processing applications. Various current mode and voltage mode filters and oscillators can be realized using CDDOBA. Since the work presented in this dissertation primarily deals with signal-processing a bird eye view of different approaches to signal processing is now presented.

## 1.2 Analog and Digital Signal Processing

The signal processing operations involved in many applications like communication systems, control systems, instrumentation and biomedical signal processing etc. can be implemented in two different ways

1) Analog or continuous time method and
2) Digital or discrete time method

The analog approach to signal processing was dominate for many years and it uses analog circuits such as resistors, capacitors, transistors, diodes etc. With the advent of digital computer and later microprocessors, the digital signal processing has became dominant now a days. The analog signal processing is based on natural ability of analog system to solve differential equations that describe a physical system. The solutions are obtained in real time. In contrast digital signal processing relies on numerical calculations. The method may or may not give results in real time. The digital approach has two main advantages over analog approach

1) Flexibility: Some hardware can be used to do various kind of signal processing operation, while in the core of analog signal processing one has to design a system for each kind of operation.
2) Repeatability: The same signal processing operation can be repeated again and again giving same results, while in analog systems there may be parameter variation due to change in temperature or supply voltage. Added to these, digital signal processing has many advantages like, better noise immunity than analog signal. They are compact and much cheaper than their analog counter part. Digital signals can be encrypted so

that only the intended receiver can decode it. It Enable transmission of signals over a long distance and it enables multi-directional transmission simultaneously.

Taking these advantages into account, the designers are forced to look for digital solutions rather than analog in VLSI systems. Even then, analog circuits are fundamentally necessary in many of today's complex, high performance systems. This is caused by the reality that naturally occurring signals are analog. Practically all signals in physical world are continuous in both amplitude and time, and hence always analog techniques will be required for conditioning of such signals before they can be processed by digital signal processing circuits. Therefore analog circuits act as a bridge between the real world and digital systems. Another important reason for the existence of analog signal processing is the bandwidth, which can be some order of magnitudes higher, if the signal is processed in analog circuits than in digital.

## 1.3 Current Mode Circuits and Voltage Mode Signal Processing

Fundamental definitions for voltage and current mode, used by authors in recent literatures are-

**Voltage mode:** In voltage mode circuits information is represented in form of voltage at nodes of circuit.

**Current mode:** In current mode circuits information is represented by current flowing through the branches of circuit.

Though, none of the above definitions used in recent literatures is accurate. So summarising that in voltage mode signal is represented by voltage and by current in current mode circuits is not precise as there is a current associated with a voltage node and every branch have some value of voltage associated to it. Thus a circuit is not categorised as voltage or current mode, instead they are just alternate ways of looking at same circuit. Circuit can be categorized as voltage mode and current mode signal processing circuits. In voltage mode signal processing, the receiver provide high input impedance, the voltage output is the function of input signal and is modified according to supply voltage. In current mode signal processing receiver provide low input impedance [6].

Majority of conventional analog circuits are voltage mode circuits where the circuit functioning is determined in terms of voltages at respective nodes comprising the input and the output nodes for example operational amplifier. But all these circuits experience the following disadvantages

- Output voltage value of circuit cannot change instantaneously when there is abrupt change in the input
- Voltage due to parasitic and other stray circuit capacitances.
- Bandwidth of the conventional op amp based circuits is generally low due to finite gain bandwidth product.
- Slew rate depends on the time constants for the circuits which do not have high voltage swings.
- It requires high supply voltages for better Signal Noise Ratio.

Hence, voltage mode circuits are not suitable for use in high frequency applications. In current mode circuits the whole circuit response is determined by the currents in branches and the output/input signals are mainly currents [7]. The voltage levels don't play role in determination of the circuit performance. The input nodes of current mode circuits have low impedance and resultant voltage swings there, are also small. The low impedance modifies them into low time constant circuits and their bandwidth is quite high. The slew rate of these circuits is also high when the rate of output changing is high. Current mode circuits operations do not depend on the supply voltages and they have simple architecture [8]. For high SNR the analog circuits should have immediate input and output voltage swing change capability. This can be achieved using the current mode circuits [9].

Therefore, advantages offered by current mode signalling in integrated circuits is summarised as follow

**Performance improvement**

- Low crosstalk and switching noise
- Less affected by voltage fluctuations
- High speed
- Low power consumption at high frequency

**Structural advantages**

- Simple circuitry
- Current summing without components
- Controlled gain with less dependence on feedback components

**Specific features**

- Current switching techniques
- Pseudo conductance network
- Suitable for low voltage, low power applications

## 1.4 An Overview of CDDOBA

The circuit symbol for CDDOBA is shown in figure.1. CDDOBA is a new active building block with two input p and n terminal and two outputs +w and –w terminal [5].

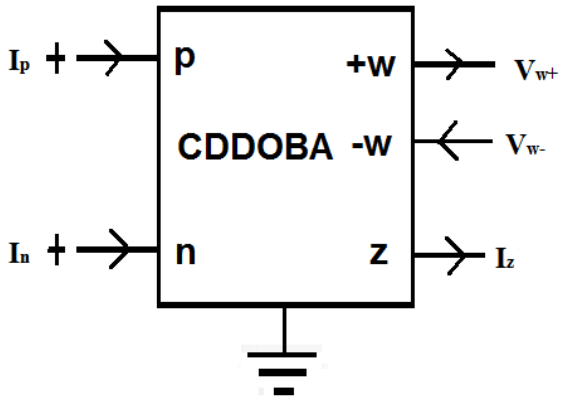


Fig.1.1.Symbol of CDDOBA

Current through z terminal is difference of currents through p and n terminal. Hence z is current output and p and n are non-inverting and inverting terminals of CDDOBA. Since voltage at +w terminal follow voltage at z terminal and voltage at –w terminal is complimentary to voltage at z and +w terminal, terminal +w and –w are voltage outputs of CDDOBA. Terminals p and n are generally forced to be at virtual ground by the architecture and impedance at these input terminals is ideally zero. Here current difference at input terminals appear as voltage output at +w and –w terminal. Hence CDDOBA can be considered as trans-impedance amplifier. Therefore in CDDOBA based amplifiers gain bandwidth limitation does not occur and it give good results in high frequency applications. CDDOBA can also be well thought-out as a collection of inverting and non-inverting current mode and inverting and non-inverting voltage mode unity-gain cells. These characteristics make CDDOBA free from the parasitic impedances and result in very high frequency operations.

## 1.5 Thesis Organization

A chapter wise overview of the dissertation is as follows:

**Chapter 1** gives an overview of signal processing, compares current mode and voltage mode signal processing. This chapter gives a brief introduction of active building block CDDOBA. It also includes the general outline of the thesis.

**Chapter 2** briefly describes about the significance of current mode circuits and the various active blocks that are introduced after Current Conveyors. Particular emphasis has been put on those works which have been presented during the last one decade.

**Chapter 3** of the dissertation gives a bipolar architecture of CDDOBA and its building blocks. At the end of chapter simulation results for some applications of CDDOBA is presented.

**Chapter 4** describes implementation of universal filter application using CDDOBA, followed by PSPICE simulation results.

**Chapter 5** describes hardware implementation of filter application of CDDOBA.

**Chapter 6** finally Summary and scope of future work in this area are outlined.

## References


1. H. Y. Chen and S. M. Kang, "A new circuit optimization technique for high performance CMOS circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 10, no. 5, pp. 670–677, May 1991.
2. Kuntman, H. A. "New Advances and Possibilities in Active Circuit Design", presented at 10th International Conference on Development and application systems, Suceava, Romania, May 2010.
3. K. Smith and A. Sedra, "The current conveyor: A new circuit building block", *Proceedings of the IEEE*, vol. 56, no. 8, pp. 1368-1369, 1968.
4. http://nptel.iitm.ac.in
5. Biolek, D., Senani, R., Biolkova, V. and, Kolka, Z. "Active Elements for Analog Signal Processing: Classification, Review, and New Proposals", *Radioengineering*, Vol.17, No.4, Dec 2008.
6. F. Yuan, "Low-voltage CMOS current-mode circuits: topology and characteristics", *IEE Proc.-Circuits Devices Syst.*, Vol. 153, No. 3, June 2006.
7. J. Fidler, "Analogue IC Design: the Current-Mode Approach", *IEE Rev.*, vol. 37, no. 1, p. 33, 1991.
8. K. CHENG and H. WANG, "Design and analysis of low-voltage current mode operational amplifier with differential-input and differential-output", *International Journal of Electronics*, vol. 85, no. 4, pp. 443-453, 1998.
9. G. W. Roberts and A. S. Sedra, A. S., "All current-mode frequency selective circuits", *Electron. Lett.*, Vol. 25, pp. 759-761, 1989.

# CHAPTER 2

# RECENT ADVANCES IN CURRENT MODE SIGNAL PROCESSING

## 2.1 Active Current Mode Circuits

In low-power and low-voltage analog systems, current-mode signal processing has been proved to be a smart strategy because of its capability of high-speed operation and low-voltage compatibility. Current-mode signal processing techniques result in active circuits with simple architectures. The current mode circuits are suitable for integration in CMOS technology as specially processed resistors or capacitors are not required. Therefore, they are friendlier with current technology making integration of mixed signal circuits more viable. In a current mode circuit if there is a current level change, it is not necessarily accompanied by the voltage level change. Thus, the operating speed of the circuit is not affected by parasitic impedances by a significant amount. Thus many conventional voltage mode active circuit topologies have been replaced by current mode designs as current mode signal processing proved to be a better choice for high performance, low voltage analog circuit design where designer is concerned with current levels for the operation of the circuits.

Hence, current-mode approach has been progressively recognized as a way to overcome the voltage mode circuits like opamps drawbacks and to realize high speed circuits. In the last two decades many new current-mode active building blocks like current-feedback opamps (CFOA), many derivatives of second generation current conveyors and current difference buffer amplifier (CDBA) have received significant attention due to their wider bandwidth and larger dynamic range. Also in addition, other active elements like four terminal floating null or (FTFN), differential difference current conveyor (DDCC),current controlled current-conveyor (CCCII), third generation current conveyor(CCIII) and differential voltage current conveyor (DVCC)have been presented in many literatures. In the following we present a brief overview of some of these active building blocks.

### 2.1.1 Second Generation Current Conveyors (CCII+ and CCII−)

A current conveyor is a form of electronic amplifier with unity gain. The three versions of generations of the idealised device are CCI, CCII and CCIII. Like conventional opamps current conveyors if configured with other circuit elements, can perform many analogue signal processing functions [1]-[3].

Current conveyors can offer better gain-bandwidth products than conventional op-amps, under both large and small signal conditions. The first generation current conveyor is a three-terminal device with the terminals named X, Y, and Z. The voltage at X follows whatever voltage is applied to Y and value of current flowing into Y also same as amount flowing into X, and is mirrored at Z which have high output impedance. In sub-type CCI+, current flowing into Y is mirrored as current into Z; while in a CCI-, current flowing into Y leads to an equivalent current flowing out of Z.

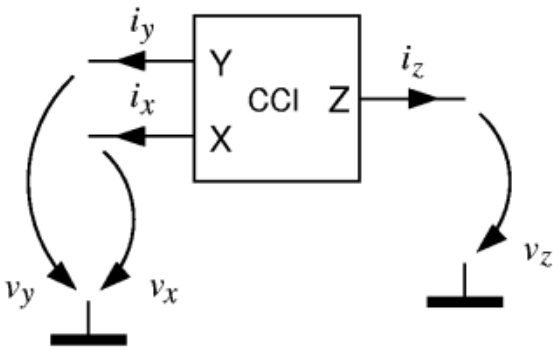


Fig.2.1. First generation current conveyor [1]

In many applications of first generation current conveyors, only one of the virtual grounds in X and Y terminal is used and we have to ground the unused terminal else connect it to an appropriate potential. This grounding has to be done carefully as a poorly grounded input terminal may lead to unwanted negative impedance at the other input terminal. Also, for many applications input terminal with high impedance is preferable. These were the reasons behind development of the second generation current-conveyor. CCII has one high and one low input impedance terminal while CCI has two low impedance inputs. Second generation current conveyor (CCII) was introduced by Sedra and Smith in 1970 [4].

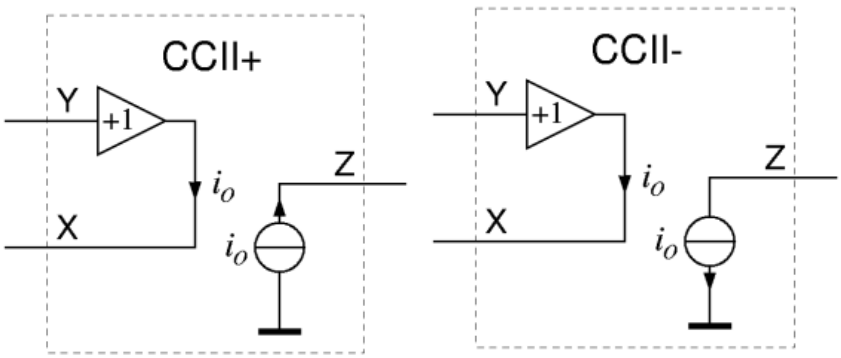


Fig.2.2. Second generation Current Conveyors [4]

The characteristic matrix representation of CCII (Second generation Current Conveyors) is:

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix}$$

### 2.1.2 Current Feedback Operational Amplifier (CFOA)

Current feedback op-amps (CFOA) started attracting attention of researchers and the analog circuit designers, as one can design amplifiers displaying a characteristic which was the most considerable departure from well-known VOAs characteristics. CFOAs have much higher slew rates ranging from few several hundred to several thousand V/μs, where as this value is 0.5 V/μs for most popular μA741-type and the general purpose VOA[5]. Also CFOAs can result in circuits capable of operating at much higher frequency ranges as compared to those possible with VOAs [6].

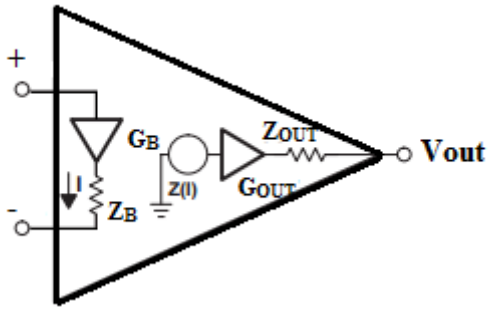


Fig.2.3. Current feedback amplifier block diagram

An input voltage, applied to the positive input terminal, is buffered by a unity gain voltage buffer GB, which results in current I through an impedance $Z_B$, which return through the negative input terminal. Hence, the inverting input has very low input impedance, corresponding to impedance $Z_B$.

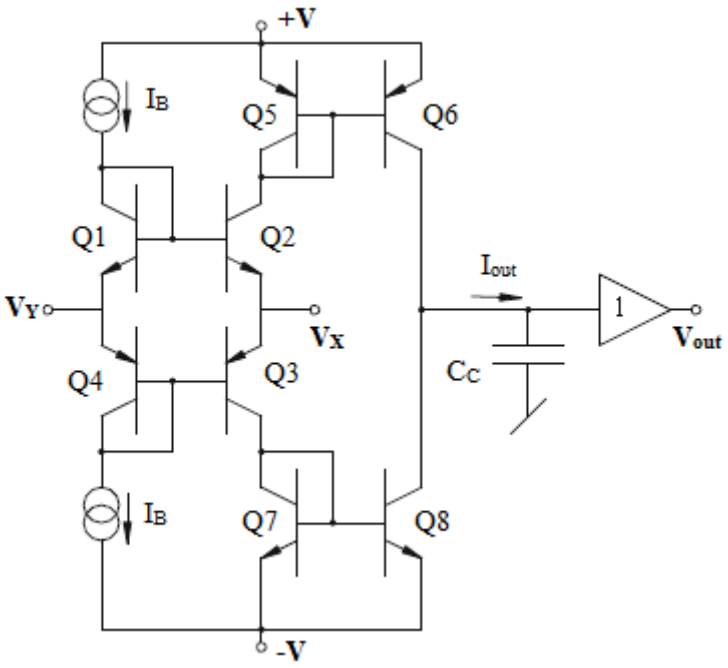


Fig.2.4. Simplified model of the CFOA

***AD844***

The AD844 is a high speed monolithic operational amplifier. It possess features like fast large signal response and high band-width, along with excellent dc performance. Though optimized for use as an inverting mode amplifier and in current-to-voltage applications, it is also appropriate for use in many non-inverting applications [7]. IC AD844 can be used in place of conventional op amps, as its current feedback architecture results in high linearity, much better ac performance and a very clean pulse response. This type of op amp results in a closed-loop bandwidth which is primarily determined by the feedback resistor and is nearly independent of the closed-loop gain. Unlike traditional op amps and other current-feedback op amps AD844 is free from the slew rate limitations. Output peak to peak change rate can be over 2000 V/μs for a full 20 V output step. Settling time is essentially independent of gain and is typically 100 ns to 0.1% [8].

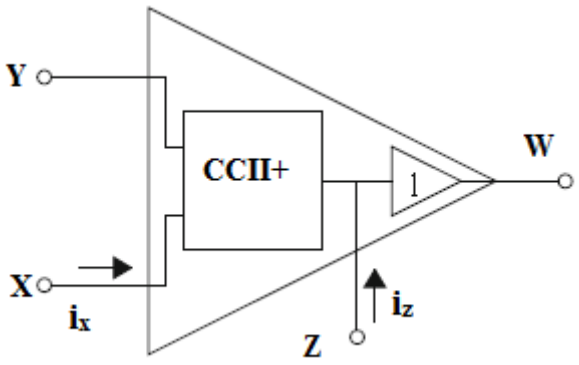


Fig.2.5. A block diagram of the internal architecture of CFOA AD844 [8]

### 2.1.3 Current Differencing Buffered Amplifier (CDBA)

Recently proposed five-terminal active element, current differencing buffered amplifier (CDBA), proved to be a versatile component in the realisation of many signal-processing circuits. It can be operated in both voltage-mode (VM) and current-mode (CM) in a wide frequency range. It can also be implemented with CMOS technology.

CDBA was introduced by Acar and Ozoguz to provide further potentials in the circuit synthesis and simplified implementation. The CDBA can offer a simple implementation, wide bandwidth and high-slew rate. Applications based on CDBA reported in the recent literatures are current-mode filters [9-11], fully integrated gyrator circuits [12], fully integrated signal process circuits [13], resistance controlled sinusoidal oscillators [14], voltage-mode filters.

The Current differencing buffered amplifier (CDBA) circuit symbol is shown in Figure 2.6

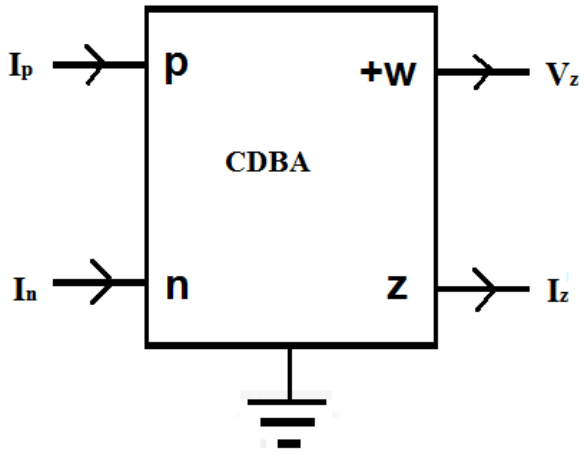


Fig.2.6. Symbol of CDBA

The current differencing buffered amplifier is characterized by equation

$$\begin{bmatrix} I_z \\ V_w \\ V_p \\ V_n \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 & -1 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_z \\ I_w \\ I_p \\ I_n \end{bmatrix}$$

According to the above characteristic matrix, the current through output z-terminal is the difference of the currents through input p-terminal and n-terminal, thus, the z-terminal is called current output while p and n-terminals are non-inverting and inverting input terminals, respectively. The output at the w-terminal is voltage output as it follows the voltage of z-terminal. The input terminals p and n are internally grounded so ideally the input impedance at the terminals p and n are internally zero.

Recently some multifunction current mode filters containing CDBA elements are published in literature [15–17]. Though, they use more than two CDBAs to implement all five (LP, HP, BP, BS and AP) filter transfer functions.

### 2.1.4 Differential Difference Current Conveyor (DDCC)

The Differential Difference Current Conveyor (DDCC) is a versatile active building block used for implementation of floating and differential input circuits [18]-[20]. In addition, other current conveyors, such as CCII (Second Generation Current Conveyors), CCIII (Third Generation Current Conveyor), DVCC (Differential Voltage Current Conveyor) and ICCII (Inverting Second Generation Current Conveyor) can be easily obtained by using DDCC. In the proposed DDCC circuit, the negative feedback action is introduced to reduce channel length modulation effect of MOS transistors. Hence, it has large linear dynamic range and less harmonic distortions. The DDCC is a six-port active building block as shown in Figure 2.7

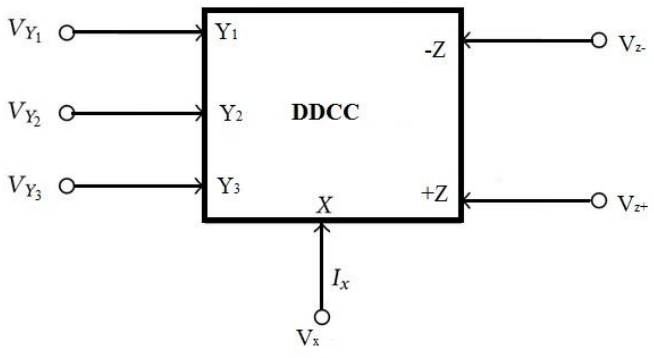


Fig.2.7. DDCC symbol [20]

DDCC has three high impedance voltage input terminals: $Y_1$, $Y_2$and $Y_3$. Also, terminal X is a current input terminal, with low input impedance. There are two current output terminals: Z- and Z+, which have high impedance.

The input-output characteristics matrix of the DDCC is as follow

$$\begin{bmatrix} V_x \\ Iy_1 \\ Iy_2 \\ Iy_3 \\ I_{z+} \\ I_{z-} \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_x \\ Vy_1 \\ Vy_2 \\ Vy_3 \\ V_{z+} \\ V_{z-} \end{bmatrix}$$

The currents *(Iz+* and *Iz-)* at output terminals follow the current through input terminal X. Current through Z+ terminal has the same polarity as $I_x$ and through Z- terminal is in the opposite polarity as $I_x$ and voltage of X terminal is related the three inputs voltage and is given as:

$$V_x = V_{y1} - V_{y2} + V_{y3} \quad (2.1)$$

$$I_{y1} = I_{y2} = I_{y3} = 0 \quad (2.2)$$

$$I_Z = \pm I_X \quad (2.3)$$

Proposed DDCC circuit has less harmonic distortion and large linear dynamic range. Also popular current conveyors, such as CCII, CCIII, ICCII, and DVCC, can be directly realized by using the DDCC. Further advantage of DDCC is that its application circuits employ less number of passive elements.

### 2.1.5 Current Controlled Current conveyor (CCCII)

In 1996 Fabre proposed second generation current controlled current conveyor (CCCII) constructed by bipolar transistors based on CCII and BJT translinear loop [21]. The CCCII requires no external resistors; hence it is appropriate in the design of oscillators and integrated filters [22]. The parasitic resistance at terminal X is given by $R_x = V_T/2I_b$. This gives electronic programmability of CCCII.

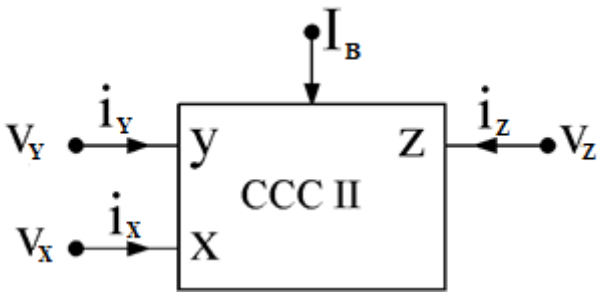


Fig.2.8. Symbol of CCCII [23]

Also, the CCCII based circuit is very suitable for high frequency operation [23]. These features are very striking to circuit designers. In analog signal processing configurations possessing electronic tunability property can be easily adapted in integrated circuit environment. The basic CCII does not have build in tuning property, while CCCII has, as a result of the adjustability feature of intrinsic resistance at port X of CCCII by bias current [24].

The characteristic equations which give relationship between the voltage and current variables at input and output terminals X, Y and Z of the CCCII can be expressed by the following matrix,

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & R_x & 0 \\ 1 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix}$$

where the positive/negative sign ± refers to plus-type or minus-type CCCII, respectively, and $R_x$ refers to the intrinsic resistance at input terminal X. $R_x$ can be adjusted by a supplied bias current $I_b$ which can be articulated through a class AB trans-linear loop, which is used as input section.

$$I_y = 0 \quad (2.4)$$

$$V_x = V_y + I_x.R_x \quad (2.5)$$

$$I_{z+} = I_x \quad (2.6)$$

$$I_{z-} = -I_x \quad (2.7)$$

### 2.1.6 Four Terminal Floating Nullor and Multi output- FTFN

New active element in signal processing which have also received considerable attention is four-terminal floating nullors (FTFNs) [25]. Current-mode filters and current mode sinusoidal oscillators employing FTFNs as active devices have been developed in the literature. It have been demonstrated that an FTFN is a more flexible and versatile active building block than a second generation current conveyor (CCII) and an operational amplifier (op-amp) [26]. Recently, implemented electronically tunable multi-output (ET-FTFN) in integrated circuit offers the flexibility in designing analog signal processing circuits [27].

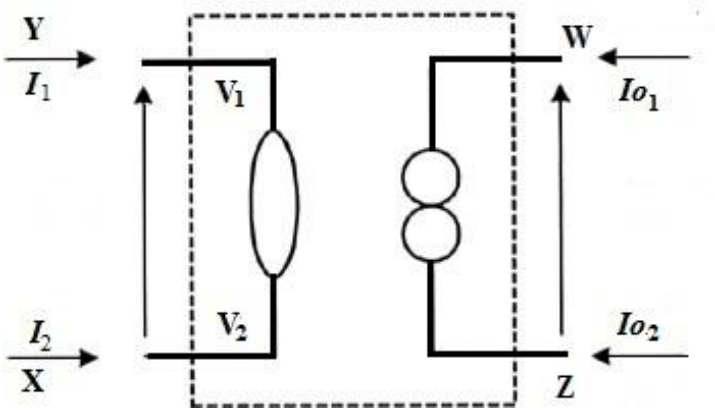


Fig.2.9. Nullor model [26]

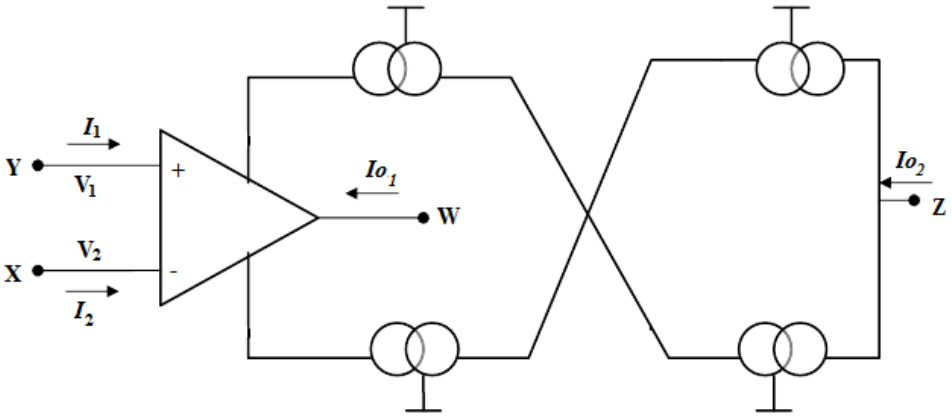


Fig2.10. Traditional implementation [26]

The Fig2.9 shows FTFN nullor model. Characteristic port relations are as follow:

$$V_1 = V_2 \quad (2.8)$$

$$I_1 = I_2 = 0 \quad (2.9)$$

$$I_{o1} = -I_{o2} \quad (2.10)$$

The output impedance of W and Z terminal are generally arbitrary. However most of the FTFNs are conventionally realized from basic type, which have low output impedance at W and high output impedance at Z.

### 2.1.7 Third Generation Current Conveyors

The third generation current conveyors (CCIIIs) can be considered as a current controlled current source with unity gain. CCIII has been proposed by A. Fabre [28]. Low gain error i.e high accuracy; wide frequency response and high linearity are the main features of third generation current conveyors. To provide good dynamic swing, high output resistance to enable cascadability; high performance current mirrors are required in structure of CCIIIs [29]-[30].

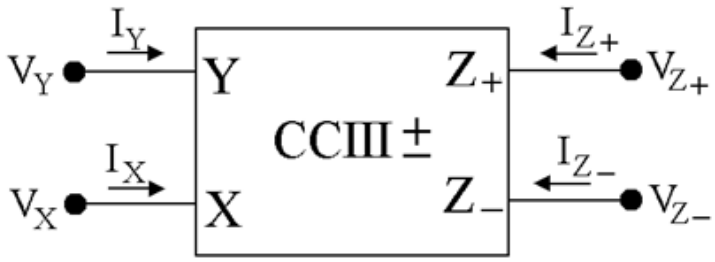


Fig.2.11.Electrical symbol of third generation current conveyor [28]

Characteristic matrix establishing input/output port relationship is as follow:

$$\begin{bmatrix} I_y \\ V_x \\ I_{z+} \\ I_{z-} \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & -1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_{z+} \\ V_{z-} \end{bmatrix}$$

The positive and negative signs define a positive and negative current controlled conveyor. The characteristic port equations are as follow:

$$I_y = -I_x \quad (2.11)$$

$$V_x = V_y \quad (2.12)$$

$$I_{z+} = I_x \quad (2.13)$$

$$I_{z-} = -I_x \quad (2.14)$$

Third generation current conveyor are proved to be a useful element to pick up the current of a floating passive element and can be utilized in realization of various inductance simulation, multi-function filters and all pass sections

## 2.2 Conclusion

In the present chapter brief overview of some of the recently introduced active building blocks like Current Feedback Operational Amplifier (CFOA), Current differencing buffered amplifier (CDBA), four terminal floating null or (FTFN), differential difference current conveyor (DDCC),current controlled current-conveyor (CCCII), third generation current conveyor(CCIII) and differential voltage current conveyor (DVCC) has been presented.

## REFERENCE


1. Elwan and A. Soliman, "Low-voltage low-power CMOS current conveyors", *IEEE Trans. Circuits Syst. I*, vol. 44, no. 9, pp. 828-835, 1997.
2. I. Awad and A. Soliman, "New CMOS realization of the CCII-", *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 46, no. 4, pp. 460-463, 1999.
3. A. Arbel and L. Goldminz, "Output stage for current-mode feedback amplifiers, theory and applications," *Analog Int. Circuit Signal Processing*, vol.2, pp.243-255, 1992.
4. K. Smith and A. Sedra, "The current conveyor: A new circuit building block", *Proceedings of the IEEE*, vol. 56, no. 8, pp. 1368-1369, 1968.
5. http://www.analog.com/media/en/training-seminars/tutorials/MT-034.pdf
6. William H. Gross, "Current Feedback Amplifier Do's and Don'ts" – Design Note 46
7. www.analog.com
8. http://www.analog.com/media/en/technical-documentation/datasheets/AD844.pdf
9. S. Özoguz, A. Toker, C. Acar, "A new current-mode continuous time fully integrated universal filters", *Elect Lett*, vol. 35, pp. 97–98,1999.
10. Kacar, Fırat, and Y. Ozcelep. "CDBA Based Voltage-Mode First-Order All-pass Filter Topologies," *IU-JEEE*, vol.11,pp.1327-1332, 2011.
11. C. Acar, H. Sedef, — "Realization of nth-order current transfer function using current differencing buffered amplifiers", *Int J Electron*, vol.90, pp.277-283,2003
12. A. Toker, S. Ozoguz, C. Acar, — "CDBA-based fully-integrated gyrator circuit suitable for electronically tunable inductance simulation", *Int. J. of Electronics (AEÜ)*, vol.54,pp. 293-296,2000.
13. S. Özoguz, A. Toker, M. A. İbrahim, C. Acar, — "A new versatile building block: Current differencing amplifier and its applications", In Proceedings of The European Conference on Circuit Theory and Design, ECCTD'99,pp. 90-93, 1999.
14. S. Özcan, A. Toker, C. Acar, H. Kuntman, O. Çiçekoğlu, — "Single resistance controlled sinusoidal oscillators employing current differencing buffered amplifier", Microelec J, vol.31, pp.169-174,2000.
15. A. Toker, S. Özoğuz and C. Acar, "Current-mode KHN-equivalent biquad using CDBAs", *Electron. Lett.*, vol. 35, no. 20, p. 1682, 1999.

16. S. Özoğuz, A. Toker and C. Acar, "Current-mode continuous-time fully-integrated universal filter using CDBAs", *Electron. Lett.*, vol. 35, no. 2, p. 97, 1999.
17. S. Özcan, H. Kuntman and O. Çiçekolu, "Cascadable Current Mode Multipurpose Filters Employing Current Differencing Buffered Amplifier (CDBA)", *AEU - International Journal of Electronics and Communications*, vol. 56, no. 2, pp. 67-72, 2002.
18. H. Elwan and A. Soliman, "Novel CMOS differential voltage current conveyor and its applications", *IEE Proceedings - Circuits, Devices and Systems*, vol. 144, no. 3, p. 195, 1997.
19. S. Gupta and R. Senani, "Comment: CMOS differential difference current conveyors and their applications", *IEE Proceedings - Circuits, Devices and Systems*, vol. 148, no. 6, p. 335, 2001.
20. C. Chang, M. Swamy and A. Soliman, "Analytical synthesis of voltage-mode even/odd-nth-order differential difference current conveyor and fully differential current conveyor II-grounded resistor and capacitor universal filter structures", *Int. J. Circ. Theor. Appl.*, vol. 43, no. 10, pp. 1263-1310, 2014.
21. A. Fabre, O. Saaid, F. Wiest and C. Boucheron, "High frequency applications based on a new current controlled conveyor", *IEEE Trans. Circuits Syst. I*, vol. 43, no. 2, pp. 82-91, 1996.
22. C. Wang, J. Xu, A. Keskin, S. Du and Q. Zhang, "A new current-mode current-controlled SIMO-type universal filter", *AEU - International Journal of Electronics and Communications*, vol. 65, no. 3, pp. 231-234, 2011.
23. "A New Approach for Low Voltage CMOS based on Current-controlled Conveyors", *International Journal of Engineering*, vol. 27, no. 5, 2014.
24. Z. Abbas, M. Olivieri, M. Yakupov and A. Ripp, "Design centering/yield optimization of power aware band pass filter based on CMOS current controlled current conveyor (CCCII+)", *Microelectronics Journal*, vol. 44, no. 4, pp. 321-331, 2013.
25. R. Senani, "A novel application of four-terminal floating nullors," *Proceedings of the IEEE*, vol. 75, no. 11, pp. 1544–1546, 1987.
26. U. Çam, O. Çiçekoğlu, and H. Kuntman, "Current-mode single-input Three-Output (SITO) universal filter employing FTFNs and reduced number of passive components," *Frequenz*, vol. 54, no. 3-4, Jan. 2000.

27. S. A. Tekin and M. Alçı, "Design and applications of electronically Tunable floating resistor using differential amplifier," *Electronics and Electrical Engineering*, vol. 19, no. 4, Apr. 2013.
28. A. Fabre, "Third-generation current conveyor: A new helpful active element," *Electronics Letters*, vol. 31, no. 5, pp. 338–339, Mar. 1995.
29. H. Kuntman, O. Çiçekoğlu, and S. Özoğuz, "A modified Third generation current conveyor, its characterization and applications," *Frequenz*, vol. 56, no. 1-2, Jan. 2002.
30. A. Piovaccari, "CMOS integrated third-generation current conveyor," *Electronics Letters*, vol. 31, no. 15, pp. 1228–1229, Jul. 1995.

# CHAPTER 3

# CIRCUIT IMPLEMENTATION AND GENERAL APPLICATIONS OF CDDOBA

## 3.1 Introduction

In the present chapter we present the basic architecture and port relationships of CDDOBA. The generic architecture of CDDOBA and its behavioral model and an exemplary implementation using off the shelf available component AD844 along with general signal processing applications of CDDOBA has been presented.

## 3.2 CDDOBA Architecture

The Current Differencing Differential Output Buffered Amplifier (CDDOBA) is a multi-terminal active component with two input and two output terminals. This element combines high bandwidth and very high-speed large signal response with outstanding dc performance [1]. It is a versatile active component which can be used in both current and voltage mode applications. It can be used in place of conventional op amps in many applications and its current mode architecture results in much better ac performance and high linearity. CDDOBA's closed-loop bandwidth is almost independent of the closed-loop gain. It is free from the slew rate limitations common in conventional op amps and other current-feedback circuits. It is introduced to explore extra signal processing possibilities. So from above we conclude that CDDOBA can offer some features over conventional circuits such as absence of parasitic impedance, high-slew rate, wide bandwidth and simple implementation. In this dissertation, CDDOBA configuration using IC AD844 is presented providing low input impedances at ports p and n, input terminal p and n are internally grounded and have very high output impedance at port z, a good linearity.

It comprise of basic two blocks i.e a current differencing unit with low impedance input terminals p and n with zero voltage drop ideally and output z giving current difference and another is differential output voltage buffer which takes input from current differencing unit and give output at one terminal and its complimentary voltage at another.

The characteristic equations of CCDOBA can be given as

$$V_p = V_n = 0 \qquad (3.1)$$

$$I_z = I_p - I_n \quad (3.2)$$

$$V_{w+} = +V_z \quad (3.3)$$

$$V_{w-} = -V_z \quad (3.4)$$

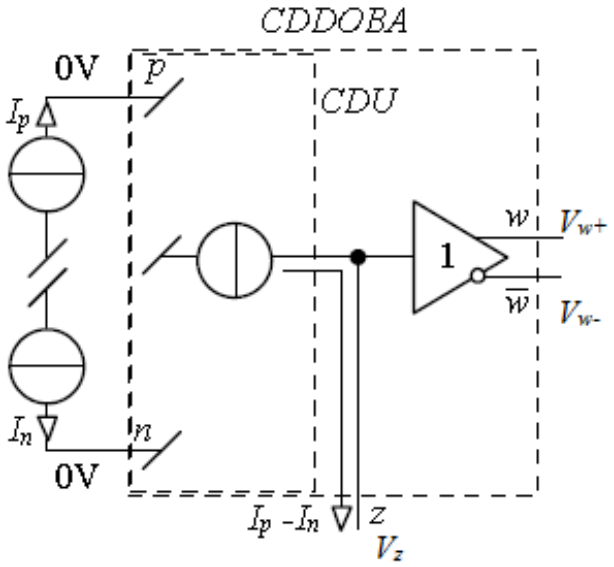


Fig.3.1. Ideal CDDOBA [1]

Current and voltage characteristics of CDDOBA are described by given matrix, where $i_p$ and $i_n$ are current at input terminal p and n respectively and $i_z$, $i_{w+}$ ,$i_{w-}$ are output currents at terminal z, w+ and w- respectively. Similarly $v_p$ and $v_n$ are voltage at input terminal p and n, which is ideally zero as p and n are internally grounded and $v_z$, $v_{w+}$, $v_{w-}$ are voltages at output terminals respectively.

$$\begin{bmatrix} I_z \\ V_{w+} \\ V_{w-} \\ V_p \\ V_n \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 1 & -1 \\ 1 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_z \\ I_{w+} \\ I_{w-} \\ I_p \\ I_n \end{bmatrix}$$

According to above matrix and characteristic equations, current through output terminal z is difference of current through input terminals, so z is known as current output, p terminal and n terminal are non inverting and inverting respectively. Since voltage at w+ and w- terminal follows voltage at z terminal in, in phase and out of phase manner, so these are two voltage outputs of CDDOBA. Input terminals are internally grounded so ideally input impedance at p and n terminal is zero and practically very low.

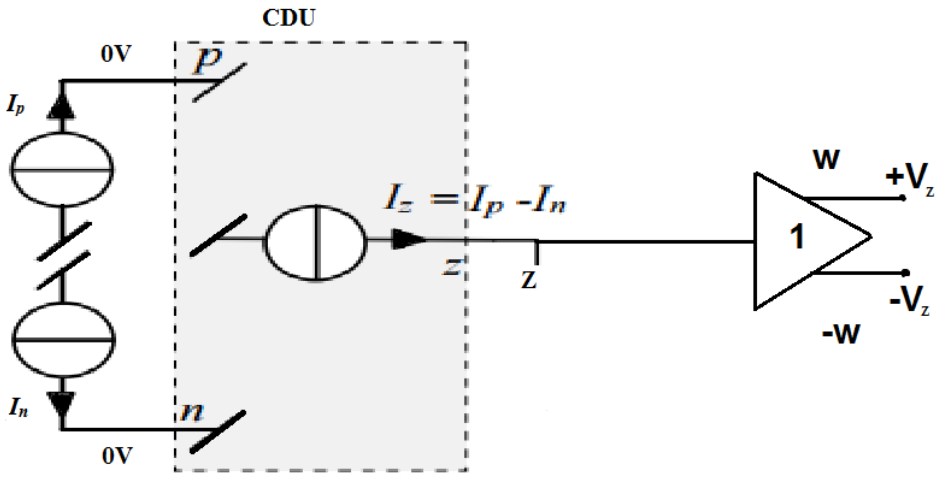


Fig.3.2. Current Differencing Differential Output Buffered Amplifier

In this chapter, characteristic equation and basic building blocks of CDDOBA are discussed. From above discussion we conclude that due to both voltage and current outputs CDDOBA can be used for voltage and current applications and it overcomes the limitations of op amp like limited bandwidth and slew rate problems.

## 3.3 Basic Building Blocks of CDDOBA

In broad sense CDDOBA comprise of two basic building blocks i.e current difference unit and unity gain voltage buffer with complimentary outputs. In this section these basic blocks are discussed.

### 3.3.1 Current Difference Unit

The Current Differencing Unit (CDU) is a fundamental building block of numerous analog signal processing active elements such as CDTA (Current Differencing Transconductance Amplifier), DCVC (Differential Current Voltage Conveyor), OTRA (Operational Transresistance Amplifier) or CDBA (Current Differencing Buffered Amplifier. In these circuits CDU serves as an input block [1]. Purpose of CDU is to receive current input signals $I_p$ and $I_n$, at low-impedance input terminals *p* and *n*, and convey currents difference of these inputs through high-impedance output terminal *z* for further processing.

There is a twin purpose of the practically low, and ideally zero input impedance at *p* and *n* terminals.

First, it enables, in coupling with an external circuit, as CDU utilizes input gates for a straight voltage-to-current conversion. Second, it removes the impact of parasitic impedances on

current conveyance into the CDU [2]. A positive consequent phenomenon consists in conserving practically very low, ideally zero voltage of *p* and *n* input terminals. The high, ideally infinity impedance of the output *z* terminal of CDU is required due to its required performance as an ideal current source for providing independent load $Z_L$. In other words, value of the output z-current should be independent of the loading impedance.

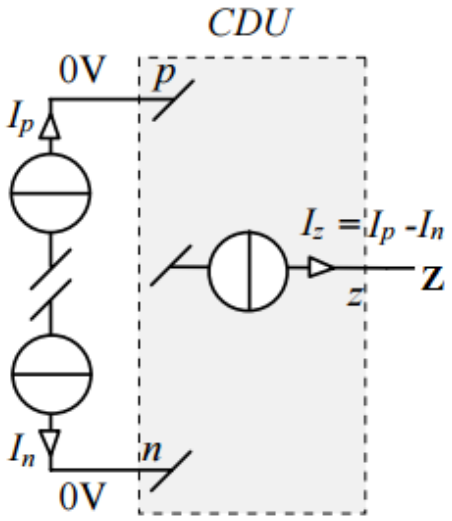


Fig.3.3. Ideal Current Differencing unit [40]

In reality, the CDU have some internal impedances i.e $Z_p$, $Z_n$, and $Z_o$ according to Figure 3.4. In addition with external impedances $Z_{ip}$, $Z_{in}$, and $Z_L$, they lead to a non ideal CDU behaviour. The input impedances $Z_p$ and $Z_n$ have also inductive components, which adversely affects the circuit performance by increasing the input impedance at higher frequencies. The internal current source is other contributor of non ideal behaviour since its current gain *b* is not unity, also it is dependent on frequency, and it is determined from nonlinear I/V characteristic. Also nonlinear properties of different internal blocks may come into effect, depending on a tangible implementation of the CDU.

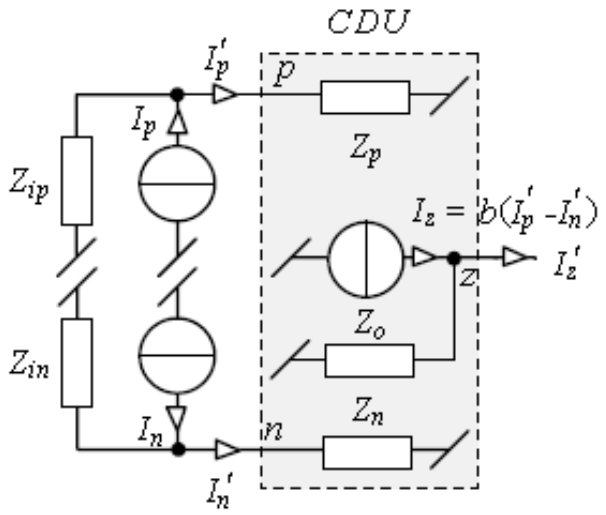


Fig.3.4. CDU with parasitic impedances being considered [1]

From above discussion it is concluded that CDU show nonzero parasitic impedances at p and n terminals. But in spite of deviation from ideal behaviour, these impedances are purposely implemented in practical circuit analysis, with the aim of their precise predetermination at least for low-frequency region. In this dissertation we restrict our discussion to ideal CDU.

### 3.3.2 Voltage Buffer Unit

Voltage follower is an electronic circuit whose main function is to cascade a high impedance source with a low impedance load without significant distortion or attenuation of the signal. So the output voltage of buffer replicates the input voltage of buffer with loading the source. Buffers are generally used in analog systems to diminish the loss of signal strength due to too much loading of output nodes. In simple words, buffer amplifier is an amplifier used in electronic systems which is designed to have an amplifier gain of one (1). They are primarily used in impedance matching. The advantage of which is maximization of energy transfer between the systems or circuits. The two main types of buffers are voltage buffer and current buffer. The purpose of each is to isolate the mentioned characteristics to avoid loading of input circuit from output stage [5].

Another name for buffer amplifier is voltage follower. A voltage buffer amplifier is used to transfer voltage from a first circuit with high output impedance level, to a second circuit, having a low input impedance level. The intermediate buffer amplifier forbids the second circuit from loading the first circuit, without any interference with its desired operation. A buffer is unity-gain amplifier with extremely high input resistance and very low output resistance, it is also known as Voltage Follower. The ideal voltage buffer properties are:

output resistance should be zero and Input resistance should be infinite. Also perfect linearity, in spite of signal amplitudes, fast output response independent of speed of the input signal. CDDOBA have two output terminals with complimentary voltage values. Voltage buffer is output unit of CDDOBA.

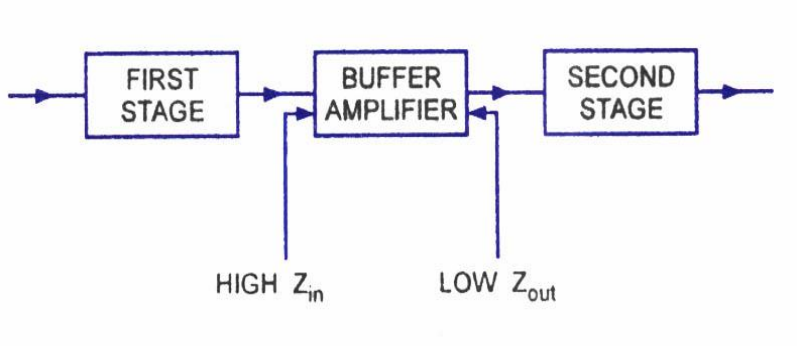


Fig.3.5. Buffer amplifier used to cascade circuits with mismatched impedance values [5]

## 3.4 CDDOBA Implementation Using AD844

Active current signalling circuit CDDOBA is realized by commercially available CFAs, AD844. Derived from conventional implementation of CDBA which uses two AD844s and result in a noisy output w terminal. Proposed circuit contain four CFAs. This new implementation transfers *w* terminal voltage of second AD844 into the *p*-terminal of the third AD844 and z terminal voltage of third AD844 into p terminal of fourth.

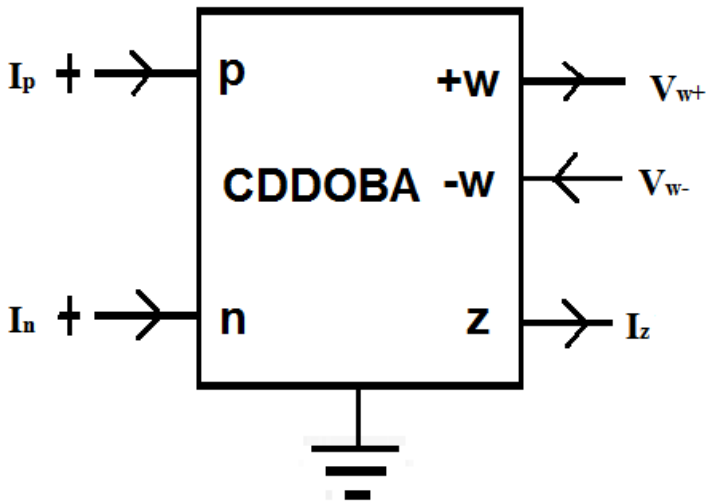


Fig.3.6. Block diagram of Ideal CDDOBA

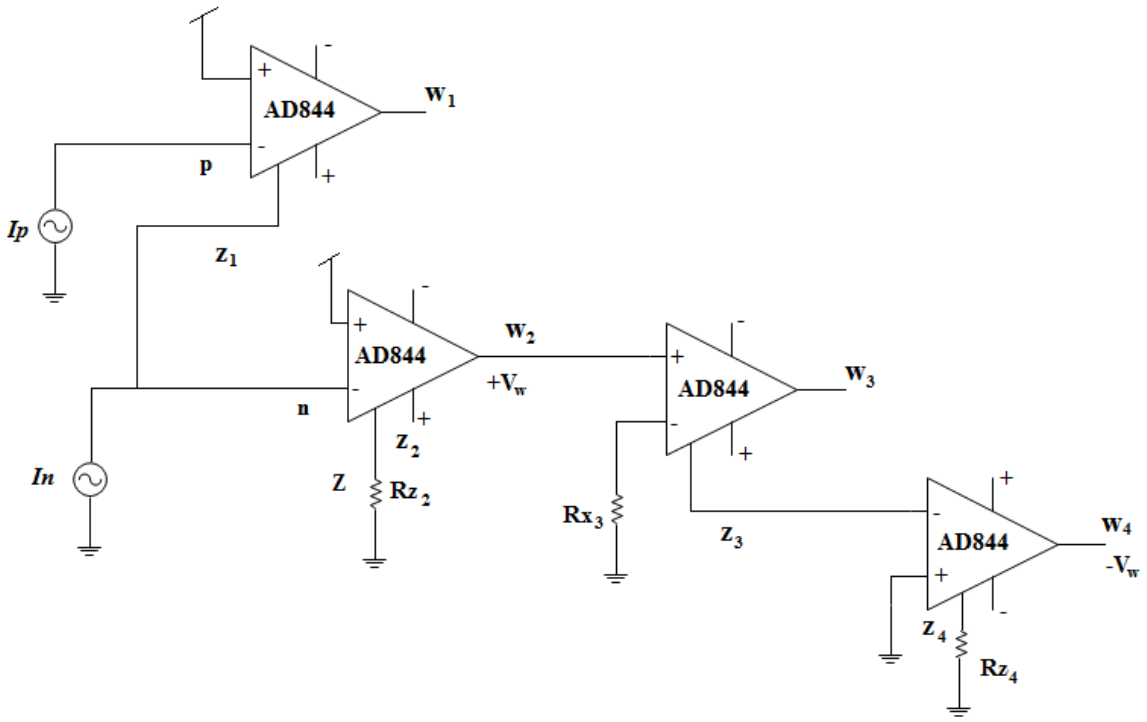


Fig.3.7. CDDOBA implementation using AD844

Four AD844 CDDOBAs shows good agreement between simulated and experimental results at frequency lesser than few MHz but at high frequency range divergence arise because of stray capacitances of AD844s which results in attenuations at high frequencies. CDDOBA advantages are mainly in the implementation of continuous-time filters [7].

**Simulation settings**

CDDOBA implementation using AD844 as shown in Figure 3.7, was simulated in PSPICE using AD844 SPICE Macro-model library file. The bias supply voltages were chosen as ±5V. The following terminating impedances were used in characterization of the CDDOBA as $R_{w1}$=10KΩ, $R_{x3}$=10KΩ, $R_{w3}$=10KΩ, $R_{z4}$=10KΩ, $R_{w4}$=10KΩ.

The following PSPICE analysis has been carried out to show the input output port relationship.

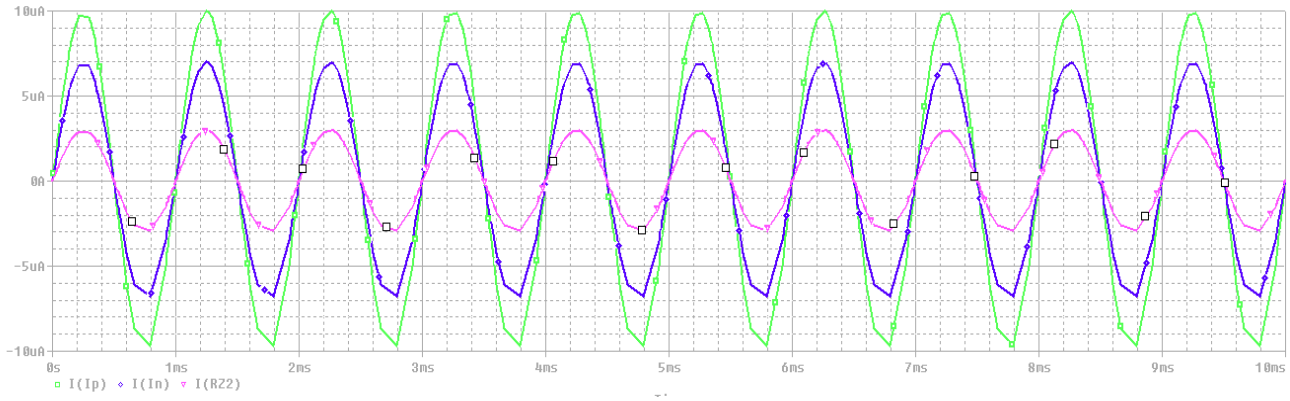


Fig.3.8. Transient response to show that current at ports z is difference of current at p and n

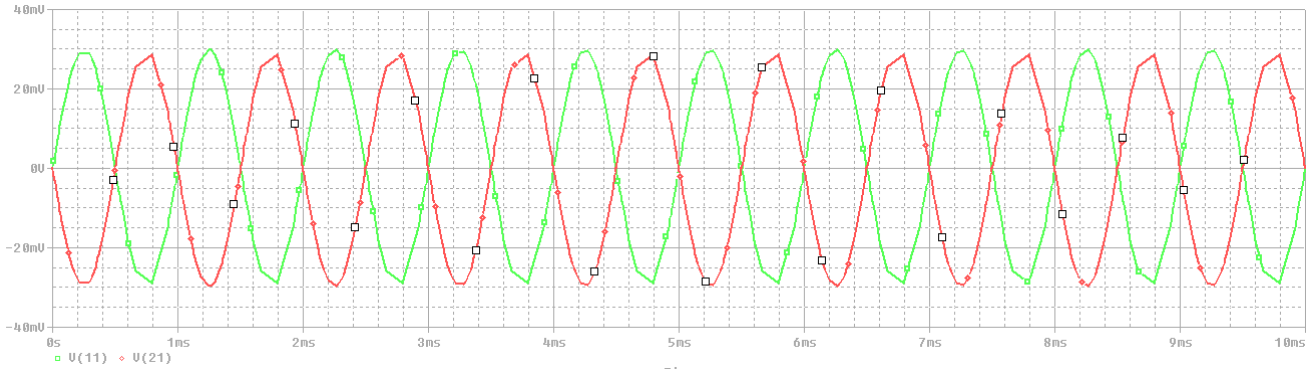


Fig.3.9. Transient response to show that voltage value at w+ and w- terminal is complimentary

## 3.5 Application of CDDOBA in Signal Processing

### 3.5.1 Amplifier

An amplifier gives the output that is scaled version of input voltage/current signal. Broadly amplifiers can be classified on the basis of their circuit configuration and methods of operation. In real world, sensors like piezo-electric, thermocouple etc. have small output signal. So by using amplifier their output can be amplified to drive the further circuitry such as lamp. Gain is basically ratio of the output divided by the input. Gain is unit less quantity as it's a ratio. In electronic three types of amplifier gain can be measured such as Voltage Gain (Av), Current Gain (Ai) and Power Gain (Ap). Further amplifier can be classified on the basis of polarity of input and output as inverting and non-inverting. Voltage mode amplifier is realized using CDDOBA as shown in Figure 3.10. It consists of one CDDOBA and two resistors $R_1$ and $R_2$. Input is applied at p terminal and output is taken at $+V_w$ and $-V_w$ terminals.

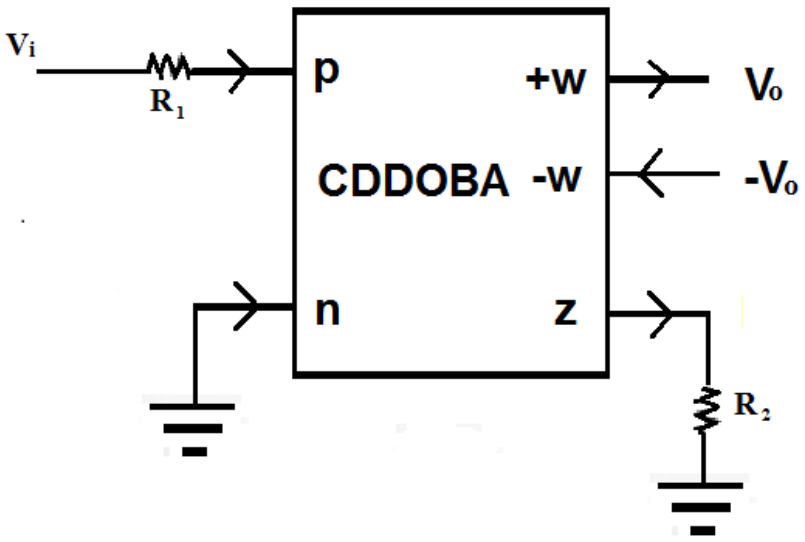


Fig.3.10. Block diagram of amplifier realized using CDDOBA

Amplifier designed using CDDOBA can serve as both inverting and non-inverting amplifier with cut off frequencies in MHz range. A simple CDDOBA amplifier circuit using IC AD844 is shown in figure 3.11. The voltage gain of circuit is described as follow

When output taken at +w terminal transfer function is

$$\frac{Vo_1}{V_i} = \frac{R_2}{R_1} \tag{3.5}$$

Similarly, If output taken at –w terminal it act as inverting amplifier with transfer function

$$\frac{Vo_2}{V_i} = -\frac{R_2}{R_1} \tag{3.6}$$

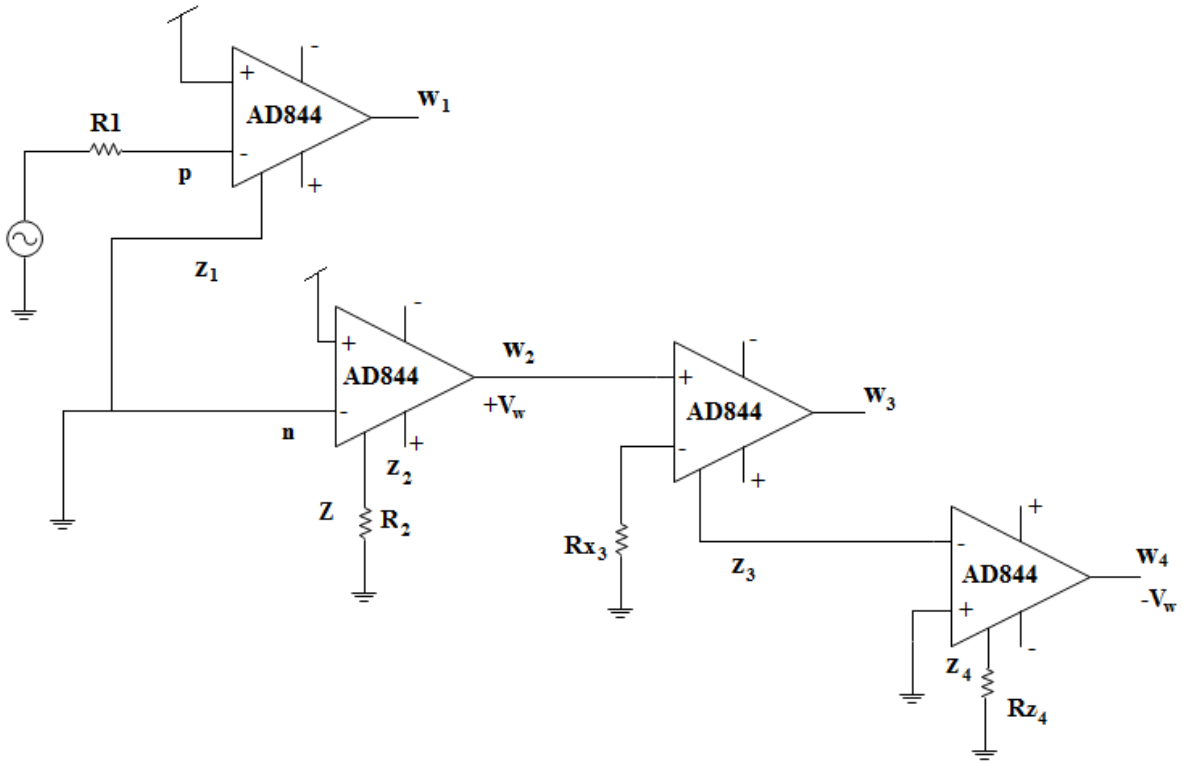


Fig.3.11. Simple amplifier realized using CDDOBA

**Simulation settings**

The amplifier shown in Figure 3.11 was simulated in PSICE. The bias supply voltages were taken as ±5V. The passive component values are $R_{w1}$= 10KΩ, $R_{x3}$= 10KΩ, $R_{w3}$= 10KΩ, $R_{z4}$= 10KΩ, $R_{w4}$=10KΩ, $R_1$=1KΩ and $R_2$=2KΩ.

The PSPICE simulation results shows the cut off frequencies and gain are

Inverting amplifier = 2.79MHz  Non inverting amplifier = 4.5MHz

Input voltage = 10mV  Output Voltage = 20mV  Gain = 2


Fig.3.12. Frequency response of simple Amplifier using CDDOBA

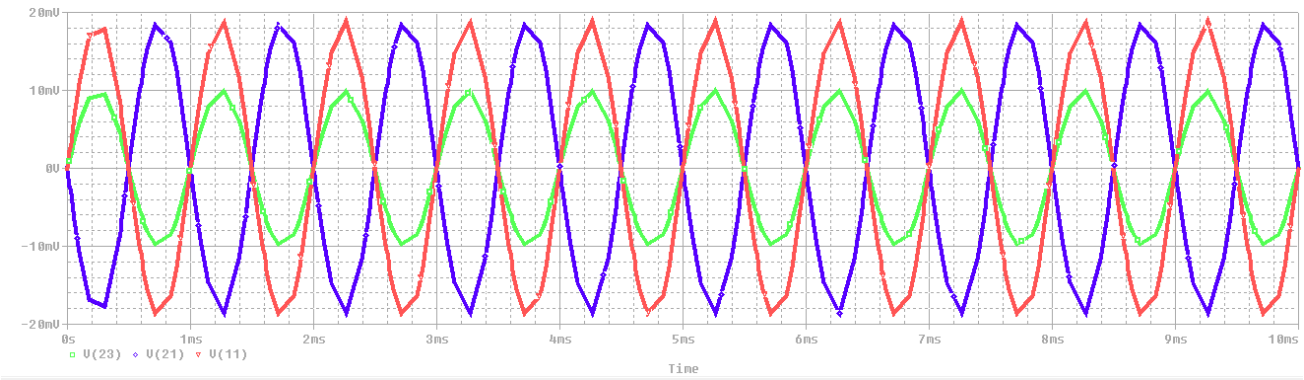


Fig.3.13. Transient response of simple Amplifier using CDDOBA

### 3.5.2 Differentiator and Integrator

***Differentiator***

Differentiation is a linear operation in analog signal processing that gives the derivative of the signal processed. Differentiation can be used as peak detector: the derivative of a signal gives a zero crossing whenever the analog signal attains a peak value. If a signal is filtered and then passed through the differentiator, this method is more robust then detecting the peak amplitude because added noise could give erratic outcomes. Proposed differentiator design using CDDOBA is as shown in Figure 3.13. It uses two resistors and one capacitor. Input is applied at p terminal and output is taken at +w and –w terminal and get lead of 90º and lag of 90º respectively at these terminals. The input output relation can be characterized as

At terminal +w

$$\frac{V_o}{V_i} = \frac{sCR_2}{1+R_1Cs} \qquad (3.7)$$

At terminal –w

$$\frac{V_o}{V_i} = -\frac{sCR_2}{1+R_1Cs} \qquad (3.8)$$

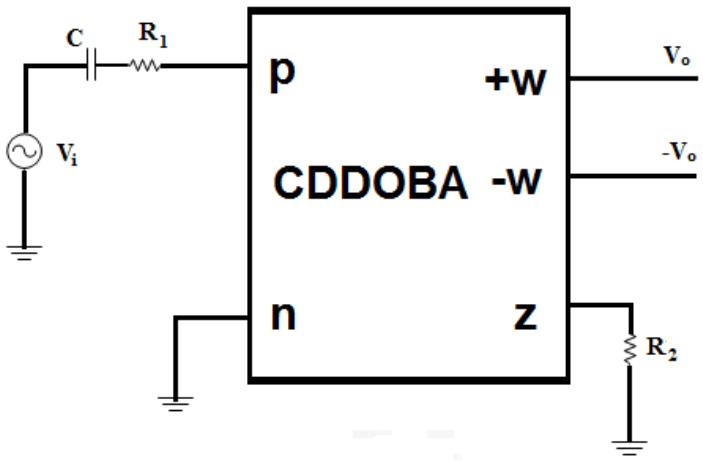


Fig.3.14. Differentiator using CDDOBA (Block diagram)

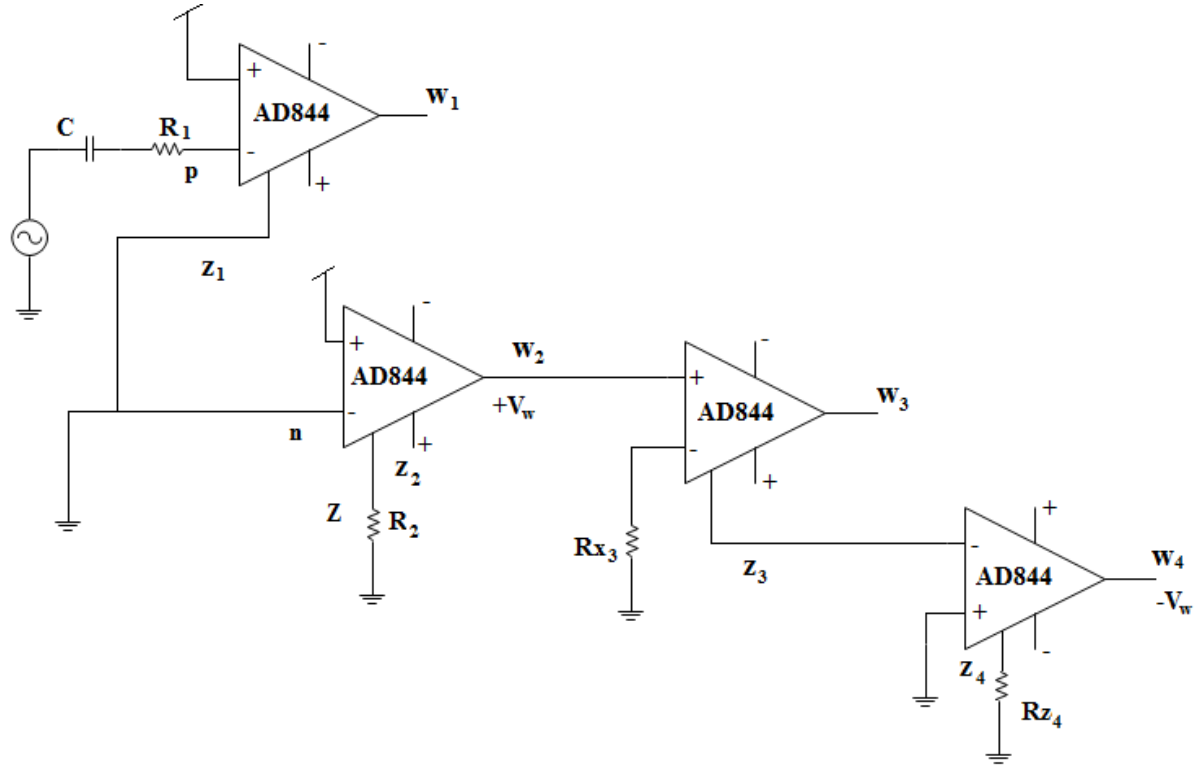


Fig.3.15. CDDOBA based differentiator

**Simulation settings**

The differentiator shown in figure 3.15 was simulated using PSPICE. The bias supply voltages were taken as ±5V. The passive component values are $R_{w1}$=10KΩ, $R_{x3}$=10KΩ, $R_{w3}$=10KΩ, $R_{z4}$=10KΩ, $R_{w4}$=10KΩ, $R_1$=100Ω, $R_2$=20KΩ and C= 25nF. Applied input triangular wave is of amplitude 50mV.

The time response of the Fig 3.15 is shown as follow

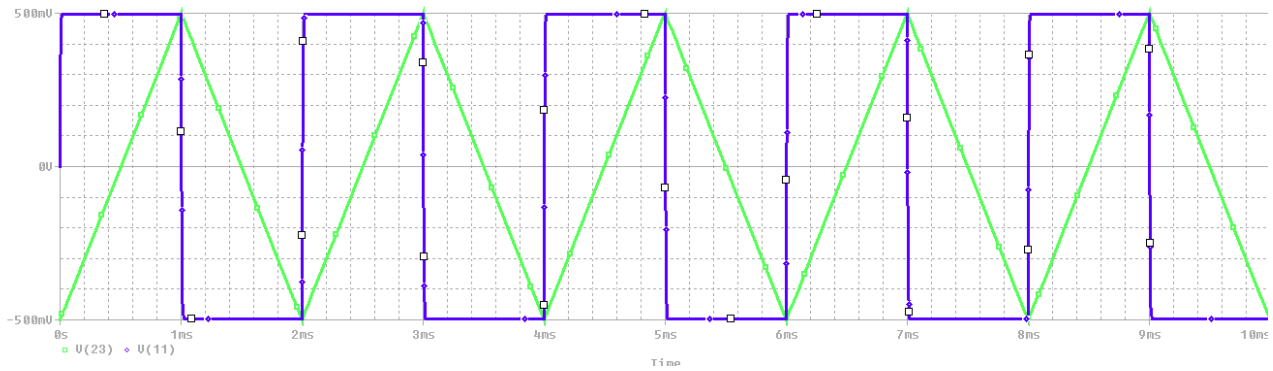


Fig.3.16. Time response of differentiator realized using CDDOBA

***Integrator***

Integration is a basic linear function in analog signal processing. Mathematically, the integral gives the area under the wave form or analog signal. Infrequency domain, integration is defined by a transfer characteristic whose slope decreases by 20dB/decade. Proposed integrator design using CDDOBA is as shown in Fig. It uses one resistors and one capacitor. Input is applied at p terminal and output is taken at +w and –w terminal and get lag of 90º and lead of 90º respectively at these terminals. Transfer function at two output terminals is given as

At terminal +w

$$\frac{V_o}{V_i} = \frac{1}{R_1 Cs} \tag{3.9}$$

At terminal –w

$$\frac{V_o}{V_i} = -\frac{1}{R_1 Cs} \tag{3.10}$$

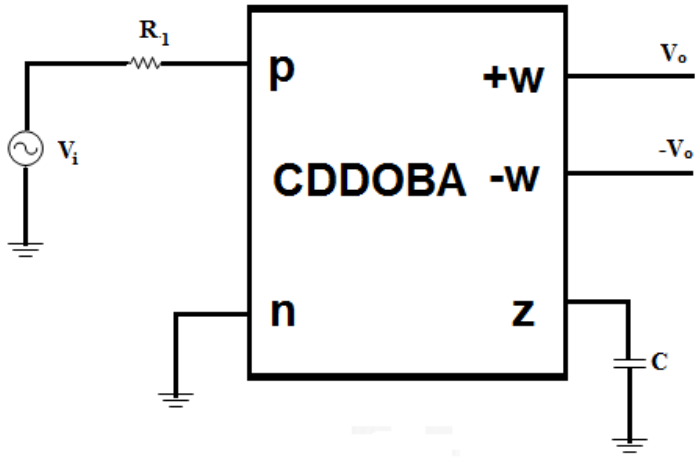


Fig.3.17. Integrator using CDDOBA (Block diagram)

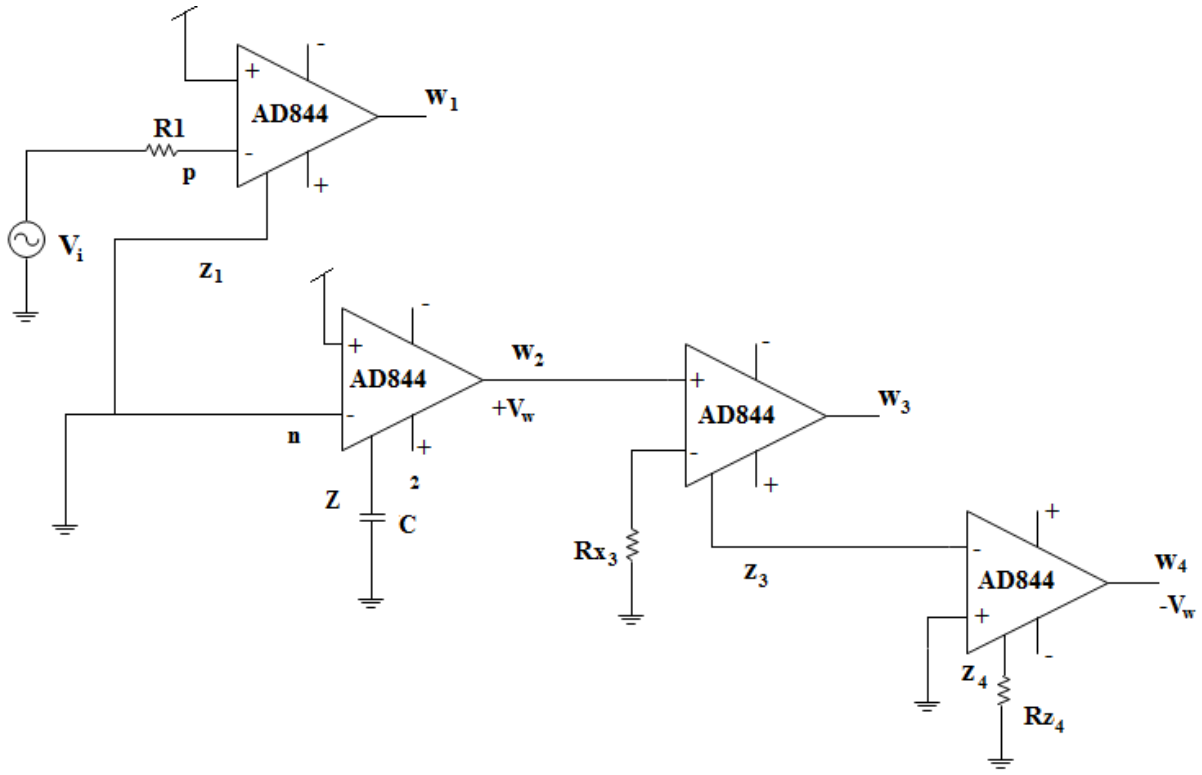


Fig.3.18. CDDOBA based Integrator

**Simulation settings**

The integrator shown in Figure 3.18, was simulated using PSPICE. The bias supply voltages were taken as ±5V. The passive component values are $R_{w1}$= 10KΩ, $R_{x3}$= 10KΩ, $R_{w3}$= 10KΩ, $R_{z4}$=10KΩ, $R_{w4}$=10KΩ, $R_1$=10KΩ and C= 100nF. Applied input square wave is of amplitude value 2.5V. The time response is shown in Figure 3.19.

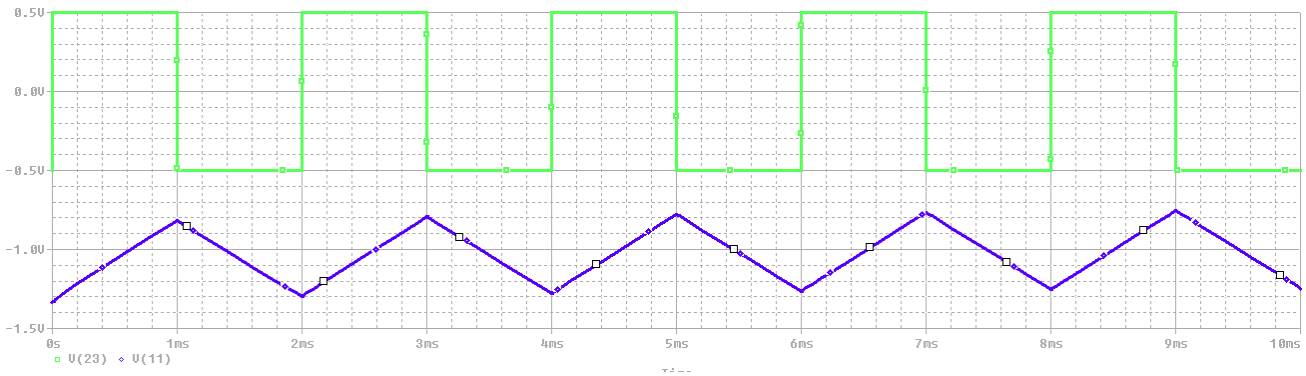


Fig.3.19. Time response of integrator implemented using CDDOBA

### 3.5.3 First Order Filters

CDDOBA advantages are mainly in designing continuous time filters. In following sections first order low pass, high pass and all pass filter are realized using CDDOBA and simulation results are compared with filters designed using conventional op-amp using same passive component values.

#### *3.5.3.1 First Order Low Pass Filter*

A low-pass filter is a filter that passes signals with a frequency lower than a certain cut off frequency and attenuates signals with frequencies higher than the cut off frequency. The amount of attenuation for each frequency depends on the filter design. The filter is sometimes called a high-cut filter, or treble cut filter in audio applications. Low-pass filters exist in many different forms, including electronic circuits (such as a *hiss filter* used in audio), anti-aliasing filters for conditioning signals prior to analog-to-digital conversion, digital filters for smoothing sets of data, acoustic barriers, blurring of images, and so on. Figure 3.19 shows the implementation of first order low pass filter using CDDOBA. It consist of CDDOBA circuit realized using commercially available IC AD844 and two resistors and one capacitor. The input-output relation is characterised as

$$\frac{V_o}{V_i} = -\frac{R_2}{R_1} \cdot \frac{1}{1+R_2Cs} \tag{3.11}$$

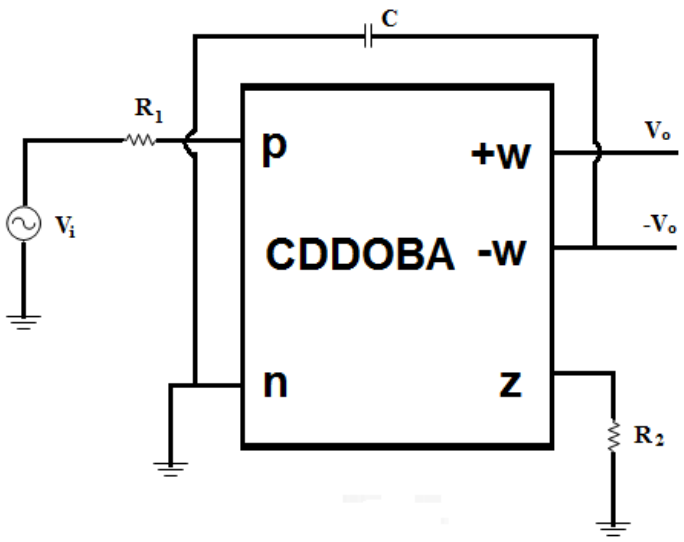


Fig.3.20. Implementation of first order LPF using CDDOBA

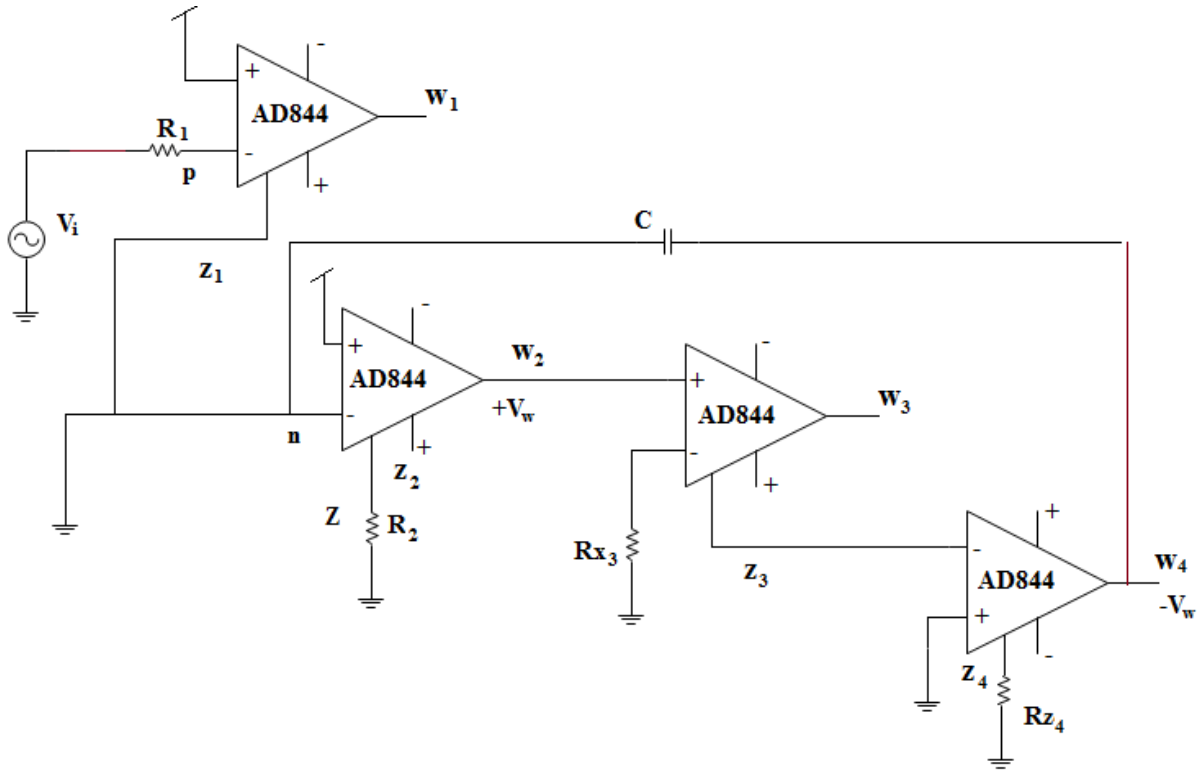


Fig.3.21. First order LPF using IC AD844

**Simulation settings**

The low pas filter shown in Figure 3.21, was simulated using PSPICE. The bias supply voltages were taken as ±5V. The passive component values are $R_{w1}$= 10KΩ, $R_{x3}$= 10KΩ, $R_{w3}$= 10KΩ, $R_{z4}$=10KΩ, $R_{w4}$=10KΩ, $R_1$=1KΩ, $R_2$=2KΩ and C=100nF. To get the cut off frequency of 795.77 Hz applied voltage is 50mV.

The PSPICE simulation results shows the cut off frequency is 800.67 Hz

Transient response of both output terminals of LPF at frequency 100Hz is shown below

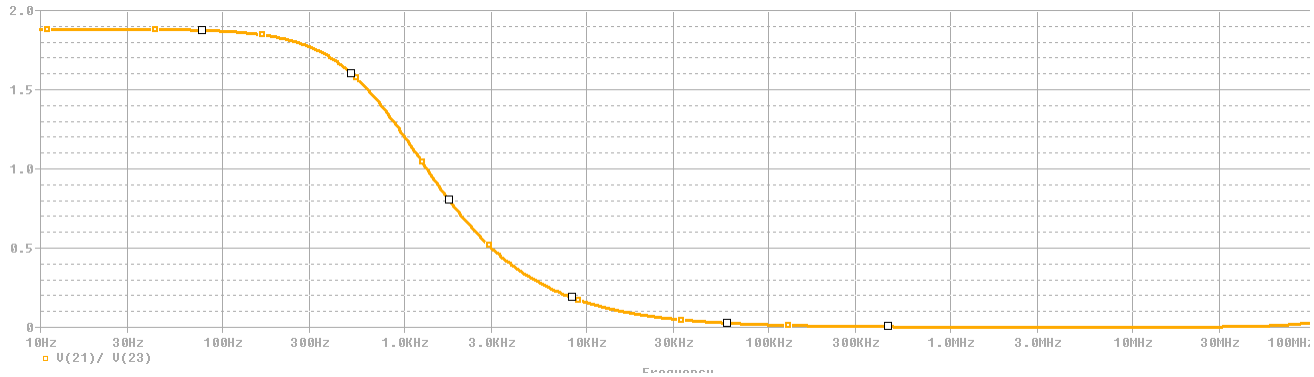


Fig.3.22.Frequency response of first order low pass filter using CDDOBA

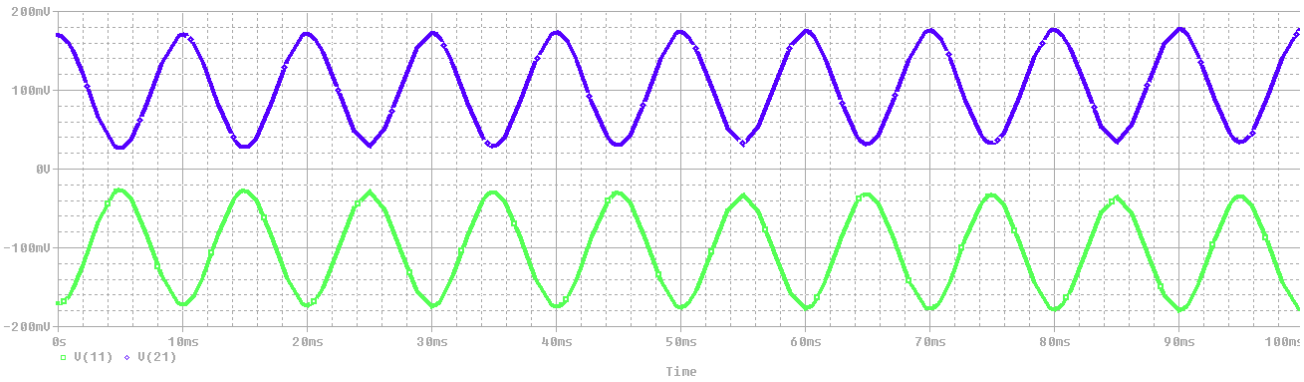


Fig.3.23.Transient response of first order low pass filter using CDDOBA

*3.5.3.2 First Order High Pass Filter*

A high-pass filter is an electronic filter that passes signals with a frequency higher than a certain cut off frequency and attenuates signals with frequencies lower than the cut off frequency. The amount of attenuation for each frequency depends on the filter design. A high-pass filter is usually modelled as a linear time-invariant system. It is sometimes called a low-cut filter or bass-cut filter. High-pass filters have many uses, such as blocking DC from circuitry sensitive to non-zero average voltages or radio frequency devices. They can also be used in conjunction with a low-pass filter to produce a band pass filter.

Figure 3.23 shows the implementation of first order high pass filter using CDDOBA. It consist of CDDOBA circuit realized using commercially available IC AD844 and two resistors and one capacitor. The input-output characteristic is given as

At terminal –w

$$\frac{V_o}{V_i} = -\frac{sCR_2}{1+R_1Cs} \qquad (3.12)$$

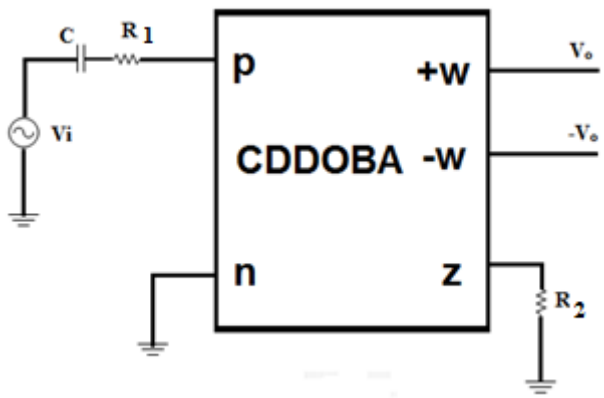


Fig.3.24. Implementation of first order HPF using CDDOBA

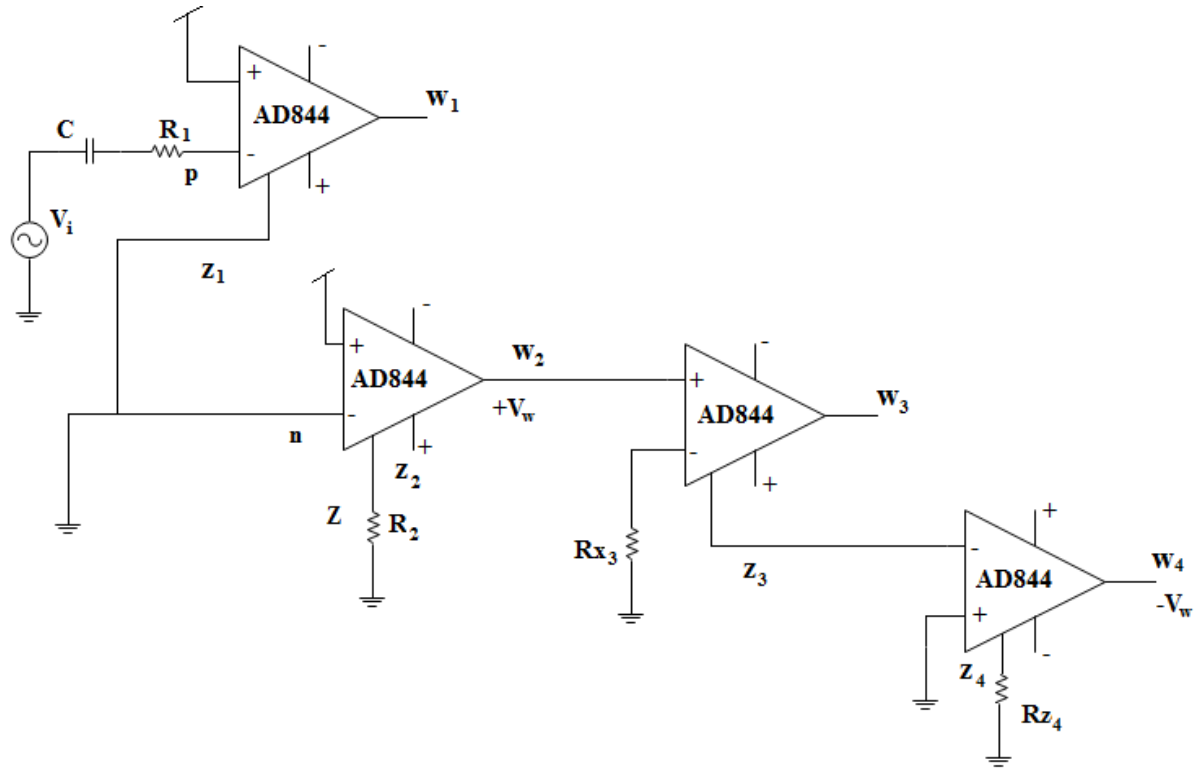


Fig.3.25. First order HPF using IC AD844

**Simulation settings**

The high pass filter shown in Figure 3.25, was simulated using PSPICE. The bias supply voltages were taken as ±5V. The passive component values are $R_{w1}$= 10KΩ, $R_{x3}$= 10KΩ, $R_{w3}$= 10KΩ, $R_{z4}$=10KΩ, $R_{w4}$=10KΩ, $R_1$=100Ω, $R_2$=200Ω and C=1nF. To get the cut off frequency of 1.59 MHz input voltage applied is 50mV.

The PSPICE simulation results shows the cut off frequency is 1.499 MHz

Transient response of both output terminals of HPF at frequency 100 KHz is shown below

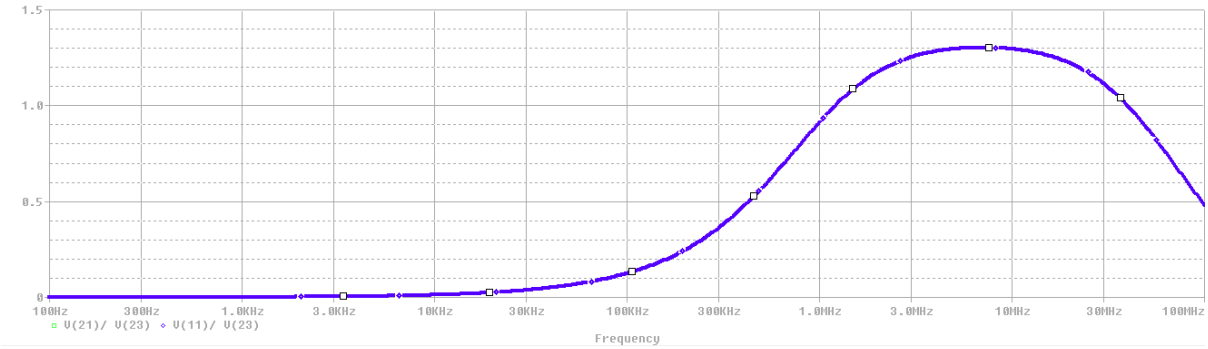


Fig.3.26. Frequency response of first order high pass filter using CDDOBA

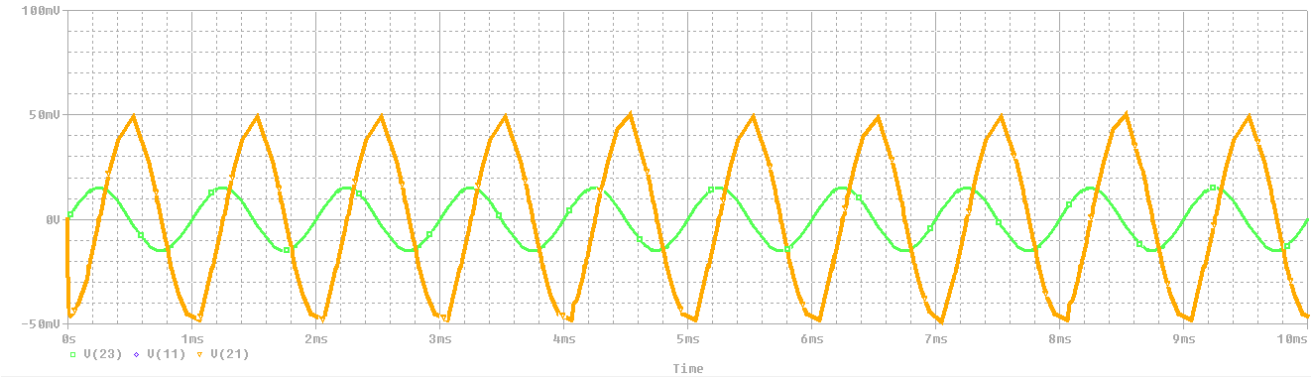


Fig.3.27. Transient response of first order high pass filter using CDDOBA

### *3.5.3.3 First Order All Pass Filter*

An all-pass filter is a signal processing filter that passes all frequencies equally in gain, but changes the phase relationship among various frequencies. It does this by varying its phase shift as a function of frequency. Generally, the filter is described by the frequency at which the phase shift crosses 90. They are generally used to compensate for other undesired phase shifts that arise in the system, or for mixing with an un shifted version of the original to implement a notch comb filter. They may also be used to convert a mixed phase filter into a minimum phase filter with an equivalent magnitude response or an unstable filter into a stable filter with an equivalent magnitude response.

All-pass filters are one of the most significant building blocks of several analog signal processing applications [5]-[6]. They are normally used to provide a frequency dependent delay whereas keeping the gain constant over the required frequency range. Figure 3.25 shows the implementation of first order all pass filter using CDDOBA. It consist of CDDOBA circuit realized using commercially available IC AD844 and two resistors and two capacitors. By mathematical analysis transfer function at –w terminal is given as follow

$$\frac{V_o}{V_i} = -\frac{R_2}{R_1} \cdot \frac{1-R_1C_1s}{1+R_2C_2s} \qquad (3.13)$$

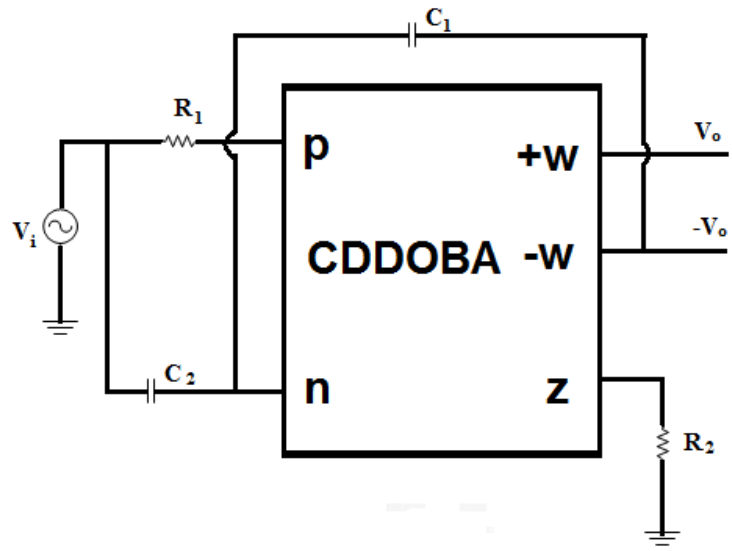


Fig.3.28. Implementation of first order all pass filter using CDDOBA

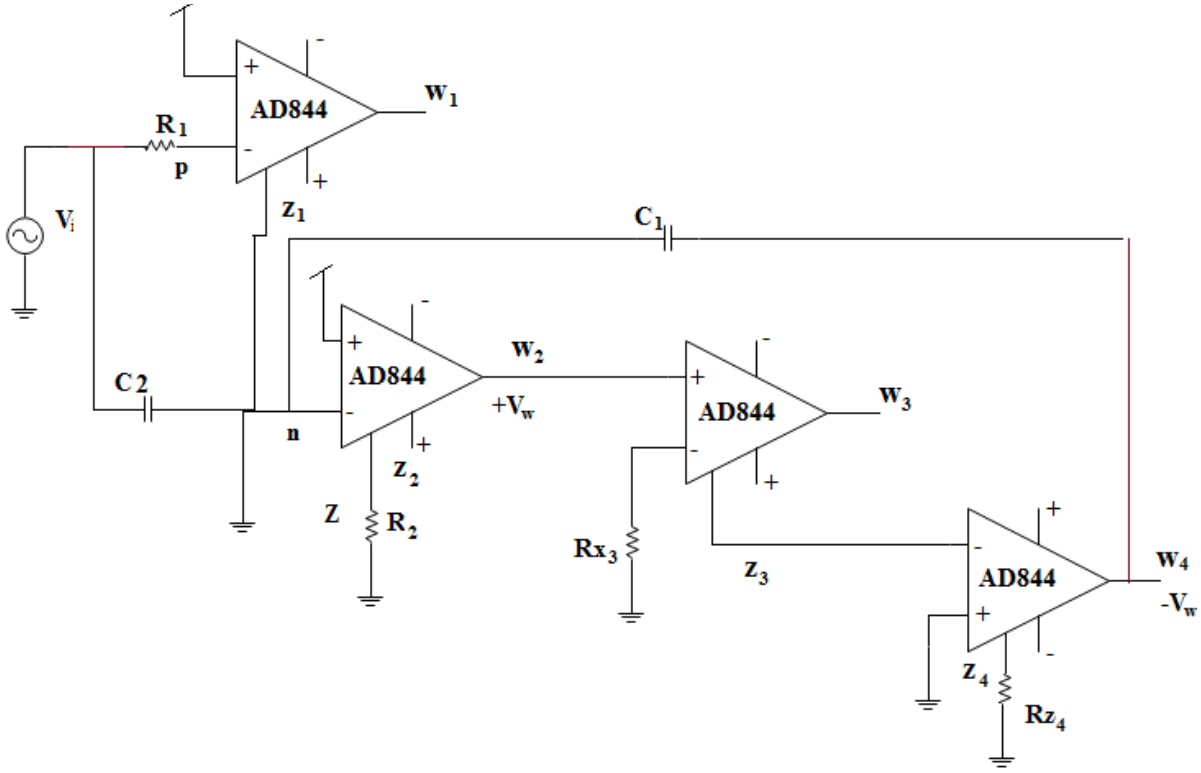


Fig.3.29. First order all pass filter using IC AD844

**Simulation settings**

The all pass filter shown in Figure 3.29, was simulated using PSPICE. The bias supply voltages were taken as ±5V. The passive component values are $R_{w1}$= 10KΩ, $R_{x3}$=10KΩ, $R_{w3}$=10KΩ, $R_{z4}$=10KΩ, $R_{w4}$=10KΩ, $R_1$=5KΩ, $R_2$=5KΩ and $C_1$=1pF, $C_2$= 1pF. Input voltage applied is 15mV.

Phase response of all pass filter is given below in Figure 3.30

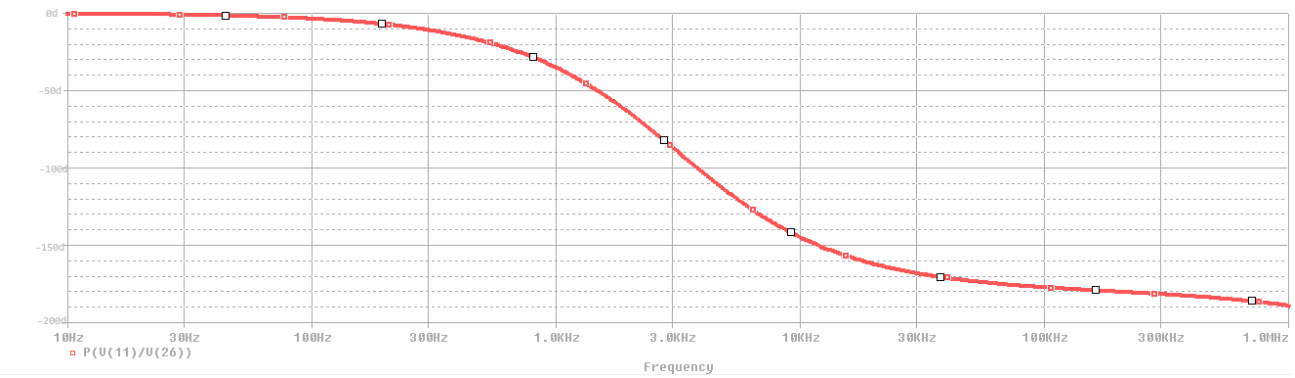


Fig.3.30.Phase response of first order all pass filter using CDDOBA

## 3.6 Conclusion

In the above chapter the basic architecture and part relationships of CDDOBA is presented. The generic architecture of CDDOBA and its behavioral model and an exemplary implementation using off the shelf available component AD844 along with general signal processing applications of CDDOBA has been presented.

## References


1. http://user.unob.cz/biolek/veda/articles/EDS08_2.pdf.
2. Kaçar, Firat, and Serdar Menekay. "Realization of a CMOS current differencing buffer amplifier and its filter application." *Electrical and Electronics Engineering (ELECO), 2011 7th International Conference on*. IEEE, 2011.
3. Aseem, Jaymeen, Jay Padaliya, and Vijay Savani. "Analysis and Characterization of Different Voltage Follower Topologies in 90 nm Technology." *International Journal of Emerging Technology and Advanced Engineering*, vol. 2, no. 12, pp. 229-235, 2012.
4. Yadav, Neeraj, et al. "Low voltage analog circuit design based on the flipped voltage follower." *International Journal of Electronics and Computer Science Engineering, ISSN*, vol. 6, no. 13, pp. 2277-1956, 2012.
5. Kacar, Fırat, and Y. Ozcelep. "CDBA Based Voltage-Mode First-Order All-pass Filter Topologies," *IU-JEEE* 11, vol. 32, no. 4, pp.1327-1332, 2011.
6. W. Tangsrirat, D. Prasertsom and W. Surakampontorn, "Low-voltage digitally controlled current differencing buffered amplifier and its application", *AEU - International Journal of Electronics and Communications*, vol. 63, no. 4, pp. 249-258, 2009.
7. C. Acar and S. Ozoguz, "A new versatile building block: current differencing buffered amplifier suitable for analog signal-processing filters", *Microelectronics Journal*, vol. 30, no. 2, pp. 157-160, 1999.

# CHAPTER 4

# BIQUAD FILTER REALIZATION USING CDDOBA

## 4.1 Introduction

In the previous chapter, applications (amplifier and filter) of CDDOBA in voltage mode signal processing have been discussed. CDDOBA is a versatile active building block similar to other derivatives of current conveyors. In this chapter, we discuss in detail about novel application of CDDOBA in the realization of voltage mode multifunction filter.

## 4.2 CDDOBA based Biquad Filter

Realisation of filters, particularly Biquad filters has been very prominent application of any block. Out of different filter configurations implemented from these blocks universal/multifunction filter realisation are preferred as they provide more than one filter function from the same structure. Apart from their usual application as standard second order building blocks for higher order filters. Multifunction Biquad filters find applications in phase locked loop FM stereo demodulators, touch tone telephone system and crossover networks used in three- way high fidelity loud speakers.

Multifunction filters can either be of fixed and usually at least three out of five generic filtering functions namely HP, LP, BP, band elimination (BE) and all pass (AP) are simultaneously available in current mode/voltage mode or both, or of variable topology type in which the nature and number of elements vary for different output responses. A multifunction Biquad is said to be 'Universal' if it is capable of realising all the five standard filter functions. Biquad/Multifunction active filters are chiefly versatile, as different filter functions can be realized using same topology. Many voltage mode Biquad filters comprise of more than one active current mode element, such as operational transconductance amplifiers, current conveyors and current feedback amplifiers, with their well known advantages of high slew rates and wide bandwidths are reported in literature [1]-[5].

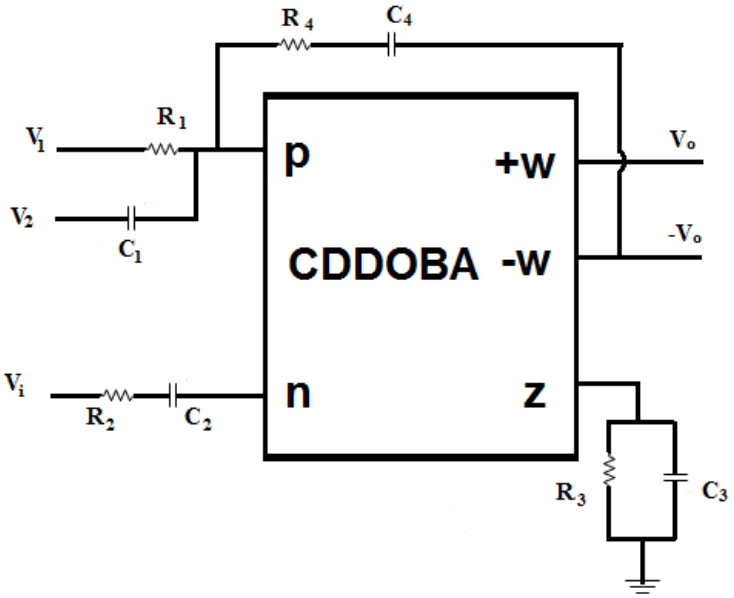


Fig.4.1 Block diagram of Biquad filter using CDDOBA

Though some active current mode element CDBA-based multi-function filters are proposed in literature, these reported circuits involve more than one CDBA. From the point of view of manufacturing cost and power dissipation, it is beneficial to keep the number of active elements at minimum.

In this section, a multi-input multi-output type voltage mode Biquad filter, employing one CDDOBA as the active element is proposed, which realizes all the five filter functions constrained to some passive elements value conditions, i.e., Low pass (LPF), High pass (HPF), Band pass (BPF), Band stop or notch (BSF) and All pass (APF), without changing the circuit topology. In this circuit with the condition $R_2C_2=R_4C_4$ (except APF and BSF), taking negative feedback to p input terminal. A Biquad voltage transfer function is as follow:

On solving, voltage at –w terminal is

$$V_o = -\left(\frac{R_3}{R_1}\right).\frac{S^2.V_2R_1C_1R_2C_2+(R_2C_2V_1+V_2R_1C_1-V_iC_2R_1)s+V_1}{s^2R_3C_3R_4C_4+(R_3C_3+R_4C_4-R_3C_4)s+1} \qquad (4.1)$$

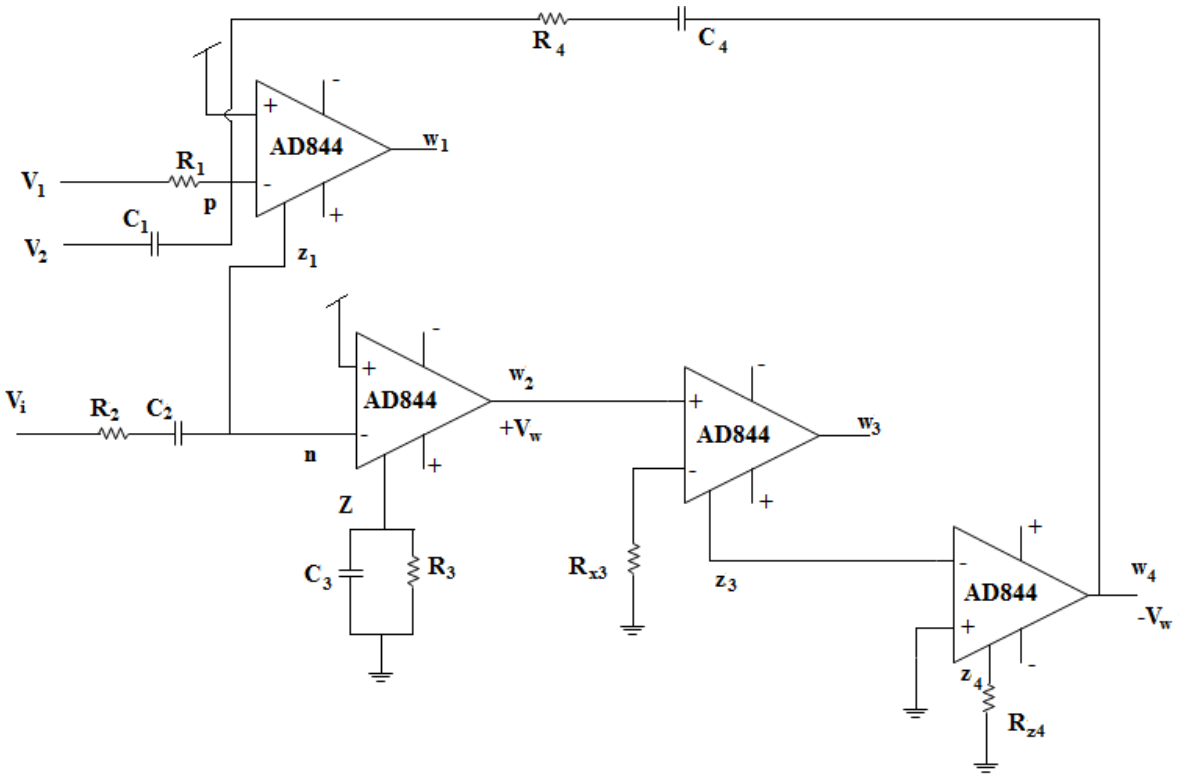


Fig.4.2.Biquad filter realization using IC AD844

**Circuit conditions**

In this circuit, with the condition $R_2C_2 = R_4C_4$ (except APF and BSF), Biquad voltage transfer functions ($V_o/V_{in}$) realize

1. LPF; if $V_2 = 0$, $V_1 = V_{in}$ , $R_1 = R_2$
2. HPF; if $V_1 = 0$, $V_2 = V_{in}$, $C_1 = C_2$
3. BPF; if $V_1 = V_2 = 0$
4. BSF; $V_1 = V_2 = V_{in}$, $R_1 = R_3 = 2R_2$, $C_2 = 2C_3 = 2C_1$
5. APF; $V_1 = V_2 = V_{in}$, $R_1 = R_3 = 4R_2$, $C_2 = 4C_3 = 4C_1$

### 4.2.1 Low pass Filter

Conditions: $V_2 = 0$, $V_1 = V_{in}$, $R_1 = R_2$, $R_2C_2 = R_4C_4$, $C_1 = 0$

On using mentioned conditions, transfer function is

$$\frac{V_o}{V_i} = -\left(\frac{R_3}{R_1}\right).\frac{1}{s^2R_3C_3R_4C_4+(R_3C_3+R_4C_4-R_3C_4)s+1} \qquad (4.2)$$

**Simulation settings**

The bias supply voltages were taken as ±5V. The passive component values are $Rw_1$=10KΩ, $R_{x3}$=10KΩ, $R_{w3}$=10KΩ, $R_{z4}$=10KΩ, $R_{w4}$=10KΩ, $R_1$=20KΩ, $R_2$=20KΩ, $R_3$=20KΩ, $R_4$=20KΩ, $C_2$=$C_4$=10nF and $C_3$=20nF. To get the cut off frequency of 562.149 Hz input voltage applied is 50mV.

Cut of frequency of low pass second order filter is 562.34 Hz. Transient response at frequency 100Hz and frequency response is as follow:

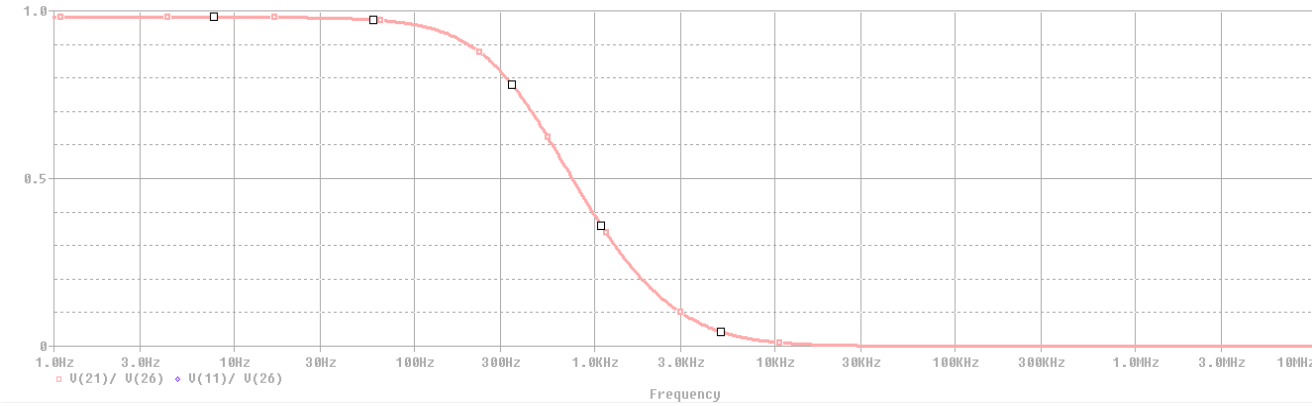


Fig.4.3. Frequency response of Second order Low pass filter

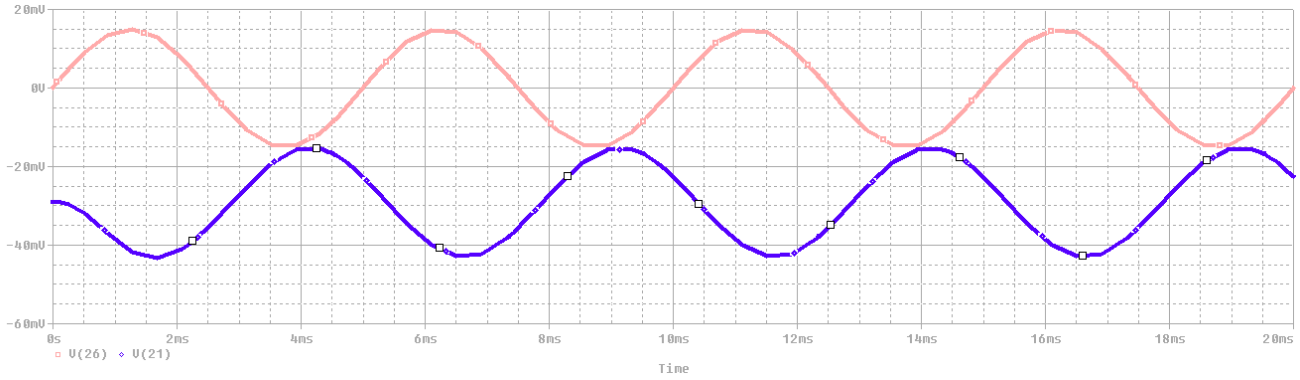


Fig.4.4. Transient response of Second order Low pass filter

### 4.2.2 High Pass Filter

Conditions: $V_1 = 0$, $V_2 = V_{in}$, $C_1 = C_2$, $R_2C_2 = R_4C_4$, $R_1$ = infinite

On using mentioned conditions, transfer function is

$$\frac{V_o}{V_i} = -R_3 \cdot \frac{s^2 . C_1 R_2 C_2}{s^2 R_3 C_3 R_4 C_4 + (R_3 C_3 + R_4 C_4 - R_3 C_4)s + 1} \qquad (4.3)$$

**Simulation settings**

The bias supply voltages were taken as ±5V. The passive component values are $Rw_1$=10KΩ, $R_{x3}$=10KΩ, $R_{w3}$=10KΩ, $R_{z4}$=10KΩ, $R_{w4}$=10KΩ, $R_2$=4KΩ, $R_4$=4KΩ, $R_3$=2KΩ and $C_1$=700pF, $C_2$=700pF, $C_3$=700pF, $C_4$=700pF. To get the cut off frequency of 80.307 KHz input voltage applied is 50mV.

Cut of frequency of high pass second order filter is 79.606 KHz. Transient response at frequency 150 KHz is as shown.

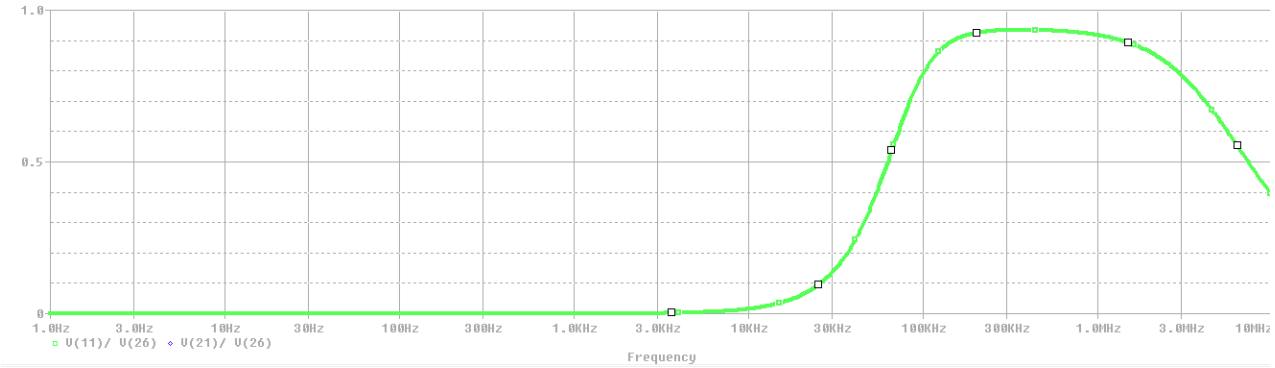


Fig.4.5. Frequency response of Second order high pass filter using CDDOBA

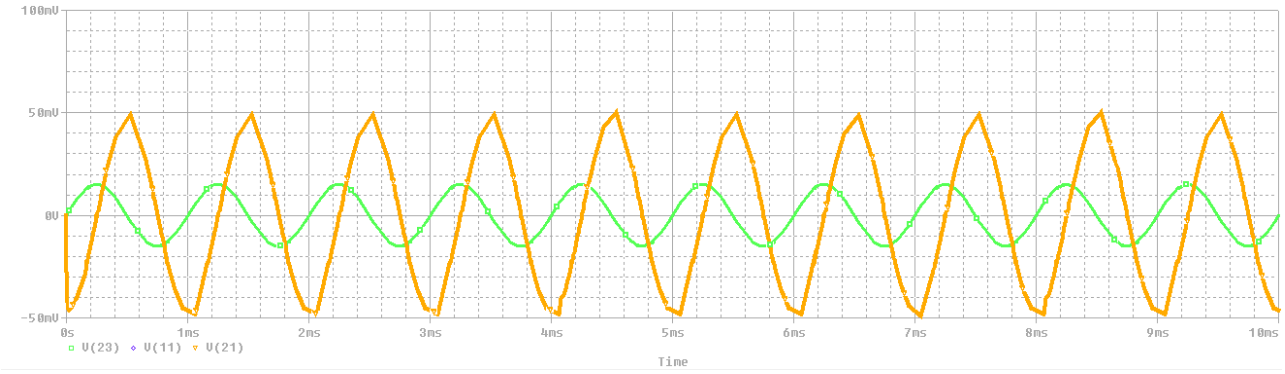


Fig.4.6. transient response of Second order high pass filter using CDDOBA

### 4.2.3 Band Pass Filter

Conditions: $V_1 = V_2 = 0$, $R_2C_2 = R_4C_4$

On using mentioned conditions, transfer function is

$$\frac{V_o}{V_i} = \frac{sR_3C_2}{s^2R_3C_3R_4C_4+(R_3C_3+R_4C_4-R_3C_4)s+1} \qquad (4.4)$$

**Simulation settings**

The bias supply voltages were taken as ±5V. The passive component values are $Rw_1$=10KΩ, $R_{x3}$=10KΩ, $R_{w3}$=10KΩ, $R_{z4}$=10KΩ, $R_{w4}$=10KΩ, $R_2$=10KΩ, $R_3$=10KΩ, $R_4$=10KΩ,

$C_2$=140nF, $C_3$=70nF and $C_4$=140nF. To get centre frequency of 160.6 Hz input voltage applied is 15mV.

Centre frequency of band pass second order filter is 163.7Hz. Transient response is taken at frequency 163Hz. PSPICE simulation result is as follow:

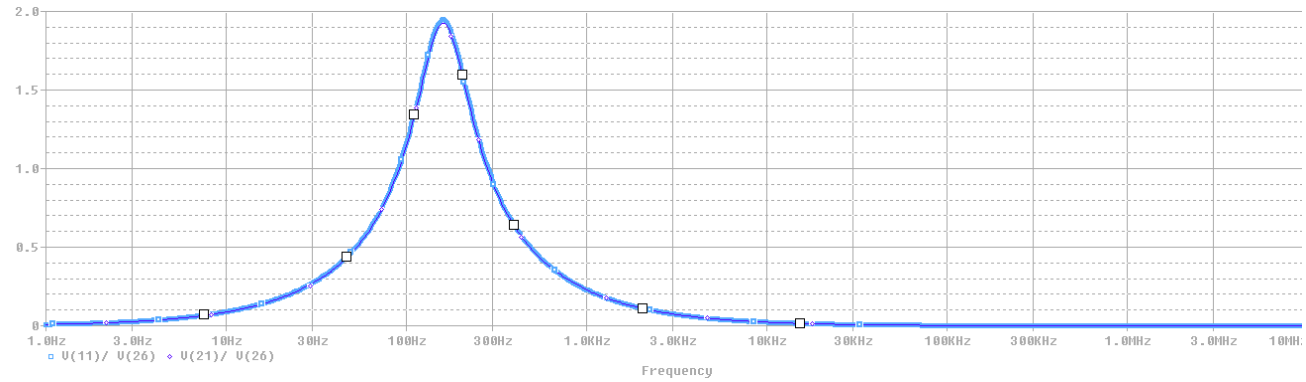


Fig.4.7. Frequency response of Second order Band pass filter implemented using CDDOBA

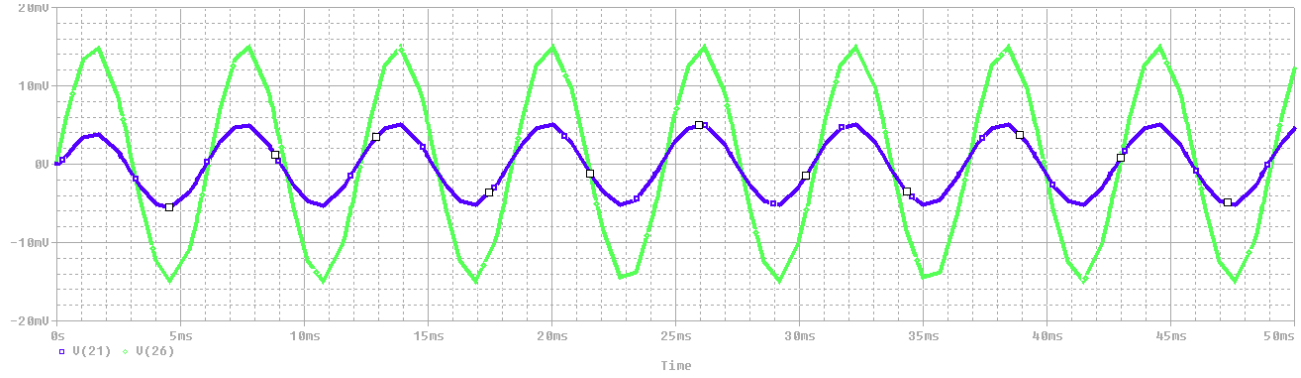


Fig.4.8. Transient response of Second order Band pass filter implemented using CDDOBA

### 4.2.4 Band Stop Filter

Conditions: $V_1 = V_2 = V_{in}$, $R_1 = R_3 = 2R_2$, $C_2 = 2C_3 = 2C_1$, $R_4$ and $C_4$ omitted

On using mentioned conditions, transfer function is

$$\frac{V_o}{V_i} = \frac{s^2 R_1 R_2 C_1 C_2 + 1}{s^2 R_3 C_3 R_2 C_2 + (R_3 C_3 + R_2 C_2)s + 1} \qquad (4.5)$$

**Simulation settings**

The bias supply voltages were taken as ±5V. The passive component values are $Rw_1$=10KΩ, $R_{x3}$=10KΩ, $R_{w3}$=10KΩ, $R_{z4}$=10KΩ, $R_{w4}$=10KΩ, $R_1$=40KΩ, $R_3$=40KΩ, $R_2$=20KΩ, $C_1$=10nF, $C_3$=10nF and $C_2$=20nF. To get the centre frequency of 397.5 Hz input voltage applied is 15mV.

Centre frequency of Band reject second order filter is 397.1Hz. Transient response is taken at frequency 100Hz. PSPICE simulation result is as follow:

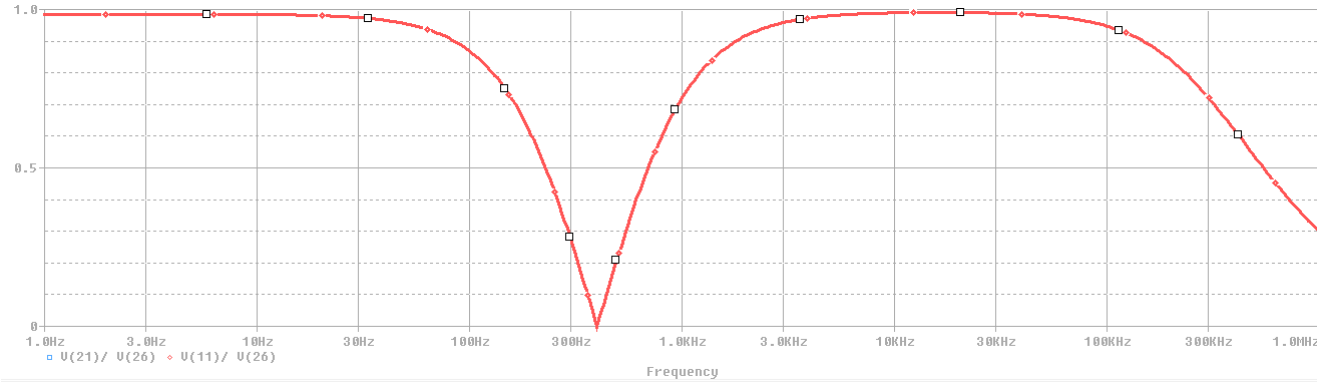


Fig.4.9. Frequency response of Second order band stop filter implementation using CDDOBA

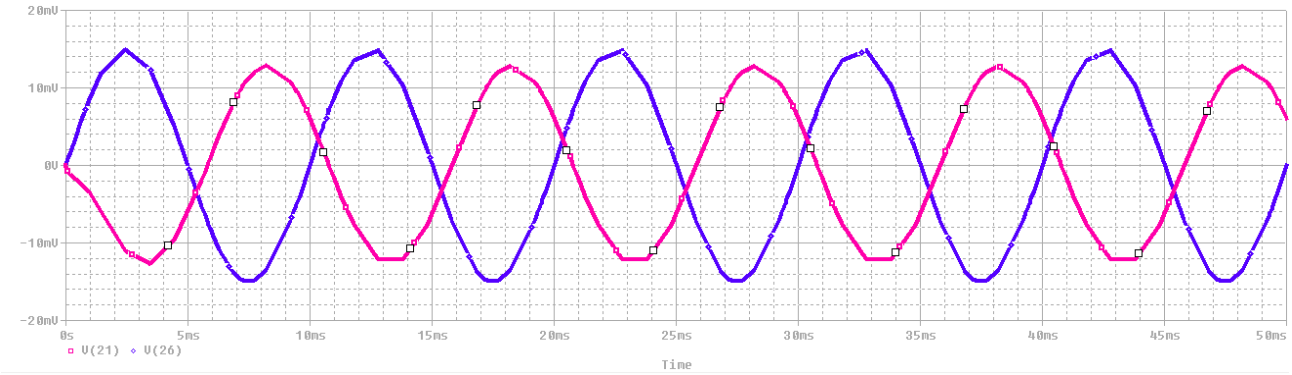


Fig.4.10. Transient response of Second order band stop filter implementation using CDDOBA

### 4.2.5 All Pass Filter

Conditions: $V_1 = V_2 = V_{in}$, $R_1 = R_3 = 4R_2$, $C_2 = 4C_3 = 4C_1$, $R_4$ and $C_4$ omitted

On solving using mentioned conditions, transfer function is

$$\frac{V_o}{V_i} = \frac{s^2R_1R_2C_1C_2+(C_1R_1+C_2R_2-C_2R_1)s+1}{s^2R_3C_3R_2C_2+(R_3C_3+R_2C_2)s+1} \qquad (4.6)$$

With above conditions fulfilled it behaves as all pass filter.

**Simulation settings**

The bias supply voltages were taken as ±5V. The passive component values are $Rw_1$=10KΩ, $R_{x3}$=10KΩ, $R_{w3}$=10KΩ, $R_{z4}$=10KΩ, $R_{w4}$=10KΩ, $R_1$=50KΩ, $R_3$=50KΩ, $R_2$=12.5K, $C_2$=4nF and $C_1$=1nF, $C_3$=1nF. Input voltage applied is 15mV.

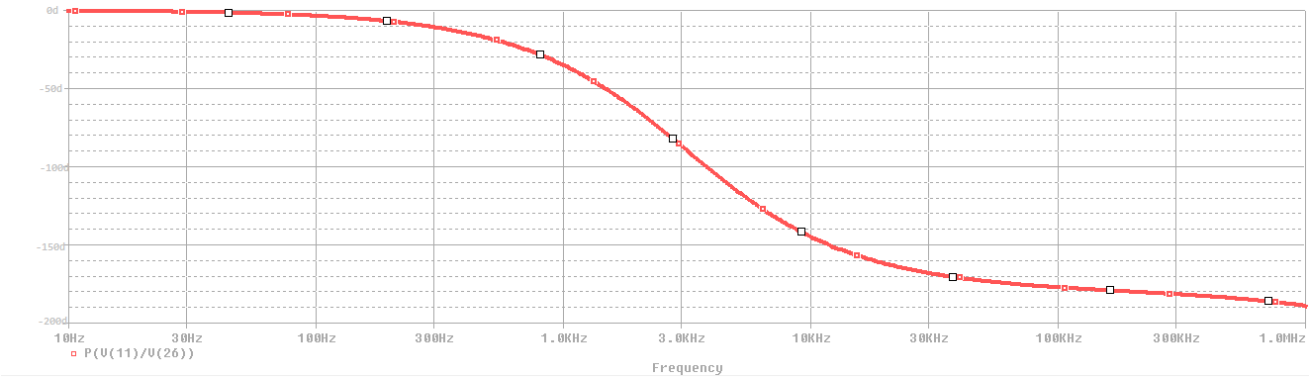


Fig.4.11. Phase response of Second order all pass filter using CDDOBA

## 4.3 Conclusion

This chapter covers the basic theory of Biquad filters. In this chapter implementation of voltage mode CDDOBA Biquad filter with IC AD844 have been proposed and simulated which verify the usability of CDDOBA in analog signal processing among the novel active building blocks.

## References


1. S. Özoğuz, A. Toker and C. Acar, "Current-mode continuous-time fully-integrated universal filter using CDBAs", *Electron. Lett.*, vol. 35, no. 2, p. 97, 1999.
2. A. Keskin, "Multi-function biquad using single CDBA", *Electr Eng*, vol. 88, no. 5, pp. 353-356, 2005.
3. S. Bashir and N. Shah, "Voltage Mode Universal Filter Using Current Differencing Buffered Amplifier as an Active Device", *CS*, vol. 03, no. 03, pp. 278-281, 2012.
4. C. Cakir, S. Minaei and O. Cicekoglu, "Low voltage low power CMOS current differencing buffered amplifier", *Analog Integrated Circuits and Signal Processing*, vol. 62, no. 2, pp. 237-244, 2009.
5. A. Keskin *, "Voltage-mode high-Q band-pass filters and oscillators employing single CDBA and minimum number of components", *International Journal of Electronics*, vol. 92, no. 8, pp. 479-487, 2005.

# CHAPTER 5

# EXPERIMENTAL RESULTS

## 5.1 Introduction

In the present chapter some of the experimental results which we have obtained using hardware implementation of CDDOBA are presented.

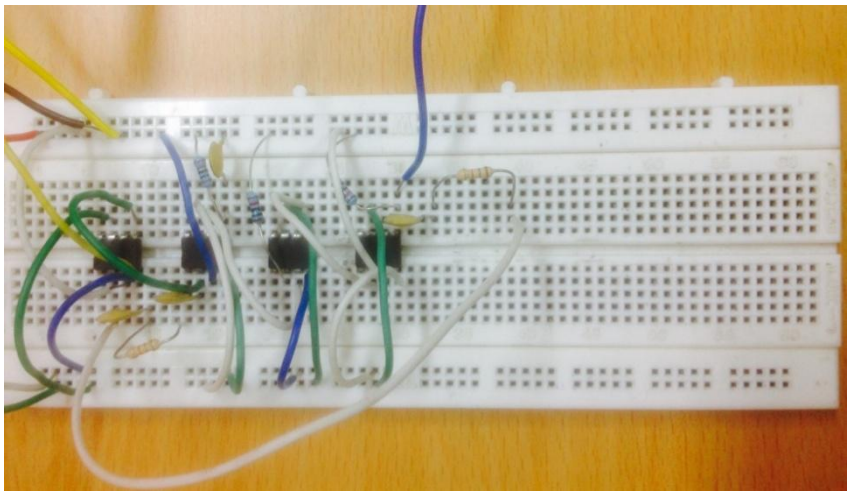

Fig.5.1. Hardware realisation of CDDOBA using IC AD844

## 5.2 First Order Low Pass Filter

Figure 5.2 shows the implementation of first order low pass filter using CDDOBA. It consist of CDDOBA circuit realized using commercially available IC AD844 and two resistors and one capacitor. The input-output relation is characterised as

$$\frac{V_o}{V_i} = -\frac{R_2}{R_1} \cdot \frac{1}{1+R_2Cs} \qquad (5.1)$$

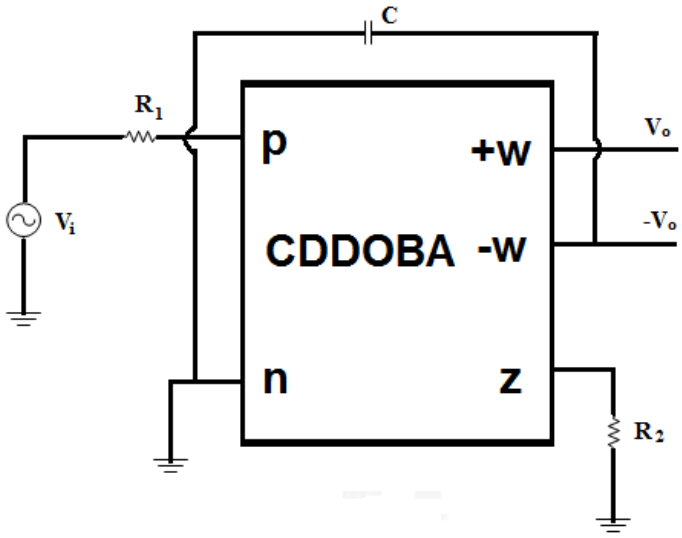


Fig.5.2. Implementation of first order LPF using CDDOBA

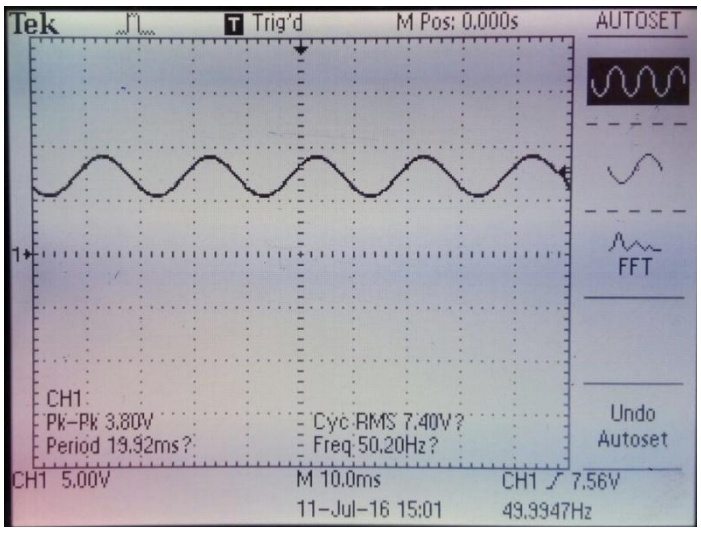


Fig.5.3 First order low pass filter output

**Experimental settings**

The bias supply voltages were taken as ±12V. The passive component values are $R_{w1}$= 10KΩ, $R_{x3}$= 10KΩ, $R_{w3}$= 10KΩ, $R_{z4}$=10KΩ, $R_{w4}$=10KΩ, $R_1$=8KΩ and C=100nF. To give a cut off frequency of 198.75 Hz input voltage applied is $1V_{pp}$.

The experimental results show that the cut off frequency is 180.6 Hz.

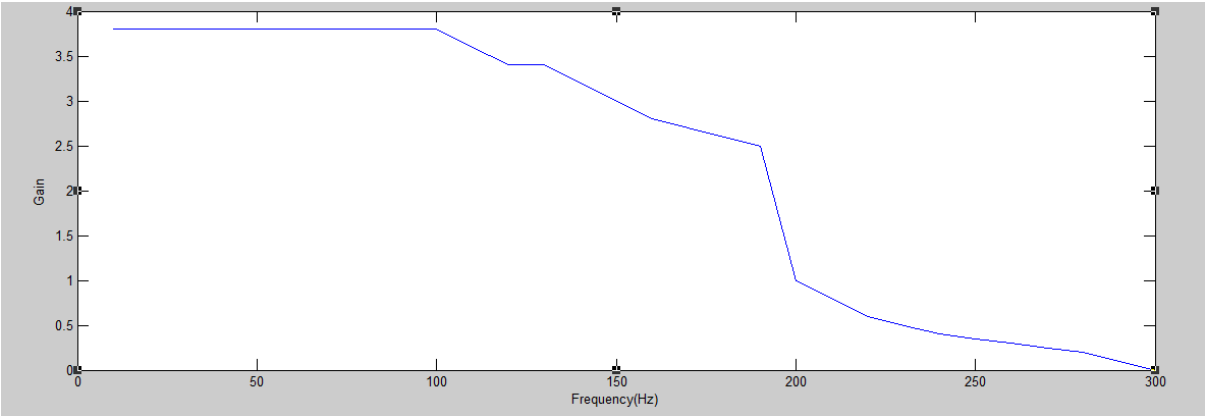


Fig.5.4.First Order Low pass filter plot

## 5.3 First Order High Pass Filter

Figure 5.5 shows the implementation of first order high pass filter using CDDOBA. It consist of CDDOBA circuit realized using commercially available IC AD844 and two resistors and one capacitor. The input-output characteristic is given as

$$\frac{V_o}{V_i} = -\frac{sCR_2}{1+R_1Cs} \tag{5.2}$$

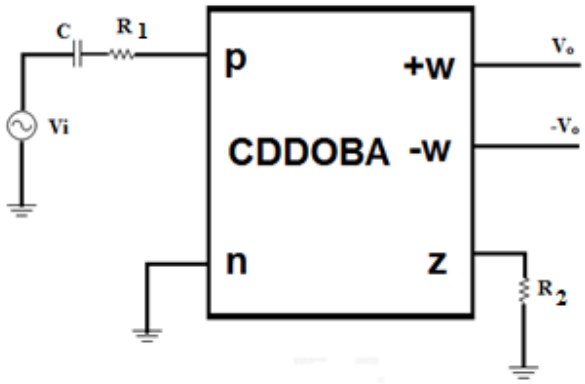


Fig.5.5 Implementation of first order HPF using CDDOBA

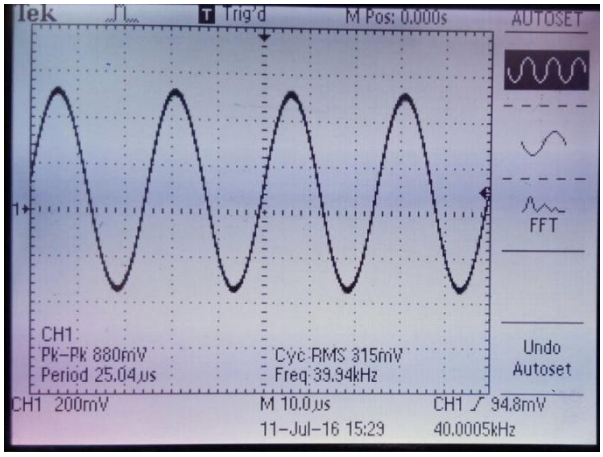


Fig.5.6 First order high pass filter output

**Experimental settings**

The bias supply voltages were taken as ±12V. The passive component values are $R_{w1}$= 10KΩ, $R_{x3}$= 10KΩ, $R_{w3}$= 10KΩ, $R_{z4}$=10KΩ, $R_{w4}$=10KΩ, $R_1$=10KΩ, $R_2$=1 KΩ and C=100nF. To give cut off frequency of 15.9 KHz input voltage applied is $1V_{pp}$.

The experimental results show the cut off frequency is 13.5 KHz.

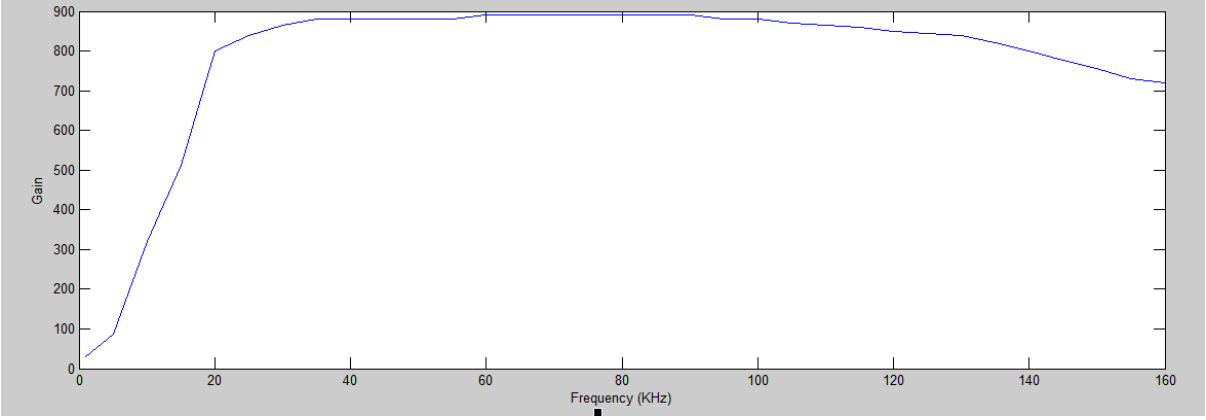


Fig.5.7. First Order High pass filter plot

## 5.4 Second Order Low Pass Filter

Figure 5.8 show the implementation of first order low pass filter using CDDOBA. Transfer function is

$$\frac{V_o}{V_i} = -\left(\frac{R_3}{R_1}\right).\frac{1}{s^2R_3C_3R_4C_4+(R_3C_3+R_4C_4-R_3C_4)s+1} \qquad (5.3)$$

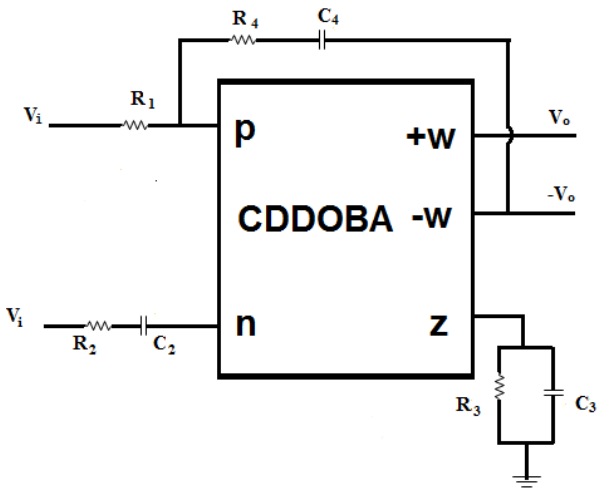


Fig.5.8 Implementation of second order LPF using CDDOBA

**Experimental settings**

The bias supply voltages were taken as ±12V. The passive component values are $Rw_1$=10KΩ, $R_{x3}$=10KΩ, $R_{w3}$=10KΩ, $R_{z4}$=10KΩ, $R_{w4}$=10KΩ, $R_1$=10KΩ, $R_2$=10KΩ, $R_3$=20KΩ, $R_4$=20KΩ, $C_2$=$C_4$=10nF and $C_3$=20nF. To give cut off frequency of 563.8 Hz input voltage applied is $1V_{pp}$.

Cut of frequency of low pass second order filter from experimental values is 500 Hz. Experimental result is as follow:

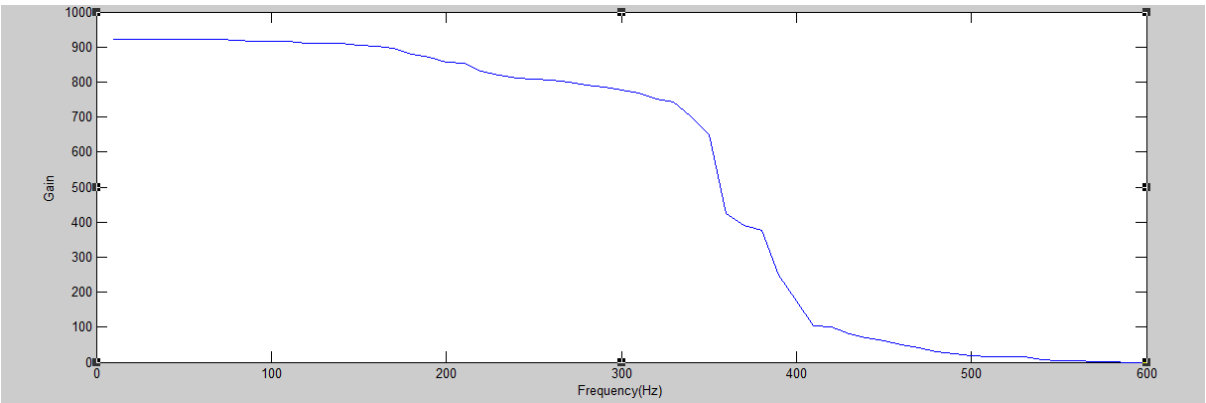


Fig.5.9. Second Order Low pass filter plot

## 5.5 Second Order High Pass Filter

Figure 5.10 show the implementation of second order high pass filter using CDDOBA. Transfer function is

$$\frac{V_o}{V_i} = -R_3 . \frac{s^2 . C_1 R_2 C_2}{s^2 R_3 C_3 R_4 C_4 + (R_3 C_3 + R_4 C_4 - R_3 C_4)s + 1} \qquad (5.4)$$

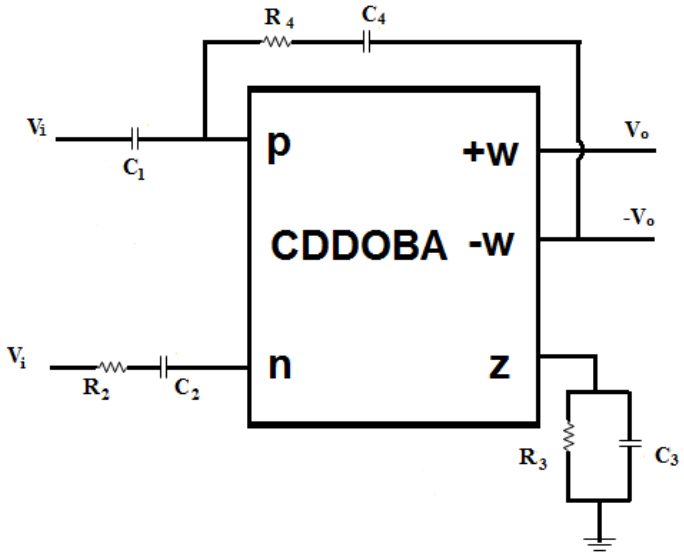


Fig.5.10 Implementation of second order HPF using CDDOBA

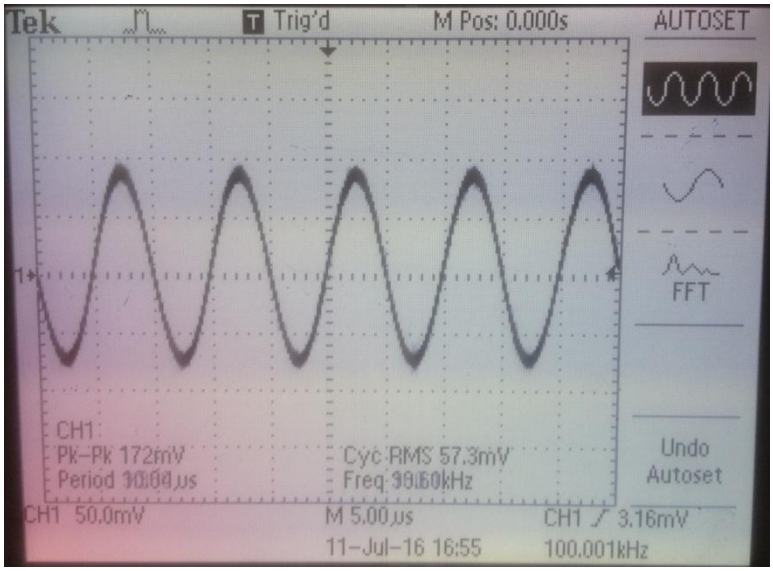


Fig.5.11Second order high pass filter output

**Experimental settings**

The bias supply voltages were taken as ±12V. The passive component values are $Rw_1$=10KΩ, $R_{x3}$=10KΩ, $R_{w3}$=10KΩ, $R_{z4}$=10KΩ, $R_{w4}$=10KΩ, $R_2$=1.8KΩ, $R_3$=1KΩ, $R_4$=1.8KΩ, $C_1$= 2nF $C_2$= 2nF $C_4$=2nF and $C_3$=2nF. To give cut off frequency of 59.255 KHz input voltage applied is $1V_{pp}$.

Cut of frequency of high pass second order filter is 55 KHz. Experimental result is as follow:

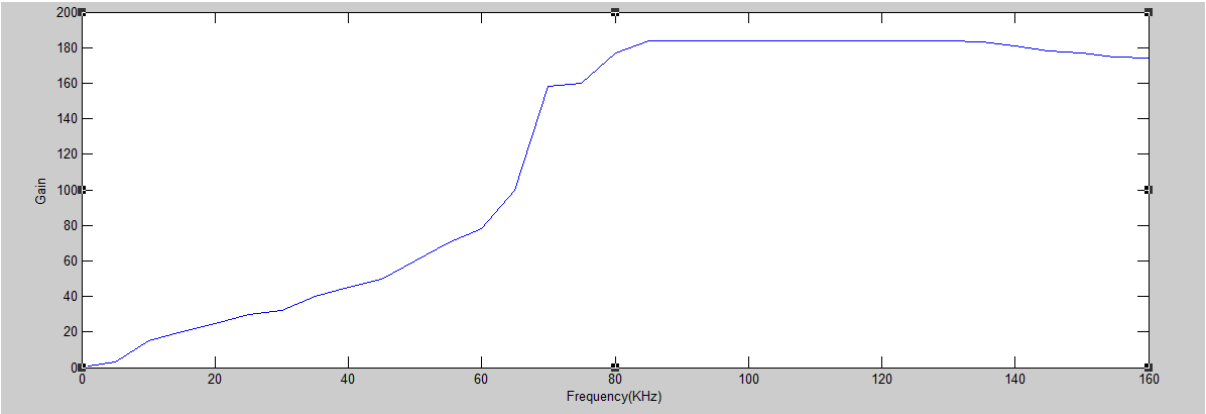


Fig.5.12 Second Order High pass filter plot

## 5.6 Conclusion

In present chapter some of the experimental results which we have obtained using the hardware implementation of CDDOBA has been presented. Experimental results for frequency responses are incorporated to verify the theory, which verify the usability of CDDOBA in analog signal processing among the novel active building blocks.

# CHAPTER 6

# SUMMARY AND SCOPE FOR FUTURE WORK

In the present work a new active current element current differencing differential output buffered amplifier (CDDOBA) and its applications in different signal processing circuits has been realized. CDDOBA is a versatile active component which can be used in both current and voltage mode applications. It can be used in place of conventional op amps in many applications and its current mode architecture results in much better ac performance and wider bandwidth.

A chapter wise summary of the project is as follows:

**Chapter 1** gives an overview of signal processing, compares current mode and voltage mode signal processing. This chapter gives a brief introduction of active building block CDDOBA. It also includes the general outline of the thesis.

**Chapter 2** briefly describes about the significance of current mode circuits and the various active blocks that are introduced after Current Conveyors. Particular emphasis has been put on those works which have been presented during the last one decade.

**Chapter 3** of the dissertation gives a bipolar architecture of CDDOBA and its building blocks. At the end of chapter simulation results for some applications of CDDOBA is presented.

**Chapter 4** describes implementation of universal filter application using CDDOBA, followed by PSPICE simulation results.

**Chapter 5** describe the hardware implementation CDDOBA filter applications.

**Chapter 6** finally Summary and scope of future work in this area are outlined.

**Scope of future work:** The work presented in thesis has concentrated mainly on active building block introduced in the domain of analog signal processing and special emphasis has been put on current mode active building block current differencing differential output buffered amplifier (CDDOBA) and its applications. This work can be extended to use of CDDOBA as active building block for more applications like voltage based multivibrators, analog multiplier etc. Thus there is ample scope for extending this work in future.

# APPENDIX

## PSpice model file used for process. AD844 SPICE Macro-model

```
* Node assignments
*               non-inverting input
*               | inverting input
*               | | positive supply
*               | | | negative supply
*               | | | | output
*               | | | | | compensation node
*               | | | | | |
.SUBCKT AD844  1 2 99 50 28 12
*
* INPUT STAGE
*
R1   99  8     1E3
R2   10 50     1E3
V1   99  9     11
D1   9   8     DX
V2   11 50     11
D2   10 11     DX
I1   99  5     258E-6
I2   4  50     258E-6
Q1   50  3  5  QP
Q2   99  3  4  QN
Q3   8   6 30  QN
Q4   10  7 30  QP
R3   5   6     300E3
R4   4   7     300E3
*C1   99  6     8.8E-15
*C2   50  7     8.8E-15
*
* INPUT ERROR SOURCES
*
GB1  99  1     POLY(1)  1  22  150E-9  90E-9
GB2  99 30     POLY(1)  1  22  200E-9  90E-9
VOS  3   1     50E-6
LS1  30  2     1E-8
CS1  99  2     1E-12
CS2  50  2     1E-12
*
EREF 97  0     22  0  1
```

```
*
* GAIN STAGE & DOMINANT POLE
*
R5   12 97     3E6
C3   12 97     5.5E-12
G1   97 12     99  8  1E-3
G2   12 97     10 50  1E-3
V3   99 13     4.3
V4   14 50     4.3
D3   12 13     DX
D4   14 12     DX
*
* POLE AT 70 MHZ
*
R8  17 97     1E6
C4  17 97     3.18E-15
G4  97 17     12 22  1E-6
*
* POLE AT 300 MHZ
*
R12 21 97     1E6
C8  21 97     0.318E-15
G8  97 21     17 22  1E-6
*
* OUTPUT STAGE
*
ISY 99 50     5.1E-3
R13 22 99     16.7E3
R14 22 50     16.7E3
R15 27 99     30
R16 27 50     30
L2  27 28     6E-8
G9  25 50     21 27  33.33E-3
G10 26 50     27 21  33.33E-3
G11 27 99     99 21  33.33E-3
G12 50 27     21 50  33.33E-3
V5  23 27     0.5
V6  27 24     0.5
D5  21 23     DX
D6  24 21     DX
D7  99 25     DX
D8  99 26     DX
D9  50 25     DY
D10 50 26     DY
```

```
*
* MODELS USED
*
.MODEL QN   NPN(BF=1E9 IS=1E-15)
.MODEL QP   PNP(BF=1E9 IS=1E-15)
.MODEL DX   D(IS=1E-15)
.MODEL DY   D(IS=1E-15 BV=50)
.ENDS AD844
*$
```