ANALYSIS, DESIGN AND CONTROL OF DSTATCOM AND ITS APPLICATIONS

by

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CERTIFICATE

This is to certify that the thesis entitled "**Analysis, Design and Control of DSTATCOM and its Applications**" being submitted by **Mr. Manoj Badoni** for the award of degree of Doctor of Philosophy in the Department of Electrical Engineering, Delhi Technological University, Delhi, is the record of student's own work carried out by him under our supervision. The contents of this research work have not been submitted in part or full to any other university or institute for award of any degree.

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ABSTRACT

The widespread use of power electronics based equipment is increasing these days. Poor power quality at power distribution level is attributed to a number of reasons and the increase in power electronics based loads is one of the major causes. These loads are nonlinear in nature and generate harmonic currents which propagate to other connected loads at the point of common coupling (PCC). Some other power quality problems viz. high reactive power demand, voltage regulation, load unbalancing and poor power factor cause concern to the electric utility and consumers of electric power supply. The current related power quality problems include harmonic currents, high reactive power burden, poor voltage regulation and unbalanced loads.

A number of power converter based solutions have been developed in the recent past due to the progress in speed and capacity of power semiconductor technology. The group of devices used for power quality improvement in distribution systems is referred to as custom power devices. A specific shunt connected custom power device used for the mitigation of current related power quality problems is widely known as a distribution static compensator (DSTATCOM). An implementation and control of DSTATCOM have become possible due to advancement in digital signal processing (DSP) and self-commutating semiconductor devices. The major components used for design of DSTATCOM include voltage source converter (VSC), interfacing inductors, ripple filters and DSP (Digital Signal Processor).

Performance of DSTATCOM mainly depends on the control algorithm used for the estimation of fundamental active and reactive components of reference currents. These reference currents are used for the generation of switching pulses for control of VSC used in DSTATCOM. The control algorithms for DSTATCOM have been divided into four categories in this proposed work. These

include the conventional control algorithms, adaptive theory based control algorithms, recursive theory based control algorithms and artificial intelligence based control algorithms.

The conventional control algorithms considered are based on power balance theory (PBT), instantaneous reactive power theory (IRPT), conductance based and instantaneous symmetrical component theory (ISCT). These control algorithms for the control of three-phase DSTATCOM, are used for harmonic currents reduction, reactive power compensation and load balancing in power factor correction (PFC) and voltage regulation modes. These algorithms are extended for voltage regulation operation, which are also required in various isolated power generation systems such as an isolated diesel generator, isolated micro hydro, biogas and biomass based generation systems.

The control algorithms developed under adaptive theory are based on Wiener filter, fixed step size least mean square (FSSLMS) along with its variants and variable step size least mean square (VSSLMS). The control algorithms developed under the category of recursive theory are based on variable forgetting factor recursive least square (VFFRLS), recursive inverse (RI) and immune feedback principle. The category of artificial intelligence based algorithms includes adaptive neuro fuzzy inference system (ANFIS), real time recurrent learning (RTRL) and immune feedback based control algorithms.

All these control algorithms are developed in MATLAB using SIMULINK and Sim-power system (SPS) tool boxes. Real time performance of these control algorithms for power quality improvement has been extensively tested using simulation studies and experimentally on the prototype of DSTATCOM developed in the laboratory.

Additionally, the three phase DSTATCOM system is utilized for grid integration of solar photovoltaic (SPV) array. The VSC used in this system serves the purpose of power converter, which is used to transfer power generated from SPV array to the grid along with functions of power quality improvement such as harmonic currents elimination, reactive power compensation and load balancing in PFC and voltage regulation modes under linear and nonlinear loads. The performance of this system is studied with three control algorithms viz. synchronous reference frame theory (SRFT), Wiener filter and recursive inverse based control algorithms.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF SYMBOLS

v_{sa}, v_{sb}, v_{sc}	Phase-a, b, c PCC voltages
i_{sa}, i_{sb}, i_{sc}	Phase-a, b, c supply currents
i_{la}, i_{lb}, i_{lc}	Phase-a, b, c load currents
i_{Ca}, i_{Cb}, i_{Cc}	Phase-a, b, c compensator currents
R_s and L_s	Source impedance
C_{dc}	DC bus capacitance
V_{dc}	DC bus voltage
L_f	Interfacing inductance
R_f and C_f	Ripple filter
u_{pa}, u_{pb}, u_{pc}	Unit inphase templates
u_{qa}, u_{qb}, u_{qc}	Unit quadrature templates
V_t	Amplitude of PCC voltage
P_{dx}	Cross-correlation vector
R_x	Correlation matrix of input data
μ	Step size parameter
w_{ap}, w_{bp}, w_{cp}	Fundamental active power weights of phase a, b ,c of load currents
w_{ap}, w_{bp}, w_{cp}	Fundamental reactive power weights of phase a, b ,c of load currents
k	Kalman gain
λ	Forgetting factor
η	Weight learning parameter
γ	Stabilization factor
α	Momentum

μ_{a1}, μ_{a2}, μ_{a3}	Fuzzy membership functions
ω and g	Network parametric weights
S, S_1 and S_2	Total set of parameters, set of premise parameters and set of consequent parameters

CHAPTER-I
INTRODUCTION

1.1 GENERAL

Power quality problems in electric distribution systems have increased tremendously. The main concern of electricity consumer is the uninterruptable power supply with improved power quality. There are sensitive loads such as hospitals and processing plants that require clean and uninterruptable electric power supply [1]. A voltage dip of short duration in processing plant can extensively damage a batch of product, which cost them significant amount of money [2-5]. Substantial increase in nonlinear loads such as converters, switch mode power supplies (SMPS), electric arc furnaces, computers and house hold electronic equipment installed at the distribution level plays a major cause in distorting the sinusoidal waveform of supply voltages and currents. The power quality problems are expressed in terms of deviation in voltage, current and frequency, which causes failure of consumer equipment [6-11]. The power quality problems are related to voltage at point of common coupling (PCC) and current drawn from AC mains. The power quality problems related to voltage at PCC are voltage sag/swell, interruption, harmonic, notching and flickers [12-20]. The power quality problems related to current are harmonics, reactive power, excessive neutral current and unbalanced currents which are affecting performance of electric distribution system [21-29]. The mitigation of harmonics and other power quality issues along with the supply of reliable quality power to consumers is an important task of utilities. Various types of power filters have been developed such as passive, active and hybrid in series, shunt or combination of both for mitigation of power quality problems [30-50]. Custom power devices, which use power electronic based controllers for distribution systems can enhance the quality and reliability of power delivered by electric distribution system. These devices can be shunt connected, series connected or a combination of both series and shunt

connected at PCC [51-84]. A number of international standards are developed by various organizations such IEEE (Institute of Electrical and Electronics Engineers) and IEC (International Electrotechnical Commission) to specify the permissible limit of power quality problems and to provide guidelines for the end user, manufacturer and utility to improve the quality of power [85-91]. The critical and sensitive loads are protected from power quality problems by monitoring these power quality events. The objectives of power quality monitoring are prediction of performance of the load and the selection of power quality mitigation system [92-97].

The acceptable solution for current related power quality problems at distribution level is an active shunt compensator which is also commonly named as the distribution static compensator (DSTATCOM) [98-99]. The DSTATCOM is used for mitigation of current related power quality problems such as harmonics distortion, poor power factor, load unbalancing and voltage regulation in unity power factor (UPF) and voltage regulation modes. Tremendous progress in the field of power semiconductor devices and signal processing has been made the implementation of DSTATCOM as cost effective [100-102]. The research in this area has led to developments in the area of different configurations and control algorithms for control of the shunt compensator. The DSTATCOM is configured based on the number of switching devices, the use of isolation transformer and the use of type of transformer for neutral current compensation. Mainly DSTATCOM configurations are divided into two major categories such as three phase three wire and three phase four wire [103-105]. The capability of DSTATCOM to mitigate current related power quality issues enables it to be utilized in small hydro power generation, air-craft power system and electric ship supply system.

1.2 STATE OF ART

Substantial literature has been reported on the shunt compensators and their control techniques for power quality improvements at distribution level. Shunt compensation provides several power quality improvement features such as harmonics elimination, reactive power compensation, load balancing and PCC voltage regulation [106-109]. The building block of DSTATCOM is insulated gate bipolar transistors (IGBTs) based voltage source converter (VSC) [110]. Different configurations of DSTATCOM are possible which include three-leg, four-leg and six-leg VSCs [111-112]. The internal control of DSTATCOM is a prerequisite to generate gating pulses of its VSC and to achieve desired performance in steady state as well as dynamic load conditions.

The effectiveness of DSTATCOM depends upon the type of control algorithm used for estimation of fundamental component of load currents. The fundamental real and reactive components of load currents are further utilized to estimate reference supply currents, which are used for the generation of switching pulses for voltage source converter (VSC) used as DSTATCOM. Practical implementation of DSTATCOM becomes feasible due to advancement in power electronics devices, DSPs (Digital Signal Processors) and sensors [113-120]. Fast and accurate control algorithms need to be developed for DSTATCOM which can also be realized experimentally. Different techniques for extracting harmonics from distorted load current have been suggested by various authors. The control algorithm should have fast response and stable operation in both steady state and dynamic load conditions. The selection of a control algorithm depends upon processing time, mathematical complexity, fast response, stable operation and easy implementation. Based on the operating principle and mathematical formulation control algorithms can be divided into four parts such as conventional control algorithms [121-142],

adaptive theory based control algorithms [143-161], recursive theory based control algorithms [162-176] and artificial intelligence based control algorithms [177-193]. The VSC in DSTATCOM is used as power converter to transfer power generated from solar photovoltaic array to the grid. The functions of DSTATCOM such as harmonics elimination, reactive power compensation and load balancing in UPF and voltage regulation modes are also utilized by the grid connected SPV system [194-206].

Some conventional control algorithms reported in the literature are based on power balance theory, instantaneous reactive power theory, admittance based control and instantaneous symmetrical component theory. The conventional control algorithms are already reported in the literature and mostly used for power factor correction (PFC) operation. However, the application of conventional control algorithms can be extended for voltage regulation in various isolated power generation system such as isolated diesel generator, isolated micro-hydro, biogas and biomass systems [121-142]. Adaptive control has also been recognized as a powerful control technique for extracting fundamental reference currents from the distorted load currents. This provides a systematic approach for automatic adjustment of controllers in real time in order to achieve desired performance. The Wiener filter based control algorithm has been found suitable in terms of complexity and less computational burden. Adaptive least mean square (LMS) based control algorithms with fixed step and variable step are reported in the literature, where variable step LMS has been found to have advantages in terms of fast convergence and less steady state error [143-161].

Recursive theory based control algorithms can also be used to the control the DSTATCOM. These algorithms perform well even in distorted environment under steady state and dynamic load conditions. Recursive theory based algorithms include recursive least square (RLS) theory,

and recursive inverse theory etc. RLS based control algorithm offers faster convergence, but it is computationally demanding. However, recursive inverse based control algorithm offers less computational complexity with moderate convergence. Recently some publications have proposed the application of immune feedback based control algorithm for control of single phase inverter and three phase inverter, where dead time elimination and space vector PWM control have been used. Variants of recursive algorithms have been used for the control of the shunt compensator [162-176].

Exhaustive literature has been reported on the use of artificial intelligence based control algorithms for control of DSTATCOM over the past two decades. These control techniques are based on artificial neural network (ANN), fuzzy logic and adaptive neuro fuzzy inference system (ANFIS). Some of the publications refer to the use of these techniques for control of DC bus voltage and AC bus voltage regulation while in others these control algorithms have been used for estimation of fundamental active and reactive power components of load currents. The recurrent neural network (RNN) has been found suitable for real time applications, because it does not retain the information about large number of previous training data. Several gradient based techniques are used for training RNN such as back propagation through time (BPTT), recurrent back propagation (RBP), and real time recurrent learning (RTRL) [177-193]. In some cases, artificial intelligence based techniques such as ANFIS can be used to obtain step size parameter of adaptive LMS based control techniques. The step size parameter for LMS techniques learns fast and improves its steady state as well as dynamic performances.

1.3 CUSTOM POWER DEVICES

The power quality problems at distribution system arise due to harmonics, low power factor, poor voltage regulation, load unbalancing and excessive neutral current. The custom power

devices are used to mitigate above mentioned power quality problems at the distribution system. The custom power devices are used to enhance the quality and reliability of power that is delivered to consumer. These devices can be connected in shunt, series or in combination of both. The custom power devices used at the distribution system include DSTATCOM, dynamic voltage restorer (DVR) and combination of both DSTATCOM and DVR known as unified power quality conditioner (UPQC), which are used for mitigation of current and voltage related power quality problems. The shunt connected device such as DSTATCOM is used for compensation of current related power quality problems with self-supported DC bus voltage. The main components of DSTATCOM are power converter such as VSC, voltage/ current sensors, signal processing devices, interfacing inductors and ripple filters. The DSTATCOM has capability of mitigating power quality problems such as harmonics, poor power factor and load unbalancing in PFC and voltage regulation modes.

1.4 SCOPE OF THE WORK

Based on the exhaustive literature review of the design and development of the shunt compensator and its control techniques, it has been identified that there are some major issues in the development of control algorithms which are needed to be resolved. These issues include the speed of response, convergence, computational burden, complexity, static error, robustness and stable operation in steady state and dynamic conditions.

The main objectives of the proposed research work are to design and develop a three-phase shunt compensator, to implement some new control algorithms for this configuration and to investigate some of the applications of DSTATCOM in grid integration of renewable energy sources such as solar photovoltaic (SPV) systems. The detailed description of the proposed work is as follows.

1.4.1 Investigations on Three Phase DSTATCOM

The design and rating selection of three-phase, three-leg DSTATCOM depend on the required power quality features it is expected to mitigate. Depending on the reactive power compensation required along with harmonics elimination and load balancing, the design of DSTATCOM is carried out in detail. The power circuit components of the DSTATCOM are insulated gate bipolar transistors (IGBTs) based VSC, DC bus capacitor, interfacing inductors, ripple filters, linear and nonlinear loads and supply system need to be designed properly. The control of the DSTATCOM can be implemented on DSP. The appropriate sensor circuits are required for sensing the signals (load currents, supply currents DC bus voltage and PCC voltages) in a developed prototype of DSTATCOM. These sensed signals are made available to the control algorithms through ADC channels of DSP. The generated switching signals from the DSP are used to drive gating circuit of three phase VSC used as DSTATCOM and to achieve the desired control.

1.4.2 Classifications of Control Algorithms for DSTATCOM

The proposed control algorithms are divided into four major sub-categories which include conventional control algorithms, adaptive theory based control algorithms, recursive theory based control algorithms and artificial intelligence based control algorithms. The detailed descriptions of these algorithms are as follows.

1.4.2.1 Conventional Control Algorithms for DSTATCOM

The control algorithms investigated under this category are based on power balance theory, instantaneous reactive power theory, conductance based Fryze theory and instantaneous symmetrical component theory. The performance of these control algorithms is tested through

simulation and implementation on the prototype developed in the laboratory. The system performance is studied in power factor correction (PFC) and voltage regulation modes under linear and nonlinear loads. These algorithms have already been developed in the literature for PFC operation. In the proposed research work, these algorithms are also extended for voltage mode. The voltage regulation is required in various isolated power generation systems such as isolated diesel generator, isolated micro-hydro, biogas and biomass based systems. It is also required in distributed generation system, when the system is operating in islanding mode. The conventional algorithms are developed and tested on the developed DSTATCOM system in the laboratory. The performance of these algorithms are also compared with the proposed control algorithms presented in the following sections.

1.4.2.2 Adaptive Theory Based Control Algorithms for DSTATCOM

The control algorithms investigated under this category include Wiener filter, fixed step size least mean square (FSSLMS), variable step size least mean square (VSSLMS). Different variations of VSSLMS are studied, tested and compared to control DSTATCOM. The performance of these control algorithms is verified using MATLAB based Simulink models which are also implemented experimentally in PFC and voltage regulation modes of DSTATCOM under nonlinear loads.

1.4.2.3 Recursive Theory Based Control Algorithms for DSTATCOM

The control algorithms investigated under this category are based on recursive theory and include algorithms such as variable forgetting factor recursive least mean square (VFFRLS), variable forgetting factor based recursive inverse (VFFRI) and immune feedback principle for the control of three phase DSTATCOM. These algorithms are tested through simulation and

implementation in PFC and voltage regulation modes of DSTATCOM under linear and nonlinear loads.

1.4.2.4 Artificial Intelligence Based Control Algorithms for DSTATCOM

The control algorithms investigated under this category are based on principle of human intelligence to achieve a specific task for which they are designed. These control techniques have the capability of learning, self-organizing or self-adapting. The control algorithms developed under this category are based on adaptive neuro fuzzy inference system (ANFIS), real time recurrent learning (RTRL) and adaptive neuro fuzzy inference system least mean square (ANFIS-LMS) for the control of three phase DSTATCOM. The performances of these algorithms are studied using simulation results and test results in PFC and voltage regulation modes under balanced/unbalanced linear and nonlinear loads.

1.4.3 DSTATCOM Application to Grid Integration of Solar Photovoltaic (SPV) Array System

The DSTATCOM provides load compensation and solves several power quality problems such as power factor correction, meeting the reactive power demand and providing voltage regulation. It provides reactive power compensation in grid connected SPV systems. The transfer of real power into the grid is also possible, if a source of real power is connected at the DC bus of the VSC. Solar photovoltaic array has been designed, simulated and analyzed for real power transfer along with power quality improvement at the distribution system.

1.5 OUTLINE OF CHAPTERS

The content of the thesis have been divided into following chapters.

Chapter-I: This chapter presents several power quality issues and solutions using custom power devices. The scope of work includes investigation on three phase DSTATCOM and classification

of control algorithms for improving power quality problems such as harmonics, reactive power and load unbalancing. These algorithms are divided into four sub-groups such as conventional control algorithms, adaptive theory based control algorithms, recursive theory based control algorithms and artificial intelligence based control algorithms.

Chapter-II: This chapter includes the literature review on quality problems and their solutions. Exhaustive literature survey on the configurations and control algorithms for the shunt compensator is given in this chapter. Based on the exhaustive literature review, identified research areas are presented at the end of this chapter.

Chapter-III: This chapter presents system configuration of three phase DSTATCOM. The design and selection of various component of DSTATCOM such as VSC, DC bus voltage, DC bus capacitance, interfacing inductors and ripple filter are given in detail. The design of voltage sensor circuits, current sensor circuits, gating circuits for generation of pulses for three phase VSC are discussed in this chapter. The designs of interfacing inductors used for the laboratory prototype of DSTATCOM are presented in this chapter.

Chapter-IV: This chapter includes the need of controller and classification of different algorithms for the control of DSTATCOM. Mathematical formulation, MATLAB based modeling and DSP based implementation of conventional control algorithms are presented here. Simulation and test results of conventional control algorithms are also given. These test results are studied based on MATLAB simulation models and verified experimentally on the developed DSTATCOM prototype for a variety of loading conditions.

Chapter-V: This chapter presents mathematical formulation, MATLAB based modeling and DSP based implementation of adaptive theory based control algorithms for DSTATCOM. Performance of adaptive theory based control algorithm is presented using simulation as well as

experimental results obtained on a developed prototype of DSTATCOM. Control algorithms investigated in this category include Wiener filter, fixed step size least mean square (FSSLMS), variable step size least mean square (VSSLMS) and its variations for the control of DSTATCOM.

Chapter-VI: This chapter deals with the mathematical formulation, MATLAB based modeling and DSP based implementation of recursive theory based control algorithms for DSTATCOM. The control algorithms such as VFFRLS, VFFRI and immune feedback based algorithms for control of three-phase DSTATCOM have been developed and verified using simulation and test results.

Chapter-VII: This chapter includes the mathematical formulation, MATLAB based modeling and DSP based implementation of artificial intelligence based control algorithms for control of DSTATCOM. The algorithms developed under this category are based on ANFIS, RTRL and ANFIS-LMS for the control of three-phase VSC used as DSTATCOM. The simulation results are obtained using MATLAB based simulation. The performance of these algorithms are verified experimentally on the developed prototype of the DSTATCOM.

Chapter-VIII: This chapter presents design and simulation of a solar photovoltaic (SPV) array fed grid in balanced generating system. This system includes SPV array, a DC-DC boost converter and a VSC for seamless transfer of generated solar power along with all the features of DSTATCOM such as harmonics elimination, reactive power compensation and load balancing in PFC and voltage regulation modes.

Chapter-IX: This chapter summarizes performance of different control algorithms presented for DSTATCOM and highlights the main conclusions of the proposed work. The scope of further work in this area is also enlisted at the end of this chapter.

CHAPTER-II
LITERATURE REVIEW

2.1 GENERAL

In the previous chapters, various power quality problems, mitigation techniques using custom power devices are presented. The scope of the work is discussed, which includes investigation of control algorithms for DSTATCOM and its application in grid connected solar photovoltaic system. This chapter deals with the literature review related to power quality mitigation techniques using active shunt compensator, power quality standards and identified control algorithms. The solutions to power quality problems and configurations of active shunt compensator are reviewed. The control algorithms for DSTATCOM presented in the literature is investigated. The control algorithms are investigated and categorized into conventional controls, adaptive theory based controls, recursive theory based controls and artificial intelligence based controls. The applications of DSTATCOM and control algorithms are investigated in integration of renewable energy sources such as solar photovoltaic system to the utility grid. The identified research areas such as control algorithms, which are fast, robust and work well in distorted environment are discussed along with the application of DSTATCOM to grid integration of solar photovoltaic system at the end of chapter.

2.2 LITERATURE SURVEY ON POWER QUALITY PROBLEMS AND THEIR SOLUTIONS

The problems related to power quality are reviewed here. There are several power quality problems related to voltage and currents, such as voltage sag, voltage swell, notches, harmonics, reactive power and load unbalancing. The power quality problems and their solutions are reviewed and given as follows.

2.2.1 Power Quality Problems [1-29]

The injection of harmonics at power distribution level is a cause of major concern to power system engineers. The reasons are mainly due to increase in the power electronics loads, which cause supply current and voltage to become non-sinusoidal [1]. The power electronics based loads are realized using solid state converters. Nonlinear loads are usually classified as harmonics current sources and voltage sources. Some of the harmonic producing loads include converters, switch mode power supplies (SMPS), electric arc furnaces, inverters and personal computers [2-3]. The others advantages of solid state converters are the decrease in the losses, an increase overall efficiency and increasing production [4-8]. The consequence of this is more penetration of nonlinear loads, which increase harmonic level, distortions and notches in the system. The use of renewable energy sources such as solar photovoltaic (SPV) in the distributed generation has increased power quality issues. These sources require solid state converters and there is variation in input power, which causes current and voltage related power quality problems occur at PCC [9-11].

Three phase converters, which are used to convert DC to AC require commutation of the AC from one phase to another. During this period, there is a momentary short circuit between the two phases, which cause periodic voltage disturbance called notching [12]. This appears due to source impedance and isolating inductance between the converter and the point being mentioned, which causes extra burden on the insulation of electrical equipment [13]. Due to loads with solid state rectifiers, arcing equipment and switching power supplies noise can occur in the power system. This problem can be worse by improper grounding. Noise disturbed various electronics equipment [14-16].

There is not only the problem of harmonics, but also other power quality problems such as reactive power, excessive neutral current, load unbalancing and unregulated voltage [17-18]. An increase demand of reactive power by load reduces the supply power factor. This effect causes low power factor is overloading the power cables and equipment failure. The load unbalancing is due to removal of a phase load, can increase or the decrease of current in any phase. The unbalanced load draws unbalanced currents from utility [19-20].

The disturbances in supply voltages are due to short duration voltage variations and long duration voltage variations. The short duration voltage variations are voltage sag, voltage swell and an interruption [21-25]. Voltage sag is basically decrease in r.m.s. voltage at the power frequency ranging from half cycle to a minute, voltage swell is an increase in voltage upto a level 1.1 to 1.8PU in r.m.s. voltage at power frequency ranging from half cycle to a minute and an interruption occurs when the supply voltage decrease to less than 0.1PU for a period of time not exceeding one minute. Long duration voltage variations are under voltage and overvoltage. These are defined as less than 90% and greater than 110% for the period longer than one minute respectively. The under voltage is due to switching on large load or switching off a large capacitor bank. The overvoltage is due to switching off large load or energizing a capacitor bank. These voltage variations have significant impact on domestic and industrial consumers. The process chain can stop even due to small duration of voltage interruption, which causes huge production can be wasted [26-29].

2.2.2 Power Quality Solutions [30-84]

Passive filters such as tuned L-C circuits have been used to compensate harmonics in the past. The various configurations for passive filters are such as single tuned, double tuned, triple tuned,

quadruple tuned, damped and automatically tuned. The other configurations of passive filters are passive series filter, passive shunt filter and combination of both. The passive series filters are used to prevent a particular harmonic component from voltage fed type loads by offering large impedance to that frequency component. The passive shunt filters are used to mitigate the harmonic current and partially to meet reactive power requirement of current fed type loads. Combining both series and shunt passive filters called hybrid passive filters. The hybrid passive filters can eliminate voltage and current harmonics. It can balance and also regulate the terminal voltages. Although the passive filters have low initial cost and are efficient, yet they suffer from problems of bulky size, higher space requirements, detuning with age and possibility of resonance with load or system impedance [30-39].

Power converters based solutions have now been developed especially due to progress in speed and capacity of power semiconductor technology in power electronics [40]. High speed and higher capacity power converters are employed for mitigating power quality related problems such as power factor correction, harmonics compensation, voltage sag/swell, voltage flicker and unbalanced/fluctuating loads [41-45]. The devices which can mitigate these power quality problems are custom power devices such as active power filters (APFs) [46-50]. The topologies of these devices existed are series, shunt or combination of both.

An active series compensator is used mitigate voltage related power quality problems such as harmonics, voltage sag, voltage swell, flickers, voltage fluctuations and imbalance [51]. Theses power quality problems increase losses in the system and stop functioning of sensitive loads causes loss of production [52-53]. An active series compensator is connected in series with the AC mains using a matching transformer used to inject the voltage of required magnitude and frequency and to restore the voltage across the loads to protect the sensitive loads and reduces

the losses in the system. It is also useful to damp out harmonics propagation caused by resonance between the line impedance and passive shunt compensator [54-56]. These compensators are known as solid state series compensators (SSCs) and dynamic voltage restorers (DVRs) [57-58]. The IGBTs (Insulated Gate Bipolar Transistors) based voltage source converters (VSC) is used in these compensator to inject equal and opposite voltage of disturbance in series with AC mains to provide clean and regulated voltage.

The shunt APFs are applicable for current related power quality problems and sometimes known as distribution static compensator (DSTATCOM) [59-64]. The DSTATCOM is used to mitigate current related power quality problems such as power factor correction (PFC), harmonics compensation, load unbalancing and voltage regulation [65-67]. The major factors in advancing the shunt compensator are the introduction of fast solid state devices. In the initial stage, bipolar junction transistors (BJTs) and power metal oxide semiconductor field effect transistors (MOSFETs) and gate turn off thyristor (GTOs) have been used to develop shunt compensator. The introduction of IGBTs has boosted up DSTATCOM technology and considered ideal solid state device for it [68-72].

The improvement in the sensor technology such as Hall effect voltage and current sensors with accurate sensing, vast variety, reasonable cost and easy availability has contributed to enhance the performance of shunt compensator [73-74]. The advancement in the technology of signal processing, starting from the use of discrete analog and digital computers, microprocessors, microcontrollers and DSPs (Digital Signal Processors) has also contributed in enhancing the performance of DSTATCOM. Tremendous development in DSP technology has made possible to implement fast and complex control algorithms for control of VSC used in DSTATCOM [75-78].

Combining active series and active shunt compensators can compensate for both voltage and current related power quality problems. A custom power device known as unified power quality conditioner (UPQC) is combination of both series and shunt compensators [79-80]. This consists of two voltage source converters joint back to back with common DC bus capacitor. The shunt device for UPQC known as DSTATCOM used to compensate for current related power quality problems such as harmonics elimination, reactive power compensation and load balancing. The series connected device of UPQC is known as DVR used to compensate for voltage harmonics, sag, swell, flickers, notches and voltage unbalancing [81-84].

2.3 POWER QUALITY STANDARDS [85-91]

The quality of power affects end user in many ways such as equipment failure, power loss and loss of production. A number of power quality standards have been developed by various organizations, to maintain an acceptable level of power quality at utility level [85]. The various aspects of power quality such as permissible level of deviations, mitigation and monitoring are defined in these standards. Several power quality standards are defined by IEEE (The Institute of Electrical and Electronics Engineers) and IEC (The International Electrotechnical Commission). An IEEE-519-1992standard [86], is recommended practice and the requirement for harmonic control at distribution level. The guidelines for the design of electric power system with nonlinear loads are provided and the limits are set for steady state and dynamic load conditions. This standard recognizes the responsibility that end user do not degrade the voltage if the utility serving other users by requiring nonlinear current from the utility and also recognizes the responsibility of the utilities to provide voltage close to sine wave. The other IEEE standards are IEEE-1159-1995 [87] recommended practice for monitoring electric power quality and IEEE-1100-1999 [88] recommended practice for powering and grounding sensitive electric equipment.

An IEEE 1459-2010 [89] standard stipulates that maximum efficiency in electrical network is obtained when only the fundamental active current is demanded and also the PCC voltages contain the fundamental positive sequence component. Apart from this, several IEC standards are recommended such as IEC 6100-2-2, IEC-61000-2-4, IEC-61000-3-2 and IEC-61000-4-15. These standards recommended compatibility levels for low frequency conducted disturbance and signaling in public supply systems, compatibility level in industrial plants for low frequency conducted disturbance, limits for harmonic current emissions and functional and design specifications for flicker measuring apparatus [90-91].

2.4 LITERATURE REVIEW ON POWER QUALITY MONITORING [92-97]

In electric distribution system, power quality disturbance such as voltage sag/swell, over voltage, under voltage, harmonic distortion, spikes, notches, transients etc., need to be identified before necessary mitigation action can be taken. Dash et al. [92] have introduced a new approach based on an adaptive neural network for the estimation of harmonic amplitudes and phase and total harmonic distortions. Gaouda et al. [93] have presented wavelet transform for monitoring power quality problems. They have identified the ability of wavelet transform to separate power quality problems that overlap in both time and frequency. Yang and Liao [94] have identified degraded performances of wavelet transform due to the existence of noises riding on the signal. They have proposed a de-noising scheme for enhancing performances of wavelet transform based power quality monitoring. This scheme can detect and localized the occurrence of the power disturbances in the noisy environment. Voltage sag detection techniques have been discussed in various literature based on Fourier transform, phase lock loop (PLL) and matrix method [95]. Some authors have presented power quality monitoring techniques such as S-transform, probabilistic neural network, Stockwell transform etc. [96-97].

2.5 LITERATURE REVIEW ON CONFIGURATIONS OF DSTATCOM [98-120]

The increase in current related power quality problems has led interest of various researchers in developing active shunt compensator also known as distribution shunt compensator (DSTATCOM). The DSTATCOM is capable of compensating various current related power quality problems such as reactive power, harmonics, neutral current and load balancing in power factor correction (PFC) and voltage regulation modes. The basic objective of PFC mode is to compensate for the reactive power by connecting shunt compensator parallel to the consumer load. Voltage at the PCC is generally not regulated and there is some voltage drop due to internal impedance of the utility and distribution network. Therefore, the purpose of operating shunt compensator in voltage regulation mode is to regulate voltage at PCC. Singh et al. [98] have presented a comprehensive study of configurations of DSTATCOM. They have suggested that the DSTATCOM can be configured based on the number of switching devices used, use of isolation transformer and use of type of transformer for neutral current compensation. A number of configurations such as three phase three wire and three phase four wire are reported in the literature [99]. The active shunt compensators can also be classified based on the type of converters used such as voltage source converter and current source converter. The detail literature survey on configurations of DSTATCOM is given as follows.

2.5.1 Three Phase Three Wire DSTATCOM Configuration

Three phase three wire system requires three leg VSC used as DSTATCOM and used for compensation of consumer load in three phase three wire distribution system. The DSTATCOM under this configuration is able to mitigate various power quality problems such as harmonics, reactive power, voltage regulation and load balancing. Gyugyi and Strycula [100] have introduce first the concept of active shunt compensator in 1976. In three phase three wire system, there is

absence of neutral current conductor, consequently absence of zero sequence current components. Peng et al. [101] have presented active power filter using quad series voltage source pulse width modulation (PWM) converters to suppress harmonics by injecting compensating currents. Fugita and Akagi [102] have discussed the capability of shunt active power filter to regulate the distribution line voltage by means of adjusting reactive power. Simulation and experimental results have been shown to verify the effectiveness of shunt active power filter capable of both harmonic damping and voltage regulation.

Mishra et al. [103] have presented operation of a DSTATCOM in voltage control mode. The DSTATCOM used as a voltage regulator to maintain voltage of a particular bus. The amplitude of the bus voltage is calculated, whereas its phase angle is generated from the DC capacitor control loop. Chandra et al.[104] have discussed shunt active power filter for voltage regulation, harmonic elimination, power factor correction and load balancing. In this, a three phase IGBTs based current controlled voltage source converter (CC-VSC) with DC bus capacitor is used as shunt active power filter. Singh et al. [105] have discussed modeling and design of different control strategies for three phase, three wire DSTATCOM. Singh et al. [106] have investigated a three-pole shunt active power filter system working with three phase/single phase load. They have developed a prototype model which operates in two modes, three pole device and four pole device. Babaei et al. [107] have discussed symmetrical and asymmetric multilevel inverter topologies with reduced switching devices. They designed multilevel inverter with reduced number of switching device in comparison with the other topologies. Modeling of DSTATCOM using battery energy storage system with improved power quality is also reported in the literature [108].The presented system is designed for voltage control, power factor correction and active power control.

2.5.2 Three Phase Four Wire DSTATCOM Configuration

This configuration of DSTATCOM in three phase four wire system is for mitigation of neutral current along with other power quality problems such as harmonics elimination, reactive power compensation and load balancing. Four wire configurations can be classified as isolated and non-isolated based on type of transformers and number of switches used by VSC. Various connections of VSC such as four leg VSC, three leg VSC with split capacitors, three single phase VSCs, three leg VSC with zig-zag transformer etc. are used in four wire configuration.

Singh et al. [109], have presented three phase, four wire DSTATCOM system for load balancing, neutral current compensation, power factor correction and voltage regulation feeding commercial and domestic consumers. Various topologies are available in the literature for three phase four wire DSTATCOM system for compensating neutral current along with necessary compensation features of three phase three wire system [110]. These topologies are classified as three H bridge, three phase four wire capacitor mid-point and three phase four wire four leg [111-113]. The H-bridge shunt compensator topology uses three H-bridge voltage source converters which are connected through isolation transformers. The basic difference between capacitor mid-point topology and four wire four leg topologies is the number of power semiconductor devices and the connection of the neutral wire. Shukla et al.[114] have discussed two different multilevel topologies for three phase four wire DSTATCOM. These are diode clamped multilevel inverter and flying capacitor multilevel inverter. The advantages of multilevel inverters in DSTATCOM are smaller filter size, lower switching losses, lower electromagnetic interference, and lower voltage stress of power semiconductors. The need of interconnecting transformer can be eliminated with the help of multilevel inverters [115]. The topology of DSTATCOM is reported based on non-isolated three leg VSC with a zig-zag transformer. This is used to reduce neutral

current and advantageous due to passive compensation and less complexity over the active compensator [116]. The other transformers such as T-connected, star and hexagon are also used along with three leg VSC as three phase four wire DSTATCOM [117-118]. The isolated topologies for three phase four wire DSTATCOM are based on three single phase VSC, consist of three H-bridge VSCs that supported by common DC storage capacitor and three leg VSC with transformers [119-120].

2.6 LITERATURE REVIEW ON CONTROL ALGORITHMS

The effectiveness of shunt compensator depends upon control technique used for estimation of reference supply currents, which are used for generation of switching pulses for three phase VSC used as DSTATCOM. The estimated reference supply currents consist of fundamental active and reactive component of load currents. Substantial literature is available on control algorithms for DSTATCOM. The developed control algorithms are classified into four major categories such as conventional control algorithms, adaptive theory based control algorithms, recursive theory based control algorithms and artificial intelligence based control algorithms. The literature survey on the developed control algorithms is given as follows.

2.6.1 Conventional Control Algorithms[121-142]

These control algorithms are based on the theories such as power balance theory, instantaneous reactive power theory, conductance based and instantaneous symmetrical component theory. Singh et al. [121] have developed a method for shunt compensator, which is used to compensate reactive power and balance the load of three phase, four wire distribution system. Singh et al. [122] have presented active power filter for three phase, three wire system to eliminate harmonics and to compensate for reactive power under nonlinear loads. Singh et al. [123] have developed power balance theory for active power filter for controlling the flow of real power

from the AC mains to the load, harmonics and reactive power from the active filter to the load. A number of literature is available where power balance theory based control algorithm is used for harmonics mitigation, reactive power compensation and load balancing [124]-[125].

Akagi et al. [126] have discusses instantaneous reactive power compensator comprising switching devices which require no energy storage devices and the instantaneous imaginary power has been introduced on the same basis as the conventional instantaneous real power for the three phase system. Substantial literature is available on instantaneous reactive power theory for shunt compensator using multiple voltage source PWM converters, three phase four wire system, three phase power system used for sinusoidal or non-sinusoidal, balanced or unbalanced, three-phase power systems with or without zero sequence currents and voltages and power quality enhancement in distributed generation system [127-131]. In some literature, the conductance based control algorithm is developed for voltage regulation of asynchronous generator in isolated small hydro power generation [132]. This type of algorithm is applied to shunt compensator for mitigation of current related power quality problems [133-135]. Ghosh and Joshi [136] have presented new concept of reactive power generation in power distribution system for load balancing and power factor correction. Rao et al. [137] have discussed instantaneous symmetrical theory to explore various control strategy of load compensation under balanced and unbalanced supply voltages and merits and demerits of these control algorithms are presented based on total harmonic distortion, power factor of source currents and compensator ratings. This theory is discussed in the literature for compensation of load in three phase four wire distribution system, load compensation under unbalanced and distorted voltages and control of micro grid VSC for bidirectional power flow along with power quality compensator [138-142].

2.6.2 Adaptive Theory Based Control Algorithms [143-161]

Adaptive control techniques provide a systematic approach for automatic adjustment of controllers in real time in order to achieve desired performance. This area is developed in terms of adaptive filtering, control algorithms and analysis. Adaptive control can provide automatic tuning in closed loop for the developed controller parameters [143-145]. Luo and Hou [146] have discussed a new adaptive detecting method for harmonics and reactive currents based on adaptive interference cancelling theory. Adaptive detecting approach of harmonic current for active power filter based on a neuron through studying mapping relation and learning algorithm of the neuron model and its realization using analog circuitry have been presented in the literature [147-149]. Elnadyet al. [150] have presented a novel method for the mitigation of the voltage sag and voltage flicker by using adaptive and extended Kalman filter and its derivatives. In some literature, an adaptive notch filtering approach is introduced to extract the harmonic and reactive current components for power quality improvement in grid-connected converters [151-152]. Arya et al. [153] have developed leaky least mean square (LMS) based control algorithm for control of three phase DSTATCOM, with improved dynamic response and fast convergence. Various other adaptive filtering techniques based on Wiener filter, fixed step LMS and variable step size LMS have been presented for numerous applications of noise reduction in signal processing and harmonic detection in shunt active power filter [154-160]. Singh et al. [161] have presented an implementation of adaptive filter for three phase DSTATCOM for harmonics elimination, reactive power compensation and load balancing.

2.6.3 Recursive Theory Based Control Algorithms [162-176]

In the recursive techniques, computation starts with initial conditions and the information contained in new data samples is used to update the old estimated values [162]. Chen et al. [163]

have designed a shunt active power filter based on recursive least square (RLS) control algorithm for compensation of reactive power, harmonics and load balancing. Zawawi et al. [164] have presented RLS based control algorithm for harmonic identification. Pereira et al. [165] have discussed two control techniques based on LMS and RLS to improve the transient response time of harmonic detection. The variable forgetting factor RLS control techniques has been used for various applications in signal processing such as signal representation, system identification etc. [166-169]. The recursive inverse control technique uses variable step size and instantaneous value of the autocorrelation matrix in the coefficient update equation that leads to an improved performance of the algorithm in terms of fast convergence and less steady state error [170-172]. Recursive theory such as immune feedback based control techniques recent application includes the control of a single phase inverter [173], and a three phase inverter [174]. The literature review shows the application of immune based feedback law for a single STATCOM for voltage control [175], as well as multiple STATCOM [176]. The authors have taken a 10 machine, 39 node system and used STATCOM for the control of voltage at the bus bar where STATCOM is installed. They have applied humoral immune system for control of two STATCOM. Both the papers present simulation results for large interconnected power system.

2.6.4 Artificial Intelligence Based Control Algorithms [177-193]

The control algorithms based on artificial intelligence work on the principle of human intelligence to achieve a specific task for which they are designed. These control algorithms have the capability of learning, self-organizing or self-adapting. Singh et al. [177] have designed and developed a neural network based control scheme for selective compensation of current related power quality problems. Arya et al. [178] have presented learning-based anti-Hebbian control algorithm for compensation of linear and nonlinear loads. This algorithm is proposed to control

the DSTATCOM reactive power compensation, harmonics elimination and load balancing. The controllers based on intelligent techniques such as neural network, fuzzy logic and adaptive neural-fuzzy network have been presented in the literature [179-183]. Various authors have proposed in the literature that the parameters of conventional controller such as proportional integral (PI) vary according to variation in system parameters and require exact mathematical model of the system. However, intelligent controllers such as fuzzy, adaptive neuro-fuzzy etc. are robust and exhibit better transient and steady state response than conventional PI controller [184-185].

The other type of artificial intelligence control technique is recurrent neural network (RNN) [186]. The back propagation and back propagation through time learning methods for neural network retain the information about large number of previous training data, which can be drawback for the real time application. This can be overcome by the recurrent neuron network such as (RNN). Several gradient based techniques are used for training RNN such as back propagation through time (BPTT), recurrent back propagation (RBP) [187], and real time recurrent learning (RTRL) [188-190]. The variable step size LMS based control technique exhibits fast convergence and less static error [191-193]. The step size estimated using ANFIS learns faster and achieves less error in estimation.

2.7 LITERATURE REVIEW ON DSTATCOM APPLICATION TO GRID INTEGRATION OF SPV ARRAY [194-207]

The voltage source converter (VSC) used to interface renewable energy source (RES) such as solar photovoltaic (SPV) array can be used to incorporate power quality solutions. The VSC can be utilized as power converter to inject power generated from SPV array to the grid and perform functions of DSTATCOM such as harmonics elimination, reactive power compensation and load balancing [194-197]. The solar photovoltaic-micro turbine grid interface using VSI has been

given the voltage support and control in rural application with sliding mode control [198]. Chidurala et al. [199] have presented application of PV inverter as a solar-DSTATCOM with a new control strategy provides the individual phase voltage regulation, harmonics and reactive power compensation at the integration point during both day and night time. Tsengenes and Adamidis [200] have given a strategy for better utilization of the SPV system, according to this strategy during sunlight the system sends active power to the grid and at the same time compensates the reactive power of the load. In case there is no sunlight, the inverter only compensates the reactive power of the load. Essakiappan et al. [201] have indicated that power converter used in SPV system operates at high frequency, which produce common mode voltage at the output in addition to the differential mode voltage. This increases the voltage on the lines and switches potentially leading to reduction in lifetime. Thus it is prerequisite to minimize effect of common mode voltage and current in SPV system.

Villalva et al. [202] have proposed a method of modeling and simulation of photovoltaic arrays. Verma et al. [203] have designed solar photovoltaic array of 20kW peak power capacity. In this a current synchronous detection based control of a grid interfaced SPV power generating system is presented with an improved power quality at AC mains. Singh et al. [204] have proposed design of various components of SPV system such as SPV array panel, DC-DC boost converter, DC bus capacitance, DC bus voltage and AC interfacing inductors. Kamatchi Kannan et al. [205] have investigated a three-phase DSTATCOM, which is fed by PV array or battery operated DC–DC boost converter is proposed for power quality improvement in the distribution system. Jain et al. [206] have proposed a solar energy conversion system also performs in improving power quality at PCC. This consists of a boost converter, which serves the purpose of maximum power point tracking (MPPT) and VSC, which performs reactive power compensation, harmonics

elimination and feeds solar power to the grid. Singh et al. [207] have proposed an improved linear sinusoidal tracer (ILST)-based control algorithm for a single-stage, three-phase grid connected solar photovoltaic (SPV) system, not only feeds extracted solar energy into the grid but it also helps in improving power quality in the distribution system.

2.8 IDENTIFIED RESEARCH AREAS

Based on exhaustive literature review on power quality problems, monitoring and mitigation techniques, the research areas which have been identified based on this review are some major issues related to complexity, computational burden, response time and robustness need to be resolved in development of control algorithms for DSTATCOM and its applications. The key objectives of the proposed research work are aimed to design and develop some new control algorithms for three phase DSTATCOM, which perform faster with reduced complexity and computational burden. The application areas of DSTATCOM in integrating RES such as SPV array to the grid have also been proposed. This system can be utilized as power converter to inject power generated from SPV array to the grid and performs functions of DSTATCOM such as harmonic elimination, reactive power compensation and load balancing.

The algorithms which are identified in this investigation are classified into four major categories based on their operating principle. These algorithms are classified as conventional control algorithms, adaptive theory based control algorithms, recursive theory based control algorithms and artificial intelligence based control algorithms for control of three phase DSTATCOM. The detail description of these investigated control algorithms and DSTATCOM application to grid integration of SPV array are given as follows.

- **Conventional Control Algorithms**

In conventional control algorithms, the estimation of reference supply currents for generation of switching pulses for control of three phase VSC are performed with investigated power balance theory (PBT), instantaneous reactive power theory (IRPT), conductance based control algorithm and instantaneous symmetrical component theory (ISCT).

- **Adaptive Theory Based Control Algorithms**

In adaptive theory based control, the control techniques provide a systematic approach for automatic adjustment of controllers in real time in order to achieve desired performance. These control algorithms can provide automatic tuning in closed loop for the developed controller parameters. The control algorithms investigated under this category are based on Wiener filter theory, fixed step size least mean square (FSSLMS) and variable step size least mean square (VSSLMS). Different variants of LMS technique are designed, developed and compared for control of three phase DSTATCOM.

- **Recursive Theory Based Control Algorithms**

The control techniques under this category works by starting computation with initial conditions and the information contained in new data samples is used to update the old estimated values. The control algorithms investigated under this category are based on recursive theory and include algorithms such as variable forgetting factor recursive least mean square (VFFRLS), variable forgetting factor based recursive inverse (VFFRI) and immune feedback principle for estimation of reference supply currents, which are used to control three phase VSC used as DSTATCOM.

- **Artificial Intelligence Based Control Algorithms**

The control algorithms under this category are based on the principle of human intelligence to achieve a specific task for which they are designed. These control algorithms have the capability

of learning, self-organizing or self-adapting. The control algorithms investigated under this category are based on intelligent techniques such as fuzzy logic, adaptive neuro fuzzy inference system (ANFIS), real time recurrent learning (RTRL) and adaptive neuro fuzzy inference system -least mean square (ANFIS-LMS) for estimation of reference supply currents, which are used to control of three phase VSC used as a DSTATCOM.

- **DSTATCOM Application to Grid Integration of SPV Array**

The VSC used in DSTATCOM is utilized as power converter to inject power generated from SPV array to the grid. The functions of DSTATCOM of such as harmonic elimination, reactive power compensation, voltage regulation and load balancing are also performed along with injecting real power to the grid. The two stage three phase SPV grid connected system is developed, which consists of DC-DC boost converter and VSC as power converter. The duty cycle of DC-DC boost converter is determined by maximum power point tracking (MPPT) algorithm. The control of VSC for real power injection along with power quality improvement is performed with the developed control algorithms mentioned under above categories.

2.9 CONCLUSIONS

Extensive research work has been carried out in the area of shunt active compensator in terms of configuration, control and its applications. This technology has been found to be well established and practical shunt compensators are installed at distribution level for mitigating current related power quality problems. It has been observed after review of literature that significant development is carried out in the broad area of active shunt compensator. However, there exists a scope in terms of development of fast, less complex and accurate control algorithms with less computational burden. The application of shunt compensator for integrating RES such as SPV to the grid is a recent trend and needs to be explored further.

CHAPTER-III
DESIGN AND DEVELOPMENT OF DSTATCOM

3.1 GENERAL

This chapter deals with the design and development of a three phase DSTATCOM at distribution level. The selected DSTATCOM configuration consists of three-leg voltage source converter (VSC) with insulated gate bipolar transistors (IGBTs) using antiparallel diodes and a DC capacitor. The simulation model of the system is developed in MATLAB environment using SIMULINK and Sim Power System (SPS) tool boxes. The simulation study is carried out using components such as VSC works as current controlled voltage converter. The interfacing inductors along with ripple filters are used to limit the ripple currents. A set of three phase linear/nonlinear loads are considered in this distribution system to be compensated by proposed DSTATCOM. An experimental prototype is developed in the laboratory to validate the simulated performance of DSTATCOM. This developed system uses VSC as a DSTATCOM, which is controlled by digital signal processor (DSP). The system configuration, simulation and hardware development of DSTATCOM are discussed in detail in different sections of this chapter.

3.2 CONFIGURATION OF THREE PHASE DSTATCOM

This section discusses the configuration and design of three phase DSTATCOM. Fig. 3.1 shows the block diagram of three-phase distribution static compensator (DSTATCOM). A three phase AC mains with grid impedance, shown using series L_s-R_s branch, feeds a variety of loads. The DSTATCOM is designed using three phase voltage source converter (VSC) and it is realized using a three leg converter bridge having six insulated gate bipolar transistors (IGBTs) with anti-parallel diodes and high value capacitors at DC side. Interfacing inductors (L_f) are used at the AC

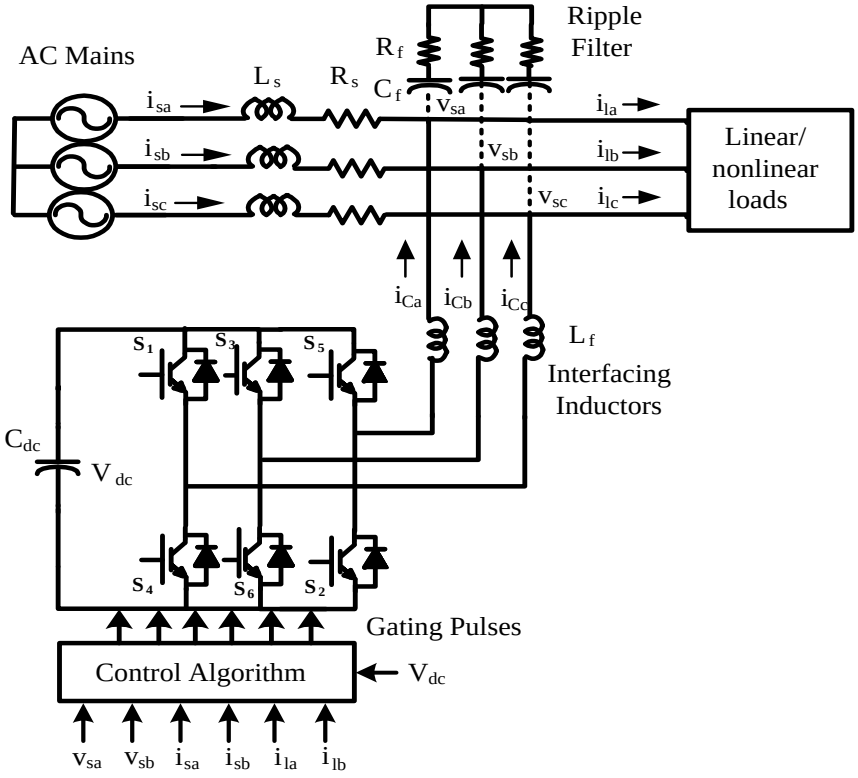


Fig. 3.1 Schematic diagram of the DSTATCOM

side of VSC, which couple the VSC to the grid. Series connected capacitive (C_f) and resistive (R_f) elements at PCC help to reduce the high frequency switching noise generated by the switching of IGBTs. Three phase linear and nonlinear loads are connected at the point of common coupling (PCC) to be compensated by proposed DSTATCOM. The linear load is realized using three phase star connected R-L branches. The nonlinear load is realized using a three phase uncontrolled bridge rectifier with series R-L branch.

3.3 OPERATING PRINCIPLE AND FEATURES OF DSTATCOM

The DSTATCOM is a shunt connected static converter. It comprises of a VSC having semiconductor devices such as IGBTs with antiparallel diodes [61]. The single line diagram of shunt compensator is shown in the Fig. 3.2, which presents the basic operating concept of the shunt compensator. The three leg VSC is used in the system, where switches of each leg

switched on and off once in a complete cycle. The antiparallel diodes allow flow of current in the reverse direction. The VSC output RMS voltage is given as,

$$V_{LL} = \frac{\sqrt{3}mV_{dc}}{2\sqrt{2}} \tag{3.1}$$

where V_{dc} is the DC bus voltage and m is the modulation index. The shunt compensator is able to supply leading reactive power if V_{LL} is greater than the PCC line voltage (v_{ab}), otherwise it draws lagging reactive power from the AC mains.

The load current (i_l) for the nonlinear load at n^{th} sampling instant is given as,

$$i_l(t) = I_{lf}\sin(wt + \emptyset_f) + \sum_{h=5,7\ldots}^{\infty} I_{lh}\sin(h\omega t + \emptyset_h) \tag{3.2}$$

where I_{Lf}, I_{Lh}, $\emptyset_f$ and $\emptyset_h$ denote the peak value of fundamental load current, peak value of harmonic current, phase angle of fundamental component of load current and phase angle of the harmonic component of load current respectively. It is observed from Eq. (3.2), that the load current can be broadly divided into two parts. The first part corresponds to fundamental component and second part corresponds to harmonics component. Fundamental and harmonic components can be further divided into two parts viz. one part corresponding to active power

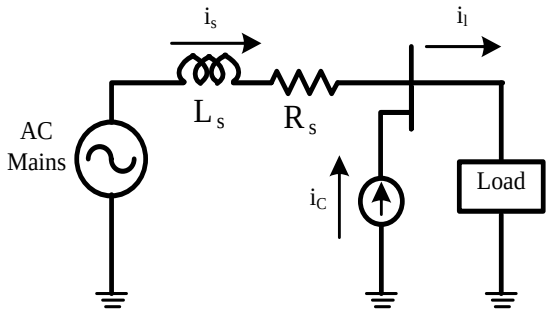


Fig. 3.2 Basic Principle of DSTATCOM

components (i_{lfp} and i_{lhp}) and another part corresponding to reactive power components (i_{lfq} and i_{lhq}), as shown in Eqns. (3.3) and (3.4),

$$i_l(n) = i_{lf} \sin \omega n \cos \emptyset_f + i_{lf} \cos \omega n \sin \emptyset_f$$

$$+ \sum_{h=3,5,7\ldots}^{\infty} (i_{lh} \sin h\omega n \cos \emptyset_f + i_{lh} \cos h\omega n \sin \emptyset_f) \quad (3.3)$$

$$i_l(n) = i_{lfp} + i_{lfq} + i_{lhp} + i_{lhq} \quad (3.4)$$

The shunt active compensator should compensate for harmonics and reactive current (i_{lfq}, i_{lhp} and i_{lhq}), so that the supply provides only fundamental active current (i_{lfp}) component of the load current.

3.4 DESIGN OF COMPONENTS FOR THREE PHASE DSTATCOM

The design of three phase VSC based DSTATCOM is presented here. The main components of shunt compensators are VSC, voltage sensors, current sensors, interfacing inductors and ripple filters [1, 9]. The parameters for design components are given in Appendix-A.

3.4.1 Design and Selection of Voltage Source Converter

The design and selection of three phase VSC depends upon the compensation requirement such as harmonic elimination, reactive power compensation and load balancing. The rating of VSC should be greater than the harmonic and reactive power compensation required for linear and nonlinear loads. The rating of VSC considered here is around 415V, 50Hz and 25kVA for the load compensation of 20kVA.

3.4.2 Design and Selection of DC Bus Voltage

The DC bus voltage is calculated as [1],

$$V_{dc} = 2\sqrt{2}V_{LL}/\sqrt{3}m = \frac{2\sqrt{2}\times 415}{\sqrt{3}} = 677.69\text{V} \quad (3.5)$$

where V_{LL} is the AC line voltage of the shunt compensator and m is modulation index. Modulation index m is selected 1 and AC line voltage of DSTATCOM is 415V, then V_{dc} is obtained as 677.69V. Thus the DC bus voltage is selected as 700V.

3.4.3 Design and Selection of DC Bus Capacitance

The design of DC bus capacitance of VSC is given as [1],

$$C_{dc} = 6k_1V_{ph}aI_{ph}t/(V_{dc}^2 - V_{dc1}^2) = \frac{6\times 0.1\times 239.60\times 1.2\times 19\times 0.015}{(700^2 - 677.69^2)} = 1599\mu\text{F} \quad (3.6)$$

where V_{dc} is nominal DC bus voltage, V_{dc1} is minimum voltage level of the DC bus voltage, a overloading factor selected to be 1.2, the constant k_1 is selected 0.1, V_{ph} is phase voltage, I_{ph} is phase current and 't' represents time by which DC bus voltage is to be recovered. According to above given formula in Eqn. 3.6, DC bus capacitance (C_{dc}) is calculated to be around 1599μF and is selected as 1650μF.

3.4.4 Design and Selection of AC Interfacing Inductors

The design of AC interfacing inductors is given by the formula as [9],

$$L_f = \sqrt{3}mV_{dc}/(12a\,f_sI_{crpp}) = \frac{\sqrt{3}\times 1\times 700}{12\times 1.2\times 10000\times 2.85} = 2.95\text{mH} \quad (3.7)$$

where m is the modulation index, V_{dc} DC bus voltage, a is overloading factor selected 1.2 and I_{crpp} is current ripple of the 15% of VSC current. Switching frequency f_s, is selected to be at least two times the frequency of the highest order harmonic to be compensated by the shunt compensator and it is also related to the speed of the processor as sampling frequency depends

upon the speed of the processor. Here sampling frequency is selected as 10 kHz. The calculated value of interfacing inductor is 2.95mH and a value of 3mH is selected.

3.4.5 Design and Selection of Ripple Filters

The ripple filters are used to filter the high frequency switching noise generated by switching of IGBTs in the PCC voltages. These are high pass filters tuned at half the switching frequency and selected as capacitor with series resistance (R_f-C_f). Considering small time constant of the filter $C_fR_f=T_s/10$, where T_s is switching time [9]. For a switching frequency of 10kHz, the value of ripple filter parameters are calculated to be $R_f=3\Omega$ and $C_f=3.33\mu F$. The impedance at fundamental frequency is around 956Ω, which is sufficiently large. Due to this large impedance ripple filter will draw negligible fundamental frequency current. However, at 10kHz its impedance is 5.57Ω, which is quite low to absorb all high frequency components.

3.4.6 Design and Selection of Voltage and Current Rating of IGBTs

The voltage rating of IGBTs of VSC under dynamic load condition is given as [9],

$$V_{sm} = V_{dc} + \Delta V_{dc} = 700 + 70 = 770\text{V} \quad (3.8)$$

where ΔV_{dc} is the 10% overshoot in the DC bus voltage under dynamic load condition. If a reference value of DC bus voltage is selected as 700V, then voltage rating of switches is calculated to be 770V. The IGBTs voltage rating is selected 1200V, after considering appropriate safety factor.

Current rating of IGBTs of VSC under dynamic load condition is given as,

$$i_{sm} = 1.25(I_{sw} + I_{cr}) = 1.25(26.8 + 5.37) = 40.21A \quad (3.9)$$

where I_{sw} and I_{cr} are the peak values of compensator current (26.8A, for nonlinear load specified in Appendix-A) and the allowed ripple currents considering 20%. The current rating is calculated

40.21A. The IGBT module, SKM150GB12V (Semikron make) is selected. The voltage and current rating for selected IGBT module are 1200V and 231A respectively.

3.5 DEVELOPMENT OF PROTOTYPE OF THREE PHASE DSTATCOM

The development of various components for the prototype model of DSTATCOM developed in the laboratory is presented here. This system requires the development and selection of three phase VSC, DC bus capacitor, voltage sensing circuits, current sensing circuits, interfacing inductors, linear and nonlinear loads to be compensated. The development of DSTATCOM hardware prototype, VSC, voltage sensors, current sensors, gating circuit, interfacing inductors and ripple filters are given as follows.

3.5.1 Hardware Configuration of Prototype of DSTATCOM

The prototype of three-phase DSTATCOM is implemented in the laboratory. The system is developed at lower voltage rating of 110V, 50Hz due to available equipment rating constrains in the laboratory. Fig. 3.3 shows the layout of the developed three-phase DSTATCOM. The input of auto-transformer is three phase AC mains of 415V, 50Hz and the output voltage is set at 110V. It feeds linear and nonlinear loads. The DSTATCOM is designed using three phase VSC. This uses six IGBTs with anti-parallel diodes and high value capacitor at DC side. The IGBT module, (Semikron make SKM150GB12V) is used in VSC [208]. The control operation of the VSC used as DSTATCOM is performed with the help of DSP (dSPACE 1104 R&D controller board) embedded in personal computer (PC). The DSP (dSPACE 1104) is real time controller based on a 603 PowerPC floating-point processor [209]. This includes slave DSP subsystem based on the TMS320F240. The PCC voltages (v_{sa}, v_{sb}), supply currents (i_{sa}, i_{sb}), load currents (i_{la}, $i_{lb,}$ i_{lc}) and DC bus voltage (V_{dc}) are sensed by Hall effect voltage and current sensors. Appropriate buffer circuitry is designed for voltage and current sensors using operational

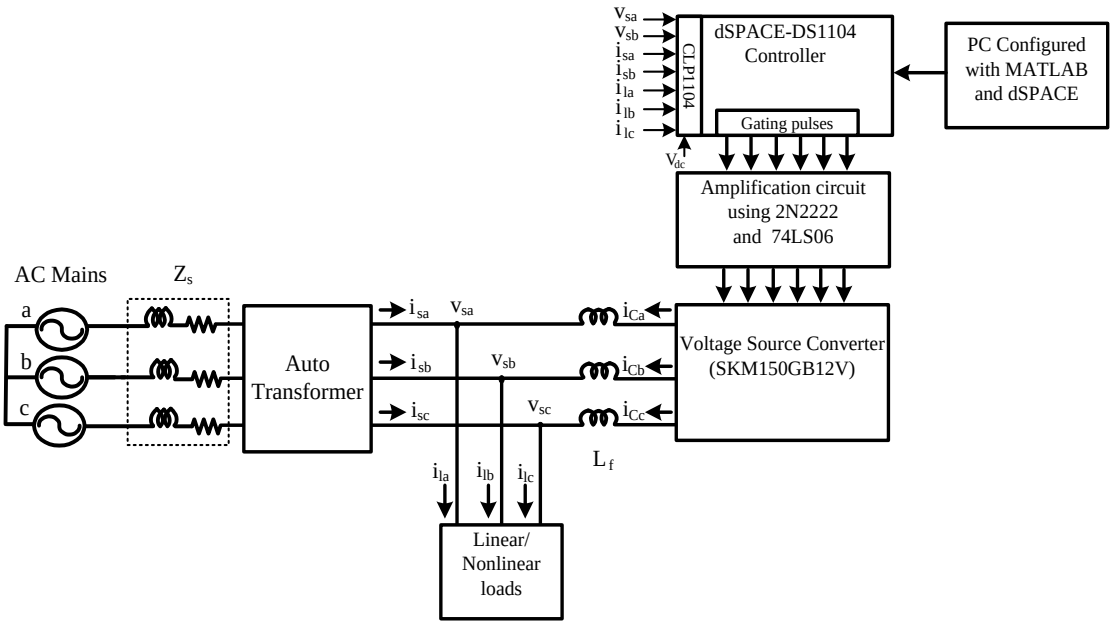


Fig. 3.3 Layout of three phase DSTATCOM

amplifier (OP07). The photograph of developed three phase DSTATCOM in the laboratory is shown in Fig. 3.4. The parameters for developed DSTATCOM system are given in Appendix-B. The control algorithm for generation of reference supply currents is developed in MATLAB environment using SIMULINK and SPS tool boxes. This algorithm is implemented using DSP-dSPACE as shown in Fig. 3.5. The DSP based implementation is mainly divided into three blocks, ADC block, scaling of signals along with control algorithm block and PWM current controller block. The output of voltage and current sensors are given as inputs to the ADC channels of DSP (dSPACE 1104R&D controller board). The dSPACE 1104 contains two different types of ADCs for the analog input channels. The first type contains one 16-bit ADC with four multiplexed (ADC1-ADC4) input signals. The second type contains four 12-bit parallel ADCs with one input signal each (ADC5-ADC8). The signal from ADC channels are scaled up to get the actual values of PCC voltages, supply currents, load currents and DC bus voltage. These signals are given as inputs to the control algorithm for generation of reference supply

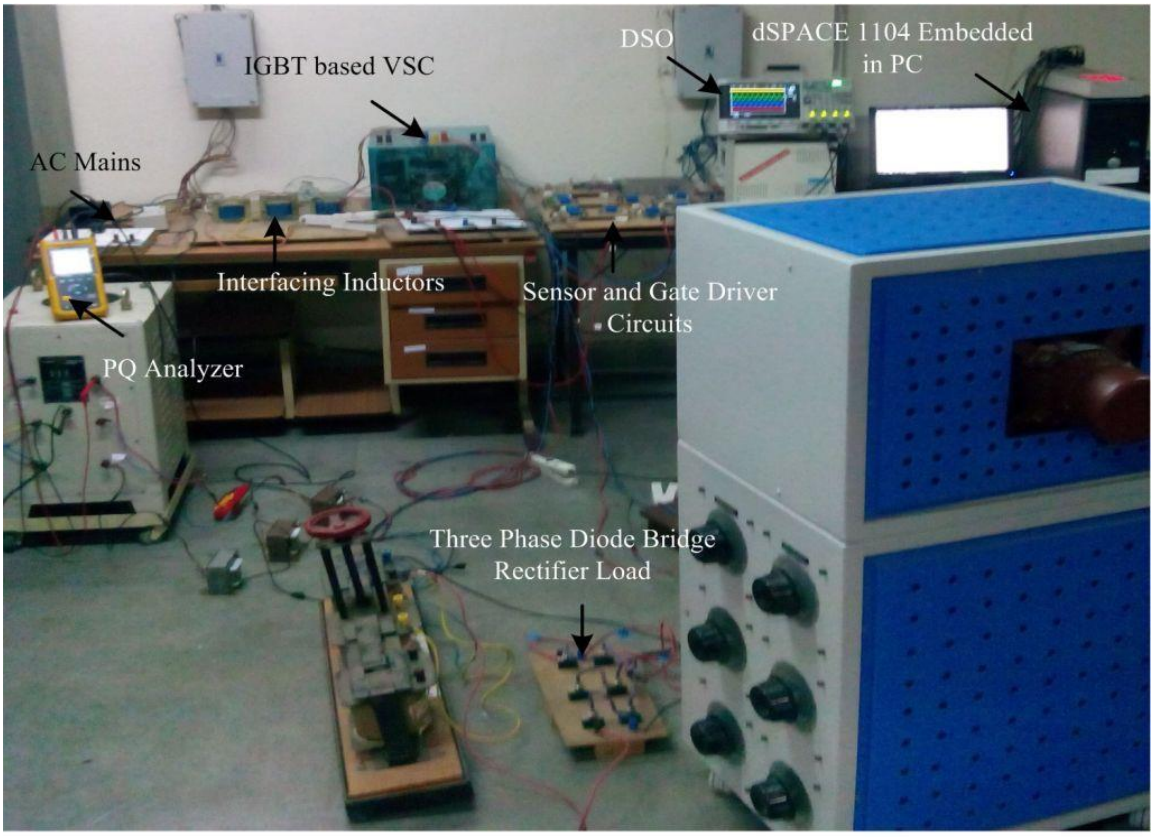


Fig. 3.4 Experimental prototype developed of DSTATCOM in the laboratory

currents. The switching pulses for VSC are taken from PWM port of DSP-dSPACE through the gate driver circuit. The AC side of the VSC is connected to the PCC with the help of interfacing inductors. An implementation of DC and AC bus PI voltage controllers are shown in Figs. 3.6 and 3.7. An implementation of pulse width modulation (PWM) switching in DSP-dSPACE using DS 1104SL_DSP_PWM3 block is shown in Fig. 3.8.

3.5.2 Development of Voltage Source Converter

Fig. 3.9 shows the photograph of VSC (Semikron make) used to developed DSTATCOM prototype in the laboratory. It consists of insulated gate bipolar transistors (IGBTs) with anti-parallel diodes. The rating of the DC bus capacitor and DC bus voltage of capacitor are 1650µF and 800V respectively. The control of VSC is performed with the help of control algorithm implemented on DSP-dSPACE. Switching pulses are generated from PWM port of DSP-

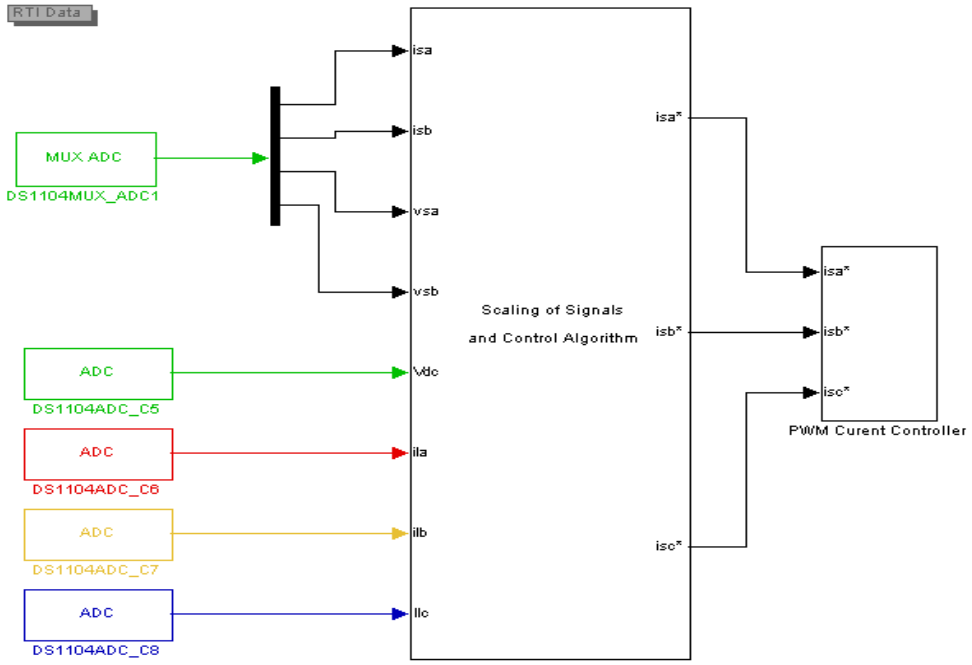


Fig. 3.5 Software for DSP implementation of control for DSTATCOM

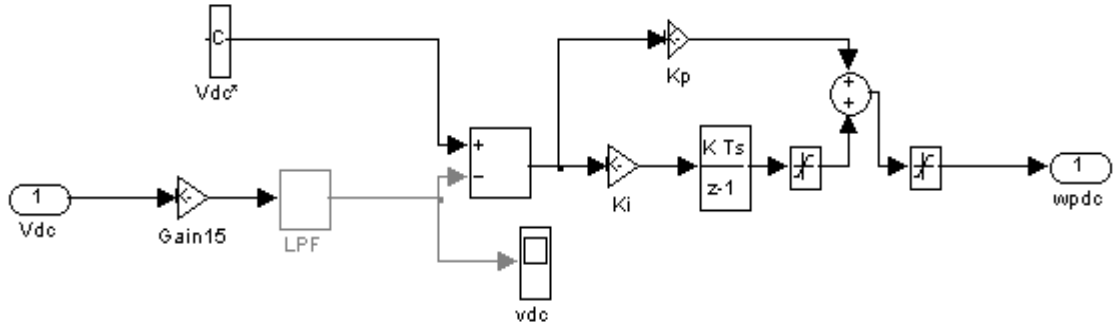


Fig. 3.6 Implementation of DC bus PI controller

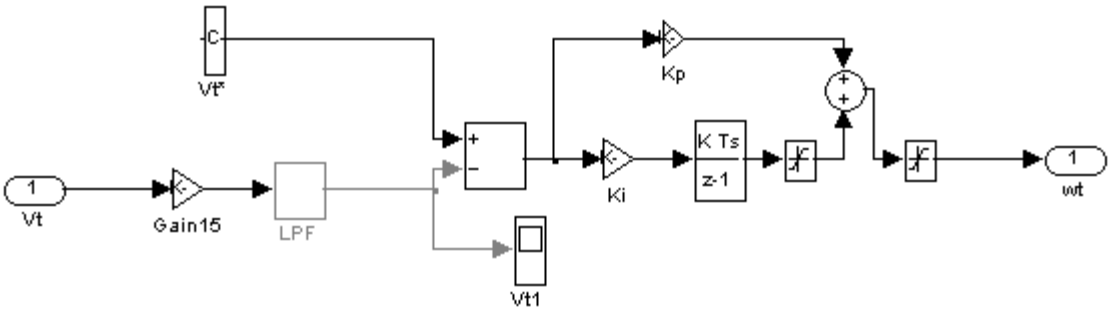


Fig. 3.7 Implementation of AC bus PI controller

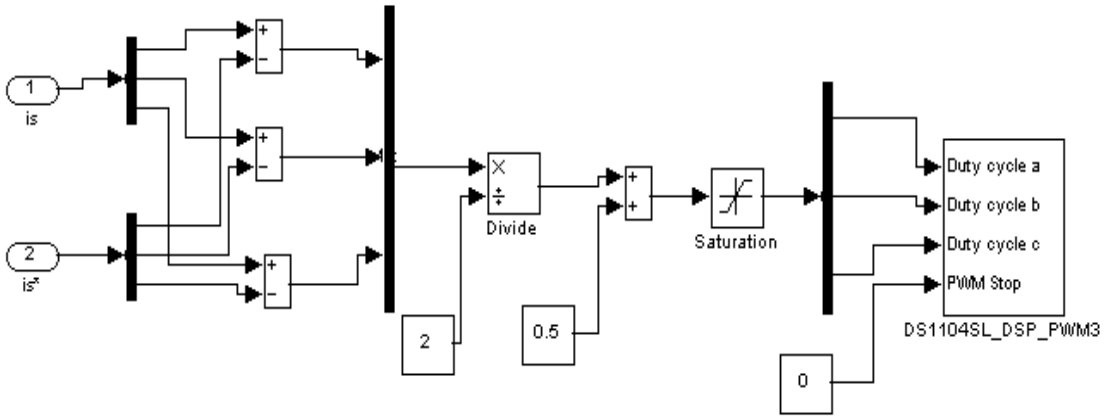


Fig. 3.8 Implementation of PWM current controller

dSPACE and fed to gate driver circuit, which gives 15V output pulses for operation of IGBTs of VSC.

3.5.3 Development of Voltage Sensor Circuit

Figs. 3.10(a) and (b) show the schematic diagram and photograph of voltage sensor circuits. Voltage sensors are used to sense voltages at PCC. For the three phase balanced AC mains

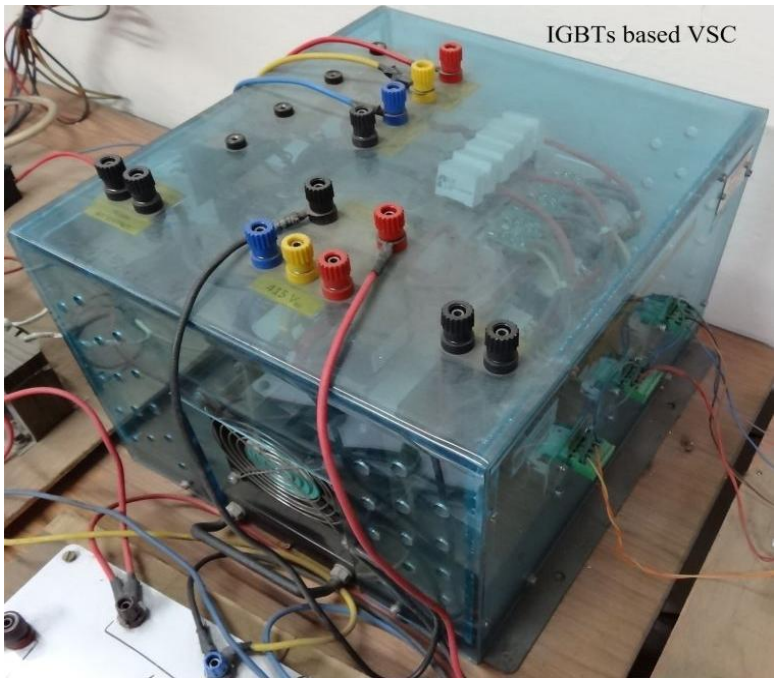


Fig. 3.9 Voltage source converter

voltage, two voltage sensors (LEM LV-25-P) are used [210]. These voltage sensors operate at ±15V DC supply as shown in Fig. 3.10(a). The sensed voltage signal from the voltage sensor is fed to the buffer circuitry. The buffer circuitry is designed using operational amplifier (OP07) with appropriate resistances values. The output signal of buffer circuit is given input to the developed control algorithm through analog to digital (ADC) channel of DSP-dSPACE. Fig. 3.11 shows photograph of DC bus voltage sensor (LEM LV-25-P/SP5). High wattage input resistance (47kΩ, 5W) is used in this circuit. The output signal of this sensor is also fed to buffer circuitry and then ADC channel of DSP-dSPACE.

3.5.4 Development of Current Sensor Circuit

Figs. 3.12(a), (b) and Fig. 3.13 show the schematic diagram and photographs of Hall effect

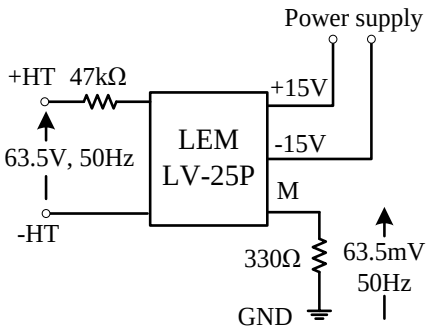


Fig. 3.10(a) Schematic diagram of voltage

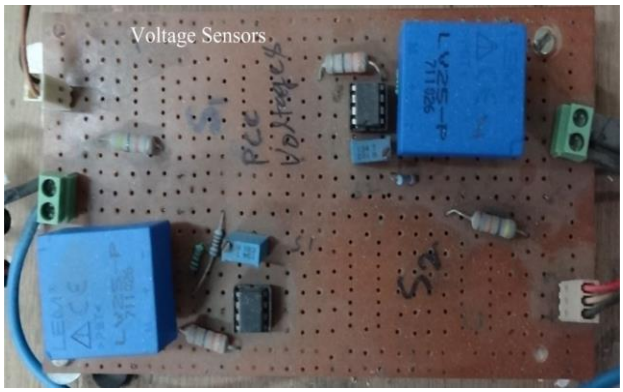


Fig. 3.10(b) PCC voltage sensors

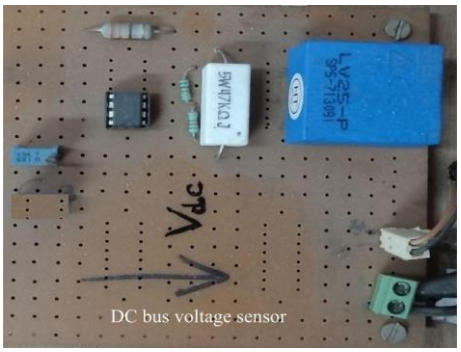


Fig. 3.11 DC bus voltage sensor

current sensor circuit for sensing the load and supply current. For balanced three phase AC mains, two Hall effect current sensors (LEM LA-25) are used for sensing supply side currents and three current sensors (LEM LA-25) are utilized for sensing the load side currents [211]. These current sensors operate at ±15V DC supply as shown in Fig. 3.12(a) and fed to the ADC channels of DSP-dSPACE through appropriate buffer circuitry.

3.5.5 Development of Gating Circuit

Fig. 3.14(a) and (b) show the schematic diagram and photograph of gating circuit. The magnitude of output pulses from PWM port of DSP-dSPACE is 0-5V, but the IGBTs of VSC operates at 0-15V gating pulses. Therefore, the gating circuit is required, which amplify output

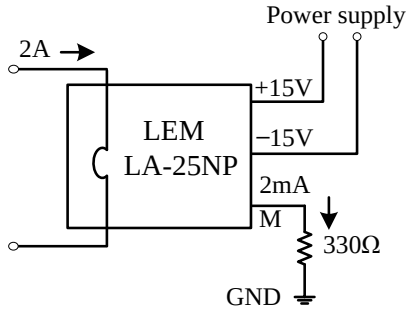


Fig. 3.12(a) Schematic diagram of current sensor

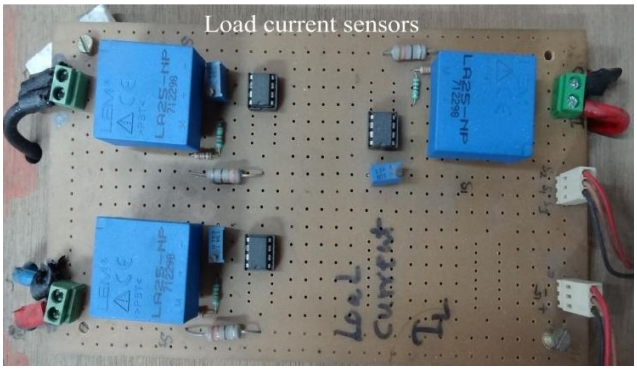


Fig. 3.12(b) Load current sensors

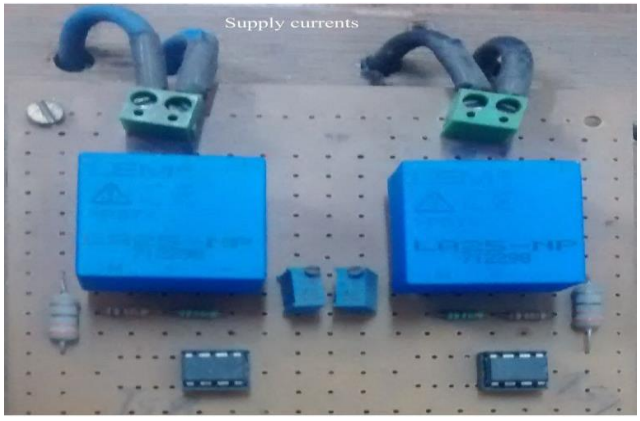


Fig. 3.13 Supply current sensors

gating pulses from PWM port of DSP to 15V. This circuit is designed using 7406 hex inverter integrated circuit, n-p-n transistor (2N2222) and appropriate resistances. Six similar circuits are designed to provide 15V gating pulses to operate the six IGBTs of VSC.

3.5.6 Development of Interfacing Inductors

The design and selection of interfacing circuit are given in section 3.5 and the photograph of interfacing inductors is shown in Fig. 3.15. The value of interfacing inductors depends upon value of DC bus voltage of VSC, switching frequency and allowed percentage ripple current. The rating of interfacing inductor designed here is 3mH and 10A current. The equation for calculating number of turns (N) [212], of the inductor is given as,

$$N = LI_m/(A_cB_m) = \frac{3\times0.001\times10\times\sqrt{2}}{8.658\times10^{-4}\times1} = 49 \quad (3.10)$$

where L is inductance in Henry, I_m is peak value of rated inductor current in A, A_c is core cross section area m^2 and B_m is the flux density in Tesla selected 1T for CRGO. The value of N calculated from Eqn. 3.10 is 49 and it is selected 50. The gauge of wire is given as,

$$a = I/j = \frac{10}{3} = 3.33\text{mm}^2 \quad (3.11)$$

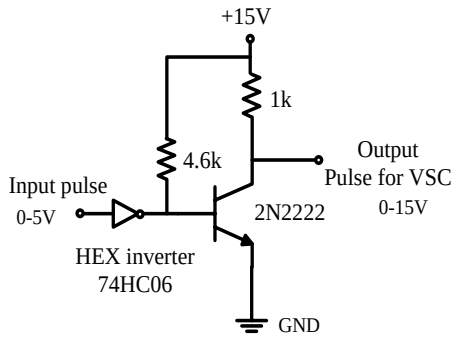


Fig. 3.14(a) Schematic diagram of gating circuit

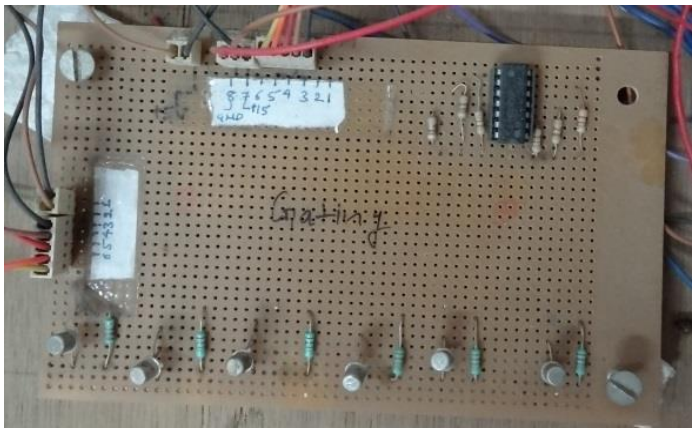


Fig. 3.14(b) Developed gating pulses circuit

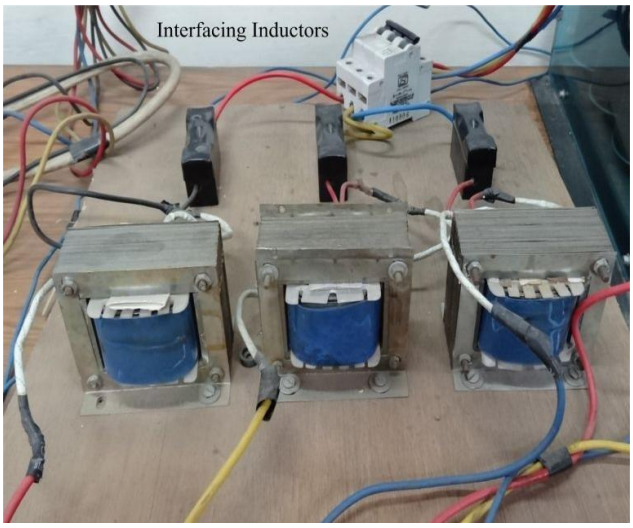


Fig. 3.15 Development of interfacing Inductors

where I is rated inductor r.m.s. current (A) and J current density (A/mm^2) and the value of gauge 'a' calculated is 3.33mm^2. The air gap length (l_g) is given as,

$$l_g = \mu_0 N^2 A_c / L = \frac{4\pi\times10^{-7}\times50^2\times8.658\times10^{-4}}{0.003} = 0.9\text{mm} \quad (3.12)$$

where L is inductance in Henry, N is the number of turns, A_c denotes the core cross section area cm^2 and $\mu_0 = 4\pi*10^{-7}$ H/m. The value of air gap is calculated to be 0.9mm. The calculated values of number of turns (N), wire gauge (a) and air gap length (l_g) are used to design the interfacing inductor having value of 3mH.

3.5.7 Development of Ripple Filter

The design of series R-C ripple filter is shown in Fig 3.16. The values of R and C are selected here are 4Ω and 5μF respectively. The design of these filters is the same as presented in section 3.4.5. These filters are connected at the PCC in parallel with the load and offer high impedance (637Ω) to the fundamental frequency current. Therefore negligible fundamental current is drawn by the ripple filter. However, its impedance at switching frequency of 10kHz is 3.18Ω. This is

Fig. 3.16 Development of resistive capacitive (R-C) ripple filters

quite low to such all switching ripples. The loss in this ripple filter is 2.25W only, which is negligible.

3.6 RESULTS AND DISCUSSION

The detailed discussion on designed and selected values of the components of DSTATCOM for simulation purpose and developed components for hardware prototype is presented here. Testing results of developed DSTATCOM components such as voltage sensors, current sensors, gating circuit and interfacing inductors are also presented. Step by step design and development of the components are given as follows.

3.6.1 Results of Designed of DSTATCOM

The design and simulation are carried out at full rating of AC mains 415V, 50Hz according to Indian power distribution system. The design and selection of various components of DSTSTCOM such as VSC, DC bus capacitance, DC bus voltage, interfacing inductors and ripple filter are same as given in section 3.4. The VSC is selected of 415V, 50Hz and 25kVA rating. The selected IGBT module for VSC is SKM150GB12V (Semikron make), having voltage and current rating as 1200V and 231A. The DC bus voltage and DC bus capacitance are selected as

700V and 1650μF. The value of interfacing inductor is selected around 3mH. The R-C value of ripple filter is selected around 3Ω and 3.33μF. The designed values of these components are given in Table-3.1.

3.6.2 Results of Developed Prototype of DSTATCOM

The experimental prototype of the DSTATCOM is developed in the laboratory at the lower rating of 110V, 50Hz due to available equipment rating constraints in the laboratory. The design and selection of various components of DSTATCOM such as VSC, DC bus capacitance, DC bus voltage, interfacing inductors and ripple series R-C filters are same as given for simulation purpose. The development of VSC, voltage sensors, current sensors, gating circuit, interfacing inductor and ripple filters same as discussed in section 3.5. The selected IGBT module for VSC is SKM150GB12V. The value DC bus capacitance, DC bus voltage, interfacing inductors and ripple R_f-C_f filters are selected 1650μF, 200V, 3mH and 3Ω-5μF respectively for developed

TABLE-3.1
SYSTEM PARAMETERS OF DSTATCOM FOR SIMULATION

Supply voltage	Three phase 415V, 50Hz with source impedance (L_s=1mH, R_s=0.04Ω)
VSC rating	25kVA
DC bus capacitance	1650μF
DC bus voltage	700V
Interfacing inductor	3μF
Ripple R_f-C_f series filter	3Ω-4μF
Load parameters	Three phase diode bridge rectifier with R=15Ω and L=100mH
Switching frequency	10kHz

TABLE-3.2
SYSTEM PARAMETERS OF DEVELOPED DSTATCOM

Supply voltage	Three phase 110V, 50Hz with source impedance (L_s=3.5mH, R_s=0.1Ω)
VSC rating	25kVA
DC bus capacitance	1650μF
DC bus voltage	200V
Interfacing inductor	3μF
Ripple R_f-C_f series filter	4Ω-5μF
Load parameters	Linear load: 15kVA, 0.73 lagging pf Nonlinear load: Three phase diode bridge rectifier with R=15Ω and L=100mH
Switching frequency	10kHz

prototype of DSTATCOM. The rating of components selected for developed prototype is summarized in Table-3.2.

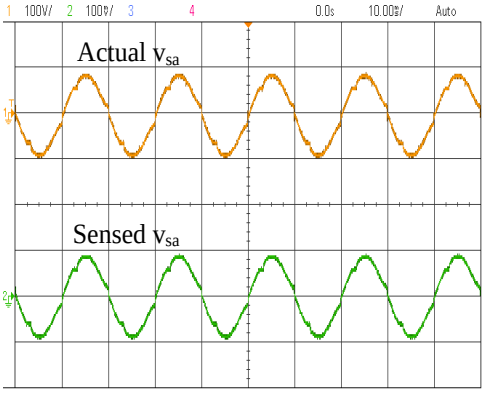
3.6.3 Testing Results of Developed DSTATCOM

Testing results of developed system components such as voltage sensors, current sensors, gating circuit and interfacing inductors is carried out here. Interfacing of voltage and current sensors with the ADC channels of DSP-dSPACE and selection of gain values for sensors output and are also presented.

3.6.3.1 Testing Results of Voltage Sensors

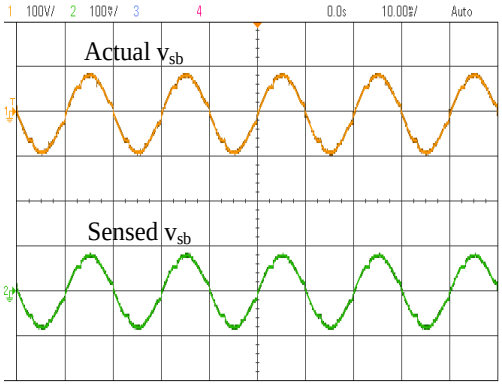
Fig. 3.17 shows the testing results of PCC and DC bus voltage sensors. Only two PCC voltage sensors are required for balanced three phase system. Third phase of voltage is calculated from other two phases. Figs. 3.17(a) and (b) present actual PCC voltages and sensed PCC voltages corresponding to phase ‘a’ and ‘b’ respectively. The actual magnitude of PCC voltages are obtained from high voltage differential voltage probe (Tektronix P5200A). The actual PCC voltage magnitude is 179.8V (P-P), whereas sensed PCC voltage magnitude is 185mV (P-P). Therefore, the value of gains selected around 971.89, for output signals of PCC voltage sensors to achieve actual magnitudes. Fig. 3.17(c) shows waveforms of sensed phase ‘a’, sensed phase ‘b’ and calculated phase ‘c’ of PCC voltages. Fig. 3.17(d) shows waveforms of actual and sensed DC bus voltage of VSC used as DSTATCOM. Initially the DC bus voltage magnitude is at peak amplitude of line voltage around 155.5V and the output of DC bus voltage sensor is 279mV. Therefore, the gain value selected for DC bus voltage sensor is around 557.3, used to obtain actual value of DC bus voltage.

3.6.3.2 Testing Results of Supply Current Sensors



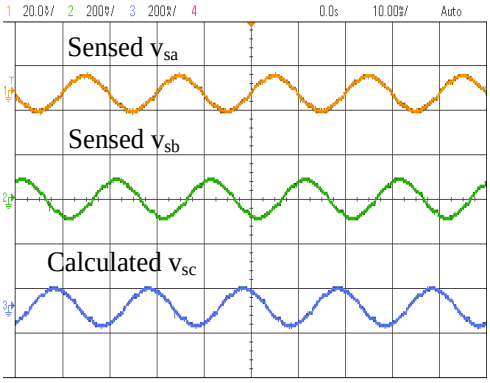
Ch. 1-2- 100V/div-100mV/div, Time axis-10ms/div

(a)



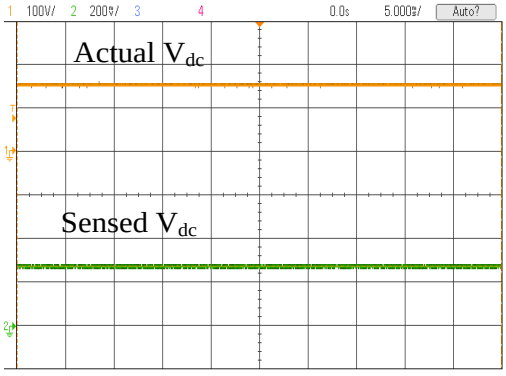
Ch. 1-2- 100V/div-100mV/div, Time axis-10ms/div

(b)



Ch. 1, 2 and 3- 200mV/div, Time axis-10ms/div

(c)

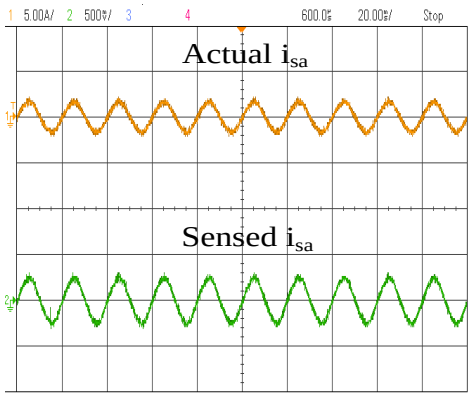


Ch. 1-2- 100V/div-200mV/div, Time axis-5ms/div

(d)

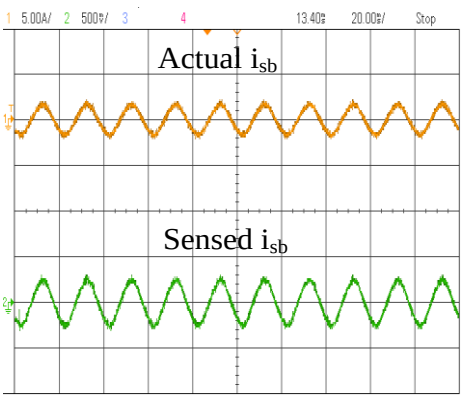
Fig. 3.17 Actual and sensed PCC voltages and DC bus voltage

Fig. 3.18 shows testing results of supply current sensors. For balanced three phase system only two phases (phase ‘a’ and ‘b’) of are required to be sensed. Third phase (phase ‘c’) is calculated from other two phases. Figs. 3.18(a) and (b) depict waveforms of actual current and sensed current corresponding to phase ‘a’ and phase ‘b’ respectively. The actual waveforms of currents are obtained from current probes (Agilent 1146A). It is observed from these results that the actual magnitude of phase ‘a’ of supply current is 5A (P-P), whereas magnitude of sensed current is 165mA (P-P). Therefore, the selected gain value of supply current is around 30.3, which is used to obtain actual magnitude. Fig. 3.18(c) depicts waveforms of sensed phase ‘a’, sensed phase ‘b’ and calculated phase ‘c’ for balanced three phase system.



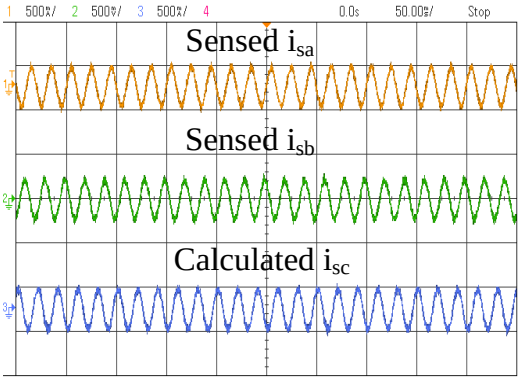
Ch. 1-2- 5A/div-500mA/div, Time axis-20ms/div

(a)



Ch. 1-2- 5A/div-500mA/div, Time axis-20ms/div

(b)



Ch. 1, 2 and 3 -500mA/div, Time axis-50ms/div

(c)

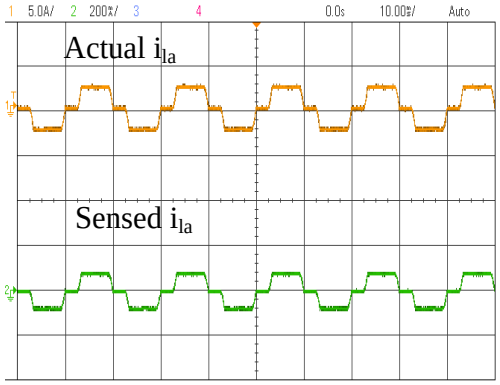
Fig. 3.18 Actual and sensed supply currents

3.6.3.3 Testing Results of Load Current Sensors

Fig. 3.19 shows test results of load current sensors. Three current sensors are required for sensing three phases of load currents. Figs. 3.19(a), (b) and (c) show waveforms of actual load currents and sensed load currents corresponding to phase ‘a’, phase ‘b’ and phase ‘c’ respectively. Actual load currents are observed by using current probe (Agilent 1146A). The gain value selected for load current sensor is 30.3, same as selected for supply currents sensors. Fig. 3.19(d) shows waveforms of sensed all three phases of load currents.

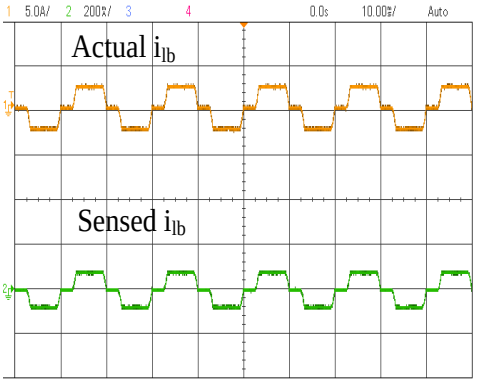
3.6.3.4 Testing Results of Gating Circuit

Gating circuit is developed to amplify gating pulses generated from PWM port of DSP-dSPACE.



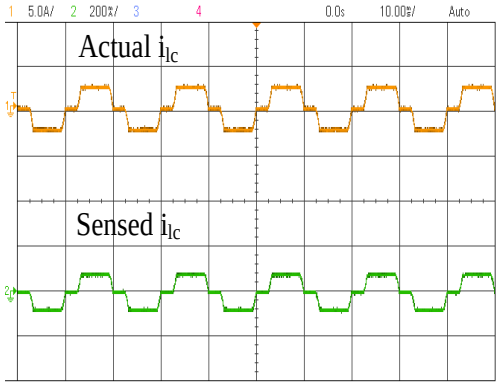
Ch. 1-2- 5A/div-200mA/div, Time axis-10ms/div

(a)



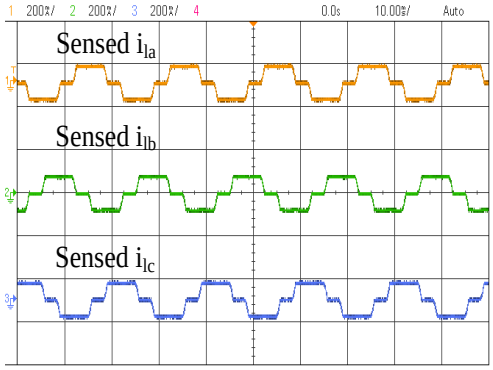
Ch. 1-2- 5A/div-200mA/div, Time axis-10ms/div

(b)



Ch. 1-2- 5A/div-200mA/div, Time axis-10ms/div

(c)



Ch. 1, 2 and 3 -200mA/div, Time axis-10ms/div

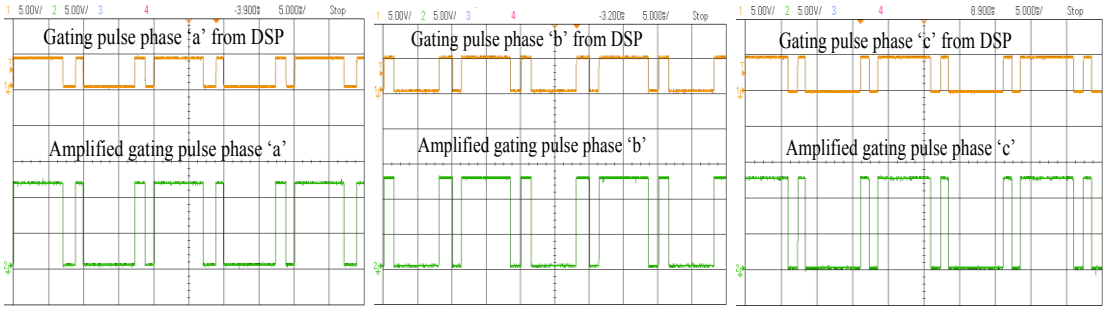
(d)

Fig. 3.19 Actual and sensed load currents

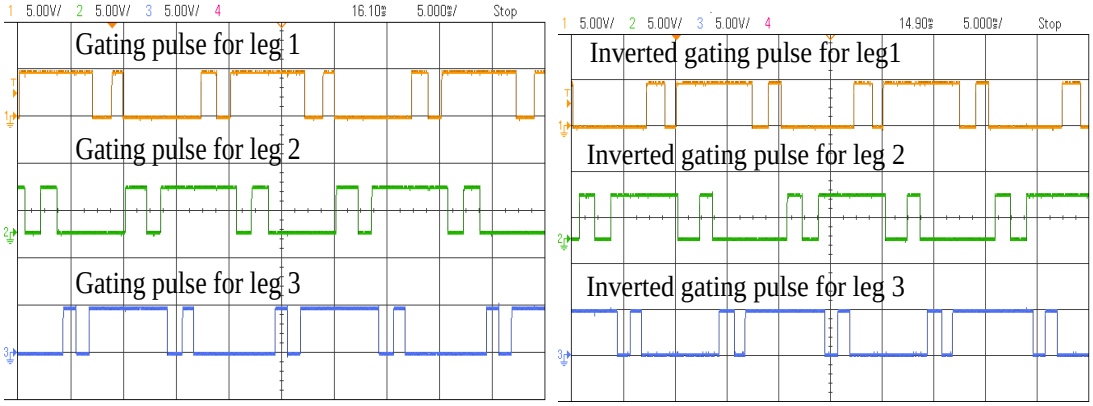
Fig. 3.20 shows the test results of gating circuit. Figs. 3.20(a), (b) and (c) show gating pulses output from digital to analog converter (DAC) channels of DSP-dSPACE and amplified pulses after gating circuit corresponding to phase ‘a’, phase ‘b’ and phase ‘c’ respectively. It is observed from these results that the amplitude of pulses output from DAC channels are 5V and these pulses get amplified to 13V after gating circuit. These results show that gating pulse amplified upto 13V after gating circuit, which is sufficient to derive IGBTs of VSC. Figs. 3.20(d) and (e) present waveforms of gating pulse generated from PWM current controller of DSP and their inverted pulses corresponding to phase ‘a’, phase ‘b’ and phase ‘c’.

3.6.3.6 Testing Results of Interfacing Inductor

The interfacing inductors are developed for connecting AC side of VSC to the PCC point of grid.



Ch. 1-2: 5V/div, Time axis-5ms/div (a) Ch. 1-2: 5V/div, Time axis-5ms/div (b) Ch. 1-2: 5V/div, Time axis-5ms/div (c)



Ch. 1, 2 and 3: 5V/div, Time axis-5ms/div (d) Ch. 1, 2 and 3: 5V/div, Time axis-5ms/div (e)

Fig. 3.20 Gating pulses for three phase VSC

The fixed value of inductor is designed for interfacing VSC to the PCC point. The design of interfacing inductors is same as given in section 3.4. Fig. 3.21 shows testing results of designed

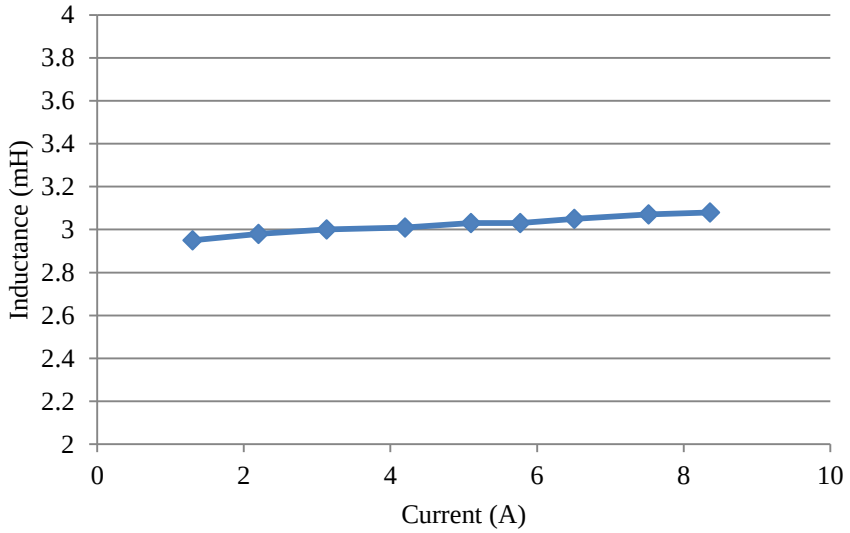
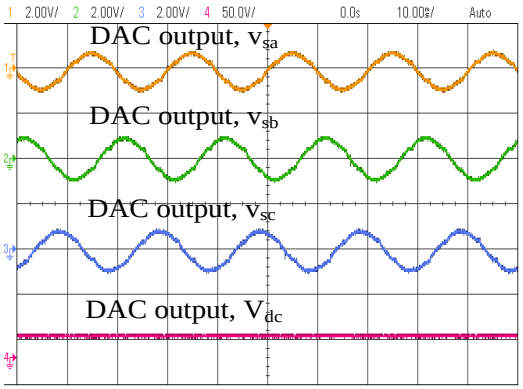


Fig. 3.21 Variation of inductance value with current

interfacing inductor. This result shows variation of inductor value with the output current of compensator. It is observed from this result that variation in inductance is from 2.95mH to 3.08mH, while variation in current is 1A to 9A. Small variation in inductance value is observed in the operating current range.

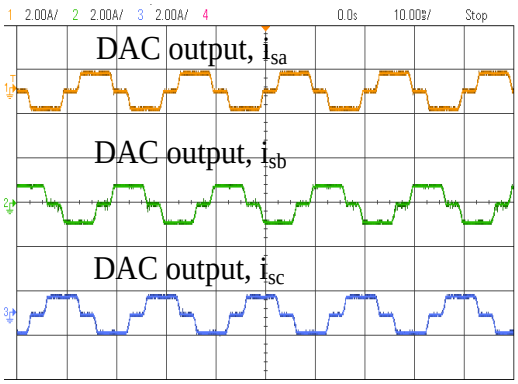
3.6.3.6 Implementation Using DSP-dSPACE 1104

The outputs from voltage and current sensor circuits are given inputs to the ADC channels of DSP (dSPACE 1104 R&D controller board). These signals can be observed with the help of DAC channels of DSP as shown in Fig. 3.22. Fig. 3.22(a) shows waveforms of PCC voltages (v_{sa}, v_{sb} and v_{sc}) and DC bus voltage (V_{dc}) from DAC channels of DSP-dSPACE. Figs. 3.22(b) and (c) show waveforms of supply currents (i_{sa}, i_{sb} and i_{sc}) and load currents (i_{la}, i_{lb} and i_{lc}) from



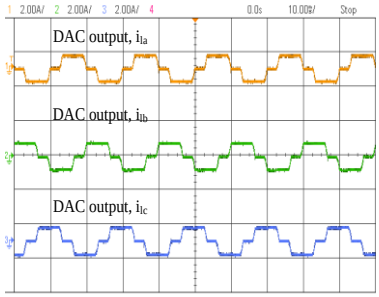
Ch. 1, 2, 3: 2V/div, Ch. 4: 50V/div, Time axis-10ms/div

(a)



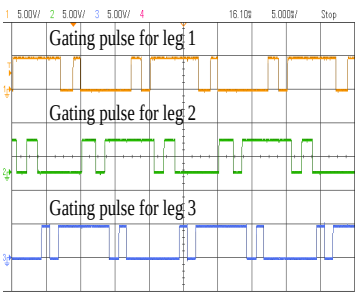
Ch. 1, 2, 3: 2A/div, Time axis-10ms/div

(b)



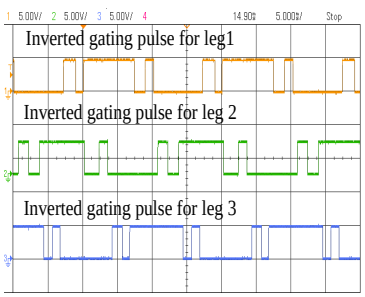
Ch. 1, 2, 3: 2A/div, Time axis-10ms/div

(c)



Ch. 1, 2, 3: 5V/div, Time axis-5ms/div

(d)



Ch. 1, 2, 3: 5V/div, Time axis-5ms/div

(e)

Fig. 3.22 Output signals from DAC channels and PWM port of DSP-dSPACE

DAC channels of DSP-dSPACE. These signals are scaled up and given input to the control algorithm for estimation of reference supply currents. The gating pulses for IGBTs of VSC from PWM current controller are shown in Figs. 3.22(d) and (e). These pulses are given input to the gating circuit for amplification and amplified pulses are used to control three phase VSC.

3.7 CONCLUSIONS

The three phase DSTATCOM has been designed and developed in the laboratory for real time validation. The design and selection of different components of DSTATCOM such as VSC, DC bus capacitance, interfacing inductors, ripple filters and rating of IGBTs have been presented. Hall effect voltage and current sensors with appropriate buffer circuitry have been developed for laboratory prototype. Gating circuit has been developed for amplification of gating pulses from PWM current controller of DSP-dSPACE. Interfacing inductors and ripple filters have also been developed and fixed at their designed values. The simulation model of control algorithm has been implemented with the help of DSP (dSPACE 1104) for estimation of reference supply currents. The developed components of DSTATCOM such as voltage sensors, current sensors, gating circuit and interfacing inductor have been tested. The ADC channels, DAC channels and PWM port of DSP-dSPACE have also been tested for proper operation of developed DSTATCOM prototype.

CHAPTER-IV
CLASSIFICATIONS OF CONTROL ALGORITHMS FOR DSTATCOM

4.1 GENERAL

Performance of the DSTATCOM depends upon the type of control algorithm used to estimate the reference currents. This chapter deals with classifications of the control algorithms for control of DSTATCOM. The control algorithms have been classified into four categories such as classical control algorithms, adaptive theory based control algorithms, recursive theory based control algorithms and artificial intelligence based control algorithms. The PCC voltages, supply currents, load currents and DC bus voltage of VSC used as DSTATCOM are sensed and used in different categories of control algorithms for estimation of reference supply currents. Various features of DSTATCOM such as harmonics elimination, reactive power compensation and load balancing in power factor correction (PFC) and voltage regulation modes are performed with these control algorithms. This chapter also presents mathematical modeling, modeling and simulation, DSP based implementation and performance of the conventional control algorithms for the DSTATCOM. These algorithms are developed in MATLAB using SIMULINK and Sim Power System (SPS) tool boxes. Experimental verification of these algorithms is performed on a developed prototype in the laboratory using voltage source converter (VSC) as a DSTATCOM and DSP (dSPACE 1104 R&D controller board) as controller.

4.2 CONFIGURATION AND OPERATING PRINCIPLE OF DSTATCOM

The DSTATCOM is a shunt connected device where IGBTs based voltage source converter (VSC) is used. Fig. 4.1 shows the schematic diagram of VSC based DSTATCOM. A three-phase, AC mains with grid impedance, shown using series R_s-L_s branch, feeds a three phase linear/ nonlinear load. The DSTATCOM is designed using three-leg voltage source converter

(VSC) which uses six insulated gate bipolar transistors (IGBTs) with anti-parallel diodes and DC link capacitor (C_{dc}) at DC side. Interfacing inductors (L_f) are used at the AC side of VSC, which couple the VSC to the grid. High frequency switching noise generated by switching of IGBTs of VSC is reduced with the help of series connected capacitive (C_f) and resistive (R_f) elements at the point of common coupling (PCC). The nonlinear load is represented as uncontrolled bridge rectifier with series R-L branch. The voltages at PCC (v_{sa} and v_{sb}), supply currents (i_{sa}, and i_{sb}), load currents (i_{la}, i_{lb} and i_{lc}) and DC bus voltage (V_{dc}) of VSC are sensed and given to the DSP. These signals are processed by the DSP to generate appropriate switching pulses for three phase VSC.

A hardware prototype of the system is implemented in the laboratory using DSP (dSPACE 1104 R&D controller board). Hall Effect voltage and current sensors are used to sense real time

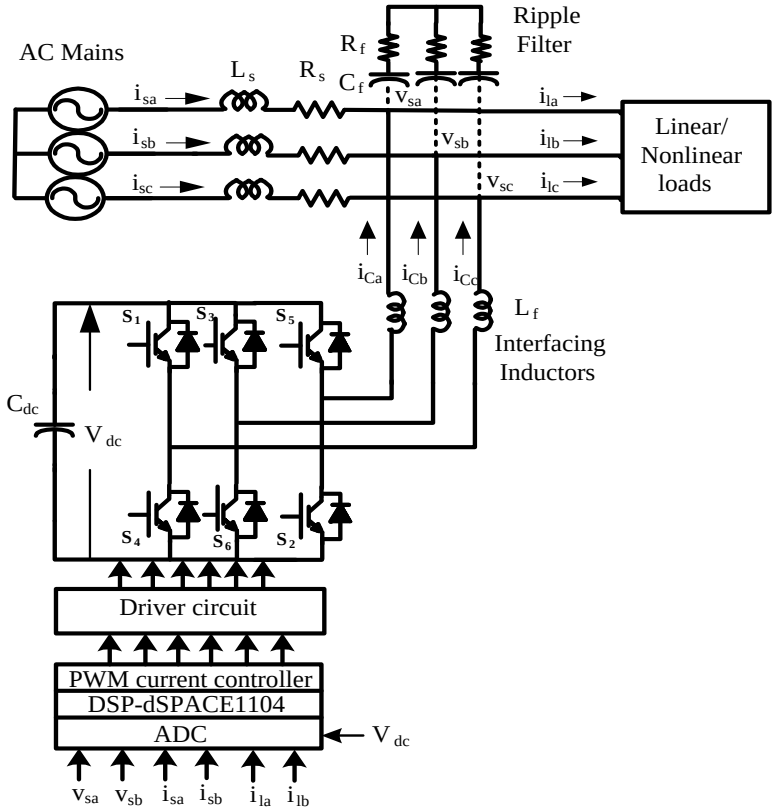


Fig. 4.1 Schematic diagram of the DSTATCOM

feedback signals. The design of sensor circuitry and various components of DSTATCOM are same as given in section 3.6. Switching pulses generated by DSP are used to derive three phase VSC, which generates compensator currents (i_{Ca}, i_{Cb} and i_{Cc}).

4.3 REQUIRMENT OF CONTROL ALGORITHMS IN DSTATCOM

The control algorithms required for DSTATCOM are used to estimate the reference supply currents. The PCC voltages, supply currents, load currents and self-sustained DC bus voltage of VSC are sensed and given input to the control algorithm. These input signals are processed in the control algorithm and reference supply currents are estimated. The estimated reference supply currents are compared with the sensed supply currents and generated currents errors are used to drive PWM current controller, which generates switching pulses for IGBTs of three phase VSC used as a DSTATCOM.

4.4 CLASSIFICATION OF CONTROL ALGORITHMS

This section presents classification of control algorithms for control of the DSTATCOM. These control algorithms are used to estimate the three phase reference supply currents. These control algorithms are mainly divided into four parts such as conventional control algorithms, adaptive theory based control algorithms, recursive theory based control algorithms and artificial intelligence based control algorithms. The detailed description of these control algorithms is given as follows.

4.4.1 Conventional Control Algorithms

The control algorithms investigated under this category are based on power balance theory, instantaneous reactive power theory, conductance based and symmetrical component theory. The

performance of these control algorithms is tested through simulation and implementation on the prototype developed in the laboratory. System performance is studied in power factor correction (PFC) and voltage regulation modes under nonlinear loads. These algorithms are already developed in various literature for UPF operation. Here these algorithms are extended for voltage regulation operation also. The voltage regulation is required in various isolated power generation systems such as isolated diesel generator, isolated micro hydro, biogas and biomass. It is also necessary in distributed generation system, when the system is in islanding mode. These algorithms are tested on the developed DSTATCOM system and their performances are compared with the newly developed control algorithms presented in the following sections.

4.4.2 Adaptive Theory Based Control Algorithms

The adaptive theory based control approach provides self-adjustment of controller parameters in real time to achieve desired performance in steady state and dynamic load conditions. The control algorithms investigated under this category include Wiener filter, fixed step size least mean square (FSSLMS), variable step size least mean square (VSSLMS). Different variations of VSSLMS are studied, tested and compared to control DSTATCOM. The performance of these control algorithms is verified using MATLAB based Simulink models which are also implemented experimentally in PFC and voltage regulation modes of DSTATCOM under nonlinear loads.

4.4.3 Recursive Theory Based Control Algorithms

In the recursive techniques, computation starts with initial conditions and the information contained in new data samples is used to update the old estimated values. The control algorithms investigated under this category are based on recursive theory and include algorithms such as variable forgetting factor recursive least mean square (VFFRLS), variable forgetting factor based

recursive inverse (VFFRI) and immune feedback principle for the control of three phase DSTATCOM. These algorithms are tested through simulation and implementation in PFC and voltage regulation modes of DSTATCOM under nonlinear loads.

4.4.4 Artificial Intelligence Based Control Algorithms

Artificial intelligence based control algorithms work on the principle of human intelligence to achieve a specific task for which they are designed. These control algorithms have the capability of learning, self-organizing or self-adapting. The control algorithms investigated under this category are based on intelligent techniques such as fuzzy logic, adaptive neuro fuzzy inference system (ANFIS), real time recurrent learning (RTRL) and ANFIS-LMS for the control of three phase DSTATCOM. The performance of these algorithms is studied using simulation results and test results in PFC and voltage regulation modes under balance/unbalanced nonlinear loads have been obtained.

4.5 BASIC PRINCIPLE AND MATHEMATICAL FORMULATION OF CONVENTIONAL CONTROL ALGORITHHMS

This section presents the basic principle and mathematical formulation of conventional control algorithms. The control algorithm discussed under this categories are based on power balance theory, instantaneous reactive power theory, conductance and instantaneous symmetrical component theory. The detailed description and mathematical formulation of these conventional control algorithms are discussed as follows.

4.5.1 Power Balance Theory Based Control Algorithm [121-125]

The power balance theory based control algorithm is used to generate reference supply currents. This section is divided into three parts. The first part presents the estimation of active power components of reference supply currents. The second part deals with the estimation of reactive

power components of reference supply currents and the estimation of reference supply currents along with generation of switching pulses is presented in the third part.

4.5.1.1 Estimation of Fundamental Active Power Components of Reference Supply Currents Using Power Balance Theory Based Control Algorithm

Fig. 4.2 shows block diagram of power balance based control algorithm. The phase voltages (v_{sa}, v_{sb} and v_{sc}) at PCC are sensed and their amplitude (V_t) is calculated as,

$$V_t = \sqrt{\frac{2}{3}(v_{sa}^2 + v_{sb}^2 + v_{sc}^2)} \tag{4.1}$$

Using PCC voltage magnitude, the unit inphase components are calculated as,

$$u_{pa} = v_{sa}/V_t;\ u_{pb} = v_{sb}/V_t;\ \text{and}\ u_{pc} = v_{sc}/V_t \tag{4.2}$$

The voltage at DC bus (V_{dc}) of the VSC used as a DSTATCOM is sensed and subtracted from the reference DC bus voltage (V_{dc}^*) for generation of error signal (V_{de}). The error signal is passed through a proportional integral (PI) controller. The output of PI controller (i_{pdc}) regulates the DC bus voltage at reference value and also meets VSC losses. The PI controller output at n^{th} sampling instant is given as,

$$i_{pdc}(n) = i_{pdc}(n-1) + k_{pd}\big(v_{de}(n) - v_{de}(n-1)\big) + k_{id}\big(v_{de}(n)\big) \tag{4.3}$$

where k_{pd} and k_{id} are proportional and integral gains of DC bus voltage PI controller.

The instantaneous active power (p_l) of load is calculated as,

$$p_l = (v_{sa}i_{la} + v_{sb}i_{lb} + v_{sc}i_{lc}) = p_{ldc} + p_{lac} \tag{4.4}$$

The active power component of load contains DC as well as AC components. This is passed through a low pass filter (LPF) to filter out AC ripple components and the DC fundamental

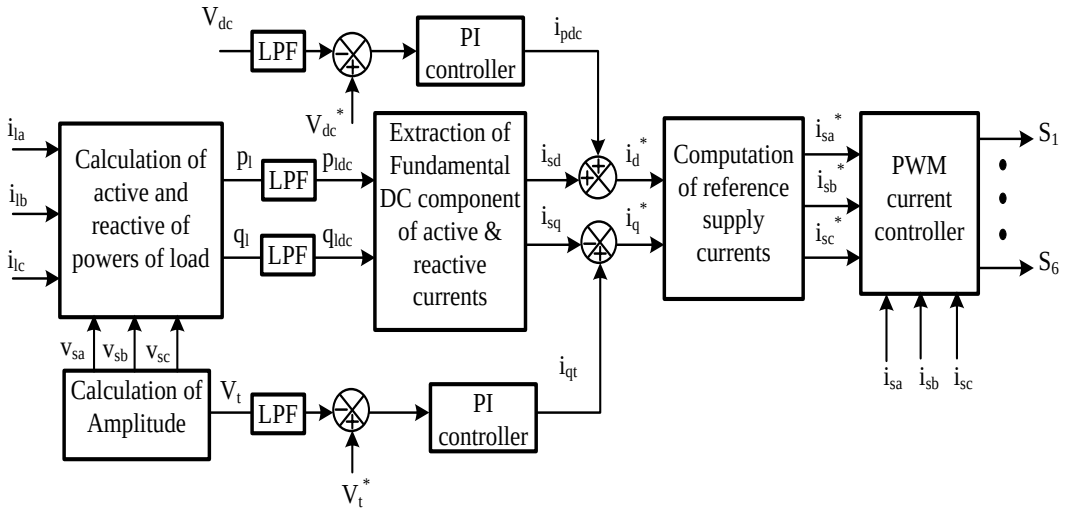


Fig. 4.2 Block diagram of PBT based control algorithm [125]

active power component of load (p_{ldc}) is extracted. The fundamental active power component of load current (i_{sd}) is calculated as,

$$i_{sd} = \left(\frac{2}{3}\right)\left(\frac{p_{ldc}}{V_t}\right) \tag{4.5}$$

Reference active power component of load current (i_d^*) is computed by adding output of DC bus PI controller (i_{pdc}) and active power component of load current (i_{sd}) as,

$$i_d^* = i_{pdc} + i_{sd} \tag{4.6}$$

Active power components of reference supply currents (i_{sa}^*, i_{sb}^* and i_{sc}^*) are estimated from unit inphase templates (u_{pa}, u_{pb} and u_{pc}) and reference active power component (i_d^*) of load current as,

$$i_{pa}^* = i_d^* u_{pa},\ i_{pb}^* = i_d^* u_{pb} \text{ and } i_{pc}^* = i_d^* u_{pc} \tag{4.7}$$

These active power components of reference supply currents are used to estimate reference supply currents given as follows.

4.5.1.2 Estimation of Fundamental Reactive Power Components of Reference Supply Currents Using Power Balance Theory Based Control Algorithm

The unit quadrature vectors of PCC voltages are calculated from unit inphase voltages (u_{pa}, u_{pb} and u_{pc}) as,

$$u_{qa} = -u_{pb}/\sqrt{3} + u_{pc}/\sqrt{3} \tag{4.8}$$

$$u_{qb} = \sqrt{3}\,u_{pa}/2 + (u_{pb} - u_{pc})/2\sqrt{3} \tag{4.9}$$

$$u_{qc} = -\sqrt{3}\,u_{pa}/2 + (u_{pb} - u_{pc})/2\sqrt{3} \tag{4.10}$$

The voltage regulation using DSTATCOM can be performed by using another PI controller over the terminal voltage. The error (v_{te}) between amplitude of PCC voltage (V_t) and its reference quantity (V_t^*) is calculated. The error is passed through PI controller and output (i_{qt}) can be computed at n^{th} sampling instance as,

$$i_{qt}(n) = i_{qt}(n-1) + k_{pq}\big(v_{te}(n) - v_{te}(n-1)\big) + k_{iq}\big(v_{te}(n)\big) \tag{4.11}$$

where k_{pq} and k_{iq} are proportional and integral gains for AC bus PI controller.

The instantaneous reactive power component (q_l) of load is calculated a,

$$q_l = \left(\frac{1}{3}\right)\{(v_{sa} - v_{sb})i_{la} + (v_{sb} - v_{sc})i_{lb} + (v_{sc} - v_{sa})i_{lc}\} = q_{ldc} + q_{lac} \tag{4.12}$$

The DC fundamental component of load reactive power (q_{ldc}) is extracted after instantaneous reactive power component of load (q_l) is passed through LPF. The amplitude of fundamental active power component of load current is given as,

$$i_{sq} = \left(\frac{2}{3}\right)\left(\frac{q_{ldc}}{V_t}\right) \tag{4.13}$$

Reference reactive power component of load current (i_q^*) is computed by output of AC bus voltage PI controller (i_{qt}) and reactive power component of load current (i_{sq}) as,

$$i_q^* = i_{qt} - i_{sq} \tag{4.14}$$

The fundamental reactive power component of reference supply currents (i_{qa}^*, i_{qb}^* and i_{qc}^*) are estimated from the output unit quadrature templates (u_{qa}, u_{qb} and u_{qc}) and reference reactive power component (i_q^*) as,

$$i_{qa}^* = i_q^* u_{qa},\ i_{qb}^* = i_q^* u_{qb} \text{ and } i_{qc}^* = i_q^* u_{qc} \tag{4.15}$$

These reactive components of reference supply currents are used with active reference supply currents to estimate reference supply currents given as follows.

4.5.1.3 Generation of Reference Supply Currents and Switching Pulses for Three Phase VSC

Reference supply currents (i_{sa}^*, $i_{sb}^*$and i_{sc}^*) for the three phases are determined by the addition of respective active and reactive supply currents calculated in Eqn. (4.7) and Eqn. (4.15) as,

$$i_{sa}^* = i_{pa}^* + i_{qa}^*,\ i_{sb}^* = i_{pb}^* + i_{qb}^* \text{ and } i_{sc}^* = i_{pc}^* + i_{qc}^* \tag{4.16}$$

These reference supply currents (i_{sa}^*, $i_{sb}^*$and i_{sc}^*) are compared with the sensed supply currents (i_{sa}, i_{sb} and i_{sc}) and current errors (i_{sae}, i_{sbe} and i_{sce}) are generated. These current errors are passed through PWM current controller for generation of switching pulses for the three phase VSC.

4.5.2 Instantaneous Reactive Power Theory Based Control Algorithm [126-131]

This section presents the mathematical formulation of instantaneous reactive power theory (IRPT) based control algorithm. The IRPT based control algorithm is used to estimate the reference supply currents. The active and reactive power components of loads are calculated

using the PCC voltages and load currents and transforming them from three-phase to two-phase using Clark's transformation. The detailed description of IRPT based control algorithm is given as follows.

4.5.2.1 Estimation of Reference Supply Currents From IRPT Based Control Algorithm

Fig. 4.3 shows the block diagram of IRPT based control algorithm. Three phase PCC voltages (v_{sa}, v_{sb} and v_{sc}) are sensed and their amplitude is calculated same as given in Eqn. (4.1) of section 4.5.1. The unit inphase templates are calculated from the PCC voltages and their magnitudes are same as calculated in Eqn. (4.2) of section 4.5.1. The voltage at DC bus (V_{dc}) of VSC is sensed and compared with the reference DC bus voltage (V_{dc}^{*}), thus the generated error is passed through PI controller. The output (p_{loss}) of DC bus PI controller is same as given in Eqn. (4.3) of section 4.5.1.

The instantaneous active and reactive powers are calculated using the PCC voltages (v_{sa}, v_{sb} and v_{sc}) and load currents (i_{la}, i_{lb} and i_{lc}) by using three to two phase transformation (a-b-c to α-β) as,

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{2/3} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix} \tag{4.17}$$

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \sqrt{2/3} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i_{la} \\ i_{lb} \\ i_{lc} \end{bmatrix} \tag{4.18}$$

These transformed voltages (v_α, v_β) and currents (i_α, i_β), instantaneous active (p_l) and reactive (q_l) power are computed as,

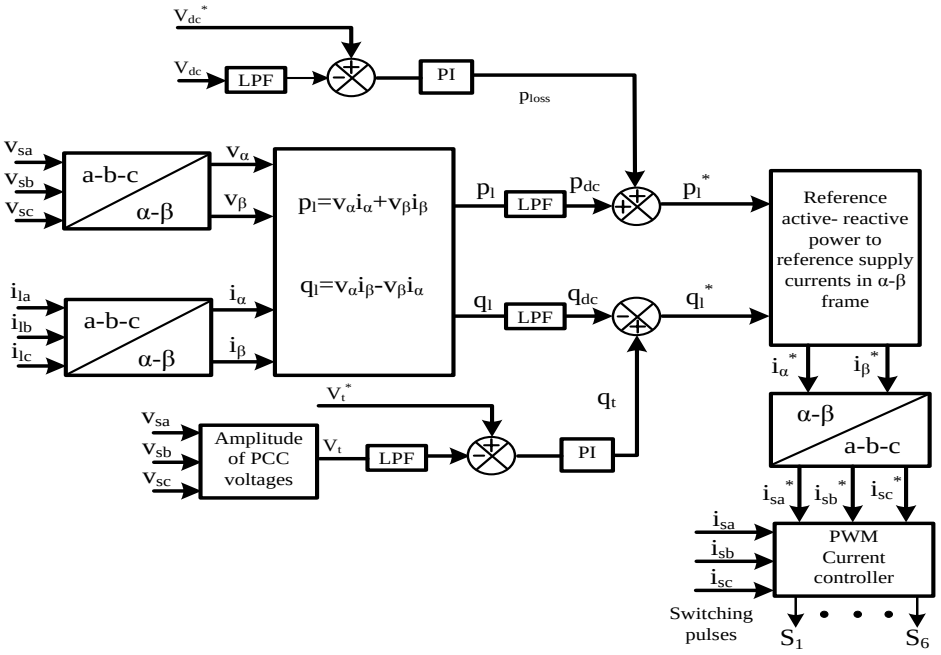


Fig. 4.3 Block diagram of IRPT based control algorithm [130]

$$\begin{bmatrix} p_l \\ q_l \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{4.19}$$

The active (p_l) and reactive (q_l) power of load contains AC as well as DC components.

$$p_l = p_{ac} + p_{dc} \tag{4.20}$$

$$q_l = q_{ac} + q_{dc} \tag{4.21}$$

The AC components (p_{ac} and q_{ac}) are considered distortions and the DC components (p_{dc} and q_{dc}) are considered as the fundamental active and reactive powers. The fundamental active and reactive power components (p_{dc} and q_{dc}) of the load are extracted by using low pass filters (LPFs).

Reference active power component (p_l^*) is calculated by adding output of DC bus PI controller (p_{loss}) and fundamental active power component of load (p_{dc}) as,

$$p_l^* = p_{loss} + p_{dc} \tag{4.22}$$

Unit quadrature templates (u_{qa}, u_{qb} and u_{qc}) are calculated from unit inphase templates (u_{pa}, u_{pb} and u_{pc}) same as given in Eqns. (4.8), (4.9) and (4.10) of section 4.5.1. The magnitude of PCC voltages are calculated as given in Eqn. (4.1) and compared to reference PCC voltage magnitude (V_t^*). Thus the generated error signal (v_{te}) is passed through PI controller whose output (q_t) is the same as given in section 4.5.1.

The reference reactive power component (q_l^*) is calculated by using output of AC bus PI controller (q_t) and fundamental reactive power component of load (q_{dc}) as,

$$q_l^* = q_t - q_{dc} \tag{4.23}$$

Reference reactive power component (q_l^*) is calculated by adding output of DC bus PI controller (p_{loss}) and fundamental active power component of load (p_{dc}) as,

Reference currents in α-β frame (i_α^* and i_β^*) are estimated as,

$$\begin{bmatrix} i_\alpha^* \\ i_\beta^* \end{bmatrix} = \frac{1}{v_\alpha^2 + v_\beta^2} \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \begin{bmatrix} p_l^* \\ q_l^* \end{bmatrix} \tag{4.24}$$

These reference currents in α-β frame (i_α^* and i_β^*) are used to estimate reference supply currents as,

$$\begin{bmatrix} i_{sa}^* \\ i_{sb}^* \\ i_{sc}^* \end{bmatrix} = \sqrt{2/3} \begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ -1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i_\alpha^* \\ i_\beta^* \end{bmatrix} \tag{4.25}$$

These reference supply currents (i_{sa}^*, i_{sb}^* and i_{sc}^*) are used along with sensed supply currents to generate switching pulses given as follows.

4.5.2.2 Generation of Switching Pulses for Three Phase VSC

The reference supply currents (i_{sa}^*, $i_{sb}^*$and i_{sc}^*) estimated from Eqn. (4.25) are compared with sensed supply currents (i_{sa}, i_{sb} and i_{sc}) and current errors (i_{sae}, i_{sbe} and i_{sce}) are generated. These current errors are given to PWM current controller, which generates switching pulses for three phase VSC used as DSTATCOM.

4.5.3 Conductance Based Control Algorithm [132-135]

The conductance based control algorithm is used to estimate reference supply currents, which are used along with sensed supply currents to generate switching pulses. This section is divided into three parts. The first part presents estimation of fundamental active components of reference supply currents. The second part deals with estimation of fundamental reactive components of reference supply currents and third part presents generation of switching pulses for three phase VSC used as a DSTATCOM.

4.5.3.1 Estimation of Fundamental Active Components of Reference Supply Currents from Conductance Based Control Algorithm

Fig. 4.4 shows the block diagram of the conductance based control algorithm. In this algorithm the PCC voltages (v_{sa}, v_{sb} and v_{sc}) are sensed and amplitude (V_t) is calculated same as given in Eqn. (4.1) of section 4.5.1. Unit inphase templates (u_{pa}, u_{pb} and u_{pc}) are computed by using (V_t) same as given in Eqn. 4.2 of section 4.5.1. Voltage at DC bus (V_{dc}) is sensed and compared with reference DC bus voltage (V_{dc}^*). Thus the generated error (v_{de}) is passed through DC bus voltage PI controller. The output of DC bus PI controller (P_d) is same as given in section 4.5.1.

The corresponding conductance (G_d) is computed as,

$$G_d = {P_d}\Big/{\{V_t^2(u_{pa}^2 + u_{pb}^2 + u_{pc}^2)\}} \tag{4.26}$$

The instantaneous active power of load (P_l) is calculated as,

$$P_l = \{V_t(u_{pa}i_{la} + u_{pb}i_{lb} + u_{pc}i_{lc})\} = P_{ldc} + P_{lac} \tag{4.27}$$

The calculated load instantaneous active power contains fundamental DC (P_{ldc}) as well as AC component (P_{lac}). Therefore LPF is used to extract fundamental DC component of instantaneous active power of load.

The corresponding conductance of the fundamental load current is computed as,

$$G_l = {P_{ldc}}/{\{V_t^2(u_{pa}^2 + u_{pb}^2 + u_{pc}^2)\}} \tag{4.28}$$

The reference conductance (G_{sp}) of reference supply current is estimated by adding G_d and G_l

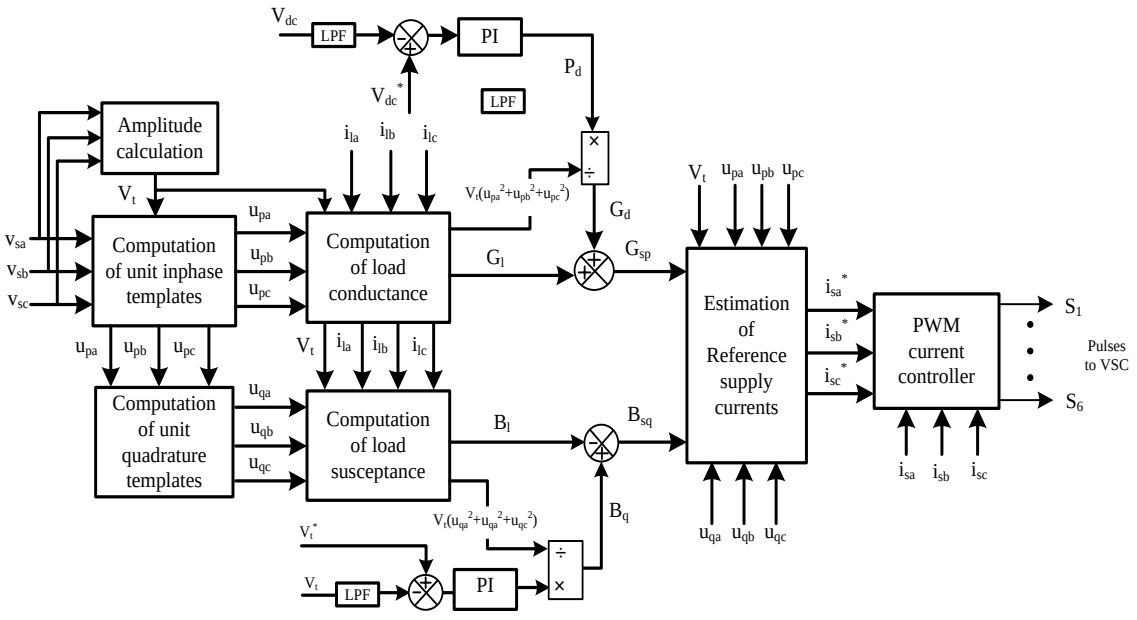


Fig. 4.4 Block diagram of conductance based control algorithm [132]

given as,

$$G_{sp} = G_d + G_l \tag{4.29}$$

Fundamental active component of reference supply currents are estimated as,

$$i_{pa}^{*} = G_{sp} V_t u_{pa},\ i_{pb}^{*} = G_{sp} V_t u_{pb} \text{ and } i_{pc}^{*} = G_{sp} V_t u_{pc} \tag{4.30}$$

These fundamental active components of reference supply current are used to estimate reference supply currents given as follows.

4.5.3.2 Estimation of Fundamental Reactive Components of Reference Supply Currents From Conductance Based Control Algorithm

The unit quadrature (u_{qa}, u_{qb} and u_{qc}) components are calculated from unit in phase templates same as given in Eqns. (4.8), (4.9) and (4.10) of section 4.5.1. The magnitude of PCC voltages are calculated as given in Eqn. (4.1) and compared to reference PCC voltage magnitude (V_t^*). Thus the generated error signal (v_{te}) is passed through PI controller whose output (Q_t) is same as given in section 4.5.1.

The corresponding susceptance (B_q) is given as,

$$B_q = {Q_t}\Big/{\{V_t^2(u_{qa}^2 + u_{qb}^2 + u_{qc}^2)\}} \tag{4.31}$$

The instantaneous reactive power of the load (Q_l) is calculated as,

$$Q_l = -\{V_t(i_{la}u_{qa} + i_{lb}u_{qb} + i_{lc}u_{qc})\} = Q_{ldc} + Q_{lac} \tag{4.32}$$

The instantaneous reactive power consists of fundamental DC and oscillating AC components. The fundamental DC component (Q_{ldc}) of load is extracted with the help of LPF.

The susceptance of fundamental load is calculated as,

$$B_l = {Q_{ldc}}\Big/{\{V_t^2(u_{qa}^2 + u_{qb}^2 + u_{qc}^2)\}} \tag{4.33}$$

The reference susceptance corresponding to reference supply current is estimated as,

$$B_{sq} = B_q - B_l \tag{4.34}$$

The fundamental components of reactive reference supply current are estimated as,

$$i_{qa}^* = B_{sq} V_t u_{qa},\ i_{qb}^* = B_{sq} V_t u_{qb} \text{ and } i_{qc}^* = B_{sq} V_t u_{qc} \tag{4.35}$$

These components are used with fundamental active reference supply current to estimate reference supply currents given as follows.

4.5.3.2 Generation of reference supply currents and Switching Pulses

The reference supply currents (i_{sa}^*, i_{sb}^* and i_{sc}^*) are estimated by adding active and reactive components of reference supply currents given as,

$$i_{sa}^* = i_{pa}^* + i_{qa}^*,\ i_{sb}^* = i_{pb}^* + i_{qb}^* \text{ and } i_{sc}^* = i_{pc}^* + i_{qc}^* \tag{4.36}$$

The reference supply currents (i_{sa}^*, $i_{sb}^*$and i_{sc}^*) estimated from Eqn. (4.36) are compared with sensed supply currents (i_{sa}, i_{sb} and i_{sc}) and current errors (i_{sae}, i_{sbe} and i_{sce}) are generated. These current errors are given to PWM current controller, which generates switching pulses for three phase VSC used as DSTATCOM.

4.5.4 Instantaneous Symmetrical Component Theory Based Control Algorithm [136-142]

The instantaneous symmetrical component theory (ISCT) based control algorithm is used to estimate reference supply currents. The input signals such as PCC voltages, load currents, supply currents and DC bus voltage are sensed and feedback to the control algorithm. The detail description and mathematical formulation of the control algorithm are given as follows.

4.5.4.1 Estimation of Reference Supply Currents from ISCT Based Control Algorithm

Fig. 4.5 shows the block diagram of the control algorithm. PCC voltages (v_{sa}, v_{sb} and v_{sc}) are sensed and their amplitude is calculated same as given in Eqn. (4.1) of section 4.5.1. The voltage at DC bus (V_{dc}) of VSC is sensed and compared by reference DC bus voltage (V_{dc}^{*}), thus the generated error is passed through PI controller. The output of DC bus PI controller (p_{loss}) is same as given in section 4.5.1.

The instantaneous active power (P_l) is obtained from PCC voltages and load currents (i_{la}, i_{lb} and i_{lc}) as,

$$P_l = v_{sa}i_{la} + v_{sb}i_{lb} + v_{sc}i_{lc} \tag{4.37}$$

The instantaneous active power consists pulsating AC power and fundamental DC power (P_{dc}). The fundamental DC power is extracted after passing instantaneous active power through LPF.

Reference active power (P_{ref}) is obtained by adding output of DC bus PI controller (P_{loss}) and fundamental DC component instantaneous active power (P_{dc}) as,

$$P_{ref} = P_{loss} + P_{dc} \tag{4.38}$$

If ϕ is the phase difference between PCC voltage and fundamental supply current then the angle β is defined as,

$$\beta = \frac{\tan\phi}{\sqrt{3}} \tag{4.39}$$

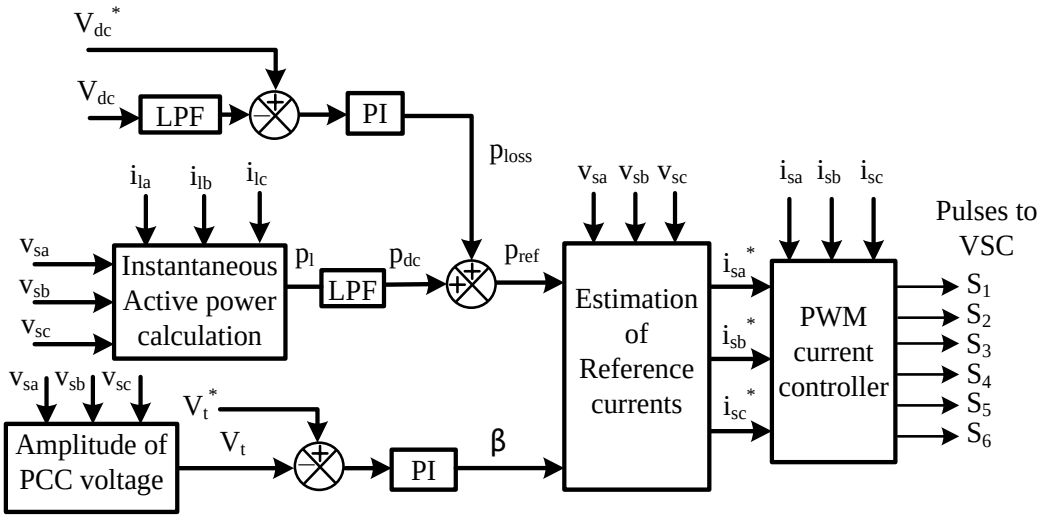


Fig. 4.5 Block diagram of ISCT based control algorithm [138]

Reference supply currents are obtained from PCC voltages, reference active power and angle β as,

$$i_{sa}^{*} = \frac{\{v_{sa}+(v_{sb}-v_{sc})\beta\}}{A} P_{ref} \tag{4.40}$$

$$i_{sb}^{*} = \frac{\{v_{sb}+(v_{sc}-v_{sa})\beta\}}{A} P_{ref} \tag{4.41}$$

$$i_{sc}^{*} = \frac{\{v_{sc}+(v_{sa}-v_{sb})\beta\}}{A} P_{ref} \tag{4.42}$$

where the term A is given as,

$$A = \sum_{i=a,b,c} v_{si}^{2} \tag{4.43}$$

4.5.1.2 Generation of Switching Pulses for Three Phase VSC

The reference supply currents (i_{sa}^{*}, i_{sb}^{*} and i_{sc}^{*}) estimated from Eqn. (4.40) to Eqn. (4.42) are compared with sensed supply currents (i_{sa}, i_{sb} and i_{sc}) and current errors (i_{sae}, i_{sbe} and i_{sce}) are generated. These current errors are given to PWM current controller, which generates switching

pulses for three phase VSC used as DSTATCOM.

4.6 MATLAB BASED MODELING OF CONVENTIONAL CONTROL ALGORITHMS

This section presents MATLAB modeling of conventional control algorithms for control of DSTATCOM. The conventional control algorithms such as power balance theory, instantaneous reactive power theory, conductance based control and instantaneous symmetrical component theories are developed using MATLAB/SIMULINK for estimation of reference supply currents. The detail description of MATLAB based modeling of these control algorithms are given as follows.

4.6.1 Power Balance Theory Based Control Algorithm

Fig. 4.6 shows MATLAB model of power balance theory (PBT) based control algorithm. The simulation study of DSTATCOM with PBT based control algorithm is performed in MATLAB

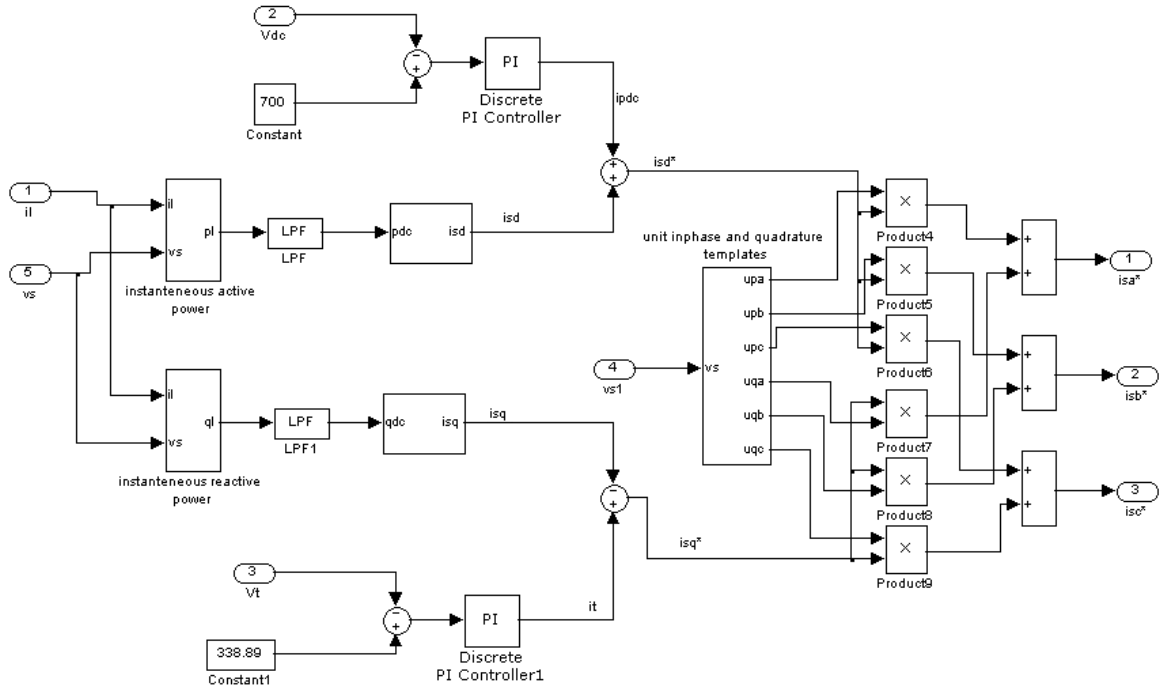


Fig. 4.6 MATLAB based model of PBT based control algorithm

environment using SIMILINK and Sim Power System (SPS) tool box. Inputs to the control algorithm are PCC voltages (v_{sa}, v_{sb} and v_{sc}), supply currents (i_{sa}, i_{sb} and i_{sc}), load currents (i_{la}, i_{lb} and i_{lc}) and self-sustained DC bus voltage (V_{dc}). The control algorithm with these inputs is used to estimate reference supply currents. The reference supply currents are used with sensed supply currents for generation of switching pulses.

4.6.2 Instantaneous Reactive Power Theory Based Control Algorithm

The simulation study of DSTATCOM with IRPT based control algorithm is performed in MATLAB environment using SIMULINK and SPS tool box. Simulation model of control algorithm is used to generate reference supply currents as shown in Fig. 4.7. Inputs to the control algorithm as shown in MATLAB model are PCC voltages (v_{sa}, v_{sb} and v_{sc}), supply currents (i_{sa}, i_{sb} and i_{sc}), load currents (i_{la}, i_{lb} and i_{lc}) and self-sustained DC bus voltage (V_{dc}) for control of DSTATCOM.

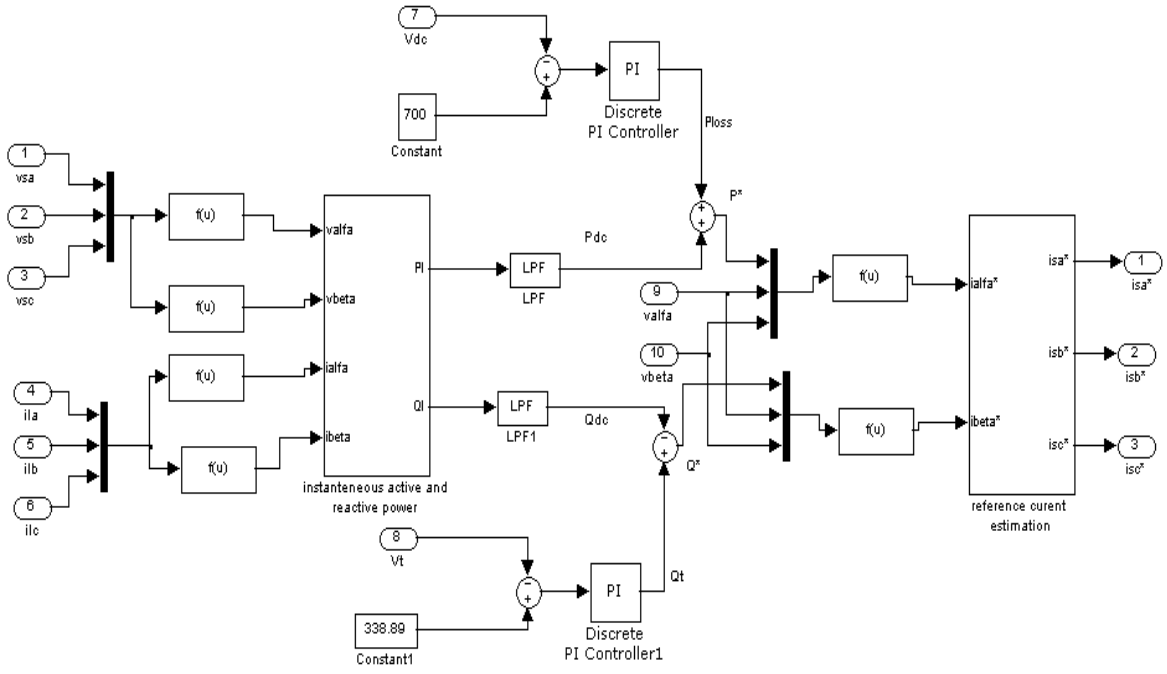


Fig. 4.7 MATLAB based model of IRPT based control algorithm

4.6.3 Conductance Based Control Algorithm

The simulation of conductance based control algorithm for DSTATCOM is developed in MATLAB using SIMULINK and SPS tool box. The Simulink model of the control algorithm is shown in Fig. 4.8, where inputs to the control algorithm are PCC voltages (v_{sa}, v_{sb} and v_{sc}), supply currents (i_{sa}, i_{sb} and i_{sc}), load currents (i_{la}, i_{lb} and i_{lc}) and self-sustained DC bus voltage (V_{dc}). The Simulink model of conductance based control algorithm is used to estimate reference supply current for control of DSTATCOM.

4.6.4 Instantaneous Symmetrical Component Theory Based Control Algorithm

Fig. 4.9 shows the Simulink model of ISCT based control algorithm for control of DSTATCOM. The simulation model of the control algorithm is developed in MATLAB environment using SIMULINK and SPS tool box. The inputs to the control algorithm are PCC

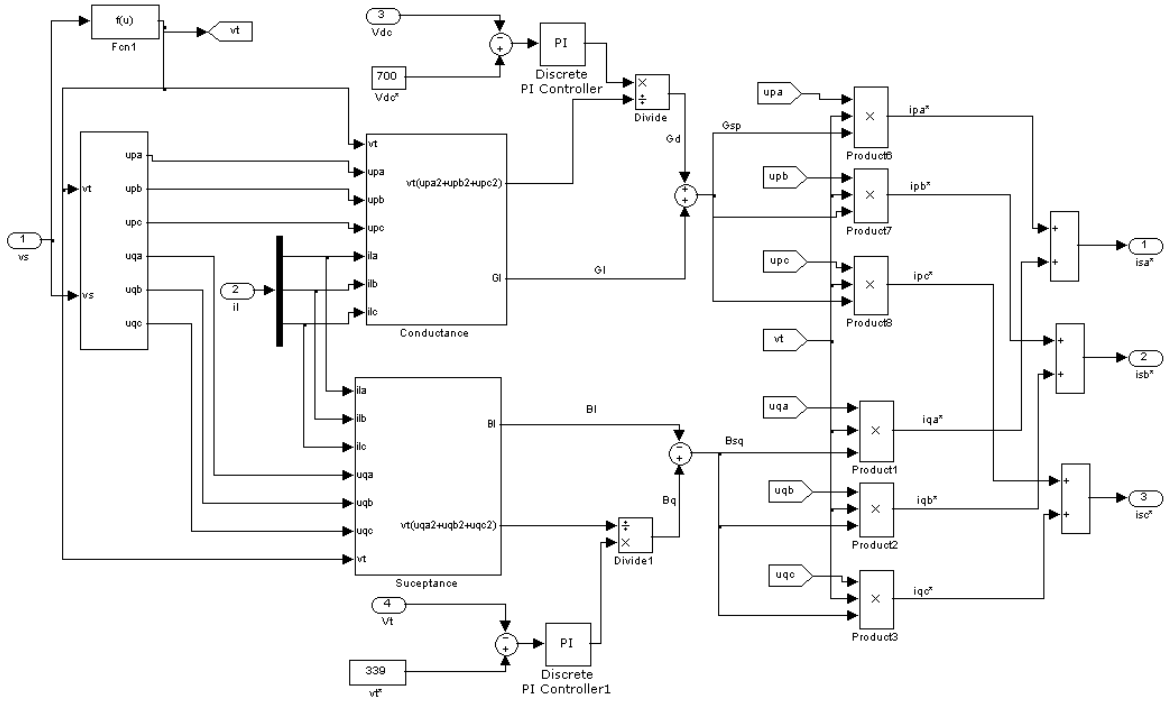


Fig. 4.8 MATLAB based model of conductance based control algorithm

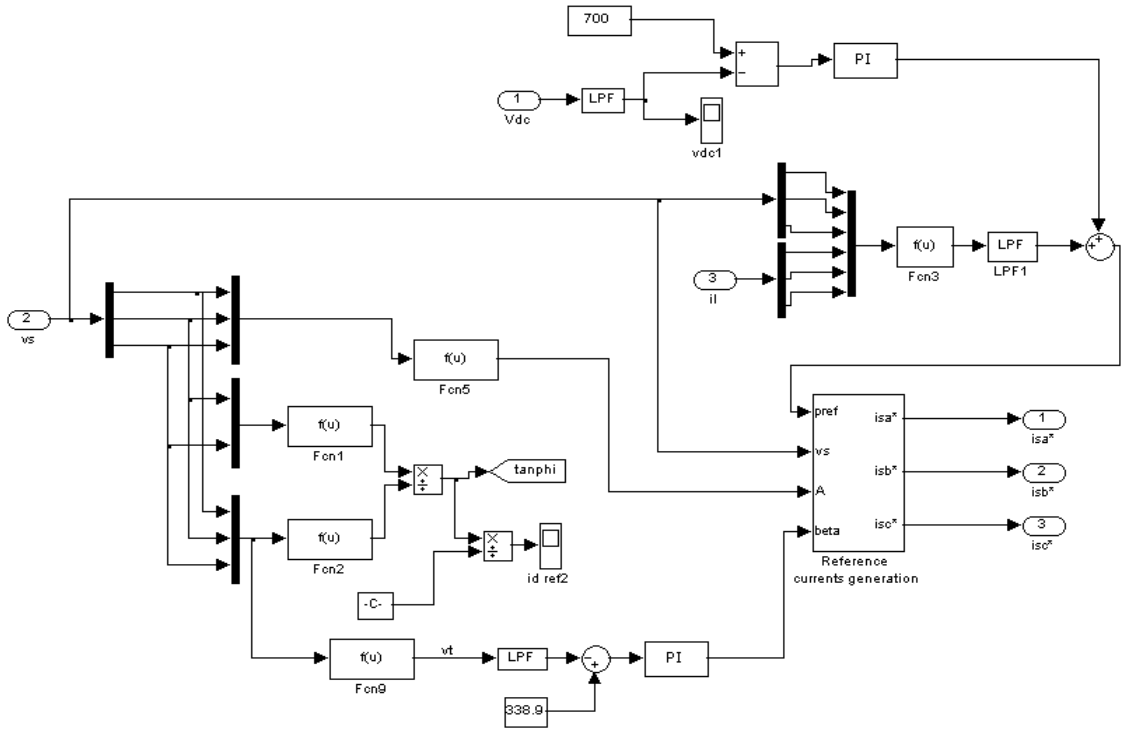


Fig. 4.9 MATLAB based model of ISCT based control algorithm

voltages (v_{sa}, v_{sb} and v_{sc}), supply currents (i_{sa}, i_{sb} and i_{sc}), load currents (i_{la}, i_{lb} and i_{lc}) and self-sustained DC bus voltage (V_{dc}). The control algorithm with these input signals used to estimate reference supply currents and generate switching pulses for three phase VSC.

4.7 DSP IMPLEMENTATION OF CONVENTIONAL CONTROL ALGORITHMS

This section presents DSP (dSPACE 1104 R&D controller board) based implementation of conventional control algorithms. The real time performance of conventional control algorithms such as PBT, IRPT, conductance based and ISCT based control algorithms are tested in developed prototype in the laboratory.

4.7.1 DSP Implementation of Power Balance Theory Based Control Algorithm

The implementation of PBT based control algorithm is implemented in DSP (dSPACE-1104 R&D controller board) used to generate gating pulses for the three phase VSC. The DSP

(dSPACE 1104) is real time controller based on a 603 PowerPC floating-point processor. This includes slave DSP subsystem based on the TMS320F240 digital signal processor. The DSP hardware and software give the facility to generate real time switching pulses from real time signals with the use of SIMULINK model of the control algorithm. The simulation model of PBT based control algorithm used for DSP implementation is given in Fig. 4.10. This shows DSP (dSPACE 1104) based implementation of control algorithm for generating gating pulses for three phase VSC.

The DSP based implementation is mainly divided into three blocks ADC block, scaling of signals block along with control algorithm block and PWM current controller block. Implementations of DC and AC bus PI controllers are shown in Figs. 4.11 and 4.12, respectively. An implementation of pulse width modulation (PWM) switching in DSP-dSPACE using DS 1104SL_DSP_PWM3 block is presented in Fig. 4.13. The solver option used for the implementation is based on the fixed-step type with discrete (no continuous state) solver.

The sampling time (T_s) is selected as 55μs for PBT based control algorithm. The DC bus PI controller proportional and integral gains are calculated using Ziegler-Nichols unit step response algorithm. The tuned values of PI controller gains are selected very close to calculated values.

4.7.2 DSP Based Implementation of IRPT Based Control Algorithm

The IRPT based control algorithm is implemented using DSP (dSPACE 1104 R&D controller board). This controller is used to generate six switching pulses for three phase VSC used as DSTATCOM. The DSP based implementation needs real time signals of PCC voltages, supply currents, load currents and DC bus voltage through appropriate sensors and sensors circuitry. These real time signals are processed by DSP using SIMULINK based control algorithm and six real time switching signals are generated for switching on and off of the six IGBTs of the VSC.

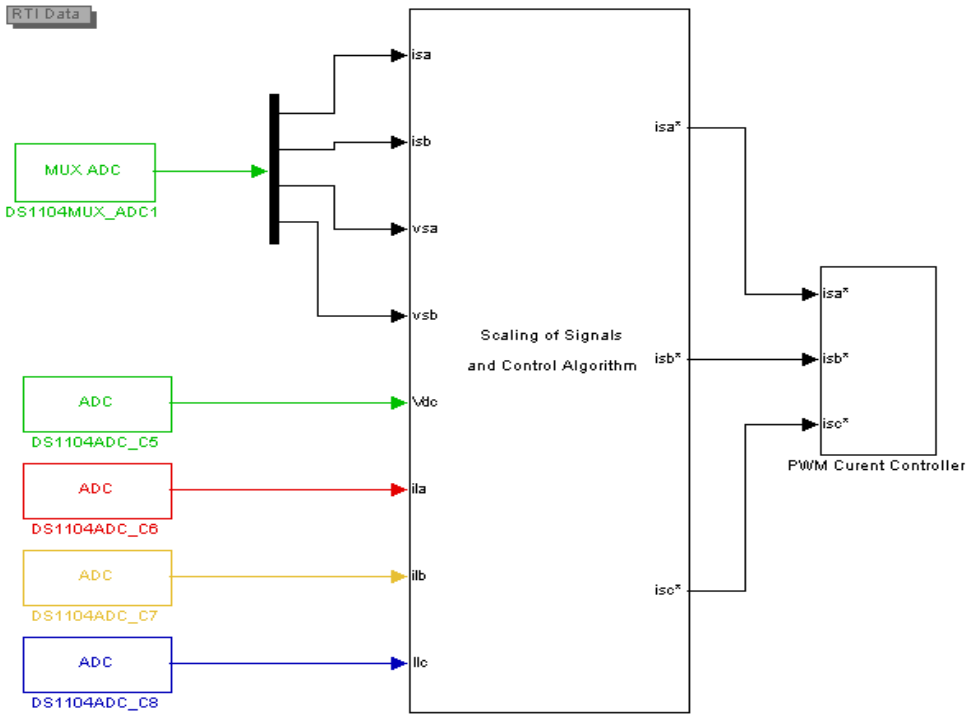


Fig. 4.10 Software for DSP implementation of control for DSTATCOM

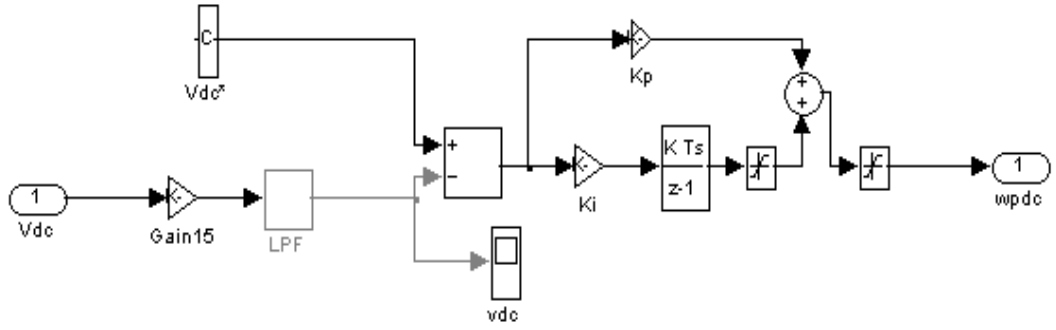


Fig. 4.11 Implementation of DC bus PI controller

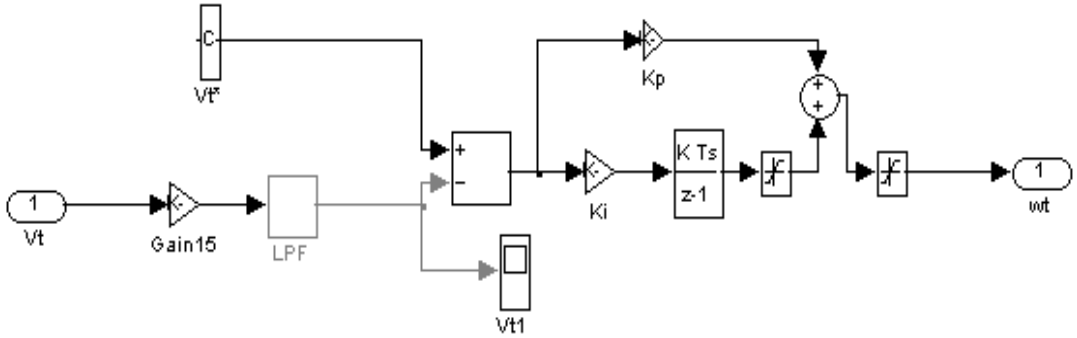


Fig. 4.12 Implementation of AC bus PI controller

The model of IRPT based control algorithm used for real time implementation is same as discussed in simulation study. DSP (dSPACE 1104) based implementation of control algorithm

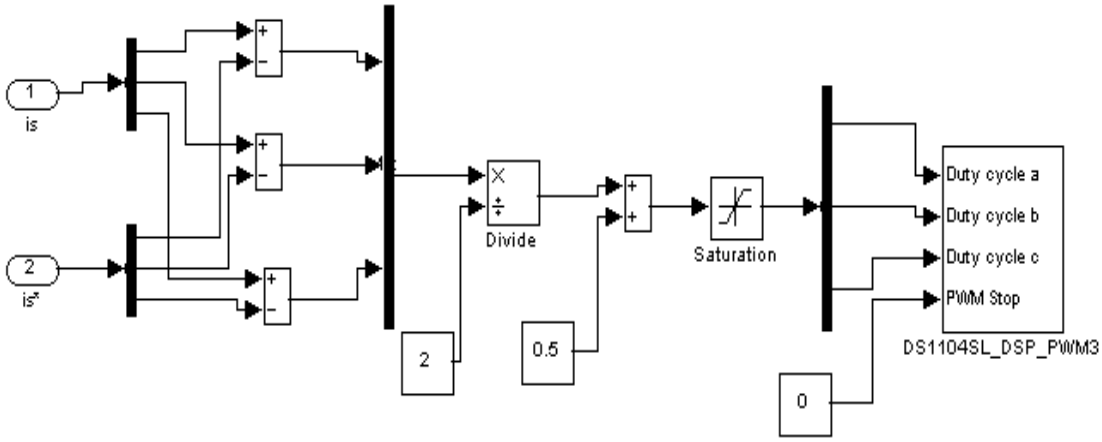


Fig. 4.13 Implementation of PWM current controller

for generating switching pulses of DSTATCOM is same as presented in section 4.7.1. The DSP based implementation is mainly divided into three blocks ADC block, scaling of signals block along with control algorithm block and PWM current controller block. An Implementation of DC bus PI controller and PWM current controller for switching pulse generation are also same as given in section 4.7.1. The IRPT based control algorithm for the control of DSTATCOM takes a sampling time of approximately 55μs. The proportional and integral gains of PI controllers are calculated using standard Ziegler-Nichols unit step response algorithm and the values required in implementation are selected very close to the calculated values.

4.7.3 DSP Based Implementation of Conductance Based Control Algorithm

The implementation of conductance based control algorithm is performed using DSP (dSPACE1104 R&D controller board). The DSP controller board requires real time signals viz. PCC voltages, supply currents and load currents, which are sensed from appropriate sensors and buffer circuitry. The sensed signals are then processed by the MATLAB based control algorithm implemented on dSPACE 1104 controller board. After processing, this controller is used to generate switching pulses for the three phase VSC working as DSTATCOM. The model of conductance based control algorithm used for DSP implementation is the same as discussed in

simulation. The DSP based implementation of conductance based control algorithms is same as given in 4.7.1.

Implementation of DC bus PI controller and PWM current controller for switching pulse generation is the same as discussed in section 4.7.1. The sampling time (T_s) taken by the control algorithm for control of DSTATCOM is around 65μs. The proportional and integral gains of PI controllers are calculated using the standard Ziegler-Nichols unit step response algorithm and the values required in implementation are selected very near to the calculated values.

4.7.4 DSP Implementation of Instantaneous Symmetrical Component Theory Based Control Algorithm

The implementation of ISCT based control algorithm is performed using DSP (dSPACE1104 R&D controller board). The DSP controller board requires real time signals viz. PCC voltages, supply currents and load currents, which are sensed from appropriate sensors and buffer circuitry. The sensed signals are then processed by the MATLAB based control algorithm implemented on dSPACE 1104 controller board. After processing, this controller is used to generate switching pulses for the three phase VSC working as DSTATCOM. The model of ISCT based control algorithm used for DSP implementation is the same as discussed in simulation. The DSP based implementation of ISCT based control algorithms is same as given in 4.7.1. DC bus PI controller and PWM current controller for generation of switching pulses are implemented same as given in section 4.7.1. The sampling time (T_s) taken by the control algorithm for control of DSTATCOM is selected 60μs.

4.8 RESULTS AND DISCUSSION

The results of conventional control algorithms are presented in simulation and developed setup.

This section presents simulation as well as experimental performances of these conventional control algorithms. The simulated performances of these control algorithms are performed using MATLAB/SIMULINK environment. The experimental performance of these control algorithms is achieved by implementing in DSP. The detail discussions on simulation and experimental performances of these control algorithms are given as follows.

4.8.1 Performance of DSTATCOM With Power Balance Based Theory Based Control Algorithm

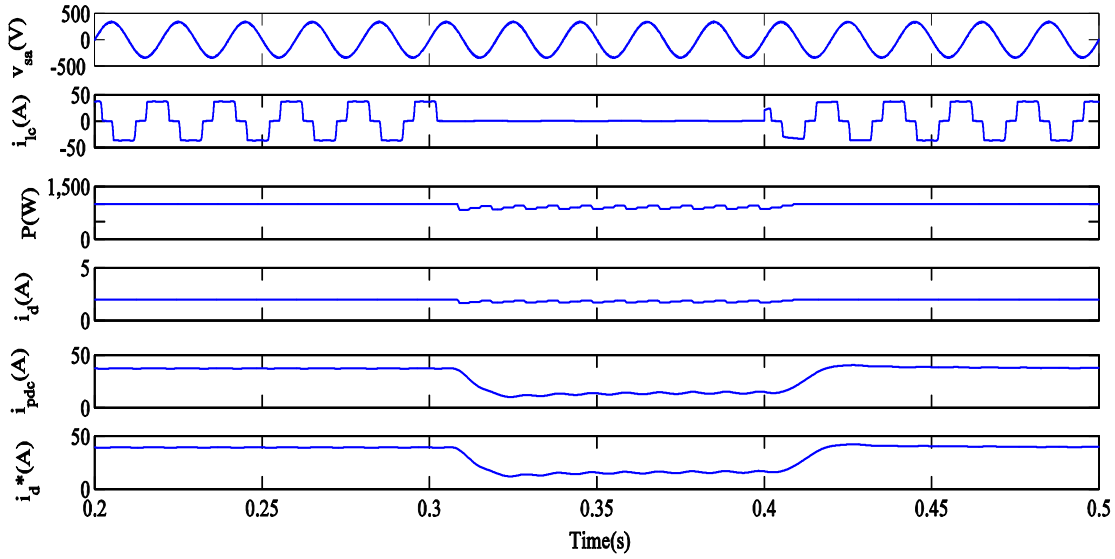
The simulated as well as experimental performances of power balance theory (PBT) based control algorithm are discussed here. The performance of DSTATCOM to achieve harmonic elimination, reactive power compensation and load balancing is presented for PBT based control algorithm. Both the simulation and experimental results are presented for PFC and voltage regulation modes under linear and nonlinear loads.

4.8.1.1 Simulated Performance of DSTATCOM in PFC and Voltage Regulation Modes

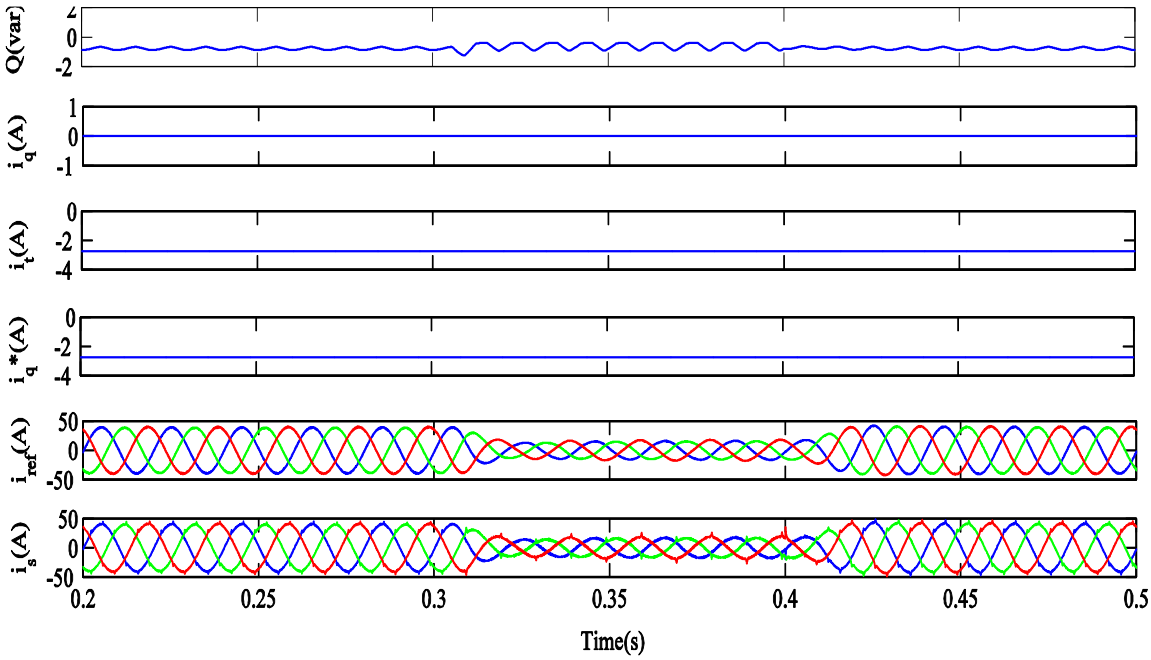
This section presents the simulated performance of DSTATCOM with PBT based control algorithm. The results presented for PFC and voltage regulation modes of DSATCOM are given as follows.

A. Performance of PBT Based Control Algorithm in Voltage Regulation Mode Under Nonlinear Load

Fig. 4.14 shows the performance and intermediate signals of PBT based control algorithm. Fig. 4.14(a) shows waveforms of instantaneous active power (P), estimated fundamental active power component of current (i_d), output of DC bus PI controller (i_{pdc}) and reference active power component of current (i_d^*) along with phase 'a' of PCC voltage (v_{sa}) and phase 'c' of load current (i_{lc}). These results are presented for steady state (before t=0.3s) and unbalanced load (t=0.3s to



(a)



(b)

Fig. 4.14 Intermediate signals of PBT based control algorithm in voltage regulation mode

t=0.4s) conditions. Fig. 4.14(b) shows waveforms of instantaneous reactive power (Q), fundamental reactive current component (i_q), output of AC bus voltage PI controller (i_t), reference reactive current component (i_q^*), reference supply currents (i_s^*) along with actual supply currents (i_s). These results show that reference currents are followed by supply currents properly in steady state and unbalanced load conditions.

B. Performance of DSTATCOM in Power Factor Correction Mode

Fig. 4.15 shows the performance of the DSTATCOM under nonlinear load in PFC mode. The waveforms shown are PCC voltages (v_s), supply currents (i_s), load currents (i_{la}, i_{lb} and i_{lc}), compensator currents (i_{Ca}, i_{Cb} and i_{Cc}) and self-sustained DC bus voltage (V_{dc}). Performance of the system is observed in steady state (before t=0.3s) and unbalanced load (t=0.3s to t=0.4s) conditions. Unbalancing is created in the load current, when phase 'c' is switched off. It is observed from these results that supply currents are balanced and sinusoidal in steady state and unbalanced load conditions. The DC bus voltage is regulated to the reference value of 700V

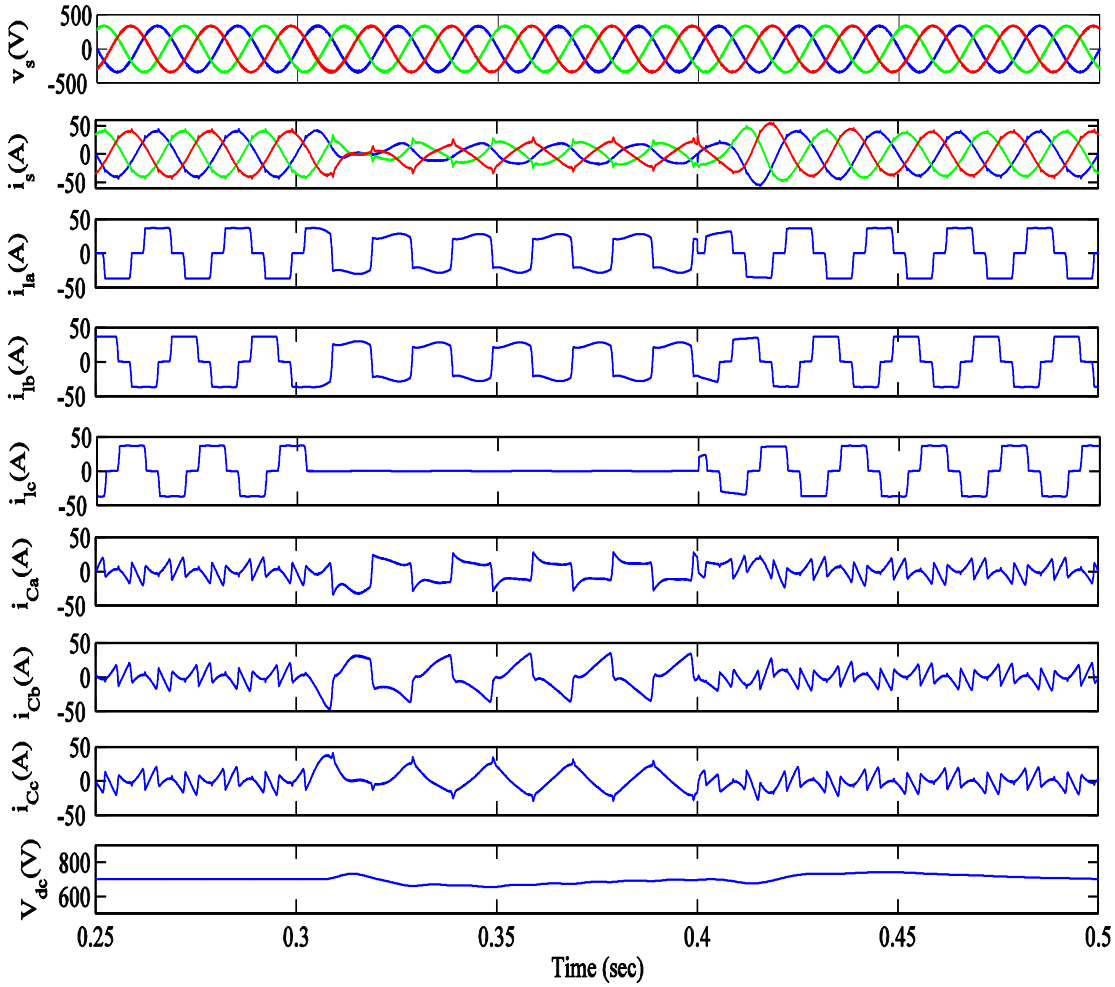


Fig. 4.15 Performance of DSTATCOM in PFC mode

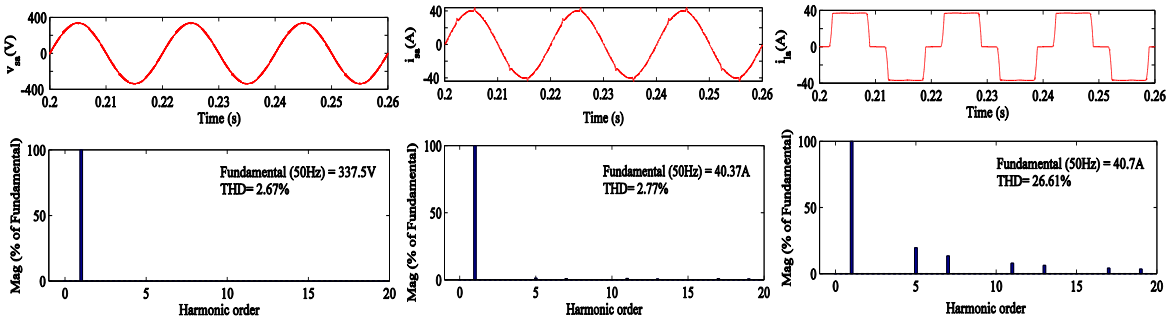
became of the action of PI controller.

Fig. 4.16 shows harmonic spectra of phase 'a' of PCC voltage (v_{sa}), supply current (i_{sa}) and load current (i_{la}). These results show the THDs of 2.67%, 2.77% and 26.61% in PCC voltage, supply current and load current respectively. It is observed from these results that the THD obtained in supply current is 2.77%, whereas there is 26.61% THD in load current. The THDs in PCC voltage and supply current are within the limit specified by IEEE-519 standard.

C. Performance of DSTATCOM in Voltage Regulation Mode

Fig. 4.17 shows performance of DSTATCOM in voltage regulation mode. The waveforms presented in these results are PCC voltages (v_s), supply currents (i_s), load currents (i_{la}, i_{lb} and i_{lc}), compensator currents (i_{Ca}, i_{Cb} and i_{Cc}), DC bus voltage (V_{dc}) and amplitude of PCC voltage (V_t). These results are shown for steady state (before t=0.3s) as well as unbalanced load (t=0.3s to t=0.4s) conditions. Supply currents are observed balanced and sinusoidal during both steady state and unbalanced load conditions. The amplitude of PCC voltage is regulated at its reference value of 338.8V due to action of PI controller.

Fig. 4.18 shows harmonic spectra of phase 'a' of PCC voltage (v_{sa}), supply current (i_{sa}) and load



(a) (b) (c)

Fig. 4.16 Harmonic spectra of (a) PCC voltage, v_{sa} (b) supply current, i_{sa} (c) load current, i_{la} in PFC mode

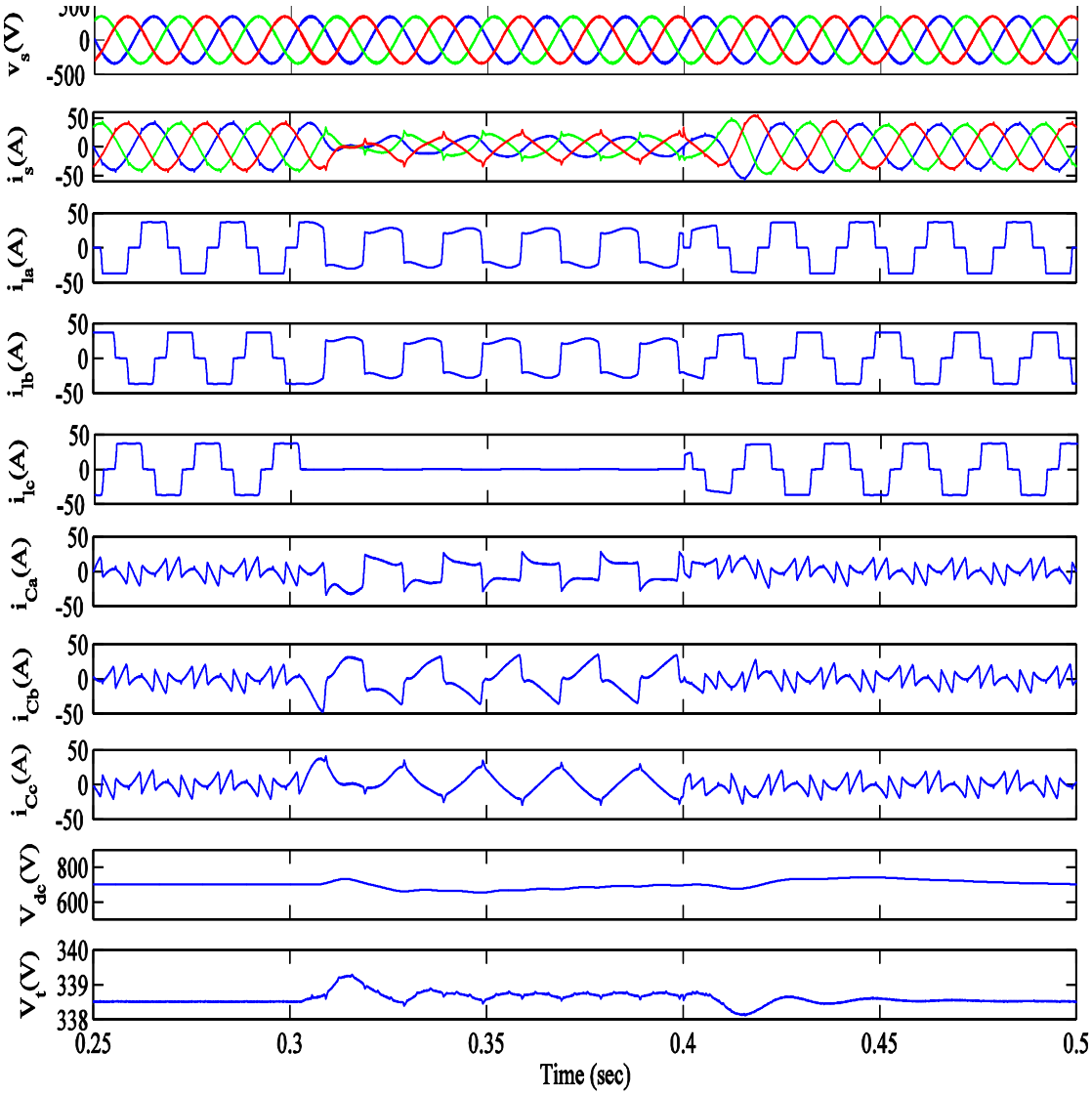
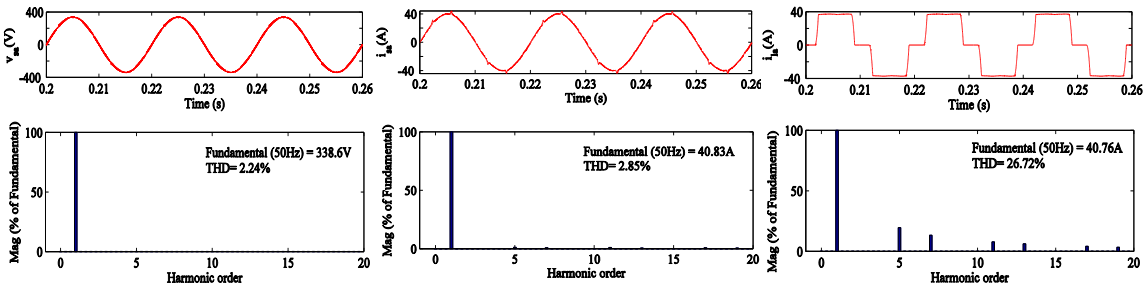


Fig. 4.17 Performance of DSTATCOM in voltage regulation mode

current (i_{la}). These results show the THDs of 2.24%, 2.85% and 26.72%, in PCC voltage, supply current and load current respectively. It is observed from these results that the THD obtained in supply current is 2.85%, whereas there is 26.72% THD in load current. The THDs in PCC voltage and supply current are within the limit specified by IEEE-519 standard.

4.8.1.2 Experimental Performance of DSTATCOM in PFC and Voltage Regulation modes



(a) (b) (c)

Fig. 4.18 Harmonic spectra of (a) PCC voltage, v_{sa} (b) supply current, i_{sa} (c) load current, i_{la} in voltage regulation mode

This section discusses the experimental performance of PBT based control algorithm in PFC and voltage regulation mode under nonlinear and linear loads. The test results are recorded using power quality analyzer (Fluke 43B) and four channel DSO (Agilent DSO-X 2014A) on the developed laboratory prototype. The test results for DSTATCOM with PBT based control algorithm are given as follows.

A. Steady State Performance of DSTATCOM Under Nonlinear and Linear Load in PFC Mode

Fig. 4.19 shows steady state performance of DSTATCOM in PFC mode. Figs. 4.19(a), (c) and (e) show waveforms of phase 'a' of supply current (i_{sa}), load current (i_{la}) and compensator current (i_{Ca}) along with PCC voltage (v_{sa}). Figs. 4.19(b), (d) and (f) present harmonic spectra of supply current, load current and PCC voltage. These results show the THD of 4.2%, 20.5% and 2.6% in supply current, load current and PCC voltage respectively. The improved THD is achieved in supply current due to action of the shunt compensator and has been found within the limit specified by IEEE-519 standard. Fig. 4.20 shows simulation results at same rating (110V) for which experimental system is developed in the laboratory. These results present waveforms of PCC voltages (v_{sa}), supply currents (i_{sa}), load currents (i_{sa}), compensator currents (i_{Ca}) and DC bus voltage (V_{dc}). Supply currents are observed balanced and sinusoidal during steady state

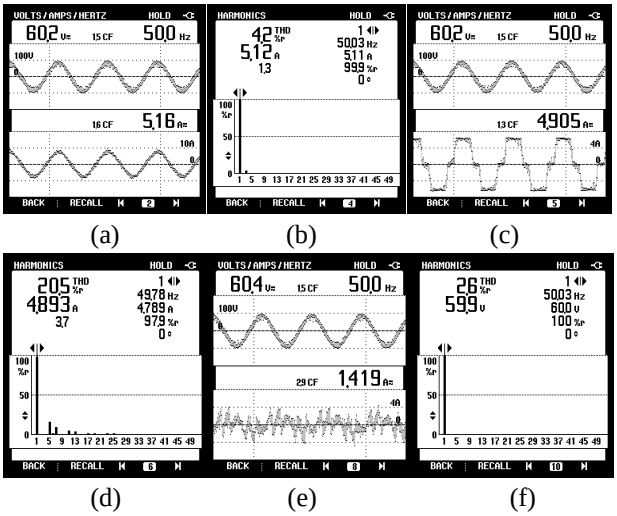


Fig. 4.19 Steady state performance of DSTATCOM in PFC mode (a), (c) and (e) i_{sa}, i_{la} and i_{Ca} along with v_{sa} (b), (d) and (f) Harmonic spectra of i_{sa}, i_{la} and v_{sa}

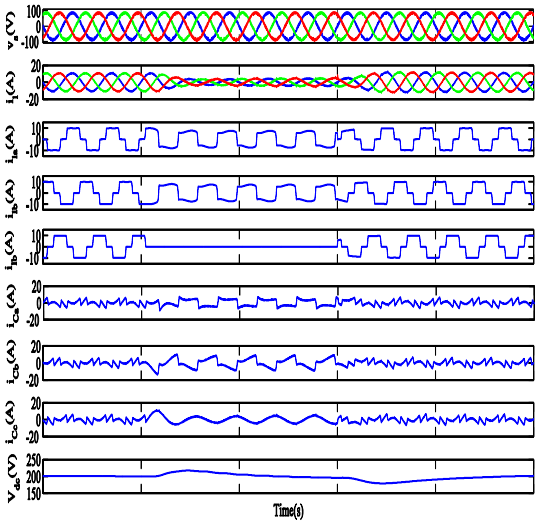


Fig. 4.20 Simulated performance of DSTATCOM in PFC mode under nonlinear load

(before t=0.3s) and unbalance load (t=0.3s to t=0.4s) conditions. The voltage at DC bus of VSC is regulated at the reference value of 200V due to the action of PI controller.

Fig. 4.21 shows steady state performance of the DSTATCOM under linear lagging PF load in PFC mode. Figs. 4.21(a)-(c) show waveforms of phase 'a' of supply current (i_{sa}), load current (i_{la}) and compensator current (i_{Ca}) along with PCC voltage (v_{sa}). Figs. 4.21 (d)-(f) show

waveforms of supply power (P_s), load power (P_l) and compensator power (P_C). The values of supply and load apparent power are 0.255kVA and 0.287kVA respectively. The power factor on supply side is improved (1 DPF) as the reactive power demand of the load is compensated by DSTATCOM. Fig. 4.22 shows simulated performance of the DSTATCOM under linear load in PFC mode at the same rating for which experimental system is developed. The waveforms of PCC voltages (v_s), supply currents (i_s), load currents (i_{la}, i_{lb} and i_{lc}), compensator currents (i_{Ca}, i_{Cb} and i_{Cc}) and self-sustained DC bus voltage (V_{dc}) are presented in these results. It is observed

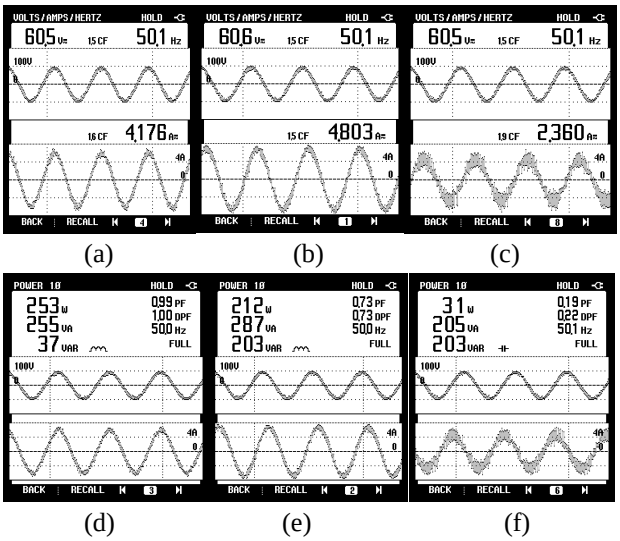


Fig. 4.21 Steady-state performance of DSTATCOM at linear lagging PF load in PFC mode (a) v_{sa} and i_{sa} (b) v_{sa} and i_{la}(c) v_{sa} and i_{Ca} (d) P_s (e) P_l (f) P_C

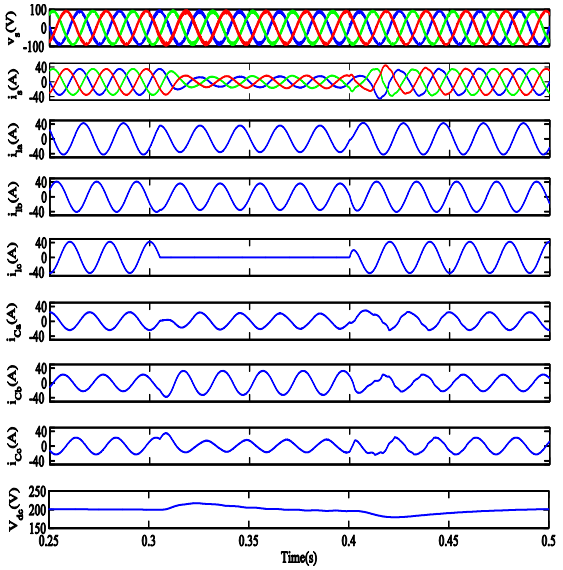


Fig. 4.22 Simulated performance of DSTATCOM in PFC mode under linear load

from the results that supply currents are maintained balanced and sinusoidal in steady state and unbalance load conditions.

B. Dynamic performance of DSTATCOM in PFC mode

Fig. 4.23 presents dynamic performance of DSTATCOM in PFC mode under nonlinear load. Figs. 4.23 (a), (b) and (c) show waveforms of supply currents (i_{sa}, i_{sb} and i_{sc}), load currents (i_{la}, i_{lb} and i_{lc}) and compensator currents (i_{Ca}, i_{Cb} and i_{Cc}) along with phase 'a' of PCC voltage (v_{sa}). These results are shown for steady state and unbalanced load conditions. It is observed from these results that supply currents are balanced and sinusoidal in each load condition. Fig. 4.23(d) shows waveforms of phase 'c' of supply current (i_{sc}), load current (i_{lc}) and compensator current (i_{Cc}) along with DC bus voltage (V_{dc}). It is observed from these results that DC bus voltage has achieved the reference value within few cycles during unbalanced load conditions.

C. Steady State Performance of DSTATCOM in Voltage Regulation Mode

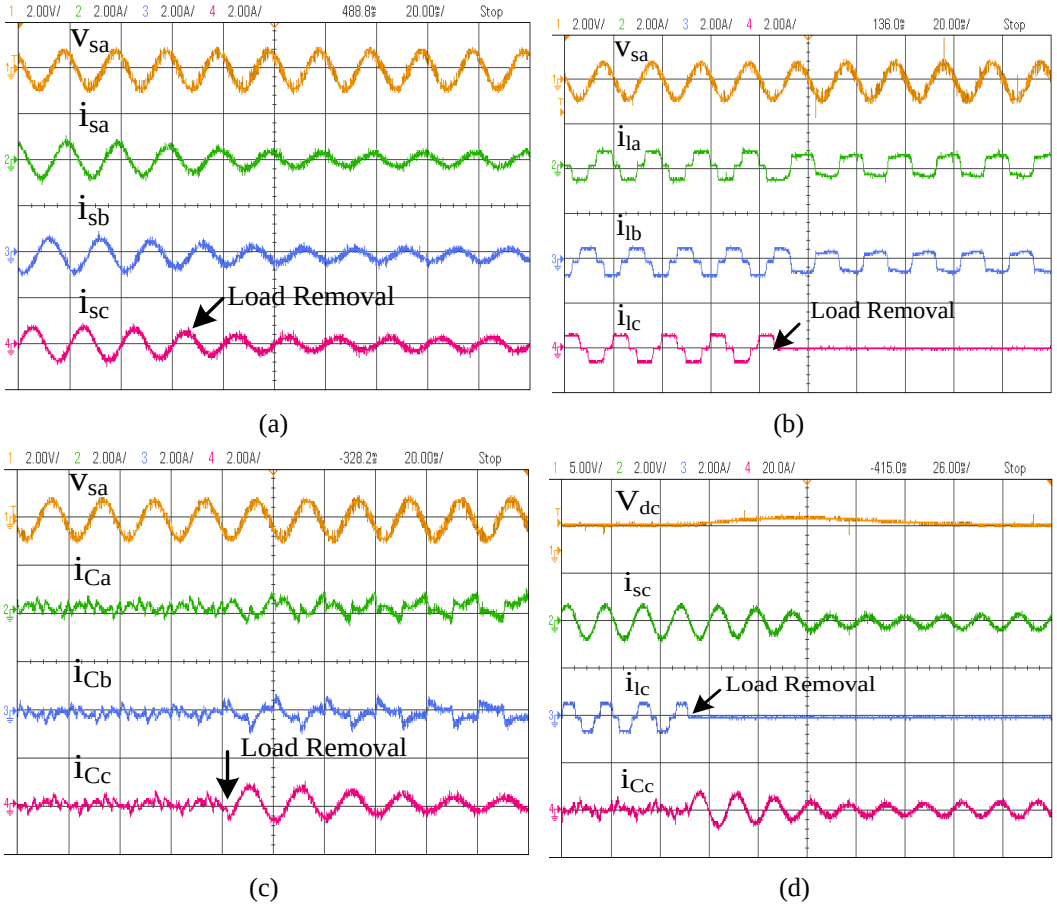


Fig. 4.23 Dynamic performance of DSTATCOM in PFC mode

Fig. 4.24 presents steady state performance of DSTATCOM in voltage regulation mode using PBT based control algorithm. Figs. 4.24(a), (c) and (e) show waveforms of phase 'a' of supply current (i_{sa}), load current (i_{la}) and compensator current (i_{Ca}) along with PCC voltage (v_{sa}). Figs. 4.24(b), (d) and (f) show harmonic spectra of supply current, load current and PCC voltage. These results present THD of 4.3%, 21.0% and 3.3% in supply current, load current and PCC voltage respectively. An improved THD is achieved in supply current after compensation which is within the limit specified by IEEE-519 standard. Figs. 4.24(g), (h) and (i) show reactive powers in supply (Q_s), load (Q_l) and compensator (Q_C). It is observed from these results that values of supply and load reactive powers are 0.18kVAR and 0.09kVAR respectively. These

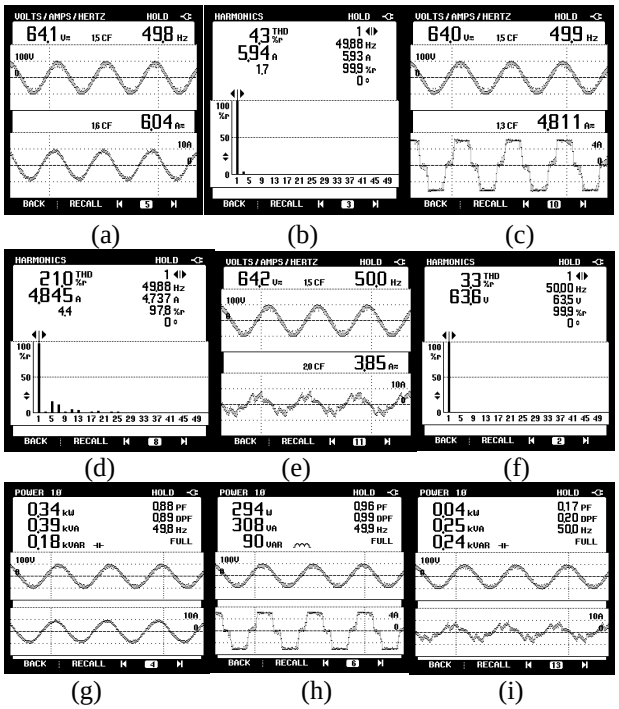


Fig. 4.24 Steady state performance of DSTATCOM in voltage regulation mode (a),(c) and (e) i_{sa}, i_{la} and i_{Ca} along with v_{sa} (b),(d) and (f) Harmonic spectra of i_{sa}, i_{la} and v_{sa} (g), (h) and (i) Q_s, Q_l and Q_C

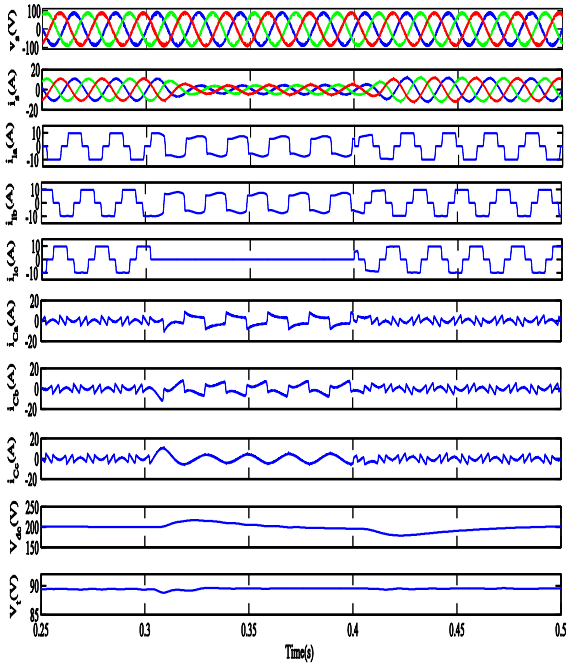


Fig. 4.25 Simulated performance of DSTATCOM in voltage regulation mode

results present satisfactory performance of the control algorithm used for PCC voltage regulation along with harmonic elimination.

Fig. 4.25 presents simulated performance of DSTATCOM in voltage regulation mode at the same voltage rating for which experimental prototype is developed. These results present waveforms of PCC voltages (v_s), supply currents (i_s), load currents (i_{la}, i_{lb} and i_{lc}), compensator currents (i_{Ca}, i_{Cb} and i_{Cc}), self-sustained DC bus voltage (V_{dc}) and amplitude of PCC voltage (V_t). It is observed from these results that DC bus voltage and amplitude of PCC voltage are regulated at their reference values in steady state (before t=0.3s) and unbalance load condition (t=0.3 to t=0.4s) respectively.

D. Dynamic Performance of DSTATCOM in Voltage Regulation Mode

Fig. 4.26 shows the dynamic performance of DSTATCOM in voltage regulation mode with PBT based control algorithm. Fig. 4.26(a) presents waveforms of regulated DC bus voltage (V_{dc}), regulated amplitude of PCC voltage (V_t) along with phase 'a' of supply voltage (i_{sa}) and load current (i_{la}) in steady state and unbalanced load conditions. It is observed from these results that supply currents are maintained balanced and sinusoidal in steady state and unbalanced load conditions. The amplitude of PCC voltage magnitude (V_t) is boosted from 85V to 90V, as shown in Fig. 4.26(b).

4.8.2 Performance of DSTATCOM with Instantaneous Reactive Power Theory Based Control Algorithm

The simulated and experimental performances of DSTATCOM with IRPT based control algorithm are presented here. The simulation study is performed in MATLAB/SIMULINK environment. Experimental verification of IRPT based control algorithm is performed with developed prototype in the laboratory. The detail descriptions of simulation as well as experimental results are given as follows.

4.8.2.1 Simulated Performance of DSTATCOM in PFC and Voltage Regulation Modes

Simulated performance of DSTATCOM in PFC and voltage regulation modes using IRPT based

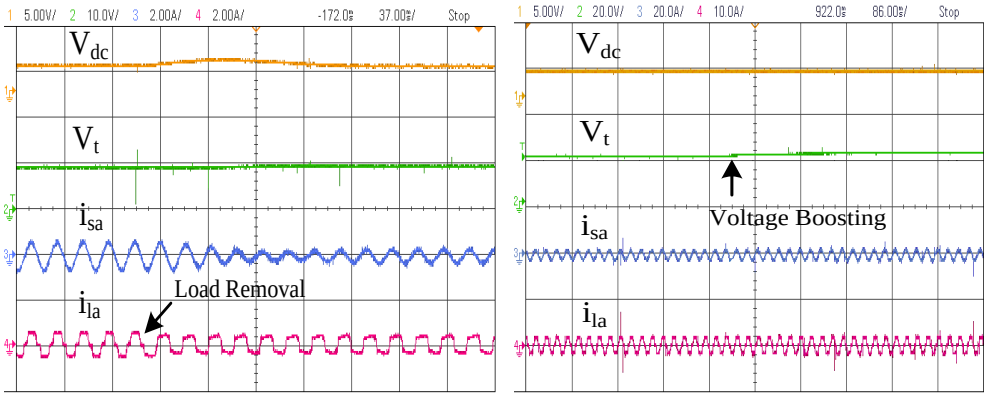


Fig. 4.26 Dynamic performance of DSTATCOM in voltage regulation mode under nonlinear load

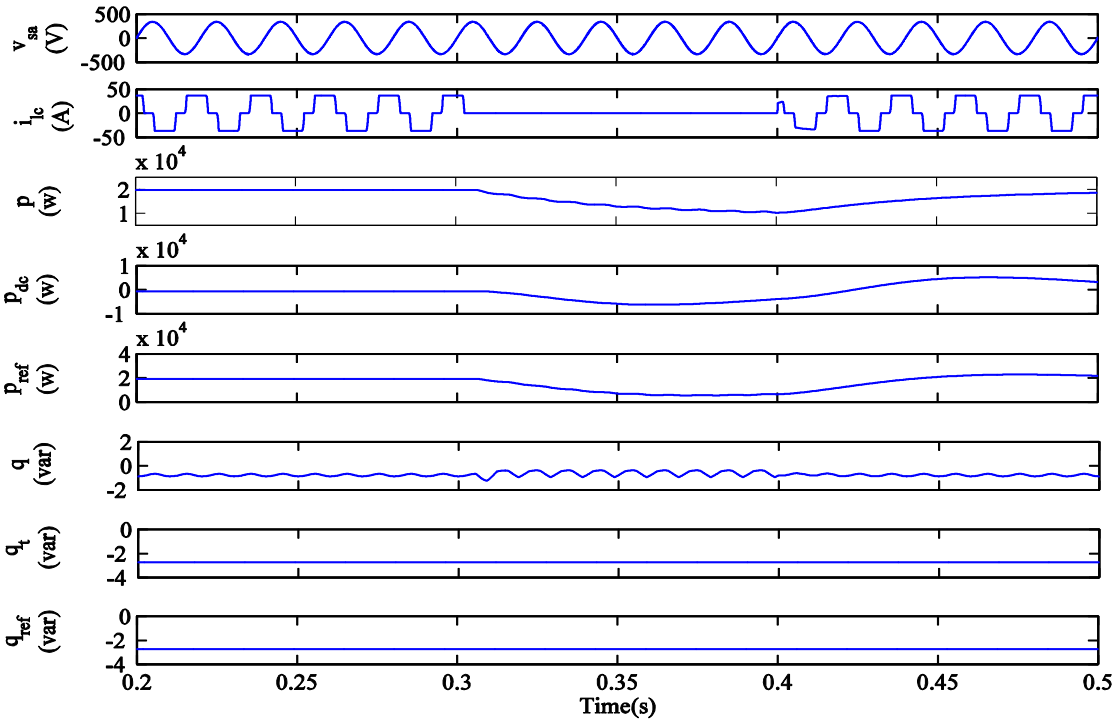
control algorithm is presented here. This is divided into three parts. The first part presents performance and intermediate signals of the control algorithm. The second and third parts present the performance of DSTATCOM in PFC and voltage regulation modes.

A. Performance of IRPT Based Control Algorithm in Voltage Regulation Mode Under Nonlinear Load

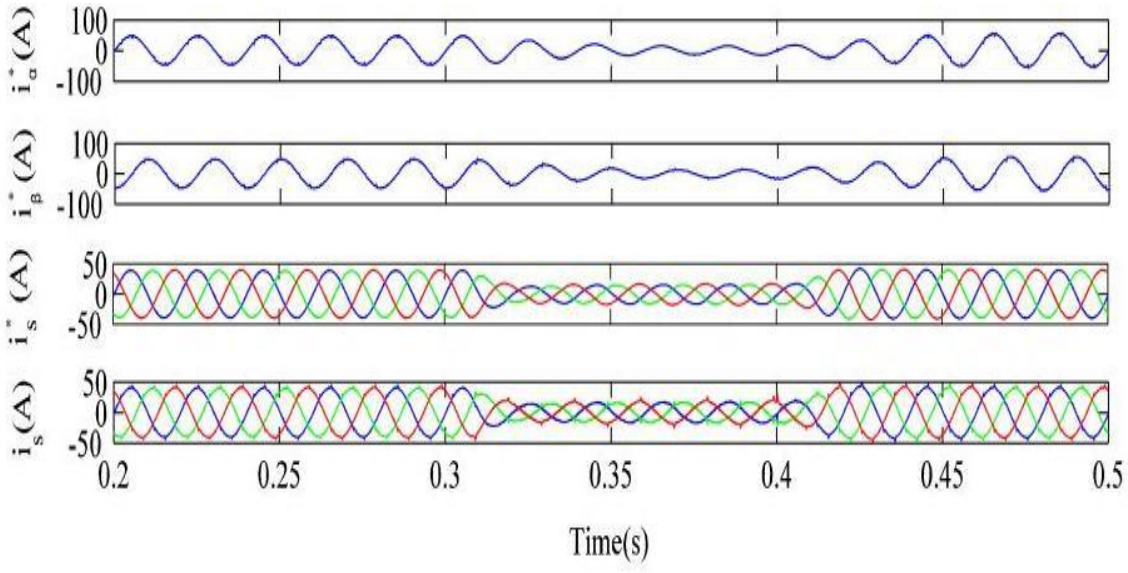
Fig. 4.27 shows performance and intermediate signals of IRPT based control algorithm in voltage regulation mode. Fig. 4.27(a) shows the waveforms of instantaneous active power (p), output of DC bus voltage PI controller (p_{dc}), reference active power (p_{ref}), instantaneous reactive power (q), output of AC bus voltage PI controller (q_t) and reference reactive power (q_{ref}). These results are presented for steady state (before t=0.3s) and unbalanced load (t=0.3s to t=0.4s) condition. Fig. 4.27(b) shows waveforms of alpha and beta components (i_α^* and i_β^*) of reference supply currents along with reference supply (i_s^*) and actual supply (i_s) currents. It is observed from the results that reference supply currents are perfectly followed by actual supply currents in steady state and unbalance load conditions.

B. Performance of DSTATCOM in PFC mode Using IRPT Based Control Algorithm

Fig. 4.28 shows the performance of DSTATCOM in PFC mode using IRPT based control algorithm. Waveforms of PCC voltages (v_s), supply currents (i_s), load currents (i_{la}, i_{lb} and i_{lc}), compensator currents (i_{Ca}, i_{Cb} and i_{Cc}) and voltage of self-sustained DC bus (V_{dc}) are shown in these results. It is observed from these results that under steady state condition upto t=0.3s, the supply currents are balanced sinusoidal and the DC bus voltage is regulated at its reference value of 700V. An unbalancing in the load is created when phase 'c' of load is switched off. It is observed that the supply currents are balanced sinusoidal with reduced magnitude during load unbalancing.



(a)



(b)

Fig. 4.27 Intermediate signals of PBT based control algorithm in voltage regulation mode

Fig. 4.29 shows the harmonic spectra of phase 'a' of PCC voltage (v_{sa}), supply current (i_{sa}) and load current (i_{la}) in PFC mode under nonlinear load. Total harmonic distortions (THDs) of v_{sa}, i_{sa} and i_{la} are 1.73%, 2.79% and 26.61% respectively. It is observed from these results that the

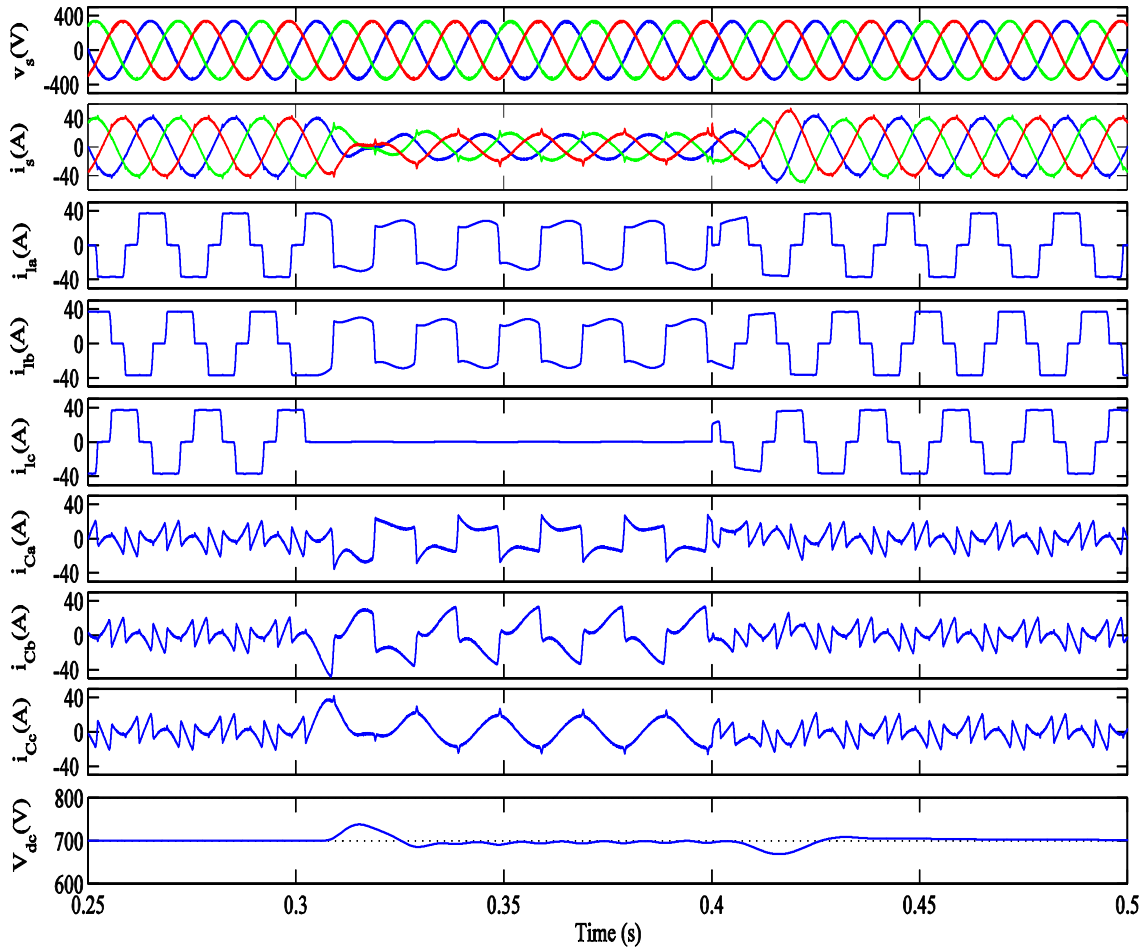
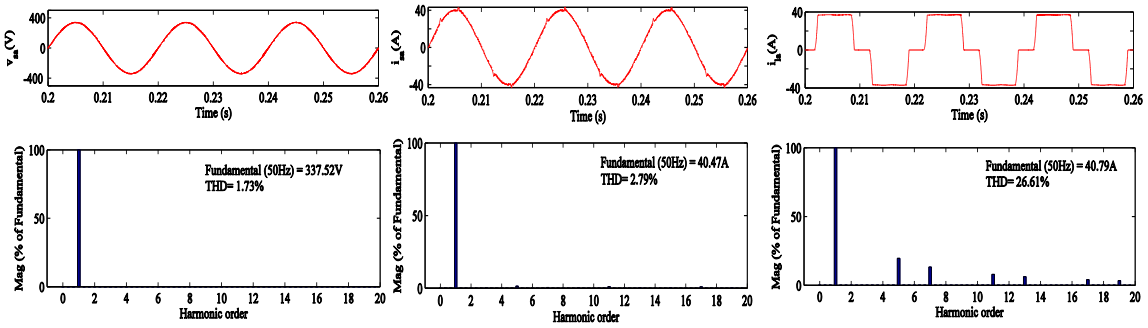


Fig. 4.28 Performance of DSTATCOM in PFC mode using IRPT based control algorithm



(b) (b) (c)

Fig. 4.29 Harmonic spectra of (a) PCC voltage, v_{sa} (b) supply current, i_{sa} (c) load current, i_{la} in PFC mode

2.79% THD in supply current is achieved, whereas there is 26.61% THD in load current. The THD values of PCC voltage and supply current are within the limit of IEEE-519 standard.

C. Performance of DSTATCOM in Voltage Regulation Mode Using IRPT Based Control Algorithm

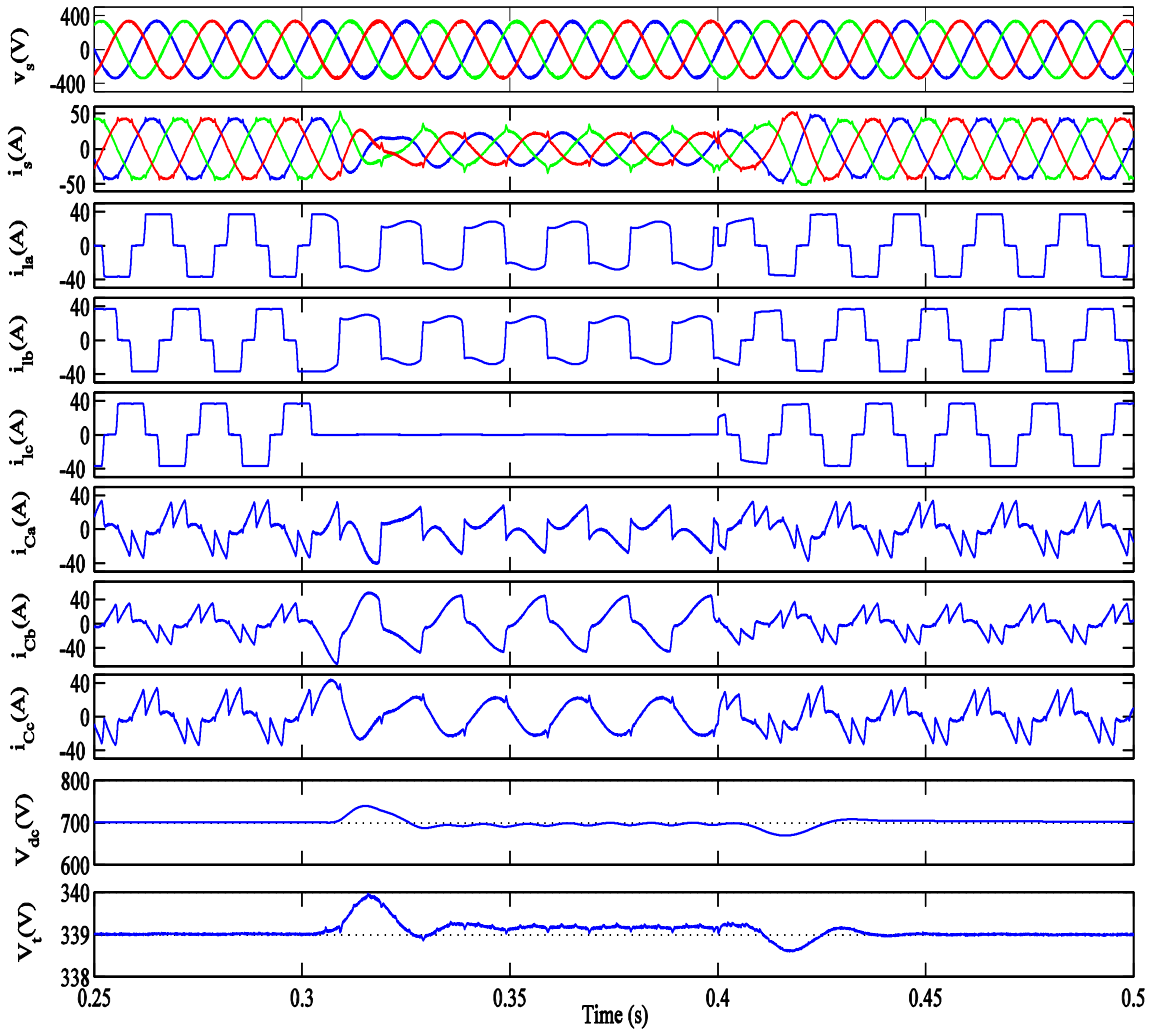


Fig. 4.30 Performance of DSTATCOM in voltage regulation mode using IRPT based control algorithm

Fig. 4.30 shows the performance of DSTATCOM in voltage regulation mode with IRPT based control algorithm. These results show the waveforms of PCC voltages (v_s), supply currents (i_s), load currents (i_{la}, i_{lb} and i_{lc}), compensator currents (i_{Ca}, i_{Cb} and i_{Cc}), DC bus voltage (V_{dc}) and amplitude of AC bus voltage (V_t). It is observed from these results that under steady state condition (before t=0.3s), the supply currents are balanced and sinusoidal and the DC and AC bus voltages are regulated at their reference value of 700V and 339V. During unbalanced load condition (t=0.3s to t=0.4s) supply currents are also maintained balanced and sinusoidal with reduced magnitude due to DSTATCOM action.

Fig. 4.31 shows the harmonic spectra of phase 'a' of PCC voltage (v_{sa}), supply current (i_{sa}) and load current (i_{la}) in PFC under nonlinear load. Total harmonic distortions (THDs) of PCC voltage, supply current and load current are 1.96%, 3.49% and 26.62% respectively. It is observed from these results that the 3.49% THD in supply current is achieved, whereas there is

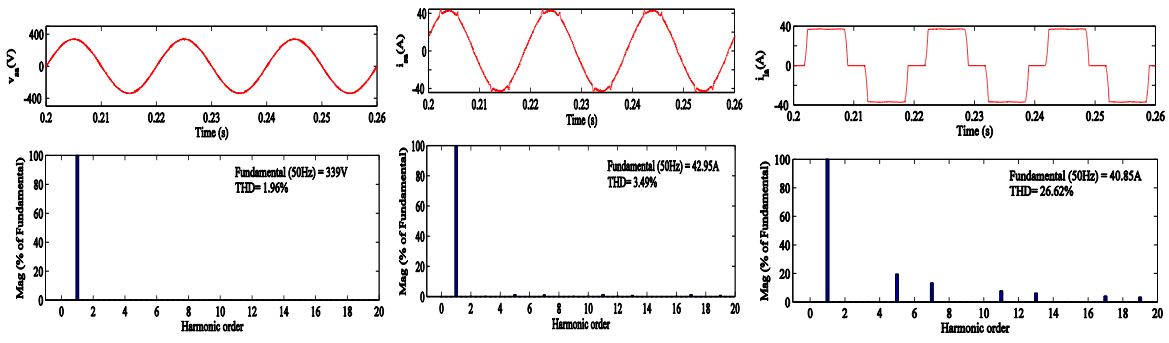
26.62% THD in load current. The THD values of PCC voltage and supply current are within the limit of IEEE-519 standard.

4.8.2.2 Experimental Performance of DSTATCOM in PFC Mode

The performance IRPT based control algorithm is validated using experimental prototype developed in the laboratory. This control algorithm is tested for steady state and dynamic load conditions. The test results are recorded using power quality analyzer (Fluke 43B) and digital storage oscilloscope. The detail description of the experimental results is given as follows.

A. Steady State Performance of DSTATCOM Using IRPT Based Control Algorithm

Fig. 4.32 shows steady state performance of DSTATCOM under nonlinear load. Figs. 4.32(a), (c) and (e) show waveforms of phase 'a' of supply current (i_{sa}), load current (i_{la}) and compensator current (i_{Ca}) along with PCC voltage (v_{sa}). Figs. 4.32(b), (d) and (f) present



(c) (b) (c)

Fig. 4.31 Harmonic spectra of (a) PCC voltage, v_{sa} (b) supply current, i_{sa} (c) load current, i_{la} in voltage regulation mode

harmonic spectra of supply current, load current and PCC voltage. These results show THD of 4.2%, 22.5% and 3.4% in supply current, load current and PCC voltage respectively. The improved THD is achieved in supply current due to action of DSTATCOM, which is found within the limit specified by IEEE-519 standard.

Fig. 4.33 shows simulation study at same rating (110V) for which experimental system is developed in the laboratory. These results present waveforms of PCC voltages (v_{sa}), supply currents (i_{sa}), load currents (i_{sa}), compensator currents (i_{Ca}) and DC bus voltage (V_{dc}). Supply currents are observed balanced and sinusoidal during steady state (before t=0.3s) and unbalance load (t=0.3s to t=0.4s) conditions. The voltage at DC bus is regulated at the reference value of 200V due to the action of PI controller.

B. Dynamic Performance of DSTATCOM Using IRPT Based Control Algorithm

Fig. 4.34 shows dynamic performance of DSTATCOM under nonlinear load. Figs. 4.34 (a), (b)

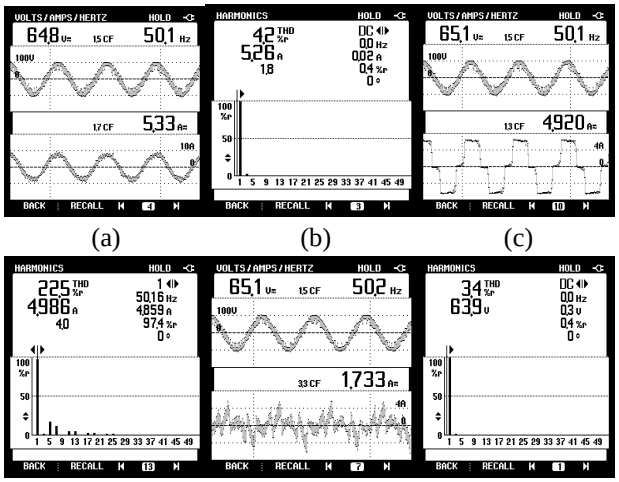


Fig. 4.32 Steady state performance of DSTATCOM in PFC mode (a), (c) and (e) i_{sa}, i_{la} and i_{Ca} along with v_{sa} (b), (d) and (f) Harmonic spectra of i_{sa}, i_{la} and v_{sa}

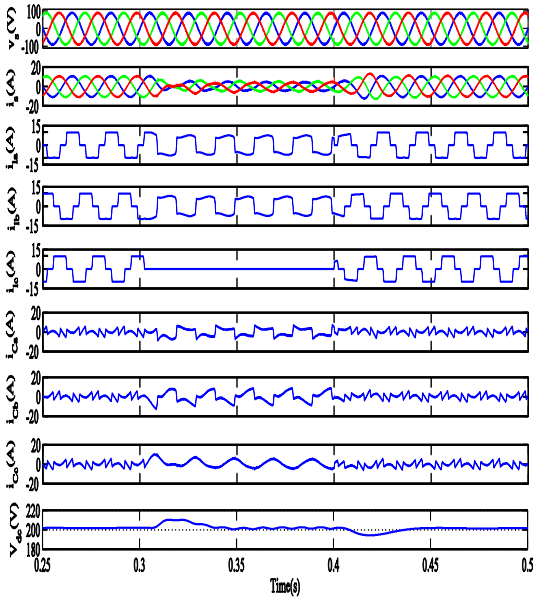


Fig. 4.33 Simulated performance of DSTATCOM in PFC mode

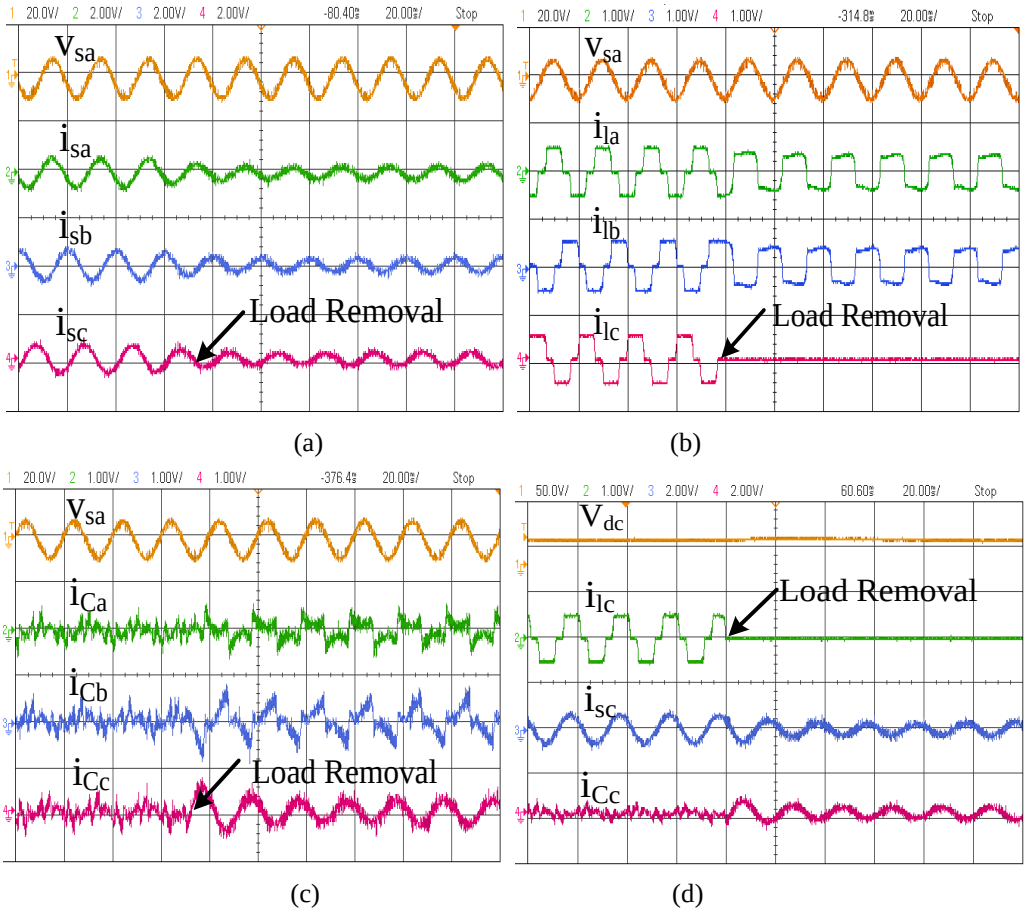


Fig. 4.34 Dynamic performance of DSTATCOM under nonlinear load

and (c) show waveforms of supply currents (i_{sa}, i_{sb} and i_{sc}), load currents (i_{la}, i_{lb} and i_{lc}) and compensator currents (i_{Ca}, i_{Cb} and i_{Cc}) along with phase 'a' of PCC voltage (v_{sa}). These results are shown for steady state and unbalanced load conditions. It is observed from these results that supply currents are balanced and sinusoidal in each load conditions. Fig. 4.34(d) shows waveforms of phase 'c' of supply current (i_{sc}), load current (i_{lc}) and compensator current (i_{Cc}) along with DC bus voltage (V_{dc}). It is observed from these results that the DC bus voltage achieves the reference value within few cycles during unbalanced load condition.

4.8.3 Performance of DSTATCOM With Conductance Based Control Algorithm

Performance of DSTATCOM such as harmonics elimination and load balancing with conductance based control algorithm is presented here. Simulation study of the control algorithm

is performed in MATLAB/SIMULINK environment. Experimental verification of the control algorithm is performed on developed prototype in the laboratory. The detail descriptions of simulation as well as experimental results are given as follows.

4.8.3.1 Simulated Performance of DSTATCOM With Conductance Based Control Algorithm

Performance of the conductance based control algorithm is presented in the form of simulation results. The features of DSTATCOM such as harmonics elimination and load balancing are presented.

A. Performance of Conductance Based Control Algorithm

Fig. 4.35 shows performance and intermediate signals of conductance based control algorithm. Fig. 4.35(a) shows the waveforms of phase 'a' of PCC voltage (v_{sa}), phase 'c' of load current (i_{lc}), load conductance (G_l), corresponding conductance computed from output of DC bus PI controller (G_d), reference conductance (G_{sp}), load susceptance (B_l), corresponding susceptance computed from output of AC bus PI controller, reference susceptance (B_{sq}), reference supply currents (i_s^*) and sensed supply currents (i_s). These waveforms are shown for steady state (before t=0.3s) and unbalanced (t=0.3s to t=0.4s) load conditions. Satisfactory performance of the control algorithm is observed under all the load conditions. The actual currents follow the reference supply currents perfectly.

B. Performance of DSTATCOM in With Conductance Based Control Algorithm in PFC Mode

Fig. 4.36 presents the performance of DSTATCOM with the control algorithm. These results show the waveforms of PCC voltages (v_s), supply currents (i_s), load currents (i_{la}, i_{lb} and i_{lc}), compensator currents (i_{Ca}, i_{Cb} and i_{Cc}) and voltage of self-sustained DC bus (V_{dc}). It is observed

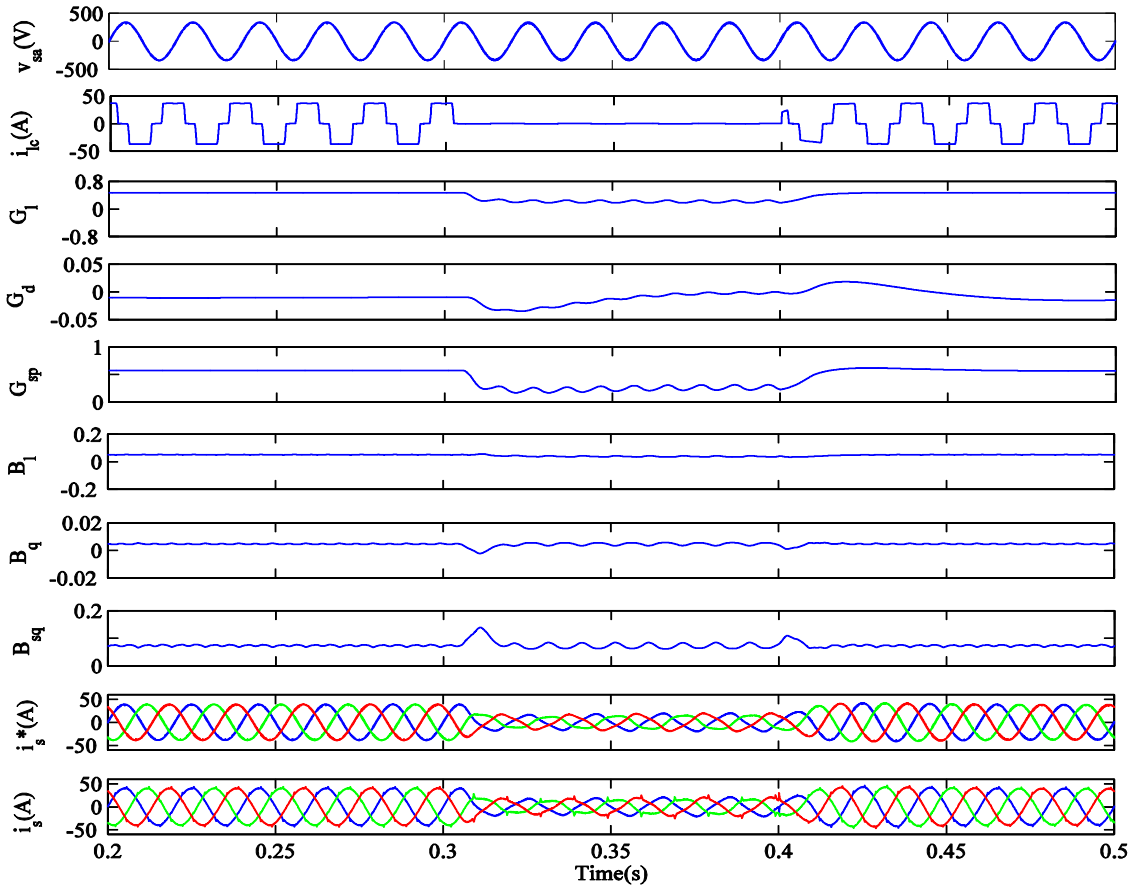


Fig. 4.35 Performance of conductance based control algorithm

from these results that under steady state condition (before t=0.3s) the supply currents are balanced and sinusoidal. The DC bus voltage is regulated at its reference value of 700V. the unbalanced load currents (t=0.3s to t=0.4s) are observed when phase 'c' of load is switched off. The supply currents are maintained balanced and sinusoidal during unbalancing due to compensation provided by DSTATCOM.

Fig. 4.37 shows the harmonic spectra of phase 'a' of PCC voltage (v_{sa}), supply current (i_{sa}) and load current (i_{la}) in PFC under nonlinear load. Total harmonic distortion (THD) of PCC voltage, supply current and load current are 2.04%, 2.81% and 26.59% respectively. It is observed from these results that THD of 2.81% in supply current is achieved, whereas there is 26.59% THD in

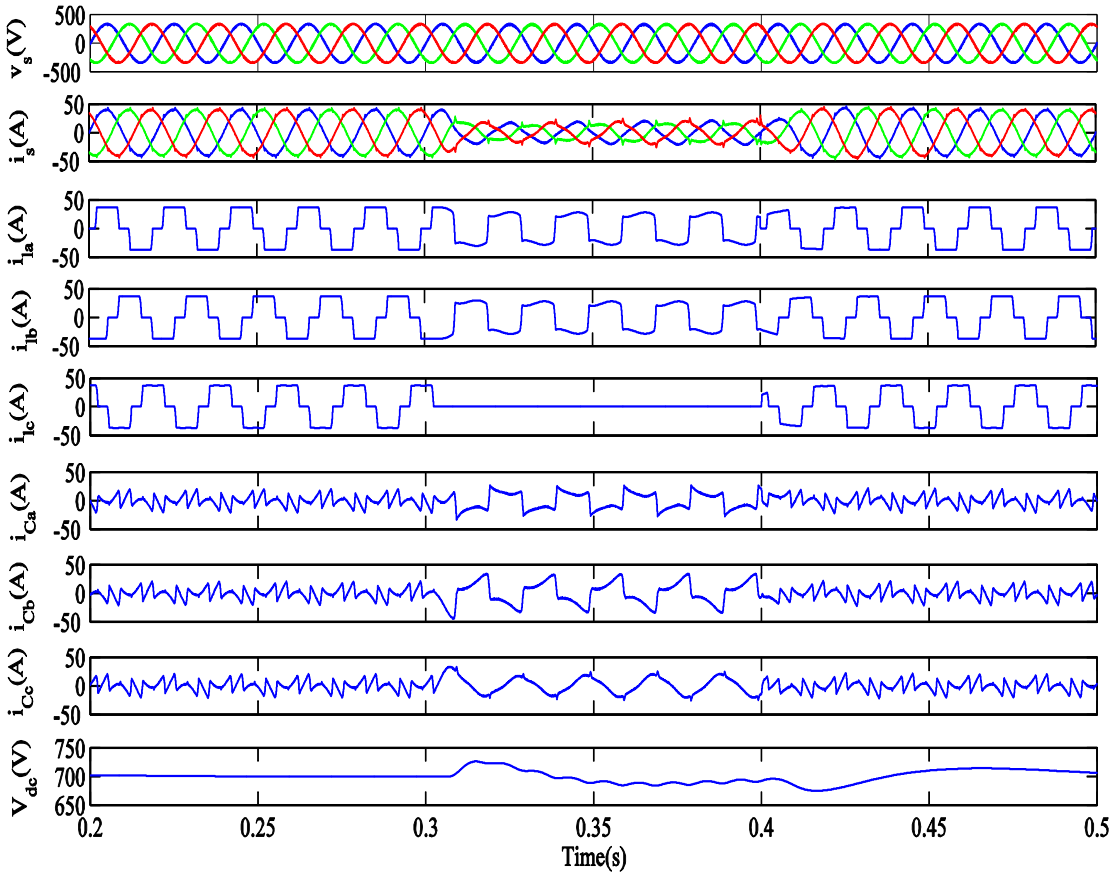
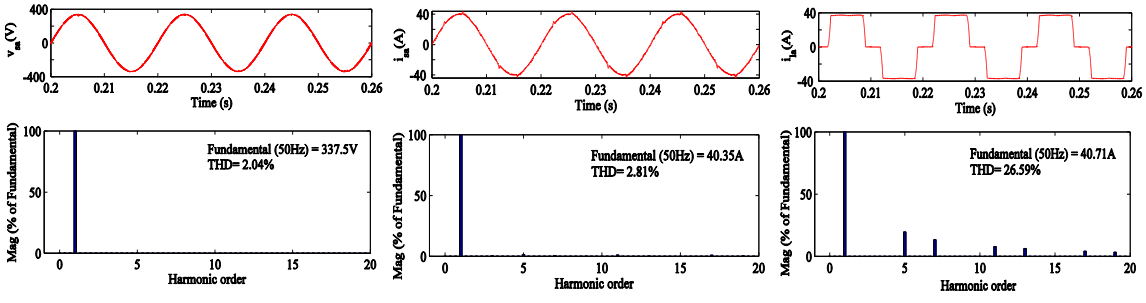


Fig. 4.36 Performance of DSTATCOM with conductance based control algorithm in PFC mode

load current. The THD values of PCC voltage and supply current are within the limit of IEEE-519 standard.

C. Performance of DSTATCOM in Voltage Regulation Mode Using Conductance Based Control Algorithm



(a) (b) (c)

Fig. 4.37 Harmonic spectra of (a) PCC voltage, v_{sa} (b) supply current, i_{sa} (c) load current, $i_{la,}$ in PFC mode

Fig. 4.38 shows performance of DSTATCOM in voltage regulation mode using conductance based control algorithm. These results show waveforms of PCC voltages (v_s), supply currents (i_s), load currents (i_{la}, i_{lb} and i_{lc}), compensator currents (i_{Ca}, i_{Cb} and i_{Cc}), DC bus voltage (V_{dc}) and amplitude of PCC voltage (V_t). In steady state condition (before t=0.3s), supply currents are observed balance and sinusoidal by control action of shunt compensator. The DC and AC bus voltages are regulated at their reference values of 700V and 339V respectively. An unbalancing is created in the load during t=0.3s to t=0.4s. Results show that even in unbalanced load

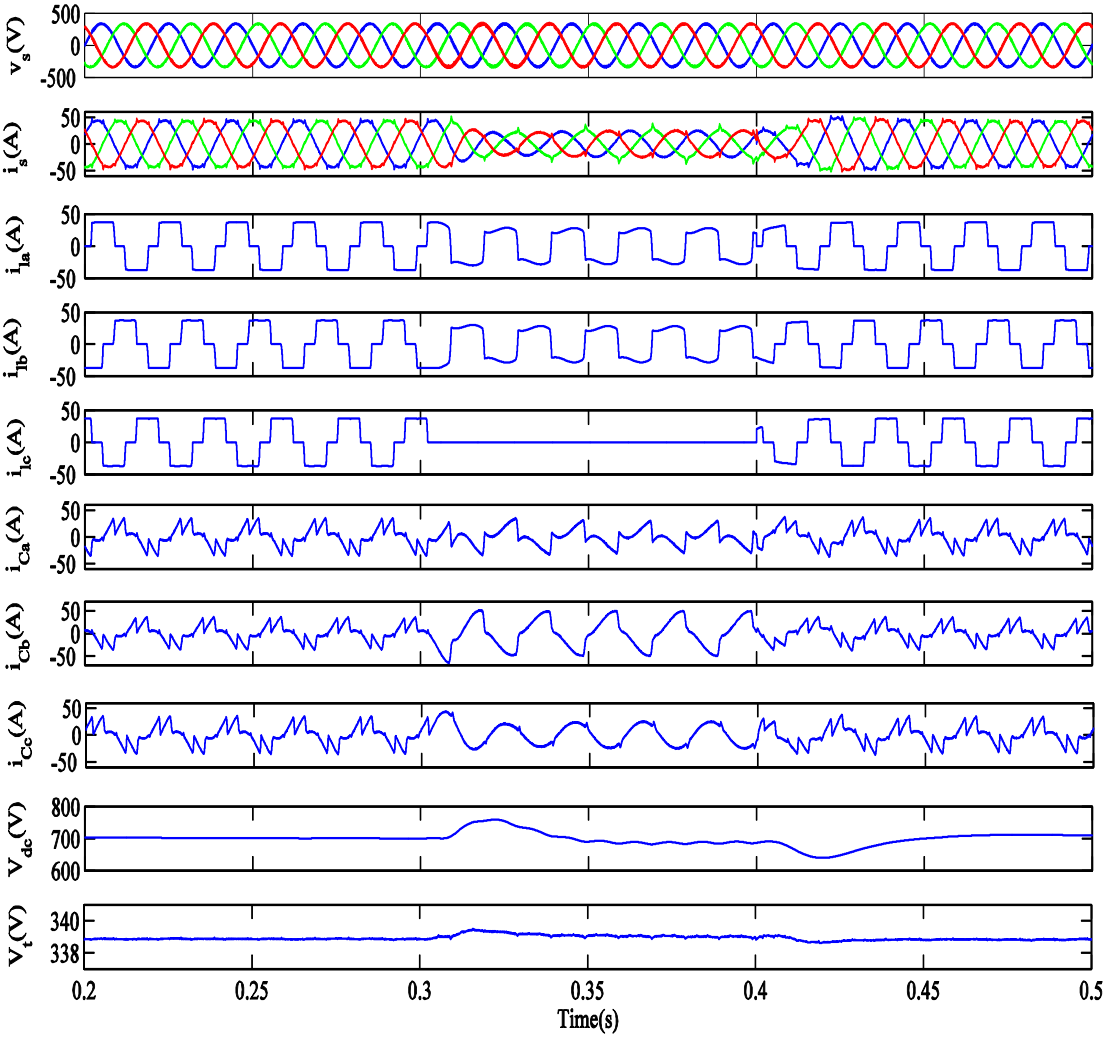


Fig. 4.38 Performance of DTATCOM in voltage regulation mode using conductance based control algorithm

condition supply currents are balanced and sinusoidal. These results show satisfactory performance of conductance based control algorithm is in voltage regulation mode.

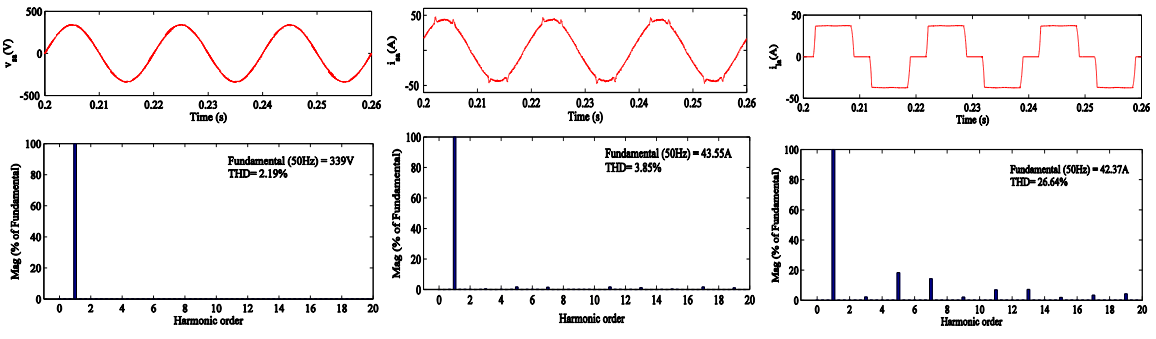
Fig. 4.39 shows the harmonic spectra of phase 'a' of PCC voltage (v_{sa}), supply current (i_{sa}) and load current (i_{la}) in PFC under nonlinear load. Total harmonic distortion (THD) of PCC voltage, supply current and load current are 2.19%, 3.85% and 26.64% respectively. It is observed from these results that THD of 3.85% in supply current is achieved, whereas there is 26.64% THD in load current. The THD values of PCC voltage and supply current are within the limit specified by IEEE-519 standard.

4.8.3.2 Experimental Performance of DSTATCOM With Conductance Based Control Algorithm

Experimental performance of DSTATCOM with conductance based control algorithm is presented here. This is divided into two parts. The first part presents the steady state performance of the system and the second part presents the dynamic performance of DSTATCOM with the control algorithm.

A. Steady State Performance of DSTATCOM With Conductance Based Control Algorithm

Fig. 4.40 shows the steady state performance of DSTATCOM under nonlinear load. Figs.



(a) (b) (c)

Fig. 4.39 Harmonic spectra of (a) PCC voltage, v_{sa} (b) supply current, i_{sa} (c) load current, $i_{la,}$ in voltage regulation mode

4.40(a), (c) and (e) show waveforms of phase 'a' of supply current (i_{sa}), load current (i_{la}) and compensator current (i_{Ca}) along with PCC voltage (v_{sa}). Figs. 4.40(b), (d) and (f) present harmonic spectra of supply current, load current and PCC voltage. These results show THD of 4.1%, 23.9% and 3.7% in supply current, load current and PCC voltage respectively. The improved THD is achieved in supply current due to action of DSTATCOM. The THD percentage in supply current is found within the limits specified by IEEE-519 standard.

Fig. 4.41 shows the simulation study of the system at (110V, L-L) rating which is for the same rating as the experimental system developed in the laboratory. These results present the waveforms of PCC voltages (v_{sa}), supply currents (i_{sa}), load currents (i_{sa}), compensator currents (i_{Ca}) and DC bus voltage (V_{dc}). Supply currents are observed to be balanced and sinusoidal during steady state (before t=0.3s) and under unbalanced load conditions (t=0.3s to t=0.4s). The voltage at the DC bus is regulated at the reference value of 200V due to the action of PI controller.

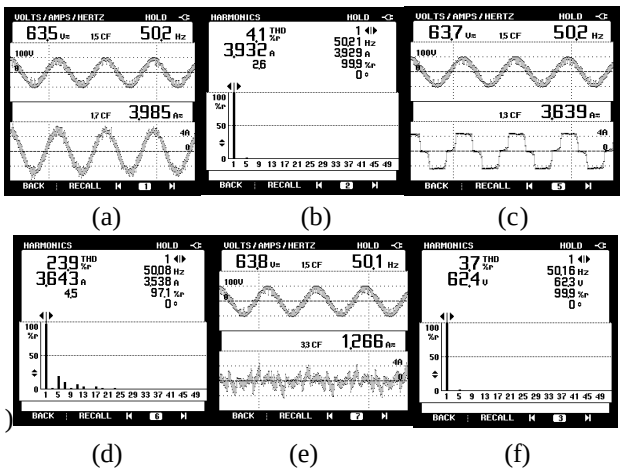


Fig. 4.40 Steady state performance of DSTATCOM (a), (c) and (e) i_{sa}, i_{la} and i_{Ca} along with v_{sa} (b), (d) and (f) Harmonic spectra of i_{sa}, i_{la} and v_{sa}.

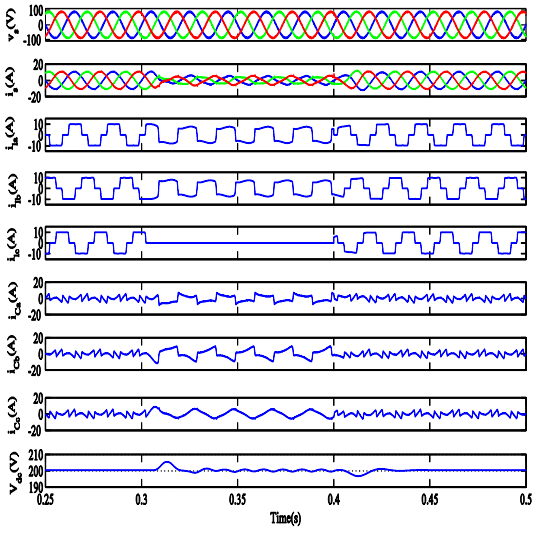


Fig. 4.41 Simulated performance of DSTATCOM in PFC mode

B. Dynamic Performance of DSTATCOM With Conductance Based Control Algorithm

Fig. 4.42 shows the dynamic performance of DSTATCOM under nonlinear load. Figs. 4.42 (a), (b) and (c) show the waveforms of supply currents (i_{sa}, i_{sb} and i_{sc}), load currents (i_{la}, i_{lb} and i_{lc}) and compensator currents (i_{Ca}, i_{Cb} and i_{Cc}) along with phase 'a' of PCC voltage (v_{sa}). These results are shown for steady state and unbalanced load conditions. It is observed from these results that supply currents are balanced and sinusoidal under different load conditions. Fig. 4.42(d) shows the waveforms of phase 'c' of supply current (i_{sc}), load current (i_{lc}) and compensator current (i_{Cc}) along with DC bus voltage (V_{dc}). These results show that the DC bus voltage achieves the reference value within a few cycles during unbalanced load condition.

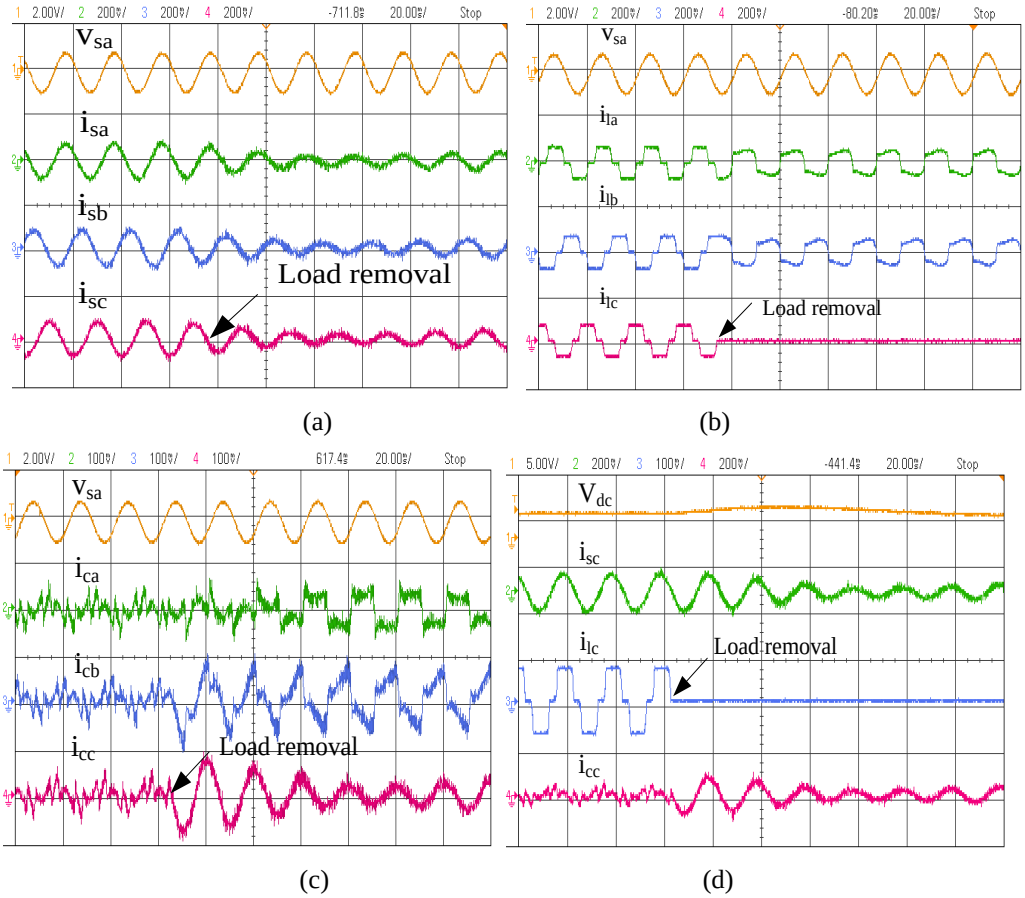


Fig. 4.42 Dynamic performance of DSTATCOM under nonlinear load

4.8.4 Performance of DSTATCOM With Instantaneous Symmetrical Component Theory Based Control Algorithm

Performance of DSTATCOM with instantaneous symmetrical component theory based control algorithm is presented here. Both simulation and experimental results are presented. Simulation study is performed in MATLAB using SIMULINK and SPS tool box. The experimental performance of the control algorithm is demonstrated on a prototype developed in the laboratory.

4.8.4.1 Simulated Performance of DSTATCOM in PFC and Voltage Regulation Modes

Simulated performance of DSTATCOM with ISCT based control algorithm is presented here. This is divided into three parts. The first part deals with the performance of the ISCT based control algorithm. The second and the third part deal with the performance of DSTATCOM in PFC and voltage regulation mode.

A. Performance of ISCT Based Control Algorithm for DSTATCOM

Fig. 4.43 presents the performance and intermediate signals with ISCT based control algorithm. This shows the waveforms of phase 'a' of PCC voltage (v_{sa}), phase 'c' of load current (i_{lc}), fundamental component of instantaneous active power (p_{dc}), output of DC bus PI controller (p_{loss}), reference active power (p_{ref}), output of ac bus PI controller (β), reference supply currents (i_s*) along with actual supply currents (i_s). These results are presented for steady state (before t=0.3s) and unbalanced (t=0.3s to t=0.4s) load conditions. Satisfactory performance of control algorithm is observed and reference currents are perfectly tracked by actual supply currents.

B. Performance of DSTATCOM in PFC Mode With ISCT Based Control Algorithm

Fig. 4.44 shows the performance of DSTATCOM in PFC mode with ISCT based control algorithm. Waveforms of PCC voltages (v_s), supply currents (i_s), load currents (i_{la}, i_{lb} and i_{lc}),

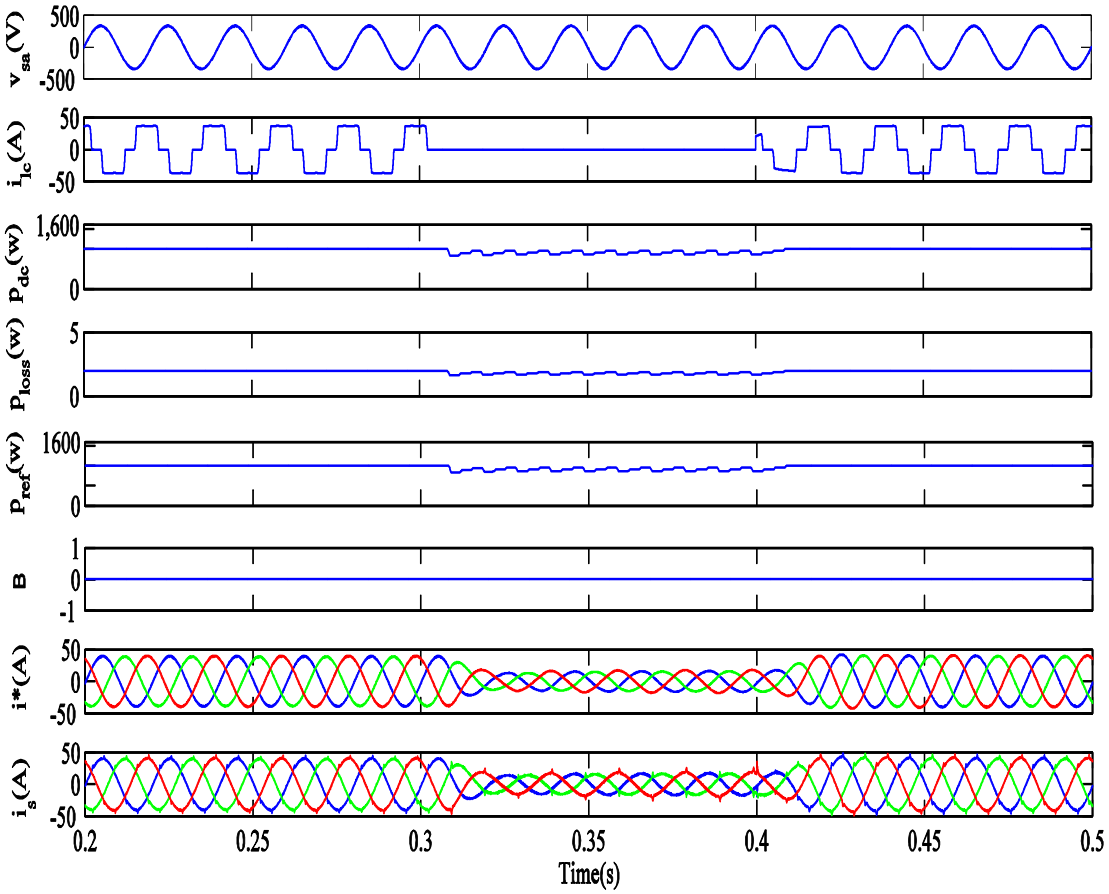


Fig. 4.43 Performance of ISCT based control algorithm for DSTATCOM

compensator currents (i_{Ca}, i_{Cb} and i_{Cc}) and voltage of self-sustained DC bus (V_{dc}) are shown in these results. It is observed from these results that under steady state condition upto t=0.3s the supply currents are balanced and sinusoidal. Moreover, the DC bus voltage is regulated at its reference value of 700V. An unbalancing in the load is created when phase 'c' of load is switched off. It is observed that the supply currents still remain balanced and sinusoidal but have a reduced magnitude during unbalanced load conditions.

Fig. 4.45 shows the harmonic spectra of phase 'a' of PCC voltage (v_{sa}), supply current (i_{sa}) and load current (i_{la}) in PFC mode under nonlinear load. Total harmonic distortions (THDs) of PCC voltage, supply current and load current are 1.61%, 2.82% and 26.61% respectively. It is observed from these results that the 2.82% THD in supply current is achieved, whereas there is

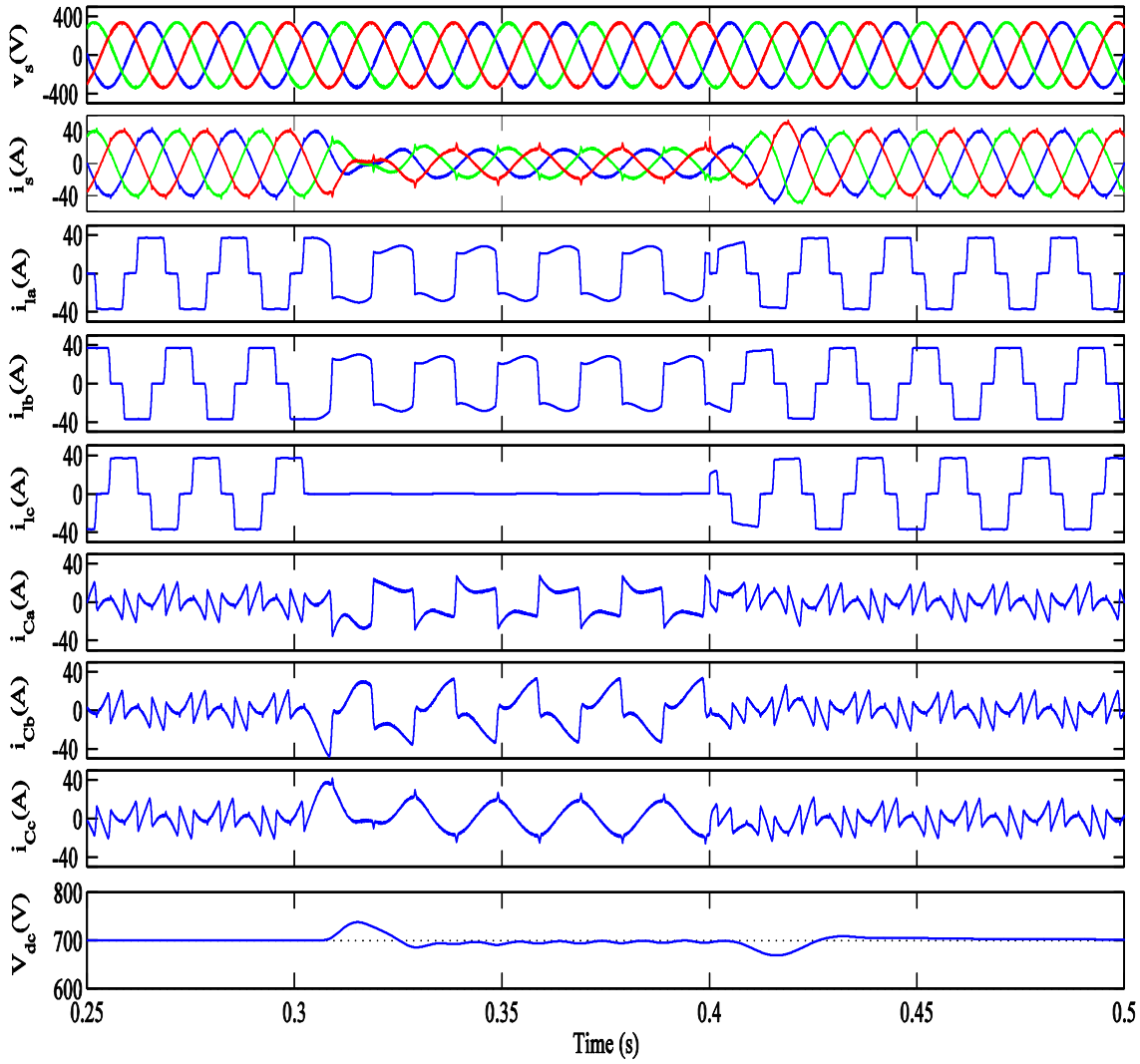
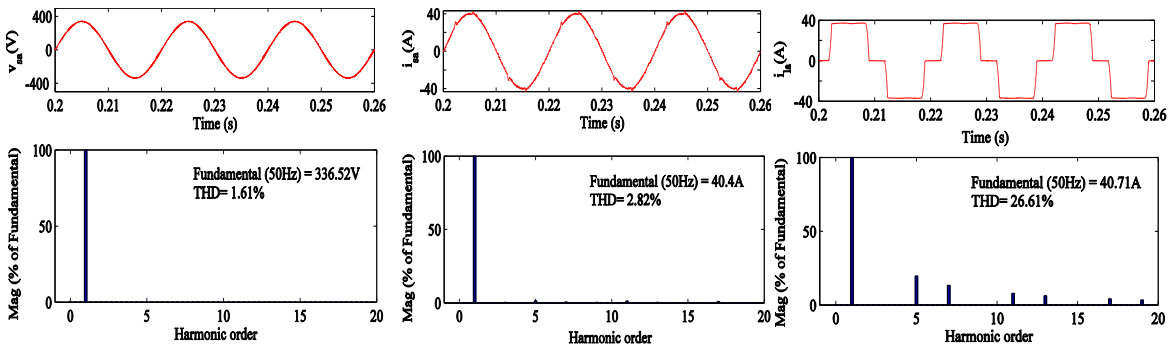


Fig. 4.44 Performance of DSTATCOM in PFC mode

26.61% THD in load current. The THD values of PCC voltage and supply current are within the limits specified by IEEE-519 standard.

C. Performance of DSTATCOM in Voltage Regulation Mode With ISCT Based Control Algorithm

Fig. 4.46 shows the performance of DSTATCOM in voltage regulation mode with ISCT based control algorithm. These results show the waveforms of PCC voltages (v_s), supply currents (i_s), load currents (i_{la}, i_{lb} and i_{lc}), compensator currents (i_{Ca}, i_{Cb} and i_{Cc}), DC bus voltage (V_{dc}) and amplitude of AC bus voltage (V_t). It is observed from these results that under steady state



(a) (b) (c)

Fig. 4.45 Harmonic spectra of (a) PCC voltage, v_{sa} (b) supply current, i_{sa} (c) load current, i_{la} in PFC mode

condition (before t=0.3s) the supply currents are balanced sinusoidal and the DC and AC bus voltages are regulated at their reference value of 700V and 338.78V. During unbalanced load condition (t=0.3s to t=0.4s), supply currents remain balanced and sinusoidal although they have reduced magnitude. Fig. 4.47 shows the harmonic spectra of phase 'a' of PCC voltage (v_{sa}), supply current (i_{sa}) and load current (i_{la}) in PFC under nonlinear load. Total harmonic distortions (THDs) of PCC voltage, supply current and load current are 1.76%, 3.33% and 26.73% respectively. It is observed from these results that 3.33% THD in supply current is achieved, whereas there is 26.73% THD in load current. The THD values of PCC voltage and supply current are within the limit of IEEE-519 standard.

4.8.4.2 Experimental Performance of DSTATCOM in PFC Mode

The performance of ISCT based control algorithm is tested experimentally on a developed prototype. The performance of DSTATCOM is tested in steady state and unbalanced load conditions. The detailed description of the experimental results is given as follows.

A. Steady State performance of DSTATCOM With ISCT Based Control Algorithm

Fig. 4.48 shows the steady state performance of DSTATCOM under nonlinear load. Figs. 4.48(a), (c) and (e) show waveforms of phase 'a' of supply current (i_{sa}), load current (i_{la}) and

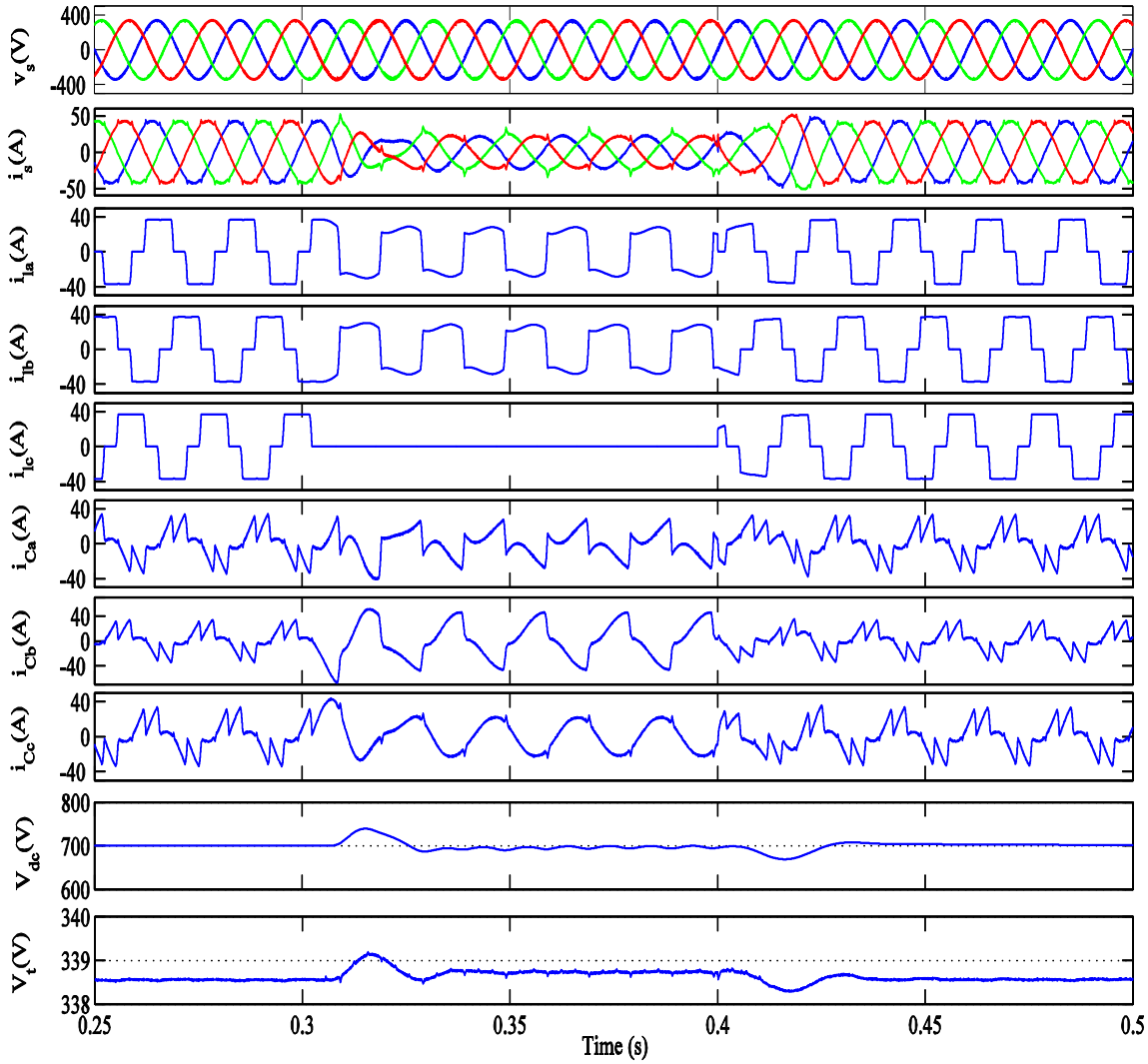
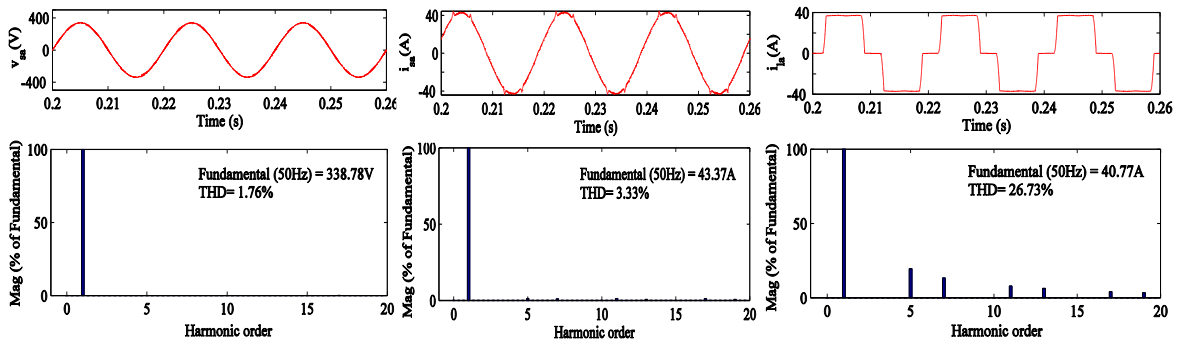


Fig. 4.46 Performance of DSTATCOM in voltage regulation mode

compensator current (i_{Ca}) along with PCC voltage (v_{sa}). Figs. 4.48(b), (d) and (f) present harmonic spectra of supply current, load current and PCC voltage. These results show THD of 4.2%, 22.5% and 3.4% in supply current, load current and PCC voltage respectively. Improved THD is achieved in supply current due to the action of DSTATCOM, and the supply currents meet the harmonic distortion standards specified by IEEE-519.

Fig. 4.49 shows the simulation study at 110V system for which experimental system is developed in the laboratory. These results present the waveforms of PCC voltages (v_{sa}), supply currents (i_{sa}), load currents (i_{sa}), compensator currents (i_{Ca}) and DC bus voltage (V_{dc}). Supply



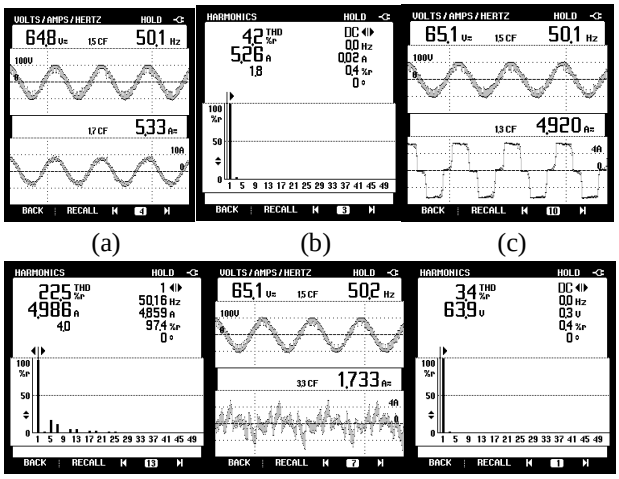
(a) (b) (c)

Fig. 4.47 Harmonic spectra of (a) PCC voltage, v_{sa} (b) supply current, i_{sa} (c) load current, i_{la} in voltage regulation mode

currents are observed to be balanced and sinusoidal during steady state (before t=0.3s) and unbalanced load conditions (t=0.3s to t=0.4s). The voltage at the DC bus is regulated at the reference value of 200V due to the action of PI controller.

B. Dynamic Performance of DSTATCOM With ISCT Based Control Algorithm

Fig. 4.50 shows the dynamic performance of DSTATCOM with ISCT based control algorithm under nonlinear load. Figs. 4.50 (a), (b) and (c) show the waveforms of supply currents (i_{sa}, i_{sb} and i_{sc}), load currents (i_{la}, i_{lb} and i_{lc}) and compensator currents (i_{Ca}, i_{Cb} and i_{Cc}) along with phase



(a) (b) (c)

(d) (e) (f)

Fig. 4.48 Steady state performance of DSTATCOM (a), (c) and (e) i_{sa}, i_{la} and i_{Ca} along with v_{sa} (b), (d) and (f) Harmonic spectra of i_{sa}, i_{la} and v_{sa}.

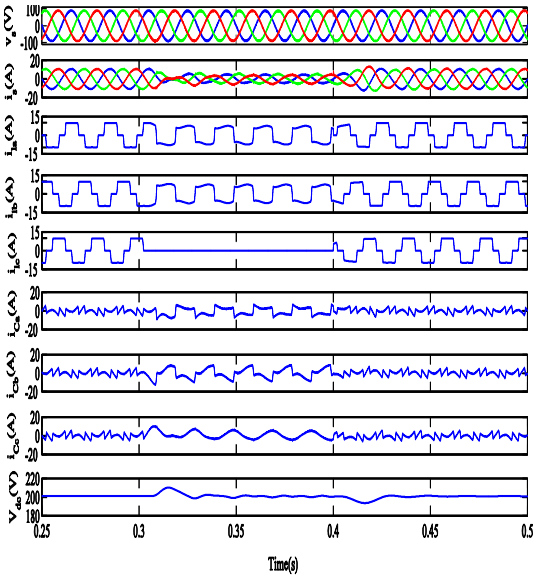


Fig. 4.49 Simulated performance of DSTATCOM in PFC mode

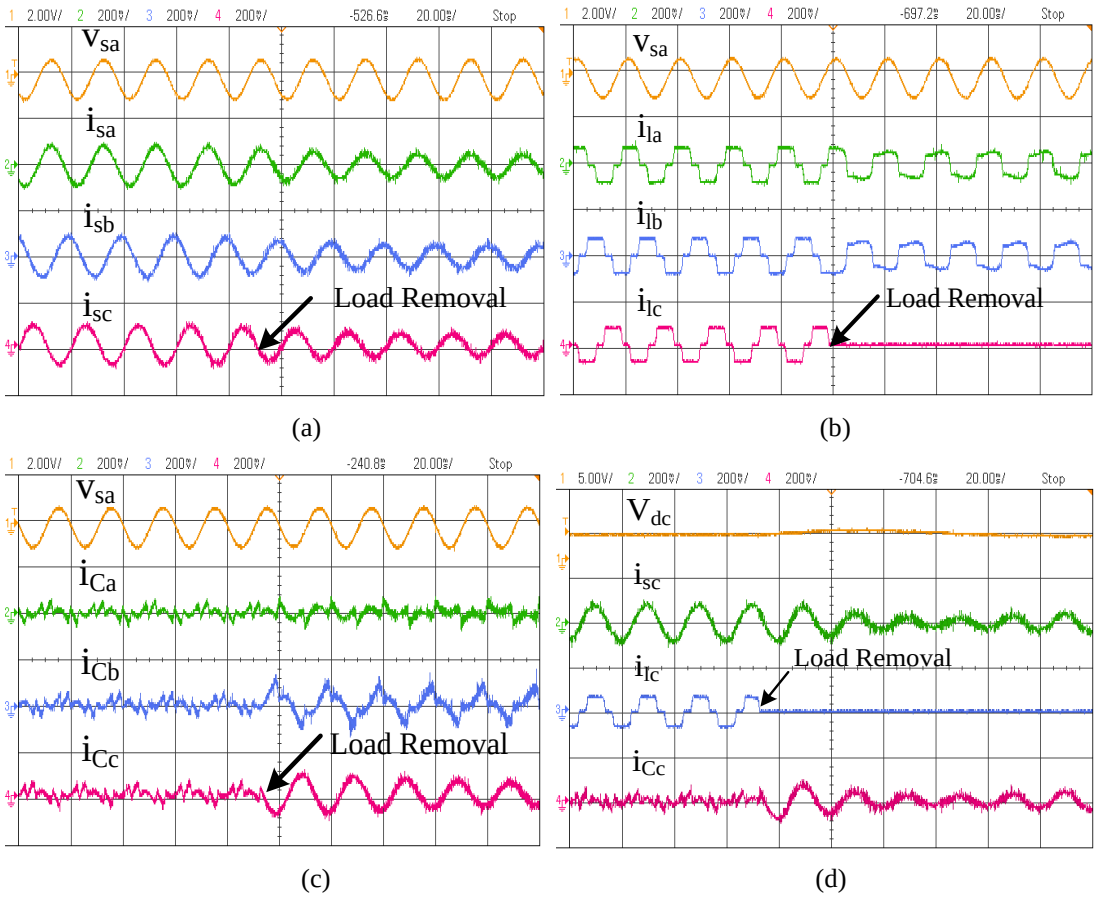


Fig. 4.50 Dynamic performance of DSTATCOM under nonlinear load

'a' of PCC voltage (v_{sa}). These results are observed under steady state and unbalanced load conditions. It is observed from these results that the supply currents are balanced and sinusoidal under different loading conditions. Fig. 4.50(d) shows the waveforms of phase 'c' of supply current (i_{sc}), load current (i_{lc}) and compensator current (i_{Cc}) along with DC bus voltage (V_{dc}). These results show that the DC bus voltage achieves the reference value of 200V within few cycles during unbalanced load condition.

4.9 CONCLUSIONS

The classification of control algorithms and performance of conventional control algorithms have been presented in this chapter. The control algorithms have been classified based on basic

methodology used for them. The control algorithms categorized under conventional control algorithms are based on power balance theory, instantaneous reactive power theory, conductance based and symmetrical component theory based. Detailed mathematical formulation along with their block diagram and simulation models of conventional control algorithms have been presented in this chapter. The performance of DSTATCOM for improvement of several power quality problems such as harmonic elimination, reactive power compensation and load balancing have been presented with conventional control algorithms in PFC and voltage regulation modes. Experimental verification of the control algorithms have been performed with the prototype developed in the laboratory. The results have been shows sinusoidal and balanced supply currents in steady state and unbalance load conditions. The test results show THD of 4.2%, 4.2%, 4.1% and 4.2% in supply current in case of PBT, IRPT, conductance based and ISCT based control algorithms.

CHAPTER-V
ADAPTIVE THEORY BASED CONTROL ALGORITHMS FOR DSTATCOM

5.1 GENERAL

In previous chapter, classification of different types of control algorithms has been discussed. The development of conventional control algorithms along with detailed description of simulation and experimental results have been reported in earlier chapter. This chapter deals with the adaptive theory based control algorithms for DSTATCOM. The adaptive theory based control approach provides self-adjustment of controller parameters in real time to achieve desired performance in steady state and dynamic load conditions. This chapter includes the mathematical formulation of adaptive theory based control algorithms, their modeling in Matlab/Simulink and implementation using DSP. This class of algorithms include Wiener filter, least mean square (LMS) and variable step size least mean square (VSSLMS) for control of DSTATCOM. The fundamental active and reactive power components of load currents are estimated and their average weights are computed. These average weights are used to generate reference supply currents. Various functions of DSTATCOM such as harmonics elimination, reactive power compensation and load balancing are demonstrated in power factor correction (PFC) and voltage regulation modes.

A model of three phase VSC based DSTATCOM connected at point of common coupling (PCC) is developed and its performance with adaptive theory based control algorithms is simulated in MATLAB environment using SIMULINK and Sim Power System (SPS) tool boxes. Hardware implementation of three phase DSTATCOM consists of IGBTs (Insulated Gate Bipolar Transistors) based VSC (Voltage Source Converter), Hall Effect voltage and current sensors with appropriate buffer circuitry, interfacing inductors, three phase nonlinear load and DSP(dSPACE 1104R&D) controller board with TMS320F240 as a slave DSP.

5.2 CONFIGURATION AND OPERATING PRINCIPLE OF DSTATCOM

The DSTATCOM is a shunt connected device where IGBTs based voltage source converter (VSC) is used. Fig. 5.1 shows the schematic diagram of VSC based DSTATCOM. A three-phase, AC mains with grid impedance, shown using series R_s-L_s branch, feeds a three phase nonlinear load. The DSTATCOM is designed using three-leg VSC which uses six insulated gate bipolar transistors (IGBTs) with anti-parallel diodes and DC link capacitor (C_{dc}) at DC side. Interfacing inductors (L_f) are used at the AC side of VSC, which couple the VSC to the grid. High frequency switching noise generated by switching of IGBTs of VSC is reduced with the help of series connected capacitive (C_f) and resistive (R_f) elements at the point of common

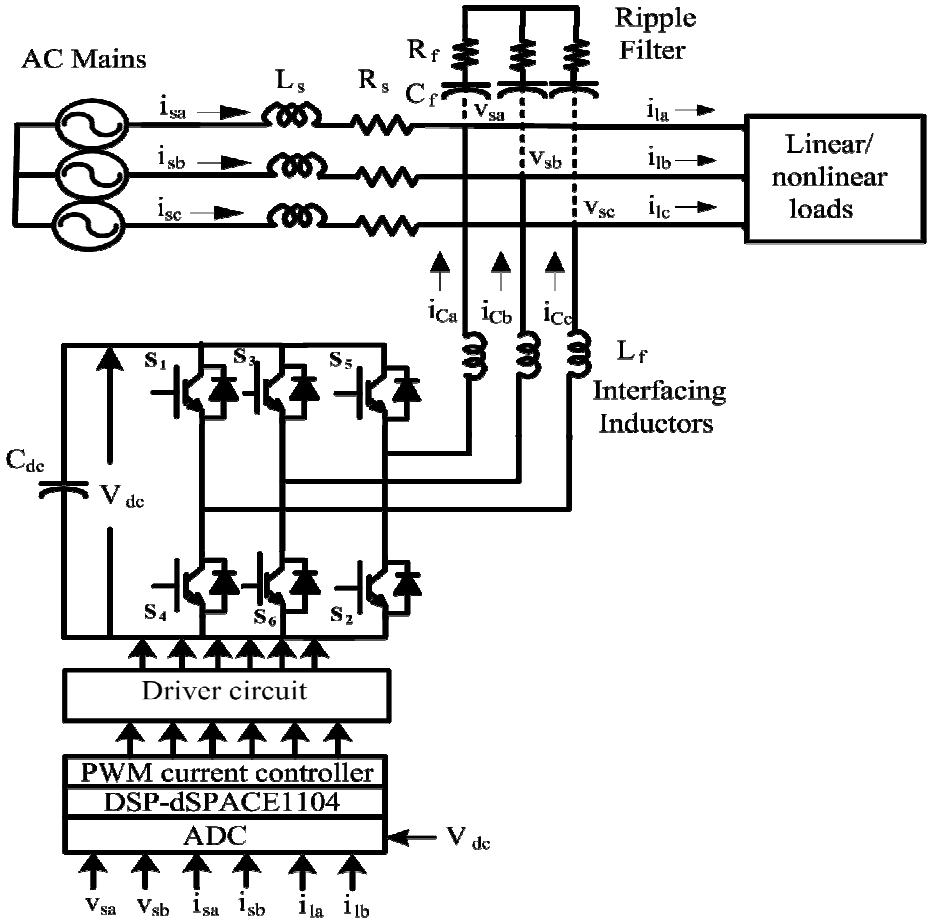


Fig. 5.1 Schematic diagram of the DSTATCOM

coupling (PCC). The nonlinear load is represented as uncontrolled bridge rectifier with series R-L branch. Three phase voltages at PCC (v_{sa} and v_{sb}), supply currents (i_{sa} and i_{sb}), load currents (i_{la}, i_{lb}) and DC bus voltage (V_{dc}) are sensed and given to the DSP. These signals are processed by DSP to generate appropriate switching pulses for three phase VSC. A hardware prototype of the system is implemented in the laboratory using DSP (dSPACE 1104 R&D controller board). Hall Effect voltage and current sensors are used to sense real time feedback signals. The design of sensor circuitry and various components of DSTATCOM are presented in section 5.5.1. Switching pulses generated by DSP are used to derive three phase VSC, which generates compensator currents (i_{Ca}, i_{Cb} and i_{Cc}).

5.3 BASIC PRINCIPLE AND MATHEMATICAL FORMULATION OF ADAPTIVE THEORY BASED CONTROL ALGORITHMS

In adaptive theory based control algorithms, the estimation of fundamental active and reactive power components of load currents are based on adaptive parameters of input signals which could be fixed or variable parameters. The advantage of using fixed parameters is reduced complexity which makes less computational burden on DSP processor. However, there is tradeoff between convergence rate and steady state error in case of fixed parameters. The advantages of using variable parameters are to achieve fast convergence and less steady state error, but these results in increased computational burden on DSP processor. This category of control algorithms include Wiener filter, Least Mean Square (LMS) and variable step size least mean square (VSSLMS) based algorithms for control of DSTATCOM.

5.3.1 Wiener Filter Based Control Algorithm for DSTATCOM [154-155]

This Wiener filtering technique is known as linear optimization discrete time filter. This requires a priori information about the statistics of the data to be processed. These filters are optimum

because of minimizing an appropriate function of error, known as mean square error (MSE). A control algorithm based on Wiener filter is proposed for the extraction of fundamental component of reference supply currents from distorted load currents.

Mathematical formulation of Wiener filter based control algorithm is given here for weight estimation and reference currents generation for control of the DSTATCOM. This section is divided into three parts. The first part presents estimation of reference supply currents corresponding to fundamental active power components of load currents. The second part presents estimation of reference supply currents corresponding to reactive power components of load currents and generation of reference supply currents along with switching pulses is presented in third part.

5.3.1.1 Estimation of Fundamental Active Power Components of Reference Supply Currents Using Wiener Filter Based Control Algorithm

Fig. 5.2 shows the block diagram of control algorithm where voltages (v_{sa}, v_{sb} and v_{sc}) at the PCC are sensed and their amplitude is calculated as given,

$$V_t = \sqrt{2(v_{sa}^2 + v_{sb}^2 + v_{sc}^2)/3} \tag{5.1}$$

Using PCC voltage magnitude, the unit inphase components are calculated as,

$$u_{pa} = v_{sa}/V_t;\ u_{pb} = v_{sb}/V_t;\ \text{and}\ u_{pc} = v_{sc}/V_t \tag{5.2}$$

The voltage at DC bus (V_{dc}) of the VSC used as a DSTATCOM is sensed and subtracted from the reference DC bus voltage (V_{dc}^*) for generation of error signal (V_{de}). The error signal is passed through the proportional integral (PI) controller. The output of PI controller (w_{pdc}) regulates the DC bus voltage at reference value and also meets VSC losses. The PI controller output at n^{th} sampling instant is given as,

$$w_{pdc}(n) = w_{pdc}(n-1) + k_{pd}\{V_{de}(n) - V_{de}(n-1)\} + k_{id}\{V_{de}(n)\} \quad (5.3)$$

where k_{pd} and k_{id} are proportional and integral gains of DC bus PI controller.

Extraction of weights corresponding to fundamental active power component of load current is given as follows. If $i_l(n)$ is the load current and $i_{est}(n)$ is estimated fundamental load current at n^{th} sampling instant then the mean square error {J(n)}, which is function of error {e(n)}, is given as,

$$J(n) = E\{(i_l(n) - i_{est}(n))\} = E\{e^2(n)\} \quad (5.4)$$

where $e(n)$ is the error between the sensed load current, $i_l(n)$ and estimated load current, $i_{est}(n)$. The estimated current quantity can be expressed as,

$$i_{est}(n) = \sum_{m=0}^{M-1} w_m x(n-m) = w^T x(n) \quad (5.5)$$

where $w = [w_1, w_2, \ldots w_{M-1}]^T$ represent M×1 vector of the filter coefficients or weights,

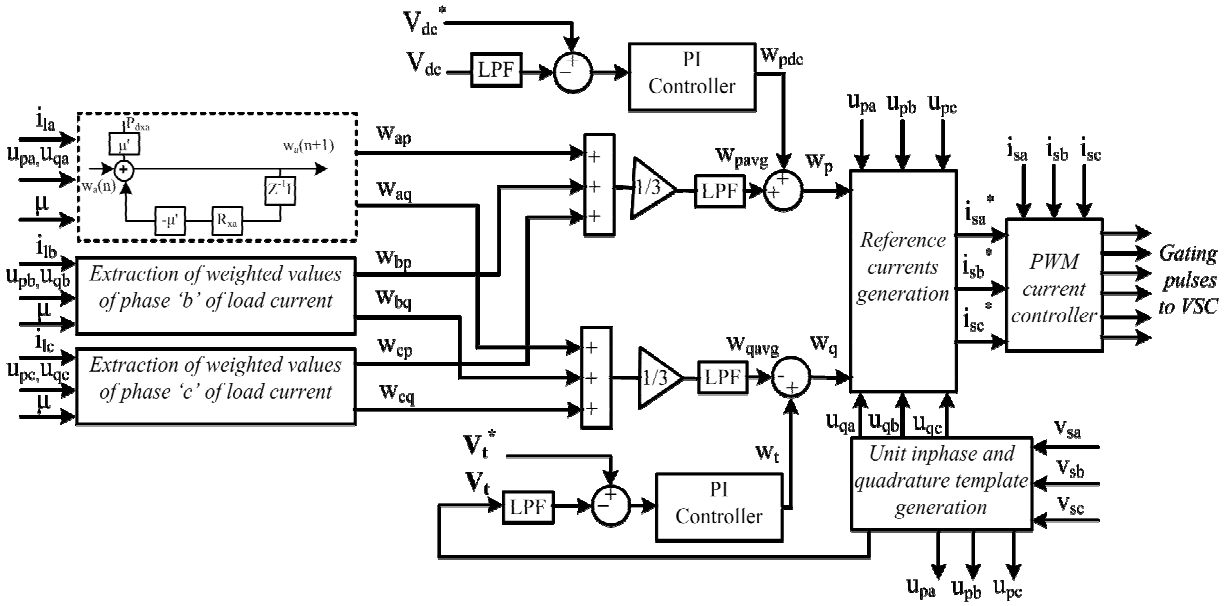


Fig. 5.2 Block diagram of Wiener filter based control algorithm for DSTATCOM

$x(n) = [x(n), x(n-1) \ldots x(n-M+1)]^T$ is M×1 vector of the input parameters and M is the order of the filter.

From these equations mean square error for the estimation of fundamental load current is given as,

$$J(n) = E\{[i_l(n) - w^T x(n)]^2\}$$

$$= E\{[i_l(n) - w^T x(n)][i_l(n) - w^T x(n)]^T\}$$

$$= E\{{i_l}^2(n)\} - 2w^T E\{i_l(n)x(n)\} + w^T E\{x(n)x^T(n)\}w \quad (5.6)$$

It is supposed that the filter coefficients do not change with time, based upon this Eqn. (5.6) is modified as,

$$J(n) = \sigma_d^2 - 2w^T P_{dx} + w^T R_x w \quad (5.7)$$

where σ_d^2 is variance of the desired quantity,$i_l(n)$, $P_{dx} = [p_{dx}(0), p_{dx}(1), \ldots, p_{dx}(M-1)]^T$ is the cross-correlation vector between desired quantity and input vector and R_x is the correlation matrix of the input data, which is a symmetric matrix because the random process is supposed to be stationary.

The steepest-descent method is used to find the minimum value of mean square error (MSE) (J_{min}). The weights in the weight vector achieve their optimum values at the minimum MSE. The update is started with initial value $w(0)$ and mean square error surface point corresponding to the gradient vector, $\nabla J(w(0))$is computed. The value of gradient vector $-\nabla J(w(0))$ is computed and added with $w(0)$ to obtain $w(1)$. This process is continued until optimum value of weights

corresponding to fundamental active and reactive components of load currents are achieved. If $w(n)$ is the filter coefficient vector at n^{th} sampling instant then its update is given as,

$$w(n+1) = w(n) - \mu\nabla J\big(w(n)\big) \tag{5.8}$$

where $w(n+1)$ is the updated value of the filter-coefficient vector. The gradient vector $\{\nabla J\big(w(n)\big)\}$ is given as,

$$\nabla J\big(w(n)\big) = -2P_{dx} + 2R_x w(n) \tag{5.9}$$

From Eqn. (5.8) and Eqn. (5.9), updated weights can be expressed in terms of previous weights as,

$$w(n+1) = w(n) + 2\mu[P_{dx} - R_x w(n)] = [I - 2\mu R_x]w(n) + 2\mu P_{dx} \tag{5.10}$$

where μ is the step size and I is the identity matrix. The value of step size parameter (μ) must be less than 1 for convergence. The auto-correlation matrix (R_x) and the cross-correlation vector (P_{dx}), applied in steepest-descent algorithm have to be estimated at the start of the algorithm.

The optimum weights (w_{ap}, w_{bp} and w_{cp}) corresponding to fundamental active component of load currents for the three phases are obtained using the weight update rule given in Eqn. (5.10) as,

$$w_{ap}(n+1) = [I - 2\mu R_{xa}]w_{ap}(n) + 2\mu P_{dxa} \tag{5.11}$$

$$w_{bp}(n+1) = [I - 2\mu R_{xb}]w_{bp}(n) + 2\mu P_{dxb} \tag{5.12}$$

$$w_{cp}(n+1) = [I - 2\mu R_{xc}]w_{cp}(n) + 2\mu P_{dxc} \tag{5.13}$$

The average magnitude of weights (w_{pavg}) corresponding to active power components (w_{ap}, w_{bp} and w_{cp}) is given as,

$$w_{pavg} = (w_{ap} + w_{bp} + w_{cp})/3 \quad (5.14)$$

The total reference weight (w_p) corresponding to active power component is obtained by adding the average weight (w_{pavg}) and the output of DC bus PI controller (w_{pdc}) as,

$$w_p = w_{pavg} + w_{pdc} \quad (5.15)$$

The reference currents $\left(i_{pa}^*, i_{pb}^* \text{and } i_{pc}^*\right)$ of the three phases corresponding to fundamental active component can be computed by using Eqn. (5.2) and Eqn. (5.15) as,

$$i_{pa}^* = w_p u_{pa},\ i_{pb}^* = w_p u_{pb} \text{ and } i_{pc}^* = w_p u_{pc} \quad (5.16)$$

These active reference supply currents $\left(i_{pa}^*, i_{pb}^* \text{and } i_{pc}^*\right)$ are used to estimate reference supply currents.

5.3.1.2 Estimation of Fundamental Reactive Power Components of Reference Supply Currents Using Wiener Filter Based Control Algorithm

The unit quadrature vectors of PCC voltages are calculated from unit inphase voltages (u_{pa}, u_{pb} and u_{pc}) as,

$$u_{qa} = -u_{pb}/\sqrt{3} + u_{pc}/\sqrt{3} \quad (5.17)$$

$$u_{qb} = \sqrt{3}\,u_{pa}/2 + (u_{pb} - u_{pc})/2\sqrt{3} \quad (5.18)$$

$$u_{qc} = -\sqrt{3}\,u_{pa}/2 + (u_{pb} - u_{pc})/2\sqrt{3} \quad (5.19)$$

The voltage regulation using DSTATCOM can be performed using another PI controller. The error (v_{te}) between amplitude of PCC voltage (V_t) and its reference quantity (V_t^*) is calculated. The error is passed through a PI controller and output (w_t) can be computed at n^{th} sampling instance as,

$$w_t(n) = w_t(n-1) + k_{pq}\{v_{te}(n) - v_{te}(n-1)\} + k_{iq}\{v_{te}(n)\} \quad (5.20)$$

where k_{pq} and k_{iq} are proportional and integral gains for AC bus voltage PI controller.

The optimum weights (w_{aq}, w_{bq} and w_{cq}) corresponding to fundamental reactive power component of load currents are also calculated by using Eqn. (5.10) as,

$$w_{aq}(n+1) = [I - 2\mu R_{xa}]w_{aq}(n) + 2\mu P_{dxa} \quad (5.21)$$

$$w_{bq}(n+1) = [I - 2\mu R_{xb}]w_{bq}(n) + 2\mu P_{dxb} \quad (5.22)$$

$$w_{cq}(n+1) = [I - 2\mu R_{xc}]w_{cq}(n) + 2\mu P_{dxc} \quad (5.23)$$

The average weight (w_{qavg}) of reactive power component of load current can be calculated from the amplitude of load reactive weight components (w_{aq}, w_{bq} and w_{cq}) such as,

$$w_{qavg} = (w_{aq} + w_{bq} + w_{cq})/3 \quad (5.24)$$

The amplitude of reactive power component of reference supply currents can be calculated by subtracting the output of PI controller (w_t), which is leading reactive power component used to compensate for voltage drop due to supply impedance and loading on the system and average reactive weight (w_{qavg}) given as,

$$w_q = w_t - w_{qavg} \quad (5.25)$$

The reference current corresponding to fundamental reactive power component can be calculated using Eqn. (5.17) to Eqn. (5.19) and Eqn. (5.25) as,

$$i_{qa}^* = w_q u_{qa},\ i_{qb}^* = w_q u_{qb} \text{ and } i_{qc}^* = w_q u_{qc} \quad (5.26)$$

These fundamental reactive components of reference supply currents are used with fundamental active components of reference supply currents to generate reference supply currents given as follows.

5.3.1.3 Generation of Reference Supply Currents and Switching Pulses

The summation of active (i_{pa}^*, i_{pb}^* and i_{pc}^*) and reactive (i_{qa}^*, i_{qb}^* and i_{qc}^*) components of reference supply currents using Eqn. (5.16) and Eqn. (5.25) gives the total reference supply currents (i_{sa}^*, i_{sb}^* and i_{sc}^*) as,

$$i_{sa}^* = i_{pa}^* + i_{qa}^*, i_{sb}^* = i_{pb}^* + i_{qb}^* \text{ and } i_{sc}^* = i_{pc}^* + i_{qc}^* \quad (5.27)$$

The supply currents (i_{sa}, i_{sb} and i_{sc}) are sensed and compared with these reference supply currents (i_{sa}^*, i_{sb}^* and i_{sc}^*) and the current errors (i_{sae}, i_{sbe} and i_{sce}) are generated. These current errors are passed through PWM current controller, which generates switching pulses for three phase VSC used as DSTATCOM.

5.3.2 Least Mean Square Based Control Algorithm for DSTATCOM [143]

The least mean square (LMS) is a linear adaptive technique. It consists of an adaptive process. It involves automatic adjustment of the system parameters in accordance with the estimation error. There are several variants of least mean square techniques but the most popular techniques include the basic least mean square, normalized least mean square (NLMS) and signed error least mean square (SLMS). These variants of LMS techniques are used to estimate weights corresponding to fundamental active and reactive power components of load currents. The estimated weights are used to generate reference supply currents and finally switching pulses for three phase DSTATCOM.

This section deals with the mathematical formulation of LMS based control algorithm for three-phase DSTATCOM. The Least Mean Square (LMS) based control algorithms are developed. Different methods of LMS such as basic LMS, normalized LMS (NLMS) and signed error LMS (SLMS) based control algorithms are designed and verified for DSTATCOM. Detailed block diagram of control algorithm is shown in Fig. 5.3 and basic building block of LMS based control method is shown in Fig. 5.4.

5.3.2.1 Estimation of Fundamental Active Power Components Reference Supply Currents From LMS Based Control Algorithm

The voltages at PCC (v_{sa}, v_{sb} and v_{sc}) are sensed and magnitude, V_t is calculated as,

$$V_t = \sqrt{2(v_{sa}^2 + v_{sb}^2 + v_{sc}^2)/3} \tag{5.28}$$

Unit inphase templates are calculated from PCC voltages and their magnitude same as discusses in section 5.3.1. Voltage at DC bus (V_{dc}) is sensed and compared with reference DC bus voltage (V_{dc}^*), thus the generated error is passed through PI controller. The output (w_{pdc}) of DC bus PI controller is same as given in section 5.3.1. Fundamental weights corresponding to active and reactive power components of load currents are calculated from variants of LMS techniques given as follows.

A. Basic Least Mean Squares Approach

Consider the load connected to the three-phase system to be nonlinear in nature. The periodic nonlinear load current can be regarded as the sum of several harmonics components. The Fourier analysis of the load current shows the presence of harmonics of order fifth, seventh, eleventh, thirteenth etc. with diminishing magnitude. Mathematically, it is represented at n^{th} sampling time as,

$$i_h = a_h \cos h\omega n + b_h \sin h\omega n \tag{5.29}$$

where 'h' is the order of the harmonics. The components a_h and b_h represent the weights associated with harmonics of order 'h'. The fundamental current can be extracted from the load current and represented as,

$$i_1 = a_1 \cos \omega n + b_1 \sin \omega n \tag{5.30}$$

where a_1 and b_1 represent the weights associated with cosine and sine frequency components of fundamental component of load current. The knowledge of these weights and the cosine and sine components of the fundamental and harmonics terms can help to estimate the load current (i_{est}) as,

$$i_{est} = w^T x(n) \tag{5.31}$$

The estimated load current is obtained from these two vectors $x(n)$ and weights w, which can be

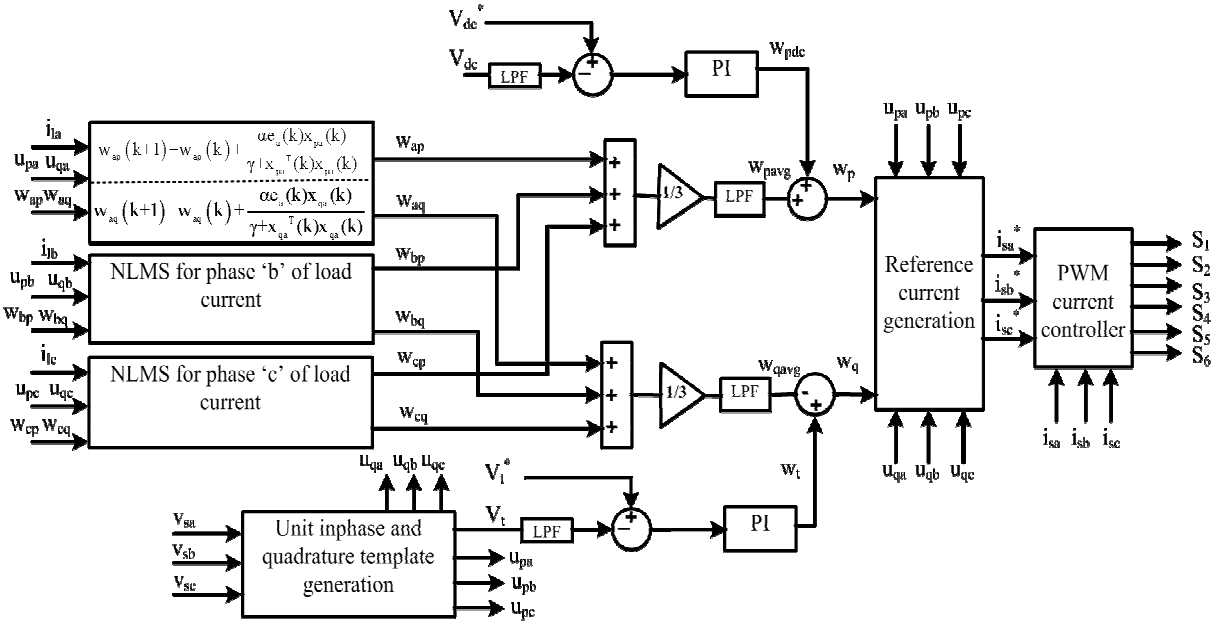


Fig. 5.3 Block Diagram of the control algorithm for DSTATCOM using NLMS based control algorithm

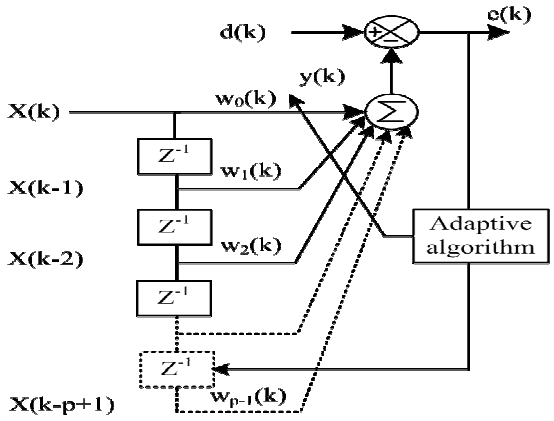


Fig. 5.4 Block diagram of basic LMS method

depicted as,

$$x(k) = [cosnw \;\; sinnw \; cos5nw \; sin5nw \ldots] \tag{5.32}$$

$$w = [w_{a1} w_{b1} w_{a5} w_{b5} \ldots] \tag{5.33}$$

The fundamental active and reactive components of load current correspond to weights w_{a1}, w_{b1}. Other weights such as w_{ah}, w_{bh}... etc. corresponds to '*h*' order component. A suitable algorithm can be used to isolate these weights and to obtain the fundamental or higher order harmonics. Selective harmonics extraction as well as compensation can be carried out from the weight vector.

The error between the estimated (i_{est}) and the sensed load current (i_l) is represented as,

$$e(n) = i_l - i_{est} \tag{5.34}$$

The adaptive algorithm is now applied to find the optimal weight vector. The load current is now estimated using the LMS algorithm such that the estimated load current is as close to the sensed value as is theoretically possible. Including 1^{st}, 5^{th}, 7^{th}, 11^{th} and 13^{th} order harmonics result in lower error and an accurate estimation of load current. The representation of weights, *w(n)* and input vector *x(n)* is depicted in Fig. 5.4. In this figure, the output *y(n)* denotes the estimated load

current (i_{est}) from the weights and input vector *x(n)*. The error is computed as the difference of sensed load current, *d(n)* and the estimated current, *y(n)*.

Considering that the cost function is to be minimised which is $J(n)$ and the mean square error (MSE) has to be minimised as,

$$J(n) = E\{d(n) - w^T x(n)\}^2$$

$$= E\{d^2(n) + w^T R(n) w(n) - 2w^T p(n)\} \quad (5.35)$$

where $R((n) = E[x(n)x^T(n)]$is the correlation matrix of the observed values of load current components and $p(n) = E[d(n)x^T(n)]$denotes the cross-correlation vector between the observed input vector $x(n)$ and the desired vector $d(n)$.

Using the steepest descent method, if $w(n)$ is the weight coefficient at step, n^{th} instant then its updated value $w(n+1)$ at the $(n+1)^{th}$ instant can be expressed as,

$$w(n+1) = w(n) - \mu' \nabla J(n) \quad (5.36)$$

and $$\nabla J(n) = -2\,p(n) + 2R(n)w(n) \quad (5.37)$$

Hence, the weight updation using Eqn. (5.36) becomes,

$$w(n+1) = w(n) + 2\mu' p(n) - 2\,\mu\, R(n) w(n)$$

$$= w(n) + 2\,\mu' x(n)[\, d(n) - w^T x(n)]$$

$$= w(n) + \mu e(n) x(n) \quad (5.38)$$

where $e(n)$ denotes the error $e(n) = d(n) - w^T x(n)$ and step size $\mu = 2\,\mu'$. The basic LMS recursive relation for updating the weight coefficients is given by Eqn. (5.38).

B. Normalized Least Mean Square Algorithm

A problem commonly encountered in the design of adaptive filters is the selection of step size parameter, μ. In the harmonic reduction problem, a step size parameter $\mu(n)$ is used. To evaluate the a *posteriori* estimation error $\acute{\varepsilon}$ at the n^{th} instant,

$$\acute{\varepsilon}(n) = d(n) - w(n+1)^T x(n) \tag{5.39}$$

Using $d(n) = w^T x(n)$ in Eqn. 5.39, this can be modified as,

$$\acute{\varepsilon}(n) = \varepsilon(n)\left[1 - \mu(n)x^T(n)x(n)\right] \tag{5.40}$$

If $\mu(n) = \frac{1}{x^T(n)x(n)}$ then $\acute{\varepsilon}(n)$ becomes zero. Under this condition, the recursive weight equation as depicted in Eqn. (5.38) is modified as,

$$w(n+1) = w(n) + \frac{e(n)x(n)}{x^T(n)x(n)} \tag{5.41}$$

Another variation of this NLMS algorithm is shown in Eqn. (5.42) where α is the new normalized adaptation constant and γ is a small positive number.

$$\mathrm{w(n+1) = w(n) + \frac{\alpha e(n)x(n)}{\gamma + x^T(n)x(n)}} \tag{5.42}$$

The need of γ arises to ensure the weight updation does not become excessively large even if $x^T(n)\,x(n)$ becomes small temporarily.

C. Sign Error Least Mean Square Algorithm

This LMS is also a modified version of the basic LMS. The differences arise in terms of simplicity in implementation and a more robust operation. The three versions of Sign Error LMS viz. Sign Data LMS, Sign Error LMS and Sign- Sign LMS are presented as,

$$\mathrm{w(n+1) = w(n) + \mu \hat{e}(n)x(n)} \tag{5.43}$$

where

$$\hat{e}(n) = sgn[d(n) - y(n)] \tag{5.44}$$

$$= 1 \; if \; d(n) = y(n) > 0$$

$$= 0 \; if \; if \; d(n) = y(n) = 0$$

$$= -1 \; if \; d(n) - y(n) < 0$$

Signed Data LMS uses the *sgn* function in calculation of *x* and not in error *e(n)*. This function is represented as,

$$w(n+1) = w(n) + \mu e(n) sgn[x(n-i)] \tag{5.45}$$

Sign- Sign LMS is also a modified version of this with *sgn* function denoted in both *e(n)* and *x(n)* as,

$$w(n+1) = w(n) + \mu \, sgn[e(n)] sgn[x(n-i)] \tag{5.46}$$

These schemes differ in the number of mathematical operations such as addition, multiplication and speed of convergence. All schemes are dependent on the choice of step size parameter (μ). The updated weights are used in the feedback loop to obtain the reference currents.

The weights (w_{ap}, w_{bp} and w_{cp}) corresponding to active power component of load currents are extracted from one of the above presented technique and their average weight (w_{pavg}) is given as,

$$w_{pavg} = \frac{w_{ap} + w_{bp} + w_{cp}}{3} \tag{5.47}$$

The reference active power weight (w_p) is calculated by adding average weight (w_{pavg}) and output of DC bus PI controller (w_{pdc}) as,

$$w_p = w_{pavg} + w_{pdc} \tag{5.48}$$

The active reference supply currents (i_{pa}^*, i_{pb}^* and i_{pc}^*) are calculated using w_p and unit inphase templates (u_{pa}, u_{pb} and u_{pc}) as,

$$i_{pa}^* = w_p u_{pa},\ i_{pb}^* = w_p u_{pb} \text{ and } i_{pc}^* = w_p u_{pc} \tag{5.49}$$

These active reference supply currents are used to estimate reference supply currents, which is discussed as follows.

5.3.2.2 Estimation of Fundamental Reactive Power Components of Reference Supply Currents From LMS Based Control Algorithm

Unit quadrature templates (u_{qa}, u_{qb} and u_{qc}) are calculated from unit inphase templates (u_{pa}, u_{pb} and u_{pc}) same way as given in section 5.3.1. The magnitude of PCC voltages are calculated as given in Eqn. (5.28) and compared to reference PCC voltage magnitude (V_t^*). Thus the generated error signal (v_{te}) is passed through PI controller which output (w_t) is same as given in section 5.3.1.

The weights (w_{qa}, w_{qb} and w_{qc}) corresponding to reactive power components of load currents are extracted from variants of LMS technique same as active power weights are calculated and their average weight is computed as,

$$w_{qavg} = \frac{w_{aq}+w_{bq}+w_{cq}}{3} \tag{5.50}$$

Reference reactive power weight (w_q) is calculated by subtracting average reactive power weight (w_{qavg}) from output of AC bus PI controller (w_t) as,

$$w_q = w_t - w_{qavg} \tag{5.51}$$

The reference reactive power components of supply currents (i_{qa}^*, i_{qb}^* and i_{qc}^*) are calculated from the reference reactive power weight w_q and unit quadrature templates (u_{qa}, u_{qb} and u_{qc}) as,

$$i_{qa}^{*} = w_q u_{qa},\ i_{qb}^{*} = w_q u_{qb} \text{ and } i_{qc}^{*} = w_q u_{qc} \quad (5.52)$$

These fundamental reactive components of reference supply currents are added with fundamental active component of reference supply currents to estimate reference supply currents.

5.3.2.3 Generation of Reference Supply Currents and Switching Pulses for Three Phase VSC

Reference supply currents (i_{sa}^{*}, $i_{sb}^{*}$and i_{sc}^{*}) for the three phases are determined by the addition of respective active and reactive supply currents calculated in Eqn. (5.49) and Eqn. (5.52) as,

$$i_{sa}^{*} = i_{pa}^{*} + i_{qa}^{*},\ i_{sb}^{*} = i_{pb}^{*} + i_{qb}^{*} \text{ and } i_{sc}^{*} = i_{pc}^{*} + i_{qc}^{*} \quad (5.53)$$

These reference supply currents (i_{sa}^{*}, $i_{sb}^{*}$and i_{sc}^{*}) are compared with sensed supply currents (i_{sa}, i_{sb} and i_{sc}) and current errors (i_{sae}, i_{sbe} and i_{sce}) are generated. These current errors are passed through PWM current controller for generation of switching pulses for the three phase VSC.

5.3.3 Variable Step Size Least Mean Square Based Control Algorithm for DSTATCOM [156-158]

This section presents development of variable step size least mean square (VSSLMS) based adaptive control algorithm for DSTATCOM. This control technique is based on least mean square method, which step size is adjusted using Lorentzian function. This adaptive technique is used to estimate the weights corresponding to the fundamental active and reactive power component of load current. The VSSLMS based algorithm is used for control of DSTATCOM for various power quality improvement features viz. power factor improvement, voltage regulation, harmonics compensation and balancing of loads.

5.3.2.1 Estimation of Fundamental Active Power Components of Reference Supply Currents From VSSLMS Based Control Algorithm

Fundamental active power components of reference supply current are estimated with VSSLMS.

The block diagram of the VSSLMS based control algorithm is shown in Fig. 5.5. The voltage amplitude at the PCC is calculated as,

$$V_t = \sqrt{2(v_{sa}^2 + v_{sb}^2 + v_{sc}^2)/3} \tag{5.54}$$

Inphase unit templates of PCC voltages (u_{pa}, u_{pb} and u_{pc}) are calculated from PCC voltages and PCC voltage magnitude (V_t) same as given in section 5.3.1. Voltage at DC bus (V_{dc}) is sensed and compared by reference DC bus voltage (V_{dc}^*), thus the generated error (v_{de}) is passed through PI controller. The output of DC bus voltage PI controller (w_{pdc}) is same as given in section 5.3.1.

The weights (w_{pa}, w_{pb} and w_{pc}) corresponding to active power components of load currents are calculated from VSSLMS based control algorithm. The non-sinusoidal load current can be expanded by Fourier series as,

$$i_l(n) = I_{lf}\sin(wn + \emptyset_f) + \sum_{h=5,7\ldots}^{\infty} I_{lh}\sin(h\omega n + \emptyset_h) \tag{5.55}$$

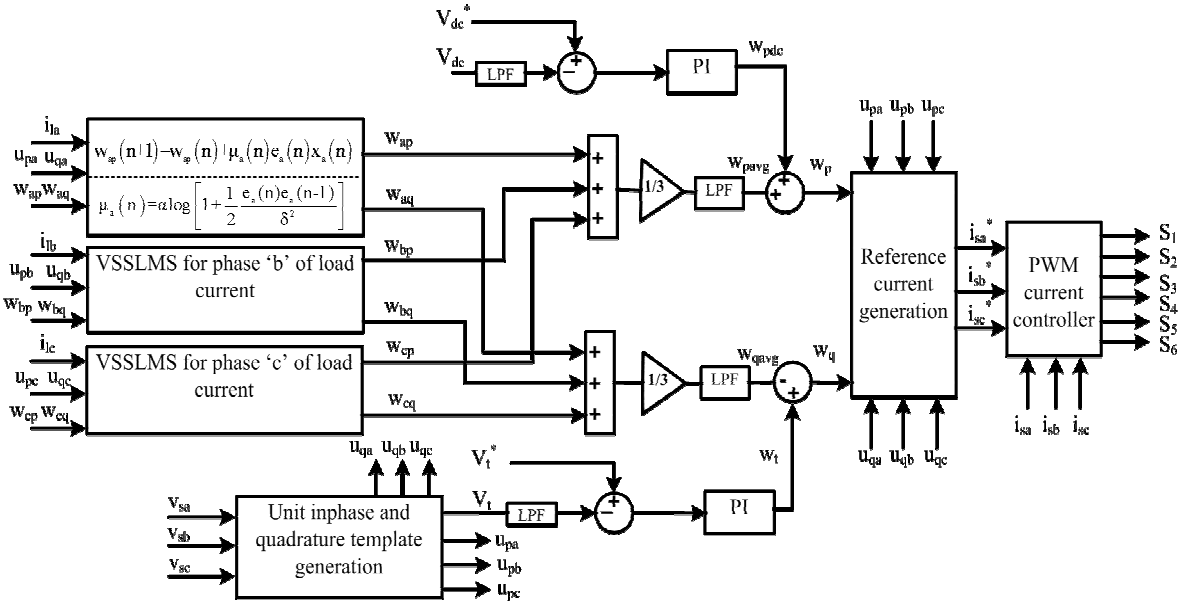


Fig. 5.5 Block diagram of VSSLMS based control algorithm for DSTATCOM

where I_{lf}, I_{lh}, $\emptyset_f$and $\emptyset_h$denote the peak value of fundamental load current, peak value of harmonic current, phase angle of fundamental component of load current and phase angle of the harmonic component of load current respectively. It is observed from Eqn. (5.55), that the load current can expressed as the sum of the fundamental component and harmonics. The fundamental and harmonic components can be further subdivided into two parts corresponding to real power components (i_{lfp} and i_{lhp}) and reactive power components (i_{lfq} and i_{lhq}), as shown in Eqn. (5.56) and Eqn. (5.57),

$$i_l(n) = I_{lf} \sin \omega n \cos \emptyset_f + I_{lf} \cos \omega n + \sum_{h=3,5,7\ldots}^{\infty} (I_{lh} \sin h\omega n \cos \emptyset_f + \cos h\omega n \sin \emptyset_f) \quad (5.56)$$

$$i_l(n) = i_{lfp} + i_{lfq} + i_{lhp} + i_{lhq} \quad (5.57)$$

After simplifying these equations, one also can write fundamental and harmonics components of load current separately as,

$$i_{lf}(n) = w_{ap} \sin \omega n + w_{aq} \cos \omega n \quad (5.58)$$

$$i_{Lh}(n) = w_{aph} \sin h\omega n + w_{aqh} \cos h\omega n \quad (5.59)$$

where $h = 5,7 \ldots . \infty$ corresponds to the order of harmonics w_{ap} and w_{aq} are weighted values of the sine and cosine terms of the load current corresponding to the fundamental component, and $w_{aph}$and w_{aqh} are the weighted values of the sine and cosine terms of the load current corresponding to the harmonics.

The load current can now be estimated as,

$$i_{est}(n) = w^T x(n) \quad (5.60)$$

where the sine and cosine vector is $x(n) = [\sin \omega n \cos \omega n \ \sin 5\omega n \cos 5\omega n \ ...]^T$ and the corresponding weight vector is given as $w^T = [w_{ap}\, w_{aq} w_{ap5} w_{aq5} \ ...]$.

Let $i_l(n)$ be the actual value of load current, $x(n)$ be the input vector and w^T is the weight vector, then the error {e(n)} in predicting the load current can be calculated as,

$$e(n) = \ i_l(n) - w^T x(n) \tag{5.61}$$

The objective here is to minimize mean square error $E[e(n)^2]$. This can be achieved by LMS method. In this method, the weights are iteratively determined to achieve minimum error, by using the updation rule as,

$$w(n+1) = w(n) + 2\mu e(n) x(n) \tag{5.62}$$

This rule in Eqn. (5.62) forms the basis of adaptive LMS method and involves the evaluation of $x(n)$ and $w(n)$ at each iteration. The symbol μ denotes the step size which controls the stability and convergence rate of the LMS method. The convergence of this adaptive method is ensured by determining the value of step size. The step size must lie between $0<\mu<x_{max}$, where x_{max} is the largest Eigen value of the autocorrelation matrix of the input signal.

In the case of fixed step LMS algorithm, the value of μ is optimized and is maintained at constant value throughout the iterative process. The optimized value of μ minimizes the steady state error at zero value or accelerates the rate of convergence. If μ is higher, this leads to faster convergence rate but steady state error increases. On the contrary, smaller value of μ reduces the steady state error and it decreases the rate of convergence.

To improve the overall performance, these factors i.e. convergence rate, tracking capability and steady state error, the value of μ must be selected appropriately. To achieve this, a variable step

size LMS (VSSLMS) adaptive algorithm is proposed here. This algorithm uses Lorentzian function, and the improved step size factor $\mu(n)$ can be expressed as,

$$\mu(n) = \alpha \log\left[1 + \frac{1}{2}\frac{e(n)e(n-1)}{\delta^2}\right] \tag{5.63}$$

The step size μ(n) is a function of α, δ and the correlation value of the error calculated at each sample time. Parameter α controls the convergence rate and δ controls the changes in step size in the steady state condition when the steady state error is close to zero. Both of these parameters together vary step size $\mu(n)$ as shown in Eqn. (5.63). In the beginning of simulation, the error $e(n)$ is larger, and due to this, $\mu(n)$ is also larger, which speeds up the convergence rate. Due to fast convergence, the error is reduced gradually and $\mu(n)$ also decreases. In this way, using Lorentzian function, the proposed control algorithm achieves faster convergence and lower steady state error. This algorithm also exhibits improved stability under distorted load conditions and even under unbalanced load condition.

The general equation for updating the weight vector using LMS technique is given in Eqn. (5.62) where μ could be taken as constant or variable. Moreover, using VSSLMS, the step-size $\mu(n)$ value is updated using Lorentzian function as depicted in Eqn. (5.63).

The weights (w_{pa}, w_{pb} and w_{pc}) corresponding to active power component of load currents are calculated from the above discussed VSSLMS based control algorithm and their average weight is given as,

$$w_{pavg} = (w_{ap} + w_{bp} + w_{cp})/3 \tag{5.64}$$

The total weight w_p corresponding to fundamental active power components of reference supply

current is obtained by the addition of the average weight (w_{pavg}) and active power component for regulating DC bus voltage w_{ploss} given as,

$$w_p = w_{pavg} + w_{ploss} \tag{5.65}$$

The active power components of reference supply current (i_{pa}^*, i_{pb}^* and i_{pc}^*) are expressed as,

$$i_{pa}^* = w_p u_{pa},\ i_{pb}^* = w_p u_{pb} \text{ and } i_{pc}^* = w_p u_{pc} \tag{5.66}$$

These fundamental active power components of currents are used to estimate reference supply currents given as follows.

5.3.1.1 Estimation of Fundamental Reactive Power Components of Reference Supply Currents Using VSSLMS Based Control Algorithm

Unit quadrature templates (u_{qa}, u_{qb} and u_{qc}) are calculated from unit inphase templates (u_{pa}, u_{pb} and u_{pc}) same manner as given in section 5.3.1. The magnitude of PCC voltages are calculated as given in Eqn. (5.54) and compared to reference PCC voltage magnitude (V_t^*). Thus the generated error signal (v_{te}) is passed through PI controller which output (w_t) is same as given in section 5.3.1.

The weights (w_{qa}, w_{qb} and w_{qc}) corresponding to reactive power component of load current are calculated similarly as active power weights are calculated by VSSLMS based control technique discussed above and their average weight (w_{qavg}) is given as,

$$w_{qavg} = (w_{aq} + w_{bq} + w_{cq})/3 \tag{5.67}$$

The output of the PI controller (w_t) denotes a leading reactive power component to compensate for the voltage drop due to loading and supply impedance of the system. The total fundamental reactive power component of reference supply current (w_q) is given as,

$$w_q = w_t - w_{qavg} \tag{5.68}$$

The reactive power components of reference currents (i_{qa}^*, i_{qb}^* and i_{qc}^*) are expressed as,

$$i_{qa}^* = w_q u_{qa}, i_{qb}^* = w_q u_{qb} \text{ and } i_{qc}^* = w_q u_{qc} \tag{5.69}$$

These fundamental reactive components of reference supply currents are added with fundamental active components of reference supply currents to estimate reference supply currents given as follows.

5.3.3.3 Generation of Reference Supply Currents and Switching Pulses

The summation of reference active and reactive power components of Eqn. (5.66) and Eqn. (5.69) can be considered as total reference currents (i_{sa}^*, i_{sb}^* andi_{sc}^*). These reference currents are compared with the sensed supply currents (i_{sa}, i_{sb} and i_{sc}) and the current error is extracted. This error is then passed through PWM current controller for generation of switching pulses for the three phase VSC.

5.4 MATLAB MODELING OF ADAPTIVE THEORY BASED CONTROL ALGORITHMS

This section presents MATLAB based modeling of adaptive theory based control algorithms for control of the DSTATCOM. The adaptive techniques such as Wiener filter, normalized LMS and VSSLMS based control algorithms are developed using MATLAB/SIMULINK for generation of reference supply currents. The detail description of MATLAB based model of the control algorithms are given as follows.

5.4.1 MATLAB Model of Wiener Filter Based Control Algorithm

The simulation model of algorithm is developed in MATLAB environment using SIMULINK.

The simulation model of Wiener filter based control algorithm is used to estimate the reference supply currents as shown in Fig. 5.6(a). The PCC voltages (v_{sa}, v_{sb} and v_{sc}), supply currents (i_{sa}, i_{sb} and i_{sc}), load currents (i_{la}, i_{lb} and i_{lc}) and DC bus voltage (V_{dc}) are sensed and used by control algorithm for estimation of reference supply currents. Simulation model for estimation of weights corresponding to active and reactive power component using Wiener filter is shown in Fig. 5.6(b).

5.4.2 MATLAB Model of NLMS Based Control Algorithm

The simulation model of NLMS based control algorithm is shown in Figs. 5.7(a) and (b), which is used to generate the reference supply currents for control of DSTATCOM. Simulation study of the system is done in MATLAB environment using SIMULINK and Sim Power System (SPS) tool boxes. The PCC voltages (v_{sa}, v_{sb} and v_{sc}), supply currents (i_{sa}, i_{sb} and i_{sc}), load currents (i_{la}, i_{lb} and i_{lc}) and DC bus voltage (V_{dc}) are sensed and fed to the Simulink model of the NLMS

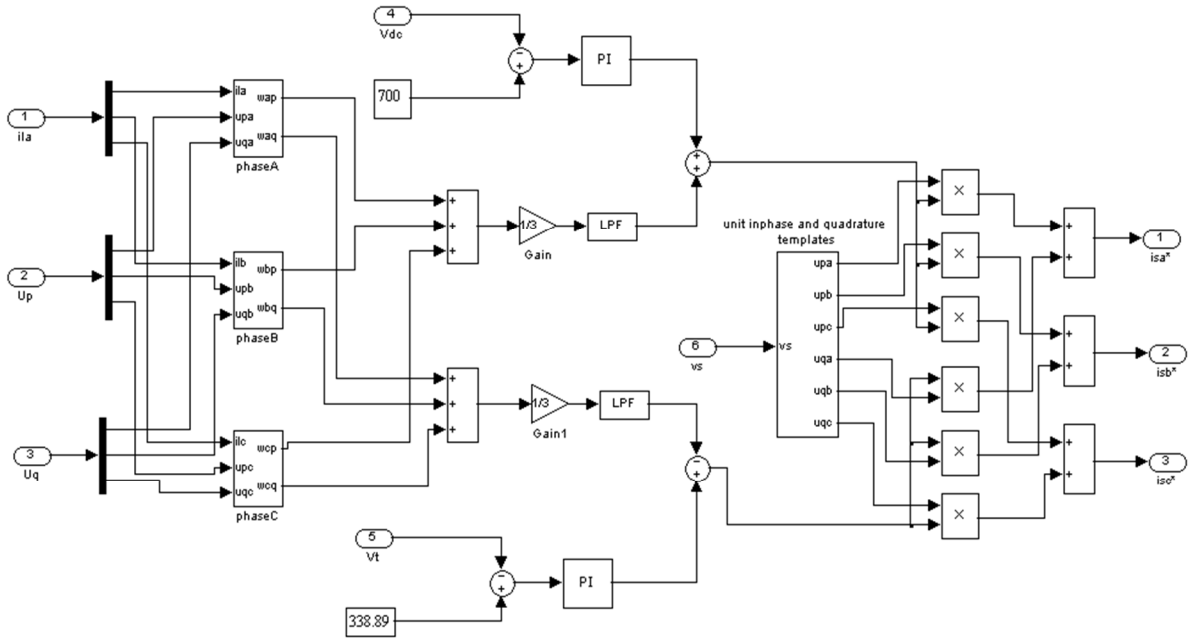


Fig. 5.6(a) Simulation model of Wiener filter based control algorithm for extraction of reference supply currents

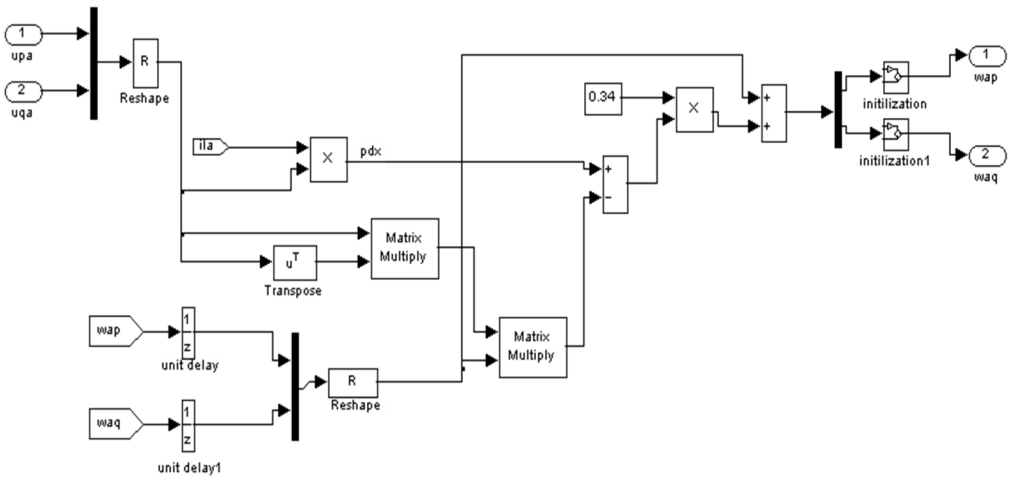


Fig. 5.6(b) Simulation model for estimation of active and reactive power component of phase 'a' of load current

based control algorithm. The NLMS technique is used to estimate weights corresponding to fundamental active and reactive power component of load currents.

5.4.3 MATLAB Model of VSSLMS Based Control Algorithm

Figs. 5.8(a) and (b) show the simulation model of VSSLMS based control algorithm, which is

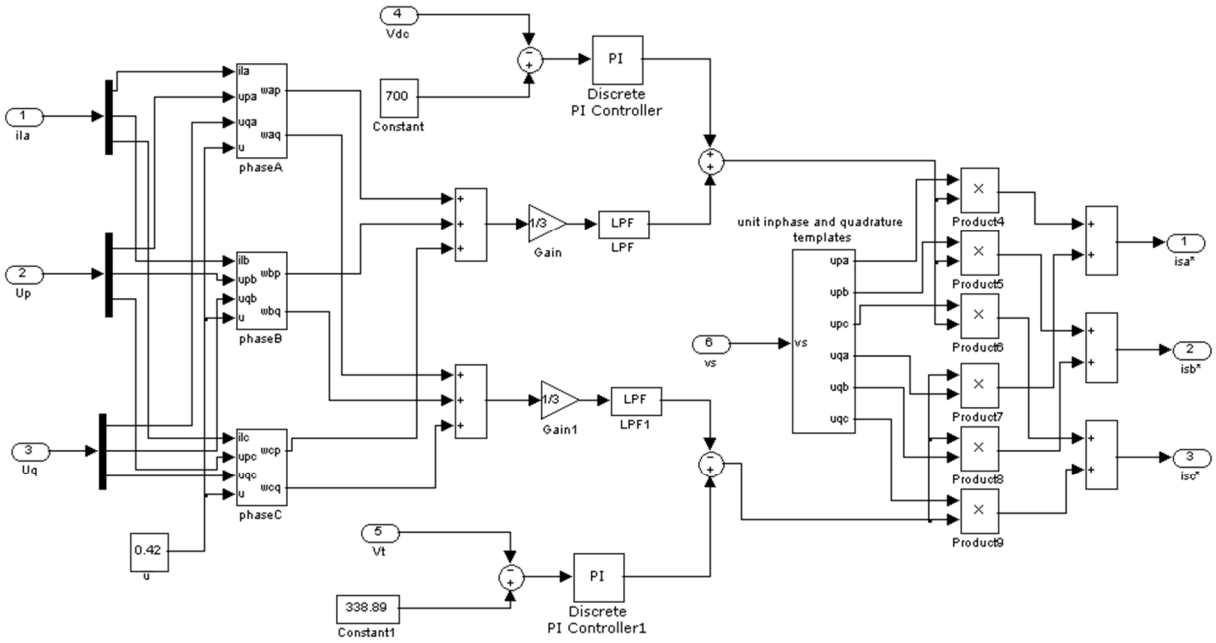


Fig. 5.7(a) Simulink model of NLMS technique based control algorithm

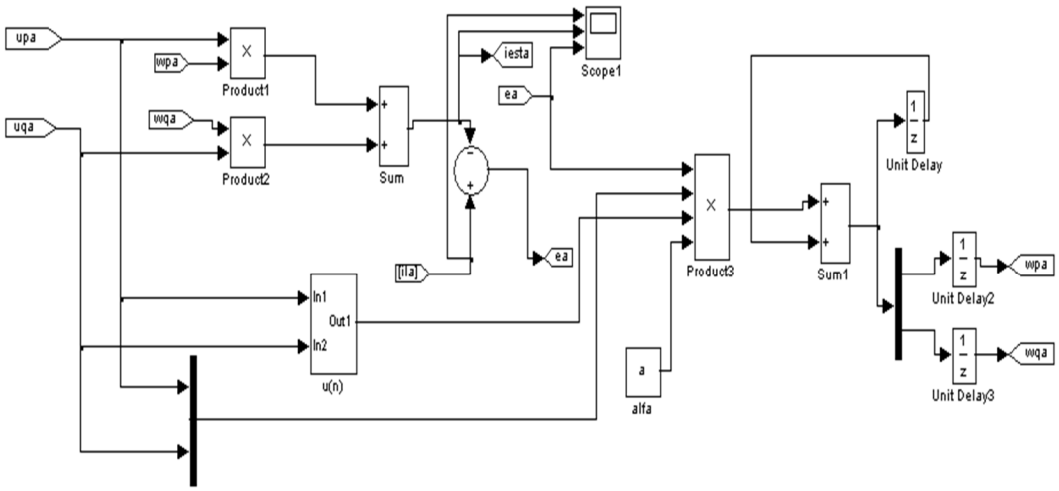


Fig. 5.7(b) Simulink model for estimation of weights from NLMS technique

used to generate the reference supply currents for the control of DSTATCOM. Simulation study of the system is performed in MATLAB environment using SIMULINK and Sim Power System (SPS) tool boxes. The PCC voltages (v_{sa}, v_{sb} and v_{sc}), supply currents (i_{sa}, i_{sb} and i_{sc}), load currents (i_{la}, i_{lb} and i_{lc}) and DC bus voltage (V_{dc}) are sensed and fed to the Simulink model of the VSSLMS based control algorithm. The VSSLMS technique is used to estimate the weights corresponding to the fundamental active and reactive power component of load currents.

5.5 DSP IMPLEMENTATION OF ADAPTIVE THEORY BASED CONTROL ALGORITHMS

This section deals with DSP (dSPACE 1104 R&D controller board) based implementation of adaptive theory based control algorithms. The real time performance of adaptive theory based control algorithms is tested on developed prototype in the laboratory.

5.5.1 DSP Implementation of Wiener Filter Based Control Algorithm

The Wiener filter based control algorithm is implemented in DSP (dSPACE-1104 R&D controller board) used to generate gating pulses for the IGBTs of three phase VSC. The DSP (dSPACE 1104) is real time controller based on a 603 PowerPC floating-point processor. This includes slave DSP subsystem based on the TMS320F240 digital signal processor. The DSP

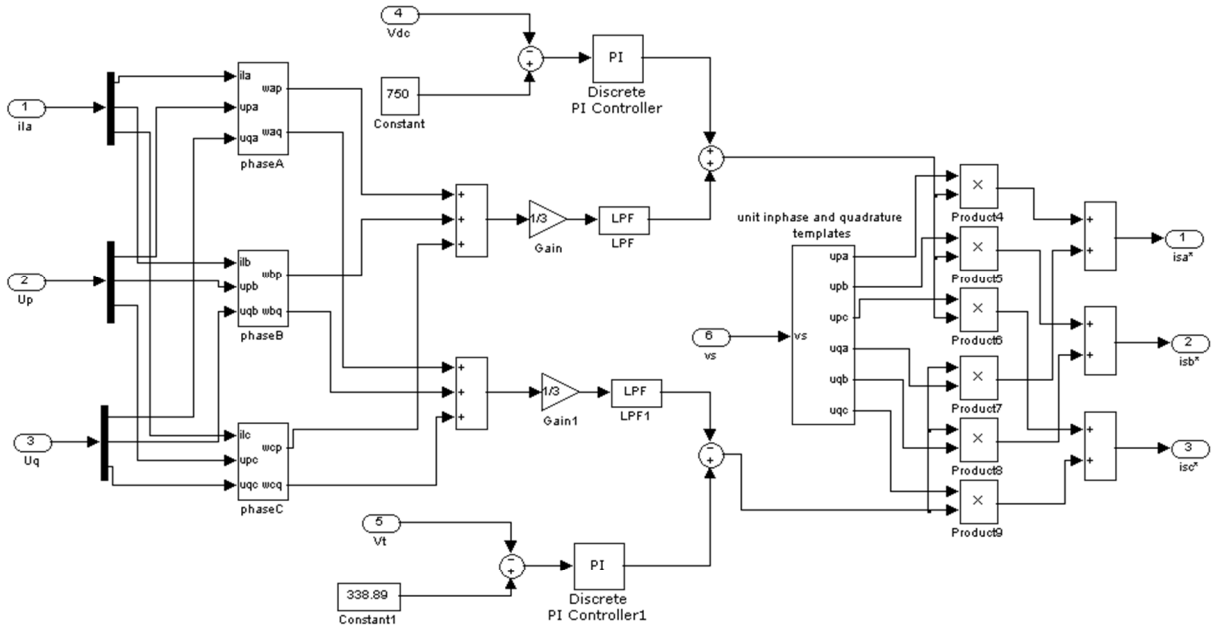


Fig. 5.8(a) Simulink model of VSSLMS technique based control algorithm

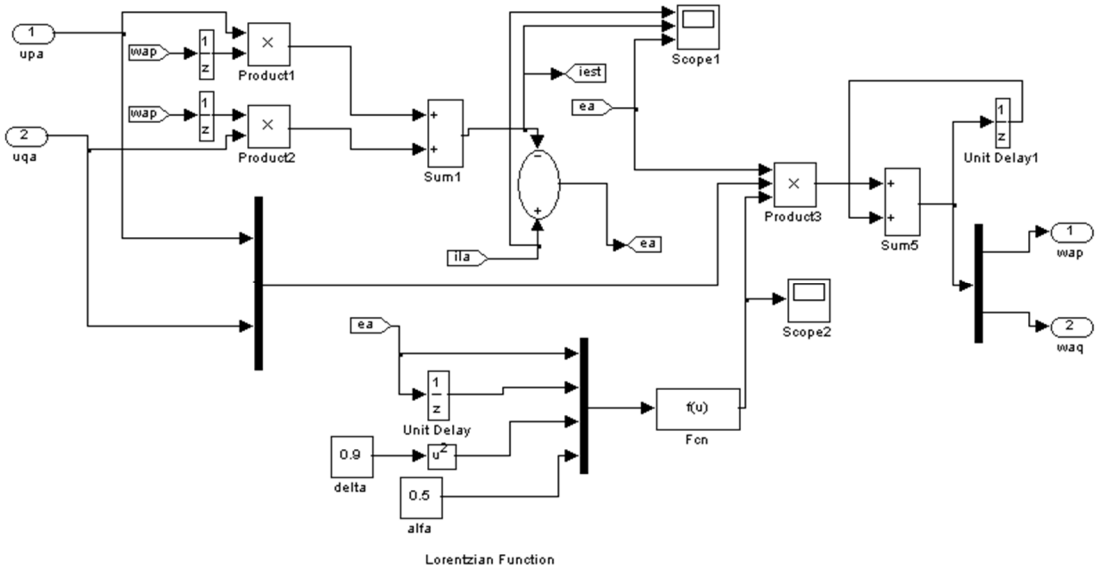


Fig. 5.8(b) Simulink model for estimation of weights from VSSLMS technique

hardware and software give the facility to generate real time switching pulses from real time signals with the use of SIMULINK model of the control algorithm. The simulation model of Wiener filter based control algorithm used for DSP implementation is given in Fig. 5.6. DSP (dSPACE 1104) based implementation of control algorithm for generating switching pulses of

VSC is same as given in section 4.7.1. The DSP based implementation is mainly divided into four blocks ADC block, scaling of signals block along with control algorithm block and PWM current controller block. Implementation of DC and AC bus PI controllers is same as given in 4.7.1. An implementation of pulse width modulation (PWM) switching in DSP-dSPACE using DS 1104SL_DSP_PWM3 block is presented same as in section 4.7.1. The solver option used for the implementation is based on the fixed-step type with discrete (no continuous states) solver. The sampling time (T_s) is selected as 45μs for Wiener filter based control algorithm. The DC bus PI controller proportional and integral gains calculated using Ziegler-Nichols unit step response algorithm. The tuned values of PI controller gains are selected very close to calculated values.

5.5.2 DSP Based Implementation of NLMS Based Control Algorithm

The NLMS based control algorithm is implemented using DSP (dSPACE 1104 R&D controller board). This controller is used to generate six switching pulses for IGBTs of a three phase VSC of DSTATCOM. The DSP based implementation needs real time signals of PCC voltages, supply currents, load currents and DC bus voltage through appropriate sensors and sensors circuitry. These real time signals are processed by DSP using SIMULINK based control algorithm and six real time switching signals are generated for switching on and off of the six IGBTs of the VSC.

The model of NLMS based control algorithm used for real time implementation is same as discussed in simulation study. DSP (dSPACE 1104) based implementation of control algorithm for generating switching pulses of DSTATCOM is same as presented in section 4.7.1. The DSP based implementation is mainly divided into four blocks ADC block, scaling of signals block along with control algorithm block and PWM current controller block. Implementation of DC bus PI controller and PWM current controller for switching pulse generation are also same as given in section 4.7.1. The NLMS based control algorithm for control of DSTATCOM takes a

sampling time of approximately 50μs. The proportional and integral gains of PI controllers are calculated using standard Ziegler-Nichols unit step response algorithm and the values required in implementation are selected very close to the calculated values.

5.5.3 DSP Based Implementation of VSSLMS Based Control Algorithm

The implementation of MATLAB model of VSSLMS based control algorithm is performed using DSP (dSPACE1104 R&D controller board). The DSP controller requires real time signals viz. PCC voltages, supply currents and load currents, which are sensed from appropriate sensors and buffer circuitry. The sensed signals are then processed by the MATLAB based control algorithm implemented on DSP (dSPACE1104 controller board). After processing, this controller is used to generate switching pulses for the three phase VSC working as DSTATCOM. The model of VSSLMS based control algorithm used for DSP implementation is the same as discussed in simulation study and is shown in Fig. 5.8. The DSP based implementation of VSSLMS based control algorithms is same as given in 4.7.1.

An implementation of DC bus voltage PI controller and PWM current controller for switching pulse generation is the same as discussed in section 4.7.1. The sampling time (T_s) taken by VSSLMS based control algorithm for control of DSTATCOM is around 60μs. The proportional and integral gains of PI controllers are calculated using the standard Ziegler-Nichols unit step response algorithm and the values required in implementation are selected very near to the calculated values.

5.6 RESULTS AND DISCUSSION

The adaptive theory based control algorithms discussed in previous sections are developed using MATLAB environment using SIMULINK and Sim Power System (SPS) tool boxes. This section discusses the performance of these control algorithms using simulation and experimental

test results. The test results are recorded using a power quality analyzer (Fluke 43B) and four channel digital oscilloscope (Agilent DSO-X 2014A) on the developed prototype of DSTATCOM.

5.6.1 Performance of DSTATCOM With Wiener Filter Based Control Algorithm

The performance of DSTATCOM for harmonics elimination, reactive power compensation and load balancing is achieved in PFC and voltage regulation modes under nonlinear load. The simulation and experimental test results for Wiener filter based control algorithms are discussed as follows.

5.6.1.1 Simulated Performance of DSTATCOM in PFC and Voltage Regulation Modes

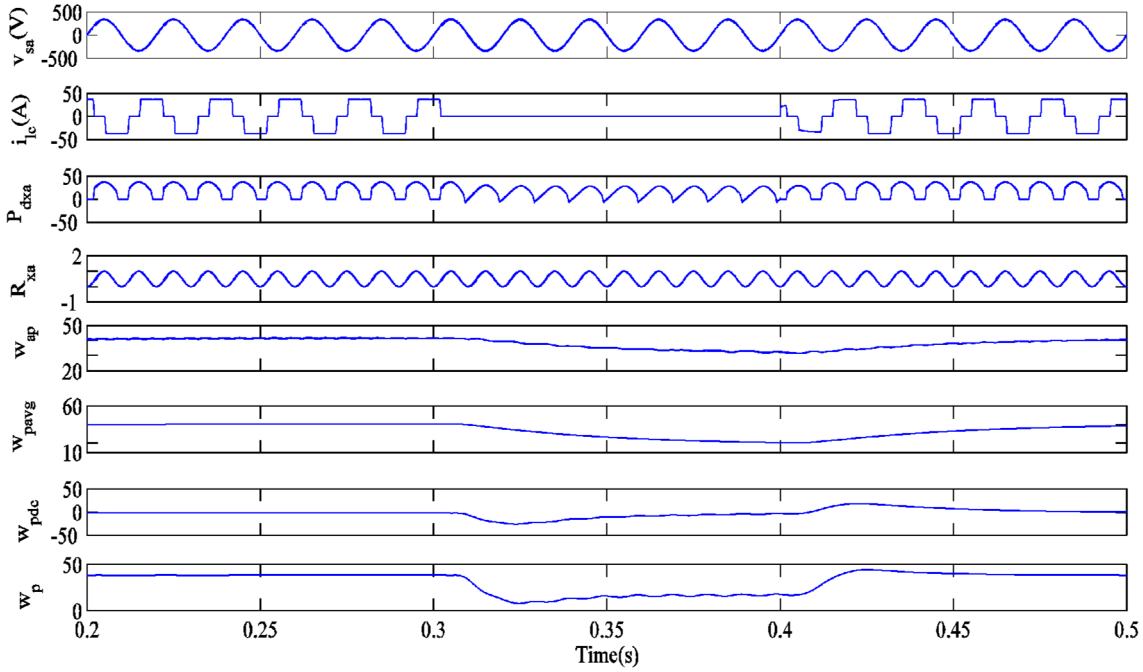
This section presents the simulated performance of DSATCOM using Wiener filter based control algorithm. The performance of DSTATCOM controlled in PFC mode and voltage regulation mode is discussed.

A. Performance of Wiener Filter Based Control Algorithm in Voltage Regulation Mode Under Nonlinear Load

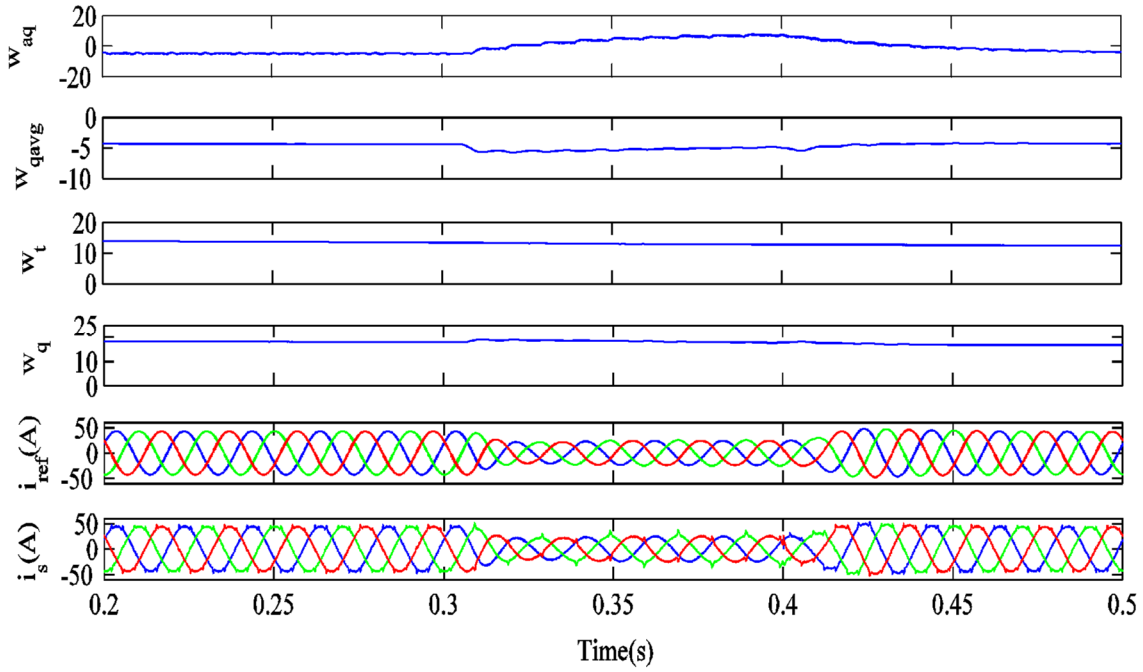
Fig. 5.9 shows the performance and intermediate signals of Wiener filter based control algorithm in voltage regulation mode under nonlinear load. Fig. 5.9(a) shows waveforms of P_{dxa} which is the cross correlation vector between the desired quantity and input quantity, R_x is the correlation matrix of the input data, weight corresponding to active power component of phase 'a' of load current (w_{ap}), average and filtered active power weight (w_{pavg}), output of DC bus PI controller (w_{pdc}) and reference active power weight (w_{pt}) along with phase 'a' of PCC voltage (v_{sa}) and phase 'c' of load current (i_{lc}).

These results are shown for steady state condition (before t=0.3s) as well as unbalanced load condition. Unbalancing in the load is created during t=0.3s to t=0.4s, when phase 'c' of load is

switched off. Fig. 5.9(b) shows the waveforms of weight corresponding to reactive power component of phase 'a' of load current (w_{aq}), average and the filtered reactive power weight (w_{qavg}), output of AC bus PI controller (w_t), reference reactive power weight (w_q) which include



(a)



(b)

Fig. 5.9 Performance of Wiener filter based control algorithm under nonlinear load in voltage regulation mode

w_{qavg} and w_t, reference supply currents (i_s^*) and supply currents (i_s). It is observed from these results that the supply currents are tracking the reference currents and the proposed control algorithm performs satisfactory in steady state as well as in dynamic and unbalanced load conditions.

B. Performance of DSTATCOM in Power Factor Correction Mode Under Nonlinear Load

Fig. 5.10 shows the performance of the shunt compensator under nonlinear load for PFC mode. The waveforms shown are PCC voltages (v_s), supply currents (i_s), load currents (i_{la}, i_{lb} and i_{lc}),

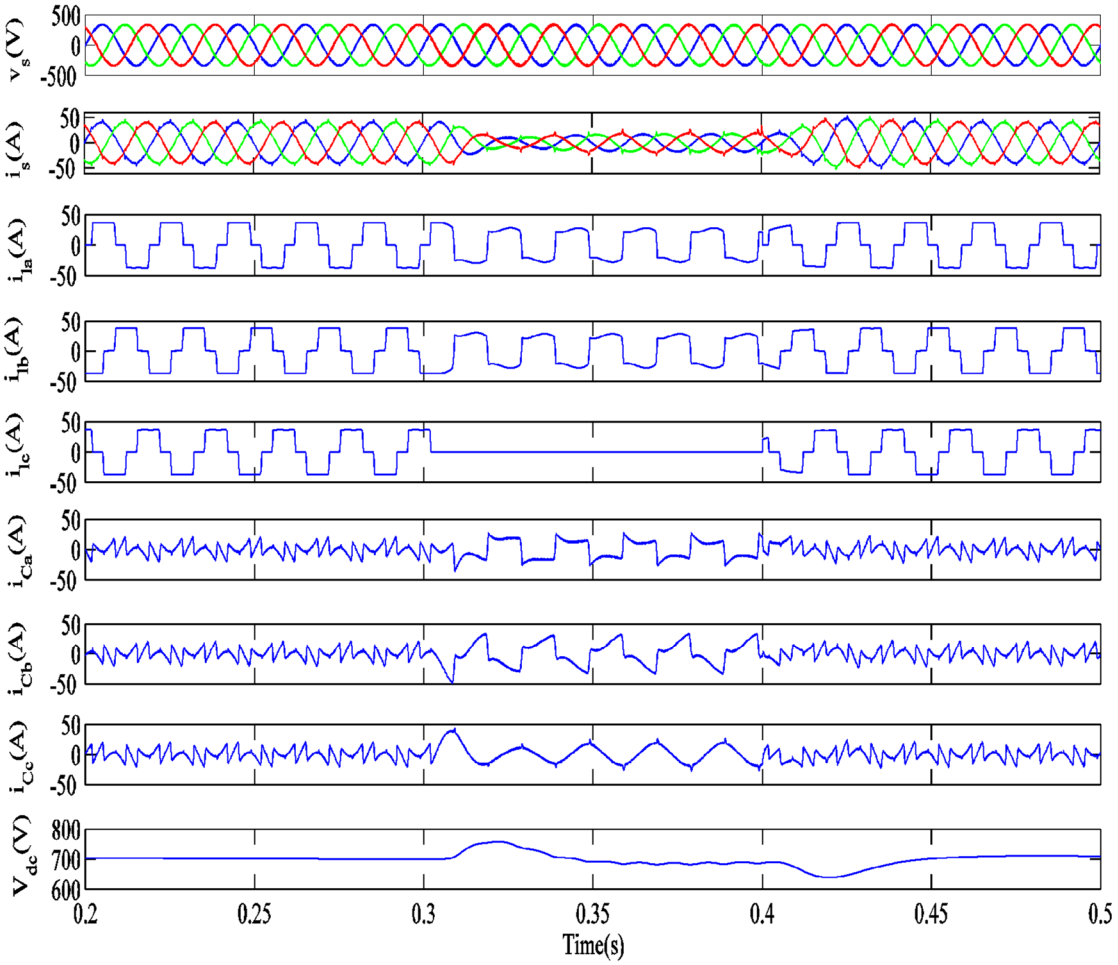
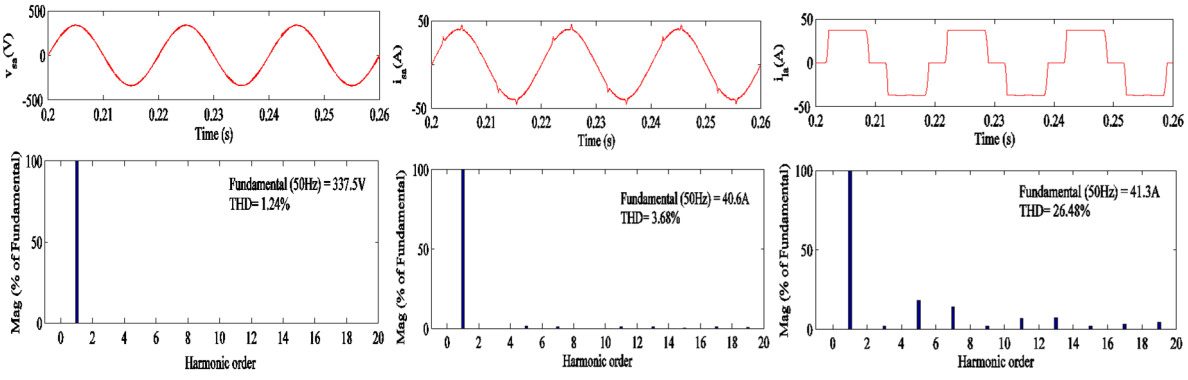


Fig. 5.10 Steady state and dynamic performance of DSTATCOM in PFC mode under nonlinear load

compensator currents (i_{Ca}, i_{Cb} and i_{Cc}) and self-sustained DC bus voltage (V_{dc}). It can be observed from Fig. 5.10 that before t=0.3s, the system is under steady state condition and the DC bus voltage is regulated to its reference value of 700V. One phase (phase '*c*') of load is now switched off at t=0.3s till t=0.4s. During this period, it is observed that supply currents are sinusoidal and balanced although having reduced magnitude. The voltage at the DC bus of the VSC also achieves its reference value of 700V within a couple of cycles. The DSTATCOM performs satisfactorily under steady state and unbalanced load conditions. The supply voltages and currents are observed to be in phase, thus indicating power factor improvement of supply currents to unity.

Fig. 5.11 shows the waveforms and harmonic spectra of phase '*a*' of PCC voltage (v_{sa}), supply current (i_{sa}) after compensation and load current (i_{la}). The values of THDs of the phase 'a' of PCC voltage, supply current and load current are observed 1.24%, 3.68% and 26.48% respectively. It can be observed from these results that the harmonic distortions of PCC voltage and supply current are within the 5% limit specified by IEEE-519 standard.

C. Performance of DSTATCOM in Voltage Regulation Mode Under Nonlinear Load



(a) (b) (c)

Fig. 5.11 Harmonic spectra of (a) PCC voltage, v_{sa} (b) supply current, i_{sa} (c) load current, i_{la} in PFC mode

Steady state and dynamic performances of the DSTATCOM for voltage regulation under nonlinear load are observed using Wiener filter based control algorithm in Fig. 5.12. This figure shows the waveforms of PCC voltages (v_s), supply currents (i_s), load currents (i_{la}, i_{lb} and i_{lc}), compensator currents (i_{Ca}, i_{Cb} and i_{Cc}), self-sustained DC bus voltage (V_{dc}) and regulated magnitude of PCC voltage (V_t). It also shows the response of the system from t=0.2s to t=0.3s, under steady state condition. During this condition, the DC bus voltage and magnitude of PCC voltage are maintained at their reference values of 700V and 338.8V respectively. During the interval t=0.3s to t=0.4s, one phase (phase '*c*') of load is switched off. It is observed that even

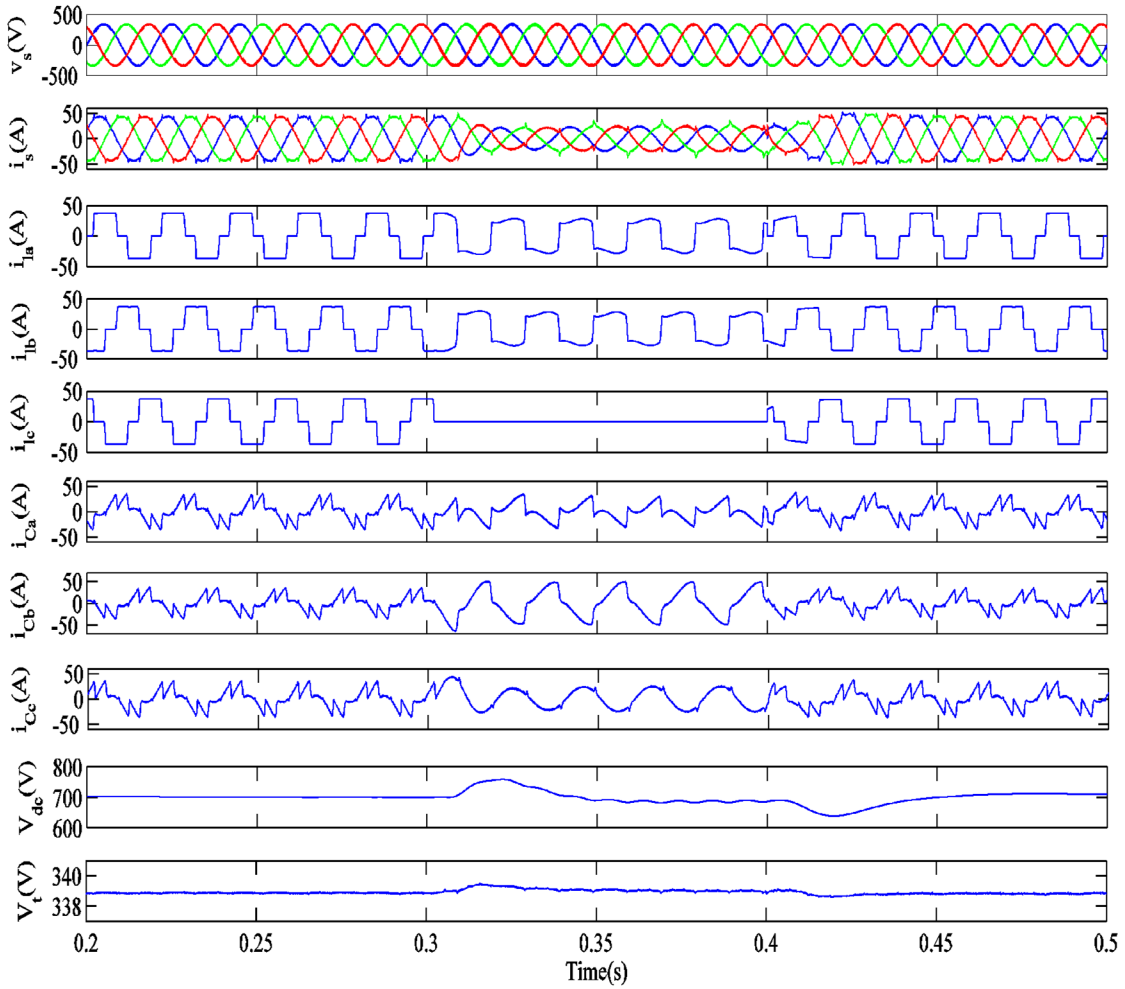


Fig. 5.12 Steady state and dynamic performance of DSTATCOM in voltage regulation under nonlinear load

under unbalanced load condition, the supply currents are sinusoidal and balanced. During this period, the DC bus voltage and magnitude of PCC voltages are regulated to their reference values within couple of cycles due to action of the PI controllers.

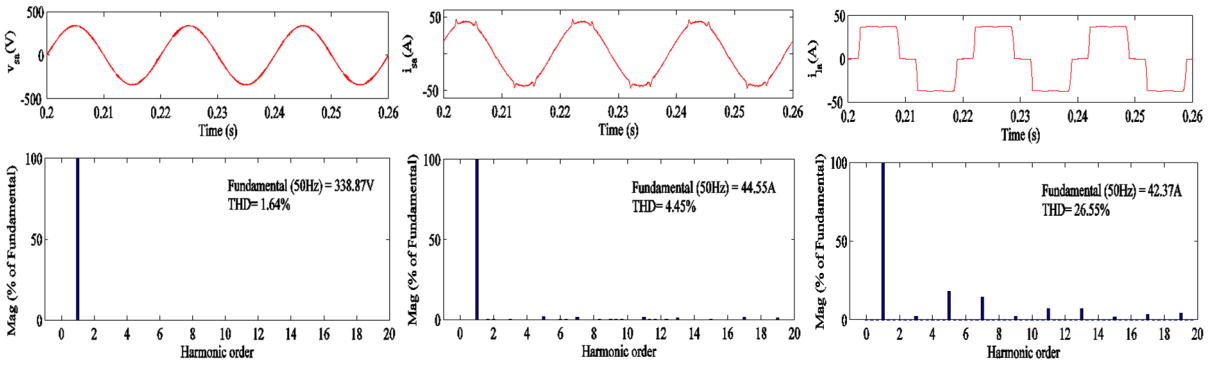
Fig. 5.13 depicts the waveforms and harmonic spectra of phase '*a*' of PCC voltage (v_{sa}), supply current (i_{sa}) after compensation and load current (i_{la}). The values of THDs of the phase '*a*' of PCC voltage, supply current and load current are observed to be 1.64%, 4.45% and 26.55% respectively. It can be observed from these results that the harmonic distortions of PCC voltage and supply current meet the limit specified in IEEE-519 standard.

5.6.1.2 Experimental Performance of DSTATCOM in PFC and Voltage Regulation Modes

This section discusses the experimental performance of Wiener filter based control algorithm under nonlinear and linear loads in PFC and voltage regulation modes. The test results for DSTATCOM with Wiener filter based control algorithm are given as follows.

A. Response of Wiener Filter Based Control Algorithm

The intermediate signals representing performance of Wiener filter based control algorithm for



(a) (b) (c)

Fig. 5.13 Harmonic spectra of (a) PCC voltage, v_{sa} (b) supply current, i_{sa} (c) load current, i_{la} in voltage regulation mode.

DSTATCOM in voltage regulation mode are shown in Figs. 5.14(a)-(d). The waveforms of phase 'a' of PCC voltage (v_{sa}), filtered PCC voltage (v_{saf}), phase 'a' of load current (i_{la}) and active power weight (w_{ap}) corresponding to phase 'a' of load current are shown in Fig. 5.14(a). Fig. 5.14(b) shows waveforms of active power weight (w_{ap}), average magnitude of active power weights (w_{pavg}), output of DC bus PI controller (w_{pdc}) and reference active power weight (w_p). Fig. 5.14(c) shows waveforms of reactive power weight (w_{aq}), average magnitude of reactive power weights (w_{qavg}), output of AC bus PI controller (w_t) and reference reactive power weight (w_q). The waveforms of reference supply currents (i_{sa}^*, i_{sb}^* and i_{sc}^*) along with phase '*a*' of PCC voltage are shown in Fig. 5.14(d). It can be observed from these intermediate signals that the

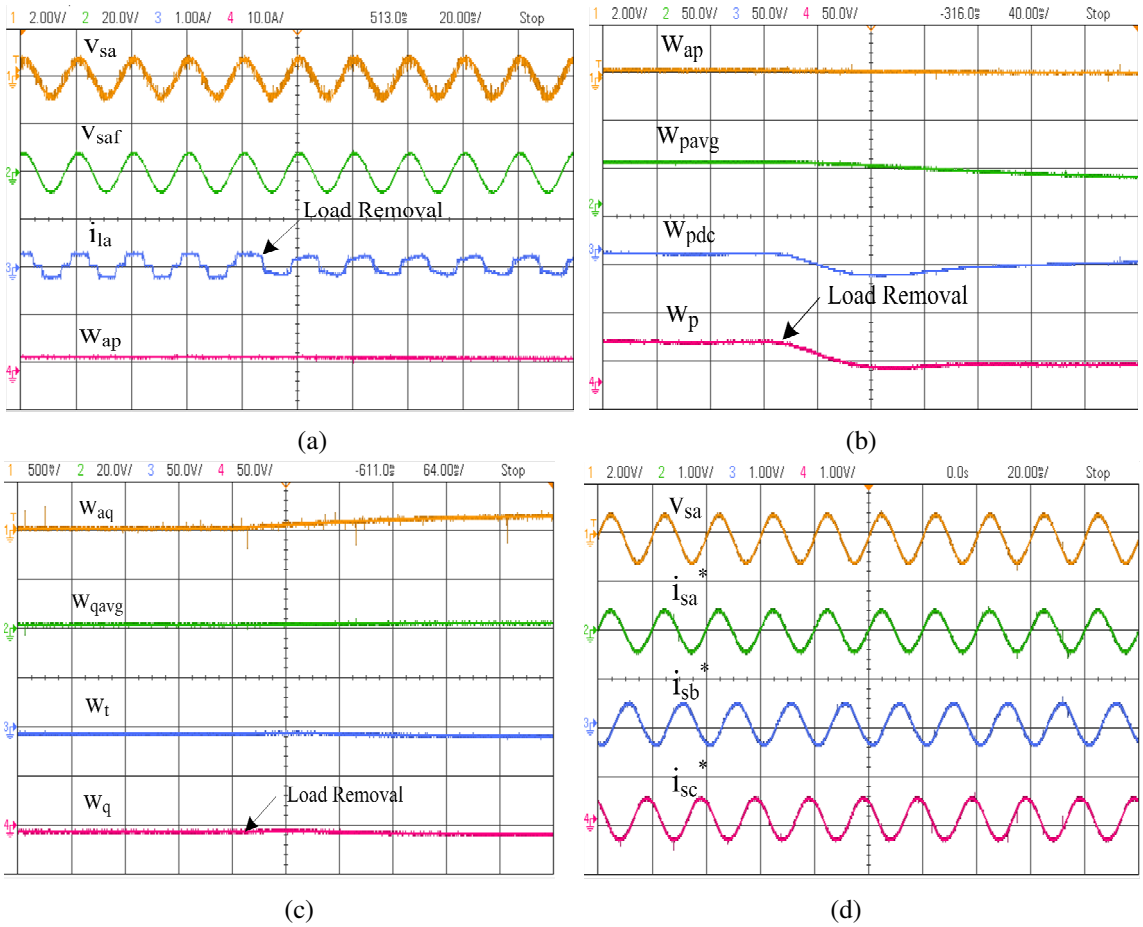


Fig. 5.14 Intermediate signals (a) v_{sa}, v_{saf}, i_{la} and w_{ap} (b) w_{ap}, w_{pavg}, w_{pdc} and w_p (c) w_{aq}, w_{qavg}, w_t and w_q (d) reference supply currents along with v_{sa}

Wiener filter based control algorithm is able to extract the fundamental weight components very quickly under dynamic load conditions. These extracted weights are used to generate the reference supply currents and the compensator performs well under wide variation of loading conditions including load unbalancing.

B. Steady State Performance of DSTATCOM in PFC Mode Under Nonlinear and Linear Loads

The steady state performance of DSTATCOM using Wiener filter based control algorithm under nonlinear load is presented in Fig. 5.15. The waveforms of supply current (i_{sa}), load current (i_{la}) and compensator current (i_{Ca}) along with PCC voltage (v_{sa}) are presented in Figs. 5.15(a), (c) and (e). Harmonic spectra corresponding to phase '*a*' of supply current (i_{sa}), load current (i_{la}) and PCC voltage are shown in Figs. 5.15(b), (d) and (f). The values of THD in supply current, load current and PCC voltage are observed to be 3.9%, 20.3% and 2.6% respectively. It can be observed from this figure that after compensation, THD in supply current has reduced to 3.9%, while the load current has THD of 20.3%. The DSTATCOM performs satisfactorily and maintains THD in PCC voltage and supply current within the limit prescribed by IEEE-519 standard. Fig. 5.16 shows the simulated performance of the DSTATCOM using Wiener filter based control algorithm at same voltage rating for which experimental system is developed. This shows the waveforms of PCC voltages (v_s), supply currents (i_s), load currents (i_{la}, i_{lb} and i_{lc}), compensator current (i_{Ca}, i_{Cb} and i_{Cc}) and self-sustained DC bus voltage (V_{dc}). The supply currents are balanced and sinusoidal and DC bus voltage is regulated at the reference voltage of 200V during steady state (before t=0.3s) and unbalanced load condition (t=0.3s to t=0.4s).

Fig. 5.17 shows steady state performance of the DSTATCOM under linear lagging PF load in PFC mode. Figs. 5.17(a)-(c) show waveforms of phase 'a' of supply current (i_{sa}), load current (i_{la}) and compensator current (i_{Ca}) along with PCC voltage (v_{sa}). Figs. 5.17 (d)-(f) show

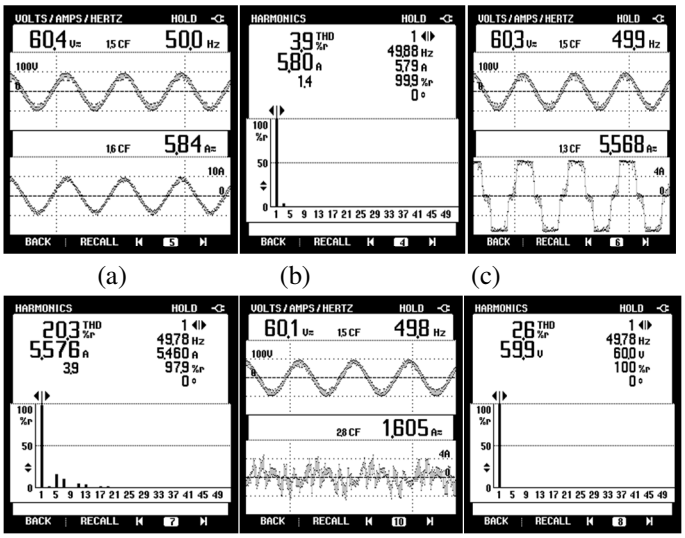


Fig. 5.15 Steady state performance of DSTATCOM under nonlinear load (a) v_{sa} and i_{sa} (b) harmonic spectrum of i_{sa} (c) v_{sa} and i_{la} (d) harmonic spectrum of i_{la} (e) v_{sa} and i_{Ca} (f) harmonic spectrum v_{sa} in PFC mode

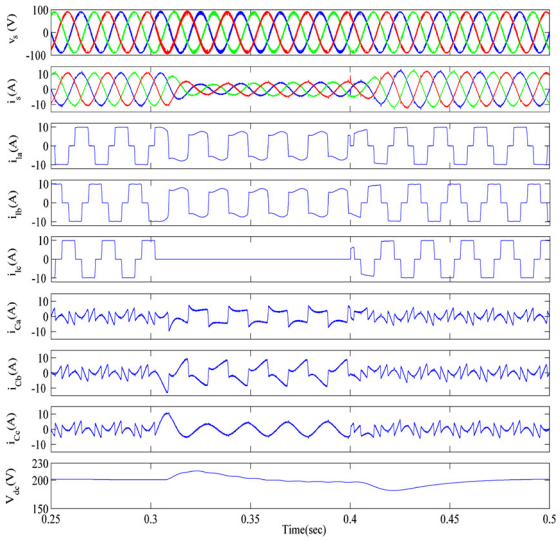
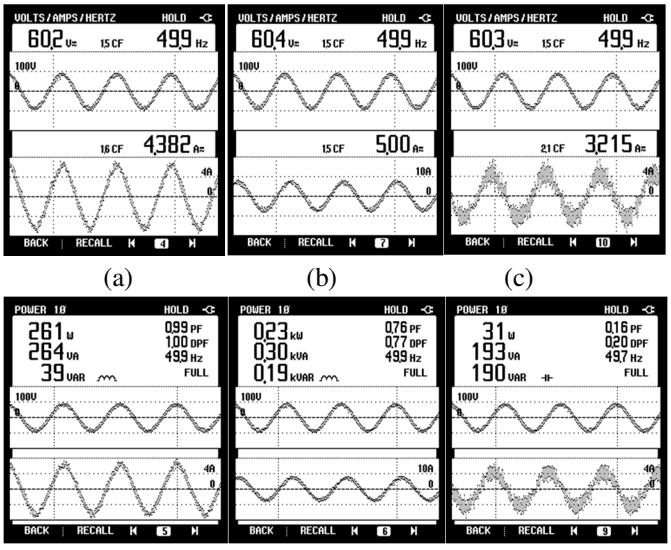


Fig. 5.16 Performance of DSTATCOM in PFC mode under nonlinear load

waveforms of supply power (P_s), load power (P_l) and compensator power (P_C). The values of supply and load apparent powers are 0.264 and 0.30kVA respectively. The power factor on supply side is improved (close to 1 DPF) as the reactive power demand of the load is compensated by DSTATCOM. Fig. 5.18 shows simulated performance of the DSTATCOM under linear load in PFC mode at the same rating for which experimental system is developed. The waveforms of PCC voltages (v_s), supply currents (i_s), load currents (i_{la}, i_{lb} and i_{lc}), compensator current (i_{Ca}, i_{Cb} and i_{Cc}) and self-sustained DC bus voltage (V_{dc}) are presented in these results. It is observed from the results that supply currents are maintained balanced and sinusoidal in steady state and unbalance load conditions.

C. Dynamic Performance of DSTATCOM Under Nonlinear Load in PFC Mode

Dynamic performance of DSTATCOM is presented in Fig. 5.19 under nonlinear load using Wiener filter based control algorithm. Waveforms of the supply currents (i_{sa}, i_{sb} and i_{sc}), load currents (i_{la}, i_{lb} and i_{lc}), compensator current (i_{Ca}, i_{Cb} and i_{Cc}) and phase '*a*' of PCC voltage (v_{sa})



(a) (b) (c)

(d) (e) (f)

Fig. 5.17 Steady-state performance of DSTATCOM at linear lagging PF load in PFC mode (a) v_{sa} and i_{sa} (b) v_{sa} and i_{la} (c) v_{sa} and i_{Ca} (d) P_s (e) P_l (f) P_C

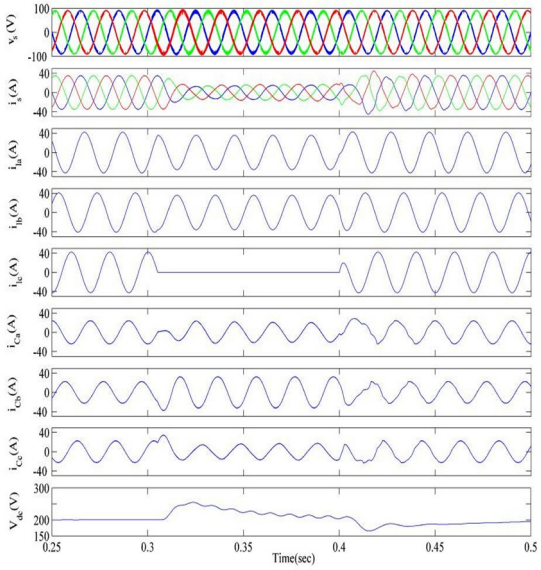


Fig. 5.18 Performance of DSTATCOM in PFC mode under linear load

are shown in Figs. 5.19(a)-(c). It can be observed from these results that the supply currents are balanced and sinusoidal even under unbalanced load conditions. Fig. 5.19(d) shows waveforms of DC bus voltage (V_{dc}), phase '*c*' of supply current (i_{sc}), phase '*c*' of load current (i_{lc}) and phase '*c*' of compensator current (i_{Cc}). It can be observed from this figure that the DC bus voltage achieves its reference voltage of 200V under unbalanced load conditions also when one phase of the load is removed.

D. Steady State Performance of DSTATCOM in Voltage Regulation Mode

Fig. 5.20 shows steady state performance of DSTATCOM in voltage regulation mode using Wiener filter based control algorithm. Figs. 5.20(a), (c) and (e) show waveforms of phase 'a' of supply current (i_{sa}), load current (i_{la}) and compensator current (i_{Ca}) along with PCC voltage (v_{sa}). Figs. 5.20(b), (d) and (f) show harmonic spectra of supply current, load current and PCC voltage. These results present THD of 4.3%, 21.2% and 3.1% in supply current, load current and PCC voltage respectively. Improved THD is achieved in supply current after compensation which is

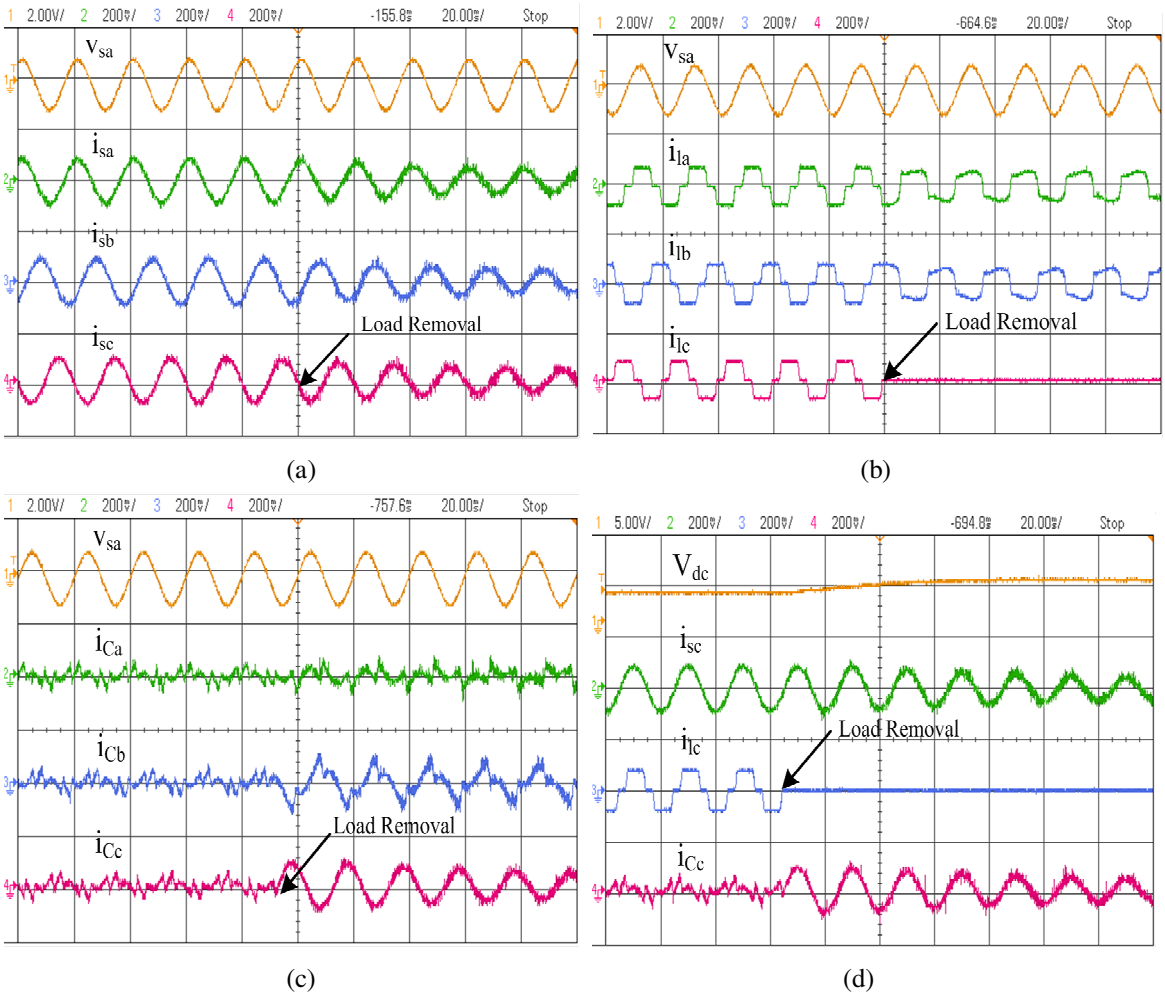


Fig. 5.19 Dynamic performance of DSTATCOM under nonlinear load (a) v_{sa}, supply currents (b) v_{sa}, load currents (c) v_{sa}, compensator currents (d) V_{dc}, i_{sa}, i_{la} and i_{Ca}

within the limit specified by IEEE-519 standard. Figs. 5.20(g), (h) and (i) show reactive powers in supply (Q_s), load (Q_l) and compensator (Q_C). It is observed from this result that reactive powers in supply and load are 0.14kVAR and 0.10kVAR respectively.

Fig. 5.21 shows simulated performance of DSTATCOM in voltage regulation mode at the same voltage rating for which experimental prototype is developed. These results present waveforms of PCC voltages (v_s), supply currents (i_s), load currents (i_{la}, i_{lb} and i_{lc}), compensator current (i_{Ca}, i_{Cb} and i_{Cc}), self-sustained DC bus voltage (V_{dc}) and amplitude of PCC voltage (V_t). It is observed from this result that DC bus voltage and amplitude of PCC voltage are regulated at

their reference value of 200V and 89.9V in steady state (before t=0.3s) and unbalance load condition (t=0.3 t0 t=0.4s) respectively.

E. Dynamic Performance of DSTATCOM in Voltage Regulation Mode

Fig. 5.22 shows the dynamic performance of DSTATCOM in voltage regulation mode. Fig. 5.22(a) presents waveforms of regulated DC bus voltage (V_{dc}), regulated amplitude of PCC voltage (V_t) along with phase 'a' of supply current (i_{sa}) and load current (i_{la}) in steady state and unbalance load conditions. It is observed from these results that supply currents are maintained balanced and sinusoidal in steady state and unbalanced load conditions. The amplitude of PCC voltage magnitude (V_t) is boosted from 85.5V to 89V, as shown in Fig. 5.22(b).

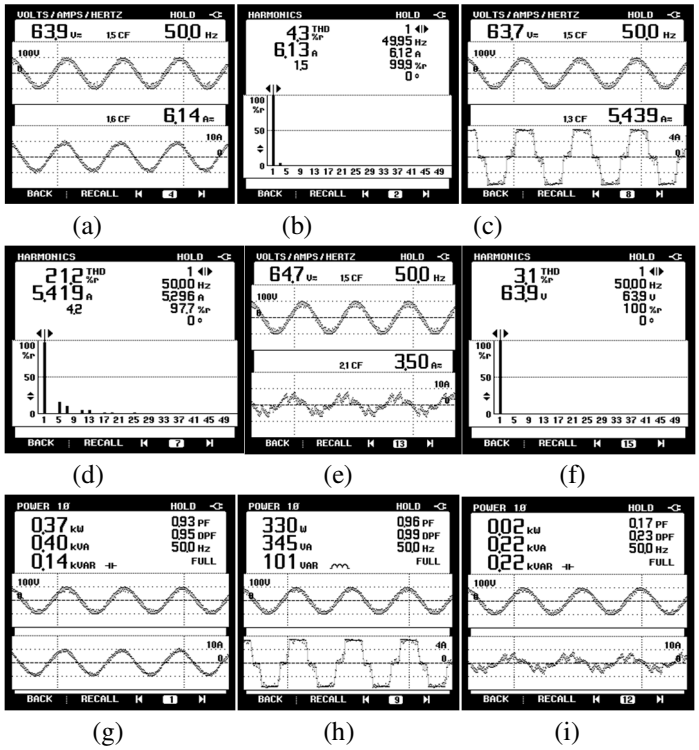


Fig. 5.20 Steady state performance of DSTATCOM under nonlinear load in voltage regulation mode(a),(c) and (e) i_{sa}, i_{la} and i_{Ca} along with v_{sa} (b),(d) and (f) harmonic spectra of i_{sa}, i_{la} and v_{sa} (g),(h) and (i) Q_s, Q_l and Q_C

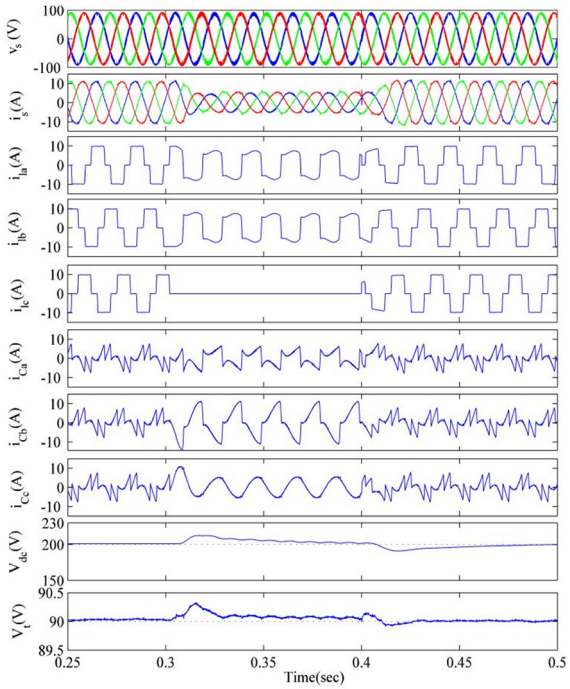
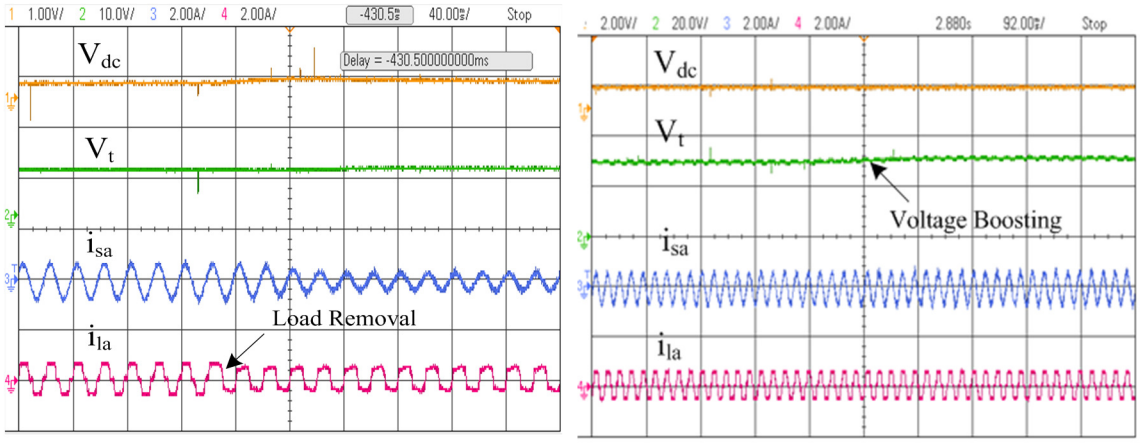


Fig. 5.21 Performance of DSTATCOM in voltage regulation mode under nonlinear load



(a) (b)

Fig. 5.22 Dynamic performance of DSTATCOM in voltage regulation mode under nonlinear load

5.6.2 Performance of DSTATCOM With Least Mean Square Based Control Algorithm

The variants of LMS techniques such as basic LMS, NLMS and SLMS are given in the section 5.3.2. This section deals with the performance of DSTATCOM using NLMS based control algorithm. Various features of DSTATCOM such as harmonics elimination, reactive power compensation and load balancing are discussed in PFC and voltage regulation modes under nonlinear load. Simulation results are studied for both PFC and voltage regulation modes, whereas test results are recorded for PFC mode under nonlinear load. The simulation and experimental test results for NLMS based control algorithms are discussed as follows.

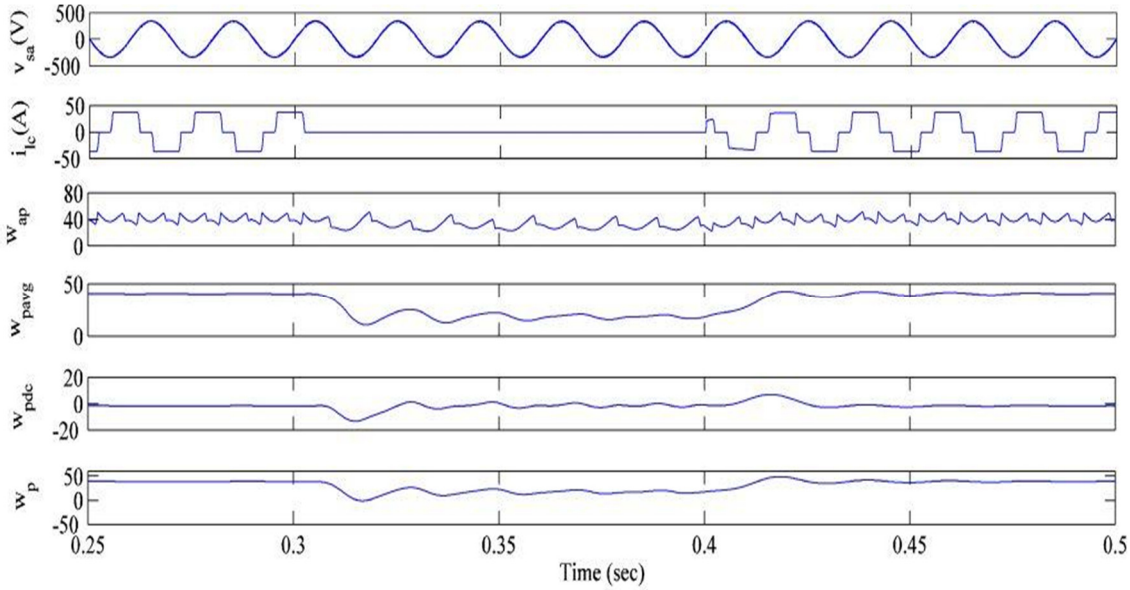
5.6.2.1 Simulated Performance of DSTATCOM in PFC and Voltage Regulation Mode

This section presents the performance of NLMS based control algorithm, performance of the DSTATCOM in PFC and voltage regulation modes along with the intermediate signals. The simulation results of DSTATCOM with NLMS based control algorithm are given as follows.

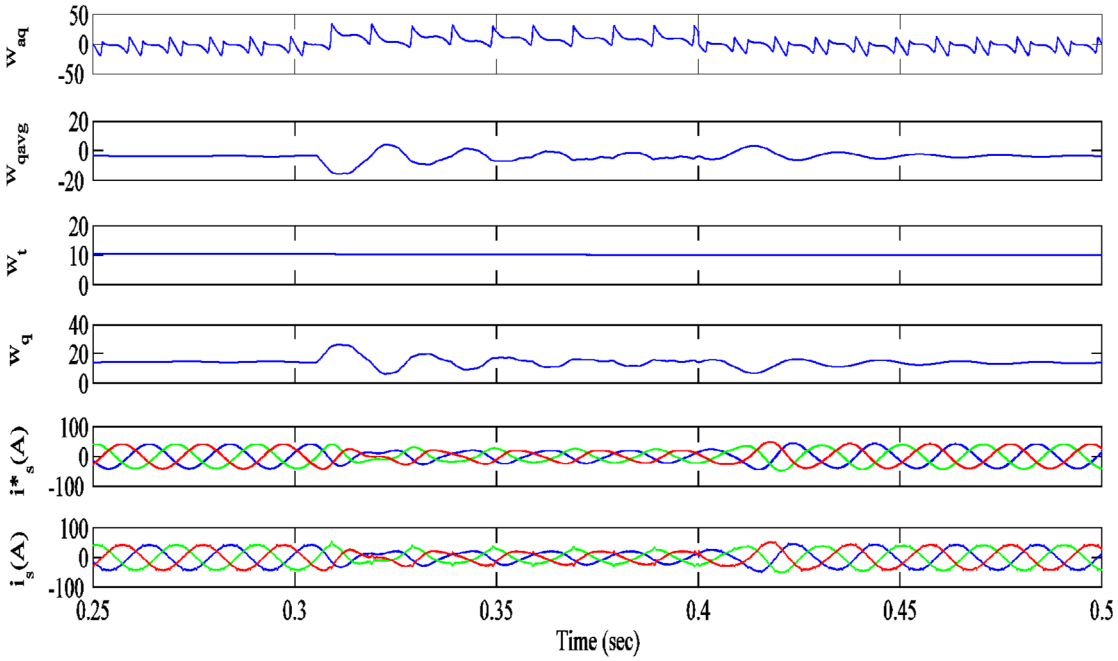
A. Performance and Intermediate Signals of NLMS Based Control Algorithm in Voltage Regulation Mode Under Nonlinear Load

Figs. 5.23(a) and (b) show intermediate signals of NLMS based control algorithm in voltage regulation mode. Fig. 5.23(a) shows waveforms of PCC voltage phase 'a' (v_{sa}), load current

phase ‘c’ (i_{lc}), weight corresponding to phase ‘a’ of load current (w_{ap}), filtered value of average active power weight (w_{pavg}), output of DC bus PI controller (w_{pdc}) and reference active power weight (w_p), which include w_{pavg} and w_{pdc}. These results are presented for steady state condition



(a)



(b)

Fig. 5.23 Performance and intermediate signals of NLMS based control algorithm in voltage regulation mode under nonlinear load

(before t=0.3s) and unbalanced load condition (t=0.3s to t=0.4s), when phase 'c' of load current is switched off. Fig. 5.23(b) shows the waveforms of weighted value (w_{aq}) corresponding to reactive power weight of phase 'a' of load current, filtered value of average reactive power weight (w_{qavg}), output of AC bus PI controller (w_t), reference reactive power weight (w_q), generated reference currents (i_s^*) and supply currents (i_s). It is observed from this figure that the supply currents perfectly track the reference currents in steady state and unbalanced load conditions.

B. Performance of NLMS Based Control Algorithm in PFC Mode Under Nonlinear Load

Fig. 5.24 shows the waveforms of PCC voltages (v_s), supply currents (i_s), load currents (i_{la}, i_{lb}

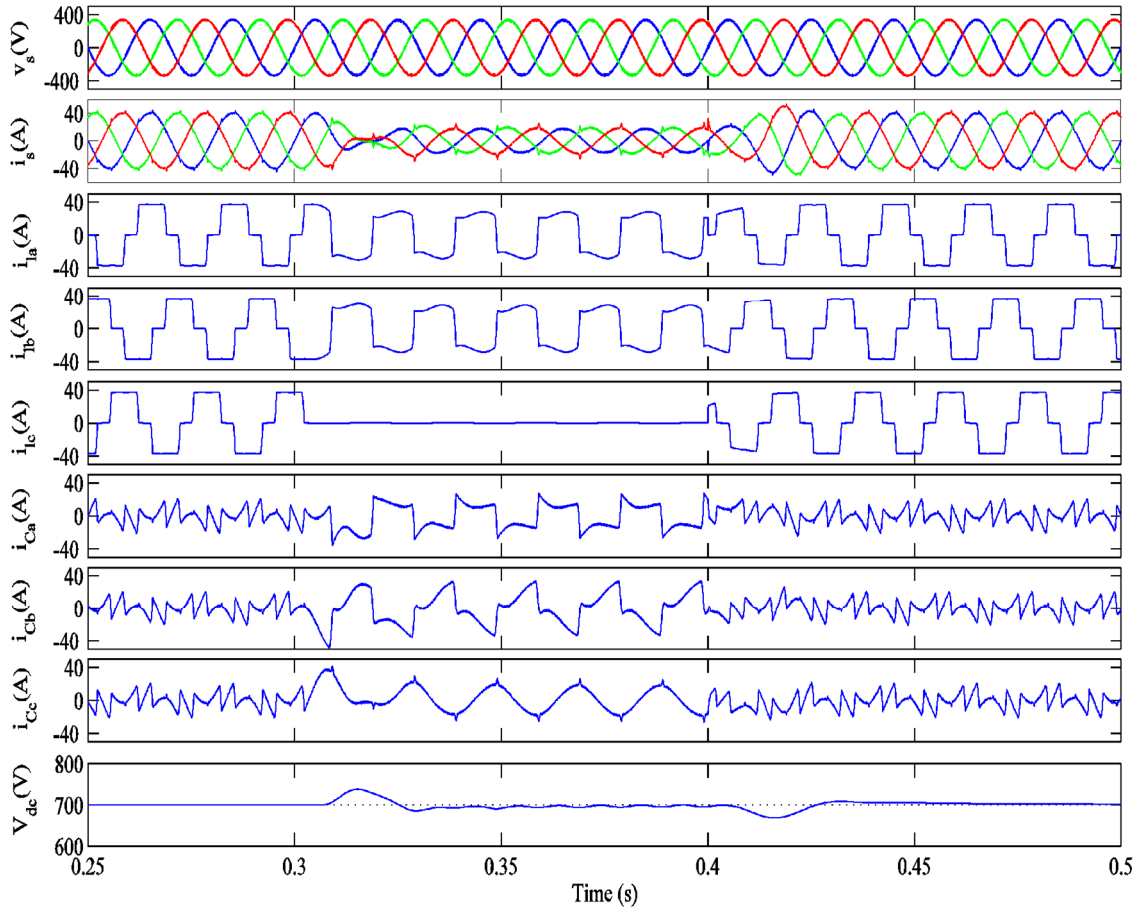


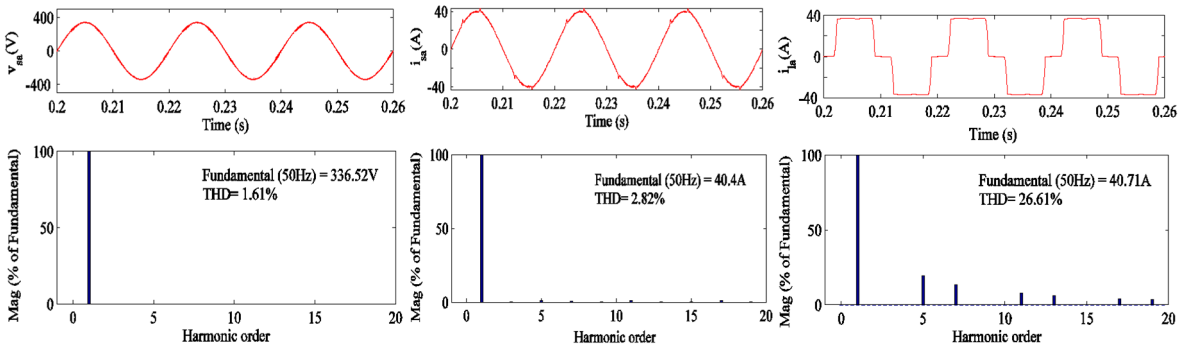
Fig. 5.24 Performance of NLMS based control algorithm in PFC mode

and i_{lc}), compensator currents (i_{Ca}, i_{Cb} and i_{Cc}) and self-sustained DC bus voltage (V_{dc}). These results are presented for both steady state and unbalanced load conditions. During steady state (till t=0.3s) condition, it is observed that supply currents are balanced and sinusoidal. The voltage at DC bus is regulated to the reference value of 700V. An unbalancing is created in load during t=0.3s to 0.4s, when phase 'c' of load is switched off. It is observed from these results that during unbalancing, the supply currents are still balanced and sinusoidal. The voltage at the DC bus achieves its reference value within a couple of cycles.

Fig. 5.25 shows the harmonic spectra of phase 'a' of supply voltage (v_{sa}), supply current (i_{sa}) and load current (i_{la}). The THDs of 1.61%, 2.82% and 26.61% are obtained in v_{sa}, i_{sa} and i_{la} respectively. It is observed from these results that 2.82% THD is obtained in supply current, whereas there is 26.61% THD in load current. The THD in supply voltage and supply current lies within the limit specified by international standard such as IEEE-519.

C. Performance of NLMS Based Control Algorithm in Voltage Regulation Mode Under Nonlinear Load

Fig. 5.26 shows the waveforms of PCC voltages (v_s), supply currents (i_s), load currents (i_{la}, i_{lb} and i_{lc}), compensator currents (i_{Ca}, i_{Cb} and i_{Cc}), self-sustained DC bus voltage (V_{dc}) and PCC voltage



(a) (b) (c)

Fig. 5.25 Harmonic spectra of phase 'a' of (a) supply voltage, v_{sa} (b) supply current, i_{sa} (c) load current, i_{la} in PFC mode

magnitude (V_t). The system is under steady state condition upto t=0.3s, and during this time it is observed that the supply currents are balanced and sinusoidal. The voltage at DC bus and PCC voltage magnitude are regulated to their reference values of 700V and 338.8V respectively. An unbalancing is created in the load during t=0.3s to 0.4s, when phase 'c' of load is switched off. During load unbalancing, it is observed that supply currents are still balanced and sinusoidal although reduced in magnitude. The voltage at the DC bus and PCC voltage magnitude achieve their reference values within a couple of cycles.

Fig. 5.27 shows the harmonic spectra of phase 'a' of supply voltage (v_{sa}), supply current (i_{sa}) and

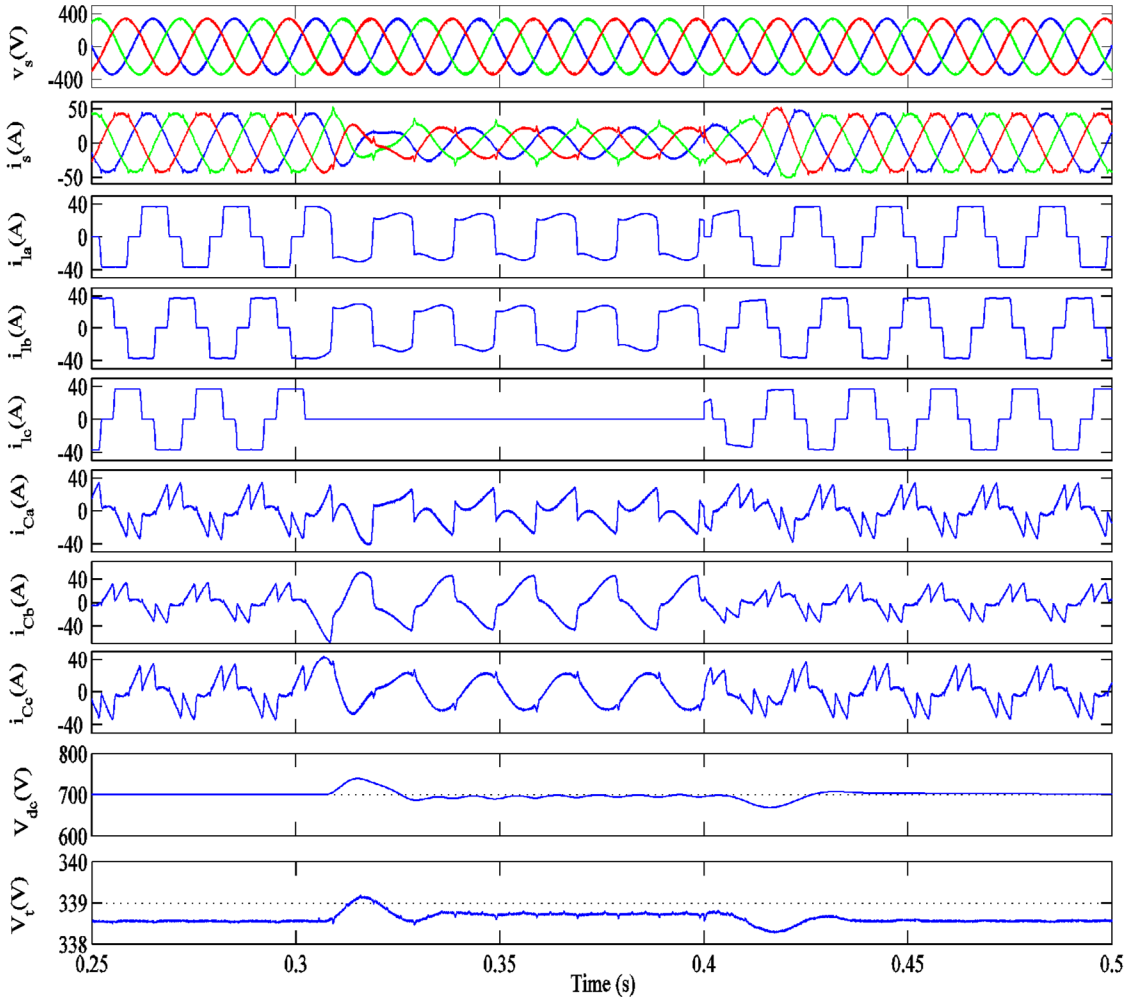
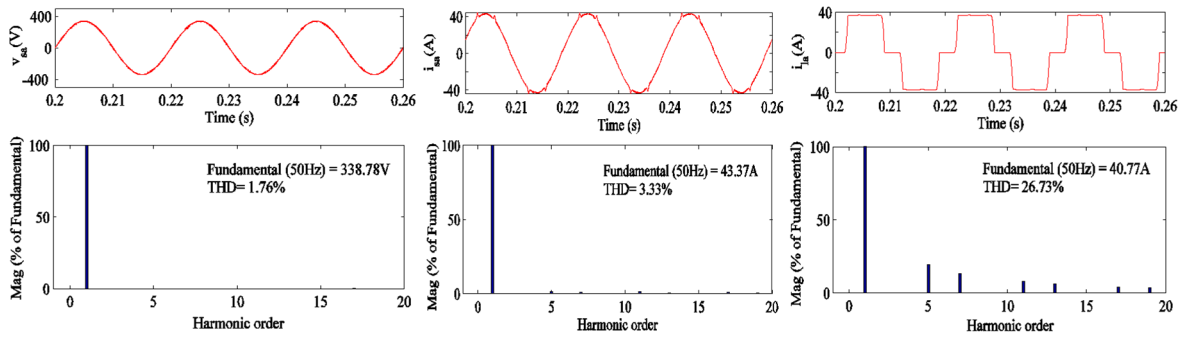


Fig. 5.26 Performance of NLMS based control algorithm in voltage regulation mode



(a) (b) (c)

Fig. 5.27 Harmonic spectra of phase 'a' of (a) supply voltage, v_{sa} (b) supply current, i_{sa} (c) load current, i_{la} in voltage regulation mode

load current (i_{la}). These results show THDs of 1.76%, 3.33% and 26.73% in v_{sa}, i_{sa} and i_{la} respectively. These results show the THD of 3.33% obtained in supply current, whereas there is THD of 26.73% of load current. The THD obtained in supply voltage and supply current lie within the limit specified by IEEE-519 standard.

5.6.2.2 Experimental Performance of DSTATCOM With NLMS Based Control Algorithm in PFC Mode

Experimental performance of DSTATCOM in PFC mode is presented in this section. The first part discusses the performance and intermediate signals for NLMS based control algorithm and the second part discusses the performance of DSTATCOM in steady state and dynamic conditions.

A. Performance of the NLMS Based Control Algorithm for DSTATCOM

Fig. 5.28 shows the performance of NLMS based control algorithm for DSTATCOM under nonlinear load. Fig. 5.28(a) shows waveforms of phase 'a' of PCC voltage (v_{sa}), PCC filtered voltage (v_{saf}), phase 'c' of load current (i_{lc}) and step size parameter ($\mu(k)$). Fig. 5.28(b) shows reference DC bus voltage (V_{dc}^{*}), sensed DC bus voltage (V_{dc}), filtered DC bus voltage (V_{dcf}) and output of DC bus PI controller (w_{pdc}).

Fig. 5.28(c) shows averaged value of active power weight (w_{pavg}), output of DC bus PI controller (w_{pdc}) and their summation which is reference active power weight (w_p) along with filtered DC bus voltage (V_{dcf}). Fig. 5.28(d) shows phase 'a' of load current (i_{la}), its estimated fundamental

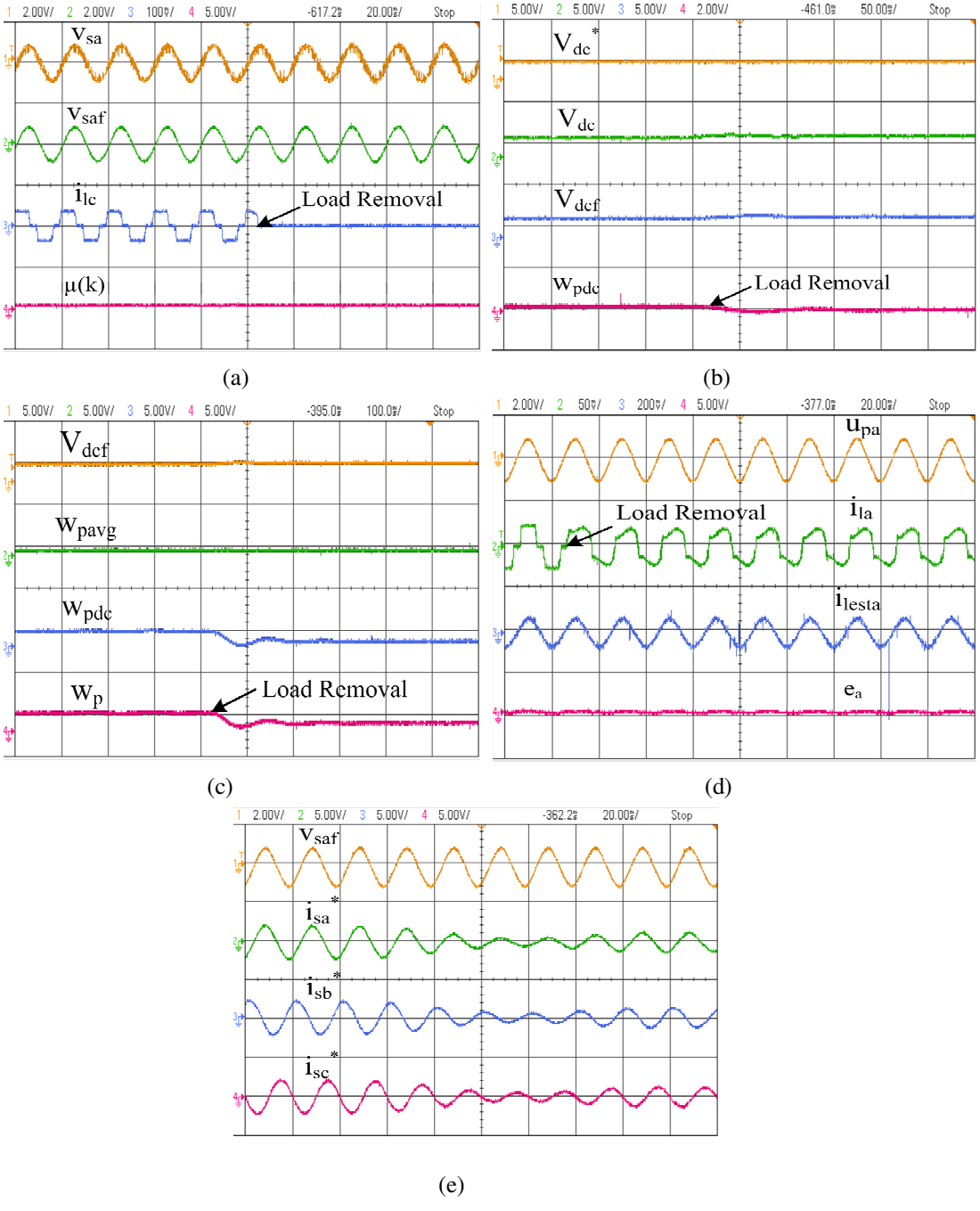


Fig. 5.28 Performance and intermediate signals of NLMS based control algorithm under nonlinear load

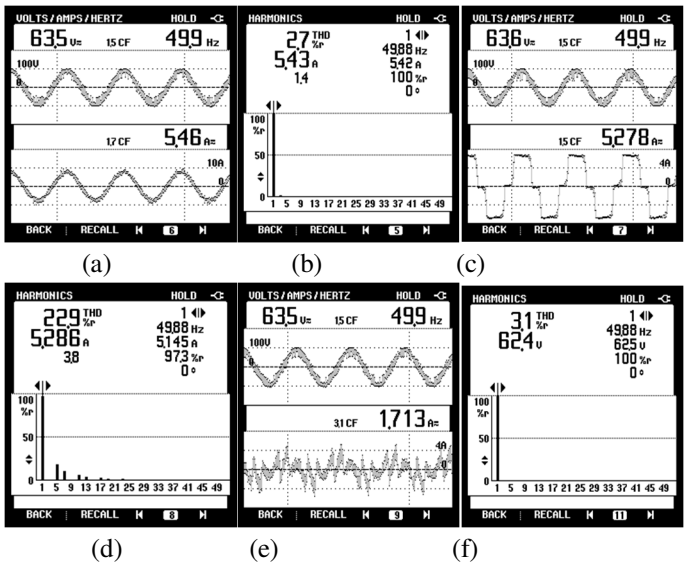
component (i_{esta}) and error between them (e_a) along with inphase unit template of PCC voltage (u_{pa}). Fig. 5.28(e) shows the reference supply currents (i_{sa}^*, $i_{sb}^*$and i_{sc}^*) along with phase 'a' of filtered PCC voltage (v_{taf}). It is observed that the phase 'a' of reference supply current is in phase with v_{taf} showing power factor correction. These results are shown for steady state as well as unbalanced load conditions, which is created when phase 'c' of load is switched off. The performance of the NLMS based control algorithm is observed to be satisfactory under steady state as well as dynamic load conditions.

B. Steady State Performance of DSTATCOM With NLMS Based Control Algorithm Under Nonlinear Load

Fig. 5.29 shows the performance of DSTATCOM in steady state condition. Figs. 5.29(a), (c) and (e) show the waveforms for supply current, load current and compensator current (i_{sa}, i_{la} and i_{Ca}) along with PCC voltage (v_{sa}). Figs. 5.29(b), (d) and (f) show harmonic spectra of supply current, load current and PCC voltage which have THDs of 2.7%, 22.9% and 3.1% in i_{sa}, i_{la} and v_{ta} respectively. It is observed from these test results that 2.7% THD is obtained in i_{sa}, whereas there is 22.9% THD in i_{la}. The THDs in supply current and PCC voltage are within the limit specified by international standards.

Fig. 5.30 shows simulated performance of DSTATCOM using NLMS based control algorithm at the same voltage rating for which experimental prototype is developed. Waveforms of PCC voltages (v_s), supply currents (i_{sa}, i_{sb} and i_{sc}), load currents (i_{la}, i_{lb} and i_{lc}), compensator currents (i_{Ca}, i_{Cb} and i_{Cc}) and DC bus voltage (V_{dc}) are shown in these results. It is observed from these results that supply currents are balance and sinusoidal in steady state (before t=0.3s) and unbalanced (t=0.3s to t=0.4s) load condition. The DC bus voltage is regulated at the reference voltage of 200V.

C. Dynamic Performance of DSTATCOM Under Unbalance Load Condition



(a) (b) (c)

(d) (e) (f)

Fig. 5.29 Steady state performance of DSTATCOM controlled using NLMS based control algorithm (a) v_{sa}, i_{sa} (b) Harmonic spectrum of, i_{sa} (c) v_{sa}, i_{la} (d) Harmonic spectrum of, i_{la} (e) v_{sa}, i_{Ca} (f) Harmonic spectrum of v_{sa}

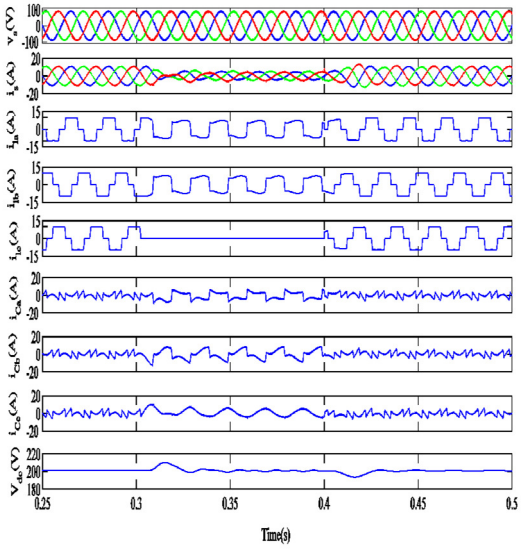


Fig. 5.30 Performance of DSTATCOM in PFC mode

Fig. 5.31 shows the responses of the system under unbalanced load conditions. Figs. 5.31(a)-(c) show the variation of supply currents (i_{sa}, i_{sb} and i_{sc}), load currents (i_{la}, i_{lb} and i_{lc}) and compensator currents (i_{Ca}, i_{Cb} and i_{Cc}) along with phase 'a' of PCC voltage (v_{sa}) in steady state and unbalanced load condition. It is observed from these results that supply currents are balanced and sinusoidal with reduced magnitude, in case of unbalanced load. Fig. 5.31(d) shows the variation of V_{dc} along with phase 'c' of supply current, load current and compensator current (i_{sa}, i_{la} and i_{Ca}) under steady state conditions and unbalanced load condition. The DC bus voltage rises when the load is removed. However, the controller action is able to bring the DC bus voltage back to its reference value of 200V.

5.6.3 Performance of DSTATCOM With Variable Step Size Least Mean Square Based Control Algorithm

The performance of DSTATCOM for power quality improvement features such as harmonics reduction, reactive power compensation and load balancing is studied in PFC and voltage regulation modes under nonlinear load. Simulation results are studied for both PFC and voltage

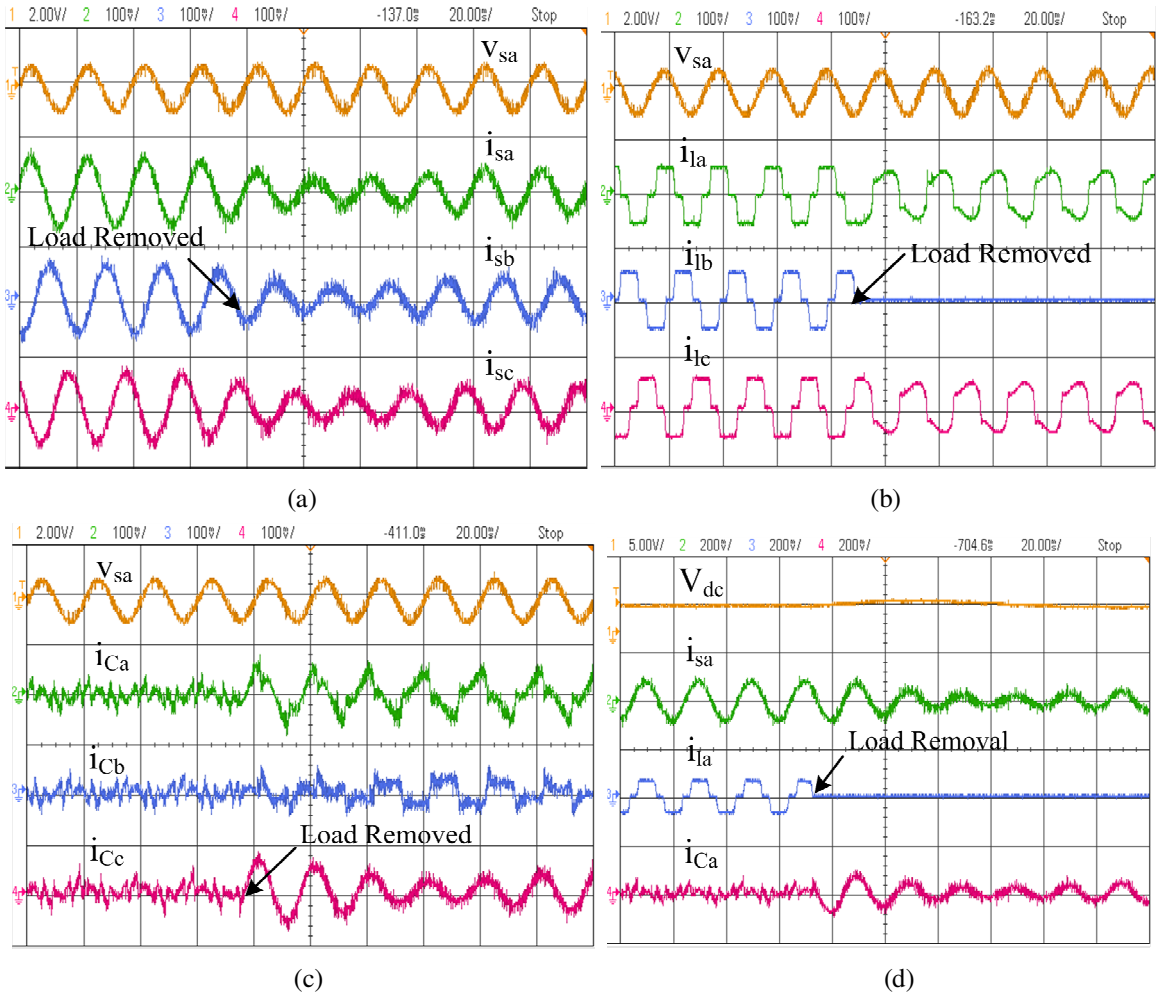


Fig. 5.31 Dynamic performance of shunt compensator under nonlinear load using NLMS based control algorithm

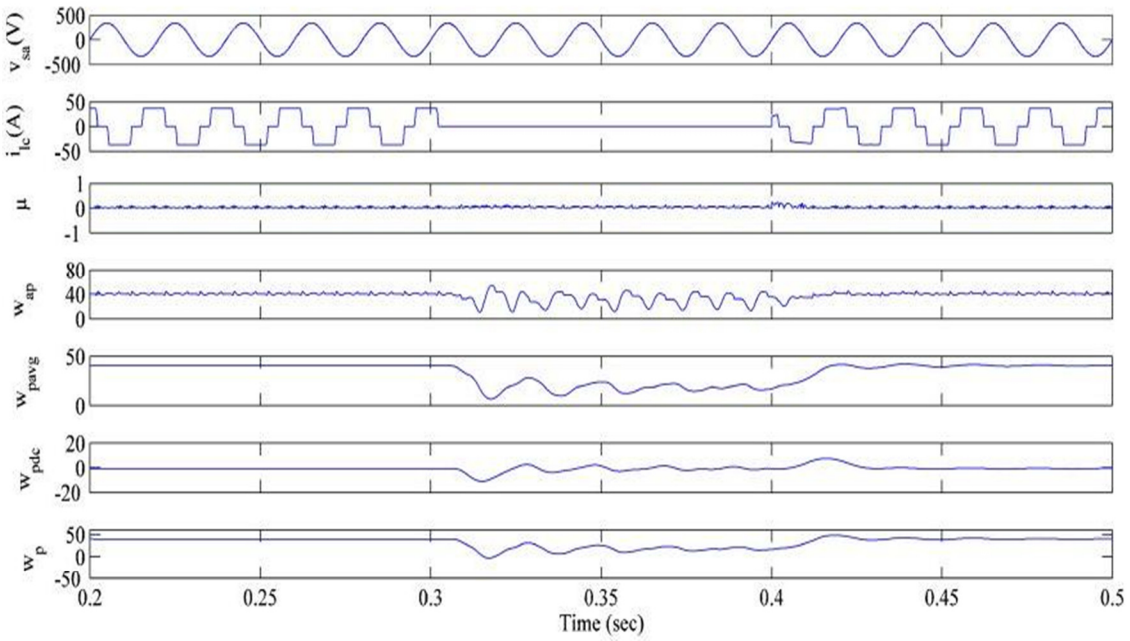
regulation modes, whereas test results are recorded for PFC mode under nonlinear load. The simulation and test results for VSSLMS based control algorithms are discussed as follows.

5.6.3.1 Simulated Performance of DSTATCOM in PFC and Voltage Regulation Modes With VSSLMS Based Control Algorithm

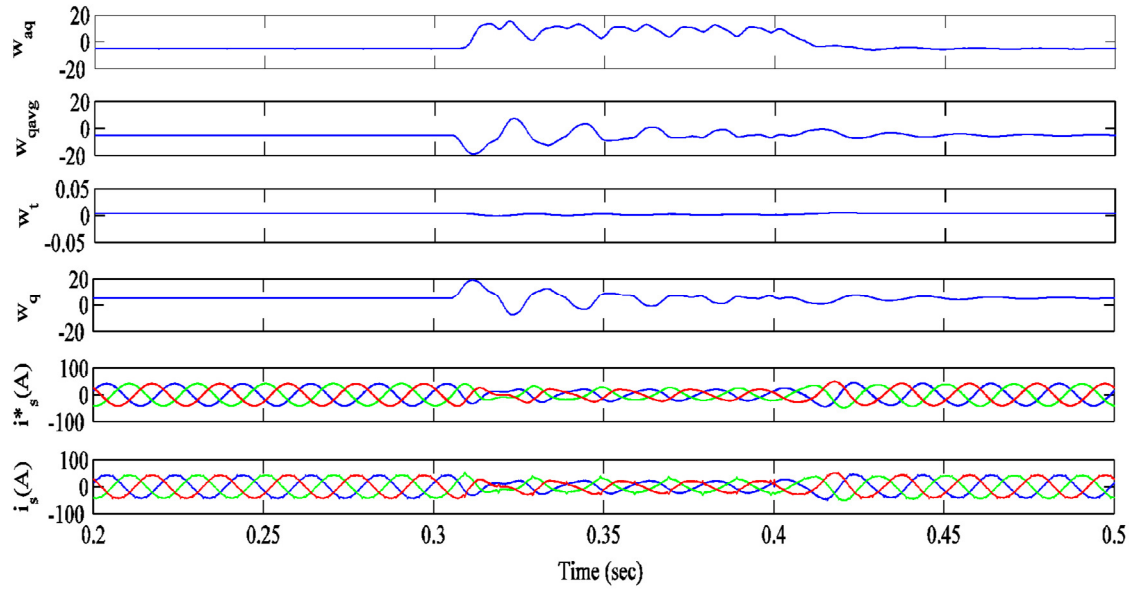
This section presents the performance and intermediate signals obtained with VSSLMS based control algorithm for DSTATCOM. The performance of the system with DSTATCOM controlled in PFC and in voltage regulation modes are studied here.

A. Performance and Intermediate Signals of VSSLMS Based Control in Voltage Regulation Mode Under Nonlinear Load

Figs. 5.32(a) and (b) show the simulation results obtained along with the intermediate signals using VSSLMS based control algorithm in voltage regulation mode. Fig. 5.32(a) shows the waveforms of PCC voltage phase 'a' (v_{sa}), load current phase 'c' (i_{lc}), variable step size (μ),



(a)



(b)

Fig. 5.32 Performance and intermediate signals of VSSLMS based control algorithm in voltage regulation mode under nonlinear load

weighted value corresponding to phase 'a' of load current (w_{ap}), filtered value of average active power weight (w_{pavg}), output of DC bus PI controller (w_{pdc}) and reference active power weight (w_p), which is the addition of w_{pavg} and w_{pdc}. These results are presented for steady state condition (before t=0.3s) and unbalanced load condition (t=0.3s to t=0.4s), when phase 'c' of load current is switched off. Fig. 5.32(b) shows the waveforms of weight (w_{aq}) corresponding to reactive power component of phase 'a' of load current, filtered value of average reactive power weight (w_{qavg}), output of AC bus PI controller (w_t), reference reactive power weight (w_q), generated reference currents (i_s^*) and supply currents (i_s). It is observed from these results that the supply currents perfectly track the reference supply currents in steady state and unbalanced load conditions, as determined by the algorithm. It is observed that the performance of the system is satisfactory under varying load conditions as highlighted in this figure.

B. Performance of DSTATCOM in Power Factor Correction Mode Using VSSLMS Algorithm

The response of the system with DSTATCOM under varying nonlinear load is shown in Fig. 5.33 for VSSLMS algorithm. This represents the waveforms of PCC voltages (v_s), supply currents (i_s), load currents (i_{la}, i_{lb} and i_{lc}), compensator currents (i_{Ca}, i_{Cb} and i_{Cc}) and DC bus voltage (V_{dc}). It can be observed here that even when the load currents are unbalanced due to removal of phase 'c' up to t=0.8s, the voltage at DC bus is regulated to its reference value of 750V by PI controller action. After t=0.8s, phase 'c' of the load is reconnected and unbalancing in load is removed. It is observed from these results that when the load is suddenly reconnected at t=0.8s, a dip in DC bus voltage is observed. The DC bus voltage takes around one cycle (t=0.8s to t=0.82s) to regain its voltage back to the reference value. During dynamic load changes (t=0.8s to t=0.82s), there is a slight distortion in supply currents but as soon as DC bus

voltage is restored back to its reference value by PI controller action, the supply currents become perfectly balanced and sinusoidal.

The harmonic spectra of phase 'a' of PCC voltage (v_{sa}), supply current (i_{sa}) and load current (i_{la}) are shown in Fig. 5.34. It can be observed from these results that the THDs in phase 'a' PCC voltage, supply current and load current are 1.61%, 1.72% and 26.66% respectively. This shows the improved THD in supply current 1.72%, whereas there is 26.66% THD in load current. The THD in supply current lies within the limit of limit of 5% as specified in IEEE-519 standard. These results validate the satisfactory performance of DSTATCOM under power quality aspects

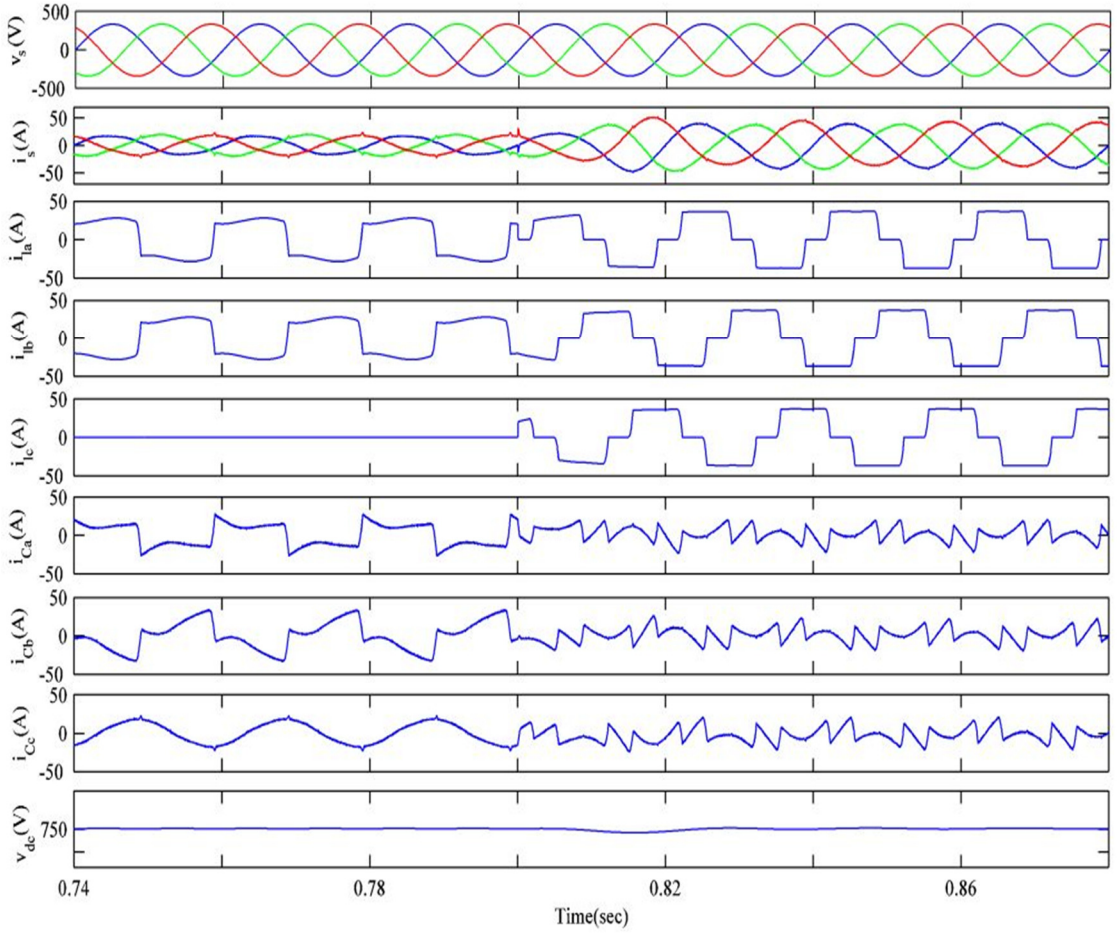
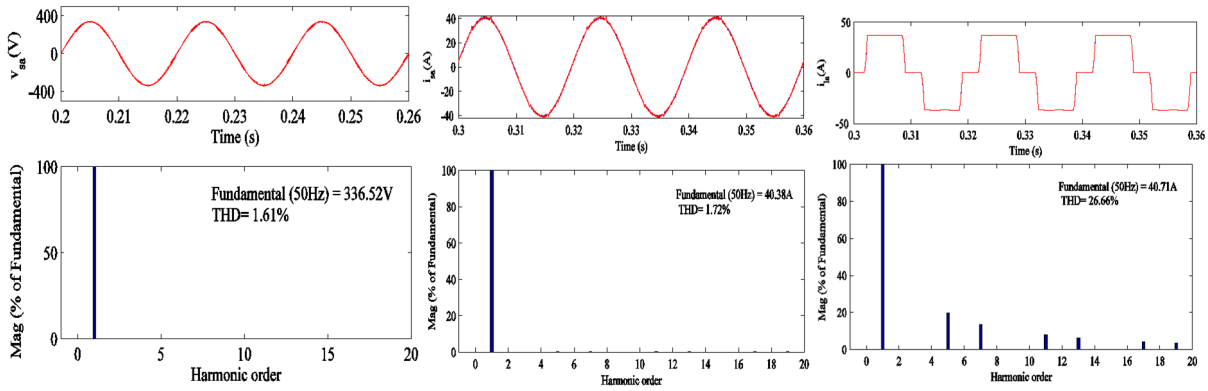


Fig. 5.33 Dynamic performance of compensator for PFC mode under varying non-linear load



(a) (b) (c)

Fig. 5.34 Harmonic spectra of (a) PCC voltage (b) source current (i_{sa}) and (b) load current (i_{la}) in PFC using VSSLMS

such as load balancing and harmonics reduction.

C. Performance of DSTATCOM in Voltage Regulation Mode Using VSSLMS

The response of DSTATCOM for voltage regulation mode under varying nonlinear load is shown in Fig. 5.35. These results show the waveforms of PCC voltages (v_s), supply currents (i_s), load currents (i_{la}, i_{lb} and i_{lc}), compensator currents (i_{Ca}, i_{Cb} and i_{Cc}), voltage at DC bus (V_{dc}) and amplitude of PCC voltage (V_t). It is observed here that the load currents are unbalanced due to removal of phase 'c' up to t=0.8s. The DC bus voltage is regulated to its reference value of 750V under steady state condition and the PCC voltage is maintained at its reference voltage of 338.8V. At t=0.8s, phase 'c' of load current is reconnected and unbalancing in the load is removed. It is observed from these results that dip in DC bus voltage and PCC voltage are experienced when the load is suddenly reconnected. The DC bus voltage and PCC voltage take around one cycle (t=0.8s to t=0.82s) to regain their reference values of 700V and 338.8V respectively. The harmonic spectra of phase 'a' of PCC voltage (v_{sa}), supply current (i_{sa}) and load current (i_{la}) are shown in Fig. 5.36. It is observed from these results that the THDs of phase 'a' PCC voltage (v_{sa}), supply current (i_{sa}) and load current (i_{la}) are 1.76%, 2.32 % and 26.66%.

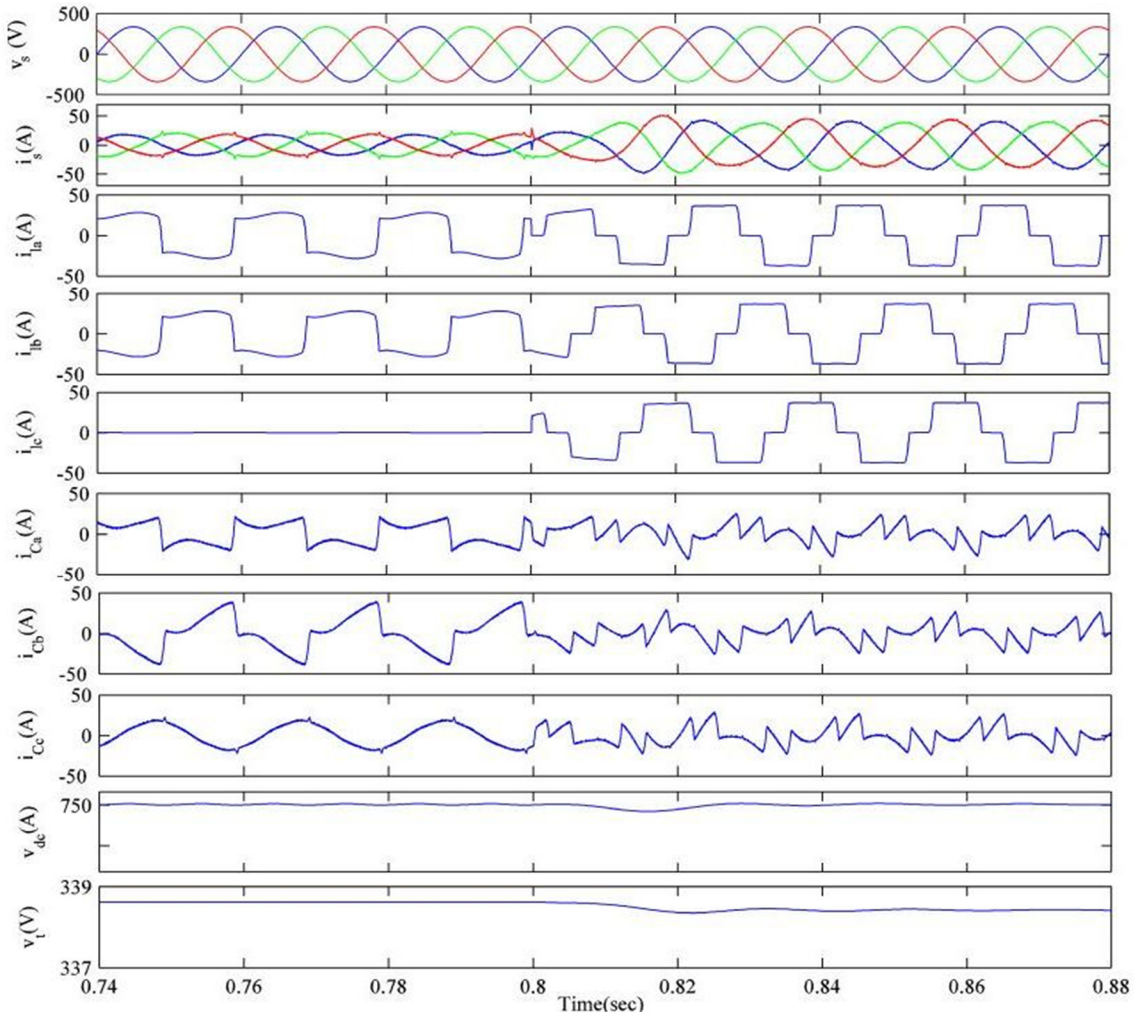
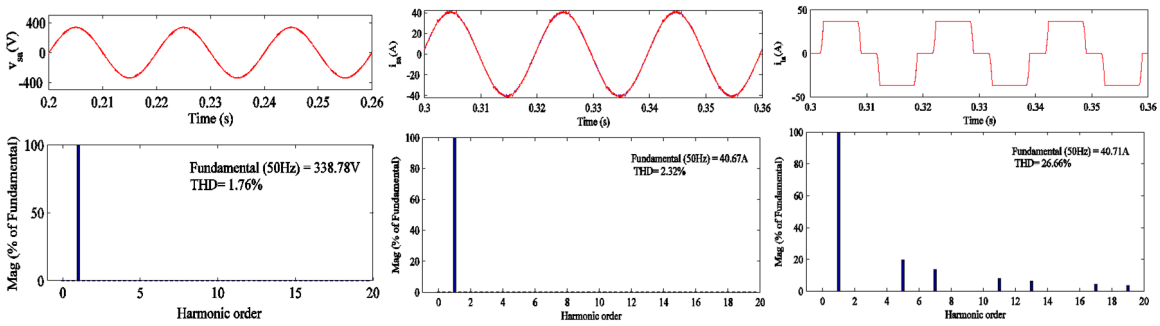


Fig. 5.35 Dynamic performance of compensator for voltage regulation mode under varying nonlinear load for VSSLMS

The THD achieved in supply current is 2.32%, whereas there is 26.66% THD in load current. The THD in supply current lies within the limit specified by IEEE-519 standard. These results show the performance of DSTATCOM is satisfactory in regulating the PCC voltage, load balancing and harmonic elimination in voltage regulation mode.

5.6.3.2 Experimental Performance of DSTATCOM in PFC Mode With VSSLMS Based Control Algorithm

The experimental results of control algorithm are taken by prototype developed in the laboratory.



(a) (b) (c)

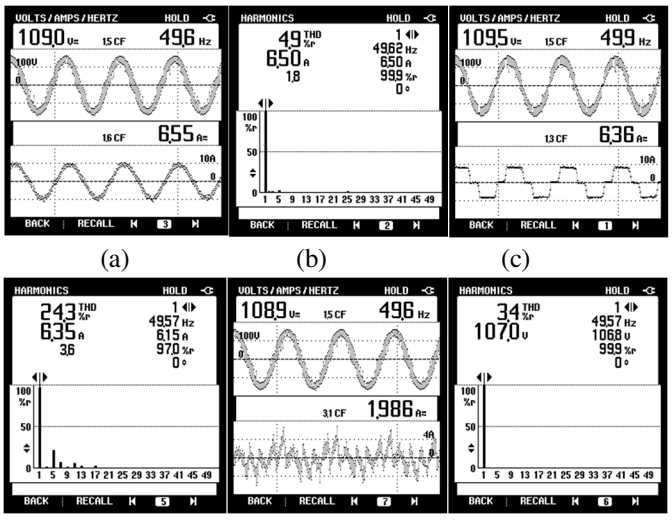
Fig. 5.36 Harmonic spectra of (a) PCC voltage (a) source current (i_{sa}) and (b) load current (i_{la}) in voltage regulation using VSSLMS

Experimental test results of the system with DSTATCOM are presented here. The steady state performance of the system is discussed first and then the dynamic performance of DSTATCOM using VSSLMS control algorithm is presented.

A. Steady State Performance of the System with DSTATCOM Under Nonlinear Load

Fig. 5.37 shows the steady state performance of DSTATCOM under nonlinear load. Figs. 5.37 (a) and (b) show PCC line voltage (v_{ab}) with phase 'a' of supply current and harmonics spectrum of supply current, which has THD of the order of 4.9% after compensation. Fig. 5.37 (c) and (d) show PCC voltage (v_{ab}) along with phase 'a' of load current (i_{la}) and harmonics spectrum of load current, which has THD of the order of 24.3%. Fig. 5.37(e) shows the phase 'a' compensator current (i_{Ca}) along with PCC voltage (v_{ab}). Fig. 5.37(f) shows harmonic spectrum of PCC voltage, which has THD of 3.4%. It can be observed from these test results that supply current has THD of 4.9%, whereas there is a THD of 24.3% in load current. The THD value of supply voltage and supply current lie within the permitted limit of IEEE-519 standard.

Fig. 5.38 shows simulated performance of DSTATCOM using VSSLMS based control algorithm at the same voltage rating for which experimental prototype is developed. Waveforms of PCC



(a) (b) (c)

(d) (e) (f)

Fig. 5.37 Steady state performance of DSTATCOM (a), (c) and (e) i_{sa}, i_{la} and i_{Ca} along with v_{ab} (b), (d) and (f) harmonic spectra of i_{sa}, i_{la} and v_{ab}

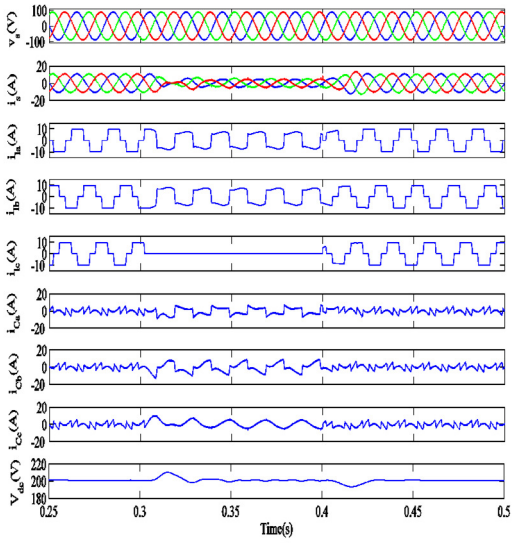


Fig. 5.38 Performance of DSTATCOM in PFC mode

voltages (v_s), supply currents (i_{sa}, i_{sb} and i_{sc}), load currents (i_{la}, i_{lb} and i_{lc}), compensator currents (i_{Ca}, i_{Cb} and i_{Cc}) and DC bus voltage (V_{dc}) are shown in these results. It is observed from these results that supply currents are balanced and sinusoidal in steady state (before t=0.3s) and unbalanced (t=0.3s to t=0.4s) load condition. The DC bus voltage is regulated at the reference voltage of 200V in steady state as well as in dynamic load conditions.

B. Dynamic Performance of System with DSTATCOM Under Nonlinear Load

Fig. 5.39 shows the dynamic performance of DSTATCOM under nonlinear load. Fig. 5.39(a)-(c) shows supply currents (i_{sa}, i_{sb} and i_{sc}), load currents (i_{la}, i_{lb} and i_{lc}) and compensator currents (i_{Ca}, i_{Cb} and i_{Cc}) along with PCC voltage of phase 'a' (v_{sa}). These test results are shown for steady state and unbalanced load conditions, when phase 'c' of load current is switched off. It is observed from these results that supply currents are perfectly balanced and sinusoidal in steady state and unbalanced load condition. The dynamics of DC bus voltage (V_{dc}) with phase 'c' of supply current (i_{sc}), load current (i_{lc}) and compensator current (i_{Cc}) are shown in Fig. 5.40(a). An

unbalancing in the load is created by removing one phase of load and it is observed that DC bus voltage settles down to a reference value of 200V within a cycle due PI controller action. Dynamic performance of the weights corresponding to fundamental power component of load currents (w_{ap}, w_{bp} and w_{cp}) with variable step size $\mu(k)$ are shown in Fig. 5.40(b). It can be observed from this figure that the magnitude of weight corresponding to phase 'c' (w_{cp}) becomes zero when the load in this phase is removed and the weights corresponding to other two phases (w_{ap} and w_{bp}) are reduced in magnitude. The value of variable step size $\mu(k)$ is also affected by

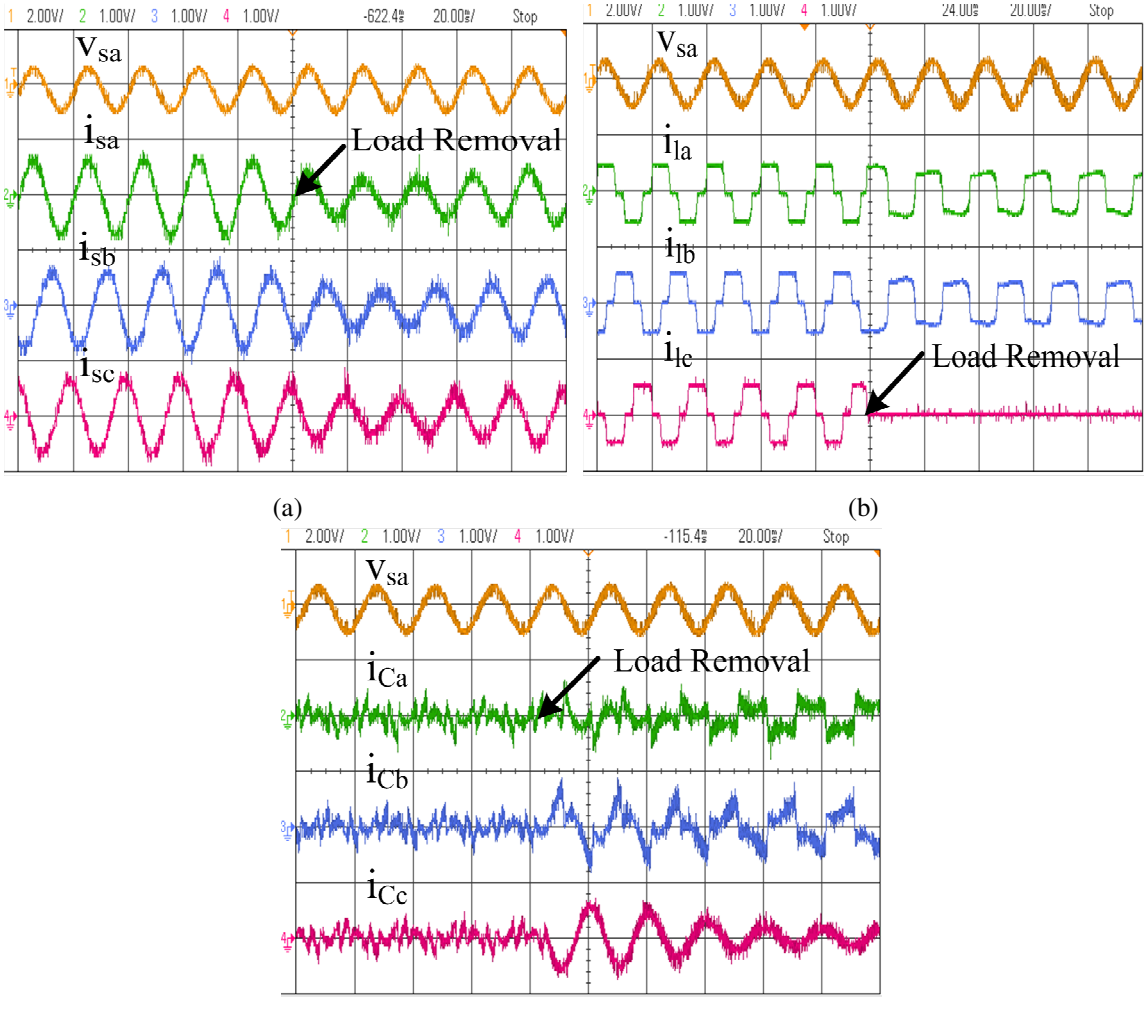
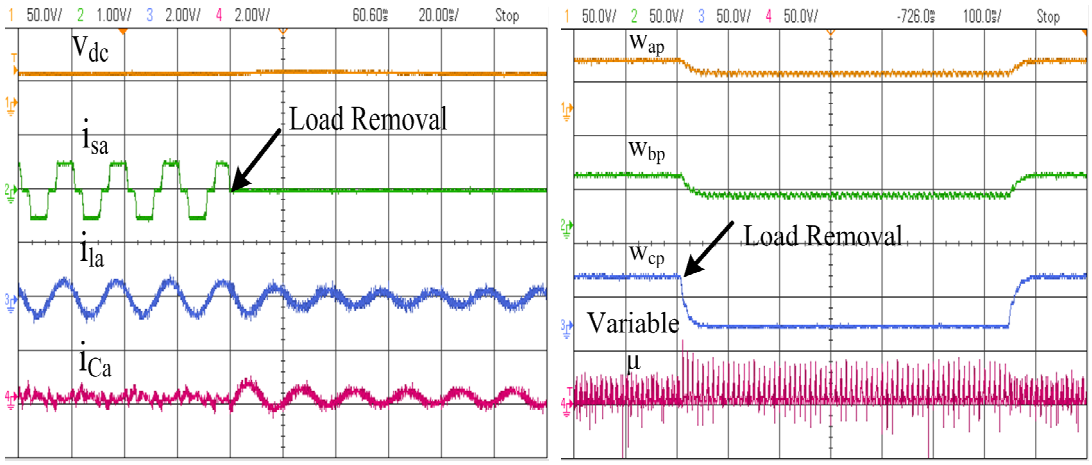


Fig. 5.39 Dynamic performance of DSTATCOM using VSSLMS based control algorithm (a) v_{sa}, i_{sa}, i_{sb} and i_{sc} (b) v_{sa}, i_{la}, i_{lb} and i_{lc} (c) v_{sa}, i_{Ca}, i_{Cb} and i_{Cc}



(a) (b)

Fig. 5.40 Dynamic performance of DSTATCOM (a) V_{dc}, i_{sc}, i_{lc} and i_{Cc} (b) w_{ap}, w_{bp}, w_{cp} and Variable μ

load unbalancing. These test results show the satisfactory performance of the shunt compensator under dynamics in maintaining DC bus voltage and fast weight convergence.

5.7 CONCLUSIONS

This chapter has presented mathematical formulation and performances of adaptive theory based control algorithms for DSTATCOM. The adaptive theory based control techniques such as Wiener filter, least mean square and variable step size least mean square based control algorithms have been developed. Mathematical analysis and formulation of these control algorithms have been presented. The simulated performances of these control algorithms have been presented for various power quality problems such as harmonics, power factor and load unbalancing in both PFC and voltage regulation modes. Real time performances of these control algorithms have been tested on developed laboratory prototype in the laboratory. Test results have shown 2.3%, 2.7% and 4.9% THD in supply current in case of Wiener filter, NLMS and VSSLMS based control algorithms respectively. Supply currents have been achieved balanced and sinusoidal during balanced and unbalanced load conditions.

CHAPTER-VI
RECURSIVE THEORY BASED CONTROL ALGORITHMS FOR DSTATCOM

6.1 GENERAL

In the previous chapter, adaptive theory based control algorithms have been used for the control of DSTATCOM. This chapter deals with recursive theory based control algorithms, which calculate the coefficients in a recursive manner to minimize a weighted linear least square cost function. In the recursive techniques, computation starts with initial conditions and the information contained in new data samples is used to update the old estimated values. These recursive theory based control algorithms include such as variable forgetting factor recursive least square (VFFRLS), recursive inverse (RI) and immune feedback. Mathematical formulation, MATLAB/SIMULINK based simulation study and DSP based implementation of these control algorithms are carried out for control of DSTATCOM. These control algorithms are used to estimate the fundamental active and reactive power components of load currents and their average weights are computed. These average weights are used to estimate reference supply currents. Various functions of DSTATCOM such as harmonic elimination, reactive power compensation and load balancing are demonstrated in power factor correction (PFC) and voltage regulation modes.

6.2 CONFIGURATION AND OPERATING PRINCIPLE OF DSTATCOM

The DSTATCOM is a shunt connected device where IGBTs based voltage source converter (VSC) is used. Fig. 6.1 shows the schematic diagram of VSC based DSTATCOM. A three-phase, AC mains with grid impedance, shown using series L_s-R_s branch, feeds a three phase nonlinear load. The DSTATCOM is designed using three-leg voltage source converter (VSC) which uses six insulated gate bipolar transistors (IGBTs) with anti-parallel diodes and DC link capacitor (C_{dc}) at DC side. Interfacing inductors (L_f) are used at the AC side of VSC, which

couple the VSC to the grid. High frequency switching noise generated by switching of IGBTs of VSC is reduced with the help of series connected capacitive (C_f) and resistive (R_f) elements at the point of common coupling (PCC). The nonlinear load is represented as uncontrolled bridge rectifier with series R-L branch. The voltages at PCC (v_{sa} and v_{sb}), supply currents (i_{sa}, and i_{sb}), load currents (i_{la}, i_{lb} and i_{lc}) and DC bus voltage (V_{dc}) are sensed and given to the DSP. These signals are processed by DSP to generate appropriate switching pulses for three phase VSC. A hardware prototype of the system is implemented in the laboratory using DSP (dSPACE 1104 R&D controller board). Hall Effect voltage and current sensors are used to sense real time feedback signals. The design of sensor circuitry and various components of DSTATCOM are same as given in section 3.6. Switching pulses generated by DSP are used to derive three phase

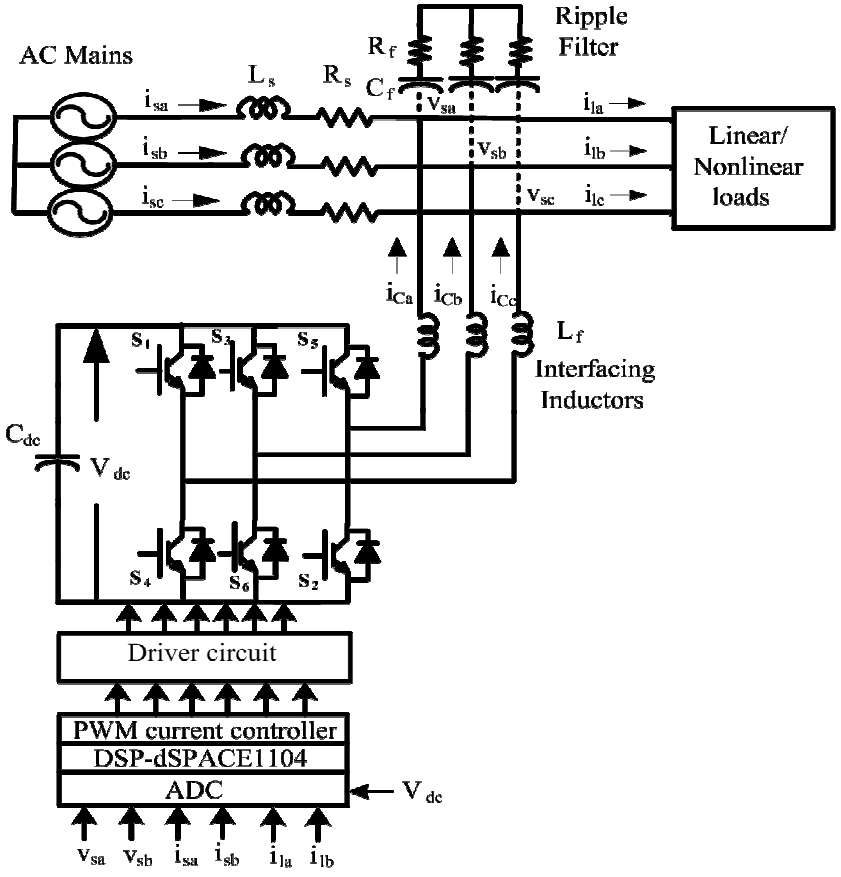


Fig. 6.1 Schematic diagram of the DSTATCOM

VSC, which generates compensator currents (i_{Ca}, i_{Cb} and i_{Cc}).

6.3 BASIC PRINCIPLE AND MATHEMATICAL FORMULATION OF RECURSIVE THEORY BASED CONTROL ALGORITHMS

This section deals with basic principle and mathematical formulation of recursive theory based control algorithms. The control algorithms under this category include variable forgetting factor recursive least square (VFFRLS), recursive inverse (RI) and immune feedback based control algorithms. Detail description of basic principle and mathematical formulation is given as follows.

6.3.1 Variable Forgetting Factor Recursive Least Square Based Control Algorithm [163-169]

The recursive least square method estimates least square (LS) value of the filter coefficients *w(n-1)* at $n\text{-}1^{th}$ iteration, by determining its estimate at the n^{th} iteration using the recently arrived data. To develop the recursive methods of least squares, computation can be started with the known initial conditions and then the old estimates are updated based on the newest information available from the fresh data samples.

This section is divided into three parts. First part presents the estimation of fundamental active power component of load current. Second part formulates the estimation of fundamental reactive power component of load current and using VFFRLS based control algorithm and the derivation of reference supply currents along with switching pulse generation for VSC of DSTATCOM is given in the third part.

6.3.1.1 Estimation of Fundamental Active Power Components of Reference Supply Currents Using VFFRLS Based Control Algorithm

Fig. 6.2 shows the block diagram of control algorithm where voltages (v_{sa}, v_{sb} and v_{sc}) at the PCC are sensed and their amplitude is calculated as given as,

$$V_t = \sqrt{2(v_{sa}^2 + v_{sb}^2 + v_{sc}^2)/3} \tag{6.1}$$

Using PCC voltage magnitude, the unit inphase components are calculated as,

$$u_{pa} = v_{sa}/V_t;\ u_{pb} = v_{sb}/V_t;\ \text{and}\ u_{pc} = v_{sc}/V_t \tag{6.2}$$

The sensed DC bus voltage (V_{dc}) is filtered using a low pass filter (LPF) to suppress ripples. The reference value of DC bus voltage (V_{dc}^*) is compared with the sensed DC bus voltage (V_{dc}) to estimate an error (v_{de}). This error is then passed through a proportional integral (PI) controller which output is used to regulate the voltage at DC bus to its reference value and to meet VSC losses. The output of PI controller at n^{th} sampling instant is given as,

$$w_{pdc}(n) = w_{pdc}(n-1) + k_{pd}\{v_{de}(n) - v_{de}(n-1)\} + k_{id}\{v_{de}(n)\} \tag{6.3}$$

where k_{pd} and k_{id} are the gains of PI controller.

The fundamental active power components (w_{ap}, w_{bp} and w_{cp}) of load currents are estimated by

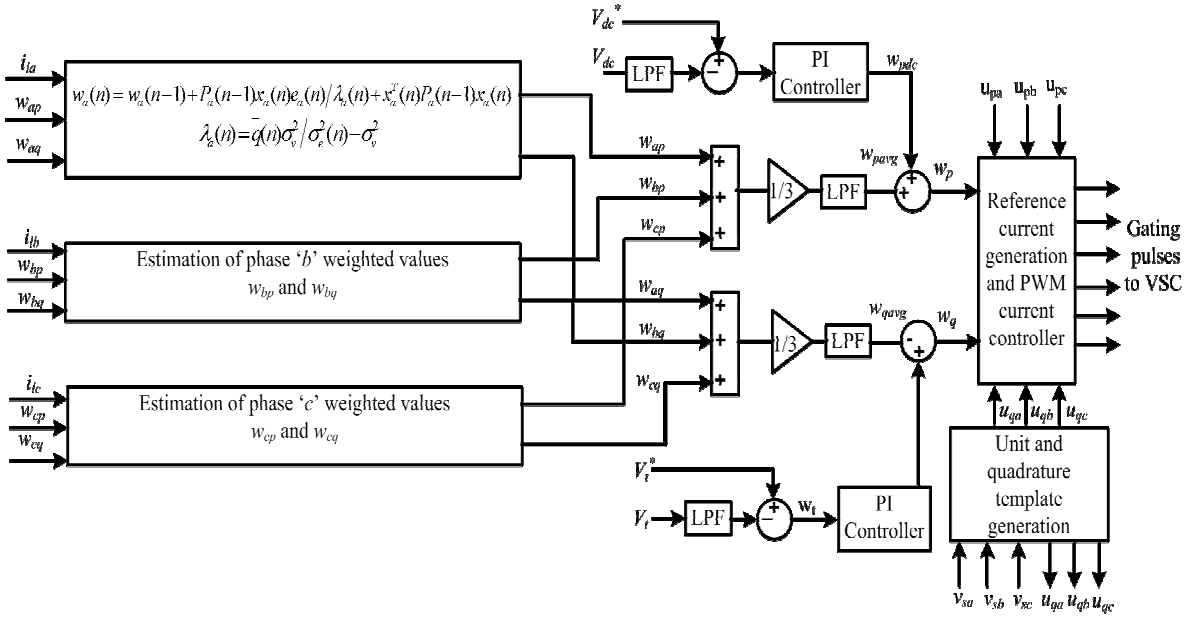


Fig. 6.2 Block diagram of the VFFRLS based control algorithm

VFFRLS based control technique. The recursive least square (RLS) technique is used to minimize a function of error known as cost function *J(n)*, this function is defined at n^{th} sampling instant as,

$$J(n) = \sum_{k=1}^{n} \eta\,(n) e^2(n) \tag{6.4}$$

where $\eta\,(n)$ and *e(n)* denote the weighting factor and error respectively. The error *e(n)* can be expressed as,

$$e(n) = i_{la}(n) - i_{laf}(n) = i_{la}(n) - w^T(n-1)x(n) \tag{6.5}$$

where $i_{la}(n)$ and $i_{laf}(n)$ are the desired and the estimated quantities of load currents, input vector $x(n)=[x(n)\ x(n\text{-}1)\ldots\ldots x(n\text{-}M+1)]^T$ and weight vector $w(n)=[w_1(n)\ w_2(n)\ldots w_M(n)]^T$, where M is the length of the vector *w(n)*.

The weight updation rule for RLS technique is given as,

$$k(n) = \frac{P(n-1)x(n)}{\lambda + x^T(n)P(n-1)x(n)} \tag{6.6}$$

$$w(n) = w(n-1) + k(n)e(n) \tag{6.7}$$

$$P(n) = \frac{1}{\lambda}[P(n-1) - k(n)x^T(n)P(n-1)] \tag{6.8}$$

where *k(n)* and *P(n)* are the vector of Kalman gain and inverse of input correlation matrix.

The factor λ denotes the forgetting factor, which plays an important role in learning of the algorithm. The value of this factor lies between 0 to 1. In fixed forgetting factor RLS method, if λ is closer to 1, the algorithm achieves fast convergence but with reduced tracking capability. The tracking capability of the algorithm may be improved at reduced value of λ, but this also

reduces the speed of convergence. In order to meet this conflicting demand, a variable forgetting factor RLS method is proposed.

Parameter *e(n)* in Eqn. (6.5) is *a priori* error and computed at time '*n-1'*. The *a posteriori* error is given as,

$$\varepsilon(n) = i_{la}(n) - w^T(n)x(n) \tag{6.9}$$

From Eqn. (6.5), Eqn. (6.7) and Eqn. (6.9) *a posteriori* error can be modified as,

$$\varepsilon(n) = e(n)[1 - x^T(n)k(n)] \tag{6.10}$$

The forgetting factor $\lambda(n)$ can be adjusted according given as follows ,

$$E\{\varepsilon(n)e(n)\} = E\{v^2(n)\} \tag{6.11}$$

where $E\{v^2(n)\}=\sigma_v^2$ and this is the power of distortion in system. By using Eqn. (6.6) and Eqn. (6.10) in Eqn. (6.11), it results in,

$$E\{\varepsilon(n)e(n)\} = E\left\{e^2(n)\left[1 - \frac{x^T(n)P(n-1)x(n)}{\lambda(n)+x^T(n)P(n-1)x(n)}\right]\right\} \tag{6.12}$$

The expression for variable forgetting factor $\lambda(n)$ can computed by using Eqn. (6.11) and Eqn. (6.12) as,

$$\lambda(n) = \frac{\bar{q}(n)\sigma_v^2}{\sigma_e^2(n)-\sigma_v^2} \tag{6.13}$$

where $q(n) = x^T(n)P(n-1)x(n)$ and $E\{e^2(n)\} = \sigma_e^2(n)$, $E\{\bullet\}$ is power of the a priori error. The value $\bar{q}(n)$ is given as,

$$\bar{q}(n) = \alpha\bar{q}(n-1) - (1-\alpha)q(n) \tag{6.14}$$

where α is the weighting factor. Here it is supposed that the forgetting factor (FF) is deterministic. The updation of weight vector *w(n)* from Eqn. (6.7), with variable forgetting factor, gives weights (w_{ap}, w_{bp} and w_{cp}) corresponding to fundamental active and reactive power components of load currents.

The average weighted value (w_{pavg}) of weights w_{ap}, w_{bp} and w_{cp} of reference supply current is given as,

$$w_{pavg} = \frac{w_{ap}+w_{bp}+w_{cp}}{3} \tag{6.15}$$

The loss component (w_{pdc}) obtained from the PI controller as given by Eqn. (6.3) is added to the average fundamental active power weight (w_{pavg}) from Eqn. (6.15) to obtain the, reference active power weight as,

$$w_p = w_{pavg} + w_{pdc} \tag{6.16}$$

The reference currents corresponding to fundamental active power are estimated from in-phase unit vectors (u_{pa}, u_{pb} and u_{pc}) and reference active power weight (w_p) as,

$$i_{pa}^* = w_p u_{pa},\ i_{pb}^* = w_p u_{pb} \text{ and } i_{pc}^* = w_p u_{pc} \tag{6.17}$$

where i_{pa}^*, i_{pb}^* and i_{pc}^* are estimated fundamental active reference supply currents.

6.3.1.2 Estimation of Fundamental Reactive Power Components of Reference Supply Currents From VFFRLS Based Control Algorithm

The unit quadrature templates (u_{qa}, u_{qb} and u_{qc}) are computed from unit inphase templates as,

$$u_{qa} = -u_{pb}/\sqrt{3} + u_{pc}/\sqrt{3} \tag{6.18}$$

$$u_{qb} = \sqrt{3}\,u_{pa}/2 + (u_{pb} - u_{pc})/2\sqrt{3} \tag{6.19}$$

$$u_{qc} = -\sqrt{3}\,u_{pa}/2 + (u_{pb} - u_{pc})/2\sqrt{3} \quad (6.20)$$

Another PI controller is used to regulate the PCC voltage to its reference value. The magnitude of PCC voltage (V_t) and selected reference value (V_t^*) are compared and output error (v_{te}) is passed through PI controller. The output of PI controller (w_t) is used to regulate PCC voltage magnitude to its reference value and at the n^{th} sampling instant it is given as,

$$w_t(n) = w_t(n-1) + k_{pq}\{v_{te}(n) - v_{te}(n-1)\} + k_{iq}\{v_{te}(n)\} \quad (6.21)$$

where k_{pq} and k_{iq} are gains for the second PI controller realized for voltage regulation at PCC.

The fundamental reactive power components (w_{aq}, w_{bq} and w_{cq}) of load currents are estimated similarly as given above by VFFRLS based control technique and the average weighted value (w_{qavg}) is calculated as,

$$w_{qavg} = \frac{w_{aq}+w_{bq}+w_{cq}}{3} \quad (6.22)$$

Reference reactive power weight (w_q) is obtained by using output of AC bus PI controller (w_t) and the average reactive weight (w_{qavg}) as,

$$w_q = w_t - w_{lqav} \quad (6.23)$$

The unit quadrature templates (u_{qa}, u_{qb} and u_{qc}) and reference reactive power weight (w_q) are used to estimate the reactive power component of reference supply currents (i_{qa}^*, i_{qb}^* and i_{qc}^*) as,

$$i_{qa}^* = w_q u_{qa},\ i_{qb}^* = w_q u_{qb} \text{ and } i_{qc}^* = w_q u_{qc} \quad (6.24)$$

Thus the reference active and reactive components of reference supply current are estimated and used to generate reference supply currents, which is discussed in next section.

6.3.1.3 Generation of Reference Supply Currents and Switching Pulses

The summation of active (i_{pa}^*, i_{pb}^* and i_{pc}^*) and reactive (i_{qa}^*, i_{qb}^* and i_{qc}^*) components of reference supply currents using Eqn. (6.17) and Eqn. (6.24) gives the total reference supply

currents (i_{sa}^*, i_{sb}^* and i_{sc}^*) as,

$$i_{sa}^* = i_{pa}^* + i_{qa}^*, i_{sb}^* = i_{pb}^* + i_{qb}^* \text{ and } i_{sc}^* = i_{pc}^* + i_{qc}^* \quad (6.25)$$

The sensed supply currents (i_{sa}, i_{sb} and i_{sc}) are compared with these reference supply currents (i_{sa}^*, $i_{sb}^*$and i_{sc}^*) and the current errors (i_{sae}, i_{sbe} and i_{sce}) are generated. These current errors are passed through PWM current controller, which generates switching pulses for three phase VSC used as DSTATCOM.

6.3.2 Recursive Inverse Based Control Algorithm [170-172]

The recursive inverse technique is based on the recursive theory. This algorithm is robust under distorted environment, with considerable reduction in computational complexity, which makes less computation burden in real time implementation. The weighted values of the fundamental active and reactive power component of load currents are extracted and the reference supply currents are generated using this algorithm. The proposed algorithm is used for harmonics elimination, reactive power compensation and load balancing in power factor correction and voltage regulation mode along with regulation of self-sustained DC bus voltage. The implementation of this algorithm is simple and is based on some mathematical operations such as multiplication, division and addition, for error calculation and weight updation. The mathematical formulation of recursive inverse based control algorithm for estimation of fundamental active and reactive power components of reference supply currents and generation of switching pulses for three phase VSC used as DSTATCOM is given as follows.

6.3.2.1 Estimation of Fundamental Active Power Components of Reference Supply Currents From Recursive Inverse Based Control Algorithm

Fig. 6.3 shows the block diagram of recursive inverse based control algorithm, where phase PCC voltages (v_{sa}, v_{sb} and v_{sc}) are sensed and magnitude (V_t) is calculated as,

$$V_t = \sqrt{\frac{2}{3}\left(v_{sa}^2 + v_{sb}^2 + v_{sc}^2 \right)} \tag{6.26}$$

Unit inphase templates are calculated from PCC voltages and their magnitude same as given in section 6.3.1(A). The voltage at DC bus (V_{dc}) of VSC is sensed and compared by reference DC bus voltage (V_{dc}^*), thus the generated error is passed through PI controller. The output (w_{pdc}) of DC bus PI controller is same as given in section 6.3.1.

Fundamental weights (w_{ap}, w_{bp} and w_{cp}) corresponding to active power component of load currents are extracted by recursive inverse technique. The extraction of fundamental active component of phase 'a' of load current (i_{laf}) from distorted value (i_{la}) of same phase is described here for phase 'a' of the load current and other components for phase 'b' and 'c' are computed similarly. The *a priory* error is given as,

$$e(n) = i_{la} - i_{laf} \tag{6.27}$$

The fundamental current component of phase 'a' of load current is estimated from weighted

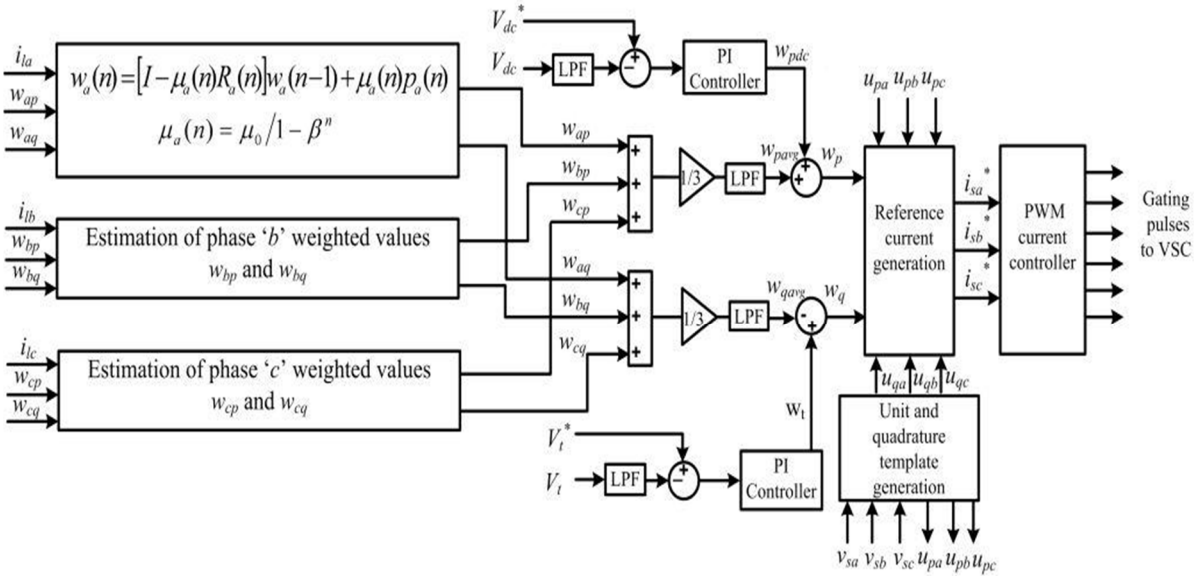


Fig. 6.3 Block diagram of recursive inverse based control algorithm for DSTATCOM

vector and input parameter such as,

$$i_{laf} = x^T(n)w(n-1) \tag{6.28}$$

The value of i_{laf} obtained from Eqn. (6.28) is used in Eqn. (6.27), which gives,

$$e(n) = i_{la} - x^T(n)w(n-1) \tag{6.29}$$

where $x(n)=[x(n), x(n-1),\ldots,x(n-M+1)]^T$ is M×1 vector of input parameters, $w=[w_1, w_2,\ldots, w_{M-1}]$ is M×1 weight vector of the filter and M is order of the adaptive filter.

In the recursive inverse adaptive filtering technique, the weight vector updation rule is given as,

$$w(n) = [I - \mu(n)R(n)]w(n-1) + \mu(n)p(n) \tag{6.30}$$

where $w(n)$ is the weight vector, I is identity matrix of order M×M, $R(n)$ is the autocorrelation vector of input vector of order M×M, $\mu(n)$ is the variable step size and $p(n)$ is the estimate of the cross correlation vector between the desired output signal and input vector of length M. The autocorrelation vector $R(n)$ and cross correlation vector $P(n)$, are given as,

$$R(n) = \beta R(n-1) + \delta(n)x(n)x^T(n) \tag{6.31}$$

$$P(n) = \beta P(n-1) + \delta(n)i_{la}x(n) \tag{6.32}$$

where β is the forgetting factor ($0<\beta<1$) and $\delta(n)$ is nonnegative scalar given as,

$$\delta(n) = \frac{1}{\|x(n)e(n)\|} \tag{6.33}$$

The variable step size $\mu(n)$ gives as,

$$\mu(n) = \frac{\mu_0}{1-\beta^n} \tag{6.34}$$

where $\mu_0 < \mu_{max}$ and $\mu_{\max} = \frac{2(1-\beta)}{\lambda_{\max}(R_{xx})}$, μ_0 is selected to be less than $2/\lambda_{max}$,

$R_{xx}=E[x(n)x^T(n)]$ and the product $\lambda_{max}(R_{xx})$ are the maximum Eigen values of autocorrelation vector R_{xx}.

Based upon the weight updation given in Eqn. (6.30), weighted values ($w_{ap,}$ w_{bp} and w_{cp}) corresponding active power components of load currents are determined. The average weight (w_{pavg}) of fundamental active power weight components of three phase load currents is calculated by mathematical expression as,

$$w_{pavg} = \frac{w_{ap} + w_{bp} + w_{cp}}{3} \tag{6.35}$$

The reference active power weight (w_p) is computed by adding output of DC bus PI controller (w_{pdc}) and average active power weight (w_{pavg}) as,

$$w_p = w_{pavg} + w_{pdc} \tag{6.36}$$

Fundamental active power component of reference supply currents are estimated from unit inphase templates (u_{pa}, u_{pb} and u_{pc}) and reference active power weight (w_p) as,

$$i_{pa}^{*}=w_p u_{pa},\ \ i_{pb}^{*}=w_p u_{pb} \text{ and } i_{pc}^{*}=w_p u_{pc} \tag{6.37}$$

These active power components (i_{pa}^{*}, i_{pb}^{*} and i_{pc}^{*}) of reference supply currents are used to generate total reference supply currents as follow.

6.3.2.2 Estimation of Fundamental Reactive Power Components of Reference Supply Currents From Recursive Inverse Based Control Algorithm

Unit quadrature templates (u_{qa}, u_{qb} and u_{qc}) are calculated from unit inphase templates (u_{pa}, u_{pb} and u_{pc}) same as given in section 6.3.1. The magnitude of PCC voltages are calculated as given in Eqn. (6.26) and compared to reference PCC voltage magnitude (V_t^*). Thus the generated error signal (v_{te}) is passed through PI controller whose output (w_t) is same as given in section 6.3.1.

The weighted values corresponding to fundamental reactive power component of load currents (w_{aq}, w_{bq} and w_{cq}) are extracted from the above discussed recursive inverse based technique and their average weight (w_{qavg}) is calculated by mathematical expression as,

$$w_{qavg} = \frac{w_{aq} + w_{bq} + w_{cq}}{3} \tag{6.38}$$

The magnitude of reference supply reactive power components (w_q) is evaluated by using average reactive power weighted value (w_{qavg}) and output of AC bus PI controller (w_t) as,

$$w_q = w_t - w_{qavg} \tag{6.39}$$

Fundamental reactive power components of reference supply currents are estimated from unit quadrature templates (u_{qa}, u_{qb} and u_{qc}) and reference reactive power weight (w_q) as,

$$i_{qa}^* = w_q u_{qa},\ i_{qb}^* = w_q u_{qb} \text{ and } i_{qc}^* = w_q u_{qc} \tag{6.40}$$

These reactive power components (i_{qa}^*, i_{qb}^* and i_{qc}^*) of reference supply currents are used to generate total reference supply currents as follows.

6.3.2.3 Generation of Reference Supply Currents and Switching Pulses

The summation of active (i_{pa}^*, i_{pb}^* and i_{pc}^*) and reactive (i_{qa}^*, i_{qb}^* and i_{qc}^*) components of

reference supply currents using Eqn. (6.37) and Eqn. (6.40) gives the total reference supply currents (i_{sa}^*, i_{sb}^* and i_{sc}^*) as,

$$i_{sa}^* = i_{pa}^* + i_{qa}^*, i_{sb}^* = i_{pb}^* + i_{qb}^* \text{ and } i_{sc}^* = i_{pc}^* + i_{qc}^* \quad (6.41)$$

The sensed supply currents (i_{sa}, i_{sb} and i_{sc}) are compared with the reference supply currents (i_{sa}^*, i_{sb}^* and i_{sc}^*) given in Eqn. (6.41) and the current errors (i_{sae}, i_{sbe} and i_{sce}) are generated. These current errors are given to PWM current controller, which generates switching pulses for three phase VSC used as DSTATCOM.

6.3.3 Immune Feedback Based Control Algorithm [173-176]

The fundamental active and reactive power weights of load currents are extracted from the immune feedback principle. These weights are used to generate reference supply currents. The proposed control algorithm for DSTATCOM is used to mitigate power quality problems such as harmonics, reactive power and load unbalancing with self-supported DC bus in both unity power factor and voltage regulation modes. Mathematical formulation of immune feedback based control algorithm consists of estimation of fundamental active reference supply currents, estimation of fundamental reactive supply currents and generation of switching pulses for VSC. The detailed mathematical formulation of the control algorithm is given as follows.

6.3.3.1 Estimation of Fundamental Active Power Components of Reference Supply Currents From Immune Feedback Based Control Algorithm

Fig. 6.4 shows block diagram of the immune feedback based control algorithm. The amplitude of PCC voltage is estimated by using three phase voltages (v_{sa}, v_{sb} and v_{sc}) as,

$$V_t = \sqrt{2(v_{sa}^2 + v_{sb}^2 + v_{sc}^2)/3} \quad (6.42)$$

Inphase unit templates of PCC voltages u_{pa}, u_{pb} and u_{pc} are calculated from PCC voltages and PCC voltage magnitude (V_t) same as given in section 6.3.1(A). Voltage at DC bus (V_{dc}) is sensed and compared by reference DC bus voltage (V_{dc}^*), thus the generated error (v_{de}) is passed through PI controller. The output of DC bus PI controller (w_{pdc}) is same as given in section 6.3.1(A).

The fundamental active power weights (w_{ap}, w_{bp} and w_{cp}) components of load current are extracted by immune feedback based control technique. The incremental weight equation based on immune feedback principle at $(n+1)^{th}$ sampling instant is given as,

$$\Delta w(n+1) = \eta[1 - \gamma\{\Delta w(n) - \Delta w(n-1)\}^2]\frac{\delta J(n)}{\delta w(n)} + \alpha\Delta w(n) \tag{6.43}$$

where the parameters η, γ and α are weight learning parameter, stabilization factor and momentum respectively. The cost function is denoted by *J(n)* expressed as,

$$J(n) = \frac{1}{2}e(n)^2 \tag{6.44}$$

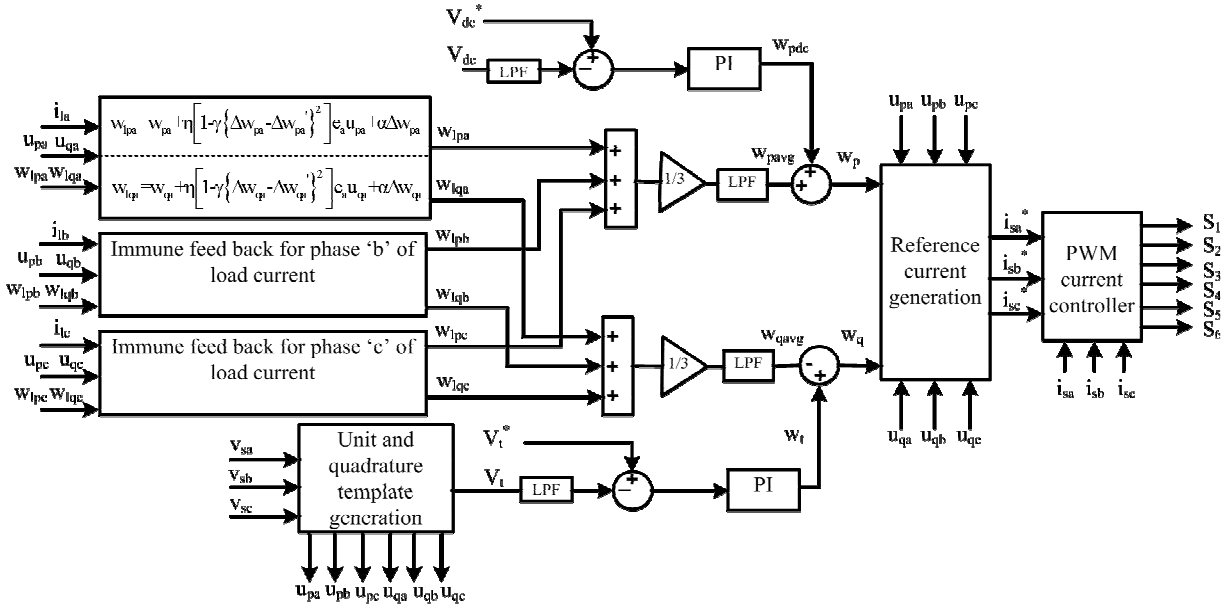


Fig. 6.4 Block diagram of immune feedback based control algorithm for DSTATCOM

where *e(n)* is the error between the sensed value of load current (i_l) and estimated value of load current (i_e), is given as,

$$e(n) = i_l - i_e \tag{6.45}$$

The estimated load current is computed using weight vector w^T=[w_p, w_q…] and input vector *x(n)*=[u_p, u_q…], where w_p, w_q are weighted values of active and reactive power components of load current and u_p, u_q are inphase and quadrature unit templates of PCC voltages. The estimated load current is product of weight vector (*w*) and input vector (*x(n)*) given as,

$$i_e = wx^T(n) \tag{6.46}$$

The weight updation rule for immune feedback at $n+1^{th}$ sampling instant is given as,

$$w(n+1) = w(n) + \Delta w(n+1) \tag{6.47}$$

The Eqn. (6.51) is modified by replacing value of *Δw(n+1)* from Eqn. (6.47) and given at $(n+1)^{th}$ sampling instant as,

$$w(n+1) = w(n) + \eta[1 - \gamma\{\Delta w(n) - \Delta w(n-1)\}^2]\frac{\delta J(n)}{\delta w(n)} + \alpha\Delta w(n) \tag{6.48}$$

where partial differentiation $\frac{\delta J(n)}{\delta w(n)}$, can be simplified in terms of product of estimated error (*e(n)*) and input vector (*x(n)*). The weight updation given in Eqn. (6.48), is modified for weighted values corresponding to active power components (w_{lpa}, w_{lpb} and w_{lpc}) of load currents and are given as follow,

$$w_{lpa} = w_{pa} + \eta\left[1 - \gamma\left\{\Delta w_{pa} - \Delta w_{pa}'\right\}^2\right]e_a u_{pa} + \alpha\Delta w_{pa} \tag{6.49}$$

$$w_{lpb} = w_{pb} + \eta\left[1 - \gamma\left\{\Delta w_{pb} - \Delta w_{pb}'\right\}^2\right]e_b u_{pb} + \alpha\Delta w_{pb} \tag{6.50}$$

$$w_{lpc} = w_{pc} + \eta \left[1 - \gamma\{\Delta w_{pc} - \Delta w_{pc}'\}^2\right] e_c u_{pc} + \alpha \Delta w_{pc} \quad (6.51)$$

The average weighted values corresponding to active (w_{pavg}) power components of load currents is calculated as,

$$w_{pavg} = \frac{w_{lpa}+w_{lpb}+w_{lpc}}{3} \quad (6.52)$$

The reference active power weight is calculated by adding average active power weight (w_{pavg}) and output of DC bus PI controller (w_{pdc}) and is given as,

$$w_p = w_{pavg} + w_{pdc} \quad (6.53)$$

The reference supply currents (i_{pa}^*, i_{pb}^* and i_{pc}^*) corresponding to fundamental active power component of load currents are estimated using inphase unit templates (u_{pa}, u_{pb} and u_{pc}) and reference active power weight (w_p) as,

$$i_{pa}^* = w_p u_{pa},\ i_{pb}^* = w_p u_{pb} \text{ and } i_{pc}^* = w_p u_{pc} \quad (6.54)$$

These fundamental active power components of reference supply currents along with fundamental reactive power components of reference supply currents are used to generate reference supply currents.

6.3.3.2 Estimation of Fundamental Reactive Power Components of Reference Supply Currents From Immune Feedback Based Control Algorithm

Unit quadrature templates (u_{qa}, u_{qb} and u_{qc}) are calculated from unit inphase templates (u_{pa}, u_{pb} and u_{pc}) same as discussed in section 6.3.1. The magnitude of PCC voltages are calculated as given in Eqn. (6.42) and compared to reference PCC voltage magnitude (V_t^*). Thus the generated error signal (v_{te}) is passed through PI controller whose output (w_t) is same as discussed in section 6.3.1.

The weight updation given in Eqn. (6.48), is modified for extraction of weighted values corresponding to reactive power components (w_{lqa}, w_{lqb} and w_{lqc}) of load currents and are given as,

$$w_{lqa} = w_{qa} + \eta \left[1 - \gamma\{\Delta w_{qa} - \Delta w_{qa}'\}^2\right] e_a u_{qa} + \alpha \Delta w_{qa} \tag{6.55}$$

$$w_{lqb} = w_{qb} + \eta \left[1 - \gamma\{\Delta w_{qb} - \Delta w_{qb}'\}^2\right] e_b u_{qb} + \alpha \Delta w_{qb} \tag{6.56}$$

$$w_{lqc} = w_{qc} + \eta \left[1 - \gamma\{\Delta w_{qc} - \Delta w_{qc}'\}^2\right] e_c u_{qc} + \alpha \Delta w_{qc} \tag{6.57}$$

The average weighted values corresponding to reactive (w_{qavg}) power components of load currents is calculated as,

$$w_{qavg} = \frac{w_{lqa} + w_{lqb} + w_{lqc}}{3} \tag{6.58}$$

The reference weight corresponding to reactive power component of load current, w_q is computed by subtracting average reactive power weight (w_{qavg}) from the output of PI controller (w_t) such as,

$$w_q = w_t - w_{qavg} \tag{6.59}$$

The reference supply currents corresponding to the fundamental reactive power component of load currents (i_{qa}^*, i_{qb}^* and i_{qc}^*) are computed from unit quadrature templates (u_{qa}, u_{qb} and u_{qc}) and reference reactive power weight (w_q) as,

$$i_{qa}^* = w_q u_{qa}, i_{qb}^* = w_q u_{qb} \text{ and } i_{qc}^* = w_q u_{qc} \tag{6.60}$$

These fundamental reactive power components of reference supply currents are used to generate reference supply currents.

6.3.3.3 Generation of Reference Supply Currents and Switching Pulses

The fundamental active (i_{pa}^*, i_{pb}^* and i_{pc}^*) and reactive (i_{qa}^*, i_{qb}^* and i_{qc}^*) power components of reference supply currents as given by Eqn. (6.54) and Eqn. (6.60) are used to generate reference supply currents (i_{sa}^*, i_{sb}^* and i_{sc}^*) as,

$$i_{sa}^* = i_{pa}^* + i_{qa}^*, i_{sb}^* = i_{pb}^* + i_{qb}^* \text{ and } i_{sc}^* = i_{pc}^* + i_{qc}^* \quad (6.61)$$

These reference supply currents are compared with sensed supply currents (i_{sa}, i_{sb} and i_{sc}) and current errors are generated. These currents errors are passed through PWM current controller for generation of switching pulsed for three phase VSC.

6.4 MATLAB BASED MODELING OF RECURSIVE THEORY BASED CONTROL ALGORITHMS

This section presents MATLAB based modeling of recursive theory based control algorithms for control of the DSTATCOM. The recursive techniques such as VFFRLS, recursive inverse and immune feedback based control algorithms are developed using MATLAB/SIMULINK for generation of reference supply currents. The detail description of MATLAB based model of the control algorithms is given below.

6.4.1 Modeling and Simulation of VFFRLS Based Control Algorithm

The modeling and simulation of DSTATCOM using VFFRLS based control algorithm are performed in MATLAB environment using SIMULINK and SPS tool box. Fig. 6.5(a) shows the developed model of VFFRLS based control algorithm in SIMULINK for the generation of reference supply currents. The inputs to the control algorithm are PCC voltages (v_s), supply currents (i_{sa}, i_{sb} and i_{sc}), load currents (i_{la}, i_{lb} and i_{lc}) and self-sustained DC bus voltage (V_{dc}). Simulation model for fundamental active and reactive weight extraction corresponding to phase

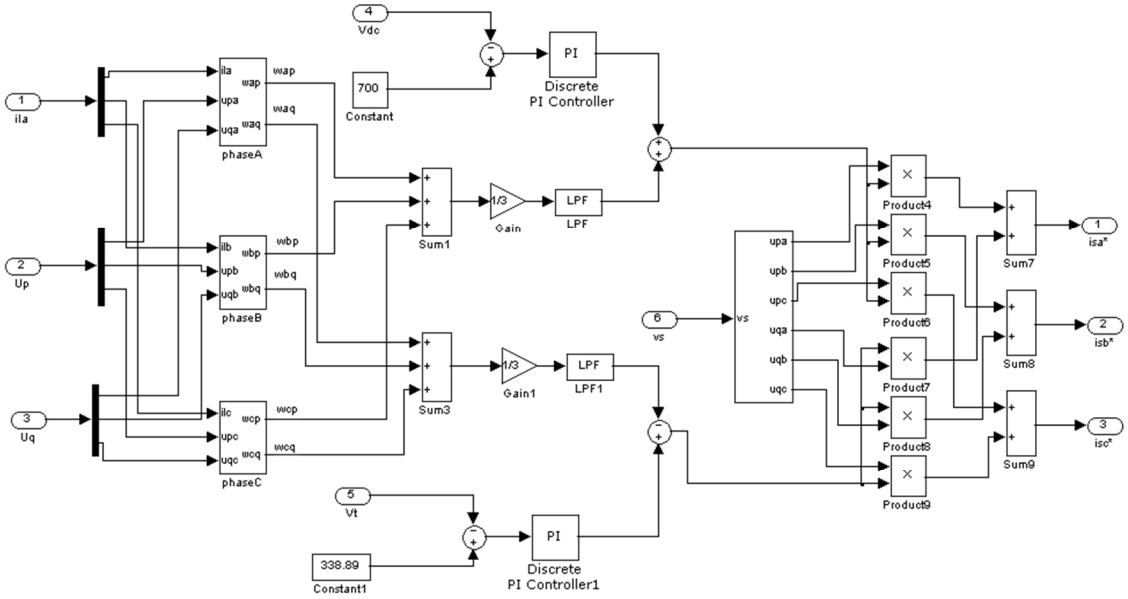


Fig. 6.5(a) Simulink model for generation of reference supply currents using VFFRLS based control algorithm for DSTATCOM

'a' of load current using VFFRLS technique is presented in Fig. 6.5(b).

6.4.2 Modeling and Simulation of Recursive Inverse Based Control Algorithm

The MATLAB/SIMULINK based model of the recursive inverse based control algorithm is developed using SPS tool box. As shown in Fig. 6.6(a), simulation model of the control

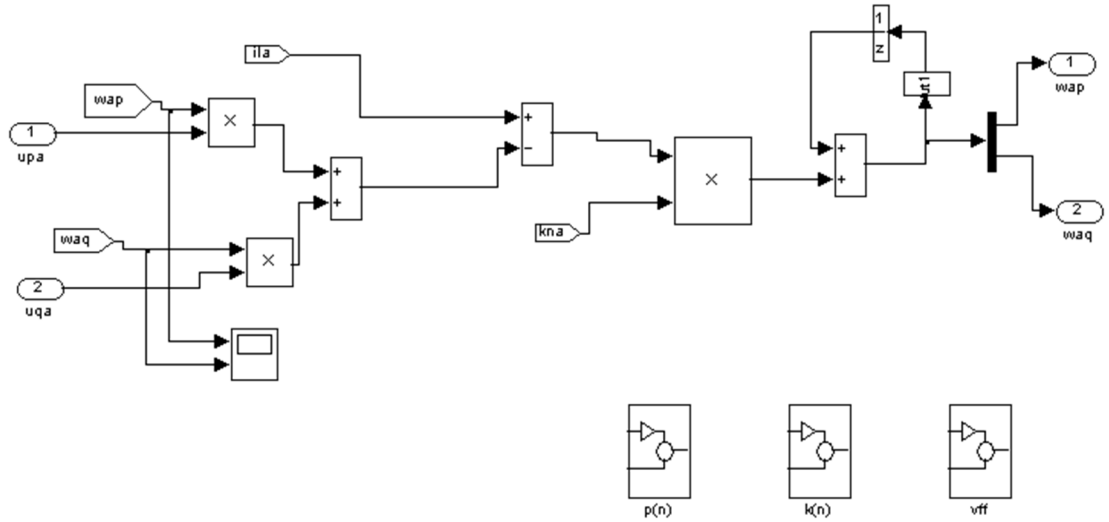


Fig. 6.5(b) Simulink model for extraction of active and reactive weights of load current phase 'a' from VFFRLS based control algorithm

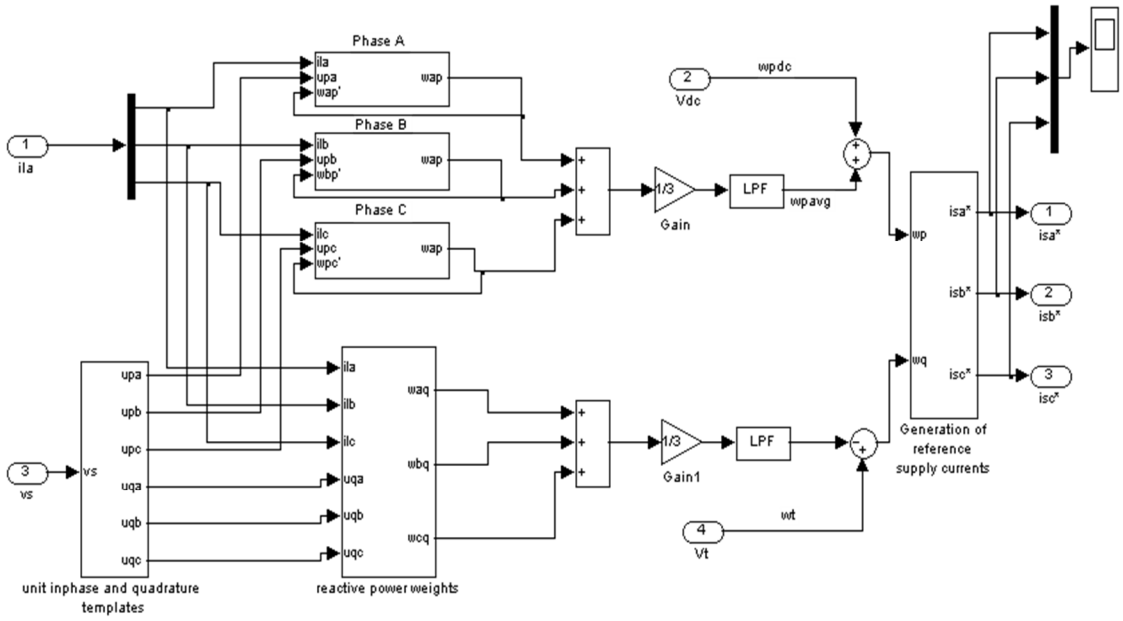


Fig. 6.6(a) Simulink model for generation of reference supply currents using recursive inverse based control algorithm for DSTATCOM

algorithm is used for generation of reference supply currents. The inputs to the control algorithm as shown in SIMULINK model are PCC voltages (v_s), supply currents (i_{sa}, i_{sb} and i_{sc}), load currents (i_{la}, i_{lb} and i_{lc}) and self-sustained DC bus voltage (V_{dc}) used for control of DSTATCOM. Fig. 6.6(b) shows the extraction of fundamental active and reactive power components of load currents form the recursive inverse based control algorithm.

6.4.3 Modeling and Simulation of Immune Feedback Based Control Algorithm

The modeling and simulation of immune feedback based control algorithm for control of DSTATCOM are performed in MATLAB/SIMULINK using SPS tool box. The SIMULINK based model of the control algorithm is presented in Fig. 6.7(a), where input signals to the control algorithms are PCC voltages (v_s), supply currents ($i_{sa,}$ i_{sb} and i_{sc}), load currents (i_{la}, i_{lb} and i_{lc}) and self-sustained DC bus voltage (V_{dc}). Fig. 6.7(b) shows the extraction of fundamental active and reactive weighted value corresponding to phase ‘a’ of load current.

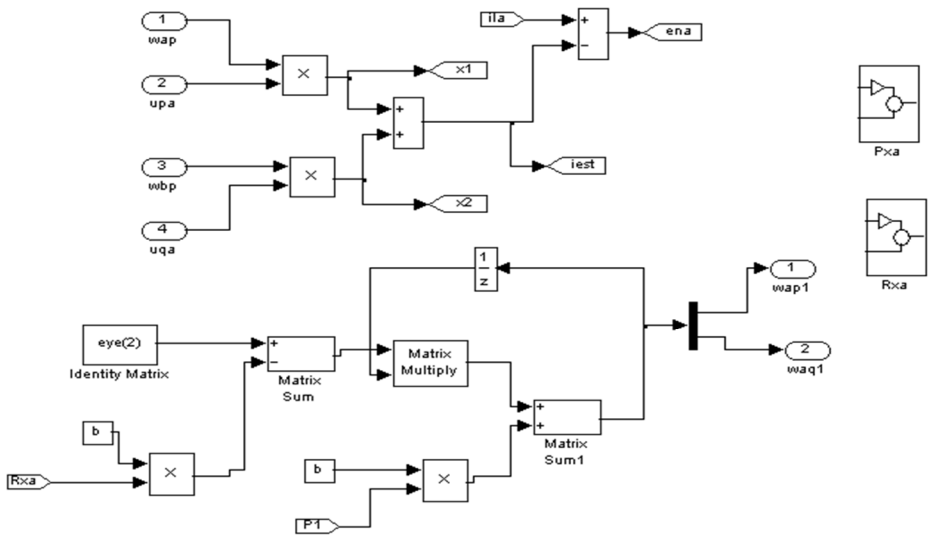


Fig. 6.6(b) Simulink model for extraction of active and reactive weights of load current phase 'a' from recursive inverse based control algorithm

6.5 DSP IMPLEMENTATION OF RESURSIVE THEORY BASED CONTROL ALGORITHMS

This section presents DSP implementation of recursive theory based control algorithms used to generate switching pulses for three phase VSC.

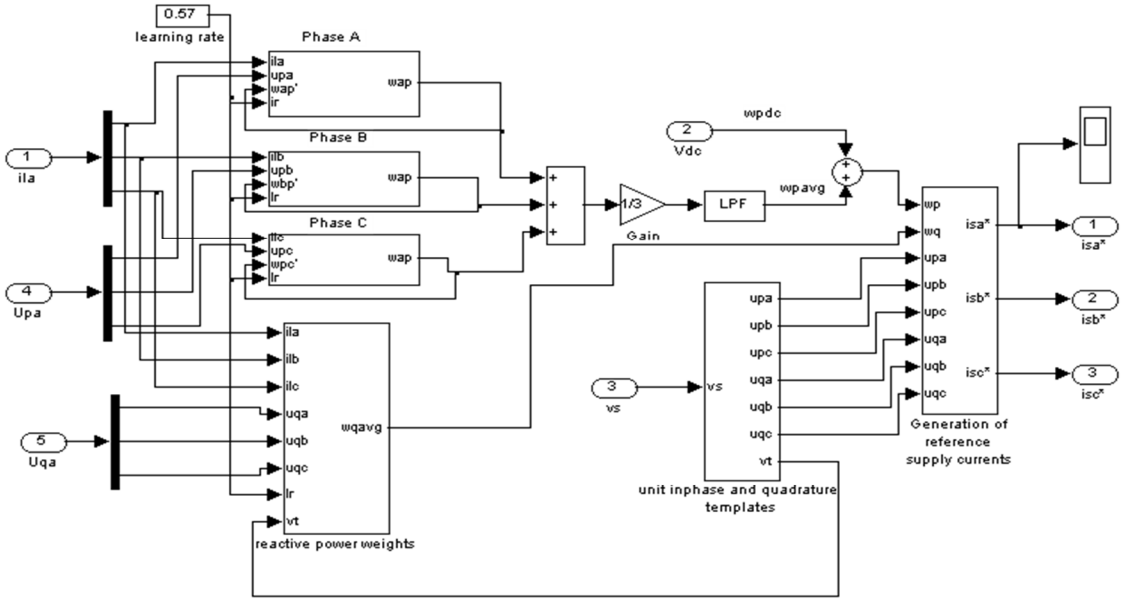


Fig. 6.7(a) Simulink model for generation of reference supply currents using immune feedback based control algorithm for DSTATCOM

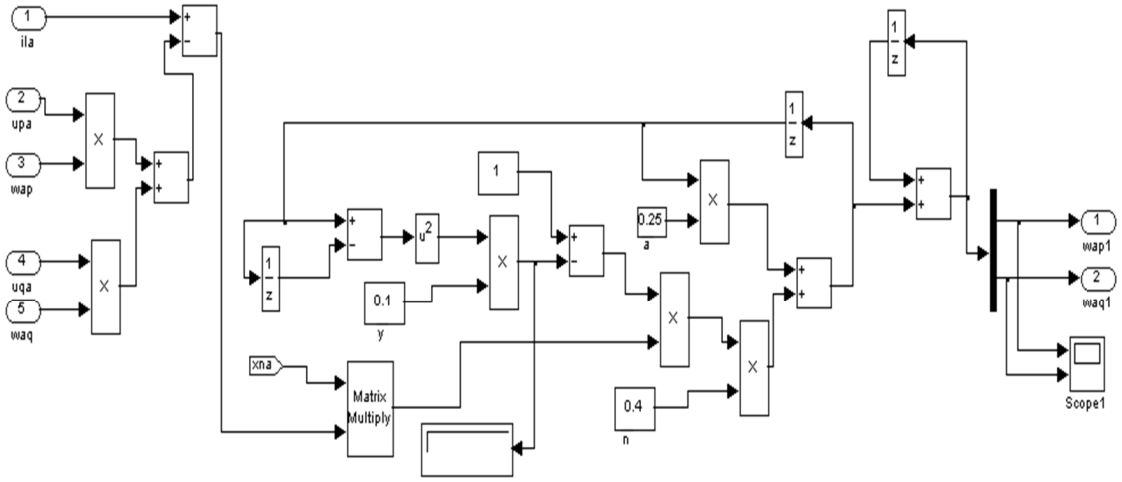


Fig. 6.7(b) Simulink model for extraction of active and reactive weights of load current phase 'a' from immune feedback based control algorithm

6.5.1 VFFRLS Based Control Algorithm

The VFFRLS based control algorithm is implemented using DSP (dSPACE 1104 R&D controller board) and is used to generate gating pulses for the three phase VSC based DSTATCOM. The implementation of DSTATCOM requires real time sensing for signals of PCC voltages, supply currents, load currents and DC bus voltage. These signals are sensed from Hall Effect voltage and current sensors with appropriate buffer circuitry. The design and selection of DC bus capacitance, DC bus voltage, interfacing inductors, sensor circuitry and gating circuitry for hardware implementation of DSTATCOM are same as discussed in section 3.6. The DSP (dSPACE 1104) based implementation of control algorithm for generating switching pulses for DSTATCOM, implementation of controlling circuit for DC bus PI controller and implementation of pulse width modulation (PWM) switching in DSP (dSPACE 1104) using DS 1104SL_DSP_PWM3 block are same as presented in section 4.7.1.The sampling time (T_s) is selected 55μs for VFFRLS based control algorithm. The DC bus PI controller proportional and integral gains are calculated using Ziegler-Nichols unit step response algorithm. The selected value of PI controllers gains are tuned very close to the calculated values.

6.5.2 Recursive Inverse Based Control Algorithm

The recursive inverse based control algorithm for DSTATCOM is implemented using DSP (dSPACE 1104 R&D controller board). Input signals to the controller such as PCC voltages, supply currents, load currents and DC bus voltage are sensed using Hall Effect voltage and current sensors and with the help of appropriate buffer circuitry. The design and selection of DC bus voltage, DC bus capacitance, interfacing inductors, sensor circuitry and gating circuitry is same as discussed in section 3.6. The DSP based implementation of control algorithm for generating switching pulses for DSTATCOM, implementation of DC bus PI controller circuit and implementation of PWM switching in DSP-dSPACE using DS 1104SL_DSP_PWM3 are same as discussed in section 4.7.1. The sampling time (T_s) taken by the DSP is around 50µs for recursive inverse based control algorithm.

6.5.3 Immune Feedback Based Control Algorithm

The immune feedback based control algorithm is implemented using DSP (dSPACE 1104) for real time control of the DSTATCOM. The inputs to the controller are PCC voltage, supply currents, load currents and DC bus voltage are sensed using Hall Effect voltage and current sensors. Design and selection of DC bus voltage, DC bus capacitance, interfacing inductor, sensor circuitry and gating circuit are same as discussed in section 3.6. These sensed signals are provided to the controller through ADC channels and processed through slave DSP subsystem based on the TMS320F240 DSP microcontroller. The DSP-dSPACE based implementation of control algorithm for generating switching pulses for DSTATCOM, implementation of controlling circuit for DC bus PI controller and Implementation of pulse width modulation (PWM) switching in DSP-dSPACE using DS 1104SL_DSP_PWM3 block are the same as

presented in section 4.7.1. Sampling time (T_s) taken by the immune feedback based control algorithm is around 45µs.

6.6 RESULTS AND DISCUSSION

The performance of recursive theory based control algorithms with simulation and experimental test results are illustrated here. Simulation results are obtained using SIMULINK and SPS tool-box. Test results are recorded using a power quality analyzer (Fluke 43B) and four channel digital oscilloscope (Agilent DSO-X 2014A) on the developed prototype of DSTATCOM.

6.6.1 Performance of DSTATCOM With VFFRLS Based Control Algorithm

The performance of DSTATCOM for mitigation of power quality problems such as harmonics reduction, reactive power compensation and load balancing is achieved in PFC and voltage regulation modes under nonlinear loads. Simulation results are studied for both PFC and voltage regulation modes, whereas experimental test results are recorded for PFC mode under nonlinear load. Simulation and experimental results for variable forgetting factor recursive least square (VFFRLS) based control algorithms are discussed as follow.

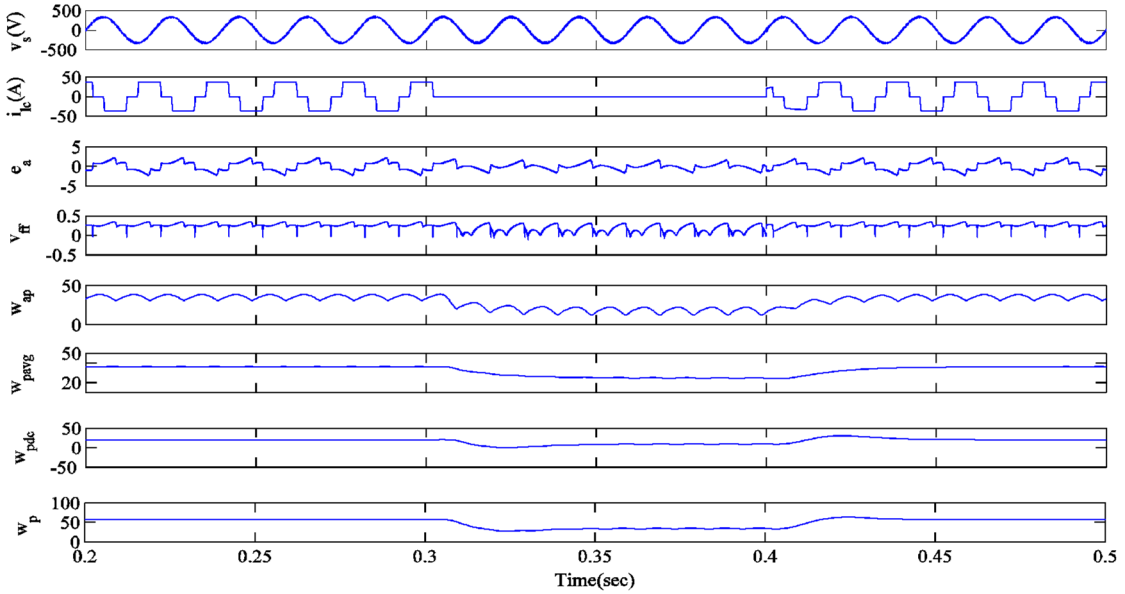
6.6.1.1 Simulated Performance of DSTATCOM in PFC and Voltage Regulation Modes

Simulated performance of DSTATCOM with VFFRLS based control algorithm is presented here. This is divided into three parts. First part discusses the performance and intermediate signals of control algorithm, second and third parts discuss the performance of DSTATCOM in PFC mode and voltage regulation mode respectively.

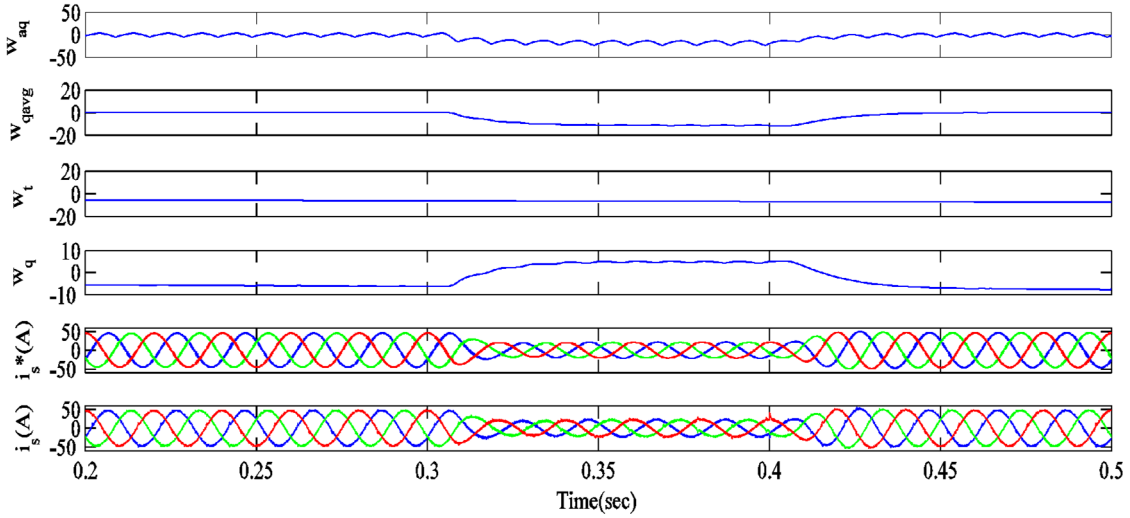
A. Performance of System With VFFRLS Based Control Algorithm in Voltage Regulation Mode Under Nonlinear Load

Figs. 6.8(a) and (b) show the performance and intermediate signals with VFFRLS based control algorithm for control of DSTATCOM in voltage regulation mode. Fig. 6.8(a) shows the

waveforms of PCC phase ‘a’ of voltage (v_{sa}), phase ‘c’ of load current (i_{lc}), error between phase ‘a’ of sensed load current and its estimated quantity (e_a), variation of variable forgetting factor (v_{ff}), active power weight corresponding to phase ‘a’ of load current (w_{ap}), average active power weight (w_{pavg}), output of DC bus PI controller (w_{pdc}) and reference reactive power weight (w_p), which includes average active power weight and output of DC bus PI controller. These results are taken for steady state (before t=0.3s) and unbalanced load conditions (t=0.3s to t=0.4s).



(a)



(b)

Fig. 6.8 Performance and intermediate signals of VFFRLS based control algorithm in voltage regulation mode

Unbalancing in load is created when phase 'c' of load is switched off.

Fig. 6.8(b) shows waveforms of reactive power weight (w_{bq}) corresponding to phase 'b' of load current, average reactive power weight (w_{qavg}), output of AC bus PI controller (w_t), reference reactive power weight (w_q), estimated reference supply currents (i_s^*) and sensed supply currents (i_s). It is observed from these results that control algorithm achieves mitigation of several power quality problems for which it has been designed and performs satisfactory in steady state and unbalanced load conditions.

B. Performance of DSTATCOM in PFC Mode Under Nonlinear Load

Fig. 6.9 shows the dynamic performance of DSTATCOM controlled in PFC mode under nonlinear load. The waveforms of PCC voltages (v_s), supply currents (i_s), load currents (i_{la}, i_{lb} and

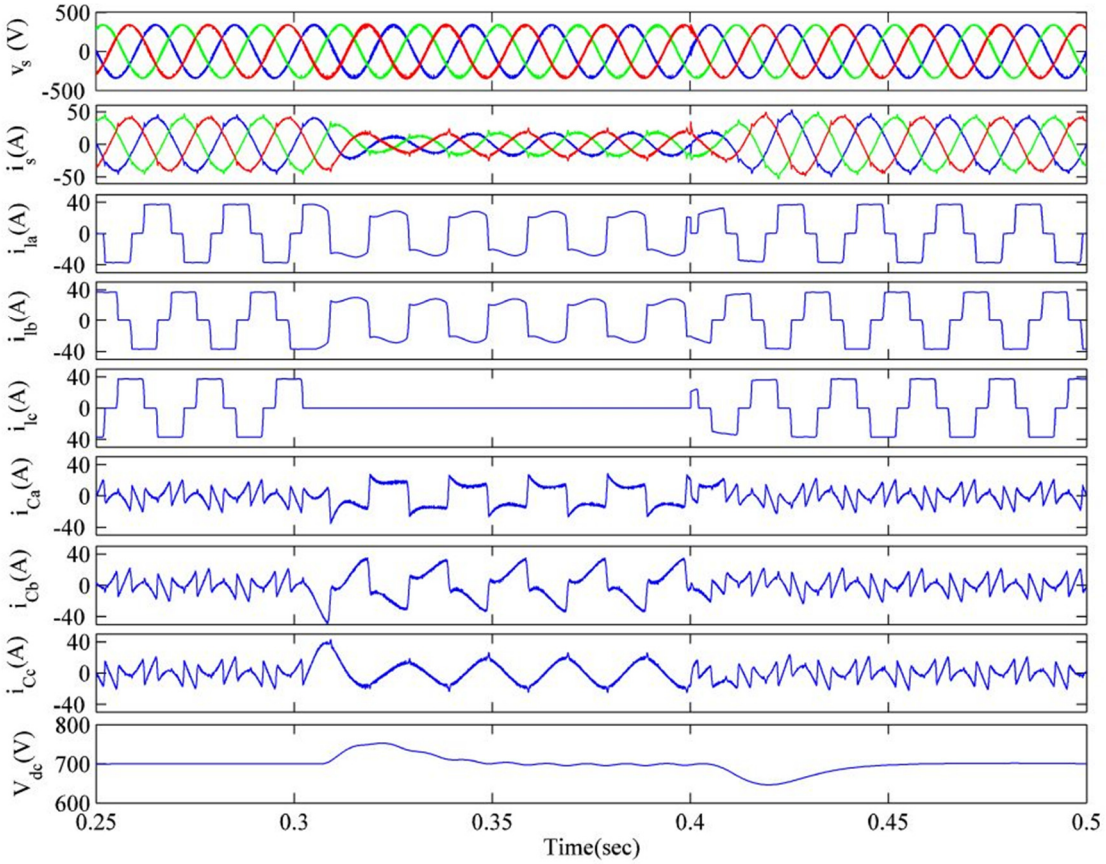


Fig. 6.9 Performance of shunt compensator in PFC mode under varying nonlinear load

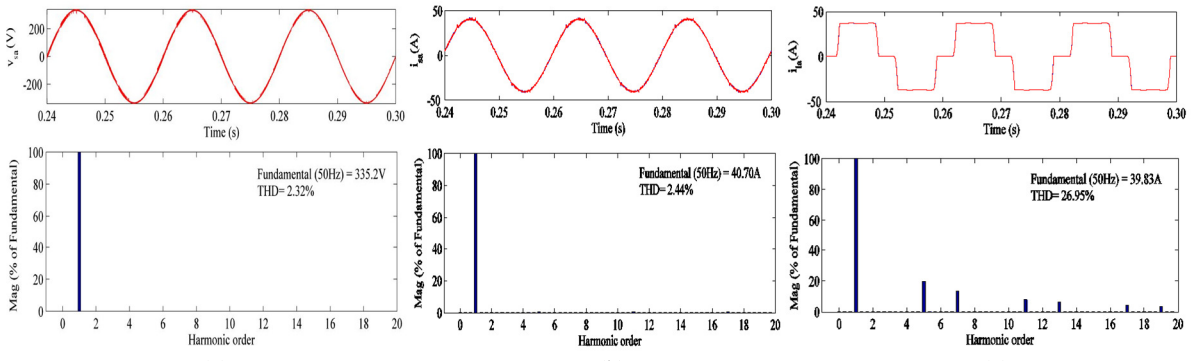
i_{lc}), compensator currents (i_{Ca}, i_{Cb} and i_{Cc}) and voltage of self-sustained DC bus (V_{dc}) are shown in this figure. It can be observed from Fig. 6.9 that under steady state condition upto t=0.3s, the supply currents are balanced and sinusoidal and the DC bus voltage is regulated at its reference value of 700V. Unbalancing in the load is created by switching off phase 'c' of load, during the time interval t=0.3s to t=0.4s. It can be observed that the supply currents are still balanced and sinusoidal with reduced magnitude during load unbalancing.

Fig. 6.10 shows the harmonic spectra of phase 'a' of PCC voltage (v_{sa}), supply current (i_{sa}) and load current (i_{la}) in unity power factor mode under nonlinear load. Total harmonic distortions (THDs) of v_{sa}, i_{sa} and i_{la} are 2.32%, 2.44% and 26.95% respectively. It can be observed from these results that a 2.44% THD in supply current is achieved when the THD in load current is 26.95%. The THD values of v_{sa} and i_{sa} are within the limit of IEEE-519 standard.

The shunt compensator provide satisfactory performance in maintaining the sinusoidal balanced supply currents, regulating the DC bus voltage and reduces harmonics in unity power factor correction mode under steady state and dynamic load conditions.

C. Performance of DSTATCOM in Voltage Regulation Mode Under Nonlinear Load

Fig. 6.11 depicts the performance of a shunt compensator in voltage regulation mode at PCC.



(a) (b) (c)

Fig. 6.10 Harmonic spectra of (a) PCC voltage, v_{sa} (b) Supply current, i_{sa} (c) load current, i_{la} in PFC mode

This shows the waveforms of PCC voltages (v_s), supply currents (i_s), load currents (i_{la}, i_{lb} and i_{lc}), compensator currents (i_{Ca}, i_{Cb} and i_{Cc}), voltage of self-sustained DC bus (V_{dc}) and PCC voltage amplitude (V_t). It can be observed from these results that under steady state condition upto t=0.3s, supply currents are balanced, sinusoidal and the voltage at DC bus is regulated to its reference value 700V and PCC voltage magnitude is regulated to its reference value of 338.8 V. Dynamic load changes are introduced by switching off phase '*c*' of load from t=0.3s to t=0.4s. The DC bus and PCC voltage PI controllers are able to regulate DC bus voltage and magnitude of PCC voltage to their reference values. Supply currents in all the three phases are balanced and

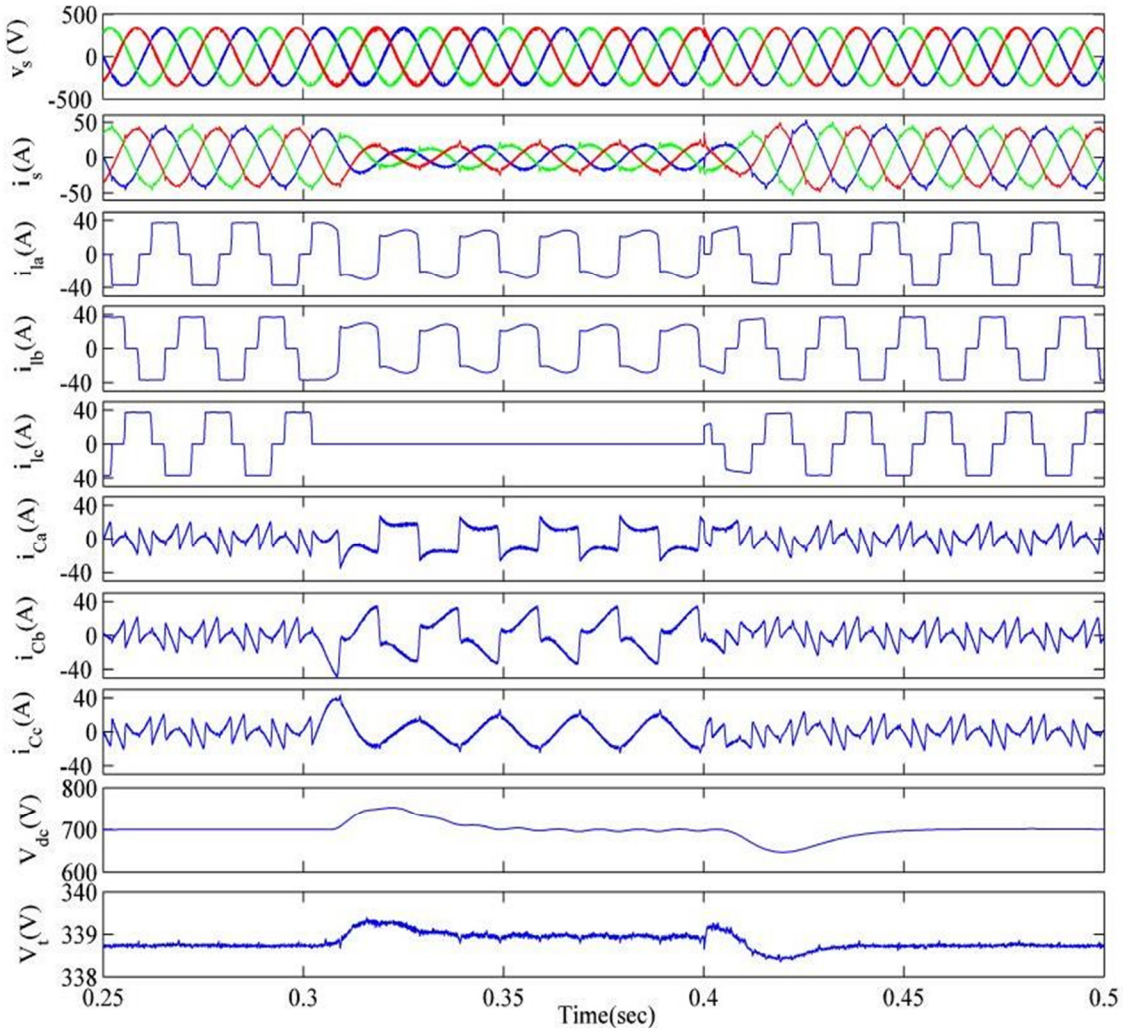


Fig. 6.11 Performance of shunt compensator in voltage regulation mode under varying nonlinear load

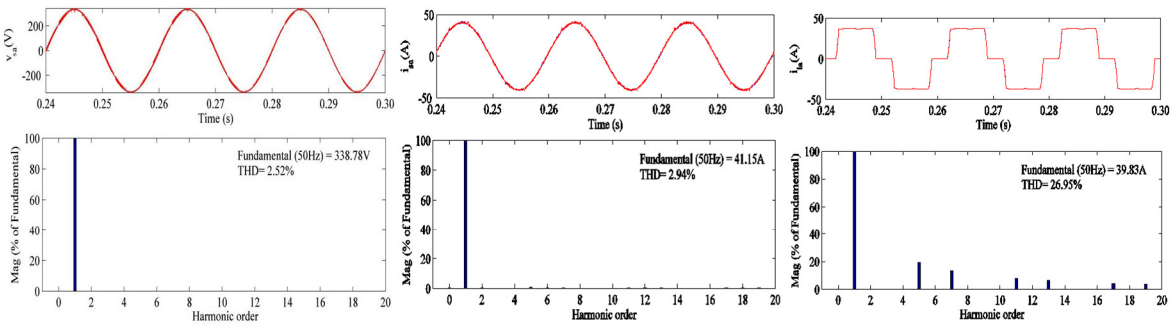
sinusoidal even though the load currents are distorted and unbalanced which are mitigated by DSTATCOM.

Fig. 6.12 shows the harmonic spectra of phase '*a*' of PCC voltage (v_{sa}), supply current (i_{sa}) and load current (i_{la}) in voltage regulation mode under nonlinear load. The total harmonic distortions (THDs) of v_{sa}, i_{sa} and i_{la} are 2.52%, 2.94% and 26.95% respectively. It is observed form these figures that 2.94% THD in supply current is achieved when THD in load current is 26.95%. The THD values of v_{sa} and i_{sa} are within permitted limit specified in IEEE-519 standard. The performance of DSTATCOM is found satisfactory in balancing supply currents, DC bus voltage regulation, PCC voltage magnitude regulation and harmonics reduction.

6.6.1.2 Experimental Performance of DSTATCOM in PFC and Voltage Regulation Modes

The real time performance of DSTATCOM with VFFRLS based control algorithm is studied on the developed experimental prototype of DSTATCOM here. This is divided into three parts. First part presents the test results for system performance and intermediate signals of control algorithm. Second part presents the steady state performance of the DSTATCOM and dynamic performance of DSTATCOM is discussed in the third part.

A. Performance of VFFRLS Based Control Algorithm Under Nonlinear Load



(a) (b) (c)

Fig. 6.12 Harmonic spectra of (a) PCC voltage, v_{sa} (b) Supply current, i_{sa} (c) load current, i_{la} in voltage regulation mode

Fig. 6.13 shows the dynamic performance and intermediate signals of VFFRLS based control algorithm. These results are recorded under dynamic load changes when phase 'c' of the load is switched off. Fig. 6.13(a) shows waveform of phase 'a' of PCC voltage, filtered PCC voltage (v_{saf}), load current (i_{la}) and variable forgetting factor (μ). Fig.6.13(b) shows waveform of weight corresponding to active power component of phase 'a' of load current (w_{ap}), average active power weight (w_{pavg}), output of DC bus PI controller (w_{pdc}) and reference active power weight (w_p), which include average active power weight and DC bus PI controller output. Fig. 6.13(c) presents waveform of weight corresponding to fundamental reactive power component of phase 'a' of load current (w_{aq}), average reactive power weight (w_{qavg}), output of AC bus PI controller (w_t) and reference reactive power weight (w_q). Fig. 6.13 (d) shows waveforms of reference

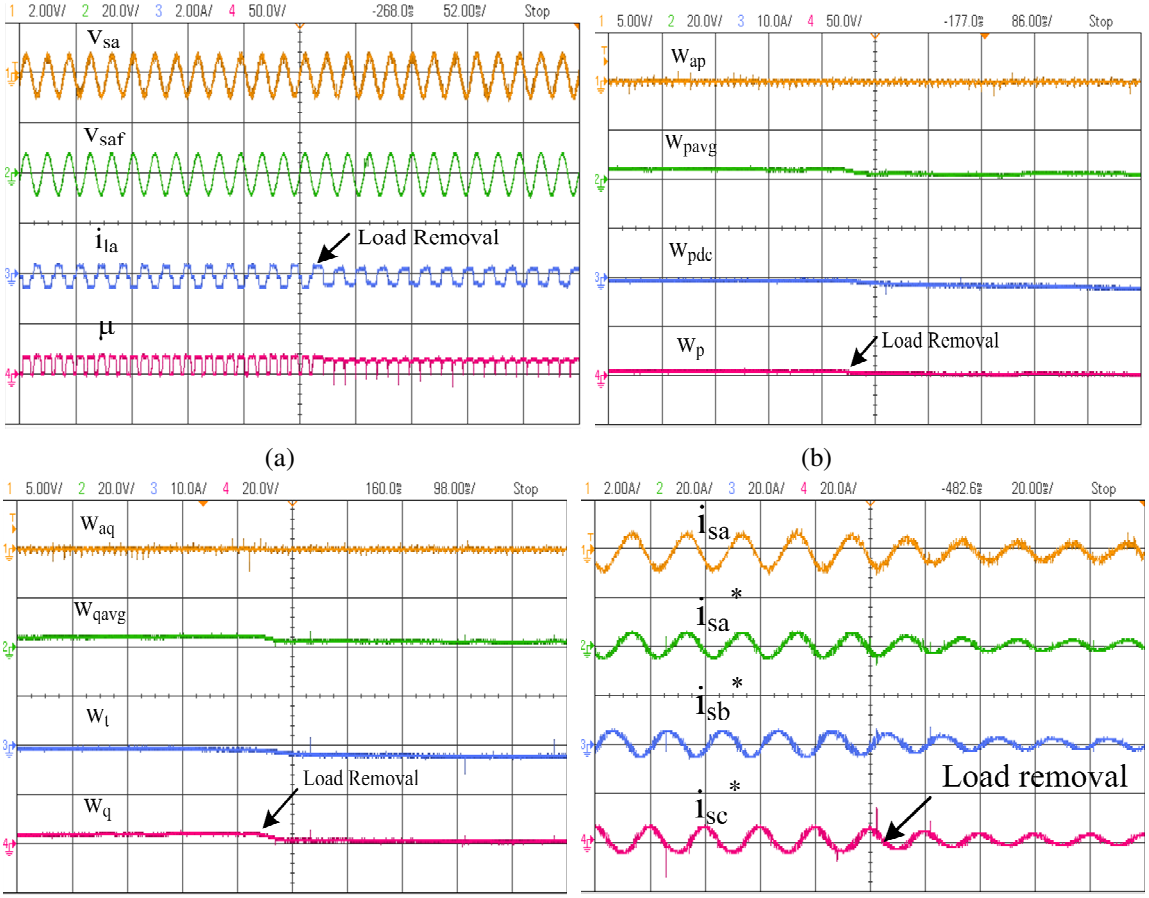


Fig. 6.13 Intermediate signals of VFFRLS control algorithm for DSTATCOM under nonlinear load

supply currents (i_{sa}^*, i_{sb}^* and i_{sc}^*) along with phase 'a' of actual supply current. These results show satisfactory performance of the system with shunt compensator under dynamic load change conditions.

B. *Steady State Performance of DSTATCOM Using VFFRLS Based Algorithm Under Nonlinear and Linear Loads*

The performance of DSTATCOM controlled using VFFRLS is shown in Fig. 6.14 at steady state condition. Figs. 6.14(a)-(c) depict phase '*a*' of supply current (i_{sa}), load current (i_{la}) and compensator current (i_{Ca}) along with PCC voltage (v_{sa}). Figs. 6.14(d)-(f) show the harmonic spectra of supply current (i_{sa}), load current (i_{la}) and PCC voltage (v_{ab}). The total harmonic distortion (THD) in i_{sa}, i_{la} and v_{ab} are observed to be 3.3%, 20.2% and 2.1% respectively. It can be observed from these figures that THD in supply current is reduced to 3.3% whereas load current has a THD of 20.2%. Fig. 6.15 shows the simulated performance of the DSTATCOM using VFFRLS based control algorithm at same voltage rating for which experimental system is developed. This shows the waveforms of PCC voltages (v_s), supply currents (i_s), load currents

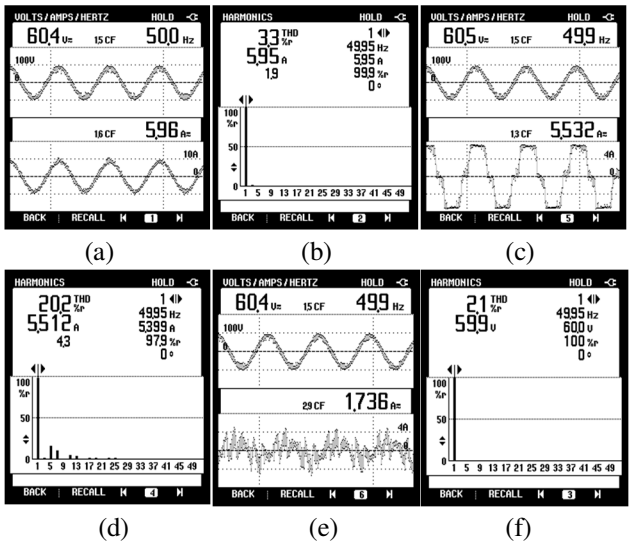


Fig. 6.14 Steady state performance of DSTATCOM under nonlinear load (a), (c) and (e) i_{sa}, i_{la} and i_{Ca} with v_{sa} (b), (d) and (f) harmonic spectra of i_{sa}, i_{la} and v_{sa}

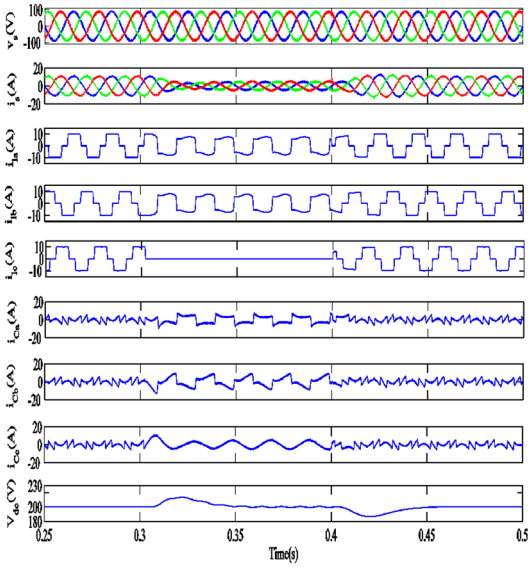


Fig. 6.15 Performance of DSTATCOM under nonlinear load in PFC mode

(i_{la}, i_{lb} and i_{lc}), compensator current (i_{Ca}, i_{Cb} and i_{Cc}) and self-sustained DC bus voltage (V_{dc}). The supply currents are balanced and sinusoidal and DC bus voltage is regulated at the reference voltage of 200V during steady state (before t=0.3s) and unbalanced load condition (t=0.3s to t=0.4s).

Fig. 6.16 shows steady state performance of the DSTATCOM under linear lagging PF load in PFC mode using VFFRLS based control algorithm. Figs. 6.16(a)-(c) show waveforms of phase 'a' of supply current (i_{sa}), load current (i_{la}) and compensator current (i_{Ca}) along with PCC voltage (v_{sa}). Figs. 6.16(d)-(f) show waveforms of supply power (P_s), load power (P_l) and compensator power (P_C). The values of supply and load apparent powers are 0.260 and 0.286kVA respectively. The power factor on supply side is improved (close to 1 DPF) as the reactive power demand of the load is compensated by DSTATCOM. Fig. 6.17 shows simulated performance of the DSTATCOM under linear load in PFC mode at the same rating for which experimental system is developed. The waveforms of PCC voltages (v_s), supply currents (i_s), load currents (i_{la}, i_{lb} and i_{lc}), compensator current (i_{Ca}, i_{Cb} and i_{Cc}) and self-sustained DC bus voltage (V_{dc}) are

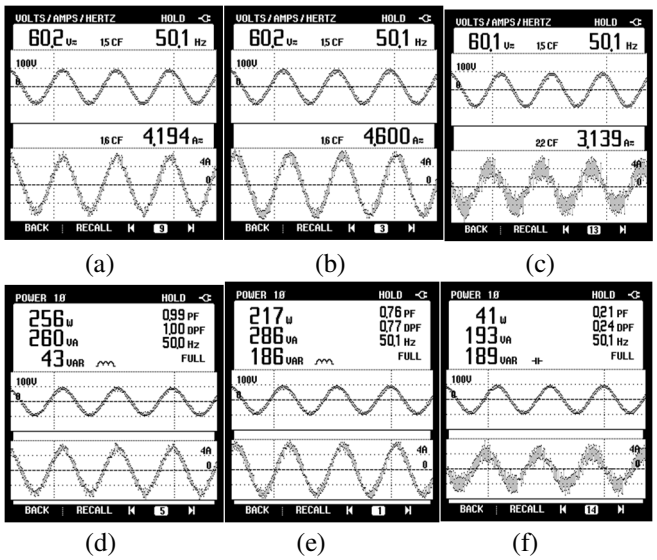


Fig. 6.16 Steady state performance of DSTATCOM under linear load (a), (b) and (c) i_{sa}, i_{la} and i_{Ca} with v_{sa} (d), (e) and (f) P_s, P_l and P_C

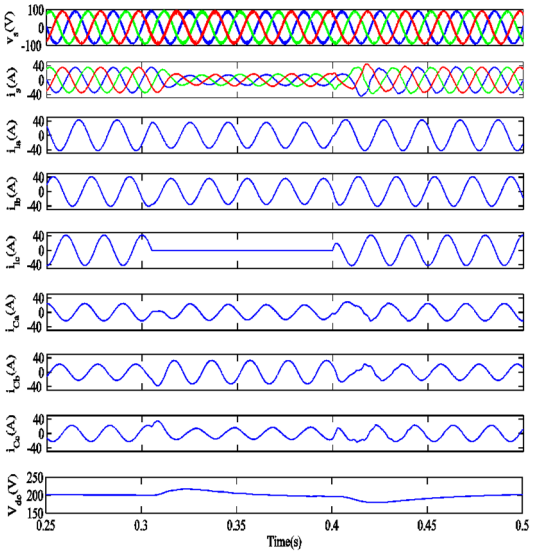


Fig. 6.17 Performance of DSTATCOM in PFC mode under linear load

presented in these results. It is observed from the results that supply currents are maintained balanced and sinusoidal in steady state and unbalance load conditions.

C. Dynamic Performance of DSTATCOM With VFFRLS Based Control Algorithm

Test results for dynamic performance of DSTATCOM are shown in Fig. 6.18. Figs. 6.18(a)-(c) show the supply currents (i_{sa}, i_{sb} and i_{sc}), load currents (i_{la}, i_{lb} and i_{lc}) and compensator currents (i_{Ca}, i_{Cb} and i_{Cc}) respectively along with PCC voltage (v_{sa}). Fig. 6.18(d) depicts the waveforms of DC bus voltage (V_{dc}), phase '*c*' of load current (i_{lc}), supply current (i_{sc}) and compensator current (i_{Cc}). It is observed from the test results that the supply currents are balanced and sinusoidal and the DC bus voltage is regulated to its reference value under varying load conditions when DSTATCOM is controlled using VFFRLS algorithm.

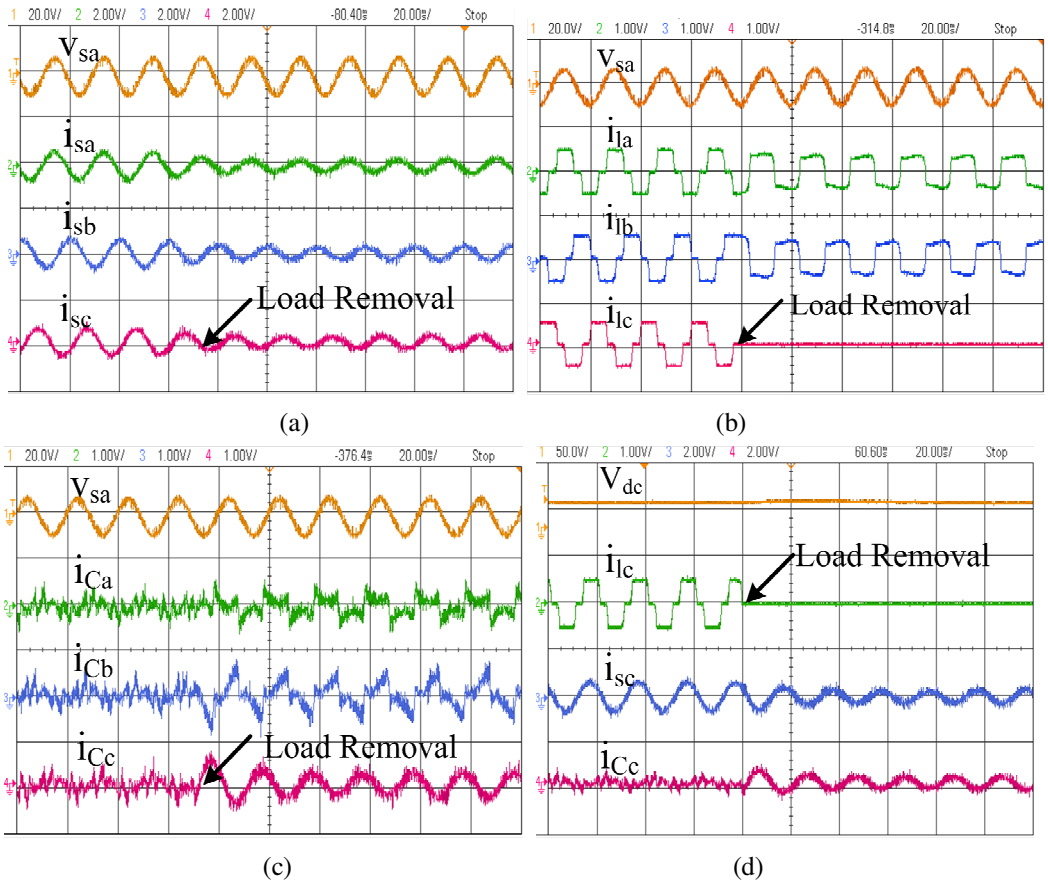


Fig. 6.18 Dynamic performance of DSTATCOM using VFFRLS base control algorithm under nonlinear load

D. Steady State Performance of DSTATCOM in Voltage Regulation Mode

Fig. 5.19 shows steady state performance of DSTATCOM in voltage regulation mode. Figs. 5.19(a), (c) and (e) present waveforms of phase 'a' of supply current (i_{sa}), load current (i_{la}) and compensator current (i_{Ca}) along with PCC voltage (v_{sa}). Figs. 5.20(b), (d) and (f) show harmonic spectra of phase 'a' of supply current, load current and PCC voltage. The THDs of 4.6%, 20.5% and 3.9% in supply current, load current and PCC voltage are presented by these results. Figs. 5.19 (g), (h) and (i) show reactive powers in supply (Q_s), load (Q_l) and compensator (Q_C). It is observed from this result that reactive powers in supply and load are 0.16kVAR and 0.106kVAR respectively.

Fig. 6.20 shows simulated performance of DSTATCOM using VFFRLS based control algorithm

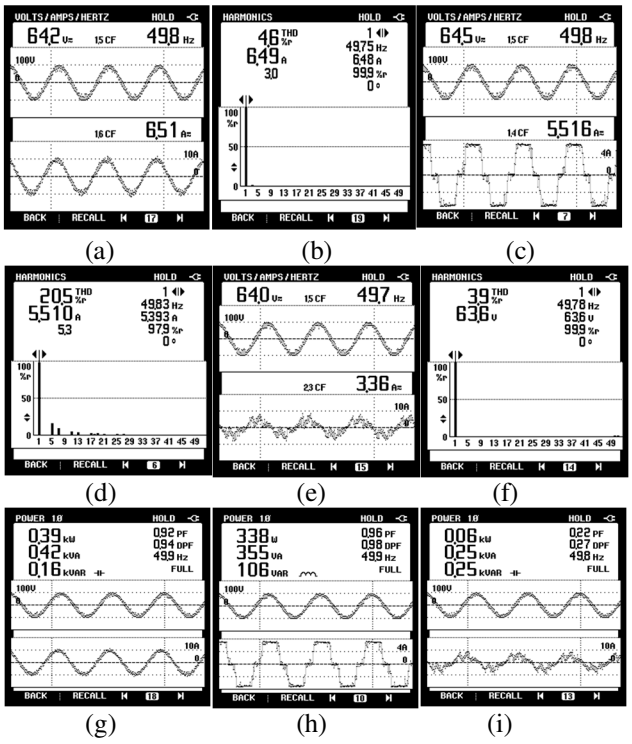


Fig. 6.19 Steady state performance of DSTATCOM under nonlinear load in voltage regulation mode(a),(c) and (e) i_{sa}, i_{la} and i_{Ca} along with v_{sa} (b),(d) and (f) harmonic spectra of i_{sa}, i_{la} and v_{sa} (g),(h) and (i) Q_s, Q_l and Q_C

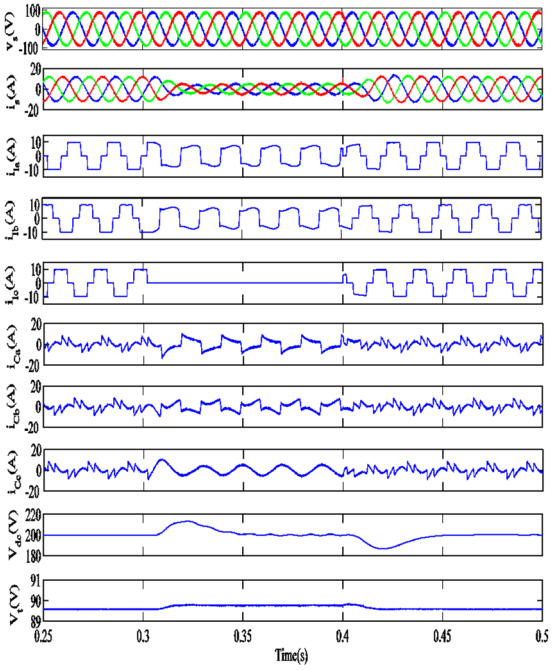
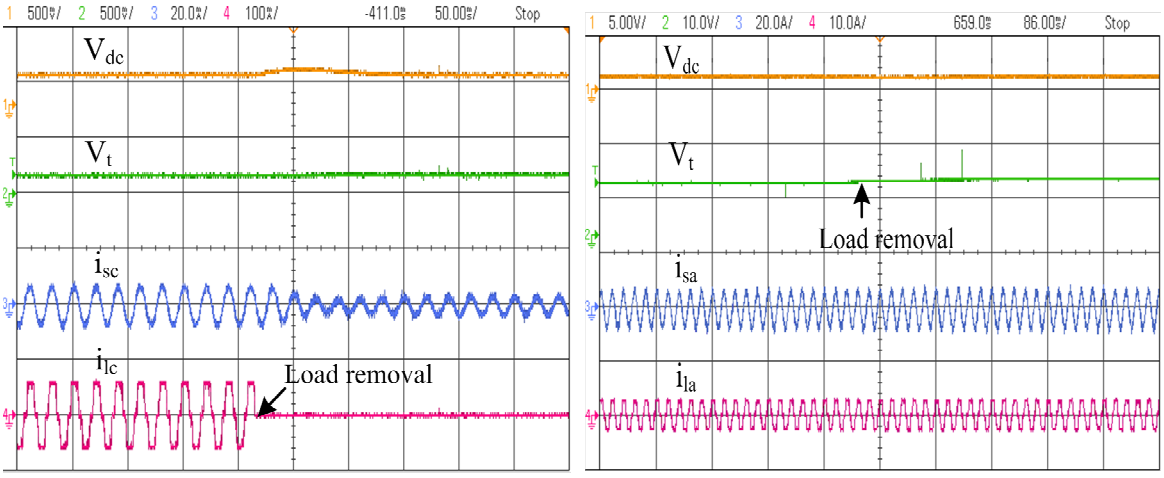


Fig. 6.20 Performance of DSTATCOM under nonlinear load in voltage regulation mode

in voltage regulation mode at the same voltage rating for which experimental prototype is developed. This result presents waveforms of PCC voltages (v_s), supply currents (i_s), load currents (i_{la}, i_{lb} and i_{lc}), compensator current (i_{Ca}, i_{Cb} and i_{Cc}), self-sustained DC bus voltage (V_{dc}) and amplitude of PCC voltage (V_t). It is observed from this result that DC bus voltage and amplitude of PCC voltage are regulated at their reference values in steady state (before t=0.3s) and unbalance load condition (t=0.3 t0 t=0.4s) respectively.

E. Dynamic Performance of DSTATCOM in Voltage Regulation Mode

Fig. 6.21 shows dynamic performance of DSTATCOM in voltage regulation mode under nonlinear load. Fig. 6.21 (a) shows waveform of DC bus voltage (V_{dc}), PCC voltage magnitude (V_t), phase 'c' of supply current (i_{lc}) and phase 'c' of load current (i_{lc}). These results are shown for steady state and unbalanced load conditions. It is observed from this result that supply current is balanced and sinusoidal along with regulated DC bus voltage in steady state and unbalanced load conditions. Similar waveforms are shown in Fig. 6.21(b), to shows the effect of PCC voltage regulation. These results show the boosting of PCC voltage magnitude, which is boosted



(a) (b)

Fig. 6.21 Dynamic performance of DSTATCOM in voltage regulation mode

from 86V to 89V due to action of AC bus PI controller.

6.6.1 Performance of DSTATCOM With Recursive Inverse Based Control Algorithm

This section presents simulation and experimental results of the DSTATCOM controlled using recursive inverse based control algorithm under nonlinear load. The simulation results are obtained using a model developed in MATLAB environment using SIMULINK with SPS tool box. Experimental verification of control algorithm is made on the prototype developed in the laboratory and the test results are recorded using power quality analyzer and DSO.

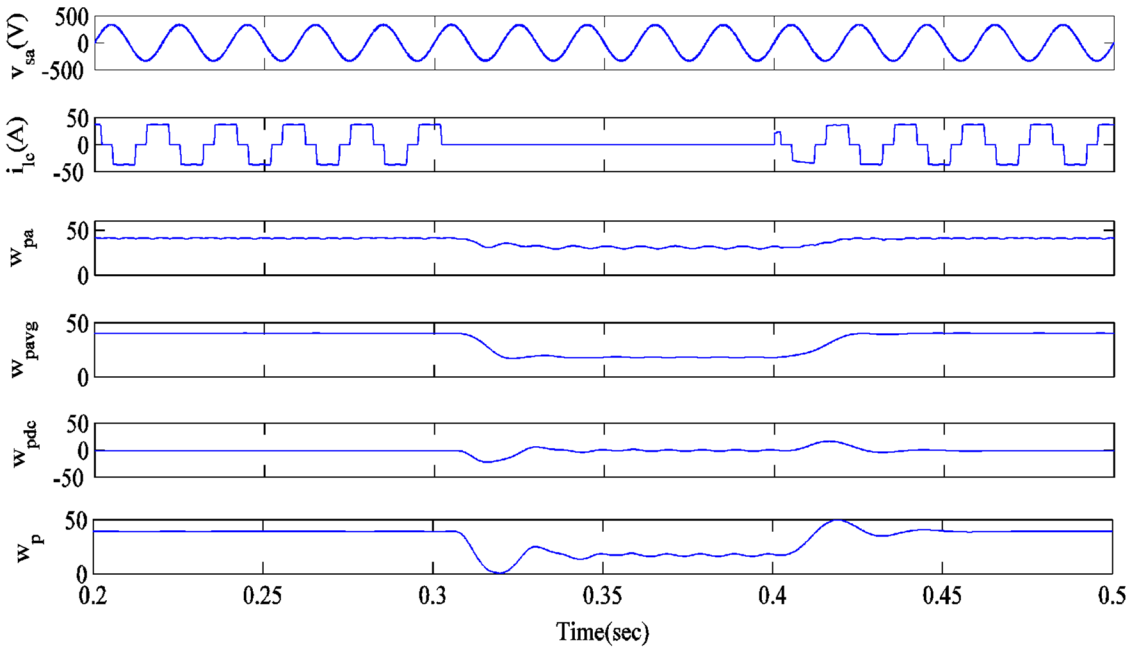
6.3.2.1 Simulated Performance of DSTATCOM in PFC and Voltage Regulation Modes

Simulated performance of DSTATCOM controlled using recursive inverse based control algorithm is studied in this section. This is divided into three parts. The first part discusses the performance of recursive inverse based control algorithm. The second and the third part present the performance of DSTATCOM in PFC and voltage regulation modes respectively. The simulated performances of control algorithm for DSTATCOM are studied as follows.

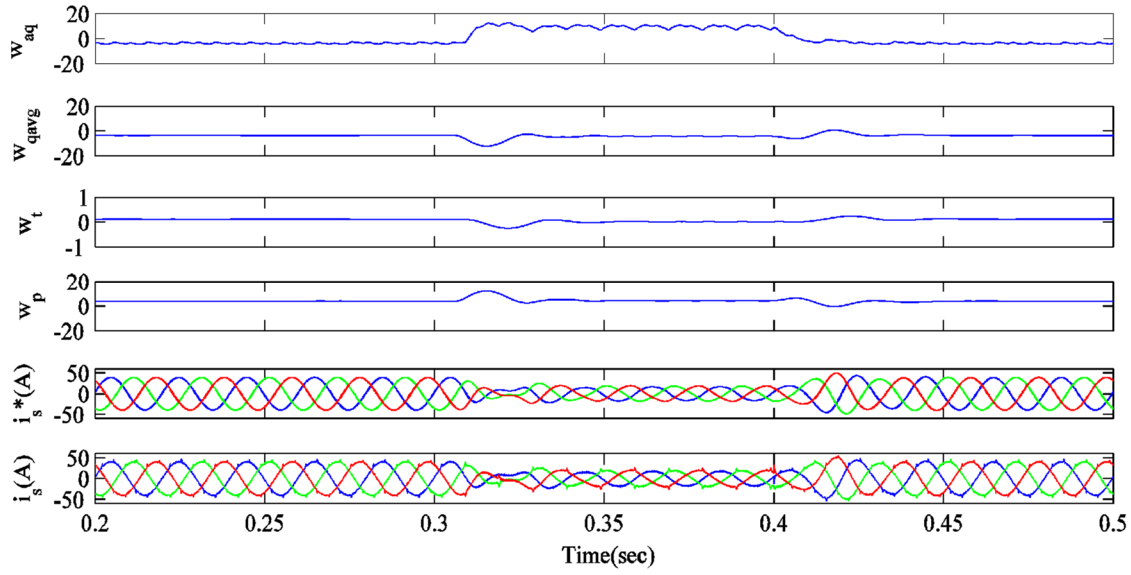
A. Performance of DSTATCOM With Recursive Inverse Based Control Algorithm in Voltage Regulation Mode

Fig. 6.22 shows the performance and intermediate signal of recursive inverse based control algorithm for control of DSTATCOM. Fig. 6.22(a) shows the waveforms of active power weight corresponding to phase 'a' of load current (w_{ap}), average active power weight (w_{pavg}), output of DC bus PI controller (w_{pdc}) and reference active power weight (w_p) along with phase 'a' of PCC voltage (v_{sa}) and phase 'c' of load current. This result is shown under steady state conditions (before t=0.3s) and unbalanced nonlinear load condition (t=0.3s to t=0.4s). An unbalance in the load is created when phase 'c' of load current is switched off.

Fig. 6.22(b) shows the waveforms of reactive power weight corresponding to phase 'b' of load current (w_{aq}), average reactive power weight (w_{qavg}), output of AC bus PI controller, reference reactive power weight (w_q) along with reference supply currents (i_s^*) and actual supply currents (i_s). It can be observed from these results that supply currents perfectly track the reference supply



(a)



(b)

Fig. 6.22 Performance and intermediate signals of recursive inverse based control algorithm in voltage regulation mode

currents in steady state condition at unbalanced load.

B. *Performance of DSTATCOM With Recursive Inverse Based Control Algorithm in Power Factor Correction (PFC) Mode*

Fig. 6.23 shows the performance of DSTATCOM in power factor correction mode. This shows the waveforms of PCC voltages (v_s), supply currents (i_s), load currents (i_{la}, i_{lb} and i_{lc}), compensator currents (i_{Ca}, i_{Cb} and i_{Cc}) and self-sustained DC bus voltage (V_{dc}). Fig. 6.23 shows the steady state response of the system till t=0.3s. During this time, the supply currents in all the three phases are balanced and sinusoidal and the DC bus voltage is regulated to its reference value of 700V due to the action of the shunt compensator. An unbalancing in the load is created

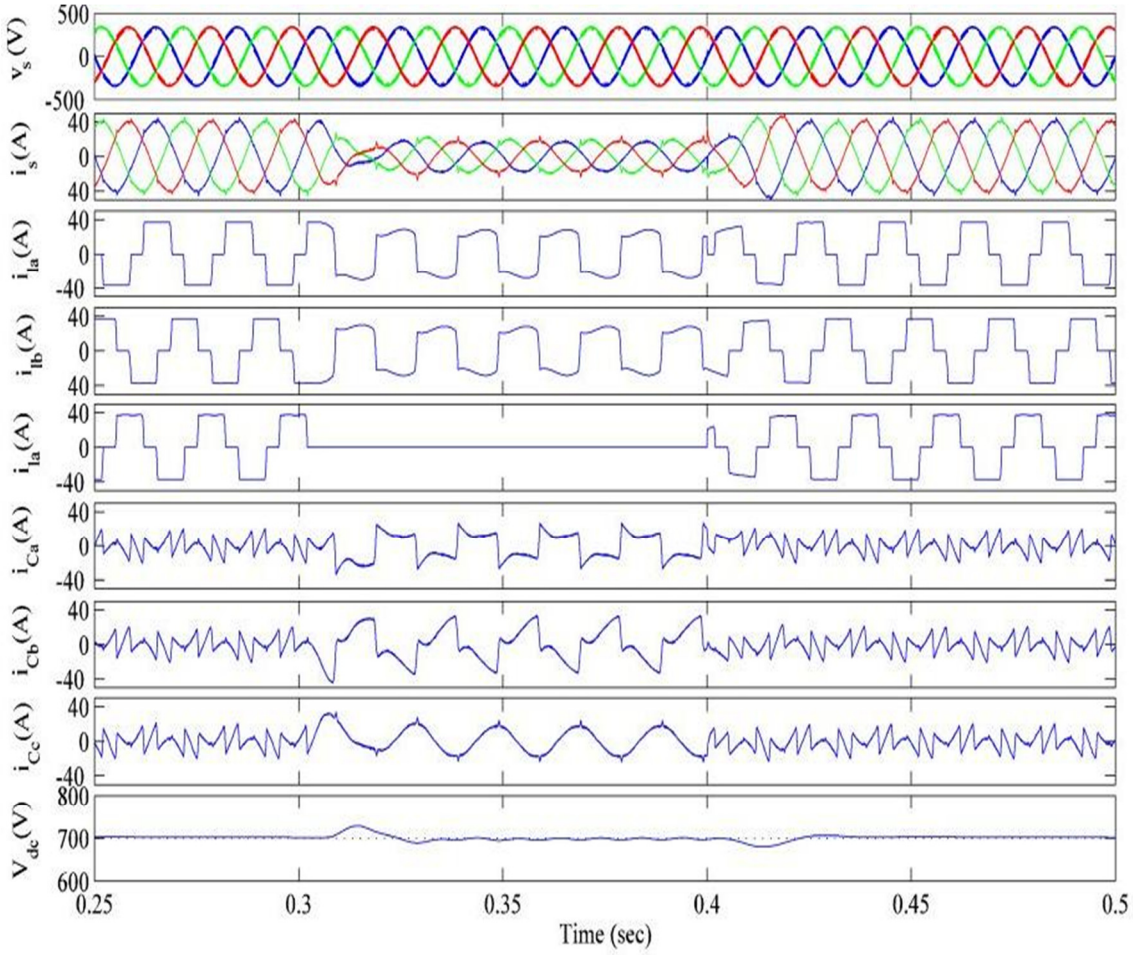


Fig. 6.23 Performance of DSTATCOM in PFC mode under nonlinear load

from t=0.3s to t=0.4s. During this time, phase 'c' of the load is switched off. It can be observed from these results that during load unbalancing the supply currents are still balanced and sinusoidal with reduced magnitude. The DC bus voltage is regulated to its reference value. After t=0.4 s, the load is restored back to its normal balanced condition.

Figs. 6.24(a)-(c) show the harmonic spectra of phase 'a' of PCC voltage (v_{sa}), supply current (i_{sa}) and load current (i_{la}). This shows the THD of 2.85%, 2.79% and 26.49% in PCC voltage, supply current and load current respectively. It can be observed from these results that the performance of DSTATCOM is satisfactory in maintaining unity power factor at the supply side. The DSTATCOM is also able to reduce harmonic content from 26.49% to 3.59% in supply current and works well under unbalanced load condition.

C. Performance of DSTATCOM in Voltage Regulation Mode Under Nonlinear Load

Fig. 6.25 shows the performance of proposed control algorithm for DSTATCOM in voltage regulation mode. This figure shows the waveforms of PCC voltages (v_s), supply currents (i_s), load currents (i_{la}, i_{lb} and i_{lc}), compensator currents (i_{Ca}, i_{Cb} and i_{Cc}), self-sustained DC bus voltage

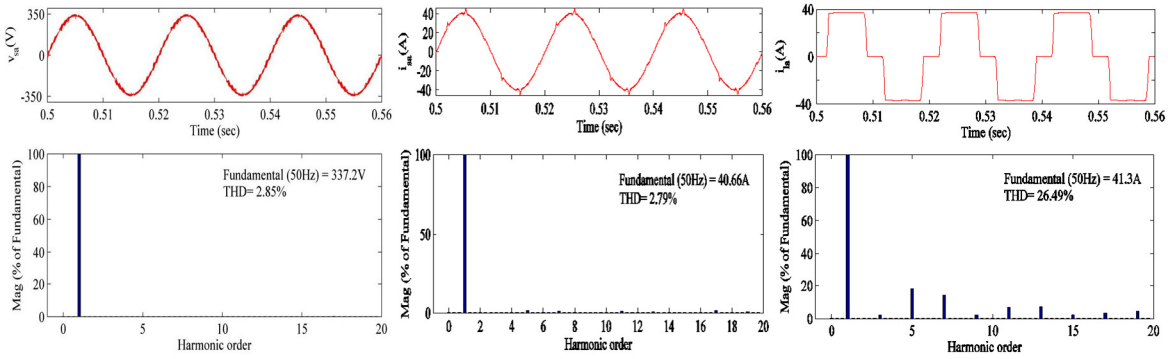


Fig. 6.24 Harmonic spectra of phase 'a' of (a) PCC voltage (b) supply current and (c) load current in PFC mode

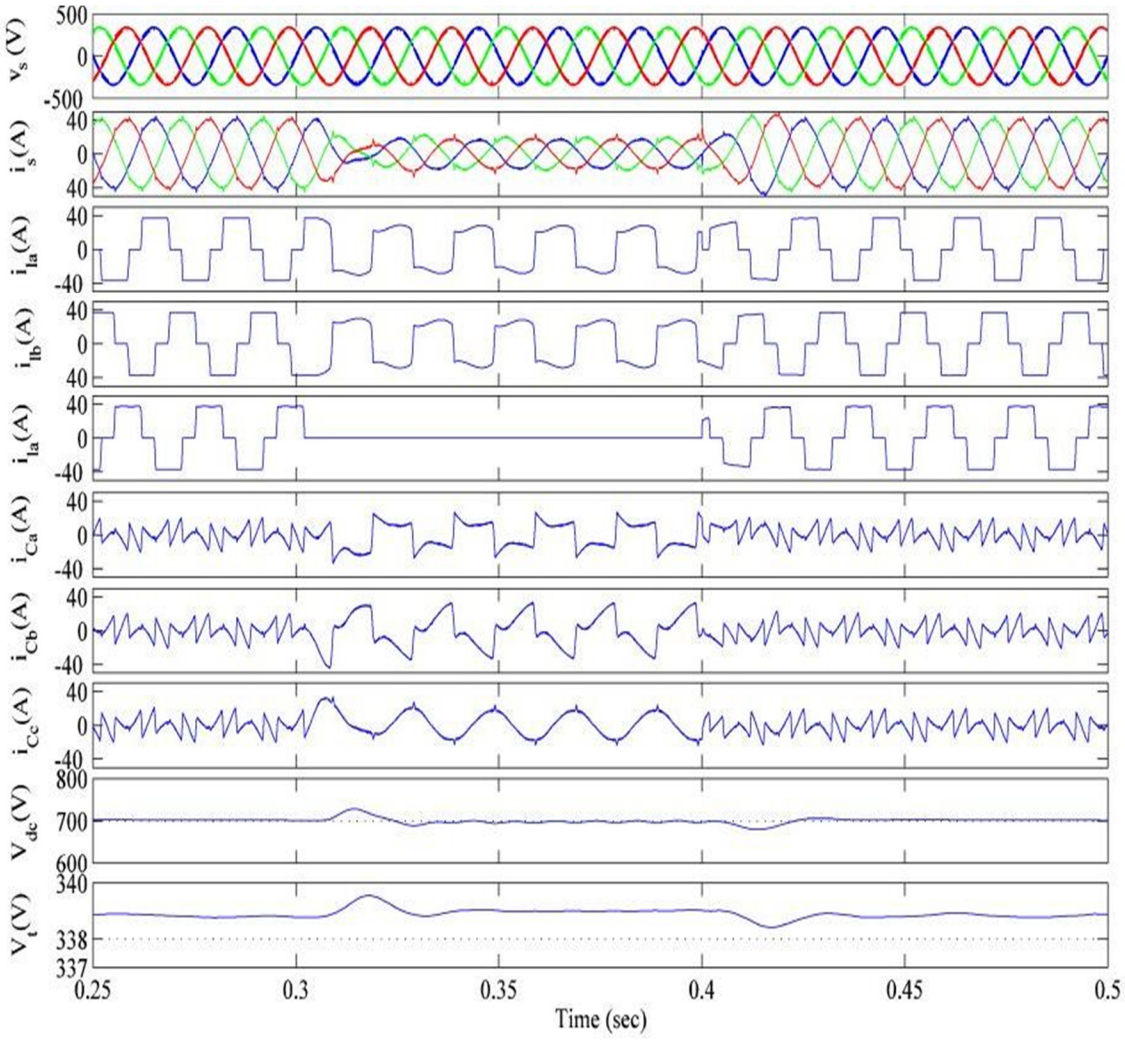


Fig. 6.25 Performance of DSTATCOM in voltage regulation mode under nonlinear load

(V_{dc}) and magnitude of PCC voltage (V_t). These results show that the system is under steady state till t=0.3s, and the supply currents are balanced and sinusoidal. The DC bus voltage and PCC voltage are regulated to their reference value of 700V and 338.89V due to the action of both the PI controllers. An unbalancing in the load is created at t=0.3s, when phase 'c' is switched off. During load unbalancing (t=0.3s to t=0.4s) it is observed from the results that the supply currents are still balanced and sinusoidal. The DC bus voltage and PCC voltage are settled down to their reference values within 1 to 1.5 cycles. The unbalancing in load is removed by reconnecting

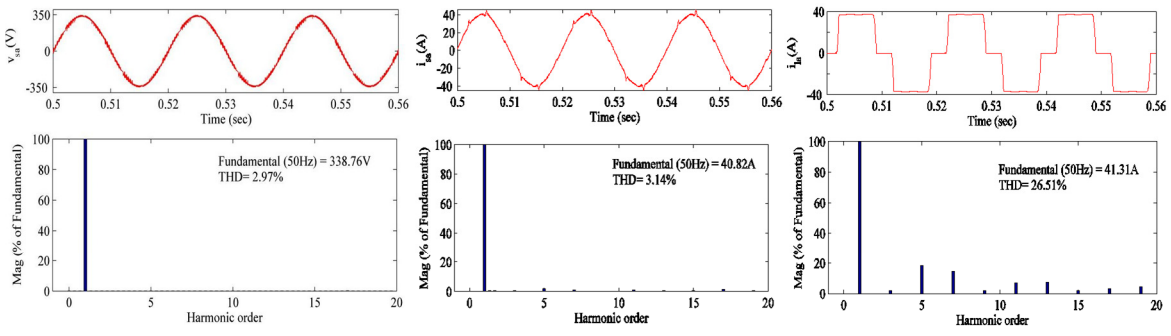
phase ‘c’ at t=0.4s, and dynamics in DC bus voltage and PCC voltage are observed for 1 to1.5 cycles. After t=0.4s, the system is settled down again under steady state condition.

Figs. 6.26 (a)-(c) show the harmonic spectra of phase ‘a’ PCC voltage (v_{sa}), supply current (i_{sa}) and load current (i_{la}). These results show THDs of 2.97% in PCC voltage, 3.14% in supply current and 26.51% in load current. The THDs of PCC voltage and supply currents are within the limits specified by IEEE-519 standard. These results show the satisfactory performance of DSTATCOM in regulating the PCC voltage to its reference value and reducing the THD in supply current within the specified international limits.

6.6.2.2 Experimental Performance of DSTATCOM in PFC Mode

This section discusses the performance of recursive inverse based control algorithm on the prototype developed in the laboratory. First part discusses the performance of control algorithm. The second and third parts present the performance of DSTATCOM for mitigation of power quality problems such as harmonics reduction and load balancing.

A. Performance of Recursive Inverse Based Control Algorithm for DSTATCOM



(a) (b) (c)

Fig. 6.26 Harmonic spectra of phase ‘a’ of (a) PCC voltage (b) supply current and (c) load current in voltage regulation mode

Fig. 6.27 shows the intermediate signals obtained using the proposed control algorithm of shunt compensator. Fig. 6.27(a) shows the waveforms of weighted values corresponding to fundamental active power component of load (w_{ap}, w_{bp} and w_{cp}) along with their average weight (w_{pavg}). These results show the fast convergence of weighted values even under unbalanced load condition when one phase of the load is switched off. Fig. 6.27(b) shows the waveforms of average weighted value (w_{pavg}), output of DC bus PI controller (w_{pdc}), reference weighted value (w_p) which is calculated by addition of w_{pavg} and w_{pdc} and phase 'a' of active reference supply current (i_{pa}^*). These waveforms show the dynamics of the system when one phase of load is switched off. Fig. 6.27(c) gives the waveforms of phase 'a' PCC voltage (v_{sa}), filtered phase 'a' PCC voltage (v_{sa1}) which is used in the control algorithm for reference current generation, phase

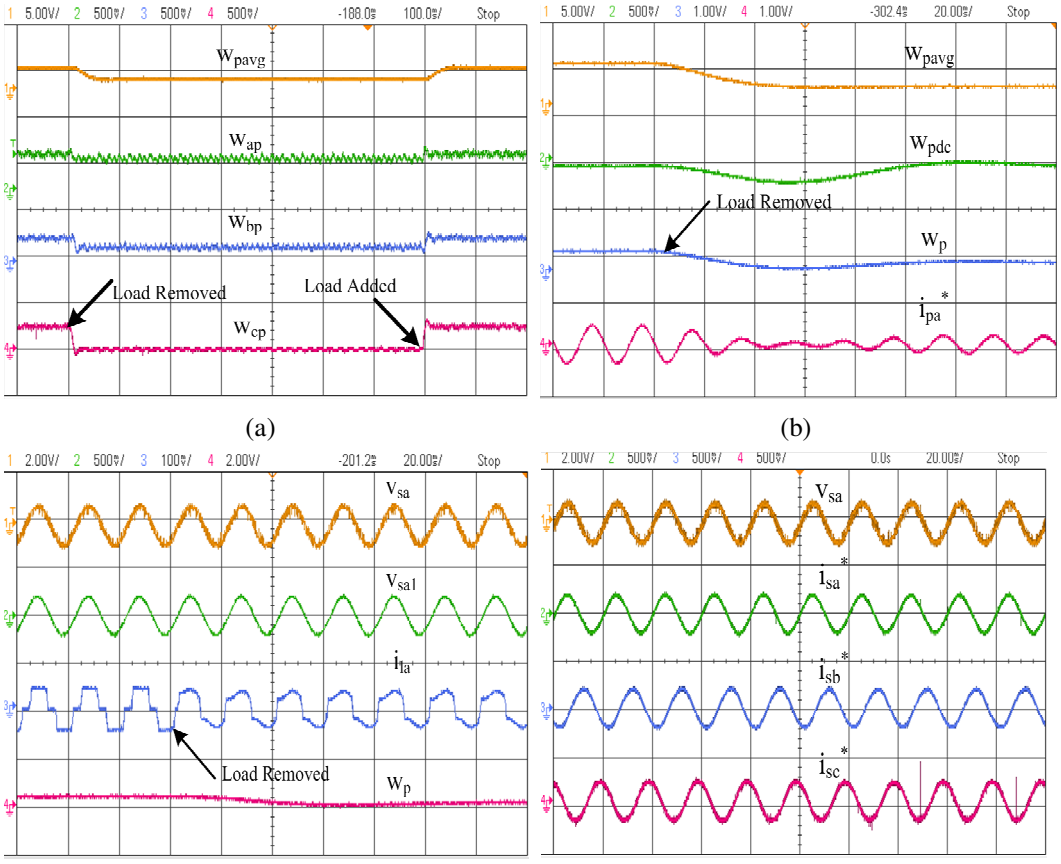


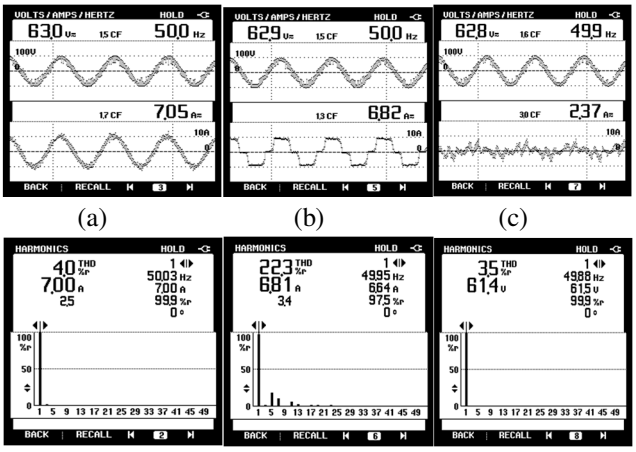
Fig. 6.27 Intermediate signals of recursive inverse based control algorithm

'a' load current (i_{la}) and reference weighted value (w_p), for the case when phase 'c' of load current is switched off. Fig. 6.27(d) gives the waveforms of reference supply currents (i_{sa}^*, i_{sb}^* and i_{sc}^*) along with phase 'a' PCC voltage (v_{sa}).

B. Steady State Performance of DSTATCOM Under Nonlinear Load

Figs. 6.28(a)-(f) show the steady state performance of DSTATCOM under nonlinear load. Figs. 6.28(a)-(c) depict the waveforms of phase 'a' supply current (i_{sa}), load current (i_{la}) and compensator current (i_{Ca}) along with PCC voltage (v_{sa}). Figs. 6.28(d)-(f) depict the harmonic spectra of phase 'a' supply current, load current and PCC voltage. These results show the THD of 4% in supply current, THD of 22.3% in load current and THD of 3.5% in PCC voltage respectively. These results show satisfactory performance of DSTATCOM in maintaining THD in supply currents and PCC voltage within the limit specified by international standards.

Fig. 6.29 shows the simulated performance of the DSTATCOM using recursive inverse based control algorithm at same voltage rating for which experimental system is developed. These



(a) (b) (c)

(d) (e) (f)

Fig. 6.28 Steady state performance of DSTATCOM under nonlinear load (a), (b) and (c) i_{sa}, i_{la} and i_{Ca} along with v_{sa} (d), (e) and (f) harmonic spectra of i_{sa}, i_{la} and v_{sa}

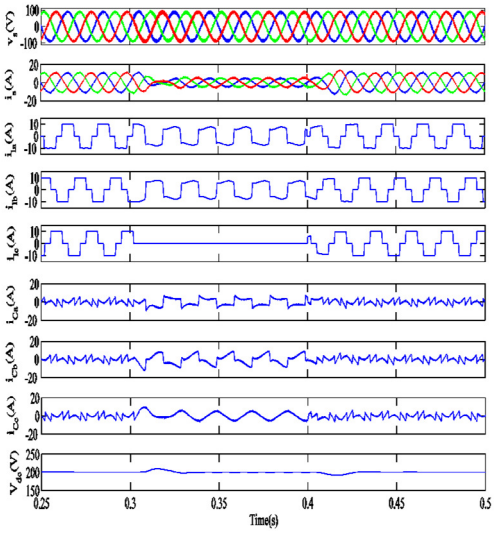


Fig. 6.29 Simulated performance of DSTATCOM in PFC mode

results show the waveforms of PCC voltages (v_s), supply currents (i_s), load currents (i_{la}, i_{lb} and i_{lc}), compensator current (i_{Ca}, i_{Cb} and i_{Cc}) and self-sustained DC bus voltage (V_{dc}). It is observed from these results that supply currents are balanced and sinusoidal along with regulated DC bus voltage at the reference voltage of 200V during steady state (before t=0.3s) and unbalanced load condition (t=0.3s to t=0.4s).

C. Dynamic Performance of DSTATCOM Under Nonlinear Load

Fig. 6.30 shows the dynamic performance of DSTATCOM under nonlinear load. Figs. 6.30(a)-(c) depict the waveforms of supply currents (i_{sa}, i_{sb} and i_{sc}), load currents (i_{la}, i_{lb} and i_{lc}) and compensator currents (i_{Ca}, i_{Cb} and i_{Cc}) along with phase 'a' PCC voltage (v_{sa}). These results show the performance when an unbalance is created in the load. This is created in load when phase 'c'

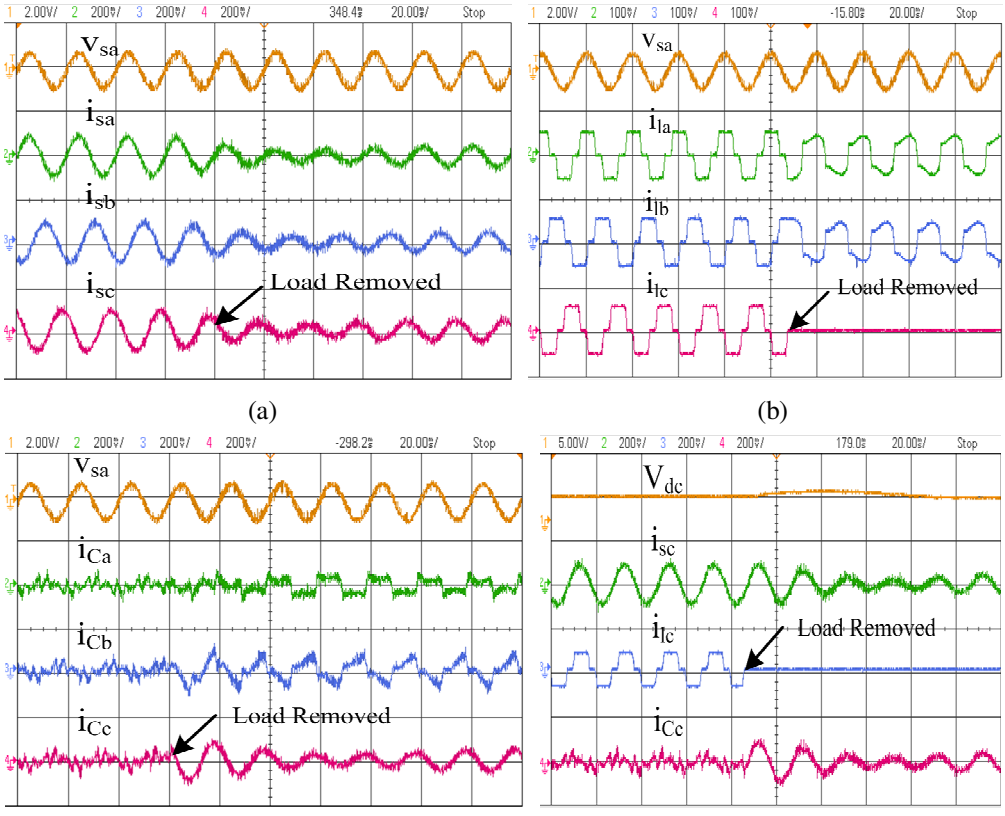


Fig. 6.30 Dynamic performance of DSTATCOM under nonlinear load

is switched off. During steady state and unbalanced load condition, it is observed from these test results that the supply currents are balanced and sinusoidal. Fig. 6.30(d) shows the waveforms of DC bus voltage (V_{dc}), phase 'c' supply current (i_{sc}), phase 'c' load current (i_{lc}) and phase 'c' compensator current (i_{Cc}). These results show the variation of DC bus voltage when an unbalance is created in the load. The DC bus voltage achieves its reference value of 200V, within 1.5 to 2 cycles. It can be observed from these test results that the DSTATCOM performs load balancing and power factor correction.

6.6.3 Performance of DSTATCOM with Immune Feedback Based Control Algorithm

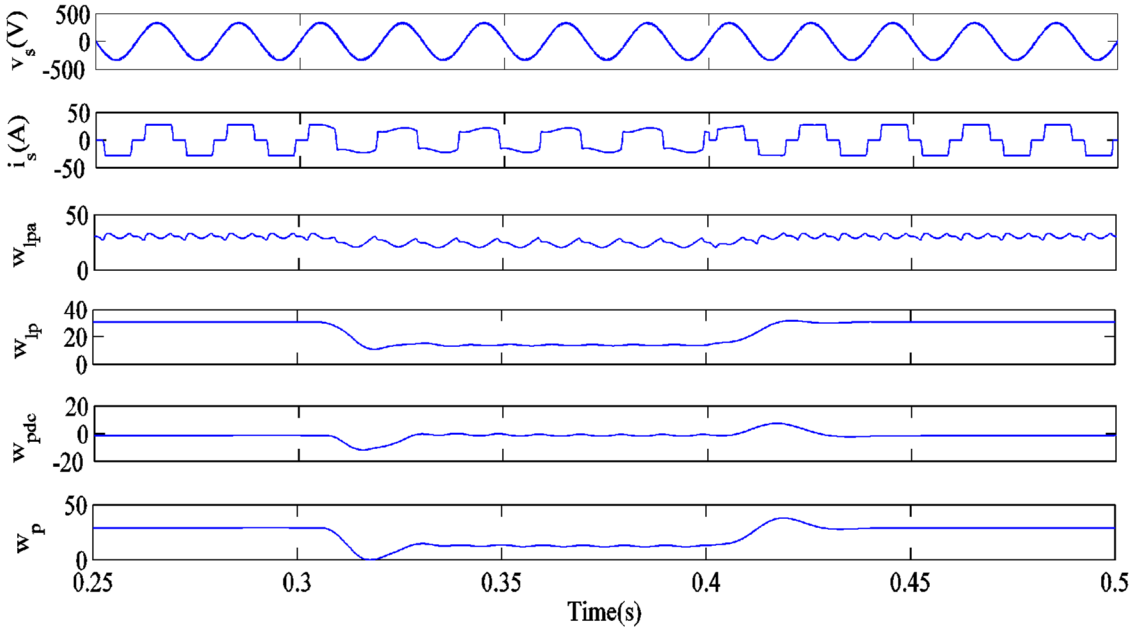
The performance of immune feedback based control algorithm for control of DSTATCOM is studied here. The features of DSTATCOM such as harmonics elimination, reactive power compensation and voltage regulation are demonstrated with immune feedback based control algorithm. The simulated performance is studied in PFC and voltage regulation modes, whereas the real time performance of DSTATCOM on the prototype developed in the laboratory is presented in PFC mode.

6.6.3.1 Simulated Performance of DSTATCOM in PFC and Voltage Regulation Modes

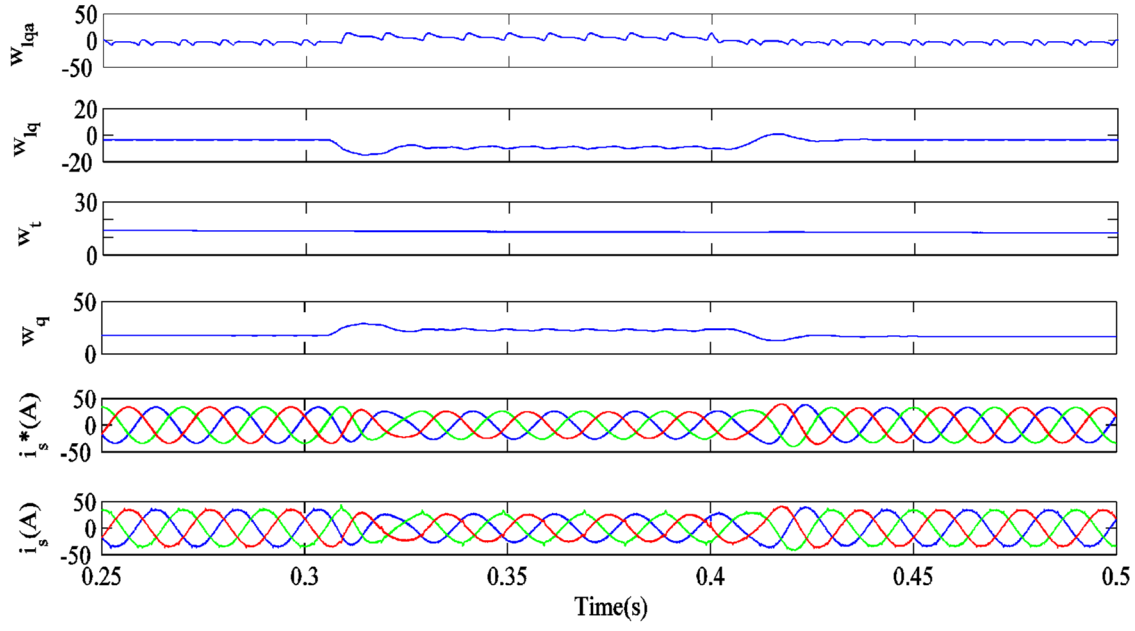
This section presents simulated performance of DSTATCOM with immune feedback based control algorithm. It is divided into three parts. The first part discusses the performance and intermediate signals of control algorithm. The second and the third parts deal with the performance of DSTATCOM in PFC and voltage regulation modes under varying nonlinear load.

A. Performance of Immune Feedback Based Control Algorithm for DSTATCOM

Figs. 6.31(a) and (b) show the performance of proposed control algorithm for the shunt compensator in voltage regulation mode. Fig. 6.31(a) shows the waveforms of unit in phase template (u_{pa}), generated error (e_a) between sensed (i_{la}) and estimated load current, weighted value (w_{lpa}) corresponding to active power component of phase 'a' of load current, estimated



(a)



(b)

Fig. 6.31 Performance and intermediate signals of immune feedback based control algorithm for DSTATCOM in voltage regulation mode

average weighted value (w_{pavg}), sensed DC bus voltage (V_{dc}), filtered DC bus voltage (V_{dcf}), output of DC bus PI controller (w_{pdc}) and reference active power weight (w_p) along with phase 'a' of supply voltage (v_{sa}). Before t=0.3s, the load currents are balanced and system is in steady state condition. An unbalancing is created in load during t=0.3s to t=0.4s, when phase 'c' of load is switched off. It is observed from these results that weight corresponding to active power component of load current converges to a constant value in steady state as well as in unbalanced load condition.

Fig. 6.31(b) shows the waveforms of unit quadrature template (u_{qa}), weight corresponding to reactive power component of phase 'a' of load current (w_{lqa}), average reactive power weight (w_{qavg}), amplitude of PCC voltage (V_t), filtered amplitude of PCC voltage (V_{tf}), output of AC bus PI controller (w_t) and reference reactive power weight (w_q) and reference supply currents (i_s^*) along with sensed supply currents (i_s). These results show the weight corresponding to reactive power component of load current converges in unbalanced load condition. The supply currents track the reference currents perfectly. The performance of the shunt compensator is observed to be satisfactory with the immune feedback based control algorithm.

B. Performance of DSTATCOM in PFC mode Under Nonlinear Load

Fig. 6.32 shows the performance of the shunt compensator under nonlinear load. The waveforms are shown for PCC voltages (v_s), supply currents (i_{sa}, i_{sb} and i_{sc}), load currents (i_{la}, i_{lb} and i_{lc}), compensator currents (i_{Ca}, i_{Cb} and i_{Cc}) and DC link voltage (V_{dc}). It can be observed from this figure that the system is under steady state condition till t=0.3s and the DC link voltage is maintained at its reference voltage of 700V. One phase (phase '*c*') of load is now switched off from t=0.3s to t=0.4s. It is observed that the load currents are unbalanced and non-sinusoidal,

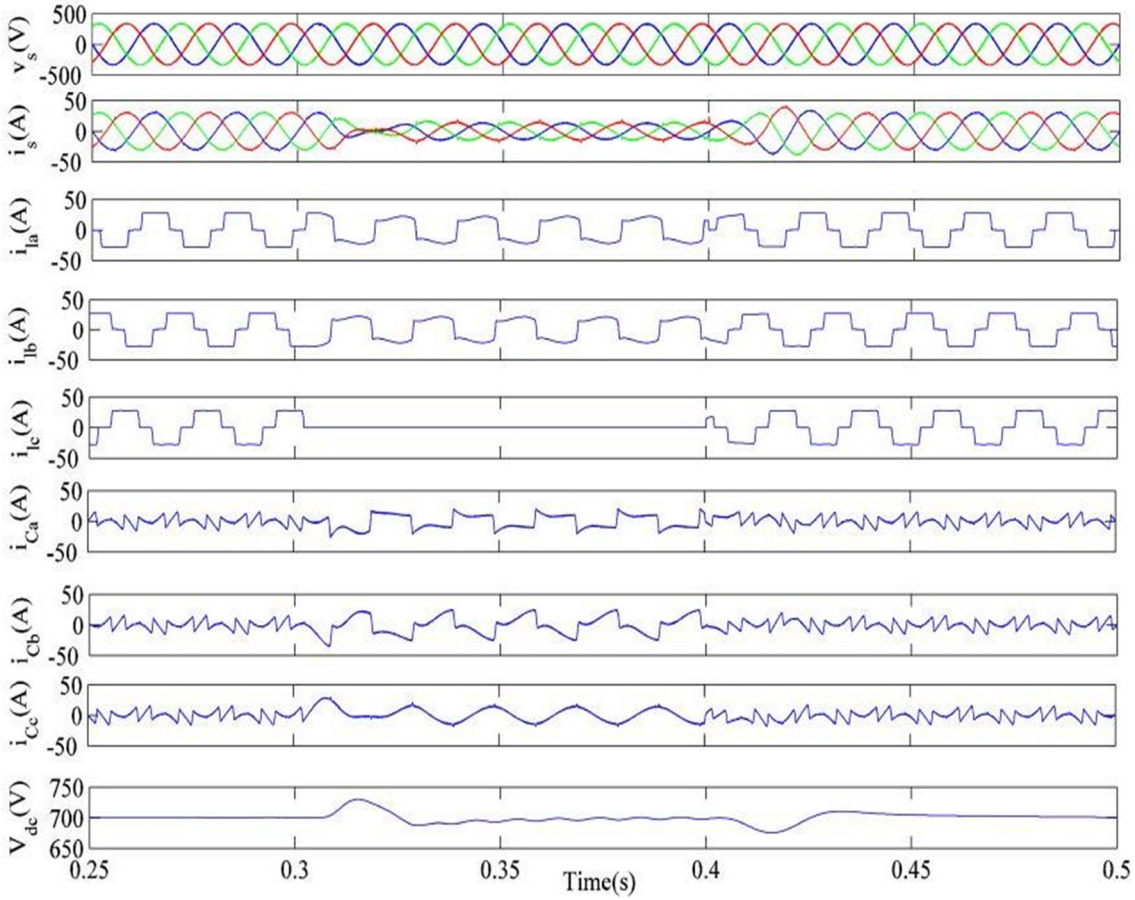
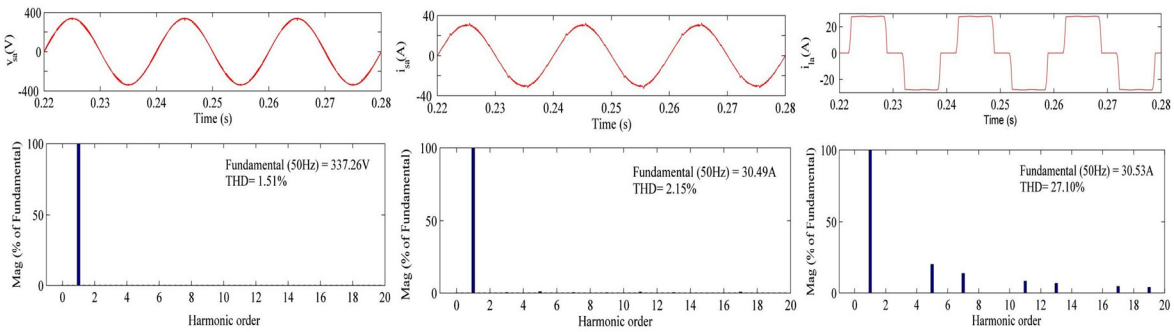


Fig. 6.32 Performance of shunt compensator using immune feedback in PFC mode

however the supply currents are sinusoidal and balanced. The DC link voltage is regulated to its reference value of 700V with the action of PI controller within a couple of cycles. The performance of DSTATCOM is satisfactory under load unbalancing. The supply voltages and supply currents are observed to be in phase and thus power factor correction capability of DSTATCOM is observed.

Fig. 6.33 shows the waveforms and harmonic spectra of PCC voltage (v_{sa}), supply current (i_{sa}) after compensation and load current (i_{la}) in PFC mode. The values of THDs of the phase 'a' of PCC voltage, supply current and load current are observed to be 1.51%, 2.15%, and 27.10% respectively. It can be observed from these results that the harmonic distortion of supply current lies within the limit 5% specified by IEEE-519 standard.



(a) (b) (c)

Fig. 6.33 Harmonic spectra of Phase 'a' of (a) PCC voltage, v_{sa} (b) supply current, i_{sa} (c) load current, i_{la} in PFC mode

C. Performance of DSTATCOM in Voltage Regulation Mode Under Nonlinear Load

Fig. 6.34 shows the performance of the shunt compensator under nonlinear load in voltage regulation mode. These results show waveforms for the PCC voltages (v_s), supply currents (i_{sa}, i_{sb} and i_{sc}), load currents (i_{la}, i_{lb} and i_{lc}), compensator currents (i_{Ca}, i_{Cb} and i_{Cc}), self-sustained DC link voltage (V_{dc}) and PCC voltage magnitude (V_t). It can be observed from this figure that the system is under steady state condition till t=0.3s and the DC link voltage and PCC voltage magnitudes are maintained at their reference voltages of 700V and 338.8V respectively. One phase (phase '*c*') of load is now switched off from t=0.3s upto t=0.4s. It is observed that the load currents are unbalanced and non-sinusoidal. However, the supply currents are sinusoidal and balanced. The DC link voltage and PCC voltage are regulated to their reference values with the action of PI controller within a couple of cycles. The performance of DSTATCOM is observed to be satisfactory in voltage regulation mode.

Fig. 6.35 shows the waveforms and harmonic spectra of phase 'a' of PCC voltage (v_{sa}), supply current (i_{sa}) after compensation and load current (i_{la}) in voltage regulation mode. The values of THDs of the phase 'a' of PCC voltage, supply current and load current are observed as 1.74%,

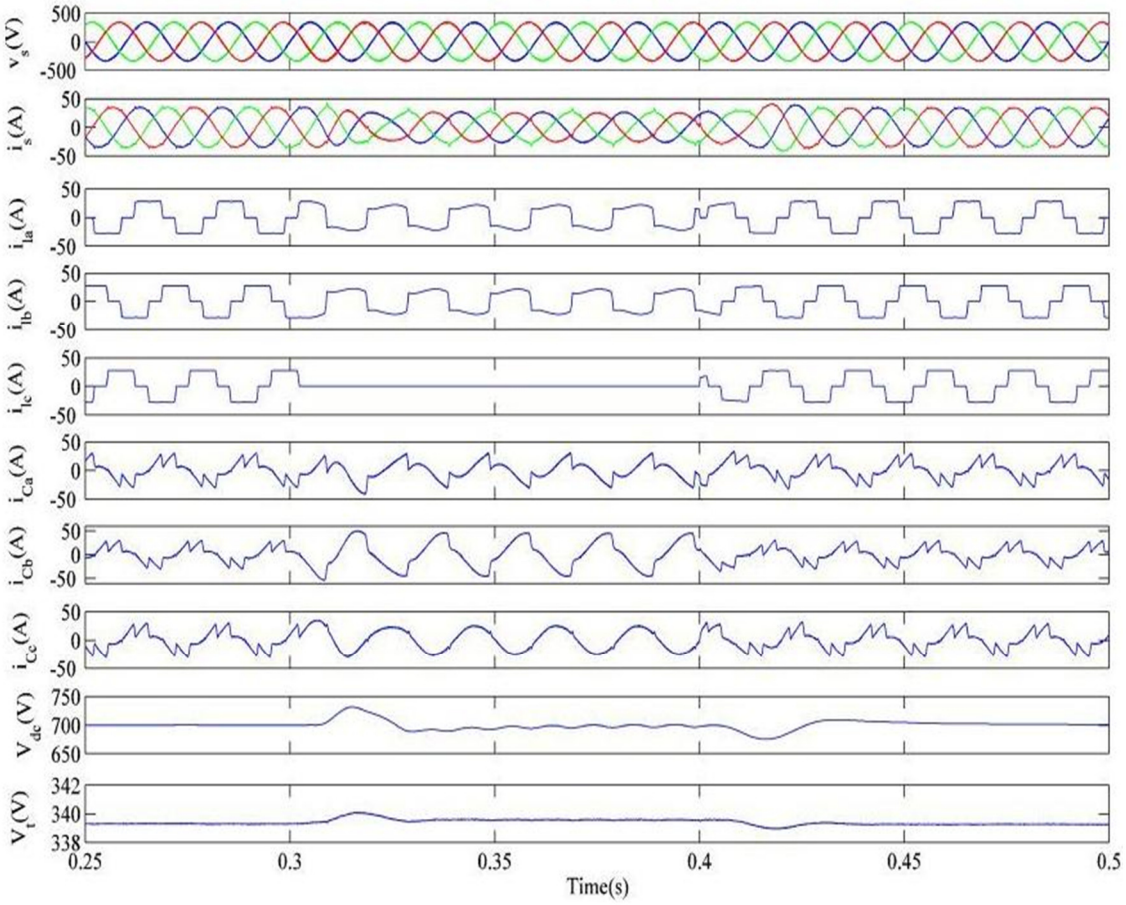


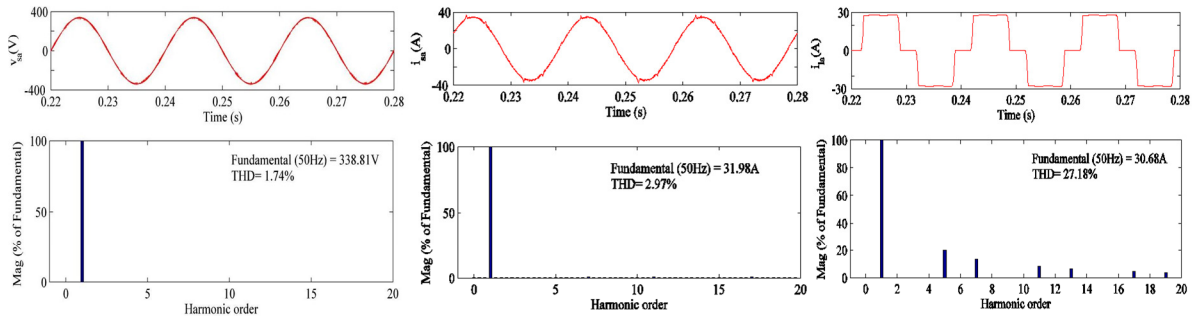
Fig. 6.34 Performance of shunt compensator using immune feedback in voltage regulation mode

2.97%, and 27.18% respectively. It can be observed from these results that the harmonic distortion of supply current lies within the limit 5% specified by IEEE-519 standard.

6.6.3.2 Experimental Performance of DSTATCOM in PFC Mode

This section presents the experimental performance of DSTATCOM with immune feedback based control algorithm. It is divided into three parts. The first part discusses the real time performance of the control algorithm. The second and third part discuss harmonic reduction and load balancing performance of DSTATCOM in PFC mode.

A. Performance of DSTATCOM With Immune Feedback Based Control Algorithm Under Nonlinear Load



(a) (b) (c)

Fig. 6.35 Harmonic spectra of Phase 'a' of (a) PCC voltage, v_{sa} (b) supply current, i_{sa} (c) load current, i_{la} in voltage regulation mode

Fig. 6.36 shows the performance of proposed control algorithm for control of DSTATCOM in PFC mode under nonlinear load. Fig. 6.36(a) shows the waveforms of inphase unit template (u_{pa}) and load current (i_{la}) along with phase 'a' of PCC voltage (v_{sa}) and its filtered value (v_{saf}). Fig. 6.36(b) shows the waveforms of sensed DC bus voltage (V_{dc}), filtered DC bus voltage (V_{dcf}), error signal (V_{de}) between reference DC bus and sensed DC bus voltage and the output of DC bus PI controller. Fig. 6.36(c) shows the waveforms of error signal (e_a), incremental weighted value (Δw_{pa}), delayed weighted value (w_{pa}) and weighted value corresponding to active power component of phase 'a' of load current. Fig. 6.36(d) shows the average weighted value (w_{pavg}) corresponding to the active power component of load, output of DC bus PI controller (w_{pdc}) and reference active power weight (w_p) along with w_{lpa}. Fig. 6.36(e) shows the reference supply currents (i_{sa}^*, i_{sb}^* and i_{sc}^*) along with phase 'a' of sensed supply current (i_{sa}). It is observed from these results that the shunt compensator performs satisfactory in steady state and unbalanced load condition using the immune based control algorithm.

B. Steady State Performance of DSTATCOM with Immune Feedback Based Control Algorithm Under Nonlinear Load

The steady state performance of DSTATCOM can be observed from Fig. 6.37. The waveforms of supply voltage and supply current (v_{sa} and i_{sa}), supply voltage and load current (v_{sa} and i_{la}) and

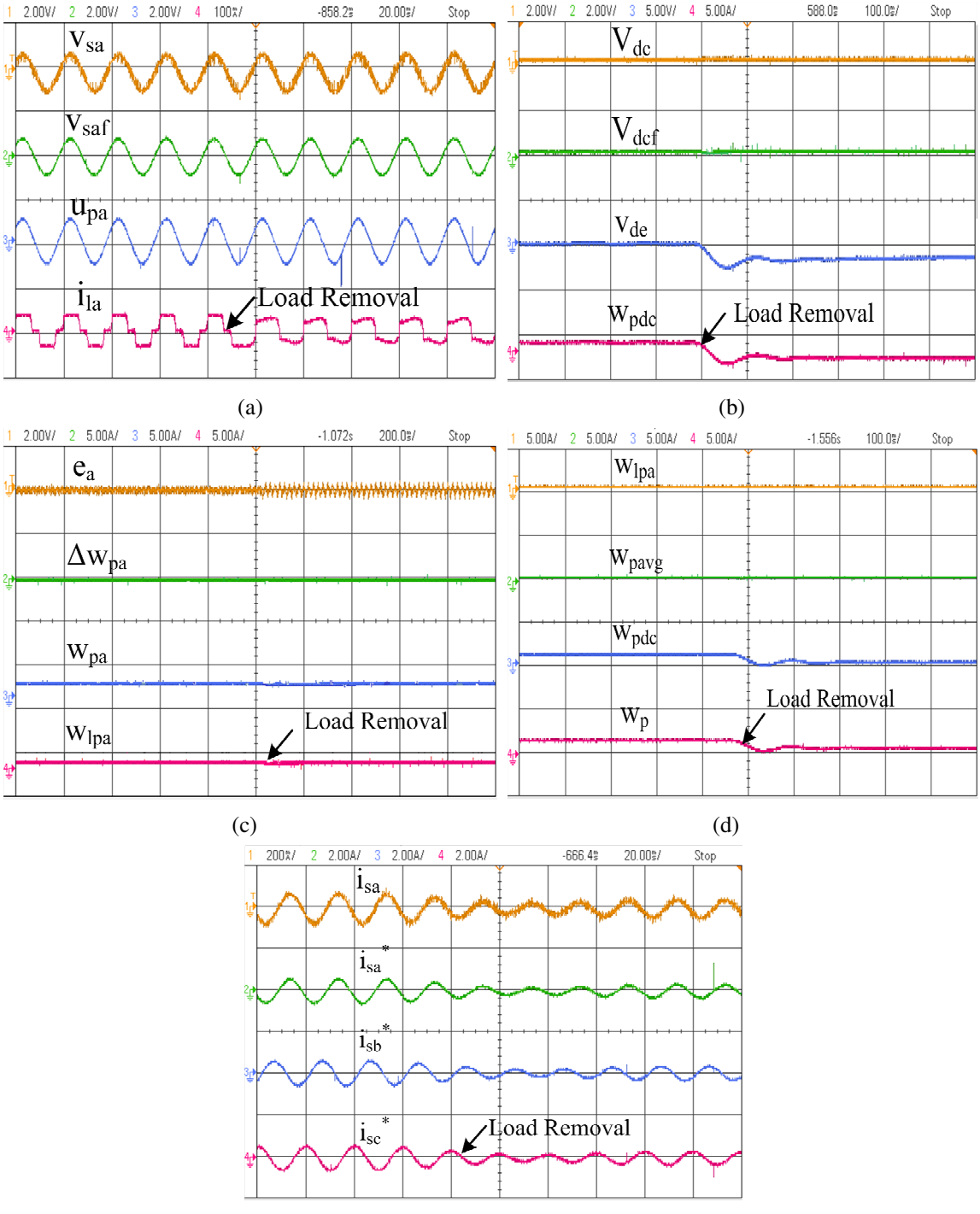


Fig. 6.36 Experimental performance of shunt compensator with immune feedback based control algorithm

supply voltage and compensator current (v_{sa} and i_{Ca}) are shown in Figs. 6.37(a)-(c). Harmonic spectra corresponding to phase '*a*' of supply current (i_{sa}), load current (i_{la}) and PCC voltage are shown in Figs. 6.37(d)-(f). It is observed that the percentage of THDs in supply current, load

current and PCC voltage are 2.3%, 22.9% and 3.2% respectively. It can be observed from the steady state response of the system that the DSTATCOM is able to correct the power factor of the supply current and reduce the THD in supply current to less than 5% level specified in an IEEE-519 standard.

Fig. 6.38 shows the simulated performance of the DSTATCOM using immune feedback based control algorithm at same voltage rating for which experimental system is developed. This shows the waveforms of PCC voltages (v_s), supply currents (i_s), load currents (i_{la}, i_{lb} and i_{lc}), compensator current (i_{Ca}, i_{Cb} and i_{Cc}) and self-sustained DC bus voltage (V_{dc}). It is observed from these results that supply currents are balanced and sinusoidal along with regulated DC bus voltage at the reference voltage of 200V during steady state (before t=0.3s) and unbalanced load condition (t=0.3s to t=0.4s).

C. Dynamic Performance of DSTATCOM Under Nonlinear Load

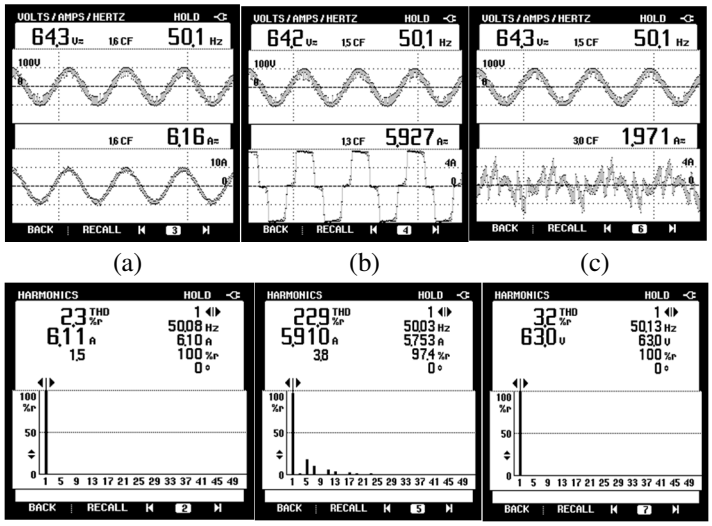


Fig. 6.37 Steady state performance for power factor correction using DSTATCOM with nonlinear load (a)-(c) waveforms of supply current, i_{sa} load current, i_{la} and compensator current, i_{Ca} along with v_{sa} (d)-(f) Harmonic spectra of i_{sa}, i_{la} and i_{Ca}

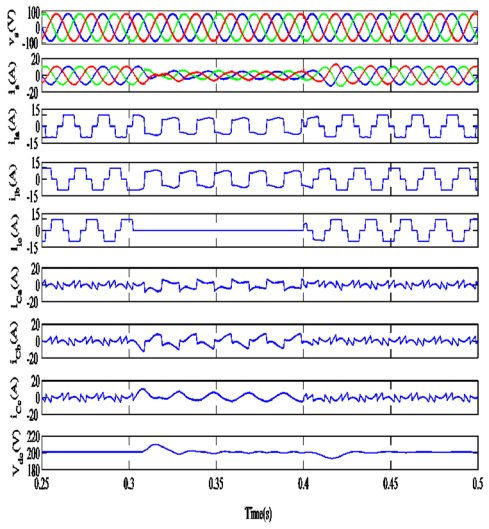


Fig. 6.38 Simulated performance of DSTATCOM in PFC mode

Figs. 6.39(a)-(d) show dynamic performance of DSTATCOM under nonlinear load. Fig. 6.39(a) shows the waveforms of supply voltage (v_{sa}) and the three phase supply currents (i_{sa}, i_{sb} and i_{sc}) when load on phase 'c' is suddenly removed. It is observed that the supply currents decrease in magnitude but are sinusoidal and balanced. Fig. 6.39(b) shows the supply voltage (v_{sa}) and the three phase load currents (i_{la}, i_{lb} and i_{lc}) when load in phase 'c' is suddenly removed. Fig. 6.39(c) shows the supply voltage (v_{sa}) and three phase compensator currents (i_{Ca}, i_{Cb} and i_{Cc}) under the same load dynamics. It is observed from these results that the compensator currents increase and provide the necessary current injection during the unbalanced load condition. Fig. 6.39(d) shows the waveforms of DC link voltage (V_{dc}), load current (i_{lc}) supply current (i_{sc}) and compensator

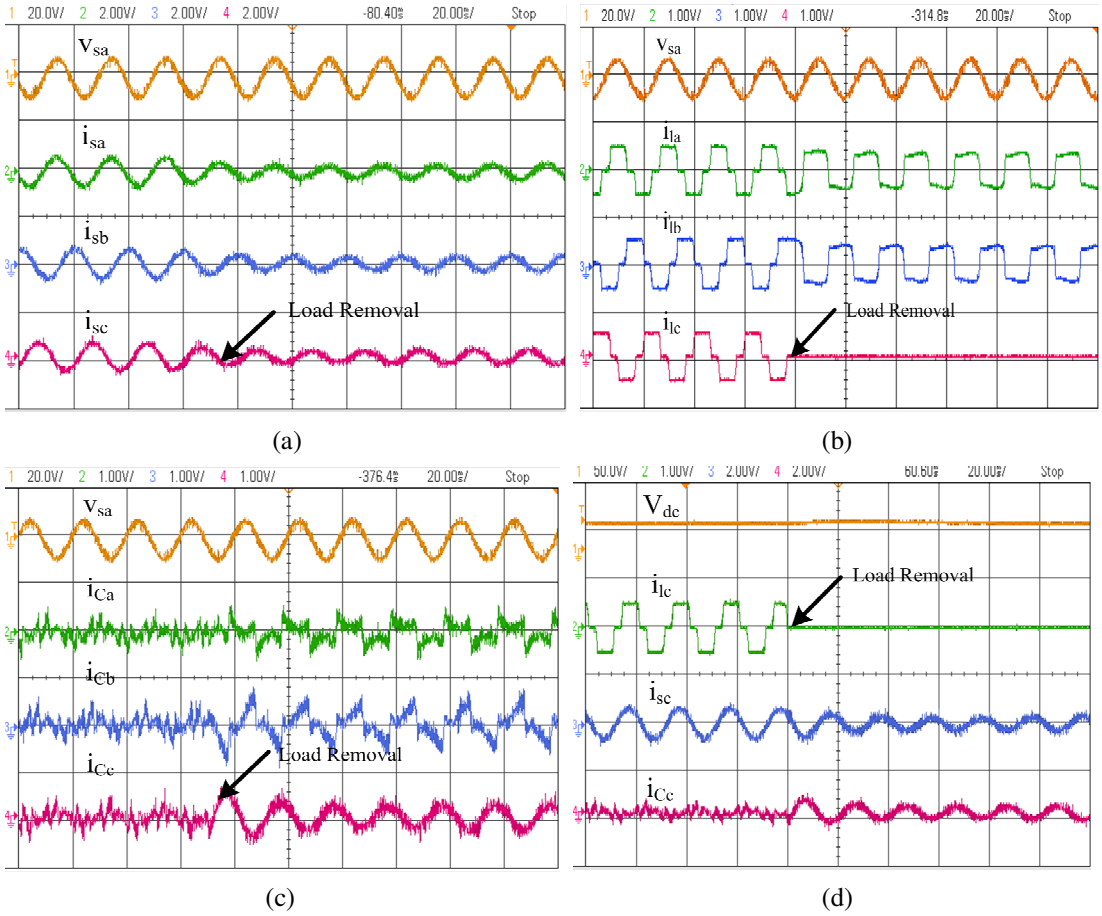


Fig. 6.39 Experimental results of the system under dynamic load conditions (a) v_{sa}, and supply currents (i_{sa}, i_{sb}, i_{sc}) (b) v_{sa}, and load currents (i_{la}, i_{lb}, i_{lc}) (c) v_{sa}, and compensator currents (i_{Ca}, i_{Cb}, i_{Cc}) (d) V_{dc}, i_{lc}, i_{sc}, i_{Cc}

current (i_{Cc}) of phase 'c'. This result shows that the DC bus voltage is regulated to its reference value within couple of cycles during unbalanced load currents.

6.7 CONCLUSIONS

The mathematical formulation and performance of recursive theory based control algorithms for the DSTATCOM has been presented here. The basic principle of recursive theory has been explained and variable forgetting factor based recursive least square algorithm, the recursive inverse and immune feedback based control algorithms have also been discussed under this classification. These control algorithms have been developed in MATLAB environment using SIMULINK and SPS tool boxes. The application of DSTATCOM for harmonics elimination, reactive power compensation, power factor correction and load balancing have been demonstrated with each of these algorithms. Simulation results have been presented for control of DSTATCOM in PFC and voltage regulation modes under steady state as well as dynamic load conditions. Real time validation of these control algorithms have been done on the prototype model developed in the laboratory. The performance of DSTATCOM with recursive theory based control algorithms has been observed to be satisfactory in PFC and voltage regulation modes.

CHAPTER-VII
ARTIFICIAL INTELLIGENCE BASED CONTROL ALGORITHMS FOR DSTATCOM

7.1 GENERAL

Recursive theory based control algorithms have been used in the previous chapter for the control of DSTATCOM. This chapter presents control algorithms for DSTATCOM based on artificial intelligence. Soft computing based control algorithms pertain to the broad area of artificial intelligence. These control algorithms work on the principle of human intelligence to achieve a specific task for which they are designed. Intelligent control systems have capability of learning, self-organizing or self-adapting. These control algorithms are based on adaptive neuro fuzzy inference system (ANFIS) and recurrent neural network learning technique. These control algorithms are applied to control DSTATCOM and to mitigate current related power quality problems such as harmonic currents, reactive power and load unbalancing.

7.2 CONFIGURATION AND OPERATING PRINCIPLE OF DSTATCOM

Fig. 7.1 shows the schematic diagram of VSC based DSTATCOM connected at point of common coupling (PCC). A three-phase AC mains feeds a three phase nonlinear load with grid impedance represented by a series resistive inductive branch (R-L). DSTATCOM is designed using three-leg voltage source converter (VSC) and uses six insulated gate bipolar transistors (IGBTs) with anti-parallel diodes and DC link capacitor (C_{dc}) at DC side. Interfacing inductors (L_f) are used at the AC side of VSC, which couple the VSC to the grid. High frequency switching noise generated by switching of IGBTs is reduced with the help of ripple filters (R_f-C_f). These filters comprise series connected capacitive (C_f) and resistive (R_f) elements at the PCC. The nonlinear load is connected in the form of uncontrolled bridge rectifier with series R-L branch. Voltages at PCC (v_{sa}, v_{sb}), supply currents (i_{sa}, i_{sb}), load currents (i_{la}, i_{lb} and i_{lc}) and DC

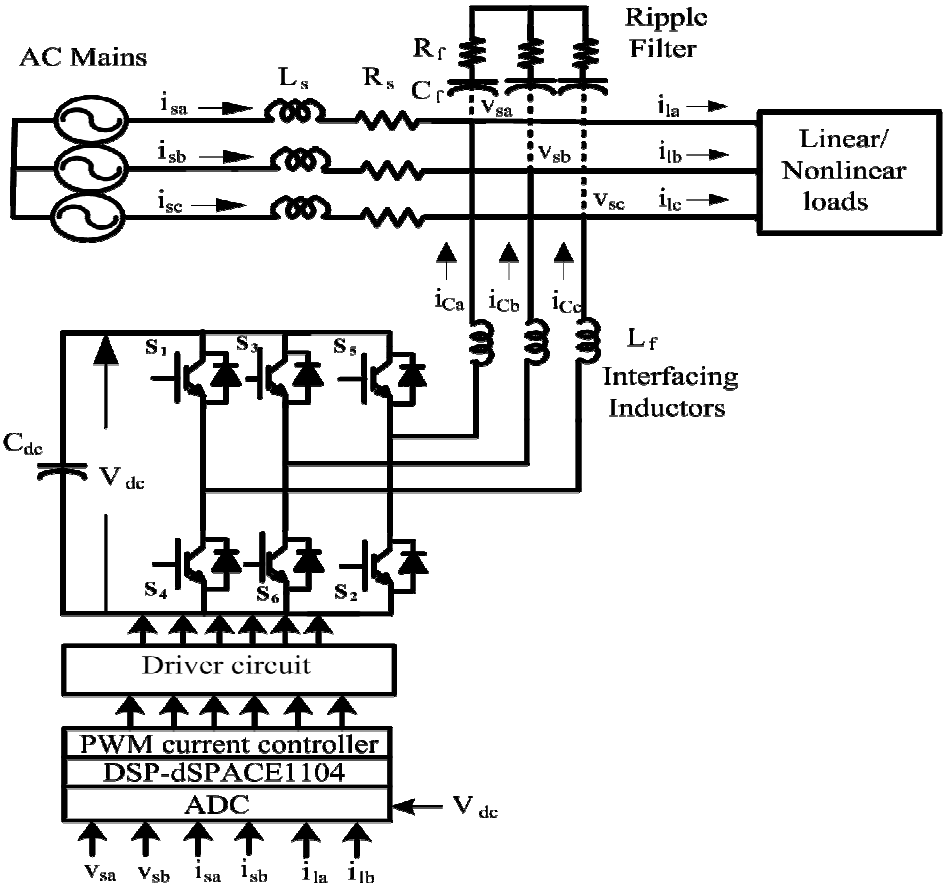


Fig. 7.1 Schematic diagram of the DSTATCOM

bus voltage (V_{dc}) are sensed and given to the controller. These signals are processed by the controller to generate appropriate switching pulses for the three phase VSC. A hardware prototype of the system is implemented in the laboratory using DSP-dSPACE 1104 R&D controller board. Hall Effect voltage and current sensors are used to sense real time signals. The design of sensor circuitry and various components of DSTATCOM are the same as given in section 3.6. Switching pulses generated by DSP are used to drive three phase VSC, which generates compensator currents.

7.3 BASIC PRINCIPLE AND MATHEMATICAL FORMULATION OF ARTIFICIAL INTELLIGENCE BASED CONTROL ALGORITHMS

This section deals with the basic principle and mathematical formulation of artificial intelligence based control algorithms developed for control of DSTATCOM. The control algorithms

presented under this category are based on adaptive neuro fuzzy inference system (ANFIS), real time recurrent learning (RTRL) and adaptive neuro fuzzy inference system-least mean square (ANFIS-LMS). These control algorithms are used to estimate the fundamental active and reactive power components of reference supply currents from the distorted load currents. The DSTATCOM controlled using artificial intelligence based techniques is used to mitigate several power quality problems such as harmonics current elimination, reactive power compensation and load balancing in power factor correction (PFC) and voltage regulation modes.

7.3.1 Adaptive Neuro Fuzzy Inference System Based Control Algorithm for DSTATCOM [179-185]

The design and implementation of a DSTATCOM based on adaptive neuro fuzzy inference system (ANFIS) based controller is presented in this section. Self-sustained DC bus voltage and PCC voltage magnitude are regulated by ANFIS controller. Active and reactive power fundamental components of load currents are extracted using i_d-i_q theory. This section is divided into three parts, the first part presents the development of ANFIS controller, the second part presents learning algorithm for ANFIS architecture and the third part deals with the generation of switching pulses for three phase VSC used as DSTATCOM. Detailed mathematical formulation of the control algorithm is given as follows.

7.3.1.1 Design of Adaptive Neuro-Fuzzy Inference Based Controller

Fig. 7.2(a) shows the block diagram of ANFIS based algorithm for control of DSTATCOM. Neural networks are good for recognizing pattern, but may not be too good at explaining how they reach their decisions. However, fuzzy logic provides high-level cognitive features as it can deal with issues such as approximate reasoning and neural language processing. Neural networks and fuzzy logic are complementary of each other and their combination provides the benefits of

both the techniques. Both of them make an adaptive network known as adaptive network based fuzzy inference system (ANFIS). The structure of ANFIS with 2-input, 3-MFs (associated with each input) and 9-rules is shown in Fig. 7.2(b). This figure shows square and circle nodes, which are used to reflect different adaptive capabilities. A first order Sugeno-type fuzzy system is used for ANFIS controller. The structure of ANFIS is shown in Fig. 7.2(b) and fuzzy membership functions are shown in Fig. 7.2(c). The node function of each layer is described as follows.

Layer1: Two inputs are assigned to this layer: one is error (V_{dc}^{*}-V_{dc}) and the other input is the

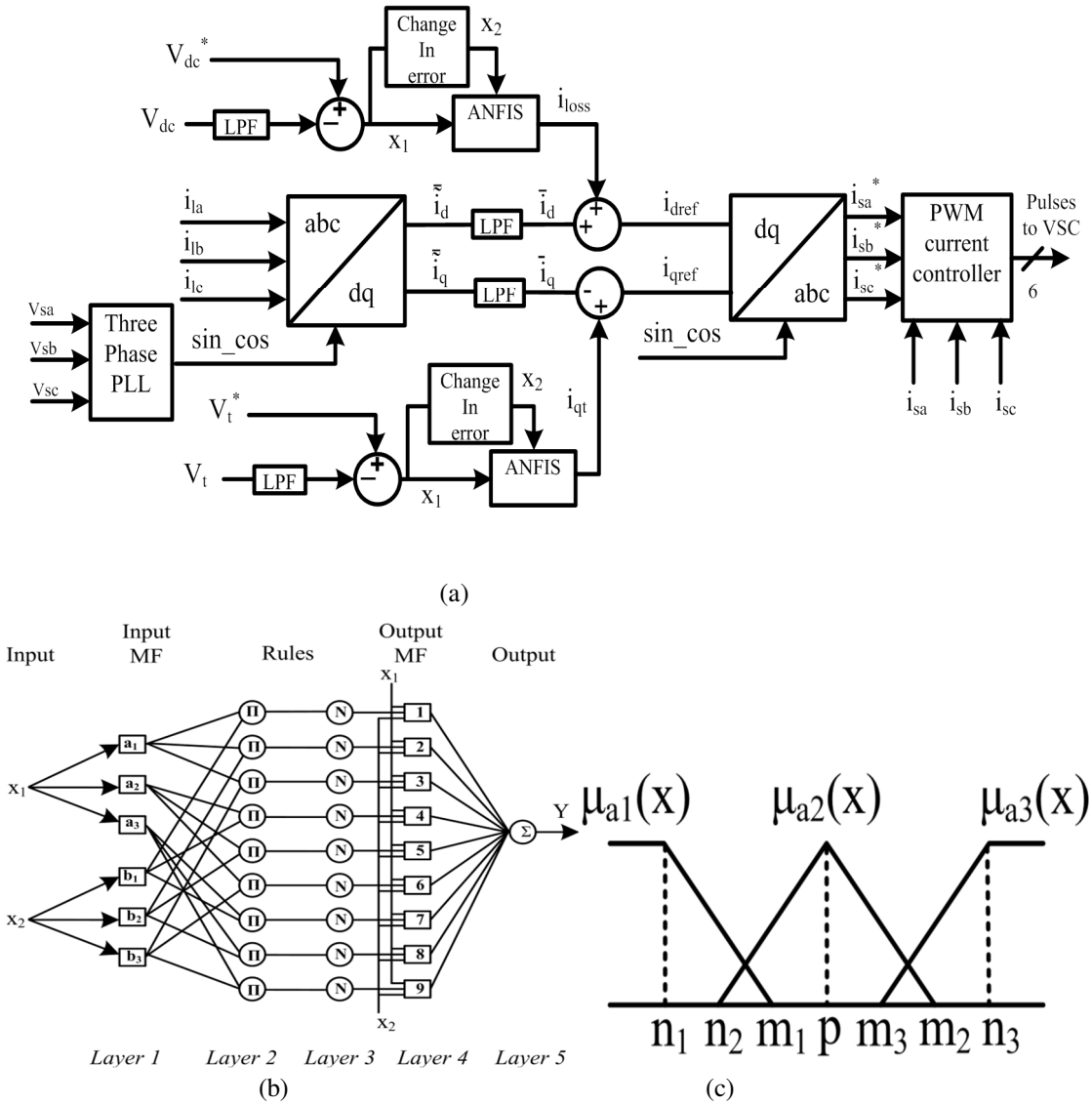


Fig. 7.2 ANFIS based control algorithm (a) Block diagram (b) ANFIS structure (c) Fuzzy rules

change in error denoted by x_1 and x_2 respectively. This layer is known as fuzzyfication layer. The corresponding node equations for the three membership functions (MFs) are given as follows.

$$\mu_{a1}(x) = \begin{cases} 0, & x > m_1 \\ \frac{m_1 - x}{m_1 - n_1}, & n_1 \le x \le m_1 \\ 1, & x < n_1 \end{cases} \tag{7.1}$$

$$\mu_{a2}(x) = \begin{cases} 0, & x \le m_1 \\ \frac{x - n_2}{p - n_2}, & n_2 < x \le p \\ \frac{m_2 - x}{m_2 - p}, & p < x < m_2 \\ 0, & x \ge m_2 \end{cases} \tag{7.2}$$

$$\mu_{a3}(x) = \begin{cases} 0, & x < m_1 \\ \frac{x - m_3}{n_3 - m_3}, & m_3 \le x \le n_3 \\ 1, & x > n_3 \end{cases} \tag{7.3}$$

There are three membership functions (MFs) corresponding to each input and each MF is represented by a square bracket. The trapezoidal and triangular MFs are used where $\{m_i, n_i\}$ is the parameter set, and i=1,2,3.

These parameters change with the variation in error and this generates the linguistic value of each membership function.

Layer 2: In this layer, every node is fixed and labeled as Π. It multiplies the input signal and forwards the product as output,

$$w_k = \mu_{ai}(x_1) * \mu_{bi}(x_2) \tag{7.4}$$

where i=1,2,3 and k=1,2,3,….,9.

The **o**utput of each node represents the firing strength.

Layer 3: Each node in this layer is fixed node labeled N. This layer normalized degree of activation of rules.

$$\bar{w}_k = \frac{w_k}{w_1+w_2+\cdots+w_9} \tag{7.5}$$

where k=1,2,3,…,9.

The output of each layer is called normalized weight.

Layer 4: Each node of this layer is a square node with node function given as,

$$O_k = \bar{w}_k . f_i = \bar{w}_k . (p_i . x_1 + q_i . x_2 + r_i) \tag{7.6}$$

where k=1,2,3..9 and i=1,2,3.

where quantity $\bar{w}_k$ is the output of layer 3 and $\{p_i, q_i$ and $r_i\}$ is a parameter set. Parameters in this layer are also referred as consequent parameters.

Layer 5: This is the output neuron and it contains a single circled neuron labeled Σ. This neuron computes the output as summation of all incoming signals as,

$$Y = \sum_{k=1}^{9} \bar{w}_k f_k \tag{7.7}$$

where Y represents the current component of the grid required to regulate the DC bus voltage and feeds loss component of VSC (i_{loss}).

7.3.1.2 Learning Algorithm for ANFIS Architecture

The learning of ANFIS is carried out using hybrid learning algorithm. This algorithm is the combination of gradient descent and least square error (LSE) method, and used to identify parameters as,

$$w_k = \mu_{a_1 i_1}(x_1) \times \mu_{a_2 i_2}(x_2) \times \ldots \times \mu_{a_n i_n}(x_n) \tag{7.8}$$

where $k_j \epsilon(1,2\ldots.MF_j)$, j=1,2…n; MF_1,MF_2…MF_n are membership functions for n input ANFIS structure, $\mu_{a_j i_j}$ is the value of the i_j^{th} membership function, w_k is the firing of k^{th} rule and MF_j is the number of membership function for the j^{th} input given as,

$$f_k = \sum_{j=1}^{n} a_j^i x_j + b^i \tag{7.9}$$

where i=1,2….R.

This is the ANFIS structure with R rules, where a_j^i,b^i denote the linear parameters of the i_{th}, rule.

The output of ANFIS can be expressed as,

$$Y = \frac{\sum_{i=1}^{R} w_i f_i}{\sum_{i=1}^{R} w_i} \tag{7.10}$$

The objective function of the system is defined as,

$$E(k) = Y_d(k) - Y(k) \tag{7.11}$$

where $Y_d(k)$and $Y(k)$ are the desired output and controller output respectively.

The input vector is given as,

$$\vec{X}(k) = [x_1(k), x_2(k), \dots, x_n(k), 1]^T \tag{7.12}$$

The weights are defined by R*(n+1) matrix as,

$$A = \begin{bmatrix} a_1^1 a_2^1 \dots a_n^1 b^1 \\ a_1^2 a_2^2 \dots a_n^2 \; b^2 \\ \vdots \\ a_1^R a_2^R \dots a_n^R \; b^R \end{bmatrix} \tag{7.13}$$

The output vector is (n×1) and can be given as,

$$Y = \begin{bmatrix} Y_1 \\ \vdots \\ Y_n \end{bmatrix}$$

The output Eqn. (7.10) can be written as,

$$Y = A\vec{X} \tag{7.14}$$

The squared error $\left\| A\vec{X} - Y \right\|^2$ in Eqn. (7.14) is minimized when $\vec{X} = \vec{X}^*$, called least square estimator (LSE) , which satisfy the normal equation given as,

$$\vec{X}^* = (A^T A)^{-1} AY \tag{7.15}$$

where A^T is the transpose of A and $(A^T A)^{-1}$ is the pseudo-inverse of A if A^T is non-singular matrix.

In a given feed forward adaptive network, it is assumed that if it has L number of layers and kth layer has N(k) nodes, then the node function (or node output) of node 'n' in k^{th} layer can be given as,

$$Y_{k,n} = f_{k,n}\left(Y_{k-1,1} \dots Y_{k-1,N(k-1)}, a, b, c \dots\right) \tag{7.16}$$

where a,b,c are the parameters of k^{th}node. Here, it is assumed that the training data set has P entries, an error measure can be defined for the $p^{th}(1 \leq p \leq P)$ entry of the training data set as the sum of the square of the error is given as,

$$E_p = \sum_{i=1}^{N(L)}\left(d_i - Y_{L,i}\right)^2 \tag{7.17}$$

where quantity d_i denotes the i^{th} component of the p^{th} output vector and $Y_{L,i}$ is i^{th} component of the real output vector, which is formed by representing p^{th} input vector in the network. The overall measured error is $E = \sum_{p=1}^{P} E_p$ and the purpose here is to minimize E. Developing a learning procedure for implementing gradient descent in overall error E minimization requires the error rate to be calculated as,

$$e_{l,k} = \frac{\partial E_p}{\partial Y_{l,k}} \tag{7.18}$$

for the i^{th} output node at layer l,

and $e_{l,k} = -2\left(d_k - Y_{l,k}\right)$

The error signal can be derived iteratively, for the internal node at the ith position of layer l, by using the chain rule as,

$$\frac{\partial E_p}{\partial Y_{l,k}} = \sum_{q=1}^{N(l+1)} \frac{\partial E_p}{\partial Y_{l+1,k}} \cdot \frac{\partial f_{l+1,q}}{\partial Y_{l,k}} = \sum_{q=1}^{N(l+1)} e_{l+1,q} \cdot \frac{\partial f_{l+1,q}}{\partial Y_{l,k}} \tag{7.19}$$

If α is parameter of the k^{th} node at layer l, it is given as,

$$\frac{\partial E_p}{\partial \alpha} = \frac{\partial E_p}{\partial Y_{l,k}} . \frac{\partial f_{l,k}}{\partial \alpha} = e_{l,k} . \frac{\partial f_{l,k}}{\partial \alpha} \tag{7.20}$$

The derivative of E with respect to α can be given as,

$$\frac{\partial E_p}{\partial \alpha} = \sum_{p=1}^{P} \frac{\partial E_p}{\partial \alpha} \tag{7.21}$$

Thus, the equation of updation of generic parameter α is given as,

$$\Delta\alpha = -\eta \frac{\partial E_p}{\partial \alpha} \tag{7.22}$$

where η is learning rate. For the parameter α it may be written as,

$$\alpha_{new} = \alpha_{old} + \Delta\alpha = \alpha_{old} - \eta \frac{\partial E_p}{\partial \alpha} \tag{7.23}$$

In this type of learning, update occurs only after the entire set of training data pair is presented. If S is total set of parameters, S_1 and S_2 are set of premise and consequent parameters respectively. In hybrid learning algorithm, each set of training data pair consists of forward pass and backward pass. In forward pass, where S_1 is unchanged and S_2 is computed using LSE. In this, the node outputs of the network are computed layer by layer. This process is continued till the corresponding row in the matrices A and Y of Eqn. (7.14) is obtained and it is repeated to form the complete matrix. After obtaining the matrix the output parameters of consequent parameter set S_2 are computed using Eqn. (7.15).

The error and the derivative of error with respect to each node of the output are calculated by Eqn. (7.18) and Eqn. (7.19). These error signals circulate from the output end towards the input end, in backward pass and the gradient vector is achieved for each training data entry. At the end for all data pairs, updating of the input parameters is shown by Eqn. (7.23).

7.3.1.3 Generation of Reference Supply Currents and Switching Pulses

The control algorithm for three-phase VSC is developed using d-q theory as shown in Fig. 7.2. Three phase load currents (i_{la}, i_{lb} and i_{lc}), supply currents (i_{sa}, i_{sb} and i_{sc}) and PCC voltages (v_{sa}, v_{sb} and v_{sc}) are sensed using current and voltage sensors respectively. Load currents are converted from abc to dq0 components by the use of Park transformation equations which are given as,

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_{la} \\ i_{ib} \\ i_{ic} \end{bmatrix} \tag{7.24}$$

In the synchronously rotating frame, all the components of load current at fundamental frequency (ω) are transformed into DC quantity, given as,

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \cos \omega t & \sin \omega t \\ -\sin \omega t & \cos \omega t \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{7.25}$$

The DC components of active load current (i_d) contain DC as well as some harmonic components as shown in Eqn. (7.26). Filtering of these harmonic components has been done by low pass filter (LPF).

$$i_d = \bar{i_d} + \tilde{i_d} \tag{7.26}$$

The control algorithm is developed in such a way that supply must deliver DC component of load current ($\bar{i_d}$) and active power component of current for maintaining DC bus voltage and meeting the losses (i_{loss}). The active power component of current 'i_{loss}' is obtained from the output of ANFIS controller. The reference component of currents (i_d^*) are computed from Eqn. (7.27) as,

$$i_d^* = \bar{i_d} + i_{loss} \tag{7.27}$$

The amplitude terminal voltage (V_t) at PCC is calculated as,

$$V_t = \sqrt{\frac{2}{3}\,(v_{sa}^2 + v_{sb}^2 + v_{sc}^2)} \tag{7.28}$$

The error and change in error between reference terminal PCC voltage (V_t^*) and actual terminal PCC voltage (V_t) are evaluated and passed through ANFIS controller to generate reactive component of current (i_{qt}) for voltage regulation. The reference quadrature component is given as,

$$i_q^* = i_{qt} - \bar{i_q} \tag{7.29}$$

At fundamental frequency, the active reference components of current(i_d^*) is easily converted to αβ components using Eqn. (7.30), which can then be easily converted into reference supply currents (i_{sa}^*, $i_{sb}^*$and i_{sc}^*) by reverse Clark transformation as,

$$\begin{bmatrix} i_\alpha^* \\ i_\beta^* \end{bmatrix} = \begin{bmatrix} \cos\omega t & -\sin\omega t \\ \sin\omega t & \cos\omega t \end{bmatrix} \begin{bmatrix} i_d^* \\ i_q^* \end{bmatrix} \tag{7.30}$$

$$\begin{bmatrix} i_{sa}^* \\ i_{sb}^* \\ i_{sc}^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_\alpha^* \\ i_\beta^* \end{bmatrix} \tag{7.31}$$

These reference supply currents (i_{sa}^*, i_{sb}^*andi_{sc}^*) are compared with the sensed supply currents (i_{sa}, i_{sb} and i_{sc}) and errors are achieved. These errors are then passed through PWM current controller for generation of six switching pulses for VSC.

7.3.2 Real Time Recurrent Learning Based Control Algorithm [186-190]

The recurrent neural network (RNN) uses feedback from the output layer to the previous layer, and is often defined as feedback network. In this case, the output of a neuron depends not only on the current input signals, but also on the previous inputs. This kind of network comprises internal memory and due to this, it behaves like a dynamic network. The learning technique of recurrent neural network is based on real time recurrent learning (RTRL). In this section, this learning RTRL method is applied for the control of DSTATCOM. This is a forward gradient learning method, because gradient information at some instant is forward propagated. In the

RTRL algorithm, there is no need to collect data over a period of time and hence the model learning is performed in real time. Mathematical analysis and formulation of the control algorithm are given as follows.

7.3.2.1 Estimation of Fundamental Active Power Component of Reference Supply Currents

Fig. 7.3 shows block diagram of RTRL based control algorithm for control of DSTATCOM. The phase voltages (v_{sa}, v_{sb} and v_{sc}) at PCC is sensed and amplitude is estimated as,

$$V_t = \sqrt{\frac{2}{3}\left(v_{sa}^2 + v_{sb}^2 + v_{sc}^2\right)} \tag{7.32}$$

The in-phase unit templates (u_{pa}, u_{pb} and u_{pc}) are estimated from the sensed PCC voltages and the amplitude of the PCC voltage (V_t) and given as,

$$u_{pa} = \frac{v_{sa}}{V_t}, u_{pb} = \frac{v_{sb}}{V_t} \text{ and } u_{pc} = \frac{v_{sc}}{V_t} \tag{7.33}$$

The voltage at DC bus (V_{dc}) is sensed and compared with reference DC bus voltage (V_{dc}^*), thus the voltage error at nth sampling instant is computed as,

$$v_{de}(n) = V_{dc}^*(n) - V_{dc}(n) \tag{7.34}$$

The voltage error $v_{de}(n)$, is then processed through a proportional integrator (PI) controller. The output of the PI controller is used to provide sufficient current component for regulating DC bus voltage and to meet DSTATCOM system losses. The output of PI controller at n^{th} sampling instant is given as,

$$w_{pdc}(n) = w_{pdc}(n-1) + k_{pd}\left\{v_{de}(n) - v_{de}(n-1)\right\} + k_{id}v_{de}(n) \tag{7.35}$$

where k_{pd} and k_{id} are the proportional and integrator gains of PI controller for regulating DC bus voltage.

The RTRL based control technique is used to extract weights corresponding to fundamental active power component of load current for the three phases. A single neuron based network is considered to estimate the weighted value of load active power current component. Consider the input vector *x(n)* at sampling time '*n*' and output vector *y(n+1)* at sampling time '*n+1*', the forward response of the network is given as,

$$y(n+1) = f\left(s(n+1)\right) \tag{7.36}$$

where *s(n+1)* represents the input to the neuron and given as,

$$s(n+1) = \omega x(n) + g y(n) \tag{7.37}$$

where ω and g are parametric weights corresponding to input vector *x(n)* and feedback from output *y(n)* to the neuron respectively. The neuron has nonlinear activation function such as sigmoid activation function given as,

$$y(n+1) = f\left(s(n+1)\right) = \frac{1}{1+e^{-s(n+1)}} \tag{7.38}$$

The output *y(n+1)* is the estimated quantity of phase 'a' of load current i_{esta}, which is

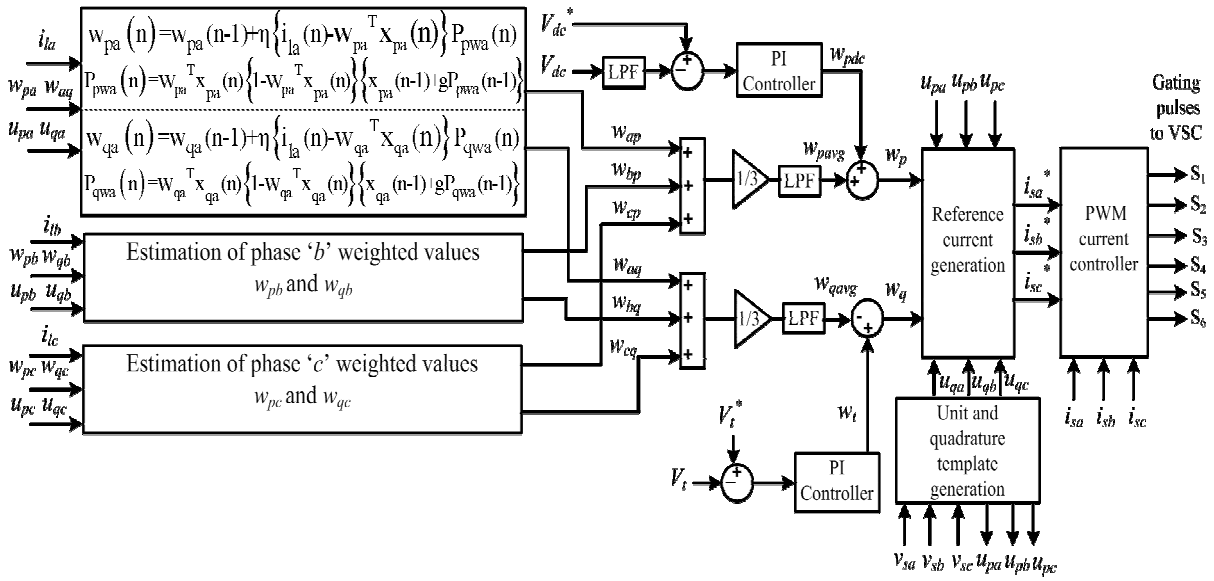


Fig. 7.3 Block diagram of RTRL based control algorithm

fundamental power component of load current. The i_{esta} component of load current is estimated from the actual or desired quantity of phase 'a' of load current $y_d(n+1)$, which also can be represented as i_{la}. The cost function $E(n+1)$ is a quadratic function of instantaneous error, which is defined as,

$$E(n+1)=\frac{1}{2}\left(i_{la}(n+1)-i_{esta}(n+1)\right)^2 \tag{7.39}$$

The network parametric weights ω and g, can be defined using gradient-descent algorithm such as,

$$\omega(n+1)=\omega(n)-\eta\frac{\partial E(n+1)}{\partial \omega} \tag{7.40}$$

$$g(n+1)=g(n)-\eta\frac{\partial E(n+1)}{\partial g} \tag{7.41}$$

Differentiating E w.r.t synaptic weight vector ω as,

$$\frac{\partial E(n+1)}{\partial \omega}=-\left[i_{la}(n+1)-i_{esta}(n+1)\right]\frac{\partial y(n+1)}{\partial \omega} \tag{7.42}$$

Here the variable $P_\omega(n+1)$ is defined as, $P_\omega(n+1)=\frac{\partial i_{esta}(n+1)}{\partial \omega}$ which is known as the sensitivity element which is known as the sensitivity element and initialized as $P_\omega(0)=0$.

$$P_\omega(n+1)=\frac{\partial i_{esta}(n+1)}{\partial \omega}=\frac{\partial i_{esta}(n+1)}{\partial s(n+1)}\times\frac{\partial s(n+1)}{\partial \omega} \tag{7.43}$$

Since $i_{esta}(n+1)=y(n+1)=\frac{1}{1+e^{-s(n+1)}}$, differentiating this results in,

$$\frac{\partial y(n+1)}{\partial s(n+1)}=i_{esta}(n+1)\{1-i_{esta}(n+1)\} \tag{7.44}$$

Again, $\frac{\partial s(n+1)}{\partial \omega}=\frac{\partial}{\partial \omega}\{\omega x(n)+gi_{esta}(n)\}$

$$\frac{\partial s(n+1)}{\partial \omega} = x(n) + g\frac{\partial i_{esta}(n)}{\partial \omega} = x(n) + gP_{\omega}(n) \tag{7.45}$$

Now using the value of Eqn. (7.44) and Eqn. (7.45) in Eqn. (7.43), the value of $P_{\omega}(n+1)$ is given as,

$$P_{\omega}(n+1) = i_{esta}(n+1)\{1 - i_{esta}(n+1)\}\{x(n) + gP_{\omega}(n)\} \tag{7.46}$$

From Eqn. (7.46) it is observed that by computing the gradient information at sampling time '*n*', it is easy to compute gradient information at sampling time '*n+1*'. This is the basic ideology of real time recurrent networks.

Similarly the variable for feedback layer is given as,

$$P_{g}(n+1) = i_{esta}(n+1)\{1 - i_{esta}(n+1)\}\{x(n) + gP_{g}(n)\} \tag{7.47}$$

The weight update rule for RTRL is given as,

$$\omega(n+1) = \omega(n) + \eta\{i_{la}(n+1) - i_{esta}(n+1)\}P_{\omega}(n+1) \tag{7.48}$$

$$g(n+1) = g(n) + \eta\{i_{la}(n+1) - i_{esta}(n+1)\}P_{g}(n+1) \tag{7.49}$$

The value of $P_{\omega}(n+1)$ and $P_{g}(n+1)$ are computed from Eqn. (7.46) and Eqn. (7.47) respectively. The extracted weighted values (w_{ap}, w_{bp} and w_{cp}) corresponding to active power components of load currents are computed from Eqn. (7.48). The average of active power component (w_{pavg}) of load weighted values is estimated using Eqn. (7.50)

$$w_{pavg} = \frac{w_{ap} + w_{bp} + w_{cp}}{3} \tag{7.50}$$

The output of DC bus PI controller (w_{pdc}) is added to the average value of active power weight (w_{pavg}) and the reference active power weight (w_{p}) is computed as,

$$w_{p} = w_{pavg} + w_{pdc} \tag{7.51}$$

The reference supply currents (i_{pa}^*, i_{pb}^* and i_{pc}^*) corresponding to active power component are estimated from w_p and the inphase unit templates. The reference inphase current components (i_{pa}^*, i_{pb}^* and i_{pc}^*) are computed as,

$$i_{pa}^* = w_p u_{pa}\ ,\ i_{pb}^* = w_p u_{pb} \text{ and } i_{pc}^* = w_p u_{pc} \tag{7.52}$$

These active components of reference supply currents are used to generate reference supply currents.

7.3.2.2 Estimation of Fundamental Reactive Power Component of Reference Supply Currents

The quadrature unit templates of three phase PCC voltage (u_{qa}, u_{qb} and u_{qc}) are estimated from inphase unit templates (u_{pa}, u_{pb} and u_{pc}) given in Eqn. (7.33) as,

$$u_{qa} = \frac{(-u_{pb} + u_{cp})}{\sqrt{3}}\ ,\ u_{qb} = \frac{(3u_{pa} + u_{pb} - u_{pc})}{2\sqrt{3}} \text{ and } u_{qb} = \frac{(-3u_{pa} + u_{pb} - u_{pc})}{2\sqrt{3}} \tag{7.53}$$

The estimated amplitude of PCC voltage (V_t) is compared with reference amplitude (V_t^*) and thus voltage error (v_{te}) is computed as,

$$v_{te}(n) = V_t^*(n) - V_t(n) \tag{7.54}$$

The error value is passed through a PI controller and the output of AC bus PI controller (w_t) at n^{th} sampling instant is given as,

$$w_t(n) = w_{qd}(n-1) + k_{pq}\{v_{te}(n) - v_{te}(n-1)\} + k_{iq} v_{te}(n) \tag{7.55}$$

Now the weighted values (w_{aq}, w_{bq} and w_{cq}) corresponding to reactive power component of load currents are calculated from RTRL control technique. The average weighted value (w_{qavg}) corresponding to reactive power weights is calculated as,

$$w_{qavg} = \frac{w_{aq} + w_{bq} + w_{cq}}{3} \tag{7.56}$$

The value of average reactive power weight (w_{qavg}) is subtracted from the output of AC bus PI controller (w_t) and the reference reactive power weight (w_q) is computed as,

$$w_q = w_t - w_{qavg} \tag{7.57}$$

The quadrature reference supply currents (i_{qa}^*, i_{qb}^* and i_{qc}^*) are estimated from quadrature unit templates and reference reactive power weight w_q such as,

$$i_{qa}^* = w_q u_{qa},\ i_{qb}^* = w_q u_{qb} \text{ and } i_{qc}^* = w_q u_{qc} \tag{7.58}$$

These reactive power components of reference currents are added to the active power components of reference supply currents to achieve reference supply currents as discussed below.

7.3.2.3 Generation of Reference Supply Currents and Switching Pulses

The reference supply currents (i_{sa}^*, i_{sb}^* and i_{sc}^*) are generated by adding the active and reactive components of reference supply currents given by Eqn. (7.52) and Eqn. (7.58) such as,

$$i_{sa}^* = i_{pa}^* + i_{qa}^*,\ i_{sb}^* = i_{pb}^* + i_{qb}^* \text{ and } i_{sc}^* = i_{pc}^* + i_{qc}^* \tag{7.59}$$

The actual supply currents (i_{sa}, i_{sb} and i_{sc}) are sensed and compared with the reference supply current (i_{sa}^*, i_{sb}^* and i_{sc}^*) to generate current errors (i_{sae}, i_{sbe} and i_{sce}). These current errors are passed through pulse width modulation (PWM) current controller to generate switching pulses for the three phase VSC.

7.3.3 Adaptive Neuro Fuzzy Inference System Least Mean Square (ANFIS-LMS) Based Control Algorithm [191-193]

This section deals with adaptive least mean square (LMS) technique, in which the step size parameter is updated using adaptive neuro fuzzy inference system (ANFIS). An adaptive neuro fuzzy inference system least mean square (ANFIS-LMS) based control algorithm is developed and its mathematical formulation is presented in this section. The proposed control algorithm is

used for the control of DSTATCOM and has the ability to improve various aspects of power quality such as harmonics compensation, voltage regulation, power factor correction and load balancing in PFC and voltage regulation modes.

7.3.3.1 Estimation of Fundamental Active Power Components of Reference Supply Currents

Fig. 7.4 shows the block diagram of ANFIS-LMS based control algorithm. Amplitude (V_t) of PCC voltages (v_{sa}, v_{sb} and v_{sc}) is calculated and it is given as,

$$V_t = \sqrt{2(v_{sa}^2 + v_{sb}^2 + v_{sc}^2)/3} \tag{7.60}$$

Unit in-phase templates (u_{pa}, u_{pb} and u_{pc}) are calculated by PCC voltages (v_{sa}, v_{sb} and v_{sc}) and their amplitude (V_t) is calculated in a similar manner as given in section 7.3.2(A). The voltage at DC bus (V_{dc}) is sensed and compared with reference DC bus voltage (V_{dc}^*), which gives an error (v_{de}). This error is passed through PI controller and its output is (w_{pdc}) which is already described in section 7.3.2(A).

The weight values corresponding to active power components of load currents are calculated using ANFIS-LMS based control technique. The weight updation rule of this control algorithm at n^{th} sampling instant is given as,

$$w(n+1) = w(n) + 2\mu(n)e(n)x(n) \tag{7.61}$$

where e(n) is error between actual (i_l) and estimated ($w^T x(n)$) load current, x(n) is input vector which consists of unit inphase templates (u_{pa}, u_{pb} and u_{pc}), w(n) is weight vector and μ(n) is the step size parameter calculated using the ANFIS controller.

The structure of ANFIS is developed with two inputs, three membership functions (MFs) and nine rules are same as shown in Fig 7.2(b). This represents both square and circular nodes, to identify different adaptive capabilities. The ANFIS structure uses first order Sugeno type fuzzy inference system. The function of each layer of ANFIS structure is given as follows.

Layer 1: This is the fuzzification layer, having two inputs. One input of this layer is error (x_1=e(n)) between actual and estimated value of load current ($i_l(n) - w^T x(n)$) and other input is the change in error (x_2=Δe(n)). Each input function corresponds to three MFs and the shape of MFs is represented as square bracket. The internal structure of each square bracket represents trapezoidal and triangular MFs. Equations related to each MFs are given as,

$$\mu_{a1}(x_1) = \mu_{b1}(x_2) = \begin{cases} 0, & x > m_1 \\ \frac{m_1 - x}{m_1 - n_1}, & n_1 \le x \le m_1 \\ 1, & x < n_1 \end{cases} \tag{7.62}$$

$$\mu_{a2}(x_1) = \mu_{b2}(x_2) = \begin{cases} 0, & x \le m_1 \\ \frac{x - n_2}{p - n_2}, & n_2 < x \le p \\ \frac{m_2 - x}{m_2 - p}, & p < x < m_2 \\ 0, & x \ge m_2 \end{cases} \tag{7.63}$$

$$\mu_{a3}(x_1) = \mu_{b3}(x_2) = \begin{cases} 0, & x < m_1 \\ \frac{x - m_3}{n_3 - m_3}, & m_3 \le x \le n_3 \\ 1, & x > n_3 \end{cases} \tag{7.64}$$

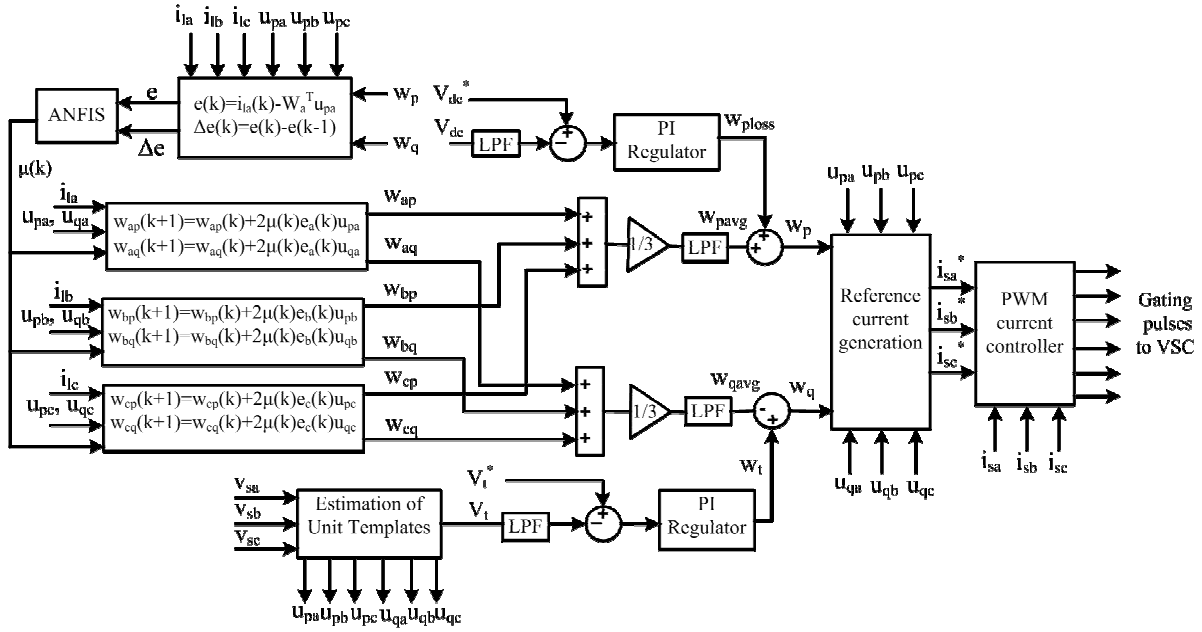


Fig. 7.4 Block diagram of ANFIS-LMS based control algorithm for DSTATCOM

where{m_i, n_i} are set of parameters, and value of i=1,2,3. The parameters {m_i, n_i} change with the change in value of error and correspondingly generate the linguistic value of each MF. These parameters are known as *premise* parameters.

Layer 2: This layer is known as implication layer and each node in this layer is fixed node. This layer represented as Π and the output of each node of this layer is multiplication of its input signals,

$$w_k = \mu_{aij}(x_1)\,\mu_{bij}(x_2) \tag{7.65}$$

where k=1,2,..9, i=1,2,3 and j=1, 2, 3. Each node in this layer represents firing strength of the rule.

Layer 3: Every node in this layer is also a fixed node and represented by N. This is also known as normalizing layer given as,

$$\overline{w}_k = \frac{w_k}{w_1+w_2+\cdots+w_9} \tag{7.66}$$

where k=1,2,….9 and output of each node in this layer is called the normalized firing strength.

Layer 4: This is known as defuzzifing layer and every node in this layer is adaptive. The nodes of this layer are represented by square shape and the node function is given as,

$$O_k = \overline{w}_k f_k = \overline{w}_k(p_k x_1 + q_k x_2 + r_k) \tag{7.67}$$

where p_k,q_k and r_k are the *consequence* parameters.

Layer 5: This is a single node layer represented by summation. The output of this layer represents the summation of the all input signals. The node function for this layer is given as,

$$Y = \sum_{k=1}^{9} \overline{w}_k f_k \tag{7.68}$$

The ANFIS LMS algorithm is used to compute the step size parameters μ(k), which is used to find optimum weight vector for LMS algorithm.

Learning of premise (m_i and n_i) and consequence parameters (p_k, q_k and r_k) in ANFIS structure is carried out with the hybrid learning algorithm, which is discussed in section 7.3.1. This uses least square and gradient descent methods to find consequent and premise parameters respectively. The ANFIS structure proposed here, uses forward pass and backward pass learning algorithm. Suppose S, S_1 and S_2 represent total set of parameters, set of premise parameters and set of consequent parameters respectively, then in the forward pass S_1 is unchanged and S_2 is computed using least square error algorithm. The forward pass presents the input vector and node output to this. It can be calculated layer by layer till the corresponding data is obtained and process is repeated. Once all data have been obtained, the value of consequence parameter set S_2 can be obtained and it also computes error signal for each training pair.

In the backward pass, S_2 is unchanged and parameters of S_1 are computed using gradient descent algorithm such as back-propagation. The error signal computed above propagates from output towards input end. The gradient vector is found for each training data entry and updating of input parameters is performed with gradient descent algorithm.

Active power weights (w_{ap}, w_{bp} and w_{cp}) corresponding to the load currents are extracted using Eqn. (7.61) and μ(n) calculated by ANFIS controller as,

$$w_{ap}(n+1) = w_{ap}(n) + 2\mu_a(n)e_a(n)u_{pa} \tag{7.69}$$

$$w_{bp}(n+1) = w_{bp}(n) + 2\mu_b(n)e_b(n)u_{pb} \tag{7.70}$$

$$w_{cp}(n+1) = w_{cp}(n) + 2\mu_c(n)e_c(n)u_{pc} \tag{7.71}$$

The average weight of active power weights (w_{ap}, w_{bp} and w_{cp}) is calculated as,

$$w_{pavg} = (w_{ap} + w_{bp} + w_{cp})/3 \tag{7.72}$$

This average weight (w_{pavg}) is added to the output of DC bus PI controller and reference active power weight (w_p) is calculated as,

$$w_p = w_{pavg} + w_{pdc} \tag{7.73}$$

Active power components of reference supply currents (i_{sa}, i_{sb} and i_{sc}) are estimated from the reference active power weight (w_p) and unit inphase templates (u_{pa}, u_{pb} and u_{pc}) as,

$$i_{pa}^* = w_p u_{pa},\ i_{pb}^* = w_p u_{pb} \text{ and } i_{pc}^* = w_p u_{pc} \tag{7.74}$$

These active power components of reference supply currents are used to calculate total reference supply currents.

7.3.3.2 Estimation of Fundamental Reactive Power Component of Reference Supply Currents

Unit quadrature templates (u_{qa}, u_{qb} and u_{qc}) of PCC voltages (v_{sa}, v_{sb} and v_{sc}) are calculated from unit inphase templates (u_{pa}, u_{pb} and u_{pc}) same as given in section 7.3.2(B). PCC voltage amplitude (V_t) is calculated from Eqn. (7.60) and compared with reference PCC voltage, consequently an error signal (v_{te}) is generated. This error signal is passed through a second PI controller which output is (w_t). The equations for the same are described in section 7.3.2(B).

Reactive power weights (w_{aq}, w_{bq} and w_{cq}) corresponding to load current are extracted from Eqn. (7.61) and μ(n) is computed from the ANFIS controller as,

$$w_{aq}(n+1) = w_{aq}(n) + 2\mu_a(n)e_a(n)u_{qa} \tag{7.75}$$

$$w_{bq}(n+1) = w_{bq}(n) + 2\mu_b(n)e_b(n)u_{qb} \tag{7.76}$$

$$w_{cq}(n+1) = w_{cq}(n) + 2\mu_c(n)e_c(n)u_{qc} \tag{7.77}$$

The average weight of the extracted reactive power weights (w_{aq}, w_{bq} and w_{cq}) is calculated as,

$$w_{qavg} = (w_{aq} + w_{bq} + w_{cq})/3 \tag{7.78}$$

This average weight (w_{qavg}) is subtracted with output of AC bus PI controller and reference reactive power weight (w_q) is calculated as,

$$w_q = w_t - w_{qavg} \tag{7.79}$$

The estimated reference reactive power components of currents are calculated from the reference reactive power weight (w_q) and unit quadrature templates as,

$$i_{qa}^{*} = w_q u_{qa},\ i_{qb}^{*} = w_q u_{qb} \text{ and } i_{qc}^{*} = w_q u_{qc} \quad (7.80)$$

The estimated active and reactive power components are added to generate total reference supply currents.

7.3.3.3 Generation of Reference Supply Currents and Switching Pulses

The summation of reference active and reactive power components of Eqn. (7.74) and Eqn. (7.80) are considered as reference currents (i_{sa}^{*}, i_{sb}^{*} and i_{sc}^{*}). These reference currents are compared with the sensed supply currents ($i_{sa}, i_{sb}$and i_{sc}) and current errors (i_{sae}, i_{sbe} and i_{sce}) are evaluated. These current errors are passed through pulse width modulation (PWM) current controller for the generation of switching pulses for three-phase VSC used as DSTATCOM.

7.4 MATLAB MODELING OF CONTROL ALGORITHMS BASED ON ARTIFICIAL INTELLIGENCE TECHNIQUES

Modeling of artificial intelligence techniques based control algorithms using MATLAB is presented here. The control algorithms discussed are based on adaptive neuro fuzzy inference system (ANFIS) controller, real time recurrent learning (RTRL) and adaptive neuro fuzzy inference system least mean square (ANFIS-LMS). The detailed discussion on MATLAB/SIMULINK models for these control algorithms are given as follows.

7.4.1 Adaptive Neuro Fuzzy Inference System Based Control Algorithm

Fig. 7.5 shows the simulation model of ANFIS based control algorithm using MATLAB in SIMULINK and Sim Power system (SPS) tool box. The ANFIS based controller is used for regulation of DC bus and PCC voltage amplitude to their reference values. Inputs to the DC bus

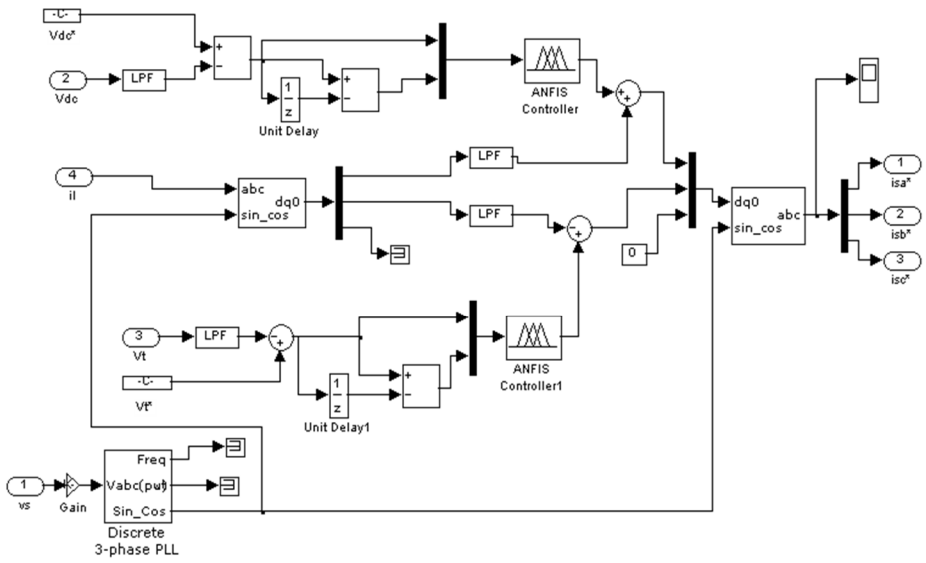


Fig. 7.5 Simulink model of ANFIS based control algorithm for DSTATCOM

ANFIS controller are error (e) and change in error (Δe) between reference DC bus voltage (V_{dc}*) and sensed DC bus voltage (V_{dc}). Similarly for the AC bus ANFIS controller, the inputs are the error and change in error between the reference PCC voltage magnitude (V_t^*) and calculated PCC voltage magnitude (V_t). The outputs of the ANFIS controllers are used along with the active-reactive (i_d-i_q) components of load currents, for the generation of reference supply currents.

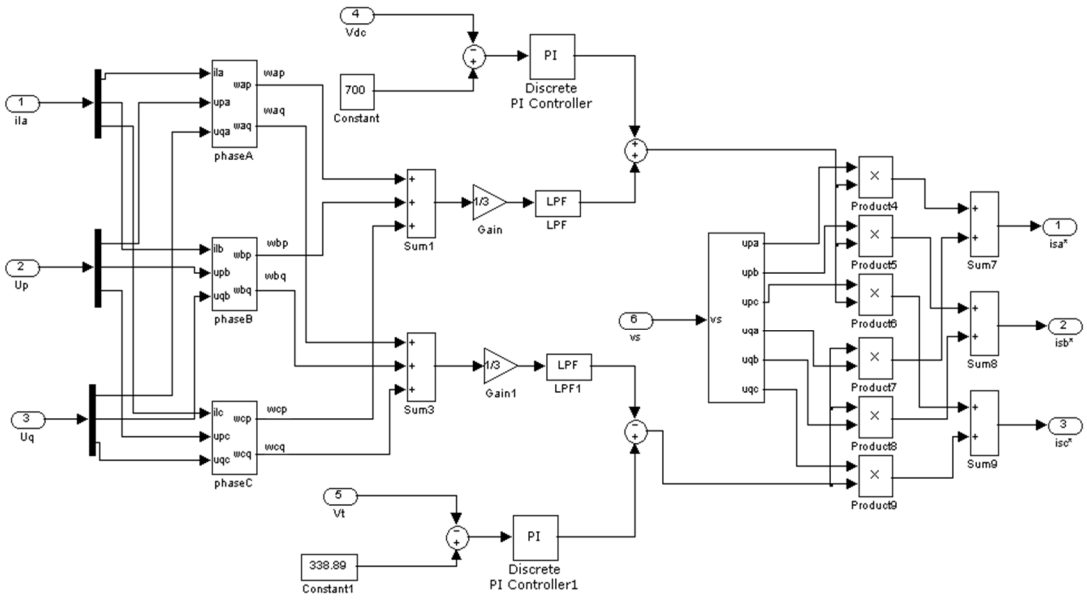
7.4.2 Real Time Recurrent Learning Based Control Algorithm

Fig. 7.6(a) shows the simulation model of real time recurrent learning (RTRL) based control algorithm developed in MATLAB using SIMULINK and SPS tool box. This control algorithm is used for generation of reference supply currents (i_{sa}^*, $i_{sb}^*$and i_{sc}^*) from distorted load currents. The inputs to the RTRL based control algorithms are PCC voltages (v_s), supply currents (i_{sa}, i_{sb} and i_{sc}), load currents (i_{la}, i_{lb} and i_{lc}) and self-sustained DC bus voltage (V_{dc}). The extraction of weights corresponding to the fundamental active and reactive power component of phase 'a' of load current using RTRL technique is shown in Fig. 7.6(b). In a similar manner the RTRL

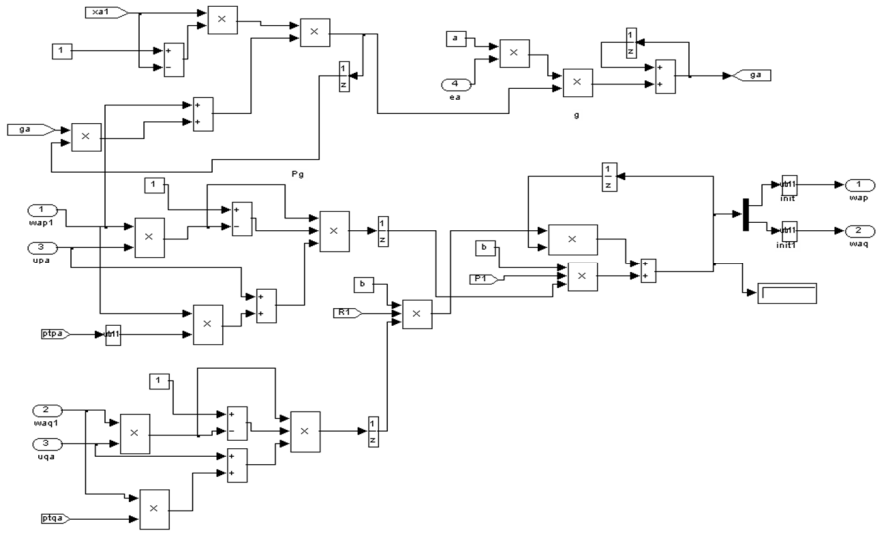
technique is used to extract active and reactive weights corresponding to phase ‘b’ and phase ‘c’ of load currents.

7.4.3 ANFIS-LMS Based Control Algorithm

The MATLAB/SIMULINK based model of ANFIS-LMS based control algorithm is developed



(a)



(b)

Fig. 7.6 Simulink model of (a) RTRL based control algorithm (b) RTRL technique for extraction of weights

using SPS tool box. Fig. 7.7 shows the developed simulation model of the control algorithm used for the generation of reference supply currents. The ANFIS controller is used to compute the step-size parameter (μ) for LMS technique. The inputs to the control algorithm as shown in SIMULINK model are PCC voltages (v_s), supply currents (i_{sa}, i_{sb} and i_{sc}), load currents (i_{la}, i_{lb} and i_{lc}) and self-sustained DC bus voltage (V_{dc}) used for control of DSTATCOM. The LMS technique with ANFIS controller is used to extract weight corresponding to active (w_{ap}, w_{bp} and w_{cp}) and reactive (w_{aq}, w_{bq} and w_{cq}) power components of load currents. The average weights (w_{pavg} and w_{qavg}) corresponding to active and reactive power weights are calculated and used with the output of DC and AC bus PI controller to estimate the reference supply currents.

7.5 DSP IMPLEMENTATION OF ARTIFICIAL INTELLIGENCE BASED CONTROL ALGORITHMS

This section presents an implementation of artificial intelligence based control techniques using

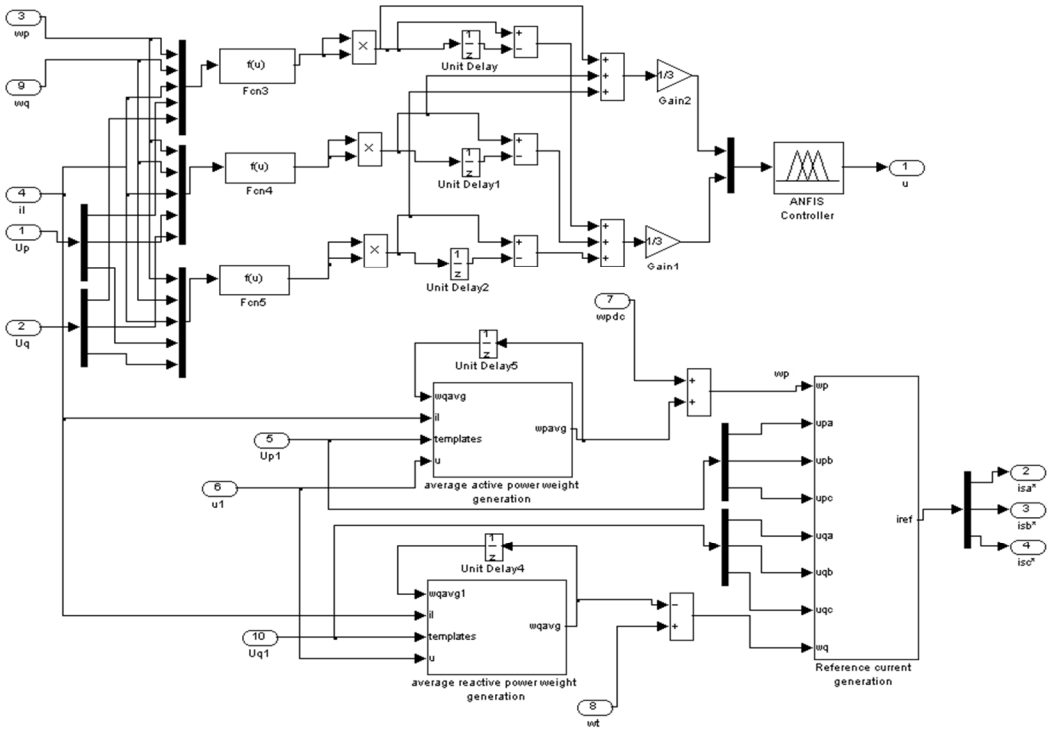


Fig. 7.7 Simulink model of ANFIS-LMS based control algorithm

DSP (dSPACE 1104 R&D Controller Board) for generation of the switching pulses for three phase VSC. The control techniques discussed under this category are based on adaptive neuro fuzzy inference system (ANFIS), real time recurrent learning (RTRL) and adaptive neuro fuzzy inference system least mean square (ANFIS-LMS). The detailed description of implementation on DSP of these control algorithms is given as follows.

7.5.1 Adaptive Neuro Fuzzy Inference System (ANFIS) Based Control Algorithm

The ANFIS based control algorithm is implemented using DSP (dSPACE 1104 R&D Controller Board) and is used to generate gating pulses for the three phase VSC based DSTATCOM. The DSP (dSPACE 1104) is real time controller based on a 603 PowerPC floating-point processor. This includes slave DSP subsystem based on the TMS320F240 DSP microcontroller. The DSP hardware and software have given the facility to generate real time switching pulses from real time signals with the use of SIMULINK model of the control algorithm. The implementation of DSTATCOM requires real time sensing of PCC voltages, supply currents, load currents and DC bus voltage. These signals are sensed from Hall Effect voltage and current sensors with appropriate buffer circuitry. The design and selection of DC bus capacitance, DC bus voltage, interfacing inductors, sensor circuitry and gating circuitry for hardware implementation of DSTATCOM are already discussed in section 3.6. The DSP based implementation of control algorithms for generating switching pulses for DSTATCOM, implementation of DC and AC bus PI controller along with pulse width modulation (PWM) switching using DS 1104SL_DSP_PWM3 block have been discussed in section 4.7.1. The sampling time (T_s) is selected 60μs for ANFIS based control algorithm.

7.5.2 Real Time Recurrent Learning (RTRL) Based Control Algorithm

The RTRL based control algorithm is implemented using DSP (dSPACE 1104 R&D Controller Board) and is used to generate gating pulses for the three phase VSC based DSTATCOM. The implementation of DSTATCOM requires real time sensing of PCC voltages, supply currents, load currents and DC bus voltage. These signals are sensed from Hall Effect voltage and current sensors with appropriate buffer circuitry and discussed in section 3.6. The DSP based implementation of control algorithm is presented in section 4.7.1. The sampling time (T_s) is selected 65μs for RTRL based control algorithm.The DC bus PI controller proportional and integral gains are calculated using Ziegler-Nichols unit step response algorithm. The selected value of PI controllers gains are tuned very close to the calculated values.

7.5.3 Adaptive Neuro Fuzzy Inference System Least Mean Square (ANFIS-LMS) Based Control Algorithm

The ANFIS-LMS based control algorithm is implemented using DSP (dSPACE 1104 R&D Controller Board) and is used to generate gating pulses for the three phase VSC. The implementation of DSTATCOM is carried out in a similar manner as discussed for the above two algorithms. The DSP (dSPACE 1104) based implementation of control algorithm is used for generating switching pulses for DSTATCOM. Implementation of pulse width modulation (PWM) switching in DSP (dSPACE 1104) using DS 1104SL_DSP_PWM3 block is already presented in section 4.7.1. The sampling time (T_s) is selected 60μs for ANFIS-LMS based control algorithm.

7.6 RESULTS AND DISCUSSION

The artificial intelligence based control algorithms presented in the previous section are developed using MATLAB using SIMULINK and SPS tool box. This section deals with performance of DSTATCOM with these control algorithms for mitigation of power quality

problems in PFC and voltage regulation modes. The simulation and test results for the three control algorithms are given as follows.

7.6.1 Performance of DSTATCOM With Adaptive Neuro Fuzzy Inference System (ANFIS) Based Control Algorithm

Simulation and experimental performance of DSTATCOM with ANFIS based control algorithm is presented here. The simulation results are taken in MATLAB/SIMULINK environment and presented for PFC and voltage regulation modes. The test results are obtained on the DSTATCOM prototype developed in the laboratory.

7.6.1.1 Simulated Performance of DSTATCOM in PFC and voltage regulation Modes

This section is divided into three parts. The first part deals with the performance of the ANFIS based control algorithm. The second and third parts present performance of DSTATCOM in PFC and voltage regulation modes.

A. Performance of ANFIS Based Control Algorithm in Voltage Regulation Mode Under Nonlinear Load

Fig. 7.8 shows the intermediate signals of ANFIS based control algorithm for DSTATCOM controlled in voltage regulation mode. This result shows the waveforms of PCC voltages (v_s), load currents (i_l), active DC component of load current (i_d), output of DC bus PI controller (i_{loss}), reference active DC current component (i_{dref}), amplitude of PCC voltage (V_t), output of AC bus PI controller (i_{qt}), reactive DC component of load current (i_q) and reference reactive DC current component (i_{qref}). These results are shown for steady state (before t=0.3s) and unbalanced load conditions (t=0.3s to t=0.4s) under nonlinear load. Satisfactory performance of the ANFIS based control algorithm is observed from these results.

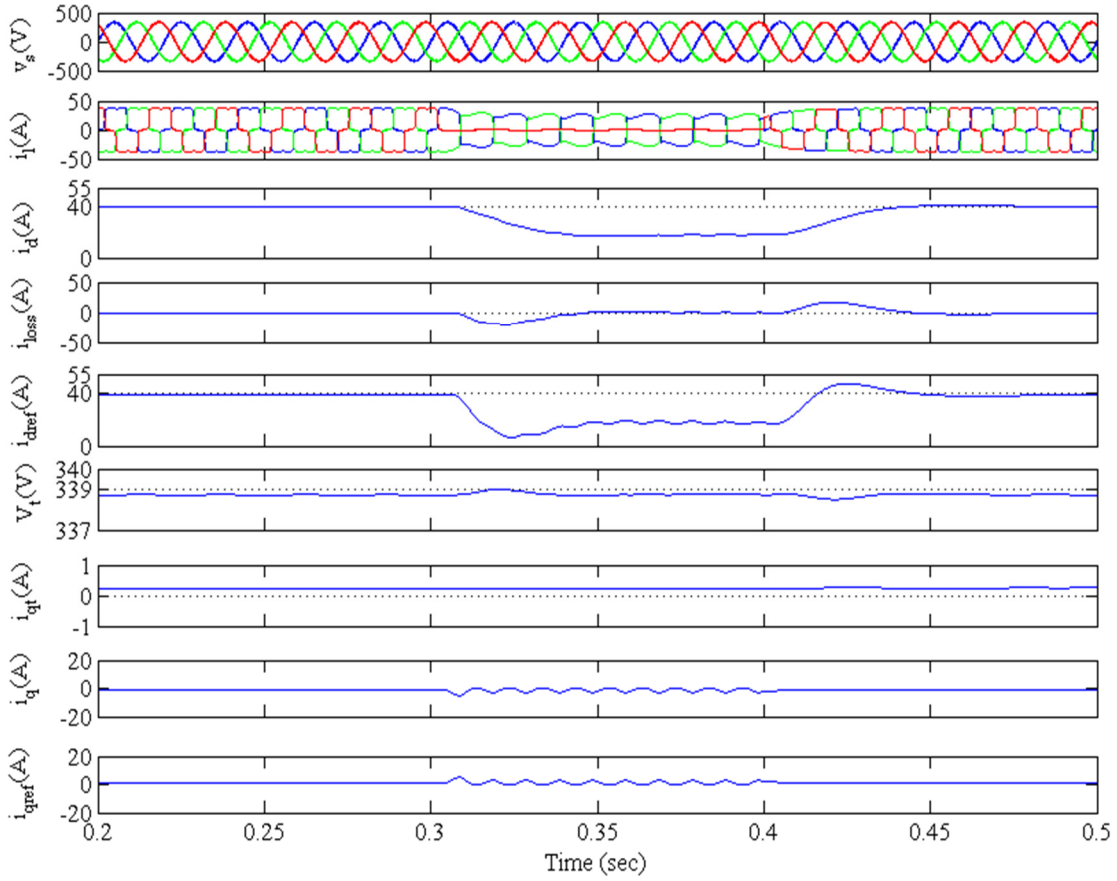


Fig. 7.8 Performance of ANFIS based control algorithm for DSTATCOM

B. Performance of DSTATCOM in PFC mode With ANFIS Based Control Algorithm

Fig. 7.9 shows the performance of DSTATCOM under PFC mode. This figure shows phase voltages at PCC (v_s), source currents (i_s), load currents (i_{la}, i_{lb} and i_{lc}), compensator currents ($i_{Ca,}$ i_{Cb} and i_{Cc}) and the DC bus voltage (V_{dc}). These results are obtained at a nonlinear load of R_l=12Ω and L=100mH. The system is under fixed load condition before t=0.3s. Phase 'c' load is suddenly disconnected at t=0.3s, and it is reconnected at t=0.4s. Simulated results show that the control algorithm not only maintains the DC bus voltage but also the supply currents are balanced and sinusoidal during this interval. Fig. 7.10 shows harmonic spectra for phase 'a' PCC voltage (v_{sa}), supply current (i_{sa}) and load current (i_{la}). These results show the THD of 1.15% in PCC voltage, 2.55% in supply current and 26.52% in load current. It is shown in Fig. 7.9 and

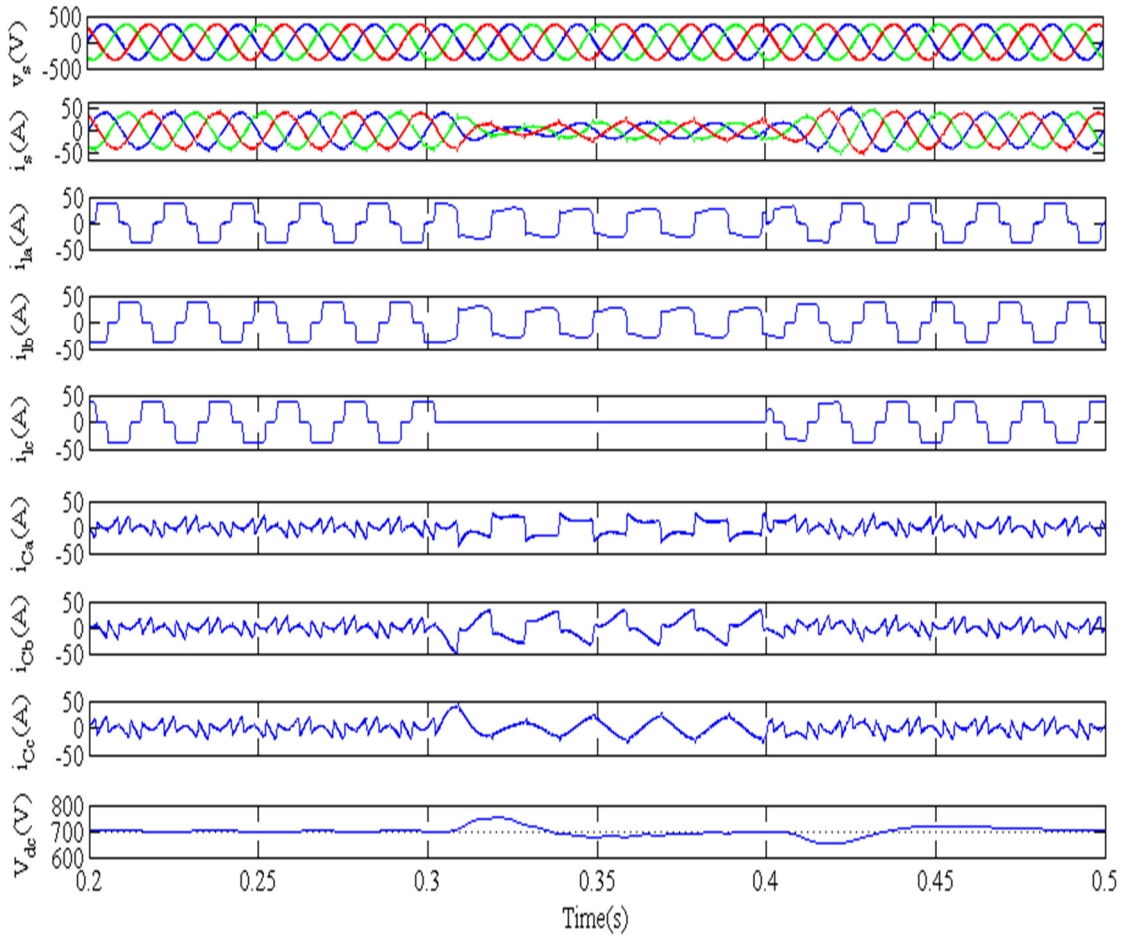
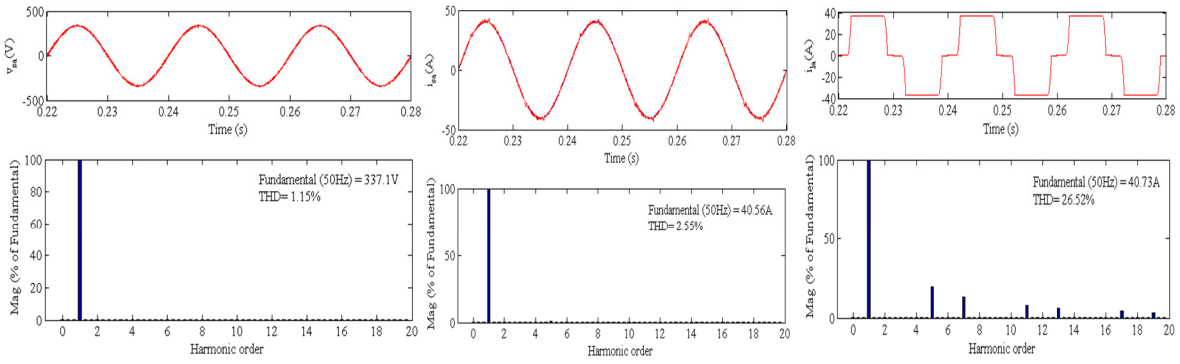


Fig. 7.9 Performance of DSTATCOM in PFC mode

Fig. 7.10 that the DSTATCOM is able to perform the functions of harmonic reduction in PFC mode.

B. Performance of DSTATCOM in Voltage Regulation Mode With ANFIS Based Control Algorithm



(a) (b) (c)

Fig. 7.10 Harmonic spectra of (a) PCC voltage, v_{sa} (b) supply current, i_{sa} (c) load current, i_{la} in PFC mode

Fig. 7.11 shows the dynamic performance of DSTATCOM for voltage regulation mode. In this mode, the amplitude of PCC voltage is maintained at 338.89V by injecting the leading reactive power by the VSC. The performance of the ANFIS controller for DSTATCOM is observed under nonlinear load. Fig. 7.11 represents voltage at PCC (v_s), supply currents (i_s), load currents (i_{la}, i_{lb} and i_{lc}), compensator currents (i_{Ca}, i_{Cb} and i_{Cc}), DC bus voltage (V_{dc}) and the PCC voltage magnitude (V_t). These results are obtained under nonlinear load of R_l=12Ω and L=100mH till 0.3s. Phase 'c' of the load is suddenly disconnected at t=0.3s, and reconnected at t=0.4s. Fig. 7.12 shows the harmonic spectra of phase 'a' of PCC voltage (v_{sa}), supply current (i_{sa}) and load

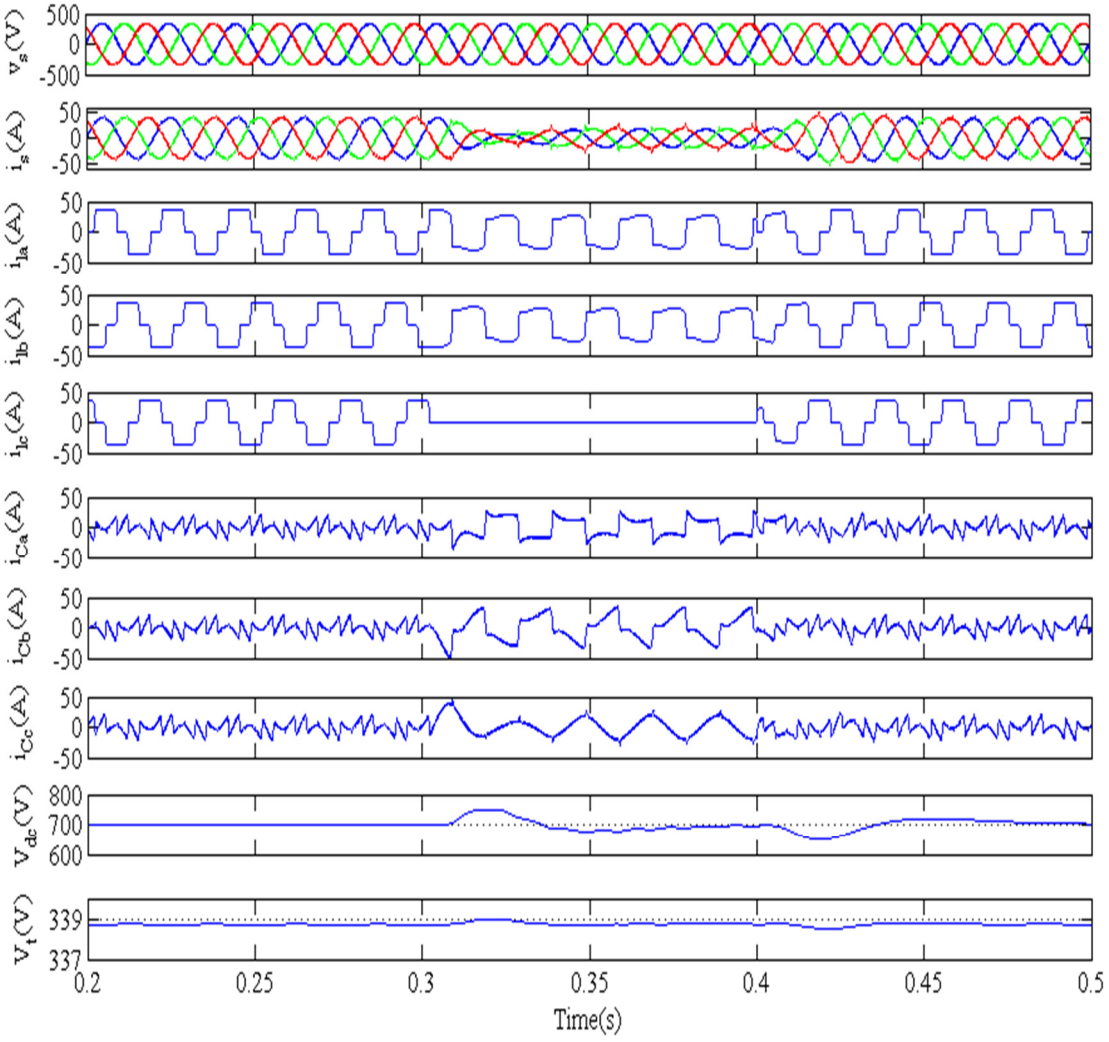
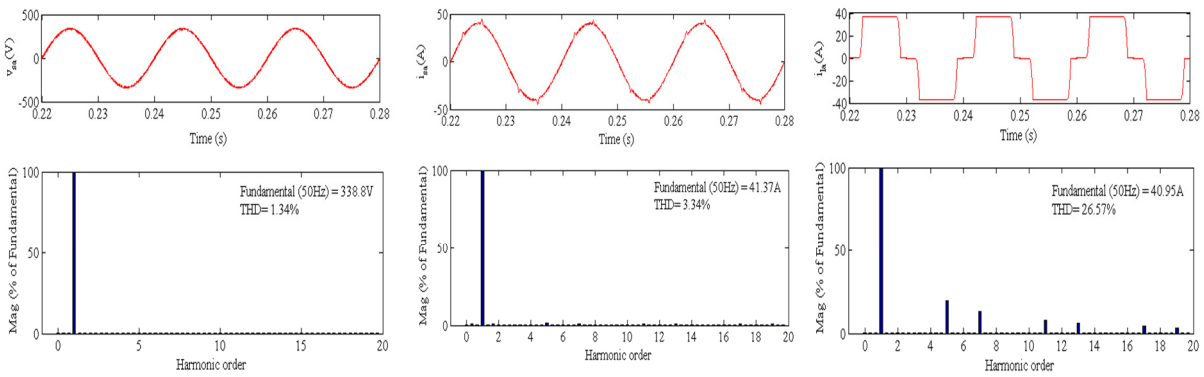


Fig. 7.11 Performance of DSTATCOM in voltage regulation mode



(a) (b) (c)

Fig. 7.12 Harmonic spectra of (a) PCC voltage, v_{sa} (b) supply current, i_{sa} (c) load current, i_{la} in voltage regulation mode

current (i_{la}). These results show THD of 1.34% in PCC voltage, 3.34% in supply current and 26.57% in load current. Amplitude of PCC voltage is regulated at 338.89V even during unbalance load condition from t=0.3s to t=0.4s.

7.6.1.2 Experimental Performance of ANFIS Based Control Algorithm in PFC Mode

Experimental performance of DSTATCOM with ANFIS based control algorithm in PFC mode is presented here. This is divided into two parts. The first part deals with the steady state performance of DSTATCOM and the dynamic performance of the system is presented in the second part.

A. Steady State Performance of DSTATCOM With ANFIS Based Control Algorithm

Fig.7.13 shows the performance of DSTATCOM in steady state condition. Figs. 7.13(a), (c) and (e) show the waveforms of phase 'a' of supply current (i_{sa}), load current (i_{la}) and compensator current (i_{Ca}) along with PCC voltage (v_{sa}). Figs. 7.13(b), (d) and (f) show the harmonic spectra of supply current (i_{sa}), load current (i_{la}) and PCC voltage (v_{sa}). These results show that THD of 3.3%, 23.2% and 3.3% in supply current, load current and PCC voltage respectively. It is observed from the experimental results that THD of supply current and PCC voltage are well within the limit of IEEE-519 standard.

Fig. 7.14 shows simulated performance of the DSTATCOM at the same rating (110V, 50Hz) for which experimental prototype is developed. These results shows waveforms of PCC voltage (v_s), supply currents (i_s), load currents (i_l), compensator currents (i_C) and DC bus voltage (V_{dc}). These results are shown for steady state (Before t=0.36) and unbalanced load (t=0.36s to t=0.46s) conditions. It is observed from these results that supply currents are balance and sinusoidal along with regulated DC bus voltage in steady state and unbalanced load conditions.

B. Dynamic Performance of DSTATCOM With ANFIS Based Control Algorithm

Fig. 7.15 shows the performance of DSTATCOM system when the phase 'c' of load current is removed. Figs. 7.15(a)-(c) show three phase supply currents (i_{sa}, i_{sb} and i_{sc}), load currents (i_{la}, i_{lb} and i_{lc}) and compensator currents (i_{Ca}, i_{Cb} and i_{Cc}) with PCC voltage (v_{sa}) respectively. It is observed form these waveforms that supply currents are balanced even after removal of a phase

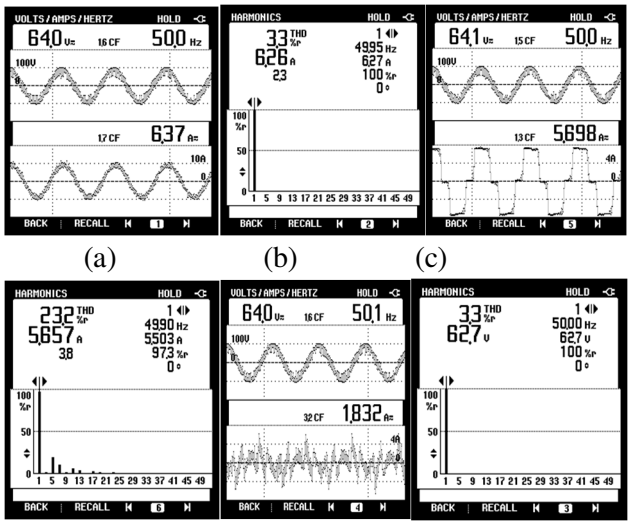


Fig. 7.13 Steady state performance (a),(c) and (e) i_{sa}, i_{la} and i_{Ca} along with v_{sa} (b),(d) and (f) harmonic spectra of supply current, load current and PCC voltage

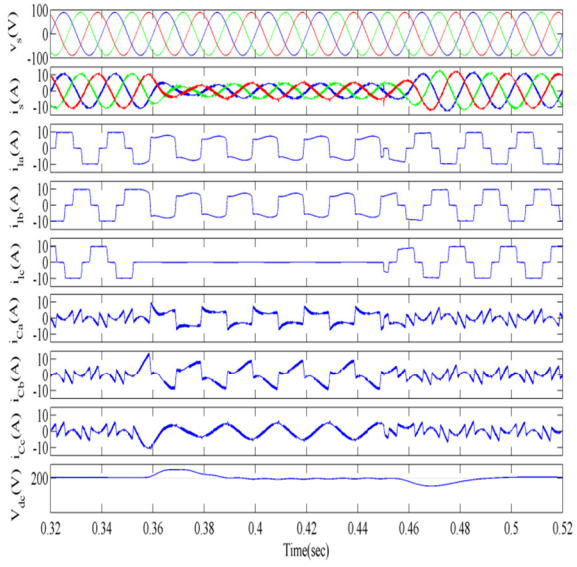


Fig. 7.14 Performance of DSTATCOM in PFC mode under nonlinear load

of load current. Fig. 7.15(d) shows DC bus voltage (V_{dc}) with phase 'c' of supply current (i_{sc}), load current (i_{lc}) and compensator currents (i_{Cc}). It is observed from Fig. 7.15(d) that the DC bus

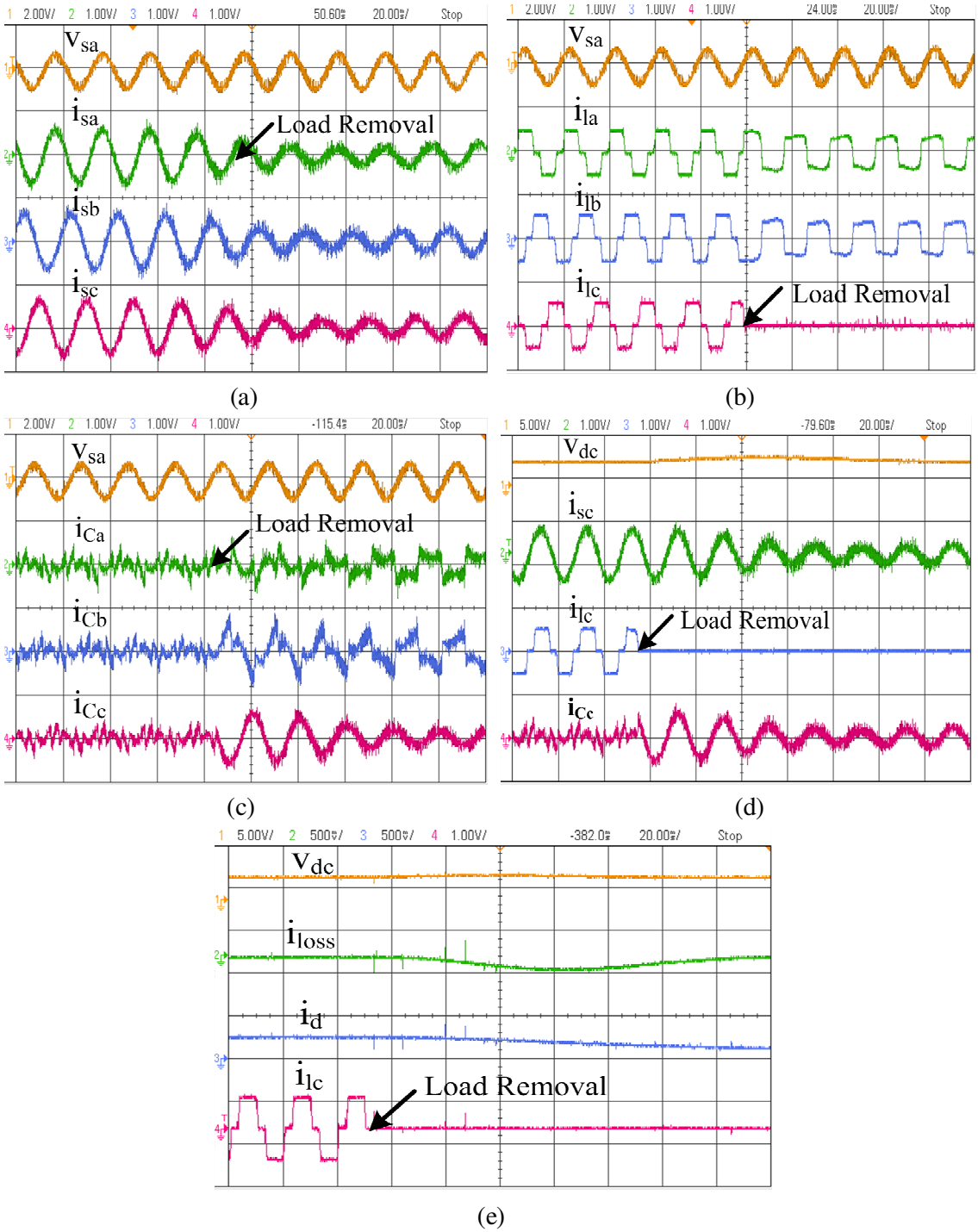


Fig. 7.15 Dynamic performance of DSTATCOM (a) v_{sa}, i_{sa}, i_{sb} and i_{sc} (b) v_{sa}, i_{la}, i_{lb} and i_{lc} (c) v_{sa}, i_{Ca}, i_{Cb} and i_{Cc} (d) V_{dc}, i_{sc}, i_{lc} and i_{Cc} (e) V_{dc}, i_{loss}, i_d and i_{lc}

voltage (V_{dc}) is regulated using ANFIS controller which achieves its reference value within few cycles. Fig. 7.15(e) shows the intermediate signals such as output of DC bus PI controller (i_{loss}) and active current component of load (i_d), components along with DC bus voltage (V_{dc}) and phase 'c' of load current (i_{lc}). Results show the adequate performance of ANFIS controller and control algorithm for DSTATCOM under dynamic nonlinear load.

7.6.2 Performance of Real Time Recurrent Learning (RTRL) Based Control Algorithm

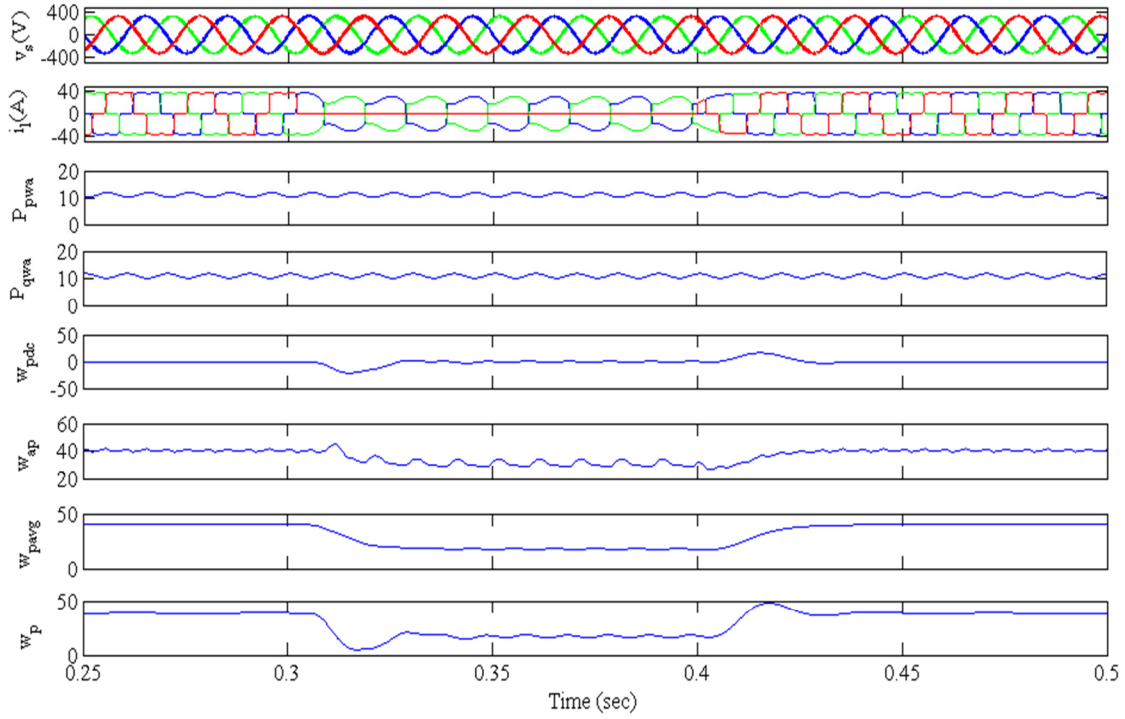
This section presents the simulation and experimental performance of RTRL based control algorithm for the control of DSTATCOM. The performance of the control algorithm is presented in PFC and voltage regulation modes using simulation models developed in MATLAB/SIMULINK environment. The experimental performance of the control algorithm is presented using the prototype model developed in the laboratory. The performance of the RTRL based control algorithm is discussed in detail as follows.

7.6.2.1 Simulation Results for the Control of DSTATCOM in PFC and voltage regulation Modes using RTRL Algorithm

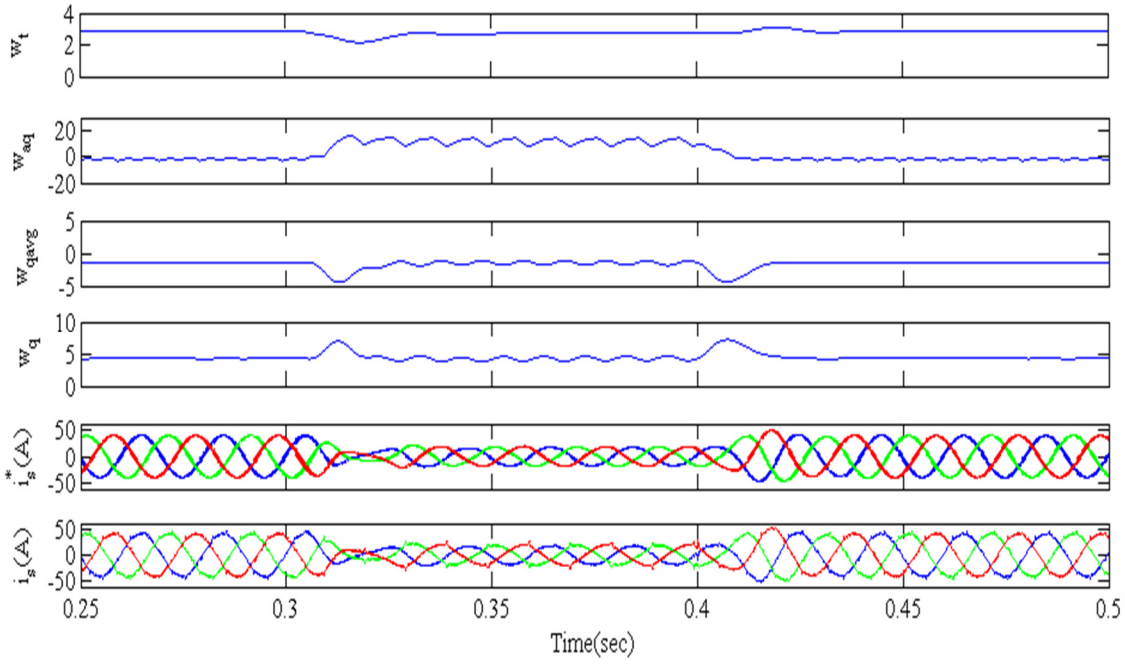
Simulation results showing the performance of DSTATCOM in PFC and voltage regulation modes with RTRL based control algorithm are presented here. This is divided into three parts. The first part presents the performance of the control algorithm. The second and third parts present the performance of DSTATCOM in PFC and voltage regulation mode.

A. Performance of RTRL Based Control Algorithm in Voltage Regulation Mode Under Nonlinear Load

Figs. 7.16(a) and (b) show the intermediate signals for the control algorithm used to generate the reference supply currents. Fig. 7.16(a) shows of sensed load currents (i_l), sensitivity element corresponding to active (P_{pwa}) and reactive (P_{qwa}) power components, output of DC bus PI controller (w_{pdc}), weighted value corresponding to active power component of phase 'a' of load



(a)



(b)

Fig. 7.16 Performance of RTRL based control algorithm in voltage regulation mode

current (w_{pa}), filtered average weighted value (w_{pavg}) of active power component of load current

and reference weight corresponding to active power component (w_p) along with PCC voltages (v_s). Fig. 7.16(b) shows waveforms of output of AC bus PI controller (w_t), weighted value corresponding to reactive power component of phase 'a' of load current (w_{qa}), filtered average reactive power weight (w_{qavg}), reference reactive power weight (w_q), estimated reference supply currents (i_s^*) and the actual sensed supply currents (i_s). These signals are shown in voltage regulation mode under nonlinear load. It is observed from these results that the control algorithm performs satisfactory in steady state (before t=0.3s) and unbalanced load (t=0.3s to t=0.4s) conditions. The generated reference supply currents are compared with the sensed supply current (i_s) and it is observed that the actual currents track the reference currents under steady state as

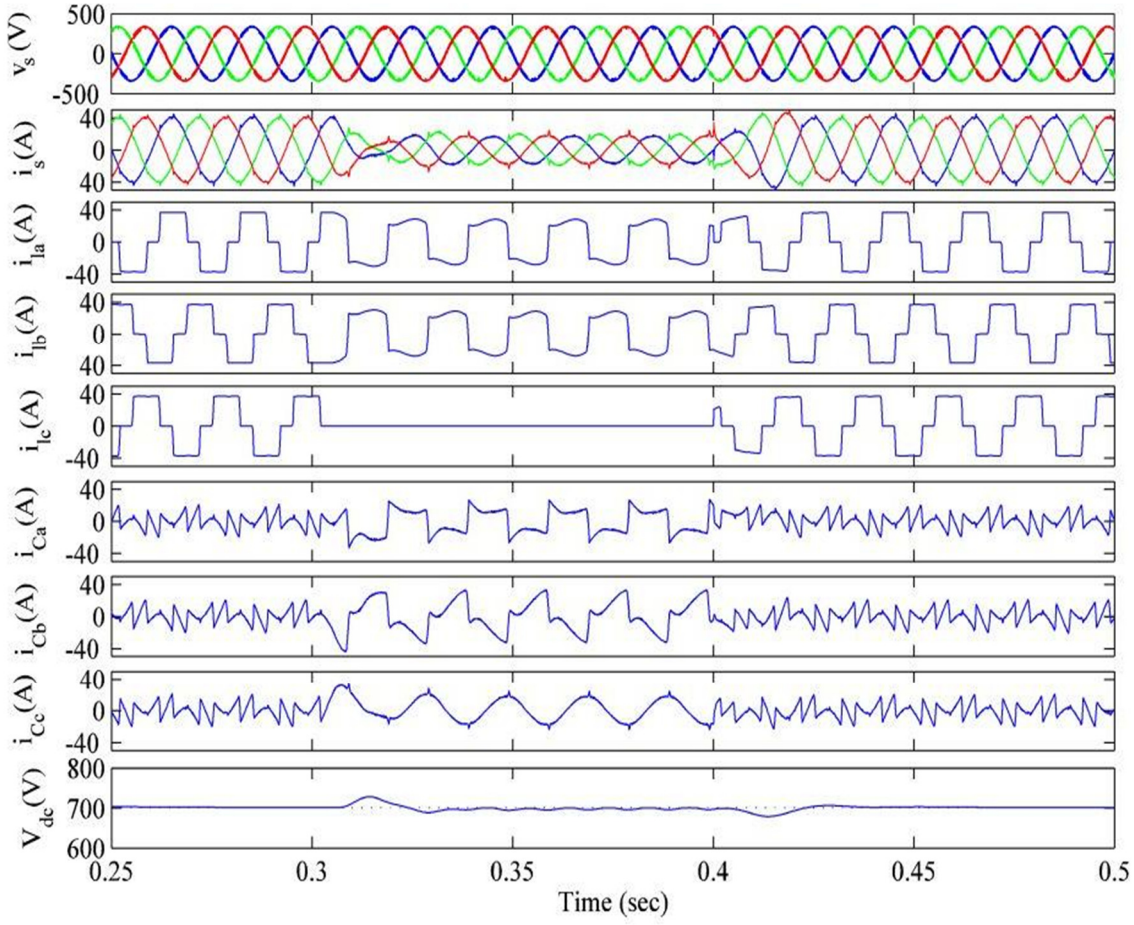
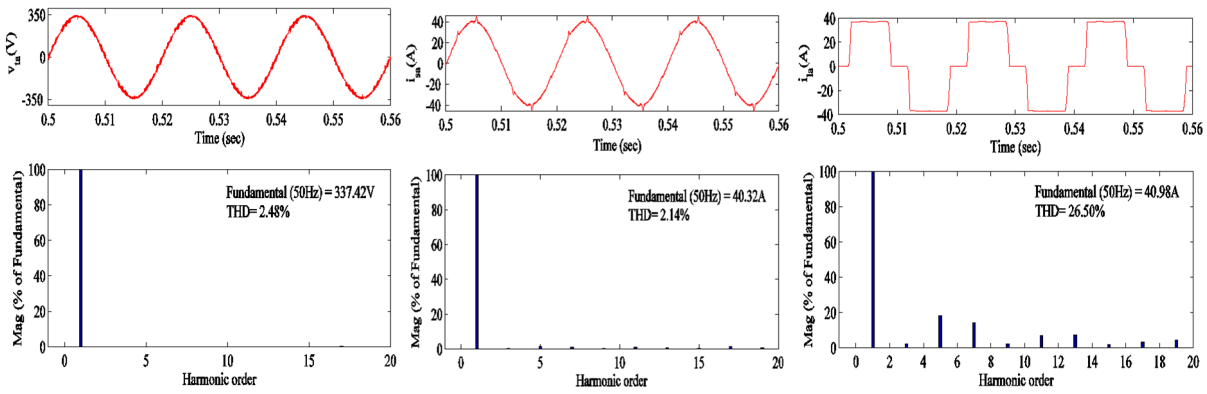


Fig. 7.17 Performance of DSTATCOM in PFC mode under nonlinear load



(a) (b) (c)

Fig. 7.18 Harmonic spectra of (a) PCC voltage, v_{sa} (b) supply current, i_{sa} (c) load current, i_{la} in PFC mode

well as dynamic load conditions.

B. Performance of DSTATCOM in PFC Mode Under Nonlinear Load

Fig. 7.17 shows the performance of shunt compensator in PFC mode under nonlinear load. The waveforms of PCC voltages (v_s), supply currents (i_s), load currents (i_{la}, i_{lb} and i_{lc}), compensator currents (i_{Ca}, i_{Cb} and i_{Cc}) and self-sustained DC bus voltage (V_{dc}) are shown in this figure. Steady state condition occurs in the system before t=0.3s and it is observed that the supply currents are balanced, sinusoidal and inphase with PCC voltages. The DC bus voltage is regulated to a reference voltage of 700V. At t=0.3s, unbalancing is created in the load, when phase 'c' load is switched off. This condition remains till t=0.4s and it is observed that the supply currents are still balanced and sinusoidal. During the period of load unbalancing, the DC bus voltage is regulated to its reference value of 700V, within a cycle. The overshoot/undershoot in the voltage level is of the order of 8V.

Fig. 7.18 shows the harmonic spectra of phase 'a' of PCC voltage (v_{sa}), supply current (i_{sa}) and load current (i_{la}) in PFC mode. The THD obtained in PCC voltage, supply current and load current are 2.48%, 2.14% and 26.50% respectively. It is observed from these results that 2.14%

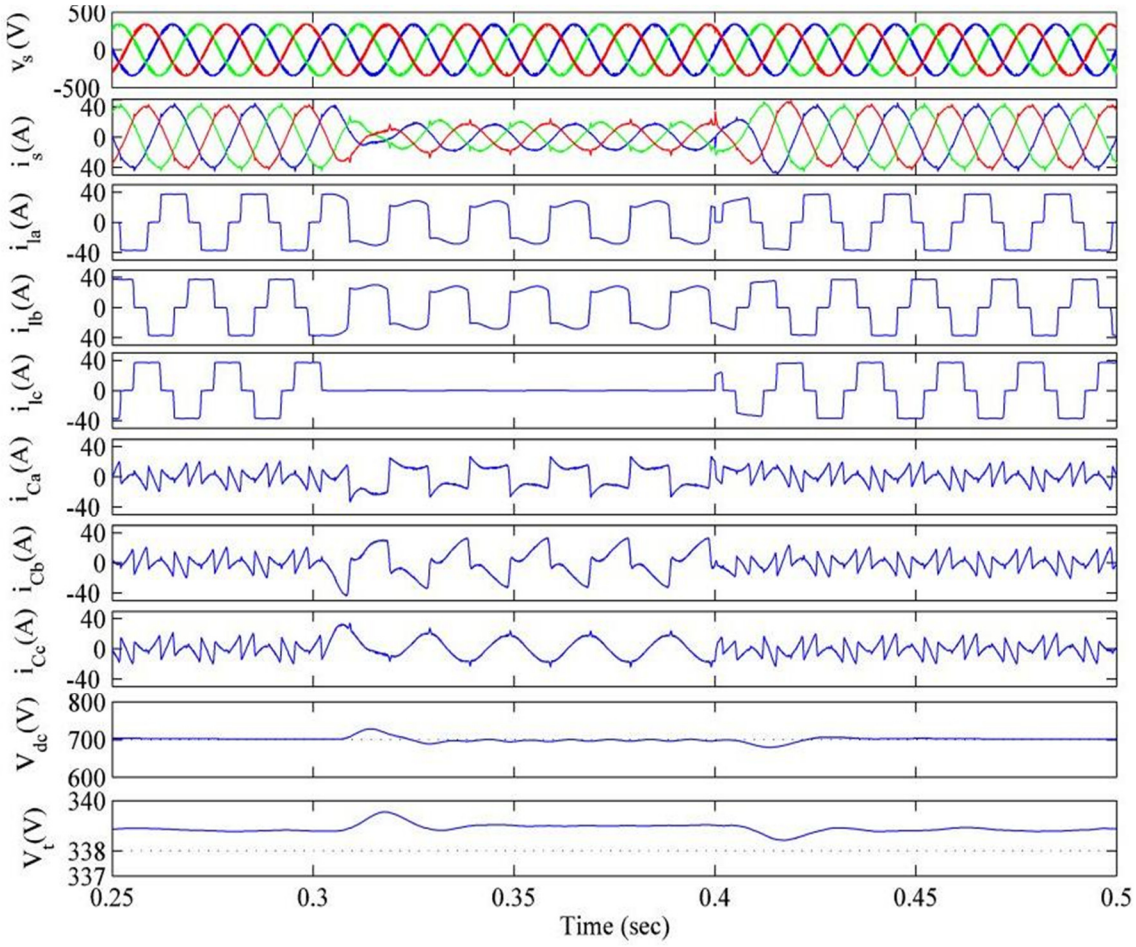
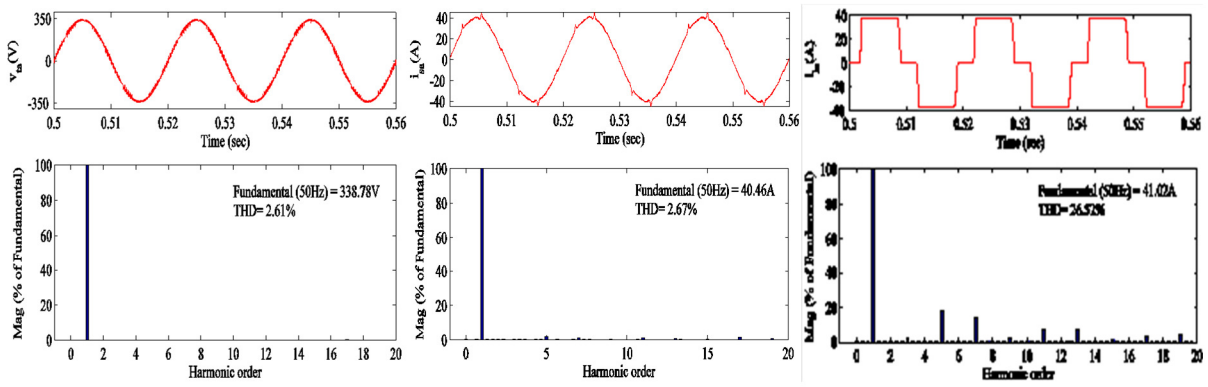


Fig. 7.19 Performance of DSTATCOM in voltage regulation mode under nonlinear load

THD is achieved in supply current, whereas there is 26.50% THD in load current. The THDs obtained in supply voltage and supply currents are within the limits specified by IEEE-519 standard.

C. Performance of DSTATCOM in Voltage Regulation Mode Under Nonlinear Load

Fig. 7.19 shows the performance of a shunt compensator in voltage regulation mode. The waveforms of PCC voltages (v_s), supply currents (i_{sa}), load currents (i_{la}, i_{lb} and i_{lc}), compensator currents (i_{Ca}, i_{Cb} and i_{Cc}), DC bus voltage (V_{dc}) and amplitude of PCC voltage (V_t) are shown in this figure. It is observed from the results that the system is in steady state and the supply currents are balanced and sinusoidal till t=0.3s. The DC bus voltage and amplitude of PCC



(a) (b) (c)

Fig. 7.20 Harmonic spectra of (a) PCC voltage, v_{sa} (b) supply current, i_{sa} (c) load current, i_{la} in voltage regulation mode

voltage are regulated at reference values of 700V and 338.8V respectively. At t=0.3s, phase 'c' of load is suddenly switched off, which creates unbalancing in the load currents. During load unbalancing (t=0.3s to t=0.4s), it is observed from the results that the three phase supply currents are still balanced and sinusoidal although reduced in magnitude. The DC bus voltage and amplitude of PCC voltage are regulated to their reference value within a cycle by controller action.

The harmonic spectra of phase 'a' of PCC voltage (v_{sa}), supply current (i_{sa}) and load current (i_{la}) are shown in Fig. 7.20. The THDs of PCC voltage, supply current and load current are observed to be 2.61%, 2.67% and 26.52% respectively. It is concluded from these results that 2.67% THD is obtained in supply current, whereas there is THD of 26.52% in the load current. The THDs obtained in the supply voltage and supply current in voltage regulation mode are within the limit specified by IEEE-519 standard.

7.6.2.2 Experimental Performance of RTRL Based Control Algorithm in PFC and Voltage Regulation Mode Under Nonlinear and Linear Loads

Experimental performance of RTRL based control algorithm on the prototype developed in the laboratory is presented here. This is divided into three parts. The first part deals with the

experimental performance of the control algorithm. The other two parts present the performance of DSTATCOM under steady state and dynamic load conditions respectively.

A. *Performance of the RTRL Based Control Algorithm*

Fig. 7.21 shows the intermediate signals of RTRL based control algorithm for control of DSTATCOM. Test results in Fig. 7.21(a) show the waveforms of PCC voltage (v_{sa}), filtered PCC voltage (v_{saf}), phase 'c' of load current (i_{lc}) and sensitivity element (P_{pwa}). Fig. 7.21(b) shows

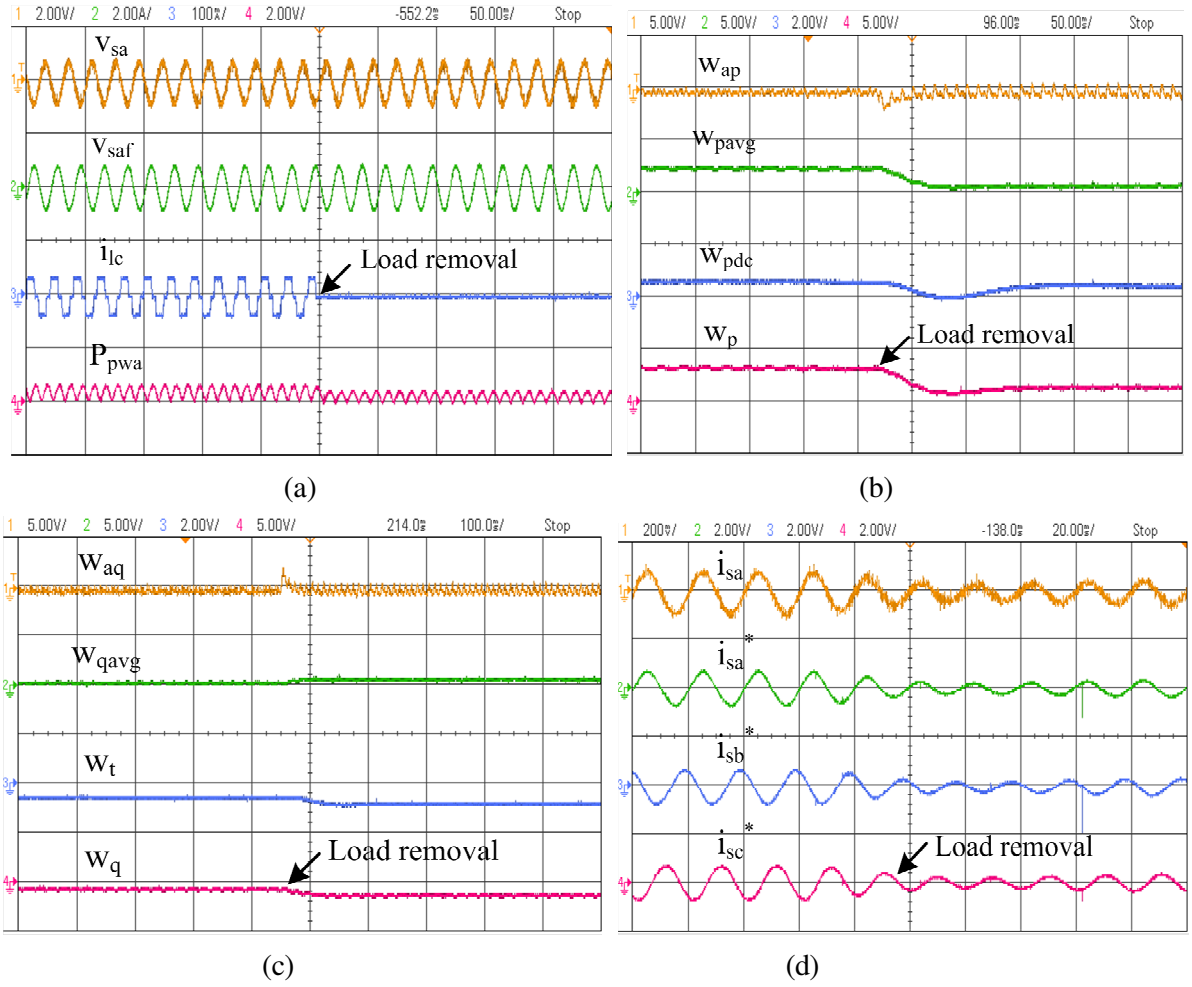


Fig. 7.21 Intermediate signals of RTRL control algorithm (a) v_{sa}, v_{saf}, i_{lc} and P_{pwa} (b) w_{ap}, w_{pavg}, w_{pdc} and w_p(c) w_{aq}, w_{qavg}, w_t and w_q (d) i_{sa}, i_{sa}^*, i_{sb}^* and i_{sc}^*

weight corresponding to fundamental active power component of phase 'a' of load current (w_{ap}), average active power weight (w_{pavg}), output of DC bus PI controller (w_{pdc}) and reference active power weight (w_p). Fig. 7.21(c) shows the waveforms of weight corresponding to fundamental reactive power component of phase 'a' of load current (w_{aq}), average active power weight (w_{qavg}), output of AC bus PI controller (w_t) and reference reactive power weight (w_t). These results are shown for steady state as well as unbalance load conditions, when one phase of load is switched off. Fig. 7.21(d) shows the reference supply currents (i_{sa}^*, i_{sb}^* and i_{sc}^*) along with the phase 'a' sensed supply current (i_{sa}). It is observed from these results that the average weighted value converges in steady state as well as in unbalanced load conditions. The sensed supply currents track the reference supply currents perfectly. These results show the satisfactory performance of the RTRL based control algorithm for DSTATCOM.

B. Steady State Performance of DSTATCOM With RTRL Based Control Algorithm in PFC Mode

Fig. 7.22 shows the steady state performance of DSTATCOM using RTRL based control algorithm under nonlinear load. Figs. 7.22(a)-(c) show the results of phase 'a' of supply current (i_{sa}), load current (i_{la}) and compensator current (i_{Ca}) along with PCC voltage (v_{sa}). Figs. 7.22(d)-(f) show the harmonic spectra and THD of phase 'a' of supply current (i_{sa}), load current (i_{la}) and PCC voltage (v_{sa}), which are observed to be 3.9%, 21.7% and 3.3% respectively. It is observed from these results that THD of 3.9% is obtained in supply current, whereas load current has THD of 21.7%. These results show the satisfactory performance of DSTATCOM using RTRL based control algorithm and the supply voltage and the supply current THDs are within the limit specified by international standards.

Fig. 7.23 shows the simulated performance of the DSTATCOM using RTRL based control algorithm at same voltage rating (110V, 50Hz) for which experimental system is developed. This shows the waveforms of PCC voltages (v_s), supply currents (i_s), load currents (i_{la}, i_{lb} and i_{lc}), compensator current (i_{Ca}, i_{Cb} and i_{Cc}) and self-sustained DC bus voltage (V_{dc}). The supply currents are balanced and sinusoidal and DC bus voltage is regulated at the reference voltage of 200V during steady state (before t=0.3s) and unbalanced load condition (t=0.3s to t=0.4s).

Fig. 7.24 shows steady state performance of the DSTATCOM under linear lagging PF load in PFC mode. Figs. 7.24(a)-(c) show waveforms of phase 'a' of supply current (i_{sa}), load current (i_{la}) and compensator current (i_{Ca}) along with PCC voltage (v_{sa}). Figs. 7.24(d)-(f) show waveforms of supply apparent power (P_s), load apparent power (P_l) and compensator apparent power (P_C). The values of supply and load apparent powers are 0.29 and 0.31kVA respectively. The power factor on supply side is improved (close to 1 DPF) as the reactive power demand of the load is provided by DSTATCOM.

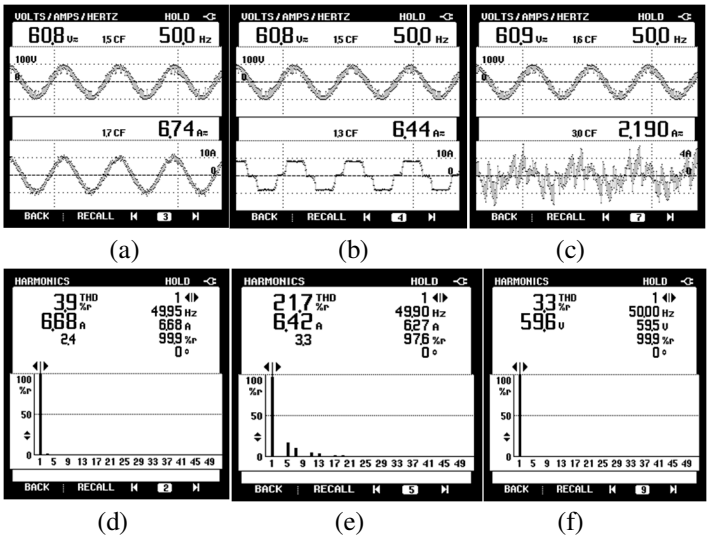


Fig. 7.22 Steady state performance of DSTATCOM under non-linear load (a)-(c) i_{sa}, i_{la}, i_{Ca} along with v_{sa} (d)-(f) harmonic spectra of i_{sa}, i_{la} and i_{Ca} in PFC mode

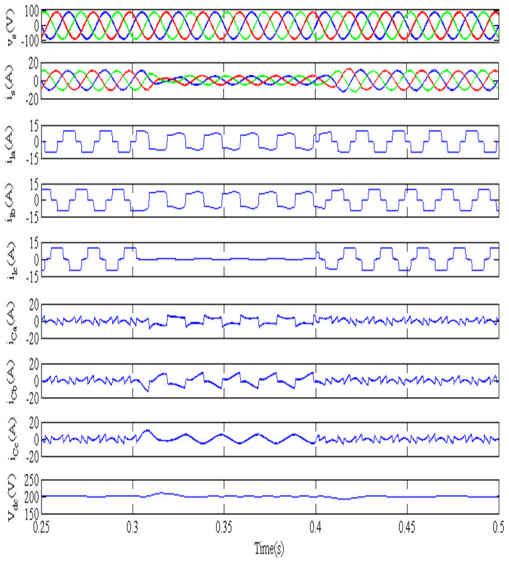


Fig. 7.23 Simulated performance of DSTATCOM in PFC mode

Fig. 7.25 shows simulated performance of the DSTATCOM under linear load in PFC mode at the same rating (110V, 50Hz) for which experimental prototype is developed. The waveforms of PCC voltages (v_s), supply currents (i_s), load currents (i_{la}, i_{lb} and i_{lc}), compensator current (i_{Ca}, i_{Cb} and i_{Cc}) and self-sustained DC bus voltage (V_{dc}) are shown by these results. It is observed from these results that supply currents are maintained balanced and sinusoidal in steady state (before t=0.3s) and unbalance load (t=0.3s to t=0.4s) conditions. The DC bus voltage is regulated at its reference value of 200V under varying load conditions.

C. *Dynamic Performance of DSTATCOM With RTRL Based Control Algorithm in PFC Mode*

Fig. 7.26 shows dynamic performance of DSTATCOM under nonlinear load. Figs. 7.26(a)-(c) show the results of supply currents (i_{sa}, i_{sb} and i_{sc}), load currents (i_{la}, i_{lb} and i_{lc}) and compensator currents (i_{Ca}, i_{Cb} and i_{Cc}) along with the filtered PCC voltage (v_{saf}). These results show the satisfactory performance of DSTATCOM in maintaining supply currents balanced and sinusoidal, even under unbalanced load condition. Fig. 7.26(d) shows the waveform for DC bus

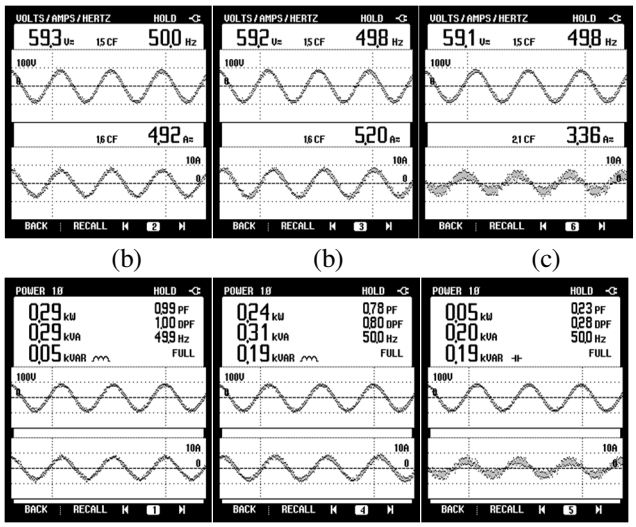


Fig. 7.24 Steady state performance of DSTATCOM under liner load (a)-(c) i_{sa}, i_{la}, i_{Ca} along with v_{sa} (d)-(f) P_s, P_l and P_C in PFC mode

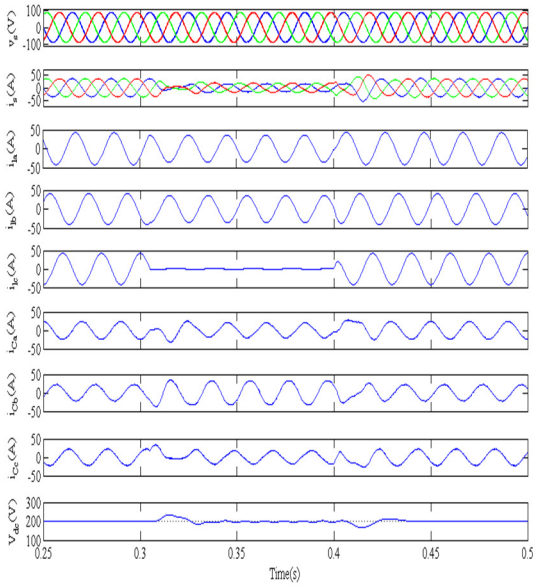


Fig. 7.25 Simulated performance of DSTATCOM in PFC mode under linear load

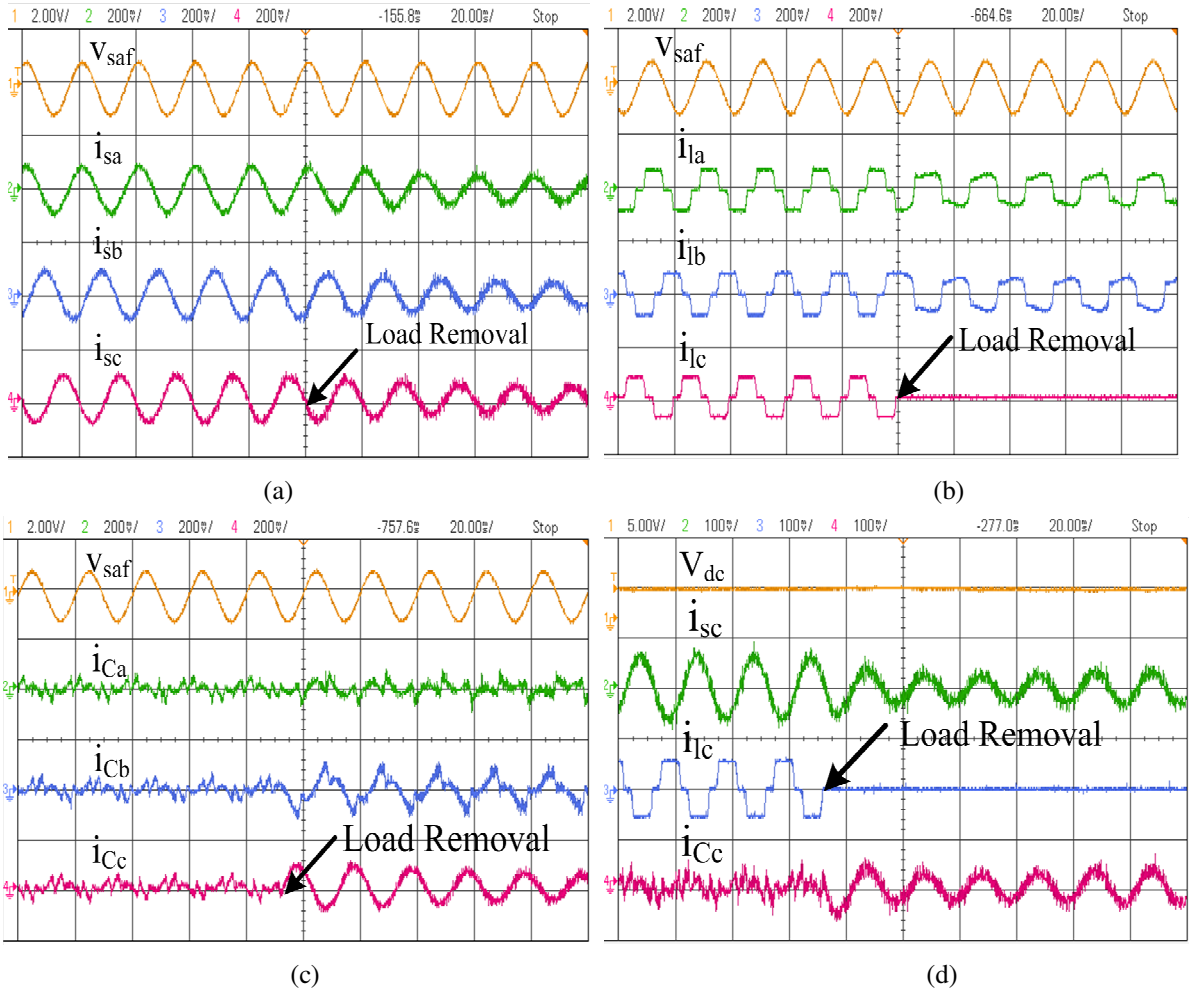


Fig. 7.26 Dynamic performance of DSTATCOM under nonlinear load (a) v_{saf}, supply currents (b) v_{saf}, load currents (c) v_{saf}, compensator currents (d) V_{dc}, i_{sc}, i_{lc} and i_{Cc} in PFC mode

voltage (V_{dc}), supply current of phase 'c' (i_{sc}), load current of phase 'c' (i_{lc}) and compensator current of phase '*c*' (i_{Cc}). It is observed from these results that DC bus voltage is regulated to its reference value of 200V with the PI controller action with small overshoot during unbalanced load condition.

2. *Steady State Performance of DSTATCOM in Voltage Regulation Mode*

Fig. 7.27 shows steady state performance of DSTATCOM in voltage regulation mode using RTRL based control algorithm under nonlinear load. Figs. 7.27(a), (b) and (c) show waveforms

of phase 'a' of supply current (i_{sa}), load current (i_{la}) and compensator current (i_{Ca}) along with PCC voltage (v_{sa}). Figs. 7.27(d), (e) and (f) show harmonic spectra of supply current, load current and PCC voltage. These results present THD of 4.8%, 20.4% and 3.5% in supply current, load current and PCC voltage respectively. Improved THD is achieved in supply current after compensation which is within the limit specified by IEEE-519 standard. Figs. 7.27(g), (h) and (i) show reactive powers in supply (Q_s), load (Q_l) and compensator (Q_C). It is observed from this result that reactive powers in supply and load are 0.11kVAR and 0.12kVAR respectively. Leading reactive power is observed in supply side, which is required for PCC voltage regulation. Fig. 7.28 shows simulated performance of DSTATCOM in voltage regulation mode at the same voltage rating (110V, 50Hz) for which experimental prototype is developed. These results

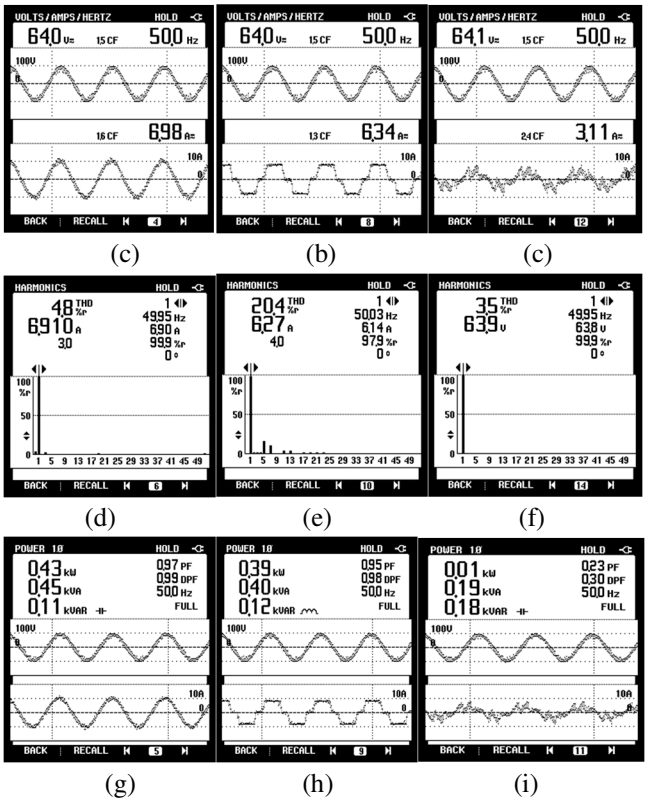


Fig. 7.27 Steady state performance of DSTATCOM under liner load (a)-(c) i_{sa}, i_{la}, i_{Ca} along with v_{sa} (d)-(f) harmonic spectra of i_{sa}, i_{la} and v_{sa} (g)-(i) Q_s, Q_l and Q_C in voltage regulation mode

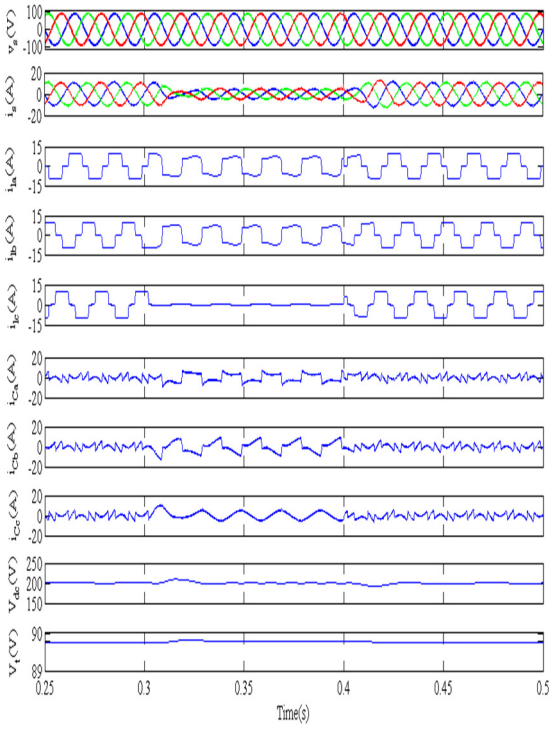
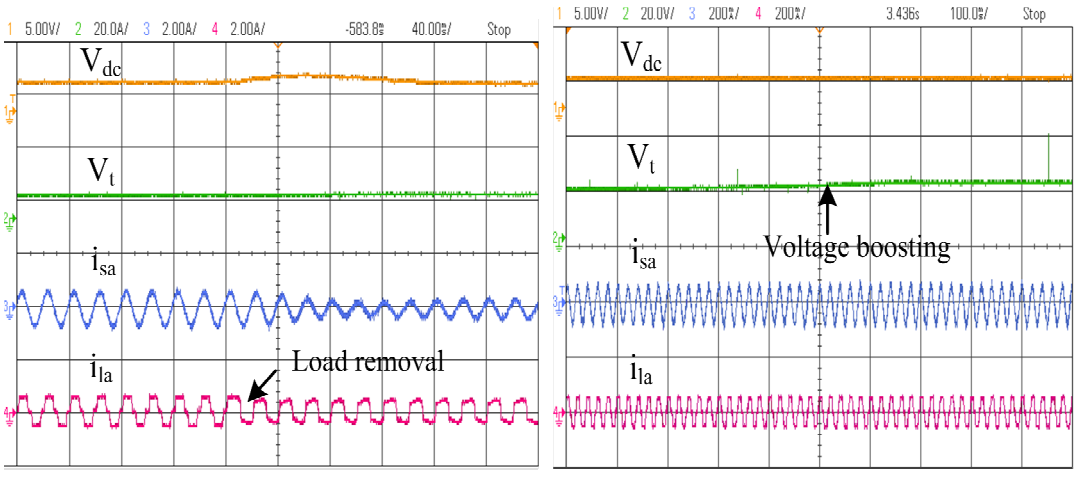


Fig. 7.28 Simulated performance of DSTATCOM in voltage regulation mode

present waveforms of PCC voltages (v_s), supply currents (i_s), load currents (i_{la}, i_{lb} and i_{lc}), compensator current (i_{Ca}, i_{Cb} and i_{Cc}), self-sustained DC bus voltage (V_{dc}) and amplitude of PCC voltage (V_t). It is observed from this result that DC bus voltage and amplitude of PCC voltage are regulated at their reference value of 200V and 89.9V in steady state (before t=0.3s) and unbalance load condition (t=0.3 t0 t=0.4s) respectively.

3. *Dynamic Performance of DSTATCOM in Voltage Regulation Mode Under Nonlinear Load*

Fig. 7.29 shows the dynamic performance of DSTATCOM in voltage regulation mode under nonlinear load. Fig. 7.29(a) presents waveforms of regulated DC bus voltage (V_{dc}), regulated amplitude of PCC voltage (V_t) along with phase 'a' of supply current (i_{sa}) and load current (i_{la}) in steady state and unbalance load conditions. It is observed from these results that supply currents are maintained balanced and sinusoidal in steady state and unbalanced load conditions. Fig. 7.29(b) shows waveforms of DC bus voltage (V_{dc}), PCC voltage amplitude (V_t), phase 'a' of supply current (i_{sa}) and phase 'a' of load current (i_{la}). It is observed from this result that the amplitude of PCC voltage magnitude (V_t) is boosted from 85V to 89V, due to the AC bus PI



(a) (b)

Fig. 7.29 Dynamic performance of DSTATCOM in voltage regulation mode

controller action.

7.6.3 Performance of DSTATCOM with ANFIS-LMS Based Control Algorithm

This section presents the simulation and experimental results depicting the performance of DSTATCOM using ANFIS-LMS based control algorithm. Simulation models are developed in MATLAB/SIMULINK environment for PFC and voltage regulation modes. Experimental results for the ANFIS-LMS based control algorithm for control of DSTATCOM are carried out on the DSTATCOM prototype developed in the laboratory.

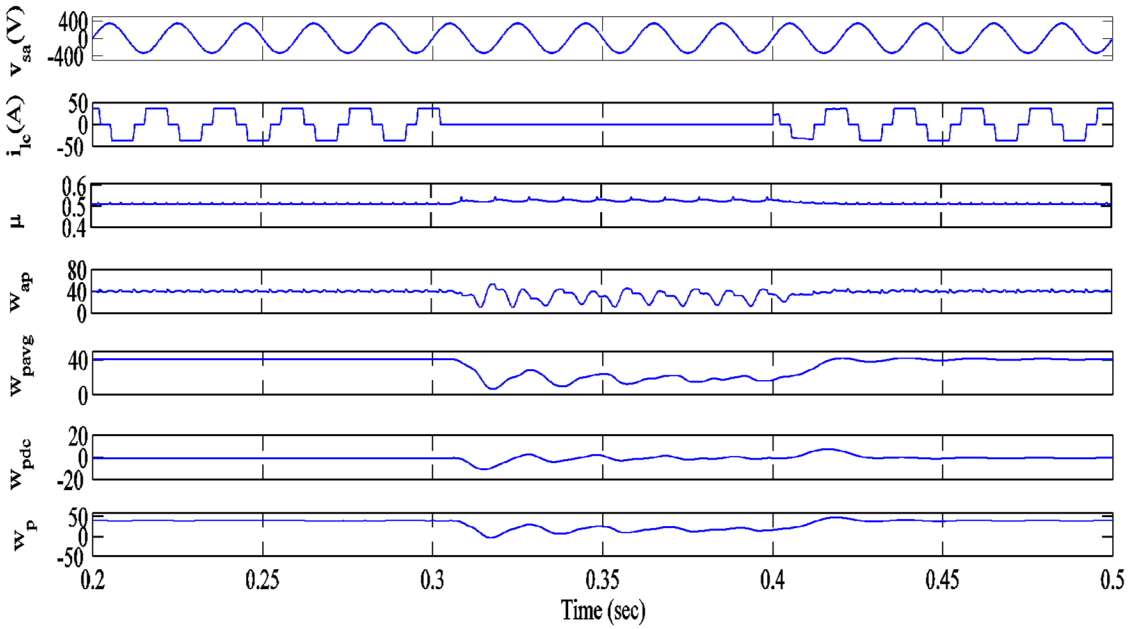
7.6.3.1 Simulated Performance of DSTATCOM in PFC and Voltage Regulation Modes

Simulated performance of ANFIS-LMS based control algorithm for control of DSTATCOM is presented here. This is divided into three parts. The first part presents performance of the ANFIS-LMS based control algorithm. The second and third parts deal with the performance of the DSTATCOM in PFC and voltage regulation modes.

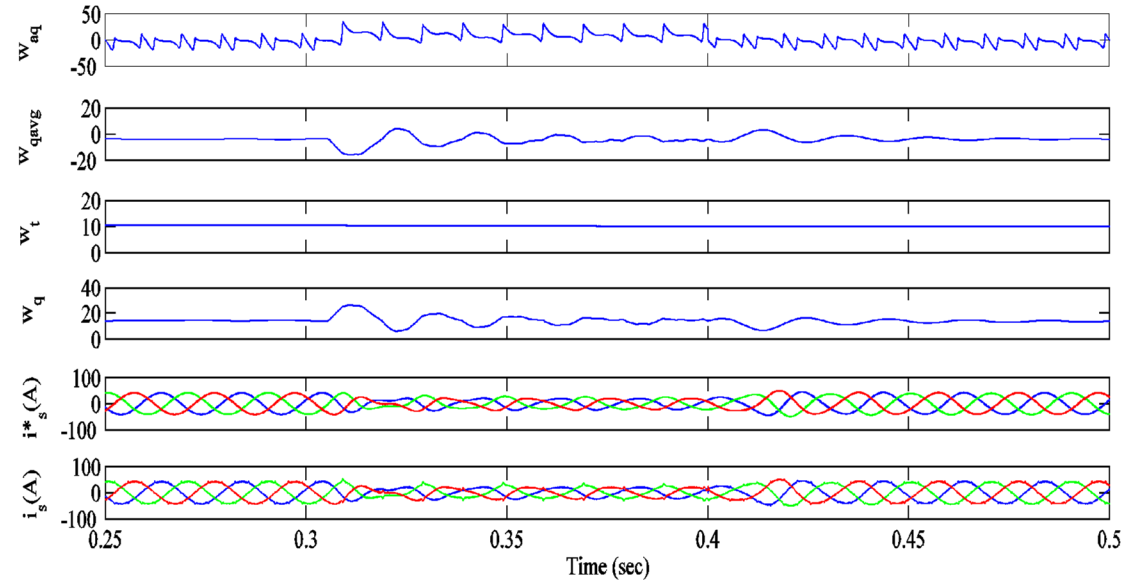
A. Performance of ANFIS-LMS Based Control Algorithm in Voltage Regulation Mode

Fig. 7.30 shows the performance and intermediate signals of ANFIS-LMS based control algorithm for control of DSTATCOM. Fig. 7.30(a) show the waveforms of variable step size parameter (μ), weight corresponding to active power component of phase 'a' load current (w_{ap}), average active power weight (w_{pavg}), output of DC bus PI controller (w_{pdc}) and reference active power weight (w_p) along with phase 'a' PCC voltage (v_{sa}) and phase 'c' load current (i_{lc}). These results are presented for steady state (before t=0.3s) and unbalanced load conditions (t=0.3s and t=0.4s).

Fig. 7.30(b) shows the waveforms of weight (w_{aq}) corresponding to reactive power component of load current, average reactive power weight (w_{qavg}), output of AC bus PI controller (w_t),



(a)



(b)

Fig. 7.30 Performance of ANFIS-LMS based control algorithm for voltage regulation mode

average reactive power weight (w_q), reference supply currents (i_s^*) and sensed supply currents (i_s). It is observed from this result that sensed supply currents follow the reference supply currents.

B. Performance of DSTATCOM in PFC Mode Using ANFIS-LMS Based Control Algorithm

Fig. 7.31 depicts the dynamic performance of the shunt compensator for power factor correction (PFC) under unbalanced load condition. In this figure, the waveforms of PCC voltages (v_s), supply currents (i_s), load currents (i_{la}, i_{lb} and i_{lc}), compensator currents (i_{Ca}, i_{Cb} and i_{Cc}) and DC bus voltage (v_{dc}) are presented. Unbalancing is created in load current during t=0.74s to t=0.8s, when phase 'c' load is disconnected. During load unbalancing, it is observed that the supply currents are sinusoidal and balanced with reduced amplitude. The voltage at DC bus is regulated and achieves reference value of 750V. After t=0.8s, phase 'c' load is re-connected and it is observed that DC bus voltage achieves its reference value within a cycle.

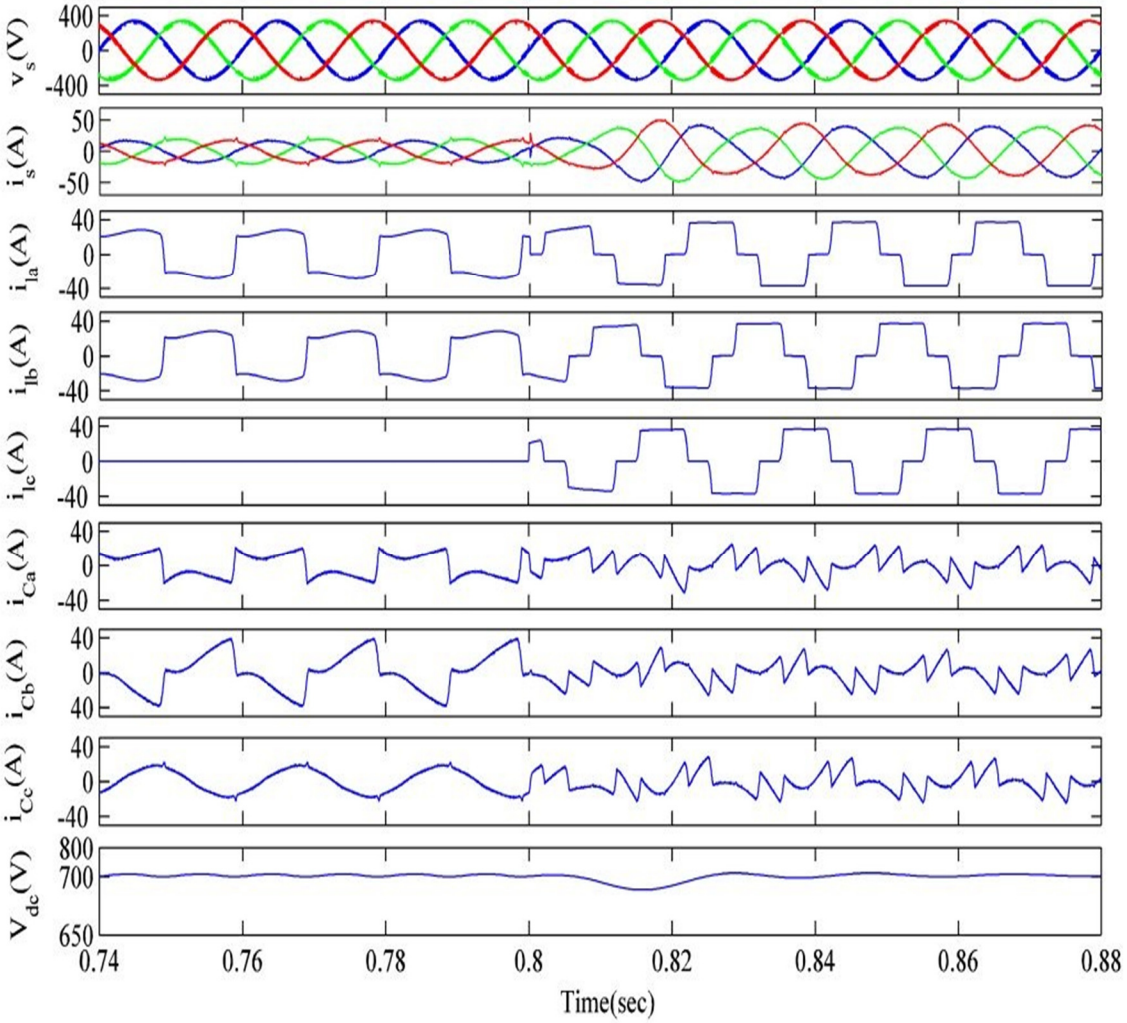
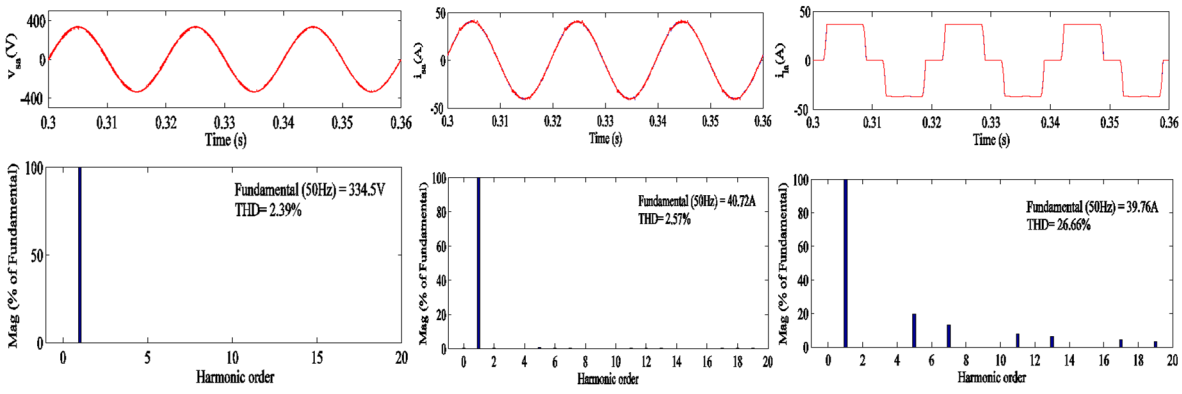


Fig. 7.31 Performance of compensator for PFC mode under varying non-linear load

Fig. 7.32 presents the harmonic spectra for phase 'a' PCC voltage (v_{sa}), supply current (i_{sa}) and load current (i_{la}) along with their waveforms. Figs. 7.32(a)-(c) show 2.39%, 2.57 % and 26.66% THDs in phase 'a' PCC voltage (v_{sa}), supply current (i_{sa}) and load current (i_{la}) respectively. The DSTATCOM with the help of ANFIS-LMS based control is able to achieve 2.57% THD in supply current which lies within the limit specified by IEEE-519 standard, even when load current THD is 26.66%. Fig. 7.24 and Fig. 7.25 depict satisfactory performance of DSTATCOM with ANFIS-LMS based control algorithm under varying load condition in PFC mode.

C. Performance of DSTATCOM in Voltage Regulation Mode Using ANFIS-LMS Based Control Algorithm

The performance of the shunt compensator in voltage regulation mode under varying load condition is depicted in Fig. 7.33. In this figure, the waveforms of PCC voltages (v_s), supply currents (i_s), load currents (i_{la}, i_{lb} and i_{lc}), compensator currents (i_{Ca}, i_{Cb} and i_{Cc}), voltage at DC bus (V_{dc}) and magnitude of PCC voltage (V_t) are presented. Unbalancing in load is created during t=0.74s to t=0.8s, when phase 'c' load is disconnected. During unbalancing, it is observed that supply currents are balanced and sinusoidal. The magnitude of PCC voltage is regulated at



(a) (b) (c)

Fig. 7.32 Waveforms and harmonic spectra of phase 'a' of (a) PCC voltage, v_{sa} (b) supply current, i_{sa} and (c) load current, i_{la} in PFC mode.

reference value of 338.8V. After t=0.8s, phase 'c' load is reconnected and it is observed that PCC voltage achieves its reference value of 338.8V within one cycle with the action of PI controller. Figs. 7.34(a)-(c) show harmonic spectra of phase 'a' PCC voltage (v_{sa}), supply current (i_{sa}) and load current (i_{la}) along with their waveforms respectively. These results depict 2.69%, 2.71 % and 26.83% THD in PCC voltage, supply current and load current respectively. It is observed from these results that supply current achieves 2.71% THD, whereas there is 26.83% THD in load current. These results show the THDs of supply current and PCC voltage are within the limit specified by IEEE-519 standard. Fig. 7.33 and Fig. 7.34, depict the performance of

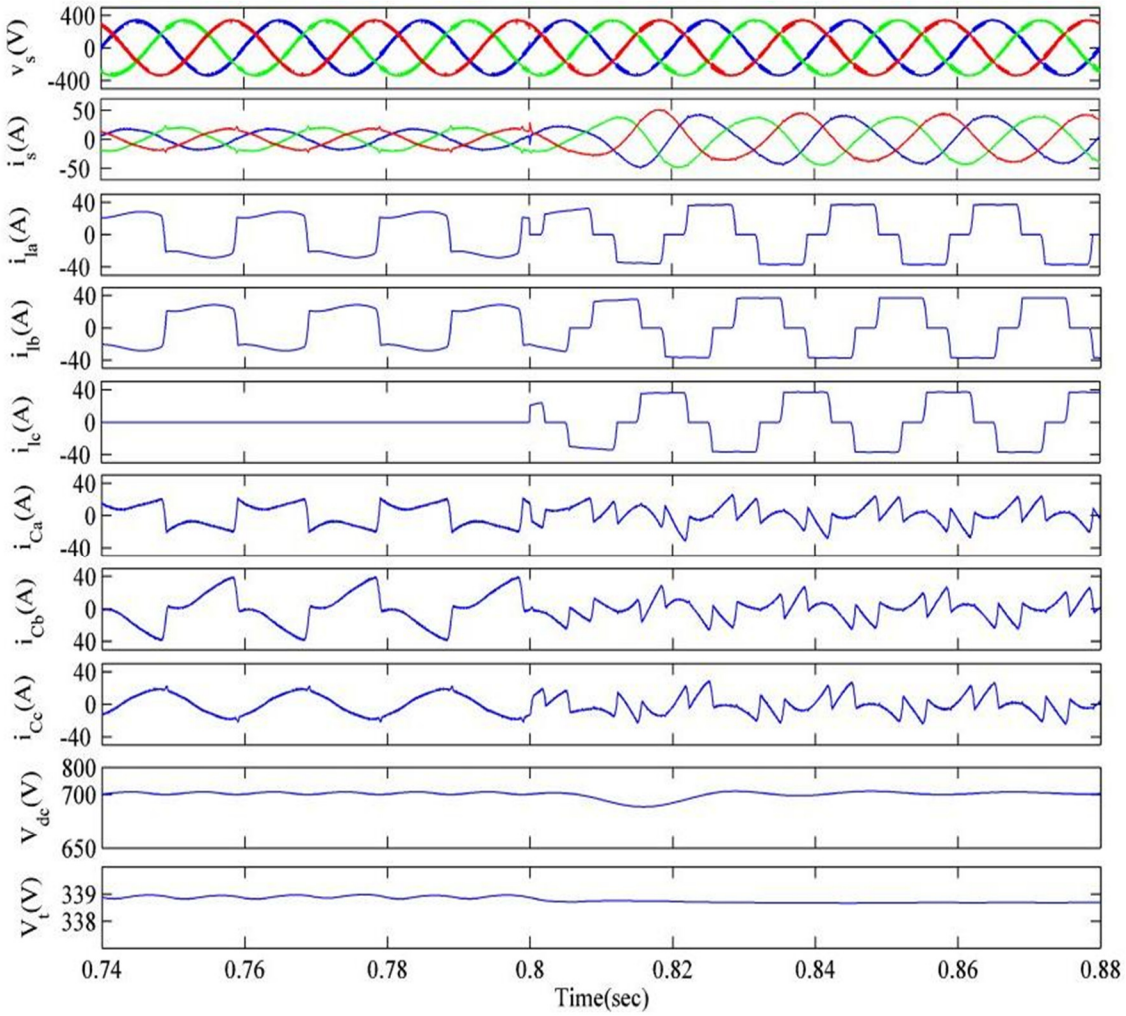
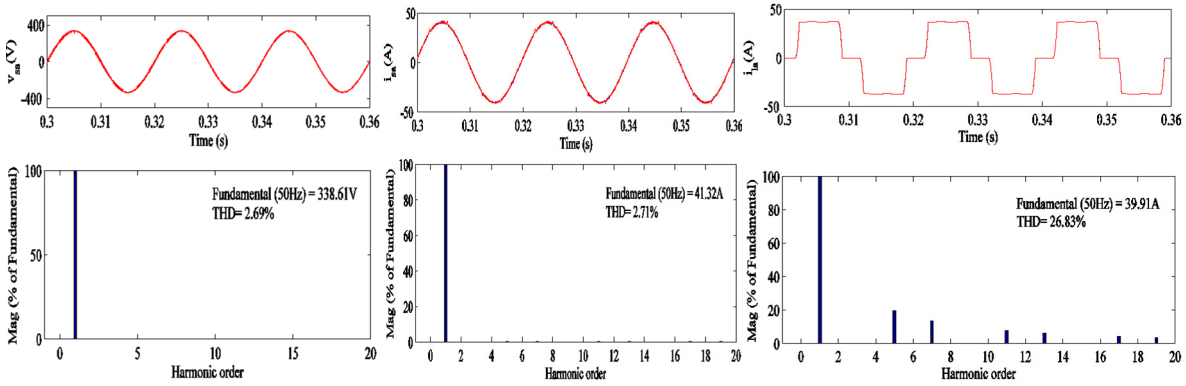


Fig. 7.33 Performance of compensator for voltage regulation mode under varying nonlinear load



(a) (b) (c)

Fig. 7.34 Waveforms and harmonic spectra of phase 'a' of (a) PCC voltage, v_{sa} (b) supply current, i_{sa} and (c) load current, i_{la} in voltage regulation mode.

DSTATCOM with ANFIS-LMS control algorithm under varying load condition in voltage regulation mode.

7.6.3.2 Experimental Performance of DSTATCOM with ANFIS-LMS Based Control Algorithm in PFC Mode

Experimental performance of DSTATCOM with ANFIS-LMS based control algorithm in PFC mode is presented here. This is divided into three parts. The first part presents performance of the control algorithm. The second and third parts present performance of the DSTATCOM in steady state and dynamic load conditions.

A. Performance of ANFIS-LMS Based Control Algorithm for DSTATCOM

Figs. 7.35(a)-(e) show the performance of the proposed ANFIS-LMS based control algorithm for control of DSTATCOM showing the intermediate signals. Fig. 7.35(a) shows the phase 'a' PCC voltage (v_{sa}) and its filtered value (v_{sa1}) along with phase 'c' load current (i_{lc}) and average value of active power weight (w_{pavg}). Fig. 7.35(b) shows the error (e), the change in error (Δe), variable step size (μ) along with unit in phase component of phase 'a' PCC voltage (u_{pa}). Fig. 7.35(c) shows the output of DC bus PI controller (w_{ploss}), average active power weight (w_{pavg}), reference active power weight (w_p) along with output of DC bus PI controller (V_{dc}). Fig. 7.35(d) shows the

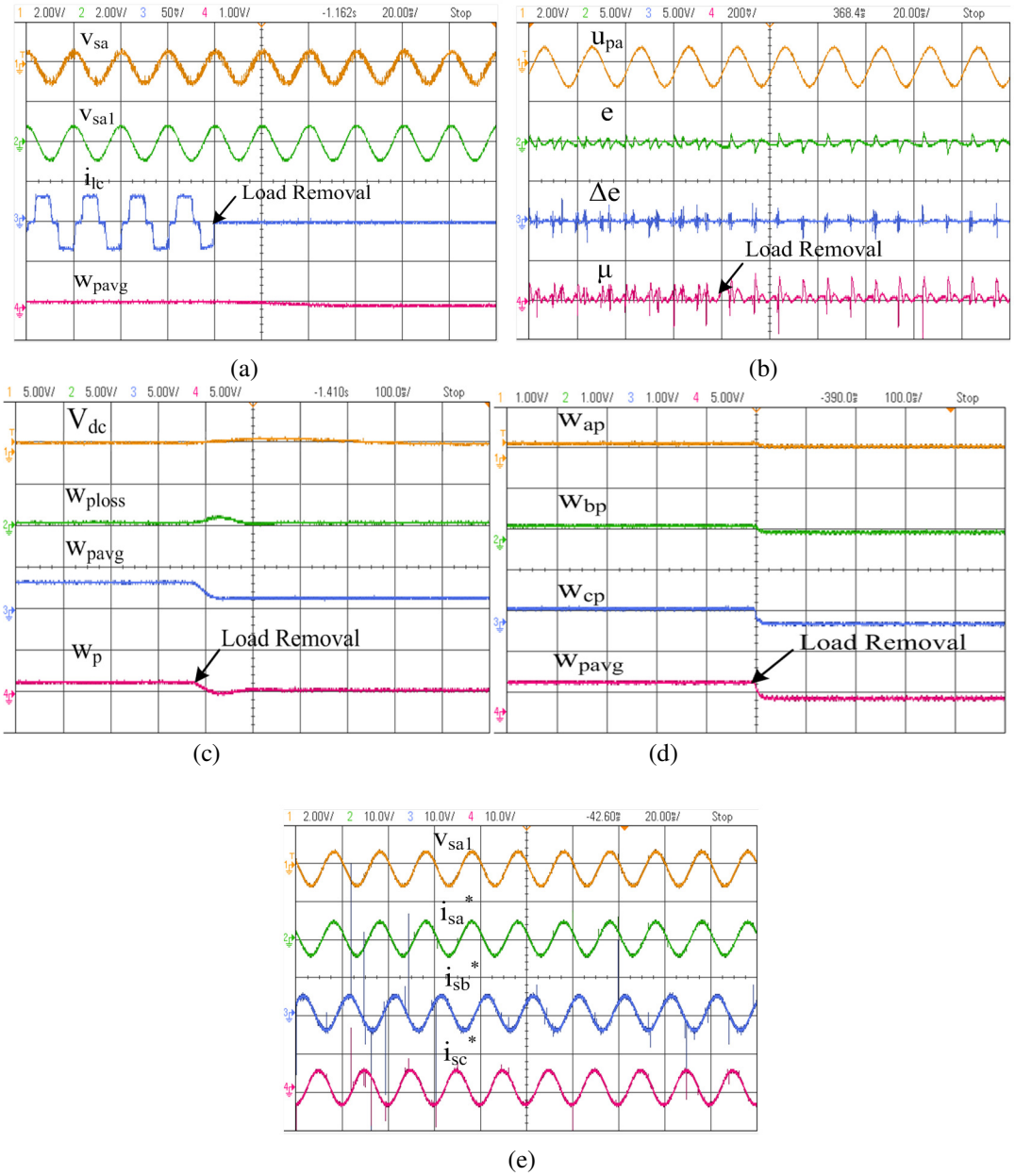


Fig. 7.35 Intermediate signals for dynamic load condition under nonlinear load (a) v_{sa}, v_{sa1} i_{lc} and w_{pavg} (b) $u_{pa,}$ e, Δe and μ (c) V_{dc}, w_{ploss}, w_{pavg} and w_p (d) w_{ap}, w_{bp}, w_{cp} and w_{pavg} (e) v_{sa1}, i_{sa}^*, i_{sb}^* and i_{sc}^*

weights corresponding to the fundamental active power components of three phase load currents (w_{ap}, w_{bp} and w_{cp}) along with their average weight (w_{pavg}). These results are presented for varying load conditions when phase 'c' load current is switched off. Fig. 7.35(e) shows reference currents (i_{sa}^*, i_{sb}^* and i_{sc}^*) along with filtered PCC voltage (v_{sa1}). These results show satisfactory

performance of ANFIS-LMS based control algorithm for control of DSTATCOM is satisfactory.

B. Performance of DSTATCOM Under Steady State Condition Using ANFIS-LMS Based Control Algorithm

Fig. 7.36 depicts the performance of the DSTATCOM under steady state condition. Figs. 7.36(a)-(c) show the waveforms of the phase 'a' supply current (i_{sa}), load current (i_{la}) and DSTATCOM current (i_{Ca}) along with PCC voltage (v_{ab}). The harmonic spectra of phase 'a' of supply current (i_{sa}), load current (i_{la}) and PCC voltage (v_{ab}) are shown in Figs. 7.36 (d)-(f).The THD of 4.9%, 24.7% and 3.9% are obtained in i_{sa}, i_{la} and v_{ab} respectively. It is observed from these results that the THDs of supply current and PCC voltage lie within the limits specified by IEEE-519 standard.

Fig. 7.37 shows the simulation study at 110V, 50Hz system for which experimental system is developed in the laboratory. These results present the waveforms of PCC voltages (v_{sa}), supply currents (i_{sa}), load currents (i_{sa}), compensator currents (i_{Ca}) and DC bus voltage (V_{dc}). Supply

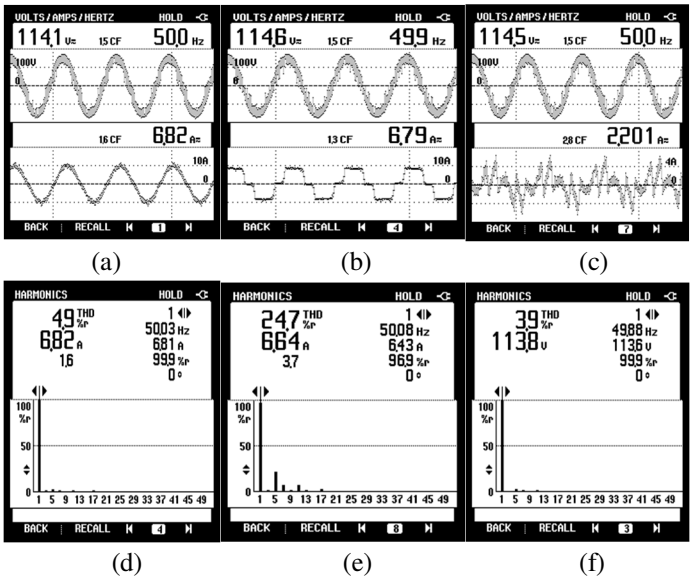


Fig. 7.36 Steady state performance of DSTATCOM under nonlinear load (a) v_{ab} and i_{sa} (b) v_{ab} and i_{la} (c) v_{ab} and i_{Ca} (d) harmonic spectrum of i_{sa} (e) harmonic spectrum of i_{la} and (f) harmonic spectrum of v_{ab}.

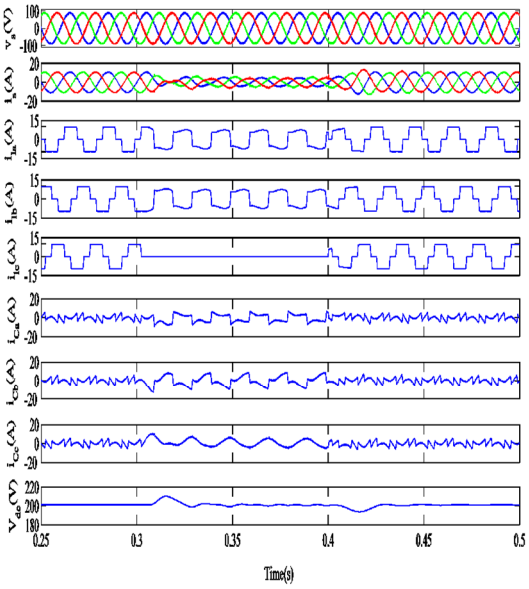


Fig. 7.37 Simulated performance of DSTATCOM in PFC mode

currents are observed to be balanced and sinusoidal during steady state (before t=0.3s) and unbalanced load conditions (t=0.3s to t=0.4s). The voltage at the DC bus is regulated at the reference value of 200V due to the action of PI controller.

C. Dynamic Performance of DSTATCOM Using ANFIS-LMS Based Control Algorithms

The dynamic performance of shunt compensator is recorded with oscilloscope and depicted in Fig. 7.38. Figs. 7.38(a)-(c), show waveforms of supply currents (i_{sa}, i_{sb} and i_{sc}), load currents (i_{la},

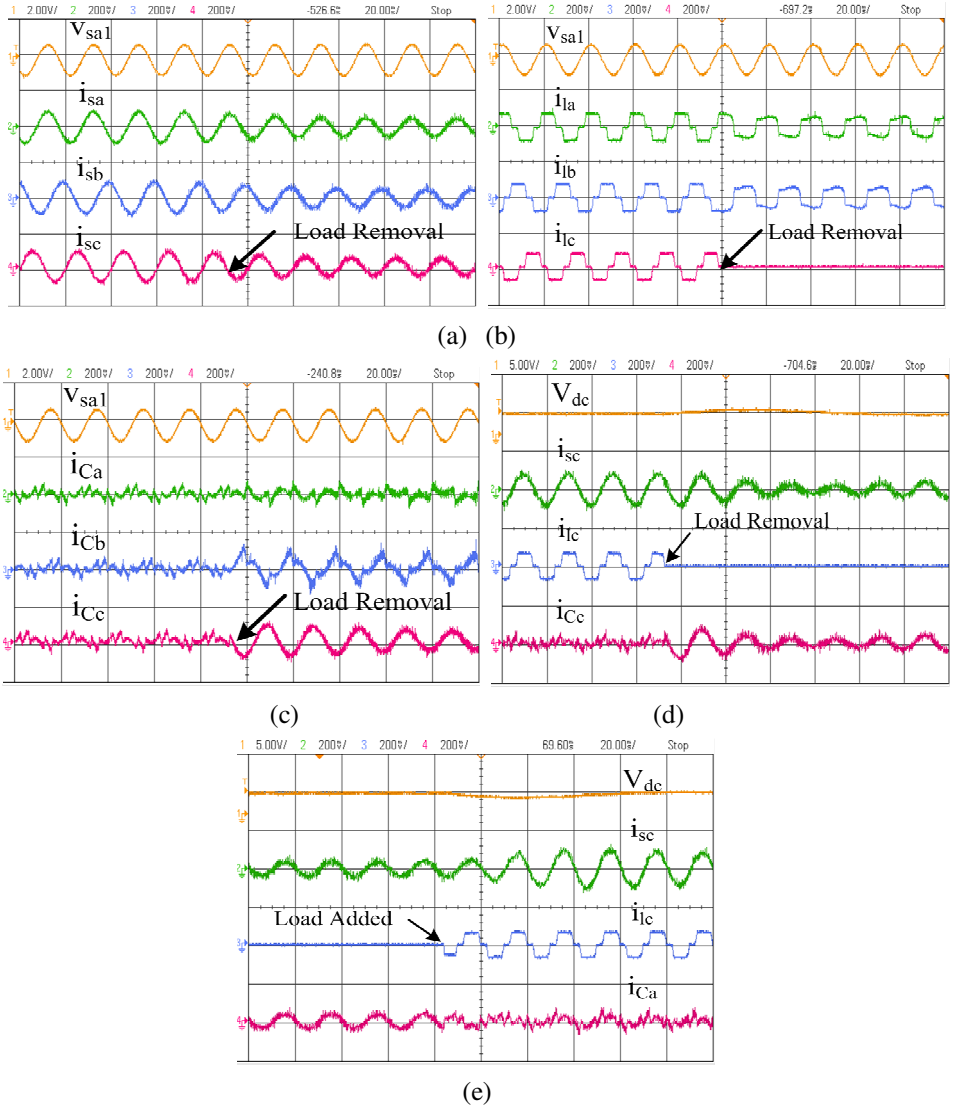


Fig. 7.38 Performance of shunt compensator for dynamic load condition under nonlinear load (a) v_{sa}, i_{sa}, i_{sb} and i_{sc} (b) v_{sa}, i_{la}, i_{lb} and i_{lc} (c) v_{sa}, i_{Ca}, i_{Cb} and i_{Cc} (d) V_{dc}, i_{sc}, i_{lc} and i_{Cc} for load removal (e) V_{dc}, i_{sc}, i_{lc} and i_{Cc} for load added

i_{lb} and i_{lc}) and DSTATCOM currents (i_{Ca}, i_{Cb} and i_{Cc}) along with filtered PCC voltage (v_{sa1}) under both steady state and unbalanced load conditions. It is observed from these results that the supply currents are sinusoidal and balanced with reduced magnitude, when phase 'c' load is disconnected. Figs. 7.38(d) and (e) show the waveforms of the DC bus voltage (v_{dc}), phase 'c' supply current (i_{sc}), phase 'c' load current (i_{lc}) and phase 'c' compensator current (i_{Cc}) in balanced and unbalanced load conditions for both load removal and load added respectively. It is observed from this result that the DC bus voltage achieves its reference value within a few cycles. Test results depict satisfactory performance of DSTATCOM under varying load conditions with ANFIS-LMS based control algorithm.

7.7 CONCLUSION

This chapter has presented the basic principle, mathematical formulation and performance of the system with artificial intelligence based control algorithms for control of DSTATCOM. Simulation and experimental results have been demonstrated for three artificial intelligence based theories such as ANFIS, RTRL and ALFIS-LMS. The theoretical concepts related to these control algorithms, their MATLAB/SIMULINK models and their realization into DSP have been discussed. The fundamental weight extraction from load currents using the three techniques and their application for control of DSTATCOM in PFC and voltage regulation modes have been given. The performance of these control algorithms has been tested for mitigating power quality problems such as harmonic current reduction and load unbalancing. Experimental validation of these control algorithms have been performed with developed DSTATCOM prototype in the laboratory. The results have shown that the ANFIS, RTRL and ANFIS-LMS based control algorithms have given the THDs of 3.3%, 2.2% and 4.9% in supply currents respectively.

CHAPTER-VIII
DSTATCOM APPLICATION TO GRID INTEGRATION OF SPV ARRAY

8.1 GENERAL

In the previous chapters, the design and development of control algorithms have been presented for the control of DSTATCOM. These control algorithms have been divided into four categories viz. conventional control algorithms, adaptive theory based control algorithms, recursive theory based control algorithms and artificial intelligence based control algorithms. This chapter presents an application of DSTATCOM to grid integration of solar photovoltaic (SPV) array. A SPV array is connected at the DC link of the DSTATCOM. The real power demand of linear and nonlinear loads along with functions of DSTATCOM such as harmonics elimination, reactive power compensation and load balancing are demonstrated in power factor correction (PFC) and voltage regulation modes along with grid connected SPV array.

A two stage SPV power generating system is used to feed active power to the grid. The first stage consists of SPV power tracked using maximum power point tracking (MPPT) technique realized through a DC-DC boost converter. This stage presents the design of SPV array, MPPT and DC-DC boost converter. The second stage consists of coupling SPV generating system with the grid using VSC and suitable control algorithm. This stage involves the design of DC bus voltage, DC bus capacitance, VSC rating, interfacing inductors and ripple filters. The control algorithm for the control of three phase VSC is designed to evacuate power generation from SPV array during day time and provides reactive power compensation, harmonics compensation and load balancing under linear and nonlinear loads. This system is designed and modeled using MATLAB environment using SIMULINK and Sim Power System (SPS) tool boxes. The detailed description of the system configuration and design of various components of grid connected SPV power generation system are presented in the subsequent sections.

8.2 SYSTEM CONFIGURATION OF GRID INTEGRATED SPV SYSTEM

Figs. 8.1(a) and (b) show the schematic diagram and MATLAB model of the grid connected SPV system. A three-phase, AC mains with the grid impedance (series R_s-L_s branch), feeds a three phase linear and nonlinear loads. The proposed system consists of SPV array, DC-DC boost converter and a voltage source converter (VSC). The DC-DC boost converter is used to boost output voltage of SPV array designed using inductor (L_b), diode (D) and IGBT as a switch. The DC-AC conversion is performed with the help of three phase VSC and it also functions as a DSTATCOM. The VSC comprises of six insulated gate bipolar transistors (IGBTs) with anti-parallel diodes and DC link capacitor (C_{dc}) at DC side. Interfacing inductors (L_f) are used at the AC side of VSC, which couple the VSC to the grid. The high frequency switching noise generated by switching of IGBTs of VSC is reduced with the help of series connected capacitive (C_f) and resistive (R_f) elements at the point of common coupling (PCC). The linear load is represented as a combination of three series R-L branches connected in star configuration. The nonlinear load is represented as an uncontrolled bridge rectifier with series R-L branch. Voltages at PCC (v_{sa}, v_{sb}), supply currents (i_{sa}, i_{sb}), load currents (i_{la}, i_{lb}) and DC bus voltage (V_{dc}) are sensed and fed to the control algorithm. The design and selection of SPV array, DC-DC boost converter parameters, DC bus voltage, interfacing inductors and ripple filters are presented in the next section.

8.3 DESIGN OF GRID CONNECTED SPV SYSTEM

The SPV system comprises a 20kW solar photovoltaic array. The maximum voltage of PV array is tracked by maximum power point tracking (MPPT) algorithm. The SPV voltage is boosted by DC-DC boost converter. The DC output voltage of the PV array has to be converted into three

phase AC by the VSC which is coupled to the grid. Interfacing Inductors and ripple filters are suitably designed and connected to obtain sinusoidal voltage waveform. The design parameters of SPV system are given in Appendix-D. The detailed design of components used for grid connected SPV system is discussed as follows.

8.3.1 Design of Solar Photovoltaic Array [202]

The photovoltaic (PV) cell is the basic unit of the PV array. It is a semiconductor diode which converts sun light into electricity by exposing its p-n junction to light. The semiconductor device is made of silicon material (fabrication process is economically feasible in large scale), and gives output voltage around 0.5V to 0.7V under open circuit condition. The light incident on the solar cell generates charge carrier that causes electric current to flow if the cell is short circuited.

The solar photovoltaic array is designed for providing a 20kW peak power capacity. Each cell

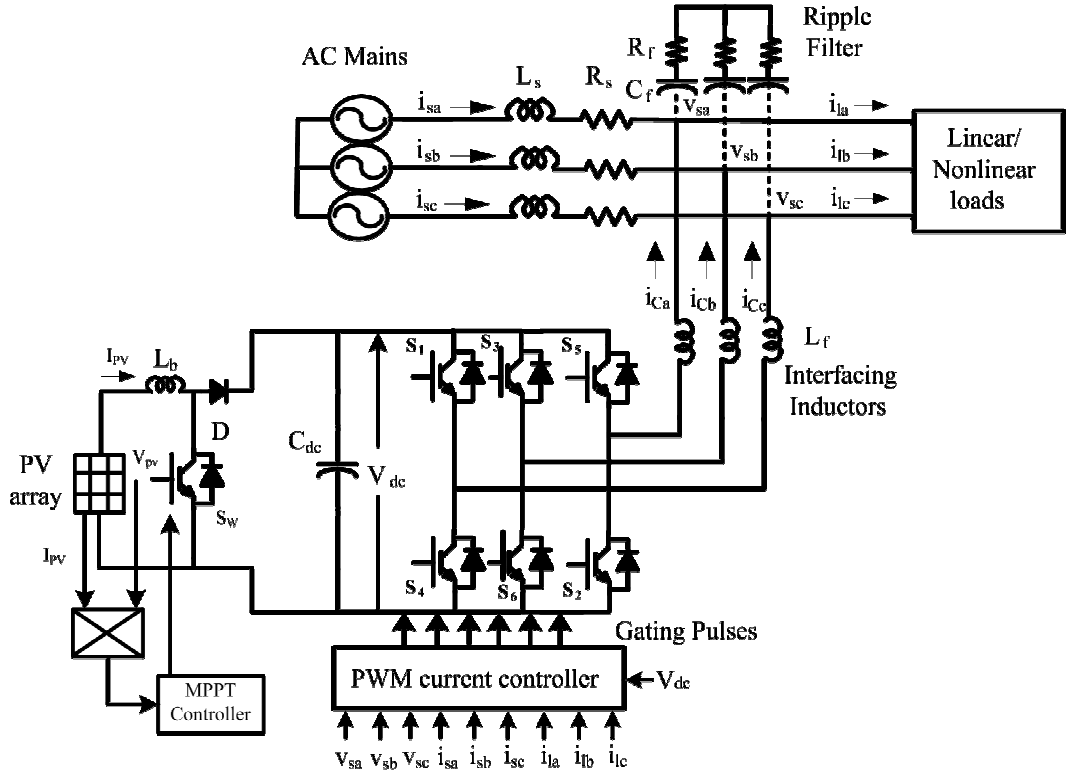


Fig. 8.1(a) System configuration of grid connected SPV system

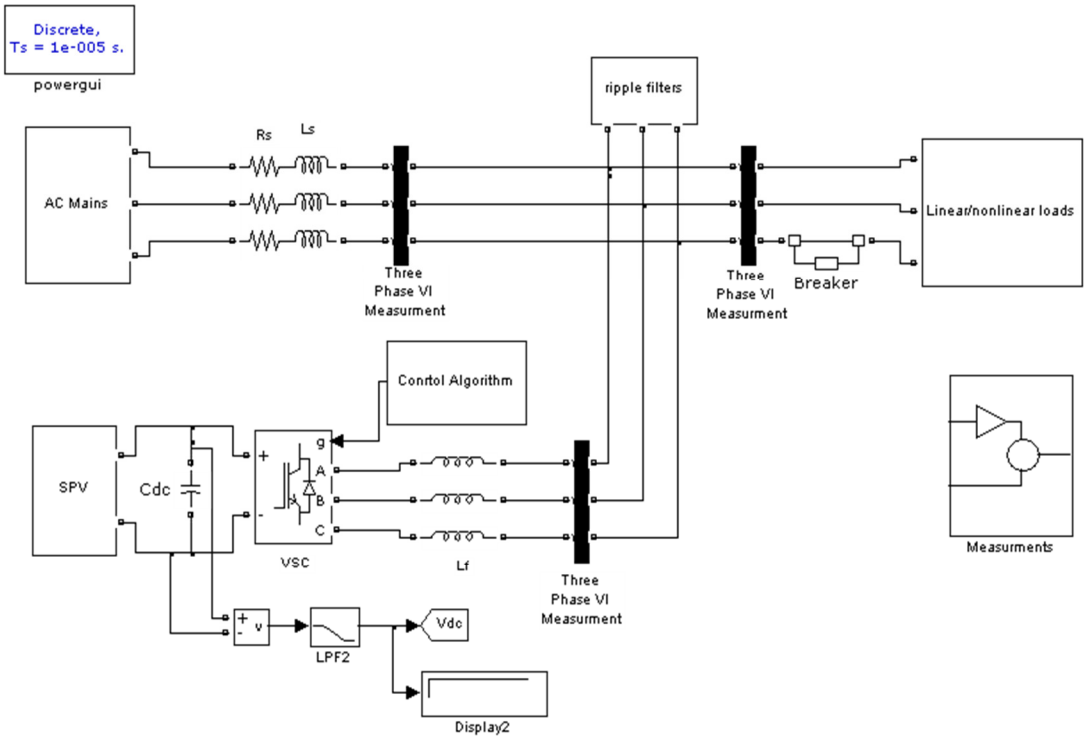


Fig. 8.1(b) MATLAB model of grid connected SPV system

has 0.62V of open circuit voltage and 4A of short circuit current. One module has 30 series cells which produce 30*0.62=18.6V of open circuit voltage and 4A of short circuit current. Maximum power for each module occurs at product of 85% of open circuit voltage (18.6*85%=15.81V) and 85% of short circuit current (4*85%=3.4A). The formation of solar PV array is made by combining these modules appropriately in series and parallel. To achieve a 20kW of peak power capacity 43 such modules are required in series and 9 such modules are required in parallel.

8.3.2 Maximum Power Point Tracking

The characteristics of SPV system are exponential in nature and depend upon the weather conditions. It is required to track the maximum power point to improve the efficiency of SPV system. The aim of maximum power point tracking (MPPT) is that the SPV array always operates at specified value of output voltage and current. Therefore, MPPT is required to adjust

the SPV array output voltage and current to appropriate values to provide maximum power to the grid. The tracking of maximum power point (MPP) requires implementation of suitable MPPT algorithm along with a DC-DC boost converter. This method computes the maximum power point by comparing the incremental conductance and the array conductance. When these two quantities appear to be same then the output voltage is termed as the maximum power point voltage. The controller maintains this voltage until the irradiation level is changed and process is repeated again. Moreover, at MPP the slope of PV characteristic curve is zero. The incremental conductance algorithm is implemented as follows [206].

$dP/dV = 0$ at MPP (8.1)

$dP/dV > 0$ left of MPP (8.2)

$dP/dV < 0$ right of MPP (8.3)

The MPPT algorithm is based as,

$$dP/dV = I + V\, dI/dV \approx I + V\, \Delta I/\Delta V \tag{8.4}$$

If the relation $dP/dV = 0$, then the conditions for MPP are derived as,

$\Delta I/\Delta V = -I/V$ at MPP (8.5)

$\Delta I/\Delta V > -I/V$ left of MPP (8.6)

$\Delta I/\Delta V < -I/V$ right of MPP (8.7)

Eqn. (8.6) and (8.7) are used to find out the direction of voltage perturbation when the operating point moves towards to the maximum power point. In this process, the terminal voltage of SPV array continuously perturbs until the condition of $\Delta I/\Delta V = -I/V$ reaches.

The flow-chart for the incremental conductance algorithm is shown in Fig. 8.2 and I-V and P-V characteristics of SPV system are shown in Fig. 8.3. The values of V(k) and I(k) at two successive instants are obtained and then the incremental changes in voltage and current are obtained using dV(k)=V(k)–V(k-1) and dI(k)=I(k)–I(k-1). The instant when the condition

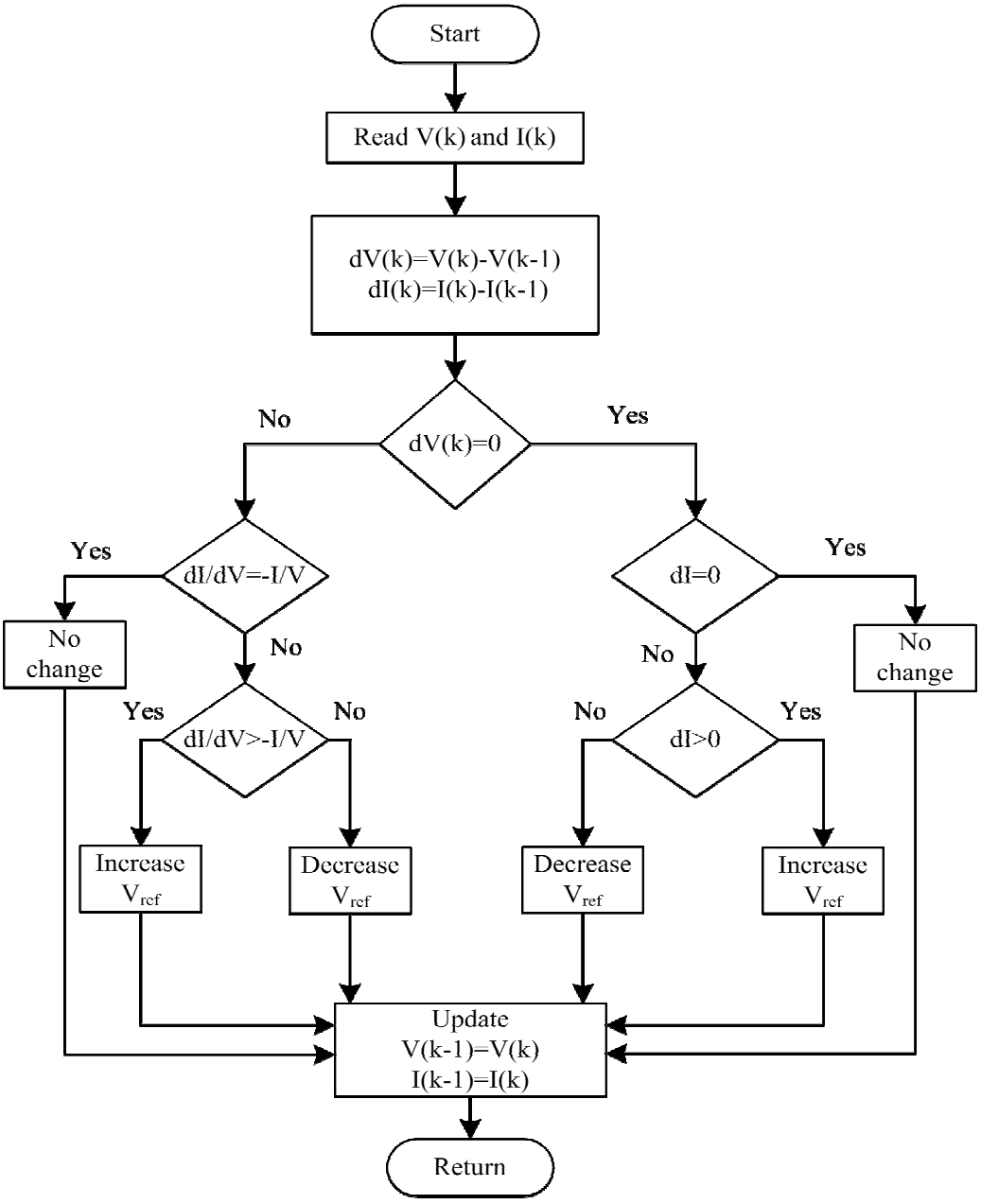
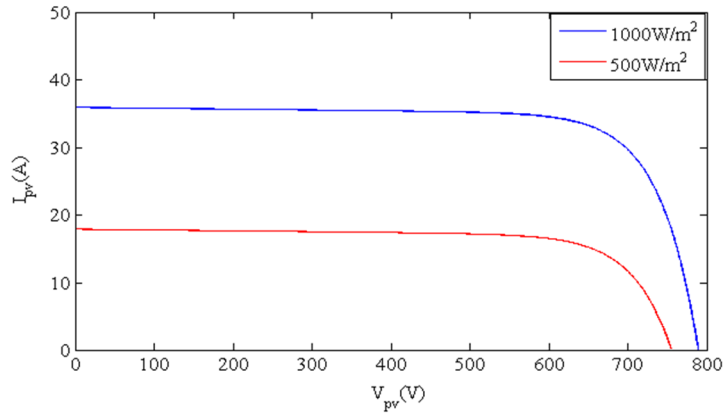


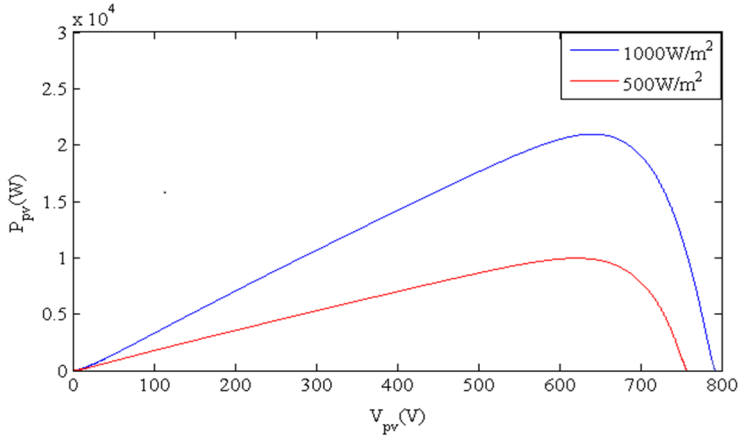
Fig. 8.2 Flow chart of incremental conductance based MPPT

dV(k)=0 is true, is determined. If the condition dI=0 is also satisfied simultaneously, then MPP has been determined.

If the condition of dI>0 occurs then it represents that the sun irradiance increases and reference voltage (V_{ref}) of MPP needs to increase. Another check is carried out by comparing ΔI/ΔV against –I/V, based upon this the control reference signal V_{ref}, is adjusted. Now if the condition dI/dV= –I/V occurs, no control action is required, and the algorithm updates the stored parameters. Furthermore if, it is observed that dI/dV> –I/V, then the reference voltage of PV array is located at the left side of MPP, and has to be raised in order to track the maximum power point. On the other hand, if ΔI/ΔV< –I/V, the operating voltage of PV module is located on the



(a)



(b)

Fig. 8.3 SPV array curves (a) current-voltage (I-V) (b) power-voltage (P-V)

right side of the MPP in PV array, and the reference voltage has to be reduced in order to get MPP. The reference PV array voltage (V_{ref}), is determined by this MPPT algorithm. This V_{ref} and DC bus voltage (V_{dc}) is used to estimate reference duty ratio for the boost converter. The reference duty ratio can be estimated as,

$$d(k) = 1 - \frac{V_{ref}(k)}{V_{dc}(k)} \tag{8.8}$$

This reference duty ratio is compared with saw-tooth waveform of 10kHz, to generate switching for the IGBT of boost converter.

8.3.3 Design of DC-DC Boost Converter

Figs. 8.4(a) and (b) show a DC-DC boost converter and its MATLAB model implemented for SPV system. The DC-DC converter converts a PV voltage to a constant DC voltage level thus providing a regulated output. It is designed to boost voltage at higher level. The design and selection of parameters for DC-DC boost converter are given as follows [203].

8.3.3.1 Design and Selection of Inductor

In the design of DC-DC boost converter, an inductor is designed. The inductor is selected based on the maximum allowed ripple current (Δi_1) for minimum duty cycle (D), at maximum input voltage (V_{pv}). The value of the input inductor (L_b) is given as,

$$L_b = \left(V_{pv} D\right) \Big/ \left(2\Delta i_1 f_{sb}\right) = \frac{680 \times 0.15}{2 \times 3.05 \times 10000} = 1.67\text{mH} \tag{8.9}$$

where D is the duty cycle given as,

$$D = 1 - \frac{V_{in}}{V_b} = 1 - \frac{680}{800} = 0.15 \tag{8.10}$$

The converter is designed to boost $V_{pv}=V_{in}=680V$ to $V_b=800V$. Thus, the calculated value of duty cycle (D) is around 0.15. The current Δi_l is the output current ripple and the value of ripple current is considered to be 10% of the input current which is considered as 30.5A. The value of Δi_l is calculated to be 3.05A, switching frequency (f_{sb}) is selected 10kHz and from the above calculated parameters, the value of inductor is selected as 1.67mH.

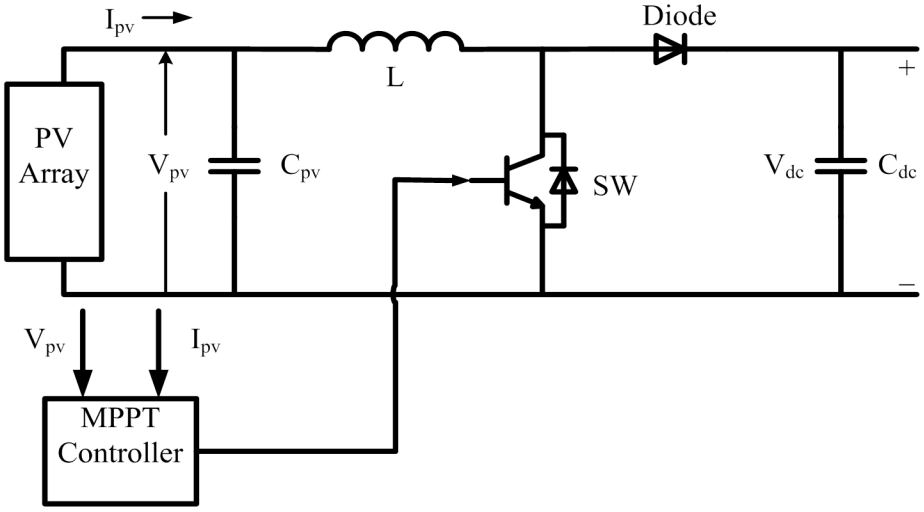


Fig. 8.4 (a) Schematic diagram of DC-DC boost converter

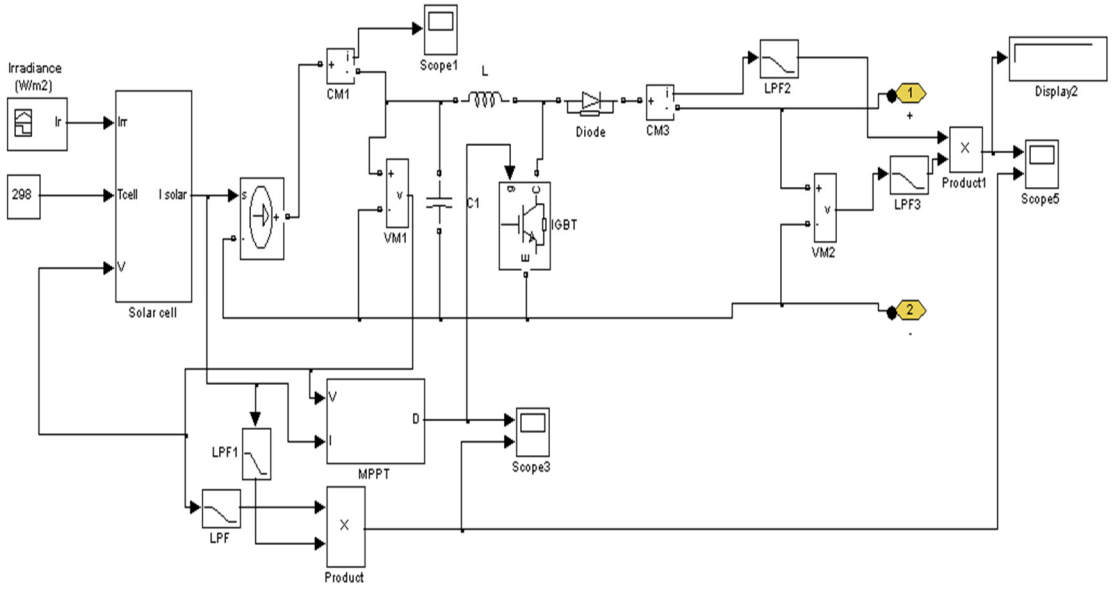


Fig. 8.4 (b) MATLAB model DC-DC boost converter

8.3.3.2 Selection of the Diode

The design considerations to be taken into account while selecting diode for DC-DC boost converter are its ability to block the required off-state voltage stress (V), have sufficient peak (A) and average current (A) handling capability, fast switching characteristic, low reverse recovery and low forward voltage drop.

8.3.4 Design of Three Phase Voltage Source Converter

A three phase VSC is used to convert the DC output voltage from SPV array to AC voltage. The VSC comprises of six IGBTs (insulated gate bipolar transistor) with antiparallel diodes. This is used for active power transfer to the grid, harmonics elimination and reactive power compensation. The design of VSC for 415V, 20kW load at 0.8pf lagging is presented here. The VSC rating is calculated around 23.32kVA and selected of 25kVA. The value of per phase load current for per phase r.m.s voltage, 239.6V is around 34.86A. This current is required to meet active power demand of load and reactive power compensation. The rating considered for harmonics elimination is 20%. Therefore, the peak current rating of device is selected around 41.83A. If two time safety factor is considered, then the device current rating becomes 83.66A. The load r.m.s. voltage is considered as 415V and peak voltage corresponds to 415*$\sqrt{2}$ V, which is around 586.89V. If a safety factor of two is considered, then the device voltage rating becomes 1200V.

8.3.5 Design of DC Bus Capacitance

The value of DC bus capacitance of the VSC for load balancing is given as [203],

$$C_d = \frac{I_d}{2*\omega*v_{dcripple}} = \frac{28.57}{2\times314\times32} = 1422\mu F \quad (8.11)$$

where I_d is the DC link current given by P_{dc}/V_{dc}, ω is angular frequency and $v_{dcripple}$ is considered 4% of DC bus voltage (V_{dc}). From Eqn. (8.11) the value of DC bus capacitance is calculated to

be 1422μF. The calculated value of DC bus capacitance is maximum by energy conservation criteria. A higher value of 1650 μF is selected for design consideration.

8.3.6 Design of Interfacing Inductors

Design of interfacing inductor (L_f) is given as [203],

$$L_f = {\sqrt{3}mV_{dc}}\Big/{(12af_s i_{crpp})} = \frac{\sqrt{3}\times 800}{12\times 1.2\times 10000\times 3.2} = 3\text{mH} \quad (8.12)$$

where m is the modulation index, V_{dc} DC bus voltage, f_s is switching frequency, a is overloading factor selected to be 1.2 and i_{crpp} is current ripple of the 10% of VSC current. The value of the interfacing inductor is calculated 3mH and selected to be around 3.2mH.

8.4 BASIC PRINCIPLE AND MATHEMATICAL FORMULATION OF CONTROL ALGORITHMS FOR GRID CONNECTED SPV SYSTEM

This section presents the basic principle and mathematical formulation of control algorithm for grid connected SPV system. The control algorithms presented for control of SPV system are based on SRFT, Wiener filter and recursive inverse algorithm. The control algorithms are designed to perform real power evacuation along with achieving functions of DSTATCOM in PFC and voltage regulation modes under linear and nonlinear loads.

8.4.1 Synchronous Reference Frame Theory Based Control Algorithm

The synchronous reference frame theory (SRFT) is based on the transformation of load currents into synchronously rotating d-q frame. The estimation of reference supply currents for the control of VSC is performed here with SRFT based control algorithm [9]. The detailed mathematical formulation of the control algorithm is given as follows.

8.4.1.1 Estimation of Fundamental Active Power Components of Reference Supply Currents

Fig. 8.5 shows the block diagram of SRFT based control algorithm. The PCC voltages (v_{sa}, v_{sb} and v_{sc}), supply currents ($i_{sa,}$ i_{sb} and i_{sc}) load currents (i_{la}, i_{lb} and i_{lc}) and DC bus voltage (V_{dc}) are sensed and fed back to the control algorithm. The load currents are transformed from abc to dq0 frame using following transformation.

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_{la} \\ i_{ib} \\ i_{ic} \end{bmatrix} \tag{8.13}$$

In the synchronously rotating frame, all the components of load currents at fundamental frequency (ω) are transformed into DC quantity, given as,

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \cos \omega t & \sin \omega t \\ -\sin \omega t & \cos \omega t \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{8.14}$$

The active current component (i_d) obtained from the above given transformation contain AC ripple component (i_{dac}) and fundamental DC component (i_{ddc}) of load currents. A low pass filter (LPF) is used to extract fundamental DC component of load current.

The voltage at DC bus (V_{dc}) is sensed and compared with reference DC bus voltage (V_{dc}^*), thus the voltage error at n^{th} sampling instant is computed as,

$$v_{de}(n) = V_{dc}^*(n) - V_{dc}(n) \tag{8.15}$$

The voltage error $v_{de}(n)$, is passed through a proportional integrator (PI) controller. The output of the PI controller is used to provide sufficient current component for regulating DC bus voltage and to meet DSTATCOM system losses. The output of PI controller (i_{pdc}) at n^{th} sampling instant is given as,

$$i_{pdc}(n) = i_{pdc}(n-1) + k_{pd}\{v_{de}(n) - v_{de}(n-1)\} + k_{id} v_{de}(n) \tag{8.16}$$

where k_{pd} and k_{id} are the proportional and integrator gains of PI controller for regulating DC bus voltage.

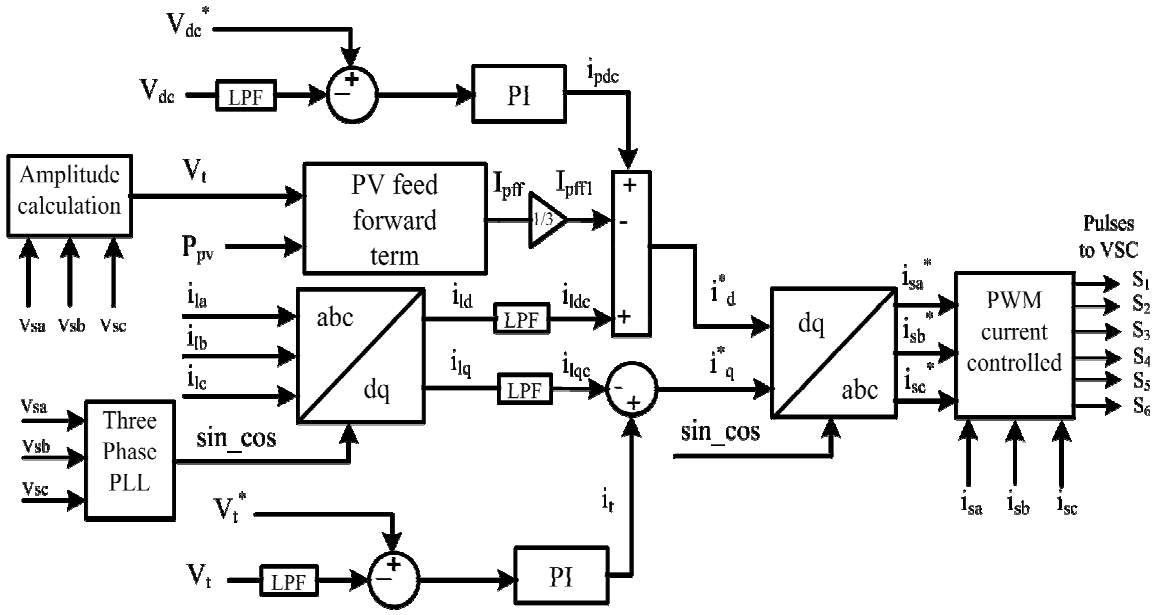


Fig. 8.5 Block diagram of SRFT based control algorithm

The total SPV power (P_{pv}) is equally divided in all three phases with respect to grid. Instantaneous feed forward compensation term (I_{pff}) of SPV system is computed for all three phases as,

$$I_{pff} = {2P_{pv}}/{V_t} \tag{8.17}$$

For three phase system, this term (I_{pff}) is divided by three to equally divide in all three phases and effective instantaneous feed forward compensation term (I_{ppf1}) is computed.

The reference active component of supply current (i_d^*) is estimated from output of DC bus PI controller (i_{pdc}), fundamental DC current component of load current (i_{ldc}) and instantaneous compensation term (I_{pff1}) as,

$$i_d^* = i_{pdc} + i_{ldc} - I_{pff1} \tag{8.18}$$

The reference active power component (i_d^*) is used to generate active current components of reference supply currents.

8.4.1.2 Estimation of Fundamental Reactive Power Components of Reference Supply Currents

The amplitude terminal voltage (V_t) at PCC is calculated as,

$$V_t = \sqrt{\frac{2}{3}\left(v_{sa}^2 + v_{sb}^2 + v_{sc}^2\right)} \tag{8.19}$$

The error (v_{te}) between reference PCC voltage amplitude (V_t^*) and actual PCC voltage amplitude (V_t) are evaluated and passed through a PI controller to generate reactive component of current (i_t) for voltage regulation. The reference reactive component (i_q^*) estimated by subtracting the reactive current component (i_{lqc}) of load from the output of AC bus PI controller (i_t) as,

$$i_q^* = i_t - i_{lqc} \tag{8.20}$$

This reference reactive component is used to estimate the reference reactive supply currents.

8.4.1.3 Generation of Reference Supply Currents and Switching Pulses

At fundamental frequency, the reference active and reactive components of currents (i_d^* and i_q^*) are converted to αβ components, which can then be easily converted into reference supply currents (i_{sa}^*, $i_{sb}^*$and i_{sc}^*) by reverse Clark transformation as,

$$\begin{bmatrix} i_\alpha^* \\ i_\beta^* \end{bmatrix} = \begin{bmatrix} \cos\omega t & -\sin\omega t \\ \sin\omega t & \cos\omega t \end{bmatrix} \begin{bmatrix} i_d^* \\ i_q^* \end{bmatrix} \tag{8.21}$$

$$\begin{bmatrix} i_{sa}^* \\ i_{sb}^* \\ i_{sc}^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_\alpha^* \\ i_\beta^* \end{bmatrix} \tag{8.22}$$

These reference supply currents (i_{sa}^*, $i_{sb}^*$and i_{sc}^*) are compared with the sensed supply currents (i_{sa}, i_{sb} and i_{sc}) and current errors are achieved. These current errors are then passed through PWM current controller for generation of gating pulses for VSC.

8.4.2 Wiener Filter Based Control Algorithm for Grid Connected SPV System

Wiener filter based control algorithm is used here to estimate reference supply for control of VSC. The Wiener filtering technique is known as linear optimization discrete time filter [154]. This requires a priori information about the data to be processed.

8.4.2.1 Estimation of Fundamental Active Power Components of Reference Supply Currents

Fig. 8.6 shows the block diagram of control algorithm where voltages (v_{sa}, v_{sb} and v_{sc}) at the PCC are sensed and their amplitude is calculated as,

$$V_t = \sqrt{2(v_{sa}^2 + v_{sb}^2 + v_{sc}^2)/3} \tag{8.23}$$

Using PCC voltage magnitude, the unit inphase components are calculated as,

$$u_{pa} = v_{sa}/V_t; u_{pb} = v_{sb}/V_t; \text{and } u_{pc} = v_{sc}/V_t \tag{8.24}$$

The voltage at DC bus (V_{dc}) of the VSC is sensed and subtracted from the reference DC bus voltage (V_{dc}^*) for generation of error signal (v_{de}). The error signal is passed through the proportional integral (PI) controller. The output of PI controller (w_{pdc}) regulates the DC bus voltage at reference value and also meets VSC losses. The PI controller output at n^{th} sampling instant is given as,

$$w_{pdc}(n) = w_{pdc}(n-1) + k_{pd}\{V_{de}(n) - V_{de}(n-1)\} + k_{id}\{V_{de}(n)\} \tag{8.25}$$

where k_{pd} and k_{id} are proportional and integral gains of DC bus PI controller.

Extraction of weights (w_{ap}, w_{bp} and w_{cp}) corresponding to fundamental active power component of load currents are same as given in section 5.3.1. The weights corresponding to fundamental active power component of load currents for the three phases are obtained as,

$$w_{ap}(n+1) = [I - 2\mu R_{xa}]w_{ap}(n) + 2\mu P_{dxa} \tag{8.26}$$

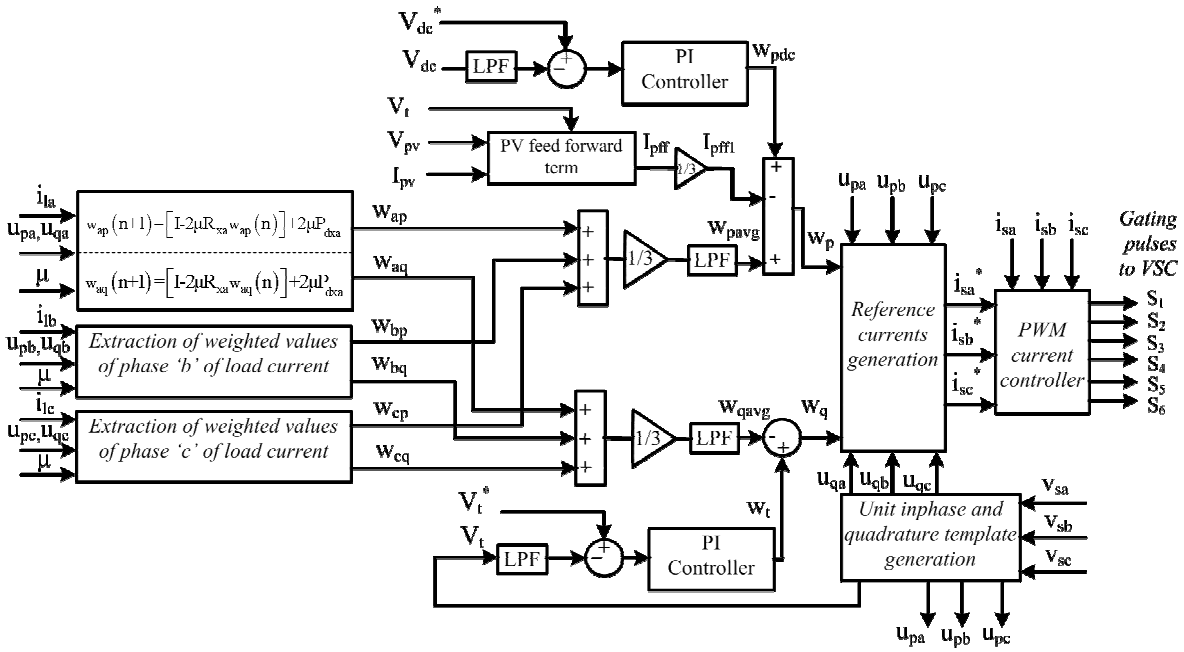


Fig. 8.6 Block diagram of Wiener filter based control algorithm for grid connected SPV system

$$w_{bp}(n+1) = [I - 2\mu R_{xb}]w_{bp}(n) + 2\mu P_{dxb} \tag{8.27}$$

$$w_{cp}(n+1) = [I - 2\mu R_{xc}]w_{cp}(n) + 2\mu P_{dxc} \tag{8.28}$$

The average magnitude of weights (w_{pavg}) corresponding to active power components is given as,

$$w_{pavg} = (w_{ap} + w_{bp} + w_{cp})/3 \tag{8.29}$$

The computation of SPV instantaneous feed forward compensation term (I_{pff}) for all three phases is given as,

$$I_{pff} = {}^{2P_{pv}}\!/_{V_t} \tag{8.30}$$

In three phase system for all three phases this term is divided by three and effective SPV instantaneous feed forward compensation term (I_{pff1}) is computed.

The total reference weight (w_p) corresponding to active power component is obtained by the average weight (w_{pavg}), output of DC bus PI controller (w_{pdc}) and I_{pff1} as,

$$w_p = w_{pavg} + w_{pdc} - I_{pff1} \tag{8.31}$$

The reference currents $\left(i_{pa}^*, i_{pb}^* \text{and } i_{pc}^*\right)$ corresponding to fundamental active components are estimated by using unit inphase templates (u_{pa}, u_{pb} and u_{pc}) and reference active power weight (w_p) as,

$$i_{pa}^* = w_p u_{pa},\ i_{pb}^* = w_p u_{pb} \text{ and } i_{pc}^* = w_p u_{pc} \tag{8.32}$$

These active reference supply currents $\left(i_{pa}^*, i_{pb}^* \text{and } i_{pc}^*\right)$ are used to estimate reference supply currents.

8.4.2.2 Estimation of Fundamental Reactive Power Component of Reference Supply Currents

The unit quadrature vectors of PCC voltages are calculated from unit inphase voltages (u_{pa}, u_{pb} and u_{pc}) as,

$$u_{qa} = -u_{pb}/\sqrt{3} + u_{pc}/\sqrt{3} \tag{8.33}$$

$$u_{qb} = \sqrt{3}\,u_{pa}/2 + (u_{pb} - u_{pc})/2\sqrt{3} \tag{8.34}$$

$$u_{qc} = -\sqrt{3}\,u_{pa}/2 + (u_{pb} - u_{pc})/2\sqrt{3} \tag{8.35}$$

The voltage regulation using DSTATCOM can be performed using another PI controller. The error (v_{te}) between amplitude of PCC voltage (V_t) and its reference quantity (V_t^*) is calculated. The voltage error is passed through a PI controller and output (w_t) can be computed at n^{th} sampling instant as,

$$w_t(n) = w_t(n-1) + k_{pq}\{v_{te}(n) - v_{te}(n-1)\} + k_{iq}\{v_{te}(n)\} \quad (8.36)$$

where k_{pq} and k_{iq} are proportional and integral gains for AC bus voltage PI controller.

The extraction of weights (w_{aq}, w_{bq} and w_{cq}) corresponding to reactive power components of load currents is already presented in section 5.3.1. The weight corresponding to fundamental reactive power component of load current for the three phases are obtained as,

$$w_{aq}(n+1) = [I - 2\mu R_{xa}]w_{aq}(n) + 2\mu P_{dxa} \quad (8.37)$$

$$w_{bq}(n+1) = [I - 2\mu R_{xb}]w_{bq}(n) + 2\mu P_{dxb} \quad (8.38)$$

$$w_{cq}(n+1) = [I - 2\mu R_{xc}]w_{cq}(n) + 2\mu P_{dxc} \quad (8.39)$$

The average weight (w_{qavg}) of reactive power component of load currents can be calculated from the amplitude of load reactive weight components (w_{aq}, w_{bq} and w_{cq}) as,

$$w_{qavg} = (w_{aq} + w_{bq} + w_{cq})/3 \quad (8.40)$$

The amplitude of reactive power component of reference supply currents can be calculated by subtracting the output of PI controller (w_t), which is leading reactive power component used to compensate for voltage drop due to supply impedance and loading on the system and average reactive weight (w_{qavg}) given as,

$$w_q = w_t - w_{qavg} \quad (8.41)$$

The reference current corresponding to fundamental reactive power component can be calculated using Eqn. (8.37) to Eqn. (8.39) and Eqn. (8.41) as,

$$i_{qa}^* = w_q u_{qa},\ i_{qb}^* = w_q u_{qb} \text{ and } i_{qc}^* = w_q u_{qc} \quad (8.42)$$

These fundamental reactive components of reference supply currents are used along with fundamental active components of reference supply currents to generate reference supply currents given as follows.

8.4.2.3 Generation of Reference Supply Currents and Switching Pulses

The reference supply currents (i_{sa}^*, i_{sb}^* and i_{sc}^*) are estimated by addition of reference active (i_{pa}^*, i_{pb}^* and i_{pc}^*) and reactive (i_{qa}^*, i_{qb}^* and i_{qc}^*) components of supply currents as,

$$i_{sa}^* = i_{pa}^* + i_{qa}^*, i_{sb}^* = i_{pb}^* + i_{qb}^* \text{ and } i_{sc}^* = i_{pc}^* + i_{qc}^* \quad (8.43)$$

The supply currents (i_{sa}, i_{sb} and i_{sc}) are sensed and compared with these reference supply currents (i_{sa}^*, i_{sb}^* and i_{sc}^*) and the current errors (i_{sae}, i_{sbe} and i_{sce}) are generated. These current errors are passed through PWM current controller, which generates switching pulses for IGBTs of three phase VSC.

8.4.3 Recursive Inverse Based Control Algorithm

The recursive inverse based control algorithm is used for the estimation of reference supply currents for control of VSC used in SPV system. This algorithm is robust under distorted environment, with considerable reduction in computational complexity [172].

8.4.3.1 Estimation of Fundamental Active Power Component of Reference Supply Currents

Fig. 8.7 shows the block diagram of recursive inverse based control algorithm. Three phase PCC voltages (v_{sa}, v_{sb} and v_{sc}) are sensed and magnitude (V_t) is calculated same as given by Eqn. (8.23) in section 8.4.2. Unit inphase templates are calculated from PCC voltages and their magnitude same as given in section 8.4.2. The voltage at DC bus (V_{dc}) of VSC is sensed and

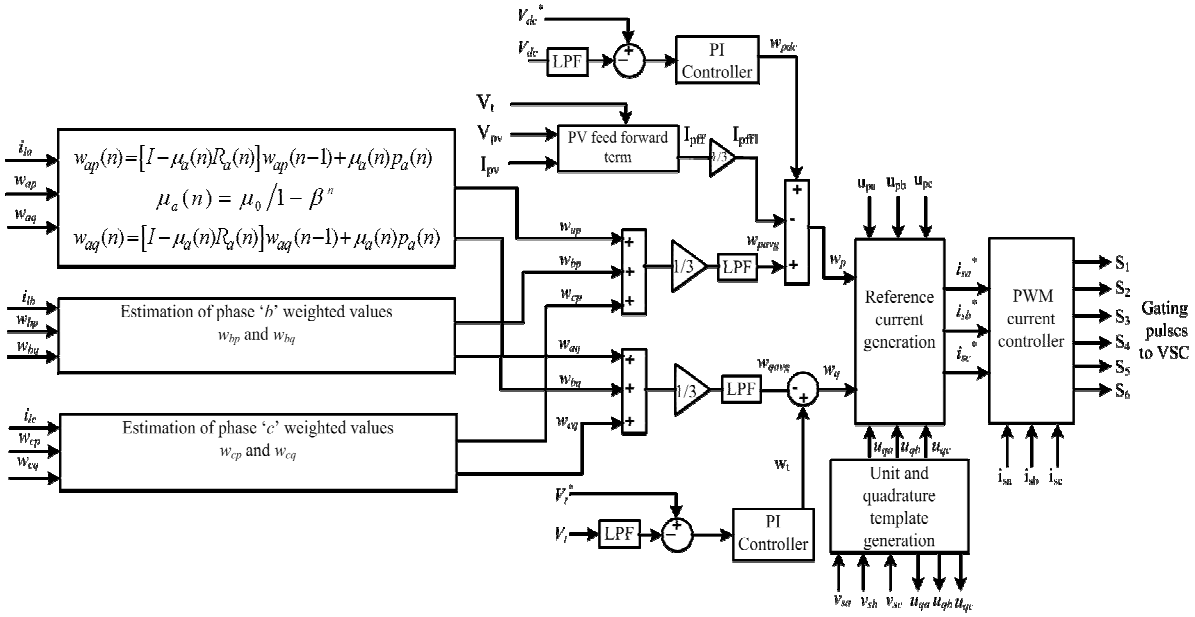


Fig. 8.7 Block diagram of recursive inverse based control algorithm for grid connected SPV system

compared with reference DC bus voltage (V_{dc}^{*}), thus the generated error is passed through the PI controller. The output (w_{pdc}) of DC bus PI controller is same as given in section 8.4.2.

The fundamental weights (w_{ap}, w_{bp} and w_{cp}) corresponding to active power component of load currents are extracted by recursive inverse technique same as given in section 6.3.2. The weights corresponding to fundamental active power components for all three phases of load currents are given as,

$$w_{ap}(n) = [I - \mu_a(n)R_a(n)]w_{ap}(n-1) + \mu_a(n)p_a(n) \tag{8.44}$$

$$w_{bp}(n) = [I - \mu_b(n)R_b(n)]w_{bp}(n-1) + \mu_b(n)p_b(n) \tag{8.45}$$

$$w_{cp}(n) = [I - \mu_c(n)R_c(n)]w_{cp}(n-1) + \mu_c(n)p_c(n) \tag{8.46}$$

The average weight (w_{pavg}) of fundamental active power weight components of three phase load currents is calculated by mathematical expression as,

$$w_{pavg} = \frac{w_{ap} + w_{bp} + w_{cp}}{3} \tag{8.47}$$

The SPV instantaneous feed forward compensation term (I_{pff}) for all three phases is computed from SPV power (P_{pv}) and magnitude of PCC voltage (V_t) as,

$$I_{pff} = {2P_{pv}}/{V_t} \tag{8.48}$$

In three phase system for all three phases this term is divided by 3 and effective SPV instantaneous feed forward compensation term (I_{pff1}) is computed.

The reference active power weight (w_p) is computed by adding average active power weight (w_{pavg}) with output of DC bus PI controller (w_{pdc}) and subtracting SPV instantaneous feed forward compensation term (I_{pff1}) as,

$$w_p = w_{pavg} + w_{pdc} - I_{pff1} \tag{8.49}$$

Fundamental active power component of reference supply currents are estimated from unit inphase templates (u_{pa}, u_{pb} and u_{pc}) and reference active power weight (w_p) as,

$$i_{pa}^{*} = w_p u_{pa},\ \ i_{pb}^{*} = w_p u_{pb} \text{ and } i_{pc}^{*} = w_p u_{pc} \tag{8.50}$$

These active power components (i_{pa}^{*}, i_{pb}^{*} and i_{pc}^{*}) of reference supply currents are used to generate total reference supply currents as follows.

8.4.3.2 Estimation of Fundamental Reactive Power Component of Reference Supply Currents

Unit quadrature templates (u_{qa}, u_{qb} and u_{qc}) are calculated from unit inphase templates (u_{pa}, u_{pb} and u_{pc}) same as given in section 8.4.2. The magnitude of PCC voltages are calculated as given

in Eqn. (8.23) and compared to reference PCC voltage magnitude (V_t^*). Thus the generated error signal (v_{te}) is passed through a second PI controller whose output (w_t) is same as given in section 8.4.2.

The weighted values corresponding to fundamental reactive power component of load currents (w_{aq}, w_{bq} and w_{cq}) are extracted from recursive inverse based technique same as presented in section 6.3.2. The fundamental weights corresponding to reactive power components for all three phases of load currents are given as,

$$w_{aq}(n) = [I - \mu_a(n) R_a(n)] w_{aq}(n-1) + \mu_a(n) p_a(n) \tag{8.51}$$

$$w_{bq}(n) = [I - \mu_b(n) R_b(n)] w_{bq}(n-1) + \mu_b(n) p_b(n) \tag{8.52}$$

$$w_{cq}(n) = [I - \mu_c(n) R_c(n)] w_{cq}(n-1) + \mu_c(n) p_c(n) \tag{8.53}$$

The average reactive power weight (w_{qavg}) is calculated by mathematical expression given as,

$$w_{qavg} = \frac{w_{aq} + w_{bq} + w_{cq}}{3} \tag{8.54}$$

The magnitude of reference supply reactive power components (w_q) is evaluated by using average reactive power weighted value (w_{qavg}) and output of AC bus PI controller (w_t) as,

$$w_q = w_t - w_{qavg} \tag{8.55}$$

The fundamental reactive power components of reference supply currents are estimated from unit quadrature templates (u_{qa}, u_{qb} and u_{qc}) and reference reactive power weight (w_q) as,

$$i_{qa}^* = w_q u_{qa},\ i_{qb}^* = w_q u_{qb} \text{ and } i_{qc}^* = w_q u_{qc} \tag{8.56}$$

These reactive power components (i_{qa}^*, i_{qb}^* and i_{qc}^*) of reference supply currents are used to generate total reference supply currents as follows.

8.4.3.3 Generation of Reference Supply Currents and Switching Pulses

The summation of active (i_{pa}^*, i_{pb}^* and i_{pc}^*) and reactive (i_{qa}^*, i_{qb}^* and i_{qc}^*) components of reference supply currents using Eqn. (8.50) and Eqn. (8.56) gives the total reference supply currents (i_{sa}^*, i_{sb}^* and i_{sc}^*) as,

$$i_{sa}^* = i_{pa}^* + i_{qa}^*, i_{sb}^* = i_{pb}^* + i_{qb}^* \text{ and } i_{sc}^* = i_{pc}^* + i_{qc}^* \quad (8.57)$$

The sensed supply currents (i_{sa}, i_{sb} and i_{sc}) are compared with the reference supply currents (i_{sa}^*, i_{sb}^* and i_{sc}^*) given in Eqn. (8.57) and the current errors (i_{sae}, i_{sbe} and i_{sce}) are generated. These current errors are given to PWM current controller, which generates switching pulses for three phase VSC used as SPV system.

8.5 MATLAB BASED MODELING OF CONTROL ALGORITHMS FOR SPV SYSTEM

The modeling of control algorithms for grid connected SPV system using MATLAB is presented here. The control algorithms developed for this system are based on SRFT, Wiener filter and recursive inverse. These algorithms are developed in MATLAB using SIMULINK and Sim Power System (SPS) tool boxes.

8.5.1 MATLAB Model of Synchronous Reference Frame Based Control Algorithm

Fig. 8.8 shows the simulation model of SRFT based control algorithm developed in MATLAB using SIMULINK and SPS tool box. This control algorithm is used for the generation of reference supply currents (i_{sa}^*, i_{sb}^* and i_{sc}^*) from distorted load currents. The inputs to the SRFT based control algorithms are PCC voltages (v_s), supply currents (i_{sa}, i_{sb} and i_{sc}), load currents (i_{la}, i_{lb} and i_{lc}) and self-sustained DC bus voltage (V_{dc}). The fundamental active and reactive current

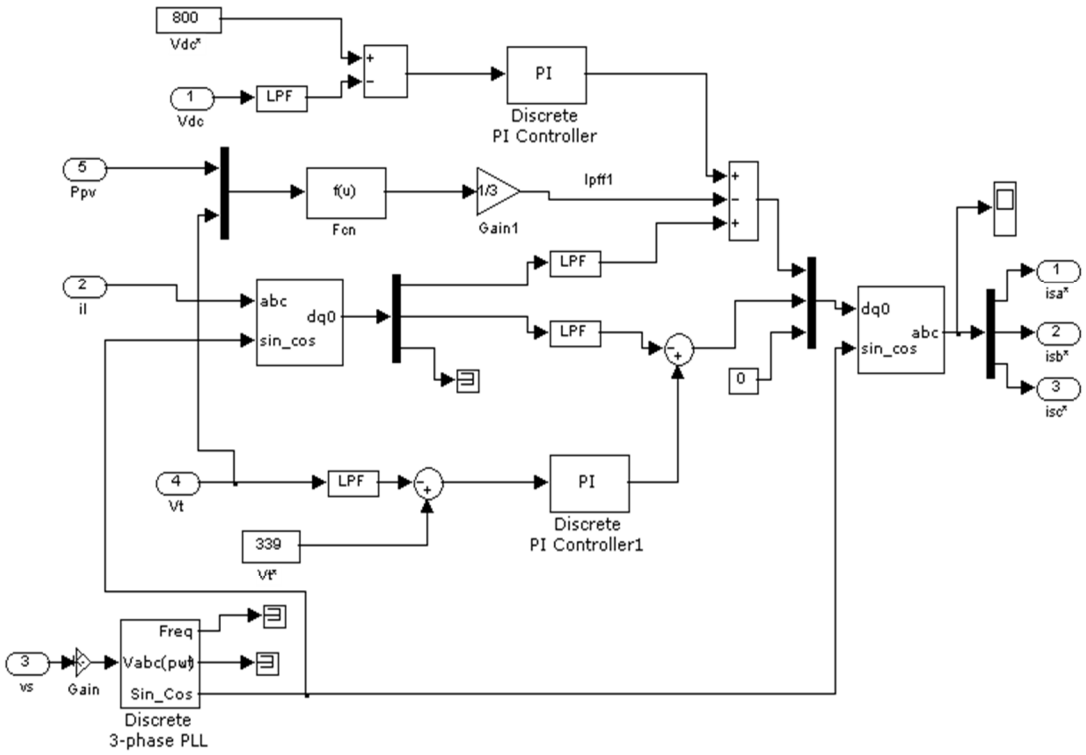


Fig. 8.8 Simulink model of SRFT based control algorithm

components of load currents are extracted using abc-dq0 transformation. These components are used with DC and AC bus PI controllers outputs for the estimation of reference supply current components. Then, the reference active and reactive current components are converted using dq0-abc transformation to estimate three phase reference supply currents.

8.5.2 MATLAB Model of Wiener Filter Based Control Algorithm

The simulation model of Wiener filter based control algorithm is used to estimate the reference supply currents. The PCC voltages (v_{sa}, v_{sb} and v_{sc}), supply currents (i_{sa}, i_{sb} and i_{sc}), load currents (i_{la}, i_{lb} and i_{lc}) and DC bus voltage (V_{dc}) are sensed by the Wiener filter based control algorithm for the estimation of reference supply currents. Simulation model for the estimation of weights corresponding to active and reactive power component using Wiener filter is given in section 5.4.1.

8.5.3 MATLAB Model of Recursive Inverse Based Control Algorithm

The MATLAB based model of the recursive inverse based control algorithm is developed using SPS tool box. Simulation model of the control algorithm is used for the generation of reference supply currents. The inputs to the control algorithm as shown in SIMULINK model are PCC voltages (v_s), supply currents (i_{sa}, i_{sb} and i_{sc}), load currents (i_{la}, i_{lb} and i_{lc}) and self-sustained DC bus voltage (V_{dc}) used for the control of DSTATCOM. The MATLAB based model and extraction of fundamental active and reactive power components of load currents from the recursive inverse based control algorithm are discussed in detail in section 6.4.2.

8.6 RESULTS AND DISCUSSION

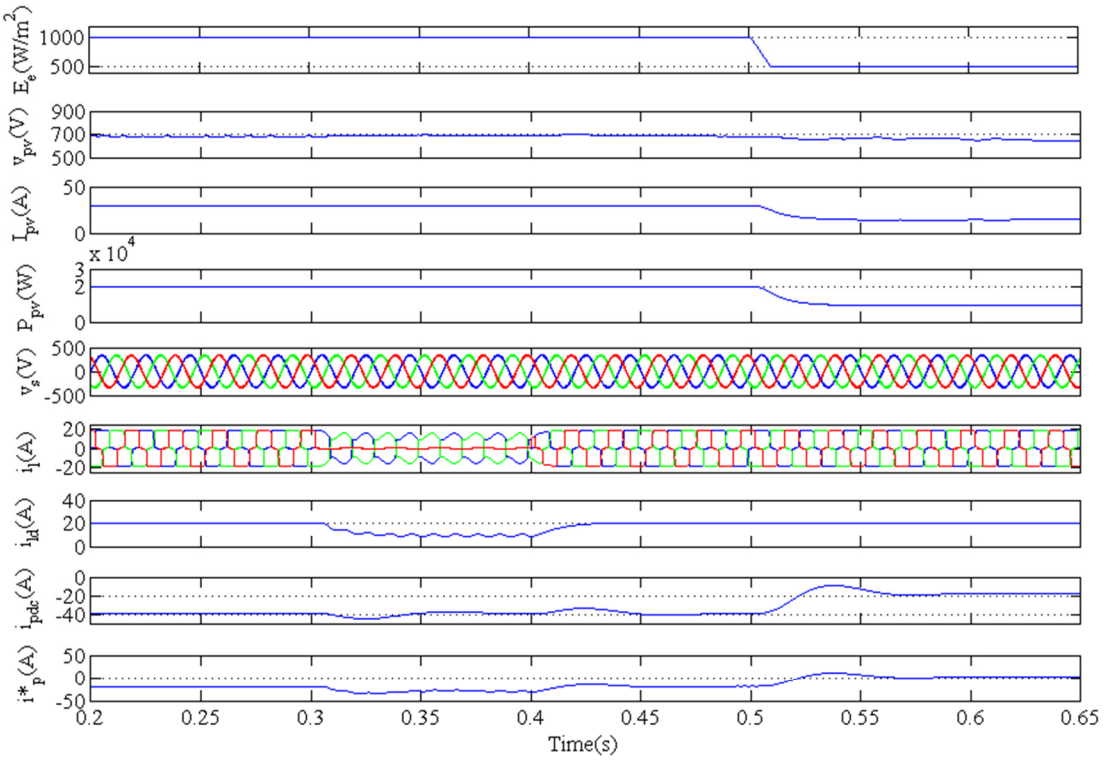
Performance of the grid connected SPV system using SRFT, Wiener filter and recursive inverse based control algorithms are presented here. The results using SPV system are presented for the transfer of real power demand along with load compensation achieved using DSTATCOM. Power quality improvement using DSTATCOM is observed for several power quality problems such as harmonics elimination, reactive power compensation and load balancing under linear and nonlinear loads. These results are taken in MATLAB environment using SIMULINK and SPS tool boxes. The detailed discussion of results of SPV system using these control algorithms is presented as follows.

8.6.1 Performance of SPV System With SRFT Based Control Algorithm

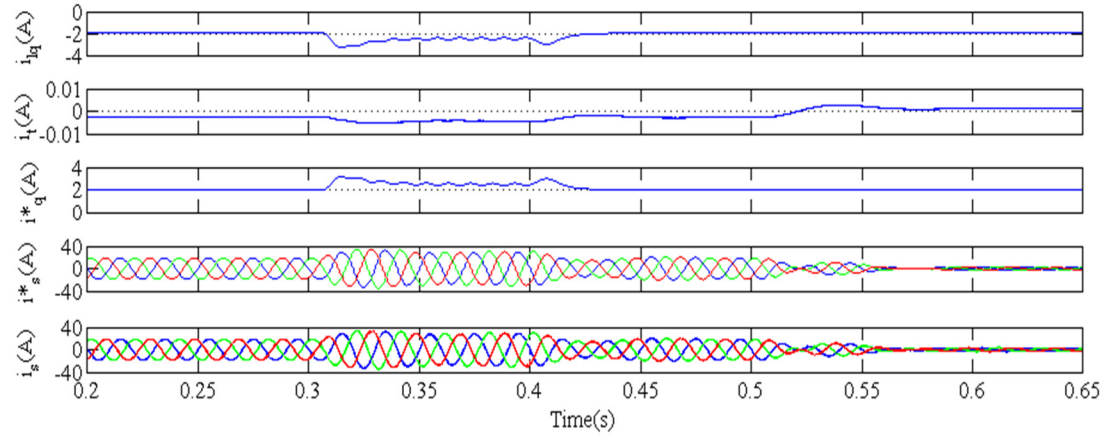
Simulated performance of SPV system with SRFT based control algorithm is presented here. These results are presented for PFC and voltage regulation modes under linear and nonlinear loads.

8.6.1.1 Performance of SRFT Based Control Algorithm

Figs. 8.9(a) and (b) show the performance with SRFT based control algorithm in voltage regulation mode under nonlinear load. Fig. 8.9(a) shows waveforms of solar irradiance level (E_e), SPV array voltage (V_{pv}), SPV array current (I_{pv}), SPV array output power (P_{pv}), PCC voltages (v_s), load currents (i_l), fundamental active DC component (i_{ld}) of load current, output of DC bus



(a)



(b)

Fig. 8.9 Performance and intermediate signals of SRFT based control algorithm for SPV system

PI controller (i_{pdc}) and active reference current component of supply current (i_p). These waveforms are shown for steady state (before t=0.3s), unbalanced load (t=0.3s to t=0.4s) and reduced solar irradiance (after t=0.5s) conditions. Fig. 8.9(b) shows waveforms of fundamental reactive DC component (i_{lq}) of load current, output of AC bus PI controller (i_t), reactive reference current component of supply current (i_q), reference supply currents (i_s^*) and actual supply currents (i_s). These results show satisfactory performance of SPV system in evacuating real power as well as maintaining quality of power at distribution level.

8.6.1.2 Performance of SPV System in PFC Mode Under Linear and Nonlinear Loads

Performance of SPV system in PFC mode under linear and nonlinear load is presented here. This is divided into four parts. The first and second parts deal with the performance and power generation of SPV system under linear load. The third and fourth parts present the performance and power generation of SPV system under nonlinear load.

A. Performance of the SPV System in PFC Mode Under Linear Load

Fig. 8.10 shows the dynamic performance of the system in PFC mode under a 20kVA and 0.8 linear lagging pf load. The waveforms of SPV voltage (V_{pv}), SPV current (I_{pv}), SPV output power (P_{pv}), PCC voltages (v_s), supply currents (i_{sa}, i_{sb} and i_{sc}), load currents (i_{la}, i_{lb} and i_{lc}), VSC currents (i_{Ca}, i_{Cb} and i_{Cc}) and DC bus voltage (V_{dc}) are shown in this figure. The supply currents are observed to be balanced and sinusoidal in steady state (before t=0.3s) condition. An unbalancing in the load is created, when phase 'c' is removed. During unbalancing (t=0.3s to t=0.4s), supply currents are also balanced and sinusoidal. The active power demand along with load balancing during unbalanced load is fulfilled by SPV system. The surplus power generated by the SPV system is fed to the utility grid. The supply voltages and currents are observed to be in phase with each other. The solar irradiance is decreased at t=0.5s to value of 500W/m^2, which

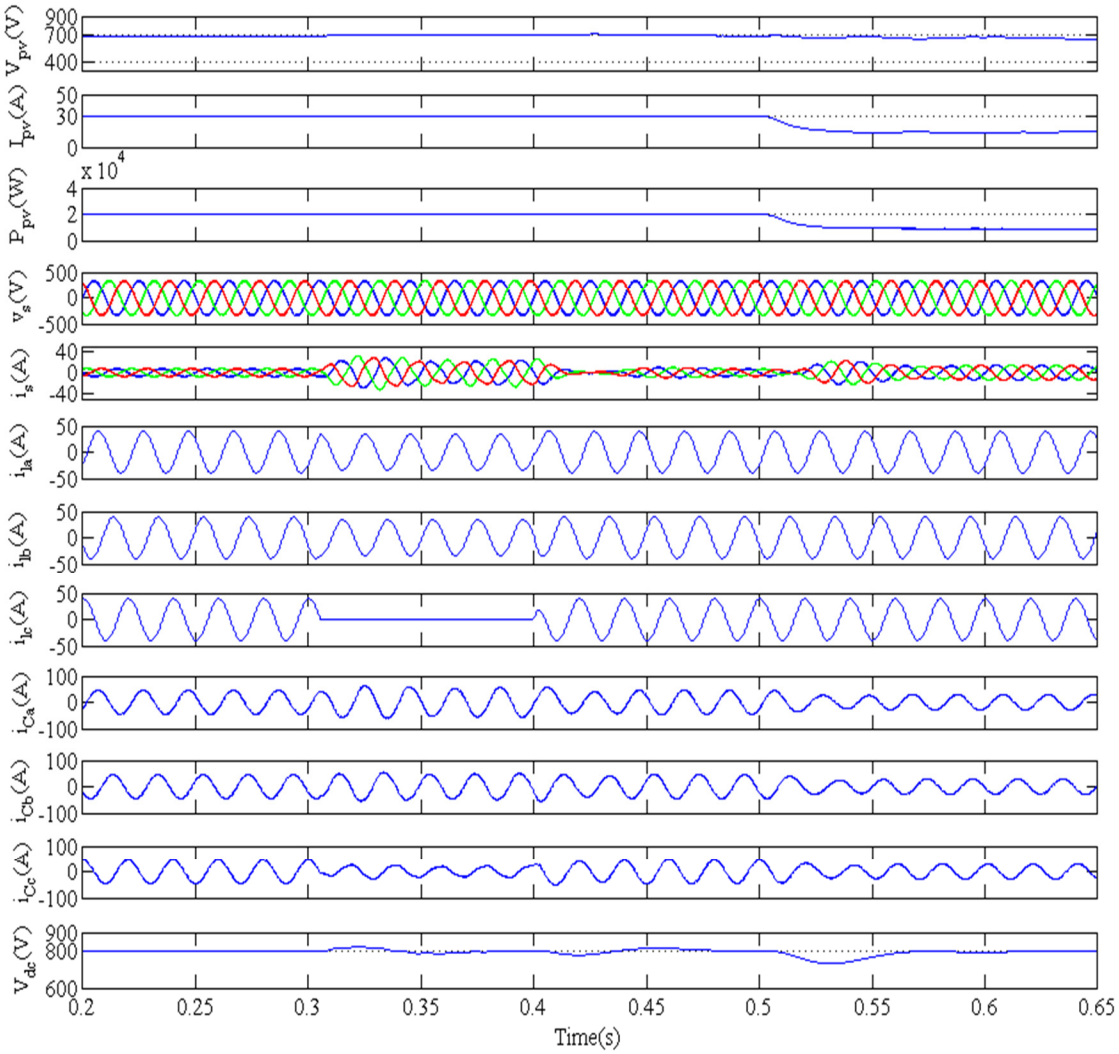


Fig. 8.10 Performance of SPV system in PFC mode under linear load

causes power generation from SPV system to decrease. The load active power demand is now partially supplied by the AC mains. The DC bus voltage of VSC is maintained to its reference value 800V under varying load conditions.

A. Performance of SPV System Under Linear Load

Fig. 8.11 shows the generation and evacuation of active and reactive powers by SPV system. The waveforms of SPV voltage (V_{pv}), SPV current (I_{pv}), SPV output power (P_{pv}), load real power (P_l), supply real power (P_s), and SPV real power (P_C), load reactive power (Q_l), supply reactive power (Q_s) and SPV reactive power (Q_C) are shown in these results. Under steady state condition

(before t=0.3s) the output voltage of SPV system is 680V and current is around 30.5A, which gives output power around 20kW. The load active power demand is approximately 16kW, which is fed by SPV system and the excess power is transferred to the AC mains as observed in Fig. 8.11. Moreover, the load reactive power demand is around 12kVAR which is fed completely by VSC and there is almost negligible reactive power burden on the AC mains.

An unbalancing is created in the load by removing phase 'c'. During load unbalancing (t=0.3s to t=0.4s), the output power of SPV system is unaffected. The active power demand of load is fulfilled by SPV system and there is negligible reactive power burden on the supply side. The

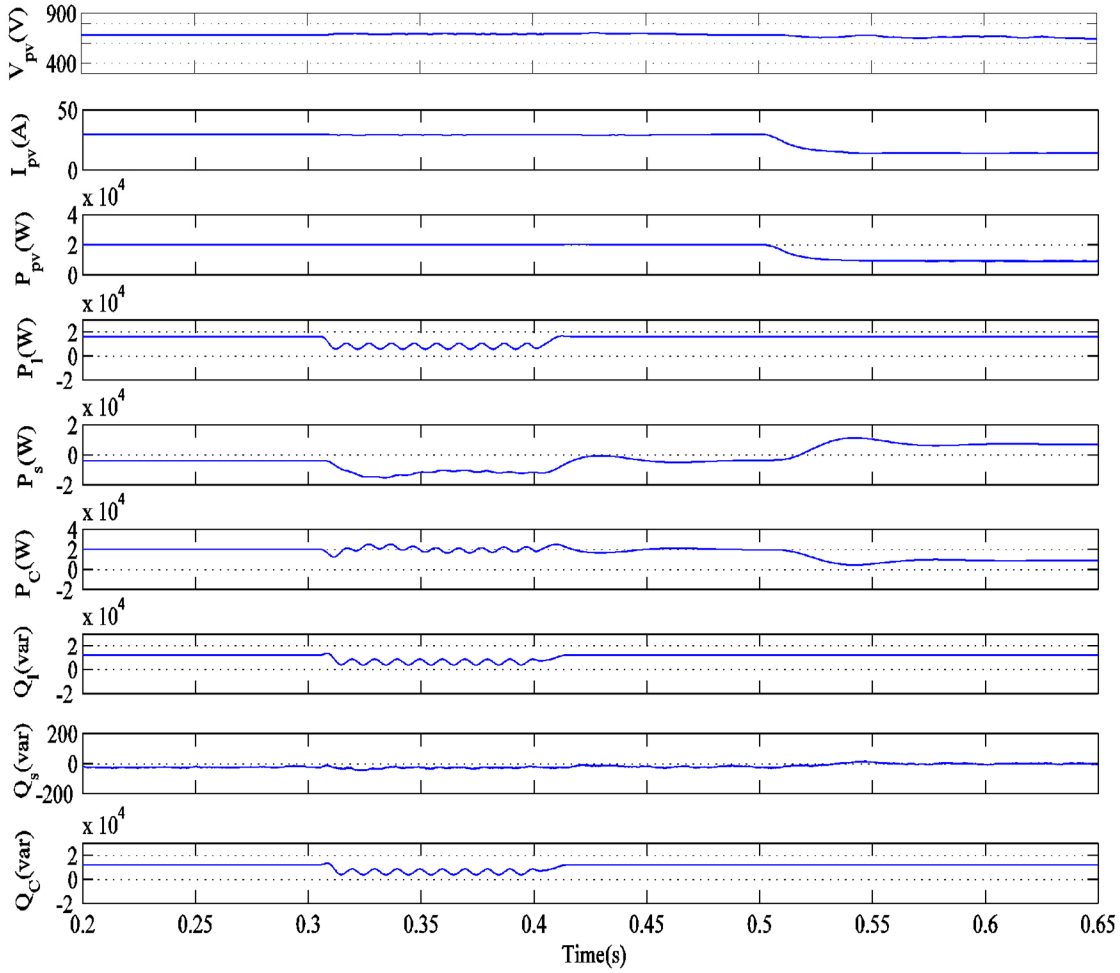


Fig. 8.11 Performance and powers of SPV array under linear load

SPV system power is reduced (after t=0.5) due to change in irradiance level from 1000W/m^2 to 500W/m^2. During this time, the active power demand around 10kW, of the load is fed by AC mains, whereas reactive power demand of the load (12kVAR) is completely fed by SPV system. The action of PI controller regulates the DC link voltage to a reference level of 800V.

C. Performance of the SPV System in PFC Mode Under Nonlinear Load

Fig. 8.12 shows performance of the SPV with SRFT based control algorithm in PFC mode under nonlinear load. The waveforms of SPV voltage (V_{pv}), SPV current (I_{pv}), SPV output power (P_{pv}),

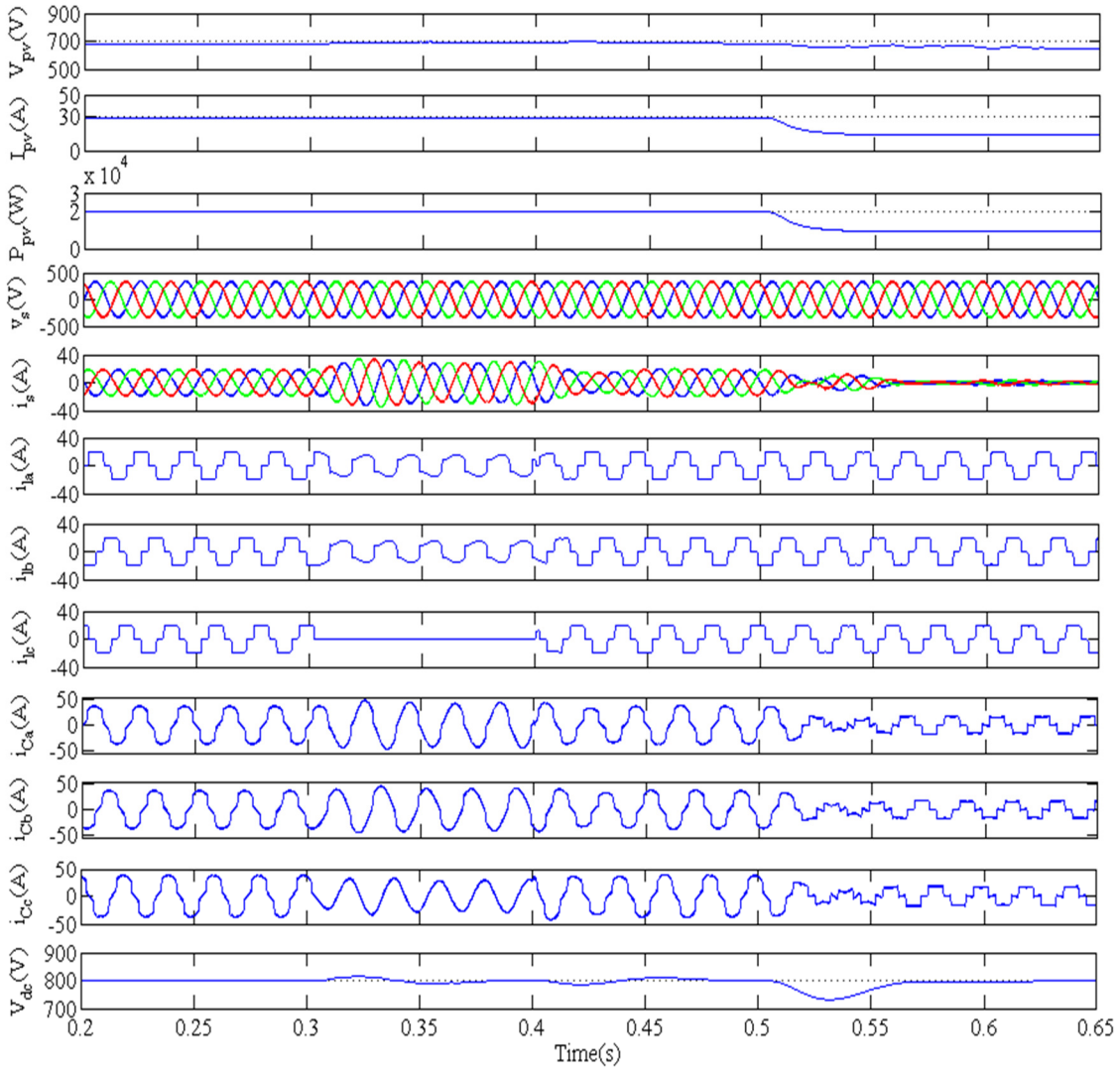
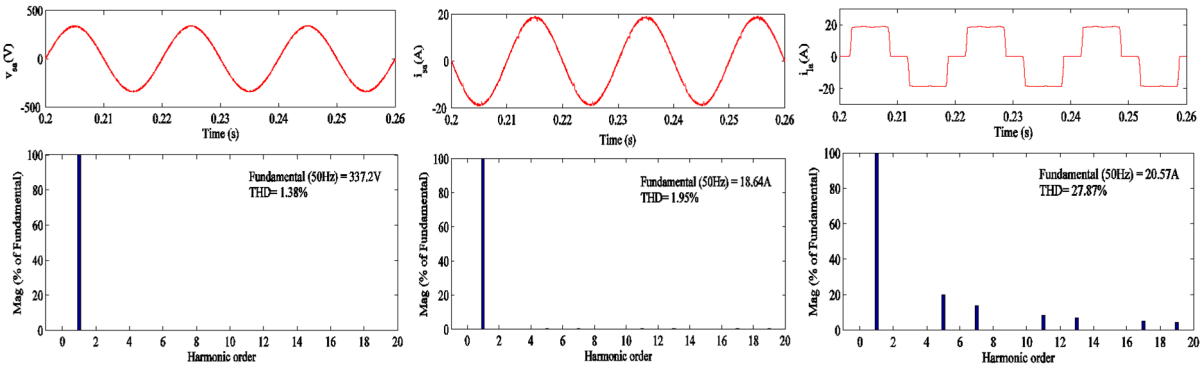


Fig. 8.12 Performance of SPV array in PFC mode under nonlinear load

PCC voltages (v_s), supply currents (i_s), load currents (i_{la}, i_{lb} and i_{lc}), VSC currents (i_{Ca}, i_{Cb} and i_{Cc}) and DC bus voltage (V_{dc}) are shown in these results. The supply currents are observed to be balanced and sinusoidal in steady state condition (before t=0.3s). An unbalancing in the load is created by removing phase 'c'. During the load unbalancing (t=0.3s to t=0.4s), supply currents are observed to be balanced and sinusoidal by VSC. The active power demand of the load during balanced load as well as unbalanced load condition is met by VSC of SPV system. The excess power generated by the system is fed to the AC mains. The solar irradiance is decreased at t=0.5s from 1000W/m^2 to 500W/m^2, which causes power generation from SPV system to decrease. The load active power demand is now partially supplied by the AC mains. The DC bus voltage of VSC is maintained to its reference value 800V.

Fig. 8.13 shows the harmonic spectra of phase 'a' of PCC voltage (v_{sa}), supply current (i_{sa}) and load current (i_{la}). These results show the THDs of 1.38%, 1.95% and 27.87% in PCC voltage, supply current and load current respectively. A THD of 1.95% is achieved in supply current, whereas there is 27.87% THD in load current. These results show the satisfactory performance of the SPV system for harmonics elimination and load balancing in PFC mode.

D. Performance of SPV System Under Nonlinear Load



(a) (b) (c)

Fig. 8.13 Harmonic spectra of phase 'a' of (a) PCC voltage, v_{sa} (b) supply current, i_{sa} (c) load current, i_{la} in PFC mode

Fig. 8.14 shows the performance of SPV system under nonlinear load. These results present the waveforms of SPV output voltage (V_{pv}), SPV current (I_{pv}), SPV power (P_{pv}), load real power (P_l), supply real power (P_s), and SPV real power (P_C), load reactive power (Q_l), supply reactive power (Q_s) and SPV reactive power (Q_C). The output voltage (V_{pv}), current (I_{pv}) and power (P_{pv}) of SPV system are 680V, 30.5A and 20kW respectively. In steady state condition (before t=0.3s), the active power demand of nonlinear load (P_l) is around 10kW, which is fed by SPV system (P_C) and excess power of 10kW is transferred to the AC mains (P_s). The reactive power demand of load (Q_l) is completely fed by the SPV (Q_C) system and there is almost negligible

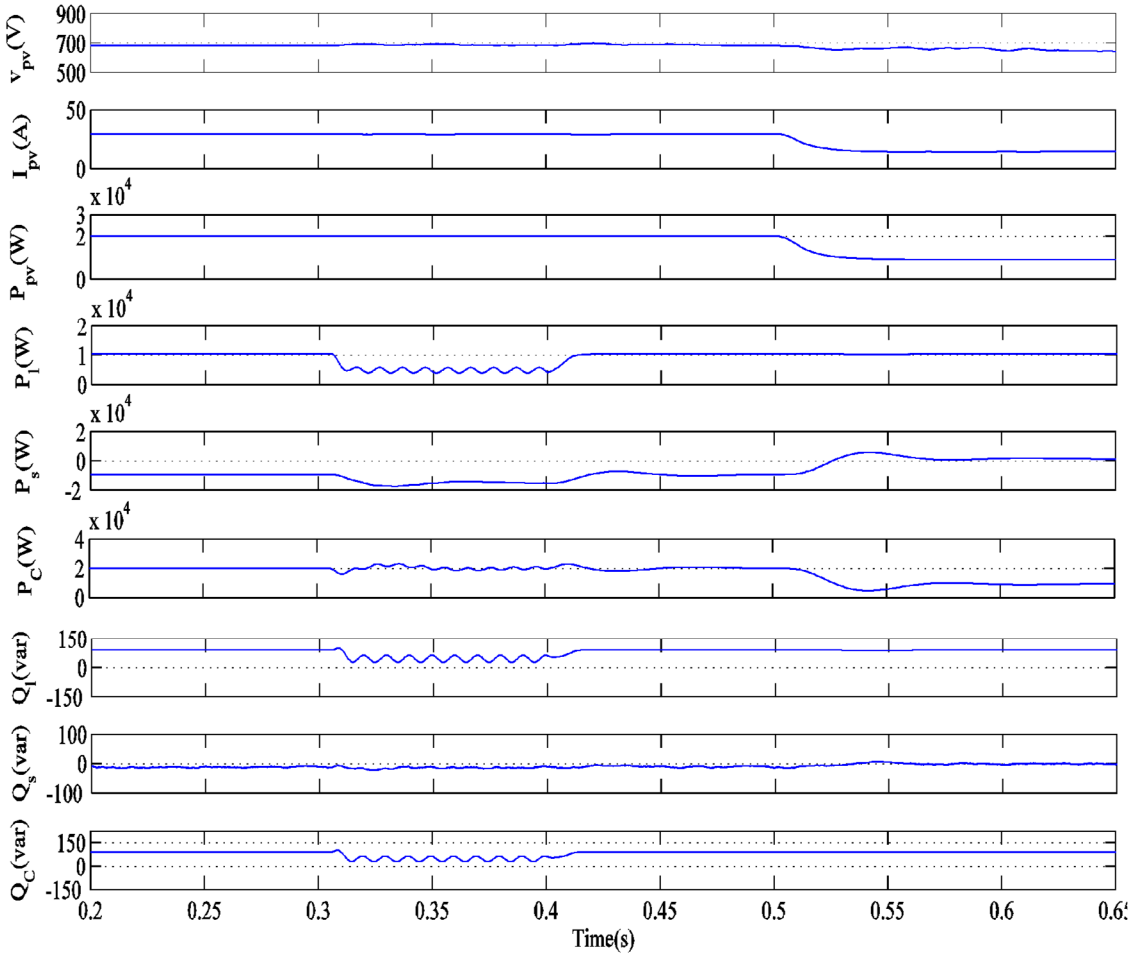


Fig. 8.14 Performance and power of SPV system under nonlinear load

reactive power burden on the supply side.

8.6.1.3 Performance of SPV System in Voltage Regulation Mode Under Linear and Nonlinear Loads

Performance of SPV system in the voltage regulation mode with SRFT based control algorithm is presented here. This is divided into two parts. The first part deals with the performance of system under linear load and the second part presents the performance of the system under nonlinear load.

A. Performance of SPV System in Voltage Regulation Mode Under Linear Load

Fig. 8.15 shows the performance of SPV system in regulating voltage at PCC under linear load. The waveforms of SPV voltage (V_{pv}), SPV current (I_{pv}), SPV output power (P_{pv}), PCC voltages (v_s), supply currents (i_s), load currents (i_{la}, i_{lb} and i_{lc}), VSC currents (i_{Ca}, i_{Cb} and i_{Cc}), DC bus voltage (V_{dc}) and PCC voltage amplitude (V_t) are shown in these results. During steady state (before t=0.3s) condition, the supply currents are observed to be balanced and sinusoidal. The voltage at the DC bus is regulated at its reference value of 800V. The PCC voltage is regulated to the reference value of 339V by injecting leading current component from SPV system. Supply currents are observed to be balanced even during unbalanced (t=0.3 to t=0.4s) load condition and excess power is transferred to the AC mains. The DC and AC bus voltages are regulated to their reference values. The power of SPV system reduced (after t=0.5s) due to change in solar irradiance to 500W/m^2. During this time, the active power demand of the load is partially fed by the AC mains.

B. Performance of SPV System in Voltage Regulation Mode Under Nonlinear Load

Fig. 8.16 shows the performance of SPV system in voltage regulation mode under nonlinear load. These results show the waveforms of SPV voltage (V_{pv}), SPV current (I_{pv}), SPV output

power (P_{pv}), PCC voltages (v_s), supply currents (i_s), load currents (i_{la}, i_{lb} and i_{lc}), VSC currents (i_{Ca}, i_{Cb} and i_{Cc}), DC bus voltage (V_{dc}) and PCC voltage amplitude (V_t). The supply currents are observed to be balanced and sinusoidal in steady state (before t=0.3s) condition. An unbalancing in the load is created by removing the load on phase 'c'. During load unbalancing (t=0.3s to t=0.4s), supply currents remain balanced and sinusoidal with the action of VSC of SPV system. The active power demand is met by the SPV system and this system connected at the DC link of

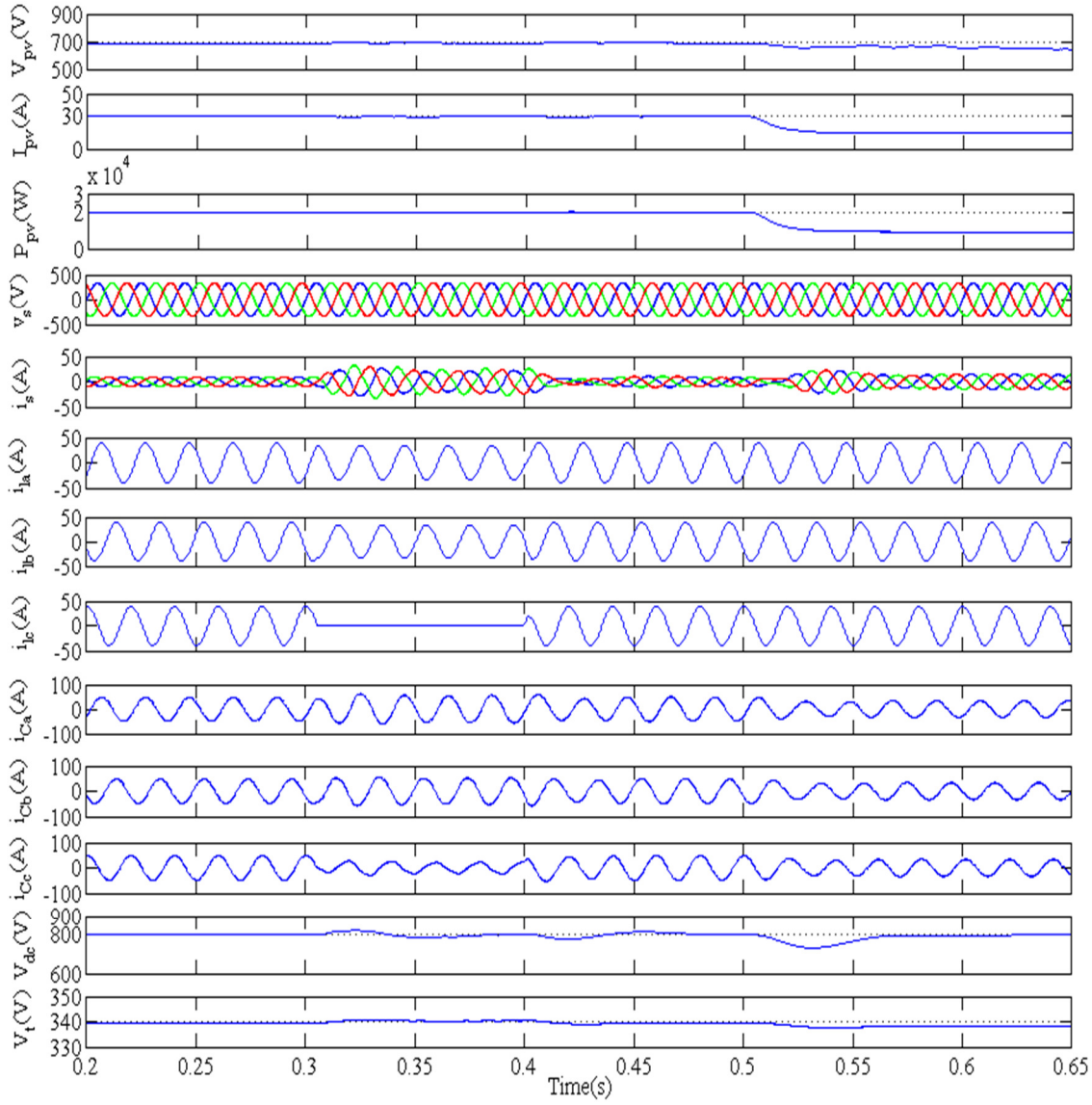


Fig. 8.15 Performance of SPV system in voltage regulation mode under linear load

the VSC and provides the load compensation. The excess power generated by the SPV system is fed into the AC mains. Solar irradiance is decreased from 1000W/m^2 to 500W/m^2 at t=0.5s, which causes power generation from SPV system to decrease to 10kW. The load active power demand is now partially supplied by the AC mains. The DC bus and AC bus voltages are maintained at their reference values of 800V and 339V respectively under varying load conditions.

Fig. 8.17 shows the harmonic spectra of phase 'a' of PCC voltage (v_{sa}), supply current (i_s) and

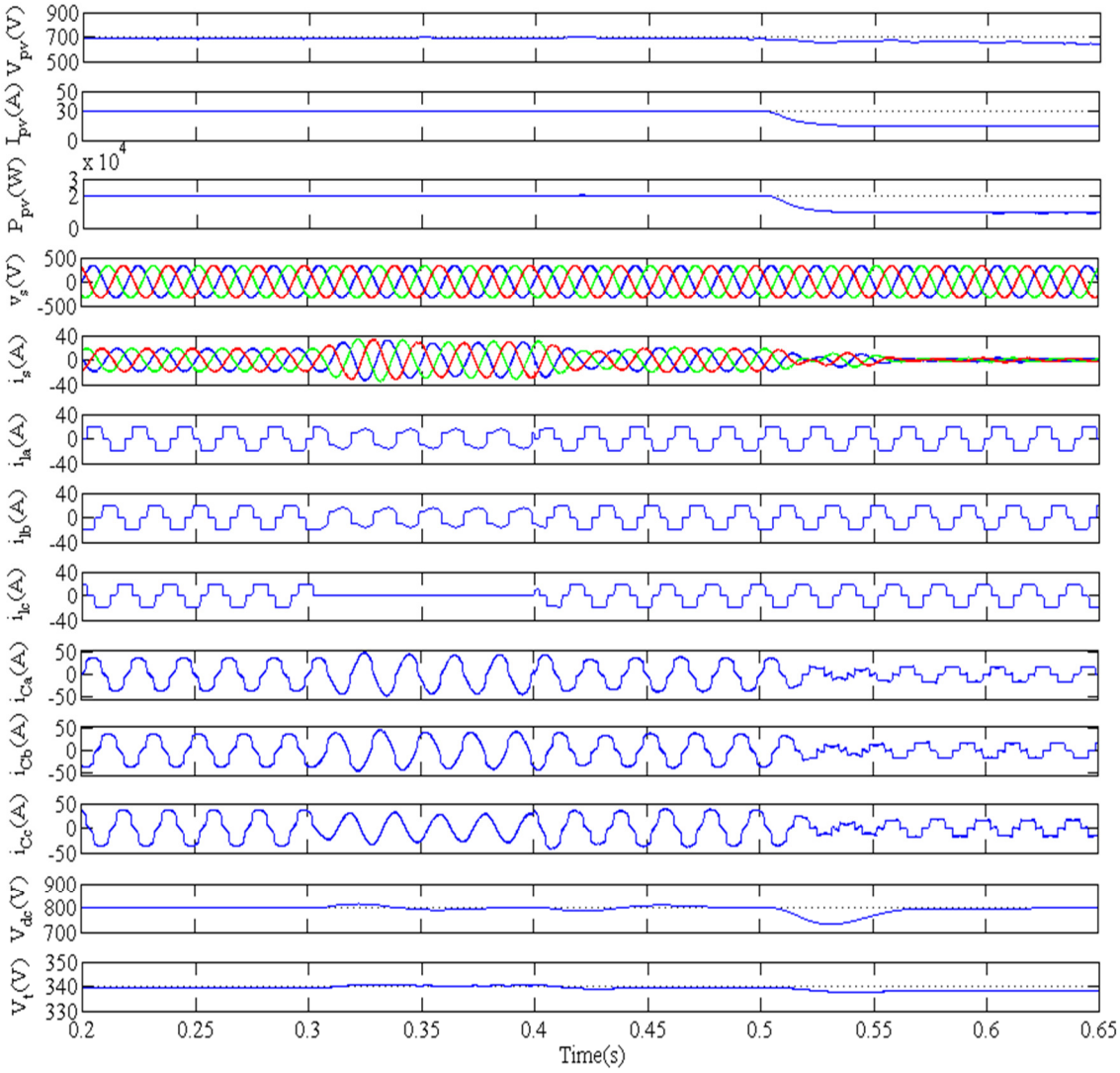
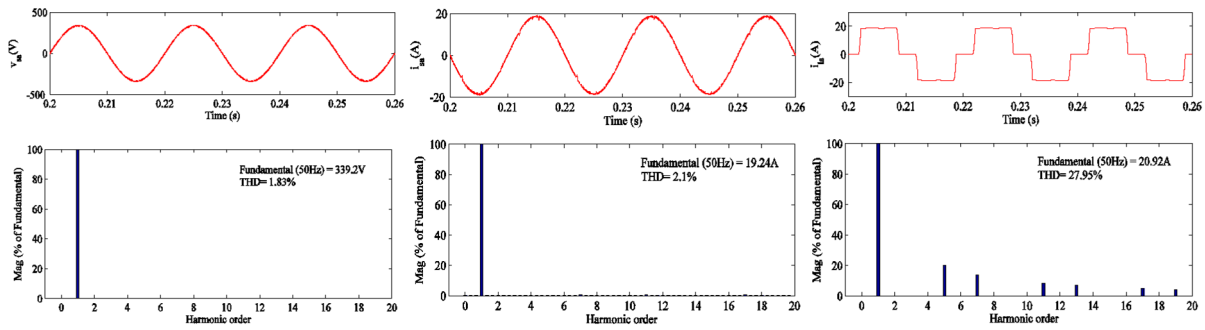


Fig. 8.16 Performance of SPV system in voltage regulation mode under nonlinear load



(a) (b) (c)

Fig. 8.17 Harmonic spectra of phase 'a' of (a) PCC voltage, v_{sa} (b) supply current, i_{sa} (c) load current, i_{la} in voltage regulation mode

load current (i_l). The harmonic spectra show THD of 1.83%, 2.1% and 27.95% in PCC voltage, supply current and load current. These results show improved THD in supply current having a value of 2.1% when there is THD of 27.95% in the load current. The THDs of PCC voltage and supply current are within the limit specified of an IEEE-519 standard.

8.6.2 Performance of SPV System With Wiener Filter Based Control Algorithm

The performance of SPV system using Wiener filter based control algorithm is presented here. The algorithm is simulated using MATLAB and Sim Power System and is tested for real power demand of the load fed from SPV system. The algorithm is also tested for power quality improvement features viz. harmonics elimination, reactive power compensation and load balancing in PFC and voltage regulation modes.

8.6.2.1 Performance of the Wiener Filter Based Control Algorithm

Fig. 8.18 shows the performance of SPV system with the Wiener filter based control algorithm in voltage regulation mode under nonlinear load. Fig. 8.18(a) shows the waveforms of solar irradiance (E_e), SPV voltage (V_{pv}), SPV current (I_{pv}), SPV output power (P_{pv}), phase 'a' of PCC voltage (v_{sa}), phase 'a' of load current (i_{la}), cross correlation vector (P_{dxa}) between the desired quantity and input quantity, correlation matrix (R_x) of the input data, weight corresponding to

active power component of phase 'a' of load current (w_{ap}), average and filtered active power weight (w_{pavg}), output of DC bus PI controller (w_{pdc}) and reference active power weight (w_p).

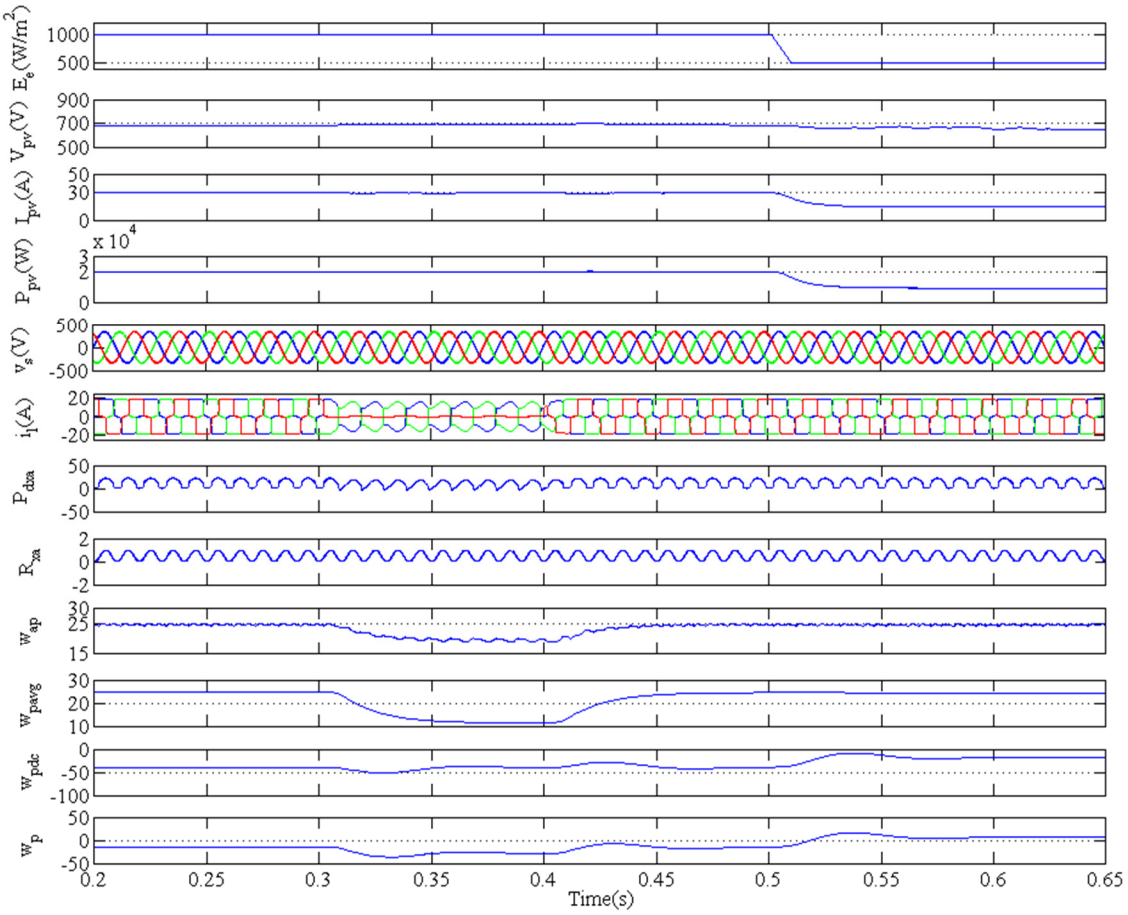
These results are shown for steady state condition (before t=0.3s) and unbalanced load condition (t=0.3s to t=0.4s) along with reduced irradiance condition (after t=0.5s) for SPV system. An unbalancing in the load is created, when phase 'c' of load is switched off at t=0.3s. Fig. 8.18(b) shows the waveforms of weight corresponding to reactive power component of phase 'a' of load current (w_{aq}), average and the filtered reactive power weight (w_{qavg}), output of AC bus PI controller (w_t), reference reactive power weight (w_q) which include w_{qavg} and w_t, reference supply currents (i_s^*) and supply currents (i_s). It is observed from these results that the supply currents follow the reference supply currents in steady state as well as dynamic load conditions. The Wiener filter based control algorithm performance is observed to be satisfactory under varied load conditions in steady state as well as in dynamic load conditions.

8.6.2.2 Performance of SPV System in PFC Mode Under Linear and Nonlinear Loads

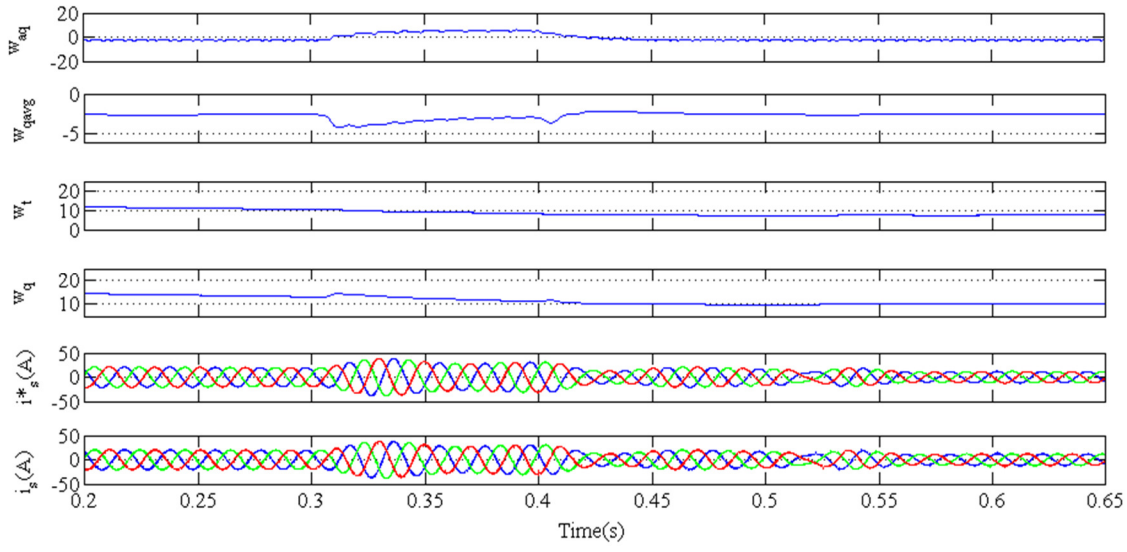
The performance of SPV system with Wiener filter based control algorithm in PFC mode is presented here. This is divided into four parts. The first two parts deal with the performance and power generation of SPV system under linear load. The third and fourth parts present performance of SPV system under nonlinear load.

A. Performance of the SPV System in PFC Mode Under Linear Load

Fig. 8.19 shows the performance of the SPV system in PFC mode under linear load of 20kVA, 0.8 lagging power factor using Wiener filter based control algorithm. The waveforms of SPV voltage (V_{pv}), SPV current (I_{pv}) and SPV output power (P_{pv}), PCC voltages (v_s), supply currents (i_s), load currents (i_{la}, i_{lb} and i_{lc}), VSC currents (i_{Ca}, i_{Cb} and i_{Cc}) and DC bus voltage (V_{dc}) are



(a)



(b)

Fig. 8.18 Performance of Wiener filter based control algorithm for grid connected SPV system

shown here. The supply currents are observed to be balanced and sinusoidal in steady state

(before t=0.3s) condition. An unbalancing is created during time period t=0.3s to t=0.4s in the load. During unbalanced load condition, supply currents remain balanced and sinusoidal due to the action of SPV system. The active power demand of the load is fulfilled by SPV system. The surplus power generated by the SPV system is fed to the AC mains. The supply voltages and currents are observed to be in phase with each other. The solar irradiance is decreased from 1000W/m^2 to 500W/m^2 at t=0.5s, which causes power generation from SPV system to decrease to 10kW. The load active power demand is now partially supplied by the AC mains. The DC bus

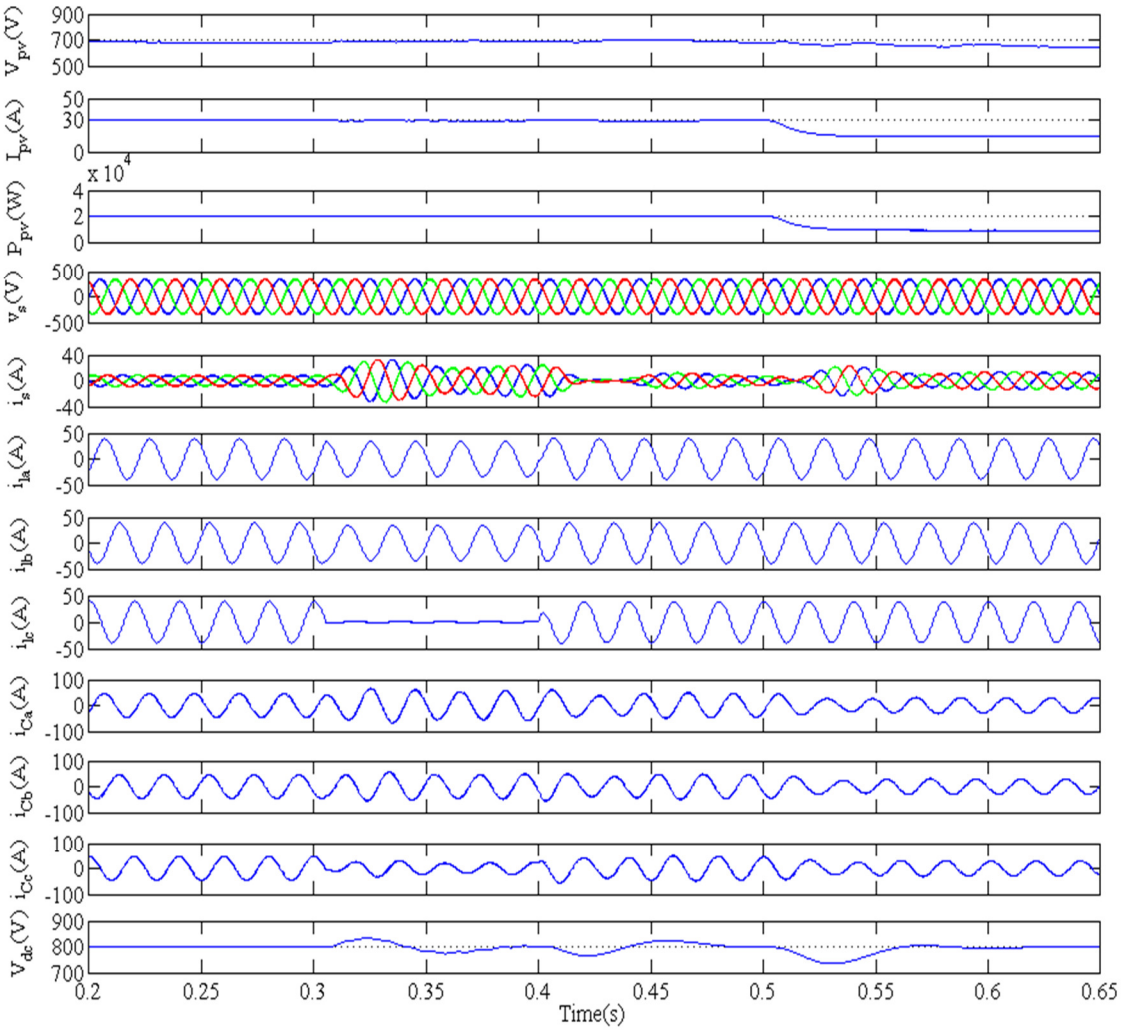


Fig. 8.19 Performance of SPV system in PFC mode under linear load

voltage of VSC is maintained to its reference value of 800V by the action of PI controller under varied load conditions.

B. Performance and Power of SPV System Under Linear Load

Fig. 8.20 shows the output current, voltage and power of SPV system. These results show the waveforms of SPV output voltage (V_{pv}), SPV current (I_{pv}), SPV power (P_{pv}), load real power (P_l), supply real power (P_s), and SPV real power (P_C), load reactive power (Q_l), supply reactive power (Q_s) and SPV reactive power (Q_C). Under steady state condition (before t=0.3s), the output voltage of SPV system is 680V, the current is around 30.5A, which gives output power around 20kW. The load active power demand is around 16kW, which is fed by SPV system and

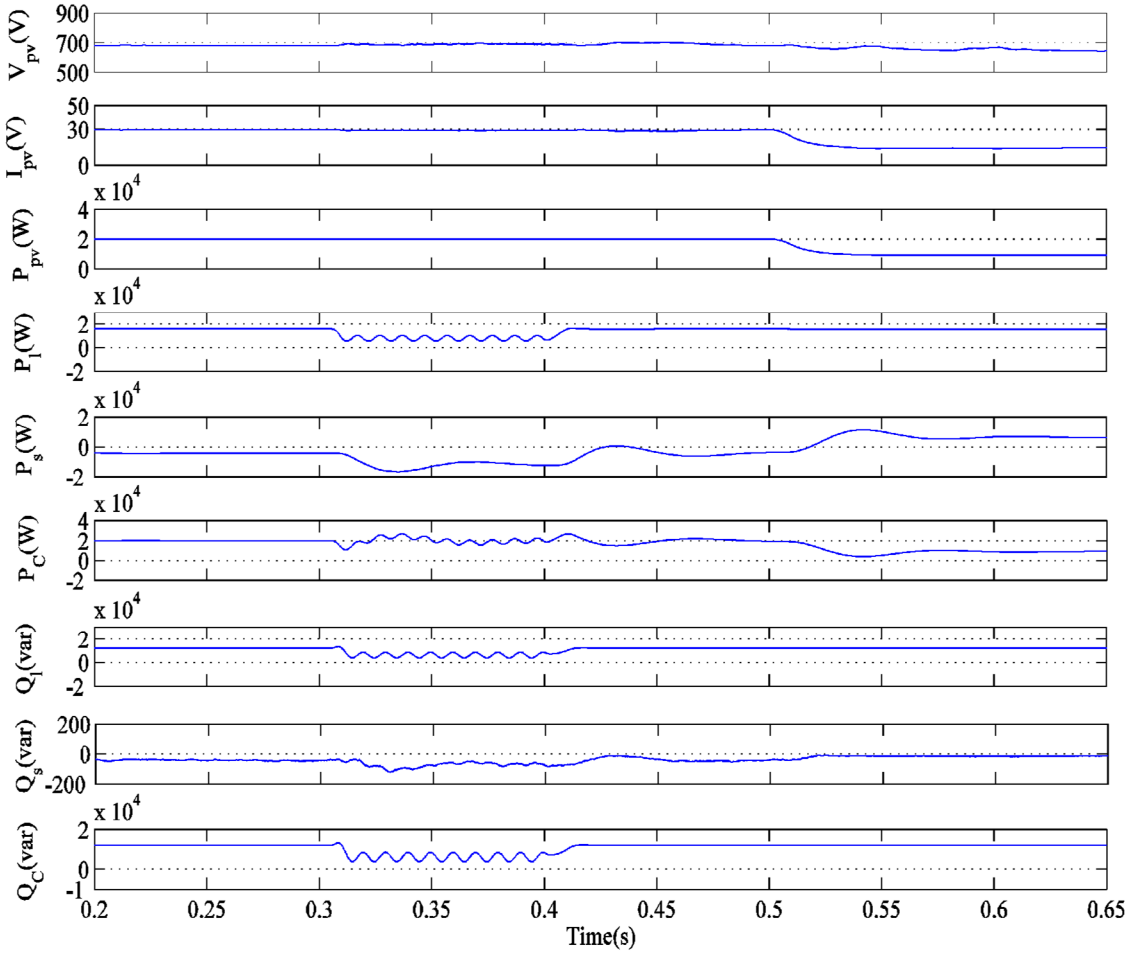


Fig. 8.20 Performance and power of SPV system under linear load

excess power is transferred to the AC mains. Additionally, the load reactive power demand is around 12kVAR, which is completely fed by SPV system and there is almost negligible reactive power required from the supply. During unbalanced (t=0.3s to t=0.4s) load condition, it is observed that the output power of SPV system is unaffected, active power demand of load is met by SPV system and there is negligible reactive power burden in the supply side. Solar irradiance level is decreased (after t=0.5s) almost half, which causes the SPV system power to reduce. During this unbalanced load operation, the active power demand of the load is partially fed by the AC mains, whereas reactive power demand of the load is completely fed by VSC of the SPV system.

C. Performance of SPV System in PFC Mode Under Nonlinear Load

Fig. 8.21 shows the performance of the SPV system with Wiener filter based control algorithm in PFC mode under nonlinear load. The waveforms of SPV voltage (V_{pv}), SPV current (I_{pv}), SPV output power (P_{pv}), PCC voltages (v_s), supply currents (i_s), load currents (i_{la}, i_{lb} and i_{lc}), VSC currents (i_{Ca}, i_{Cb} and i_{Cc}) and DC bus voltage (V_{dc}) are shown in these results. The supply currents are observed to be balanced and sinusoidal in steady state (before t=0.3s) condition. During an unbalanced load condition (t=0.3s to t=0.4s), it is observed that supply currents are again balanced and sinusoidal but of reduced magnitude. The active power demand along with load balancing is met by SPV system. The excess power generated by the system is fed to the AC mains. The solar irradiance is decreased to 500W/m^2 at t=0.5s, which causes power generation from SPV system to decrease to a value of 10kW. Since the SPV output power reduces, the load active power demand is now partially supplied by the AC mains. The DC bus voltage of VSC is maintained at its reference value 800V under steady state as well as dynamic load conditions due to action of PI controller.

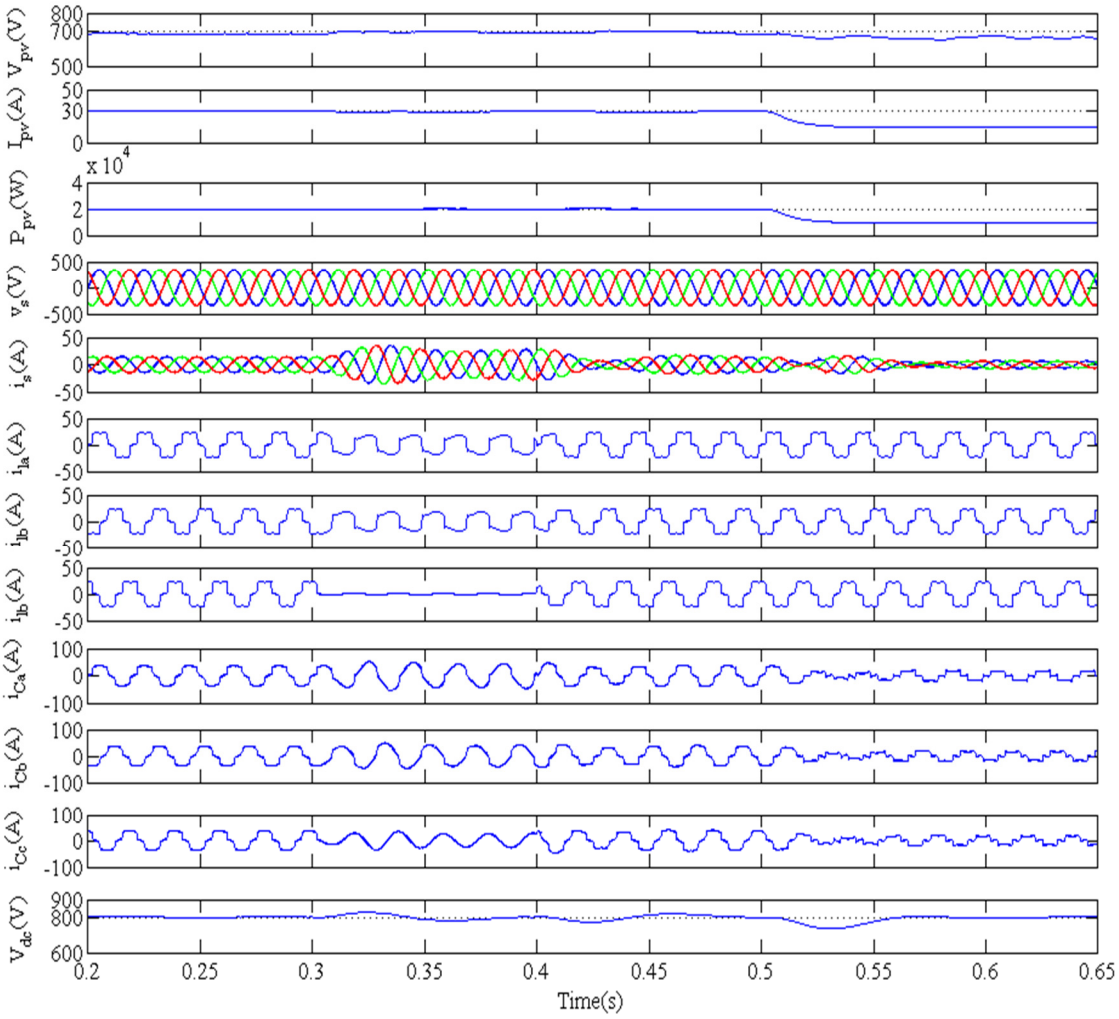
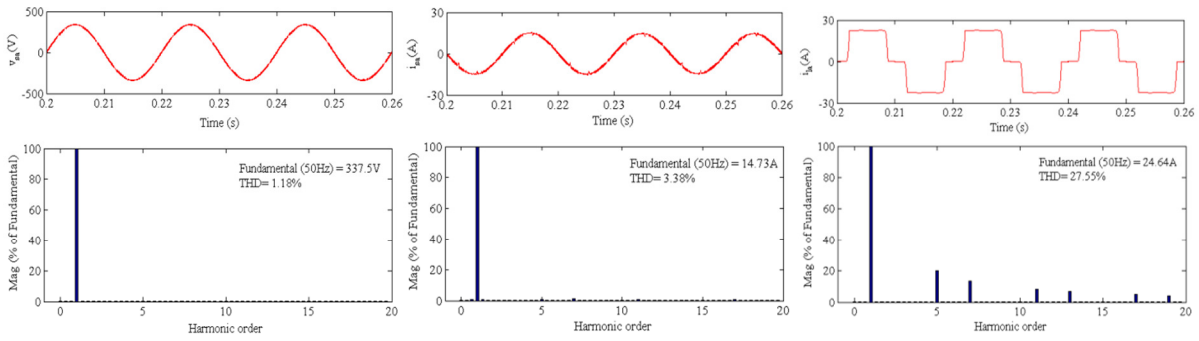


Fig. 8.21 Performance of SPV system in PFC mode under nonlinear load

Fig. 8.22 shows the harmonic spectra of phase 'a' of PCC voltage (v_{sa}), supply current (i_{sa}) and load current (i_{la}). These results show that the THD of 1.18%, 3.38% and 27.55% in PCC voltage, supply current and load current respectively. The THD in supply current is achieved as 3.38%, when there is a THD of 27.87% in load current. These results show the satisfactory performance of the SPV system in mitigating various power quality problems such as harmonics reduction and load balancing in PFC mode. The percentage of THD in PCC voltage and supply currents are within the limit specified by IEEE-519 standard.

D. Performance and Power of SPV System Under Nonlinear Load



(a) (b) (c)

Fig. 8.22 Harmonic spectra of phase 'a' of (a) PCC voltage, v_{sa} (b) supply current, i_{sa} (c) load current, i_{la} in PFC mode

Fig. 8.23 shows the performance of SPV system under a nonlinear load with Wiener filter based control algorithm. These results present the waveforms of SPV output voltage (V_{pv}), SPV current

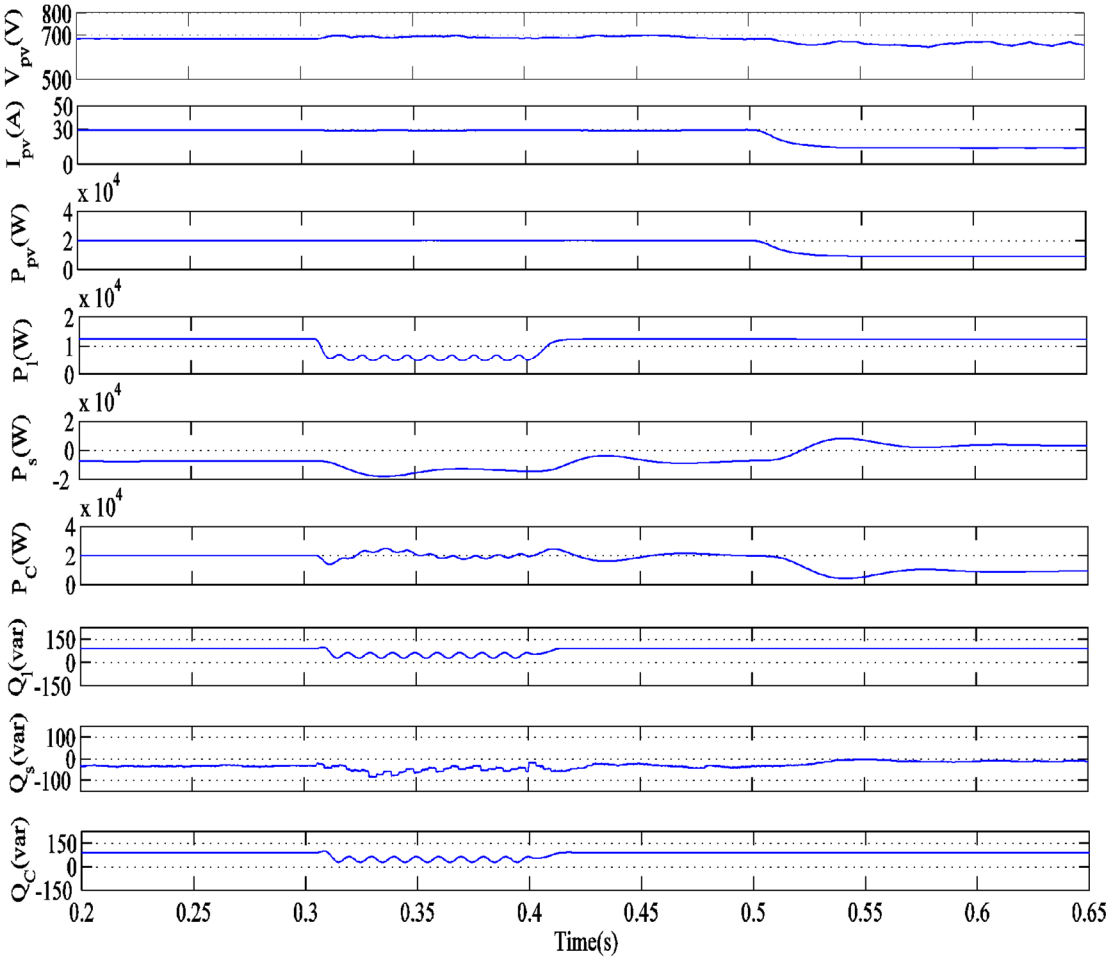


Fig. 8.23 Performance and power of SPV system under nonlinear load

(I_{pv}), SPV power (P_{pv}), load real power (P_l), supply real power (P_s), and SPV real power (P_C), load reactive power (Q_l), supply reactive power (Q_s) and SPV reactive power (Q_C). The output voltage (V_{pv}), current (I_{pv}) and power (P_{pv}) of SPV system 680V, 30.5A and 20kW respectively. Under steady state condition (before t=0.3s), the active power demand of the nonlinear load (P_l) is around 10kW, which is fed by SPV system (P_C) and the excess power is transferred to the AC mains (P_s). The reactive power demand (Q_l) of the load is completely provided by the SPV system (Q_C) and there is almost negligible reactive power burden on the supply side.

8.6.2.3 Performance of SPV System in Voltage Regulation Mode Under Linear and Nonlinear Loads

The performance of the SPV system in voltage regulation mode with Wiener filter based control algorithm is presented here. This is divided into two parts. The first part deals with the performance of the system under linear load and second part deals with the performance under nonlinear load. The detailed discussion of these results is given as follows.

A. Performance of SPV System in Voltage Regulation Mode Under Linear Load

Fig. 8.24 depicts the performance of the SPV system in regulating PCC voltage under linear load. The waveforms of SPV voltage (V_{pv}), SPV current (I_{pv}), SPV output power (P_{pv}), PCC voltages (v_s), supply currents (i_s), load currents (i_{la}, i_{lb} and i_{lc}), VSC currents (i_{Ca}, i_{Cb} and i_{Cc}), DC bus voltage (V_{dc}) and PCC voltage amplitude (V_t) are shown in these results. During steady state condition (before t=0.3s), supply currents are observed to be balanced and sinusoidal. The voltage at DC bus of VSC is regulated to its reference value of 800V. The PCC voltage is regulated to the reference value of 339V by injecting leading current component from VSC of SPV system. The supply currents are observed to be balanced during unbalanced (t=0.3 to t=0.4s) load condition and the excess power is transferred to the AC mains. The DC and AC bus

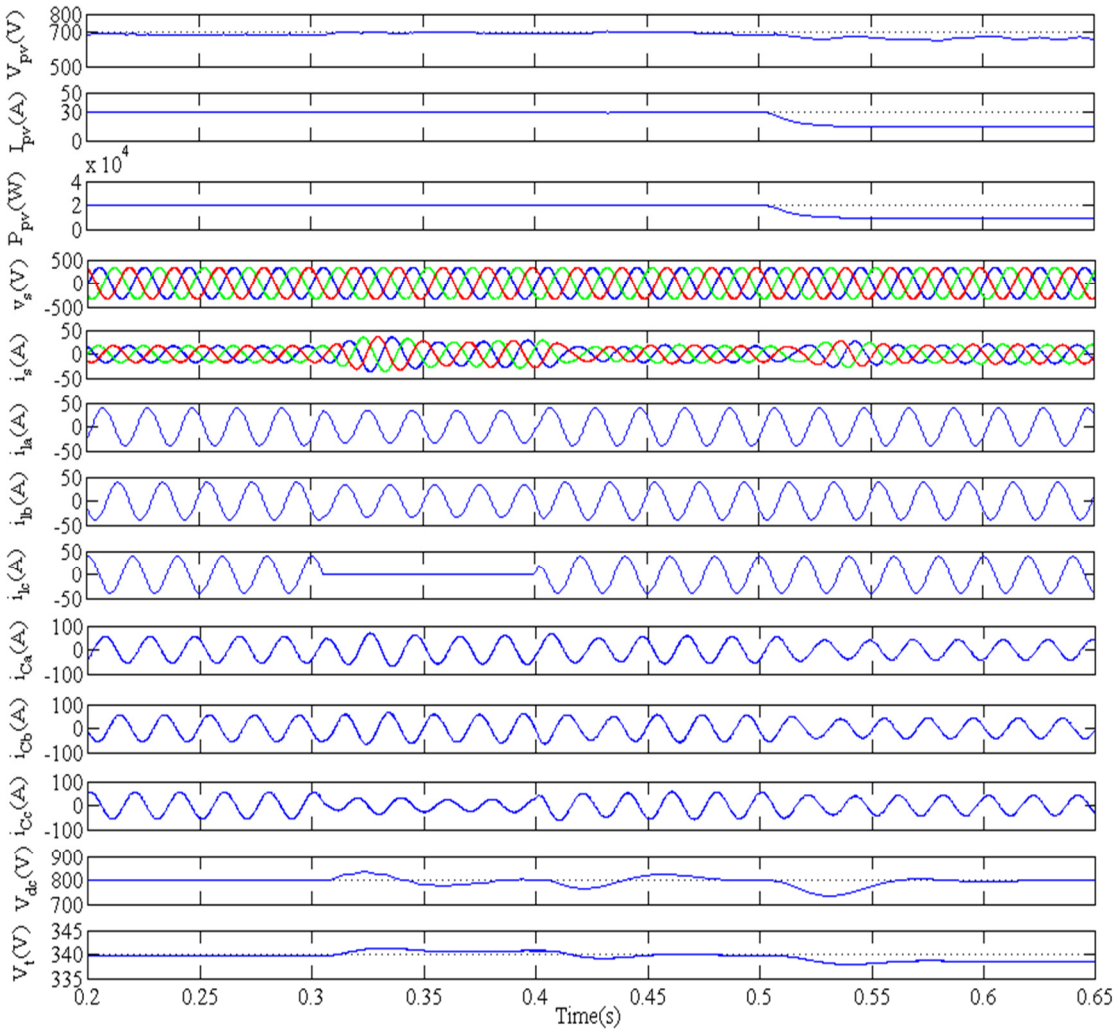


Fig. 8.24 Performance of SPV system in voltage regulation mode under linear load

voltages are regulated to their reference values under unbalanced load condition. The power of SPV system is reduced to half of its designed value to 10kW, due to change in solar irradiance after t=0.5s. During this time, the active power demand of load is met partially by the AC mains.

B. Performance of SPV System in Voltage Regulation Mode Under Nonlinear Load

Fig. 8.25 shows the performance of SPV system in voltage regulation mode under nonlinear load with Wiener filter based control algorithm. These results show the waveforms for SPV voltage (V_{pv}), SPV current (I_{pv}), SPV power (P_{pv}), PCC voltages (v_s), supply currents (i_s), load currents (i_{la}, i_{lb} and i_{lc}), VSC currents (i_{Ca}, i_{Cb} and i_{Cc}), DC bus voltage (V_{dc}) and PCC voltage amplitude

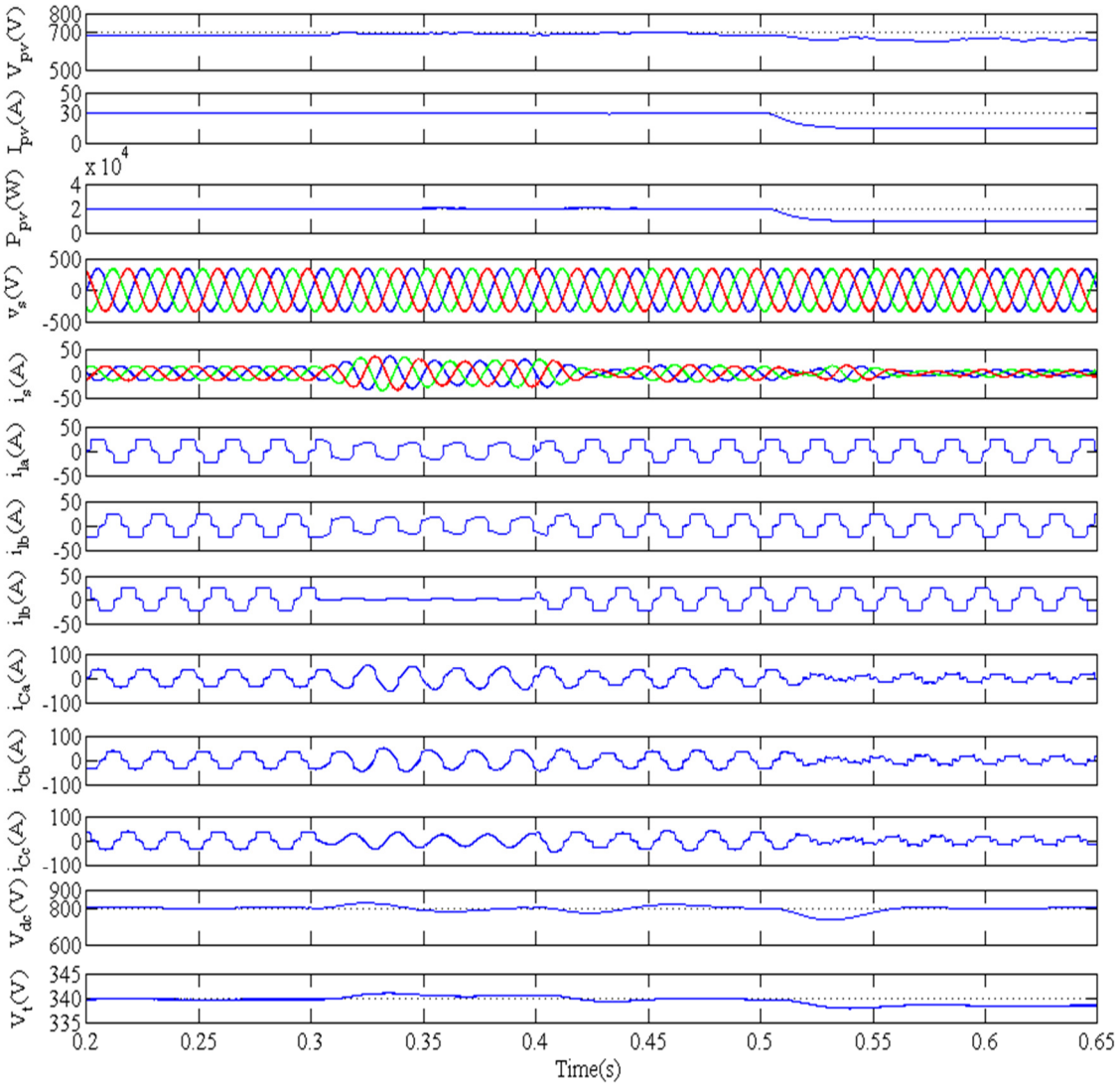


Fig. 8.25 Performance of SPV system in voltage regulation mode under nonlinear load

(V_t). The supply currents are observed to be balanced and sinusoidal in steady state (before t=0.3s) condition. During unbalanced load condition (t=0.3s to t=0.4s), the supply currents are observed to be balanced and sinusoidal but reduced in magnitude. The active power demand of the load is met by SPV system. The excess power generated by the SPV system is fed into the AC mains. The effect of decrease in solar irradiance is observed at t=0.5s which causes power generation from SPV system to decrease. Since, the SPV system is unable to meet the total power requirement of the load, hence partial active power demand of the load is supplied by the

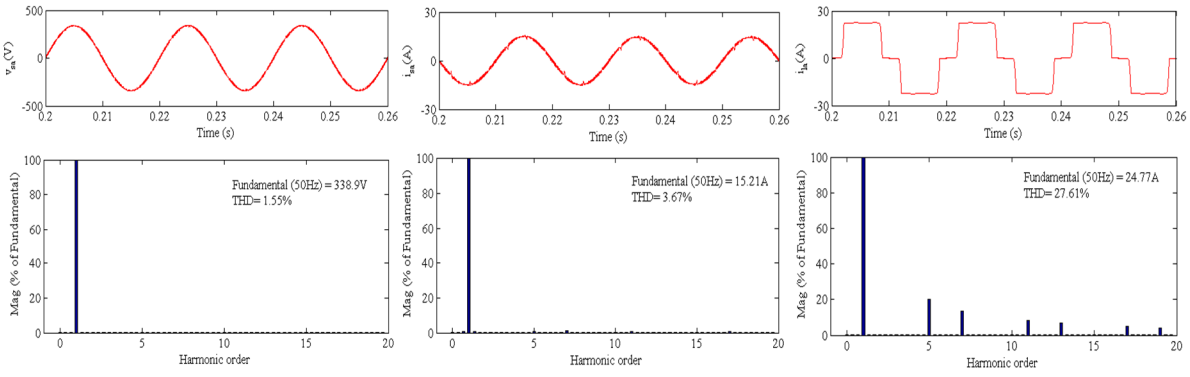
AC mains. The DC bus and AC bus voltages are maintained at their reference values of 800V and 339V respectively under varying load conditions.

Fig. 8.26 shows the harmonic spectra of phase 'a' of PCC voltage (v_{sa}), supply current (i_s) and load current (i_l). These harmonic spectra show THD of 1.55%, 3.67% and 27.61% in PCC voltage, supply current and load current. These results present improved THD in supply current having a value of 3.67% although there is THD of 27.61% in load current. The THDs of PCC voltage and supply current are also observed to be within the limit specified by IEEE-519 standard.

8.6.3 Performance of SPV System With Recursive Inverse Based Control Algorithm

The performance of the recursive inverse based control algorithm for the control of grid connected SPV system is presented here. This algorithm is tested for real power demand of the load fed from SPV system along with the load compensation. The SPV system is able to achieve harmonics reduction and provides reactive power compensation and load balancing in PFC and voltage regulation modes under linear and nonlinear loads.

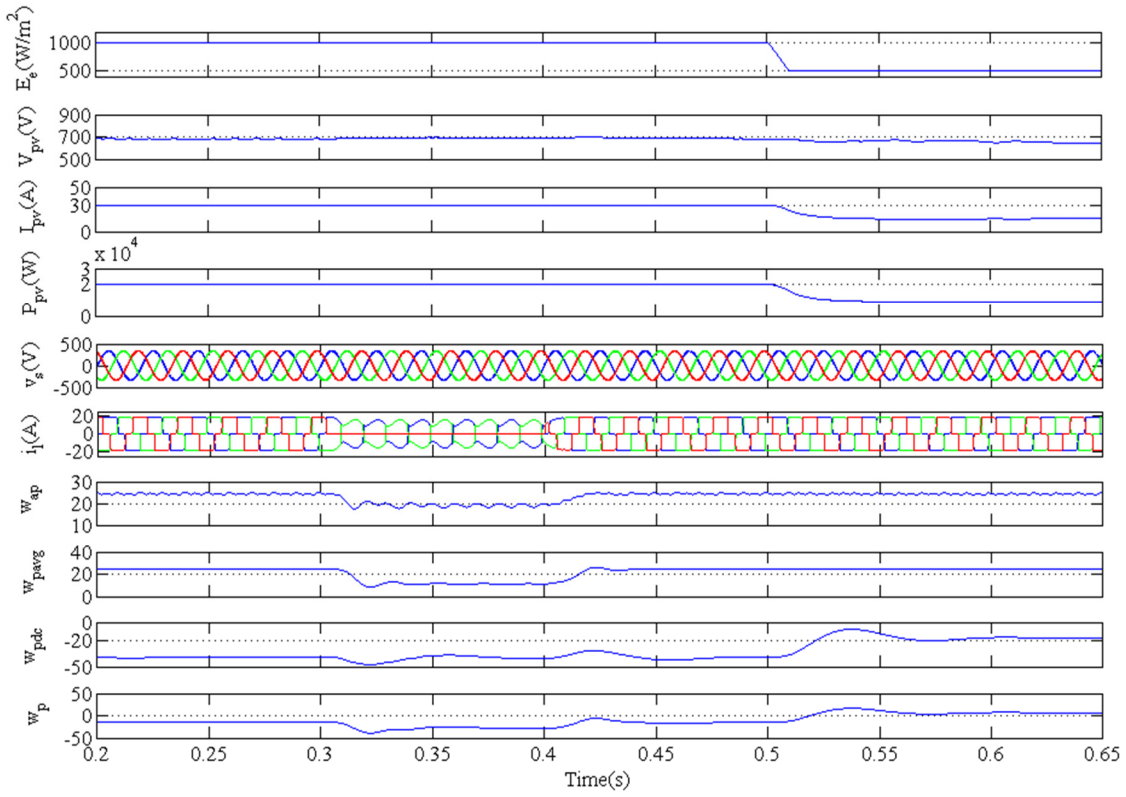
8.6.3.1 Performance of Recursive Inverse Based Control Algorithm



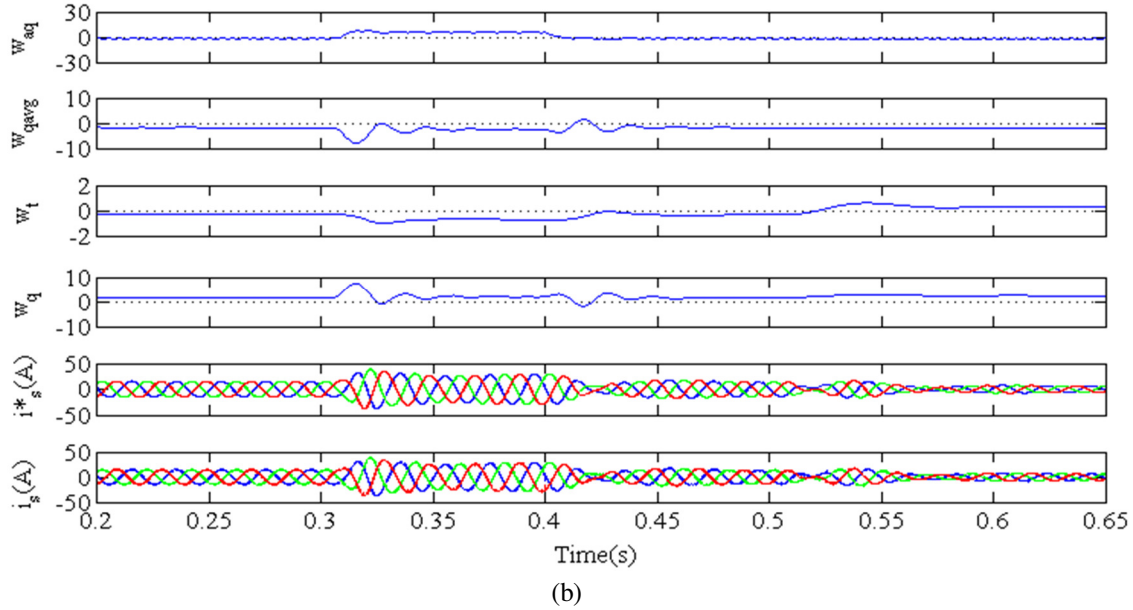
(a) (b) (c)

Fig. 8.26 Harmonic spectra of phase 'a' of (a) PCC voltage, v_{sa} (b) supply current, i_{sa} (c) load current, i_{la} in voltage regulation mode

Figs. 8.27(a) and (b) show the performance of recursive inverse based control algorithm for control of SPV system along with the intermediate signals. Fig. 8.27 (a) depicts the waveforms



(a)



(b)

Fig. 8.27 Performance and intermediate signals of recursive inverse based control algorithm

of solar irradiance (E_e), SPV voltage (V_{pv}), SPV current (I_{pv}), SPV output power (P_{pv}), PCC voltages (v_s), load currents (i_l), fundamental active power weight corresponding to phase 'a' of load current (w_{ap}), average active power weight (w_{pavg}), output of DC bus PI controller (w_{pdc}) and reference active power weight (w_p). These results are shown under steady state (before t=0.3s) condition, unbalanced load condition (t=0.3s to t=0.4s) and variable solar irradiance conditions.

Fig. 8.27(b) shows the waveforms of fundamental reactive power weight corresponding to phase 'a' of load current (w_{aq}), average reactive power weight (w_{qavg}), output of AC bus PI controller (w_t), reference reactive power weight (w_q), estimated reference supply currents (i_s^*) and actual supply currents (i_s). It is observed from these results that the actual supply currents perfectly track the reference supply currents in dynamic load conditions.

8.6.3.2 Performance of SPV System in PFC Mode Under Linear and Nonlinear Loads

Performance of SPV system using recursive inverse based control algorithm in PFC mode is presented here. The results are shown under both linear and nonlinear loads. The output power of SPV array along with load, supply and SPV system active and reactive powers are also presented.

A. Performance of SPV System in PFC Mode Under Linear Load

Fig. 8.28 shows dynamic performance of the system in PFC mode using recursive inverse based control algorithm under a linear load of 20kVA, 0.8 pf lagging load. The waveforms of SPV voltage (V_{pv}), SPV current (I_{pv}), SPV output power (P_{pv}), PCC voltages (v_s), supply currents (i_{sa}, i_{sb} and i_{sc}), load currents (i_{la}, i_{lb} and i_{lc}), VSC currents (i_{Ca}, i_{Cb} and i_{Cc}) and DC bus voltage (V_{dc}) are shown in this figure. The supply currents are observed to be balanced and sinusoidal in steady state (before t=0.3s) condition. An unbalancing in the load is created, when phase 'c' load is removed. During load unbalancing (t=0.3s to t=0.4s), it is observed that the supply currents

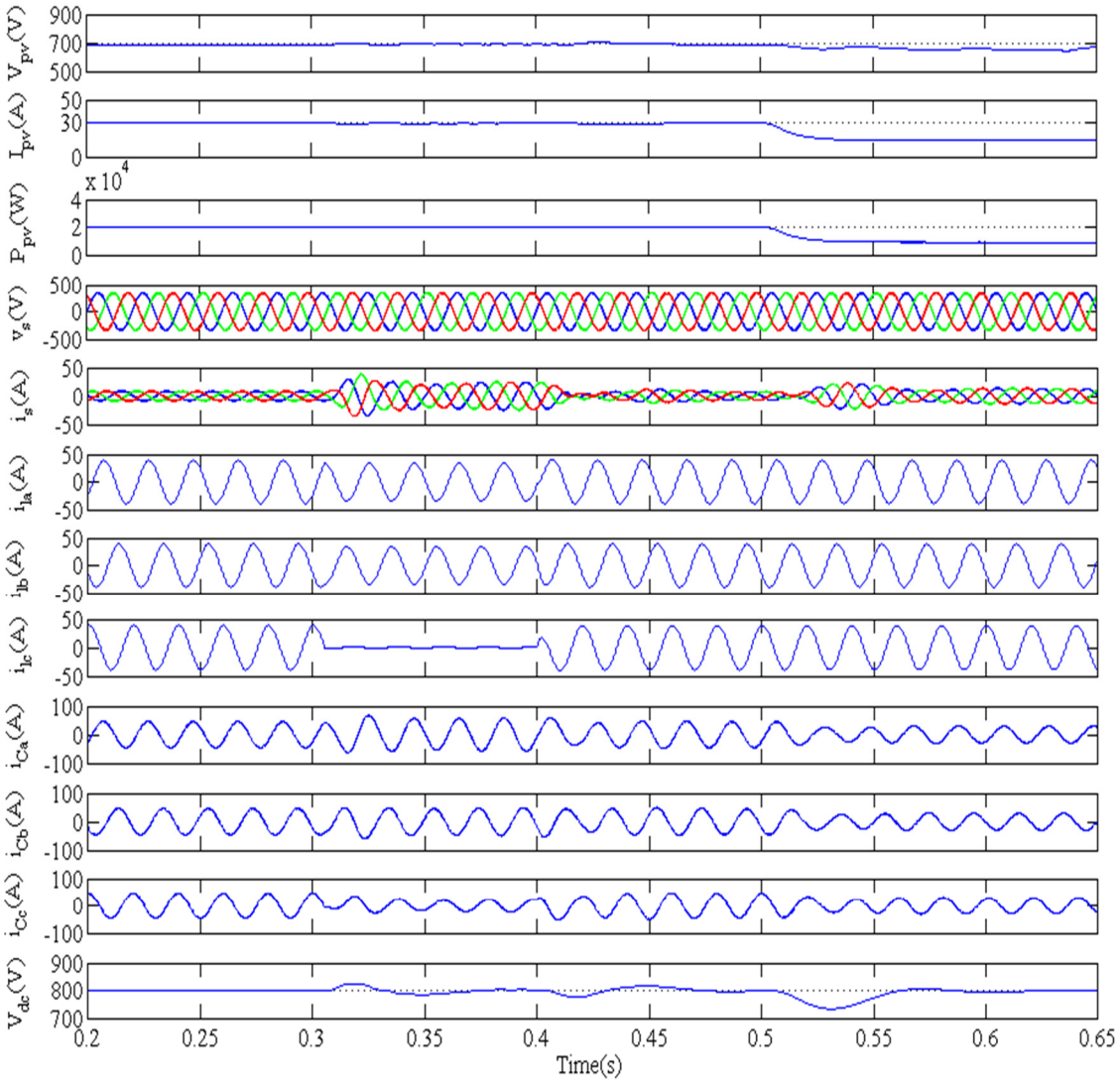


Fig. 8.28 Performance of SPV system in PFC mode under linear load

are balanced and sinusoidal with the control action of VSC of SPV system. The active power demand of the load is fulfilled by SPV system. The surplus power generated by the system is fed to the utility grid. The supply voltages and currents are observed to be in phase with each other. The solar irradiance is reduced at t=0.5s, which causes power generation from SPV system to decrease at 500W/m^2. The load active power demand is higher hence the AC mains now partially meets the load requirement. The DC bus voltage of VSC is maintained to its reference value of 800V under all dynamic load conditions.

B. Performance and Power of SPV System Under Linear Load

Fig. 8.29 presents the generation and evacuation of power by SPV system. The waveforms of SPV output voltage (V_{pv}), current (I_{pv}), power (P_{pv}), load real power (P_l), supply real power (P_s), and SPV real power (P_C), load reactive power (Q_l), supply reactive power (Q_s) and SPV reactive power (Q_C) are shown here. In steady state condition (before t=0.3s), the output voltage of SPV system is 680V, current is around 30.5A, which gives output power around 20kW. The load active power demand is around 16kW, which is fed by SPV system and an excess power is transferred to the AC mains. Similarly the load reactive power demand is around 12kVAR,

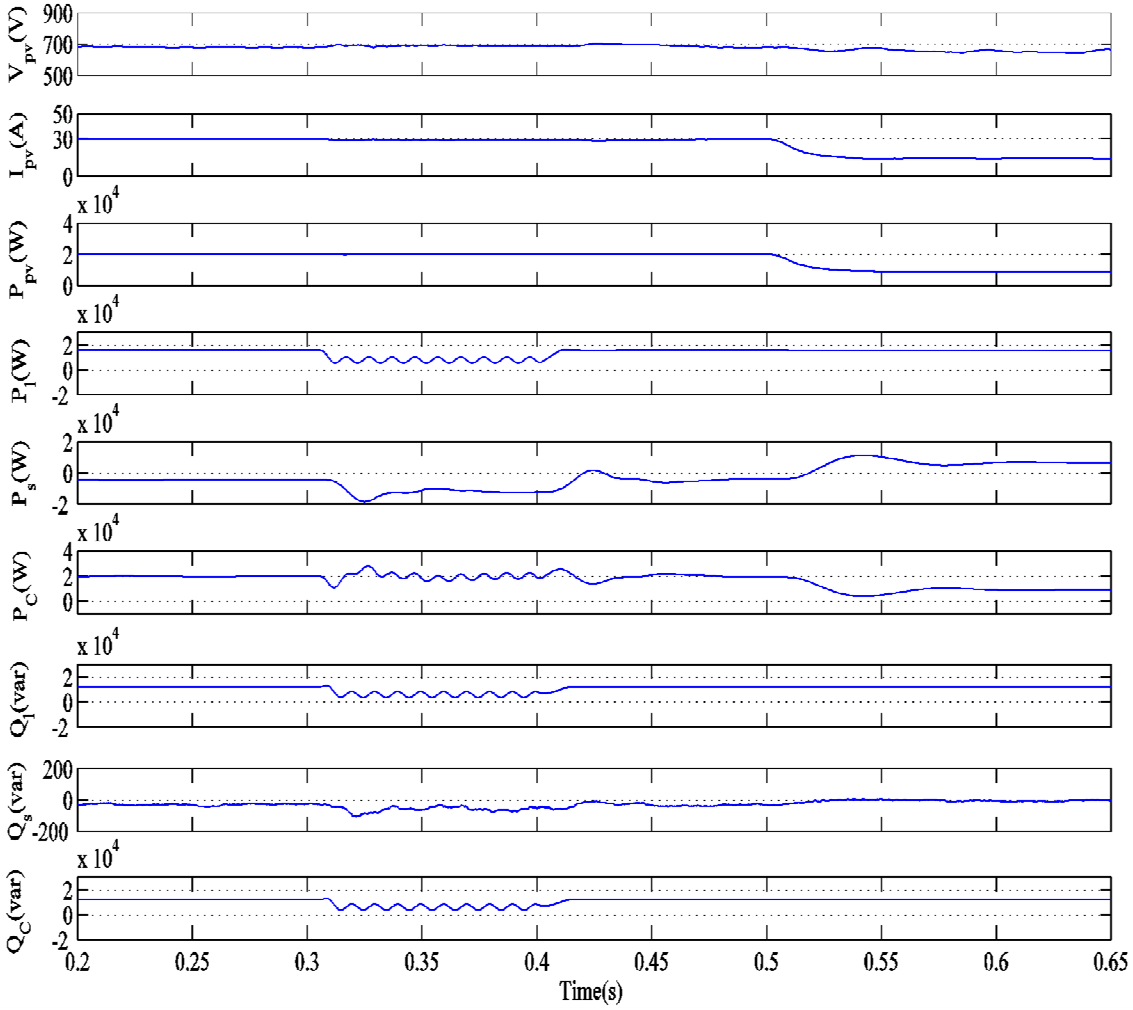


Fig. 8.29 Performance and power of grid connected SPV system under linear load

which is fed by VSC of SPV system. An unbalancing in the load is created during t=0.3s to t=0.4s. In unbalanced load condition, the output power of SPV system is unaffected and the active and reactive power demands of load are fulfilled by SPV system. Hence, there is negligible reactive power burden on the supply side. The SPV system power is reduced (after t=0.5) due to change in irradiance level from 1000W/m^2 to 500W/m^2. During this time, the active power demand of load is partially fed by the AC mains and the SPV system, whereas reactive power demand of the load is completely fed by VSC system.

C. Performance of the SPV System in PFC Mode Under Nonlinear Load

Fig. 8.30 presents the performance of the SPV with recursive inverse based control algorithm in PFC mode under nonlinear load. The waveforms of SPV voltage (V_{pv}), SPV current (I_{pv}), SPV output power (P_{pv}), PCC voltages (v_s), supply currents (i_s), load currents (i_{la}, i_{lb} and i_{lc}), VSC currents (i_{Ca}, i_{Cb} and i_{Cc}) and DC bus voltage (V_{dc}) are shown in these results. The supply currents are observed to be balanced and sinusoidal in steady state (before t=0.3s) condition. During t=0.3s to t=0.4s, the load becomes unbalanced and the supply currents are observed to be still balanced and sinusoidal under nonlinear load condition. The active power demand of load is fulfilled by SPV system. The excess power generated by the SPV system is fed to the AC mains. Solar irradiance is decreased at t=0.5s, which causes the power generation from SPV system to decrease. The load active power demand is now (after t=0.5s) partially supplied by the AC mains and partially by SPV system. The DC bus voltage of VSC is maintained to its reference value of 800V by controller action.

Fig. 8.31 shows the harmonic spectra of phase 'a' of PCC voltage (v_{sa}), supply current (i_{sa}) and load current (i_{la}). These results show a THD of 1.22%, 3.86% and 27.56% in PCC voltage, supply current and load current respectively. The THD in supply current is achieved as 3.86%,

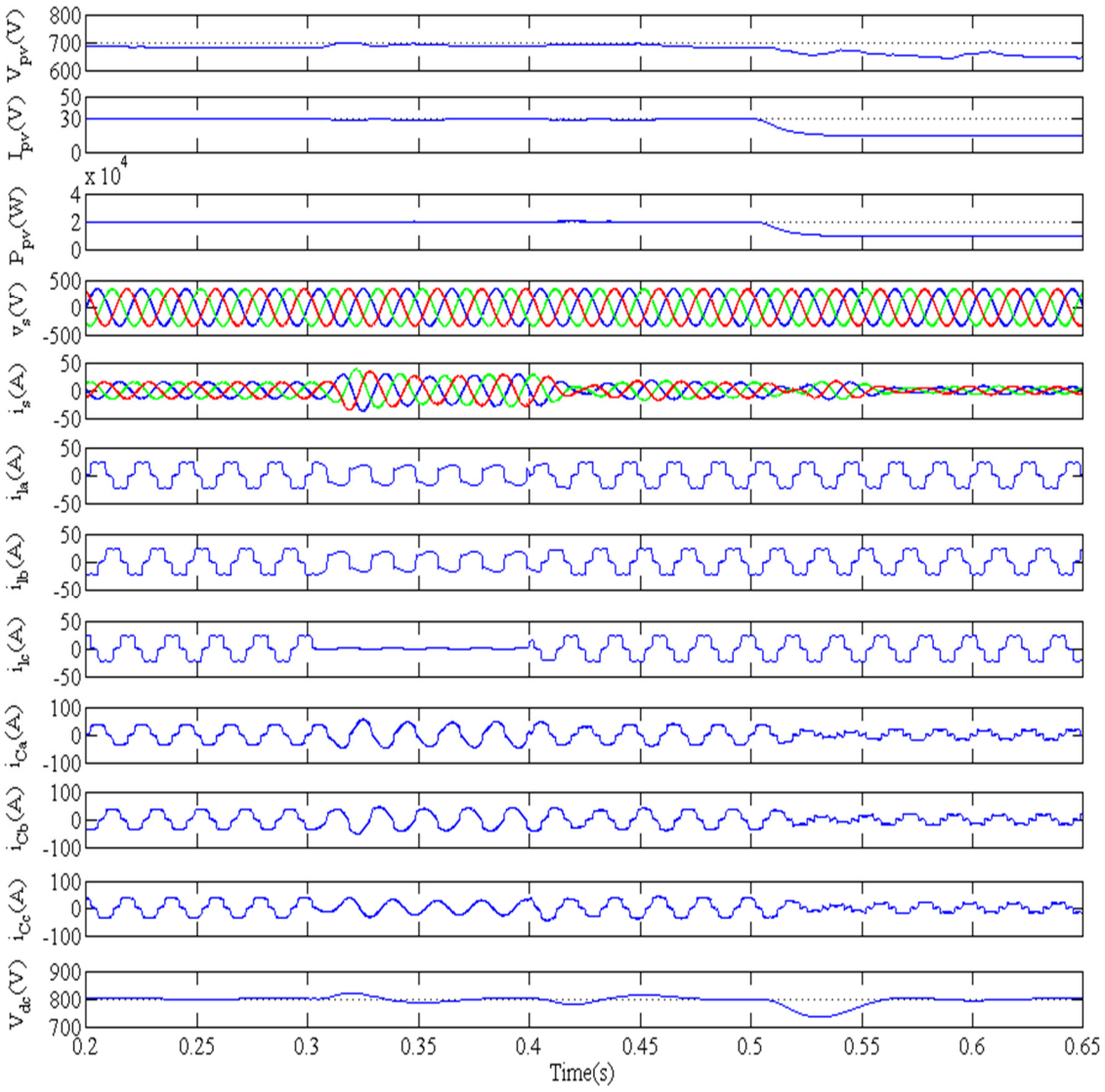


Fig. 8.30 Performance of SPV system in PFC mode under nonlinear load

whereas there is 27.56% THD in load current. These results show the satisfactory performance of the SPV system for harmonics elimination and load balancing in PFC mode. The THDs of supply current and voltage are observed to be within the limit specified by IEEE-519 standard.

D. Performance of SPV System Under Nonlinear Load

Fig. 8.32 presents the performance and power of SPV system using recursive inverse based control algorithm under nonlinear load. These results present the waveforms of SPV array voltage (V_{pv}), SPV array current (I_{pv}), SPV array power (P_{pv}), load real power (P_l), supply real

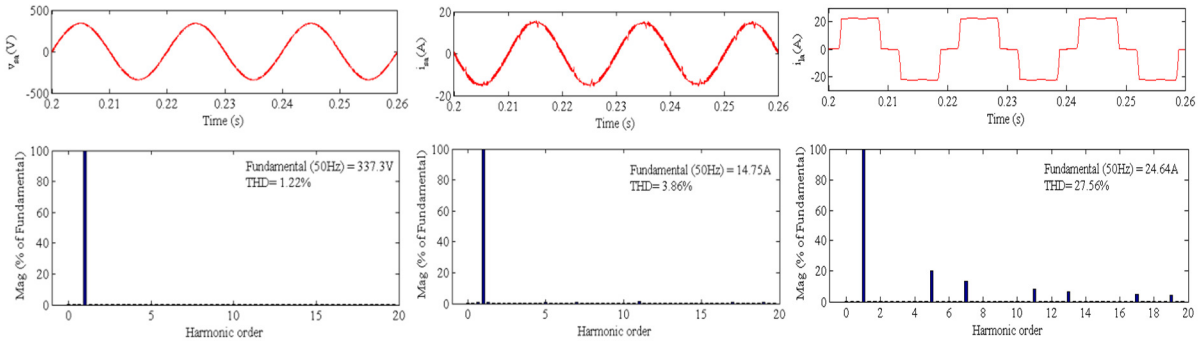


Fig. 8.31 Harmonic spectra of phase 'a' of (a) PCC voltage, v_{sa} (b) supply current, i_{sa}(c) load current, i_{la} in PFC mode

power (P_s), and SPV real power (P_C), load reactive power (Q_l), supply reactive power (Q_s) and SPV reactive power (Q_C). The output voltage (V_{pv}), current (I_{pv}) and power (P_{pv}) of SPV system

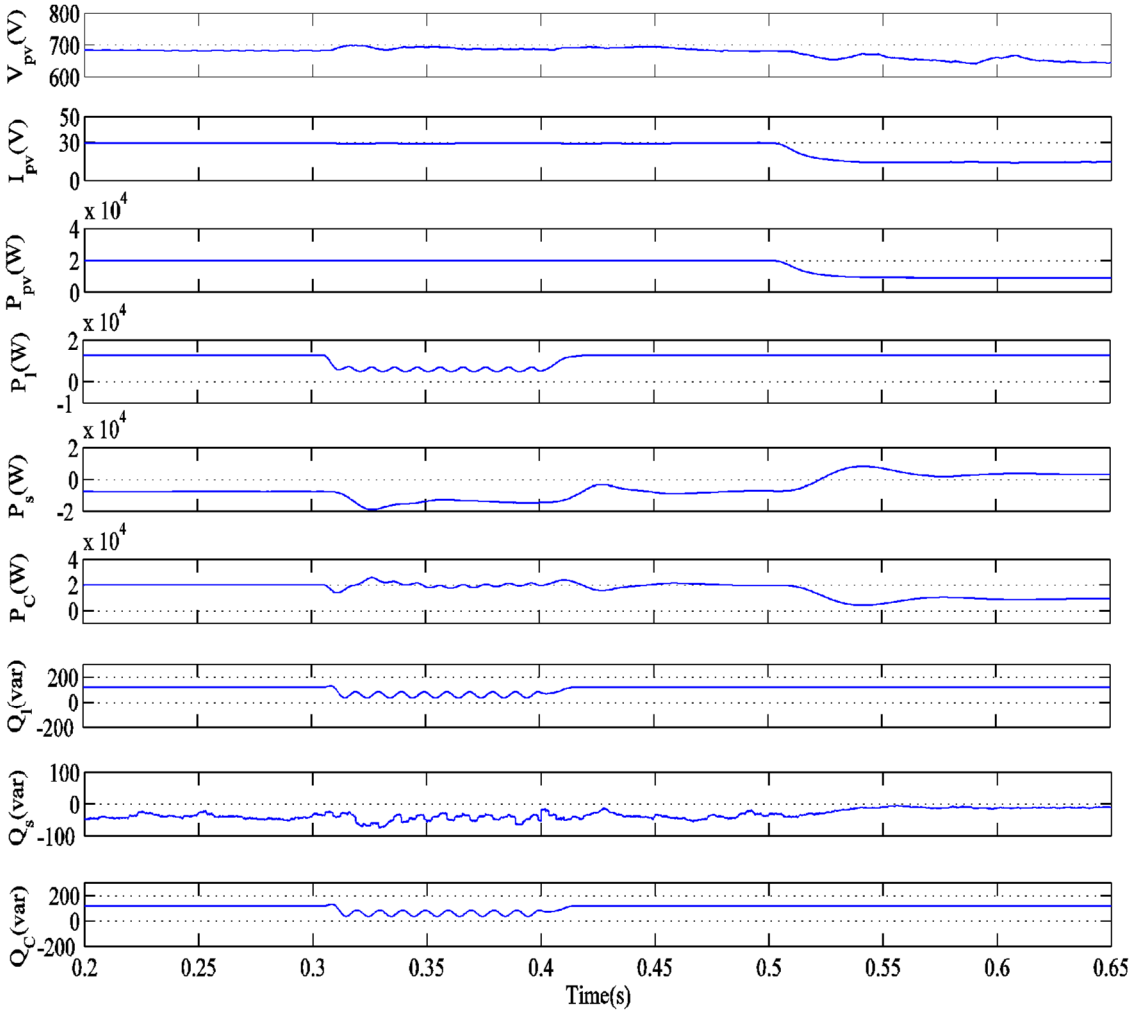


Fig. 8.32 Performance and power of SPV system under nonlinear load

are 680V, 30.5A and 20kW respectively. In steady state condition (before t=0.3s), the active power demand of nonlinear load (P_l) is around 10kW, which is fed by SPV system (P_C) and extra power is transferred to the AC mains (P_s). The reactive power demand (Q_l) of the load 12kVAR is completely fed by the SPV system (Q_C) and there is almost negligible reactive power burden on the supply side. These results present satisfactory performance of the SPV system using recursive inverse based control algorithm in feeding load active power demand along with harmonics elimination, reactive power compensation and load balancing.

8.6.3.3 Performance of SPV System in Voltage Regulation Mode Under Linear and Nonlinear Load

Performance of SPV system in voltage regulation mode with recursive inverse based control algorithm is presented here. This is divided into two parts. The first part deals with system performance under linear load and second part presents system performance under nonlinear load.

A. Performance of SPV System in Voltage Regulation Mode Under Linear Load

Fig. 8.33 presents the performance of SPV system in voltage regulation mode under linear load. The waveforms of SPV voltage (V_{pv}), SPV current (I_{pv}), SPV output power (P_{pv}), PCC voltages (v_s), supply currents (i_s), load currents (i_{la}, i_{lb} and i_{lc}), VSC currents (i_{Ca}, i_{Cb} and i_{Cc}), DC bus voltage (V_{dc}) and PCC voltage amplitude (V_t) are shown in these results. During steady state condition (before t=0.3s), supply currents are observed to be balanced and sinusoidal. The voltage at DC bus is regulated at its reference value of 800V. The PCC voltage is regulated to the reference value of 339V by injecting leading current component from SPV system. Supply currents are balanced during unbalanced (t=0.3 to t=0.4s) load condition and excess power is transferred to the AC mains. The DC and AC bus voltages are regulated to their reference values. The power of SPV system is reduced (after t=0.5s) due to change in solar irradiance.

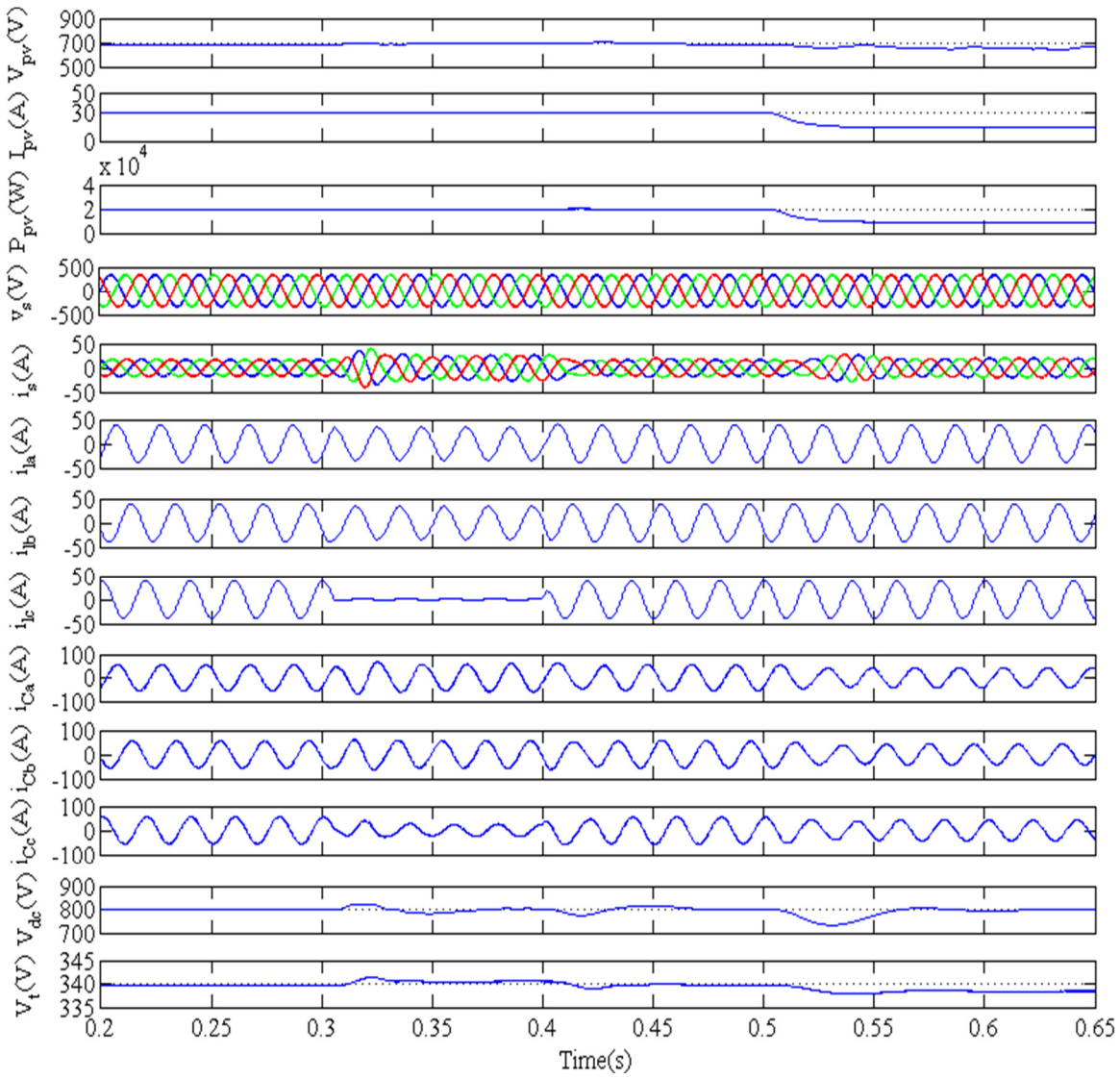


Fig. 8.33 Performance of SPV system in voltage regulation mode under linear load

During this time period, the active power demand of the load is partially fed by the supply. Moreover, the load reactive power demand is completely supplied by the VSC system.

B. Performance of SPV System in Voltage Regulation Mode Under Nonlinear Load

Fig. 8.34 presents the performance of SPV system in voltage regulation mode under nonlinear load. These results show waveforms of SPV voltage (V_{pv}), SPV current (I_{pv}), SPV output power (P_{pv}), PCC voltages (v_s), supply currents (i_s), load currents (i_{la}, i_{lb} and i_{lc}), VSC currents (i_{Ca}, i_{Cb} and i_{Cc}), DC bus voltage (V_{dc}) and PCC voltage amplitude (V_t). The supply currents are observed

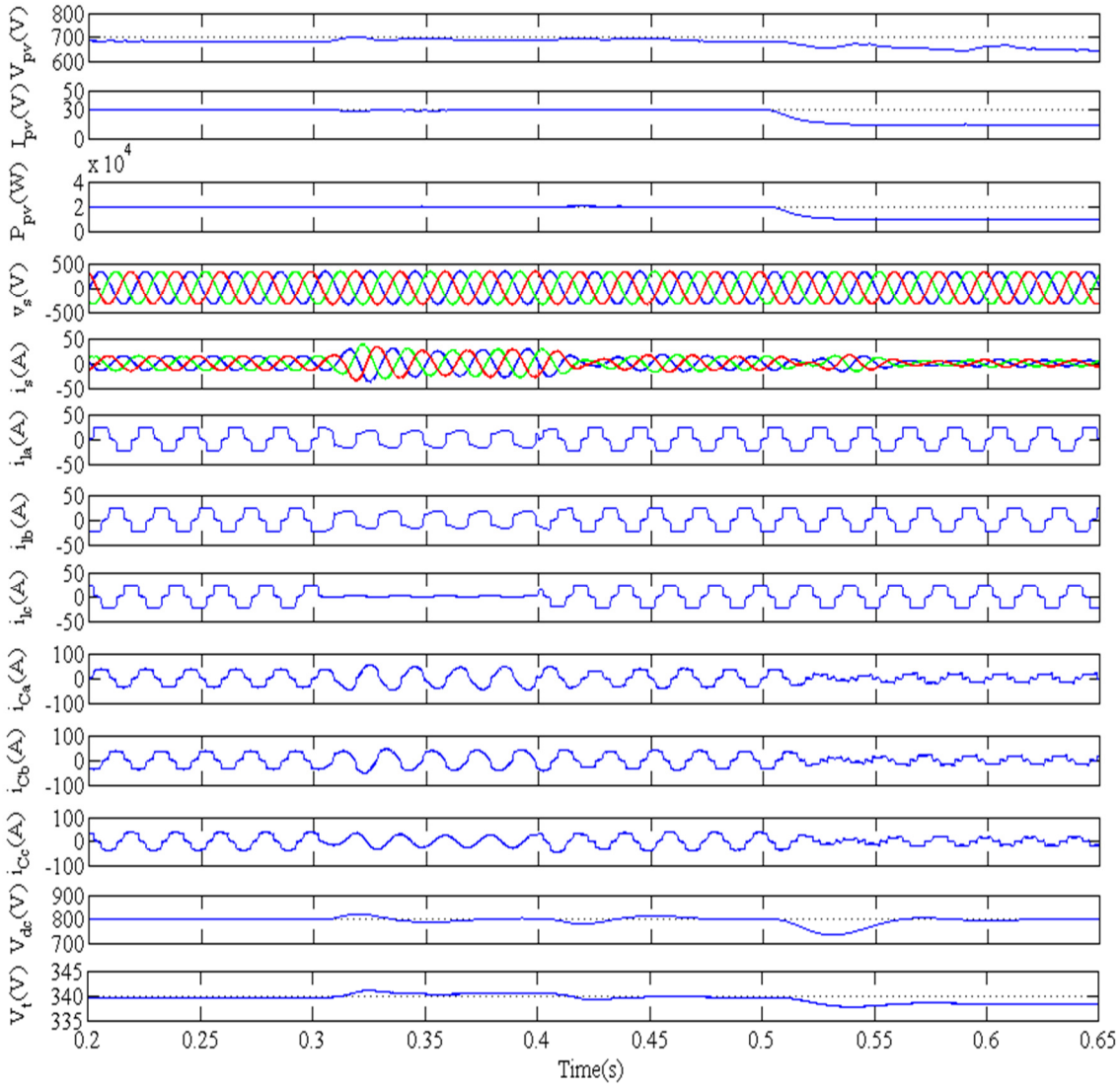


Fig. 8.34 Performance of SPV system in voltage regulation mode under nonlinear load

to be balanced and sinusoidal in steady state (before t=0.3s) condition. An unbalancing in the load is created during t=0.3s to t=0.4s. During unbalanced load, supply currents are observed balanced and sinusoidal with the control action of SPV system. The active power demand of the load is fulfilled by SPV system and the excess power generated by the system is fed to the AC mains. The solar irradiance is decreased at t=0.5s, which causes power generation from SPV system to decrease. The load active power demand is now partially supplied by the AC mains and the SPV system. The DC bus and AC bus voltages are maintained at their reference values. Fig. 8.35 shows the harmonic spectra of phase 'a' of PCC voltage (v_{sa}), supply current (i_s) and

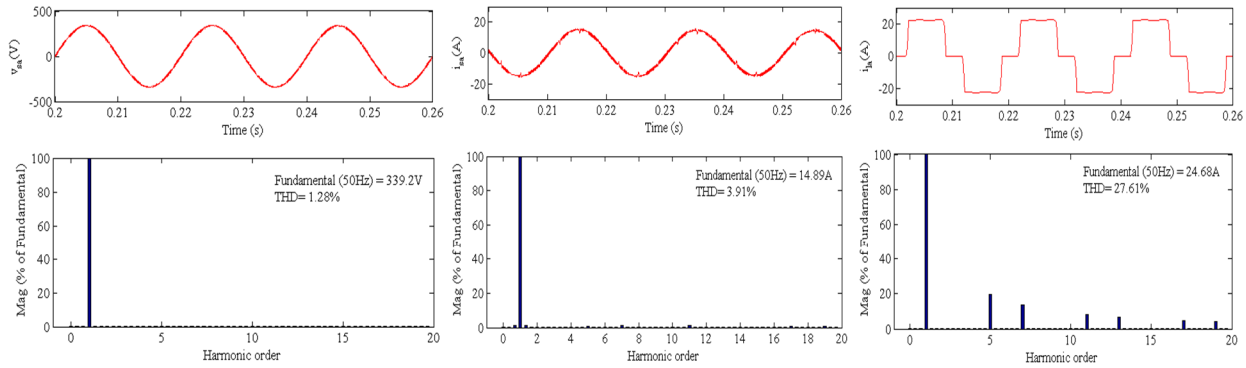


Fig. 8.35 Harmonic spectra of phase 'a' of (a) PCC voltage, v_{sa} (b) supply current, i_{sa}(c) load current, i_{la} in voltage regulation mode

load current (i_l). These harmonic spectra show THD of 1.28%, 3.91% and 27.61% in PCC voltage, supply current and load current. These results present improved THD in supply current of the order of 3.91%, whereas there is 27.61% THD in load current. The THDs of PCC voltage and supply current are observed to be less than 5% limit specified by IEEE-519 standard. These results present satisfactory performance of SPV system with recursive inverse based control algorithm in meeting real power demand of load along with providing load compensation features such as regulation of PCC voltage, harmonics reduction and load balancing.

8.7 CONCLUSIONS

The design, modeling and control of grid connected SPV system has been presented in this chapter. Various control algorithms based on SRFT, Wiener filter and recursive inverse have been developed for control of grid connected SPV system. The SPV system has been used to provide real and reactive power demand of loads along with harmonics elimination, reactive power compensation and load balancing. The performance of SPV system has been validated for both PFC and voltage regulation modes under linear and nonlinear loads. The results have been presented for linear load and nonlinear load with these control algorithms, which show satisfactory performance of SPV system in evacuating real power and improvement of power quality at distribution level. The THD in supply current has been observed within the limit

specified by international standards in case of SRFT, Wiener filter and recursive inverse based control algorithms under nonlinear loads. The reactive power demand of load under steady state condition, unbalanced load condition and reduced solar irradiance condition has been provided by SPV system using these control algorithms.

CHAPTER-IX
MAIN CONCLUSIONS AND SUGGESTONS FOR FURTHER WORK

9.1 GENERAL

The main objectives of this research work are to design and develop three phase, three-leg DSTATCOM, to implement different control algorithms and to consider its application in integrating grid connected SPV array. Several control algorithms are used to estimate reference supply currents which when compared with sensed supply currents are used to generate switching pulses for three phase VSC used as DSTATCOM. The developed control algorithms have been classified into four categories such as conventional control algorithms, adaptive theory based control algorithms, recursive theory based control algorithms and artificial intelligence based control algorithms. Various functions of DSTATCOM are presented in the proposed work which include harmonics current elimination, reactive power compensation and load balancing in PFC and voltage regulation modes under linear and nonlinear loads. The design and simulation of DSTATCOM are performed in MATLAB environment using SIMULINK and SPS tool boxes. The experimental prototype of DSTATCOM is developed in the laboratory using a VSC, DSP (dSPACE 1104 R&D controller) and Hall effect voltage and current sensors. The application of DSTATCOM in integrating renewable energy source such as SPV array to the grid is also presented. This system injects power generated from SPV array to the grid along with all the functions of DSTATCOM.

9.2 MAIN CONCLUSIONS

The control algorithms have been designed and developed for the control of three-phase, three-leg DSTATCOM. These algorithms have been categorized into four major categories based upon

their operating principle. The performance of these algorithms based on their design, tuning of parameters, computational complexity and implementation is discussed as follows.

- The design and development of conventional control algorithms for DSTATCOM have been carried out for improving current related power quality problems at the distribution system. These control algorithms included under this category are power balance theory, instantaneous reactive theory, conductance based and instantaneous symmetrical component theory based control algorithms. The extension of these control algorithms for regulation of PCC voltage magnitude has been presented in this work. The voltage regulation is required in various isolated power generation systems and distributed generation system in islanded condition and it is an important power quality issue to be studied and investigated.
- The control algorithms based on adaptive theory have been developed for control of DSTATCOM. The performance of these control algorithms have been presented for several power quality problems such as harmonics current elimination, reactive power compensation and load balancing in PFC and voltage regulation modes. The algorithms based on Wiener filter theory, fixed step size least mean square (FSSLMS) theory and variable step size least mean square (VSSLMS) theory have been developed under this category. The Wiener filter based control algorithm has been found to be simple in implementation with reduced computational burden. The variants of FSSLMS technique such as basic LMS, normalized least mean square (NLMS) and signed error least mean square (SLMS) have been identified and developed for DSTATCOM. The NLMS based control technique has been found suitable in terms of fast weight convergence and a low steady state error. It has been observed that there is a tradeoff between smaller and larger

step size in FSSLMS based approach, i.e. smaller step size leads to slow convergence rate and small steady state error, while larger step size leads to fast convergence and large steady state error. The VSSLMS based approach resolves the problem of convergence rate and steady state error and it has positive aspects such as faster convergence rate, lower steady state error and higher stability.

- Some control algorithms based on recursive theory have been implemented for current related power quality problems at the distribution system. The control of three phase VSC used as a DSTATCOM has been performed with these control algorithms. This category includes implementation of recursive least square (RLS), recursive inverse (RI) and immune feedback based control algorithms. These control techniques have been utilized to estimate the weighted values corresponding to the fundamental active and reactive power components of the distorted load currents.

  The variable forgetting factor has been utilized in RLS based control technique. The main features of variable forgetting factor recursive least square (VFFRLS) based control are that it offers fast convergence rate and robustness with system parameters than the fixed variable forgetting factor RLS. The recursive inverse based control algorithm is found useful in terms of reduced computational complexity. This has been achieved because the computation of inverse of auto correlation matrix is not required. Another algorithm based on immune feedback principle has also been developed for estimation of weighted values corresponding to fundamental active and reactive power components of load currents under this category. Various control algorithms under this category have been tested under steady state and unbalanced load conditions. Positive features of this category of control algorithm

are that they are fast, require few mathematical operations and easy to implement using DSP.

- The artificial intelligence based control algorithms have been developed based on the principle of human intelligence for mitigation of power quality problems such as reactive power compensation, harmonics current elimination and load balancing at distribution system. The control algorithms developed under this category include adaptive neuro fuzzy inference system (ANFIS), real time recurrent learning (RTRL) and adaptive neuro fuzzy inference system least mean square (ANFIS-LMS) based control algorithm.

  The ANFIS based controller for control of DC bus voltage and AC bus voltage has been observed to provide fast transient and steady state response, learns faster, produces lower error and achieves reference voltage value faster than the conventional PI controller. The RTRL based control algorithm has been used for the estimation of weighted values corresponding to fundamental active and reactive power components of load currents. This algorithm has been found suitable for real time application, because it contains dynamic elements and internal feedback elements. The efficiency of learning is improved in RTRL by providing internal feedback loops to store information for later use. The use of feedback network in recurrent network makes them suitable for fundamental weighted value estimation. Additionally, the method is completely online and simple to implement. The control algorithm based on ANFIS-LMS has also developed under this category. The major advantages of this control algorithm that have been achieved include a low static error and fast convergence of weights in steady state and unbalanced load conditions. The ANFIS controller learns faster and achieves less error in estimation of step size parameter for LMS technique.

- The VSC used for DSTATCOM has also been utilized as power converter to inject power generated from SPV array to the grid and performs functions of DSTATCOM such as harmonics current elimination, reactive power compensation and load balancing. The functions of DSTATCOM have been performed in PFC and voltage regulation modes under linear and nonlinear loads. A two stage SPV array of 20kW peak power capacity has been considered, which includes DC-DC boost converter and DC-AC power converter. The duty cycle of DC-DC boost converter has been controlled with the help of incremental conductance based maximum power point tracking (MPPT) algorithm. The control of VSC for power transfer from SPV array to grid and compensation of power quality problems have been performed with suitable control algorithms. The control algorithms developed for grid connected SPV array include SRF, Wiener filter and recursive inverse theory for estimation of fundamental active and reactive power component along with SPV power feed forward loop. Satisfactory performances of grid connected SPV system have been observed using these control algorithms in evacuating real power and improving quality of power at distribution level under linear and nonlinear loads. The reactive power demand of load has been provided by VSC used in SPV system. The THD in supply current after compensation has been observed within the limit specified by international standards.

9.3 SUGGESTIONS FOR FURTHER WORK

This research work carried out includes the development of three phase DSTATCOM, control algorithms and application of DSTATCOM in grid integration of SPV array. Time domain approach based control algorithms have been developed and subdivided into four categories. These control algorithms for control of DSTATCOM have been designed for improving current

related power quality problems at the distribution system. The research areas for further scope of work are suggested as,

- These algorithms can be extended for mitigation of power quality problems along with neutral current compensation in three phase four wire DSTATCOM systems.
- Various other time domain and frequency domain approach based control algorithms can be developed to achieve desired response of DSTATCOM.
- The developed control algorithms can be applied in isolated power generating systems such as wind based, solar based and micro-hydro based generation for power transfer to the loads, voltage regulation and compensation of power quality problems.
- Experimental verification of grid connected SPV system with the proposed control algorithms can also be extended for power transfer to the grid along with compensation of power quality problems.

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APPENDIX-A

Simulation parameters for three phase DSTATCOM

AC mains: Three phase, 415V (L-L), 50Hz with source impedance (R_s=0.04 and L_s=1mH)

Parameters of DSTATCOM,

DC bus voltage: 700V

DC bus capacitance: 1650μF

Interfacing inductors: 3mH

Ripple filters: 3Ω and 4μF

Load: Three phase diode bridge rectifier with R=15Ω and L=100mH

Calculation of current rating of IGBT:

$i_{sm} = 1.25(I_{sw} + I_{cr})$

where I_{sw} and I_{cr} are the peak values of compensator current and allowed ripple currents (20% of I_{sw}). $I_{sw(rms)}$= 18.95A

$I_{sw} = 18.95 * \sqrt{2} = 26.8$A and $I_{cr} = 26.8 * \frac{20}{100} = 5.36$A

$i_{sm} = 1.25(I_{sw} + I_{cr}) = 1.25(26.8 + 5.37) = 40.21$A

Switching frequency: 10kHz

Cut off frequency of low pass filters (LPFs),

DC bus LPF: 10Hz

AC bus LPF: 12Hz

APPENDIX-B

Parameters of developed three phase DSTATCOM hardware

AC mains: three phase, 110V (L-L), 50Hz

Parameters of DSTATCOM,

DC bus voltage: 200V

DC bus capacitance: 1566μF

Interfacing inductors: 3mH

Ripple filters: 4Ω and 5μF

Loads (i) Linear load: three phase series connected resistive inductive loads with rating 15kVA, 3-ph, 0.7 to 1pf lagging

(ii) Nonlinear load: three phase diode bridge rectifier resistive load and filter inductance, ratings of resistive load are single phase, 24A and 250V and fixed single phase variable inductance of 100mH

Controller: dSPACE DS1104 R&D Controller board with slave DSP subsystem TMS320F240

Switching frequency: 10kHz

Voltage source converter: IGBT based three legs with Semikron make SKM150GB12V IGBT module

Gate driver: SKYPER 32PRO R

Recommended temperature range: -40℃ to 150℃

Hall effect voltage sensor: LEM LV-25p

Hall effect current sensor: LEM LA-25np

Components used in gating circuit: n-p-n transistor (2N2222), hex inverter IC (7406)

Auto transformer: three phase, 415/0-415, 50Hz, 28A

Computation of PI controller proportional (k_p) and integral (k_i) gains:

The gain values are chosen based on Ziegler-Nichols method. The values of PI controller gains are found by setting initially only k_p and assuming k_i =0. The value of k_p is increased until sustained oscillation (marginally stable) takes place. That value of k_p is known as critical gain k_{cr}. The period of oscillation p_{cr} should be measured when amplitude of oscillation is quite small. According to Ziegler-Nichols method, once the value of k_{cr} and p_{cr} are obtained, the proportional k_p and integral gain k_i can be obtained as,

$k_p = 0.45\ k_{cr}$

$k_i = (1/1.2)\ p_{cr}$

APPENDIX-C

Features of developed control algorithms for three phase DSTATCOM is given in Table-C.1.

TABLE C.1

Comparison of control algorithms

Control Algorithms	Features of control algorithms			
	Modeling	Formulation	Computational burden on DSP	Dynamics of DC bus voltage
PBT	Easy	Instantaneous power and reference currents estimation	55µs	Stable
IRPT	Easy	Instantaneous active and reactive power calculation	55µs	Stable
Conductance	Complex	Computation of conductance and susceptance	65µs	Stable
ISCT	Easy	Instantaneous active power calculation	60µs	Less stable
Wiener filter	Easy	Basic mathematical operations	45 µs	Stable
FSSLMS	Easy	Basic mathematical operations	50µs	Less stable
VSSLMS	Complex	Basic mathematical operations	60µs	Stable
VFFRLS	Easy	Basic mathematical operations	55µs	Stable
Recursive inverse	Easy	Basic mathematical operations	50µs	Stable
Immune feedback	Easy	Basic mathematical operations	45µs	Stable
ANFIS	Complex	Learning of neural network	60µs	Better performance
RTRL	Complex	Learning of recurrent neural network	65µs	Stable
ANFIS-LMS	Complex	Learning of step size parameter by ANFIS	60µs	Stable

APPENDIX-D

Design parameters of grid connected SPV system

AC mains: three phase 415V, 50Hz with source impedance (R_s=0.04 and L_s=1mH)

Design parameters of 20kW SPV array: open circuit voltage V_{oc}=19V, short circuit current I_{sc}= 4A, voltage at maximum power V_{mpp}=16V, current at maximum power I_{mpp}=3.4A

Design parameters of DC-DC boost converter: duty cycle D=0.15, L_b=1.67mH, f_{sw}=10kHz

Loads: (i) Linear load of 20kVA, 0.8pf lagging

(ii) Nonlinear load, three phase diode rectifier with R=15Ω and L=100mH

DC bus voltage: 800V

DC bus capacitance: 1650μF

Interfacing inductors: 3.2mH

Ripple series R-C filters: 5Ω and 5μF

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2. M. Badoni, A. Singh and B. Singh, "Design and implementation of ANFIS based control algorithm for DSTATCOM," *Electric Power Components & Systems*, vol. 43, iss. 15, pp. 1741-1751, 2015.
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