CHAPTER 1
INTRODUCTION

1.1 Introduction

This dissertation presents a study on designing and implementation of PID controllers using current mode or voltage mode active building blocks. The proportional-integral-derivative (PID) controller is one of the most important control system used in the process control industry. A PID controller consists of three terms namely: (1) proportional, (2) integral, and (3) derivative [1]. Proportional defines with variable time for present values of the error it means for the large and positive error, the output of controller will also be large and positive. Integral defines with variable time with integration of past values of error (integration of past differences) and Derivative defined as prediction of future values of error (differences). By carefully tuning the various gains the closed loop performance of a system can be improved significantly.

Traditionally, voltage operational amplifiers are largely used in analogue PID controllers. These op-amps (operational amplifiers) based controller have large number of active and passive components required for tuning the performance of closed loop control system [2]. Operational amplifiers have two major limitations viz. slew rate and constant product of gain and bandwidth. In the most traditional industrial problems, requirements on the selection of active component is not necessary, it depends on the general synthesis procedures [3] -[6] to perform operations of PID controller, so reduced number of parameters are required to be tuned for the closed loop control system.

1.2 PID controllers using current mode active blocks

Generally, there are two modes to perform operations in any electronic circuit, they are: (i) voltage mode and (ii) current mode operations. Several voltage and current mode continuous time filters, oscillators, analog multipliers, inductance simulators and PID controllers have been developed using a new current mode active blocks in which circuits are driven by current carrying signals.

Current mode signal processing techniques have received a wide attention dur to wide bandwidth, low voltage operation, better linearity and stability properties and simple implementations of signal operations such as addition and subtraction, and are often preferable to voltage mode counterparts [2]. These components such as current conveyors

(CCs) [7], operational trans-conductance amplifiers (OTAs) [8], current feedback operational amplifiers (CFOAs) and current differencing buffer amplifier (CDBAs) [10] are considered for PID applications where speed and large bandwidth are required.

1.3 Different Current mode active blocks

The building blocks used for implementation of PID controllers can be implemented in both Bipolar as well as CMOS technology. These blocks in general fall into the categories og voltage controlled voltage source (VCVS), voltage controlled voltage source (VCVS), current controlled voltage source (CCVS) and current controlled current source (CCCS) or many a times into a combination of more than one of these blocks. The basic design of a voltage mode or current mode building block is guided by the signal processing functions it is supposed to perform. Nevertheless certain common features which may be found in most of the current mode/voltage mode building blocks are the presence of

i. Voltage/Current differencing circuits
ii. Current source biasing arrangements
iii. Minimum number of passive components
iv. Current mirror of different types for copying of signal currents and/or bias currents from one part of the circuit to the other part.

OTA is a differential VCCS (Voltage controlled Current Source) in which input voltage controls output current [8] and it is characterised by trans-conductance (g_m). the second generation current conveyor [11] is a voltage follower with input Y and output voltage terminal X, and a current follower (or current inverter) with a current input X and output Z. in third generation current conveyor [11], the input current flows into the Y-terminal and out from the X-terminal, it is assumed that a differential current input fed output in voltage form. A current feedback amplifier is equivalent to a plus type second generation current conveyor with a voltage buffer [9]. The term current feedback is used because the signal entering at the feedback node of op-amp is in the form of current signal. CDBA is a newly introduce active circuit; it is a combination of two fundamental building blocks i.e., current differencing block and voltage follower block. FTFN is a more general and flexible building blocks compared to other active elements. They are used to function more successfully in both voltage mode and control mode e.g., voltage mode op-amps and current conveyors.

The basic current mode circuit of OTA configuration is obtained from a second order integrator loop structure consisting of the loss-less integrators [8]. An implementation of the second generation current conveyor is done by using a mixed (NMOS and PMOS) translinear loop [12]. The circuit of CFOA allows almost a rail to rail input and output operation. The configuration of CDBA is same as that of a CMOS second-generation current conveyor (CCII) [7]. With the help of these devices several filters and oscillators are built. Generally most of these devices are made for current controlling operations in such a way that it provides a better performance by using biasing current.

1.4 Dissertation Outline:

In this dissertation, the first chapter covers the introduction of PID Controller. The second Chapter covers brief study of the characteristics, implementation and applications of various current mode/voltage mode active blocks used for synthesizing PID controller has been presented. In the third chapter, PID Controller design using some active blocks and in order to test these PID controllers, implementation of current mode/voltage mode PID controller is done. In the fourth chapter, a new PID Controller is made with the help of VDTA. In the fifth chapter, summary of the project has been presented along with suggestion for some future work on this topic.

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CHAPTER II

BRIEF REVIEW OF VARIOUS ACTIVE BUILDING BLOCKS

In this chapter, we present a short description of various active building blocks used for implementation of the PID controllers. Though, a very large number of active building blocks have been proposed by various research groups in recent parts [1]. In the present chapter, we have studied only those active building blocks which have been directly used for PID controller implementation.

2.1 Operational Trans-conductance Amplifier (OTA)

2.1.1 History

In 1969, RCA produced an integrated circuit, called OTA (Operational Trans-conductance Amplifier) for the purpose of commercial needs. The first publications with OTA came out in 1985, when the [2] presented to the new CMOS based OTA architectures and new filter realizations.

2.1.2 Symbol and Characteristics Equation

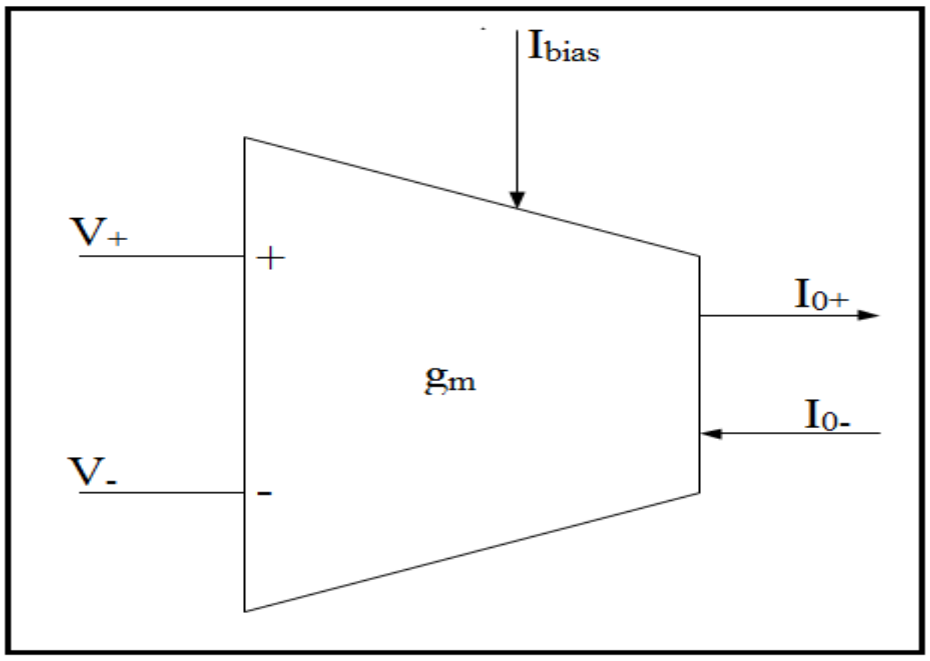

Figure 2.1.1 OTA Block Diagram

OTA is a voltage controlled current source (VCCS) in which output current is controlled by varying input voltage source and it is characterized by trans-conductance (g_m). the output current of the OTA is given as

$$I_o = g_m (V_+ - V_-),$$

Where V_+ and V_- are voltages on positive (non-inverting) and negative (inverting) input terminal of OTA.

Characteristics of ideal OTA can be summarised as below

Input impedance (Z_{in}) = ∞, Output Impedance (Z_o) = ∞, Bandwidth = ∞

2.1.3 CMOS Implementation

The Operational Trans-conductance amplifier is basically a differential voltage controlled current source and several bipolar as well as CMOS implementations have appeared in literature. In this following we present a CMOS implementation of differential input differential output OTA given in [3]. The trans-conductance is taken as follows

$$g_m = \sqrt[2]{\mu_n C_{oX} \frac{W}{L} I_b}$$

Where $\mu_n, C_{oX}, \frac{W}{L} and\ I_b$ are the electron mobility of n-type MOSFET, gate oxide capacitance per unit area, transistor aspect ratio and bias current of OTA, respectively. In the above equation, it can observe that the trans-conductance g_m is adjustable by a supplied bias current.

The complete CMOS realization of OTA using MOS transistor [3] is shown in figure 2.1.2.

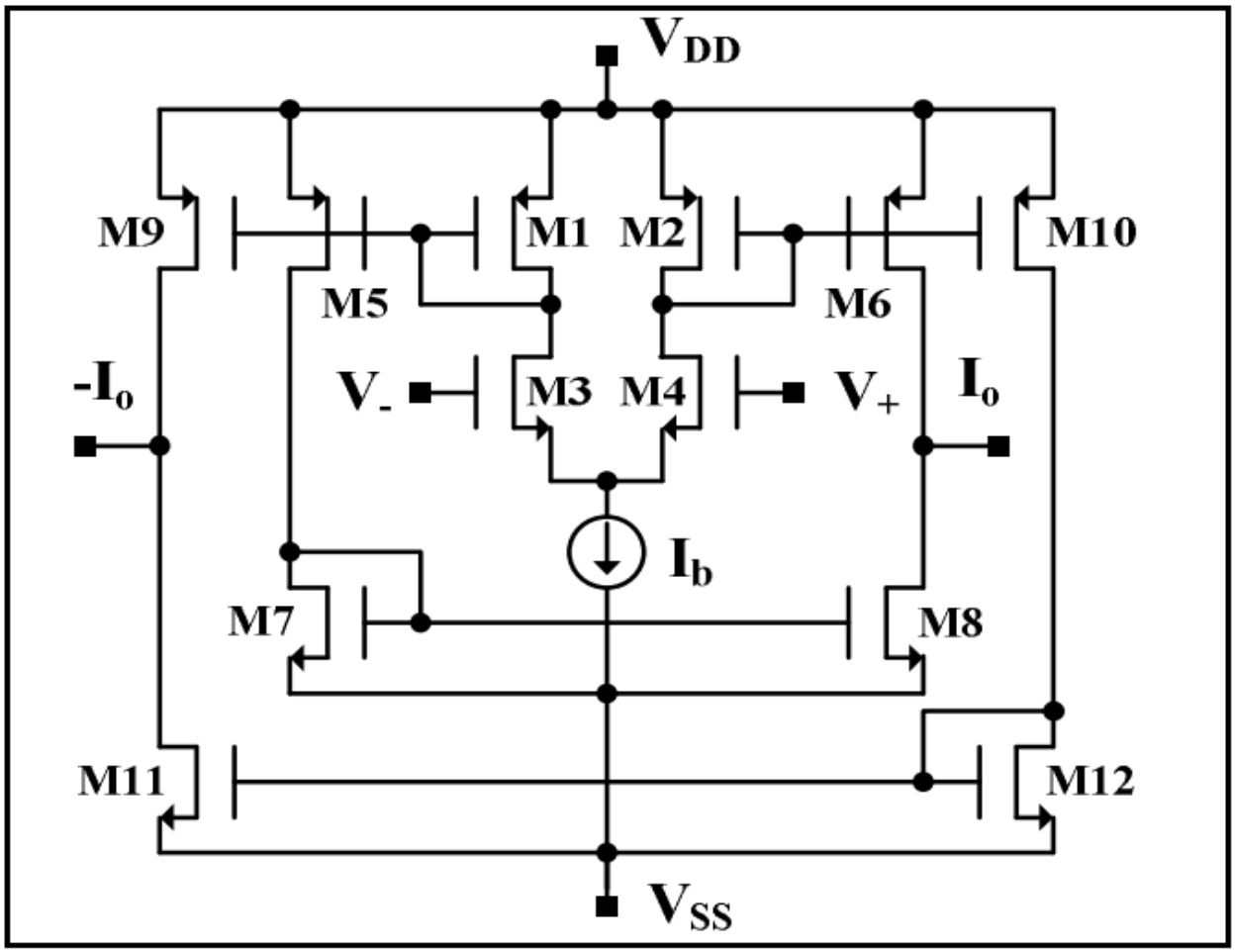

Figure 2.1.2: CMOS realisation of OTA

In [3], electronically tunable multiple- mode universal biquadratic circuits are introduced using some highly linear operational trans-conductance amplifiers (OTA) are grounded capacitor. For realisation of higher order circuit transfer function, a second order function of biquadratic circuit is a very useful block. The basic current mode circuit configuration is obtained from a second order integrator loop structure consisting of loss-less integrators. The multimode biquadratic circuits are constructed with additional OTAs to the current mode one.

2.1.4 Applications

In the recent few years, OTA-C attracts more than Operational Amplifiers IC, because it has several advantages e.g., it has wider operational linear range, and this may possible with tuning of its trans-conductance (g_m+) also, it requires a few or even no resistor for its circuitry and in addition, it is more reliable in high frequency operations as it imposes a current mode

active circuitry. OTAs, have been used for the realisation of OTA-C based filters [4]-[13], oscillators [14]-[16] in battery operated equipment. Currently, OTA element are available in the market by many manufacturers [4] a commercially available OTA element is the circuit LT1228 (Linear Technology) or MAX435 (MAXIM-Dallas Semiconductor), which is a high speed wide band trans-conductance amplifier (WTA) with high impedance inputs and output. The OTA is popular for implementing voltage controlled oscillators (VCO) and filters (VCF) for analog music synthesizers.

2.2 Current Conveyor

2.2.1 History

Sedra and Smith introduced the first generation and second generation current conveyor. The current conveyor was presented in 1968 [19] and further developed a second generation current conveyor in 1970 [20] the third generation current conveyor was proposed in 1995 [21].

2.2.2 First Generation Current Conveyor (CCI)

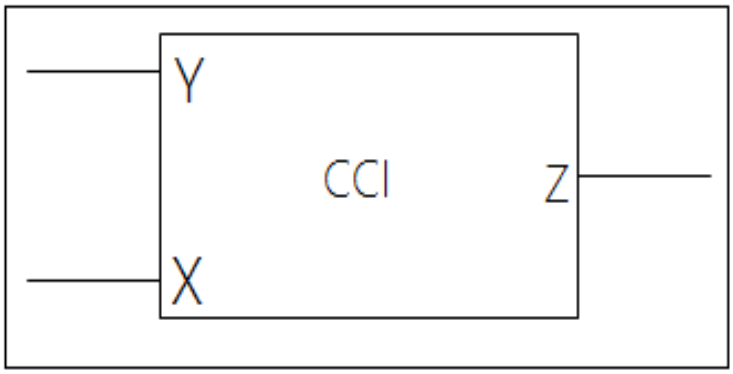

Figure 2.2.1: Block diagram of the first generation current conveyor

Current conveyor which is characterized by a three port network has terminal X, Y, and Z, as shown in figure 2.2.1. The first generation current conveyor CCI has been expressed in a matrix form as follows [23]

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_Y \\ i_X \\ v_Z \end{bmatrix}$$

The first generation current conveyor (CCI) employs both current and voltage in ports X and Y to be equal and a replica of current is conveyed to the output port Z.

2.2.3 Second Generation Current Conveyor (CCII)

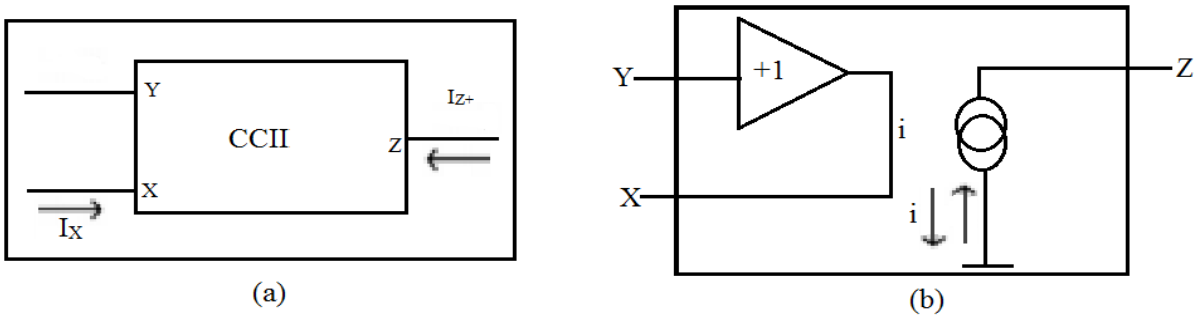

Figure 2.2.2: CCII (a) Block diagram (b) Principle of Operations: $i_{z+} = i_x$ [22]

The principle of operation of CCII+ is shown in figure 2.2.2(b). The + sign indicated its positive gain. The matrix form of CCII is as follows [22]

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_Y \\ i_X \\ v_Z \end{bmatrix}$$

The second generation current conveyor is a voltage follower with input voltage terminal Y and output voltage terminal X, and a current follower with a current input X and a current output Z connected together. The second generation current conveyor as a high input impedance terminal in which no current is flowing in terminal Y, so it used in many applications by increasing the versatility of the current conveyor-I [22]

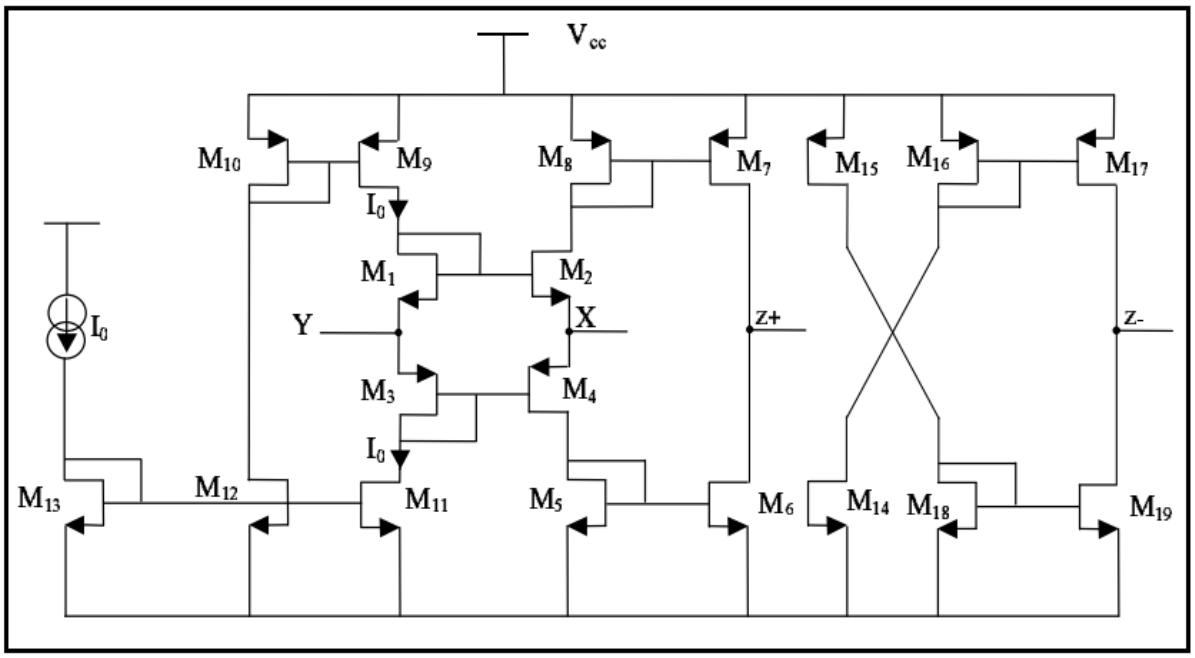

Figure 2.2.3: CCII circuit realization using CMOS [24]

2.2.4 Third Generation Current Conveyor (CCIII)

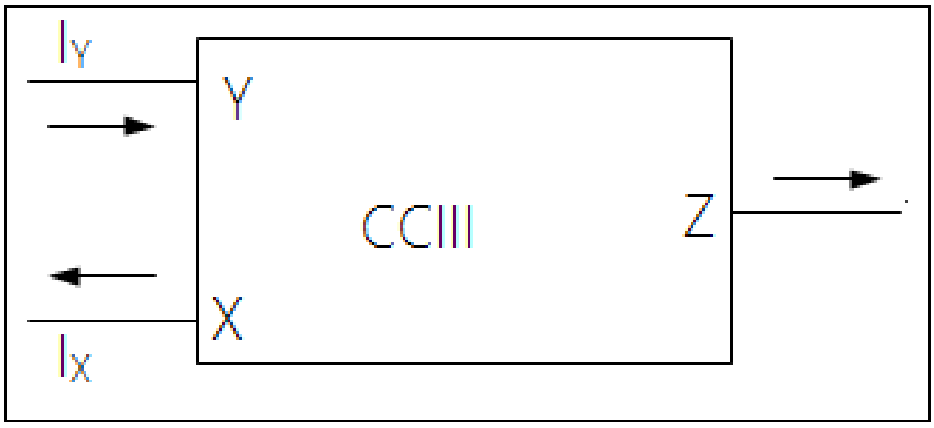

Figure 2.2.4: Block diagram of CCIII

CCIII is similar to CCI except there is opposite current transfer between X and Y terminal. The third generation current conveyor CCIII is formulated in a matrix form as follows [23]

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_Y \\ i_X \\ v_Z \end{bmatrix}$$

The input current flows into the Y-terminal and out from the X-terminal, it is assumed that a differential current input could be realised with this amplifier. However, the CCIII has high input impedance with common mode current signals, i.e. identical current are fed both to terminal Y and terminal X.

Figure 2.2.3 and 2.2.5 show CMOS realisation of CCII and CCIII respectively, using trans linear loop from [26]

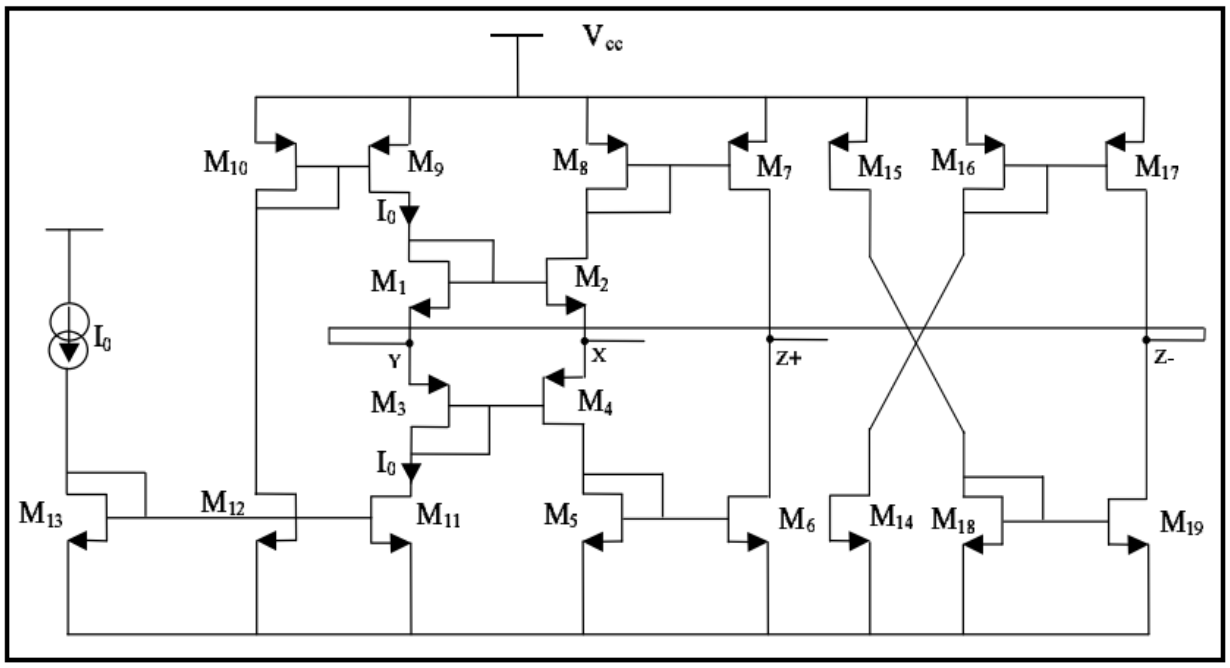

Figure 2.2.5: CCIII circuit diagram using CMOS [26]

2.2.5 Applications

There are several applications of current conveyor since it has greater linearity and wider bandwidth over the voltage mode counterparts, op-amps [29]. Some applications are described in [22], [29], [35]. Despite, there is a lot of research paper published in as filter realizations [37]-[48], oscillatory circuit [36] and in some papers some mathematical operations, like multiplication, divisions are introduced [33], [36].the current conveyor active block derives several bipolar/CMOS implemented circuits e.g., second generation current controlled current conveyor i.e., CCCII [29], dual output current conveyor i.e., DOCCII/DOCCIII [2], differential voltage i.e. DVCCII [29], [31], dual X current conveyor i.e., DXCC in which it has two X terminals, these are non-inverting terminal X_P and inverting terminal X_n [32] reference cited therein.

2.3 Current Feedback Operational Amplifier (CFOA)

2.3.1 History

The CFA was invented by David Nelson at Comlinear Corporation, and first sold in 1982 as a hybrid amplifier, the CLC103. Now recently in few years, there are several CMOS realizations for the CFOA which have been reported in the literature [49]-[55]. From beginning of the implementation of CFOA came out in existence with using only bipolar processes technology. It is well known for the current sensitivity so the techniques are intrinsically well suited to processing signals in the form of current which is given by the high bipolar junction transistor (BJT) trans-conductance.

2.3.2 Symbol and Characteristics equation

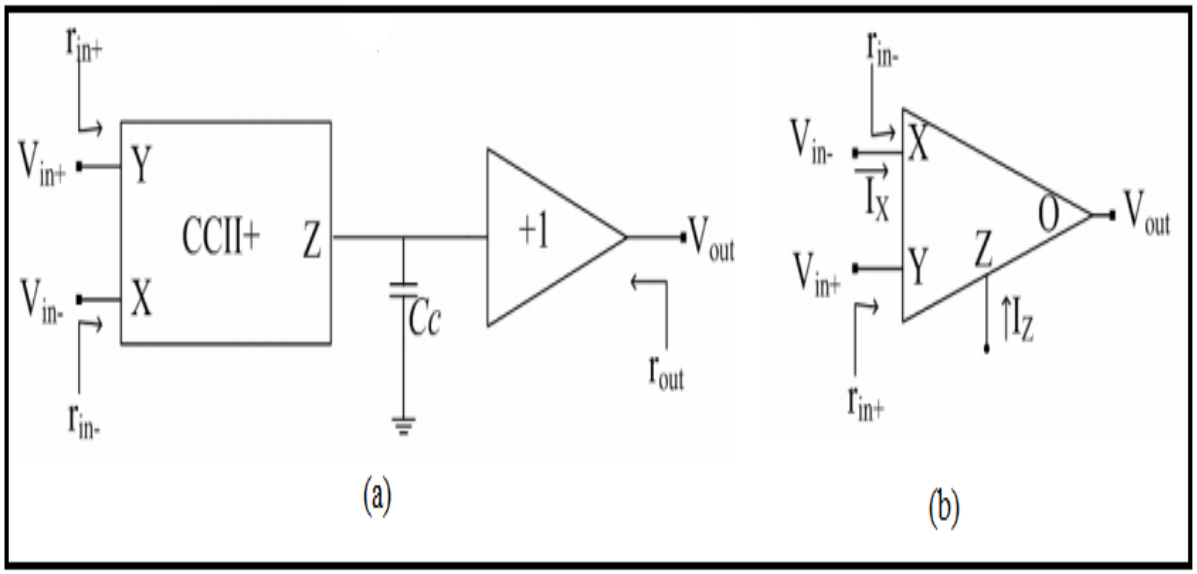

Figure 2.3.1(a) Equivalent Block Diagram of CFOA using current conveyor followed by a buffer. (b) Schematic symbol of CFOA.

The matrix form of expression for CFOA, given as below

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \\ v_w \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} * \begin{bmatrix} v_Y \\ i_X \\ v_Z \\ i_w \end{bmatrix}$$

A current feedback amplifier is equivalent to a plus type second generation current conveyor with a voltage buffer as shown in figure 2.3.1(a) [56]. The term current feedback is used because the signal entering at the feedback node of op-amp is in the form of current signal.

2.3.3 CMOS Implementation of CFOA

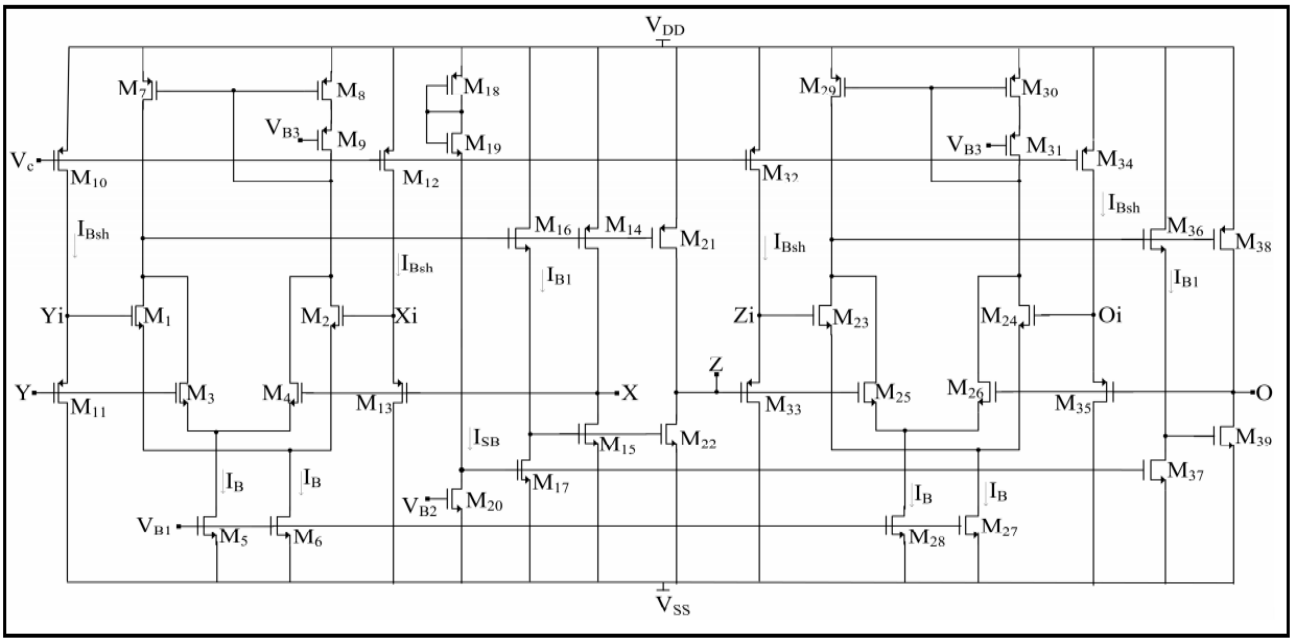

Figure 2.3.2: CMOS implementation of CFOA [56]

In [56], a CMOS low voltage current feedback operational amplifier (CFOA) is introduced. The circuit design is based on the MOS-transistor technology. This circuit allows almost all input and output operation; also, it reduces the offset voltage and provides high driving current capabilities. The CFOA has been always seen as an extension of the CCII, therefore, the design approach was to cascade a CCII+ with a voltage follower to realize the complete circuit [57]. Figure 2.3.2 shows the complete schematic circuit diagram of CFOA, using MOS technology.

2.3.4 Applications

One of the most popular CFOA namely, the AD844 from analog devices, is a 4-terminal building block. There is a growing interest employing CFOAs for the realization active filters, immitance simulators, single frequency as well as single element controlled variable frequency sinusoidal oscillators and single/multiphase oscillators using CFOA pole.

Recently, several current conveyor based and CFOA based [55], [56]-[58] oscillator are proposed in the literature.

2.4 Current Differencing Buffered Amplifier (CDBA)

2.4.1 History

The current differencing buffered amplifier is primarily introduced by Acar and Ozoguz [62]. It is a recently introduce active circuit that is a mixture of two fundamental building blocks i.e., current differencing block and voltage follower block.

2.4.2 Symbol and Characteristics Equation

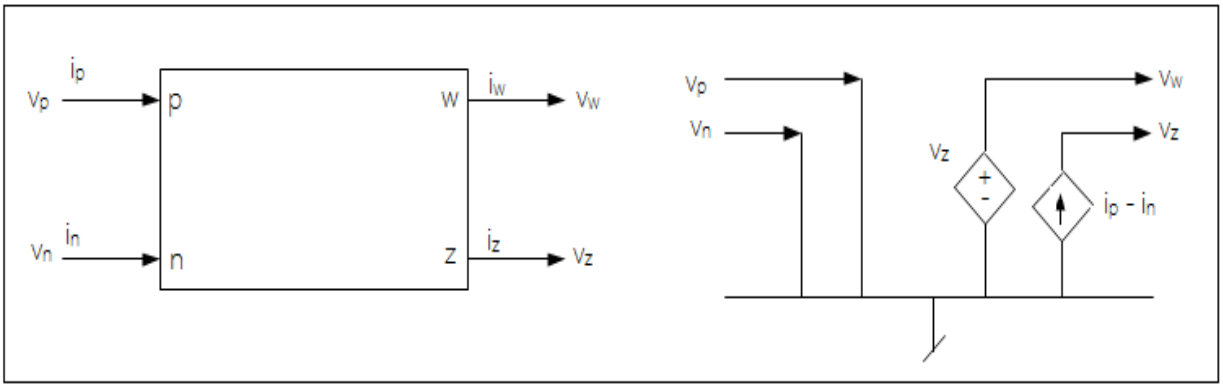

Figure 2.4.1: (a) CDBA Block Diagram **(b)** CDBA equivalent circuit[62]

It is a four terminal device; input terminals are allocated with p and n-terminal, and output terminals are allocated with w and z-terminal. The p-terminal displays, its non-inverting terminal and the n-terminal displays, its inverting terminal. The block diagram of CDBA is shown in figure 2.4.1 (a). CDBA equivalent circuit is shown in figure 2.4.1 (b). It explains the conversation of the difference of input currents to the output voltage.

It can operate in both current mode as well as voltage mode, which offer flexibility and enable to have variety of circuit design. Moreover, it is free from parasitic capacitances and appropriate for high frequency operation.

The characteristics equation of circuit describes as under in matrix form,

$$\begin{bmatrix} i_Z \\ v_W \\ i_P \\ v_n \end{bmatrix} = \begin{bmatrix} 0 & 0 & \alpha p & \alpha n \\ \beta & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} * \begin{bmatrix} v_Z \\ i_W \\ v_P \\ i_n \end{bmatrix}$$

Where current gains given by αp and αn and voltage gain β are ideally equal to one. Here, p and n terminals are internally grounded.

2.4.3 CMOS Implementation

In [63], Keskin and Hancioglu presented a current mode multifunction using two CDBAs. In this paper they realized CDBA with the help of CMOS bipolar technology.

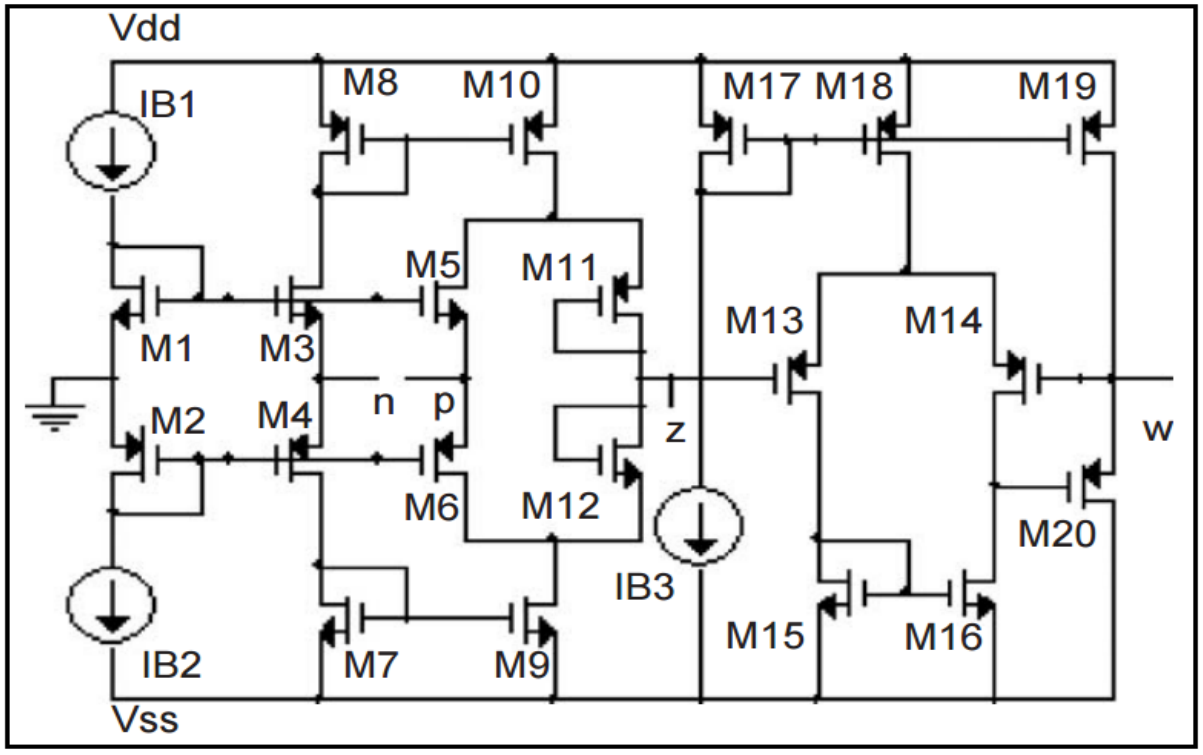

Figure 2.4.2: CDBA CMOS Realization [63]

The CDBA used in this design is realized with CMOS technology using the topology illustrated in figure 2.4.2 with supply voltages of V_{DD} = 2.5V and V_{ss} = -2.5V and biasing currents of $I_{B1} = I_{B2} = I_{B3}$ = 30μA. Figure 2.4.2 shows the complete schematic of suggested CDBA, which is based on the use of current differencing circuit (M1-M12) and the voltage

buffer circuit (M13- M20). The circuit simulation is done using 0.5µm MIETEC level – 3 real transistor model parameters for all transistors in the circuit

2.5 Voltage differencing trans-conductance Amplifier (VDTA)

2.5.1 Symbol and Characteristics Equation

The differential input OTA is a simple element for realising the voltage difference. The VDTA element with its schematic symbol in figure 2.5.1 has a high input impedance at terminal P and N, and an auxiliary terminal is Z. it has also its multiple copies of current Izc in order to increase the universality of VDTA element that's represent a new terminal Zc (Z Copy)[65]. An ideal VDTA has high impedance at its input terminal and also at high impedance at output terminal.

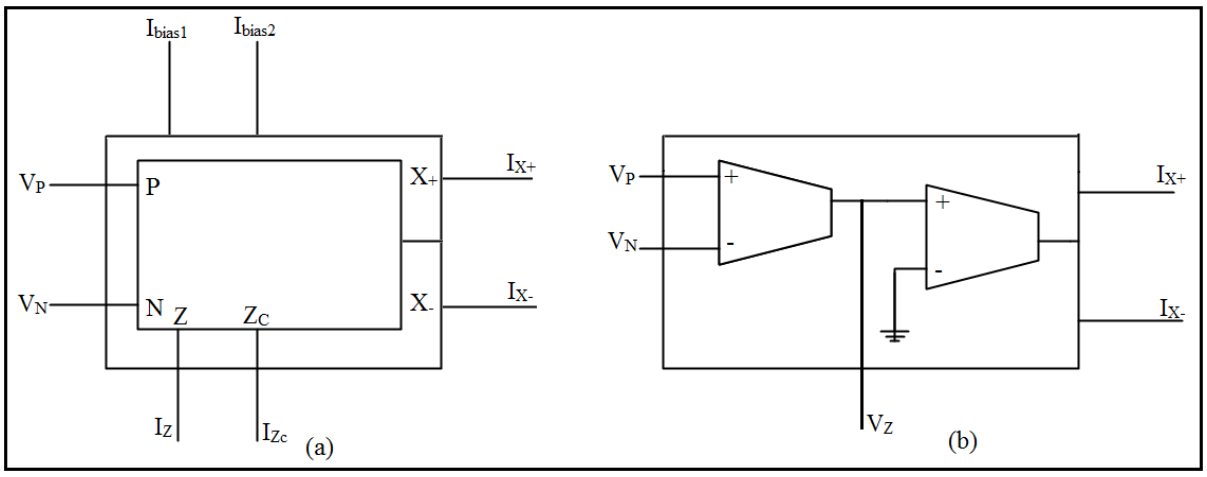

Figure 2.5.1: (a) VDTA block diagram[64] (b) OTA based VDTA

The relationship of input output terminals of VDTA can be described by the following matrix equation

$$\begin{bmatrix} I_Z \\ I_Z^+ \\ I_Z^- \end{bmatrix} = \begin{bmatrix} g_{m1} & -g_{m2} & 0 \\ 0 & 0 & g_{m1} \\ 0 & 0 & -g_{m2} \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \end{bmatrix}$$

Where g_{m1} and g_{m2} are the trans-conductance parameters of first and second stage of VDTA whose value is controlled by the biasing current I_{bias} of VDTA.

2.5.2 CMOS Implementation

In [65], Abdullah Yesil , Fırat Kacar, Hakan KUNTMAN presented a RF filter based on VDTA. In this paper they realized VDTA with the help of CMOS bipolar technology.

The VDTA used in this design is realized with CMOS technology using the topology illustrated in figure 2.5.2 with supply voltages of V_{DD} = 0.9V and V_{ss} = -0.9V and biasing currents of $I_{B1} = I_{B2} = I_{B3} = I_{B4}$ = 150µA. Figure 2.5.2 shows the complete schematic of suggested VDTA, which is based on the use of voltage differencing circuit. The circuit simulation is done using 0.18µm MIETEC level – 3 real transistor model parameters for all transistors in the circuit

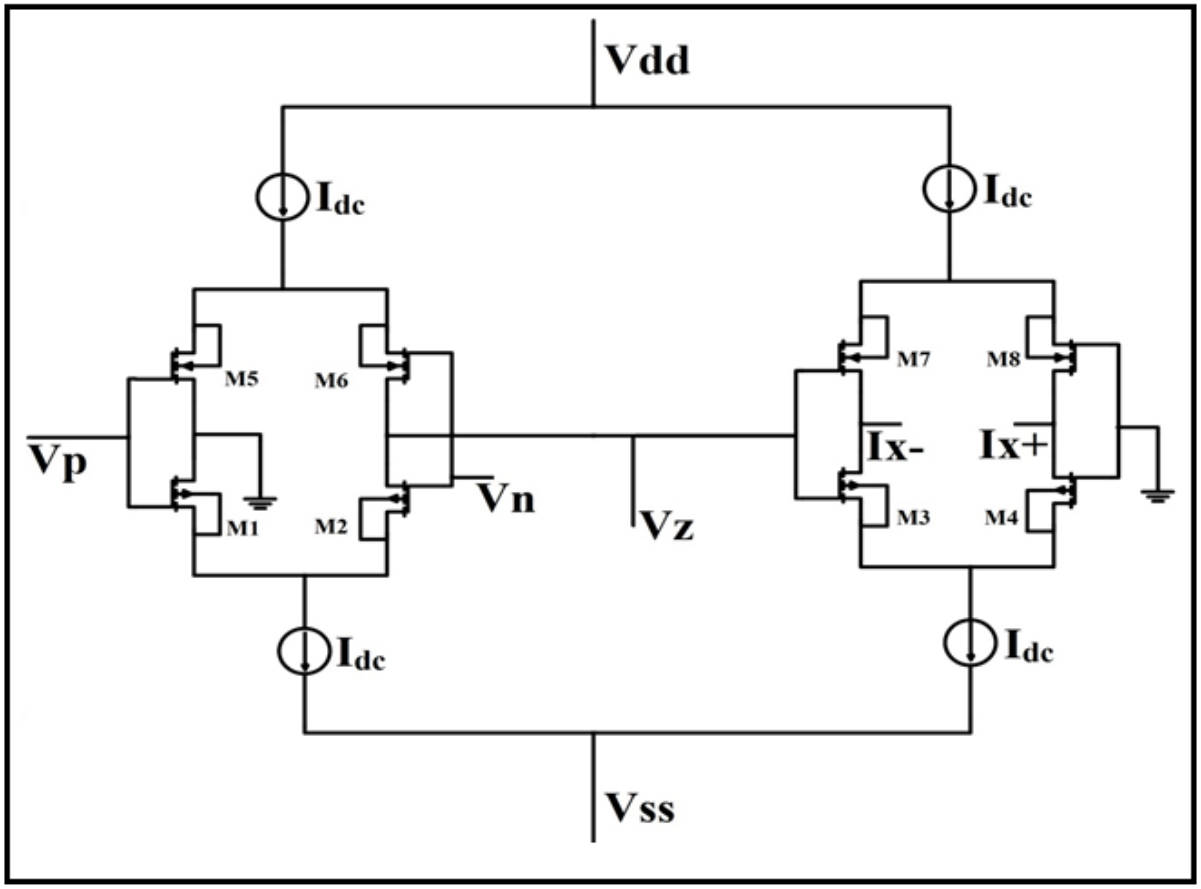

Figure 2.5.2: CMOS realization of VDTA [65].

2.6 Conclusion

In this chapter, history, characteristics, applications and CMOS implementation of the active blocks used for implementation of PID controllers are briefly discussed. The devices described are

(I) OTA-C
(II) Current Conveyor
(III) CFOA
(IV) CDBA
(V) VDTA

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CHAPTER III

DESIGN AND IMPLEMENTATION OF PID CONTROLLER USING DIFFERENT ACTIVE BLOCKS

3.0 Introduction

In the present chapter, we present a review of the design of single ended PID controllers using current mode/voltage mode active building blocks. These controllers have been designed, based on the signal flow graph of a PID controller given in [2] – [5]. The current mode/voltage mode active building blocks used are OTA, CFOA, CDBA. The terminal equations characterizing these blocks have been used for designing PID controller. Detailed simulation result for OTA and CFOA - based PID controllers are also presented.

3.1 Traditional PID controller design based on operational – amplifier

Before we present the detailed design and simulation results of the PID controllers based on other devices it is worthwhile to have a look at the traditional op-amp based PID controller which is presented in fig. 3.1.1 [1].

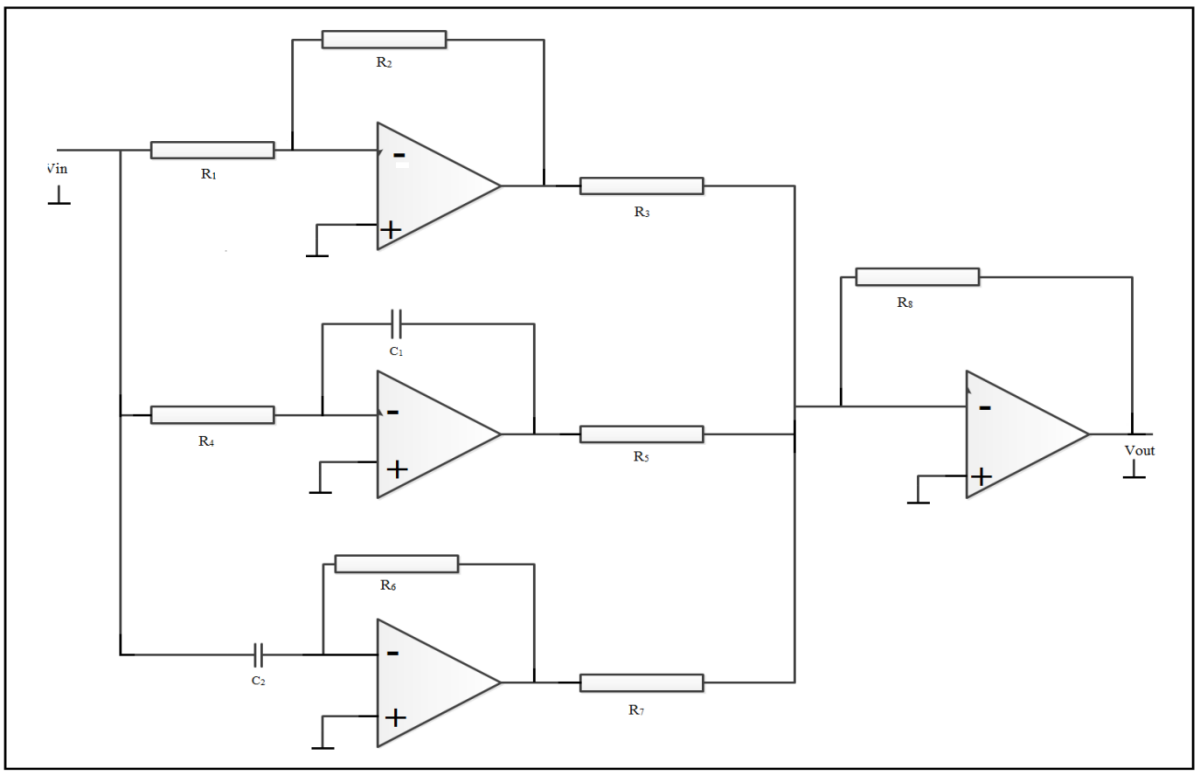

Figure 3.1.1: PID controller using op-amps [1]

In this figure, P, I, D and summer operations are recognized by I, II, III and IV respectively. It can be seen that the circuit employs four op-amps and ten floating passive elements.

The transfer function of a PID controller can be written as follows (given in [1])

$$\frac{V_o(s)}{V_I(s)} = K_P + sK_D + \frac{K_I}{s} = \frac{K_D s^2 + K_P s + K_I}{s}$$

Here,

Proportional constant,

$$K_P = \frac{R_1 R_8}{R_1 R_3}$$

Integral constant,

$$K_I = \frac{R_8}{C_1 R_4 R_5}$$

Derivative constant,

$$K_D = \frac{R_6 C_2 R_8}{R_7}$$

The signal flow graph represented of above equation is given in figure 3.1.2 which is consisting of the sub-graph for proportional, integral and derivative parts of the controllers.

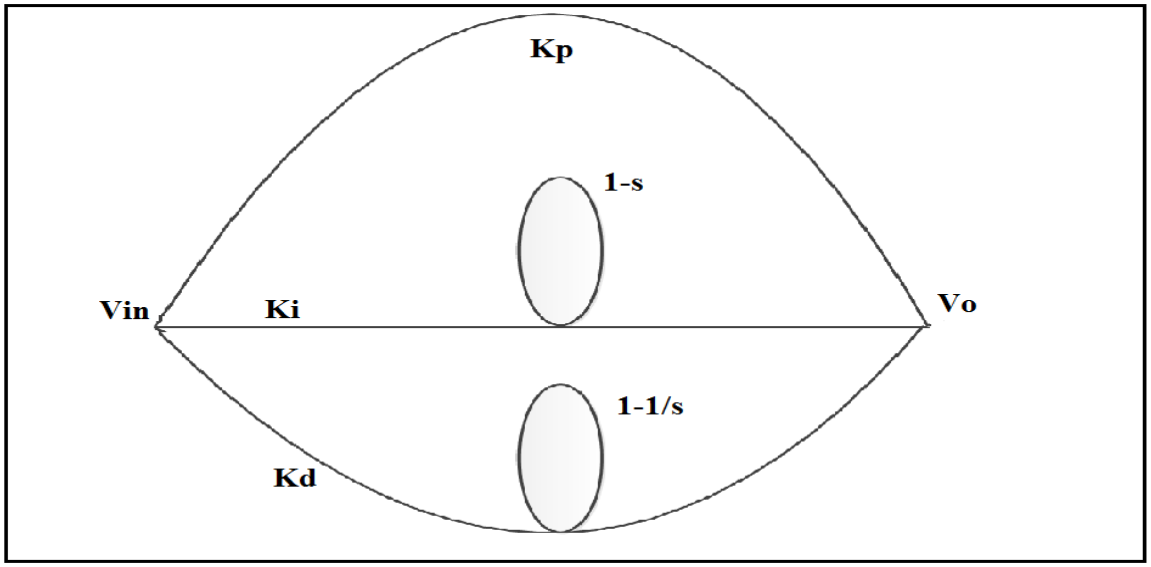

Figure 3.1.2: Signal flow graph corresponding to the transfer function of the proportional-integral-derivative controller

3.2 OTA-C based PID controller

Based on the signal flow graph shown in figure 3.1.2, the sub graphs and their corresponding blocks, using OTA-Cs are shown in following figure 3.2.1 [2]. The circuit details of OTA-C are discussed in chapter 2. With the help of characteristics of the OTA-C circuit (defined in chapter 2), a voltage mode integrator is shown in figure 3.2.1(a) and a voltage mode differentiator containing an inductor is shown in figure 3.2.1(b), which is used for the realization of differentiator circuit as given in figure 3.2.1(c). a summer circuit can be presented as shown in figure 3.2.1(d) [2].

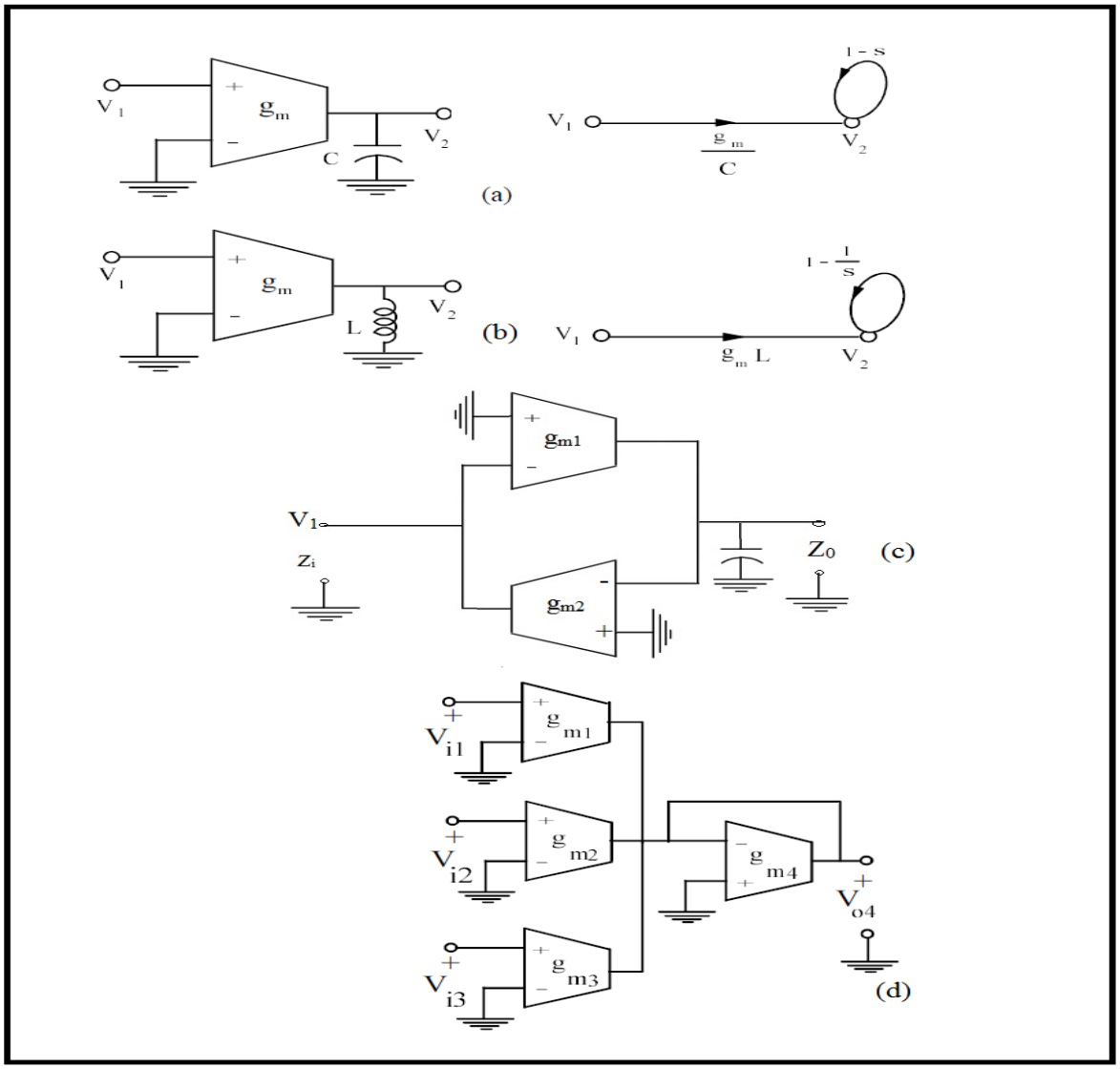

Figure 3.2.1 Basic building blocks using OTAs and grounded capacitors together with corresponding signal flow graphs (a) Integrator circuit (b) Derivative circuit (c) Inductance simulation (d) Summing circuit

In figure 3.2.1(c), OTA-C based gyrator circuit gives input impedance

$$Z_i = {}^{1}/_{g_{m1}g_{m2}Z_o} = {}^{sC}/_{g_{m1}g_{m2}}$$

From above equation, it can be observed that $Z_i$is proportional to s, so this circuit behaves as an inductor. This inductance and the OTA build a derivative circuit. The capacitor C, together with the OTA (see figure 3.2.1(a)) forms the integration circuit. The OTAs, shown in the above figure 3.2.1(d), form the weighted summing circuit.

Connecting all these sub circuits as shown in above figure 3.2.1, into a single block as shown in figure 3.2.2, performs the operation of a PID controller.

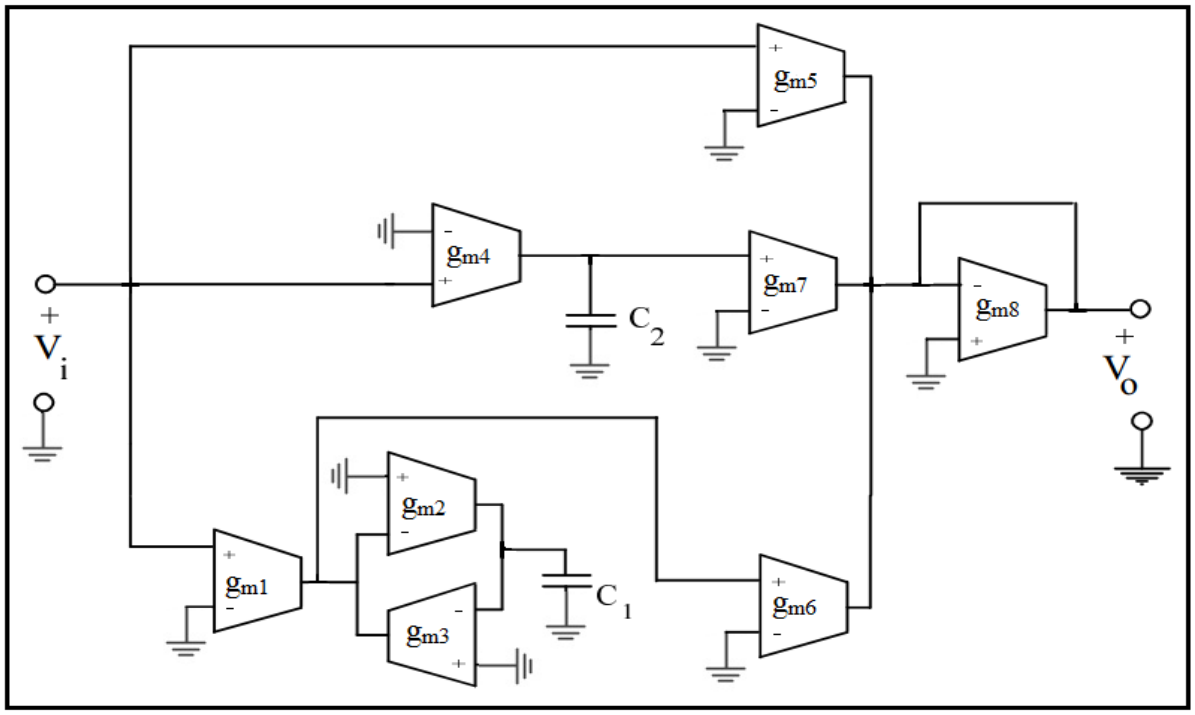

Figure 3.2.2: An OTA-C based PID controller [2]

In the figure 3.2.2, the derivative circuit is configured by simulation of gyrator which is introduced by connecting two OTAs g_{m2} and g_{m3}, together with the capacitor C1 shown in figure 3.2.2. the capacitor C_2 and OTA g_{m4} form the integrator circuit. The OTAs g_{m5}, g_{m6}, g_{m7} and g_{m8} form the weighted summing circuit. OTAs g_{m5} and g_{m8} form the proportional gain.

$$K_P = {}^{g_{m5}}/_{g_{m8}}$$

$$K_I = \frac{g_{m4}g_{m7}}{C_2 g_{m8}}$$

$$K_D = \frac{g_{m1}C_1 g_{m6}}{g_{m2}g_{m3}g_{m8}}$$

The controller gain can be assigned to the prescribed values by adjusting OTAs' trans-conductance, g_{mi} ; I = (1-8), by DC control voltages.

3.3 CFOA based PID controller

The sub graphs and their corresponding block using active building blocks of CFOAs, are shown in figure 3.3.1 [3]. The circuit configuration of CFOA is discussed in chapter 2. In figure 3.3.1(a), block and signal flow graph of an amplifier circuit is shown figure 3.3.1(b) and 3.3.1(c) represent the signal flow graph and block of an integration circuit and of a derivative circuit, respectively. Figure 3.3.1(d) block with corresponding signal flow graph of a summing circuit.

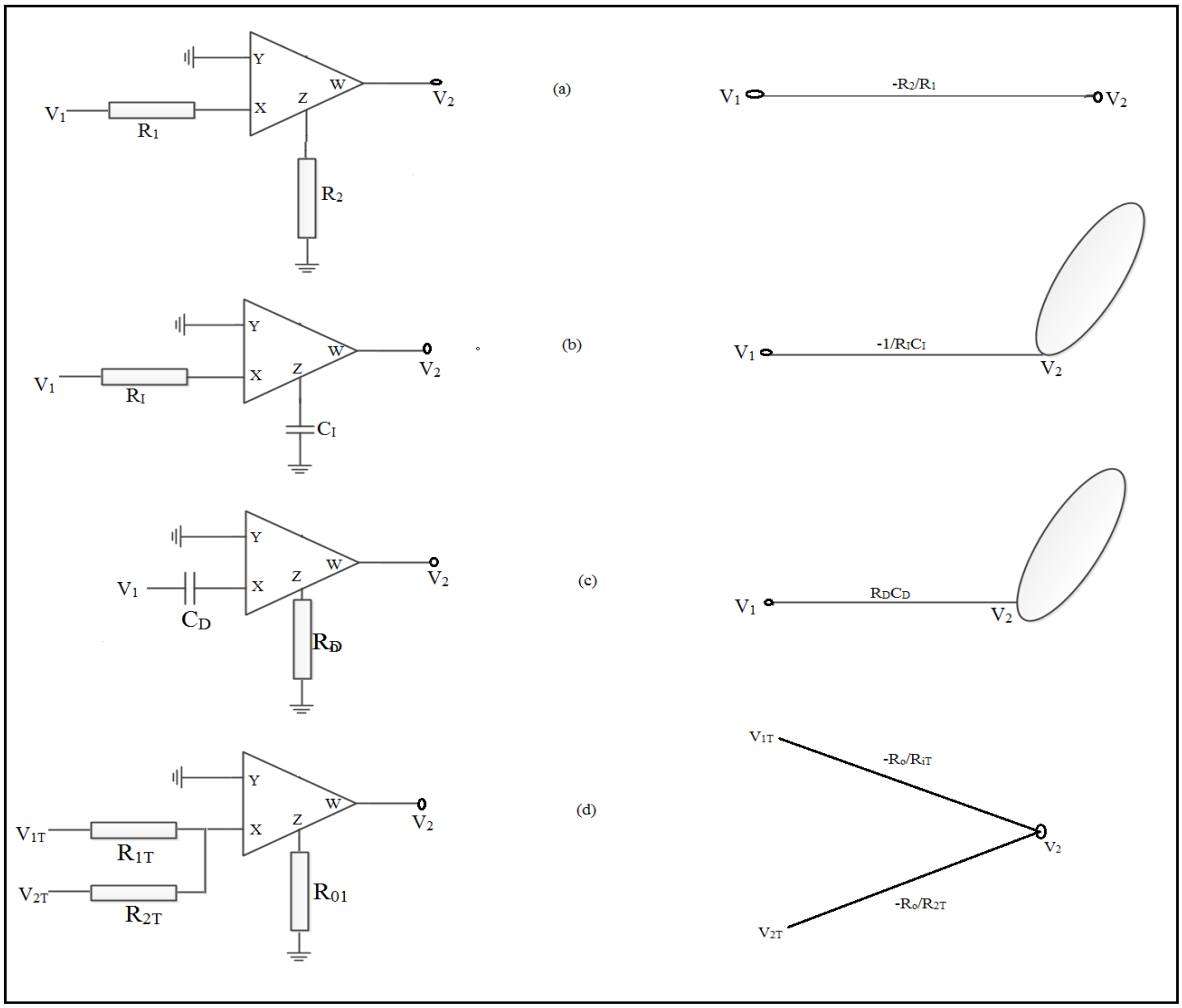

Figure 3.3.1: Basic building blocks using CFOAs (a) Amplifier, (b) integrator, (c) derivative circuit, (d) summer circuit.[3]

Figure 3.3.1(a) gives a value of $\frac{R_2}{R_1}$ for the proportional gain, figure 3.3.1(b) & (c) give the value of $\frac{1}{R_2C_1}$ for the time constant in the integrator circuit and of R_DC_D for the derivative time constant, respectively. Connecting all these blocks as shown in figure 3.3.1, in such a way they can perform the operation of a PID controller as shown in figure 3.3.2.

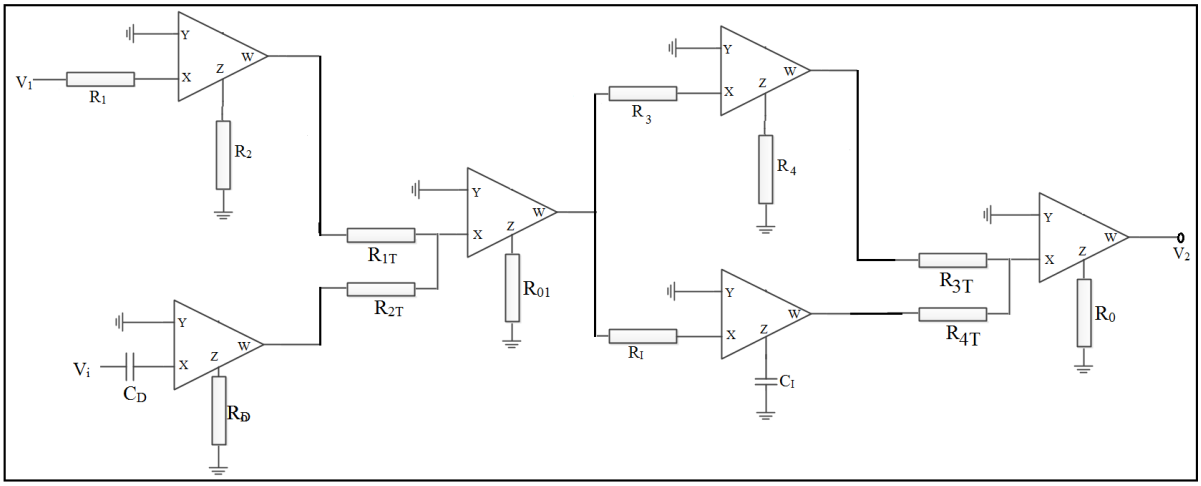

Figure 3.3.2: A CFOA based PID controller [3]

Considering all ideal cases to adjust all gains as unity, the controller coefficients are given below

$$K_p = \frac{R_2R_4}{R_1R_3} + \frac{R_DC_D}{R_IC_1}$$

$$K_I = \frac{R_2}{R_1C_1R_I}$$

$$K_D = \frac{R_DC_DR_4}{R_3}$$

3.4 CDBA based PID Controller

On the basis of a signal flow graph as shown in figure 3.1.2, the sub graph and their corresponding blocks using CDBAs are shown in figure 3.4.1 [4]. The circuit's details of CBDAs are discussed in chapter 2.

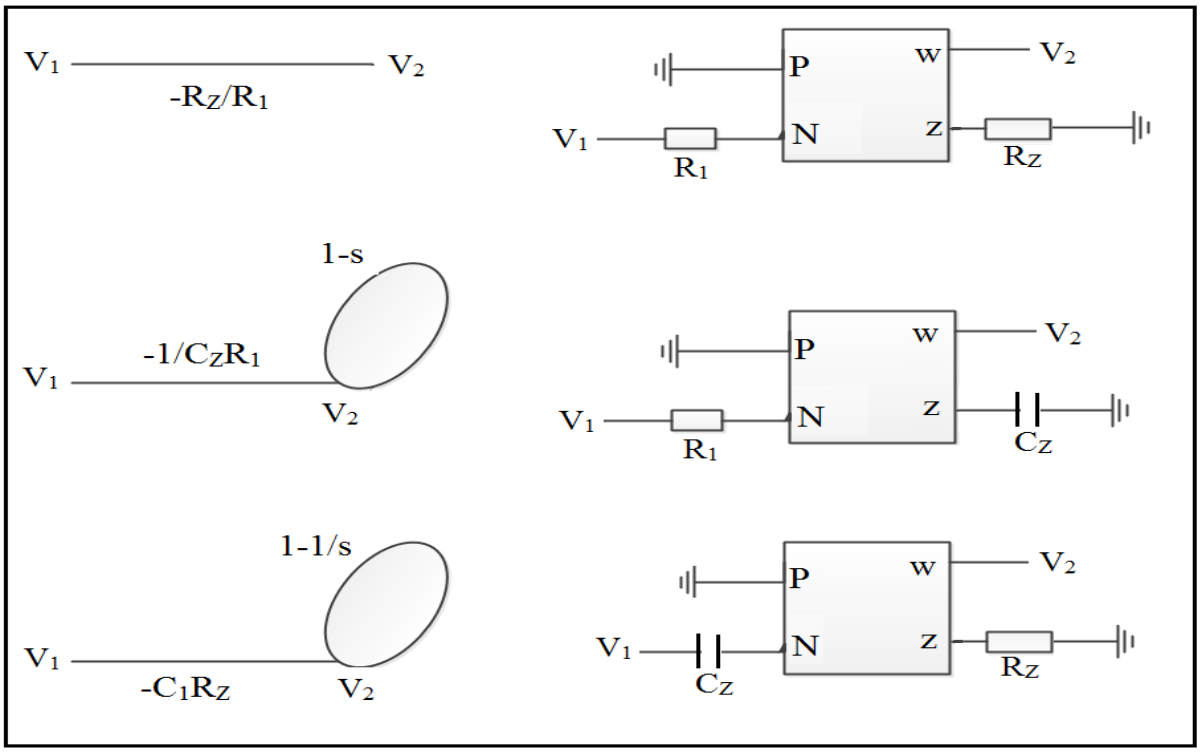

Figure 3.4.1: Sub-graphs for the PID controller and their corresponding CDBA based sub-circuits.

Connecting all these blocks as shown in figure 3.4.1, into a single block as shown in figure 3.4.2, they perform the operation of a PID controller.

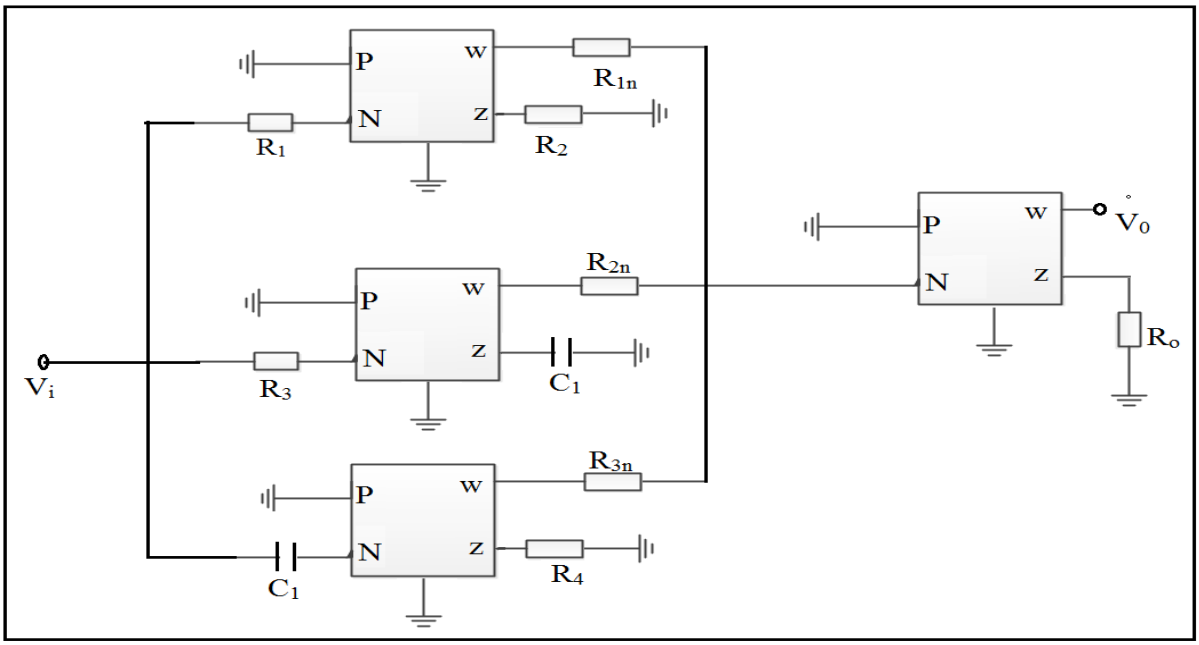

Figure 3.4.2: CDBA based PID controller [4].

Taking all ideal values, the coefficients of PID controller are given below [4]

$$K_P = \frac{R_O R_2}{R_1 R_{1n}}$$

$$K_I = \frac{R_0}{R_3 C_1 R_{2n}}$$

$$K_D = \frac{R_0 C_2 R_4}{R_{3n}}$$

3.5 Simulation

3.5.1 Implementation of OTA-C based PID controller

The voltage mode PID controller as shown in figure 3.2.2, was used to implement a closed loop system by cascaded it with the following second order system and its open loop (without controller) and closed loop time (without/with controller) response was simulated in PSPICE. The details of the simulation results are presented below.

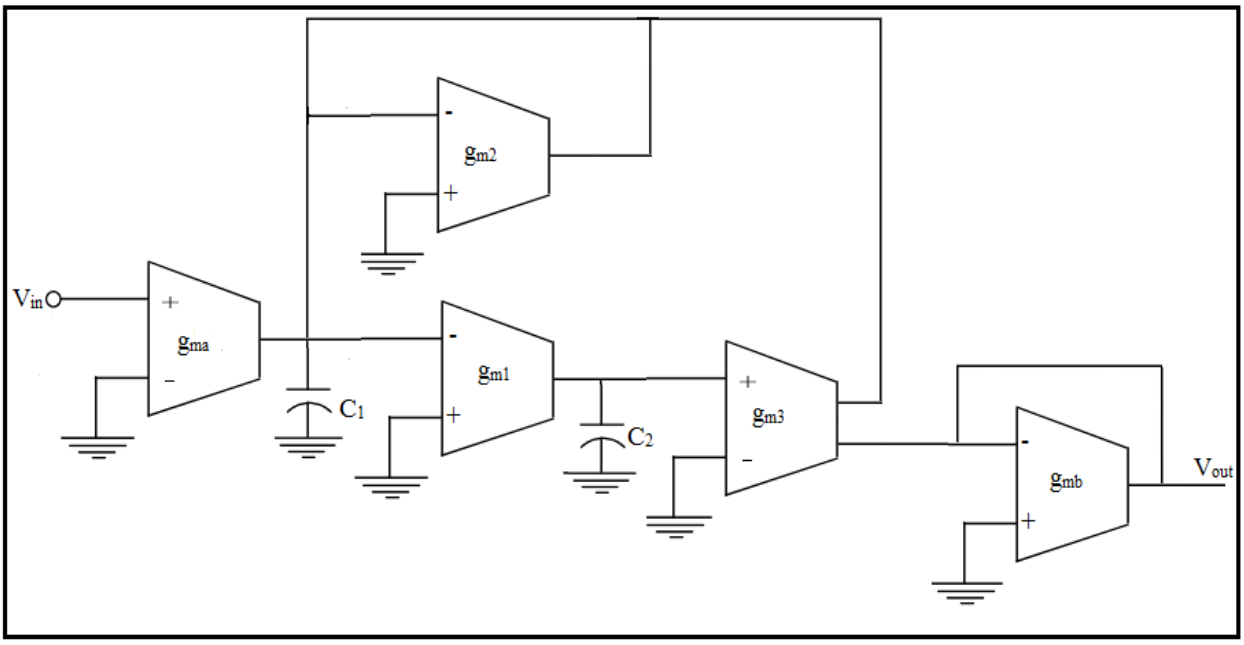

Figure 3.5.1-1: OTA –C based voltage mode second order system [6]

The second order system [6] shown in figure 3.5.1-1 gives the following transfer function

$$\frac{V_{out}(s)}{V_{in(s)}} = \frac{{}^{g_{m1}g_{m2}}/_{C_1C_2}}{s^2 + {}^{sg_{m2}}/_{C_1} + {}^{g_{m1}g_{m3}}/_{C_1C_2}}$$

Taking values of $g_{m1} = g_{m3} = g_{m4} = g_{m5} = g_{m6}$ = 165$\mu A/V$ and g_{m2} = 58.345$\mu A/V$, so that it gives damping ratio ζ=*0.177* and cut off frequency f_c=*8.758 KHz.* Simulation of this system gives open loop gain=0.958

Step response of this system without applying any controller in open loop structure is shown in figure 3.5.1-2. Step response of the uncompensated closed loop system i.e., negative feedback without any controller is shown in figure 3.5.1-3. Here the gain decreases by a factor of 0.477 from open loop gain.

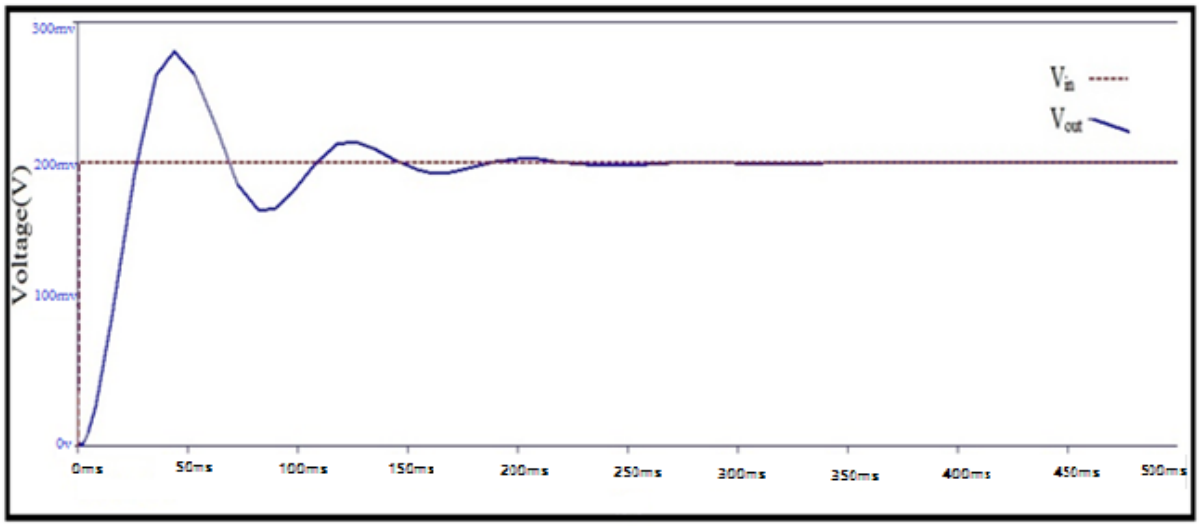

Figure 3.5.1-2: Step response of uncompensated open loop system

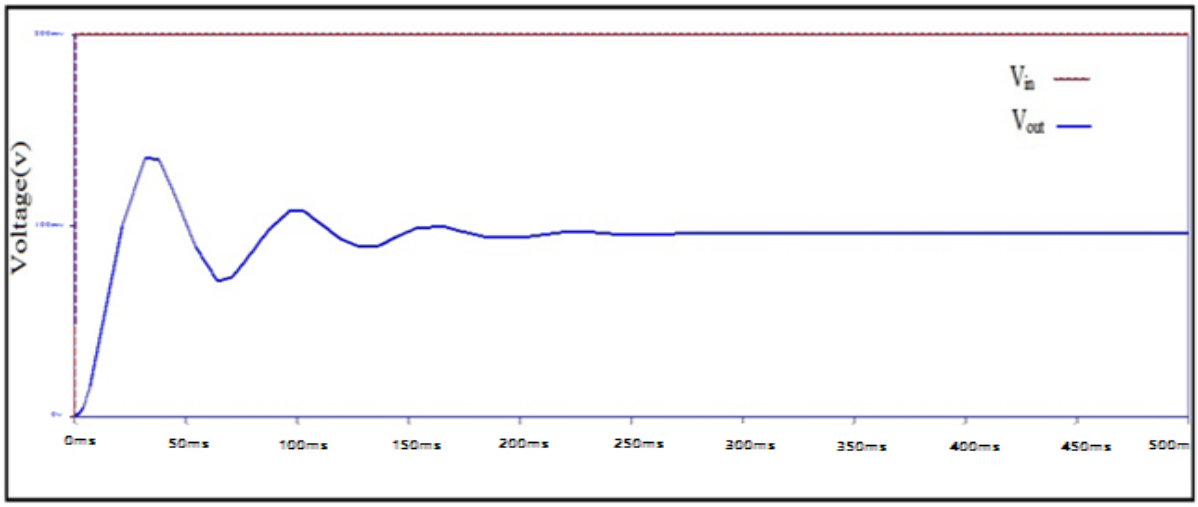

Figure 3.5.1-3: Step response of uncompensated closed loop system

Now the implementation of PID controller is done, for (a) $K_P = 1,\ K_I = 1.625 * 10^4, K_D = 0.595$ as shown in figure 3.5.1-4 and (b) $K_P = 10,\ K_I = 1.625 * 10^5, K_D = 5.95$ as shown in figure 3.5.1-5.

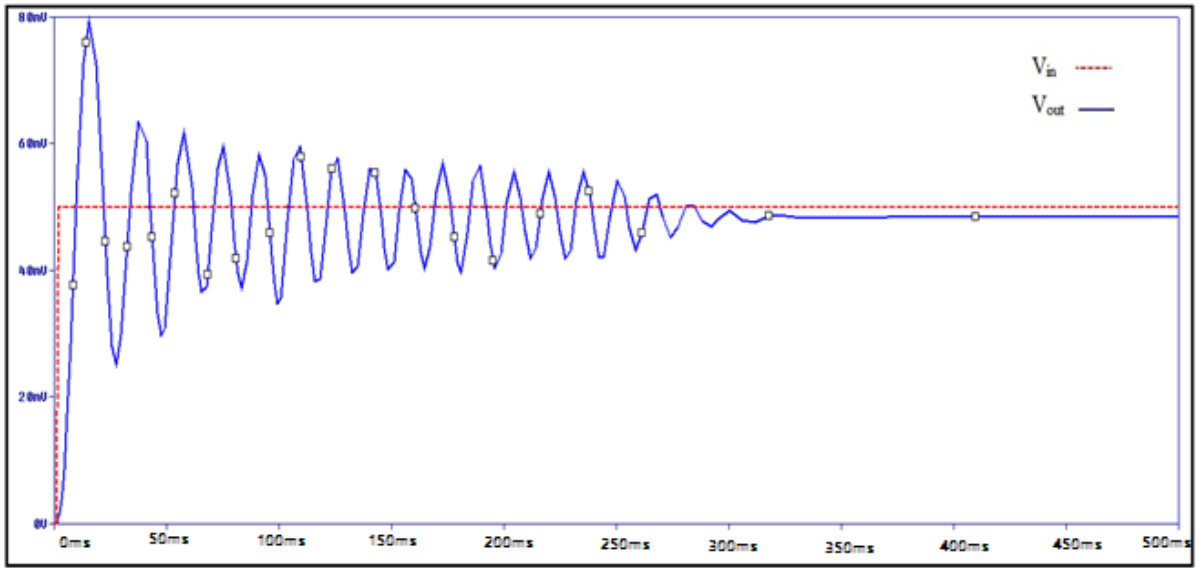

Figure 3.5.1-4: Step response of second order system with PID controller for K_P =1, K_I = $1.625 * 10^4$, K_D = 0.595

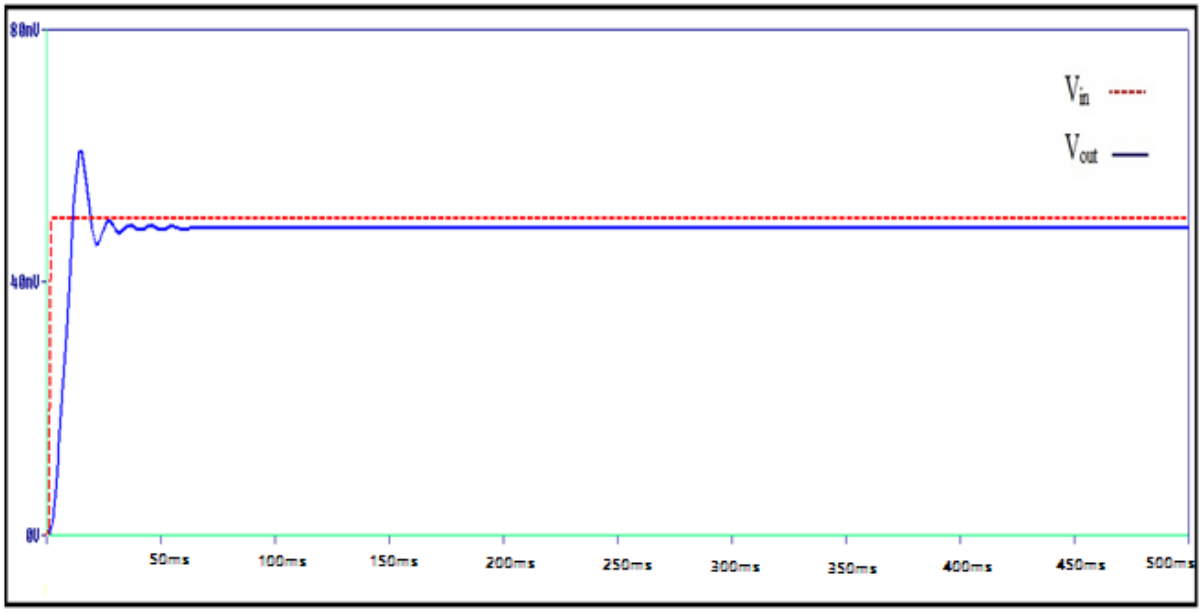

Figure 3.5.1-5: Step response of second order system with PID controller for $K_P = 10,\ K_I = 1.625 * 10^5, K_D = 5.95$

Table 3.0: Observation from the step response of the system operating in voltage mode

S.No.	Various System Configuration	Rise Time t_r (ns)	Overshoot (%)	Settling Time(t_s)	Steady State error(e_{ss})
1.	*Open loop system*	43	99	220ms	1mv
2.	*Closed loop system without PID controller*	30	74.7	270ms	29mv
3.	*Closed loop system with PID controller* $K_P = 0.1, K_I = 1.625 * 10^4, K_D = 0.595$	26	16.73	320ms	4.253mv
	$K_P = 10, K_I = 1.625 * 10^5, K_D = 5.95$	19	31	70ms	.147mv

3.5.2 Implementation of CFOA based PID controller

The PID controller as shown in figure 3.5.1, was used to implement a closed loop system by cascaded it with the following second order system and its open loop (without controller) and closed loop time (without/with controller) response was simulated in PSPICE. The details of the simulation results are presented below.

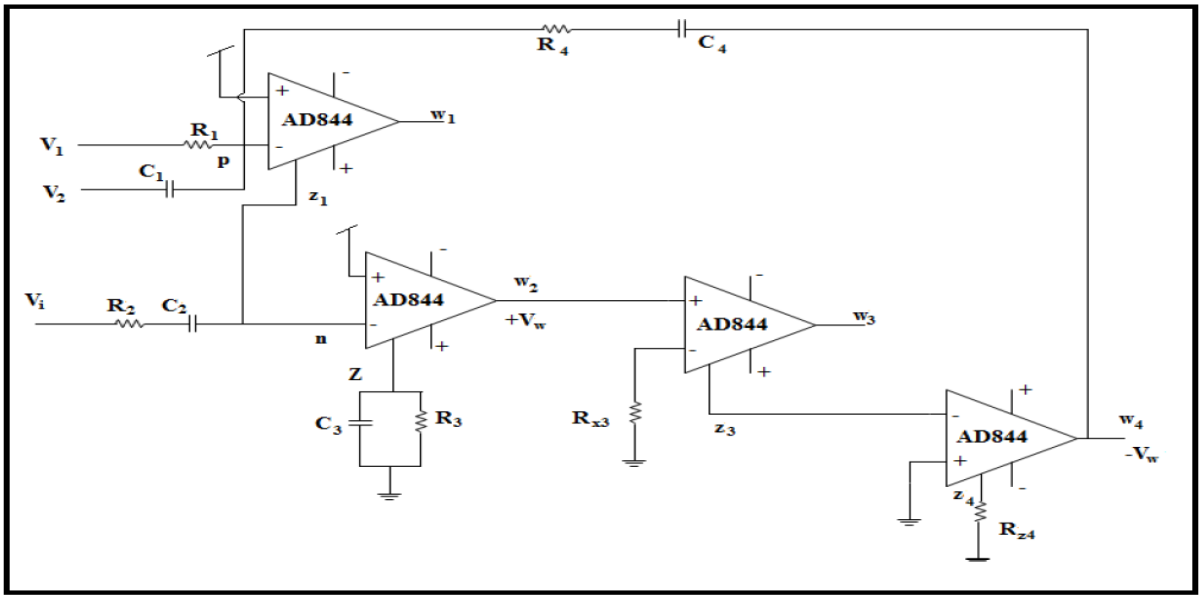

Figure 3.5.2-1 Bi-Quad Filter realization using CFOA [8]

The second order system shown in figure 3.5.2-1 gives the following transfer function

$$V_0 = \frac{s^2 V_2 R_1 C_1 R_2 C_2 + (R_2 C_2 V_1 + V_2 C_1 R_1 - V_i C_2 R_1)s + V_1}{s^2 R_3 C_3 R_4 C_4 + (R_3 C_3 + R_4 C_4 - R_3 C_3)s + 1}$$

The second order system used for PID controller is considered when $V_2 = 0$, $V_1 = V_{in}$, $R_1 = R_2$, $R_2 C_2 = R_4 C_4$, $C_1 = 0$, the transfer function related to system is

$$\frac{V_0}{V_I} = \frac{-R_3}{R_1} * \frac{1}{s^2 R_3 C_3 R_4 C_4 + (R_3 C_3 + R_4 C_4 - R_3 C_3)s + 1}$$

The bias supply voltages were taken as ±5V. The passive component values are Rw_1=10KΩ, R_{x3} =10KΩ, R_{w3} =10KΩ, R_{z4} =10KΩ, R_{w4} =10KΩ, R_1 =20KΩ, R_2 =20KΩ, R_3 =20KΩ, R_4=20KΩ, C_2 =C_4 =10nF and C_3 =20Nf and cut off frequency f_c= 562.34 Hz.

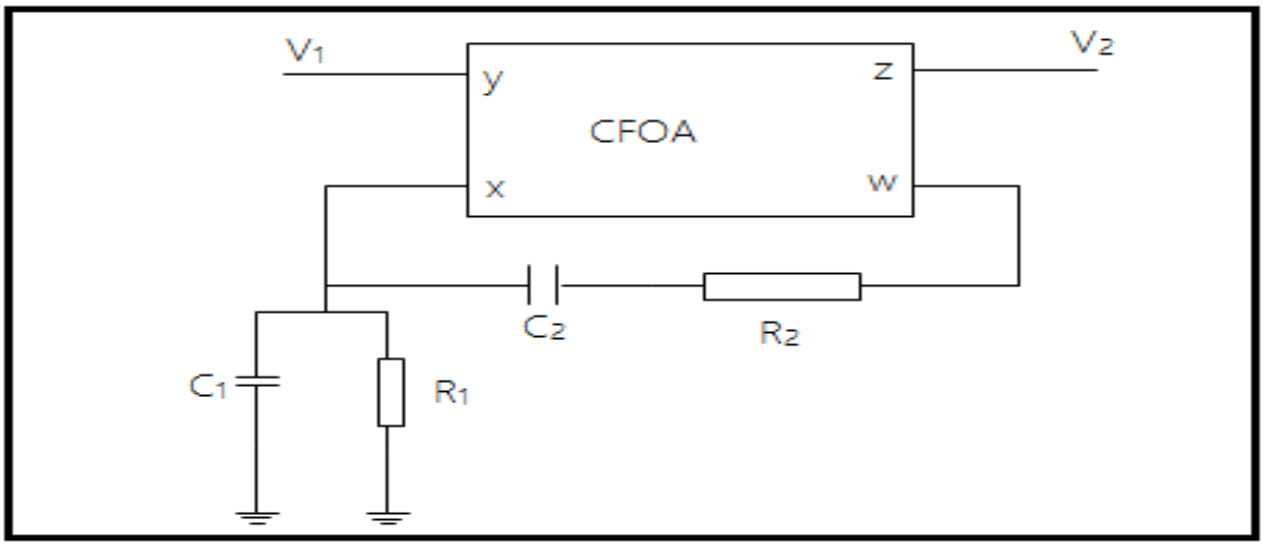

Figure 3.5.2-2: CFOA based PID controller [9]

On simulating with parameters R_1 = 1k, R_2 = 1k, C_1 = C_2 = 10nf, PID controller output shown in figure 3.5.2.3.

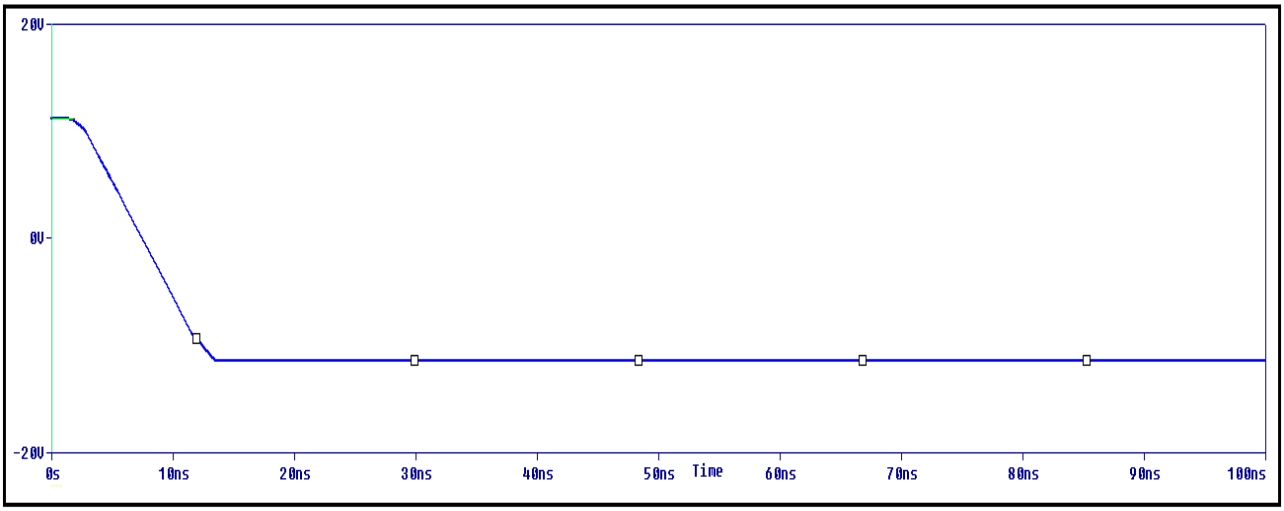

Figure 3.5.2-3 output voltage along with the applied input voltage (t_r=40ns)

3.6 Conclusion

In this chapter, a brief discussion on the synthesis methods for analog PID controller using different active blocks are described, with the help of signal flow graph techniques and their corresponding blocks. Design of OTA based, CFOA based, CCCII based, CDBA based, PID controller has been presented. The detailed simulation results on the time response studies on a OTA- based voltage mode PID controller and CFOA based PID controller has been presented.

3.7 References

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CHAPTER IV

CURRENT MODE PID CONTROLLER REALISATION USING VDTA

4.1 Introduction

The conventional PID controller has a very simple structure (which is its main advantage) and is used in a variety of process control system for control of various process parameters [1]. The conventional PID controllers have been realized with traditional voltage mode operational amplifiers and thus suffer from many drawbacks viz. low speed, low bandwidth, low dynamic range, as well as gain bandwidth conflict. Current mode active devices are getting wide attention due to their wider bandwidth, lower voltage operation and better linearity and stability properties in comparison to voltage mode devices. Many of these devices such as current conveyors [2], operational trans-conductance amplifier [3], current feedback operational amplifiers [4] and current differencing buffer amplifier [5] have been used to realize PID controllers. In the following we present a voltage controller current source PID controller using Voltage Differencing Trans-conductance Amplifier (VDTA).

4.2 Symbol and Characteristics Equation

The differential input OTA is a simple element for realising the voltage difference. The VDTA element with its schematic symbol in figure 4.2.1 has a high input impedance at terminal P and N, and an auxiliary terminal is Z. it has also its multiple copies of current Izc in order to increase the universality of VDTA element that's represent a new terminal Zc (Z Copy). An ideal VDTA has high impedance at its input terminal and also at high impedance at output terminal.

The relationship of input output terminals of VDTA can be described by the following matrix equation

$$\begin{bmatrix} I_Z \\ I_Z^+ \\ I_Z^- \end{bmatrix} = \begin{bmatrix} g_{m1} & -g_{m2} & 0 \\ 0 & 0 & g_{m1} \\ 0 & 0 & -g_{m2} \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \end{bmatrix}$$

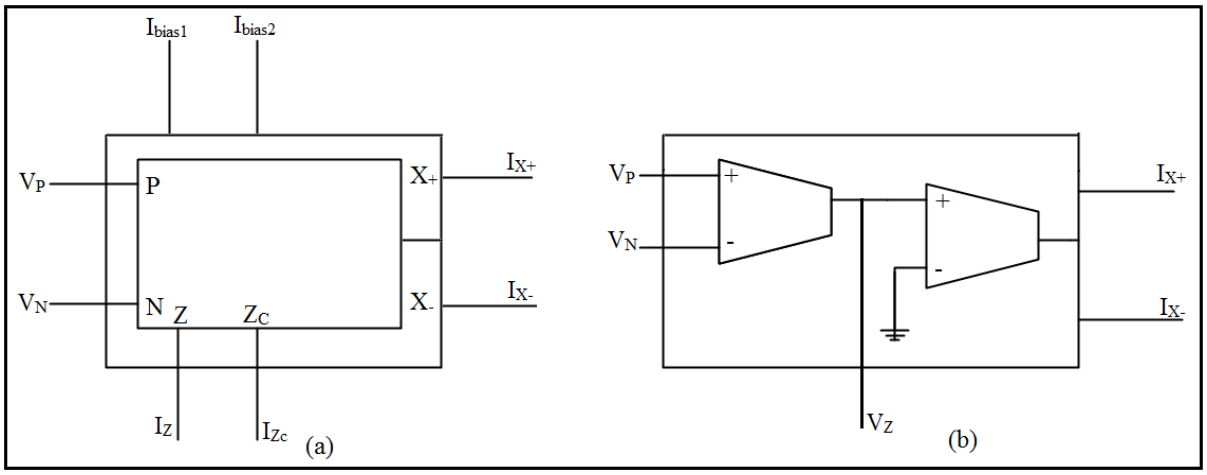

Figure 4.2.1: (a) VDTA block diagram[6] (b) OTA based VDTA

Where g_{m1} and g_{m2} are the trans-conductance parameters of first and second stage of VDTA whose value is controlled by the biasing current I_{bias} of VDTA.

4.2.1 CMOS Implementation

In [7], Abdullah Yesil , Fırat Kacar, Hakan Kuntman, presented a RF filter based on VDTA. In this paper they realized VDTA with the help of CMOS bipolar technology.

The VDTA used in this design is realized with CMOS technology using the topology illustrated in figure 4.2.2 with supply voltages of V_{DD} = 0.9V and V_{ss} = -0.9V and biasing currents of $I_{B1} = I_{B2} = I_{B3} = I_{B4}$ = 150µA. Figure 2.5.2 shows the complete schematic of suggested VDTA, which is based on the use of voltage differencing circuit. The circuit simulation is done using 0.18µm MIETEC level – 3 real transistor model parameters for all transistors in the circuit. The introduced circuit employs two Arbel-Goldminz trans-conductance. Input and output trans-conductance parameters of VDTA element in the circuit are determined by the trans-conductance of outputs transistors. It can be approximated as[7]

$$g_{m1} = (g_3 + g_4)/2,\ g_{m2} = (g_5 + g_8)/2 \text{ or } g_{m2} = (g_6 + g_7)/2$$

where g_i is the trans-conductance of i^{th} transistor defined by

$$g_i = \sqrt{I_{Bi}\mu_i C_{OX}\frac{W}{L}}$$

μ_i is (i = n, p) the mobility of the carrier for NMOS (n) and PMOS (p) transistors, C_{OX} is the gate-oxide capacitance per unit area, W is the effective channel width, L is the effective channel length and I_{Bi} is bias current of ith transistor. For 0.18um CMOS design of VDTA Width and Length is as follows.

Table 1 Width and Length aspect ratio[7]

MOS	W(μm)	L(μm)
NMOS M1, M2	3.6	.36
NMOS M3, M4	3.1	.36
PMOS M5, M6	16.64	.36
PMOS M7, M8	16.64	.36

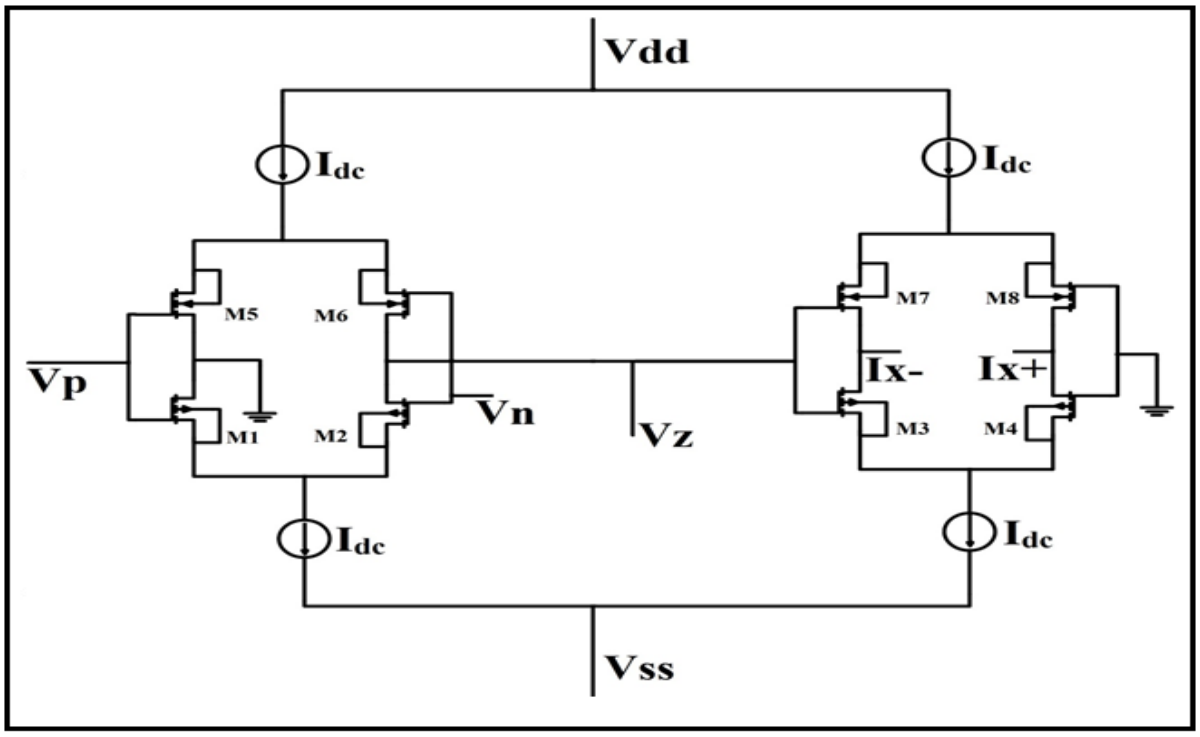

Figure 4.2.2: CMOS realization of VDTA [7].

4.3 Synthesis of a PID controller

In a PID controller circuit, four mathematical function viz. constant multiplication, integration, differentiation and summation, need to be implemented [1]. For a VCCS PID controller we must implement the following transfer function

$$H_i(s) = \frac{I_{out}(s)}{V_d(s)} = K_P + \frac{K_I}{s} + sK_D$$

By appropriately choosing the type of Z_i as resistor and /or capacitor so that a fully differential constant multiplier, a fully differential integrator, a fully differential differentiator and a fully differential summer can be realized.

4.3.1 Synthesis of P controller

Proportional defines with variable time for present values of the error it means for the large and positive error, the output of controller will also be large and positive. A Proportional Controller output voltage or current follows the input voltage or current supplied with a gain value that depends on the parameter connected to the active block. Proportional Controller designed using VDTA shown in figure 4.3.1.

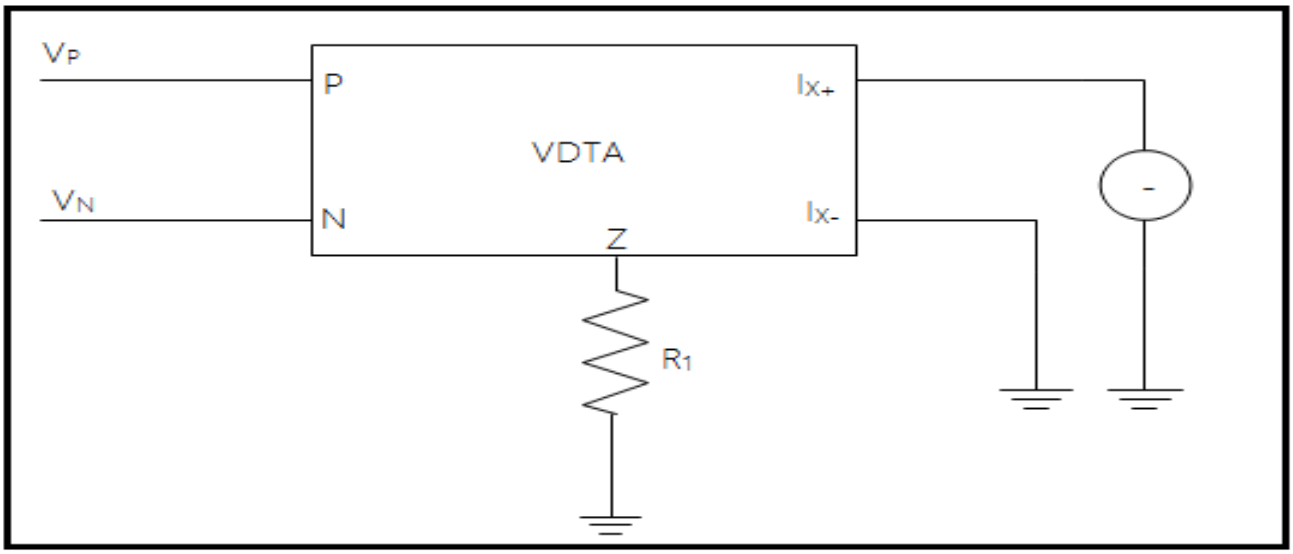

Figure 4.3.1 Proposed Proportional controller using VDTA

The proportional controller gives the following transfer function

$$H_i(s) = \frac{V_{out}(s)}{V_d(s)} = K_P = R_1 * R_2 * g_{m1} * g_{m2}$$

Taking values of $R_1 = 2\ kohm$, $g_{m1} = 416.33\ \mu A/V$, $g_{m2} = 335.231 \mu A/V$, R_2 = 4kohm so that it gives a gain of $K_P = 2.853$, now the Simulation of P-controller is done and its output is shown in figure 4.3.1-1

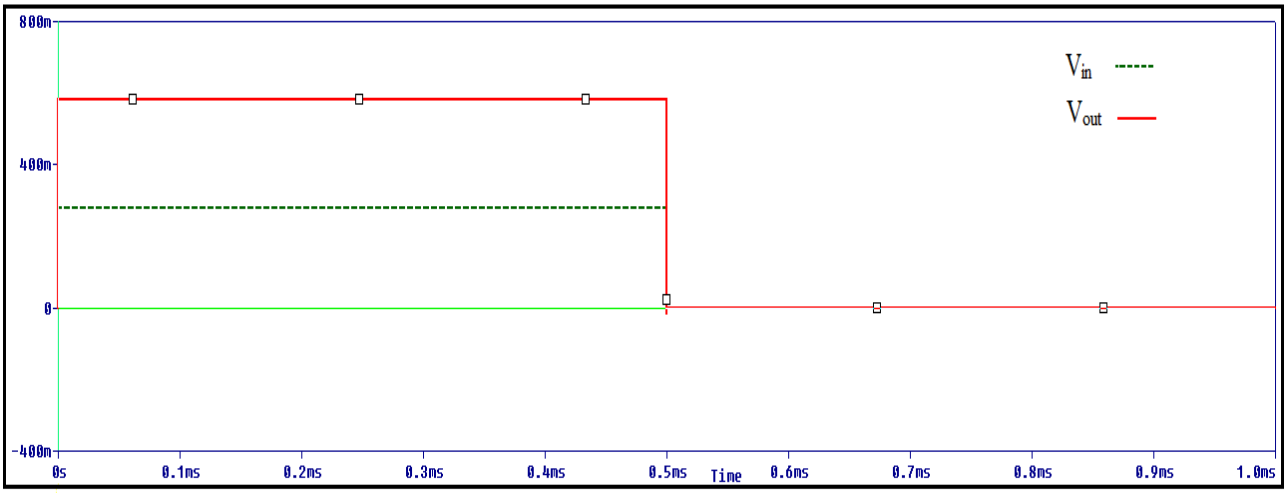

Figure 4.3.1-1 Step response of Proportional controller

4.3.2 Step response of second order system with proposed proportional controller

The PID controller is used to implement a closed loop system by cascaded it with the following second order system and its open loop (without controller) and closed loop time (without/with controller) response was simulated in PSPICE. The details of the simulation results are presented below.

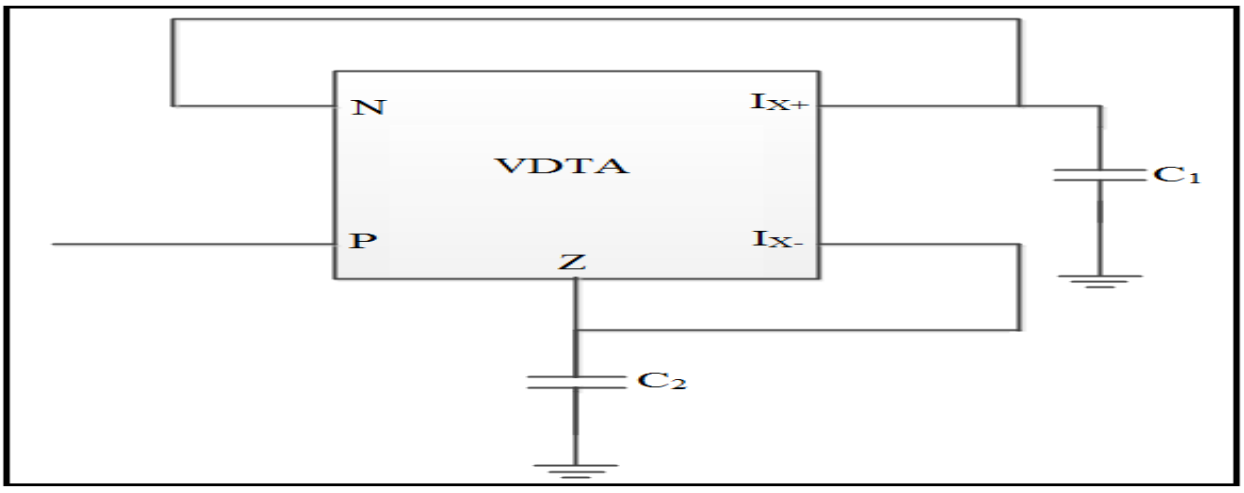

Figure 4.3.2-1: VDTA based second order system [7]

The second order system [7] shown in figure 4.3.2-1 which is a second order low pass filter gives the following transfer function

$$\frac{V_{out}(s)}{V_{in(s)}} = \frac{{}^{g_{m1}g_{m2}}/_{C_1C_2}}{s^2 + {}^{sg_{m1}}/_{C_2} + {}^{g_{m1}g_{m2}}/_{C_1C_2}}$$

Taking values of g_{m1} = 416.33$\mu A/V$ and g_{m2} = 335.231$\mu A/V$, $C_1 = 4.412pf, C_2 = 17.648pf$ so that it gives damping ratio ζ=*0.274* and cut off frequency f_c=*30.83 MHz.* Simulation of this system gives open loop gain=1.006

Step response of this system without any controller in open loop structure is shown in figure 4.3.2-2. Step response of the uncompensated closed loop system i.e., negative feedback without any controller is shown in figure 4.3.2-3. Here the gain decrease by a factor of 0.477 from open loop gain.

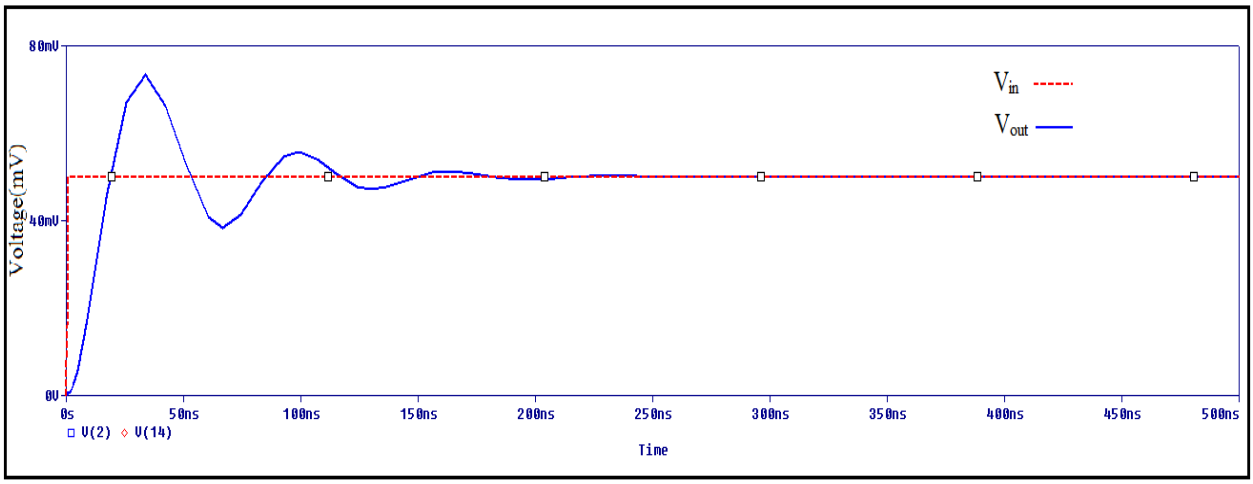

Figure 4.3.2-2: Step response of uncompensated open loop system

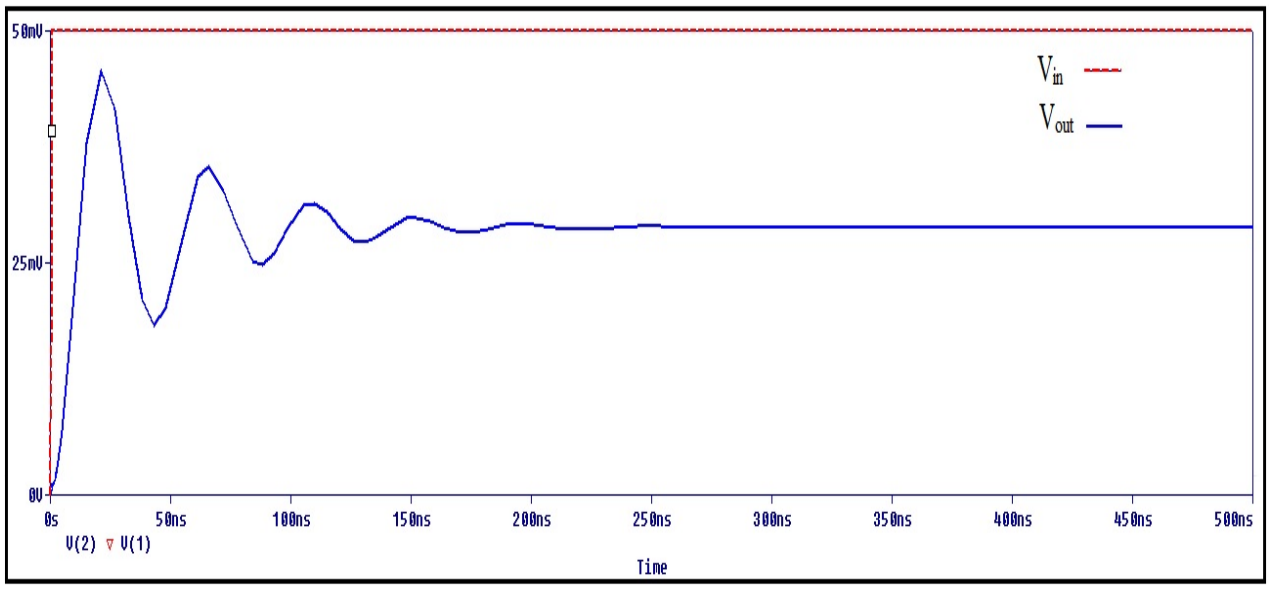

Figure 4.3.2-3: Step response of uncompensated closed loop system

Now the implementation of P controller with second order system is shown in figure 4.3.2-4 is done, for (a) K_P= 2.853, and it shows a error of 10mv as shown in figure 4.3.2-5.

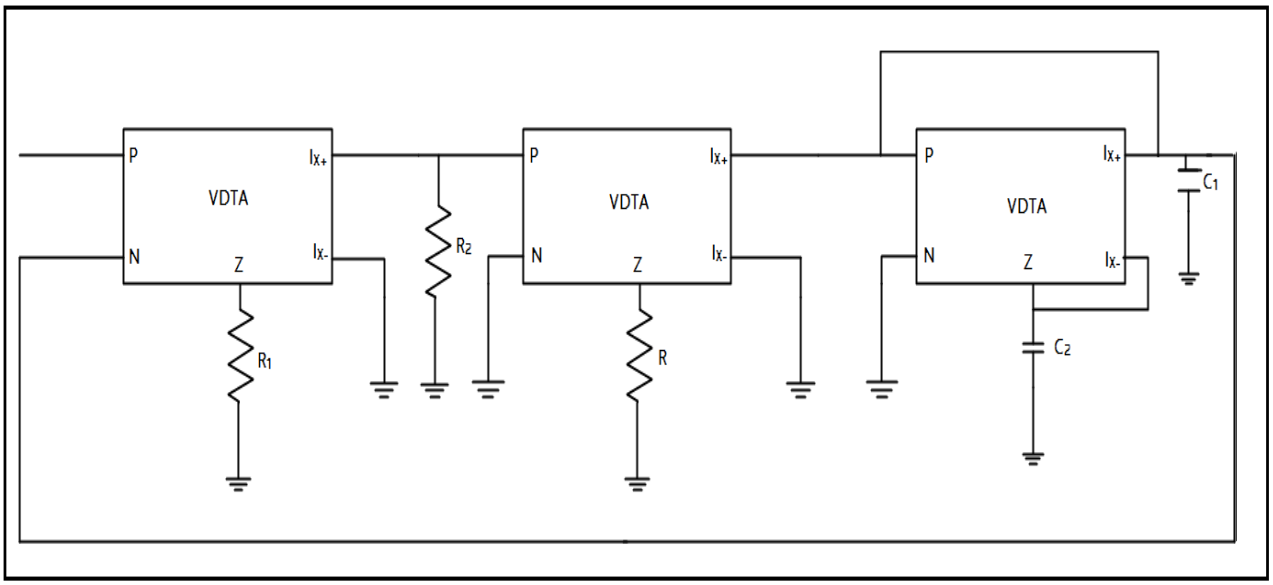

Figure 4.3.2-4: Proportional Controller with second order system

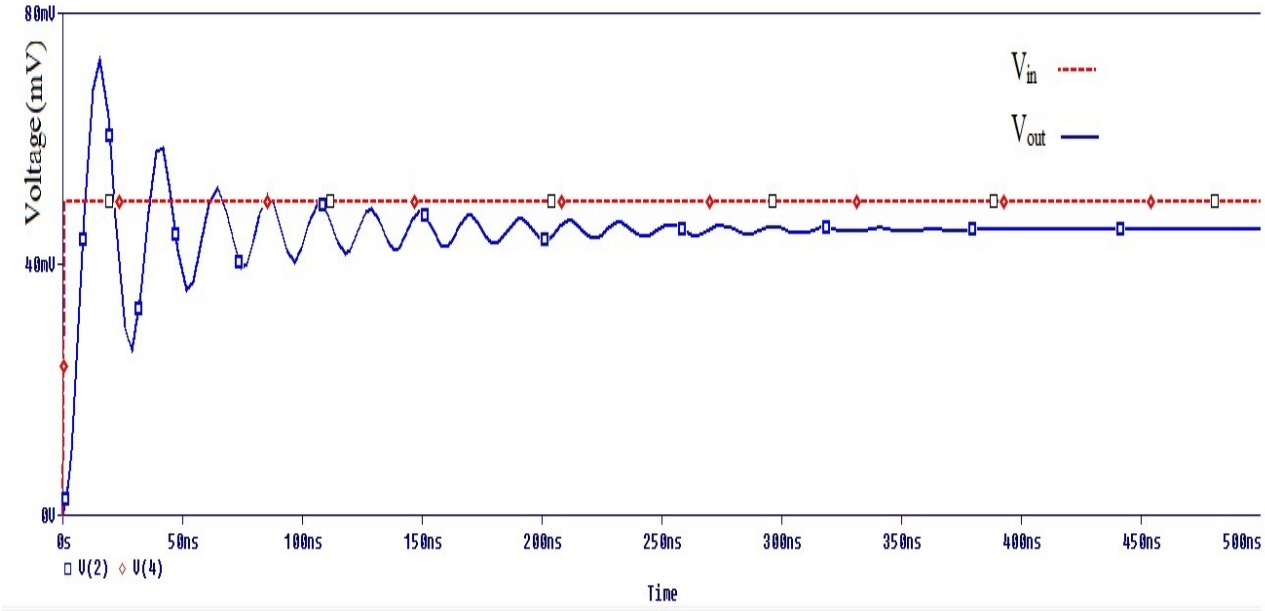

Figure 4.3.2.5: Step response of second order system with proposed proportional controller

Table:**2** Performance of closed loop system with P-controller

K_P	Rise Time(t_r)	Overshoot(M_P)	Settling Time(t_s)	Error(e_{ss})
2.853	9.3496ns	45.044%	395ns	10 mv

4.3.3 Synthesis of Integral controller

Often control systems are designed using Integral control for reducing error. In this control technique, the control systems play in the way that the control exertion is proportional to the integral of the error. The operation of integration can be accomplished helpfully utilizing the VDTA shown in figure 4.3.3-1.

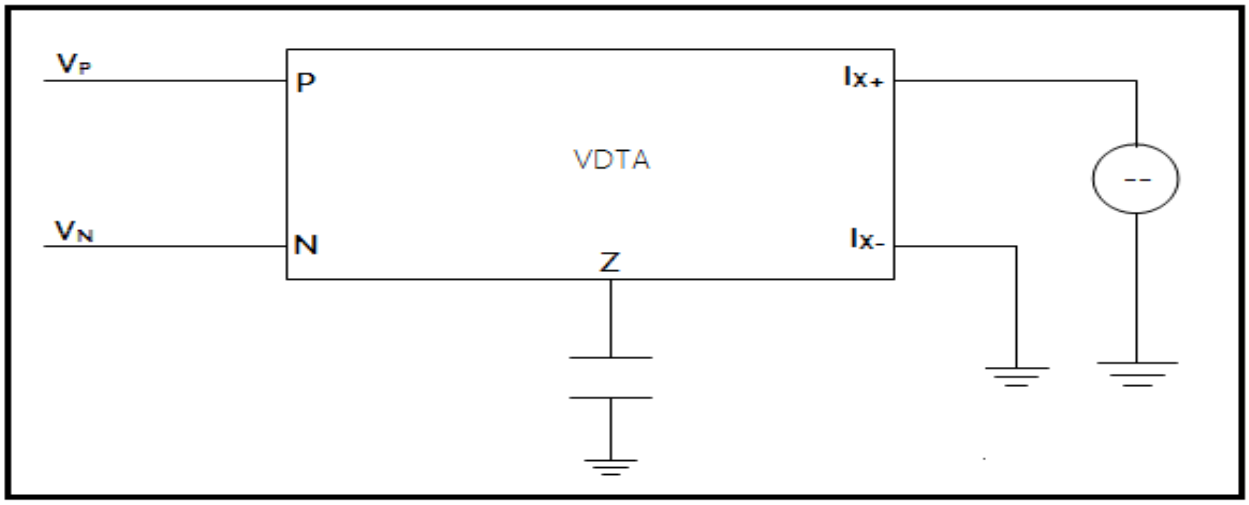

Figure 4.3.3-1 Integral controller using VDTA

The Integral controller gives the following transfer function

$$H_i(s) = \frac{I_{out}(s)}{V_d(s)} = \frac{1}{SC} * g_{m1} * g_{m2} = \frac{K_I}{s}$$

Where K_I = Integral constant = $\frac{g_{m1}g_{m2}}{c}$

Taking values of g_{m1} = 416.33$\mu A/V$ and g_{m2} = 335.231$\mu A/V$, $C =$ 4.412µf which gives K_I = 3.16 * 10^{-3} .The simulation result of this system is as shown in figure 4.3.3-2

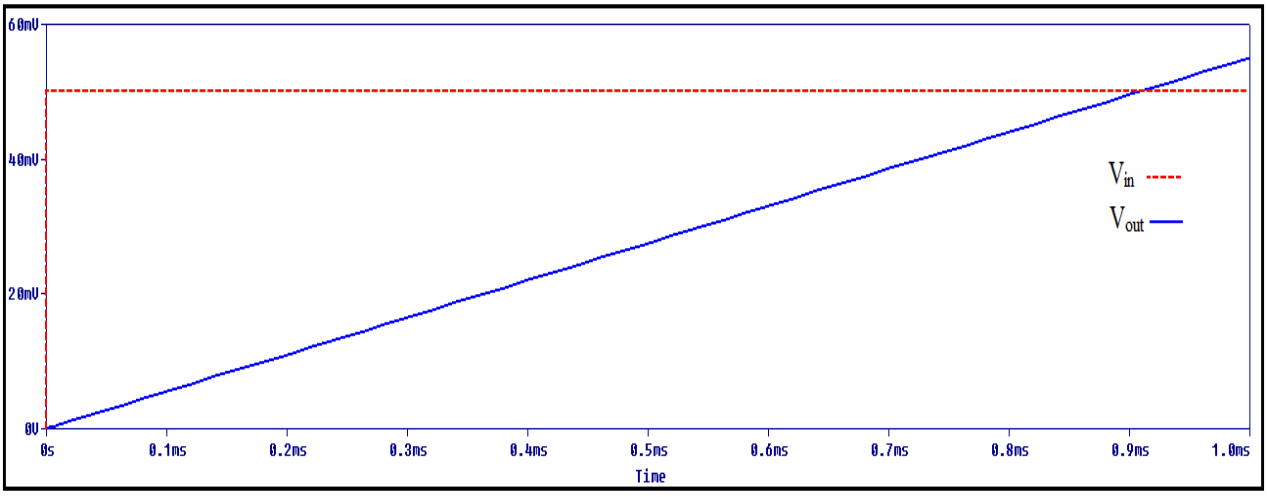

Figure 4.3.3-2 Response of integral controller with step input

4.3.4 Synthesis of Derivative Controller

The process error of the derivative is calculated by finding the slope of the error over time and multiplication of the rate of change with derivative gain K_d. The magnitude of the offering of the derivative rate to the overall control action is labelled as the derivative gain, K_d. Derivative action predicts system behaviour and thus improves settling time and stability of the system. An ideal derivative is not causal, so that implementations of PID controllers include an additional low pass filtering for the derivative term, to limit the high frequency gain and noise. Derivative action is seldom used in practice though - by one estimate in only 25% of deployed controllers because of its variable impact on system stability in real-world applications.

Generally size of electrical inductor is bulkier and not easily available. A inductor is simulated with VDTA for application purpose shown in figure 4.3.4-1(a)

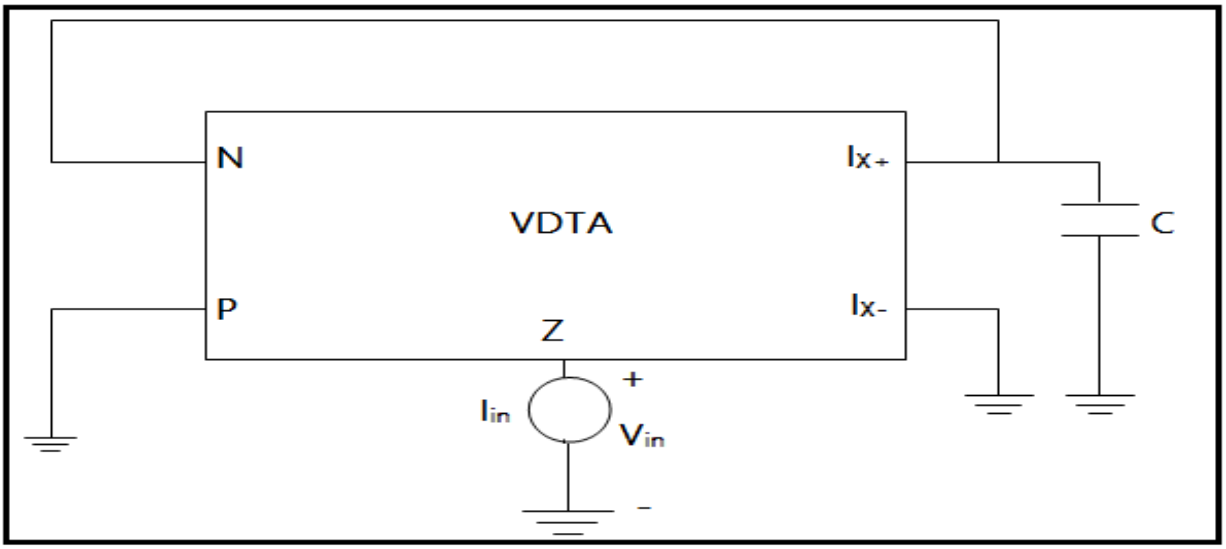

Figure 4.3.4-1(a) Inductor using VDTA

The input impedance of given VDTA circuit is

$$V_i/I_i = sC/g_{m1} * g_{m2}$$

Impedance of a network Z = V_i/I_i =sL

$$L = \frac{C}{g_{m1}g_{m2}}$$

The operation of derivative can be accomplished helpfully utilizing the VDTA shown in figure 4.3.4-1(b)

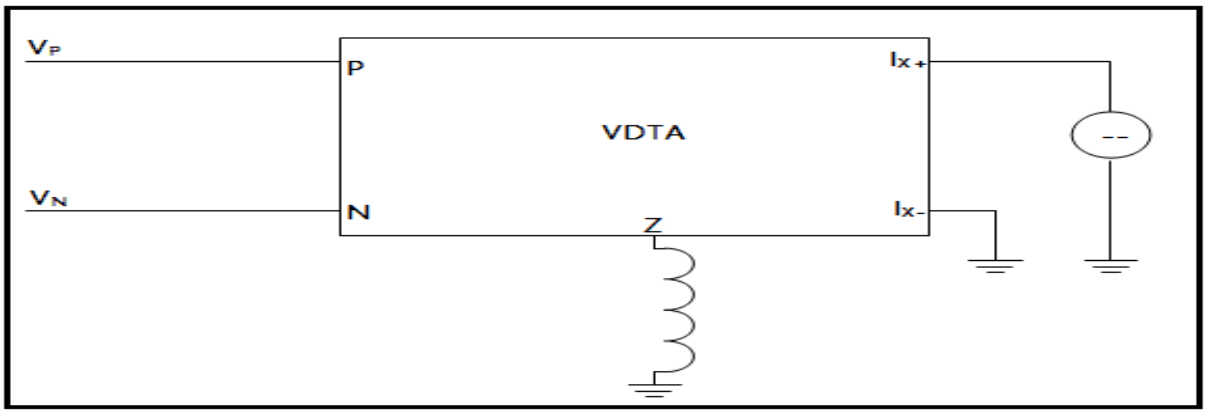

Figure 4.3.4-1(b): Derivative controller with VDTA

The derivative controller gives the following transfer function

$$H_i(s) = \frac{I_{out}(s)}{V_d(s)} = g_{m2} * \text{ sL } * g_{m1} = \text{s*K}_D$$

Where K_D = derivative constant

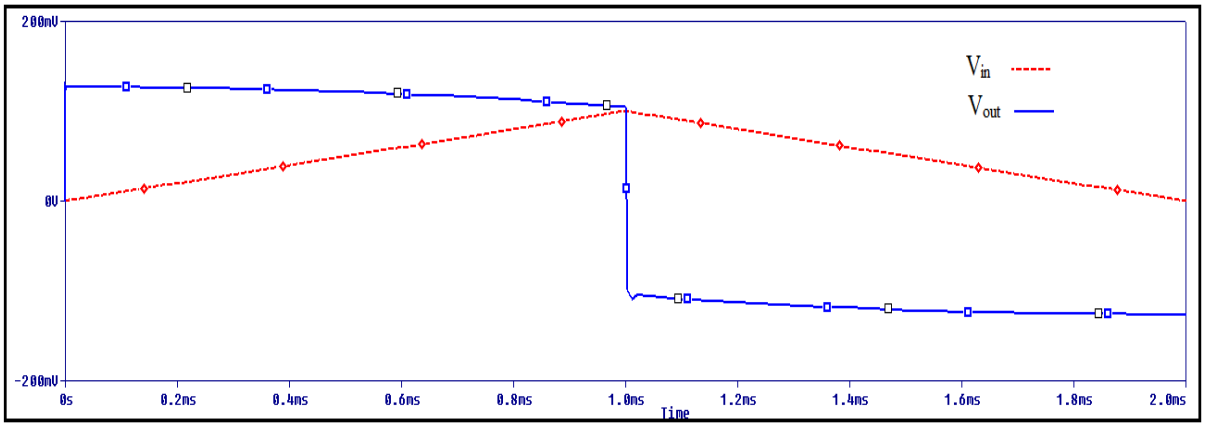

Figure 4.3.4-2 Response of derivative controller with a ramp input

Taking values of g_{m1} = 416.33$\mu A/V$ and g_{m2} = 335.231$\mu A/V$, $L = 20mH$. The simulation result is as shown in figure 4.3.4-2

4.3.5 PI CONTROLLER

A Proportional controller takes less time to reach steady state but also gives more peak overshoot and its exhibits a residual error which decreases the efficiency of plant. A Integral controller reduces the error up to zero but the negative aspects of this controller is that it takes more time to reach at steady state. Addition of these two controllers, make plant to work in good manner and decreases steady state error with less time to reach steady state. A controller using VDTA also provides large bandwidth least steady state error. A proposed PI controller using VDTA is shown below in figure 4.3.5-1

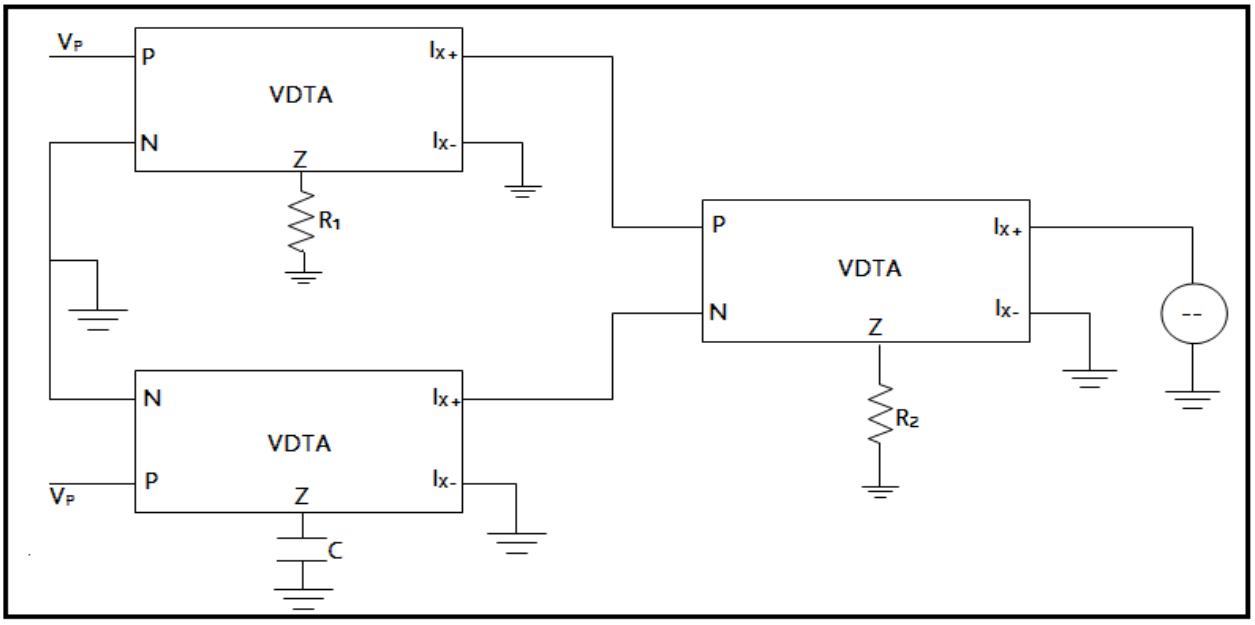

Figure 4.3.5-1: Proposed Proportional – Integral controller with VDTA

The Integral controller gives the following transfer function

$$H_i(s) = \frac{I_{out}(s)}{V_d(s)} = \left(K_P + \frac{K_I}{s}\right)$$

Where $K_P = g_{m1}^2 * g_{m1}^1 * R_1 * R_2$

$$K_I = g_{m2}^2 * g_{m2}^1 / C$$

Taking $g_{m1}^2 = g_{m2}^2 = 335.231 \mu A/V$ and $g_{m1}^1 = g_{m2}^1 = 416.33 \mu A/V$, $C = 1uf$ $R_1 = 1k$ $R_2 = 1.306k$ the value of $K_P = 1.179$ and $K_I = 1.39*10^{-6}$. The simulation result of this system is as shown in figure 4.3.5-2.

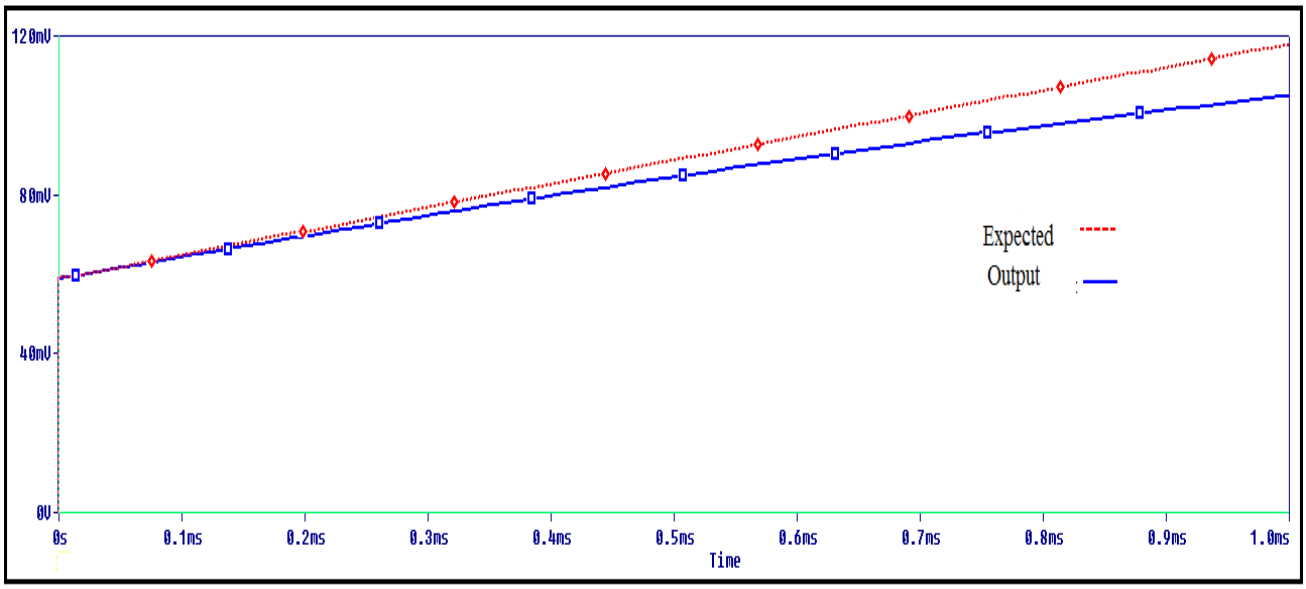

Figure 4.3.5-2: Step response of proposed Proportional Integral controller

Now the implementation of PI controller with $K_P = 1.179$, and $K_i = 1.39*10^{-6}$ is as shown in figure 4.3.5.4.

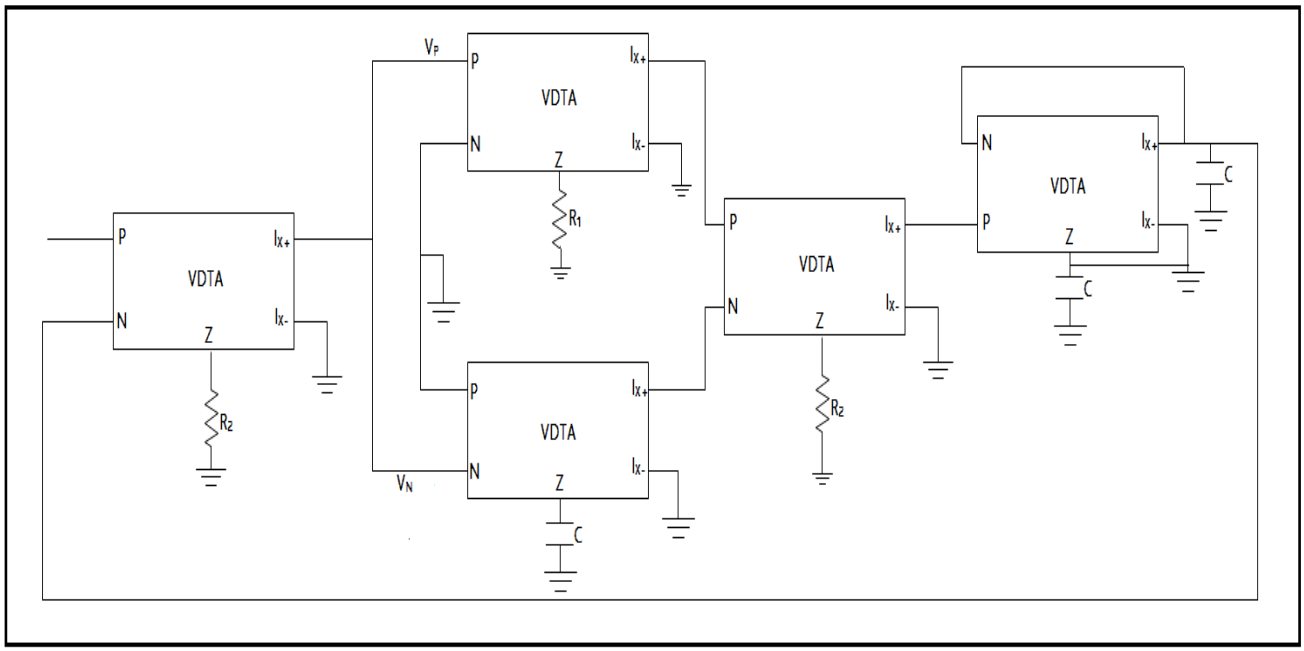

Figure 4.3.5-3: PI controller with second order system

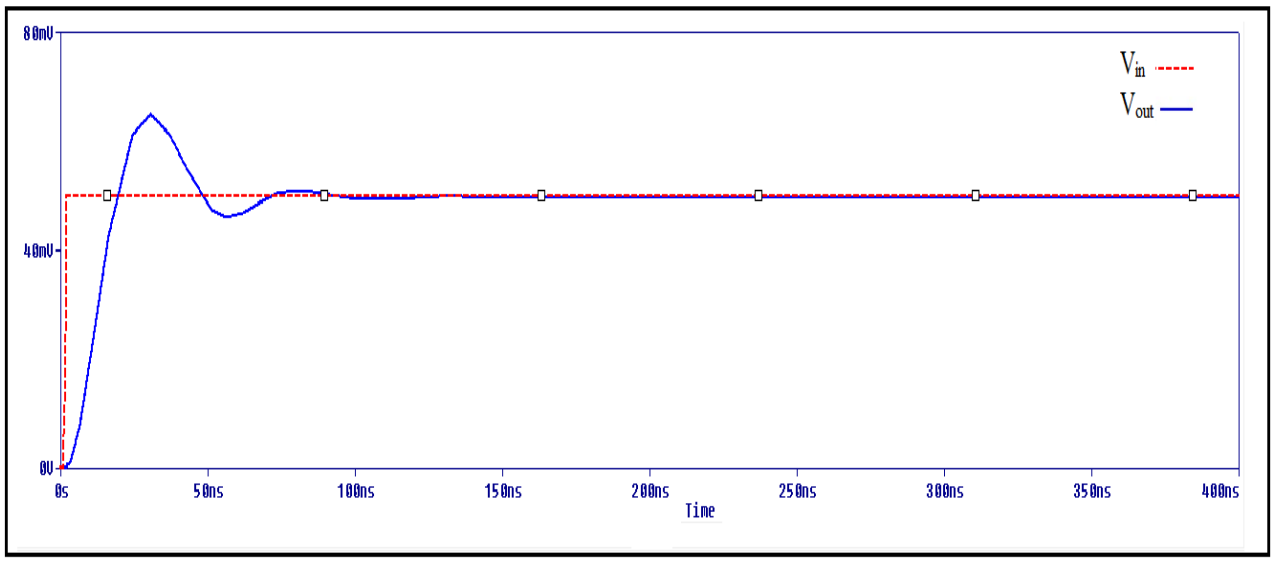

Figure 4.3.5-4: Step response of second order system with proposed PI controller

Table:**3** Performance of closed loop system with PI-controller

K_P	K_I	Rise Time(t_r)	Overshoot(M_P)	Settling Time(t_s)	Error(e_{ss})
1.179	$1.39*10^{-4}$	19.481ns	29.918%	175.97ns	0.265mv

4.3.6 PID Controller

Most practical controller used in industries or plant is PID Controller. The usefulness of PID controller lies in their general applicability to the most control systems [11]. in the field of process control systems, it is well known that the basic and modified PID control scheme have proved their usefulness in providing satisfactory control, although in many given situations they may not provide optimal control.

For a VCCS PID controller we must implement the following transfer function

$$H_i(s) = \frac{I_{out}(s)}{V_d(s)} = K_P + \frac{K_I}{s} + sK_D$$

Where K_P = proportional constant

K_I = Integral constant

K_D = Derivative controller

The PID controller proposed using VDTA is shown in figure 4.3.6-1 and simulation with second order system is shown in figure 4.3.6-2.

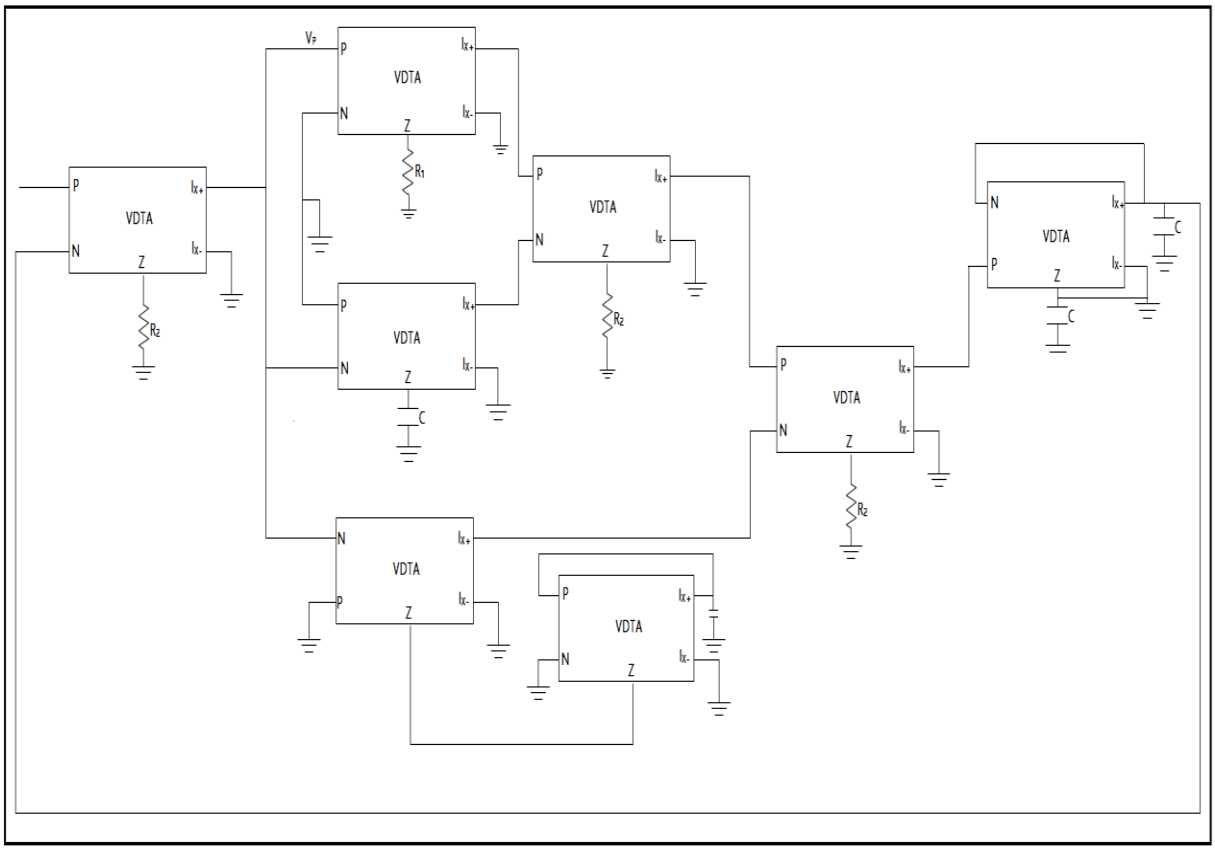

Figure 4.3.6-1 Second order system with PID controller

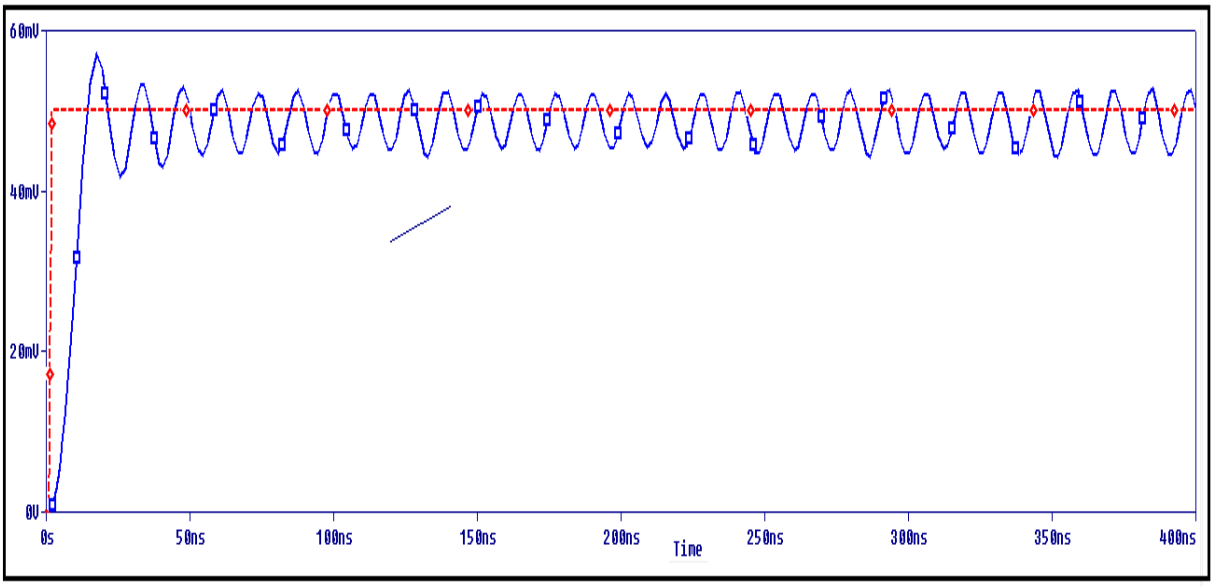

Figure 4.3.6-2 Step response of second order system with PID controller for $K_P = 1.012$, $K_I = 1.256*10^{-4}\ s^{-1}$ $K_D = 0.012\ \mu s$

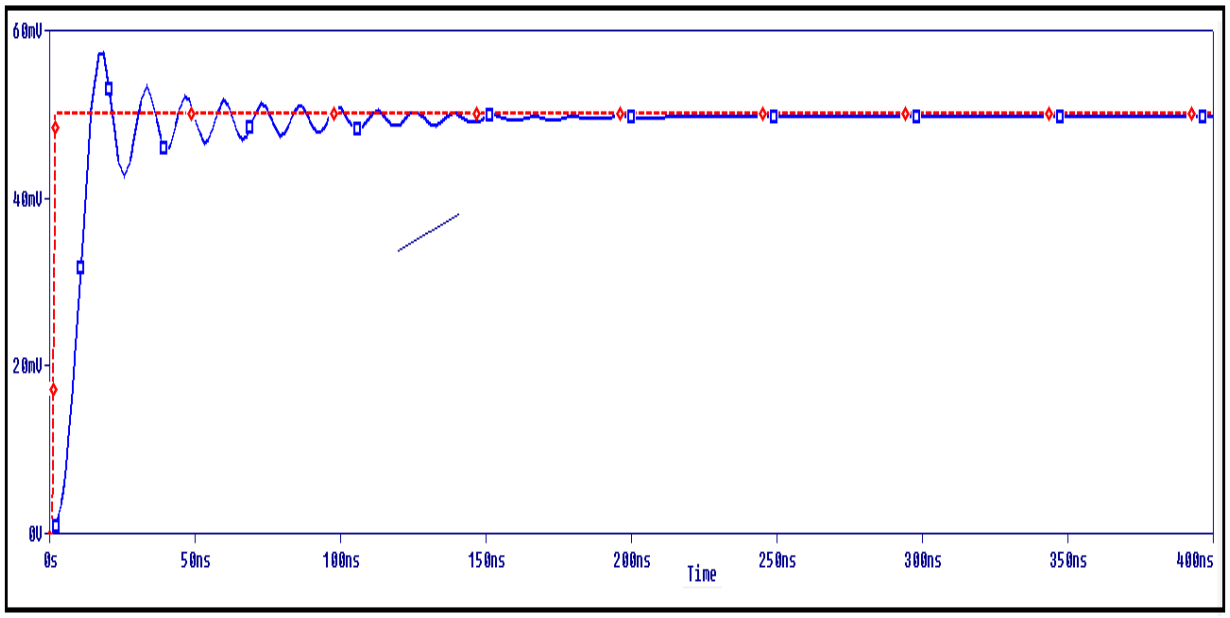

Figure 4.3.6-3 Step response of second order system with PID controller for $K_P = 2.919$, $K_I = 1.39*10^{-4}\ s^{-1}$ $K_D = 0.329\mu s$

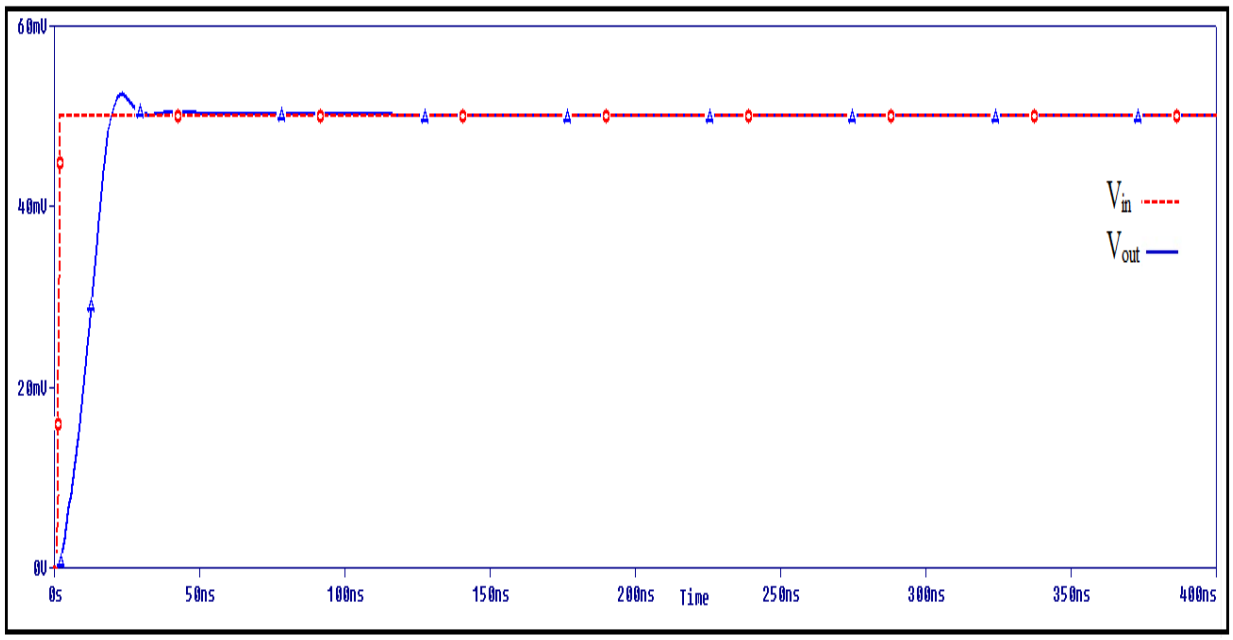

Figure 4.3.6-4 Step response of second order system with PID controller for $K_P = 2.112$, $K_I = 4.6*10^{-4}\ s^{-1}$, $K_D = 0.278\mu s$

Table 4: Performance of second order system with PID controller

Parameters	**Open Loop Uncompensated System**	**Closed Loop Uncompensated System**	**Closed Loop compensated System for K_P = 2.919, K_I =1.39*10^{-4} s^{-1}, K_D = 0.329 µs**	**Closed Loop compensated System for K_P =1.112, K_I =4.6*10^{-4}, K_D =0.278µs**
Overshoot (%)	44.82	39.12	22.938	14.294
Rise Time(µs)	20.098ns	14.21ns	14.610ns	13.961ns
Settling Time	362.745ns	230.392ns	212.338ns	45.455ns
Error	10 µV	46µV	0.674mv	.004mv

4.4 Conclusion

In this chapter, a PID controller is represented using Voltage Differencing Trans-conductance Amplifier (VDTA). The developed controller has been tested on a fully differential second order system whose open loop and closed loop time response study in PSPICE has been presented and we have noticed that with PID controller the closed loop system response improved considerably compare to without PID controller.

4.5 References

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CHAPTER V

CONCLUSION AND FUTURE SCOPE

5.1 CONCLUSION

In this dissertation I have presented a study on designing and implementation of PID controllers using current mode and voltage mode active buildings blocks. The proportional-integral-derivative (PID) controller is one of the most important control element used in the process control industry.

In chapter I, the general description of the PID controller has been presented. Some background material on various current mode and voltage mode active buildings blocks used for the implementation of PID controllers has also been presented.

In chapter II, history, characteristics, terminal equations, applications and CMOS implementation of the current mode active building blocks for implementation of PID controllers are briefly discussed. The devices described are OTA-C, CFOA, CDBA, OTRA.

In chapter III, a brief discussion on the synthesis methods for analog PID controller using different current mode active blocks are described, with the help of signal flow graph techniques and their corresponding blocks. Design of OTA based, CFOA based, CCCII based, CDBA based, and OTRA based PID controller has been presented. The detailed simulation results on the time response studies on a OTA based voltage mode PID controller and a OTRA based current mode PID controller has been presented.

In chapter IV, a new voltage controlled current source active building block VDTA based PID controller has been represented and generalised PID controller block has been developed. The develop controller has been tested on a fully differential second order system whose open loop and closed loop time response study in PSPICE has been presented. The PID controller has been implemented using a VDTA.

5.2 FUTURE SCOPE

In this project emphasis was on using those blocks for implementation of PID controllers which could be implemented with off-the shelf available components. The word presented in this project may be extended to include the transistor level design of PID controllers. Furthermore we have not carried out frequency domain analysis of the closed loop systems. These studies may be carried out to give the complete quantitative characterization of the PID controller. Thus there is ample scope for extending this work.

APPENDIX

P-Spice model file used for process. VDTA SPICE Macro model

```
.SUBCKT VDTA 1 12 3 13 9
.MODEL NMOS1 NMOS
+ LEVEL = 3
+ VTO = 0.41
+ TOX = 2.2E-09
+ NSUB = 2.0E+18
+ NFS = 6.0E+12
+ XJ = 6E-8
+ LD = 9e-9
+ UO = 390
+ VMAX = 2.2E+05
+ THETA = 0.80
+ ETA = 2.8E-03
+ KAPPA = 0.2
+ GAMMA = 0.40
+ RSH = 500
+ CGSO = 3.33449e-10
+ CGDO = 3.33449e-10
+ CGBO = 0.0
+ CJ = 4.96491e-3
+ CJSW = 2.45744e-10
.MODEL PMOS1 PMOS
+ LEVEL = 3
+ VTO = -0.41
```

+ TOX = 2.2E-09

+ NSUB = 2.0E+18

+ NFS = 6.0E+12

+ XJ = 6E-8

+ LD = 9e-9

+ UO = 175

+ VMAX = 1.1E+05

+ THETA = 0.80

+ ETA = 2.8E-03

+ KAPPA = 0.2

+ GAMMA = 0.40

+ RSH = 500

+ CGSO = 3.33449e-10

+ CGDO = 3.33449e-10

+ CGBO = 0.0

+ CJ = 4.96491e-3

+ CJSW = 2.45744e-10

M1 0 1 2 2 PMOS1 W=16.64um L=.36um

M2 3 12 2 2 PMOS1 W=16.64um L=.36um

M3 0 1 4 4 NMOS1 W=3.6um L=.36um

M4 3 12 4 4 NMOS1 W=3.6um L=.36um

M5 13 3 8 8 PMOS1 W=16.64um L=.36um

M6 9 0 8 8 PMOS1 W=16.64um L=.36um

M7 13 3 6 6 NMOS1 W=3.1um L=.36um

M8 9 0 6 6 NMOS1 W=3.1um L=.36um

I1 4 11 DC 150uA

I2 5 2 DC 150uA

I3 6 11 DC 150uA

I4 5 8 DC 150uA

VDD 5 0 DC 0.9V

VSS 0 11 DC 0.9V

.ENDS

P-Spice model file used for process. AD844 SPICE Macro-model

* AD844 SPICE Macro-model 7/91, Rev. A

* JCB / PMI

*

*

* Copyright 1991 by Analog Devices, Inc.

*

* Refer to "README.DOC" file for License Statement. Use of this model

* indicates your acceptance with the terms and provisions in the License Statement.

*

* Node assignments

* non-inverting input

* | inverting input

* | | positive supply

* | | | negative supply

* | | | | output

* | | | | | compensation node

* | | | | | |

.SUBCKT AD844 1 2 99 50 28 12

*

```
* INPUT STAGE
*
R1   99  8     1E3
R2   10 50     1E3
V1   99  9     11
D1   9   8     DX
V2   11 50     11
D2   10 11     DX
I1   99  5     258E-6
I2   4  50     258E-6
Q1   50  3  5  QP
Q2   99  3  4  QN
Q3   8   6 30  QN
Q4   10  7 30  QP
R3   5   6     300E3
R4   4   7     300E3
*C1   99  6     8.8E-15
*C2   50  7     8.8E-15
*
* INPUT ERROR SOURCES
*
GB1  99  1     POLY(1)  1  22  150E-9  90E-9
GB2  99 30     POLY(1)  1  22  200E-9  90E-9
VOS  3   1     50E-6
LS1  30  2     1E-8
CS1  99  2     1E-12
CS2  50  2     1E-12
```

```
*
EREF 97  0     22  0  1
*
* GAIN STAGE & DOMINANT POLE
*
R5   12 97     3E6
C3   12 97     5.5E-12
G1   97 12     99  8  1E-3
G2   12 97     10 50  1E-3
V3   99 13     4.3
V4   14 50     4.3
D3   12 13     DX
D4   14 12     DX
*
* POLE AT 70 MHZ
*
R8  17 97     1E6
C4  17 97     3.18E-15
G4  97 17     12 22  1E-6
*
* POLE AT 300 MHZ
*
R12 21 97     1E6
C8  21 97     0.318E-15
G8  97 21     17 22  1E-6
*
* OUTPUT STAGE
```

```
ISY 99 50     5.1E-3
R13 22 99     16.7E3
R14 22 50     16.7E3
R15 27 99     30
R16 27 50     30
L2  27 28     6E-8
G9  25 50     21 27  33.33E-3
G10 26 50     27 21  33.33E-3
G11 27 99     99 21  33.33E-3
G12 50 27     21 50  33.33E-3
V5  23 27     0.5
V6  27 24     0.5
D5  21 23     DX
D6  24 21     DX
D7  99 25     DX
D8  99 26     DX
D9  50 25     DY
D10 50 26     DY
*
* MODELS USED
*
.MODEL QN   NPN(BF=1E9 IS=1E-15)
.MODEL QP   PNP(BF=1E9 IS=1E-15)
.MODEL DX   D(IS=1E-15)
.MODEL DY   D(IS=1E-15 BV=50)
.ENDS AD844
```