DESIGN OF LOW POWER HIGH GAIN LNA USING MICROSTRIP LINES FOR WIRELESS APPLICATIONS

A Thesis submitted towards the partial fulfilment of the requirement for the

award of the degree of

Master of Technology

in

Microwave and Optical Communication

Submitted by

Pappu Kumar Verma

2K12 / MOC / 12

Under the supervised of

Dr. Priyanka Jain

Assistant Professor

Department of Electronics & Communication Engineering

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING AND APPLIED PHYSICS

DELHI TECHNOLOGICAL UNIVERSITY
(FORMERLY DELHI COLLEGE OF ENGINEERING)
DELHI-110042

JULY 2014

DELHI TECHNOLOGICAL UNIVERSITY

Established by Govt. Of Delhi vide Act 6 of 2009

(Formerly Delhi College of Engineering)

SHAHBAD DAULATPUR, BAWANA ROAD, DELHI- 110042

CERTIFICATE

This is to certify that the thesis report entitled, "**Design of Low Power High Gain LNA Using Microstrip Lines for Wireless Applications**" being submitted by **Pappu Kumar Verma** to the *Department of Electronics and Communication Engineering and Applied Physics, Delhi Technological University, Delhi* in partial fulfilment of the requirement for award of Master of Technology degree in ***Microwave and Optical Communication*** is a record of bona fide work carried out by him under the supervision and guidance of **Dr. Priyanka Jain**. The matter embodied in this report has not been submitted for the award of any other degree.

Dr. Priyanka Jain
Supervisor
Assistant Professor
Department of ECE
Delhi Technological University

Prof. Rajiv Kapoor
Head of Department
Department of ECE
Delhi Technological University

DECLARATION

I hereby declare that all the information in this document has been obtained and presented in accordance with academic rules and ethical conduct. This report is my own, unaided work. I have fully cited and referenced all material and results that are not original to this work. It is being submitted for the degree of Master of Technology in Engineering at the Delhi Technological University. It has not been submitted before for any degree or examination in any other university.

Signature :

Name : Pappu Kuamr Verma

ABSTRACT

With the rapid development of the communication industry, more and more kinds of wireless communication apparatus are needed, such as small a low noise figure, low input/output return losses, a high IIP3, low power have been the main target of the businessman and the manufacturer of the wireless communication. In this condition, swift developmental radio frequency (RF) wireless communication technology has been widely used in all fields of the world. Low noise amplifier (LNA) which is in the RF front-end circuit has the great value in this field. LNAs are a crucial element of RF receivers. Their role is to amplify the RF signal to a level that meets the sensitivity requirements of the other components (e.g. Filter). In order to achieve the required gain it is essential to make sure that the reflection coefficients S11 and S22 are minimized. In addition, LNAs are usually the bottleneck in terms of Noise Figure and distortion.

Advanced Design System (ADS) tool was used for design and simulation, and each design was tuned to get the optimum value for noise figure, gain and input reflection coefficient. LNA stand-alone gives acceptable value of noise figure and gain but the bandwidth was too narrow compared to specification. The gain was almost flat over the whole band, i.e., 2.4-2.5 GHz compared to Low-Noise Amplifier designed

In this project report work, a new approach of design and performance analysis of A Low Power High Gain LNA for Wireless Applications is performed at 2.45 GHz. Performances of different designs are compared with respect to noise figure, gain, input and output reflection coefficient. In this design process, a single stage LNA using C-S LNA with a simple C-S stage added to the 'cascode' is design with CMOS Technology. After the simulation we got the simulated result of low noise amplifier as forward voltage gain (S_{21}) of 26.486 dB, noise figure is 1.268 dB, input reflection coefficient (S_{11}) is -5.841 dB, output reflection coefficient (S_{22}) is -52.533 dB and S_{12} is -18.823 dB. Power consumed by the design is 4.49 m W with supply voltage 1.2 V.

LNA designed using HEMT (using microstrip lines) at 2.4 GHz operating frequency, simulated by ADS designed by Agilent Technologies. After the simulation it has achieved the gain 13.33 dB, noise figure 0.667dB, minimum noise figure 0.518 dB, input reflection coefficient -17.06 dB, output reflection coefficient -13.02 dB, reverse isolation coefficient -23.32 dB, stability is greater than 1 with supply voltage 5 V using microstrip lines.

ACKNOWLEDGEMENTS

I would like to express my sincere gratitude to my project supervisor, Asst. Professor **Dr. Priyanka Jain**, for her supervision, invaluable guidance, motivation and support throughout the extent of the project. I have benefitted immensely from her wealth of knowledge.

I would also like to thank **Dr. Ajeet Kumar** (Department of Applied Physics), **Prof. R. K. Sinha** (Department of Applied Physics) and **Dr. J. Panda** (Department of ECE) for their precious suggestions, support and technical help during the course of this project.

I am indebted to **Prof. Rajiv Kapoor**, Head of Department of Electronics and Communication Engineering, Delhi Technological University, for his support and encouragement in carrying out this project.

I wish to express my heart full thanks to **Prof. S.C. Sharma**, Head of Department of Applied Physics, Delhi Technological University for his support that helped me a lot in successful completion of this project.

I am also grateful to **Prof. P. B. Sharma,** Vice-Chancellor, Delhi Technological University for providing the research environment in the institute.

My gratitude is extended to my colleagues and friends who have not been mentioned here personally in making this project a success.

Last but not least, I take this opportunity to express my deepest thanks to my parents and my sister. Without their support, love and encouragement, it would not have been possible to pursue M.Tech. degree studies. I sincerely thank them.

Pappu Kumar Verma
M.TECH. (MOC)
2K12/MOC/12

TABLE OF CONTENTS

LIST OF FIGURES

FIGURES

LIST OF TABLES

TABLES

LIST OF SYMBOLS

V_{out}	Output Voltage
V_{in}	Input Voltage
Γ_s	Source Reflection Coefficient
Γ_L	Load Reflection Coefficient
K	Stability Factor
Δf	Bandwidth
f_o	Centre Frequency
G_m	Transconductance
P_D	Power Dissipation
C	Correlation coefficient
Q	Quality Factor
L	Chanel Length
g_{do}	Drain to Source Conductance
γ	Drain Noise Coefficient
δ	Gate Noise Coefficient
C_{gs}	Gate to Source Capacitance
W	Width of MOSFET
I_D	Drain Current
L	Inductor
C	Capacitor
G_T	Transducer Gain
G_P	Operating Power Gain
G_A	Available Power Gain

LIST OF ABBREVIATIONS

ISM	Instruments Scientific and Medical
ADS	Advance Design System
WLAN	Wireless Local Area Network
LNA	Low-Noise-Amplifier
BPF	Band-Pass Filter
IMN	Input Matching Network
OMN	Output Matching Network
LPD433	Low Power Device, 433 MHz
PMR446	Private Mobile Radio, 446 MHz
ITU	International Telecommunication Union
ITU-R	The ITU Radio-communication Sector
FCC	Federal Communications Commission
WDCT	Digital Cordless Telecommunications
RFID	Radio Frequency Identification
Hiper LAN	High Performance Radio LAN
Wi-Fi	Wireless Fidelity
PCB	Printed Circuit Board
PCS	Personal Communications Service
WCDMA	Wideband CDMA
ADS	Advanced Design System
WLL	Wireless Local Loop
SMD	Surface Mounted Device

Chapter 1

Introduction

1.1 Overview

RF technology has changed quite a bit since the days of Marconi and Tesla-both the men who enabled radio communications. Modern radio frequency engineering is an exciting and dynamic field; due to the beneficial inter dependency between recent developments in electronic device technology and the increase in demand for voice, data, and video communication capacity. Prior to this revolution in communications, RF technology was the nearly exclusive domain of the defence industry but the recent increase in demand for communications systems with applications such as wireless paging, broadcast video, Bluetooth transceiver, Wi–Fi (WLAN), Wi-Max, CDMA, WCDMA, EGPRS, GSM and many more is revolutionizing the technology [1-2]. RF technology is important for these applications because these require high operational frequencies which allow both large numbers of independent channels as well as significant available bandwidth per channel for high speed communication. Figure 1.1 shows some disciplines that requires RF design.

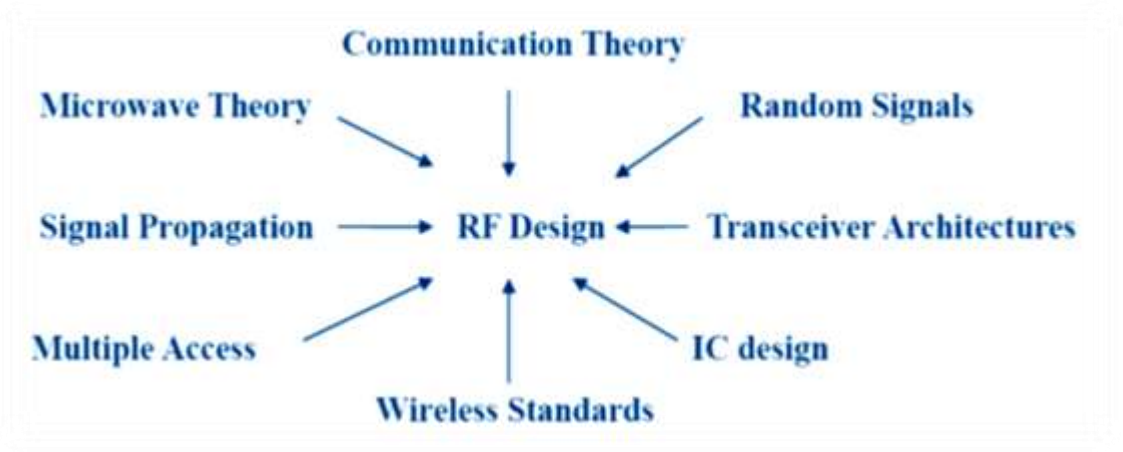


Figure 1.1: Disciplines requiring RF design [1]

The field of design in the electronics system that employs RF and Microwave Engineering includes the frequencies ranging from 300kHz to over 100GHz. RF engineering refers to the circuits/device operating in the frequency range 300kHz to over 1GHz while the microwave engineering refers to the circuits/device operating in the frequency range between 300kHz or 1GHz to over 100GHz. Unfortunately, RFIC design is quite complex when tested results are obtained that differ drastically

from the simulation result. The reasons for this disparity may normally be traced to one of the following [2]:

- The frequency of operation is such that the circuit's elements display complex behaviour, not represented by the pure element definitions utilized during the design.
- The circuit layout includes coupling paths not accounted for in the design.
- The ratio of transverse dimensions of transmission lines to wavelength is non-negligible thus, additional unwanted stored modes become available.
- The package that houses the circuit becomes an energy storage cavity, thus absorbing some of the energy propagating through it.
- The perfect (ideally) dc bias source is not adequately decoupled from the circuit.
- The degree of impedance match among interconnected circuits is not good enough, so that large voltage standing wave ratio (VSWR) is present, which give rise to inefficient power transfer and to ripples in the frequency response.

1.2 Design Flowchart

In the designing of low noise amplifier, some basic aspect of low noise amplifier should be kept in mind. Since in low noise amplifier there is trade-off between many factors i.e. gains, noise figure, stability, power consumption, and nonlinearity etc. And depending on these factors we have previously discussed different topology of low noise amplifier design. In this work we have chosen inductive source degeneration topology because this provides some beneficial advantages over other topologies as discussed in chapter 4. Inductive source degeneration topology is one of the most useful configurations for low noise amplifier design; because common source configuration provides low noise and solved the stability related problem.

Flow chart of LNA design is shown below that describes the design flow of low noise amplifier. The design starts from some basic specification means some standard output values that is desired for any circuits design these specification are scattering parameters, Gain, Noise Figure, Stability, Power, linearity etc. and our aim, tends to achieve these specified values. Second step in the design is choice of technology so here; HEMT technology has chosen for this design. Third step is choice the topology, there are different types of topologies and among them we can use topology depending on our design. Fourth step is some basic calculation like device width, gate to source capacitance and other things after that we can do the biasing to set the operating point and last if

there is some impedance mismatch so we have to do impedance matching by inserting a filter network.

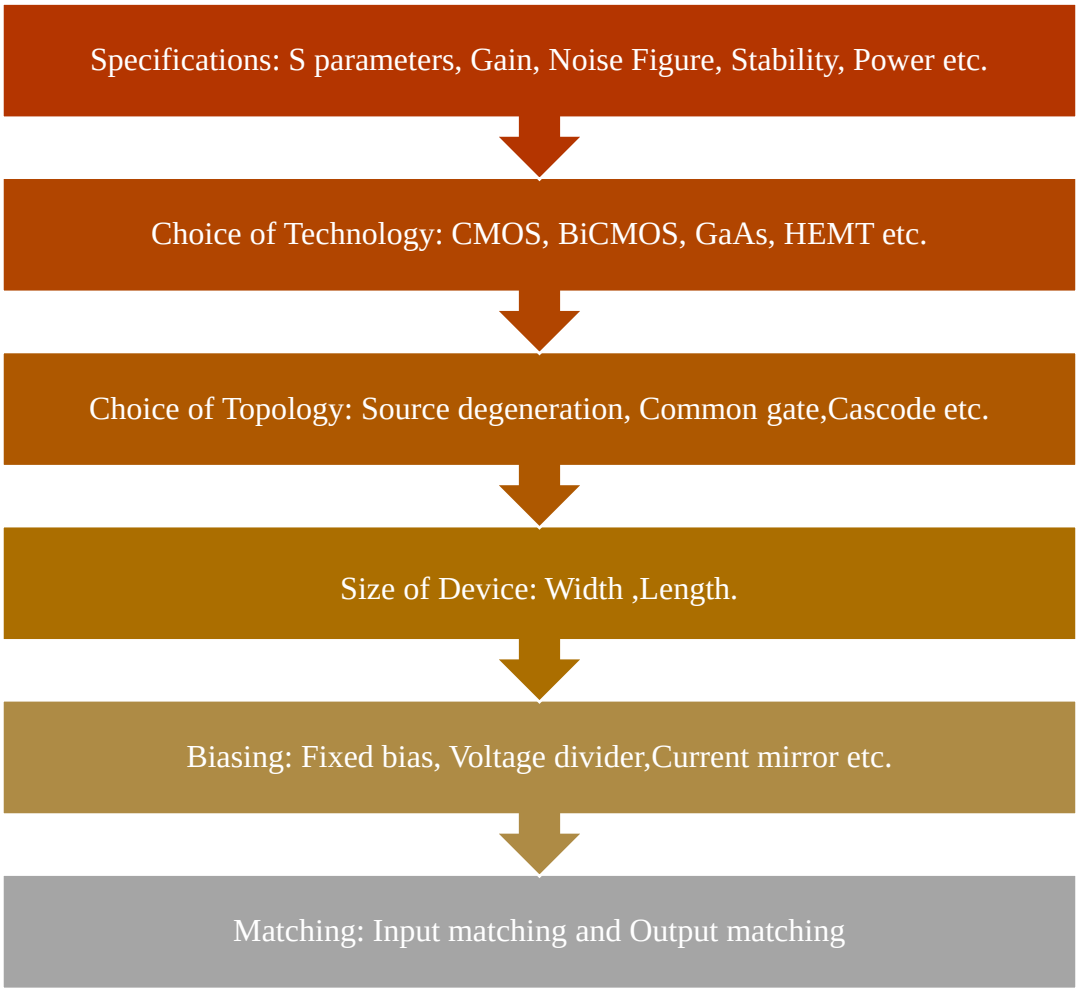


Figure.1.2: Flow chart of designing process for LNA

1.3 Motivation and Problem Statement

Being the first block of the receiver chain LNA has to be able to receive the maximum signal without reflecting any part of it at the same time it has to ensure that it adds less noise to the signal component. The input impedance of the LNA should be 50Ω to match the source impedance, also the output stage should be able to give less noise, and more gain. Since any receiving block's performance depends mainly upon the LNA performance. It is the most important block for any communication system. So a LNA circuit with high gain and very low noise figure is highly needed for any modern receiver system, at the same time it should be less power consuming. In this work my aim to design a low noise amplifier at 2.4 GHz operating frequency for wireless communication because low noise amplifier is first block of receiver circuit and it is important to give more concentration to achieving high gain and low noise figure.

1.4 Objective/Scope of present work

The main objective of the research presented in this project is to design a low noise amplifier to be used in wireless communications operation. The goal of project is to understand the concepts of RF design such as gain, noise, matching networks, and linearity that are essential for amplifiers.

In the communication system, Low noise amplifier is the second element after antenna. LNA is used to boost up the received low energy and noisy signal to a desired energy level with noise suppression. So, noise figure (NF) is the key issue of concern in this design [3-5]. The receiver is the most power hungry block and the power consumption should be as low as possible. So, noise figure and power consumption are not less important issues than gain [6-7]. With the small power consumption, the LNA should amplify the weak receiving signal to the level suitable for processing and provide gain to overcome the noise of subsequent stages while adding small amount of noise as possible. Matching of each block of the receiver is also an important issue in order to provide maximum power transfer at a particular frequency the matching is required [8-9]. Furthermore, input and output matching to the source and load can maximize the gain. Input and output impedance matching is characterized by the input and output return loss. Since, it can affect the performance of the device. The gain should be large enough and the same time noise should be as less as possible [10]. The LNA should present specific impedance at the input, e.g. 50Ω to interface with the filter or antenna. Finding the delicate balance in all issues or parameters becomes the challenge more often than simply maximizing a single key parameter. The most recognizable trade-off is between LNA gain and noise figure (NF). Linearity is also an important design issue. Third order intercept point, IP_3 (Third order intercept point) has emerged as an important parameter in LNA design. The easiest way to improve the IP_3 performance for a given frequency is to increase the current density or current drawn of LNA. Input and output return losses, S_{11} and S_{22}, are also available for trading off to achieve improved gain and NF performance. Typically, the input and output matches are designed to afford good gain and NF performance. It is a balance of performance parameters. The approach for achieving this target is to design a low noise amplifier for wireless application at 2.4 GHz operating frequency range.

The next section describes the organization of chapters in the thesis.

1.5 Thesis Structure

The thesis report is divided into six chapters, each having ample information for comprehending the concept of this project.

Chapter 1 introduces the background history of RF technology and objective of research of low noise amplifier.

Chapter 2 discussed the Low Noise Amplifier also deals the details about the research work carried out so far in the design of Low Noise Amplifier for different domain of RF.

Chapter 3 provides the details about the different basic parameters of RF circuits design i.e. different type of Gain, noise in MOSFET, Noise Figure, Stability, linearity, Bandwidth etc.

Chapters 4 presents different topology of Low Noise amplifier Design, based upon the Gain, Noise figure, and also discusses which topology is best suitable for Low Noise Amplifier.

Chapter 5 discusses about the design, simulation, and analysis result of Low Noise amplifier, and some basic step for calculating the components parameters.

Chapter 6 summarizes detailed results of simulation analysis.

The Final chapter of the thesis (Chapter 7) presents the conclusions and future aspects of this project. The significance and contribution of this work is summarized.

Chapter 2

Literature Review

2.1 Introduction

The growth of wireless service and other telecom application has pushed the semiconductor industry towards complete system on chip solutions. Wireless system comprise of a front-end and a back end section. The front end section process analog signals in the high radio frequency range, while the back end section process analog and digital signals in the baseband low frequency range.

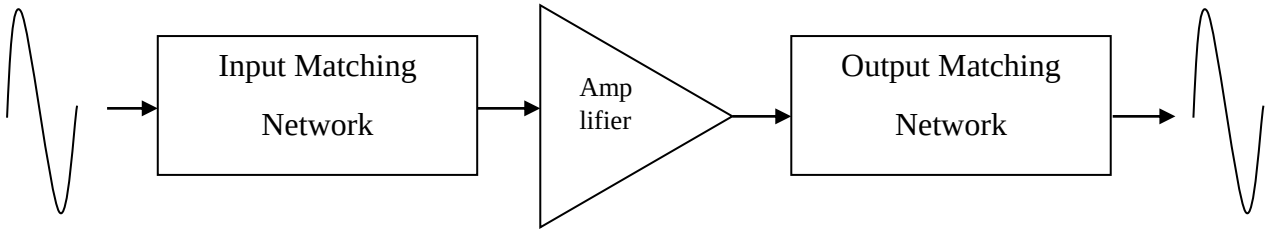


Figure 2.1: Basic low noise amplifier

The radio frequency signal received at the antenna is weak. Therefore an amplifier with high gain and good noise performance is needed to amplify this signal before it can be fed to others part of the receiver. Such an amplifier referred to as a low noise amplifier as shown in Figure 2.1. The first stage of the receiver is typically a low noise amplifier, whose main function is to provide enough gain to overcome the noise of subsequent stages (such as mixer). Aside from providing this gain while adding as little noise as possible, an LNA should accommodate large signals without distortion, and frequently must also present specific impedance. The general topology of low noise amplifier can be broken down into the three stages: input matching, amplifier and the output matching. Low noise amplifier used in various applications like ISM radio, cellular/PCS handsets, GPS receiver, cordless phone, wireless LAN, wireless data, satellite communication etc.

2.2 Literature Survey

Lot of research is being currently done in designing low noise amplifier. Some of the important papers related to this thesis work have been divided into four sub groups:

1. Application Based LNAs

2. High Gain LNAs
3. Different Matching Techniques for LNAs
4. Low Noise Techniques for LNAs

The discussions on the literature belonging to the above subgroup are given below:

2.2.1 Application Based LNAs

A low noise amplifier intended for use in a Global Positioning System (GPS) Receiver discussed by Derek K. Shaeffer et al. [11]. Inductive source degeneration topology has used for design of LNA.

A low noise amplifier, intended for use in a DECT (Digital Enhanced Cordless Communications) Receiver is presented by Jerome Le ny*et al.* [12], uses differential configuration with inductive source degeneration and constant g_m bias for design of LNA.

The concept of Concurrent Multiband Low Noise Amplifiers is presented by Hussein Hashemi et al. [13]. They discuss the advantages of field effect transistors over bipolar junction transistor and concurrent dual band low noise amplifier in communication systems.

A low-noise amplifier for use in Ultra wideband wireless receiver is introduced by Andrea Bevilacqua et al. [14]. In the design it is discussed why the low noise amplifier is essential for UWB receiver. In their design they used multi-section Chebyshev filter at the input network and buffer stage at the output stage for design of LNA.

A low noise amplifier, intended for use in Ultra wideband wireless receiver is discussed by Che-Cheng Huang1 et al. [15] in which two stage cascode amplifiers with shunt-peaked load, two 2nd order notch filters, and an output buffer has been used for design of LNA.

A low noise amplifier intended for use in Ultra wideband wireless receiver front end is presented by Qiang Li et al. [16]. In which current-reuse topology, capacitive peaking is used for design of LNA. Inductors were not used in the design.

Zhe-Yang Huang et al. [17] has discussed low noise amplifier has been designed by using wideband input impedance matching network, a cascode amplifier with shunt-peaked load, a RLC impedance feedback loop. In another design Meng-Ping Chen et al. [18] used three LC-tank cascode amplifier and one output buffer for design of LNA.

A low-noise amplifier intended for use in Wi-Max system is discussed by Yu-Lin Wang [20]. They used differential, cascode configuration RC shunt feedback and shunt peak load for design of LNA.

A low noise amplifier intended for use in Ultra wideband Wireless Receiver is also provided by ShilaShamsadini et al. [21] with two-stage, common- gate in cascade with cascode for design of LNA. Table 2.1 shows the summary of application based LNA's.

Table 2.1: Summary of Application Based LNA's

Parameters	**[11]**	**[12]**	**[14]**	**[15]**	**[16]**	**[18]**	**[20]**	**[21]**
Year	1997	2002	2004	2007	2007	2008	2009	2010
Technology(um)	0.18	0.25	0.18	0.18	0.13		0.18	0.18
S_{11}(dB)			-10	-6.4	-8.3	-11	-11	-10
S_{22}(dB)				-10.1			-10.9	
S_{21}(dB)	22	15	9.3	13.3	11	24.4	14.4	
Noise Figure(dB)	3.5	2	4	2.5	4.8	2.4	3.8	2.9
Power consumed(mw)	30	25	9	21.9	19	9.2	14.8	10

2.2.2 High Gain LNAs

Bevin G.Perumana et al. [19] had used inductorless resistive feedback with current reuse topology and tuned resistive feedback for increase of gain in low noise amplifier for multiband applications.

Shila Shamsadini et al. [21] presented two-stage, common-gate in cascade with cascode for increase in gain low noise amplifier for Ultra Wideband applications. T. Hui Teo et al. [22] used fully integrated differential configuration for increase of gain in low noise amplifier for short-range radio in biomedical devices.

Jenn-Tzer et al. [23] used differential configuration and high-Q active inductor for design of low noise amplifier for multiband application. Table 2.2 shows the summary of high gain LNA's

Table 2.2: Summary of High Gain LNA's

Parameters	[19]	[22]	[21]
Year	2008	2008	2010
Technology(um)	0.09	0.18	0.18
S_{21}(dB)	22	26	25

2.2.3 Different Matching Techniques for LNAs

Derek K. Shaeffer et al. [11], discussed the different matching topologies at the input. It includes resistive termination, 1/gm termination, shunt-series feedback, inductive degeneration. For designing LNA inductive degeneration is used because of its advantage of providing low noise figure, high linearity, and high gain.

Andrea Bevilacqua et al. [14] used an inductively degenerated common-source amplifier by embedding the input network of the amplifying device in a multi-section reactive network so that the overall input reactance is resonated over a wider bandwidth.

Zhe-Yang Huang et al. [17], used wideband input impedance matching network, a cascade amplifier with shunt-peaked load, a RLC impedance feedback loop and an output buffer for input and output matching.

Meng-Ping Chen et al. [18], used input impedance matching network that included the conventional source degeneration input matching and an inductor shunted in a shunted resistor in RF signal path. The shunted resistor in RF path saved the three inductors used for design of Butterworth filter required earlier for the design in specified application. Table 3 shows the summary of different matching techniques for LNA's.

Table 2.3: Summary of Different Matching Techniques for LNA's

Parameters	[11]	[14]	[17]	[18]	[24]
Year	1997	2004	2007	2008	2007
Technology(um)	0.6	0.18	0.18	0.18	0.13

S_{11}(dB)		-10	-10.1	-6.8	-44
S_{22}(dB)		-7	-9.76	-9.5	-12

2.2.4 Low Noise Techniques for LNAs

Derek K. Shaeffer et al. [11], had discussed the different matching topologies at the input. It includes resistive termination, $1/g_m$ termination, shunt-series feedback, inductive degeneration. For designing they used inductive degeneration because of its advantage of providing low noise figure, high linearity, and high gain.

Michael T. Reiha et al. [24], presents the reactive (negative) feedback for design of low noise amplifier, reactive feedback reduces the noise figure by reducing the input insertion loss, flat group delay and lowering input referred noise.

Andries J. Scholten et al. [25], provided the noise modelling for RF CMOS circuits that included effect of drain current noise and gate noise for short channel MOSFETs. The results was modelled with a non-quasi- static RF model, based on channel segmentation, which is capable of predicting both drain and gate current noise accurately. Two additional noise mechanisms: avalanche noise associated with the avalanche current from drain to bulk and shot noise in the direct-tunnelling gate leakage current is also discussed.

Xiao-dong Wang et al. [26], added the capacitor between the gate and the source of the input MOSFET in cascode low noise inductive degeneration topology for reducing the noise figure in amplifiers.

Jenn-Tzer Yang et al. [17], used high-Q active inductor and differential configuration for lowering the noise figure. Table 4 shows the summary of low noise techniques for LNA's.

Table 2.4: Summary of Low Noise Techniques for LNA's

Parameters	**[11]**	**[24]**	**[26]**	**[17]**
Year	1997	2007	2008	2007
Technology(um)	0.18	0.13	0.18	0.18
NF(dB)	3.5	.43	.655	0.55 o 0.758

2.3 Problem Definitions

Design of Low Noise Amplifier for wireless communication with frequency range 2.4 GHz and some specific target has to be achieving i.e.

(i) Gain should be greater than 15dB.

(ii) Noise Figure should be lower than 2.0dB.

(iii) Stability factor must be greater than 1.

(iv) Power consumption should be low.

Chapter 3

Basic Parameters of LNA Design

3.1 Two Port Network

The abstraction of the analogue block that is to be designed into a two port network is always useful in designing. So the characteristics and parameters of two port representation will be discussed. In a two port network, two port and four terminals are used to represent the characteristics of the circuit, especially in terms of current and voltage relations. The condition for any particular two terminals to be considered as a port is that current entering through one terminal must be equal to the current leaving through other terminal. And each port, two variables will be there out of them one will be independent and one will be dependent. At low frequency the two variables are voltage and current and the common two port representation are impedance matrix (Z parameter) and admittance matrix (Y parameter).

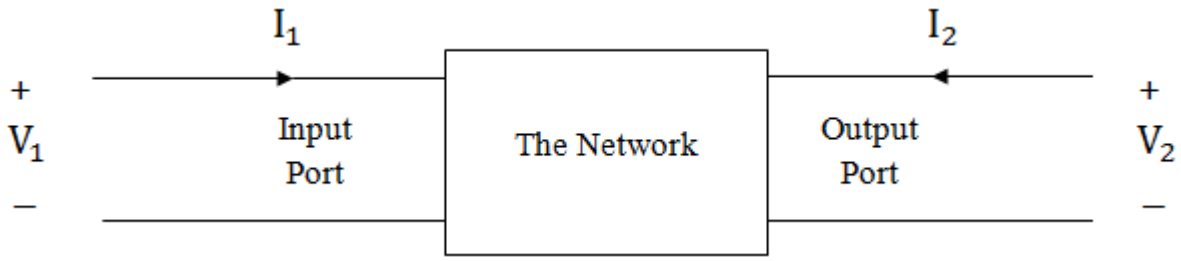


Figure 3.1: Two port network representation

The above figure shows a typical 2-port network, the impedance and admittance matrix are defined as shown in equations (3.1).and (3.2).

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} z_{11} & z_{21} \\ z_{21} & z_{22} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \tag{3.1}$$

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{21} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \tag{3.2}$$

But it is to be noted that the concept of Y and Z parameters are useful only at low frequency because at low frequency these parameters can be determined by applying either current or voltage at one port and measuring other variable by shorting and opening other port respectively, but at

very high frequency it will be very difficult to open or short any port because it needs a broadband match at high frequency and also an active two port network might oscillate if one of its port is open or short circuited. That is why a new parameter has to be defined at RF, this parameter is called scattering parameter.

3.1.1 Scattering Parameters

Since the main problem with RF was that one has to rely on open and short circuiting the other port if one has to define Y and Z parameters for RF circuits therefore scattering parameter has the advantage that they can be measured by matching source and load impedance to the reference impedance. To represent a two-port network at microwave frequencies, scattering parameters(S - parameters) can be used. S-parameters themselves (S_{11}, S_{12}, S_{21}, and S_{22}) represent reflection and transmission coefficients of the two-port under certain "matched" conditions. S_{11} is the reflection coefficient and S_{21} is the transmission coefficient at port 1 when port 2 is terminated in a load whose impedance is equal to that of the transmission line characteristic impedance. Likewise S_{22} is the reflection coefficient and S_{12} is the transmission coefficient at port 2 when port 1 is terminated in a matched load. The S parameter representation for two port network is as shown in Figure (3.2).

Figure 3.2: Two port network showing incident and reflected wave

Here in the above figure a_1 is the normalized incident wave at port and b_1 is the normalized reflected wave at the same port, v_1 and i_1 are voltage at port 1 and current entering into port 1. And the a_1, b_1, the terminal current and terminal voltage relation is expressed in Equations (3.3) and (3.4),

$$a_i = \frac{v_i + z_0 i_i}{2\sqrt{z_0}} \tag{3.3}$$

$$b_i = \frac{v_i - z_0 i_i}{2\sqrt{z_0}} \tag{3.4}$$

Here Z_0 is the reference impedance and it is taken as 50 Ω for all practical application. The overall scattering parameter in the matrix form can expressed as shown in Equation (3.5),

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} s_{11} & s_{12} \\ s_{21} & s_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{3.5}$$

But it is to be noted that the concept of Y and Z parameters are useful only at low frequency because at low frequency these parameters can be determined by applying either current or voltage at one port and measuring other variable by shorting and opening other port respectively, but at very high frequency it will be very difficult to open or short any port because it needs a broadband match at high frequency and also an active two port network might oscillate if one of its port is open or short circuited. That is why a new parameter has to be defined at RF, this parameter is called scattering parameter.

By expanding the scattering matrix the value of S_{11}, S_{12}, S_{21} and S_{22} can be expressed as shown below:

$$s_{11} = \frac{b_1}{a_1} \tag{3.6}$$

$$s_{12} = \frac{b_1}{a_2} \tag{3.7}$$

$$s_{21} = \frac{b_2}{a_1} \tag{3.8}$$

$$s_{22} = \frac{b_2}{a_2} \tag{3.9}$$

S_{11} is input reflection coefficient, S_{12} is reverse transmission coefficient, S_{21} is forward transmission coefficient, S_{22} output reflection coefficient. Clearly S_{11} is the ratio of reflected wave to the incident wave at port 1 when port 2 is perfectly matched .Perfectly matched means the load impedance is equal to the value of characteristic impedance. Similarly S_{21} is the ratio of reflected wave at port 2 to the incident wave at port 1 when port 2 is properly matched, in other way it can be said that the ratio of value of voltage received at port 2 to the voltage on port 1 is S_{21}, so it is the Gain of the circuit.

3.2 Gain of Two Port Networks

For RF circuits designers prefer to express Gain in term of power, for any circuit the purpose is to maximize Gain and in order to get maximum gain the most important concept is that there should not be any power reflection means to say that all incident power should be applied to the circuit. The basic principle of this concept is based on maximum power transfer theorem, so it needs to be explained.

3.2.1 Maximum Power Transfer Theorem

It is known that in order to the maximum power delivered by source going into the load the load impedance should be equal to the source impedance i.e. $R_s = R_L$. For the case of complex load it can be explained as follows –

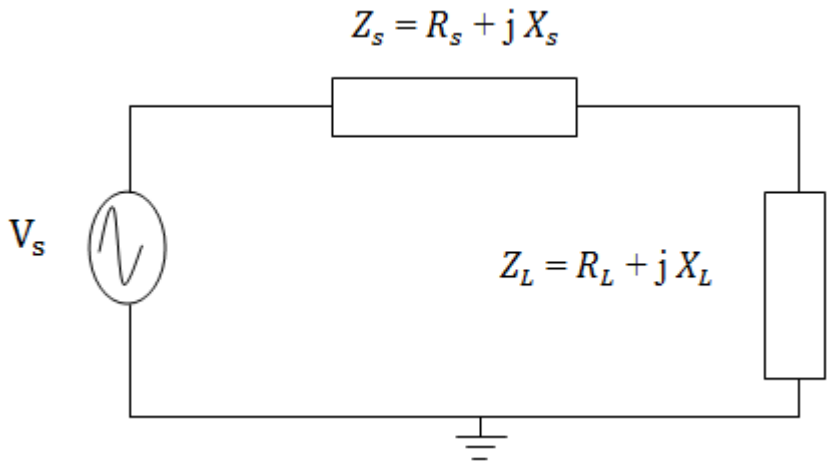


Figure 3.3: Source having complex impedance connected with complex load

From the above Figure (3.3), power delivered to the load RL is given as-

$$P_L = \frac{|V_{RL}|^2}{R_L} = \frac{R_L |V_S|^2}{|Z_L + Z_S|^2} \tag{3.10}$$

Now separating the real and imaginary part of Equation (3.10) we have

$$P_L = \frac{|V_{RL}|^2}{R_L} = \frac{R_L |V_S|^2}{(R_L + R_S)^2 + (X_L + X_S)^2} \tag{3.11}$$

Now by differentiating the above equation with respect to X_s and R_s and equating to zero, the condition for maximum power transfer can be achieved. The condition for maximum power transfer is R_L should be equal to R_s and X_L+X_s should be equal to zero. In other words it can be said that for

maximum power transfer the real impedance of load should be equal to the real impedance of the source and summation of imaginary part load impedance and source impedance must be zero. So for maximum power transfer the load impedance Z_L should be the complex conjugate of source impedance Z_s. Also it is to be noted that even in case of maximum power source will deliver only half of the available power to the load.

3.2.2 Different Gain Expression

The gain of the device is its ability to amplify the amplitude or the power of the input signal. It is defined as the ratio of the output to the input signal and is often referred to in terms of decibels.

$$Voltage\ Gain = 20\log\frac{v_{out}}{v_{in}}$$

Power gain is generally defined as the ratio of the power actually delivered to the load to the power actually delivered by the source. Three power gains are commonly used in LNA design.

(1) G_T, transducer power gain
(2) G_P, operating power gain
(3) G_A, available power gain
Besides these three gain definitions, there are three additional gain definitions we can use to evaluate the LNA design.

- G_{umx}, maximum unilateral transducer power gain
- G_{max}, maximum transducer power gain
- G_{msg}, maximum stability gain

Besides these six gain definitions, there are two gain circles that are helpful to the design of input and output matching networks.

- GPC, power gain circle
- GAC, available gain circle

(1)Transducer Power Gain

Transducer power gain, GT is defined as the ratio between the power delivered to the load and the power available from the source [27].

$$G_T = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2}|S_{21}|^2\frac{1-|\Gamma_L|^2}{|1-\Gamma_{out}\Gamma_L|^2} \qquad (3.12)$$

The transducer gain expressions are too complex for manual design. To effect an approximate gain solution, let us ignore the feedback, that is assume that $S_{12} = 0$. If an amplifier has no feedback, signals pass one way through it. Accordingly this is called unilateral gain. If $S_{12} = 0$, then $\Gamma_{in} = S_{11}$ and $\Gamma_{out} = S_{22}$ and transducer gain becomes the unilateral gain.

(2) Operating Power Gain

Operating power gain, G_P is defined as the ratio between the power delivered to the load and the power input to the network.

$$G_A = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2} \; |S_{21}|^2 \frac{1}{1-|\Gamma_{out}|^2} \tag{3.13}$$

The LNA scattering matrix is normalized in terms of the source and load resistance in Equation (3.14).

$$\Gamma_s = \Gamma_L = 0 \tag{3.14}$$

Thus, the input and output reflection coefficient are simply expressed in terms of Equation (3.15) and (3.16)

$$\Gamma_{in} = S_{11} \tag{3.15}$$

$$\Gamma_{out} = S_{22} \tag{3.16}$$

From these equations,

$$G_P = \frac{1}{1-|S_{11}|^2} \; |S_{21}|^2 \tag{3.17}$$

(3) Available Power Gain

Available power gain, G_A is defined as the ratio between the power available from the network and the power available from the source [27].

$$G_A = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2} \; |S_{21}|^2 \frac{1}{1-|\Gamma_{out}|^2} \tag{3.18}$$

From Equations 3.15 and 3.16

$$G_A = \; |S_{21}|^2 \frac{1}{1-|S_{22}|^2} \tag{3.19}$$

The power available from the source is greater than the power input to the LNA network, $G_P > G_T$. The closer the two gains are the better the input matching. Similarly, because the power available from the LNA network is greater than the power delivered to the load, $G_A > G_T$.

(4) Maximum Unilateral Transducer Power Gain

Maximum Unilateral transducer power gain G_{umx} is the transducer power gain when we assume that the reverse coupling of the LNA, S_{12} is zero, and the source and load impedances are conjugate matched to the LNA. That is $\Gamma_S = S_{11}$ and $\Gamma_L = S_{22}$. If $S_{12} = 0$ and the input and output reflection coefficient are $\Gamma_{in} = S_{11}$ and $\Gamma_{out} = S_{22}$. Thus from Equation 3.13 we get Equation 3.20.

$$G_{umx} = \frac{1}{\left|1-|S_{11}|^2\right|} \; |S_{21}|^2 \frac{1}{\left|1-|S_{22}|^2\right|} \tag{3.20}$$

(5) Maximum Transducer Power Gain

Maximum transducer power gain, G_{max} is the simultaneous conjugate matching power gain when both the input and output are conjugate matched. That is $\Gamma_S = S_{11}$ and $\Gamma_L = S_{22}$. When the reverse coupling, S_{12} is small, G_{umx} is close to G_{max}.

$$G_{\max} = \frac{|S_{21}|}{|S_{12}|}(\mathrm{k} - \sqrt{k^2 - 1}) \tag{3.21}$$

Where, K is stability factor

(6) Maximum Stability Gain

Maximum Stability gain, G_{msg} is the maximum of G_{max} when the stability condition K>1 is still satisfied.

$$G_{msg} = \frac{|S_{21}|}{|S_{12}|} \tag{3.22}$$

(7) Power Gain Circle

Power gain circle in short form is *GPC*. From Equation 3.13, G_p, is solely a function of the load reflection Γ_L. Thus we can draw power gain contours on the smith chart of Γ_L. The location for the peak of the contour corresponds to Γ_L producing the maximum G_P. We can move the peak location by changing the design of the output matching network. The best location for the contour peak is at the centre of the smith chart that is where,

$$\Gamma_L = 0$$

(8) Available Gain Circle

Available gain circle in short form is *GAC*. From Equation 3.18, we can see that G_A is solely a function of the source reflection Γ_S. Thus we can draw available gain contours on the smith chart of Γ_S. The location for the peak of the contour corresponds to Γ_S producing the maximum G_A. we can move the peak location by changing the design of the input matching network. The best location for the contour peak is at the center of the smith chart that is where $\Gamma_S = 0$.

3.3 Stability

In the presence of feedback paths from the output to input, the circuits might become unstable for certain combination of source and load impedances. An LNA design that is normally stable might oscillate at the extremes of the manufacturing or voltage variations, and perhaps at unexpectedly high or low frequencies. The stability factor is given as in Equation 3.23

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{3.23}$$

Where

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| \tag{3.24}$$

Where K > 1 and Δ < 1, the circuit is unconditionally stable. That is, the circuit does not oscillate with any combination of source and load impedance. We should perform the stability evaluation for the S parameters over a wide frequency range to ensure that K remains greater than one at all frequencies. As the coupling (S_{12}) decrease, which is as reverse isolation increase, stability improves. Techniques such as resistive loading and neutralization are used to improve stability for LNA. Equation 3.23 is valid for small signal stability. If the circuit is unconditionally stable under small signal conditions, the circuit is less likely to be unstable when the input signal is large. Aside from the two metrics K and Δ, the source and load stability circles cab be used to check LNA stability.

3.4 Noise

Noise is a random process means the value of the noise cannot be predicted at any time if the past value is known. Instantaneous value of noise cannot be predicted, a statistical model provides knowledge about some other important properties of the noise i.e. average power of noise that will be predictable.

3.4.1 Noise in MOSFET

Design of LNA using CMOS will be discussed, therefore we will discuss the main source of noise and there expression in order to be able to express them both qualitatively and quantitively in the circuits. Several kinds of noise are discussed below:

(i) Thermal Noise

It is the random motion of electrons in a conductor introduces fluctuations in the voltage measured across the conductor even if the average current is zero. The thermal noise is proportional to the absolute temperature.

(ii) Flicker Noise

The interface between the gate oxide and the silicon substrate in a MOSFET entails an interesting phenomenon. Since silicon crystal reaches an end at this interface, many "dangling" bonds appear, giving raise to extra energy states. As charge carriers move at the interface, some are randomly trapped and later released by such energy states, introducing "flicker noise" in the drain current. Since LNA design for radio frequency and flicker noise is inversely proportional to frequency so it will be ignored. Noise due to gate resistance- the charge present in the channel fluctuates and it is capacitive coupled to gate and hence noise is produced and given as [28].

$$\overline{\hat{i}_{ng}^{\,2}} \Big/ \Delta f = 4kTg_g\delta \tag{3.25}$$

Channel of MOSFET generates thermal noise and is given as-

$$\overline{\hat{i}_{ng}^{\,2}} \Big/ \Delta f = 4kTg_{d_o}\delta \tag{3.26}$$

Where g_g is the gate conductance, g_{do} is open channel conductance [26].

3.4.1.1 Input equivalent noise source

In order to able to explain the behaviour of the circuit a noisy circuit is expressed by a noiseless circuit and two sources at input.

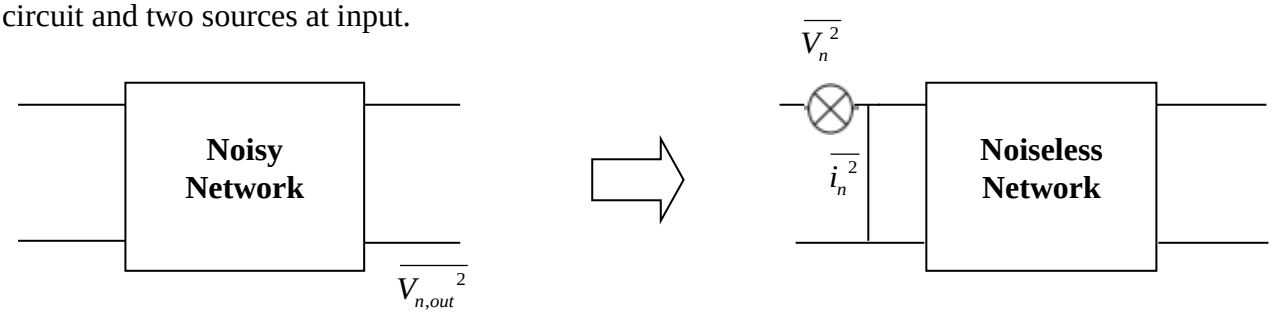


Figure3.4: Input equivalent noise source

Two noise sources one current and one voltage source is necessary because if Rs is zero(short) the noise current will flow out and only noise voltage will remain and similarly if Rs is infinite(open) only noise current will affect the circuit.

3.4.1.2 Input equivalent noise source for MOS

As shown in figure 3.5 input equivalents for noise source-

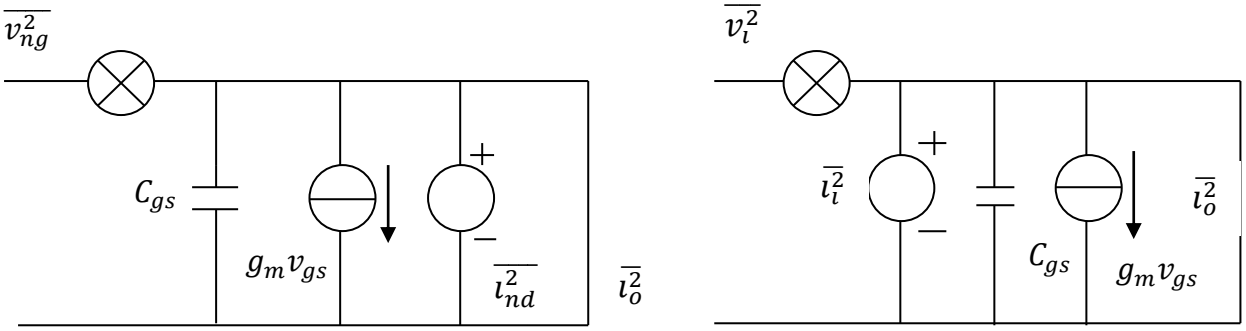


Figure 3.5: Input equivalent noise sources for MOS

By short circuiting the output of the actual circuit and equivalent circuit the relation between the equivalent current and voltage source with drain and gate noise current will be determined [27].

Case 1: when input is short circuited-

$$i_0 = g_m V_{ng} + i_{nd} \tag{3.27}$$

It should be equal to the value of io from equivalent circuit i.e.

$$i_0 = g_m V_i \tag{3.28}$$

By equating the above two equations, Equation (3.29) is obtained.

$$V_i g_m = V_{ng} g_m + i_{nd} \tag{3.29}$$

Therefore it can be written as-

$$\overline{V_i^2} = \overline{V_{ng}{}^2} + \overline{i_{nd}{}^2}\left(\frac{1}{g_m}\right)^2 \tag{3.30}$$

Case 2: when input is open circuited-

$$i_o = i_{nd} \tag{3.31}$$

And it should be equal to

$$i_0 = \left(\frac{i_i}{w_c g_s}\right) g_m \tag{3.32}$$

From the above two equations, it can also be written as-

$$\overline{\hat{i}_i^{\,2}} = \left(\frac{w_c g_s}{g_m}\right)^2 \overline{\hat{i}_{nd}^{\,2}} \tag{3.33}$$

So from Equations (3.30) and (3.33) equivalent noise source are defined, and it is to be noted that both the noise sources are correlated.

3.4.1.3 Absolute value of equivalent noise source

The correlation coefficient of the two thermal noise source is given by Equation (3.34)

$$c = \frac{\overline{\hat{i}_{ng}.i_{nd}^{\,*}}}{\sqrt{\overline{\hat{i}_{ng}^{\,2}}}\sqrt{\overline{\hat{i}_{nd}^{\,2}}}} \tag{3.34}$$

And value of c for long channel is 0.395j [5].

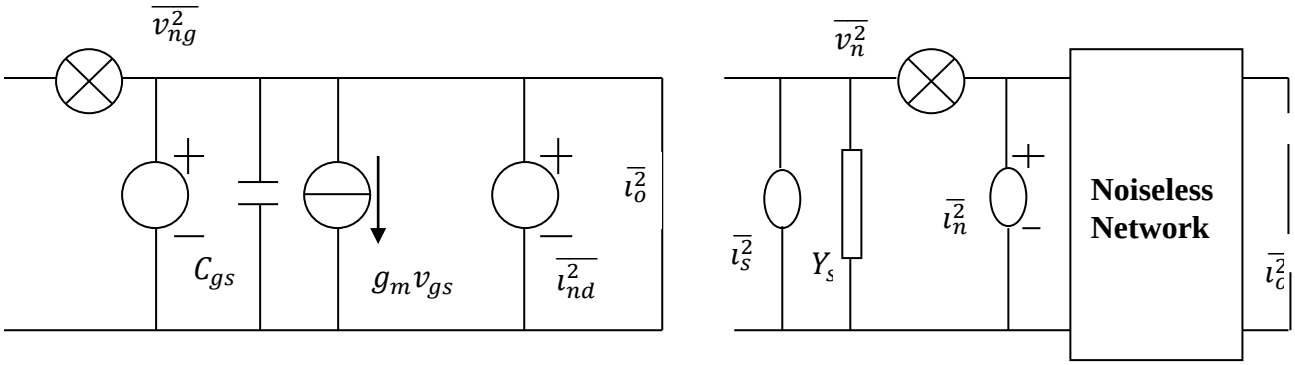


Figure 3.6: Noisy MOS replaced by noiseless source with input noise

Now again shorting the input and forcing equal current io in both the circuits, therefore

$$\overline{V_n^{\,2}} = \frac{\overline{\hat{i}_{nd}^{\,2}}}{g_m^{\,2}} = \frac{4kT\gamma g_{do}\Delta f}{g_m^{\,2}} \tag{3.35}$$

It is clear from the above equation that gate thermal noise does not contribute to this. The noise generated in Equation (3.35) can be expressed by the noise generated by a resistor of value R_n therefore

$$\overline{V_n^{\,2}} = 4KT\Delta f R_n \tag{3.36}$$

Where

$$R_n = \frac{\gamma g_{do}}{g_m^{\,2}} \tag{3.37}$$

$\overline{\hat{i}_{ng}^{\,2}}$ Will have contribution due to gate thermal noise $\overline{\hat{i}_{ng}^{\,2}}$ $ing2$ and drain thermal noise $\overline{\hat{i}_{ng}^{\,2}}$

$$\overline{i_{nl}^{\,2}} = \overline{\hat{i}_{nd}^{\,2}} \frac{\left(\omega c_{gs}^{\,2}\right)}{g_m^{\,2}} = \frac{4kT\gamma g_{do}\left(\omega c_{gs}^{\,2}\right)\Delta f}{g_m^{\,2}} \tag{3.38}$$

From Equation 3.35

$$\overline{i_{nl}^{\,2}} = \overline{v_{nl}^{\,2}}\left(\omega c_{gs}\right) \tag{3.39}$$

$\overline{i_{ng}^{\,2}}$ has two components one correlated with $\overline{v_n^{\,2}}$ and other not correlated with it

$$\overline{i_{ng}^{\,2}} = \overline{\left(i_{ngc} + i_{ngu}\right)^2} = 4KT\delta g_g \Delta f \left|c\right|^2 + 4KT\delta g_g \Delta f \left(1 - \left|c\right|^2\right) \tag{3.40}$$

Therefore total equivalent noise current can be written into two parts-

(i) Uncorrelated term

$$\overline{\hat{i}_{nu}^{\,2}} = \overline{\hat{i}_{ngu}^{\,2}} \tag{3.41}$$

It can be represented by noise generated by Yu and value is given by-

$$Y_u = G_u = \frac{\overline{\hat{i}_{nu}^{\,2}}}{4KT\Delta f} = \delta g_g \left(1 - \left|c\right|^2\right) \tag{3.42}$$

So

$$Y_u = G_u = \frac{\delta\omega^2 c_{gs}^{\,2} g_g \left(1 - \left|c\right|^2\right)}{5g_{do}} \tag{3.43}$$

(ii) Correlated term

$$\overline{\hat{i}_{nc}^{\,2}} = \overline{\hat{i}_{ngc}^{\,2}} \tag{3.44}$$

It can be represented by noise generated by Yc and is given by the following equation.

$$Y_c = \frac{i_{nc}}{V_n} = \frac{g_m i_{nc}}{i_{nd}} + j\omega c_{gs} \tag{3.45}$$

Therefore, the model of MOS transistor as a noiseless system with two input noise sources is obtained and the noise sources can be characterized completely by Y_u and Y_c.

3.5 Noise Figure

Noise factor is defined as the ratio of signal to noise ratio at input to signal to noise ratio at output and also defined as the ratio of total output noise power to the output noise power due to source alone[29]. Decibel representation of noise factor is known as noise figure. Generally signal to noise ratio is the parameter that is being used for analog circuits but in RF design since the ultimate aim is to maximize the SNR therefore noise figure is defined [29].

$$\text{Noise factor} = \frac{\text{SNRin}}{\text{SNRout}}$$

And

$$\text{Noise figure} = 10\log_{10}(\text{Noise factor})$$

Now the expression for the noise factor of MOS transistor will be derived and also the condition for the noise factor to be minimum will be determined.

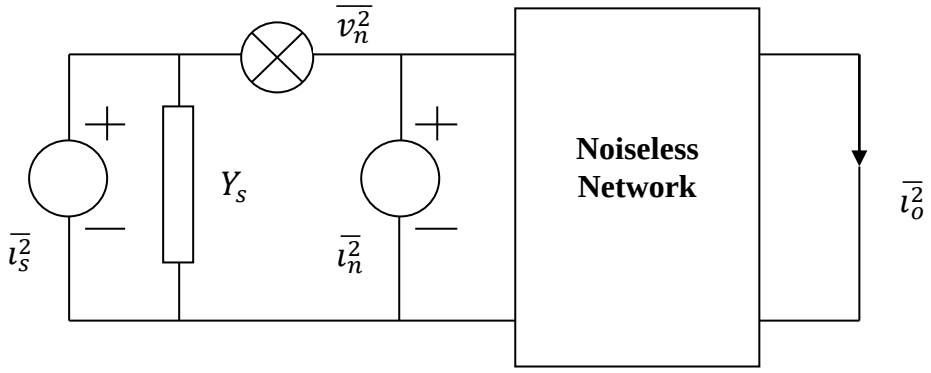


Figure 3.7: Noiseless network with equivalent noise current and voltage [30]

From the above circuit noise figure is-

$$F = \frac{\overline{\hat{\imath}_s^{\,2}} + \overline{\left(\hat{\imath}_n + Y_S V_n\right)\left(i_n^* + Y_s^* V_n^*\right)}}{\overline{\hat{\imath}_n^2}} \tag{3.46}$$

It is known that the equivalent input current in is composed of two parts one is correlated with V_n and other is correlated with it. So considering correlated and uncorrelated terms-

$$i_n = i_{nu} + i_{nc} = i_{nu} + Y_c V_n \tag{3.47}$$

Therefore,

$$F = \frac{\overline{\hat{\imath}_s^2} + \overline{\left(i_{nu} + (Y_c + Y_s)V_n\left(\hat{\imath}^*{}_{nu} + (\mathrm{Y}_c^* + \mathrm{Y}_s^*)V_n^*\right)\right.}}{\hat{\imath}_s^2} \tag{3.48}$$

$$F = \frac{\overline{\hat{\imath}_s^2} + \overline{\left(i_{nu} + (Y_c + Y_s)V_n\left(\hat{\imath}^*{}_{nu} + (\mathrm{Y}_c^* + \mathrm{Y}_s^*)V_n^*\right)\right.}}{\hat{\imath}_s^2} \tag{3.49}$$

And using above equation 3.49,

$$F = \frac{G_u + \left[\left(G_c + G_s\right)^2 + \left(B_c + B_s\right)^2\right]R_n}{Gs} \tag{3.50}$$

Here G_c+jB_c is used for Y_c and G_s+jB_s for G_s.

For MOS G_c= 0 and above equation can be written as-

$$G_u = \frac{\delta c_{gs}{}^2 \omega^2 \left(1 - |c|^2\right)}{5g_{do}} \quad , \qquad B_c = \omega c_{gs}\left(1 + \alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)$$

And $$R_n = \frac{\gamma}{\alpha g_m}$$

These values are putting in Equation 3.50

$$F = 1 + \frac{\frac{\delta\alpha\omega^2 c_{gs}\left(1-|c|^2\right)}{5g_m} + \left(\omega c_{gs}\left(1+\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)+B_s\right)^2 \frac{\gamma}{\alpha g_m}}{G_s} \tag{3.51}$$

Now in order to optimize this noise figure, Equation 3.50 will be differentiated with respect to B_s and G_s, because these are the values which are coming from source and these values will have to be optimized in order to get minimum noise figure. So by taking differentiation with respect to B_s we have-

$$B_{s\_opt} = -B_c = -\omega c_{gs}\left(1+\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right) \tag{3.52}$$

Also by differentiating with respect to G_s-

$$G_{s\_opt} = \sqrt{\frac{G_u}{R_n}} = \alpha\omega c_{gs}\left(\sqrt{\frac{\delta\left(1-|c|^2\right)}{5\gamma}}\right) \tag{3.53}$$

By using Equations 3.52 and 3.53

$$F_{\min} = 1 + \frac{2\omega}{\sqrt{5}w_T}\sqrt{\gamma\delta\left(1-|c|^2\right)} \tag{3.54}$$

This is the expression for minimum noise figure.

Also from the maximum power transfer theorem the condition for maximum power transfer and the condition for minimum noise figure cannot be satisfied simultaneously. Therefore one will have to always look for the trade off in between noise and power gain.

3.6 Noise Optimization Methods

In low noise amplifier design, determination of the minimum noise figure is a common and Well-understood procedure. Typically, a small-signal model of the amplifier is assumed, an expression for F is formed, and differentiation leads to the unique conditions for optimized noise performance [30]. In the noise optimization techniques we seek the conditions that guarantee optimized noise performance for a specified fixed design parameter, such as gain or power consumption, under the condition of perfect input matching. Now, we fix the necessary design criteria and determine the appropriate small-signal model through the optimization procedure. Because the architecture

permits selection of Q_L and L_S independently, so we can optimize the noise performance that coincides with the input match. There are two approaches for the optimization of noise figure. The first assumes a fixed transconductance, G_m, for the amplifier. The second assumes fixed power consumption. We know the equation of noise figure is [31].

$$F = 1 + \frac{R_l}{R_s} + \frac{R_g}{R_s} + \gamma\chi g_{do} R \left(\frac{\omega}{\omega_T} \right)^2_s \tag{3.55}$$

To illustrate these approaches the expression for the F in Equation 3.55 cab be recast to make its dependence on power dissipation. From equation 3.56 it is clear that condition for constant G_m is equivalent to the condition of constantω_T.

$$G_m = g_{m1} Q_{in} = \frac{g_{m1}}{\omega c_{gs} \left(R_s + w_T L_s \right)} = \frac{\omega_T}{\omega R_s \left(1 + \frac{w_T Ls}{R_s} \right)} = \frac{\omega_T}{2wR_s} \tag{3.56}$$

To maintain a fixedω_T, we need only fix the value of ρ. Hence, we will reformulate F in terms of P_D and ρ to facilitate both optimizations. The equation of F in terms of P_D and ρ is given below [31].

$$F = 1 + \frac{\gamma\omega L}{3v_{sat}} P\left(\rho, \mathrm{P}_D\right) \tag{3.57}$$

In this equation we have neglected the contribution of the gate resistance and inductor losses to the noise factor. In the Equation 3.57 (ρ,), is a ratio of two sixth order polynomials of ρ given by

$$P(\rho, \mathrm{P}_D) = \frac{\frac{P_D}{P_0} P_1(\rho) + P_2(\rho) + \frac{P_0}{P_D} P_3(\rho)}{\rho^3 \left(1 + \frac{\rho}{2} \right)^2 (1 + \rho)} \tag{3.58}$$

Where,

$$P_1 = \left(1 + \rho\right)^2 + \frac{\delta}{5\gamma} \left(1 + \rho\right)^2 \left(1 + \frac{\rho}{2} \right)^2$$

$$P_2\left(\rho\right) = 2|c| \sqrt{\frac{\delta}{5\gamma}} \left(1 + \rho\right)^3 \left(1 + \frac{\rho}{2} \right)^2$$

$$P_2\left(\rho\right) = \frac{\delta}{5\gamma} \left(1 + \frac{\rho}{2} \right)^2 \rho^4$$

Because F is a function of two variables, one can define contours of constant noise figure in ρ and P_D. Equation (3.57) suggests that optimization of proceeds by minimizing with respect to one of its arguments, keeping the other one fixed.

3.6.1 Fixed G_M Optimization

To fix the value of the transconductance, Gm, we need only assign a constant value to ρ. We know,

$$\omega_T \approx \frac{g_m}{c_{gs}} = \frac{g_m}{\frac{2}{3} wLc_{ox}} = \frac{3}{2}\frac{\alpha\mu_{eff}V_{od}}{L^2} = \frac{3\alpha\rho v_{sat}}{L} \tag{3.59}$$

The appropriate value for G_m is easily determined by substituting Equation (3.59) into the expression for as found in Equation (3.56). The value of G_m which relates to ρ, is

$$G_m = \frac{2v_{sat}\rho\left(1+\frac{\rho}{2}\right)}{2\omega R_s L\left(1+\rho\right)^2} \tag{3.60}$$

Once ρ is determined, we can minimize the noise factor by taking-

$$\frac{\delta P\left(\rho, P_D\right)}{\delta P_D} = 0$$

Which, after some algebraic manipulations result in

$$P_{D,opt.G_m} = P_0\sqrt{\frac{P_3(\rho)}{P_1(\rho)}} = P_0\frac{\rho^2}{1+\rho}\left[1+\frac{5\gamma}{\delta\alpha^2}\right]^{\frac{1}{2}} \tag{3.61}$$

This expression gives the power dissipation which yields the best noise performance for a given G_m under the assumption of matched input impedance. We know Q_L is:

$$Q_L = \frac{P_0}{P_D}\frac{\rho^2}{1+\rho} \tag{3.62}$$

By comparing Equations (3.61) and (3.62), we see immediately that this optimum occurs when [32]

$$Q_L = Q_{L,\mathrm{opt},G_m} = \sqrt{1+\frac{5\gamma}{\delta\alpha^2}} \geq 1.18 \tag{3.63}$$

Hence, the best noise performance for a given transconductance is achieved at some specific input. Note that the value 1.87 is valid only for long-channel devices. For short-channel lengths, where α < 1, we can expect the optimum Q_L to be somewhat larger. By substituting (3.63) into (3.55), we determine that the minimum noise factor (neglecting inductor and gate losses) is

$$F_{\min,G_m} = 1+\sqrt{\frac{4}{5}\delta\gamma}\left(\frac{\omega}{\omega_T}\right)\left\{|c|+\sqrt{1+\frac{5\gamma}{\delta\alpha^2}}\right\} \geq 1+1.33\left(\frac{\omega}{\omega_T}\right) \tag{3.64}$$

The value 1.33 is only valid for long-channel devices; it may be three to four times larger in the presence of high electric fields.

3.6.2 Fixed P_D Optimization

An alternate method of optimization fixes the power dissipation and adjusts ρ to find the minimum noise factor. If we assume that α << 1, then P (ρ, P_D) can be simplified to:

$$P(\rho, P_D) \approx \frac{\frac{P_D}{P_0}\left(1+\frac{\delta}{5\gamma}\right)+2|C|\sqrt{\frac{\delta}{5\gamma}}\rho^2+\frac{P_0\delta}{P_D 5\gamma}\rho^4}{\rho^3} \tag{3.65}$$

This expression is minimized for a fixed PD when $\frac{\delta P(\rho, P_D)}{\delta\rho}=0$

The solution of this equation, under the assumption that α<<1

$$\rho_{opt,P_D}{}^2 = \frac{P_D}{P_0}|C|\sqrt{\frac{5\gamma}{\delta}}\left[1+\sqrt{1+\frac{3}{|C|^2}\left(1+\frac{\delta}{5\gamma}\right)}\right] \tag{3.66}$$

By comparing Equation (3.66) to Equation (3.65), it is clear that this value for ρ is equivalent to an optimum Q_L of

$$Q_{L,opt,P_D} \approx |C|\sqrt{\frac{5\gamma}{\delta}}\left[1+\sqrt{1+\frac{3}{|C|^2}\left(1+\frac{\delta}{5\gamma}\right)}\right] \tag{3.67}$$

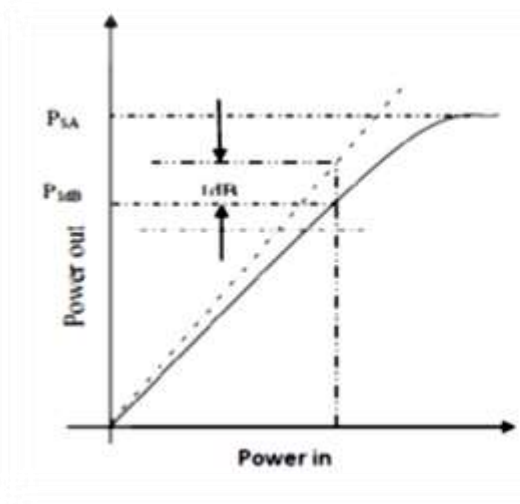
So, it is clear that the optimum Q_L for fixed power dissipation P_D is larger than the optimum Q_L for a fixed Gm. from these equations

$$F_{\min.P_D} \approx 1+2.4\frac{\gamma}{\alpha}\left(\frac{\omega}{\omega_T}\right) \geq 1+1.62\frac{\omega}{\omega_T} \tag{3.68}$$

Where the value of 1.62 is valid only in the long-channel limit; the value will be somewhat larger for short-channel devices in velocity saturation.

3.7 Linearity

The linearity of the LNA is another concern that must be taken into account. Linear operation is crucial, particularly when the input signal is weak with a strong interfering signal in close proximity. This is because in such a scenario there is a possibility for undesired inter modulation distortion such as blocking and cross modulation. Third-order intercept (IP3) and 1-dB compression point (P_{1dB}) are two measures of linearity. IP3 shows at what power level the third-order inter modulation product is equal to the power of the first-order output. IIP3 and OIP3 are the input power and output power respectively, that corresponds to IP3. P_{1dB} shows at what power level the output power drops 1 dB, as a consequence of non-linearity, relative the theoretical linear power gain [29].



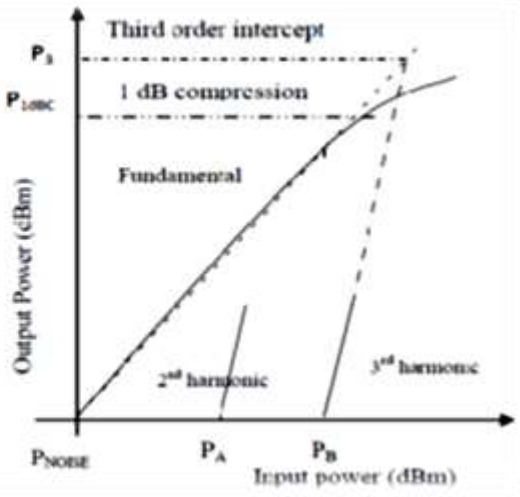


Figure 3.8: 1dB compression point

Figure 3.9: Third order intersect point

By knowing either IP3 or P1dB the other can be estimated with the following rule-of-thumb formula:

$$IP_3 = P_{1dB} + 10dB \tag{3.69}$$

Third-order intercept point is shown in Figure 3.9. Both measurements indicate an upper distortion limit for the tolerable input power, whereas the noise figure sets a lower limit. The ratio of the two determines the dynamic range of the amplifier [10].

3.8 Centre Frequency and Bandwidth

As the LNA will operate with input signals of a particular frequency band, it is desired to design it with a centre frequency and bandwidth accordingly. Looking at the transfer function of the LNA, the differential of the two points around the centre frequency f_o, where the power gain is halved, is the bandwidth, denoted Δf in Figure 3.10. Although the target bandwidth should be specified numerically, by naming convention there are two options: narrowband and wideband. And $\triangle f$ is called the bandwidth and it is difference between higher frequency component and lower frequency components and f_o is the operating frequency and this work operating frequency is 6GHz and bandwidth of system has to calculated by the simulation of circuit. We can also calculate the relative bandwidth that tells us system is wideband and narrow band.

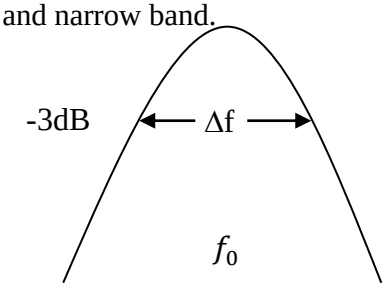


Figure 3.10: Illustration of centre frequency and bandwidth

Chapter 4

Different Topologies for LNA Design

4.1 Introduction

Typical heterodyne receiver architecture as shown in Figure 4.1 and it is clear from the above figure that the signal received from the antenna has to pass from the band select band pass filter and then it goes to the LNA. The reflection from LNA is never desired because it will affect the filter characteristic of the band pass filter preceding the LNA and hence the overall performance of receiver will be altered. Further for the signal that is being received by LNA, one has to ensure that maximum part of incoming signal is received by the LNA.

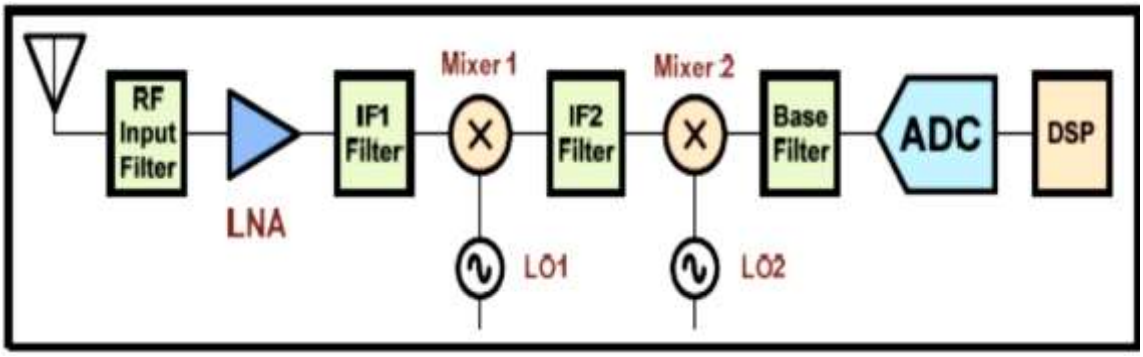


Figure 4.1: Basic heterodyne receiver architecture [36]

So the first stage of LNA will be the input matching stage which will insure that maximum signal is going into LNA for processing. And from above section it is clear that in order to get maximum power transfer theorem that is in for the signal received by the LNA to show minimum reflection the input impedance of the LNA must be complex conjugate of the source impedance. Here for simplicity it is assumed that source impedance is real and its value is 50Ω. Now it is also known that if a number of components are connected in cascade configuration than the equivalent noise figure of the chain will be-

$$F_{Tot} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + ... + \frac{F_n - 1}{G_1 G_2 ... G_{n-1}} \tag{4.1}$$

From eqn. (4.1) it is clear that the noise figure of the system mainly depends upon the noise figure of the first stage because it directly gets added to the noise figure of the system while the noise

figure of the system which comes after the first component gets divided by the gain of the preceding component and so on, so it is very important to ensure that the LNA is not adding much noise.

So from above discussion it is clear that mainly there are two conditions for LNA first is that the input impedance is matched with the source impedance and second condition is that noise figure of LNA should be minimum with high gain. Also from the above section it is clear that it is impossible to satisfy both the condition simultaneously and accurately, therefore one will have to go for trade off the respective stages of development of LNA will be discussed starting from the basic circuit of LNA possible. So that there are some topologies for LNA design are discuss below-

4.1.1 Resistive Matching

The following is the figure of the simple resistive type matching LNA circuit. As shown in the figure 4.2 the input impedance of MOSFET can be taken as infinity for particular frequency of interest so in order to get the matching R_{in} should be equal to R_s. so in the case V_{in} will be equal to half of the value of V_s. Further although it will be a broadband matching but it will show very poor performance because it can be seen that half of the signal power is already lost before going to the LNA and also this circuit is adding noise i.e. the thermal noise because of R_1 is being added to the input stage of LNA.

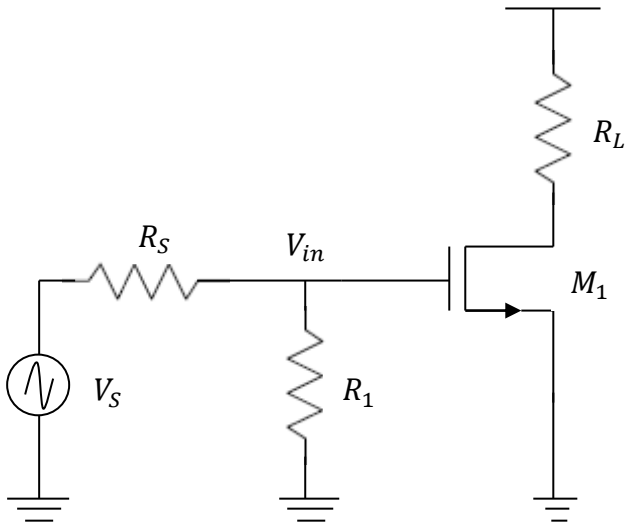


Figure 4.2: Resistive matching LNA [37]

Adding noise to the output stage of LNA will not be that dangerous because overall noise figure gets divided by the gain of preceding stages.

Noise figure of a circuit is given by following relation:

$$Noise\ Figure = \frac{total\ output\ noise}{total\ noise\ due\ to\ source}$$

Calculating noise figure from figure 4.2

Identifying the noise sources in the circuit

(i) Due to source resistance R_S

$$\overline{V_{nR_s}^{\ 2}} = 4KTBR \tag{4.2}$$

(ii) Due to termination resistance R_1

$$\overline{i_L^{\ 2}} = 4KTG_L B \tag{4.3}$$

(iii) Due to induced drain current

$$\overline{i_d^{\ 2}} = 4KT\left(\gamma g_{do}\right)B \tag{4.4}$$

In above equation γ is a constant that has value unity for linear region and reduced to 2/3 in saturation region and g_{do} is zero bias drain conductance.

(iv) Due to load resistance R_L

$$\overline{i_L^{\ 2}} = 4KTG_L B \tag{4.5}$$

G_L is the load transconductance.

So from equation 4.2 to 4.5 total output noise current is given by

$$\overline{i_0^{\ 2}} = \overline{i_d^{\ 2}} + \overline{i_L^{\ 2}} + \left(\overline{V_n^{\ 2}R_S} + \overline{V_n^{\ 2}R_1}\right)g_m^{\ 2} \tag{4.6}$$

So noise figure using equation 4.2 to 4.6 is given by-

$$F = 1 + \frac{R_1}{R_S} + \frac{\gamma}{g_m R_S} + \frac{G_L G_S}{g_m^{\ 2}} \tag{4.7}$$

From equation (4.7), it is observed that even if g_m becomes very large noise figure still will be dominated by termination resistance R_1. Hence, termination by resistor is not a good option as noise figure is very high. Clearly the value of noise figure that will be obtained from this configuration will be more than 3dB so this configuration is not practically applicable.

4.1.2 Shunt- Series Feedback Amplifier

Another possible configuration can be shunt feedback amplifier which is as shown below-

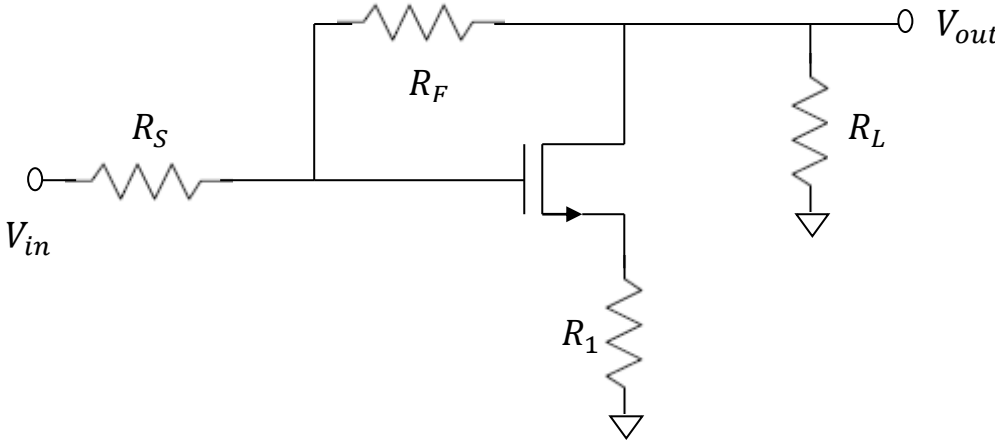


Figure 4.3: Shunt feedback amplifier [37]

It can be seen from this configuration that the main problem of previous configuration is not there i.e. half power was being attenuated before coming to the actual circuit which was responsible for the poor performance of resistive type matching circuit. It can be shown that the value of noise figure for this configuration can be represented as Equation (4.8).

$$F = 1 + \frac{R_S}{R_F}\left(1 + \frac{1}{g_m R_S}\right)^2 + \frac{\gamma}{g_m R_S} \tag{4.8}$$

It is clear from the above equation that in order to get minimum noise figure $g_m R_s$ should be more and R_F should be more, but the main problem is R_F induces noise so the both conditions contradicts each other. However the performance of this topology is better than the common source topology.

4.1.3 Common Gate Amplifier

The common gate topology for low noise amplifier as shown in Figure 4.4, the noise figure of this configuration can be calculated by considering the effect of drain current. Since the drain current is injected into the input, it adds noise in the shunt with the input noise current.

By definition,

$$Noise\ Figure = \frac{total\ output\ noise}{total\ noise\ due\ to\ source} = \frac{\overline{\hat{\imath}_s^{\,2}} + \overline{\hat{\imath}_d^{\,2}}}{\overline{\hat{\imath}_s^{\,2}}}$$

$$F = 1 + \frac{4KT\gamma Bg_{do}}{4KTBG_S} \tag{4.9}$$

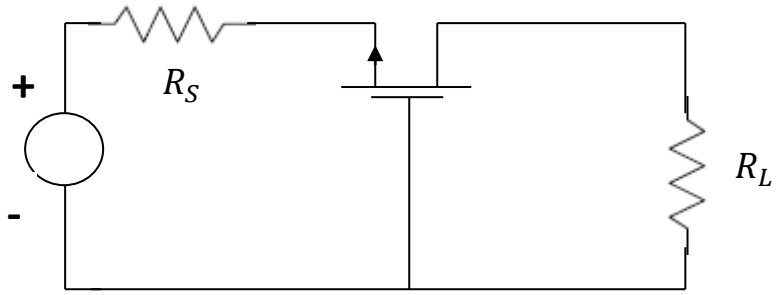


Figure 4.4: Common gate topology [37]

On solving Equation (4.8),

$$F = 1 + \frac{\gamma}{\alpha} \tag{4.10}$$

Since γ is 2/3 for saturation region and $\alpha$is unity. Putting these values in equation (4.10), noise figure is typically equal to 2.2dB and for short channel devices this value may increase to 3dB [37]. So ($1/g_m$) termination is not a good way for matching purposes.

4.1.4 Inductive Source Degeneration

Ideal inductor contributes no internal noise. However, real inductors suffer from both internal and external noise [37]. Inductive source degeneration offers the best noise match among the all techniques discussed earlier.

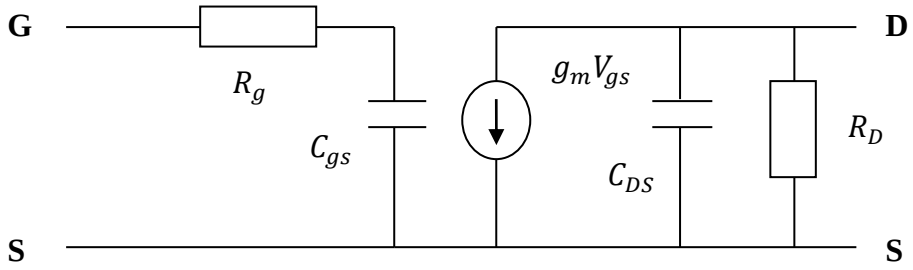


Figure 4.5: Equivalent model of MOSFET

Figure 4.5 shows the equivalent model of MOSFET consisting of voltage source in parallel with the load resistance R_D. As goal is to provide 50Ω proper termination but in reality the input of the device is reactive, with real and capacitive impedance. Capacitive reactance can be removed by adding inductive feedback to the source.

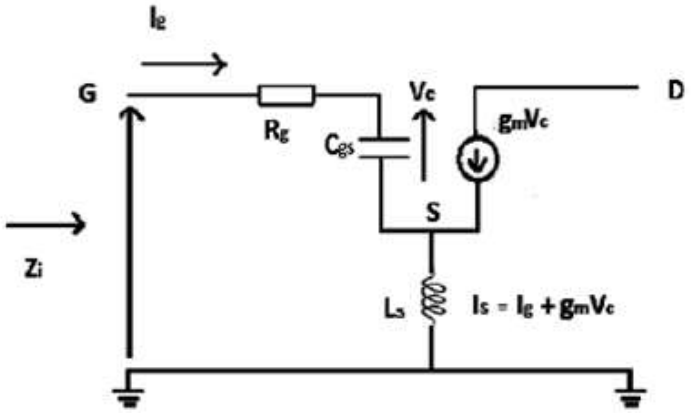


Figure 4.6: Equivalent MOSFET model with inductive source degeneration

Calculating input impedance from figure 4.6 by applying KVL at input, it comes out to be

$$Z_i = R_s + R_g + j(\mathrm{XL}_s - \mathrm{XC}_{gs}) \tag{4.11}$$

In Equation (4.11),

$$R_s = \frac{L_s g_m}{C_{gs}}$$

From equation (4.11), it can be observed that by adding series feedback, R_s +jXL_s term is added to original input impedance. Additionally, another inductor is added in series with the gate L_g that is selected to resonate with the C_{gs}. L_g is designed so that at resonant frequency it cancel out C_{gs} that is-

$$j\left(XL_S - XC_{gs}\right) = 0, \textit{ such that } Z_i = \frac{L_s g_m}{C_{gs}} = 50\Omega \tag{4.12}$$

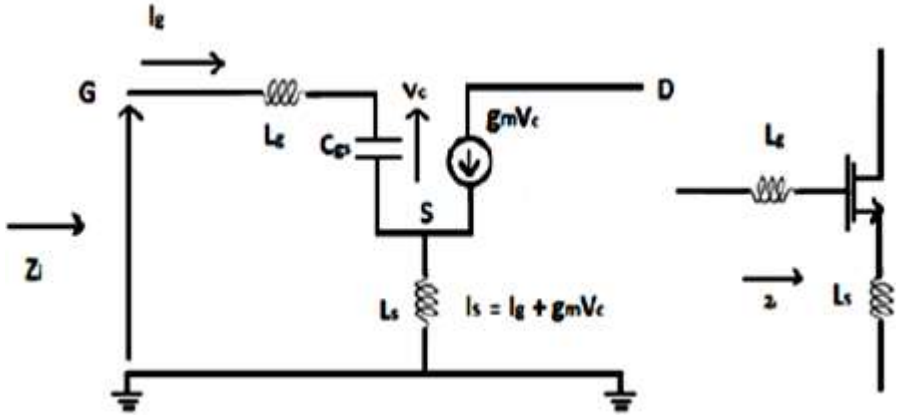


Figure 4.7: MOSFET model with inductive Gate and inductive source Degeneration

4.1.5 Cascode Inductive Source Degeneration

Miller Effect

An important phenomenon that occurs in many analog circuits is related to "Miller Effect". It states that figure 4.8 for any impedance can be converted to figure 4.9 provided that the impedance Z appears in parallel with the main signal.

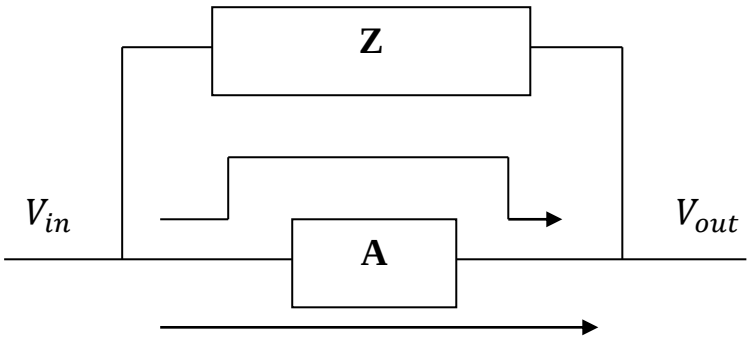


Figure 4.8: Typical Case for Miller's Theorem [38-39]

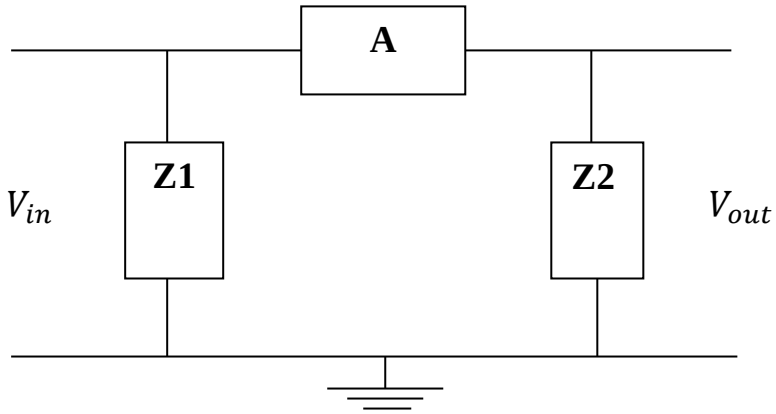


Figure 4.9: Application of Miller Theorem [38-39]

In figure 4.9

$$Z_1 = \frac{Z}{1-A} \tag{4.13}$$

And

$$Z_1 = \frac{Z}{1-A^{-1}} \tag{4.14}$$

Above Equation for Z_1 and Z_2 can be resistive, capacitive, or inductive and produces undesired results. For example if Z is capacitive in nature then at high frequencies it will limit the frequency

response both at the input and output. So, some means should be provided in order to suppress the miller effect.

Cascode Configuration

Cascode refers to the combination of common source and common gate. Main purpose of using the cascode configuration is to suppress the miller effect at the output and to increase the gain by increasing the output impedance of the circuit.

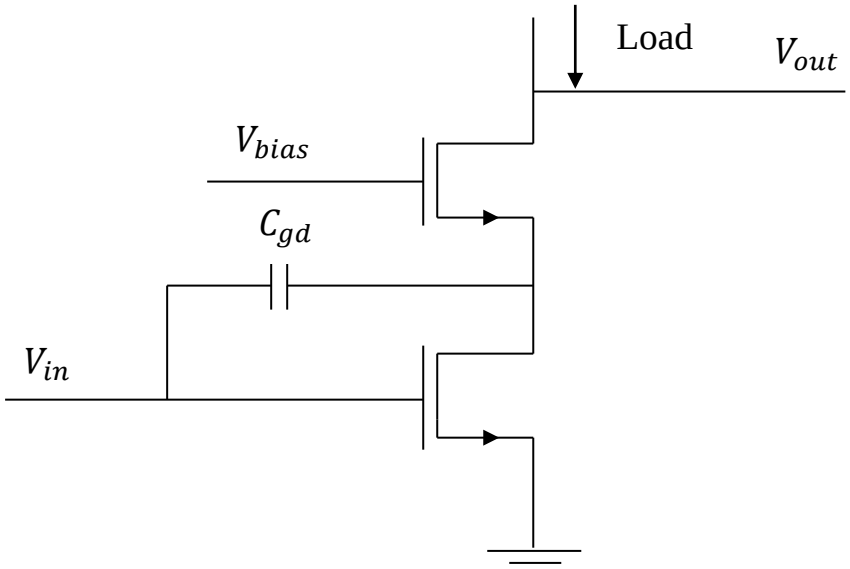


Figure 4.10: Cascode Configuration

From the figure 4.10 it is clear that the effect of miller capacitance C_{gd}has been suppressed at the output.

Inductive Load

Instead of using resistive load inductive load is used for design of the low noise amplifier because of following advantages:

- The inductor between the Cascode source and supply blocks any RF leaking to the supply rail and maybe varied in value to optimize the gain response of the LNA.
- To tune out the capacitances producing at the output, thereby providing band pass filtering.
- Compare to resistive load inductive load produces less noise

The advantages and disadvantages of different kinds of LNA topologies are shown in Table 4.1.

Table 4.1: Advantages and Disadvantages of LNA topologies

Type of Topology	Advantages	Disadvantages
Resistive termination common source	Broad band amplifier	Adding the noise from the resistor.
Common Gate	The input impedance is equal to 1/gm. It is practical to get 50 Ω	The impedance varies with the bias current.
Shunt series feedback common source	Broad band amplifier	Adding noise from resistor
Inductive degeneration common source	The source and gate inductors make the input impedance 50 Ω. Not adding the noise from the input.	The inductor is off chip at low frequency and low isolation.
Cascode inductor source degeneration	Isolation of input and output is good, higher gain, lower noise figure.	The inductor is off chip at low frequency.

As all the above topologies, inductive source degeneration configuration is best from other topologies. So we have chosen inductive source degeneration configuration, with inductive load it provides sufficient gain without adding significant noise and also a good property it provides better matching in comparison to other topologies.

Chapter 5

Design and Simulation

5.1 Introduction

In the designing of low noise amplifier, some basic aspect of low noise amplifier should be kept in mind. Since in low noise amplifier there is trade-off between many factors i.e. gains, noise figure, stability, power consumption, and nonlinearity etc. And depending on these factors we have previously discussed different topology of low noise amplifier design. In this work we have chosen inductive source degeneration topology because this provides some beneficial advantages over other topologies as discussed in chapter 4. Inductive source degeneration topology is one of the most useful configurations for low noise amplifier design; because common source configuration provides low noise and solved the stability related problem.

5.2 Step of LNA Design

Step of LNA design is describes the design flow of low noise amplifier. The design starts from some basic specification means some standard output values that is desired for any circuits design these specification are scattering parameters, Gain, Noise Figure, Stability, Power, linearity etc. and our aim, tends to achieve these specified values. Second step in the design is choice of technology so here; CMOS technology has chosen for this design. Third step is choice the topology, there are different types of topologies and among them we can use topology depending on our design. Fourth step is some basic calculation like device width, gate to source capacitance and other things after that we can do the biasing to set the operating point and last if there is some impedance mismatch so we have to do impedance matching by inserting a filter network.

5.3 Design Specifications

A Low Power High Gain LNA for 2.45 GHz operating frequency range by using 0.5um CMOS Technology, 0.5um is represents the length of device. That is the minimum length of device provided by the vender. CMOS Technology is used because of its several advantages such as low cost, low static power dissipation, low area, low noise and high dynamic range. If we goes to design any analog circuit it is mandatory to known the some design specification and that specification are

standard and our goal is to achieve the desirable result. Table 5.1 shows the target specification for LNA design.

Table 5.1: Target Specification

Parameter	Specification	Units
Frequency	2.40 to 2.85	GHz
Noise Figure	<2.5	dB
Gain	>10	dB
Power consumption	<50	mW
Source/load impedance	50	Ohms
Stability Factor	>1	
Supply Voltage	3.0	Volt

5.4 Selection of Appropriate Components

Because transistors, spiral inductors and capacitors are often used in LNA circuit, the accurate RF models are very important to predict the silicon performance of gigahertz circuits. The characteristic of transistor in low frequency is different from the one in high frequency. The parasitic effects of transistor should be considered in circuit design, which are not included in the low frequency circuit design. So the transistor model for low frequency design is quite different with the model for high frequency design. Moreover in high frequency, the inductance and Q value varies with the operating frequency and capacitor also has parasitic effects. Advanced Design System (ADS) of Agilent is used for the design of various topologies of LNA. So transistor, inductor and capacitor models should also be chosen carefully for correct design from the design library Advanced Design System (ADS) simulator. The ADS library is used for selecting other active and passive components.

5.4.1 Transistor RF Models

MOSFET models, especially the RF MOSFET models are required to predict the silicon performance accurately, such as sub-circuit short channel MOSFET models for RFIC designs. In the sub-circuit models, MOSFET is divided into two parts, an intrinsic part, and an extrinsic part.

The intrinsic part represents the main active part of the device, which can be any compact model, such as Berkeley Short-Channel IGFET Model (BSIM). However, the extrinsic part consists of most of the parasitic elements, including all the terminal access series resistance, gate resistance, overlap and junction capacitance, and substrate network. The library in ADS contains various RF and microwave transistors models.

5.4.2 Inductor RF Models

Inductors are employed for tasks such as bias feeding and impedance matching of transistor spiral inductor are similar to inductive transmission line. So many parameters and careful tradeoff must be considered for the inductor design. Spiral inductors with reasonable Q and self-resonant frequency are widely used in the RFIC designs, such as fully integrated LNA, oscillator, and impedance matching network. They are proved to be most difficult passive components to be implemented on chip. Circular square spiral inductor is defined by side length, wire width, wire space, and number of turns. The component library in ADS contains the inductor model with its variable values having maximum and minimum limit set by the vendor. The inductance value is depending on these parameters such as turns number, diameter, and width. As the turn number decreases the inductance also decreases.

5.4.3 Capacitor RF Models

Capacitors are another important passive components widely used in RF circuit design, such as impedance matching and DC block. The usage of a capacitor is primarily dependent upon the characteristics of its dielectric. The dielectric's characteristics also determine the voltage levels and the temperature extremes at which the device may be used. The component library in ADS contains the capacitor model with its variable values having maximum and minimum limit set by the vendor.

5.4.4. Resistor RF Models

Resistance is the property of a material that determines the rate at which electrical energy is converted into heat energy for a given electric current. At very high frequencies and with low-value resistors (under 50 ohms), lead inductance, and skin effect may become noticeable. The component library in ADS contains various resistor models with its variable values having maximum and minimum limit set by the vendor.

5.5 LNA Design with Lumped Component using MOS

The design on A Low Power High Gain LNA using inductive source de-generation method. Source degeneration offers lower noise figures ~2-3dB than the Common-gate LNA topographies (with NF of ~5dB). The aim of this design is step-by-step a narrow band LNA (Low noise amplifier) to work over the wireless applications. For design of narrow band LNA to work over Wireless Applications, I am using the Agilent CMOS14 0.5um process that allows a minimum gate length of 0.6um. The schematic of the LNA, I will be designing is shown in Figure 5.1,

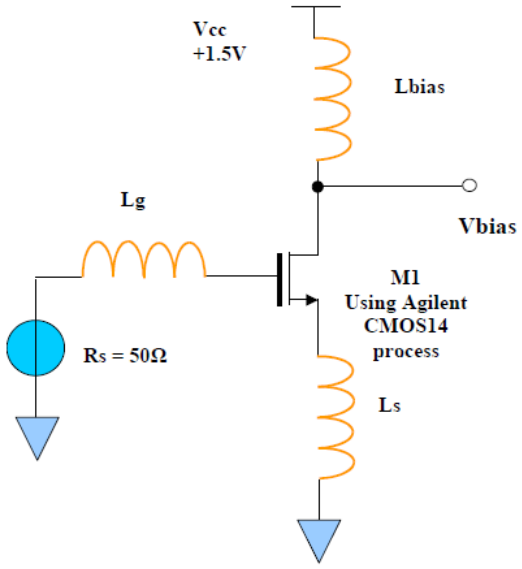


Figure 5.1: Initial LNA Schematic

5.5.1 Simulation of Basic LNA

ADS simulation setup to analyses the basic LNA design. Note I have added a current mirror and current source, together with a bias resistor to isolate the current mirror from the RF input. Note with this simulation, I have used ideal inductors i.e. no Q value has been entered and therefore have no loss.

Schematic circuit of a current mirror and current source, together with a bias resistor to isolate the current mirror from the RF input is given in figure 5.2;

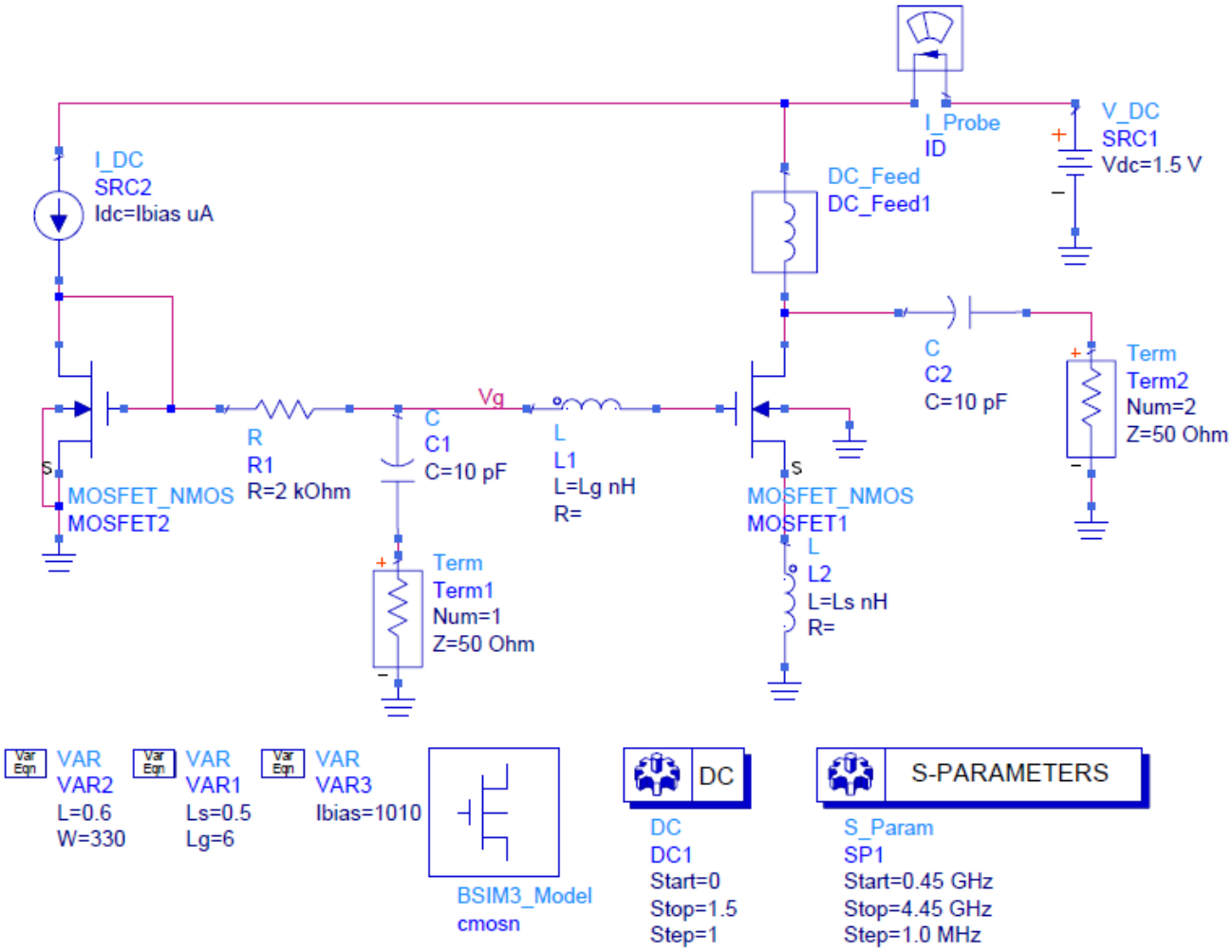


Figure 5.2: Schematic circuit of basic LNA design

5.5.1.1 Simulation Result

(i). S Parameter: S parameters is a scattering parameters as discussed in chapter 2, these are four S_{11}, S_{12}, S_{21}, S_{22}. $S_{11}$is input reflection coefficient, represents measure of how well the input impedance is match to the reference impedance. It is also known as input return loss and the input reflection coefficient $S_{11}$for 2.45 GHz frequency is -11.20 dB as shown in figure 5.3,

- S_{22} is output reflection coefficient and it represents measure of how well the output impedance is matched to load impedance. It is also known as output return loss, and the value of S_{22} at the 2.45 GHz frequency is -1.384 dB as shown in figure 5.4,

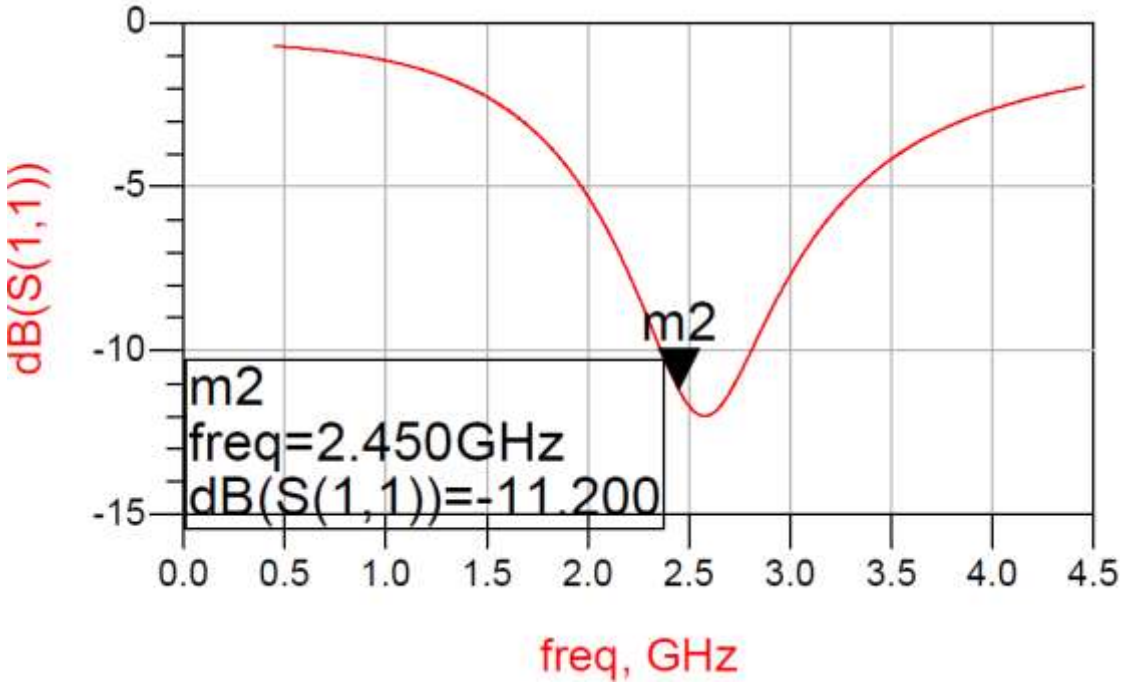


Figure 5.3: Scattering parameter S_{11}

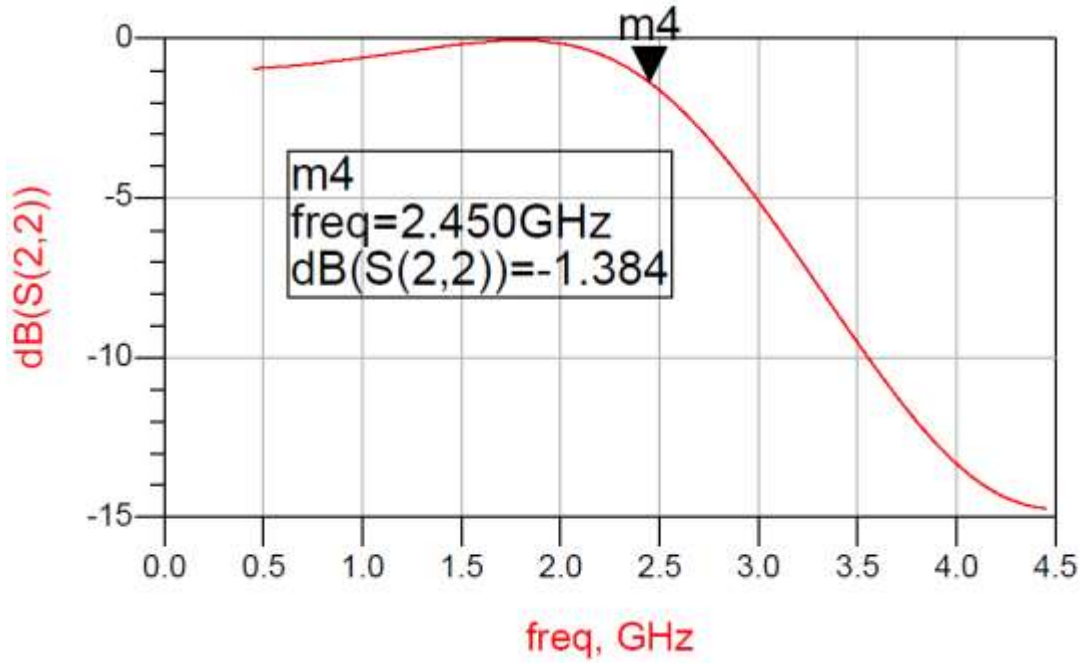


Figure 5.4: Scattering parameter S_{22}

- S_{21} is forward transmission coefficient and it is represents, measure how well the signal goes from input to output. It is also known as gain and the value of S_{21} at 2.45 GHz frequency is 12.139 dB as shown in figure 5.5

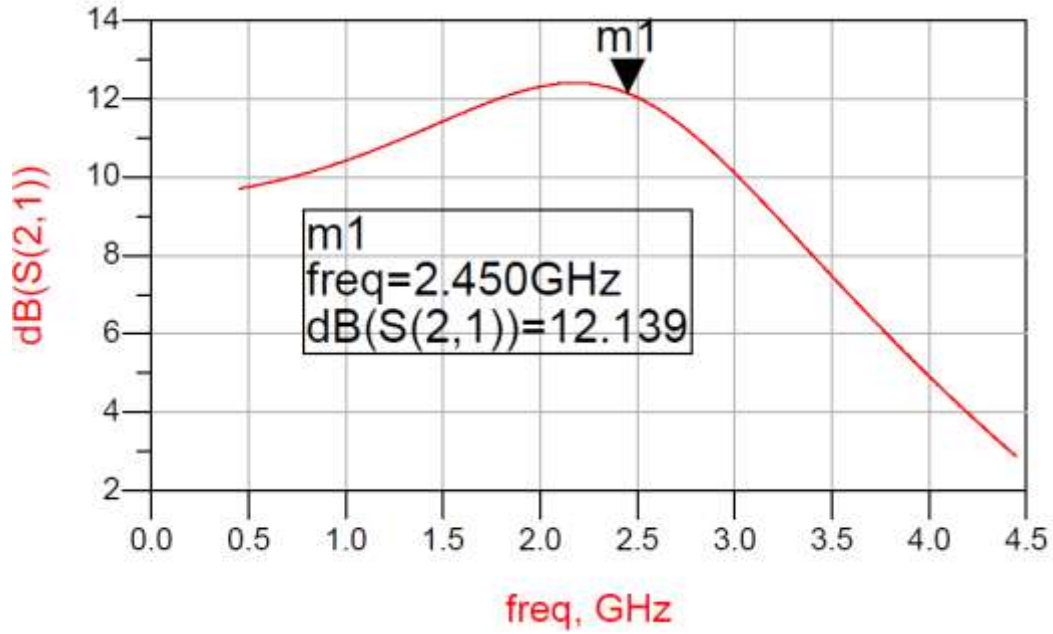


Figure 5.5: Forward Gain S_{21}

- S_{12} is reverse transmission coefficient, and measure how much the input signal is reflected back and it is also known as reverse isolation and the value of S_{12} at 2.45 GHz frequency is -13.503 dB as shown in figure 5.6

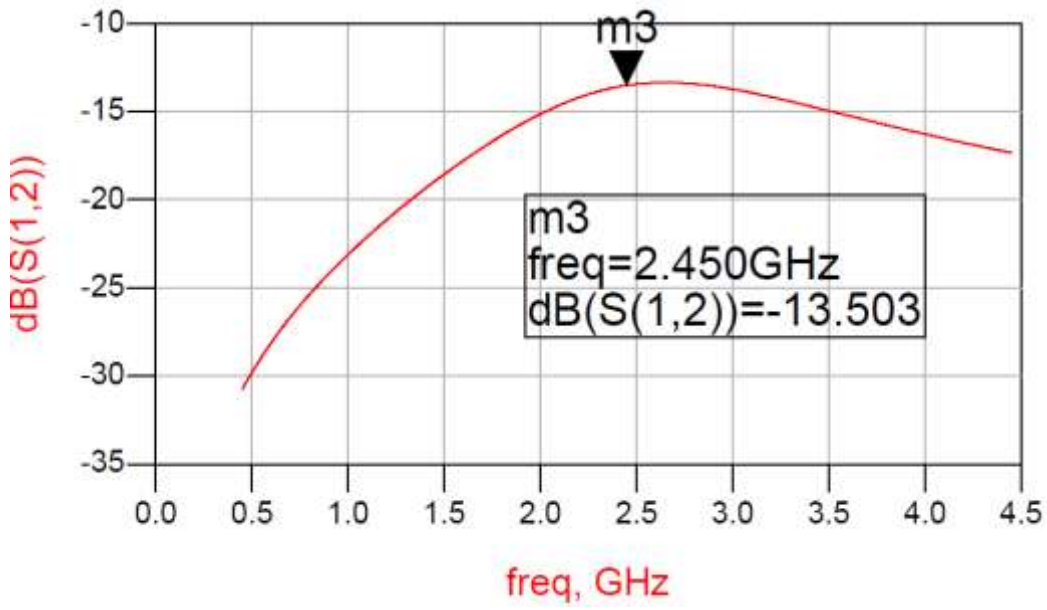


Figure 5.6: Scattering parameter S_{12}

(ii). Noise Figure: Simulation result of Noise Figure as shown in figure 5.7. This Noise Figure indicates the noise performances of device at high frequency and its value is 0.699 dB at 2.45 GHz

frequency and in the Figure 5.8 shows the minimum Noise Figure, with simulated value is 0.501 dB.

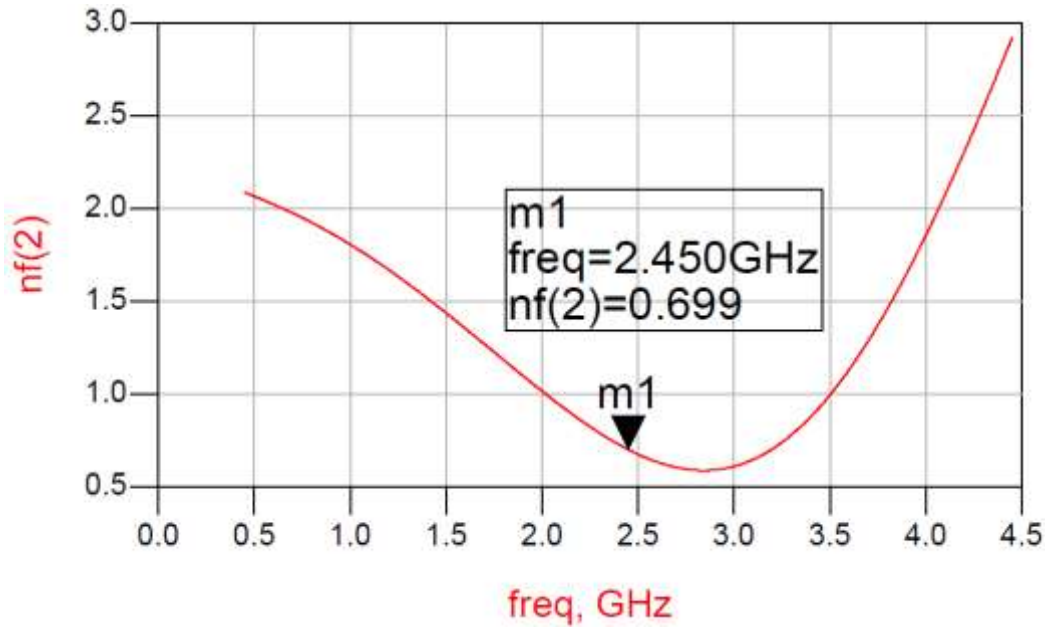


Figure 5.7: Noise Figure (NF)

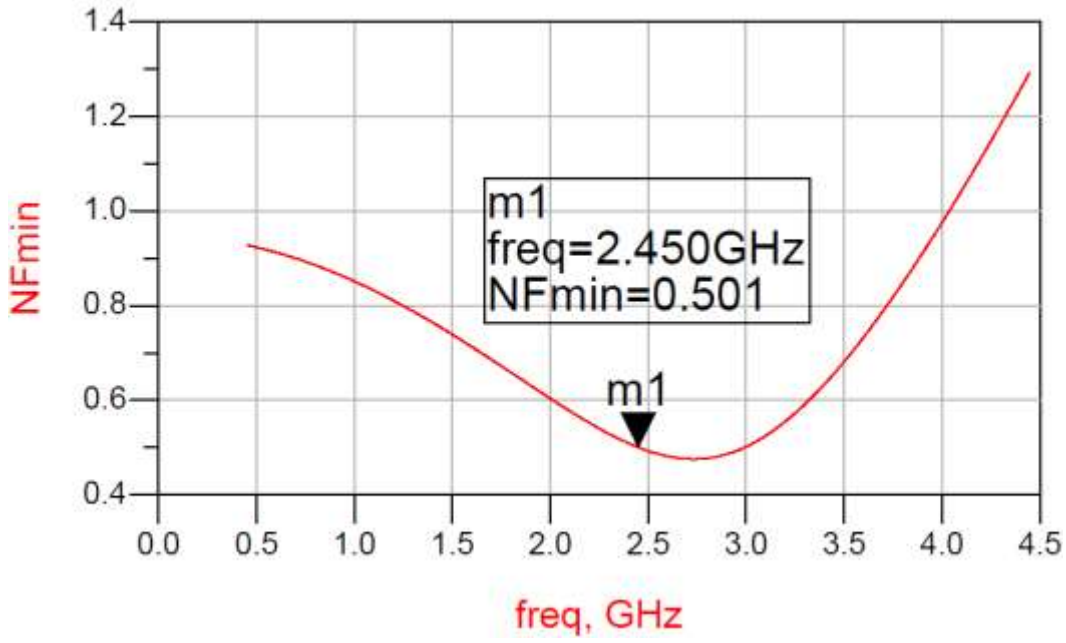


Figure 5.8: Minimum Noise Figure (NF_{min})

(iii). Power Consumption Table

5.2: Current and Voltage value,

Frequency	ID, i	V_g
0.0000 GHz	11.03 mA	1.055 V

- So, Power consumed by the designed circuit is **11.63mW**

5.5.2 Simulation of LNA With Additional cascode Stage

The cascode is a combination of a common-source device (ie our LNA) with a common-gate load. This has the effect of increasing the output impedance. We have assumed we are using a resistive load, but if we are going to connect to another stage – say another LNA or mixer, then the load will be capacitive. This capacitance will limit the frequency response of the first amplifier stage (resulting in lower gain) due to the Miller effect. Simulation of LNA with additional cascode stage is shown in figure 5.9,

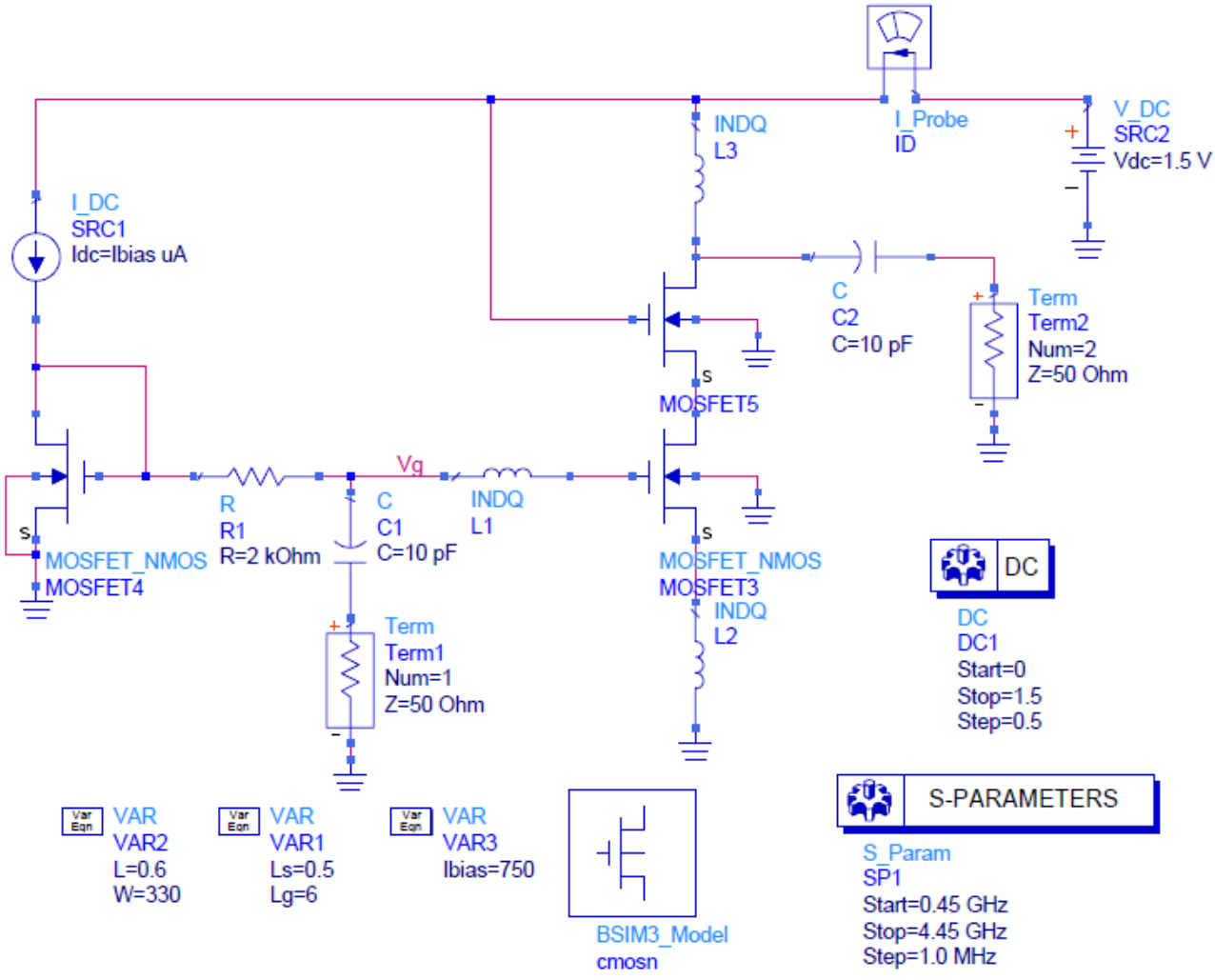


Figure 5.9: Schematic circuit of LNA design with additional cacode stage

5.5.2.1 Simulation Result

(i) S Parameter: The simulation results are shown in figure 5.10 to figure 5.13. Form figure 5.10 and figure 5.11, it can be seen that in operating frequency range input reflection coefficient S_{11} is -7.664 and output reflection coefficient S_{22} is -0.143 dB, and form figure 5.12 gain is 13.625 dB, gain flatness is good.

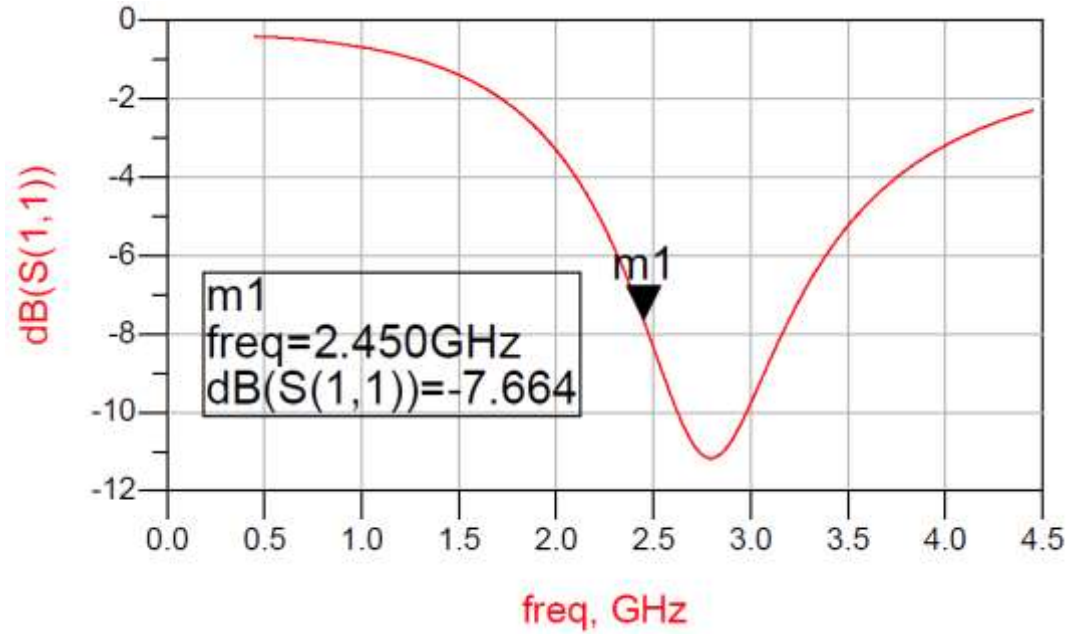


Figure 5.10: Scattering parameter S_{11}

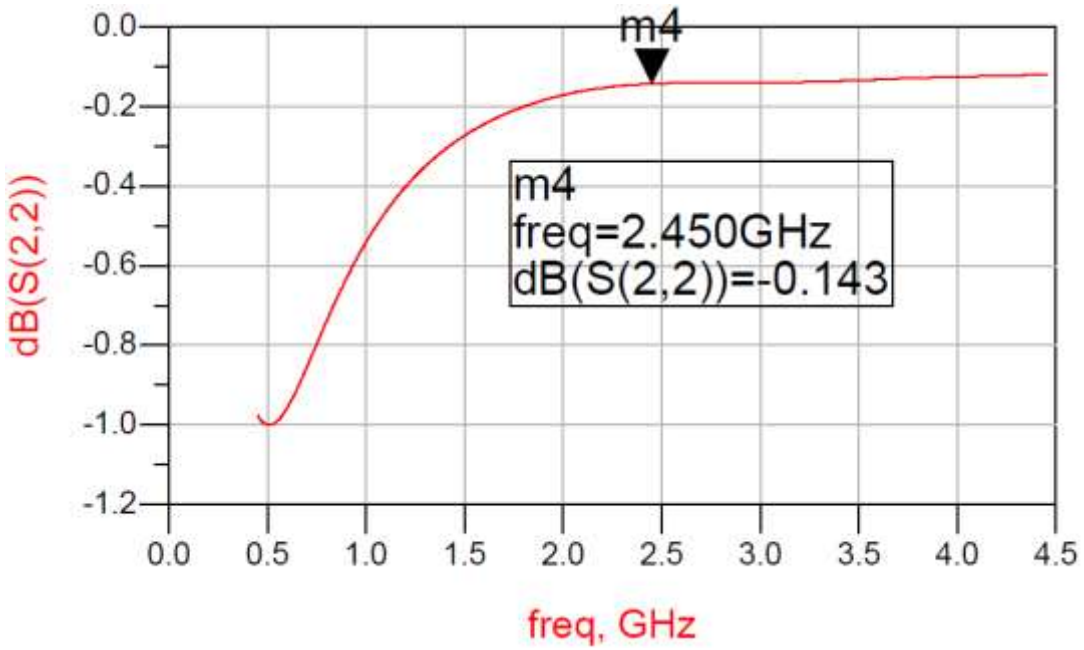


Figure 5.11: Scattering parameter S_{22}

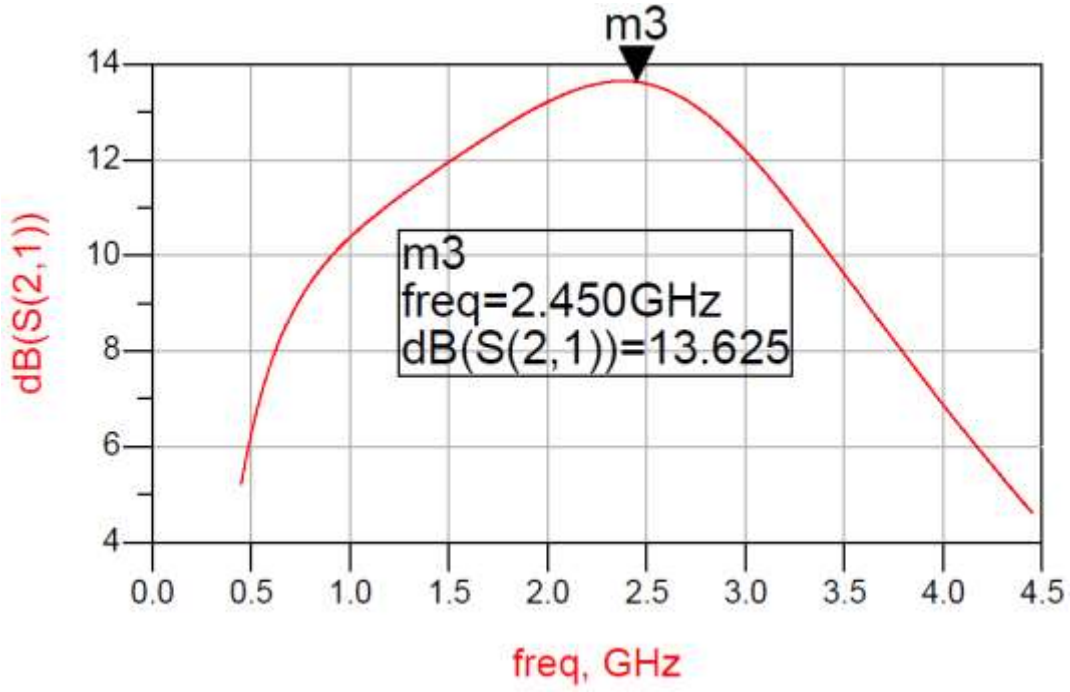


Figure 5.12: Forward Gain S_{21}

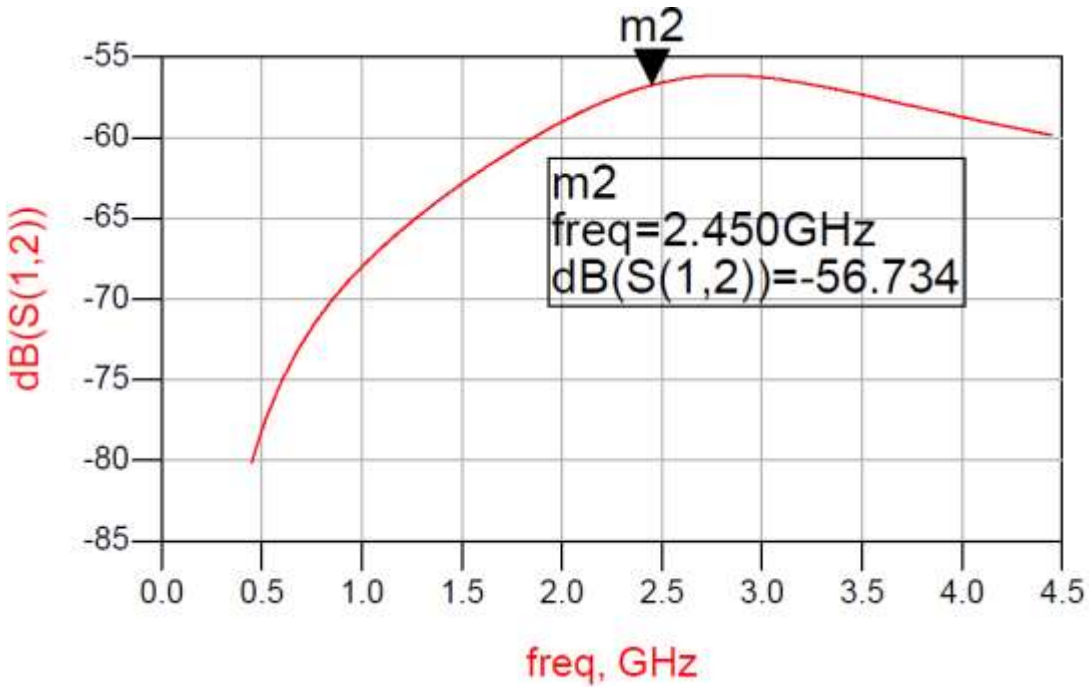


Figure 5.13: Scattering parameter S_{12}

(ii) Noise Figure

Simulation result of Noise Figure as shown in figure 5.14. This Noise Figure indicates the noise performances of device at high frequency and its value is 0.866 dB at 2.45 GHz frequency and in the Figure 5.15 shows the minimum Noise Figure, with simulated value is 0.783 dB

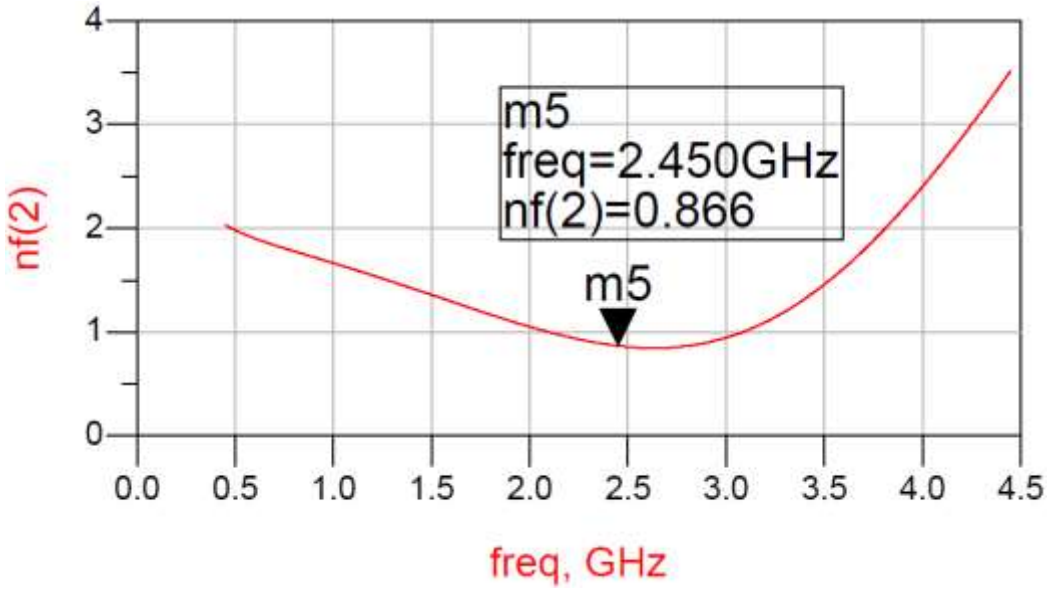


Figure 5.14: Noise Figure (NF)

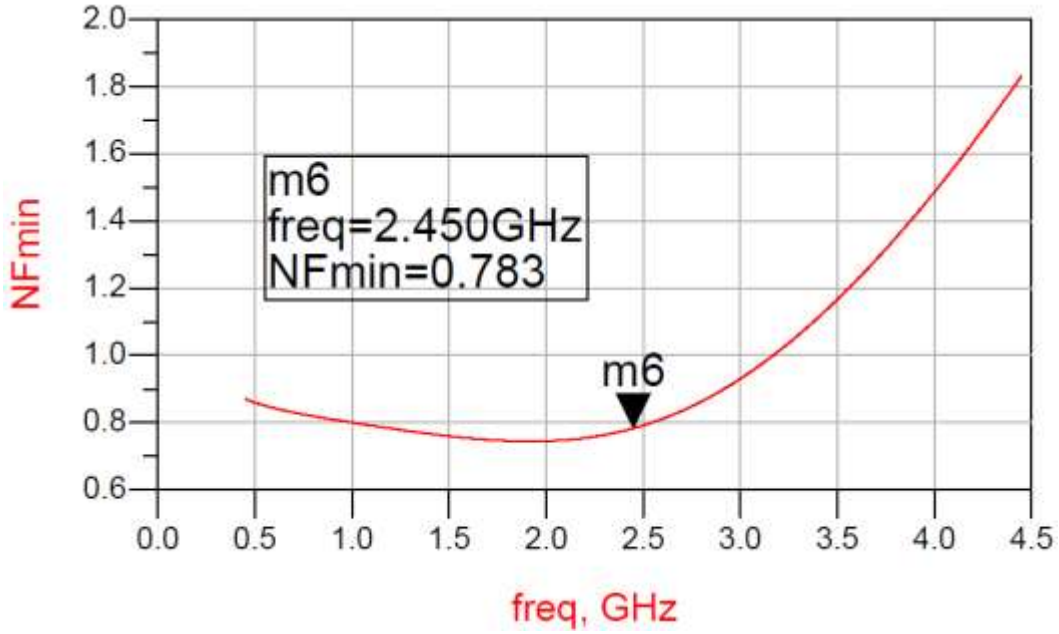


Figure 5.15: Minimum Noise Figure (NF_{min})

(iii) Power Comsumption

Table 5.3: Current and Valtage value,

Frequency	ID, i	V_g
0.0000 GHz	7.918 mA	1.023 V

- Power consumed by LNA design using Cascode technique is **8.10 mW**.

5.5.3 Simulation of C-S LNA with a simple C-S stage added to the 'cascode' output to increase the power gain of the LNA

To increase the gain of the LNA another C-S stage could be added to the cascade output. This output stage is DC coupled to the output of the first cascade stage so that is receives a correct bias to be in saturation. The increased gain will greatly improve the noise figure of the receiver as the noise figure of the second stage (most likely the mixer) will be reduced by ~1/gain_LNA.

The ADS simulation of proposed LNA is shown in figure 5.16,

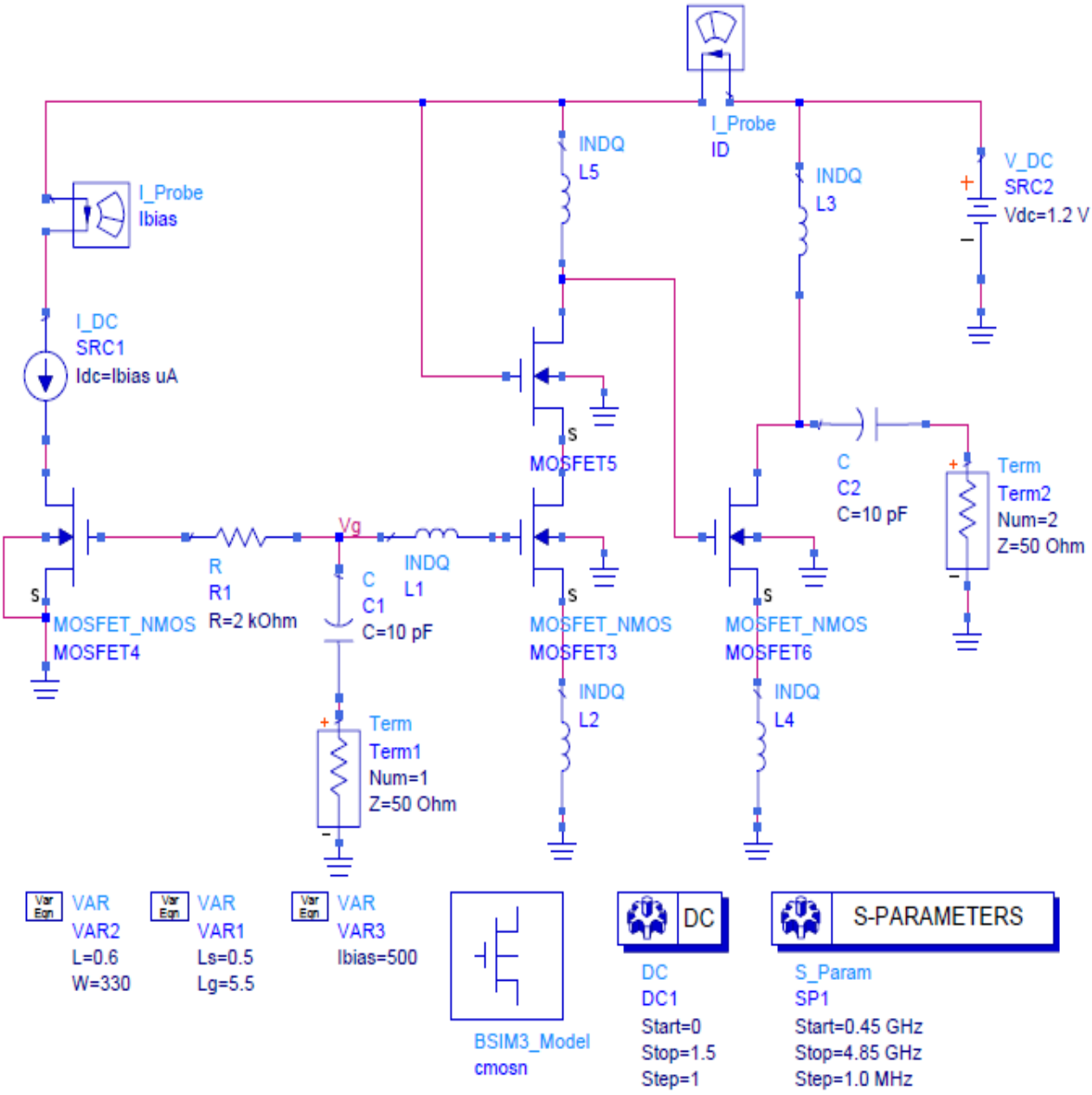


Figure 5.16: Schematic of the C-S LNA with a simple C-S stage added to the 'cascode'

5.5.3.1 Simulation Result

(i) S Parameter: The simulation results are shown in figure 5.17 to figure 5.20. Form figure 5.17 and figure 5.18, it can be seen that in operating frequency range input reflection coefficient S_{11} is -5.841 and output reflection coefficient S_{22} is -18.823 dB, and form figure 5.19 gain is 26.486 dB, gain flatness is good.

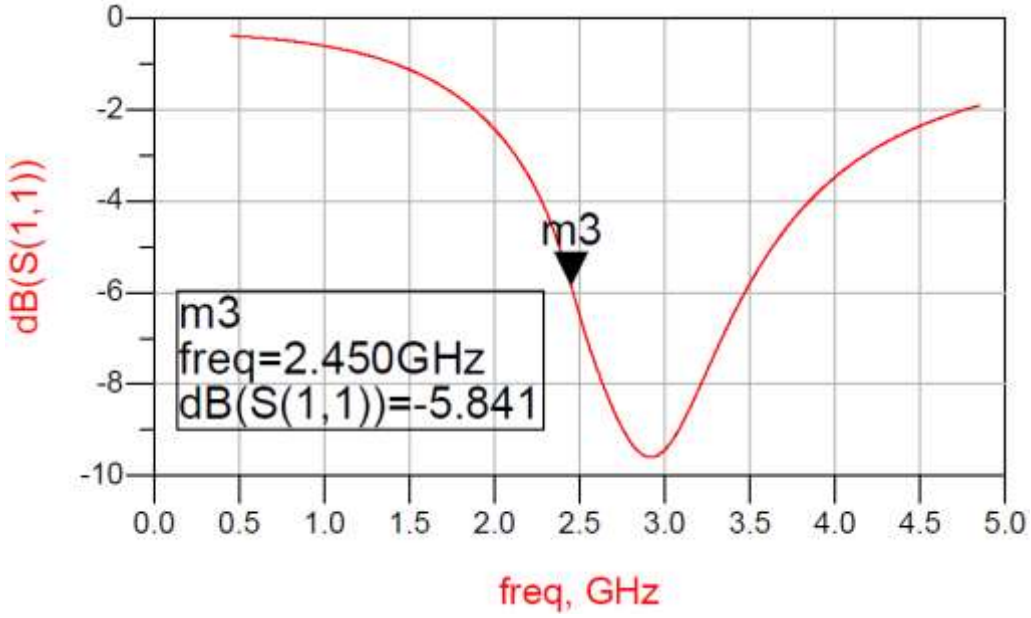


Figure 5.17: Scattering parameter S_{11}

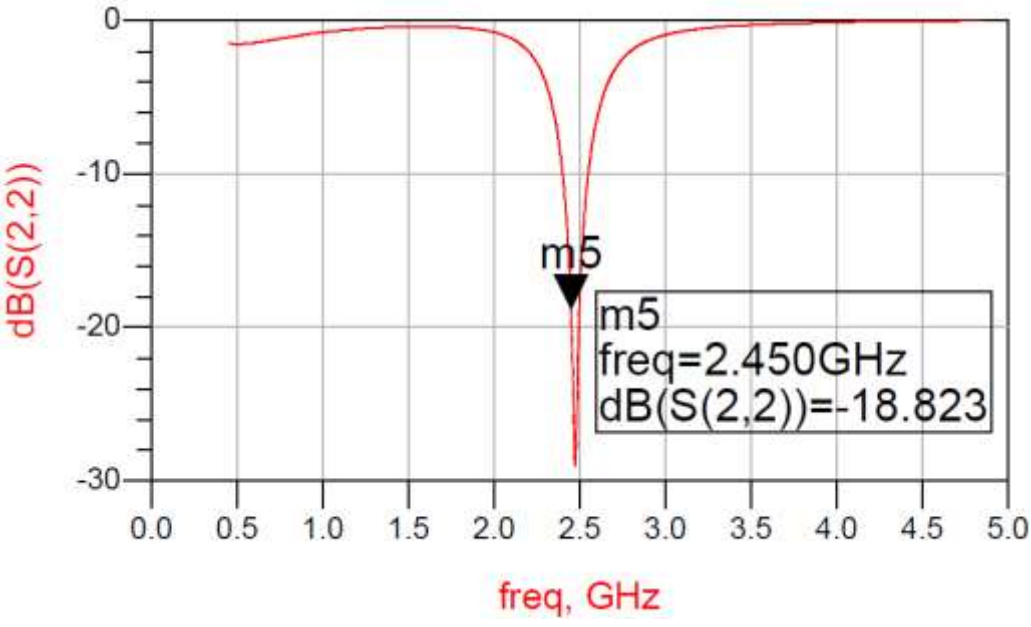


Figure 5.18: Scattering parameter S_{22}

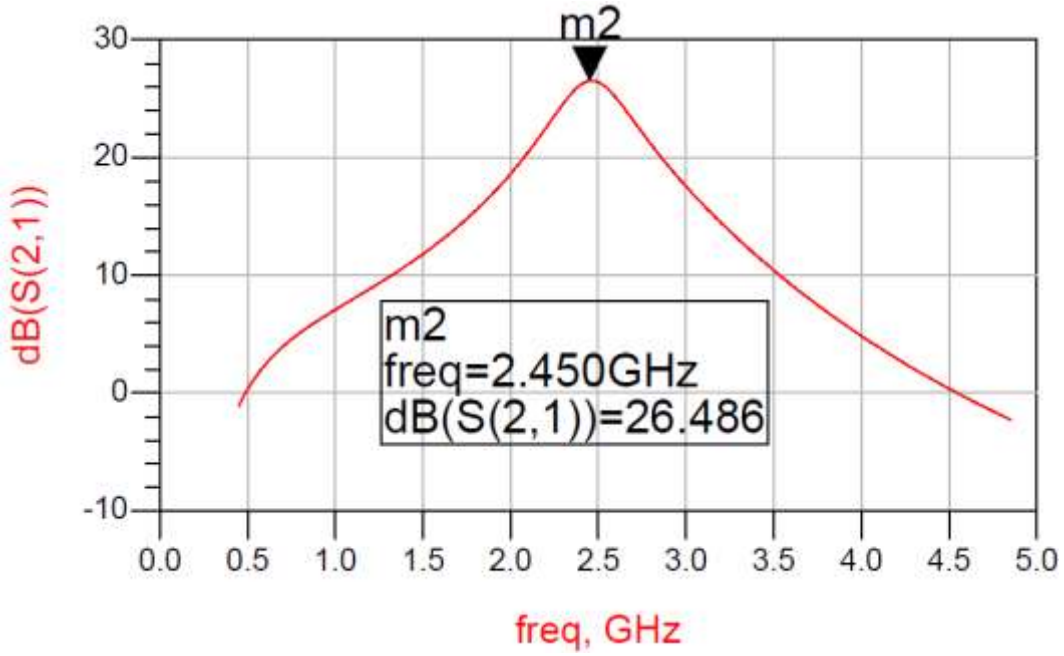


Figure 5.19: Forward Gain (S_{21})

Figure 5.20: Scattering parameter S_{12}

(ii) Noise Figure

Simulation result of Noise Figure as shown in figure 5.21. This Noise Figure indicates the noise performances of device at high frequency and its value is 1.268 dB at 2.45 GHz frequency and in the Figure 5.22 shows the minimum Noise Figure, with simulated value is 1.044 dB.

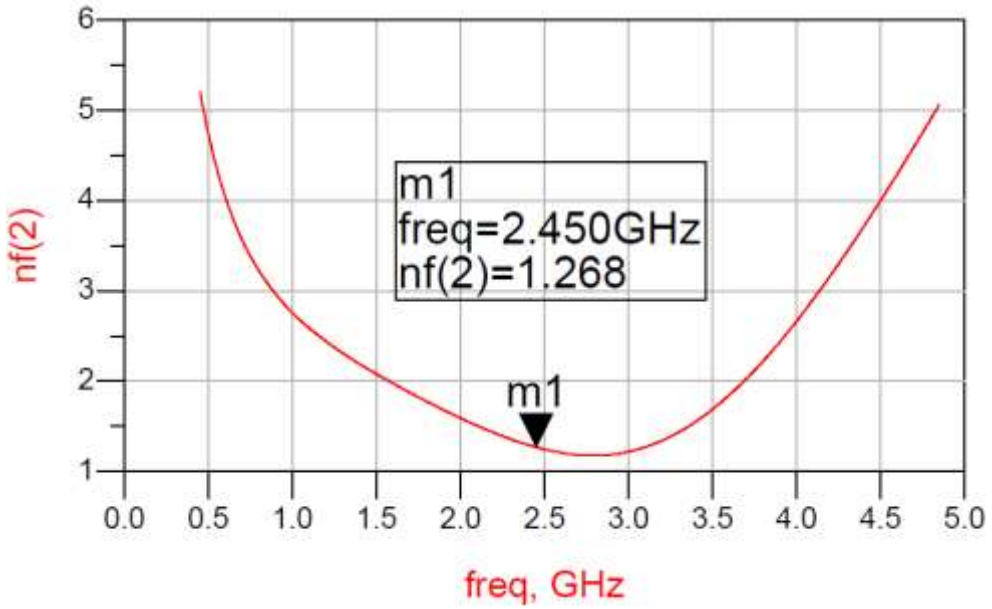


Figure 5.21: Noise Figure (NF)

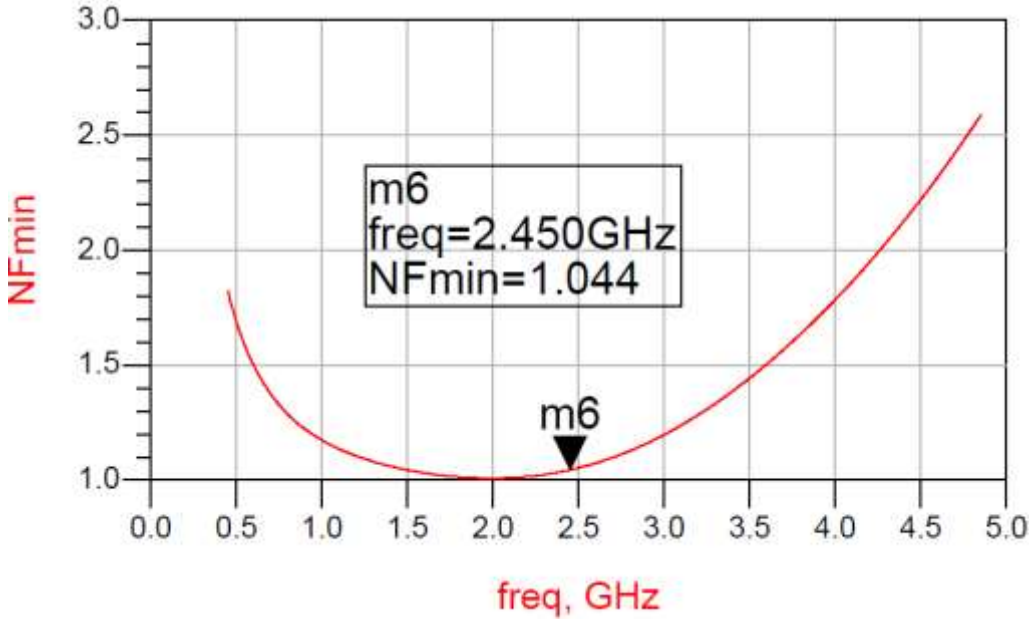


Figure 5.22: Minimum Noise Figure (NF_{min})

(iii) Power Comsumption

Table 5.4: Current and Valtage value,

Frequency	ID, i	V_g
0.0000 GHz	4.865 mA	924.8 mV

- Power consumed by LNA design using above design is **4.49 mW**.

5.5.4 Result obtained from Simulation

Based on the simulation results of all three simulation of LNA Table 5.5 shows the various performance parameters result of the design and it gives the conclusion that proposed LNA for wireless application is for better than the targeted LNA given in table 5.1,

Table 5.5: Performance Parameters

Performance parameters	**Using current mirror and current source**	**Using additional cascade stage**	**Using C-S LNA with a simple C-S stage added to the 'cascode'**
S_{11}	-11.200 dB	-7.664 dB	-5.841 dB
S_{12}	-1.384 dB	-0.143 dB	-18.823 dB
S_{21}	**12.139 dB**	**13.625 dB**	**26.486 dB**
S_{22}	-13.503 dB	-56.733 dB	-52.533 dB
Noise Figure(NF)	0.699 dB	0.866 dB	1.268 dB
(NF_{min})	0.501 dB	0.783 dB	1.044 dB
Power Consumed	**11.63 mW**	**8.10 mW**	**4.49 mW**

As shown in the above table 5.5 the values of matching parameters S_{11}, S_{12}, and S_{22} are -5.841 dB, -18.823 dB and -52.533 dB respectively, with targeted values as shown in table 5.1, of that is less than -15dB. Targeted gain is greater than 10dB whereas gain of this proposed design circuit is 26.486 dB and noise figure must be less than 2dB as given in table 5.1, noise figure of this proposed design is 1.268 dB and minimum noise figure is 1.044 dB. Power consumption of proposed LNA design in only 4.49 mW which is very less than that of the targeted power consumption and all the other performance parameters values are better than target value.

Here we have increased the gain of the MOS LNA more than 26 dB and power consumption is very less which is 4.49 mW. So we designed the circuit of C-S LNA with a simple C-S stage added to the 'cascode' output to increase the power gain of the LNA, which is 26.486 dB. Hence our proposed LNA is full filling all the criteria as given in the table 5.1, so it is a low power high gain LNA for wireless applications.

5.6 LNA Design using HEMT

Low Noise Amplifier Design for 2.4 GHz operating frequency range by using 0.18um HEMT Technology, 0.18um is represents the length of device. In this section, we design LNA using both lumped components and microstrip lines.

5.6.1 LNA Design with Lumped Components using HEMT

Transistor must be biased at appropriate operating point before used. So that, transistor can works under values required and achieve less power consumption. In this project, passive biasing method is adopted [40-42]. The component readings are determined with reference from datasheet. By referring datasheet, data of V_{ds} = 3V and I_{ds} = 60mA had be chosen because it is believed thatit can give optimum values in gain and noise figure With V_{gs} = 0.52, I_{BB}=2mA, V_{ds} = 3V and I_{ds} = 60mA.

$$R_3 = \frac{V_{gs}}{I_{BB}} = 260\Omega,\ R_4 = \frac{V_{dd} - V_{ds}}{I_{ds} + I_{BB}} = 32.26\Omega,\ R_1 = \frac{(V_{ds} - V_{gs})R_3}{V_{gs}} = 1.24k\Omega$$

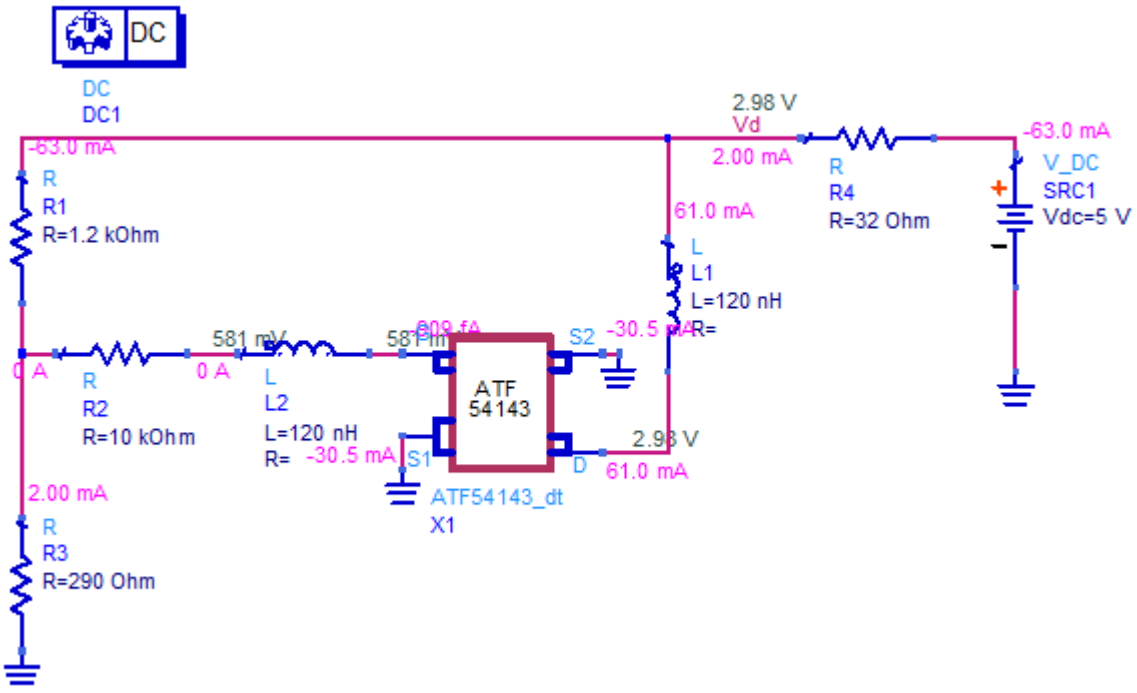


Figure 5.23: DC biasing Circuits

The R_1, R_4 and R_3 in circuit are slightly adjusted from calculated readings in order to obtain better V_{ds} and I_{ds} reading in the simulation. Given Z_L=Z_S=Z_O=50 Ω

From the data sheet which is given in appendix A, S parameter at 2.5 GHz is:

S_{11}=0.60<176.2

S_{21}=6.01<61.80

S_{12}=0.07<30.10

S_{22}=0.13<-129.7

The reflection coefficient to source, Γ_S and reflection coefficient to load, Γ_L, and the equation is shown in (5.1) and (5.2).

$$\Gamma_s = \frac{Z_S - Z_0}{Z_S + Z_0} \tag{5.1}$$

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{5.2}$$

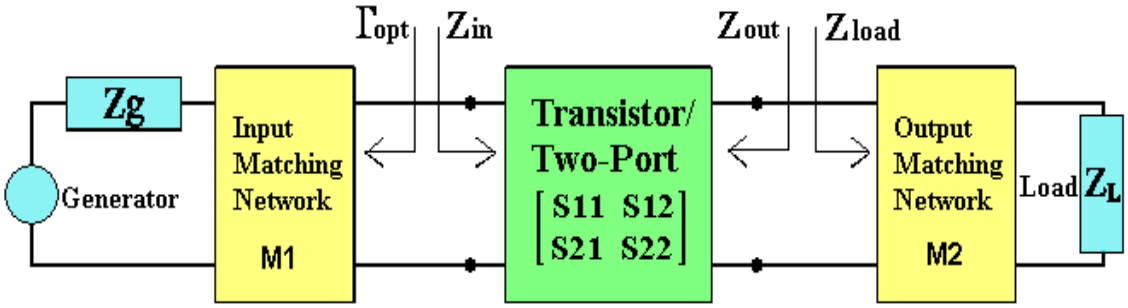


Figure 5.24: Block diagram of a single stage two port LNA model

Since given $Z_L = Z_S = Z_0 = 50\Omega$, the Γ_L and Γ_S calculated as zero. Reflection coefficient at the input and output:

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} = S_{11} = 0.60\angle 176.2 \tag{5.3}$$

$$\Gamma_{out} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} = S_{22} = 0.13\angle -129.7 \tag{5.4}$$

Power gain, G

$$G = \frac{|S_{21}|^2\left(1 - |\Gamma_L|^2\right)}{\left(1 - |\Gamma_{in}|^2\right)|1 - S_{22}\Gamma_L|} = 56.43 = 17.52dB \tag{5.5}$$

Available power gain, G_A

$$G_A = \frac{|S_{21}|^2\left(1-|\Gamma_S|^2\right)}{|1-S_{11}\Gamma_S|^2\left(1-|\Gamma_{out}|^2\right)} = 36.74 = 15.65dB \quad (5.6)$$

Transducer gain, G_T

$$G_T = \frac{|S_{21}|^2\left(1-|\Gamma_S|^2\right)\left(1-|\Gamma_L|^2\right)}{|1-\Gamma_S\Gamma_{in}|^2\,|1-S_{22}\Gamma_L|^2} = 36.12 = 15.58dB \quad (5.7)$$

5.6.1.1 Stability Consideration

The stability of an amplifier or its resistance to oscillate is an important consideration in a design. It can be determined from the Sparameters. Oscillation occurs when K< 1. This is due to the dependence of and on the source and load matching networks. An amplifier is said to be unconditionally stable if the auxiliary condition along with *Rollet's condition*, defined as in equations below, are simultaneously satisfied [40],[42].

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}S_{21}|} > 1$$

$$|\Delta| = |S_{11}S_{22}-S_{21}S_{12}| < 1$$

For this design it is found that $K = 1.009 > 1 \quad and\ \Delta = 0.3427 < 1$

5.6.1.2 Noise Figure

Besides the stability and gain requirement, noise figure is another important consideration for a microwave amplifier. In receiver applications, it often required preamplifier with as low noise figure as possible as it has dominant effect on the noise performance of the system. From the ATF-54143 datasheet,

F_{min} = 0.52,

Γ_{opt}= 0.26 and

R_N/Z_0 = 0.04 at 2.4 GHz

$$F = F_{Min} + \frac{4r_n|\Gamma_s-\Gamma_{opt}|^2}{\left(1-|\Gamma_s|^2\right)|1+\Gamma_{opt}|^2} = NF = 2.769dB$$

LNA circuit before matching

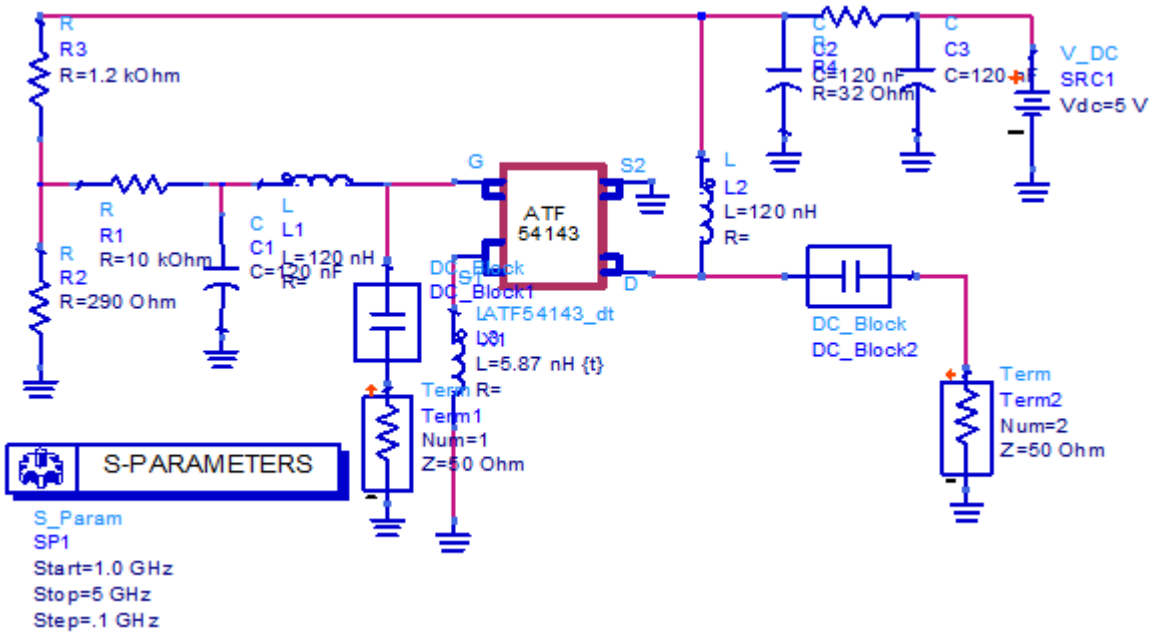


Figure 5.25: LNA circuit before matching network

5.6.1.3 Matching Network

The impedance matching basic idea is presented in Fig. 5.26, which ensembles that an impedance matching network placed between the load impedance and transmission line. Matching network is made to ideally avoid the unnecessary power loss. There are variety of factors that needed to be considered in the matching network selection e.g. complexity, implementation and adjustability. In this work, the LNA is designed by using lumped elements using L-C matching techniques.

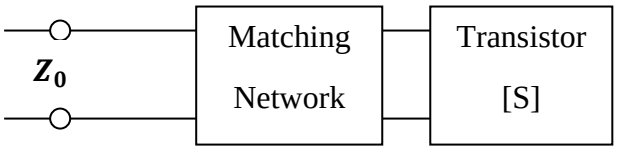


Figure 5.26: Impedance matching network

The parameters noise figure, stability factor, return loss and gain values are calculated by using above equations. While simulation results before the matching are listed as in Table 5.6.

Table 5.6: Results differences in calculated and simulation before applying matching network

Parameters	Calculated	Simulated
$\lvert\Gamma_S\rvert$	0	0.51∠-164.1
$\lvert\Gamma_L\rvert$	0	0.34∠21.3

$\|\Gamma_{in}\|$	0.60∠176.2	0.702∠169.92
$\|\Gamma_{out}\|$	0.13∠-129.7	0.037∠-70.502
K	1.1478	0.971
G	17.52 dB	17.25 dB
G_A	15.65 dB	15.31 dB
G_T	15.58 dB	15.76 dB
G_{Tmax}	15.58 dB	15.63 dB
NF	2.769 dB	0.375 dB

5.6.2 Proposed Schematic Design of LNA using HEMT

To match both impedance of input and output Lumped elements matching is added into LNA circuit with assistance of smith chart utility in ADS software. After matching from smith chart, the Lumped elements circuit will automatically generated. The components reading designed by ADS software do not exist in market. Thus, to fabricate, it must change to actual values. Matching has done using with the help of L-C matching technique.

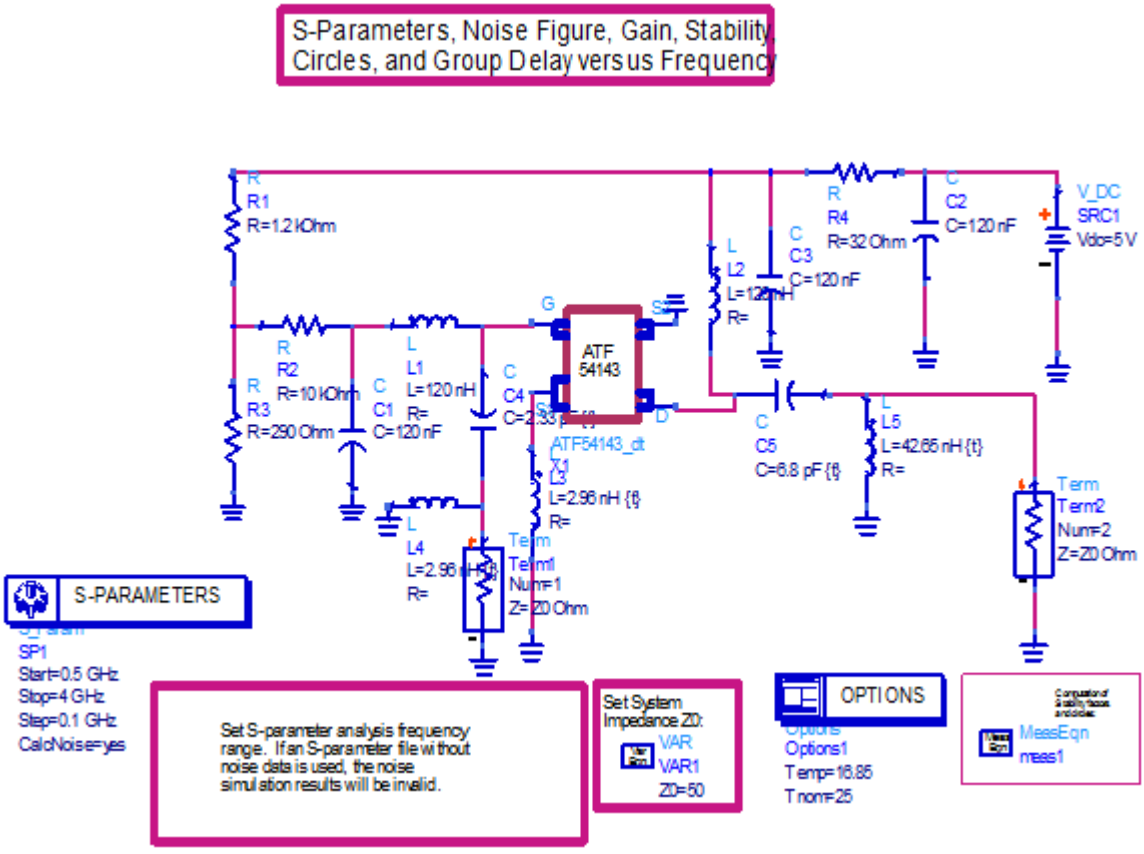


Figure 5.27: Complete LNA circuit with input and output matching circuit

Other matching techniques such as Pi match, T-match are also used to match input and output port of amplifier. But here L-C section is used for simplicity and to reduce the complexity of circuit.

The stability of this transistor is unconditionally stable at 2.4 GHz since its K constant is more than 1, which is 1.009 from the simulation. Therefore, no stability circle has to be drawn. Stability and maximum available gain are two of the more important considerations in choosing a two-port network LNA for use in amplifier design. As used here, stability measures the tendency of an LNA to oscillate.

5.6.2.1 Simulation Result

(i) S parameters: The simulation results are shown in figure 5.28 to figure 5.31. Form figure 5.28 and figure 5.29, it can be seen that in operating frequency range input reflection coefficient S_{11} is -15.082 and output reflection coefficient S_{22} is -10.261 dB, and form figure 5.19 gain is 15.227 dB, gain flatness is good.

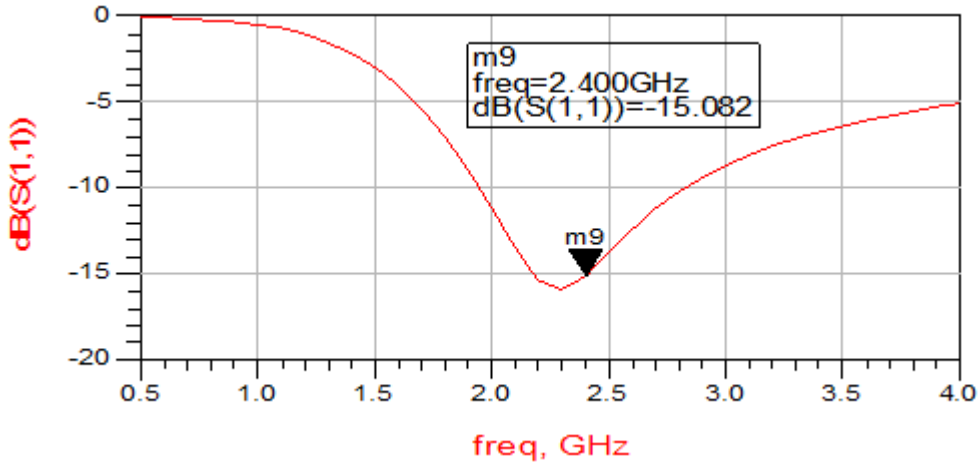


Figure 5.28: Scattering parameter S_{11}

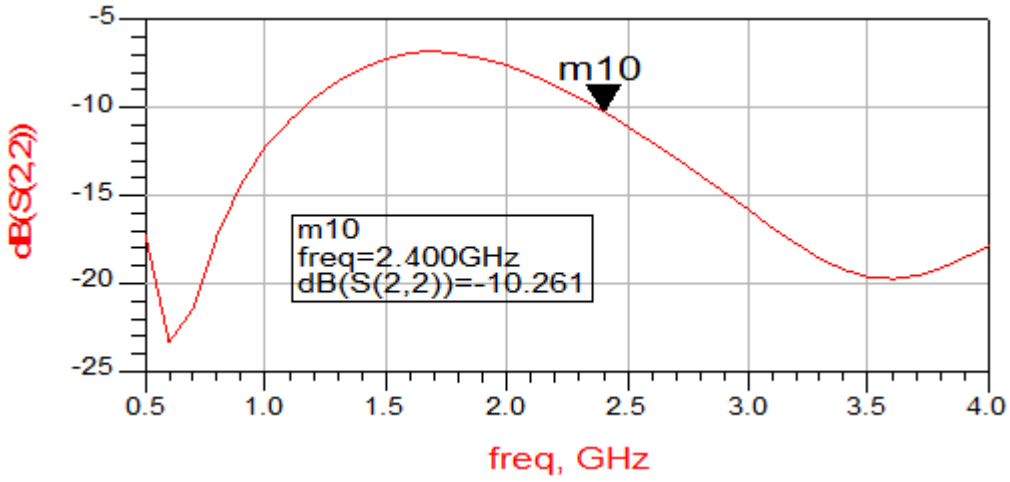


Figure 5.29: Scattering parameter S_{22}

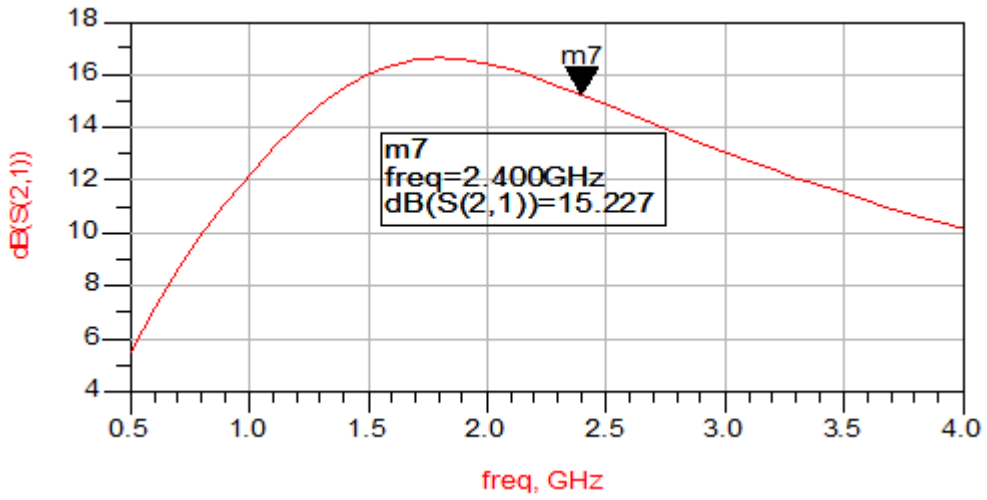


Figure 5.30: Forward Gain (S_{21})

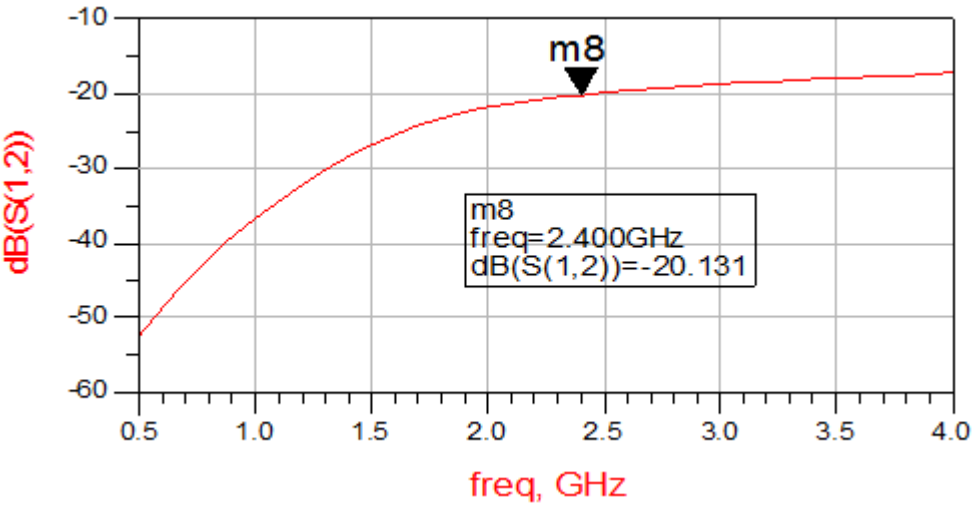


Figure 5.31: Scattering parameter S_{12}

(ii) Noise Figure

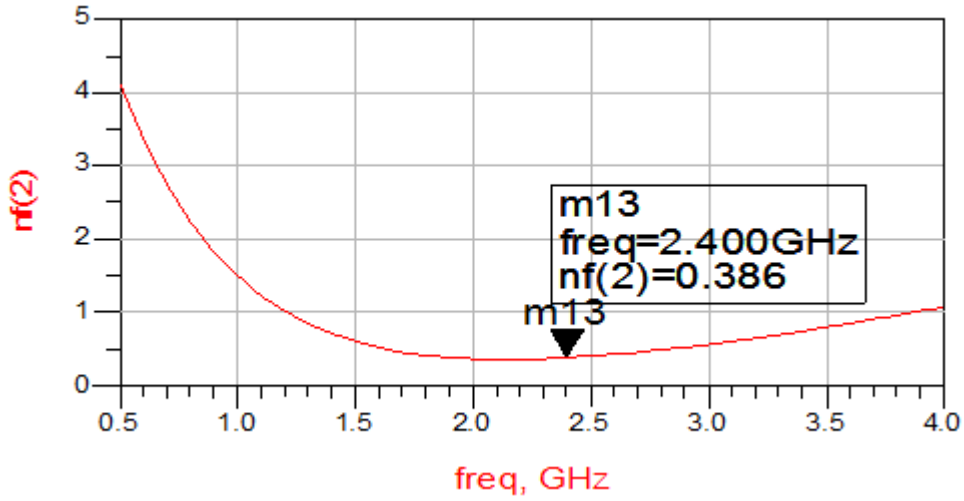


Figure 5.32: Noise Figure (NF)

Simulation result of Noise Figure as shown in figure 5.32. This Noise Figure indicates the noise performances of device at high frequency and its value is 0.386 dB at 2.45 GHz frequency and in the Figure 5.33 shows the minimum Noise Figure, with simulated value is 0.379 dB

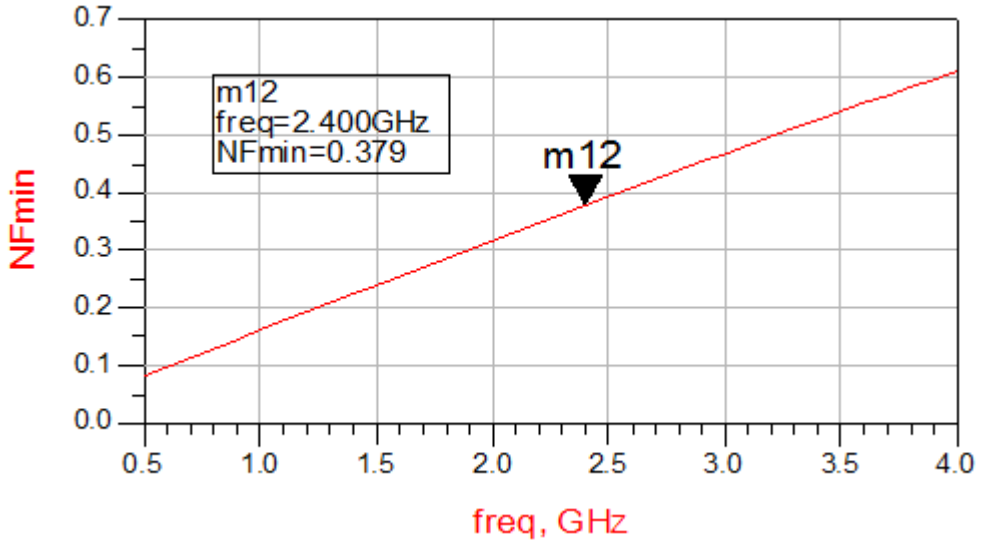


Figure 5.33: Minimum Noise Figure (NF_{min})

(iii) Stability: As we know that stability is defines by the factor K called as rollet stability factor, and this factor is describes in terms of s parameters, so that stability factor of circuit as shown in figure 5.34 and it must be greater than 1 so its value is 1.009 at 2.4 GHz frequency.

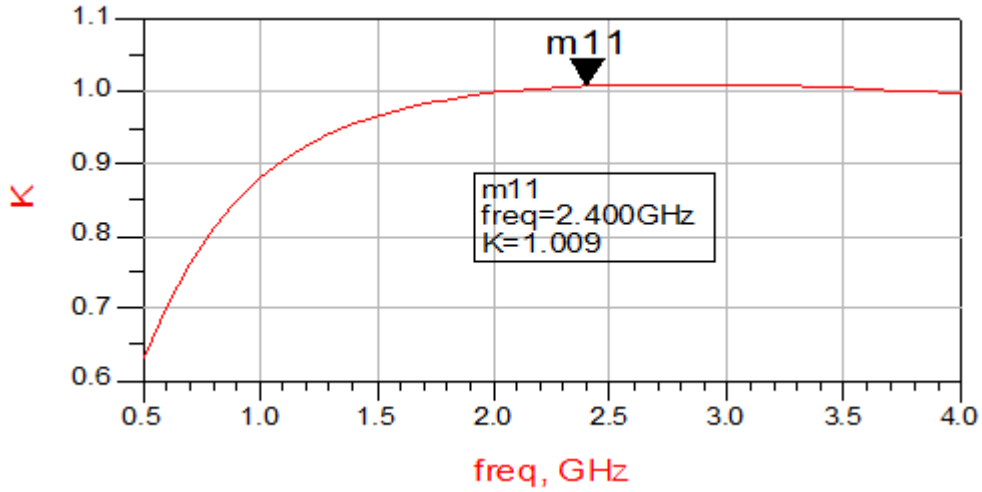


Figure 5.34: Stability factor

➢ Comparison Graph of different Gain is shown in figure 5.35.

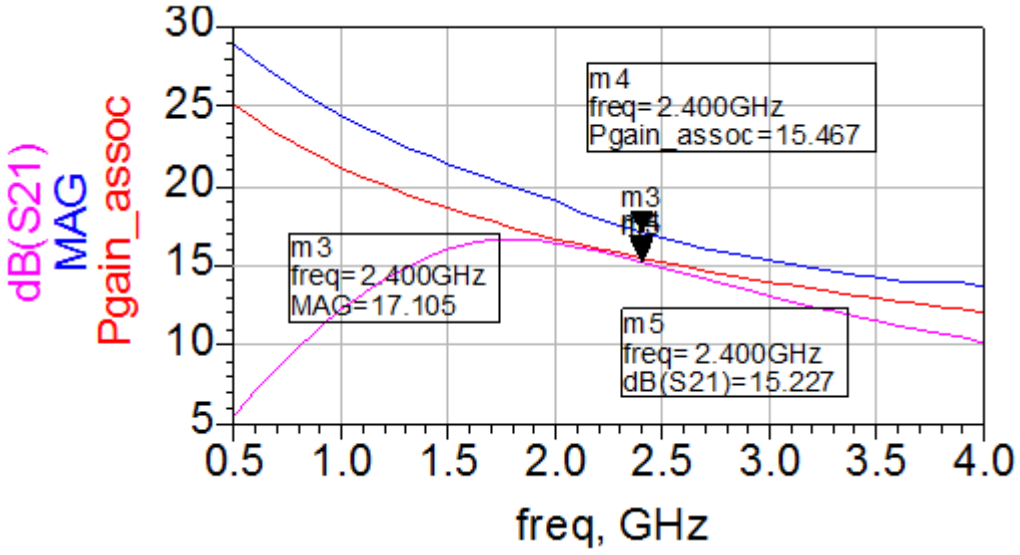


Figure 5.35: Gain Comparison

(iv) Bandwidth Calculation: As shown in the figure 5.30, the bandwidth is calculated by the help of gain graph, and the bandwidth of LNA is 500 MHz.

5.6.3 LNA Design with Microstrip Lines Components using HEMT

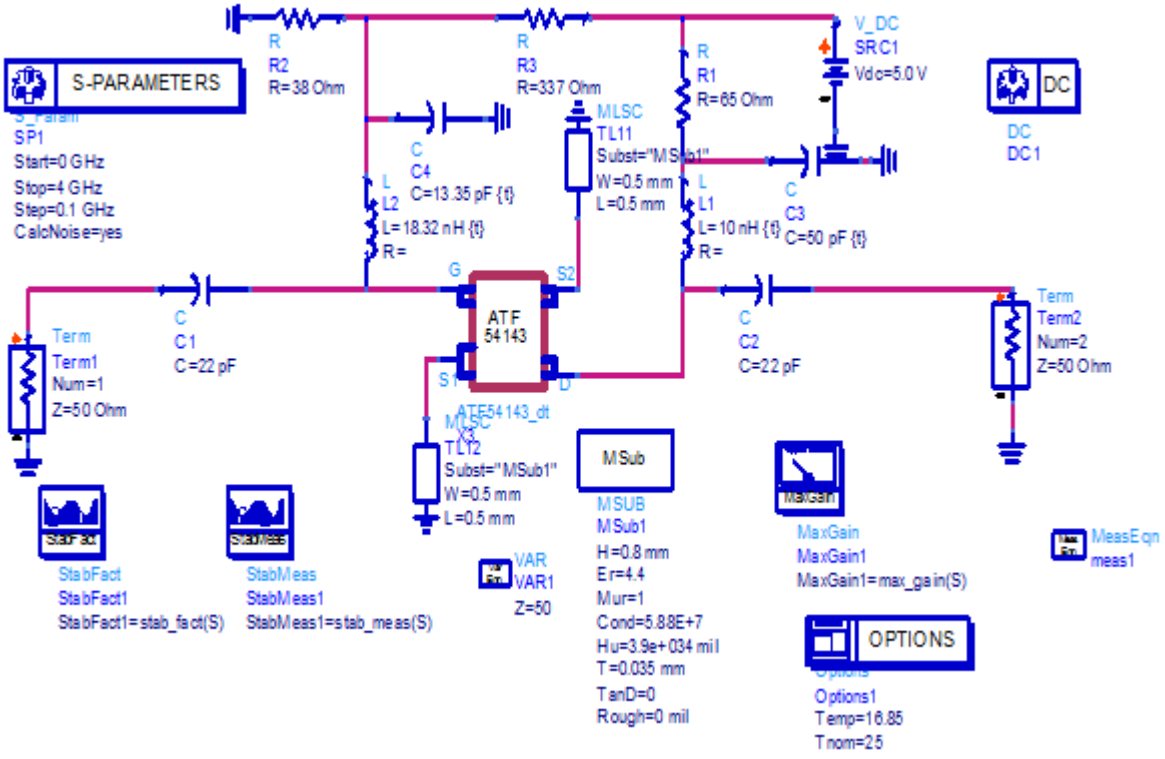


Figure 5.36: DC Bias circuit diagram

The main technical indexes of the LNA: working frequency from 2.40Hz to 2.50Hz, noise figure (NF) less than 2.0 dB, gain more than 12dB. Component choice is vital to design the LNA. According to the designing demand, Low noise PHEMT ATF-54143 manufactured by Avago has chosen and it is found that the minimum noise figure (F_{min}) is close to 0.52dB and the gain is about 16.65dB when f = 2.40GHz, V_{ds} = 3V, I_{ds} = 20 mA. It can satisfy design demand, so this point is chosen as the quiescent point of ATF-54143. DC Bias circuit is shown in Figure 5.36.

5.6.3.1 Stability of LNA

Because of the existence of reflected wave, RF amplifier will generate self-oscillation in some frequencies and cannot amplify signal. So stability is a very important factor we must take into consideration in the design of RF amplifier. We have to judge the amplifier is stable absolutely or not before designing matching circuit. Stability depends on S parameter of the transistor, matching network and biasing requirements. The sufficient and necessary conditions of absolute stability are

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}S_{21}|} > 1$$

$$|\Delta| = |S_{11}S_{22} - S_{21}S_{12}| < 1$$

ATF-54143 isn't stable absolutely in some frequencies. In order to improve stability, negative feedback circuit is added in the source electrode. The circuit is shown in Figure 5.36.In the circuit, also short Microstrip lines of appropriate length between the source and ground has added. It acts as adding feedback inductance in the source. It is very complex that directly calculating stability figure by the datasheet, so one can use stability coefficient of the ADS software to analyse the stability of the amplifier. The simulation result is shown in Figure 5.37. From the figure it has found that K coefficient is greater than 1, so the transistor is stable absolutely in working frequencies.

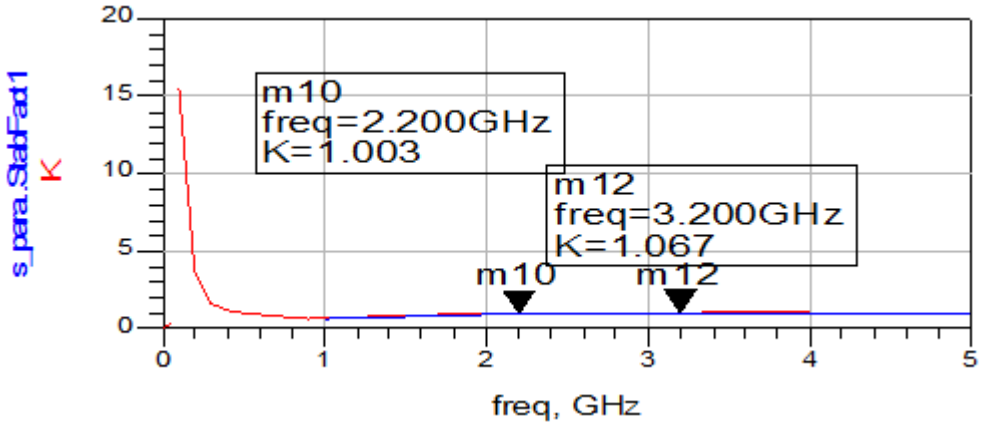


Figure 5.37: Stability factor

5.6.3.2 Design of Matching Network of Input Terminal

The design uses distributed parameter elements on account of high working frequency. It has to be balance gain and noise figure in designing because the input impedance when LNA has maximum gain is different that when LNA has minimal noise. The noise figure of receiving system is mainly determined by the first LNA, so the design uses minimal noise matching principle. In order to get minimal noise figure, reflection coefficient of input terminal must satisfy requirement of best source reflection coefficient (Γ_{opt}). If termination impedance and characteristic impedance of Microstrip line is 50 ohm, matching network of input terminal has to convert Γ^*_{opt} into 50 ohm. This design uses type L matching network. First, matching network of input terminal has designed with DA_Smith Chart Match of ADS software, roughly determine its parameters approximately, and then optimize with tuning tool of ADS software. The matching network of input terminal is shown in Figure 5.38.

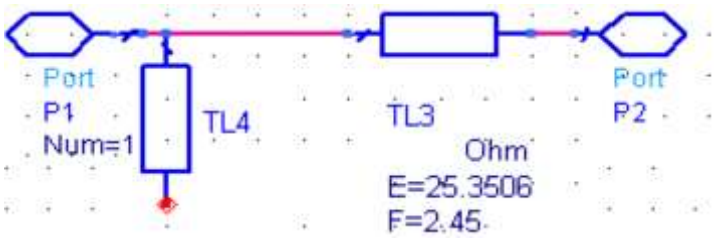


Figure 5.38: Matching network of input terminal

5.6.3.3 Design of Matching Network of Output Terminal

Matching network of output terminal is for increasing gain, improving gain flatness and input VSWR, so the design use maximum gain matching principle. Also matching network of output terminal has designed with DA_Smith Chart Match of ADS software. The simulation results show that return loss of input terminal is good, but return loss of output terminal is bad. So, it has to optimize the whole circuit with Tuning tool of ADS software, find a balance in some performance parameters of the LNA such as S_{11},S_{22},S_{21}, noise figure. The matching network of output terminal is shown in Figure 5.39.

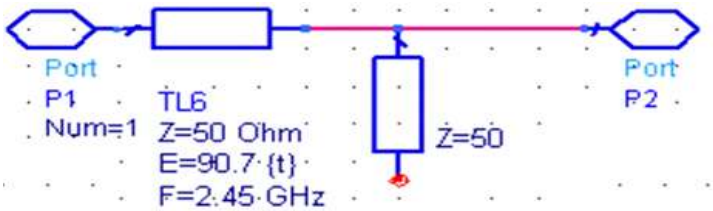


Figure 5.39: Matching network of output terminal

5.6.3.4 Determining the Size of Microstrip Line

FR4 substrate has chosen for Microstrip lines. Its relative dielectric constant Ɛr = 4.4, thickness h = 0.8 mm, permeability *Mur* = 1,metalconductivity *Cond* = 5.88e7,conductor thickness T = 0.035 mm. Width and length of matching Microstrip line can be easily computed with Microstrip line computational tool LinCale of ADS software. The schematic is shown in Figure 5.40.

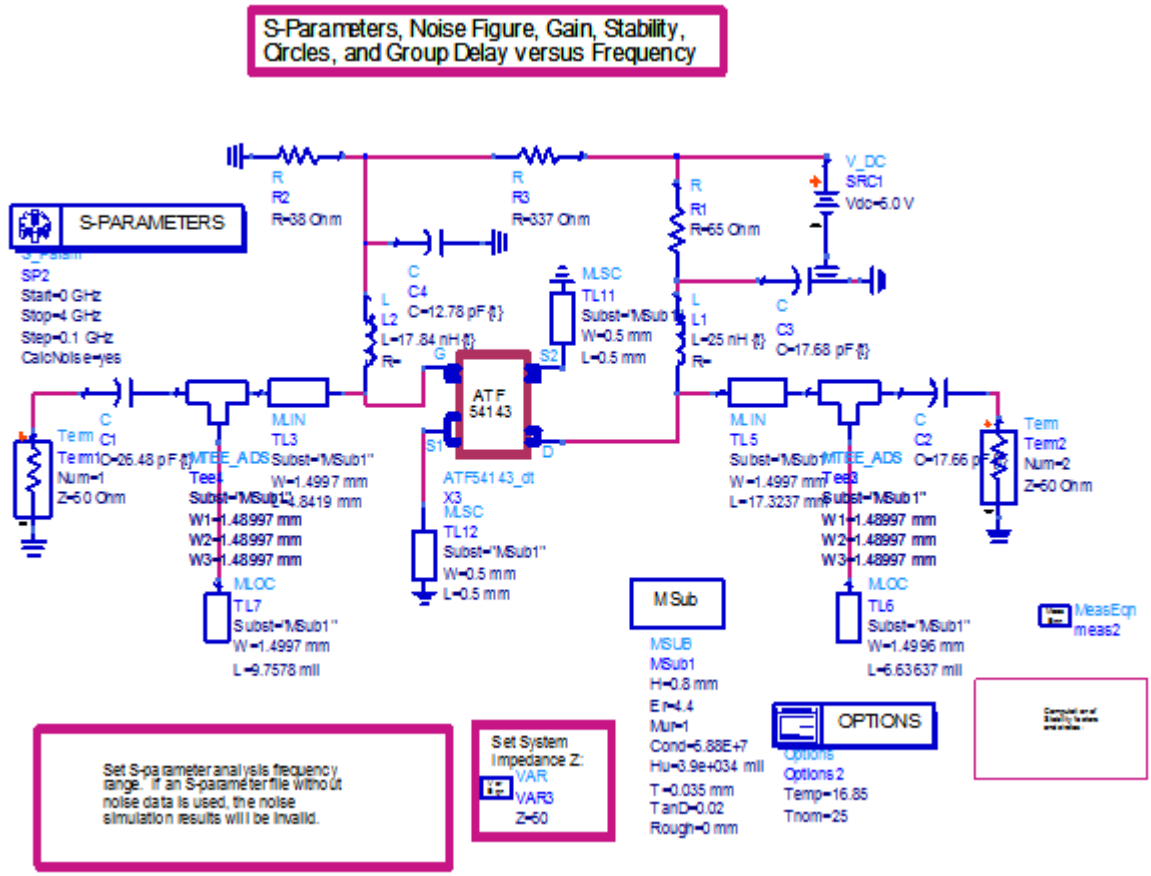


Figure 5.40: Schematic of Microstrip LNA

5.6.3.4.1 Simulation Result

(i) S parameters: The simulation results are shown in figure 5.41 to figure 5.44. Form figure 5.41 and figure 5.42, it can be seen that in operating frequency range input reflection coefficient S_{11} is -17.067 and output reflection coefficient S_{22} is -13.012 dB, and form figure 5.13 gain is 13.337 dB, gain flatness is good.

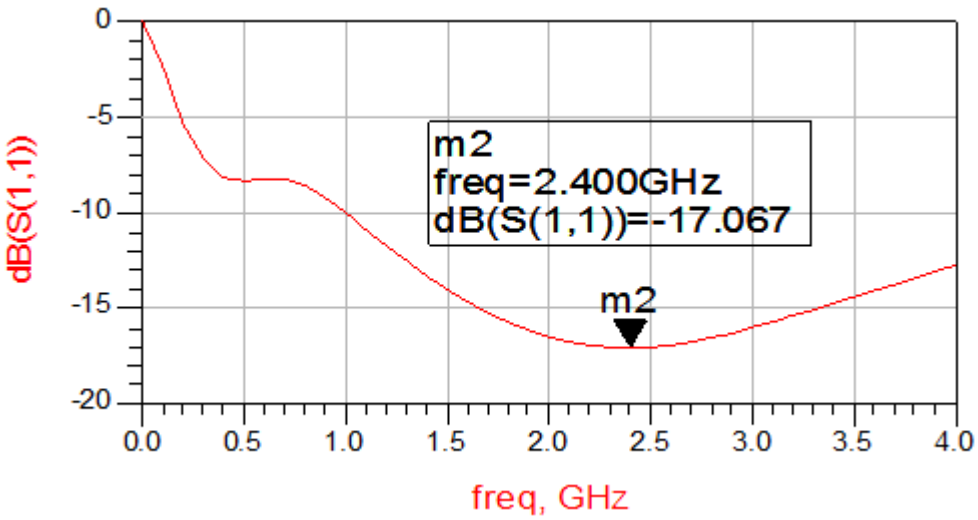


Figure 5.41: Scattering parameter S_{11}

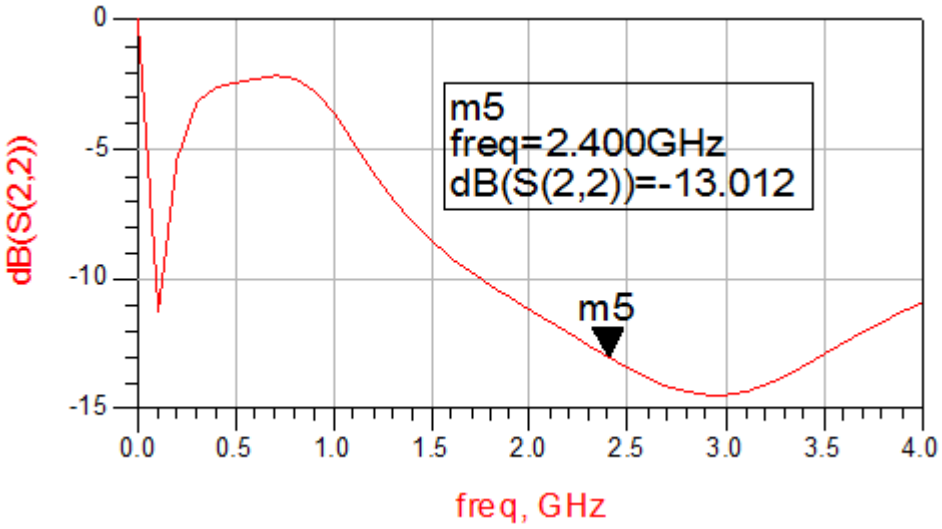


Figure 5.42: Scattering parameter S_{22}

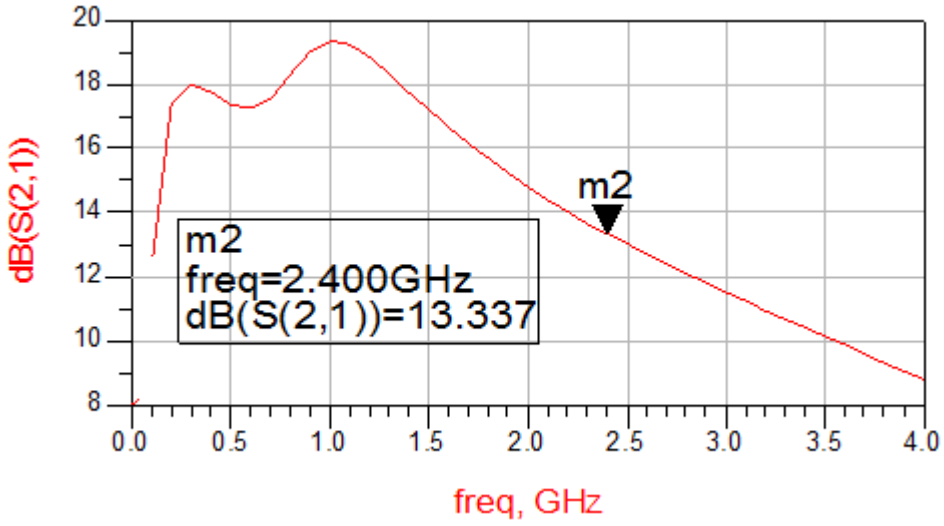


Figure 5.43: Forward Gain (S_{21})

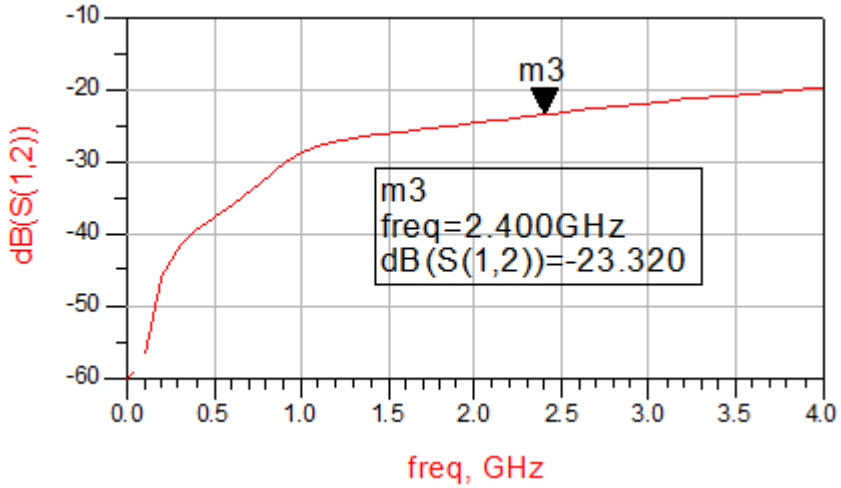


Figure 5.44: Scattering parameter S_{12}

(ii) Noise Figure

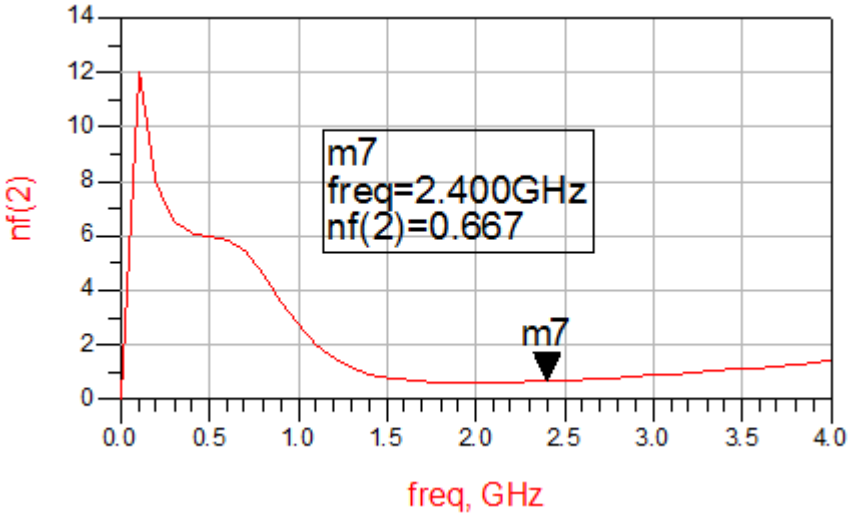


Figure 5.45: Noise Figure (NF)

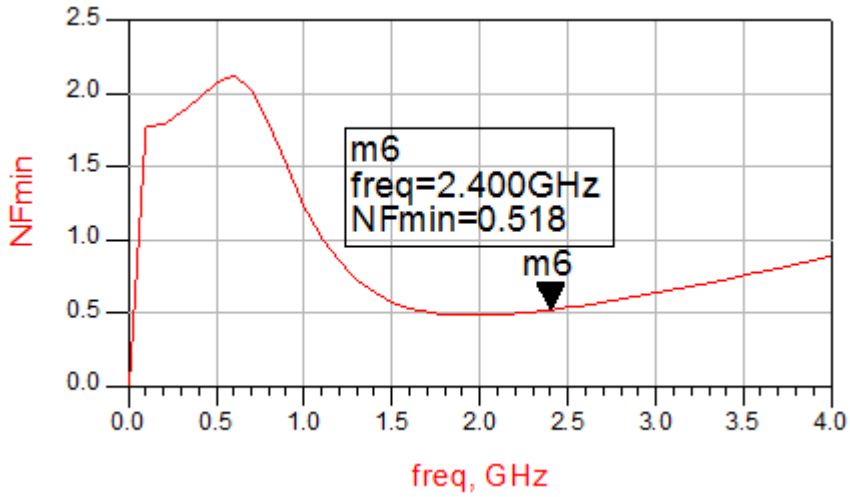


Figure 5.46: Minimum Noise Figure (NF_{min})

Simulation result of Noise Figure as shown in figure 5.45. This Noise Figure indicates the noise performances of device at high frequency and its value is 0.667 dB at 2.45 GHz frequency and in the Figure 5.46 shows the minimum Noise Figure, with simulated value is 0.518 dB

5.6.4 Results obtained from Simulation

Based on the simulation result Table 5.7 shows the various performance parameters result of the design.

Table 5.7: Performance Parameters

Performance parameters	Using discrete component	Using Microstrip lines
S_{11}	-15.08 dB	-17.06 dB
S_{12}	-20.13 dB	-23.32 dB
S_{21}	15.27 dB	13.33 dB
S_{22}	-10.26 dB	-13.02 dB
Noise Figure (NF)	0.386 dB	0.667 dB
Minimum Noise Figure (NF_{min})	0.379 dB	0.518 dB
Stability Factor(K)	1.009	1.067
Bandwidth	500 MHz	400 MHz

As shown in the above table the values of matching parameters S_{11}, S_{12}, and $S_{22}$are -17 dB, -23dB and -13dB respectively, with targeted values as shown in table 5.1, of that is less than -10dB, So desired values have achieved. Targeted gain is greater than 12dB whereas gain of this design circuit is 13.33dB and noise figure must be less than 2dB as given in table 5.1, noise figure of this design is 0.667 dB and minimum noise figure is 0.518dB and all the other performance parameters values are better than target value.

Chapter 6

Results

The LNA was designed to operate at 2.45 GHz frequency, simulated by using Advanced Design System (ADS) designed by Agilent Technologies. The key issue in the design, Gain, noise figure, Power consumption and stability was considered.

LNA designed using current mirror and current source, the simulation results are gain 12.139 dB, noise figure 0.699 dB, minimum noise figure 0.501 dB, input reflection coefficient -11.200 dB, output reflection coefficient -13.503 dB, reverse isolation coefficient -1.384 dB, power consumption 11.63 mW with supply voltage 1.5 V.

LNA designed using additional cascode stage, the simulation results are gain 13.625 dB, noise figure 0.866 dB, minimum noise figure 0.783 dB, input reflection coefficient -7.664 dB, output reflection coefficient -56.733 dB, reverse isolation coefficient -0.143 dB, power consumption 8.10 mW with supply voltage 1.5 V

LNA designed using C-S with a simple C-S stage added to the cascode, the simulation results are gain 26.486 dB, noise figure 1.268 dB, minimum noise figure 1.044 dB, input reflection coefficient -5.841 dB, output reflection coefficient -52.533 dB, reverse isolation coefficient -18.823 dB, power consumption 4.49 mW with supply voltage 1.2 V

The power consumed by the designed or simulated circuit is 4.49 mW, which is very low power consumed by the design and gain of the design is also very good, which is 26.486 dB. Power consumption and gain of LNA design is the main advantages.

Now LNA designed using HEMT (using microstrip lines) at 2.4 GHz operating frequency, simulated by ADS designed by Agilent Technologies. After the simulation it has achieved the gain 13.33 dB, noise figure 0.667dB, minimum noise figure 0.518 dB, input reflection coefficient -17.06 dB, output reflection coefficient -13.02 dB, reverse isolation coefficient -23.32 dB, stability is greater than 1 with supply voltage 5 V using microstrip lines.

Chapter 7

Conclusions

6.1 Conclusions

In order to design any circuit, it is always better to abstract away its complexity. In this project design a low power high gain low noise amplifier for 2.45 GHz for Wireless Applications covered all the important details required for the general low noise amplifier. And also a novel low noise amplifier is designed and simulated keeping view low power, high gain and low noise figure for given frequency applications. This design used inductive source degeneration topology as it provided good matching and low noise figure as compared to other topology. Additionally, power constrained noise optimization technique was used for power and noise optimization. The LNA was designed to operate at 2.45 GHz frequency, simulated by using Advanced Design System (ADS) designed by Agilent Technologies. The key issue in the design, Gain, noise figure, stability was considered. After the simulation it has achieved the Gain 26.486dB, Noise Figure 1.268dB, input reflection coefficient -5.841dB, output reflection coefficient -52.533dB, reverse isolation coefficient -18.823dB, power consumption 4.49mW with supply voltage 1.2 V using C-S LNA with a simple C-S stage added to the 'cascode'.

The power consumed by the designed or simulated circuit is 4.49 mW, which is very low power consumed by the design and gain of the design is also very good, which is 26.486dB. Power consumption and gain of design LNA is the advantages and noise figure, which is also less than 2 dB is an advantage as per the targeted specification.

LNA is also designed using HEMT (using microstrip lines) at 2.4 GHz operating frequency, After the simulation it has achieved the gain 13.33 dB, noise figure 0.667dB, minimum noise figure 0.518 dB, input reflection coefficient -17.06 dB, output reflection coefficient -13.02 dB, reverse isolation coefficient -23.32 dB, stability is greater than 1 with supply voltage 5 V using microstrip lines.

Furthermore, throughout the whole design, transistor was stable. The level of satisfaction of this project work is satisfactory. However, due to the parasitic effects and unavailability of required components, there are some deviations from expectations in the simulated results. This project work gives a closer and wide view of all the relevant background theories and design technologies to the designer.

6.2 Future Scope of present work

For investigating design of Low Noise Amplifier for RF application following work may be extended:

- Noise figure of the design LNA improved using HEMT technology but it can also be improved using MOS because MOS has already given a great gain in compression to the HEMT technology.
- This work has been implemented as a schematic design, furthermore it can be continued to layout implementation and perform post layout simulation, and could be fabricated and used some wireless applications at 2.4- 2.5GHz.
- Spiral inductor occupy large area so either inductor less or active inductors may be used for design purpose.
- Band gap reference generators may be used instead of resistors for providing bias as they produce less noise and are temperature independent.

Though the responses are satisfactory, but still there are scopes to improve the performances. Some of the circuits can be improved in design and with more proper optimization to have better responses.

In future, LNA can be design at 2.4 GHz for wireless applications using HEMT Technology, in which pHEMT having fallowing features: High linearity performance, Enhancement Mode Technology, Low noise figure, 800 micron gate width, Tape-and-Reel packaging option available and having following specifications: 2 GHz; 3V, 60 mA (Typ.), 36.2 dBm output 3rd order intercept, 20.4 dBm output power at 1 dB gain compression, 0.5 dB noise figure, 16.6 dB associated gain.

LNA for the wireless application design with pHEMT having following applications which are: Low noise amplifier for cellular/ PCS base stations, LNA for WLAN, WLL/RLL and MMDS applications, General purpose discrete E-PHEMT for other ultra low noise applications.

Hence, my future work is to design and implement a low noise amplifier for wireless application using pHEMT Technology with desecrate component and micro strip line.

REFERENCES

[1] Behzad Razavi, "RF Microelectronics", *Prentice Hall,* 1998.

[2] Hectir J. De Los Santos, "Radio Frequency Integrated Circuit Design", *Artec House*, 2003.

[3] D. K. Shaeffer and T.H.Lee, "A 1.5-V, 1.5-GHz CMOS Low Noise Amplifier" , *IEEE J. Solid-State Circuits,* vol. 32, no. 5, pp. 745-759, May 1997.

[4] A.J. Scholten and R. van Langevelde, "Compact modeling of noise in CMOS", *IEEE Conference on Custom Integrated Circuits,* 2006.

[5] Xiao-Dong Wang and Jia-you Song, "A LNA Design for WCDMA application in 0.18μm CMOS process", *IEEE International Conference on Microwave and Millimeter Wave Technology,* 2007.

[6] Michael T. Reiha and John R. Long, "A 1.2 V Reactive-Feedback 3.1-10.6 GHz Low Noise Amplifier in 0.13 μm CMOS", *IEEE J. Solid-State Circuits,* vol. 42, no.5, May 2007.

[7] T. Hui Teo and Wooi Gan Yeoh, "Low-Power Short-Range Radio CMOS Sub harmonic RF Front-End Using CG-CS LNA", *IEEE Transactions on Circuits and Systems-II Express Briefs*, vol.55, no.7, Jul. 2008.

[8] Andrea Bevilacqua and Ali M. Niknejad, "An Ultra-Wideband CMOS Low Noise Amplifier for 3.1-10.6 GHz Wireless Receivers", *IEEE J. Solid-State Circuits*, vol.39, no.12, Dec. 2004.

[9] Zhe-Yang Huang and Che-Cheng Huang, "A CMOS Low Noise Amplifier with RLC-Impedance Feedback for 3-5GHz Ultra-Wideband Wireless System", *IEEE International Symposium on Integrated Circuits*, 2007.

[10] Shila Shamsadini, Neda Bathaei and Farokh Hojat Kashanib, "0.18um 3.1-10.6GHz CMOS UWB LNA with 25 ± ldB Gain 2010", *IEEE Conference on Enabling Science and Nanotechnology*, Dec. 2010.

[11] D. K. Shaeffer and T.H.Lee, "A 1.5-V, 1.5-GHz CMOS Low Noise Amplifier", *IEEE J. Solid-State Circuits*, vol. 32, no. 5, pp. 745-759, May 1997.

[12] Jerome Le Ny, Jonathan Mckenna and Bhavana Thudi, “A 1.9 GHz Low Noise Amplifier”, *EECS 522 Analog Integrated Circuits Project*, Winter 2002.

[13] H. Hashemi and A. Hajimiri, “Concurrent Multiband Low-Noise Amplifiers—Theory, Design and Applications”, *IEEE Trans. Microwave Theory Tech.*, vol. 50, pp. 288-301, Jan. 2002.

[14] Andrea Bevilacqua and Ali M. Niknejad, “An Ultra-Wideband CMOS Low Noise Amplifier for 3.1-10.6-GHz Wireless Receivers”, *IEEE J. Solid-State Circuits*, vol.39, no.12, Dec. 2004.

[15] Christopher Bowick, John Blyler and Cheryl Ajluni, “RF Circuit Design”, 2nd ed., *Newnes*, 2007.

[16] Qiang Li and Yue Ping Zhang, “A 1.5-V 2-9.6-GHz Inductorless Low Noise Amplifier in 0.13μm CMOS”, *IEEE Transactions on Microwave Theory and Techniques*, vol.55, no.10, Oct. 2007.

[17] Zhe-Yang Huang and Che-Cheng Huang, “A CMOS Low Noise Amplifier with RLC-Impedance Feedback for 3-5GHz Ultra-Wideband Wireless System”, *IEEE International Symposium on Integrated Circuits*, 2007.

[18] Zhe-Yang Huang, Meng-Ping Chen, Yeh-Tai Hung and Che-Cheng Huang, “Design Considerations on Input Impedance Matching for Ultra-Wideband Low Noise Amplifier”, *IEEE Conference on Microwave and Millimeter Wave Technology*, 2008.

[19] Bevin G. Perumana, Stewart S.Taylor, Joy Laskar and Jing-Hong C. Zhan, “Resistive-Feedback CMOS Low Noise Amplifiers for Multiband Applications”, *IEEE Transactions on Microwave Theory and Techniques*, vol.56, no.5, May 2008.

[20] Yu-Lin Wang, Chi-Feng Lin and Man-Long Her, “Design and Implementation of Differential LNA for WiMAX system”, *IEEE Asia-Pacific Conference on Communications*, 2009.

[21] Jenn-Tzer Yang, Yi- Yuan Hang and Yuan-Hao Lee, “A 0.18um CMOS Using High- Q Active Inductors for Multi-Band Low Noise Amplifier”, *IEEE Conference on Electron Devices and Solid-State Circuits*, 2007.

[22] Michael T. Reiha and John R. Long,"A 1.2 V Reactive-Feedback 3.1-10.6 GHz Low Noise Amplifier in 0.13 μm CMOS", IEEE J. Solid-State Circuits, vol. 42, no.5, May 2007.

[23] A.J. Scholten and R. van Langevelde, "Compact modeling of noise in CMOS", *IEEE Conference on Custom Integrated Circuits*, 2006.

[24] Wai-Kai Chen "Active Network Analysis" *Advance series in Electrical and Computer Engineering*, vol.2.

[25] Lee T.H. "The Design of CMOS Radio Frequency Integrated Circuits" (second edition), *publishing House of Electronics industry*, 2006.

[26] C. H. Liao and H.R. Chuang, "A 5.7 GHz 0.18nm CMOS gain-controlled differential LNA with current reuse for WLAN receiver", *IEEE Microw. Wireless compon.Lett.* , vol.13, no.12,pp. 526-528, Dec.2003.

[27] Jung-Suk Goo, Hee-Tae Ahn, Donald J. Ladwing, Zhiping Yu, Thomas H. Lee and Robert W. Dutton, "A noise optimization technique for integrated low noise amplifiers", *IEEE J. Solid-State Circuits*, vol. 37, no.8, pp. 994-1002, Aug. 2002.

[28] Jiwei Chen, bingxue Shi, "Analysis and optimization of the impact of channel resistance on CMOS LNA noise Performance", *Microelectronics Journal* 33, p. 1027-1031. (2002).

[29] Derek K. Shaeffer, and Thomas H. Lee, "A 1.5-V, 1.5-GHz CMOS Low Noise Amplifier," *IEEE J. Solid-state Circuits*, vol. 32, no.5, pp. 745-759, May 1997.

[30] S. Ganesan, E. Sanchez-Sinencio, and J. Silva-Martinez, "A highly linear low noise amplifier," *IEEE Trans. Microw. Theory Tech*., vol. 54, no. 12, pp. 4079-4085, Dec. 2006.

[31] David M. Pozar, "Microwave and RF Wireless System," *John Willey & Sons, Inc. Third Edition*, 2000.

[32] Derek K. Shaeffer, and Thomas H. Lee, "A 1.5 V, 1.5 GHz CMOS Low Noise Amplifier," *IEEE Journal of Solid-State Circuit*, Vol.32, No.5, pp.745, May 1997.

[33] H.Hashemi and A.Hajimiri, Concurrent Multiband Low-Noise Amplifiers "Theory, Design and Applications", *IEEE Trans. Microwave Theory Tech.*, vol. 50, pp. 288-301, Jan. 2002.

[34] Nguyen, T., et. al., "CMOS Low Noise Amplifier Design Optimization Techniques," *IEEE Transactions on Microwave Theory and Techniques*, May, 2004.

[35] Sahoolizadeh, H., "Design and simulation of Low Noise Amplifier Circuit for 5 GHz to 6 GHz," *World Academy of Science, Engineering and Technology* 51, 2009, pp. 99–102.

[36] Othman, M.A., M.M. Ismail, H.A.Sulaiman, M.H.Misran "LC Matching Circuit For 2.4 Ghz LNA Using Avago ATF-54143", *IJERA, Volume:2 Issue:4*,July-Agust 2012,pp.2055-2059.

[37] M. E. Kaamouchi, M. S. Moussa, P. Delatte, G. Wybo, A. Bens, J.-P.Raskin, and D. Vanhoenacker-Janvier, "A 2.4 GHz fully integrated ESD-protected low-noise amplifier in 130-nm PD SOI CMOS technology," *IEEE Trans. Microwave Theory Tech*., vol. 55, pp. 2822-2831, Dec. 2007.

[38] A. V. Do, C. C. Boon, M. A. Do, K. S. Yeo, and A. Cabuk, "A subthreshold low-noise amplifier optimized for ultra-low-power applications in ISM band," *IEEE Trans. Microwave Theory Tech*., vol. 56, pp. 286-292, Feb. 2008.

[39] M. Cimino, H. Lapuyade, Y. Deval, T. Taris, and J.-B.Begueret, *"Design of a 0.9 V 2.45 GHz self-testable and reliability-enhanced CMOS LNA,"* IEEE J. Solid-State Circuits, vol. 43, pp. 1187-1194 May 2008.

[40] Nadia. A. Belgacem, F. , "A low power low noise CMOS amplifier for Bluetoothapplications," *Applied Electronics (AE), 2013 International Conference*, year: 2013.

Appendix A

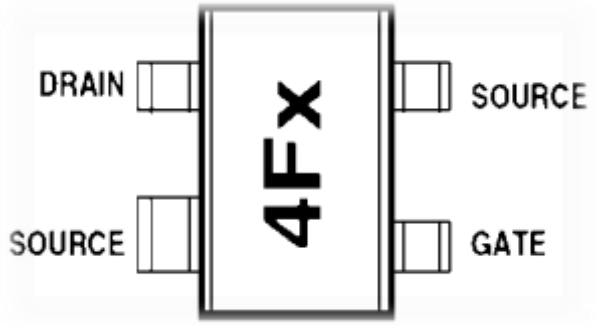
ATF-54143

Low Noise Enhancement Mode Pseudomorphic HEMTin a Surface Mount Plastic Package

Description

Avago Technologies' ATF-54143 is a high dynamic range,low noise, E-PHEMT housed in a 4-lead SC-70 (SOT-343)surface mount plastic package.The combination of high gain, high linearity and lownoise makes the ATF-54143 ideal for cellular/PCS basestations, MMDS, and other systems in the 450 MHz to 6GHz frequency range.

Pin Connections and Package Marking



Features

- High linearity performance
- Enhancement Mode Technology
- Low noise figure
- Excellent uniformity in product specifications
- 800 micron gate width
- Low cost surface mount small plastic package SOT-343 (4 lead SC-70)
- Tape-and-Reel packaging option available
- Lead-free option available

Specifications

- GHz; 3V, 60 mA (Typ.)

- 36.2 dBm output 3rd order intercept
- 20.4 dBm output power at 1 dB gain compression
- 0.5 dB noise figure
- 16.6 dB associated gain

Applications

- Low noise amplifier for cellular/PCS base stations
- LNA for WLAN, WLL/RLL and MMDS applications
- General purpose discrete E -PHEMT for other ultra low noise applications

ATF-54143 Electrical Specifications

T_A = 25°C, RF parameters measured in a test circuit for a typical device

Symbol	Parameter and Test Condition	Units	Min.	Typ.	Max.
V_{gs}	Operational Gate Voltage V_{ds} = 3V, I_{ds} = 60 mA	V	0.4	0.59	0.75
V_{th}	Threshold Voltage V_{ds} = 3V, I_{ds} = 4 mA	V	0.18	0.38	0.52
Id_{ss}	Saturated Drain Current V_{ds} = 3V, V_{gs} = 0V	µA		1	5
G_m	Transconductance V_{ds} = 3V, gm = $\Delta Id_{ss}/\Delta V_{gs}$ ΔV_{gs} = 0.75 - 0.7 = 0.05V	mho	230	410	560
Ig_{ss}	Gate Leakage Current V_{gd} = V_{gs} = -3V	µA			200
NF	Noise Figure f = 2 GHz V_{ds} = 3V, I_{ds} = 60 mA f = 900 MHz, V_{ds} = 3V, I_{ds} = 60 mA	dB		0.5 0.3	0.9
G_a	f = 2 GHz ,V_{ds} = 3V, I_{ds} = 60 mA f = 900 MHz, V_{ds} = 3V, I_{ds} = 60 mA	dB	15	16.6 23.4	18.5
OIP3	f = 2 GHz, V_{ds} = 3V, I_{ds} = 60 mA f = 900 MHz, V_{ds} = 3V, I_{ds} = 60 mA	dBm	33	36.2 35.5	
P1dB	f = 2 GHz, V_{ds} = 3V, I_{ds} = 60 mA f = 900 MHz, V_{ds} = 3V, I_{ds} = 60 mA	dBm		20.5 18.4	