Dissertation

On

DESIGN OF OSCILLATORS USING OTRA

Submitted in partial fulfilment of the requirements
For the award of degree of

Master of Technology
In
VLSI Design and Embedded System

Submitted By
GURUMURTHY KOMANAPALLI
(Roll no.:- 2K12/VLSI/10)

Under the guidance of
Dr. Rajeshwari Pandey
(Associate Professor)

Department of Electronics and Communication Engineering
Delhi Technological University
(Formerly Delhi College of Engineering)
Bawana Road, Delhi-110042
(2012-2014)

CERTIFICATE

DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of Engineering)
BAWANA ROAD, DELHI – 110042
Department of Electronics & Communication Engineering

This is to certify that the report entitled **"*Design of Oscillators using OTRA (Operational Transresistance Amplifier)*"**submitted by **Gurumurthy Komanapalli**,**Roll.No.2k12/VLSI/10** in partial fulfilment for the award of degree of Master of Technology in VLSI Design & Embedded System at **Delhi Technological University, Delhi**, is a bonafide record of student's own work carried out by him under my supervision and guidance in the academic session 2012-14. The matter embodied in dissertation has not been submitted for the award of any other degree or certificate in this or any other university or institute.

Dr. Rajeshwari Pandey

ASSOCIATE PROFESSOR
Dept. of Electronics &Communication Engineering
Delhi Technological University
(Formerly Delhi College of Engineering)
Delhi – 110042

ACKNOWLEDGEMENT

It has been rightly said, “We are build on the shoulders of others” for everything we have Achieved the credit goes to our faculty members. I would like to express my immense gratitude to my supervisor, **Associate.Prof.Dr. Rajeshwari Pandey** for her enthusiasm, encouragement, patience, & timely support. It is my privilege to have worked under her supervision. Her invaluable guidance & helpful discussion at every stage of this project helped me in timely materialization & successful completion of this project. My special thanks to **Dr. Neeta Pandey** for her support and guidance. I am grateful to my parents and my elder brothers Dr.K.V.L.Narayana and Dr.K.Sunil kumar for their moral support. They have been always around to cheer me up, in the odd times of this work. I am also thankful to my classmates for their unconditional support and motivation during this work.

Submitted by:

Gurumurthy Komanapalli
2K12/VLSI/10
M. Tech. (VLSI DESIGN & EMBEDDED SYSTEM)

ABSTRACT

The reduction of the minimum feature size of an MOS transistor for digital VLSI circuits has been ongoing for the past few decades. As the channel length is scaled down into deep sub micrometer dimensions, the lower power supply voltage is required to ensure the device reliability. To be compatible with digital VLSI technologies, analogue integrated circuits, which can operate at low supply voltages, are also receiving significant attention. This has resulted in development of various current mode analog building blocks and operational transresistance amplifiers (OTRA).OTRA is high gain current input voltage output device, both the input and output terminals are characterized by low impedance. OTRA being a current mode building block inherits the advantages of current mode processing, the input terminals are virtually grounded leading to circuits that are insensitive to stray capacitances. Being a current processing device the OTRA has a bandwidth independent of the device gain and is also not slew limited in the same manner as an OP-AMP.

Oscillators are used in various types of applications for these applications low value of total harmonic distortion (THD) is an essential requirement as higher harmonics have detrimental effects on electrical equipment The objective of the project is to design circuits of various types of oscillators i.e., Quadrature oscillator,wein bridge oscillator, sinusoidal oscillator using allpass section using Operational Transresistance Amplifier and studying THD analysis and simulate their MOS-C equivalent circuits for minimizing the chip area and for making these circuits electronically tuneable. These OTRA based designs are best suited for the Low Power and High Speed applications and Low Power Medical Devices apart from its traditional field of application i.e. Process Industry.

TABLE OF CONTENTS

Chapter 4 Design of sinusoidal oscillators using OTRA

Chapter 5 Operational transresistance amplifier based weinbridge oscillator

Chapter 6 OTRA based voltage mode third order quadrature oscillator

Chapter 7 Conclusion and Future Work

LIST OF FIGURES

LIST OF TABLES

ABBREVATIONS

CC1	First generation current conveyor
CCII	Second generation current conveyor
CDBA	Current differencing buffered amplifier
CFA	Current Feedback amplifier
CDTA	Current Difference Trans conductance Amplifier
FTFN	Four Terminal Floating Nullor
OTA	Operational Transconductance Amplifier
OTRA	Operational Trans Resistance Amplifier
MDCC	Modified differential current conveyor
THD	Total Harmonic Distortion
CCII	Second Generation current conveyor
DCVC	Differential Current Voltage Conveyor
CDBA	Current Differencing Buffered Amplifier
CFOA	Current Feedback Operational Amplifier
CCCDTA	Current-controlled Current Differencing Transconductance
QO	Quadrature oscillators
MOS-C	Mosfet- Capacitor
CO	Condition of oscillation
FO	Frequency of oscillation

CHAPTER: 1
INTRODUCTION

1.1 Background

The design of Analogue IC has traditionally been hindered by process technology as generally most of the technologies have been designed to optimize digital circuits. This draw back results in an apparent design time syndrome, where a single IC may contain only 20% analogue functions which take 80% of the design time[1]. The reduction of the minimum feature size of an MOS transistor for digital VLSI circuits has been ongoing for the past few decades. As the channel length is scaled down into deep sub micrometer dimensions, the lower power supply voltage is required to ensure the device reliability. To be compatible with digital VLSI technologies, analogue integrated circuits, which can operate at low supply voltages, are also receiving significant attention. This has resulted in development of various current-mode analogue signal processing techniques for high performance analogue circuit and system architectures, with emphasis on high speed.

The information processed by lumped electric networks can be represented by either nodal voltages or branch currents of networks. The analog circuits, where the circuit performance is determined in terms of voltage levels at various nodes including input and output nodes, are referred to as voltage-mode (VM) circuits. The advantage of Current-mode analogue signal processing over voltage signal processing is speed of operation. In voltage mode circuits the transistor are useful almost up to its f_T. Recent advances in integrated circuit technologies provide solutions to the problems that are occurring in many circuits and systems by utilizing the potential of current mode circuits. Recent developments of current-feedback operational amplifiers, which exhibit an almost constant bandwidth irrespective of closed-loop gain, together with very high slew rate, and better signal linearity and better accuracy illustrate the advantages of using a current-mode approach. Idea of the current feedback amplifiers dates back many years but it became practical with recent developments in truly complementary bipolar technology. Since they are designed for lower voltage swings, smaller supply voltages can be used. Simultaneously with the

development of current-mode applications, the mixed-mode circuits are also analyzed because of the necessity of optimizing the interface between the sub-blocks, which are working in different modes.

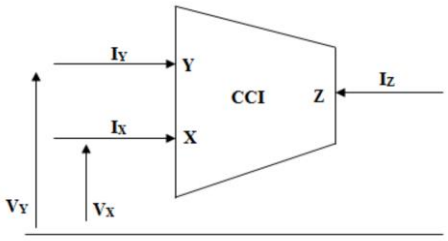
In CMOS technology, with mixed analogue and digital circuitry in VLSI, developments have centred on a new generation of analogue sampled data processing that may be referred to as switched or dynamic current circuits. These circuits include dynamic current mirrors; switched current filters memory cells and current copier. One of the primary motivations behind these developments has been the shrinking feature size of digital CMOS devices which necessitates the reduction of supply voltages. However, threshold voltage does not scale in a linear fashion with the reduction in minimum device length and so voltage domain behaviour will suffer as a consequence. Such difficulties can be overcome by operating exclusively or selectively in the current domain.

1.2 Evolution of Active Blocks[2]

Current-mode processing techniques gave tremendous impulse to the State-of-the-art analogue integrated circuit design and have resulted in development of a large number of analog building blocks (ABB). The current conveyors (CC), Current Feedback Amplifier (CFA) and Operational Trans conductance Amplifier (OTA), are the most traditional among those. A brief introduction of these ABBs is given in the following subsection.

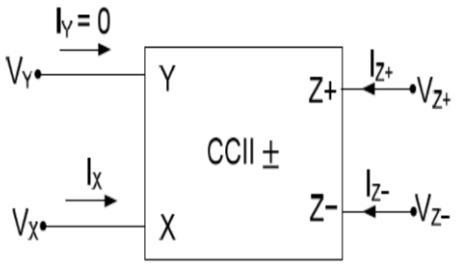
First Generation of Current Conveyor (CC I)

It is a three terminal device as shown in Fig. 1.1.The impedance level at port X and Y of first generation current conveyor is very low (ideally zero) whereas impedance level of port Z is very high (ideally infinite).The application of CCI± becomes difficult because both the ports X and Y have zero input impedance in order to sink currents. The port Y needs to control a current rather than to control a voltage, which is usually difficult to obtain in practical designs. This is the perhaps the greater limit of the CCI device and this reduces its flexibility and versatility.



$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ v_Z \end{bmatrix}$$

Fig.1.1 The CC I with its port relations.



$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix}$$

Fig.1.2The CC II with its port relations.

Second generation current conveyor (CCII) the circuit symbol for CC II is shown in Fig 1.2. The CC II differs from the first generation current conveyor in a sense that the port Y is a high impedance port i.e. there is no current flowing into port Y. The device comprises a low impedance current input/voltage output terminal X, a high-impedance voltage input terminal Y and a current output terminal Z. The port Y of the second generation current conveyor is used as a voltage input and port Z is used as a current output port. Whereas, the port X can be used as a voltage output or as a current input port. Therefore this current conveyor can be used to process both voltage and current signals.

Current Feedback Amplifier (CFA) was developed to improve the finite gain-bandwidth product of the conventional voltage - feedback operational amplifier is improved by the use of CFA. It can provide not only a constant bandwidth independent of closed loop gain but also a high slew rate capability. Usage of CFA as a basic building block in active filter design is highly beneficial on account of these factors. CFA is an operational Tran's impedance amplifier and is internally a CCII+ followed by a voltage follower as shown in Fig. 1.3.

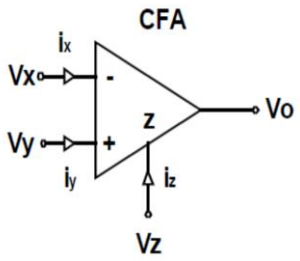


Fig.1.3 symbol Current feedback amplifier

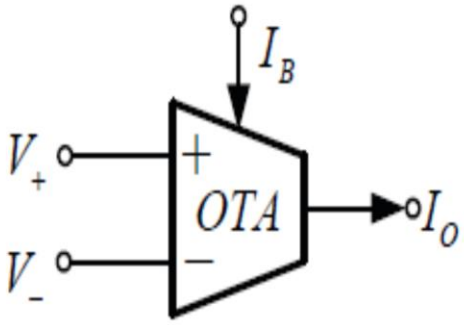


Fig 1.4(a) OTA

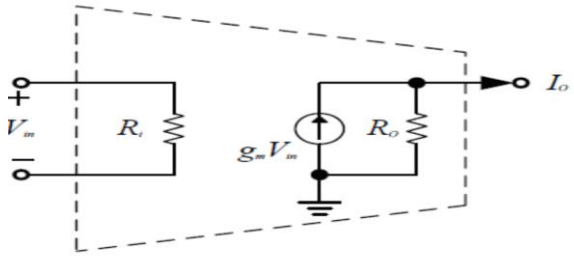


Fig 1.4(b) OTA Equivalent Circuit

Operational transconductance amplifier (OTA) is a voltage controlled current source with constant transconductance and infinite input/output impedances, that takes the differential voltage as input and provide current as the output. The output current is related to the differential input voltage as:

$$I_O = g_m (V_+ - V_-) \qquad (1.1)$$

The OTA symbol and equivalent circuit is shown in fig.1.4(a) and fig 1.4(b) respectively.

The evolution of various ABBs is happening by modification of the basic elements such as voltage feedback Amplifier (VFA), CFA, OTA and particularly current conveyors.The motivation behind such modifications is to increase the application potential of the element. The internal structure of the element should be simple in order to have high-speed operation and low power consumption. The electronic

control is yet another important requirement and has resulted in the evolution of various new elements.

In following subsections some of the ABBs derived out of combinations of VFA, CFA, OTA and CC are introduced.

Four Terminal Floating Nullor (FTFN) was introduced after the advent of Current Feedback amplifier. As part of the process of development of continuous-time circuits FTFN was introduced as more flexible and versatile building block than an operational amplifier (OP-AMP) or a second-generation current conveyor (CCII) .It is evolved by cascading CFAs. The circuit symbol of the FTFN and its realization using CFAs is shown in Fig.1.5.

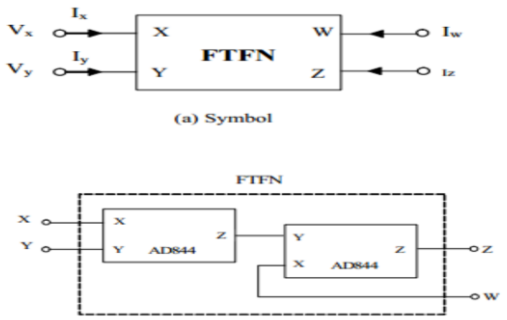


Fig 1.5 Four Terminal Floating Nullor.

Current Differencing Buffered Amplifier (CDBA) is a current-mode component also evolutes from CFA cascading, It offers advantageous features such as high slew rate, wide bandwidth absence of parasitic capacitance, and simple implementation. Since the CDBA consists of a unity-gain current differential amplifier and a unity-gain voltage amplifier, both voltage mode and current mode based circuits can be implemented using it. CDBA is represented by the circuit symbol shown in Fig. 1.6 (a) and its CFA based realization is depicted in Fig.1.6 (b).

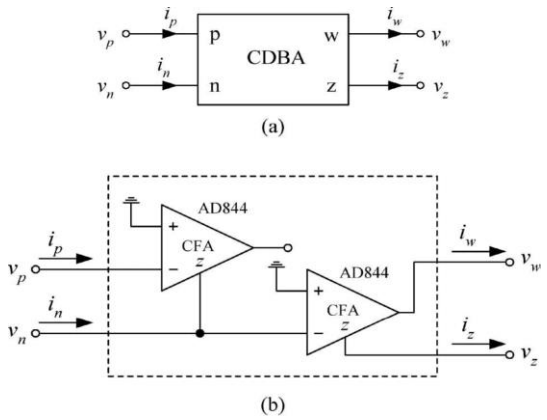


Fig.1.6 (a) symbol of CDBA
(b) Structure of CDBA using AD844

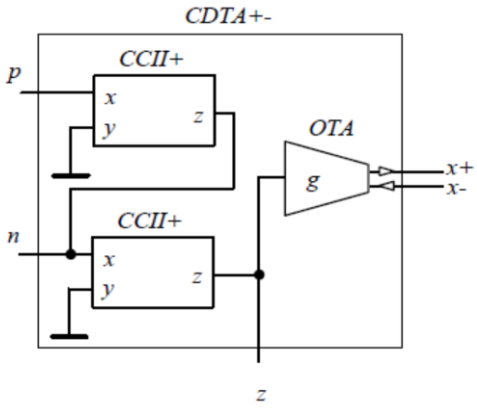


Fig 1.7 Structure of CDTA

Current Difference Trans conductance Amplifier (CDTA) is designed by adding two CC IIs and an operational transconductance amplifier (OTA) as is shown in Fig. 1.7. It has two current inputs p and n and the difference of these currents flows from terminal z into an outside load. The voltage across the z terminal is transferred by a transconductance to a current that is taken out as a current pair to the ±x terminals. In general, the transconductance is controllable electronically through an auxiliary port.

Operational transresistance amplifiers (OTRA) OTRA is high gain current input voltage output device implementing a current controlled voltage source (CCVS).The circuit symbol for OTRA is shown in Fig 1.8(a). It can be implemented using two CFAs as shown in Fig 1.8(b).

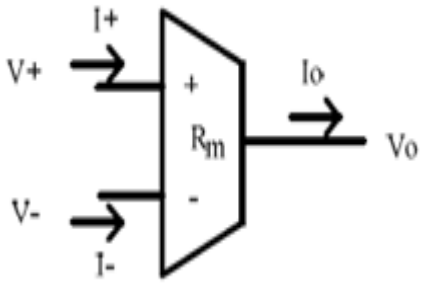


Fig 1.8(a) symbol of OTRA

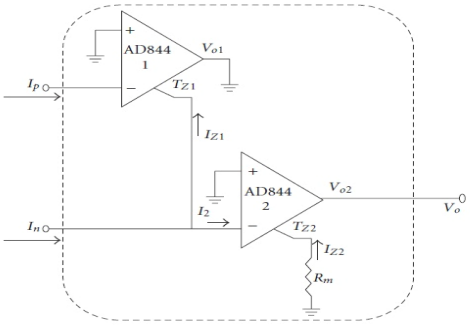


Fig 1.8(b). OTRA implementation using CFA

The evolution of various ABBs using the basic blocks is summarised in Fig. 1.9.

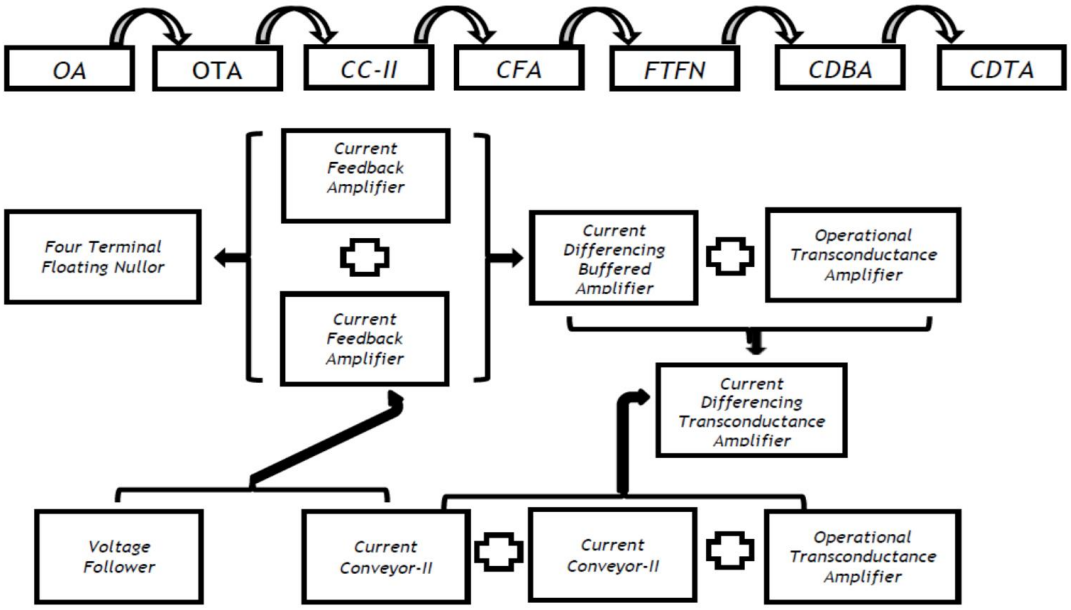


Fig.1.9 Evolution of Active Blocks [2].

1.3 Motivation

The OTRA is a high gain current input voltage output device. It has two input terminals which are virtually grounded and one low impedance output terminal. Both input and output terminals of the OTRA are characterized by low impedance resulting in circuits that are insensitive to stray capacitances. Since the OTRA has a current input and voltage output, a shunt- shunt feedback configuration is used, which places the feedback network and amplifier in parallel. A parallel configuration is suitable for low voltage operations, as it minimizes stacking of transistors thus providing more head room for signal swing. Using current feedback techniques, OTRAs have a bandwidth almost independent of closed-loop voltage gain. It provides advantages of current mode design techniques and gives voltage output, therefore, can directly drive voltage mode circuits.

1.4 Objective

Signal generators are an important class of circuits and find wide application in electronic system design. These can broadly be classified as (i) sinusoidal and (ii) non linear oscillators. Sinusoidal oscillators are widely used in consumer electronic equipment (such as radios, TVs, and VCRs), in test equipment (such as network analyzers and signal generators), and in wireless systems. For these applications low value of total harmonic distortion (THD) is an essential requirement as higher harmonics have detrimental effects on electrical equipment.

Non linear generators such as pulse, ramp and saw tooth oscillators, find use in timing and control applications. Pulse oscillators are commonly found in digital-systems clocks, and ramp oscillators are found in the horizontal sweep circuit of oscilloscopes and television sets.

The objectives of the project is

1. To perform exhaustive literature survey in the field of sinusoidal signal generation using OTRA and identify the research gaps.

2. To develop new / additional oscillator circuits using OTRA with an aims of providing design with better quality response such as independent control of pole frequency and quality factor, sensitivity towards parameter variation and total harmonic distortion.

1.5 Related Literature and Scope of the project

1.5.1 The OTRA realizations

As OTRA can be operated in voltage, current and mixed modes find its importance in numerous applications making it as a one of the basic analog building block. In the year 1992 J. J. Chen, H. W. Tsao & C. C. Chen [3] introduced the first CMOS circuit of OTRA. In Reference [4] which is published in 1995 shows that the input terminals of OTRA being virtually grounded, because of this property the advantage is the circuits designed using OTRA were insensitive to stray capacitances . In 1999 Salama and Ahmed M. Soliman introduced a simple CMOS realization of OTRA based on cascaded connection of modified differential current conveyor

(MDCC) and a common source amplifier [5]. In [6] they proposed a new circuit based on same cascaded connection of modified differential current conveyor (MDCC) and a common source amplifier as in [5] but with improved performance and less number of transistors.

The Circuit proposed in [6] is based on same input stage of OTRA proposed in [5] and a differential gain stage is used instead of the single common source amplifier and a compensation circuit is used to compensate difference between the two drain voltages of input transistors. The circuit proposed in [7] is another modification of circuit presented in [6] where differential gain stage is used instead of the single common source amplifier. Several other CMOS realizations of OTRA are also available in literature [8-9].

1.5.2 The OTRA based sinusoidal Oscillators

A number of schemes have been proposed in the literature to realize OTRA based sinusoidal oscillators [10], [11]. Topology presented by U.Cam et al. is a single resistance controlled oscillators (SRCO) [11]. Quadrature oscillators (QO) are reported in [12], [13] – [14]. R.Pandey et al. have presented three topologies of multiphase sinusoidal oscillators (MSO) in [15].

Identifying the research gaps after literature survey in this project following four new sinsoidal oscillator circuits have been presented and their functionalities have been verified using PSPICE.

1. Sinusoidal oscillator based on inverting and noninverting integrators
2. Sinusoidal oscillator using single second order allpass filter
3. OTRA based Wein bridge oscillator
4. Third order Quadrature oscillator (QO)

References

[1] C Toumazou, C A Makris, F J Lidgey and D G Haigh "TOWARDS A NEW GENERATION OF ANALOGUE IC DESIGN ARCHITECTURES".

[2] Sheik ajaz bashir, N.A shah"Active device usage in filter design- An overview" International Journal of Scientific and Research Publications, Volume 2, Issue 6, June 2012 1 ISSN 2250-3153

[3] Chen, J. J., Tsao H. W., Chen, C. C. Operational transresistance amplifier Using CMOS Technology. Electronics Letters. 1992, vol. 28, no. 22, p. 2087–2088.

[4] Selquk Kiling and Ugur Cam "Operational Transresistance Amplifier Based First-Order Allpass Filter with an Application Example" The 47th IEEE International MidwestSymposium on Circuits and Systems

[5] Chen J. J., Tsao H. W., Liu S. and Chui W., Parasitic-capacitance-insensitive current-mode filters using operational transresistance amplifiers, IEE Proc. Circuits Devices and Systems 1995, vol. 142, no. 3, p. 186–192

[6] Salama K. N., Soliman A. M., CMOS operational transresistance amplifier for analog signal processing. Microelectron J. 1999, vol. 30, issue 3, p. 235–45.

[7] Mostafa H. and Soliman A.M., A modified CMOS realization of the operational transresistance amplifier Frequenz, 2006, vol. 60, p. 70-76.

[8] Kafrawy A. K. and Soliman A. M., "New CMOS Operational Transresistance Amplifier", International Conference on Microelectronics, 2008, p. 31-34

.

[9] Kafrawy A. K. and Soliman A. M., A modified CMOS differential operational transresistance amplifier (OTRA), Int. J. Electron. Commun. 2009, (AEU) vol. 63, p. 1067-1071.

[10] K. N. Salama, A. M. Soliman, "Novel oscillators using operational transresistance amplifier," Microelectrons Journal, vol. 31, pp. 39–47, 2000.

[11] U. Cam, "A Novel Single-Resistance-Controlled Sinusoidal Oscillator Employing Single Operational Transresistance Amplifier", Analog Integrated Circuits and Signal Processing, vol. 32, pp. 183–186, 2002.

[12] K. N. Salama, A. M. Soliman, "CMOS operational transresistance amplifier for analog signal processing applications," Microelectronics Journal, vol. 30, pp. 235–245, 1999.

[13].S. Kilinc, U. Cam, "Operational trans resistance amplifier based first- order all pass filter with an application Example," in proceedings of 47th IEEE international Midwest Symposium on circuits and systems I, pp. 65–68, 2004.

[14] S. Kilinc, U. Cam, "Cascadable all pass and notch filters employing single operational transresistance amplifier," Computers and Electrical Engineering, vol.31, pp. 391–401,2005.

[15] R. Pandey, N. Pandey, M. Bothra, S. K. Paul "Operational Transresistance Amplifier-Based Multiphase Sinusoidal Oscillators," Journal of Electrical and Computer Engineering vol. 2011, Article ID 586853, 8 pages doi:10.1155/2011/586853

1.6 Organization of Dissertation

The dissertation is organized as follows:

Chapter2:

Theory of oscillators

Chapter 3:

It describes various CMOS based internal circuit structure of OTRA. This is followed by the circuit characterisation of CMOS OTRA proposed by salama and solimon,and the output cimulations are done using PSPICE . This block is further used for functional verification of various proposed circuits

Chapter 4:

In this chapter two topologies of operational transresistance (OTRA) based second order sinusoidal oscillators are proposed. The proposed oscillators are designed using combination of all pass section and lossless integrators. The proposed topologies can be made fully integrated by implementing the resistors using matched transistors operating in linear region, which also facilitates electronic tuning of oscillation frequency. The non-ideality analysis of the circuit is also given and for high frequency applications self compensation can be used. Workability of the proposed oscillators is verified through PSPICE simulations using 0.5μm AGILENT CMOS process parameters.

Chapter 5:

This chapter presents OTRA based Wien bridge oscillatorThe harmonic analysis and non-ideality analysis of the circuit is also presented and for high frequency applications self compensation can be used. Workability of the proposed wein oscillator is verified through PSPICE simulations using 0.35μm AGILENT CMOS process parameters.

Chapter 6:

This chapter presents two topologies of OTRA based voltage mode third order Quadrature Oscillator. The proposed oscillators are designed using combination of

lossy and lossless integrators. The proposed topologies can be made fully integrated by implementing the resistors using matched transistors operating in linear region, which also facilitates electronic tuning of oscillation frequency. The non-ideality analysis of the circuit is also given and for high frequency applications self compensation can be used. Workability of the proposed QOs is verified through PSPICE simulations using 0.5μm AGILENT CMOS process parameters.

Chapter 7:

In this chapter the presented work is summarized and concluded.

CHAPTER2
Theory of oscillators

2.1 The Oscillator Feedback Loop

The basic structure of a sinusoidal oscillator [1] consists of an amplifier having transfer function $A(s)$and a frequency selective network connected in a positive-feedback loop with transfer function β (s), as shown in functional block diagram of Fig.2.1. Here x_s and x_o represent the input and output signals respectively and x_f is the feedback signal. The closed loop gain $A_f(s)$ of this system can be derived as

$$A_f(s) = \frac{A(s)}{1-A(s)\beta(s)} \tag{2.1}$$

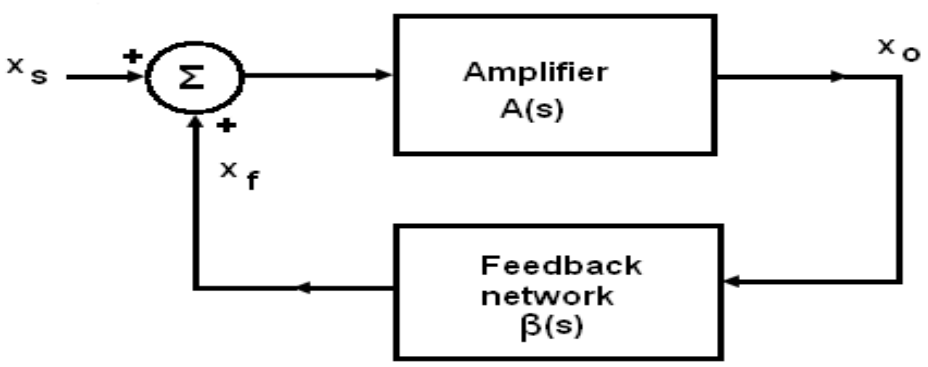


Fig.2.1 Basic structure of oscillator

The characteristic equation of this system can thus be written as

$$1 - A(s)\beta(s) = 0 \tag{2.2}$$

where $A(s)\beta(s)$ is called the loop gain $L(s)$. If at a specific frequency the loop gain of this system is equal to unity then A_f will be infinite implying that at this frequency the circuit will have a finite output for zero input signals. Such a circuit is by definition is an oscillator. Thus the condition for the closed loop system to provide sustained oscillations of frequency ω_0 can be represented as

$$L(j\omega_0) = A(j\omega_0)\beta(j\omega_0) = 1 \tag{2.3}$$

This condition is known as the Barkhuasen criterion. For the circuit to oscillate at a single frequency the oscillation criterion must be satisfied for a single frequency only; else the resulting waveform will not be a simple sinusoid. An alternative approach to the study of oscillator circuits consists of examining the circuit poles, which are the roots of the characteristic equation 2. For the circuit to produce sustained oscillations at a frequency (ω_0) the characteristic equation has to have roots at $s = \pm j\omega_0$.

The amplitude of the generated sine waves is limited, or set, using a nonlinear mechanism, implemented either with a separate circuit or using the nonlinearities of the amplifying device itself. In spite of this, these circuits, which generate sine waves utilizing resonance phenomena, are known as linear oscillators. Circuits that generate square, triangular, pulse etc. waveforms, called nonlinear oscillators or function generators, employ circuit building blocks known as multivibrators**.**

The frequency of oscillation (FO) ω_0 is determined solely by the phase characteristics of the feedback loop, the loop oscillates at the frequency for which the phase is zero. It follows that the stability of the frequency of oscillation will be determined by the manner in which the phase φ (ω_0) of the feedback loop varies with frequency. A "steep" function φ(ω_0) will result in a more stable frequency. This can be seen if one imagines a change in phase φ (ω_0) due to a change in one of the circuit components. If $d(\varphi)/d\omega_0$ is large, the resulting change in ω_0 will be small, as illustrated in Fig. 2.2.

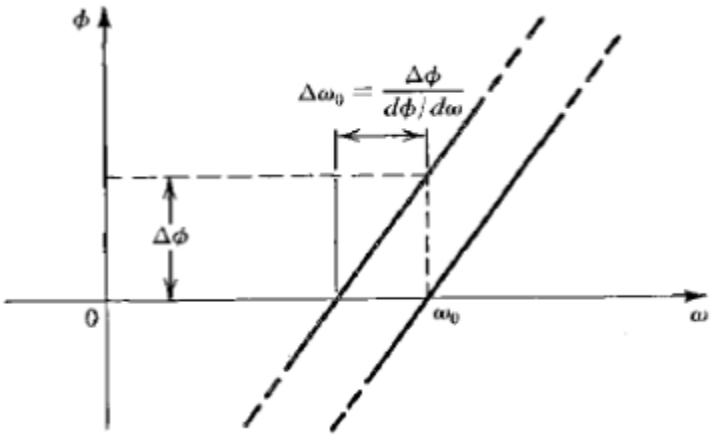


Fig2.2 Response of frequency versus phase

2.2 Total Harmonic Distortion:

Power quality is very important to commercial and industrial power system designs. Ideally, the electrical supply should be a perfect sinusoidal waveform without any kind of distortion. If the voltage/ current waveform is distorted from its ideal form it will be termed as harmonic distortion. This harmonic distortion could result because of many reasons. The harmful and damaging effects of harmonic distortion can be evident in many different ways such as electronics miss-timings, increased heating effect in electrical equipments, capacitor overloads, etc

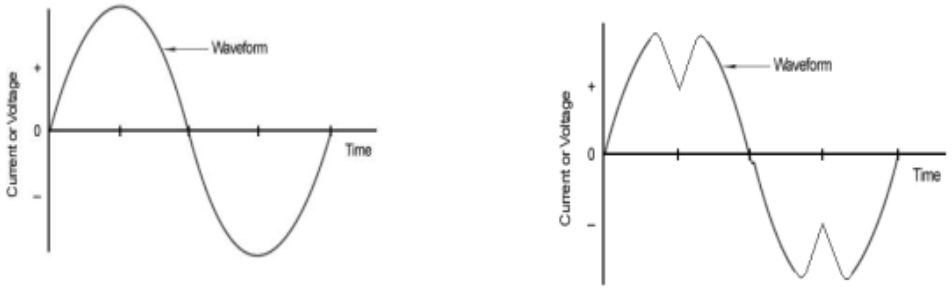


Fig 2.3 (a) Ideal Sine wave (b) Distorted Waveform

As can be observed from the waveform in Fig. 2.3, waveform distortions can drastically alter the shape of the sinusoid. However, no matter the level of complexity of the fundamental wave, it is actually just a composite of multiple waveforms called harmonics. Harmonics have frequencies that are integer multiples of the waveform's fundamental frequency. For example, given a 60Hz fundamental waveform, the 2^{nd}, 3^{rd}, 4^{th} and 5^{th} harmonic components will be at 120Hz, 180Hz, 240Hz and 300Hz respectively. Thus, harmonic distortion is the degree to which a waveform deviates from its pure sinusoidal values as a result of the summation of all these harmonic elements. The ideal sine wave has zero harmonic components.

Total harmonic distortion (THD), is the summation of all harmonic components of the voltage / current waveform compared against the fundamental component of the voltage /current wave and is given by:

$$\text{THD} = \frac{\sqrt{(V_2^2 + V_3^2 + V_4^2 + \cdots\ldots V_n^2)}}{V_1} * 100\ \% \qquad (2.4)$$

The end result is a percentage comparing the harmonic components to the fundamental component of a signal. The higher the percentage, the more distortion that is present on the mains signal.

References

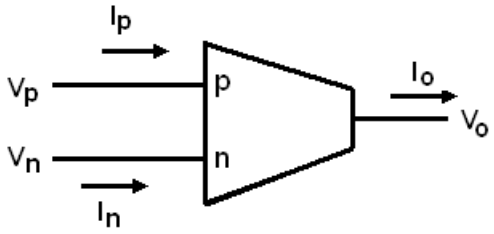
[1] A. S. Sedra and K. C. Smith. Microelectronic Circuits. Oxford University Press, New York, 2004**.**

CHAPTER-3
OPERATIONAL TRANSRESISTANCE AMPLIFIER

In this chapter OTRA [1-5] has been dealt with in detail. The ideal OTRA is introduced first which is followed by description of its CMOS based realization presented in 3.2

3.1 Basics of OTRA

The OTRA is a high gain current input voltage output device. Both input and output terminals of the OTRA are characterized by low impedance resulting in circuits that are insensitive to stray capacitances making OTRA appropriate for high frequency applications. The circuit symbol for OTRA and its small signal equivalent are shown in Fig.3.1 (a) and (b) respectively.



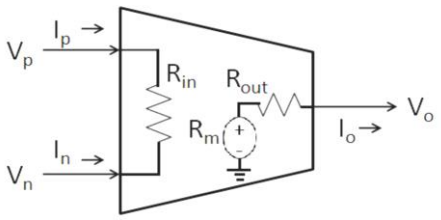


Fig. 3.1(a) symbol of OTRA (b) Small Signal AC Equivalent of OTRA

The port relationship of OTRA is represented by matrix (3.1).

$$\begin{bmatrix} V_p \\ V_n \\ V_O \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ I_O \end{bmatrix} \qquad (3.1)$$

where R_m represents transresistance gain. Ideally R_m approaches infinity there by forcing the two input currents, Ip and In, to be equal.

3.2 CMOS Realization of OTRA

The CMOS realization of low power wide band OTRA is shown in Fig.3.2. It is based on the cascaded connection of the modified differential current conveyor (MDCC) and a common source amplifier. Assuming that each of the groups of the transistors (M1-M3), (M5 and M6), (M8-M11) and (M12 and M13) are matched. And assuming that all the transistors operate in the saturation region, the circuit operation can be explained as follows. The current mirrors formed by (M8-M11) forces equal currents (IB) in the transistors M1, M2 and M3. This operation drives the gate to source voltages of M1, M2 and M3 to be equal and, consequently, forces the two input terminals to be virtually grounded.

The current mirrors formed by the transistor pairs (M10 and M11) and (M12 and M13) provide the current differencing operation, whereas the common source amplifier (M14) achieves the high gain stage. It is clear that the modified OTRA has smaller number of current mirrors than Salama and Soliman OTRA introduced in [3] which reduces the transistor mirror mismatch effect and also increases the frequency capabilities.

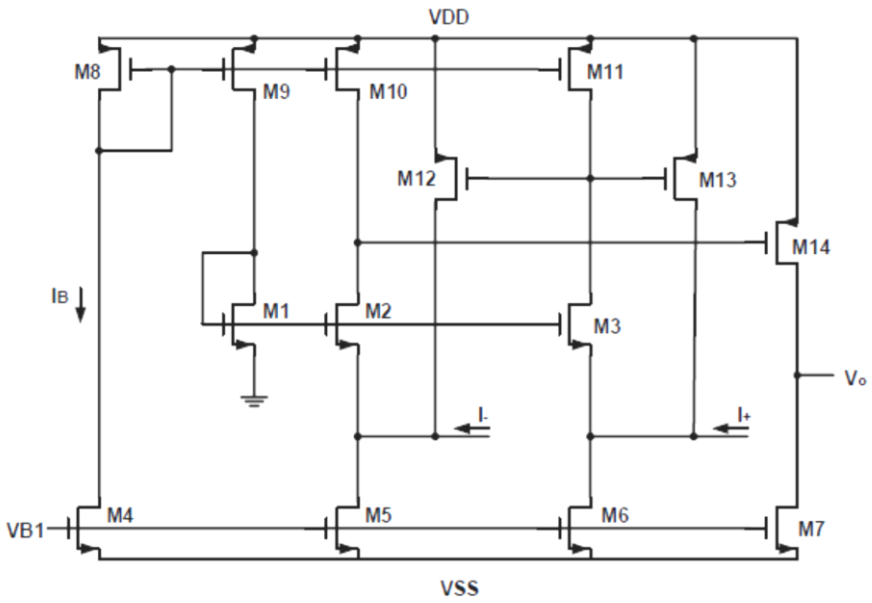


Fig3.2: CMOS implementation of OTRA [3]

The effect of finite transresistance gain of OTRA is considered and compensation is employed for high frequency applications. Ideally the transresistance gain Rm is assumed to approach infinity. However, practically Rm is a frequency dependent finite value. Considering a single pole model for the transresistance gain, Rm can be expressed as

$$\mathrm{Rm(s)} = \left(\frac{\mathrm{R_0}}{1+\frac{s}{w_0}}\right) \tag{3.2}$$

For high frequency applications the transresistance gain Rm(s) reduces to

$$\mathrm{Rm(s)} = \left(\frac{1}{sc_p}\right) \tag{3.3}$$

Where $C_p = \frac{1}{R0W0}$

For high frequency applications the effect of transistor capacitances needs to be considered.

3.3 Simulation Results OTRA

The OTRA [3] is characterized through PSPICE simulation to verify its functionalities. The aspect ratios of various transistors are taken same as in [3] and are reproduced in Table 1.

TABLE 1: Aspect ratio of the transistors in OTRA circuit.

Transistor	W (μm)/L (μm)
M_{O1}–M_{O3}	100/2.5
M_{O4}	10/2.5
M_{O5}, M_{O6}	30/2.5
M_{O7}	10/2.5
M_{O8}–M_{O11}	50/2.5
M_{O12}, M_{O13}	100/2.5
M_{O14}	50/0.5

The DC characteristic of the simulated OTRA is shown in Fig. 3.3 and the magnitude and phase responses are depicted in Fig. 3.4 (a) and (b) respectively.

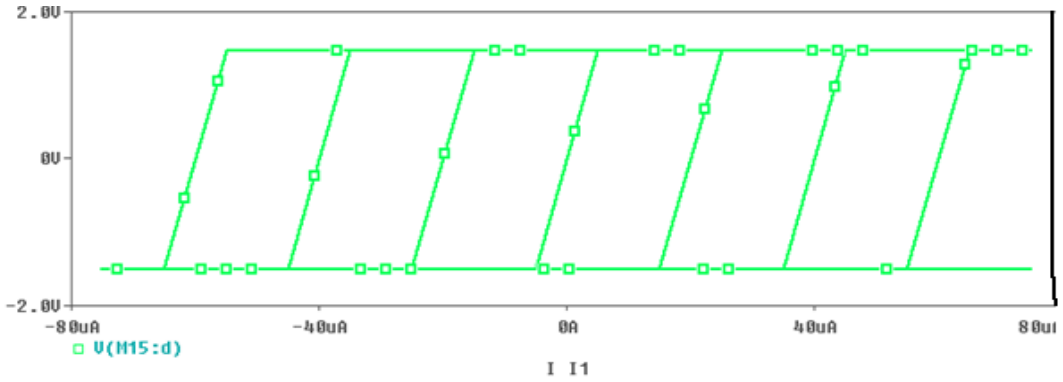


Fig.3.3 DC characteristics of OTRA

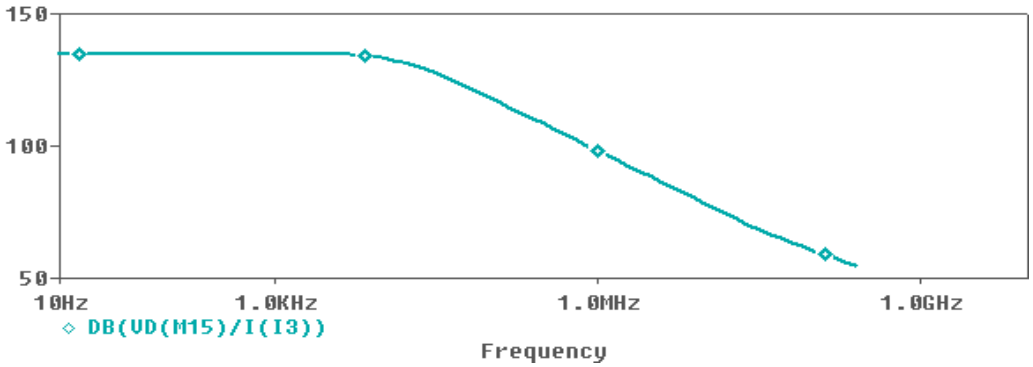


Fig.3.4 (a) Frequency response of OTRA

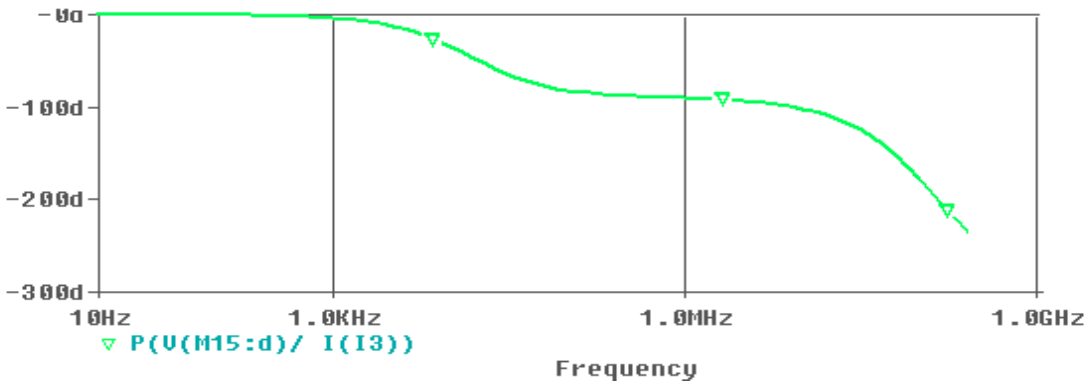


Fig.3.4 (b) Phase response of OTRA

References

[1] Chen, J. J., Tsao H. W., Chen, C. C. Operational transresistance amplifier Using CMOS Technology. Electronics Letters. 1992, vol. 28, no. 22, p. 2087–2088.

[2] Salama K. N., Soliman A. M., CMOS operational transresistance amplifier for analog signal processing. Microelectron J. 1999, vol. 30, issue 3, p. 235–45.

[3] Mostafa H. and Soliman A.M., A modified CMOS realization of the operational transresistance amplifier Frequenz, 2006, vol. 60, p. 70-76.

[4] Kafrawy A. K. and Soliman A. M., "New CMOS Operational Transresistance Amplifier", International Conference on Microelectronics, 2008, p. 31-34

[5] Kafrawy A. K. and Soliman A. M., A modified CMOS differential operational transresistance amplifier (OTRA), Int. J. Electron. Commun. 2009, (AEU) vol. 63, p. 1067-1071.

CHAPTER: 4
DESIGN OF SINUSOIDAL OSCILLATORS USING OTRA

4.1 Oscillators are an important class of circuits and find wide application in communication, instrumentation, measurement**,** and control systems.Oscillation is an effect that repeatedly and regularly fluctuates about the mean value and the Oscillator is a circuit that produces oscillation The electrical oscillations whose amplitude remains constant with time are called undamped oscillations..Oscillators are used to generate signals, e.g. used as a local oscillator to transform the RF signals to IF signals in a receiver, used to generate RF carrier in a transmitter,used to generate clocks in digital systems, as sweep circuits in TV sets and CRO [1].

Op amp oscillators are restricted to the lower end of the frequency spectrum because op amps do not have the required bandwidth to achieve low phase shift at high frequencies. Voltage-feedback op amps are limited to low kHz range since their dominant, open loop pole may be as low as 10 Hz. The new current-feedback op amps have a much wider bandwidth, but they are very hard to use in oscillator circuits because they are sensitive to feedback capacitance. Oscillators are useful for creating uniform signals that are used as a reference in applications such as audio, function generators, digital systems, and communication systems[1-2]. For these applications low value of total harmonic distortion (THD) is an essential requirement as higher harmonics have detrimental effects on electrical equipment. These higher order harmonics can also interfere with communication transmission lines since they oscillate at the same frequencies as the transmit frequency. If left unchecked, increased temperature and interference can greatly shorten the life of electronic equipment and cause damage to power systems.

Various sinusoidal oscillators are already mentioned in the literature using active current building blocks, These topologies are designed using second generation

current conveyor (CCII) [3, 4], operational transconductance amplifier (OTA) [5], second generation current controlled conveyor (CCCII) [6– 8], opamp [9] differential voltage current conveyor (DVCC) [10] , current difference transconductance amplifier (CDTA) [9,11], operational transresistance amplifier (OTRA) [12-14] and current-controlled current difference transconductance amplifier (CCCDTA) . The OTRA is a current input voltage output device [15]. Being a current processing block, it inherits all the advantages of current mode techniques [9] and provides voltage output at low impedance which can readily be used to drive voltage input circuits without increasing component count.

In this paper two topologies of second order sinusoidal oscillators based on OTRA have been presented. One of the proposed circuits makes use of allpass section designed using OTRA connected in a feedback forming closed loop whereas the other configuration uses two lossless integrators connected in non inverting and inverting mode respectively. The proposed structure Fig.4.2 and 4.3 can be made fully integrated by implementing the resistors using matched transistors operating in linear region and can be tuned electronically.

4.2 CIRCUIT DESCRIPTION

The OTRA is a high gain current input voltage output analog building block [15]. The input terminals of OTRA are internally grounded, thereby eliminating response limitations due to parasitic capacitances and resistances and hence is a suiatable choice for high frequency applications. The circuit symbol of OTRA is shown in Fig. 4.1 and the port characteristics are given by (1), where R_m is transresistance gain of OTRA.

$$\begin{bmatrix} V_p \\ V_n \\ V_O \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ I_O \end{bmatrix} \tag{4.1}$$

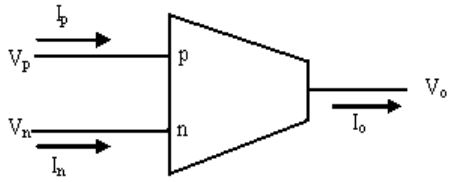


Fig.4.1. OTRA circuit Symbol

For ideal operations the R_m of OTRA approaches infinity and forces the input currents to be equal. Thus OTRA must be used in a negative feedback configuration [16].

CIRCUIT I

The first design topology is shown in Fig.4.2. It uses allpass section designed using single OTRA in the feedback forming a closed loop resulting in loop gain of the system as A(s)β(s) where A(s) is forward path gain and β(s) is feedback gain involving OTRA.

The criterion for oscillations [1] to occur, is given by

$$1- A(s)\,\beta(s) = 0 \qquad (4.2)$$

If this criterion is satisfied the closed loop system will result in sinusoidal undamped oscillations, available at nodes Vo. Routine analysis of the circuit of Fig. 4.2results in following characteristic equation as

$$2s^2c_1c_2 + s\left[2\frac{c_1}{R_2} + 2\frac{c_2}{R_1} - \frac{c_1}{R_1}\right] + \frac{2}{R_1R_2} = 0 \qquad (4.3)$$

From this characteristic equation the condition of oscillation (CO) and frequency of oscillation (FO) can be found to be

FO: $$f = \frac{1}{2\pi}\sqrt{\frac{1}{C_1C_2R_1R_2}} \qquad (4.4)$$

CO: $$c_1 = 4c_2$$

$$R_2 = 4R_1 \tag{4.5}$$

The FO can be adjusted to desired value through proper selection of resistor R_1, R_2 and c_1, c_2 would satisfy the CO.

CIRCUIT II

The second proposed oscillator configuration is shown in Fig.4.3 which makes use of two lossless integrator, connected in non inverting mode and inverting mode respectively.

The characteristic equation of the Circuit II can be deduced as

$$s^2 C_1 C_2 R_2 R_1 + 1 = 0 \tag{4.6}$$

$$\text{FO: } f = \frac{1}{2\pi}\sqrt{\frac{1}{C_1 C_2 R_2 R_1}} \tag{4.7}$$

From (4.6) it is clear that the circuit Fig.4.2 is unstable and it will always produce oscillations, the FO of oscillations can be adjusted by proper selection of resister and capacitor values.

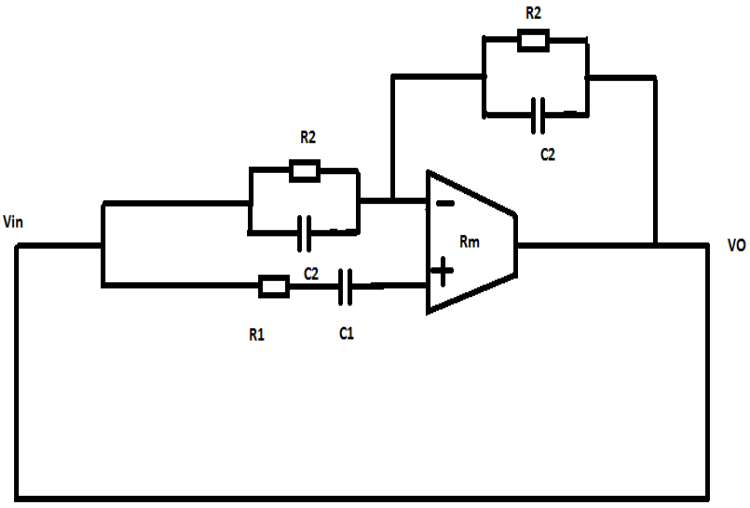


Fig.4.2. Proposed circuit I

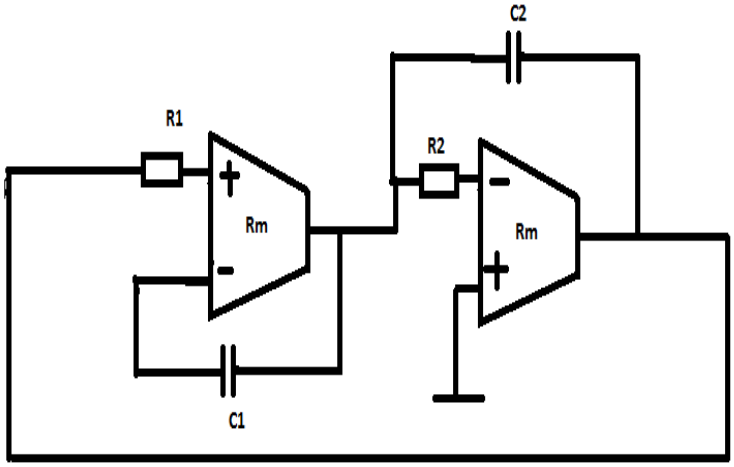


Fig.4.3 Proposed circuit II

The current differencing property of the OTRA makes it possible to implement the resistors connected to the input terminals of OTRA, using MOS transistors with complete non linearity cancellation [15]. Each resistor requires two matched n-MOSFETs connected in a manner as shown in Fig 4 which represents a typical MOS implementation of resistance connected at negative input of OTRA.

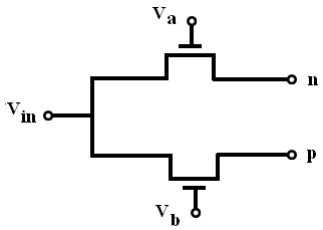


Fig.4.4. The MOS based resistor [15]

Symbols ‘p’ and ‘n’ represent the non-inverting and the inverting terminals of the OTRA. As can be seen from the figure, the voltages at the drain and the source terminals for both MOSFETs are equal. On taking the difference of the currents flowing in the two transistors, the non linearity gets cancelled out. The resistor value realized can be expressed as

$$R = \frac{1}{K_N(V_a - V_b)} \tag{4.8}$$

Where

$$K_N = \mu\, C_{OX}\, \frac{W}{L} \tag{4.9}$$

K_N needs to be determined for the transistors being used to implement the resistors and μ, C_{OX} and W/L represent standard transistor parameters. The MOS based implementation of Circuit II is shown in Fig.4.6

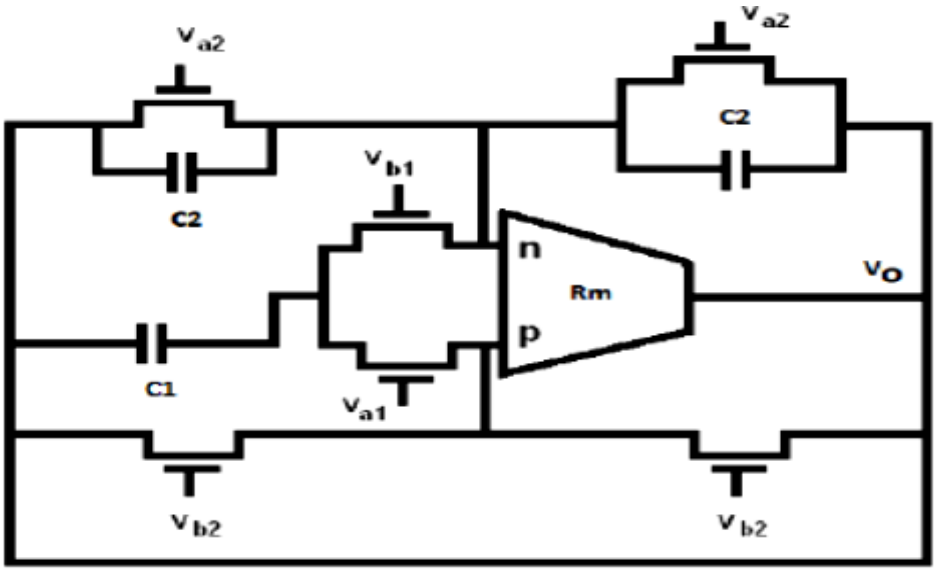


Fig.4.5. The MOS based implementation of Circuit I

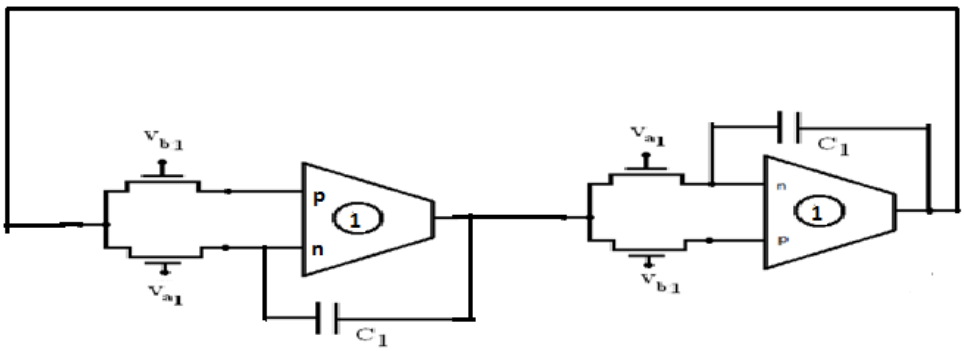


Fig.4.6. MOS based implementation of Circuit II

4.3 NON-IDEAL ANALYSIS

The output of the oscillators may deviate due to non ideality of OTRA in practice. Ideally the transresistance gain R_m is assumed to approach infinity. However, practically R_m is a frequency dependent finite value. Considering a single pole model for the trans-resistance gain, R_m can be expressed as

$$R_m(s) = \left(\frac{R_0}{1+\frac{s}{\omega_0}}\right) \tag{4.10}$$

Where R_0 is dc transresistance gain. For high frequency applications the transresistance gain $R_m(s)$ reduces to

$$R_m(s) = \left(\frac{1}{sC_p}\right) \tag{4.11}$$

Where $C_p = \frac{1}{R_0\ \omega_0}$

Taking this effect into account (4.3) modifies to

$$2s^2(c_1 + c_p)(c_2 + c_p) + s\left[2\frac{(c_1+c_p)}{R_2} + 2\frac{(c_2+c_p)}{R_1} - \frac{(c_1+c_p)}{R_1}\right] + \frac{2}{R_1R_2} = 0 \tag{4.12}$$

From (4.4) it is found that FO for circuit I changes to

$$f = \frac{1}{2\pi}\sqrt{\frac{1}{(C_1+C_p)(C_2+C_p)R_1R_2}} \tag{4.13}$$

Due to nonideality effect of OTRA (4.6) changes to

$$s^2(c_1 + c_p)(c_2 + c_p)R_1R_2 + 1 = 0 \tag{4.14}$$

The characteristic equation represented by (4.7) results in modified FO for circuit II and is expressed as

$$f = \frac{1}{2\pi}\sqrt{\frac{1}{(C_1+C_p)(C_2+C_p)R_1R_2}} \tag{4.15}$$

The effect of C_p can be eliminated by pre-adjusting the values of capacitors C_1, C_2 thus achieving self compensation.

4.4 SIMULATION RESULTS

The proposed sinusoidal undamped oscillators are verified through simulations using the CMOS implementation of the OTRA [16] and the SPICE simulations are performed using 0.5 μm CMOS process parameters provided by MOSIS (AGILENT). Supply voltages taken are ±1.5V. For both the circuits the resistor and capacitor values are taken as R_1=10K, C_1=100p, R_2=40K, C_2=25p and for circuit II R_1=$R_2$10K, C_1=C_2=100p. Both the topologies are designed for an FO of 159 KHz and the simulated value was observed to be 160 KHz and for Circuit I and II respectively. The simulated transient output and corresponding frequency spectrum for Circuit I are shown in Fig.4.7 and Fig.4.8 respectively and those for Circuit II are depicted in Fig.4.9 and Fig.4.10. The percentage total harmonic distortion (THD) Table 4.2. is 1.07% for Circuit I and that for Circuit II Table 4.3 is observed to be 2.89%.

Table.4.1 Summary for the proposed circuits

Circuit	Active element	Number of C Used	Number of R used	C.O	F.O	MOS C Implementation
Fig.2	Single OTRA	3 Floating	3 Floating	$c_1 = 4c_2$ $R_2 = 4R_1$	$f = \frac{1}{2\pi}\sqrt{\frac{1}{C_1C_2R_1R_2}}$	Possible
Fig.3	Two OTRA'S	2 Floating	2 Floating	NONE	$f = \frac{1}{2\pi}\sqrt{\frac{1}{C_1C_2\ R_2R_1}}$	Possible

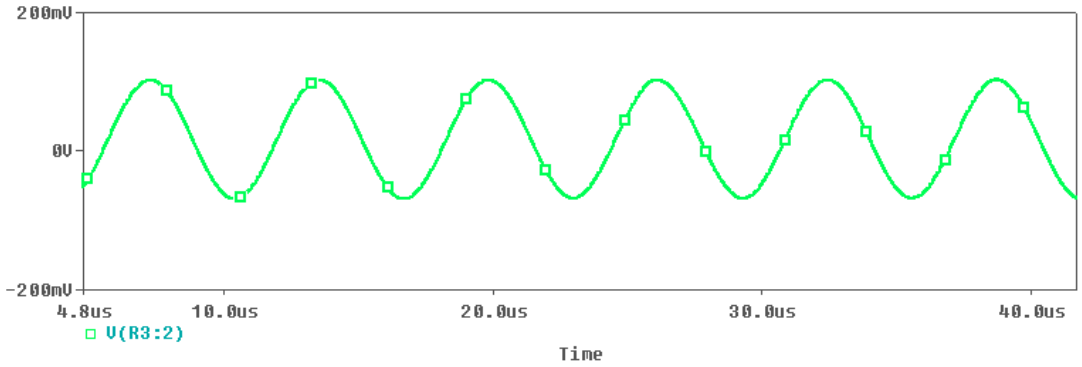


Fig.4.7 Transient Output of proposed Circuit I

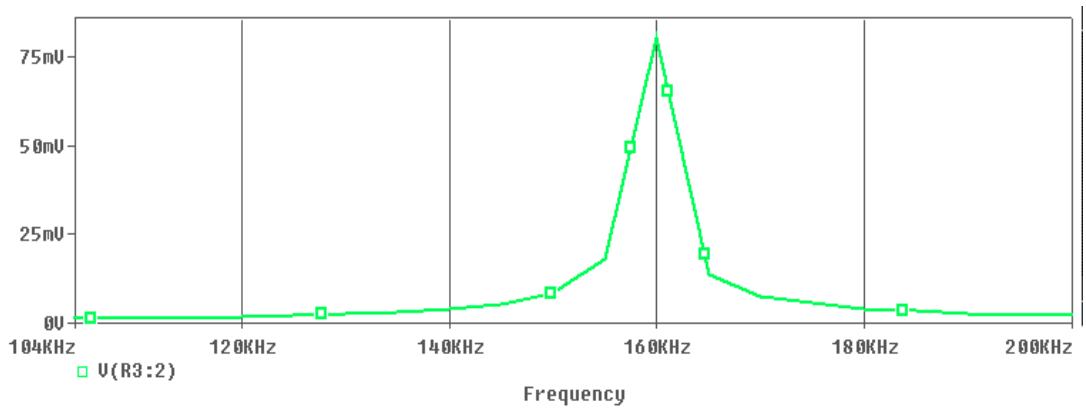


Fig.4.8 Frequency spectrum of output of Circuit I

TABLE .4.2 TOTAL HARMONIC DISTORTION FOR FIG .4.2

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE(DEG)
1	1.600E+05	8.371E-02	1.000E+00	-8.806E-01	0.000E+00
2	3.200E+05	7.362E-04	8.794E-03	1.122E+01	1.298E+01
3	4.800E+05	3.345E-05	3.996E-04	-2.769E+01	-2.505E+01
4	6.400E+05	2.786E-04	3.328E-03	-4.849E+00	-1.327E+00
5	8.000E+05	3.295E-04	3.936E-03	2.009E+01	2.449E+01
6	9.600E+05	1.451E-04	1.734E-03	-5.222E-01	4.761E+00

7	1.120E+06	1.527E-04	1.824E-03	-2.931E+01	-2.315E+01
8	1.280E+06	1.213E-04	1.449E-03	1.093E+01	1.798E+01
9	1.440E+06	1.008E-04	1.204E-03	3.406E+01	4.198E+01
10	1.600E+06	1.110E-04	1.326E-03	5.452E+00	1.426E+01
TOTAL HARMONIC DISTORTION = 1.075666E+00 PERCENT					

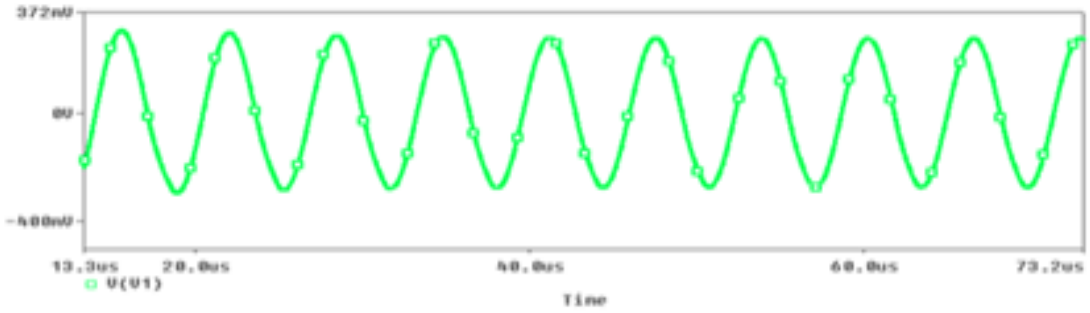


Fig.4.9 Transient output of proposed Circuit II

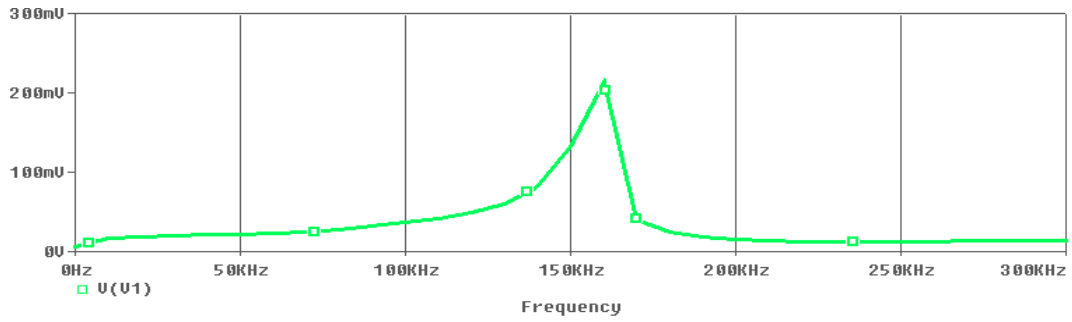


Fig..4.10Frequency spectrum of output of QO Circuit II

TABLE 4.3 TOTAL HARMONIC DISTORTIONS FOR FIG.4.3

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE(DEG)
1	1.600E+05	2.764E-01	1.000E+00	-1.784E+02	0.000E+00
2	3.200E+05	4.466E-03	1.616E-02	-1.356E+02	2.211E+02
3	4.800E+05	3.722E-03	1.347E-02	-1.408E+02	3.943E+02
4	6.400E+05	3.330E-03	1.205E-02	-1.529E+02	5.605E+02
5	8.000E+05	2.856E-03	1.033E-02	-1.669E+02	7.249E+02
6	9.600E+05	2.266E-03	8.199E-03	-1.798E+02	8.904E+02
7	1.120E+06	1.653E-03	5.980E-03	1.719E+02	1.420E+03
8	1.280E+06	1.180E-03	4.267E-03	1.727E+02	1.600E+03
9	1.440E+06	9.843E-04	3.561E-03	-1.785E+02	1.427E+03
10	1.600E+06	9.813E-04	3.550E-03	-1.747E+02	1.609E+03

TOTAL HARMONIC DISTORTION = 2.899574E+00 PERCENT

References

[1] A. S. Sedra, and K. C. Smith, Microelectronic Circuits. Oxford University Press, New York, 2004.

[2] R. Schauman and M.E. Van Valkenburg, Design of analogfilters, Oxford University Press, New York, 2001.

[3] P. Promme and K. Dejhan, "An integrable electronic controlled sinusoidal oscillator using CMOS operational transconductance amplifier," Int. J. Electron., vol.89, pp. 365–379, 2002.

[4] J. W. Horng, "Current-mode third-order quadrature oscillator using CDTAs," Active and Passive Electronic Components, 2009, Article ID 789171, p. 1-5.

[5] P. Promme and K. Dejhan, "An integrable electronic controlled sinusoidal oscillator using CMOS operational transconductance amplifier," Int. J. Electron., vol.89, pp. 365–379, 2002

[6] S Maheshwari, and I. A. Khan, "Current controlled third order quadrature oscillator," IEE Proc.-Circuits, Devices and Systems, vol. 152, pp. 605-607, 2005.

[7] S. Maheshwari and I.A. Khan, "Current controlled third order quadrature oscillator," IET Circuits Devices Systems, vol. 4, pp. 188–195,2010.

[8] S.Maheshwari and R. Verma, "Electronically Tunable Sinusoidal Oscillator Circuit," Active and Passive Electronic Components Volume 2012, Article ID 719376, 6 pages DOIi:10.1155/2012/719376

[9] Ahmed M. Soliman "Two integrator loop quadrature oscillators, Journal of Advanced Research (2013) 4, 1

[10] S. Maheshwari, "Analogue signal processing applications using a new circuit topology," IET Circuits Devices Systems vol. 3, pp.106–115. 2009.

[11] J. W. Horng, H Lee and J.Y. Wu, "Electronically tunable third order Quadrature oscillators using CDTAs," RadioEngineering vol. 19, pp. 326-330, 2010.

[12] R. Pandey, N. Pandey and S.K. Paul, "MOS-C Third Order Quadrature Oscillator using OTRA,". Third International Conference on Communication and Computer Technology, ICCCT-12, pp.77 -80, 2012.

[13] Selquk Kiling and Ugur Cam "Operational Transresistance Amplifier Based First-Order Allpass Filter with an Application Example" The 47th IEEE International MidwestSymposium on Circuits and Systems

[14] Rajeshwari Pandey, Neeta Pandey, Gurumurthy Komanapalli, Rashika Anurag "OTRA Based Voltage Mode Third Order Quadrature Oscillator" ISRN Electronics Volume 2014, Article ID 126471, 5 pages

[15] K. N. Salama and A. M. Soliman, "CMOS Operational Transresistance Amplifier for analog signal processing applications." Microelectron. J.,vol. 30, pp. 235–245, 1999

[16] H. Mostafa and A. M. Soliman, "A modified realization of the OTRA," Frequenz, vol.60, pp.70-76, 2006.

CHAPTER 5
OPERATIONAL TRANSRESISTANCE AMPLIFIER BASED WEINBRIDGE OSCILLATOR

5.1 Introduction

Wien Bridge Oscillator is one of the simplest designs to produce sine wave oscillations which use a RC network in place of the conventional LC tuned tank circuit and they form basic analog building blocks and useful in many RF applications [1-4] In 1939 William Hewlett at Stanford University incorporated it into a practical audio frequency sine wave oscillator that has low distortion and a variable frequency and also stable amplitude for the purpose of accurately measuring capacitor values. It contains two-stage RC coupled amplifier circuit which has good stability at its resonant frequency, low distortion and its ease of tuning capability makes this circuit so popular at audio frequency range.

For frequencies much below 1MHz, RC oscillators [5] become more practical than LC types because of the physical size and expense of the inductors and capacitors required at low frequencies. The frequency of oscillation in RC types, such as the phase shift oscillator, is controlled using multiple RC combinations to produce the correct amount of phase shift at the required frequency. Traditionally operational amplifiers are used to realize wein oscillator [6] however their high frequency operations are limited due to constant gain bandwidth product and low slew rate of op-amp. The current mode approach has received considerable interest due to its inherent wide bandwidth which is virtually independent of closed loop gain, greater linearity, and large dynamic range. Significant research efforts have been directed towards developing new active blocks based on this approach. . It is possible to build Wien Bridge oscillators having very low levels of distortion compared with Phase Shift designs. The active devices which are present in the literature includes Operational Amplifiers , Current feedback Operational Amplifiers (CFOA) [7] and

Operational Transconductance Amplifiers (OTA) [8], second generation current conveyors (CCIIs) [9].operational transresistance amplifier (OTRA) [10-15].

The operational transresistance amplifier (OTRA) has attracted considerable attention of analog designers due to recent developments in current-mode analog integrated circuits [10]–[15]. The operational transresistance amplifier is commercially available from several manufacturers under the name of current differencing amplifier or Norton amplifier. OTRA is a current input voltage output device [15]. Being a current processing block, it inherits all the advantages of current mode techniques and provides voltage output at low impedance which can readily be used to drive voltage input circuits without increasing component count.

5.2. CIRCUIT DESCRIPTION

The OTRA based Wien oscillator is shown in Fig. 5.1 with no input signal the circuit produces continuous output oscillations and can produce a large range of frequencies. If the voltage gain of the amplifier is too small the desired oscillation will decay and stop. If it is too large the output will saturate to the value of the supply rails and distort, therefore some method of stabilizing the amplitude of the oscillations must be provided.

The combination of buffer and OTRA is used as a voltage controlled voltage source with a gain of $K = R_4/R_3$. The amplitude stabilisation is in the form of feedback and the oscillations from the proposed design can continue indefinitely by making $C_1 = C_2 = C$.

The topology shown in Fig.5.1. uses two RC sections and a buffer and active block i.e, OTRA and the feedback forming a closed loop resulting in loop gain of the system as $A(s)\beta(s)$ where $A(s)$ is forward path gain and $\beta(s)$ is feedback gain involving OTRA. The criterion for oscillations [16] to occur, is given by

$$1-A(s)\beta(s)=0 \qquad (5.1)$$

If this criterion is satisfied the closed loop system will result in oscillations. Routine analysis of the circuit of Fig. 2 results in following characteristic equation as

$$s^2 c_1 c_2 R_1 R_2 + s[c_1 R_1 + c_2 R_2 + c_2 R_1 - \frac{C_2 R_1 R_4}{R_3}] + 1 = 0 \qquad (5.2)$$

Two basic sections form the Wien-bridge oscillator: an RC tuning network and an amplifier. Both are necessary to achieve the conditions for oscillations. The RC network is characterized by a center frequency, The condition of oscillation (CO) and frequency of oscillation (FO) can be obtained as

$$\text{CO: } K = 2 + R_1 / R_2 ;$$

$$\text{FO: } f_0 = \frac{1}{2\pi C\sqrt{R_1 R_2}} \tag{5.3}$$

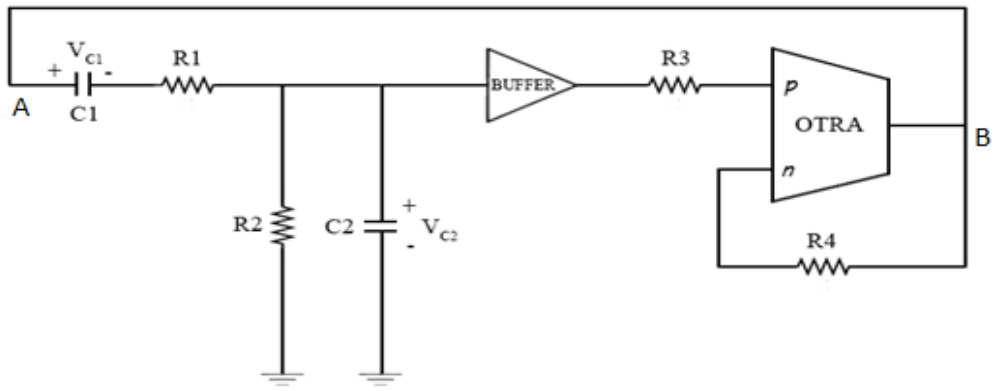


Fig. 5.1. OTRA based Wien Oscillator

5.3 NON-IDEAL ANALYSIS

The output of the oscillator may deviate due to non ideality of OTRA in practice. Ideally the transresistance gain R_m is assumed to approach infinity. However, practically R_m is a frequency dependent finite value. Considering a single pole model [17] for the trans-resistance gain, R_m can be expressed as

$$R_m(s) = \left(\frac{R_0}{1+\frac{s}{\omega_0}}\right) \tag{5.4}$$

Where R_0 is dc transresistance gain. For high frequency applications the transresistance gain $R_m(s)$ reduces to

$$R_m(s) = \left(\frac{1}{sC_p}\right) \tag{5.5}$$

Where $C_p = \frac{1}{R_0\ \omega_0}$

Taking this effect into account (5.2) modifies to

$$s^2[(c_1 + c_p)(c_2 + c_p)R_1R_2] + s[(c_1 + c_p)R_1 + (c_2 + c_p)R_2 + (c_2 + c_p)R_1 - \frac{(c_2+c_p)R_1R_4}{R_3}] + 1 = 0 \tag{5.6}$$

From (5.6) it is found that FO for Fig. 5.1 changes to

$$f = \frac{1}{2\pi}\sqrt{\frac{1}{(C_1+C_p)(C_2+C_p)R_1R_2}} \tag{5.7}$$

The effect of C_p can be eliminated by pre-adjusting the values of capacitors C_1, C_2 and thus achieving self compensation

5.4. HARMONIC ANALYSIS

The harmonic analysis of the proposed Wien oscillator using the OTRA as active building block which is shown in Fig. 5.1, the calculation of HD3 and HD2 is presented in this section. From [18] by expressing the voltage at node A at the steady state, the set of fundamental equations are derived. By following the feedback path as shown in Fig.5.1 and considering only the first three harmonics of the output voltage (due to the weakly nonlinear behaviour of the oscillator), we can write in phasor notation

$$V_{Xi}(t) = Re[V_{01}e^{jw_ot} + V_{02}e^{j2w_ot} + V_{03}e^{j3w_ot}] \tag{5.8}$$

Where w_o is the oscillation frequency and V_{Ai}, for i=1, 2, 3 are in general complex quantities (depending on w_o) with magnitude $|V_{Ai}|$ and phase $\angle V_{Ai}$. Without loss of

generality, we assume the fundamental to be a real number, and we measure the phase of the third harmonic and second harmonic with respect to it. Let us now consider the output voltage, which can be modelled by the polynomial function

$$V_Y = a_1 V_X + a_2 V_X^2 + a_3 V_X^3 \qquad (5.9)$$

Substituting (9) into (10) and evaluating [18,19]the product between the real parts of sums of phasors, considering only the terms up to the third harmonic and neglecting the dc component shown in foot note , we get

$$V_0(t) = Re[V_{Y1} e^{jw_o t} + V_{Y2} e^{j2w_o t} + V_{Y3} e^{j3w_o t}] \qquad (5.10)$$

Where $V_{Y1} = a_1(w_o)V_{01} + \frac{3}{4} a_3(w_o){V_{01}}^3$

$$V_{Y2} = a_1(w_o)V_{02} + \frac{1}{2} a_2(w_o){V_{01}}^2 + \frac{3}{2} a_3(w_o){V_{01}}^2 V_{02}$$

$$V_{Y3} = a_1(w_o)V_{03} + a_2(w_o)V_{01}V_{03} + \frac{1}{4} a_3(w_o){V_{01}}^3 \qquad (5.11)$$

The coefficients a_1, a_2, a_3 can be frequency independent which is shown in section 5.5

$V_Y = a_1[Re[V_{01} e^{jw_o t} + V_{02} e^{j2w_o t} + V_{03} e^{j3w_o t}]] + a_2[[Re\left[V_{01} e^{jw_o t} + V_{02} e^{j2w_o t} + V_{03} e^{j3w_o t}\right]]^2 + a_3[[Re\left[V_{01} e^{jw_o t} + V_{02} e^{j2w_o t} + V_{03} e^{j3w_o t}\right]]^3$

$V_Y = a_1[V_{01} cos\ w_o t + V_{02} cos\ 2w_o t + V_{03} cos\ 3w_o t] + a_2[{V_{01}}^2 cos^2\ w_o t$
$+ {V_{02}}^2 cos^2\ 2w_o t + {V_{03}}^2 cos^2\ 3w_o t$
$+ 2V_{01}V_{02} cos\ w_o t\ cos 2\ w_o t + 2V_{02}V_{03} cos 2\ w_o t\ cos 3\ w_o t$
$+ 2V_{01}V_{03} cos\ w_o t\ cos 3\ w_o t] + a_3[{V_{01}}^3 cos^3\ w_o t + {V_{02}}^3 cos^3\ 2w_o t + {V_{03}}^3 cos^3\ 3w_o t$

$+ 3{V_{01}}^2 cos^2\ w_o t[V_{02} cos 2\ w_o t + V_{03} cos 3\ w_o t] +$
$3{V_{02}}^2 cos^2 2\ w_o t[V_{01} cos\ w_o t + V_{03} cos 3\ w_o t] +$
$3{V_{03}}^2 cos^2\ 3w_o t[V_{01} cos 2\ w_o t + V_{02} cos 2\ w_o t] + 6V_{01}V_{02}V_{03} cos\ w_o t cos 2\ w_o t\ cos 3\ w_o t$

Following again the feedback path, we now compute the output voltage of the linear section fed by the signal V_B , which results to be

$$V_0(t) = Re[V_{Y1}e^{jw_o t}H(w_o) + V_{Y2}e^{j2w_o t}H(2w_o) + V_{Y3}e^{j3w_o t}H(3w_o)] \qquad (5.12)$$

From the Fig.5.1

$$H(w)=\frac{V_0(w)}{V_i(w)} =\frac{V_1(w)}{V_i(w)}.\frac{V_2(w)}{V_1(w)}.\frac{V_o(w)}{V_2(w)} \qquad (5.13)$$

$$\frac{V_1(w)}{V_i(w)} = \frac{Z_2}{Z_1+Z_2} \qquad (5.14)$$

Where $$Z_2 = R_1 \,||\, \frac{1}{S_{C1}}$$

$$Z_1 = R_2 + \frac{1}{S_{C2}}$$

For the buffer circuit by considering single pole model

$$\frac{V_2(w)}{V_1(w)} = \left(\frac{1}{1+\frac{s}{w_0}}\right) \qquad (5.15)$$

For the OTRA [15]

$$I_p=\frac{V_2}{R_3} \quad ;I_n=\frac{V_0}{R_4}; I_p = I_n$$

$$\frac{V_2}{R_3} = \frac{V_0}{R_4} \qquad (5.16)$$

From (5.15), (5.16), (5.17)

$$\frac{V_0(w)}{V_i(w)} = \frac{Z_2}{[Z_1+Z_2][1+\frac{s}{w_0}]}.\frac{R_4}{R_3} \qquad (5.17)$$

Consider the Wien oscillator of Fig. 5.1. It is well known that the oscillation frequency for this circuit is given by

$$w_0 = \sqrt{\frac{1}{c_1 c_2 R_1 R_2}}$$

and thus for this particular circuit relationship (5.13) at the oscillation frequency becomes

$$|H(w_0)| = \frac{R_4}{R_3}.\frac{1}{[1-\sqrt{\frac{1}{c_1 c_2 R_1 R_2}}][1+\frac{R_2}{R_1}+\frac{C_1}{C_2}]} \tag{5.18}$$

As we are connecting the output and input by feedback the equations (5.9) and (5.13) represents the output voltage V_0, the generic component V_{Ai} is found by equating the corresponding term of (13) at frequency iw_0 (i.e.,$V_{Xi} = V_{Yi}\, H(iw_0)$). This yields

$$V_{X1} = \sqrt{\frac{[1+\frac{R_2}{R_1}+\frac{C_1}{C_2}][1-\sqrt{\frac{1}{c_1 c_2 R_1 R_2}} - a_1\frac{R_4}{R_3}]}{3a_3}}$$

$$V_{X2} = \frac{1}{2}\, a_2\, \frac{H(2w_0)}{1-[a_1+\frac{3}{2}a_2 {V_{A1}}^2]H(2w_0)}\, {V_{X1}}^2$$

$$V_{X3} = \frac{1}{4}\, a_3\, \frac{H(3w_0)}{1-[a_1+a_2\, V_{A1}]H(3w_0)}\, {V_{X1}}^3 \tag{5.19}$$

From (5.13)

$$H(w_0) = \frac{Sc_2R_2.\frac{R_4}{R_3}}{s^2c_1c_2R_1R_2 + s(R_1c_1 + c_2R_2 + R_1c_2) + 1 + \frac{s^3}{w_0}c_1c_2R_1R_2 + \frac{s^2}{w_0}(R_1c_1 + c_2R_2 + R_1c_2) + \frac{S}{w_0}}$$

$$H(2w_0) = \frac{\mathrm{j}2\sqrt{(\frac{R_1c_2}{R_2c_1})}.\frac{R_4}{R_3}}{-3 - j6 + j2\sqrt{(\frac{R_1c_2}{R_2c_1})}\left[1+\frac{R_2}{R_1}+\frac{C_1}{C_2}\right] - 4\sqrt{(\frac{R_1c_2}{R_2c_1})}\left[1+\frac{R_2}{R_1}+\frac{C_1}{C_2}\right]}$$

$$H(3w_0) = \frac{\text{j}3\sqrt{(\frac{R_1c_2}{R_2c_1})}.\frac{R_4}{R_3}}{-8 - j24 + j3\sqrt{(\frac{R_1c_2}{R_2c_1})}\left[1 + \frac{R_2}{R_1} + \frac{C_1}{C_2}\right] - 9\sqrt{(\frac{R_1c_2}{R_2c_1})}\left[1 + \frac{R_2}{R_1} + \frac{C_1}{C_2}\right]}$$

$$\frac{H(2w_0)}{1-H(2w_0)} = \frac{\text{j}2\sqrt{(\frac{R_1c_2}{R_2c_1})}.\frac{R_4}{R_3}}{-3-j6+j2\sqrt{(\frac{R_1c_2}{R_2c_1})}\left[1+\frac{R_2}{R_1}+\frac{C_1}{C_2}\right]-4\sqrt{(\frac{R_1c_2}{R_2c_1})}\left[1+\frac{R_2}{R_1}+\frac{C_1}{C_2}\right]-\text{j}2\sqrt{(\frac{R_1c_2}{R_2c_1})}.\frac{R_4}{R_3}}$$

$$\frac{H(3w_0)}{1 - H(3w_0)} = \frac{\text{j}3\sqrt{(\frac{R_1c_2}{R_2c_1})}.\frac{R_4}{R_3}}{-8 - j24 + j3\sqrt{(\frac{R_1c_2}{R_2c_1})}\left[1 + \frac{R_2}{R_1} + \frac{C_1}{C_2}\right] - 9\sqrt{(\frac{R_1c_2}{R_2c_1})}\left[1 + \frac{R_2}{R_1} + \frac{C_1}{C_2}\right] - \text{j}3\sqrt{(\frac{R_1c_2}{R_2c_1})}.\frac{R_4}{R_3}}$$

$HD_2 = 20\log|V_{A2}/\ V_{A1}| =$

$$\frac{|a_2|\sqrt{(\frac{R_1c_2}{R_2c_1})}\frac{R_4}{R_3}\ V_{A1}}{\sqrt{(-3-4\left(\sqrt{\frac{R_1c_2}{R_2c_1}}\right)\left[1+\frac{R_2}{R_1}+\frac{C_1}{C_2}\right])^2+(-6+2\left(\sqrt{\frac{R_1c_2}{R_2c_1}}\right)\left[1+\frac{R_2}{R_1}+\frac{C_1}{C_2}\right]-2(a_1+\frac{3}{2}a_2{V_{A1}}^2\ )\sqrt{\left(\frac{R_1c_2}{R_2c_1}\right)}\frac{R_4}{R_3})^2}}$$

$HD_3 = 20\log|V_{A3}/\ V_{A1}| =$

$$\frac{\frac{3}{4}|a_3|\sqrt{(\frac{R_1c_2}{R_2c_1})}\frac{R_4}{R_3}{V_{A1}}^2}{\sqrt{(-8-9\left(\sqrt{\frac{R_1c_2}{R_2c_1}}\right)\left[1+\frac{R_2}{R_1}+\frac{C_1}{C_2}\right])^2+(-24+3\left(\sqrt{\frac{R_1c_2}{R_2c_1}}\right)\left[1+\frac{R_2}{R_1}+\frac{C_1}{C_2}\right]-3(a_1+a_2\ V_{A1})\sqrt{\left(\frac{R_1c_2}{R_2c_1}\right)}\frac{R_4}{R_3})^2}}$$

5.5 Mathematical proof for to show coefficients are frequency independent

Consider the circuit shown in Fig. 4.1 and assume to be a pure sinusoidal voltage with amplitude and frequency. Assume also the output voltage of the circuit given by (5.9)

$$V_X = V_{X1}\cos(w_0 t)$$

$$V_Y = a_1 V_X + a_2 V_X^2 + a_3 V_X^3 \qquad \text{(i)}$$

Substituting the expression of V_X into (i), we get the Fourier representation

$$V_Y = V_{Y1}\cos(w_0 t) + V_{Y2}\cos(2w_0 t) + V_{Y3}\cos(3w_0 t)$$

$$V_Y = V_{X1}\cos(w_0 t)[a_1(w_o) + \frac{3}{4}a_3(w_0){V_{x1}}^2] + a_2(w_0)\frac{V_{X1}^2}{2}$$

$$+V_{X1}\cos 2(w_0 t)[a_2(w_0)\frac{V_{X2}^2}{2}] + \frac{a_3(w_0)}{4}{V_{x1}}^3\cos(3w_0 t) \qquad \text{(ii)}$$

By neglecting the DC term in (ii) we get

$$V_{Y1} = a_1(w_o) + \frac{3}{4}a_3{V_{x1}}^3$$

$$V_{Y2} = \frac{V_{X1}^2}{2}a_2(w_0)$$

$$V_{Y3} = \frac{V_{X1}^3}{4}a_3(w_0) \qquad \text{(iii)}$$

Equation (ii) relates coefficients a_k to the magnitude of the k-th harmonic of V_{Yk}.

$$a_1 = \frac{V_{Y1} - 3V_{Y3}}{V_{x1}}; a_2 = 2\frac{V_{Y2}}{{V_{x1}}^2}$$

$$a_3 = 4\frac{V_{Y3}}{{V_{x1}}^3} \quad \text{(iv)}$$

By using the Fourier integral shown in equation (v) we can evaluate the each component of $V_{Y,k}$ and then by substituting the obtained values in relation (iv) we get the coefficients a_1, a_2, a_3 which are frequency independent (17,19)

$$V_{Y,k} = \frac{w_0}{2\pi}\int_0^{\frac{2\pi}{w_0}} V_Y(t)\, e^{jkw_0 t} \quad \text{(v)}$$

5.6 SIMULATION RESULTS

The functionality of the proposed Wien oscillator has been verified through SPICE simulations and the OTRA buffer is realized using commercially available IC AD844N as shown in Fig. 5.2 [20] .The circuit is designed for an f_o of 0.96MHz. The capacitor values are chosen as $C_1 = C_2 = 330$ pF and the resistive component values are computed as $R_1 = R_2 = 500\ \Omega$, $R_4 = 3.615\ k\Omega$ and $R_3 = 1\ k\Omega$. The supply voltages are chosen as ±1.5v for simulations. The simulated output waveform of the circuit of Fig.5.1 is shown in Fig. 5.3. The simulated f_o is observed to be 0.91MHz Fig.5.4.and is in close agreement with the theoretical value.

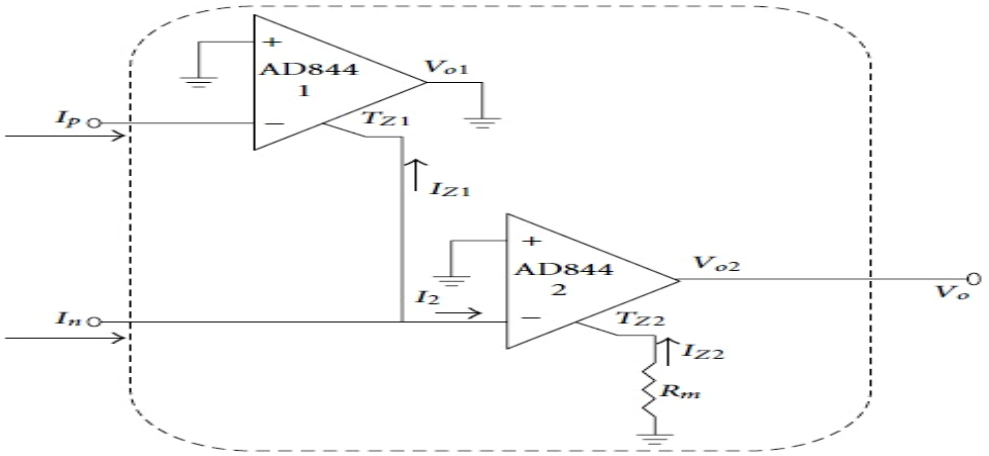


Fig. 5.2. OTRA implementation using IC AD 844AN [20]

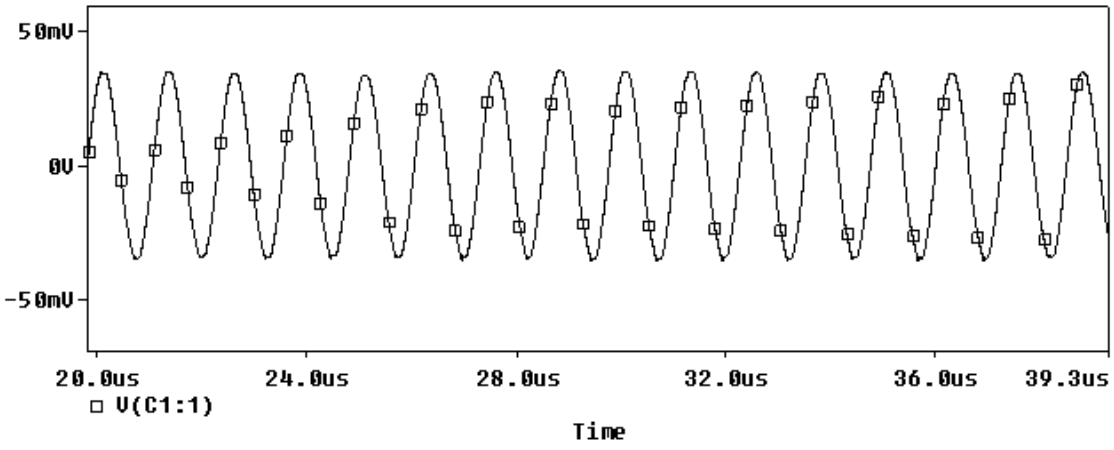


Fig. 5.3. Simulated output of Wein oscillator

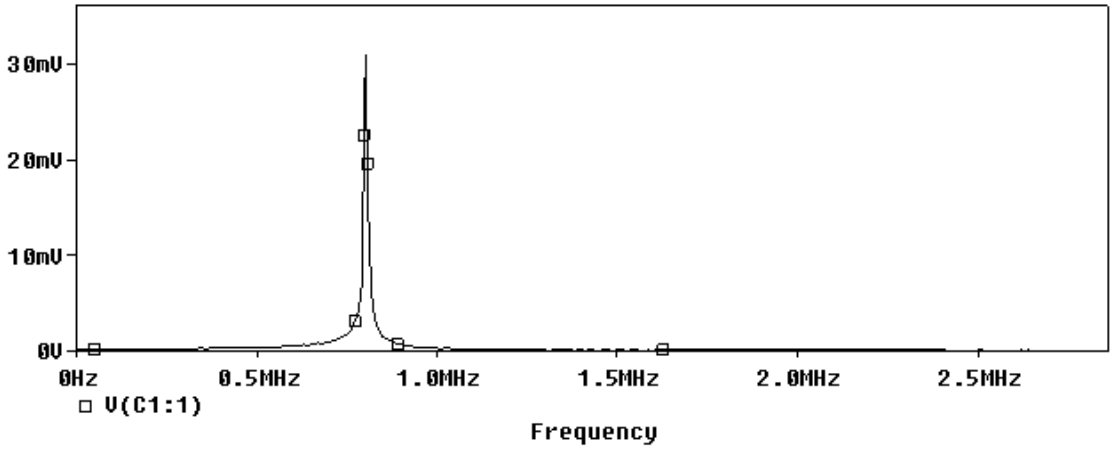


Fig. 5.4 Frequency spectrum

TABLE.5. TOTAL HARMONIC DISTORTION FOR FIG.5.1.

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE(DEG)
1	8.000E+05	1.168E-02	1.000E+00	1.403E+02	0.000E+00
2	1.600E+06	1.131E-04	9.678E-03	-1.504E+02	-4.311E+02
3	2.400E+06	1.170E-04	1.001E-02	5.027E+01	-3.707E+02
TOTAL HARMONIC DISTORTION = 1.392429E+00 PERCENT					

References

[1] I. Elahi, K. Muhammad, and P. T. Balsara, "IIP2 and DC offsets in the presence of leakage at LO frequency," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 10, pp. 647–651, Aug. 2006.

[2] L. Liu and Z. Wang, "Analysis and design of a low-voltage RF CMOS mixer," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 3, pp.212–216, Mar. 2006.

[3] U. Karthaus, "A differential two-pin crystal oscillator—concept, analysis, and implementation," *IEEE Trans. Circuits Syst. II, Exp. Briefs*,vol. 53, no. 10, pp. 1073–1077, Oct. 2006.

[4] D. N. Loizos and P. P. Sotiriadis, "A quadrature sinusoidal oscillator with phase-preserving wide-range linear frequency tunability and frequency- independent amplitude," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 11, pp. 1279–1283, Nov. 2006.

[5] A class of RC oscillators Holt, A.G.J. ; Lee, M.R. Proceedings of the IEEE Volume: 55 , Issue: 6 Digital Object Identifier: 10.1109/PROC.1967.5762 Publication Year: 1967 , Page(s): 1119

[6] A. Budak, K. Nay, "Operational amplifier circuits for the Wien Bridge oscillator," IEEE Trans Circuits Syst., vol. 28, No 2, pp 930- 934, September 1981.

[7] High-performance CMOS current feedback operational amplifier Pennisi, S. Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium

[8] P. Promme and K. Dejhan, "An integrable electronic controlled sinusoidal oscillator using CMOS operational transconductance amplifier," Int. J. Electron., 89,pp. 365–379, 2002.

[9] Precise insensitive tunable RC-oscillator realisation using current conveyors Nandi,R. Electronic Circuits and Systems, IEE Proceedings G Volume: 133 , Issue: 3

[10] H. Mostafa and A. M. Soliman, "A modified realization of the OTRA," Frequenz, vol.60, pp.70-76, 2006.

[11] C. Toumazou, F. J. Lidgey, and D. Haigh, *Analog IC Design: The Current-Mode Approach*. Exeter, U.K.: Peter Peregrinus, 1990.

[12] K. N. Salama and A. M. Soliman, "CMOS operational transresistance amplifier for analog signal processing applications," *Microelectron. J.*, vol. 30, pp. 235–245, 1999.

[13] "Novel oscillators using operational transresistance amplifier," *Microelectron. J.*, vol. 31, pp. 39–47, 2000.

[14] J. Chen, H. Tsao, S. Liu, andW. Chui, "Parasitic capacitance insensitive current-mode filters using operational transresistance amplifier," *Proc. IEE Circuit Devices Syst.*, vol. 142, no. 3, pp. 186–192, 1995.

[15] J. Chen, H. Tsao, and C. Chen, "Operational transresistance amplifierusing CMOS technology," *Electron. Lett.*, vol. 28, no. 22, pp.

[16]A. S. Sedra, and K. C. Smith, Microelectronic Circuits. Oxford University Press, New York, 2004.

[17] Rajeshwari Pandey, Neeta Pandey, Gurumurthy Komanapalli, Rashika Anurag "OTRA Based Voltage Mode Third Order Quadrature Oscillator" ISRN Electronics Volume 2014, Article ID 126471, 5 pages

[18] G. Palumbo, M. Pennisi, and S. Pennisi, "Analysis and evaluation of harmonic distortion in the tunnel diode oscillator," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2006, pp. 290–294.

[19] G. Palumbo, M. Pennisi, S. Pennisi, "Wien-type oscillators: evaluation and optimization of harmonic distortion," *IEEE Trans. Circuits Syst. II,*accepted for publication.

[20]R. Pandey, N. Pandey, M. Bothra, and S.K. Paul, "Operational Transresistance Amplifier-Based Multiphase Sinusoidal Oscillators", Journal of Electrical and Computer Engineering 2011; 8 pages DOI :10.1155/2011/586853

CHAPTER: 6
OTRA BASED VOLTAGE MODE THIRD ORDER QUADRATURE OSCILLATOR

6.1 Quadrature oscillators (QO) produce outputs having a phase difference of 90°. The phase-locked sine-cosine relationship of QO has useful applications in the field of telecommunications where the modulation scheme utilizes both in-phase and quadrature components, such as in single-sideband generators, and quadrature mixers [1]. The QOs are also used extensively in the field of instrumentation and power electronics [2]. For these applications low value of total harmonic distortion (THD) is an essential requirement as higher harmonics have detrimental effects on electrical equipment. These higher order harmonics can also interfere with communication transmission lines since they oscillate at the same frequencies as the transmit frequency. If left unchecked, increased temperature and interference can greatly shorten the life of electronic equipment and cause damage to power systems.

It is well known that a higher order networks as compared to lower order circuits, provide better accuracy, frequency response and distortion performance [3,4]. However, it has been observed that higher order QO designs have not been explored much, as only a few third order QOs [1, 3 – 16] have appeared in literature in recent years. A careful observation suggests that the reported QO designs are based on forming closed loop using (i) two lossy and one lossless integrators [3 – 5], (ii) one lossy and two lossless integrators [8], (iii) a second order low pass filter followed by an integrator [1, 6,7, 10 – 16] (iv) three low pass filters and gained feedback around the loop [9]. These topologies are designed using second generation current conveyor (CCII) [1, 6], second generation current controlled conveyor (CCCII) [7– 9], differential voltage current conveyor (DVCC) [10] opamp [5], operational transconductance amplifier (OTA) [3], current difference transconductance amplifier (CDTA) [4, 11], operational transresistance amplifier (OTRA) [12] and current-controlled current difference transconductance amplifier (CCCDTA) [13]. The

structure proposed in [15] uses Differential difference current conveyor (DDCC) and OTA whereas design of [16] is based on CCCDTA and OTA.

The OTRA is a current input voltage output device [17]. Being a current processing block, it inherits all the advantages of current mode techniques [12] and provides voltage output at low impedance which can readily be used to drive voltage input circuits without increasing component count. An extensive literature review suggests though a large number of OTRA based second order QOs [17-21] are available in literature, yet only a single third order QO topology using OTRA [12] is reported. This QO design and is based on forming a closed loop using a second order low pass filter followed by an integrator.

. In this chapter two topologies of third order QO based on OTRA have been presented which use the scheme of lossy and lossless integrators. One of the proposed circuits makes use of one inverting lossy and two lossless integrators connected in a feedback forming closed loop whereas the other configuration uses one lossless and two lossy integrators to form closed loop. The proposed structures can be made fully integrated by implementing the resistors using matched transistors operating in linear region and can be tuned electronically.

6.2 Quadrature oscillator (Using one lossy and two lossless integrators)

The first QO topology is shown in Fig.6.1. It uses two lossless integrators and a lossy inverting integrator in the feedback forming a closed loop resulting in loop gain of the system as $A(s)\beta(s)$ where $A(s)$ is forward path gain involving OTRA2, OTRA3 and $\beta(s)$ is feedback gain involving OTRA1.

The criterion for oscillations [23] to occur, is given by

$$1- A(s)\,\beta(s) =0 \qquad (6.1)$$

If this criterion is satisfied the closed loop system will result in two quadrature phase oscillations, available at nodes 1 and 2. Routine analysis of the circuit of Fig. 6.1 results in following characteristic equation as

$$s^3 c_1 c_2 c_3 R_2 R_3 + \frac{s^2 C_2 C_3 R_2 R_3}{R_4} + s c_3 \frac{R_3}{R_5} + \frac{1}{R_1} = 0 \tag{6.2}$$

From this characteristic equation the condition of oscillation (CO) and frequency of oscillation (FO) can be found to be

$$\text{FO:} \qquad f = \frac{1}{2\pi}\sqrt{\frac{1}{C_1 C_2 R_2 R_5}} \tag{6.3}$$

$$\text{CO:} \qquad R_4 R_5 = R_1 R_3 \tag{6.4}$$

The FO can be adjusted to desired value through R_2 and proper selection of resistor R_1, R_3 and R_4 would satisfy the CO.

6.3 Quadrature oscillator (Using Two lossy and one lossless integrators

The second proposed QO configuration is shown in Fig.6.2 which makes use of two lossy and one lossless integrator, all in inverting mode.

The characteristic equation of the Circuit II can be deduced as

$$s^3 C_1 C_2 C_3 R_3 + s^2 \left(\frac{C_2 C_3 R_3}{R_4} + \frac{C_1 C_3 R_3}{R_5}\right) + \frac{s C_3 R_3}{R_4 R_5} + \frac{1}{R_1 R_2} = 0 \tag{6.5}$$

$$\text{FO: } f = \frac{1}{2\pi}\sqrt{\frac{1}{C_1 C_2 R_4 R_5}} \tag{6.6}$$

$$\text{CO: } R_1 R_2 R_3 C_3 \left[R_4 C_1 + R_5 C_2\right] = R_4^2 R_5^2 C_1 C_2 \tag{6.7}$$

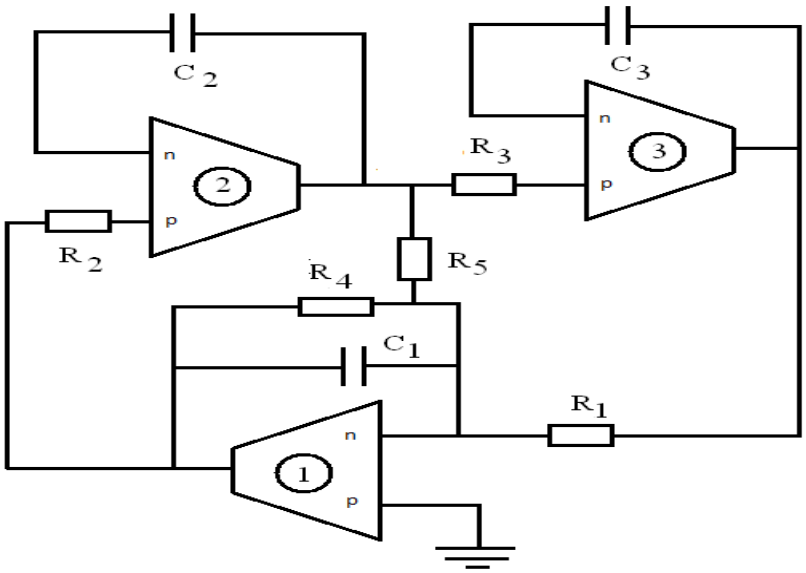


Fig.6.1. Proposed circuit I

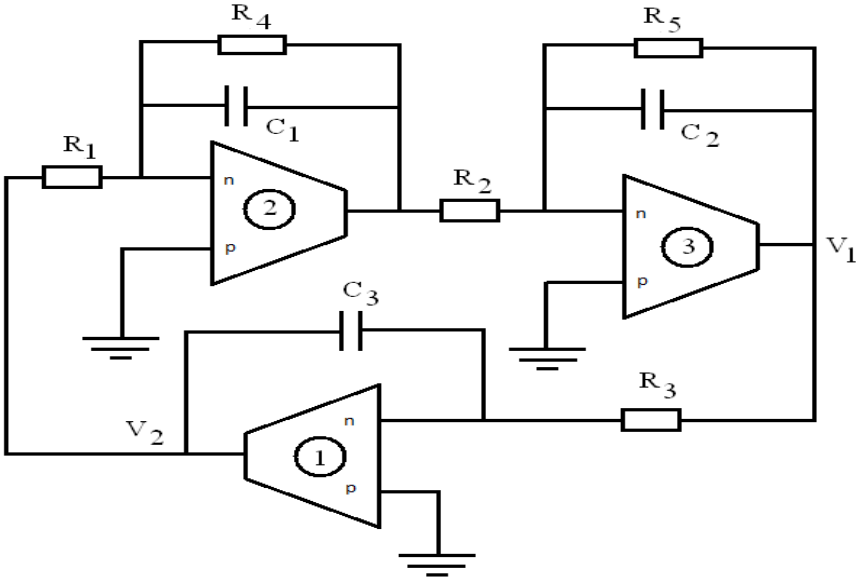


Fig.6.2 Proposed circuit II

By suitable selection of R_4 and R_5 the FO can be adjusted to desired value and proper selection of resistors R_1, R_2, and R_3 results in desired CO.

The current differencing property of the OTRA makes it possible to implement the resistors connected to the input terminals of OTRA, using MOS transistors with complete non linearity cancellation [17]. Each resistor requires two matched n-MOSFETs connected in a manner as shown in Fig 6.3 which represents a typical MOS implementation of resistance connected at negative input of OTRA.

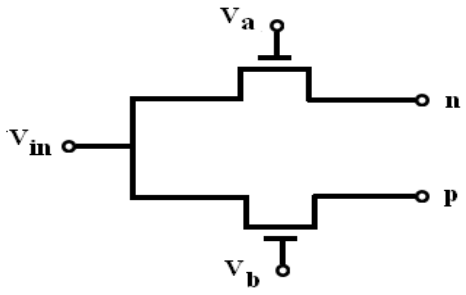


Fig.6.3. MOS based resistor [17]

Symbols ‘p’ and ‘n’ represent the non-inverting and the inverting terminals of the OTRA. As can be seen from the figure, the voltages at the drain and the source terminals for both MOSFETs are equal. On taking the difference of the currents flowing in the two transistors, the non linearity gets cancelled out. The resistor value realized can be expressed as

$$R = \frac{1}{K_N(V_a - V_b)} \tag{6.8}$$

Where

$$K_N = \mu\, C_{OX}\, \frac{W}{L} \tag{6.9}$$

K_N needs to be determined for the transistors being used to implement the resistors and μ, C_{OX} and W/L represent standard transistor parameters. The MOS based implementation of Circuit I and Circuit II are shown in Fig.6.4 and Fig. 6.5 respectively.

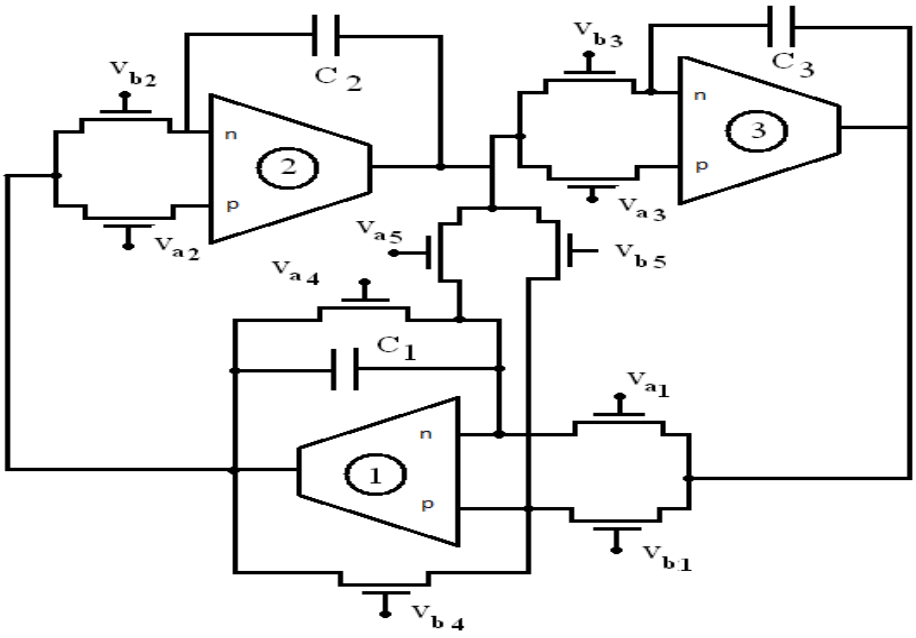


Fig.6.4. The MOS based implementation of QO Circuit I

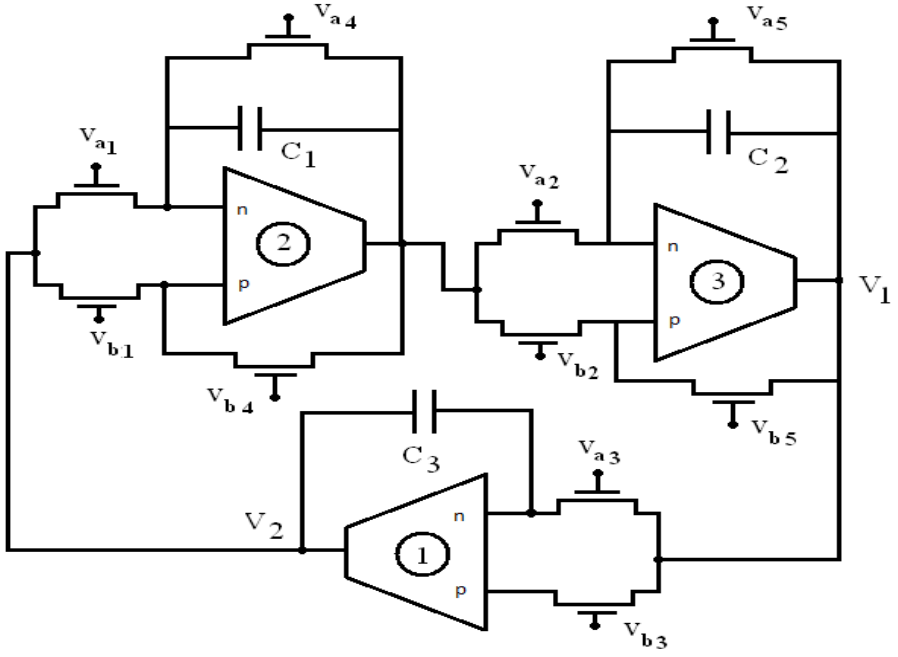


Fig.6.5. MOS based implementation of QO Circuit II

6.2 NON-IDEAL ANALYSIS

The output of the QO may deviate due to non ideality of OTRA in practice. Ideally the transresistance gain R_m is assumed to approach infinity. However, practically R_m is a frequency dependent finite value. Considering a single pole model for the trans-resistance gain, R_m can be expressed as

$$R_m(s) = \left(\frac{R_0}{1+\frac{s}{\omega_0}}\right) \tag{6.10}$$

Where R_0 is dc transresistance gain.

For high frequency applications the transresistance gain R_m (s) reduces to

$$R_m(s) = \left(\frac{1}{sC_p}\right) \tag{6.11}$$

Where $C_p = \frac{1}{R_0\ \omega_0}$

Taking this effect into account (6.2) modifies to

$$s^3(c_1+c_p)(c_2+c_p)(c_3+c_p)R_2R_3 + s^2(c_2+c_p)(c_3+c_p)\frac{R_2R_3}{R_4} + s(c_3+c_p)\frac{R_3}{R_5} + \frac{1}{R_1} = 0 \tag{6.12}$$

From (6.3) it is found that FO for circuit I changes to

$$f = \frac{1}{2\pi}\sqrt{\frac{1}{(C_1+C_p)(C_2+C_p)R_2R_5}} \tag{6.13}$$

Due to non ideality effect of OTRA (6.5) changes to

$$s^3(c_1+c_p)(c_2+c_p)(c_3+c_p)R_3 + s^2\left(\left(c_2+c_p\right)\left(c_3+c_p\right)\frac{R_3}{R_4}\right.$$
$$\left.+\left(c_1+c_p\right)\left(c_3+c_p\right)\frac{R_3}{R_5}\right) + s(c_3+c_p)\frac{R_3}{R_4R_5} + \frac{1}{R_1R_2} = 0 \quad (6.14)$$

The characteristic equation represented by (6.6) results in modified FO for circuit II and is expressed as

$$f = \frac{1}{2\pi}\sqrt{\frac{1}{(C_1+C_p)(C_2+C_p)R_4R_5}} \quad (6.15)$$

The effect of C_p can be eliminated by pre-adjusting the values of capacitors C_1, C_2 and C_3 thus achieving self compensation.

6.3 SIMULATION RESULTS

The proposed QO is verified through simulations using the CMOS implementation of the OTRA [22] which is shown in chapter 2. The SPICE simulations are performed using 0.5 μm CMOS process parameters provided by MOSIS (AGILENT). Supply voltages taken are ±1.5V. Both the QO topologies are designed for an FO of 159 KHz and the simulated value was observed to be 161 KHz and for Circuit I and II respectively. The simulated transient output and corresponding frequency spectrum for Circuit I are shown in Fig.6.6 and Fig. 6.7respectively and those for Circuit II are depicted in Fig.6.8and Fig.6.9. The percentage total harmonic distortion (THD) is 0.57% for QO Circuit I and that for Circuit II is observed to be 0.7%. These values are considerably low as compared to 6.3 % THD of QO circuit of [8].

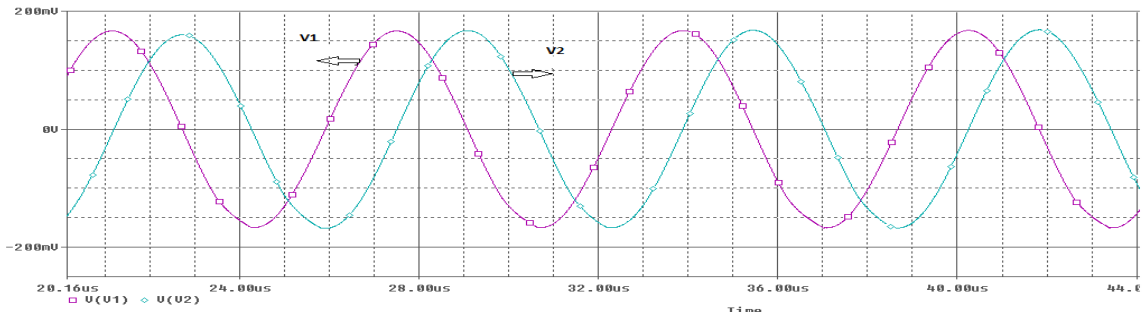


Fig.6.6 Transient Output of proposed QO Circuit I

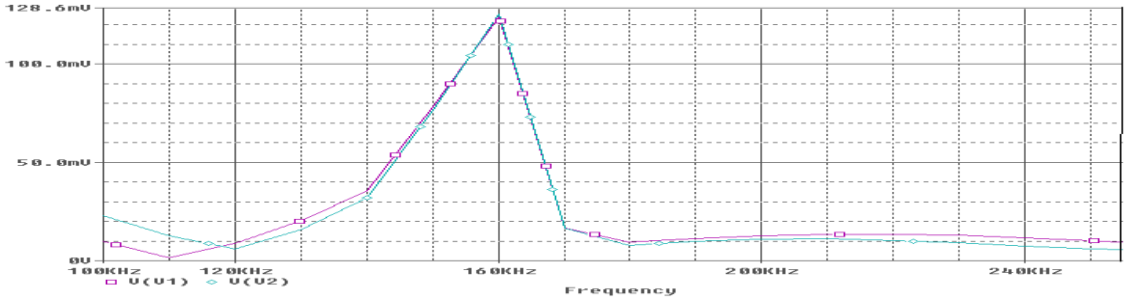


Fig.6.7 Frequency spectrum of output of QO Circuit I

TABLE.6.1 TOTAL HARMONIC DISTORTION FOR QO Circuit I

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE(DEG)
1	1.590E+05	1.664E-01	1.000E+00	1.285E+02	0.000E+00
2	3.180E+05	6.634E-05	3.987E-04	-3.792E+01	-2.949E+02
3	4.770E+05	8.920E-05	5.360E-04	3.469E+00	-3.819E+02
4	6.360E+05	5.690E-05	3.420E-04	2.738E+01	-4.865E+02
5	7.950E+05	5.302E-05	3.186E-04	1.105E+01	-6.313E+02
6	9.540E+05	4.697E-05	2.823E-04	3.717E+01	-7.336E+02
7	1.113E+06	2.596E-05	1.560E-04	2.165E+01	-8.776E+02
8	1.272E+06	3.556E-05	2.137E-04	2.709E+01	-1.001E+03
9	1.431E+06	2.084E-05	1.252E-04	4.590E+01	-1.110E+03
10	1.590E+06	1.984E-05	1.192E-04	1.732E+01	-1.267E+03
TOTAL HARMONIC DISTORTION = 9.188258E-02 PERCENT					

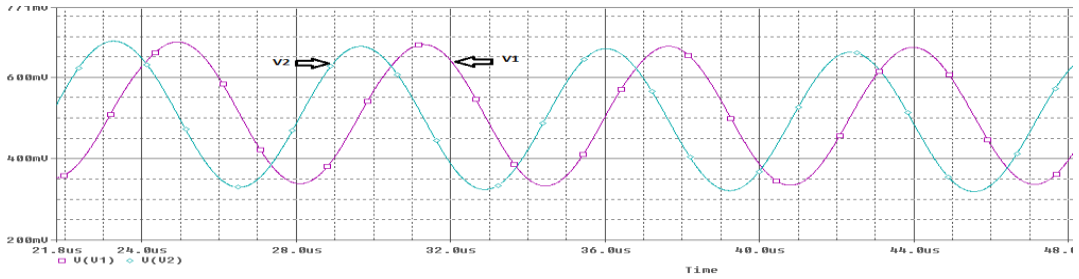


Fig.6.8 Transient output of proposed QO Circuit II

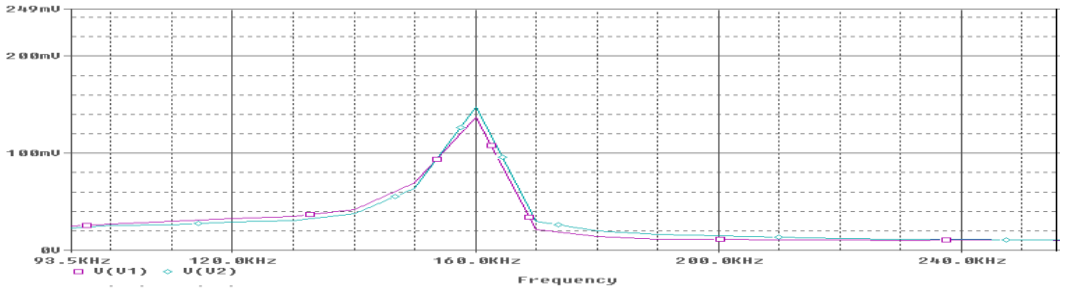


Fig.6.9 Frequency spectrum of output of QO Circuit II

TABLE.6.2 TOTAL HARMONIC DISTORTION FOR QO Circuit II

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE(DEG)
1	1.600E+05	1.665E-01	1.000E+00	-1.333E+02	0.000E+00
2	3.200E+05	1.796E-03	1.079E-02	-1.270E+02	1.396E+02
3	4.800E+05	7.988E-04	4.798E-03	-1.540E+02	2.460E+02
4	6.400E+05	2.985E-04	1.793E-03	-1.432E+02	3.902E+02
5	8.000E+05	3.953E-04	2.375E-03	-1.076E+02	5.592E+02
6	9.600E+05	4.955E-04	2.976E-03	-1.201E+02	6.800E+02
7	1.120E+06	4.570E-04	2.745E-03	-1.316E+02	8.018E+02
8	1.280E+06	4.258E-04	2.558E-03	-1.335E+02	9.332E+02
9	1.440E+06	4.450E-04	2.673E-03	-1.389E+02	1.061E+03
10	1.600E+06	4.350E-04	2.613E-03	-1.496E+02	1.184E+03
TOTAL HARMONIC DISTORTION = 1.360575E+00 PERCENT					

References

[1] J.W. Horng, C.L. Hou, C.M. Chang, W.-Y. Chung, H.-W. Tang and Y-H. Wen "Quadrature oscillators using CCIIs," Int. J. Electron, vol. 92, pp. 21–31,2005.

[2] J.W. Horng, C.L. Hou, C.M. Chang, H.P. Chou, C.T. Tin and Y.H. Wen. "Quadrature oscillators with grounded capacitors and resistors using FDCCIIs," ETRI Journal, vol.28,pp. 486 – 94,2006.

[3] P. Promme and K. Dejhan, "An integrable electronic controlled sinusoidal oscillator using CMOS operational transconductance amplifier," Int. J. Electron., vol.89, pp. 365–379, 2002.

[4] J. W. Horng, "Current-mode third-order quadrature oscillator using CDTAs," Active and Passive Electronic Components, 2009, Article ID 789171, p. 1-5.

[5] J. W. Horng, "Quadrature Oscillators using Operational Amplifiers," Active and Passive Electronic Components 2011, Article ID 320367, DOI:10.1155/2011/32036.

[6] J. W. Horng "Current/ Voltage mode third order quadrature oscillator employing two multiple outputs CCIIs and grounded capacitor," Indian Journal of Pure and Applied Physics vol.49, pp.494-498, 2011.

[7] S Maheshwari, and I. A. Khan, "Current controlled third order quadrature oscillator," IEE Proc.-Circuits, Devices and Systems, vol. 152, pp. 605-607, 2005.

[8] S. Maheshwari and I.A. Khan, "Current controlled third order quadrature oscillator," IET Circuits Devices Systems, vol. 4, pp. 188–195,2010.

[9] S.Maheshwari and R. Verma, "Electronically Tunable Sinusoidal Oscillator Circuit," Active and Passive Electronic Components Volume 2012, Article ID 719376, 6 pages DOIi:10.1155/2012/719376

[10] S. Maheshwari, "Analogue signal processing applications using a new circuit topology," IET Circuits Devices Systems vol. 3, pp.106–115. 2009.

[11] J. W. Horng, H Lee and J.Y. Wu, "Electronically tunable third order Quadrature oscillators using CDTAs," RadioEngineering vol. 19, pp. 326-330, 2010.

[12] R. Pandey, N. Pandey and S.K. Paul, "MOS-C Third Order Quadrature Oscillator using OTRA,". Third International Conference on Communication and Computer Technology, ICCCT-12, pp.77 -80, 2012.

[13]S. Lawanwisut and M. Siripruchyanun, "High Output-impedance Current-mode Third-Order Quadrature Oscillator Based on CCCCTAs," TENCON 2009 – 2009 IEEE Region 10 Conference, pp.1-4, 2009.

[14] A. Kwawsibsam, B.Sreewirote, and W. Jaikla, "Third-Order Voltage-Mode Quadratrue Oscillator Using DDCC and OTAs," 2011 International Conference on Circuits, System and Simulation, pp.317-21, 2011

[15] M. Kumngern and S. Junnapiya, "Current-Mode Third-Order Quadrature Oscillator Using Minimum Elements," 2011 International Conference on Electrical Engineering and Informatics, pp. 1 – 4, 2011.

[16] D. Duangmalai W. Jaikla, "Realization of Current-mode Quadrature Oscillator Based on Third Order Technique," ACEEE International Journal on Electrical and Power Engineering, vol.2, pp.46 – 49, 2011.

[17] K. N. Salama and A. M. Soliman, "CMOS Operational Transresistance Amplifier for analog signal processing applications." Microelectron. J.,vol. 30, pp. 235–245, 1999.

[18] K.N. Salama and A.M. Soliman, "Universal filters using the operational transresistance amplifiers," AE U—International Journal of Electronics and Communications, vol. 53, pp. 49–52, 1999.

[19] S. Kilinc and U. Cam , "Operational Transresistance Amplifier Based First-Order Allpass Filter with an Application Example," The 47th IEEE International Midwest Symposium on Circuits and System, pp. I65-I68, 2004.

[20] S. Kilinc and U. Cam, "Cascadable allpass and notch filters employing single operational transresistance amplifier," Computers and electrical Engineering vol.31, pp 391-401, 2005.

[21] C Cakir, U. Cam, and O. Cicekoglu, “Novel All pass Filter Configuration Employing Single OTRA,” IEEE Transactions on circuits and systems—ii: express briefs., vol.52, pp.122-125, 2005

[22] H. Mostafa and A. M. Soliman, “A modified realization of the OTRA,” Frequenz, vol.60, pp.70-76, 2006.

[23] A. S. Sedra, and K. C. Smith, Microelectronic Circuits. Oxford University Press, New York, 2004.

CHAPTER 7
CONCLUSION

7.1 Design of different type sinusoidal oscillators based on OTRA are presented which have low Total harmonic distortion (THD) Chapter 1 presents a brief background followed by objectives and scope of work. Chapter 2 describes the OTRA and its CMOS realization that has been used for simulation of various proposed circuits.In chapter3 two topologies of sinusoidal oscillators are presented. The first topolgy is based on lossless integrators whereas the second one is designed using second order allpass section. In chapter 4 Wein bridge oscillator is designed using OTRA. A detailed mathematical analysis has been presented for THD calculations. Two topologies of third order OTRA based quadrature oscillator are presented in chapter 5, using lossy and lossless integrators. Both the proposed topologies can be implemented using MOS-C structures which take less chip area for the design. The effect of non ideal behaviour of OTRA and high frequency compensation scheme has also been included.

All the proposed structures are simulated using PSPICE using typical 0.5 µ procss parameters. It is observed that the results are in close agreement with theoretical propositions All the proposed circuits have a very low value of % THD. The effect of non ideal behaviour of OTRA has been included in all the proposed structure.

Table: 7 Summary of Proposed Circuits

Circuit	Active element	Number of C Used	Number of R used	C.O	F.O	MOS C Implementation
Fig.3.2	Single OTRA	3 Floating	3 Floating	$c_1 = 4c_2$ $R_2 = 4R_1$	$f = \frac{1}{2\pi}\sqrt{\frac{1}{C_1C_2R_1R_2}}$	Possible
Fig.3.3	Two OTRA'S	2 Floating	2 Floating	NONE	$f = \frac{1}{2\pi}\sqrt{\frac{1}{C_1C_2\,R_2R_1}}$	Possible
Fig. 4.1	OTRA,BUFFER	One Grounded, One floating	One Grounded, One floating	$K = 2 + R_1/R_2$ K = R_4/R_3	$f_0 = \frac{1}{2\pi C\sqrt{R_1R_2}}$	Not Possible
Fig 5.1	Three OTRA'S	3 Floating	5 Floating	$R_4R_5 = R_1R_3$	$f = \sqrt{\frac{1}{C_1C_2R_2R_5}}$	Possible
Fig.5.2	Three OTRA'S	3 Floating	5 Floating	$R_1R_2R_3C_3\,[R_4C_1 + R_5C_2] = R_4^2R_5^2C_1C_2$	$f = \frac{1}{2\pi}\sqrt{\frac{1}{C_1C_2R_4R_5}}$	Possible

7.2 Future scope

In this thesis some of the sinusoidal oscillators using OTRA are discussed. There is always a possibility of scope of improvement.The presented work can further be enhanced by including the harmonic analysis for the oscillators discussed in chapter 4 and chapter 6.The phase analysis of the quadrature oscillators presented in chapter 6 can also be carried out.

It has been observed through literature survey that OTRA based non linear applications have not been paid much attention and is an area which can be further explored.

7.3 Appendix:

Simulations have been performed using SPICE at 0.5um technology and the model files provided by MOSIS (AGILENT) used have the following parameters:

```
.MODEL MBREAKN nmos
+ LEVEL=3
+ UO=460.5
+ TOX=1E-8
+ TPG=1
+ VTO=.62
+ JS=1.8E-6
+ XJ=.15E-6
+ RS=417
+ RSH=2.73
+ LD=4E-8
+ ETA=0
+ VMAX=130E3
+ NSUB=1.71E17
+ PB=.761
+ PHI=.905
+ THETA=.129
+ GAMMA=.69
+ KAPPA=0.1
+ AF=1
+ WD=1.1E-7
+ CJ=76.4E-5
+ MJ=.357
+ CJSW=5.68E-10
+ MJSW=.302
+ CGSO=1.38E-10
+ CGDO=1.38E-10
+ CGBO=3.45E-10
```

+ KF=3.07E-28

+ DELTA=0.42

+ NFS=1.2E11

+ W=90U

+ L=4U

.MODEL MBREAKP pmos

MBREAKP

+ LEVEL=3

+ UO=100

+ TOX=1E-8 + TPG=1

+ VTO=-.58

+ JS=.38E-6

+ XJ=.1E-6

+ RS=886

+ RSH=1.81

+ LD=3E-8

+ ETA=0

+ VMAX=113E3

+ NSUB=2.08E17

+ PB=.911

+ PHI=.905

+ THETA=.12

+ GAMMA=.76

+ KAPPA=2

+ AF=1

+ WD=1.4E-7

+ CJ=85E-5

+ MJ=.429

+ CJSW=4.67E-10

+ MJSW=.631

+ CGSO=1.38E-10

+ CGDO=1.38E-10

+ CGBO=3.45E-10

+ KF=1.08E-29

+ DELTA=0.81

+ NFS=.52E11

+ W=200U

+ L=4U

Hindawi Publishing Corporation
ISRN Electronics
Volume 2014, Article ID 126471, 5 pages
http://dx.doi.org/10.1155/2014/126471

Research Article

OTRA Based Voltage Mode Third Order Quadrature Oscillator

Rajeshwari Pandey,[1] Neeta Pandey,[1] Gurumurthy Komanapalli,[1] and Rashika Anurag[2]

[1] *Department of Electronics and Communication Engineering, Delhi Technological University, Delhi 110042, India*
[2] *Department of Electronics and Communication Engineering, JSS Academy of Technical Education, C-20/1 Sector 62, NOI DA, Uttar Pradesh 201301, India*

Correspondence should be addressed to Neeta Pandey; n66pandey@rediffmail.com

Received 2 February 2014; Accepted 9 March 2014; Published 29 April 2014

Academic Editors: S. Gift, R. Senani, and E. Tlelo-Cuautle

Copyright © 2014 Rajeshwari Pandey et al. This is an open access article distributed under the Creative Commons Attribution License, which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

Two topologies of operational transresistance (OTRA) based third order quadrature oscillators (QO) are proposed in this paper. The proposed oscillators are designed using a combination of lossy and lossless integrators. The proposed topologies can be made fully integrated by implementing the resistors using matched transistors operating in linear region, which also facilitates electronic tuning of oscillation frequency. The nonideality analysis of the circuit is also given and for high frequency applications self-compensation can be used. Workability of the proposed QOs is verified through PSPICE simulations using 0.5 μm AGILENT CMOS process parameters. The total harmonic distortion (THD) for both the QO designs is found to be less than 1%.

1. Introduction

Quadrature oscillators (QO) produce outputs having a phase difference of 90°. The phase-locked sine-cosine relationship of QO has useful applications in the field of telecommunications where the modulation scheme utilizes both in-phase and quadrature components, such as single-sideband generators and quadrature mixers [1]. The QOs are also used extensively in the field of instrumentation and power electronics [2]. For these applications low value of total harmonic distortion (THD) is an essential requirement as higher harmonics have detrimental effects on electrical equipment. These higher order harmonics can also interfere with communication transmission lines since they oscillate at the same frequencies as the transmit frequency. If left unchecked, increased temperature and interference can greatly shorten the life of electronic equipment and cause damage to power systems.

It is well known that higher order networks as compared to lower order circuits provide better accuracy, frequency response, and distortion performance [3, 4]. However, it has been observed that higher order QO designs have not been explored much, as only a few third order QOs [1, 3–16] have appeared in literature in recent years. A careful observation suggests that the reported QO designs are based on forming closed loop using (i) two lossy and one lossless integrators [3–5], (ii) one lossy and two lossless integrators [8], (iii) a second order low pass filter followed by an integrator [1, 6, 7, 10–16], and (iv) three low pass filters and gained feedback around the loop [9]. These topologies are designed using second generation current conveyor (CCII) [1, 6], second generation current-controlled conveyor (CCCII) [7–9], differential voltage current conveyor (DVCC) [10], op-amp [5], operational transconductance amplifier (OTA) [3], current difference transconductance amplifier (CDTA) [4, 11], operational transresistance amplifier (OTRA) [12], and current-controlled current difference transconductance amplifier (CCCDTA) [13]. The structure proposed in [15] uses differential difference current conveyor (DDCC) and OTA whereas design of [16] is based on CCCDTA and OTA.

The OTRA is a current input voltage output device [17]. Being a current processing block, it inherits all the advantages of current mode techniques [12] and provides voltage output at low impedance which can readily be used to drive voltage input circuits without increasing component count. An extensive literature review suggests though a large number of OTRA based second order QOs [17–21] are available in literature, yet only a single third order QO topology using

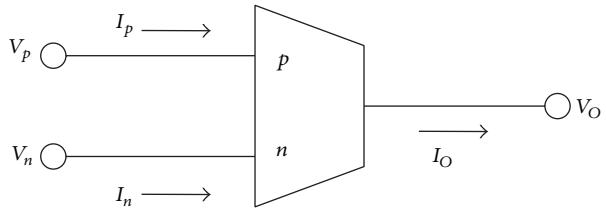


Figure 1: OTRA circuit symbol.

OTRA [12] is reported. This QO design is based on forming a closed loop using a second order low pass filter followed by an integrator.

In this paper two topologies of third order QO based on OTRA have been presented which use the scheme of lossy and lossless integrators. One of the proposed circuits makes use of one inverting lossy and two lossless integrators connected in a feedback forming closed loop whereas the other configuration uses one lossless and two lossy integrators to form closed loop. The proposed structures can be made fully integrated by implementing the resistors using matched transistors operating in linear region and can be tuned electronically.

2. Circuit Description

The OTRA is a high gain, current input voltage output analog building block [17]. The input terminals of OTRA are internally grounded, thereby eliminating response limitations due to parasitic capacitances and resistances and hence is a suitable choice for high frequency applications. The circuit symbol of OTRA is shown in Figure 1 and the port characteristics are given by (1), where R_m is transresistance gain of OTRA:

$$\begin{bmatrix} V_p \\ V_n \\ V_O \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ I_O \end{bmatrix}. \quad (1)$$

For ideal operations the R_m of OTRA approaches infinity and forces the input currents to be equal. Thus OTRA must be used in a negative feedback configuration [22].

2.1. Circuit I. The first QO topology is shown in Figure 2. It uses two lossless integrators and a lossy inverting integrator in the feedback forming a closed loop resulting in loop gain of the system as $A(s)\beta(s)$, where $A(s)$ is forward path gain involving OTRA2 and OTRA3 and $\beta(s)$ is feedback gain involving OTRA1.

The criterion for oscillations [23] to occur is given by

$$1 - A(s)\beta(s) = 0. \quad (2)$$

If this criterion is satisfied, the closed loop system will result in two quadrature phase oscillations, available at nodes 1 and 2. Routine analysis of the circuit of Figure 2 results in the following characteristic equation:

$$s^3 c_1 c_2 c_3 R_2 R_3 + \frac{s^2 C_2 C_3 R_2 R_3}{R_4} + sc_3 \frac{R_3}{R_5} + \frac{1}{R_1} = 0. \quad (3)$$

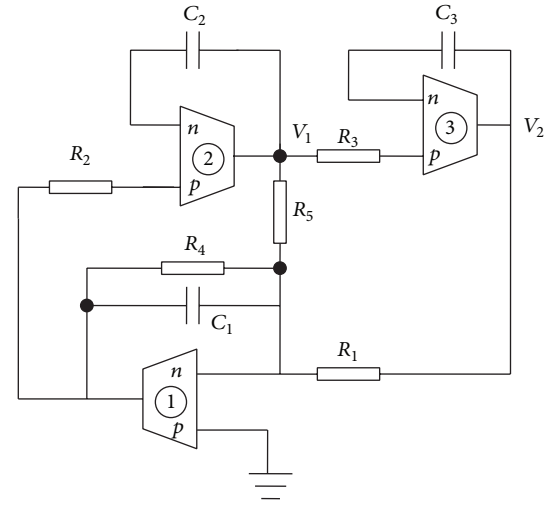


Figure 2: Proposed Circuit I.

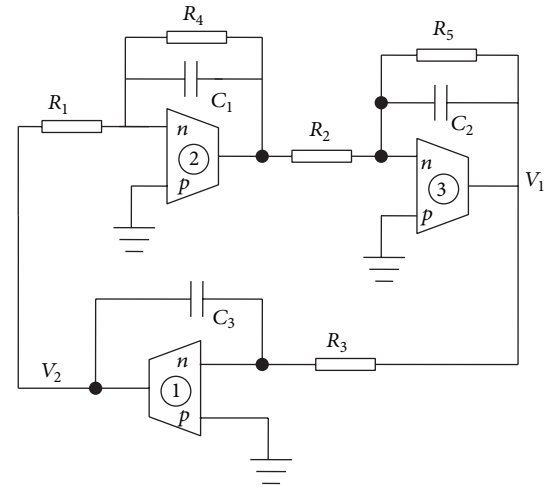


Figure 3: Proposed Circuit II.

From this characteristic equation the condition of oscillation (CO) and frequency of oscillation (FO) can be found to be FO:

$$f = \frac{1}{2\pi}\sqrt{\frac{1}{C_1 C_2 R_2 R_5}}, \quad (4)$$

CO:

$$R_4 R_5 = R_1 R_3. \quad (5)$$

The FO can be adjusted to desired value through R_2 and proper selection of resistors R_1, R_3, and R_4 would satisfy the CO.

2.2. Circuit II. The second proposed QO configuration is shown in Figure 3 which makes use of two lossy and one lossless integrators, all in inverting mode.

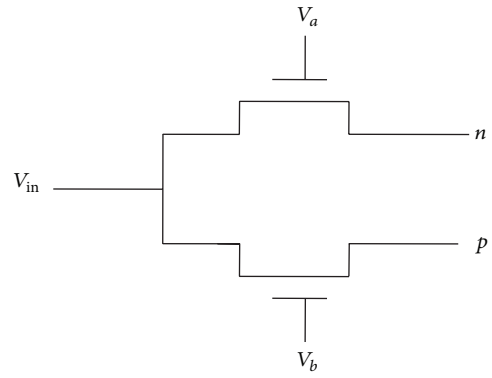


Figure 4: The MOS based resistor [17].

The characteristic equation of the Circuit II can be deduced as

$$s^3 C_1 C_2 C_3 R_3 + s^2 \left(\frac{C_2 C_3 R_3}{R_4} + \frac{C_1 C_3 R_3}{R_5} \right) + \frac{s C_3 R_3}{R_4 R_5} + \frac{1}{R_1 R_2} = 0, \tag{6}$$

FO:

$$f = \frac{1}{2\pi} \sqrt{\frac{1}{C_1 C_2 R_4 R_5}}, \tag{7}$$

CO:

$$R_1 R_2 R_3 C_3 \left[R_4 C_1 + R_5 C_2 \right] = R_4^2 R_5^2 C_1 C_2. \tag{8}$$

By suitable selection of R_4 and R_5 the FO can be adjusted to desired value and proper selection of resistors R_1, R_2, and R_3 results in desired CO.

The current differencing property of the OTRA makes it possible to implement the resistors connected to the input terminals of OTRA, using MOS transistors with complete nonlinearity cancellation [17]. Each resistor requires two matched n-MOSFETs connected in a manner as shown in Figure 4 which represents a typical MOS implementation of resistance connected at negative input of OTRA.

Symbols "p" and "n" represent the noninverting and the inverting terminals of the OTRA. As can be seen from the figure, the voltages at the drain and the source terminals for both MOSFETs are equal. On taking the difference of the currents flowing in the two transistors, the nonlinearity gets cancelled out. The resistor value realized can be expressed as

$$R = \frac{1}{K_N \left(V_a - V_b \right)}, \tag{9}$$

where

$$K_N = \mu C_{OX} \frac{W}{L}. \tag{10}$$

K_N needs to be determined for the transistors being used to implement the resistors and μ, C_{OX}, and W/L represent standard transistor parameters. The MOS based implementations of Circuit I and Circuit II are shown in Figures 5 and 6, respectively.

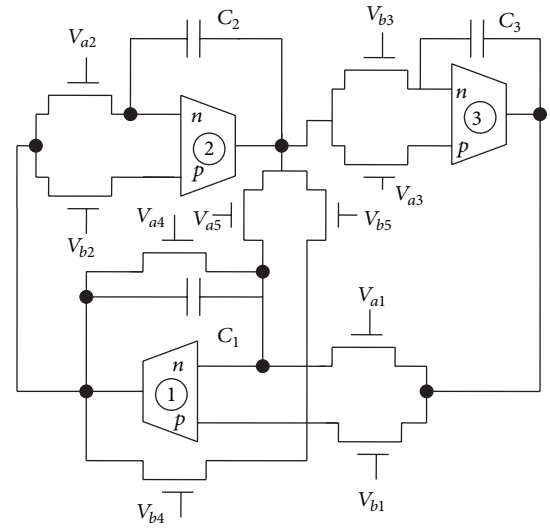


Figure 5: The MOS based implementation of QO Circuit I.

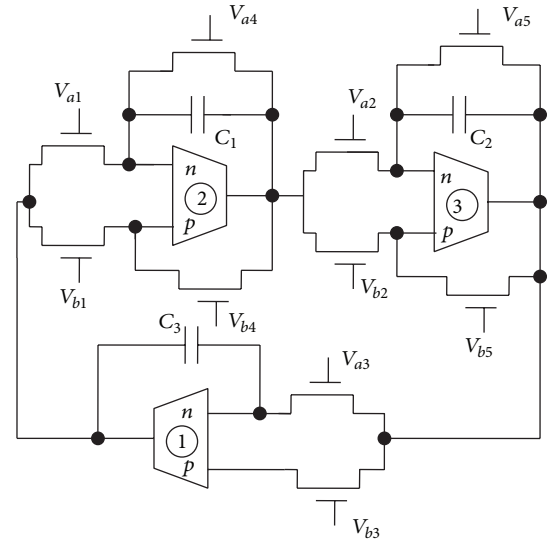


Figure 6: The MOS based implementation of QO Circuit II.

3. Nonideal Analysis

The output of the QO may deviate due to nonideality of OTRA in practice. Ideally the transresistance gain R_m is assumed to approach infinity. However, practically R_m is a frequency dependent finite value. Considering a single pole model for the transresistance gain, R_m can be expressed as

$$R_m(s) = \left(\frac{R_0}{1 + (s/\omega_0)} \right), \tag{11}$$

where R_0 is dc transresistance gain. For high frequency applications the transresistance gain $R_m(s)$ reduces to

$$R_m(s) = \left(\frac{1}{sC_p} \right), \tag{12}$$

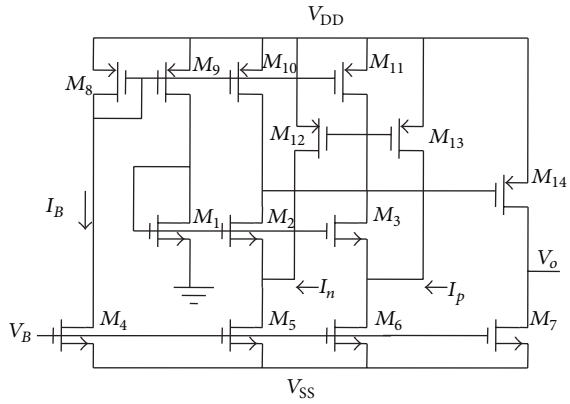


Figure 7: CMOS OTRA [22].

where

$$C_p = \frac{1}{R_0\omega_0}. \tag{13}$$

Taking this effect into account (3) modifies to

$$\begin{aligned} &s^3\left(c_1+c_p\right)\left(c_2+c_p\right)\left(c_3+c_p\right)R_2R_3 \\ &+s^2\left(c_2+c_p\right)\left(c_3+c_p\right)\frac{R_2R_3}{R_4} \\ &+s\left(c_3+c_p\right)\frac{R_3}{R_5}+\frac{1}{R_1}=0. \end{aligned} \tag{14}$$

From (14) it is found that FO for Circuit I changes to

$$f = \frac{1}{2\pi}\sqrt{\frac{1}{\left(C_1+C_p\right)\left(C_2+C_p\right)R_2R_5}}. \tag{15}$$

Due to nonideality effect of OTRA (6) changes to

$$\begin{aligned} &s^3\left(c_1+c_p\right)\left(c_2+c_p\right)\left(c_3+c_p\right)R_3 \\ &+s^2\left(\left(c_2+c_p\right)\left(c_3+c_p\right)\frac{R_3}{R_4}+\left(c_1+c_p\right)\left(c_3+c_p\right)\frac{R_3}{R_5}\right) \\ &+s\left(c_3+c_p\right)\frac{R_3}{R_4R_5}+\frac{1}{R_1R_2}=0. \end{aligned} \tag{16}$$

The characteristic equation represented by (16) results in modified FO for Circuit II and is expressed as

$$f = \frac{1}{2\pi}\sqrt{\frac{1}{\left(C_1+C_p\right)\left(C_2+C_p\right)R_4R_5}}. \tag{17}$$

The effect of C_p can be eliminated by preadjusting the values of capacitors C_1, C_2, and C_3, thus achieving self-compensation.

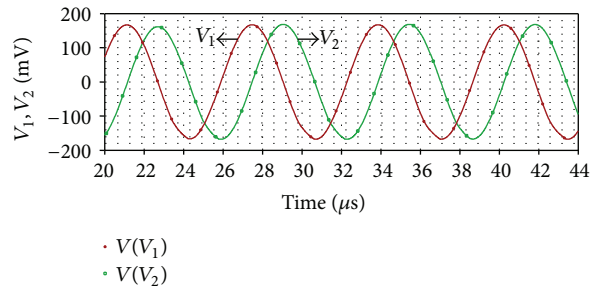


Figure 8: Transient output of proposed QO Circuit I.

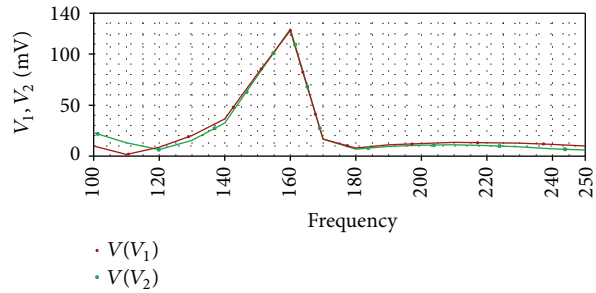


Figure 9: Frequency spectrum of output of QO Circuit I.

4. Simulation Results

The proposed QO is verified through simulations using the CMOS implementation of the OTRA [22] which is shown in Figure 7. The SPICE simulations are performed using 0.5 μm CMOS process parameters provided by MOSIS (AGILENT). Supply voltages taken are ±1.5 V. Both the QO topologies are designed for an FO of 159 KHz and the simulated value was observed to be 161 KHz for Circuits I and II, respectively. The simulated transient output and corresponding frequency spectrum for Circuit I are shown in Figures 8 and 9, respectively, and those for Circuit II are depicted in Figures 10 and 11. The percentage total harmonic distortion (THD) is 0.57% for QO Circuit I and that for Circuit II is observed to be 0.7%. These values are considerably low as compared to 6.3% THD of QO circuit of [12].

5. Conclusion

Two topologies of third order OTRA based quadrature oscillator are presented in this paper using lossy and lossless integrators. The simulations are performed using PSPICE and it is observed that the results are in close agreement with theoretical propositioned. The simulated value of % THD in both the circuits is quite low as compared to other third order structures available in literature. The effect of nonideal behavior of OTRA and high frequency compensation scheme has also been included in the proposed theory.

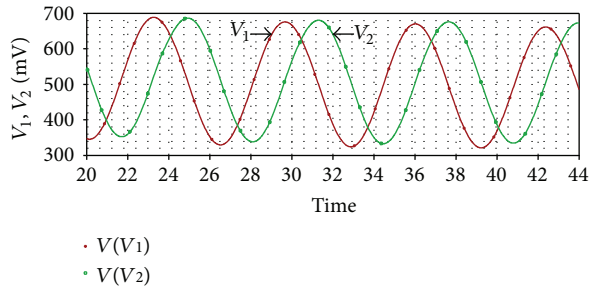


Figure 10: Transient output of proposed QO Circuit II.

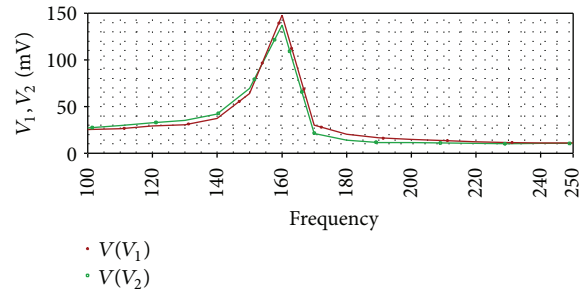


Figure 11: Frequency spectrum of output of QO Circuit II.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

References

[1] J.-W. Horng, C.-L. Hou, C.-M. Chang, W.-Y. Chung, H.-W. Tang, and Y.-H. Wen, "Quadrature oscillators using CCIIs," *International Journal of Electronics*, vol. 92, no. 1, pp. 21–31, 2005.

[2] J.-W. Horng, C.-L. Hou, C.-M. Chang, H.-P. Chou, C.-T. Lin, and Y.-H. Wen, "Quadrature oscillators with grounded capacitors and resistors using FDCCIIs," *ETRI Journal*, vol. 28, no. 4, pp. 486–493, 2006.

[3] P. Prommee and K. Dejhan, "An integrable electronic-controlled quadrature sinusoidal oscillator using CMOS operational transconductance amplifier," *International Journal of Electronics*, vol. 89, no. 5, pp. 365–379, 2002.

[4] J.-W. Horng, "Current-mode third-order quadrature oscillator using CDTAs," *Active and Passive Electronic Components*, vol. 2009, Article ID 789171, 5 pages, 2009.

[5] J.-W. Horng, "Quadrature oscillators using operational amplifiers," *Active and Passive Electronic Components*, vol. 2011, Article ID 320367, 2011.

[6] J.-W. Horng, "Current/voltage-mode third order quadrature oscillator employing two multiple outputs CCIIs and grounded capacitors," *Indian Journal of Pure and Applied Physics*, vol. 49, no. 7, pp. 494–498, 2011.

[7] S. Maheshwari and I. A. Khan, "Current controlled third order quadrature oscillator," *IEE Proceedings—Circuits Devices and Systems*, vol. 152, pp. 605–607, 2005.

[8] S. Maheshwari and I. A. Khan, "Current-mode third-order quadrature oscillator," *IET Circuits, Devices and Systems*, vol. 4, no. 3, pp. 188–195, 2010.

[9] S. Maheshwari and R. Verma, "Electronically tunable sinusoidal oscillator circuit," *Active and Passive Electronic Components*, vol. 2012, Article ID 719376, 6 pages, 2012.

[10] S. Maheshwari, "Analogue signal processing applications using a new circuit topology," *IET Circuits, Devices and Systems*, vol. 3, no. 3, pp. 106–115, 2009.

[11] J.-W. Horng, H. Lee, and J.-Y. Wu, "Electronically tunable third-order quadrature oscillator using CDTAs," *Radioengineering*, vol. 19, no. 2, pp. 326–330, 2010.

[12] R. Pandey, N. Pandey, and S. K. Paul, "MOS-C third order quadrature oscillator using OTRA," in *Proceedings of the 3rd International Conference on Computer and Communication Technology*, pp. 77–80, November 2012.

[13] S. Lawanwisut and M. Siripruchyanun, "High output-impedance current-mode third-order quadrature oscillator based on CCCCTAs," in *Proceedings of the IEEE Region 10 Conference (TENCON '09)*, pp. 1–4, November 2009.

[14] A. Kwawsibsam, B. Sreewirote, and W. Jaikla, "Third-order voltage-mode quadratrue oscillator using DDCC and OTAs," in *International Conference on Circuits, System and Simulation*, pp. 317–321, 2011.

[15] M. Kumngern and S. Junnapiya, "Current-mode third-order quadrature oscillator using minimum elements," in *Proceedings of the International Conference on Electrical Engineering and Informatics (ICEEI '11)*, pp. 1–4, July 2011.

[16] D. Duangmalai and W. Jaikla, "Realization of current-mode quadrature oscillator based on third order technique," *ACEEE International Journal on Electrical and Power Engineering*, vol. 2, pp. 46–49, 2011.

[17] K. N. Salama and A. M. Soliman, "CMOS operational transresistance amplifier for analog signal processing," *Microelectronics Journal*, vol. 30, no. 3, pp. 235–245, 1999.

[18] K. N. Salama and A. M. Soliman, "Universal filters using Operational Transresistance Amplifiers," *AEU-Archiv für Elektronik und Ubertragungstechnik*, vol. 53, no. 1, pp. 49–52, 1999.

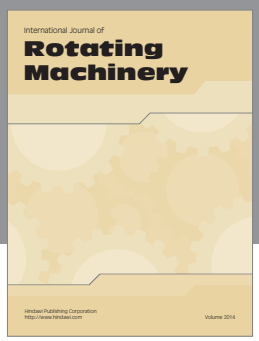
[19] S. Kilinç and U. Çam, "Operational transresistance amplifier based first-order allpass filter with an application example," in *Proceedings of the 47th Midwest Symposium on Circuits and Systems*, vol. 1, pp. 65–68, July 2004.

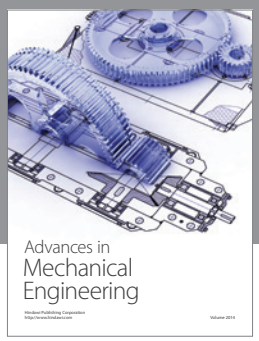
[20] S. Kilinç and U. Çam, "Cascadable allpass and notch filters employing single operational transresistance amplifier," *Computers and Electrical Engineering*, vol. 31, no. 6, pp. 391–401, 2005.

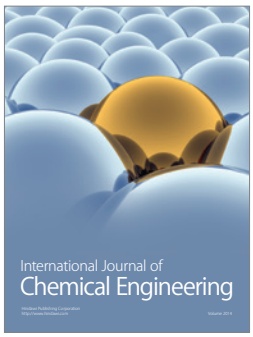
[21] C. Cakir, U. Cam, and O. Cicekoglu, "Novel allpass filter configuration employing single OTRA," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 52, no. 3, pp. 122–125, 2005.

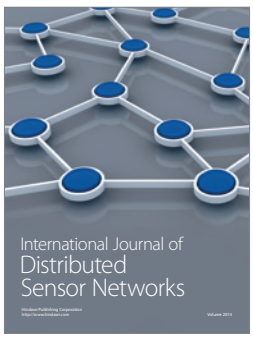
[22] H. Mostafa and A. M. Soliman, "A modified CMOS realization of the operational transresistance amplifier (OTRA)," *Frequenz*, vol. 60, no. 3-4, pp. 70–76, 2006.

[23] A. S. Sedra and K. C. Smith, *Microelectronic Circuits.*, Oxford University Press, New York, NY, USA, 2004.









Hindawi

Submit your manuscripts at
http://www.hindawi.com