CDBA based Analog Circuit Design

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by

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Certificate

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Abstract

The development in modern analog signal processing applications in the past two decades has lead to evolution from voltage mode realization to current mode analysis. In current mode, the information or signal are processed in the form of current. This shift has acquired its place in electronics circuits as better signal linearity, higher bandwidth, low voltage swing and low supply voltage requirements are the key features of CM circuits. This popularity of current-mode circuits lead to development of various current mode building blocks. Current Differencing Buffered Amplifier (CDBA) is one of them, this block processes the currents applied at its input terminals, thus due to this current processing it inherits all the advantages of the current-mode technique. Also as both current and voltage outputs are available respectively at low and high impedance nodes; this block provides further flexibility in designs. This block can be used for high frequency operation as it is free from parasitic capacitances due to internally grounded input terminals.

In this thesis elaborate discussion on the realization of CDBA block and applications such as Filters, Quadrature oscillators and Astable multivibrators based on the CDBA active block is done. Also the realizations discussed are simulated for verification of their operation. Systematic approaches to develop three new oscillator circuits, namely unconditional QOs, third order QOs and Multiphase sinusoidal oscillators are presented. These approaches are used to yield the circuits using CDBA active block. The workability of the proposed circuits is confirmed through Pspice simulations using commercially available AD844 IC's macro model which is used for the implementation of CDBA block, also third order QO is verified experimentally as well.

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List of Abbreviations

CDBA	**Current Differencing Buffered Amplifier**
FVFCS	**Flipped Voltage Follower Current Sources**
DFVF	**Differential Flipped Voltage Follower**
FVF	**Flipped Voltage Follower**
DCCCS	**Differential Current Controlled Current Source**
LVLPCR	**Low Voltage Low Power CMOS based Realization**
QOs	**Quadrature Oscillators**
CO	**Condition of Oscillation**
FO	**Frequency of Oscillation**
LPF	**Low pass filter**
VM	**Voltage mode**
CM	**Current mode**
HPF	**High pass filter**
BPF	**Band pass filter**
THD	**Total harmonic distortion**
MSO	**multi phase sinusoidal oscillator**

Chapter 1: Introduction

1.1.Motivation

Digital signal processing is a rapidly developing field and it advanced further, as growth in IC technology granted compact and efficient implementation of its algorithms on silicon chips. Even though various forms of signal processing have shifted to digital domain, but still analog circuits are essentially required in plenty of complex and high performance modern systems. It is a known fact that naturally occurring signals are analog. Therefore, analog circuits form a bridge between the digital domain and the actual world. Analog VLSI can deal with nearly all real world issues and has extended its range for new information processing applications in numerous fields like integrated sensors, image processing, speech recognition, hand writing recognition etc.

This has led to an increased interest in the evolution process of active elements which are used for analog signal processing. The adaptation involved in their development included modification in basic circuits like Voltage Feedback Amplifier (VFA), Current Feedback Amplifier (CFA), Operational Trans-conductance Amplifier (OTA), and mainly current conveyors (CC). Another direction of evolution is by inserting an entirely new element in the circuit which expands the original VFA, CFA, OTA, CC etc. The key motivation for performing such modifications is an attempt to raise the application prospective of active blocks. Concurrently, the internal structure of the element must be simple while consuming less power and operating at higher speed.

The evolution process eventually hit a road block as the designers were given a choice of choosing between the current mode (CM) or voltage mode (VM) active blocks, but advancement in IC technology in past two decades motivated VLSI designers to exploit the potential of current mode techniques. The CM provides various advantages over VM. The pros of using CM approach include high slew rates, better linearity, enhanced accuracy, broader bandwidth and reduced power consumption. The traditional analog circuits are VM circuits wherein the voltage levels at various nodes including the input and the output nodes determines the circuit parameters and performance, a simple example of such circuit is an operational amplifier. All these circuits cannot change its output voltage instantly in accordance with the abrupt transition in the input voltage due to stray and other unavoidable capacitances. Also the bandwidth of op amp based circuits is usually small due to finite unity gain bandwidth product. They require higher supply voltages to achieve better SNR and also slew rate depends on the time constants related

with the circuit. Therefore, VM circuits are not appropriate for their use at high frequency applications. In CM circuits the input/output signals are primarily currents and the entire circuit analysis is done in currents. Here, the voltage levels are not utilized for obtaining the circuit performance. CM circuits have low impedance internal nodes, where also voltage swings are small. The bandwidths of these circuits are higher and the low impedance transforms makes them low time constant circuits. Higher slew rate can be achieved if the rate of output change is large. CM circuits have simple architecture and their operations do not depend on the supply voltages.

The benefits of CM has led to evolution of many current-mode active building blocks such as Operational Transconductance Amplifiers (OTA), Current-Feedback Op-Amps (CFOA), Differential Voltage Current Conveyor (DVCC), Differential Difference Current Conveyor (DDCC), Dual X Current Conveyors (DXCCII), Current Controlled Current Conveyors (CCCII), Current Differencing Transconductance Amplifier (CDTA), Voltage Differencing Transconductance Amplifier (VDTA). A new active block called Current Differencing Buffered Amplifier (CDBA) incorporating the benefits of current mode was proposed by Acar and Ozogur in 1999. This block has gained popularity in past decades due to wide dynamic range and broad bandwidth. Also, it is suitable for high frequency operation as its internally grounded input terminals makes the circuit free from parasitic capacitances.

The growing interest in CDBA is mainly because of the flexibility and ease of implementation offered by this block. The block can be easily implemented by CMOS technology. Hardware implementation using IC AD844N can also be accomplished. Also, it offers broad range of linear and non-linear applications. These features of CDBA have captured the interest of analog designers towards it, thus motivating the designers to further explore this block to obtain satisfactory results through simulations and develop new applications using this active block.

1.2.Research objective

It can be concluded from the section 1.1 that there is a trending shift in the analog design industry towards CM circuits and that CDBA block offer certain advantages over other CM active elements. Hence this thesis proposes new configurations to existing applications using CDBA block capturing the essence of the discussion done in section 1.1. The objectives of the research are listed below,

- To study and analyse the different methods of realizing CDBA active block.

- Comparative analysis of CDBA realizations in terms of various performance parameters.
- To study and analyse various applications designed by using CDBA
- To propose new circuit configurations.
- Verification of proposed circuits by functional simulations and/or by experimentation.

Initially the literature related to CDBA and applications proposed using CDBA is reviewed which suggested the areas which could be explored to propose new designs. Signal generators such as oscillators (need to satisfy Barkhausen criteria **[1]** in order to oscillate) and multivibrators are an important class of circuits and find wide application in electronic system design. It was observed that though, a large number of sinusoidal oscillators are available in literature, yet there is scope of further investigations. As a result three new oscillator configurations are proposed. The first one is a new quadrature oscillator (QO) configuration, designed using an inverting and a non inverting integrator in colsed loop. Second proposition is a third order QO with better THD performance as compared to its second order counterpart. The third structure proposed is an all pass based multiphase sinusoidal oscillator (MSO). All the proposed designs are simulated using PSPICE to test their functionality. Also third order QO is verified using hardware implementation as well.

1.3. Thesis organization

The thesis is organised in 8 chapters, where chapter 2 reviews the history and developments through the years in the block realization of CDBA and applications made out using the CDBA active block. Various realizations of CDBA are explained in detail in chapter 3 and circuits simulated to verify the operation of the CDBA block. All standard second order filter types and linear and non linear signal generators are studied and implemented using the CDBA in chapter 4 and 5 respectively. The PSPICE simulations for functional verification of these implemented configurations are also presented. Chapter 6 presents the CDBA based three new propositions and their simulation results showing conformity with the proposed theory. These include unconditional QO, third order QO and multiphase sinusoidal oscillator. The third order QO circuit is also verified experimentally, for functionality, and results obtained are put together in chapter 7. Chapter 8 summarizes the work presented in this dissertation followed by a concluing remark highligting the objective achieved through this work.

CHAPTER 2: Literature Review

In past years, there has been trending shift to current mode design due to its various advantages over voltage mode. This lead to the development of various current mode active blocks like Operational Transconductance Amplifiers (OTA), second generation Current Conveyors (CCII), Current-Feedback Op-Amps (CFOA), Differential Voltage Current Conveyor (DVCC), Differential Difference Current Conveyor (DDCC), third-generation Current Conveyor (CCIII) etc. In 1999, a new building block called CDBA was proposed by Acar and Ozogur **[2]**. The block inherits all the properties of current mode circuits and therefore is suitable for high frequency applications. CDBA has attracted many researchers to design analog signal processing circuits and therefore a wide range of applications employing CDBA have been proposed **[3,5,9-29]**.Numerous papers have been reported on CDBA in past one and a half decade. This includes various realizations of CDBA and broad range of signal processing and generation applications such as filters, oscillators, immitance simulator, multivibrator, multiplier, etc.

2.1. Reported work on CDBA realization

C. Acar and S. Ozoguz in 1999 proposed a CDBA realization using CFOA (IC AD844) **[2]**. Two AD844 IC's were used to design CDBA block and then filters were realized using it. In the same year, C. Acar and S. Ozoguz along with A. Toker, M. A. İbrahim also proposed CMOS realization of CDBA **[3]**.

After two years, Tarim and Kuntman **[4]** proposed a high performance current differencing buffered amplifier by using two second generation current conveyors (CCII) and a voltage buffer. This design was implemented in CMOS technology incorporating only MOS transistors in it.

The NPN based current differencing buffered amplifier was proposed in 2006 by Sawangarom, Tangsrirat and Surakampontom **[5]** proposed. This CDBA could operate at a minimum power supply of 2 volts. NPN based CDBA consist of two blocks, current differencing circuit and voltage follower. The current differencing circuit is obtained by using two unity gain current amplifier and the current mirror in it reflects the current to output port. This circuit had the added advantage of using only NPN transistors which help to achieve a maximum high frequency response which was earlier limited due to the use of PNP transistors.

In the same year, W.Tangsrirat, K. Klahan, K. Kaewdang and W. Surakampontorn **[6]** proposed a low voltage wide band NMOS based CDBA, which has a low resistance at

both the current-input terminals (p, n) and at the output-voltage terminal (w). It presented that NMOS based CDBA realization was superior in terms of supply voltage and frequency range. It can operate at minimum supply voltage of ±1.25 volts. This implementation of CDBA was designed by modifying low impedance current conveyor (CCII+) to make it to function as a current differencing circuit and also a voltage buffer circuit.

The existing CDBAs did not use low-voltage power supplies and had quite high input terminal resistances, high power consumption, most of them suffer from limited output voltage swing. Therefore, Cem Cakir and Oguzhan Cicekoglu **[7]** in 2008 proposed a low voltage high performance CDBA. This circuit could operate with the power supplies down to ±0.75V and it also consumed less power than its counterparts. This circuit is based on the flipped voltage follower current sources (FVFCS) which give rise to very low input resistances at the input ports. Output stage of this CDBA offers low output impedance and a moderate output swing.

Then a year later, Cem Cakir, Shahram Minaei, and Oguzhan Cicekoglu **[8]** in 2009 proposed a low voltage low power CMOS CDBA. The circuit can operate with the minimum supply voltage of ±0.6 volts. This Low voltage CDBA circuit is based on the use of current differencing circuit and voltage buffer. This circuit offers very low terminal resistance at n and p terminal and consumes much less power as compare to the other CDBA circuits available in literature.

2.2. Reported work on CDBA Applications

2.2.1. Linear Applications

2.2.1.1 Filters

A design technique to realize continuous-time current-mode filters employing CDBAs using minimum active components was proposed by Worapong Tangsrira, Nobuo Fujii and Wanlop Surakampontorna **[9]** in 2002. They also designed fifth-order Butterworth low-pass filter and a sixth-order Chebyshev band pass filter to demonstrate the functionality of the techniques.

Visawa Sawangarom, Worapong Tangsrirat and Wanlop Surakampontom in 2006 proposed NPN based CDBA and realized all pass filter using it **[5]**. Also, in 2008 they

realized Voltage mode universal biquad filter using two CDBA **[10]** and six passive components. The configuration could realize all five types of filter with the same topology.

A. U. Keskin in 2008 proposed voltage mode band pass filter employing single CDBA **[11]**. The filters were of High quality factor and used minimum number of components.

M. Koksal, S.E. Oner and M. Sagbas in 2009 proposed a new configuration of second order multi-mode multi-function filter **[12]**. The configuration utilizes one CDBA block and four to five passive components. Four modes namely, voltage mode, current mode, trans-impedance mode and trans-admittance mode were realized with same proposed topology. Also, Low pass, band pass and high pass filters were designed using the same.

Fırat Kacard and Yasin ozcelep in 2011 proposed five new configurations of voltage mode first order all pass filter using CDBA **[13]**. They used four to five passive elements while realizing the filter.

A current-mode linear transformation filter based on CDBA for realizing higher order filters was proposed by Yuh-Shyan Hwang, Zhao-Hong Huang, Jiann-Jong Chen and Wen-Ta Lee **[14]** and also third order chebychev low pass filter was demonstrated by them to verify the functionality.

Cem Cakir, Shahram Minaei and Oguzhan Cicekoglu in 2010 proposed a new CMOS realization of CDBA that operate at low voltage **[15]**. The circuit also consumed low power and offered high performance. Then they analyzed all pass and notch filter using the proposed topology to verify the performance of the new circuit. Also, ZC-CDBA performance was demonstrated on a new current mode filter topology proposed by Ersin Alaybey, Arda Güney and Hakan Kuntman in 2013 **[16]**.

2.2.1.2 Oscillators

CDBA based resistance controlled sinusoidal oscillators were first proposed in 2000 by S. O zcana, A. Tokera, C. Acara, H. Kuntmana and O. Cicekoglu **[17]**. They gave six configurations to design sinusoidal oscillator. These oscillators are suitable for VCO implementations.

Another oscillator called multiphase sinusoidal oscillator employing CDBA as an active element was proposed by Sumaytee Pisitchalermpong, Worapong Tangsrirat and Wanlop Surakampontom in 2006 **[18]**. The circuit comprises of n cascaded blocks of lossy integrators and inverters based on CDBA. N sinusoidal waves of phase difference $\frac{180^{\circ}}{n}$ are obtained at the output of such oscillator.

A Quadrature oscillator using three CCCDBAs and two grounded capacitors which is suitable for IC architecture is proposed by Winai Jaikla, Phamorn Silapan and Montree Siripruchyanun in 2007 **[19]**. Here input bias current is used to electronically control the frequency of oscillation and condition of oscillation.

CDBA based Quadrature oscillator realized using two CDBA blocks, four resistors and two grounded capacitors **[10]** is proposed in 2008 by Worapong Tangsrirat, Tattaya Pukkalanun, and Wanlop Surakampontorn. The virtually grounded resistors employed in the circuit provide controllability on frequency of oscillation and condition of oscillation independently.

In 2010, J.K. Pathak, A.K. Singh and R. Senani presented a systematic approach to realise CDBA based Quadrature Oscillator **[20]**. They proposed a general configuration designed using low pass filter and an integrator that yielded 12 different Quadrature oscillator circuits.

Abhirup Lehiri in 2011 also proposed a low frequency quadrature sinusoidal oscillator using CDBA **[21]**. His proposed circuits use reduced number of components and low frequency is obtained due to difference term in the oscillator's frequency.

Winyu Sonjoi, Worapong Tangsrirat and Wanlop Surakampontorn proposed another electronically tunable Quadrature oscillator made up of two CCCDBA and two grounded capacitors in 2009 **[22]**. This configuration provides two sinusoidal output having phase difference of 90°. Later in 2013, the performance of this oscillator was improved by using high performance CCCDBA by **[23]**.

Ali Umit Keskin **[24]** proposed a design of minimum Component Oscillators (MCO) using Negative Impedance (NIC) approach based on CDBA. The NIC based oscillator synthesis procedure consists of two steps: a) A grounded NIC circuit of a given type of active element is found, b) a shunt branch to NIC is connected so that, any real terms are removed in complex plane and a symmetric pole pair is placed on the imaginary axis.

2.2.1.3 Immitance Simulator

Ali Ümit Keskin and Erhan Hancioglu in 2005 proposed synthetic floating inductance circuits based on CDBA **[25]**. They presented two different configurations which uses grounded capacitor. The circuits were fully integrable and also electronically tunable.

Worapong Tangsrirat and Wanlop Surakampontorn in 2006 **[26]** proposed an electronically tunable lossless floating inductance simulator. The floating inductance circuit uses only three current controlled CDBAs (CC-CDBA) and a grounded capacitor. Its equivalent inductance can linearly be tuned by means of the external bias current of the CC-CDBA. Without the employment of any external passive resistors, the proposed inductance simulation circuit is attractive for integrated circuit (IC) implementation.

2.2.1.4 Inverse filter

CDBA based universal inverse filter configuration **[27]** was proposed by Rajeshwari Pandey, Neeta Pandey, Tushar Negi and Vivek Garg in 2013. The topology was use to design all five inverse filters namely inverse low pass, inverse high pass, inverse band pass, inverse band reject and inverse all pass.

2.2.1.5 Nth order current transfer function realization

Cevdet Acar and Herman Sedef in 2003 proposed CDBA based two new configurations to realize high order current mode transfer function **[28]**. One configuration was made of one CDBA block and four passive components and the other was designed with two CDBA blocks and four passive components. These topologies had reduced number of active elements in their realization.

2.2.2. Non-linear Applications

2.2.2.1 Multivibrators

Rajeshwari Pandey, Neeta Pandey, Sajal K. Paul, Kashish Anand, and Kranti Ghosh Gautam **[29]** proposed three voltage mode astable multivibrator circuits using single CDBA. One of the circuit outputs the square wave of fixed duty cycle and other two offer duty cycle controllability. One of the controllable square wave generators employ resistance to control the duty cycle, whereas the other makes use of voltage source to electronically control it.

2.2.2.2 Multiplier

A new fully integrable fourth quadrant analog multiplier based on CDBA **[30]** was proposed by Ali Umit Keskin in 2003. The circuit gave good performance and featured reduce number of component and ease of implementation.

In 2007, Montree Siripruchyanun **[31]** designed an analog multiplier and divider using CCCDBA block. The circuits need only two CCCDBA for its construction and no passive element. The circuit also behaves as gain-controllable current amplifier. In same year, multiplier/divider circuit was designed using high performance Bi-CMOS CCCDBA **[32]**. The circuit can be used for analog signal processing based applications.

CHAPTER 3: CDBA Active building block

3.1.CDBA Terminal Characteristics

The symbol for the CDBA active block circuit is shown in figure 3.1. Two fundamental building blocks namely current substractor circuit and the voltage follower circuit are combined together to form the CDBA block. The equivalent circuit to the CDBA consists of dependent current and voltage sources and is shown in figure 3.2.

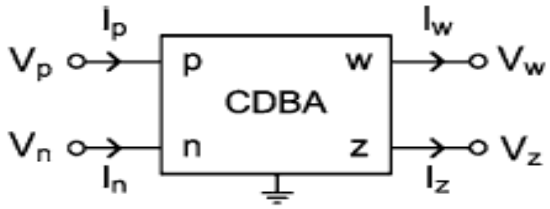

Figure 3.1 Symbol of CDBA

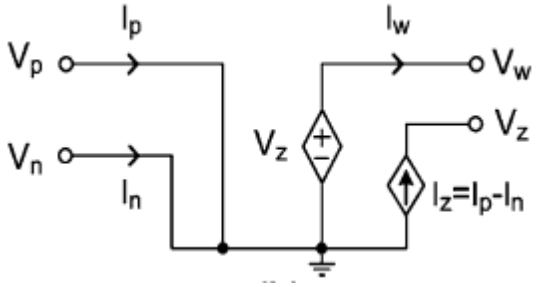

Figure 3.2 Equivalent circuit of CDBA **[15]**

The characteristics of the CDBA block can be modelled as:

$$\begin{bmatrix} i_z \\ V_w \\ V_p \\ V_n \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 & -1 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_z \\ i_w \\ i_p \\ i_n \end{bmatrix} \quad (3.1)$$

And for practical CDBA equation become

$$I_Z = \alpha_p I_P - \alpha_n I_n, V_W = \beta_v V_Z, V_P = V_n = 0 \quad (3.2\text{-}3.4)$$

Where current gains are denoted by α_p and α_n, and voltage gain by β_v , which in the ideal case should be equal to unity.

In practice, they are expressed as

$$\alpha_p = 1 - \varepsilon_p, \alpha_n = 1 - \varepsilon_n, \beta_v = 1 - \varepsilon_v \quad (3.5\text{-}3.7)$$

With

$$|\varepsilon_p| \ll 1, |\varepsilon_n| \ll 1, |\varepsilon_v| \ll 1$$

Here current-tracking errors are denoted by ε_p and ε_n and voltage-tracking error is denoted by ε_v .

If we observe the equivalent circuit and the above describing equations, we find that the difference of the currents through the p and n terminals is seen at the z-terminal of the circuit that's why we name z as the current output terminal, which has ideally infinite impedance. Also the p-terminal and n-terminal are respectively labelled as the non-inverting and inverting input terminals of the block. These p and n terminals which act as inputs to the block are grounded thereby ideally having zero input impedances at these terminals internally. The w-terminal is termed as voltage output, as the voltage at the w-terminal follows that at the z-terminal using the voltage follower circuit between the two terminals. As w-terminal is used as a voltage output hence it should ideally have zero impedance.

3.2.Realizations of CDBA

3.2.1. IC AD844 based Realization

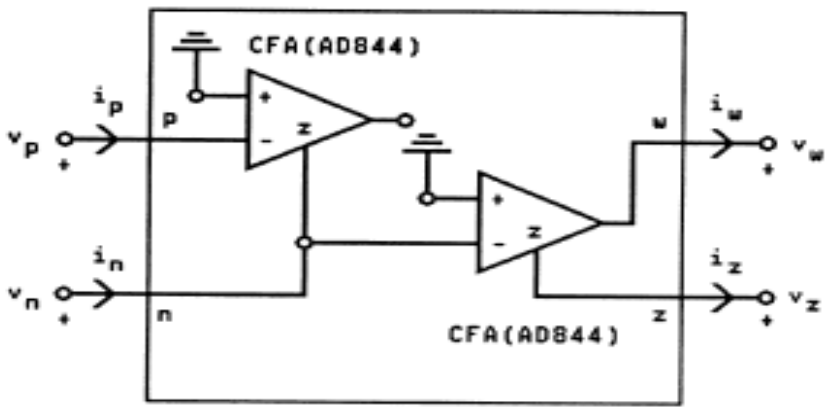

Figure 3.3 Implementation of CDBA using CFOA (AD844 IC) **[2]**

The above figure 3.3 presents the implementation of CDBA using two AD844 CFOA IC's (see Appendix A). The current at the compensation node TZ of the CFOA is ideally equal to the difference of the current applied to the noninverting and inverting terminals of the CFOA. Hence the current at the compensation node for first IC is given by:

$$i_{z1} = -i_p \tag{3.8}$$

thereby giving a resultant current of i_{n2} at the inverting terminal of second IC.

$$i_{n2} = i_n + i_{z1} \text{ Or } i_{n2} = i_n - i_p \tag{3.9}$$

Therefore the current at the Z-terminal of second IC is given by:

$$i_{z2} = i_p - i_n \tag{3.10}$$

Which is the required current at the z-terminal of CDBA, also the voltage at the w-terminal of the CFOA follows the voltage at the z-terminal using a voltage follower circuit attached between the two terminals as can be seen in the CMOS implementation of the CFOA. The voltage at the z-terminal is formed by i_{z2} current and the impedance at the z-terminal.

3.2.2. NPN Transistor based Realization

CDBA active block has being implemented by various ways and has being proposed in different literatures, but every implementation has some of its own limitations. There are certain limitations due to the use of PNP transistors in the implementation as they limit the high frequency operation of the circuit and this leads to a conclusion that CDBA should be designed in such a way that signals only pass through NPN transistors. Also due to the advances in large scale integration and increased use of complicated circuit systems and portable consumer electronics equipments, there has being a gradual increase in the need of a low voltage low power technique.

Here, a simple NPN based CDBA is presented which can operate even at a DC supply voltage of as low as 2 volts this satisfies the low power consumption need, also the signal has only NPN transistors in its signal path which helps to achieve a maximum high frequency response which was earlier limited due to the use of PNP transistors

3.2.2.1. Block Architecture

As shown in figure 3.4, the NPN based CDBA consists of two sub-circuits namely the current differencing circuits and a buffer voltage amplifier which are respectively shown in figure 3.6 and figure 3.7.

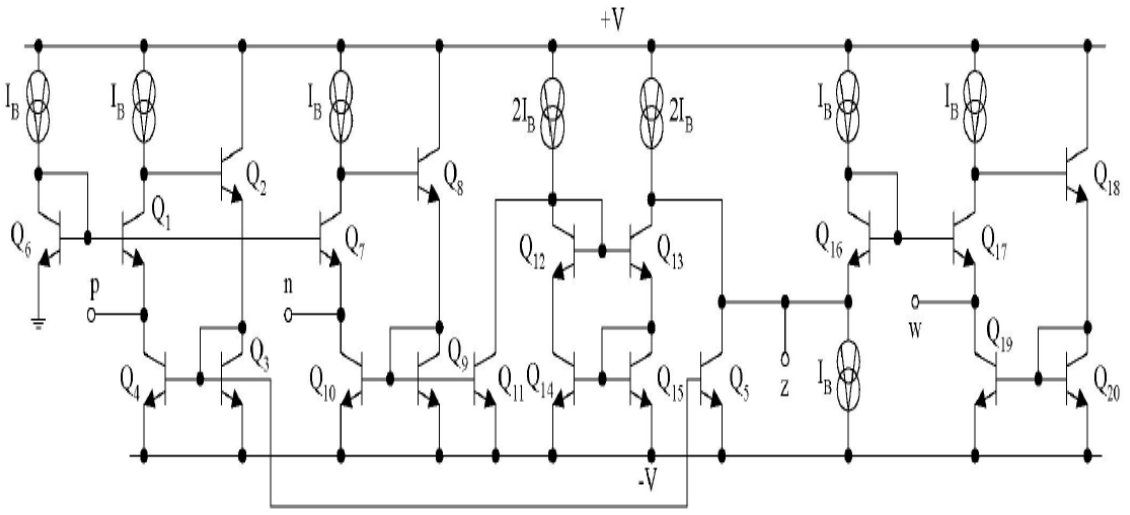

Figure 3.4 CDBA circuit using only NPN transistors **[5]**

We find from the circuit that when we traverse the path between the positive and negative supply voltages, the path has only two transistors and one biased current source. Therefore we can operate this circuit at a low supply voltage compared to other implementations with a minimum supply voltage of ($2\ V_{be} + V_{cesat}$) = 2 V (or +1 V to -1 V), Hence proving the fact that this circuit is useful for low power operations.

3.2.2.2. Circuit Description

3.2.2.2.1. Current Differencing Circuit

Current differencing circuit is obtained by combining two unity gain current amplifiers. Now if we consider figure 3.5 which depicts the circuit diagram of the unity gain current amplifier we find that Q1 through Q4 transistors form a feedback loop. Let us assume that the emitter current through the Q1 transistor is i_e, then the emitter current through the Q2 transistors becomes equal to $\beta_2 i_e$ which is also the emitter current for the Q3 transistor. Q3-Q4 transistors together form a current mirror and hence the current $\beta_2 i_e$ is reflected to the collector of Q4 transistor. Therefore following relation can be obtained:

$$i_{in} = i_e + \beta_2 i_e \tag{3.11}$$

or

$$i_e = \frac{i_{in}}{\beta_2 + 1} \tag{3.12}$$

Where,

I_{in} - the input signal current

β_2 - the current gain of transistor Q2

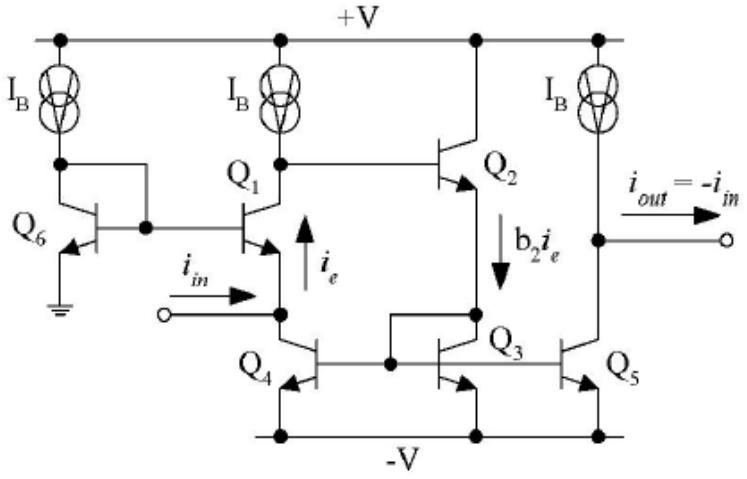

Figure 3.5 Unity gain current amplifier **[5]**

For the circuit output current i_{out} can be given by:

$$i_{out} = -\beta_2 i_e = -\frac{\beta_2}{\beta_2+1} i_{in} \quad (3.13)$$

Generally the current gain β_2 of the circuit is in several hundreds and is high enough to obtain the ratio (β_2/ β_2+1) nearly equal to 1; hence the output current of the circuit can be found to be:

$$i_{out} = -i_{in} \quad (3.14)$$

Due to the negative feedback used Between the Q1 through Q4 transistors, the value of the input resistance r_{in} of the unity gain circuit is very low and is given by the following expression below:

$$r_{in} = \frac{r_{e1}}{\beta_2} \quad (3.15)$$

Where,

$r_{e1} = V_T / I_B$ - the small signal emitter resistance

V_T - the thermal voltage.

The two groups of transistors namely Q1-Q5 and Q7-Q11 form two unity gain current amplifiers which combine together to form the current differencing circuit as shown in figure 3.6.transistors Q1 through Q5 reflect current $-i_n$ to the output port and second unity gain current amplifier Q7 through Q11 along with current mirror Q12-Q15 reflects i_p to the output port, hence the relation obtained for the output port of the circuit is:

$$i_{out} = i_p - i_n \quad (3.16)$$

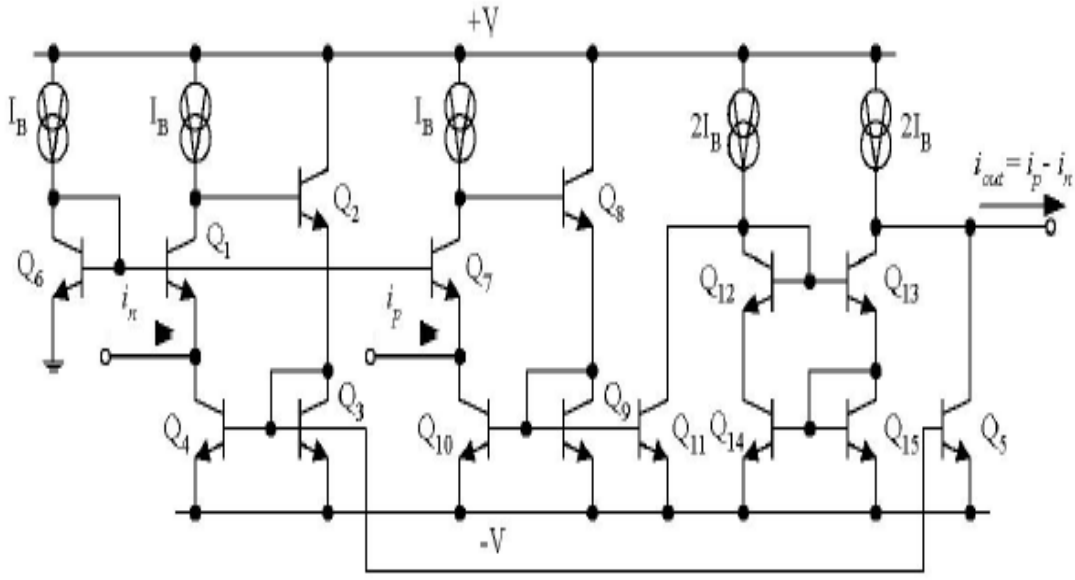

Figure 3.6 Current differencing circuit **[5]**

3.2.2.2.2. Buffered Voltage Amplifier

The voltage at terminal W(V_w) is forced to be equal to the voltage at terminal Z(V_z) with the help of transistors Q16 through Q20 which together form the buffer voltage amplifier as shown in figure 3.7, i.e. $V_w = V_z$.

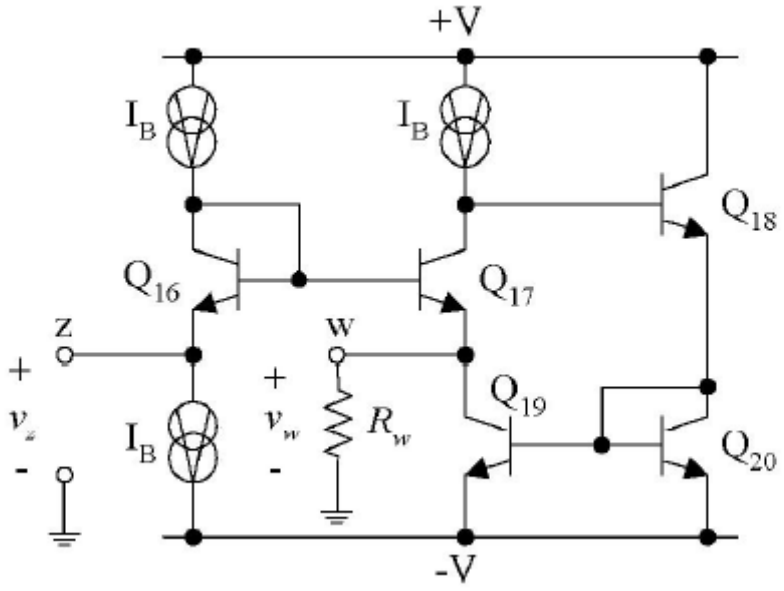

Figure 3.7 Buffer Voltage amplifier **[5]**

3.2.3. CMOS based Realization

The DCCCS block which acts the current differencing circuit, followed by the voltage follower **[33]** block combine together to form the CMOS implementation of the CDBA active block as depicted in figure 3.8.

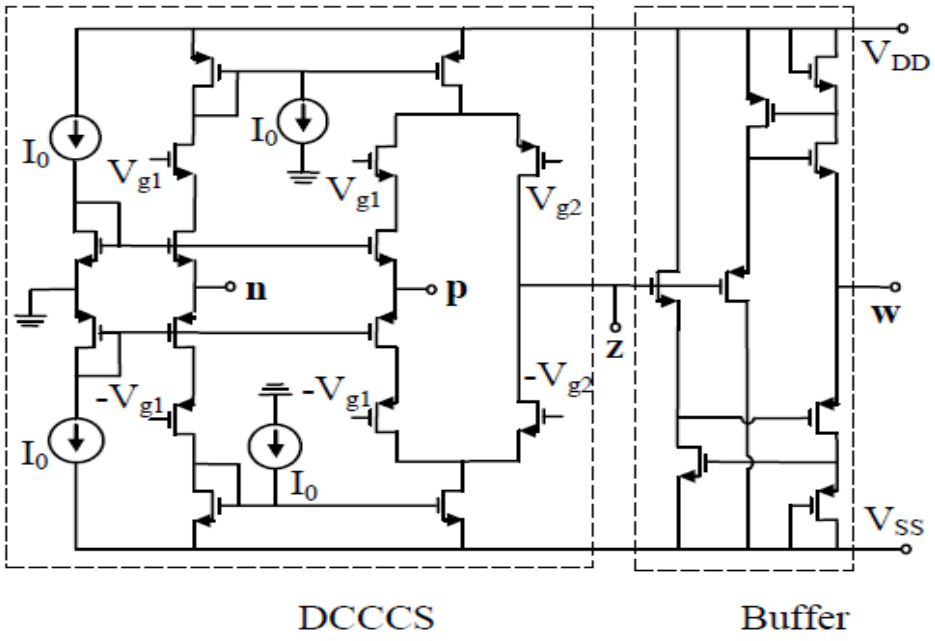

Figure 3.8 CMOS implementation of CDBA **[3]**

The CCII configuration implemented by Bruun **[34]** is slightly modified to reach to the required DCCCS circuit which is used in current CDBA block.

3.2.4. Low Voltage Low Power CMOS based CDBA (LVLP CDBA)

In the recent scenario, what we observe is a shift in the interest of researchers to low voltage circuit designs due to the advent of mobile communication systems and portable electronics and thus efforts are made to decrease the supply voltage of the circuit designs and hence minimize the power consumption. These low power capabilities are missing in the previously discussed implementations of CDBA.

Also in CMOS based CDBA, the terminal resistances are of the order of hundreds (high) of ohms and their transfer ratios for current and voltage are smaller than one. Hence, the main aim of discussing this implementation of CDBA based on the FVF technique is to overcome the disadvantages mentioned above.

3.2.4.1. Block Architecture

The low power low voltage CDBA circuit implementation can be basically divided into two blocks i.e. the current differencing circuit block and the voltage buffer circuit block, where first block replicates the difference of the current at the P and N terminal at Z terminal and second block acts as a buffer between the Z and W terminals. The complete schematic of the block can be seen in figure 3.9, where M1-M8 transistors make up the current differencing block and M9-M14 make up the voltage buffer block.

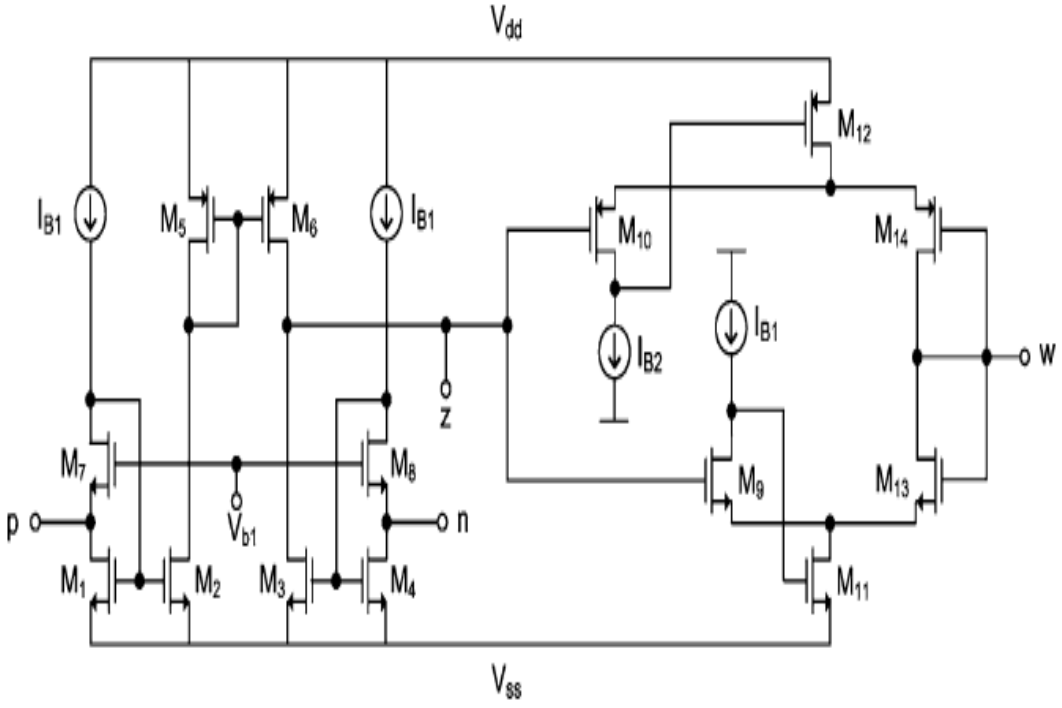

Figure 3.9 Low Power CMOS implementation **[15]**

3.2.4.2. Circuit Description

The resistances at the input terminals of the implemented CDBA block can be made very low by using FVFCS, hence the current subtraction circuit is so implemented thereby removing one of the disadvantage of other implementations.

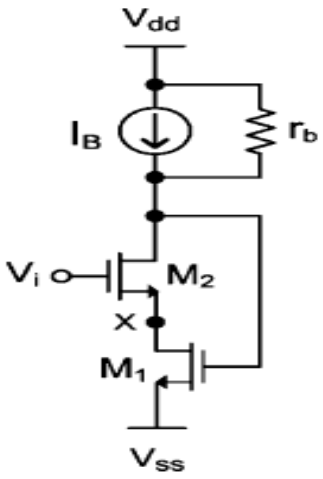

Figure 3.10 Flipped voltage follower current source (FVFCS) **[15]**

The resistance at the input terminal of the FVFCS shown in figure 3.10, when seen at the node X can be found to be;

$$R \cong \frac{\frac{1}{g_{m2}}\left(1+\frac{r_b}{r_{02}}\right)//r_{01}}{g_{m1}(r_b//g_{m2}r_{01}r_{02})} \quad (3.17)$$

Where,

r_b - output resistance of the current source

r_o - output resistance's of the transistors

g_m - trans conductance's of the transistors

For a simple current source with $r_b = r_{o2}$, the node X resistance can be found to be;

$$R \cong \frac{2}{g_{m1}g_{m2}r_{02}} \quad (3.18)$$

The current subtraction circuit which consists of the M1 to M8 transistors is illustrated in figure 3.11. The circuit can basically be understood as comprising of three current mirrors respectively constructed out of M1-M2, M3-M4 and M5-M6 transistors. Due to current mirror between M1-M2 the current flowing through M2 is $I_{B1} + i_p$ and $I_{B1} + i_n$ flows through M3 due to current mirror between M3-M4. Also the current mirror between M5-M6 leads to a current $I_{B1} + i_p$ flowing through M6, thereby replicating the difference of the currents at the P and N terminals of the CDBA to the Z terminal.

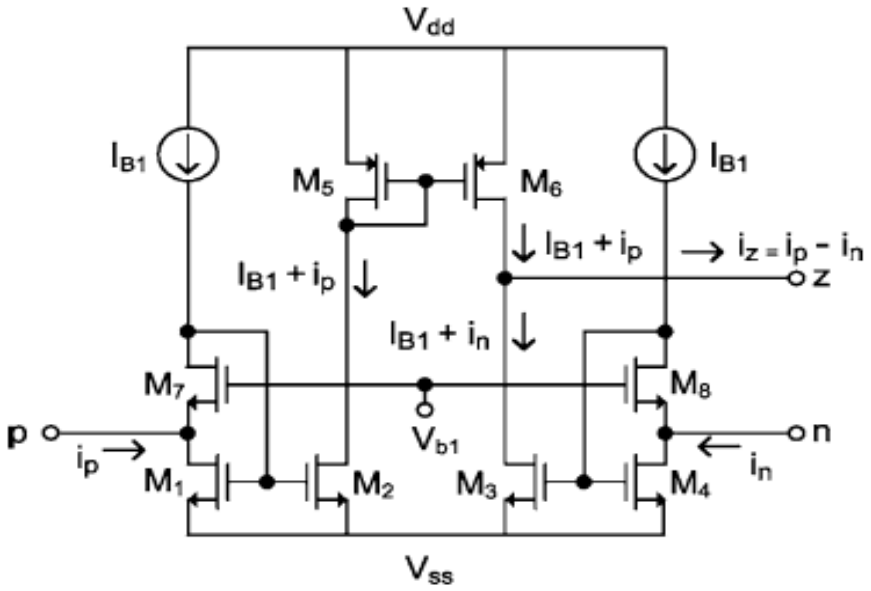

Figure 3.11 Current subtractor circuit **[15]**

Hence, terminal-z is labelled as current output. The current of the terminal-z can be expressed as follows:

$$i_z = I_{B1} + i_p - (I_{B1} + i_n) = i_p - i_n \tag{3.19}$$

For the current implementation of CDBA, the output stage is based on DFVF. The circuit for DFVF is shown in figure 3.12, where for large currents through transistor M3 the voltage at node Y remains approximately constant and also the impedance of this node is very low.

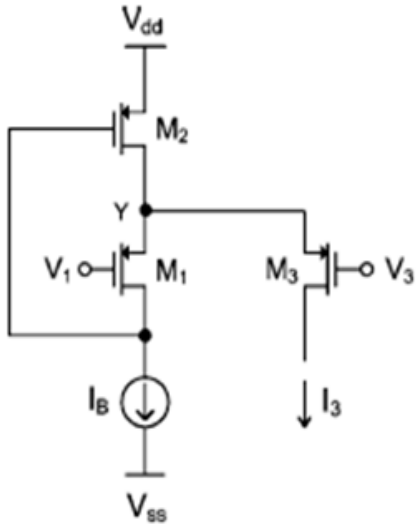

Figure 3.12 Differential flipped voltage follower (DFVF) **[15]**

This condition of constant voltage and very low impedance can be achieved if the transistors M1 and M3 are assumed to be of same sizes and the quiescent condition of

V1=V3 is observed. DFVF has another important characteristic i.e. it can operate even for very low supply voltages. The supply voltage can be reduced up to a minimum level for satisfactory performance of the circuit given by,

$$V_{dd}(min) = V_{Tp} + 2\,V_{ds,sat} \qquad (3.20)$$

The output stage circuit is a class AB voltage buffer, where M10, M12 and M9, M11 respectively form two complementary DFVF cells with current sources I_{B1} and I_{B2} as can be seen in figure 3.9. This circuit offers moderate output swing and low output impedance.

3.3. Simulation Results

3.3.1. IC AD844 based Realization

The proposed circuit is supplied by the voltages of ±5 V. For the simulations, the PSPICE model file of AD844 IC (see Appendix A) supplied by Analog Devices is used.

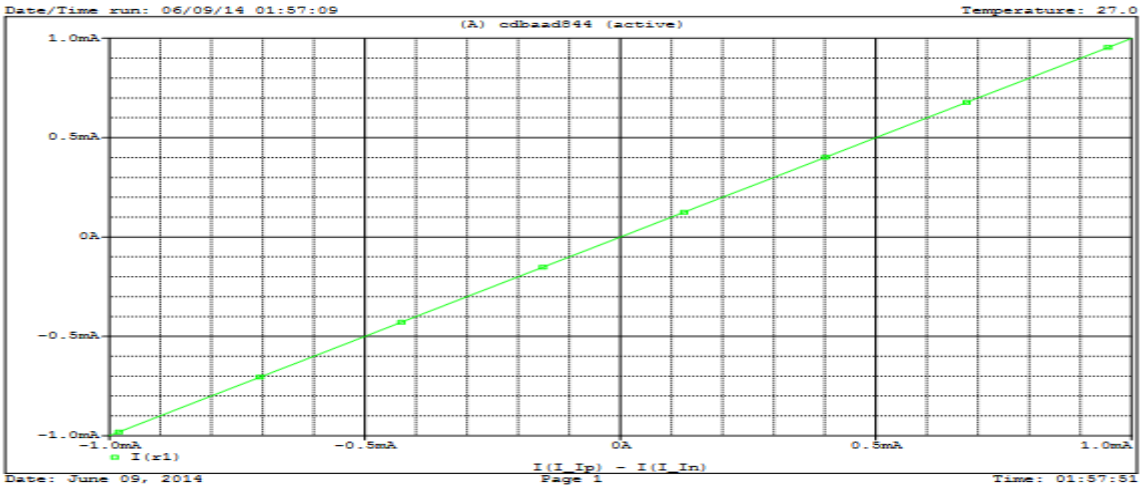

Figure 3.13 Current transfer characteristics I_z VS $I_p - I_n$ (AD844)

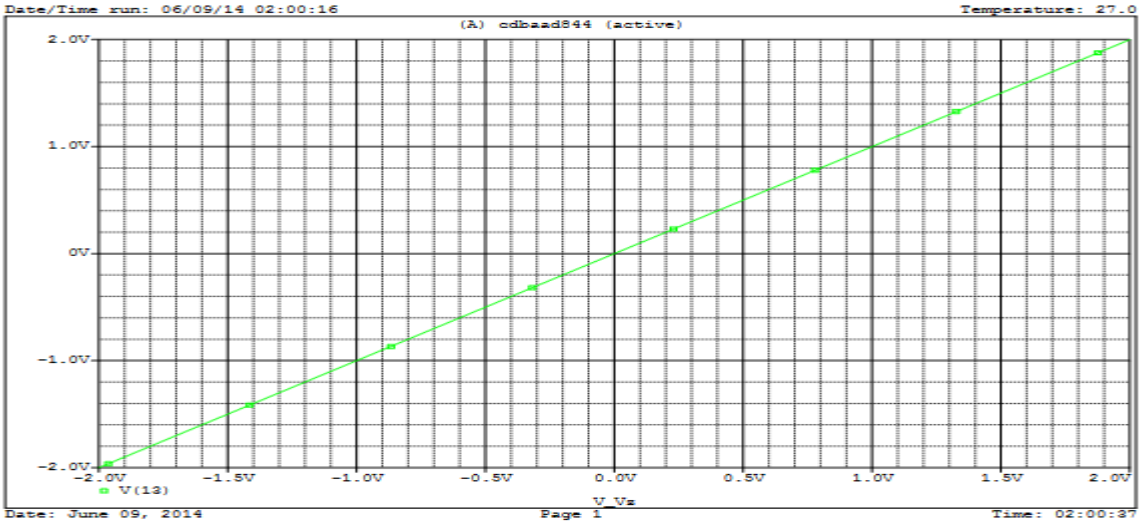

Figure 3.14 Voltage transfer characteristics V_w VS V_Z (AD844)

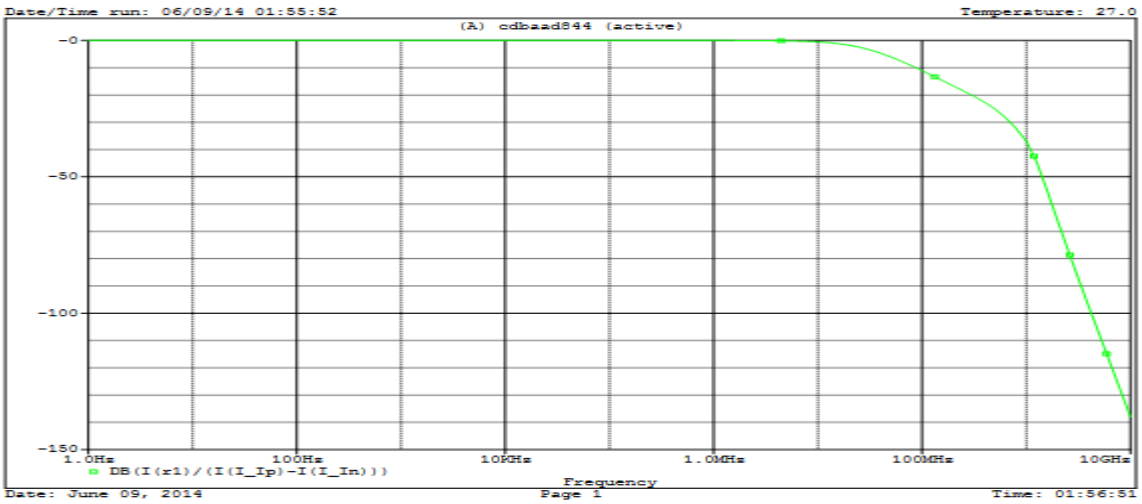

Figure 3.15 Frequency response of the current transfer ratio (AD844)

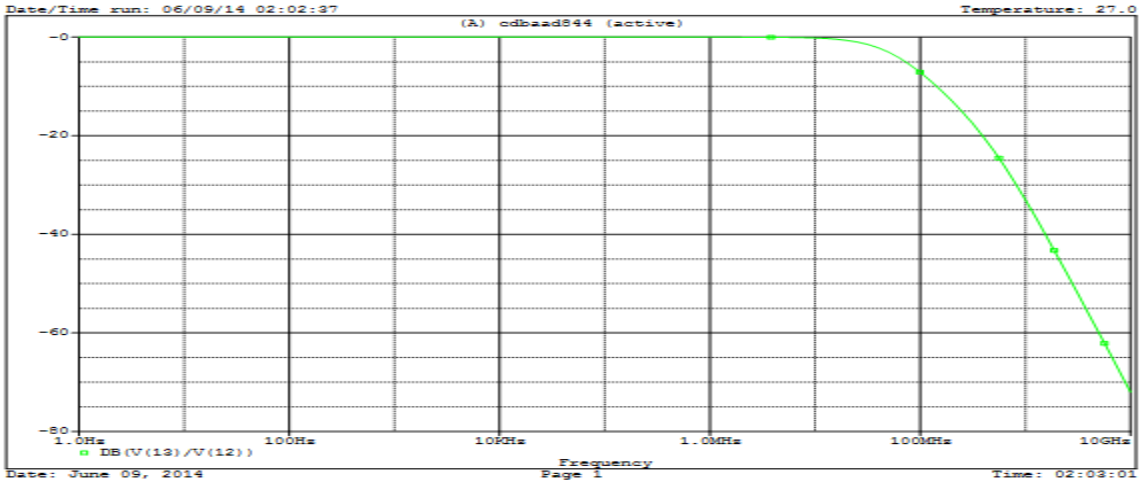

Figure 3.16 Frequency response of the voltage transfer ratio (AD844)

The DC current and voltage transfer characteristics for the current realization are shown in figure 3.13 and 3.14 respectively. It can be seen that these characteristics are linear for a large range. The current and voltage follow the given input current and voltages for as high as 1mA and 2V respectively and hence are found to be highly linear.

3.3.2. The LVLP CDBA

The supply voltage and the technology parameters used for the CDBA realization and its simulation are ±0.8 V and TSMC 0.18µm respectively. The bias currents of 56 µA and 84 µA are chosen respectively for I_{B1} and I_{B2} and the aspect ratios of the transistors used are reported in Table 3.1.

Transistor	W/L (µm/ µm)
M1,M2,M3,M4	3.6/1.8
M5,M6	180/1.8
M7,M8	180/1.8

M9	45/0.36
M10	240/0.36
M11	72/0.36
M12	240/0.36
M13	72/0.36
M14	240/0.36

Table 3.1 MOS Transistor dimensions

For the current CDBA realization the DC current transfer characteristics are displayed in figure 3.17. For the entire dynamic range at I_{B1} = 56µA the CDBA can be seen to be highly linear.

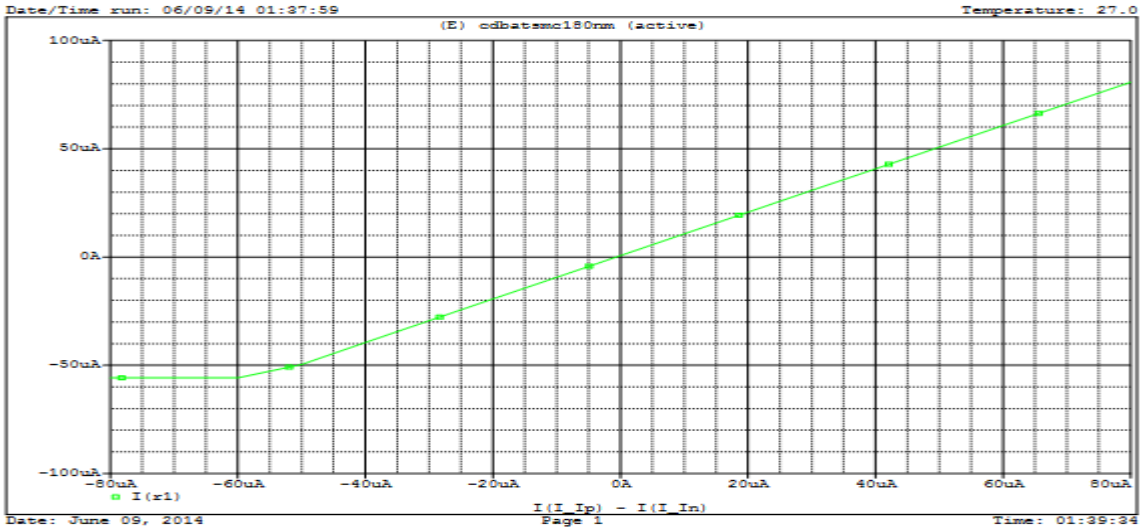

Figure 3.17 Current transfer characteristics I_z VS $I_p - I_n$ (LVLP CDBA)

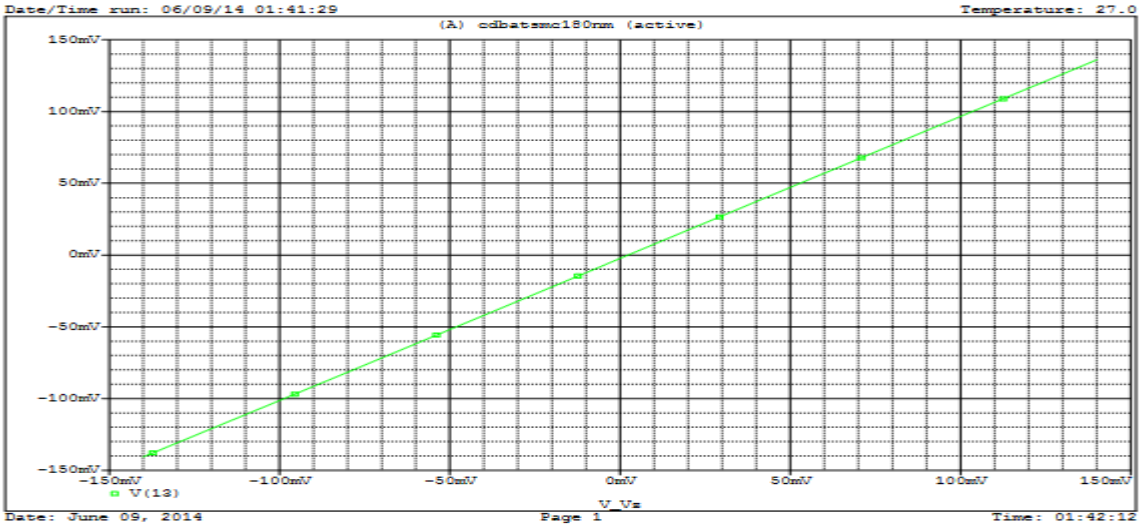

Figure 3.18 Voltage transfer characteristics V_w VS V_Z (LVLP CDBA)

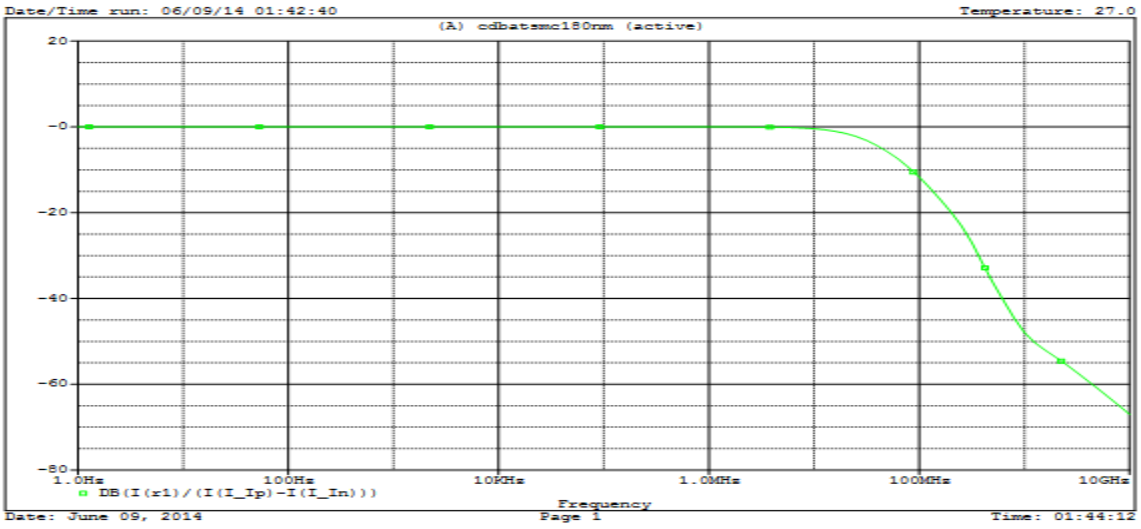

Figure 3.19 Frequency response of the current transfer ratio (LVLP CDBA)

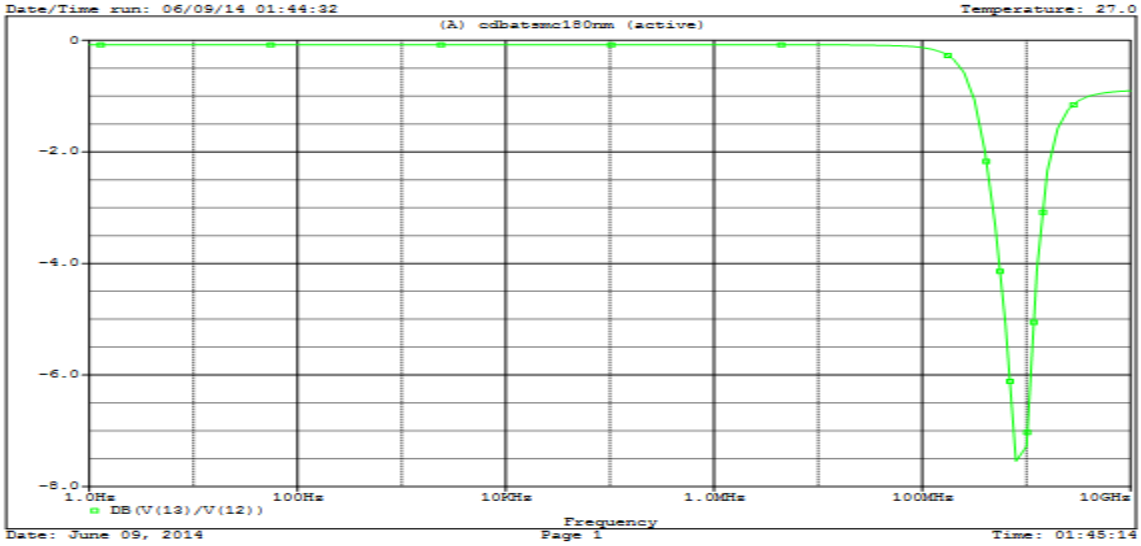

Figure 3.20 Frequency response of the voltage transfer ratio (LVLP CDBA)

The output voltage, V_w which is proportional to V_z is shown by the DC voltage transfer characteristic, given in figure 3.18. It can be seen from the simulation result of figure 3.18 that the voltage transfer error goes on increasing as the values of V_z starts to go beyond the range of ±100 mV.

The AC transfer characteristics of the currently realized CDBA are shown in figure 3.19 and 3.20, where figure 3.19 and 3.20 respectively show the frequency response for the current and voltage transfer characteristics.

3.3.3. Comparison

Various parameters of both the simulated realizations of the CDBA are shown in Table 3.2. It can be clearly seen from table 3.2 that in AD844 based realization the voltage and

current follow the required values more closely but LVLP CDBA has better voltage and current transfer bandwidths and hence can be used for higher frequency range.

Parameter	**AD844 Realization**	**LVLP CDBA Realization**
Supply voltage (V)	±5	±0.8
Current transfer ratio, $\alpha = {I_Z}/{(I_P - I_n)}$	0.9996	0.9861
Current transfer BW (MHz)	28.81	30.47
Voltage transfer ratio, $\beta = {V_w}/{V_z}$	0.9998	0.9310
Voltage transfer BW (MHz)	49	475
Power Dissipation (mW)	999.89	98.818

Table 3.2 Performance of the CDBA realizations

CHAPTER 4: Filter Realizations

4.1 Introduction

Filters are the electrical networks that process signal to modify its amplitude and/or phase characteristics in a frequency dependent manner. A filter never adds a new frequency neither it alters the component frequency of the input signal, it only varies the amplitude along with phase characteristics of the various frequency component present in the signal. Filters are often used in electronic systems to separate signals i.e. passing those of interest in certain frequency range and blocking the undesirable ones. The gain of such filters depends on signal frequency. Consider an example where the input signal comprises of desirable frequency F_1 along with an undesirable one F_2. A filter having a very low gain at F_2 and high gain at F_1 will attenuate the frequency F_2 and only useful frequency remains when the input signal is passed through it.

Analysis of filters in done in frequency domain, therefore to demonstrate its characteristics gain vs. frequency and phase vs. frequency curves are commonly used. Mathematically, a filter's frequency domain behaviour is described with the term called Transfer Function which is defined as the ratio of the Laplace transform of the output signal to the input signal fed to the filter **[35]**. Therefore, the voltage transfer function is given by,

$$H(s) = \frac{V_{OUT}(s)}{V_{IN}(s)} \tag{4.1}$$

Where $V_{OUT}(s)$ and $V_{IN}(s)$ are the output and input signal voltages respectively in laplace domain.

The magnitude of the transfer function as a function of frequency is an important analysis as it shows the variation on the amplitudes of sinusoidal signals at different frequencies due to the presence of filter. The magnitude versus frequency of a transfer function is known as the amplitude response or frequency response. Also, the amount of phase shift observed in sinusoidal signals as a function of frequency is called its phase response. Since a variation in signal's phase also corresponds to a variation in time therefore the phase characteristics of a filter turn out to be essential while dealing with complex signals where the time relationships among the signal components at different frequencies are critical. The effect of filter on the magnitude and phase of the input signal can be found by replacing s with jω in the transfer function. The magnitude is obtained by taking its absolute value i.e.

$$\left|H(\mathrm{j}\omega) = \frac{V_{OUT}(\mathrm{j}\omega)}{V_{IN}(\mathrm{j}\omega)}\right| \tag{4.2}$$

And the phase is obtained as:

$$\arg H(\mathrm{j}\omega) = \arg \frac{V_{OUT}(\mathrm{j}\omega)}{V_{IN}(\mathrm{j}\omega)} \tag{4.3}$$

An ideal filter has its amplitude response equal to unity for the desirable range of frequencies (called the pass band) and zero for any other frequency range (called the stop band). The frequency at which the transition from passband to stopband takes place is known as the cutoff frequency F_c.

The two important parameters for consideration while designing filters are cut-off frequency of the filter, Fc defined as 3 dB down frequency response from the pass band and the quality factor of the filter, Q. The Q is also sometimes given as α where:

$$\alpha = \frac{1}{\mathrm{Q}} \tag{4.4}$$

The highest power of the variable s in the transfer function of the filter is known as its order. It defines the steepness of the filter. It is also determine by the number of poles in the transfer function. A pole is a root of the denominator and a zero is a root of the numerator of the transfer function. The order of the filter is usually equals the total number of capacitors and inductors in the circuit. The Higher-order filters are therefore more costly to build as they are complicated and require more number of components. But increasing the order the filter enhances its signal discriminating power at different frequencies.

4.2 CDBA based Filter Topologies

The ancient forms of electronic filter circuits designed using combinations of Resistor (R), Capacitor (C) and Inductor (L) only are called passive filters. However, active filters are constructed using passive elements and active components (like transistors). The filtering performances of modern active filters are better compared to passive ones; also they are smaller in physical size and more flexible in application. The op-amps are widely used for designing active filter. There are various other active blocks, available in literatures which are used to implement active filters. CDBA is one among of them **[2]**. There are many CDBA topologies used to construct active filters, we are focusing on two of them namely topology (A) and topology (B) which are explained in further sections. Filters are also classified according to their response characteristics as high pass, low

pass, band pass, all pass and notch. These are described in detail in the subsequent sections of the chapter and designed using the CDBA topologies.

4.2.1 Topology (A)

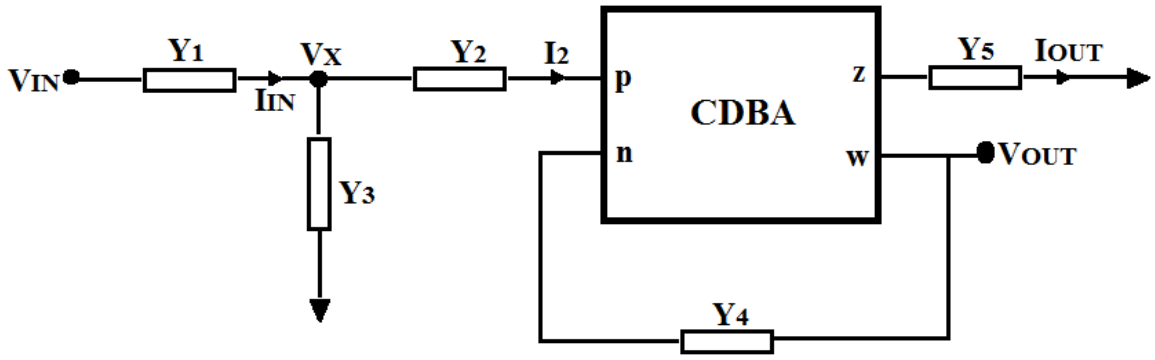

Figure 4.1 General filter topology (A) of CDBA **[12]**

The above CDBA topology is utilized to analyze the configuration for VM Filters. The voltage input V_{IN} is required to carry out VM analysis.

Using characteristic equations of CDBA given in chapter 3, the transfer function can be derived as follows:

Applying KCL at node Vx,

$$(V_{IN} - V_X)\, Y_1 = V_X Y_3 + V_X Y_2 \tag{4.5}$$

$$\frac{V_X}{V_{IN}} = \frac{Y_1}{(Y_1+Y_2+Y_3)} \tag{4.6}$$

Using characteristic equations of CDBA,

$$V_{OUT} Y_5 = V_X Y_2 - V_{OUT} Y_4 \tag{4.7}$$

$$\frac{V_{OUT}}{V_X} = \frac{Y_2}{(Y_4+Y_5)} \tag{4.8}$$

Multiplying $\frac{V_X}{V_{IN}}$ and $\frac{V_{OUT}}{V_X}$,

$$\frac{V_{OUT}}{V_{IN}} = \frac{Y_1 Y_2}{(Y_1+Y_2+Y_3)(Y_4+Y_5)} \tag{4.9}$$

Where Y_1, Y_2, Y_3, Y_4, Y_5 are the admittance in the CDBA filter topology

4.2.1.1 Low Pass Filter

A Low pass filter gives a smooth passage to low frequency signals and rejects the signal at frequencies higher than the filter's cut off frequency (f_c). Low pass filters find their application in systems or part of the system where high frequency components are to be removed from the signal. In general the transfer function of the low pass filter is,

$$H(s) = \frac{H_o}{s^2 + \frac{\omega_0}{Q}s + {\omega_0}^2} \tag{4.10}$$

Where $H_o$is pass band gain and $\omega_0 = 2\prod f_c$

Low pass filter can be designed using topology (A) of CDBA by selecting the appropriate components. For that the following G and C replacements for the admittance of the transfer function given in section 4.2.1 are done,

$Y_1 = G_1,\ Y_2 = G_2, Y_3 = sC_3,\ Y_4 = G_4,\ Y_5 = sC_5$

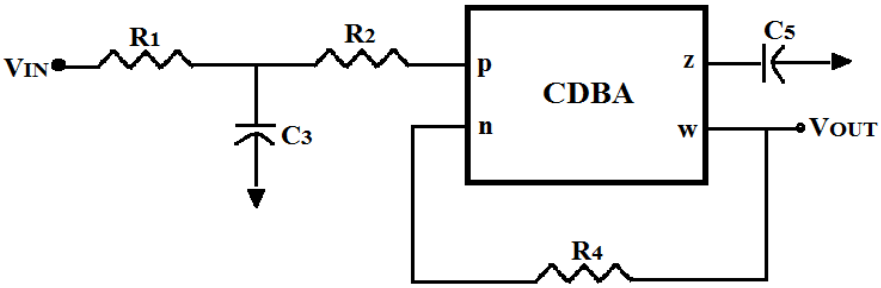

Figure 4.2 Low pass second order filter design using CDBA

By putting the above replacements transfer function of topology (A), we get transfer function for low power filter,

$$\frac{V_{OUT}}{V_{IN}} = \frac{G_1 G_2}{(G_1 + G_2 + sC_3)(G_4 + sC_5)}$$

$$= \frac{G_1 G_2}{s^2 C_3 C_5 + s(C_3 G_4 + C_5 G_1 + C_5 G_2) + G_4(G_1 + G_2)}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{\frac{G_1 G_2}{C_3 C_5}}{s^2 + s\frac{(C_3 G_4 + C_5 G_1 + C_5 G_2)}{C_3 C_5} + \frac{G_4(G_1 + G_2)}{C_3 C_5}} \tag{4.11}$$

The natural frequency ω_0 and quality factor Q can be obtained from the transfer function;

$$\omega_0 = \sqrt{\frac{G_4(G_1 + G_2)}{C_3 C_5}} \tag{4.12}$$

and

$$\frac{\omega_0}{Q} = \frac{(C_3 G_4 + C_5 G_1 + C_5 G_2)}{C_3 C_5} \tag{4.13}$$

So,

$$Q = \frac{\sqrt{C_3 C_5 G_4 (G_1 + G_2)}}{C_3 G_4 + C_5 G_1 + C_5 G_2} \tag{4.14}$$

PSPICE simulations for the types of filters namely low pass, high pass, band pass made out of topology A is done to verify the behaviour and match them with that existing in theory.

CDBA active block used is realized using the commercially available AD844 IC and its macro PSPICE model is used for simulations with a power supply of ±5V used. The simulation results for each of the filter type is presented as and when each of them is analysed. The component values for low pass filter are chosen as R1 =100, R2 =1K, C3 =1nF, R4 =1K and C5 = 10nF. Frequency response of the gain of the low pass filter is shown in figure 4.3.

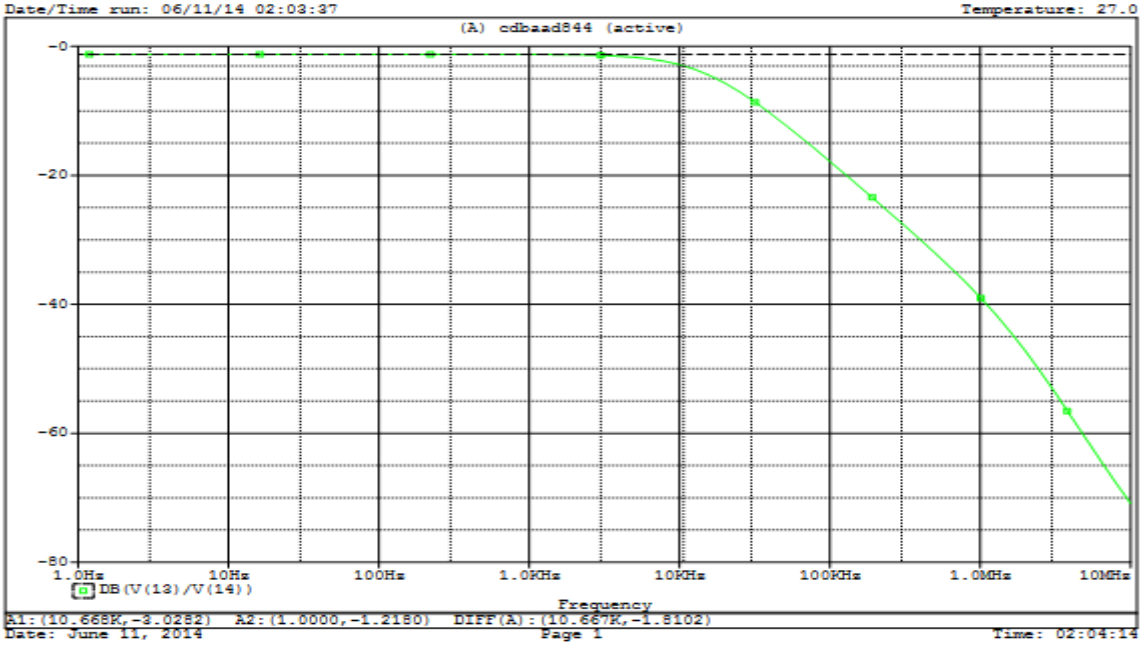

Figure 4.3 Frequency response of the gain of low pass filter

4.2.1.2 High Pass Filter

A High pass filter allows high frequency signals to pass through it and stops the signals below its cut of frequency (f_c). High pass filter can be used to block dc offset in high gain amplifiers. The transfer function of high pass filter can be obtained by adding a s^2term in the numerator of the transfer function of low pass filter and is given as,

$$H(s) = \frac{H_o s^2}{s^2 + \frac{\omega_0}{Q} s + {\omega_0}^2} \tag{4.15}$$

High pass filter design using topology (A) of CDBA can be implemented by appropriate selection of components. To accomplish that the following G and C replacements for the admittance in transfer function given in section 4.2.1are designed,

$$Y_1 = sC_1,\ Y_2 = sC_2, Y_3 = G_3,\ Y_4 = G_4,\ Y_5 = sC_5$$

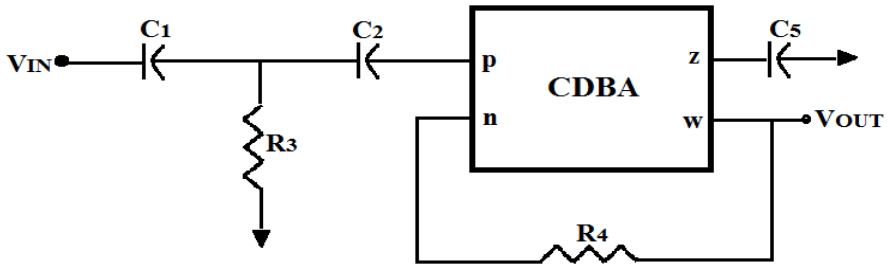

Figure 4.4 High pass second order filter design using CDBA

$$\frac{V_{OUT}}{V_{IN}} = \frac{s^2 C_1 C_2}{(sC_1+sC_2+G_3)(G_4+sC_5)}$$

$$= \frac{sC_1 G_2}{s^2(C_1+C_2)C_5+s(C_1 G_4+C_2 G_4+C_5 G_3)+G_3 G_4}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{\frac{s^2 C_1 C_2}{(C_1+C_2)C_5}}{s^2+s\frac{(C_1 G_4+C_2 G_4+C_5 G_3)}{(C_1+C_2)C_5}+\frac{G_3 G_4}{(C_1+C_2)C_5}} \quad (4.16)$$

The natural frequency ω_0 and quality factor Q can be obtained from the transfer function;

$$\omega_0 = \sqrt{\frac{G_3 G_4}{(C_1+C_2)C_5}} \quad (4.17)$$

and

$$\frac{\omega_0}{Q} = \frac{(C_1 G_4+C_2 G_4+C_5 G_3)}{(C_1+C_2)C_5} \quad (4.18)$$

So,

$$Q = \frac{\sqrt{C_5 G_3 G_4 (C_1+C_2)}}{C_1 G_4+C_2 G_4+C_5 G_3} \quad (4.19)$$

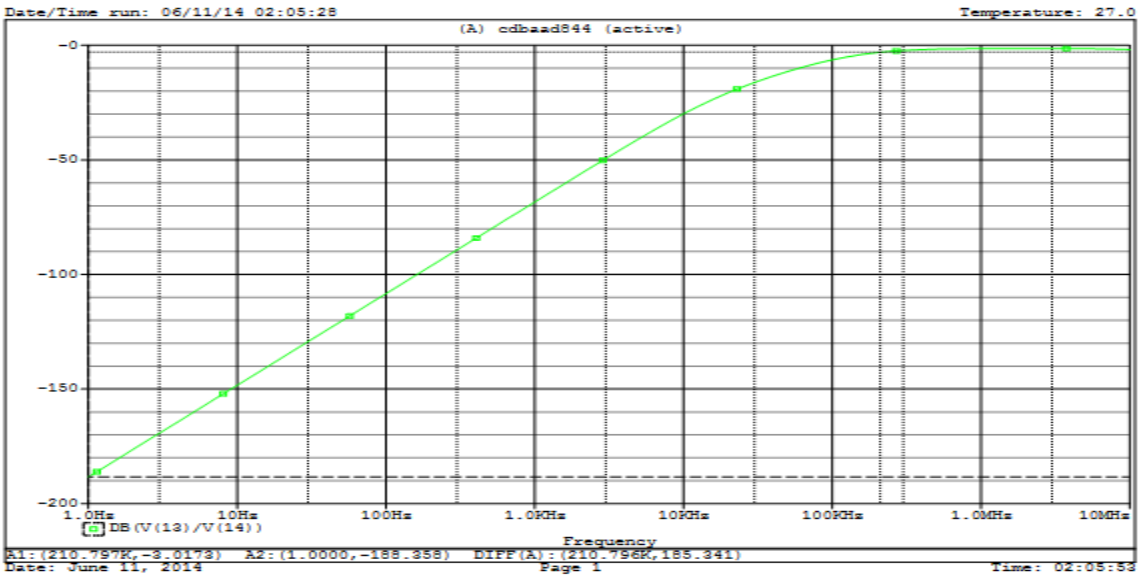

Figure 4.5 Frequency response of the gain of high pass filter

The component values for high pass filter are chosen as C1 =1nF, C2 =0.1nF, R3 =1K, R4 =100K and C5 = 0.1nF.

4.2.1.3 Band Pass Filter

A Band Pass Filter permits a specific range of frequencies to pass through, while attenuating lower and higher frequencies lying outside the desired range of frequencies. The band pass filter is widely used in audio signal processing, where a definite range of useful frequencies of sound are passed while others are blocked. Changing the numerator of low pass filter's transfer function will convert it to band pass filter given by,

$$H(s) = \frac{H_o \frac{\omega_0}{Q} s}{s^2 + \frac{\omega_0}{Q} s + {\omega_0}^2} \tag{4.20}$$

Suitable component selection in topology (A) of CDBA can lead to the construction of band pass filter. The admittance can be replaced with proper selection of these components i.e. proper G and C to get the band pass filter design,

$\boldsymbol{Y_1} = sC_1,\ \boldsymbol{Y_2} = G_2, \boldsymbol{Y_3} = sC_3,\ \boldsymbol{Y_4} = G_4,\ \boldsymbol{Y_5} = sC_5$

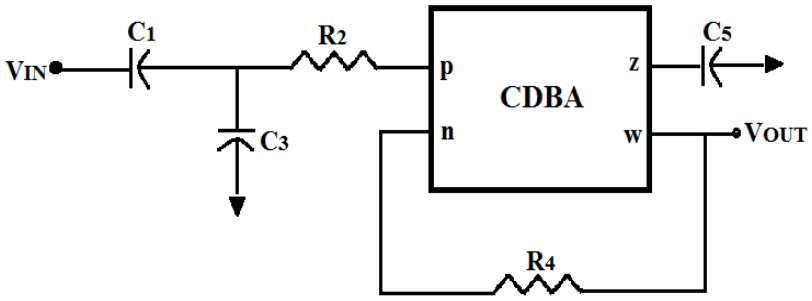

Figure 4.6 Band pass second order filter design using CDBA

$$\frac{V_{OUT}}{V_{IN}} = \frac{sC_1G_2}{(sC_1+G_2+sC_3)(G_4+sC_5)}$$

$$= \frac{sC_1G_2}{s^2(C_1+C_3)C_5+s(C_1G_4+C_3G_4+C_5G_2)+G_2G_4}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{\frac{sC_1G_2}{(C_1+C_3)C_5}}{s^2+s\frac{(C_1G_4+C_3G_4+C_5G_2)}{(C_1+C_3)C_5}+\frac{G_2G_4}{(C_1+C_3)C_5}} \tag{4.21}$$

The natural frequency ω_0 and quality factor Q can be obtained from the transfer function;

$$\omega_0 = \sqrt{\frac{G_2G_4}{(C_1+C_3)C_5}} \tag{4.22}$$

and

$$\frac{\omega_0}{Q} = \frac{(C_1G_4+C_3G_4+C_5G_2)}{(C_1+C_3)C_5} \tag{4.23}$$

So,

$$Q = \frac{\sqrt{C_5 G_2 G_4 (C_1 + C_3)}}{C_1 G_4 + C_3 G_4 + C_5 G_2} \quad (4.24)$$

The component values for band pass filter are chosen as C1 =2.2nF, R2 =470, C3 =10nF, R4 =4.7K and C5 = 1nF.

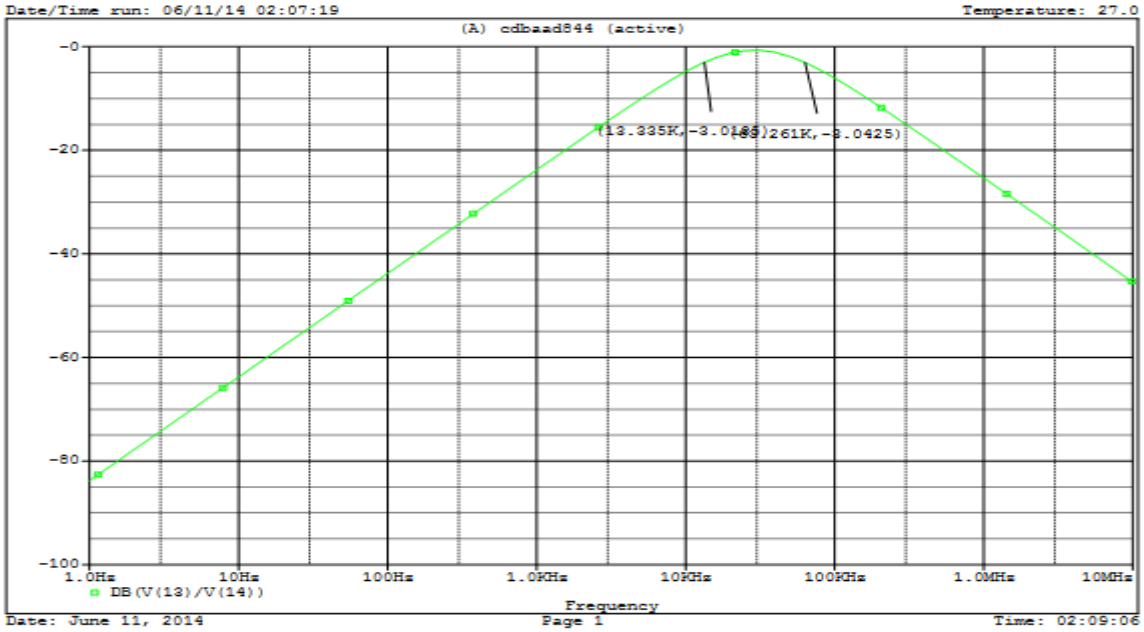

Figure 4.7 Frequency response of the gain of band pass filter

4.2.2 Topology (B)

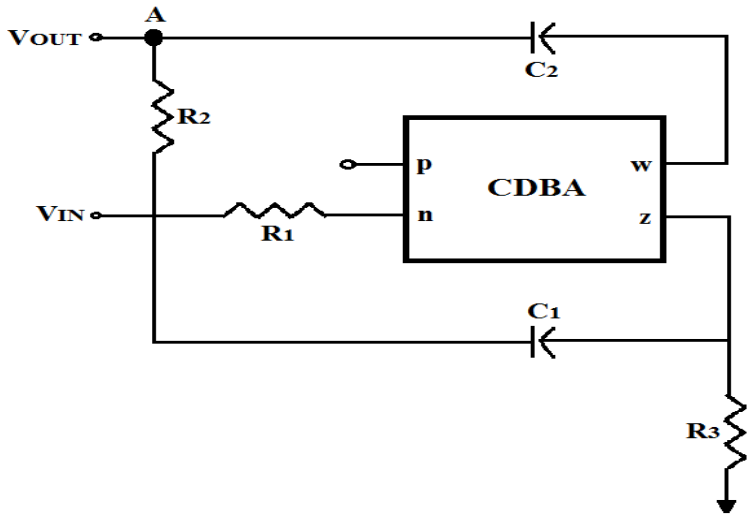

Figure 4.8 Filter topology (B) of CDBA **[15]**

The topology (B) of filter design is shown in Fig. 4.8.This topology of CDBA comprises of one CDBA block, three resistors and two capacitors.

By using characteristic equations of CDBA given in chapter 3, the transfer function can be derived as follows:

$$I_p = 0, \quad I_n = \frac{V_{IN}}{R_1}, \quad I_z = -I_n = -\frac{V_{IN}}{R_1} \tag{2.25-2.27}$$

$$I_Z = \frac{V_z}{R_3} + (V_z - V_{IN})sC_1 \tag{4.28}$$

So,

$$V_z = \frac{sC_1 - \frac{1}{R_1}}{\frac{1}{R_3} + sC_1} V_{IN} \tag{4.29}$$

Applying KCL at node A and substituting value of V_z we get,

$$V_{OUT} \frac{(sC_2R_2+1)}{R_2} \frac{(sC_1R_3+1)}{R_3} = V_{IN} \left[sC_2 \left(sC_1 - \frac{1}{R_1} \right) + \frac{sC_1R_3+1}{R_2R_3} \right]$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{s^2 + s\left(\frac{1}{C_2R_2} - \frac{1}{C_1R_1}\right) + \frac{1}{C_1C_2R_2R_3}}{s^2 + s\left(\frac{1}{C_2R_2} + \frac{1}{C_1R_3}\right) + \frac{1}{C_1C_2R_2R_3}} \tag{4.30}$$

4.2.2.1 All Pass Filter

An all pass filter does not affect the amplitude of the signal at different frequencies. It can be utilised to shift the phase of the input signal. Therefore it is also known as phase shift filter. They are used in pulsed circuits to provide phase equalization. Their application also includes SSB-SC modulation circuits. The transfer function of all pass filters is,

$$H(s) = \frac{s^2 - \frac{\omega_0}{Q}s + {\omega_0}^2}{s^2 + \frac{\omega_0}{Q}s + {\omega_0}^2} \tag{4.31}$$

An all pass filter using topology (B) is obtained by doing the following substitutions in transfer function obtained for topology B:

$$\frac{1}{C_1R_1} = \frac{2}{C_2R_2} + \frac{1}{C_1R_3} \tag{4.32}$$

Resulting transfer function obtained after the substitution is,

$$\frac{V_{OUT}}{V_{IN}} = \frac{s^2 - s\left(\frac{1}{C_2R_2} + \frac{1}{C_1R_3}\right) + \frac{1}{C_1C_2R_2R_3}}{s^2 + s\left(\frac{1}{C_2R_2} + \frac{1}{C_1R_3}\right) + \frac{1}{C_1C_2R_2R_3}} \tag{4.33}$$

The natural frequency ω_0 and quality factor Q can be obtained from the transfer function;

$$\omega_0 = \sqrt{\frac{1}{C_1C_2R_2R_3}} \tag{4.34}$$

and

$$\frac{\omega_0}{Q} = \frac{1}{C_2R_2} + \frac{1}{C_1R_3} \tag{4.35}$$

$$\text{So, } Q = \frac{\sqrt{C_1 C_2 R_2 R_3}}{C_1 R_3 + C_2 R_2} \quad (4.36)$$

PSPICE simulations for the all pass and notch filter derived from topology B is carried out to verify their functional behaviour. For simulation LVLP CDBA, designed using TSMC 0.18µm technology parameters with power supply of ±0.8V, is used.

The component values for all pass filter are chosen as R1 =2K R2 =6K R3 = 6K C1 =25pF and C2= 25pF. The magnitude frequency response of the all pass filter is shown in figure 4.9.

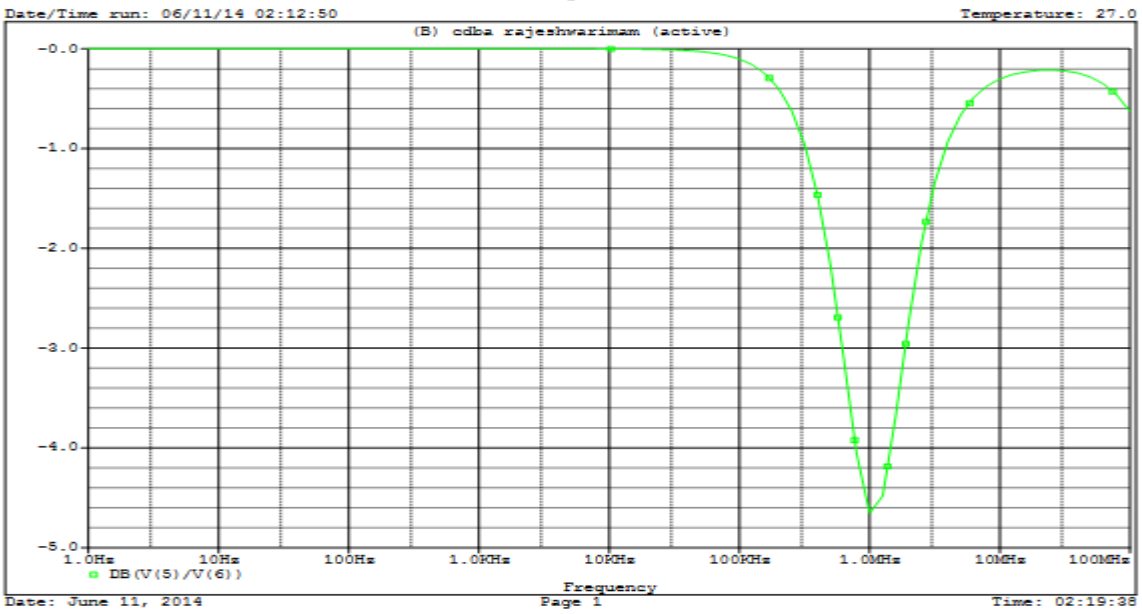

Figure 4.9 Frequency response of the gain of all pass filter

4.2.2.2 Notch Filter

It is also known as narrow band reject filter. The notch filter passes the entire frequency components lying outside its narrow stop-band. The transfer function of notch filter is given by:

$$H(s) = \frac{s^2 + {\omega_0}^2}{s^2 + \frac{\omega_0}{Q} s + {\omega_0}^2} \quad (4.37)$$

A second order notch filter from topology (B) can be obtained by satisfying the following matching condition,

$$C_1 R_1 = C_2 R_2 \quad (4.38)$$

The transfer function is obtained by substituting the above equation in general transfer function of topology (B),

$$\frac{V_{OUT}}{V_{IN}} = \frac{s^2+\frac{1}{C_1C_2R_2R_3}}{s^2+s\left(\frac{1}{C_2R_2}+\frac{1}{C_1R_3}\right)+\frac{1}{C_1C_2R_2R_3}} \quad (4.39)$$

The natural frequency ω_0 and quality factor Q is same as obtained for all pass filter;

$$\omega_0 = \sqrt{\frac{1}{C_1C_2R_2R_3}} \quad (4.40)$$

And

$$Q = \frac{\sqrt{C_1C_2R_2R_3}}{C_1R_3+C_2R_2} \quad (4.41)$$

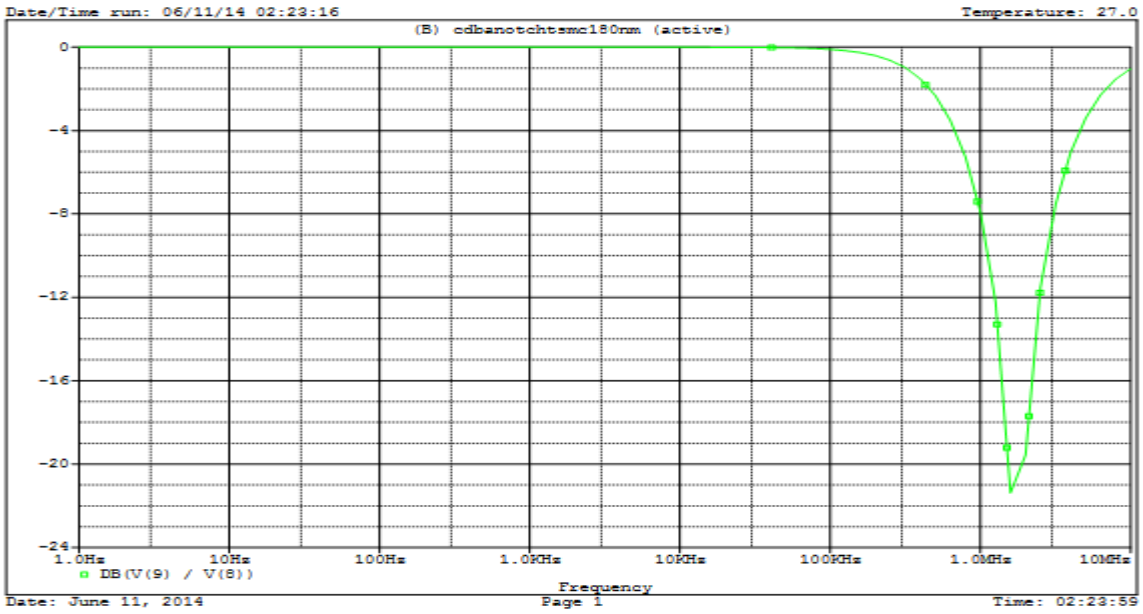

Figure 4.10 Frequency response of the gain of notch filter

Chapter 5: Signal Generators

A signal generator is a circuit which is produces signals of various shapes and frequencies used as source for many electronic circuits. Majority of circuits need some kind of input signal whose properties vary with time. The innumerable applications of signals in different domains have captured the interest of researchers to develop signal generators fulfilling the circuit needs. The signal generator circuits can broadly be classified as linear and nonlinear circuits based on their design philosophy. Linear signal generator generates AC signal of desirable frequency and amplitude. Oscillators are a type of linear signal generator and multivibrators are part of non-linear signal generator. These are explained in detail in further sections of this chapter and also they are realized with CDBA active block and their simulation results obtained by PSPICE are presented.

5.1. Linear Signal Generators

An oscillator is a linear signal generator and is regarded as an amplifier which produces its own input signal through feedback. Based on wave shapes produced by the oscillator, they can be classified broadly into two categories; Sinusoidal oscillator and Non-Sinusoidal oscillator. The oscillations in sinusoidal oscillator can be damped or undamped. There are many sine-wave oscillators like Wein bridge oscillator, Phase shift oscillator, Bubba oscillator and Quadrature oscillator. Quadrature oscillator is a type of phase shift oscillator with the feature of producing both sine and consine waves simultaneously. Next section of this chapter furnishes the analysis and implementation of quadrature oscillator using CDBA.

5.1.1. Second Order Quadrature Oscillator

The importance of QOs can be seen from the fact that it finds its use in numerous applications in measurement, signal processing and communication. It is used in single side band generators and quadrature mixers in transreceiver blocks. It is also used in selective voltmeters and vector generators for measurement purposes.

In **[20]** a systematic approach to realize QOs and to get 12 QO circuits which oscillate at same frequency, having quadrature phase difference, using CDBA has been presented. This approach has been given section 5.1.1.1 for ready reference.

The QO circuits derived in **[20]** have following attractive features:

(i) Minimum number of passive components are employed which also removes the need of component matching.

(ii) Very low passive and active sensitivities

(iii) Low harmonic distortion

(iv) Separate resistors separate resistor pairs are used to control the CO and FO of the circuits hence enabling fully uncoupled control

(v) Looking from the integrated circuit implementation perspective, the circuits have the added advantage, as resistors and capacitors are grounded/virtually grounded.

5.1.1.1. Systematic approach to realise QO circuits

A general scheme consists of a first order LPF block and an integrator bock out of which one of them is working in inverting configuration is used to realize a second order QO. The scheme is shown in Figure 5.1.

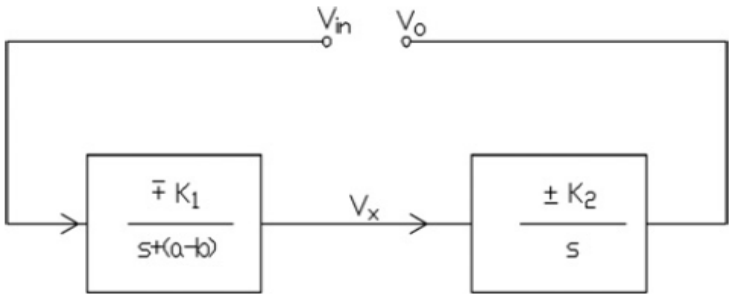

Figure 5.1 General scheme for QO realization **[20]**

The voltage transfer functions of the first-order LPF $T_1(s)$ is of type:

$$T_1(S) = \frac{V_X}{V_{in}} = \frac{K_1}{S+(a-b)} \tag{5.1}$$

Where,

K_1 and K_2 the gain constants

a and b the pole frequency

And integrator's voltage transfer function $T_2(s)$ is assumed to be of the type:

$$T_2(s) = \frac{V_O}{V_X} = \frac{K_2}{S} \tag{5.2}$$

For the oscillator circuit the loop gain can be expressed as:

$$\frac{V_o}{V_{in}} = T_1(s)T_2(s) = \frac{K_1K_2}{s[s+(a-b)]} \tag{5.3}$$

The desired characteristic transferfunction of the QO need to have the inverting configuration i.e. open loop gain of the LPF and integrator topology need to have a negative gain. This need gets us to a conclusion that one of LPF or integrators has a negative gain i.e. out of K_1 and K_2 one of them is negative. In either of the above two cases, we obtain

$$\frac{V_o}{V_{in}} = T_1(s)T_2(s) = \frac{-K_1K_2}{s[s+(a-b)]} \tag{5.4}$$

Hence the closed-loop characteristic equation is given by:

$$s^2 + s(a - b) + K_1K_2 = 0 \quad (5.5)$$

Therefore the CO is:

$$a = b$$

And the FO is found to be:

$$f_o = \frac{\sqrt{K_1K_2}}{2\pi} \quad (5.6)$$

5.1.1.2. Generation of various QO configurations using CDBAs

The generalized scheme developed in the previous section is used to generate QOs. These QOs use two CDBA blocks each to realize the LPF and integrator block of the configuration.

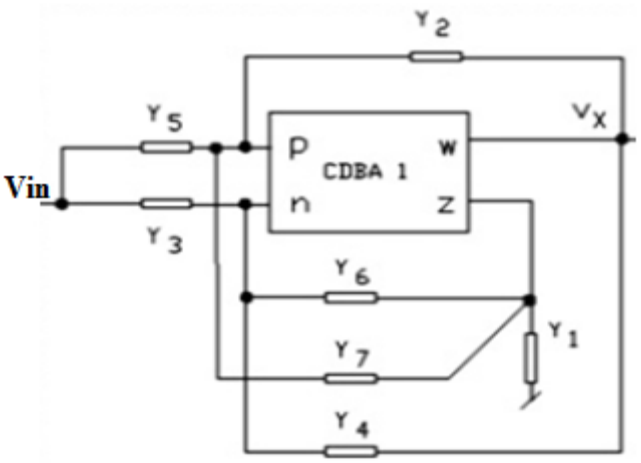

Figure 5.2 General configuration for LPF block [20]

The generalized configuration for the LPF block is shown in Figure 5.2 and its transfer function is found to be:

$$\frac{V_X}{V_{in}} = \frac{(Y_5 - Y_3)}{(Y_1 + 2Y_6 + Y_4 - Y_2)} \quad (5.7)$$

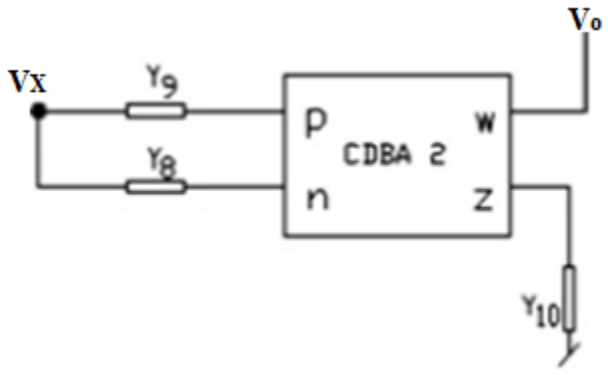

Figure 5.3 General configuration for integrator block **[20]**

Figure 5.3 depicts the same for integrator block and its transfer function is given by:

$$\frac{V_o}{V_X} = \frac{Y_9 - Y_8}{Y_{10}} \tag{5.8}$$

S.No.	Low pass filter circuits							Integrator circuits			
	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	$T_1(S)$	Y_8	Y_9	Y_{10}	$T_2(S)$
1	sC_1	$\frac{1}{R_2}$	$\frac{1}{R_3}$	$\frac{1}{R_4}$	0	0	$\frac{-1}{C_1 R_3\left[s + \frac{1}{C_1}\left(\frac{1}{R_4} - \frac{1}{R_2}\right)\right]}$	0	$\frac{1}{R_9}$	sC_{10}	$\frac{1}{sC_{10}R_9}$
2	sC_1	$\frac{1}{R_2}$	$\frac{1}{R_3}$	0	0	$\frac{1}{R_6}$	$\frac{-1}{C_1 R_3\left[s + \frac{1}{C_1}\left(\frac{2}{R_6} - \frac{1}{R_2}\right)\right]}$	0	$\frac{1}{R_9}$	sC_{10}	$\frac{1}{sC_{10}R_9}$
3	sC_1	$\frac{1}{R_2}$	0	$\frac{1}{R_4}$	$\frac{1}{R_5}$	0	$\frac{1}{C_1 R_5\left[s + \frac{1}{C_1}\left(\frac{1}{R_4} - \frac{1}{R_2}\right)\right]}$	$\frac{1}{R_8}$	0	sC_{10}	$\frac{-1}{sC_{10}R_8}$
4	sC_1	$\frac{1}{R_2}$	0	0	$\frac{1}{R_5}$	$\frac{1}{R_6}$	$\frac{1}{C_1 R_5\left[s + \frac{1}{C_1}\left(\frac{2}{R_6} - \frac{1}{R_2}\right)\right]}$	$\frac{1}{R_8}$	0	sC_{10}	$\frac{-1}{sC_{10}R_8}$
5	$\frac{1}{R_1}$	$\frac{1}{R_2}$	$\frac{1}{R_3}$	sC_4	0	0	$\frac{-1}{C_4 R_3\left[s + \frac{1}{C_4}\left(\frac{1}{R_1} - \frac{1}{R_2}\right)\right]}$	0	$\frac{1}{R_9}$	sC_{10}	$\frac{1}{sC_{10}R_9}$
6	$\frac{1}{R_1}$	$\frac{1}{R_2}$	0	sC_4	$\frac{1}{R_5}$	0	$\frac{1}{C_4 R_5\left[s + \frac{1}{C_4}\left(\frac{1}{R_1} - \frac{1}{R_2}\right)\right]}$	$\frac{1}{R_8}$	0	sC_{10}	$\frac{-1}{sC_{10}R_8}$
7	$\frac{1}{R_1}$	$\frac{1}{R_2}$	$\frac{1}{R_3}$	0	0	sC_6	$\frac{-1}{2C_6 R_3\left[s + \frac{1}{2C_6}\left(\frac{1}{R_1} - \frac{1}{R_2}\right)\right]}$	0	$\frac{1}{R_9}$	sC_{10}	$\frac{1}{sC_{10}R_9}$
8	$\frac{1}{R_1}$	$\frac{1}{R_2}$	0	0	$\frac{1}{R_5}$	sC_6	$\frac{1}{2C_6 R_5\left[s + \frac{1}{2C_6}\left(\frac{1}{R_1} - \frac{1}{R_2}\right)\right]}$	$\frac{1}{R_8}$	0	sC_{10}	$\frac{-1}{sC_{10}R_8}$
9	0	$\frac{1}{R_2}$	$\frac{1}{R_3}$	$\frac{1}{R_4}$	0	sC_6	$\frac{-1}{2C_6 R_3\left[s + \frac{1}{2C_6}\left(\frac{1}{R_4} - \frac{1}{R_2}\right)\right]}$	0	$\frac{1}{R_9}$	sC_{10}	$\frac{1}{sC_{10}R_9}$
10	0	$\frac{1}{R_2}$	0	$\frac{1}{R_4}$	$\frac{1}{R_5}$	sC_6	$\frac{1}{2C_6 R_5\left[s + \frac{1}{2C_6}\left(\frac{1}{R_4} - \frac{1}{R_2}\right)\right]}$	$\frac{1}{R_8}$	0	sC_{10}	$\frac{-1}{sC_{10}R_8}$
11	0	$\frac{1}{R_2}$	$\frac{1}{R_3}$	sC_4	0	$\frac{1}{R_6}$	$\frac{-1}{C_4 R_3\left[s + \frac{1}{C_4}\left(\frac{2}{R_6} - \frac{1}{R_2}\right)\right]}$	0	$\frac{1}{R_9}$	sC_{10}	$\frac{1}{sC_{10}R_9}$
12	0	$\frac{1}{R_2}$	0	sC_4	$\frac{1}{R_5}$	$\frac{1}{R_6}$	$\frac{1}{C_4 R_5\left[s + \frac{1}{C_4}\left(\frac{2}{R_6} - \frac{1}{R_2}\right)\right]}$	$\frac{1}{R_8}$	0	sC_{10}	$\frac{-1}{sC_{10}R_8}$

Table 5.1 Various LPF realising T1(s) and integratorT2(s), which yield the required QOs

Here, as can be seen from Figure 5.2 and 5.3 Y1 through Y6 admittances are used to realize the transfer function $T_1(s) = (V_X/V_{in}) = K_1/(s + (a - b))$ whereas Y8 through Y10 admittances are used to derive the transfer function $T_2(s) = (V_O/ V_x) = (K_2/s)$. Either of $T_1(s)$ or $T_2(s)$ is negative which the required condition to be satisfied for QOs is.

Table 5.1 lists various transfer functions which realize $T_1(s)$ of LPF circuits and $T_2(s)$ of integrator circuits. These transfer functions together realize the required kind of QOs. The QOs circuits thus derived from the transfer function are shown in Figure 5.4.

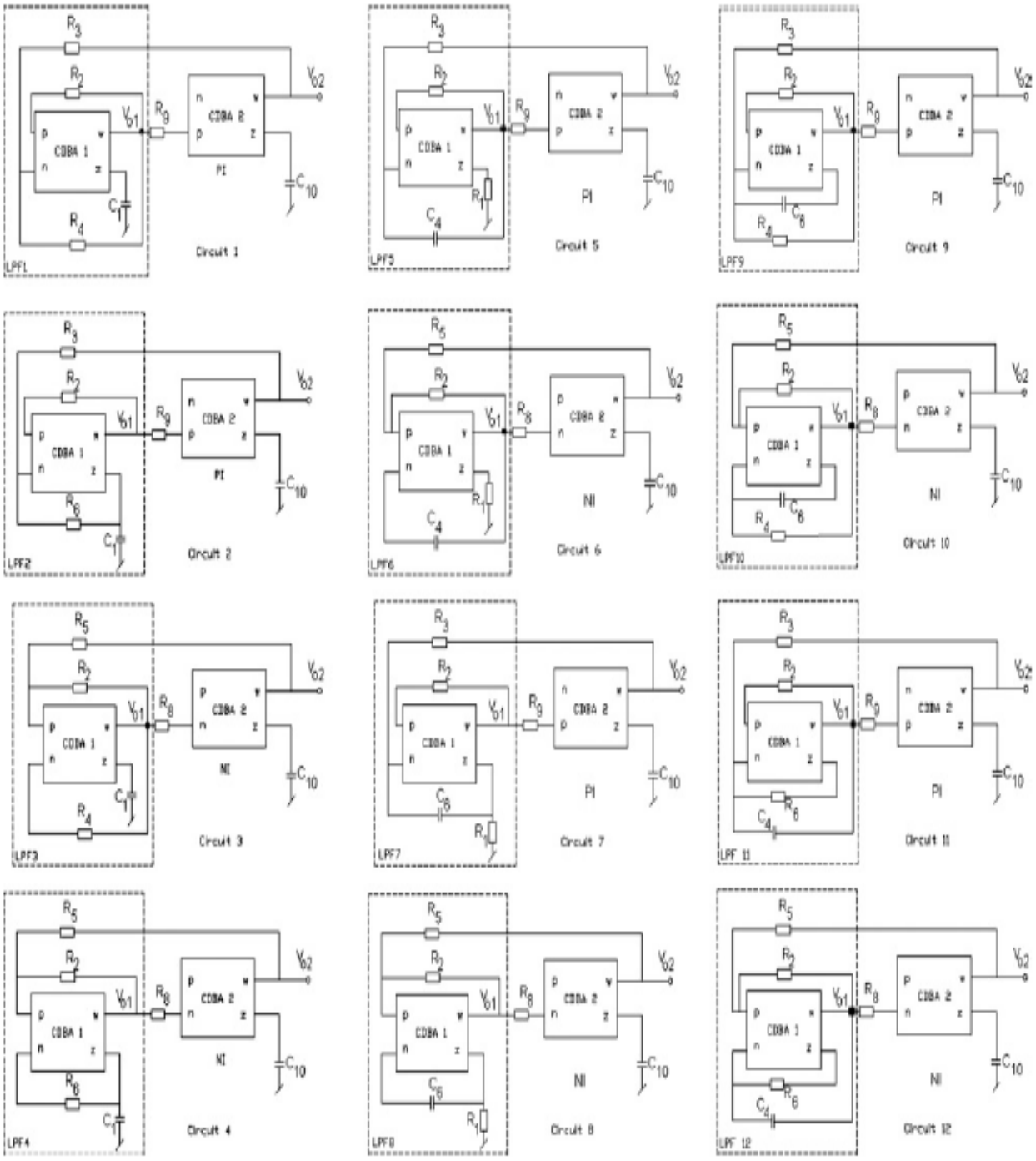

Figure 5.4 Various CDBA-based QO circuits **[20]**

QO circuit	LPF	Integrator	CO[a=b]	FO$\left[\frac{\sqrt{K_1K_2}}{2\pi}\right]$
1	LPF1	NI	$R_2 = R_4$	$\frac{1}{2\pi\sqrt{C_1C_{10}R_3R_9}}$
2	LPF2	NI	$2R_2 = R_6$	$\frac{1}{2\pi\sqrt{C_1C_{10}R_3R_9}}$
3	LPF3	I	$R_2 = R_4$	$\frac{1}{2\pi\sqrt{C_1C_{10}R_5R_8}}$
4	LPF4	I	$2R_2 = R_6$	$\frac{1}{2\pi\sqrt{C_1C_{10}R_5R_8}}$
5	LPF5	NI	$R_2 = R_1$	$\frac{1}{2\pi\sqrt{C_4C_{10}R_3R_9}}$
6	LPF6	I	$R_2 = R_1$	$\frac{1}{2\pi\sqrt{C_4C_{10}R_5R_8}}$
7	LPF7	NI	$R_2 = R_1$	$\frac{1}{2\pi\sqrt{2C_6C_{10}R_3R_9}}$
8	LPF8	I	$R_2 = R_1$	$\frac{1}{2\pi\sqrt{2C_6C_{10}R_5R_8}}$
9	LPF9	NI	$R_2 = R_1$	$\frac{1}{2\pi\sqrt{2C_6C_{10}R_3R_9}}$
10	LPF10	I	$R_2 = R_1$	$\frac{1}{2\pi\sqrt{2C_6C_{10}R_5R_8}}$
11	LPF11	NI	$2R_2 = R_6$	$\frac{1}{2\pi\sqrt{C_4C_{10}R_3R_9}}$
12	LPF12	I	$2R_2 = R_6$	$\frac{1}{2\pi\sqrt{C_4C_{10}R_5R_8}}$

Note: NI-Noninverting I-inverting

Table 5.2: parameters of the various QO circuits

Table 5.2 enlists various parameters of the circuits derived, it can be observed that CO and FO are respectively dependent on different set of resistors and can be set as needed independently of the other. This proves the uncoupled behaviour of the circuits thus derived, for eg. QO circuit 1 has two resistances R2 and R4 appearing in the CO which do not appear in the FO and the rest of the two resistors namely R3 and R9 appear in the FO

term. This fully uncoupled and independent control of CO and FO can be seen in all the other cases too.

The relationship between V01 and V02 as seen from configurations of Figure 5.4 can be expressed as:

$$\frac{V_{02}}{V_{01}} = \pm sC_{10}R_k \qquad (5.9)$$

Where,

for oscillators 3, 4, 6, 8, 10, 12 k = 8

for oscillator 1, 2, 5, 7, 9, 11 k = 9

This indicates that V01 and V02 are in quadrature phase i.e.in all the circuits thus derived the phase shift between V01 and V02 is equal to F = ±90˚.

5.1.1.3. PSPICE simulation results

All the derived CDBA based QO circuits are simulated using PSPICE to verify the theoretical results. The CDBA block is made out of commercially available AD844 IC's with supply voltages of ±12V and macro model of these IC's are used for PSPICE simulations. The component values chosen for circuit 1 are C1 = C10 = 100pF, R2 = 4KΩ, R4 = 5KΩ and R3 = R9 = 700Ω. And a simulated frequency was observed to be 2.01 MHz which was in accordance with theoretical calculations.

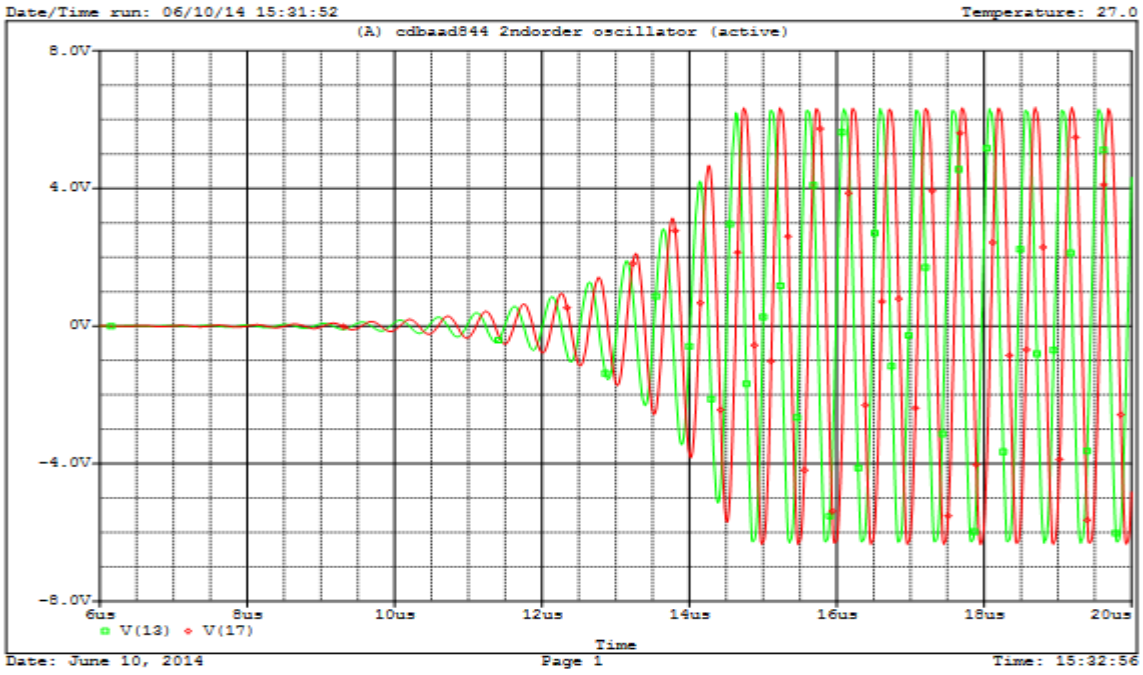

Figure 5.5 Transient waveform for oscillator circuit 1

The output waveform for the oscillator derived from circuit 1 showing the build-up of oscillations is shown in Figure 5.5 and steady state output waveform is shown in Figure

5.6, which confirms the realization of QOs. Frequency spectrum of the outputs V01 and V02 is displayed in Figure 5.7 which shows that the circuit oscillates at 2.01 MHz, also for the two outputs the phase shift was found to be between 89.27˚ and 93.20˚.

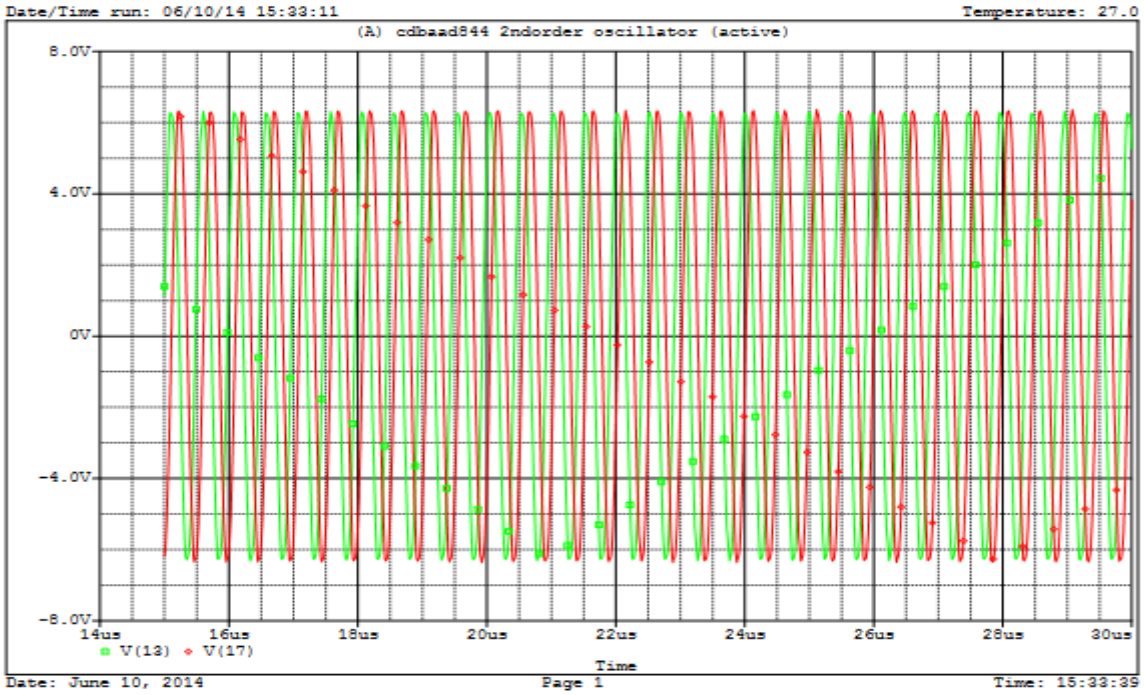

Figure 5.6 Steady state waveform for oscillator circuit 1

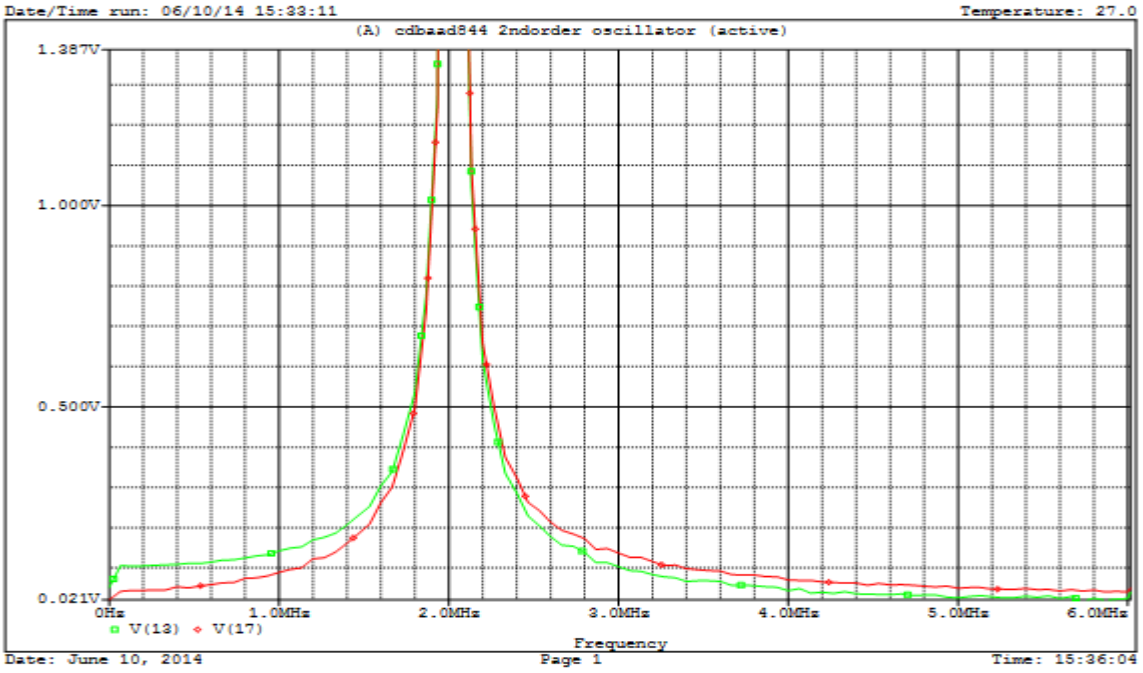

Figure 5.7 Frequency spectrum for oscillator circuit 1

5.2.Non-linear Signal Generators

This type of signal generator includes multivibrator. A multivibrator circuit rapidly switches the output between two or more states. This is achieved by the means of positive

feedback in the circuit. Based on circuit operation, multivibrators can be categorized as: Bistable, Monostable and Astable Multivibrator. Bistable multivibrator has stable output in either state and the state can be flipped to other by externally triggering the circuit. Monostable multivibrator has one stable state but the other one is unstable. The circuit get into the unstable state by the trigger pulse and returns to stable one after a set time. In astable multivibrator the output is not stable and continuously switches from one state to another indefinitely. It does not need an external assistance to oscillate. It is a free running circuit and produces a continuous square wave at output.

The astable multivibrator circuit finds numerous applications in various fields like signal processing, communication systems, digital systems etc. Few CDBA based astable multivibrator configurations are available in literature **[36-37]** and in the following section the astable multivibrators with controlled and uncontrolled duty cycle **[27]** have been discussed and simulated for functional verification.

5.2.1. Uncontrolled Duty Cycle Astable Multivibrator

An astable multivibrator circuit using CDBA block and three passive elements is shown in Figure 5.8. These passive elements include a series connection of a resistor (R_F) and a capacitor in a positive feedback loop and also a resistor (R_L) connected as load to Z-terminal in CDBA block.

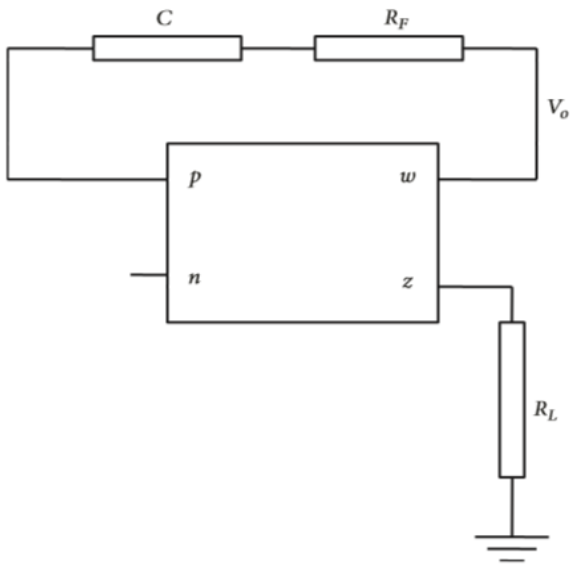

Figure 5.8 Astable multivibrator with fixed duty cycle **[27]**

The appropriate value of R_L is chosen so that it can drive the output voltage of the circuit to any one saturation level i.e. V^+_{sat} *or* V^-_{sat} which causes the feedback loop capacitor to charge shown in Figure 5.9. Further the figure depicts that after a certain voltage is

reached across the feedback capacitor that reduces the sufficient amount current in R_L switches the output voltage from $V^+_{sat}\ to\ V^-_{sat}$ and initiates the charging of capacitor in negative direction.

The threshold voltages that switches the output from $V^+_{sat}\ to\ V^-_{sat}$ or vice versa when that value is reached across feedback capacitor is given as,

$$V_{TH} = \frac{(R_L - R_F)}{R_L} V^+_{sat} \tag{5.10}$$

$$V_{TL} = \frac{(R_L - R_F)}{R_L} V^-_{sat} \tag{5.11}$$

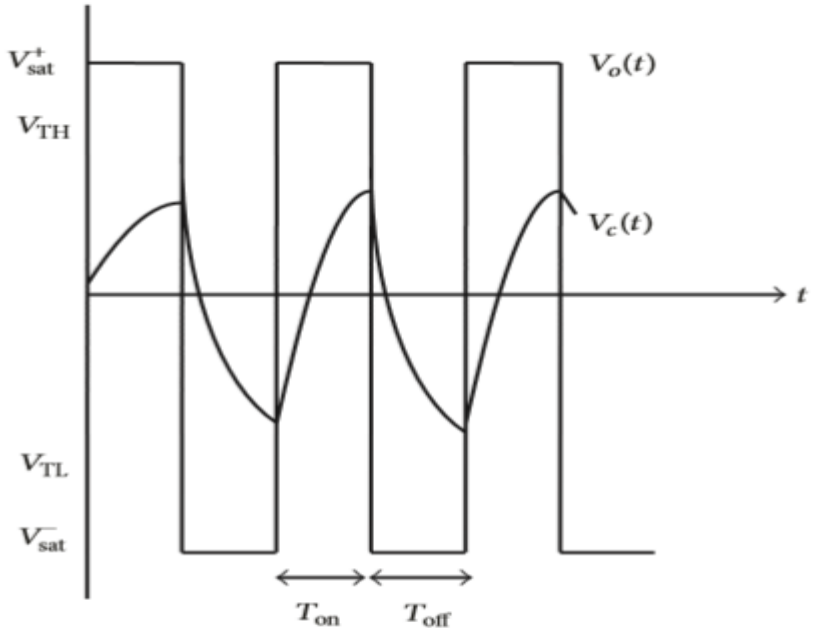

Figure 5.9 output of the astable multivibrator **[27]**

The charging time of capacitor from $V_{TL} to\ V_{TH}$ is given by:

$$T_{on} = R_F C\ In\left[\frac{2R_L}{R_F} - 1\right] \tag{5.12}$$

Similarly, the discharging time of capacitor from $V_{TH} to\ V_{TL}$ is

$$T_{off} = R_F C\ In\left[\frac{2R_L}{R_F} - 1\right] \tag{5.13}$$

where $R_L > R_F$.

As $T_{on} = T_{off}$, thus a symmetric square wave with amplitudes $V^+_{sat}\ and\ V^-_{sat}$ is obtained at the output of the multivibrator circuit. Therefore, the output is of fixed 50% duty cycle and controllable frequency given by,

$$f_o = \frac{1}{T_{on} + T_{off}} = \frac{1}{2R_F C\ In\left[\frac{2R_L}{R_F} - 1\right]} \tag{5.14}$$

PSPICE simulations for uncontrolled duty cycle multivibrator were performed to verify the theoretical predictions. For simulation CDBA block designed using PSPICE macro model of commercially available AD844 IC was used. The component values are chosen as $R_F = 20K\Omega, R_L = 50K\Omega \; and \; C = 10\mu F$. The simulated square wave output is shown in Figure 5.10. The value was observed to be 1.833Hz as against the theoretically computed value of 1.9Hz i.e. a percentage error of 3.53%.

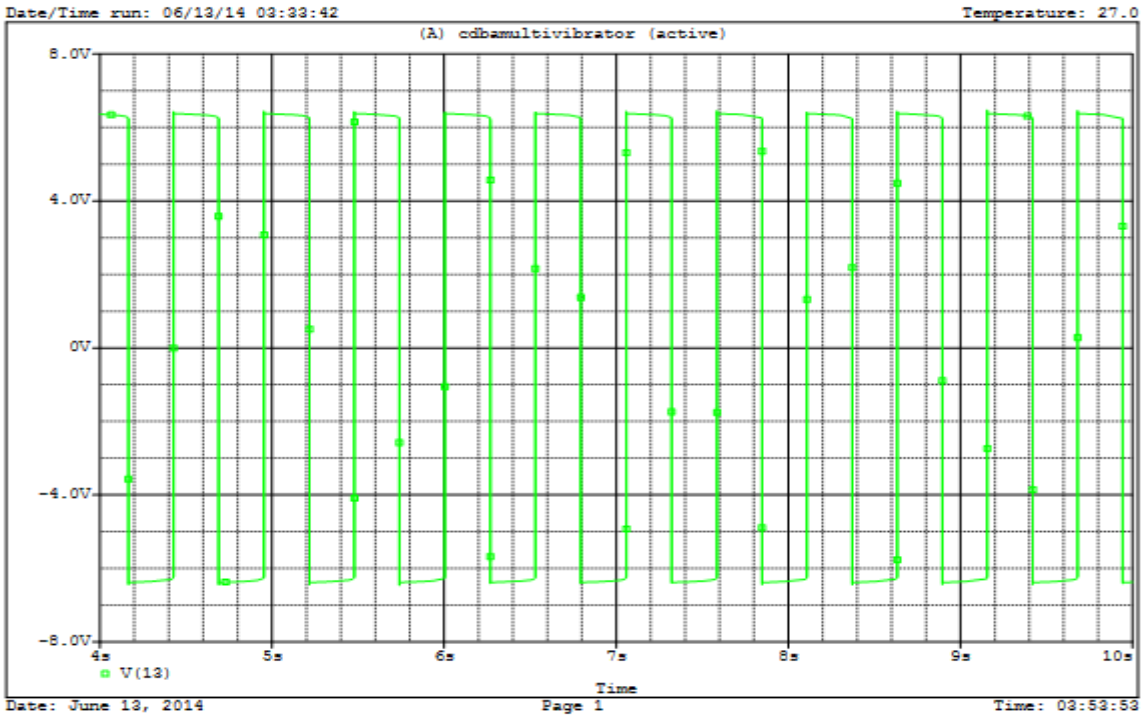

Figure 5.10 Output waveform for astable multivibrator with fixed duty cycle

5.2.2. Controlled Duty Cycle Astable Multivibrator

The astable multivibrator circuit shown in the above section generates square wave of fixed duty cycle. However to obtain the output with variable duty cycle, certain modifications in the circuit of Figure 5.8 must be made. In the subsequent sections two methods **[27]** to obtain output signals of variable duty cycle have been dealt with.

5.2.2.1 Resistor Controlled Duty Cycle Astable Multivibrator

The modifications adopted to get resistor controlled duty cycle astable multivibrator are shown in Figure 5.11. In this figure we have replaced the feedback resistor R_F (in Figure 5.8) with two pairs of a diode and a resistor connected in parallel to each other. This idea was picked up from **[38]** where this scheme was discussed for OTRA and it was adapted in **[27]** for implementing it with CDBA.

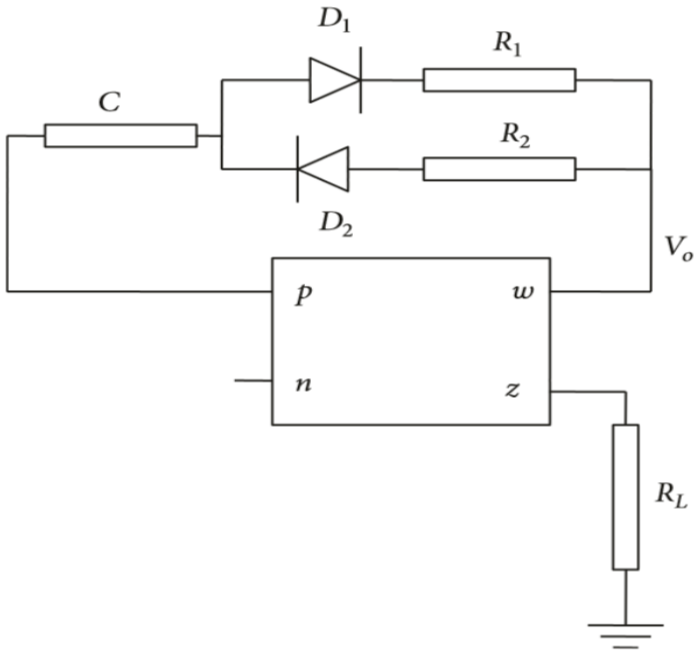

Figure 5.11 Astable multivibrator having resistor-controlled duty cycle **[27]**

Considering the diodes to be ideal, we can get the threshold voltages as,

$$V_{TH} = \frac{(R_L - R_2)}{R_L} V_{sat}^{+} \tag{5.15}$$

$$V_{TL} = \frac{(R_L - R_1)}{R_L} V_{sat}^{-} \tag{5.16}$$

Further, the charging and discharging time for the capacitor may be obtained as,

$$T_{on} = R_2 C \; In\left[\frac{2R_L - R_1}{R_2}\right] \tag{5.17}$$

and

$$T_{off} = R_1 C \; In\left[\frac{2R_L - R_2}{R_1}\right] \tag{5.18}$$

Respectively. It can be observed from the above equations of capacitor's charging and discharging time that T_{on} and T_{off} are controllable through the resistors R_1 and R_2, thus verifying the controlled duty cycle operation of the multivibrator through resistors. So, the output frequency of the variable duty cycle multivibrator can be obtained as,

$$f_o = \frac{1}{T_{on} + T_{off}} = \frac{1}{R_2 C \; In\left[\frac{2R_L - R_1}{R_2}\right] + R_1 C \; In\left[\frac{2R_L - R_2}{R_1}\right]} \tag{5.19}$$

PSPICE simulations for the circuit configuration shown in Figure 5.10 was done to verify the variation of duty cycle as the passive components of the circuit are varied. The component values are chosen as $R_L = 40K, C = 1nF$. Also, $R_1 = 25K\Omega, R_2 = 2K\Omega$ for curve 1 and $R_1 = 25K\Omega, R_2 = 2K\Omega$ for curve 2.

The output waveforms are seen in Figure 5.12 and it can be clearly seen from the simulation results that the on and off periods of the simulated waveform are not fixed i.e. they have variable duty cycle.

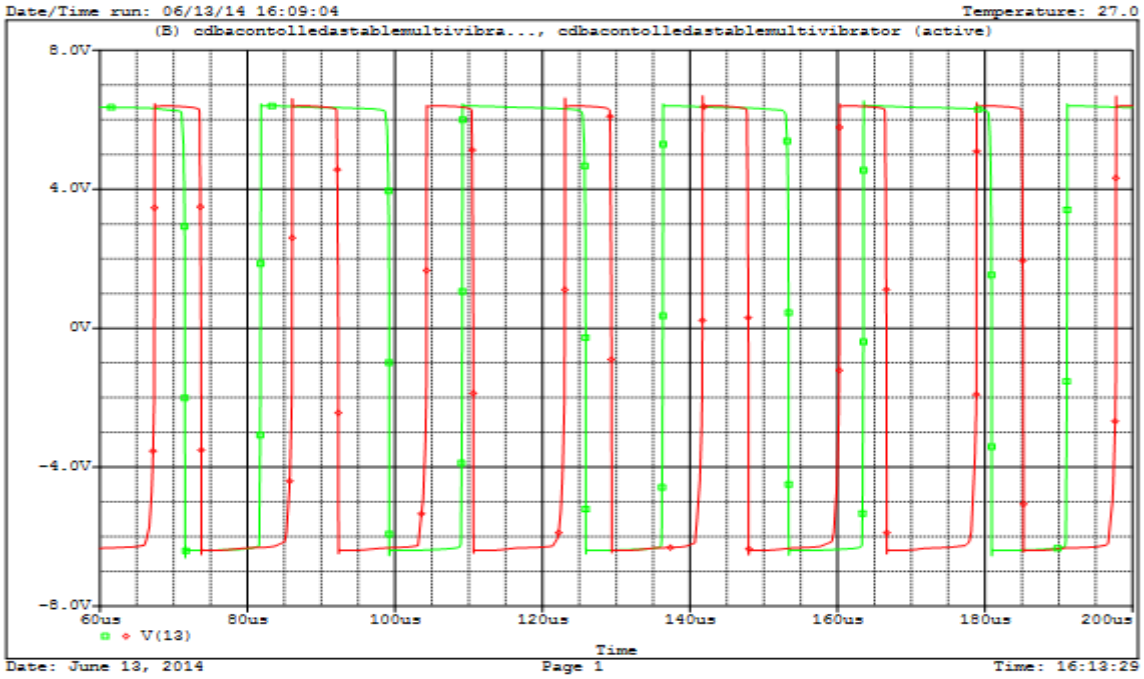

Figure 5.12.Output waveform with resistor controlled variable duty cycle

5.2.2.1 Electronically Controlled Duty Cycle Astable Multivibrator

The adaptations required in Figure 5.8 to get electronically controlled duty cycle astable multivibrator are shown in Figure 5.13. This includes inserting a DC source and a series resistor R_s to the p terminal of CDBA. This circuit controls the duty cycle of the multivibrator electronically through the external DC source voltage (V_{dc}).

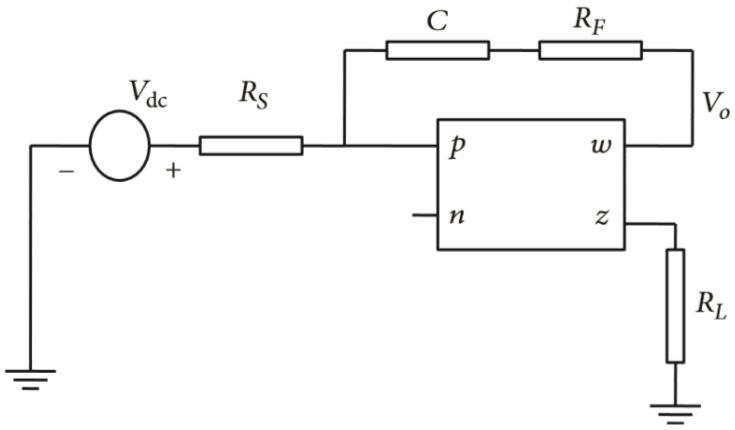

Figure 5.13 Astable multivibrator having electronically-controlled duty cycle.[36]

By analysing the circuit, we can get the threshold voltages as,

$$V_{TH} = V_{sat}^{+}\left(1 - \frac{R_F}{R_L}\right) + V_{dc}\frac{R_F}{R_S} \qquad (5.20)$$

$$V_{TL} = V_{sat}^{-}\left(1 - \frac{R_F}{R_L}\right) + V_{dc}\frac{R_F}{R_S} \tag{5.21}$$

Further, we can obtain the charging and discharging time for the capacitor as,

$$T_{on} = RC\ ln\frac{\left[\frac{2R_L}{R_F} - 1\right] - \frac{R_L V_{dc}}{V_{sat}^{+} R_s}}{\left[1 - \frac{R_L V_{dc}}{V_{sat}^{+} R_s}\right]} \tag{5.22}$$

and

$$T_{off} = RC\ ln\frac{\left[\frac{2R_L}{R_F} - 1\right] - \frac{R_L V_{dc}}{V_{sat}^{-} R_s}}{\left[1 - \frac{R_L V_{dc}}{V_{sat}^{-} R_s}\right]} \tag{5.23}$$

respectively.

It can be observed from the above equations of capacitor's charging and discharging time that T_{on} and T_{off} are controllable through the externally applied voltage, V_{dc}, thus verifying the controlled duty cycle operation of the multivibrator through source voltage. So, the output frequency of the variable duty cycle multivibrator controlled electronically can be obtained as,

$$f_o = \frac{1}{T_{on} + T_{off}} = \frac{1}{RC\left[ln\frac{\left(\frac{2R_L}{R_F} - 1\right) - \frac{R_L V_{dc}}{V_{sat}^{+} R_s}}{\left(1 - \frac{R_L V_{dc}}{V_{sat}^{+} R_s}\right)} + ln\frac{\left(\frac{2R_L}{R_F} - 1\right) - \frac{R_L V_{dc}}{V_{sat}^{-} R_s}}{\left(1 - \frac{R_L V_{dc}}{V_{sat}^{-} R_s}\right)}\right]} \tag{5.24}$$

The simulation for the circuit shown is Figure 5.13 was performed to verify its functional behaviour. The component values are chosen as $R_s = 40K\Omega, R_L = 40K\Omega, R_F = 15K\Omega$ and $C = 1nF$..

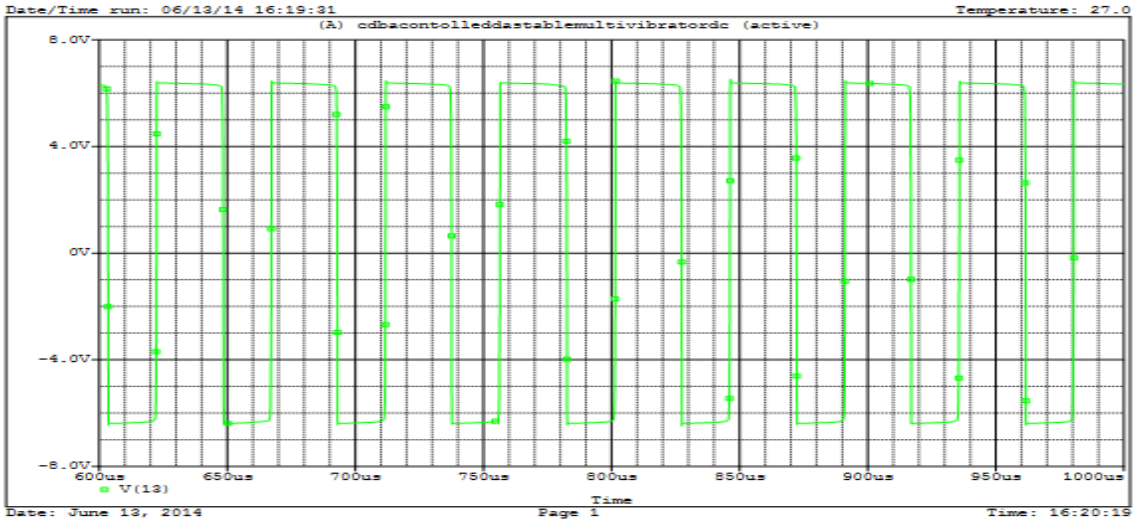

Figure 5.14 Output waveform for Vdc = 2V

The output waveforms of the circuit for three different values of Vdc that is 2V, 5V and -2V respectively are shown in Figure 5.14, 5.15 and 5.16. It can be seen that the output frequency and the duty cycle of the output waveform for the above circuit can be electronically controlled by the DC voltage supply Vdc.

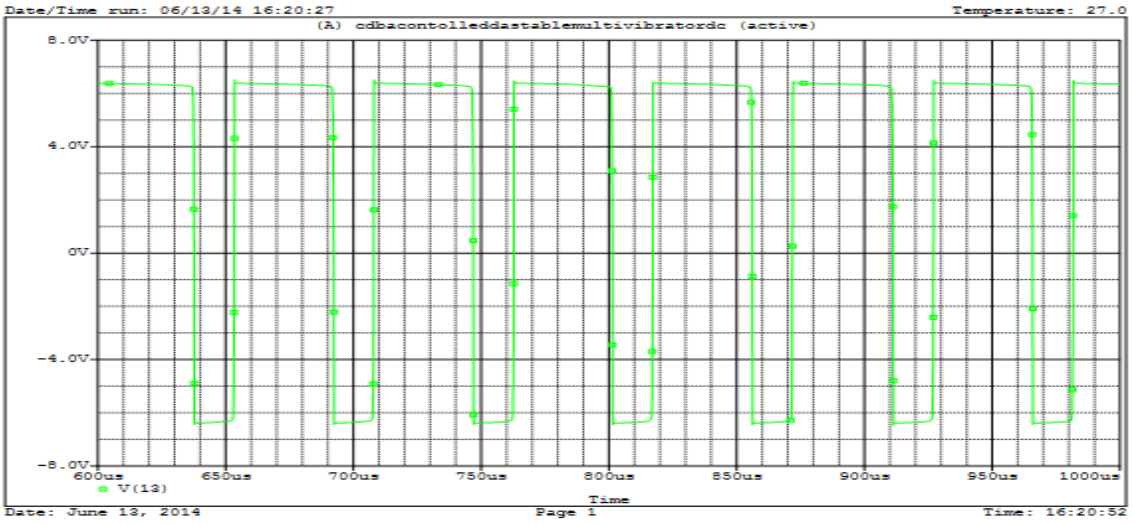

Figure 5.15 Output waveform for Vdc = 5V

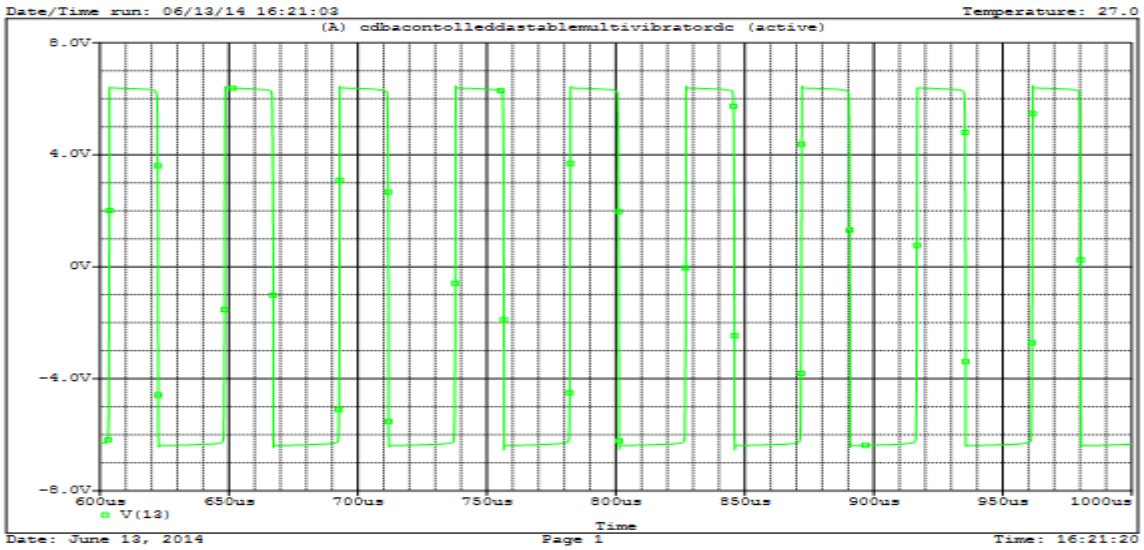

Figure 5.16 Output waveform for Vdc = -2V

Chapter 6: New Propositions

6.1.Second Order Quadrature Oscillator

This section proposes a new configuration for the quadrature oscillator circuit. As the name suggests the circuit produces two signals oscillating at the same frequency but have quadrature phase difference unconditionally. It uses an inverting and a noninverting integrators designed using CDBA connected in cascade and forming a unity gain closed loop, thus resulting in sustained oscillations. The circuit is verified using PSPICE simulations and the resulting output waveforms obtained are shown in sections to follow.

The proposed QO configuration has following key features:

(i) Minimum number of passive components are employed.

(ii) High integrated circuit implementation capability, as the circuits have resistors and capacitors grounded/virtually grounded.

6.1.1. Approach to realize QO Circuit

The QO explained earlier is made out of a feedback configuration of two integrators as shown in figure 6.1.

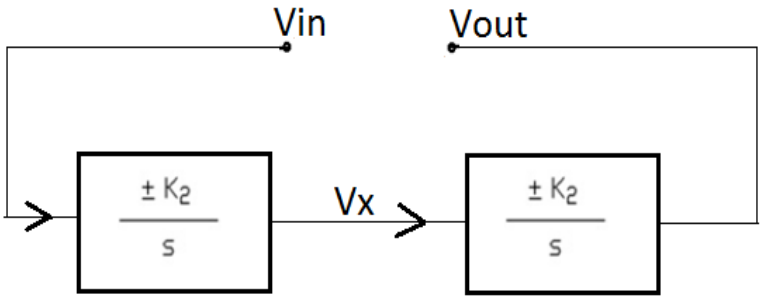

Figure 6.1 Scheme for unconditioned QO realization

The voltage transfer function for the integrator is of the type:

$$T_1(S) = \frac{V_O}{V_X} = \pm\frac{K_2}{S} \quad (6.1)$$

Where,

K_2 gain constant.

Two such integrators are combined and hence the open loop gain of the oscillator circuit can be expressed as:

$$\frac{V_o}{V_{in}} = T_1(s)T_1(s) = \pm\frac{{K_2}^2}{S^2} \quad (6.2)$$

The two integrators can be inverting or noninverting based on the condition to be satisfies for the circuit to oscillate, which is the open loop gain of the oscillator circuit should be inverting and hence the transfer function should be negative. This conclusion leads us to a

fact that either of the two integrators used in the general approach need to be inverting. Hence the QO is made out of a feedback network made of an inverting and a noninverting integrator. Therefore the open loop gain is given by:

$$\frac{V_o}{V_{in}} = T_1(s)T_1(s) = \frac{-{K_2}^2}{S^2} \quad (6.3)$$

Hence, the closed loop characteristics equation is given by:

$$s^2 + {K_2}^2 = 0 \quad (6.4)$$

This is the condition which is needed to be satisfied according to Barkhausen criteria **[1]** for the circuit to oscillate. Using the above equation it was found that the circuit is always oscillating and need not satisfy any condition for the oscillations to occur. The reason for this being the absence of the 's' term in the characteristic equation, hence the oscillator thus derived is called unconditional Quadrature oscillator. The frequency of oscillation is given below and can be varied by changing the gain of the used integrator circuit.

$$f_o = \frac{K_2}{2\pi} \quad (6.5)$$

6.1.2. Generation and Simulation Using CDBA

The above scheme is used to generate the QO circuit, where both the inverting and noninverting integrators are implemented with the help of CDBA active block. Figure 6.2 shows a generalized configuration which can irrespectively be used for the generation of any type of integrator circuit.

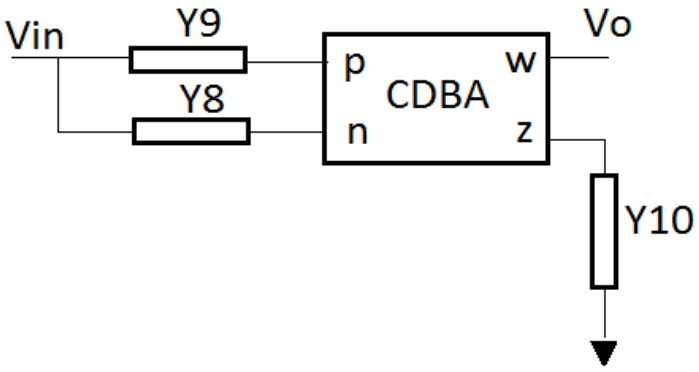

Figure 6.2 Realization of an integrator using CDBA

The transfer function thus obtained for the above configuration is given by:

$$\frac{V_o}{V_{in}} = \frac{Y_9 - Y_8}{Y_{10}} \quad (6.6)$$

Inverting integrator can be designed using above configuration by selecting the appropriate components. For that the following G and C replacements for the admittance of the transfer function given above are done,

$Y_8 = G_8,\ Y_9 = 0, Y_{10} = sC_{11}$

Thus we obtain the required transfer function of an inverting configuration

$$\frac{V_X}{V_{in}} = \frac{-1}{sC_{11}R_8} \tag{6.7}$$

Similarly for obtaining the noninverting integrator following substitutions is to be made:

$Y_8 = 0,\ Y_9 = G_9, Y_{10} = sC_{11}$

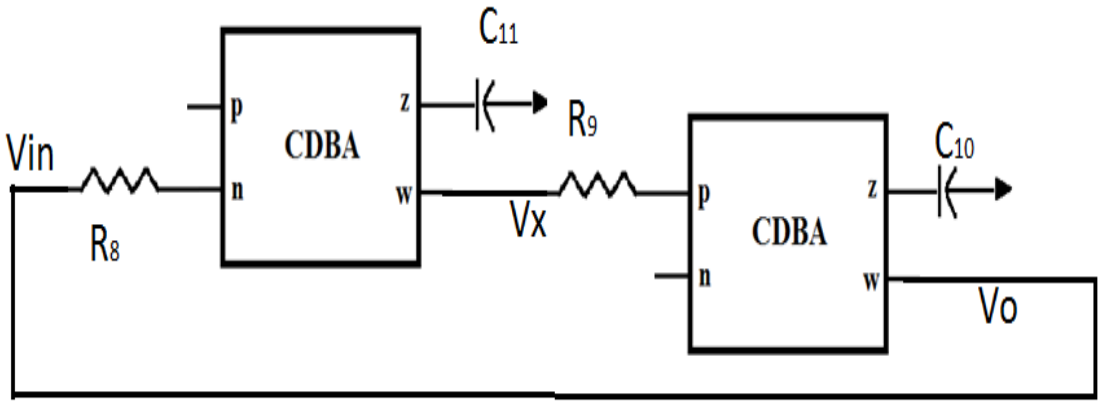

Figure 6.3 Unconditioned quadrature oscillator block diagram

Resulting in following transfer function:

$$\frac{V_o}{V_X} = \frac{1}{sC_{10}R_9} \tag{6.8}$$

The above transfer function also helps us to establish a fact that the two voltages V_o and V_X are always in quadrature phase i.e. the phase shift between V_o and V_X is equal to F = ±90˚.

When two of inverting and noninverting blocks are combined the circuit thus made oscillates in quadrature phase. The combined circuit is shown in figure 6.3.

Therefore overall open loop transfer function of the oscillator circuit thus derived can be expressed by:

$$\frac{V_o}{V_{in}} = \frac{-1}{s^2C_{10}C_{11}R_8R_9} \tag{6.9}$$

And output characteristic equation and the FO are given by:

$$s^2C_{10}C_{11}R_8R_9 + 1 = 0 \tag{6.10}$$

$$FO = \frac{-1}{\sqrt{C_{10}C_{11}R_8R_9}} \tag{6.11}$$

The frequency of oscillation of the circuit can be varied by varying any of the above component values present in the expression for FO. Also due to the absence of the ‘s’ term in the characteristic equation, the circuit thus derived oscillates unconditionally.

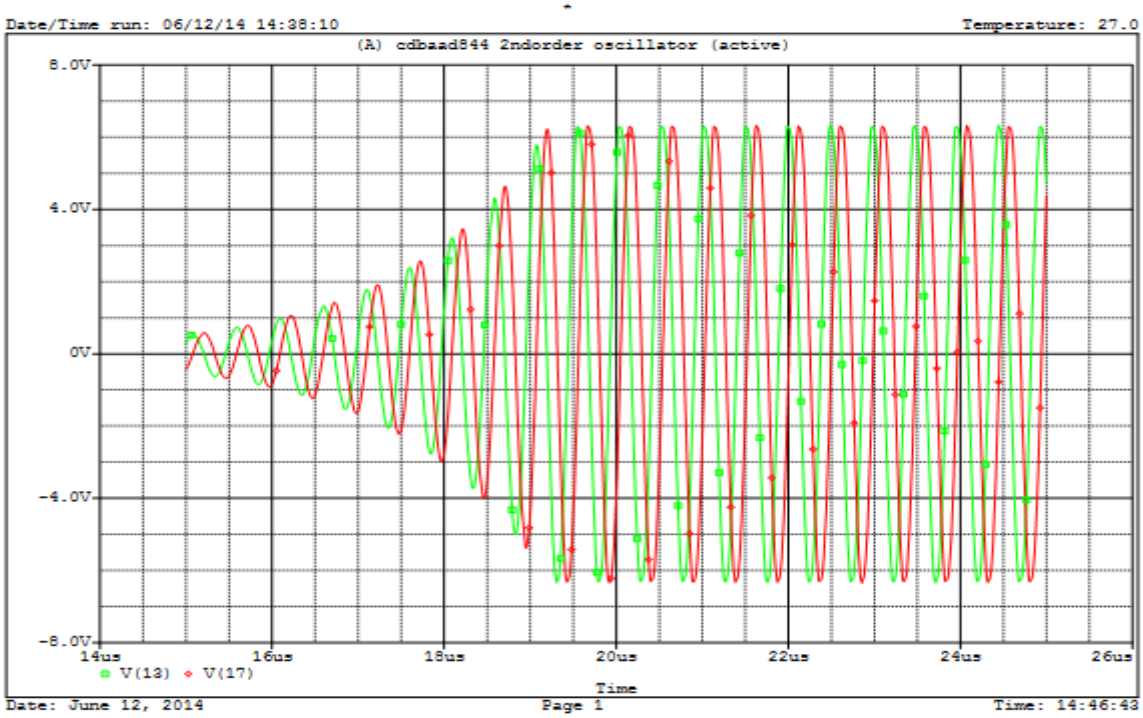

Figure 6.4 Output waveform of the unconditional QO circuit

The circuit thus derived was checked for its feasibility to obtain the desired oscillations which are quadrature in phase using the PSPICE simulations. The CDBA block is made out of commercially available AD844 IC's with supply voltages of ±5V and macro model of these IC's are used for PSPICE simulations.

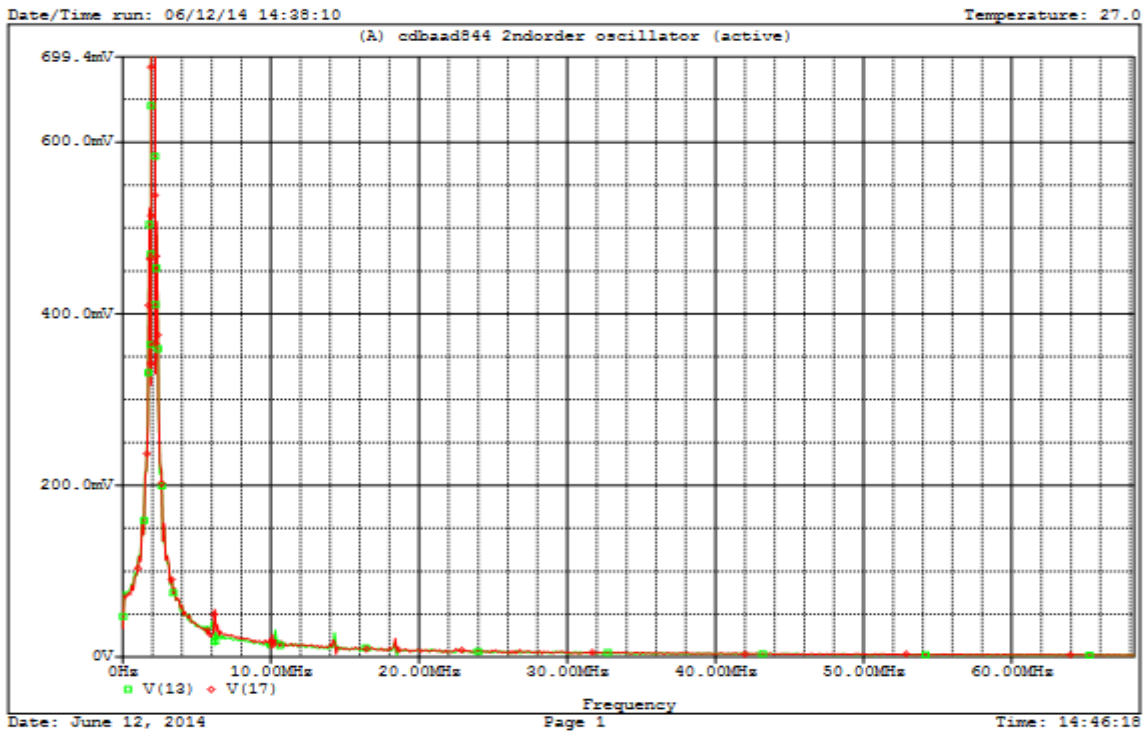

Figure 6.5 Output spectrum of the unconditional QO circuit

The PSPICE simulation was performed to verify the functional behaviour of the circuit. The component values was chosen as C1 = C10 = 100pF and R8 = R9 = 700Ω. The simulated frequency of 2.01 MHz was obtained with a percentage error of 1.35% as compared to that obtained theoretically.

The output waveform for the oscillator derived from circuit 1 showing the build-up of oscillations and steady state output waveform is shown in figure 6.4, which confirms the realization of QOs. Frequency spectrum of the outputs V01 and V02 is displayed in figure 6.5 which shows that the circuit oscillates at 2.01MHz.

6.2. Third Order Quadrature Oscillator

Third order quadrature circuits are characterized by a characteristic equation in which the highest power of the 's' term is equal to three. In the recent scenario there has been a shift to higher order circuits as it has better properties as compared to its second order counterparts. For QO also several designs **[39-43]** are reported which have lower harmonic distortion **[35]**, have better accuracy and frequency response when compared to second order QO circuits. Also the sine wave and multiple phase frequency outputs of the third-order oscillator are of high quality factor (*Q*) and high-purity.

Along with certain advantages the third order circuits has the disadvantage of using more number of active and passive components than the second order circuits i.e. second order circuits have the advantage of compact realization. Therefore one has to take care of the trade off between the better distortion performance achieved by the third order realization and the compact realization depending on the specific application for which the circuit is going to be used.

Here a third order QO circuit is proposed with the help of CDBA sub circuit blocks which are fit into predefined configurations discussed into various literatures **[44]** for realization of third order QOs. The QO is made using two configurations and PSPICE simulation results to verify its working are presented in sections to follow.

6.2.1. Approach to realize QO Circuit

The third order QO is designed using second order low pass filter and an integrator connected in feedback combination and shown in figure 6.6. The voltage transfer functions of the second-order LPF $T_1(s)$ is of type:

$$T_1(s) = \frac{V_X}{V_{in}} = \frac{\pm K_1}{s^2 + as + c} \tag{6.12}$$

Where,

K_1 and K_2 are the gain constants

a and c are the filter property constants

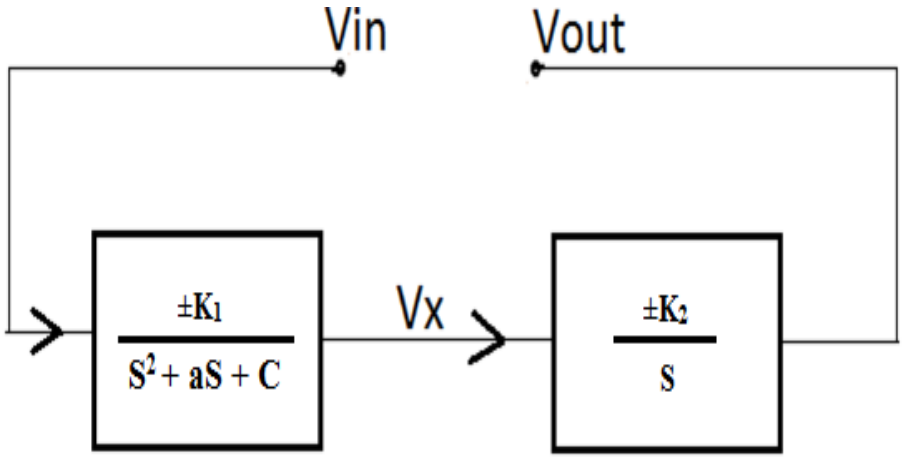

Figure 6.6 Scheme for third order QO

And that for the integrator $T_2(s)$ is assumed to be of the type:

$$T_2(s) = \frac{V_O}{V_X} = \frac{\pm K_2}{s} \tag{6.13}$$

For the oscillator circuit the loop gain can be expressed as:

$$\frac{V_o}{V_{in}} = T_1(s)T_2(s) = \frac{\pm K_1 K_2}{s[s^2 + as + c]} \tag{6.14}$$

As already explained in previous sections the open loop gain of the oscillator needs to be negative, hence either of LPF or integrator works in an inverting configuration i.e. it has a negative gain. Therefore the resultant open loop gain of the oscillator circuit is given by the following equation:

$$\frac{V_o}{V_{in}} = T_1(s)T_2(s) = \frac{-K_1 K_2}{s[s^2 + as + c]} \tag{6.15}$$

Hence the closed-loop characteristic equation is given by:

$$s^3 + as^2 + cs + K_1 K_2 = 0 \tag{6.16}$$

This is the condition which is to be fulfilled to satisfy the Barkhausen criteria [1] i.e. for the circuit to oscillate. To satisfy the above equation both the imaginary and the real part of the equation should be equal to zero separately, which leads to two equations and solving them we can find the CO and FO of the oscillator circuit.

Therefore the CO is:

$$ac = K_1 K_2 \tag{6.17}$$

And the FO is found to be:

$$f_o = \frac{\sqrt{K_1 K_2 / a}}{2\pi} = \frac{\sqrt{c}}{2\pi} \tag{6.18}$$

6.2.2. Generation and Simulation Using CDBA

The above scheme is used to generate the QO circuit, where both inverting and second order LPF are implemented with the help of CDBA active block.

The inverting integrator used for the circuit realization is realized in the same way as was done in section 6.1.2. Therefore using above mentioned configuration, by selecting the appropriate components the needed circuit can be realized. For that the following G and C replacements for the admittance of the transfer function given above are done,

$$Y_8 = G_8,\ Y_9 = 0, Y_{10} = sC_{11}$$

Thus we obtain the required transfer function of an inverting configuration

$$\frac{V_o}{V_{in}} = \frac{-1}{sC_{11}R_8} \tag{6.19}$$

The presence of the inverting integrator block between the two signals of our interest establishes the fact the two signals have a phase shift equal to F = ±90˚ i.e. they oscillate in quadrature phase difference.

Figure 6.7 shows a generalized configuration which can be used for the generation of any type of second order LPF circuit.

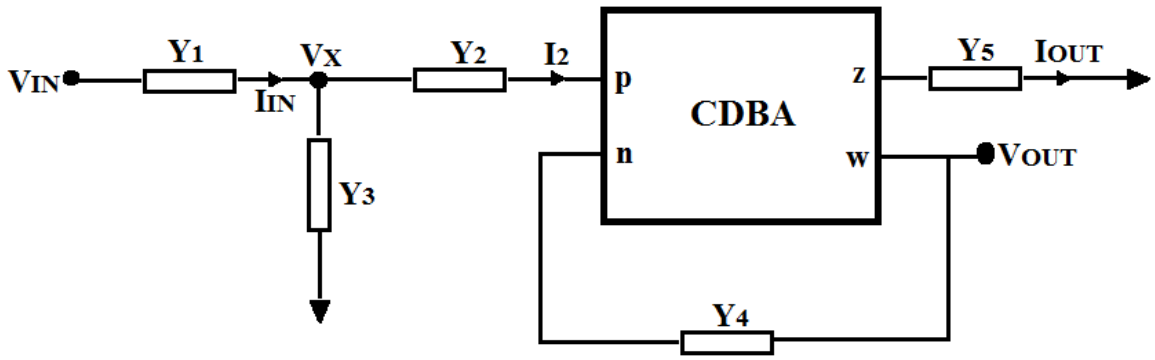

Figure 6.7 Realization of second order LPF using CDBA

The transfer function thus obtained for the above configuration is given by:

$$\frac{V_{OUT}}{V_{IN}} = \frac{Y_1Y_2}{(Y_1+Y_2+Y_3)(Y_4+Y_5)} \tag{6.20}$$

Using the above mentioned topology for LPF realization and selecting the appropriate components two configurations are proposed in preceding section; hence the QO circuit is made and simulated.

6.2.2.1. Using Configuration A

For configuration A, following G and C replacements for the admittance of the transfer function given above are done,

$$Y_1 = G_1,\ Y_2 = G_2, Y_3 = sC_3, Y_4 = G_4,\ Y_5 = sC_5$$

Thus we obtain the following transfer function for the LPF,

$$\frac{V_X}{V_{in}} = \frac{R_4}{(R_1 + R_2 + sCR_1R_2)(sCR_4 + 1)} \tag{6.21}$$

The oscillator circuit constructed using configuration A is shown in figure 6.8

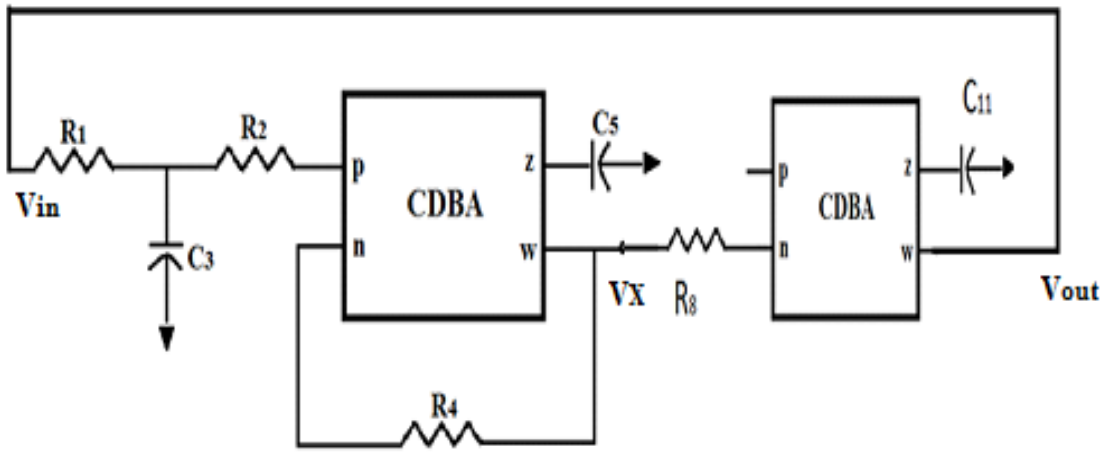

Figure 6.8 Block diagram for configuration A

Here the transfer function for the inverting block is given by:

$$\frac{V_{out}}{V_X} = \frac{-1}{sC_{11}R_8} \tag{6.22}$$

The overall transfer function of the block is thus derived and the characteristic equation made, as done in section 6.2.1 and then the characteristic equation is solved for CO and FO (here all the capacitors are assumed to be of equal value with the aim of simplifying the calculations). The obtained results are given by:

CO,

$$R_4{}^2 = R_8\left(\frac{1}{R_1} + \frac{1}{R_2}\right)(R_4R_2 + R_4R_1 + R_2R_1) \tag{6.23}$$

FO,

$$f_0 = \frac{1}{2\pi C}\sqrt{\frac{R_4}{R_8(R_4R_2 + R_4R_1 + R_2R_1)}} \tag{6.24}$$

Or

$$f_0 = \frac{1}{2\pi C}\sqrt{\frac{1}{R_4}\left(\frac{1}{R_1} + \frac{1}{R_2}\right)} \tag{6.25}$$

From the expressions derived for FO and CO we can see that suitable value of FO can be set by adjusting the values of G_1, G_2, G_4 or C and the CO can be satisfied by proper selection of G_8.

For PSPICE simulations the CDBA block designed using the macro model of AD844 IC's with supply voltages of ±5V is used. The component values was chosen as R1 = R2 = 5K, C3 = C5 = C11 = 100pF and R4 = 22K, R8 = 4K.

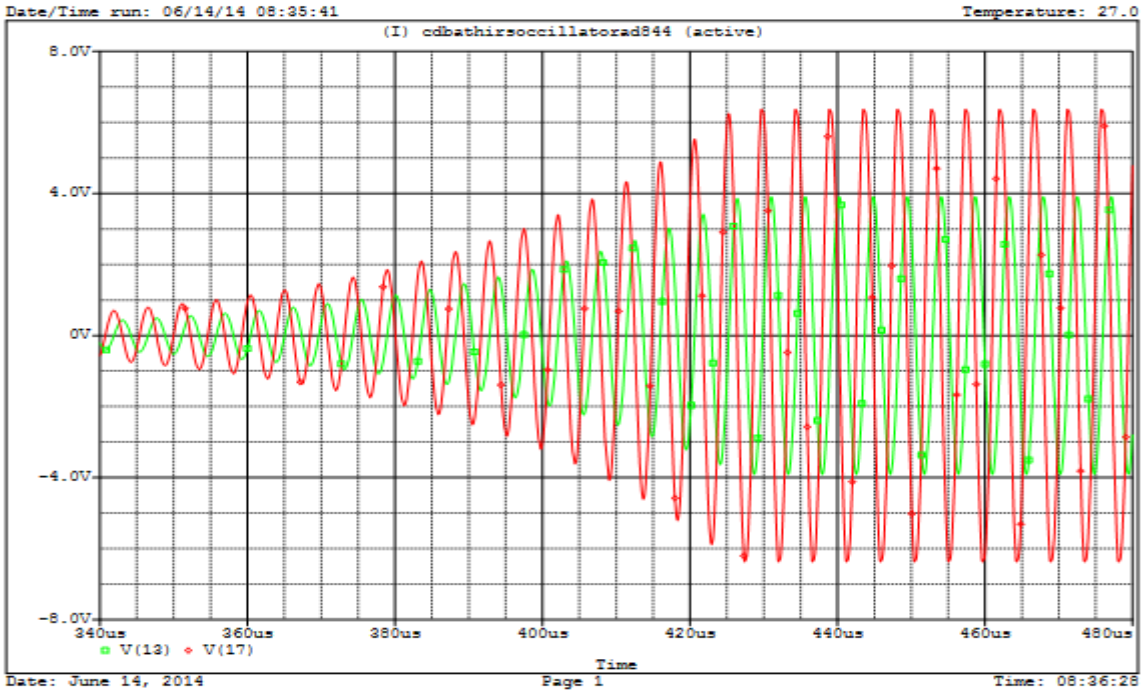

Figure 6.9 Output waveform of the third order QO circuit conf. A

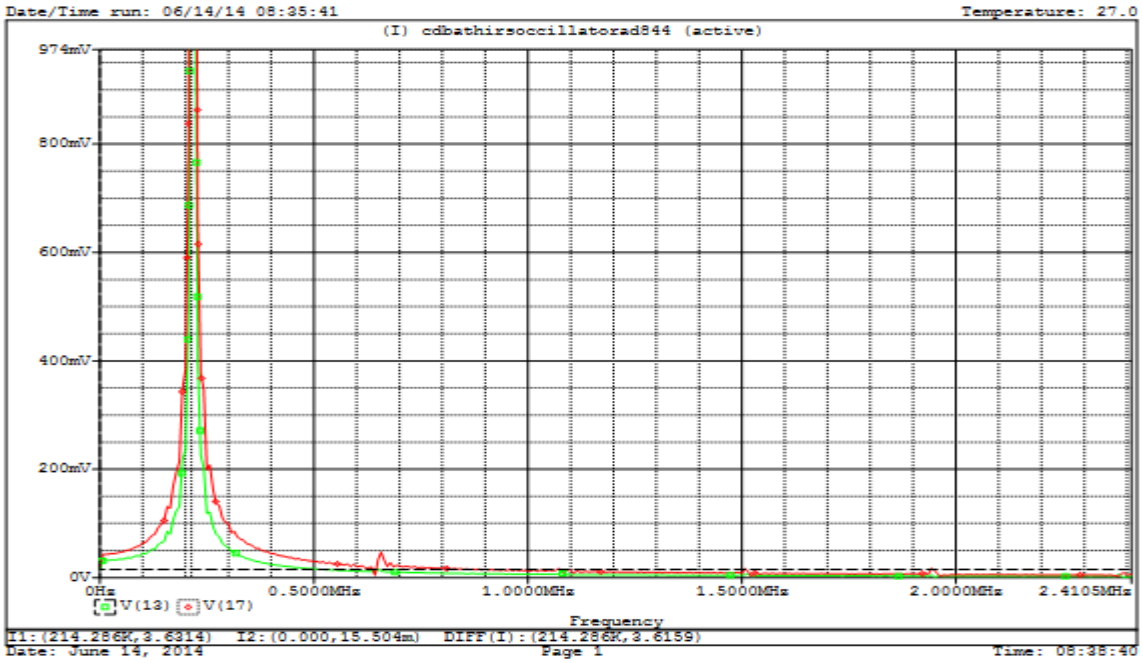

Figure 6.10 Output spectrum of the third order QO circuit conf. A

The build-up of oscillations plus steady state output waveform and output spectrum of required signal are shown in figure 6.9 and 6.10 respectively. The circuit oscillates at 214.2 KHz with a percentage error of 0.18 % as compared to an expected theoretical value of 214.6 KHz.

6.2.2.2. Using Configuration B

For configuration B, following G and C replacements for the admittance of the transfer function given above is done,

$$Y_1 = G_1,\ Y_2 = G_2, Y_3 = sC_3, Y_4 = sC_4,\ Y_5 = G_5$$

Thus we obtain the following transfer function for the LPF,

$$\frac{V_X}{V_{in}} = \frac{R_5}{(R_1 + R_2 + sCR_1R_2)(sCR_5 + 1)} \tag{6.26}$$

The oscillator circuit constructed using configuration A is shown in figure 6.11

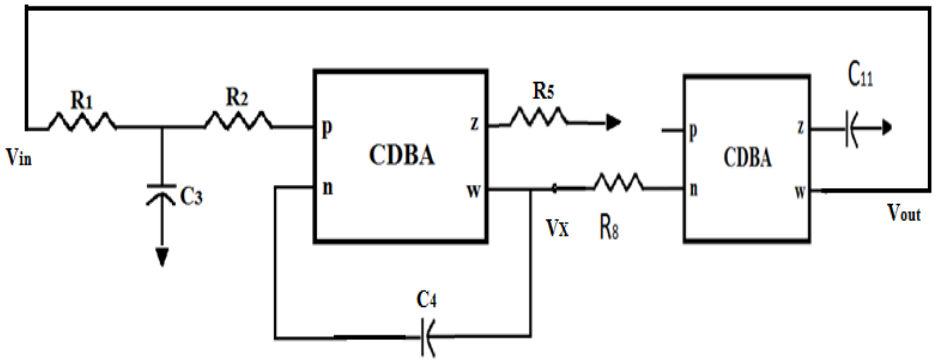

Figure 6.11 Block diagram for configuration B

Here the transfer function for the inverting block is given by:

$$\frac{V_{out}}{V_X} = \frac{-1}{sC_{11}R_8} \tag{6.27}$$

The overall transfer function of the block is thus derived and the characteristic equation made, as done in section 6.2.1 and then the characteristic equation is solved for CO and FO (here all the capacitors are assumed to be of equal value with the aim of simplifying the calculations). The obtained results are given by:

CO,

$$R_5{}^2 = R_8\left(\frac{1}{R_1} + \frac{1}{R_2}\right)(R_5R_2 + R_5R_1 + R_2R_1) \tag{6.28}$$

FO,

$$f_0 = \frac{1}{2\pi C}\sqrt{\frac{R_5}{R_8(R_5R_2 + R_5R_1 + R_2R_1)}} \tag{6.29}$$

Or

$$f_0 = \frac{1}{2\pi C}\sqrt{\frac{1}{R_5}\left(\frac{1}{R_1}+\frac{1}{R_2}\right)} \qquad (6.30)$$

Here also the FO and CO can be suitably set by varying the component values used for realization

For PSPICE simulations the CDBA block designed using the macro model of AD844 IC's with supply voltages of ±5V is used. The component values are chosen as R1 = R2 = 5K, C3 = C4 = C11 = 100pF, R5 = 22K, R8 = 4K.

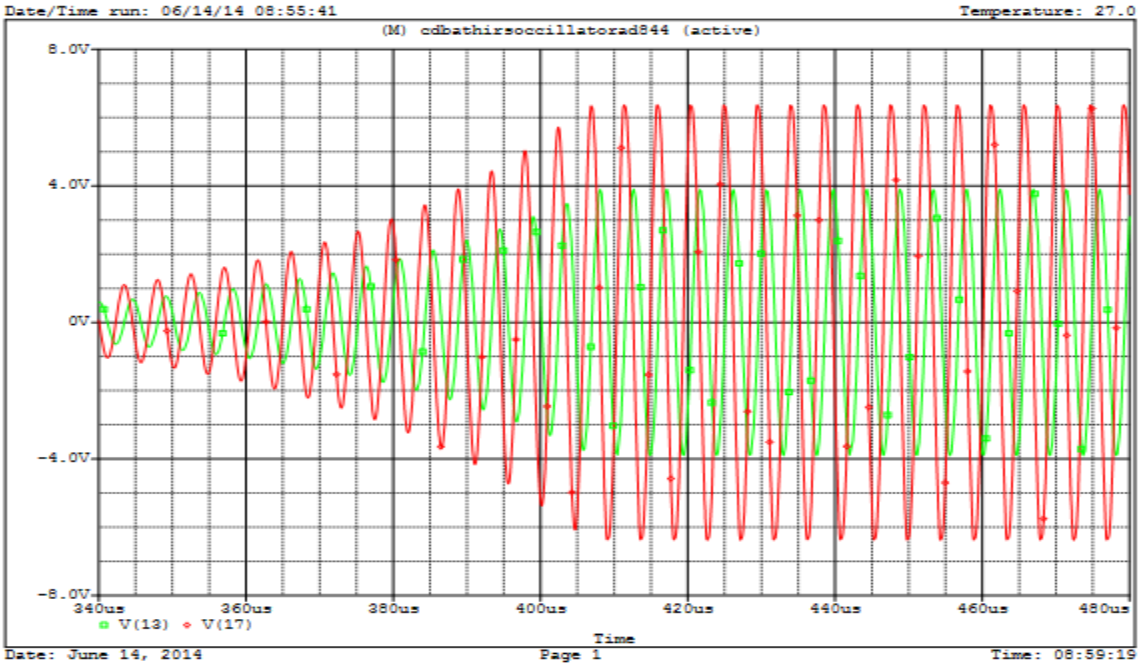

Figure 6.12 Output waveform of the third order QO circuit conf. B

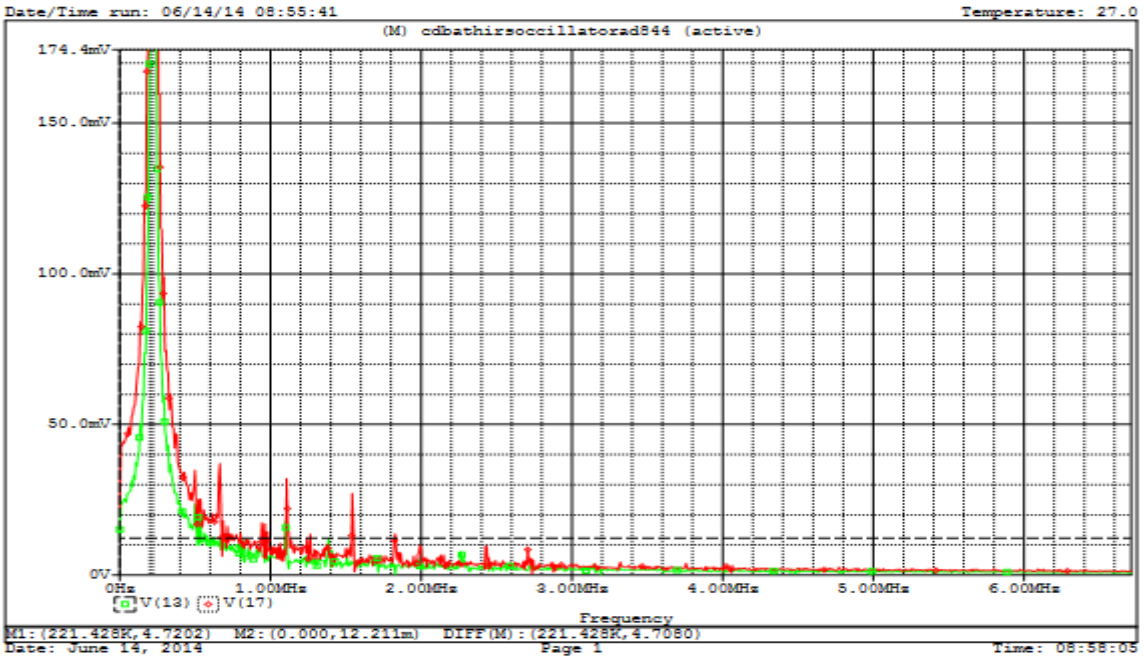

Figure 6.13 Output spectrum of the third order QO circuit conf. B

The build-up of oscillations plus steady state output waveform and output spectrum of required signal are shown in figure 6.12 and 6.13 respectively which shows that the circuit oscillates at 221.4 KHz with a percentage error of 3.16 % as compared to an expected theoretical results of 214.6 KHz.

6.3.Multiphase sinusoidal Oscillator

Multi phase sinusoidal oscillator (MSOs) is a type of oscillator circuit which is capable of producing multiple outputs i.e. multiple sinusoidal waves. These waves have some specific phase difference between them in time domain. MSO finds its extensive application in communication systems where they are used in SSB generators, quadrature mixtures and phase modulators. Other areas of its usage include power electronics, measurement systems, signal processing etc. Various conventional active blocks are proposed in literature to design N-phase MSO but most of them are CM. CDBA being CM active block with one of its output as voltage can be employed for designing VM MSO. Many applications of MSO require highly precise processes.

Here a n-phase MSO circuit is proposed with the help of CDBA sub circuit blocks which are fit into predefined configurations discussed into various literatures [19, 45] for realization of n-phase MSOs. The MSO is made using the discussed configuration and PSPICE simulation results to verify its working are presented in sections to follow.

6.3.1. Approach to realize MSO Circuit

The proposed MSO topology is shown in figure 6.14. It consists of cascaded all pass sections which are n in number to provide outputs, each having a phase difference of 180˚/n. The output voltage V_n of the *n*th stage is fed back to the input of the first stage through the voltage amplifier. Note that the voltage amplifier performing a feedback path has the gain of $-K_2$ i.e. its works as and inverting amplifier.

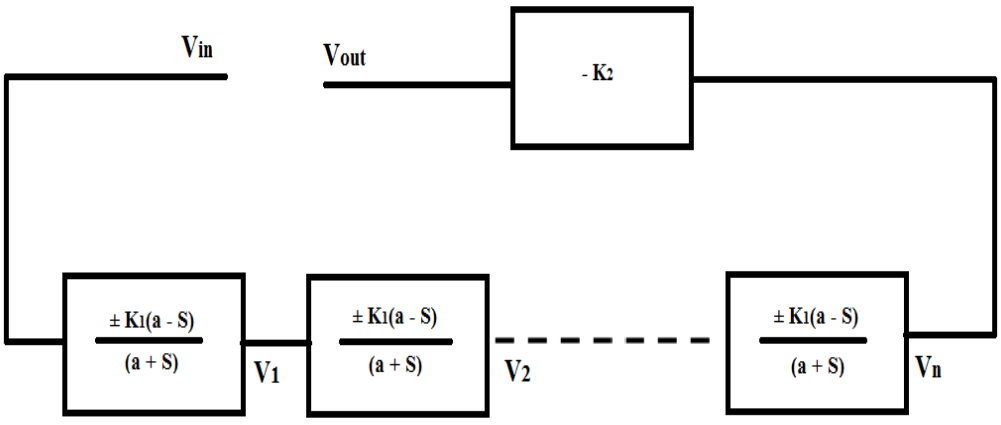

Figure 6.14 Scheme for MSO

The voltage transfer function for the all pass filter is of the type,

$$T_1(s) = \frac{\pm K_1(a-s)}{(a+s)} \quad (6.31)$$

And that of the inverter is assumed to be of the type,

$$T_2(s) = -K_2 \quad (6.32)$$

Where,

K_1 and K_2 the gain constants

a the filter constant

For the oscillator circuit n such filters and a inverter is connected in feedback thus we get the following open loop transfer function of the oscillator thus realized using such configuration,

$$\frac{V_o}{V_{in}} = T_1(s)^n T_2(s) = \pm {K_1}^n K_2 \left(\frac{(a-s)}{(a+s)}\right)^n \quad (6.33)$$

As already explained in previous sections the open loop gain of the oscillator needs to be negative, hence voltage amplifier works in an inverting configuration i.e. it has a negative gain. Therefore the resultant open loop gain of the oscillator circuit is given by the following equation:

$$\frac{V_o}{V_{in}} = T_1(s)^n T_2(s) = -{K_1}^n K_2 \left(\frac{(a-s)}{(a+s)}\right)^n \quad (6.34)$$

Hence the closed-loop characteristic equation is given by:

$$(a+s)^n + {K_1}^n K_2 (a-s)^n = 0 \quad (6.35)$$

According to Barkhausen criteria **[1]** this is the condition to be satisfied for the circuit to oscillate and provide us with n-phase voltage-output signals (n= 3, 4, 5,……) equally spaced in phase. If we substitute for n=3 and find the FO and CO for the above circuit we get following results.

Now the characteristic equation is

$$(a+s)^3 + {K_1}^3 K_2 (a-s)^3 = 0 \quad (6.36)$$

CO,

$${K_1}^3 K_2 = 1 \quad (6.37)$$

And FO is,

$$f_o = \frac{a}{\pi\sqrt{12}} \quad (6.38)$$

6.3.2. Generation and Simulation Using CDBA

The above scheme is used to generate the MSO circuit, where both all pass filter and voltage amplifier are implemented with the help of CDBA active block. Figure 6.15 shows the topology used for the realization of all pass filter using CDBA active block. The transfer function thus obtained is given by,

$$\frac{V_{out}}{V_{in}} = \frac{R_2}{R_1}\left(\frac{1-sC_4R_1}{2+sC_3R_2}\right) \tag{6.39}$$

For that the following G and C replacements for the components of the transfer function,

$R_1 = \frac{R_2}{2} = R, C_3 = C_4 = C.$

Resulting transfer function is obtained

$$\frac{V_{out}}{V_{in}} = \left(\frac{1-sCR}{1+sCR}\right) \tag{6.40}$$

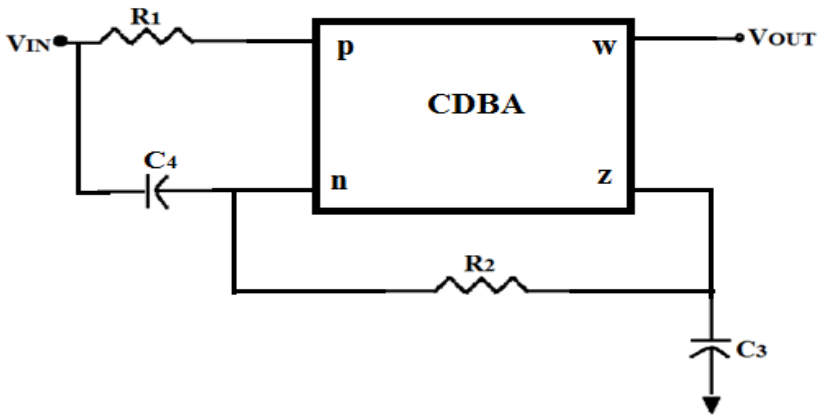

Figure 6.15 All pass filter using CDBA **[14]**

Also figure 6.16 shows the configuration used for implementation of a voltage amplifier which has a negative gain.

Figure 6.16 Voltage inverter using CDBA

The transfer function for the above block is given by,

$$\frac{V_{out}}{V_{in}} = -\frac{R_4}{R_3} \tag{6.41}$$

For that the following G and C replacements for the components of the transfer function,

$R_3 = R_a, R_4 = R$

Resulting transfer function is obtained

$$\frac{V_{out}}{V_{in}} = -\frac{R}{R_a} = -K \tag{6.42}$$

The n-phase MSO circuit is thus devised by using n such all pass filter and inverter in a feedback configuration as explained earlier in section 6.3.1. The overall configuration for MSO with 3-phase voltage-output signals equally spaced in phase with a phase difference of F=60° is shown in figure 6.17.

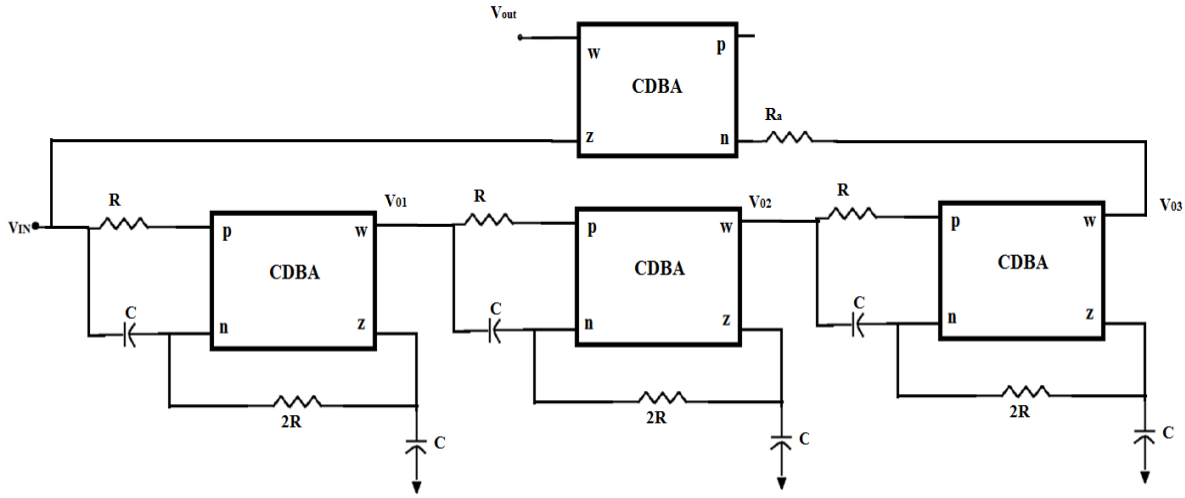

Figure 6.17 Realized MSO using CDBA

Therefore overall open loop transfer function of the oscillator circuit thus derived can be expressed by,

$$\frac{V_{out}}{V_{in}} = -K\left(\frac{1-sCR}{1+sCR}\right)^3 \tag{6.43}$$

The output characteristic equation is obtained and solved for CO and FO. These are shown in subsequent three equations and as observed the frequency of oscillation can be varied by varying the R and C component values.

$$(1+sCR)^3 + K(1-sCR)^3 = 0 \tag{6.44}$$

CO,

$$K = 1 \tag{6.45}$$

And FO,

$$f_o = \frac{1}{\pi\sqrt{12}RC} \tag{6.46}$$

The circuit thus derived was checked for its feasibility to obtain the desired oscillations which are spaced equally in phase using simulations. For PSPICE simulations the CDBA block designed using the macro model of AD844 IC's with supply voltages of ±5V is

used. The component values was chosen as C = 1nF, R = 2K and Ra = 1KΩ. The simulated frequency of 38.235 KHz was obtained with a percentage error of 16.77% as compared to that obtained theoretically. The output waveform for the oscillator derived from circuit in figure 6.17 showing the build-up of oscillations and steady state output waveform is shown in figure 6.18, which confirms the realization of MSO. Frequency spectrum of the outputs V01, V02 and V03 is displayed in figure 6.19 which shows that the circuit oscillates at 38.235 KHz.

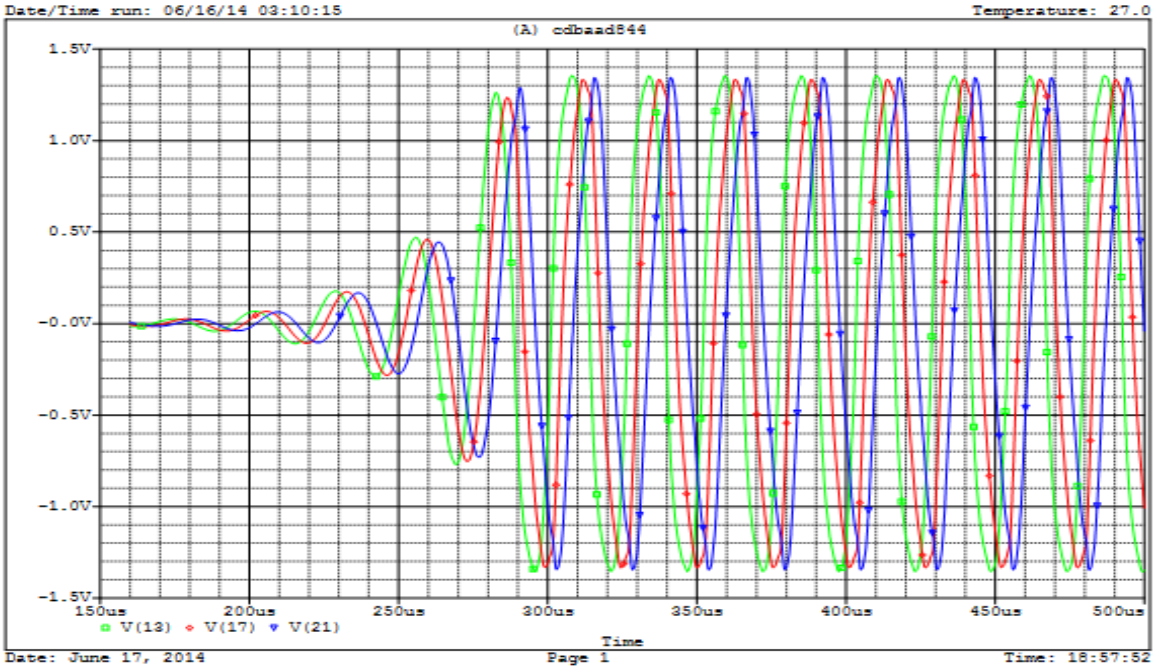

Figure 6.18 Output waveforms for MSO

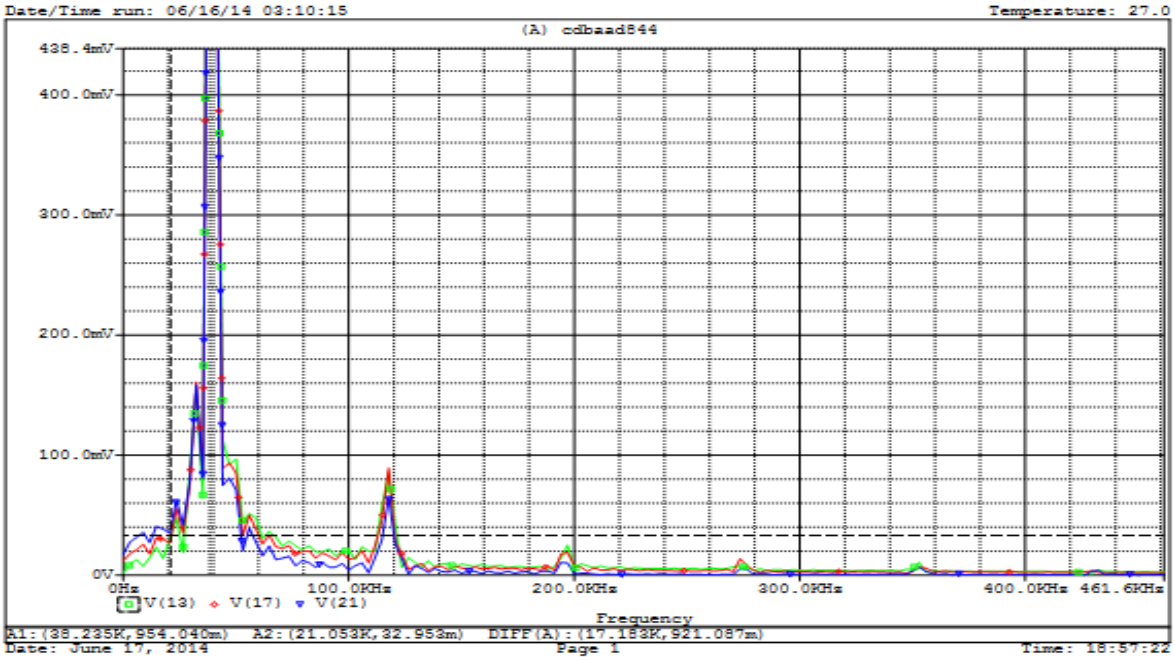

Figure 6.19 Output spectrum for MSO

Chapter 7: Hardware Implementation of QO

The functionality of the proposed third order QO circuit of figure 6.8 is verified experimentally as well. The LPF and integrator block is realized using CDBA which itself is realized using commercially available AD844N IC with supply voltages of ±5V. Figure 7.1 shows the picture of the hardware implementation of the proposed QO circuit.

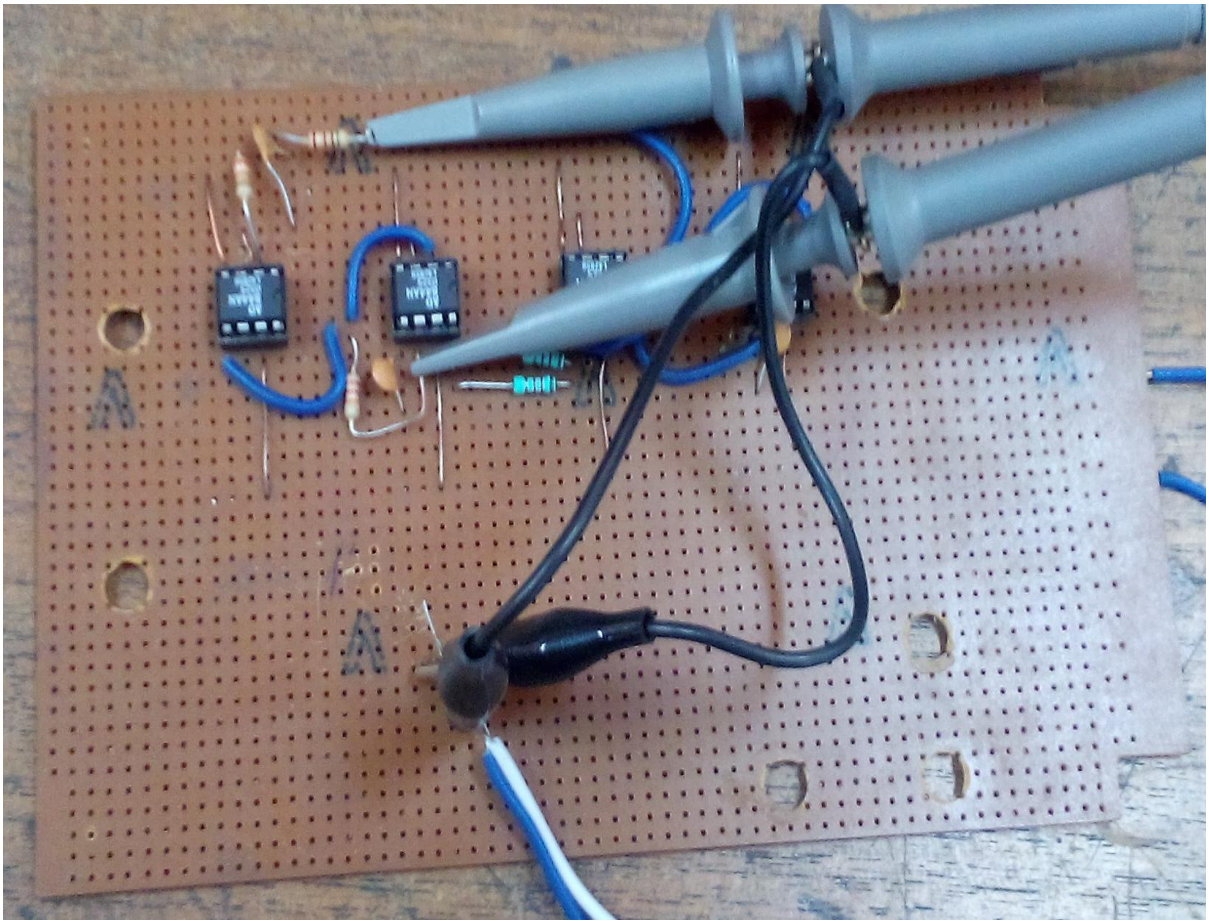

Figure 7.1 Hardware for the proposed QO circuit

The proposed circuit is verified for two different values of capacitance values whereas rest all the components are kept constant. The component values are chosen as $R_1 = R_2 = 5.1K, R_4 = 22K, R_8 = 4.1K, C_3 = C_5 = C_{11} = C$.

Figure 7.2 and 7.3 show the output waveform and output spectrum respectively for the experimented circuit with value of capacitance C = 100pF. As observed the waveforms are quadrature in phase and the frequency of oscillations is 217.83 KHz against a computed value of 214.6 KHz i.e. a percentage error of 1.5 %.

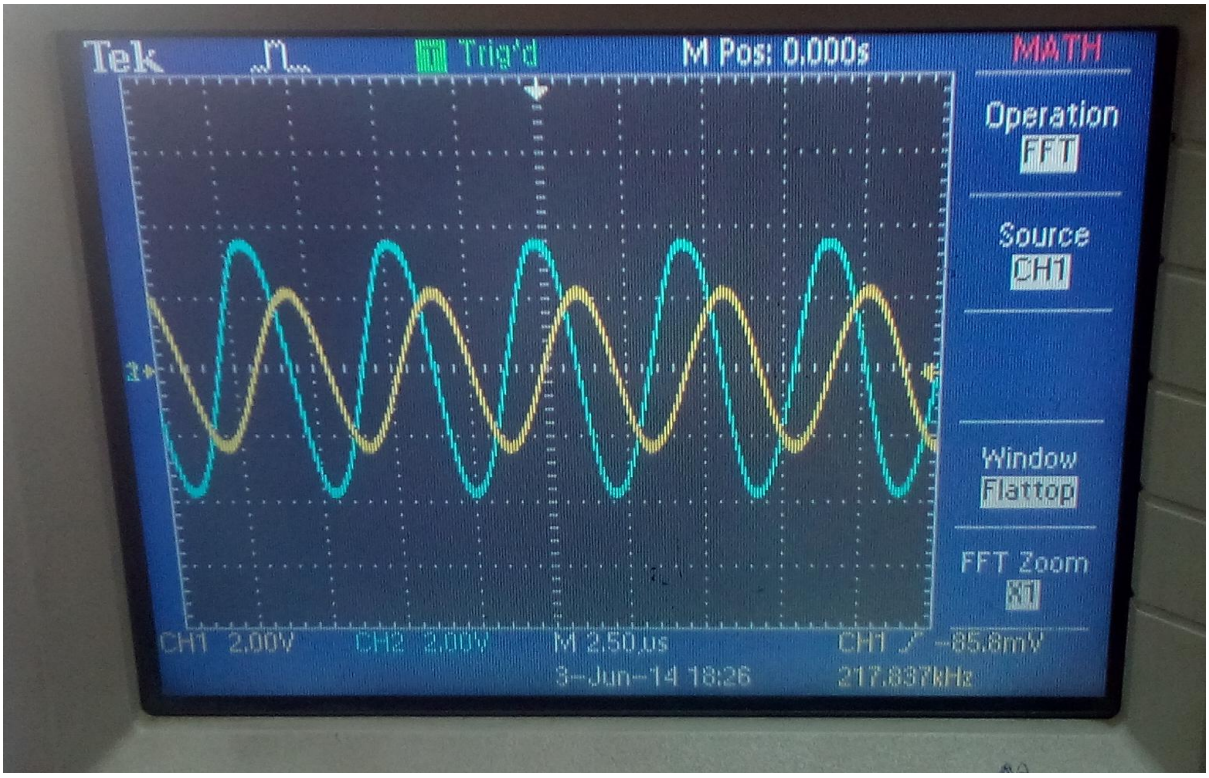

Figure 7.2 Output voltage waveform for QO with C = 100pF

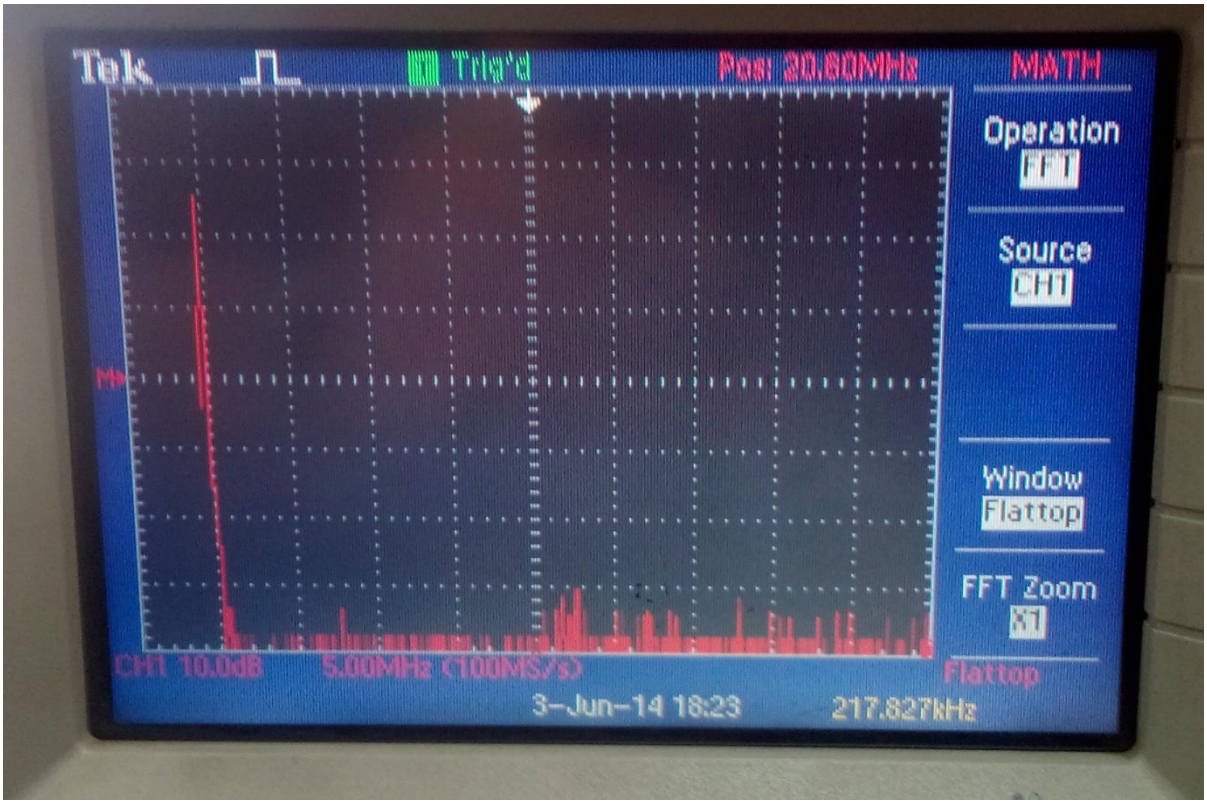

Figure 7.3 Output spectrum for QO with C = 100pF

Another screen shots shown in figures 7.4 and 7.5 respectively show the output waveform and output spectrum for the experimented circuit with value of capacitance C = 200pF.

As observed the waveforms have a phase difference equal to F = ±90˚ and the frequency of oscillations is 100.23 KHz, where theoretical value of the frequency of oscillation is 106.24 KHz i.e. a percentage error of 5.66 %.

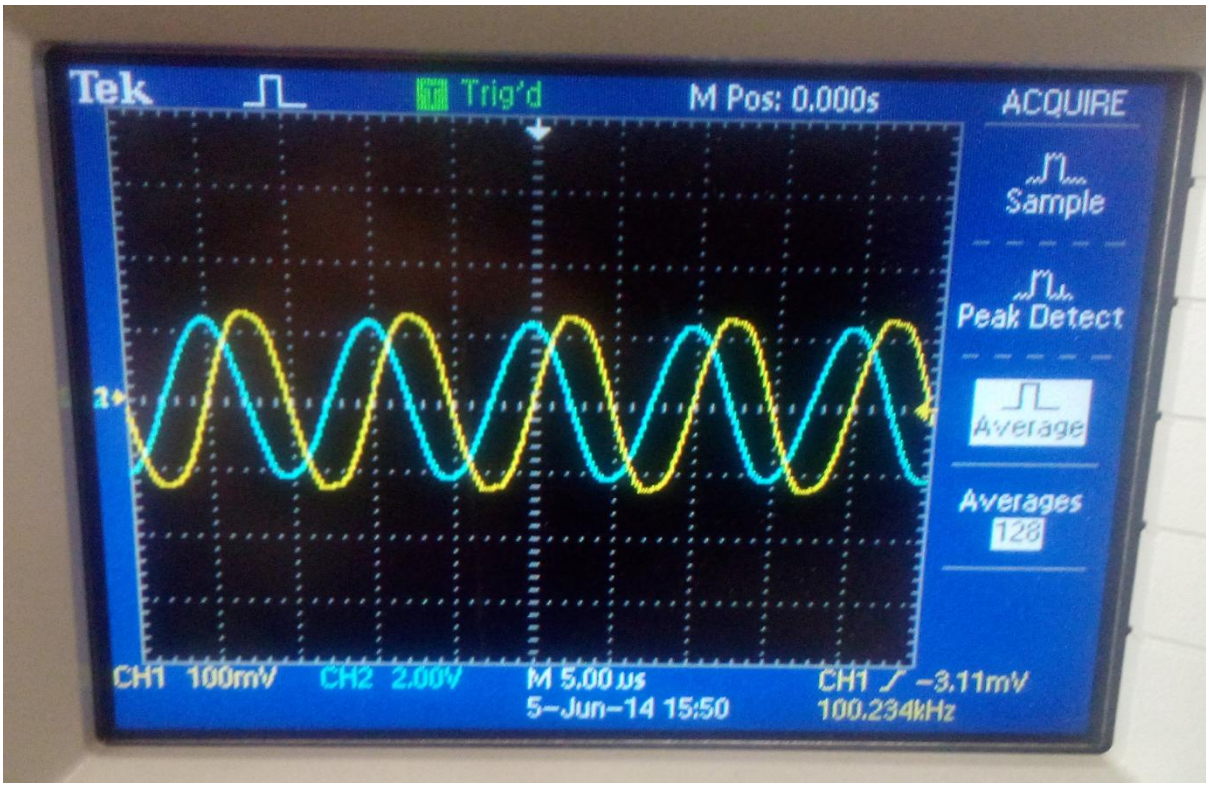

Figure 7.4 Output voltage waveform for QO with C = 200pF

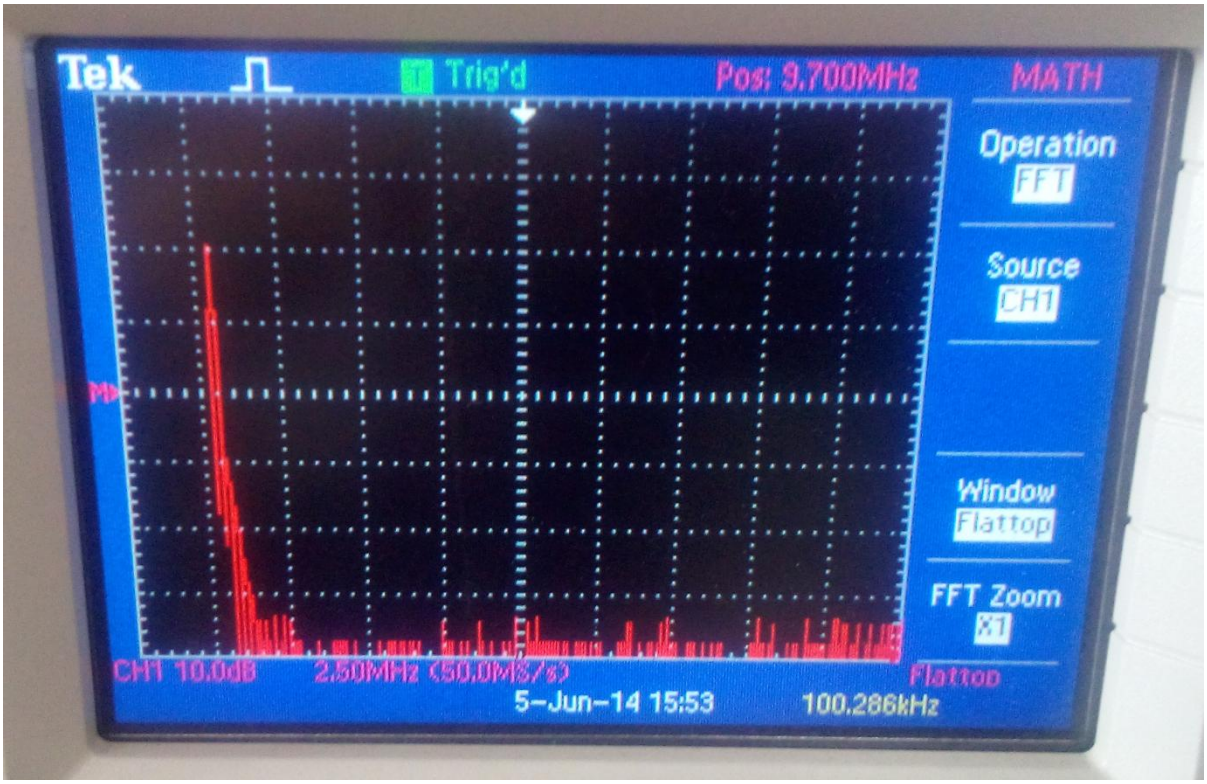

Figure 7.5 Output spectrum for QO with C = 200pF

Chapter 8: Conclusion

In this work ways to realize CDBA (a mixed mode active block) are studied. The block designed performed satisfactorily for both the realizations (AD844 IC and LVLP). The applications designed using the block are rebuilt for verification of the block. Frequencies obtained from signal generators are within the range of ±5% as compared to that calculated theoretically.

Systematic approaches to synthesize three new circuits, which are integrator based QOs, third order QOs and Multiphase sinusoidal oscillators are presented. These approaches are used to yield the respective circuits using CDBA. The proposed circuits are verified for their working using PSPICE simulations and the error percentage found in the frequency of oscillations was within ±4%. The third order QO was verified using hardware implementation as well. The experiment was performed for two different set of values of passive components and the screen shots of oscilloscope are presented.

The CDBA was implemented using the available AD844N IC (from Analog Devices Inc.). CDBA is not yet available commercially, AD844N was the only choice as CFOAs from other manufacturers such as CLC-400/401 from National Semiconductors and MAX 4223-4228 from MAX Corporation does not provide Z-terminal as an externally accessible pin which is required for the implementation of CDBA using CFOA's. This can be taken as one of the limitations of the proposed circuits for the current being, as soon as the CDBA becomes available commercially as an off-the-shelf IC it can be directly used for the implementation of all the above proposed circuits and the required results can be obtained.

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APPENDIX (A)

AD844 IC - 60 MHz, 2000 V/µs, Monolithic Op Amp

The AD844 is a high speed monolithic operational amplifier fabricated using Analog Device's junction isolated complementary bipolar (CB) process. It combines high bandwidth and very fast large signal response with excellent dc performance. Although optimized for use in current-to-voltage applications and as an inverting mode amplifier, it is also suitable for use in many non inverting applications.

The AD844 can be used in place of traditional op amps, but its current feedback architecture results in much better ac performance, high linearity, and an exceptionally clean pulse response.

This type of op amp provides a closed-loop bandwidth that is determined primarily by the feedback resistor and is almost independent of the closed-loop gain. The AD844 is free from the slew rate limitations inherent in traditional op amps and other current-feedback op amps. Peak output rate of change can be over 2000 V/µs for a full 20 V output step. Settling time is typically 100 ns to 0.1%, and essentially independent of gain. The AD844 can drive 50 Ω loads to ±2.5 V with low distortion and is short circuit protected to 80 mA.

The AD844 is available in four performance grades and three package options. In the 16-lead SOIC (R) package, the AD844J is specified for the commercial temperature range of 0°C to 70°C.The AD844A and AD844B are specified for the industrial temperature range of –40°C to +85°C and are available in the CERDIP (Q) package. The AD844A is also available in an 8-lead PDIP (N). The AD844S is specified over the military temperature range of –55°C to +125°C. It is available in the 8-lead CERDIP (Q) package.

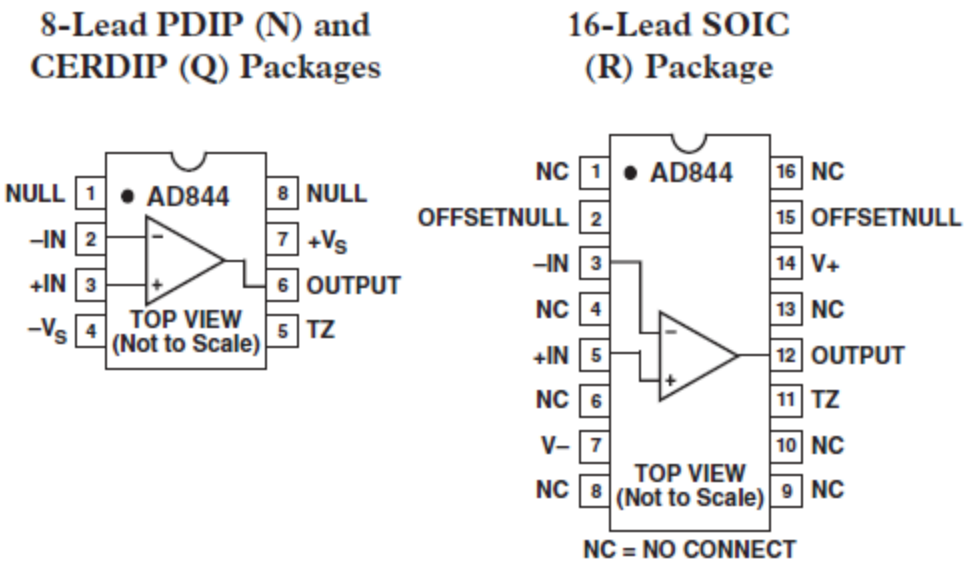

Figure A Connection diagram **[46]**

PRODUCT HIGHLIGHTS:

1. The AD844 is a versatile, low cost component providing an excellent combination of ac and dc performance.
2. It is essentially free from slew rate limitations. Rise and fall times are essentially independent of output level.
3. The AD844 can be operated from ±4.5 V to ±18 V power supplies and is capable of driving loads down to 50 Ω, as well as driving very large capacitive loads using an external network.
4. The offset voltage and input bias currents of the AD844 is laser trimmed to minimize dc errors; VOS drift is typically 1 μV/°C and bias current drift is typically equal to 9nA/°C.
5. The AD844 exhibits excellent differential gain and differential phase characteristics, making it suitable for a variety of video applications with bandwidths up to 60 MHz.
6. The AD844 combines low distortion, low noise, and low drift with wide bandwidth, making it outstanding as an input amplifier for flash A/D converters.

FEATURES:

Wide Bandwidth: 60 MHz at Gain of –1

Wide Bandwidth: 33 MHz at Gain of –10

Very High Output Slew Rate: Up to 2000 V/μs

20 MHz Full Power Bandwidth, 20 V p-p, R_L = 500Ω

Fast Settling: 100 ns to 0.1% (10 V Step)
Differential Gain Error: 0.03% at 4.4 MHz
Differential Phase Error: 0.158 at 4.4 MHz
Low Offset Voltage: 150 mV Max (B Grade)
Low Quiescent Current: 6.5 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ABSOLUTE MAXIMUM RATINGS:

Supply Voltage: ±18 V
Power Dissipation: 1.1 W for
8-Lead PDIP Package at θ_{JA} = 90°C/W.
8-Lead CERDIP Package at θ_{JA} = 110°C/W.
Output Short Circuit Duration: Indefinite
Common-Mode Input Voltage: ±VS
Differential Input Voltage: 6 V
Inverting Input Current
Continuous: 5 mA
Transient: 10 mA
Storage Temperature Range (Q): –65°C to +150°C
Storage Temperature Range (N, R): –65°C to +125°C
Lead Temperature Range (Soldering 60 sec): 300°C
ESD Rating: 1000 V

APPLICATIONS:

Flash ADC Input Amplifiers
High Speed Current DAC Interfaces
Video Buffers and Cable Drivers
Pulse Amplifiers

APPENDIX (B)

0.18 µm, level 7 parameters provided by TSMC for NMOS

```
LEVEL   = 7

+DSUB    = 0.0217897     + TNOM    = 27            TOX     = 4.1E-9
+XJ      = 1E-7                  NCH     = 2.3549E17       VTH0    = 0.3750766
+K1      = 0.5842025       K2      = 1.245202E-3     K3      = 1E-3
+K3B     = 0.0295587       W0      = 1E-7                  NLX     = 1.597846E-7
+DVT0W   = 0               DVT1W   = 0               DVT2W   = 0
+DVT0    = 1.3022984       DVT1    = 0.4021873       DVT2    = 7.631374E-3
+U0      = 296.8451012     UA      = -1.179955E-9    UB      = 2.32616E-18
+UC      = 7.593301E-11    VSAT    = 1.747147E5      A0      = 2
+AGS     = 0.452647        B0      = 5.506962E-8     B1      = 2.640458E-6
+KETA    = -6.860244E-3            A1      = 7.885522E-4     A2      = 0.3119338
+RDSW    = 105             PRWG    = 0.4826          PRWB    = -0.2
+WR      = 1                     WINT    = 4.410779E-9     LINT    = 2.045919E-8
+XL      = 0                     XW      = -1E-8                 DWG     = -2.610453E-9
+DWB     = -4.344942E-9            VOFF    = -0.0948017      NFACTOR = 2.1860065
+CIT     = 0                     CDSC    = 2.4E-4          CDSCD   = 0
+CDSCB   = 0               ETA0    = 1.991317E-3     ETAB    = 6.028975E-5
+DSUB    = 0.0217897       PCLM    = 1.7062594       PDIBLC1 = 0.2320546
+PDIBLC2 = 1.670588E-3             PDIBLCB = -0.1            DROUT   = 0.8388608
+PSCBE1  = 1.904263E10             PSCBE2  = 1.546939E-8             PVAG    = 0
+DELTA   = 0.01            RSH     = 7.1                   MOBMOD  = 1
+PRT     = 0                     UTE     = -1.5                  KT1     = -0.11
+KT1L    = 0                     KT2     = 0.022                 UA1     = 4.31E-9
+UB1     = -7.61E-18       UC1     = -5.6E-11                AT      = 3.3E4
+WL      = 0                     WLN     = 1                     WW      = 0
+WWN     = 1               WWL     = 0                     LL      = 0
+LLN     = 1                     LW      = 0                     LWN     = 1
+LWL     = 0                     CAPMOD  = 2               XPART   = 0.5
+CGDO    = 6.7E-10         CGSO    = 6.7E-10         CGBO    = 1E-12
+CJ      = 9.550345E-4     PB      = 0.8                   MJ      = 0.3762949
+CJSW    = 2.083251E-10            PBSW    = 0.8                   MJSW    = 0.1269477
+CJSWG   = 3.3E-10         PBSWG   = 0.8             MJSWG   = 0.1269477
+CF      = 0                     PVTH0   = -2.369258E-3            PRDSW   = -1.2091688
+PK2     = 1.845281E-3     WKETA   = -2.040084E-3            LKETA   = -1.266704E-3
+PU0     = 1.0932981       PUA     = -2.56934E-11    PUB     = 0
+PVSAT   = 2E3             PETA0   = 1E-4            PKETA   = -3.350276E-3    )
```

0.18 µm, level 7 parameters provided by TSMC for PMOS

```
  LEVEL   = 7

+ TNOM    = 27            TOX     = 4.1E-9
+XJ   = 1E-7                      NCH     = 4.1589E17             VTH0    = -0.3936726
+K1   = 0.5750728                 K2      = 0.0235926             K3      = 0.1590089
+K3B= 4.2687016                   W0      = 1E-6                  NLX     = 1.033999E-7
+DVT0W   = 0             DVT1W   = 0                     DVT2W   = 0
+DVT0 = 0.5560978                 DVT1    = 0.2490116             DVT2    = 0.1
+U0= 112.5106786                  UA      = 1.45072E-9    UB      = 1.195045E-21
+UC      = -1E-10        VSAT    = 1.168535E5    A0      = 1.7211984
+AGS     = 0.3806925     B0      = 4.296252E-7   B1      = 1.288698E-6
+KETA    = 0.0201833     A1      = 0.2328472     A2      = 0.3
+RDSW    = 198.7483291           PRWG    = 0.5                   PRWB    = -0.4971827
+WR      = 1                     WINT    = 0                     LINT    = 2.943206E-8
+XL      = 0                     XW      = -1E-8                 DWG     = -1.949253E-8
+DWB     = -2.824041E-9          VOFF    = -0.0979832    NFACTOR = 1.9624066
+CIT     = 0                     CDSC    = 2.4E-4        CDSCD   = 0
+CDSCB   = 0             ETA0    = 7.282772E-4   ETAB    = -3.818572E-4
+DSUB    = 1.518344E-3           PCLM    = 1.4728931     PDIBLC1 = 2.138043E-3
+PDIBLC2 = -9.966066E-6  PDIBLCB = -1E-3                 DROUT   = 4.276128E-4
+PSCBE1  = 4.850167E10           PSCBE2  = 5E-10         PVAG    = 0
+DELTA   = 0.01          RSH     = 8.2                   MOBMOD  = 1
+PRT     = 0                     UTE     = -1.5                  KT1     = -0.11
+KT1L    = 0                     KT2     = 0.022                 UA1     = 4.31E-9
+UB1     = -7.61E-18     UC1     = -5.6E-11      AT      = 3.3E4
+WL      = 0                     WLN     = 1                     WW      = 0
+WWN     = 1             WWL     = 0                     LL      = 0
+LLN     = 1                     LW      = 0                     LWN     = 1
+LWL     = 0                     CAPMOD  = 2             XPART   = 0.5
+CGDO    = 7.47E-10      CGSO    = 7.47E-10      CGBO    = 1E-12
+CJ      = 1.180017E-3   PB      = 0.8560642     MJ      = 0.4146818
+CJSW    = 2.046463E-10          PBSW    = 0.9123142     MJSW    = 0.316175
+CJSWG   = 4.22E-10              PBSWG   = 0.9123142     MJSWG   = 0.316175
+CF      = 0                     PVTH0   = 8.456598E-4           PRDSW   = 8.4838247
+PK2     = 1.338191E-3   WKETA   = 0.0246885             LKETA   = -2.016897E-3
+PU0     = -1.5089586    PUA     = -5.51646E-11  PUB     = 1E-21
+PVSAT   = 50            PETA0   = 1E-4          PKETA   = -3.316832E-3
```