Chapter-1

INTRODUCTION

1.1 Motivation

Electronic circuit design falls generally into two broad categories: analog and digital. A third category, interface circuitry, considers ways to join these two circuit realms. Digital circuitry uses electronic components and systems to represent and store numerical data and to perform algebraic and logical operations on the data. Complex digital structures are created by combining a few simple circuit building blocks (such as clocks, gates, and registers) into a vast network of components.

Analog circuitry, in contrast, is used to respond to continuously-variable electrical signals from sensors (such as microphones, thermistors, antennas, and accelerometers) or to provide continuously-variable control signals to actuators (such as loudspeakers, heaters, antennas, or motors). Analog circuitry is used, for example, to connect digital computers and circuits to many of the physical devices they use for data I/O and storage. The most important application of analog electronic circuitry is to amplify and filter the power of a minute signal so that it can be accurately measured or used to actuate control systems. There are many type of Electronic circuits i.e. amplifier, filter, oscillator, multivibrators etc.

These electronic circuits can be designed by using different active building blocks. These active blocks are Current Differencing Buffered Amplifier (CDBA), Current Feedback Operational Amplifier (CFOA), Current Controlled Current Conveyor (CCCII), Differential Voltage Current Conveyor (DVCCII) Current Differencing Trans conductance Amplifier (CDTA), Operational Trans conductance Amplifier (OTA), Operational Trans Resistance Amplifier (OTRA) etc. These active blocks find significant applications in analog signal processing.

Among these active building blocks OTRA finds significant importance because it can provide a high bandwidth independent of the gain. Hence, it does not suffer from constant gain bandwidth product like voltage op amps circuits. OTRA is also not slew limited as voltage op-amps.

1.2 Literature Review

The Operational Trans Resistance Amplifier (OTRA) is commercially available at several manufacturers under the name current differencing or Norton amplifier [1-3].These realizations are not widely used as they do not provide internal ground at the input port and they allow the input current to flow in one direction only. The former disadvantage limited the functionality of the OTRA whereas the latter forced to use external dc bias current leading to complex and unattractive designs. In recent years, several high-performance CMOS OTRA realizations have been presented. This leads to growing interest for the design of OTRA-based analog signal processing circuits.

Some of the attractive properties of OTRA are their fast speed in comparison with conventional op-amps. CMOS-OTRA is used in many of application instead of commercial operational amplifiers due to its features such as low power consumption, requirement of very low supply voltage and better result at high frequency. It reduces the zero cross-over distortion as compared to conventional op-amp. With the realization of CMOS-OTRA which is Transresistance amplifiers by which the above features arise results in improvement in multiplier, squarer or in any other circuit characteristics.

OTRA is the basic building block of a number of applications both in current and voltage and mixed modes. The first CMOS circuit of OTRA was introduced in 1992 by J. J.Chen, H. W. Tsao & C. C. Chen [4]. Reference [4] 1995 shows that the input terminals of OTRA being virtually grounded, the circuits designed using OTRA were insensitive to stray capacitances [9]. In 1999 Salama and Ahmed M. Soliman introduced a simple CMOS realization of OTRA based on cascaded connection of modified differential current conveyor (MDCC) and a common source amplifier [5]. In [6] they proposed a new circuit based on same cascaded connection of modified differential current conveyor (MDCC) and a common source amplifier as in [5] but with improved performance and less number of transistors. The Circuit proposed in [6] is based on same input stage of OTRA proposed in [5] and a differential gain stage is used instead of the single common source amplifier and a compensation circuit is used to compensate difference between the two drain voltages of input transistors. The circuit proposed in [7] is another modification of circuit presented in [6] where differential gain stage is used instead of the single common source amplifier. Several other CMOS realizations of

OTRA are also available in literature [11-13]. Circuit presented in [11] consists of a differential current controlled current source (DCCCS) followed by a voltage buffer whereas circuit reported in [12] is made of Rm cell, feedback network and output driver. A low voltage regulated cascade current mirror with a low voltage regulated cascode load forms core of the circuit proposed in [13]. Various applications of OTRA also exist in literature. Filters, Monostable Multivibrator, Analog Multiplier, Squarer using OTRA are designed in chapter-3. In the year 2000 K.N. Salamaa, A.M. Soliman published a paper on oscillators and these designs uses single as well as double OTRA's[14], this is the first paper on RC oscillators using OTRA in the literature.

1.3 Objective and Scope of the Project

The objective of the project is to present a systematic review of the available literature on OTRA, study and implement the existing structures. To meet the objectives an extensive review is carried out and it was observed that the available literature can be classified in following two categories:

1. The OTRA realizations
2. The ORTA based applications

The OTRA based realizations are studied and one of the configurations is characterized through simulations. This structure is utilized for verifying the functionalities of various OTRA based applications studied and implemented in this work.

1.4 Organization of Thesis

The thesis is organized as follows:

Chapter 2

This chapter describes the basics of OTRA and modification of OTRA in chronological order. It further describes its internal circuit structures. Terminal characteristics of these circuits have been verified through PSPICE simulations.

Chapter 3

In this chapter OTRA based filters are implemented. Different type of second order filters (LPF, HPF, BPF and BSF) have been realized using two design approaches. These filters are implemented with PSPICE 0.5 μm technology model.

Chapter 4

In this chapter OTRA based oscillators are implemented. A generic single OTRA based topology is studied and implemented first from which various configurations can be derived. Another oscillator structure having non interactive control on condition and frequency is studied and simulated next. These circuits are insensitive to parasitic input capacitances due to internally grounded terminals of OTRA [3].

Chapter 5

In this chapter OTRA based nonlinear applications i.e. analog multiplier, square, monostable multivibrator are implemented. These applications have specific use in analog signal processing.

Chapter 6

Chapter wise summary is presented in conclusion.

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CHAPTER: 2

OPERATIONAL TRANS-RESISTANCE AMPLIFIER

This chapter describes the basics of OTRA with its importance. Here, CMOS Realization of all types of OTRA is discussed and its simulation results are presented. In chronological order, development of OTRA is shown below in respective manner.

2.1 Basics of OTRA

Operational Trans-resistance Amplifier (OTRA) is a high gain current input, voltage output amplifier [1]. Symbol of OTRA is illustrated in Fig.2.1. OTRA is a three terminal device described by matrix equation:

$$\begin{bmatrix} V_p \\ V_n \\ V_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ I_o \end{bmatrix} \quad (2.1)$$

Where Rm is the transresistance gain.

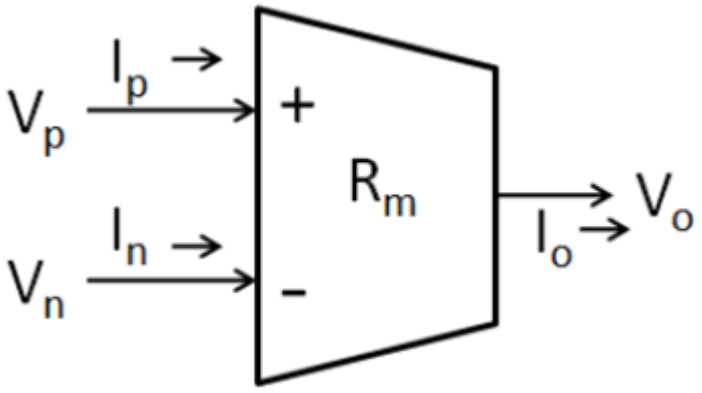

Fig. 2.1 Symbol of OTRA

From the above equation (2.1) it is clear that both input and output terminals are characterized by low impedance, thereby eliminating response limitations incurred by capacitive time constants. The

input terminals are virtually grounded leading to circuits that are insensitive to stray capacitances [4]. Ideally, the transresistance gain, R_m, approaches infinity, and external negative feedback must be used which forces the input currents, I_p and I_n, to be equal [2]. Thus OTRA must be used in a negative feedback configuration. The OTRA is not slew limited in the same fashion as voltage op amps [5]. It can provide a high bandwidth independent of the gain. Hence, it does not suffer from constant gain bandwidth product like voltage op amps circuits. The small signal ac equivalent of the OTRA is shown in the Fig. 2.2. Ideally here both R_{in} and R_{out} values are zero ohm. While value of R_m is ideally infinity.

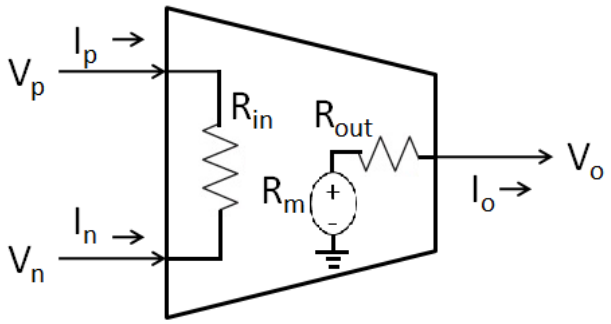

Fig. 2.2 Small Signal AC Equivalent of OTRA

Practically the transresistance gain is finite and its effect should be considered. Also, the frequency limitations associated with OTRA should be considered. Considering a single pole model for the transresistance gain, Rm [2], then:

$$R_m(s) = \frac{R_0}{1+{}^{s}/_{\omega_0}} \tag{2.2}$$

For high frequency applications, the transresistance gain, $R_m(s)$, can be expressed as:

$$R_m(s) \approx \frac{1}{sC_p} \tag{2.3a}$$

Where

$$C_p = \frac{1}{R_0\,\omega_0} \tag{2.3b}$$

where, R_o is DC open loop transresistance gain and C_p is parasitic capacitance.

2.2 The Salama and Soliman OTRA[2]

The CMOS realization of the OTRA [2] is shown in Fig.2.3. It is based on the cascaded connection of the modified differential current conveyor (MDCC) [6] and a common source amplifier [2]. Assuming that each of the groups of the transistors (M1-M3), (M4-M7), (M8 and M9), (M10 and M11), (M12 and M13) as well as (M14 and M15) are matched. And assuming that all the transistors operate in the saturation region, the circuit operation can be explained as follows. The current mirrors formed by (M4-M7) forces equal currents (IB) in the transistors M1, M2 and M3. This operation drives the gate to source voltages of M1, M2 and M3 to be equal and, consequently, forces the two input terminals to be virtually grounded. The current mirrors formed by the transistor pairs (M4 and M5), (M8 and M9), (M10 and M11) and (M14 and M15) provide the current differencing operation, whereas the common source amplifier (M17) achieves the high gain stage.

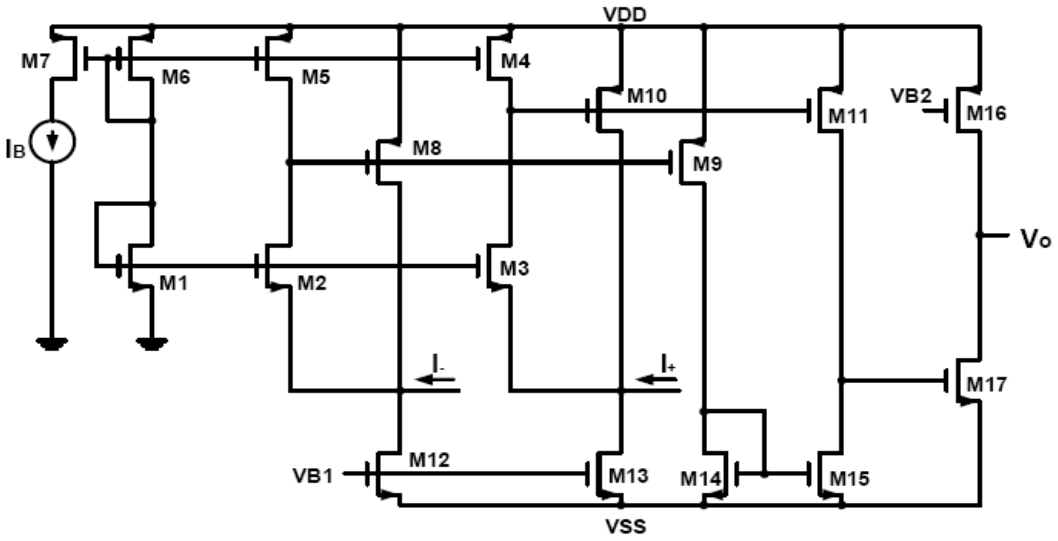

Fig. 2.3 CMOS realization of OTRA proposed in [2]

2.3 The Mostafa and Soliman OTRA [3]

The CMOS realization of the low power wide band OTRA proposed in [3] is shown in Fig.2.4. It is based on the cascaded connection of the modified differential current conveyor (MDCC) [6] and a common source amplifier [2]. Assuming that each of the groups of the transistors (M1-M3), (M5 and M6), (M8-M11) and (M12and M13) are matched. And assuming that all the transistors operate in the saturation region, the circuit operation can be explained as follows:

The current mirrors formed by (M8-M11) forces equal currents (IB) in the transistors M1, M2 and M3. This operation drives the gate to source voltages of M1, M2 and M3 to be equal and, consequently, forces the two input terminals to be virtually grounded. The current mirrors formed by the transistor pairs (M10 and M11) and (M12 and M13) provide the current differencing operation, whereas the common source amplifier (M14) achieves the high gain stage. It is clear that the modified OTRA has smaller number of current mirrors than Salama and Soliman OTRA introduced in [2] which reduces the transistor mirror mismatch effect and also increases the frequency capabilities. Moreover, this OTRA uses smaller number of transistors which reduces the power dissipation.

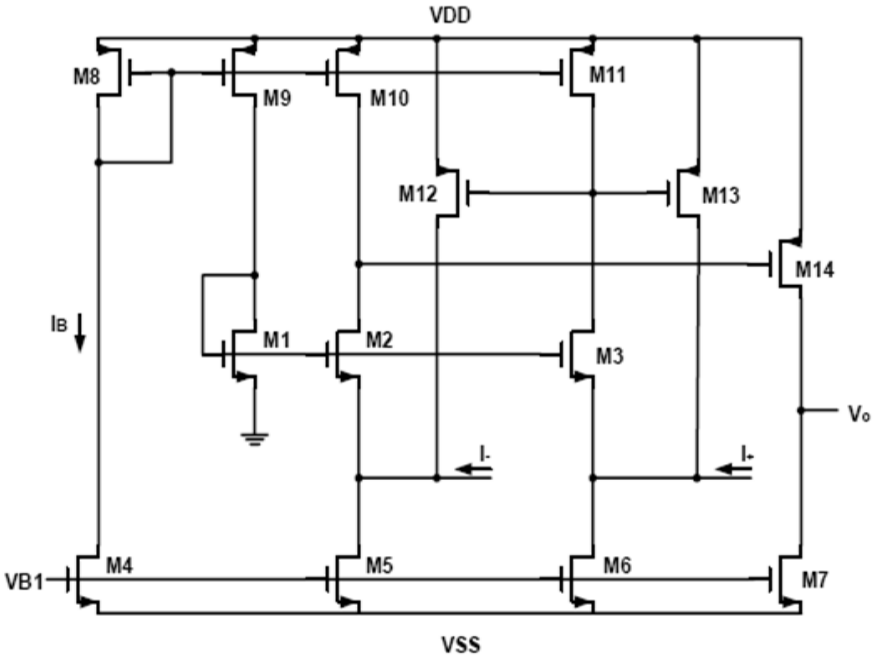

Fig. 2.4 CMOS realization of modified OTRA by Mostafa and Soliman [3]

2.4 Schematic of OTRA [3]

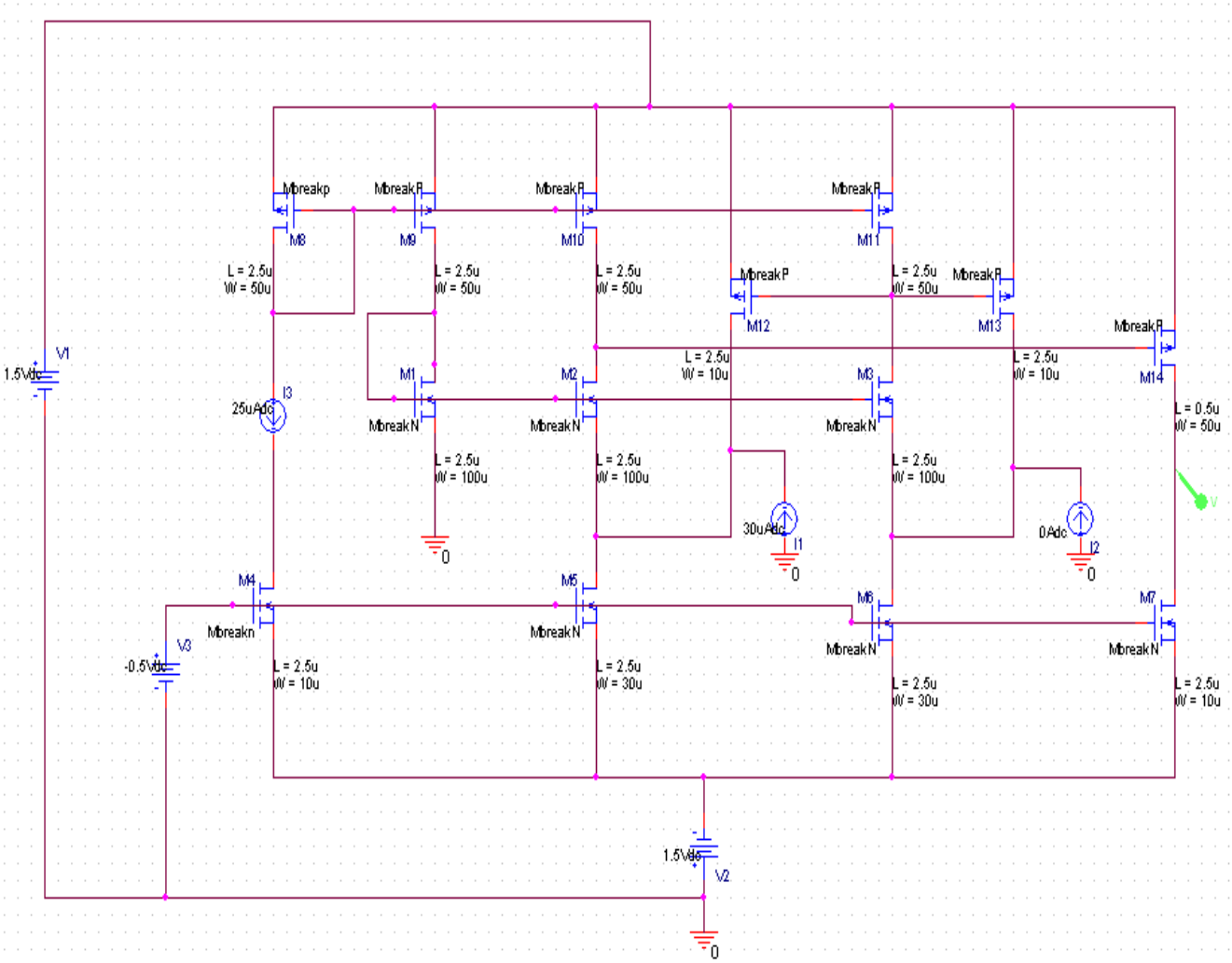

Fig. 2.5 Schematic CMOS Realization of modified OTRA [3]

2.5 Simulation results of OTRA [3]

PSPICE simulated results of OTRA [3] is shown in Fig. 2.6 and 2.7. First DC transfer characteristic and then frequency and phase response is traced. Different characteristic of simulated OTRA [3] is depicted below in subsection.

2.5.1 Characterization of OTRA [3]

Transistors aspect ratios are reported in Table 2.1. The biasing current I_b= 25µA. The biasing voltage VB1 = -0.5 V. Simulation results of modified OTRA [3] are tabulated in Table 2.2. These results can be described as follows. The input differential current range is from -50µA to 50µA (Fig.5). The offset current equals 1.25 µA. The input resistance equals 15.5 Ω . The DC open loop transresistance gain equals 82 dBΩ (= 126 MΩ) . The gain bandwidth product equals 372 GHz.Ω . The power dissipation of the circuit equals 0.9 mW. The modified OTRA [3] has a sharp peak at its open loop transresistance gain which can be removed using compensation techniques.

Table 2.1: Transistors aspect ratios of the circuit shown in Figure 2.3

Transistor	$\mathbf{W(\mu m)}/\mathbf{L(\mu m)}$
M1-M3	100/2.5
M4	10/2.5
M5, M6	30/2.5
M7	10/2.5
M8-M11	50/2.5
M12, M13	100/2.5
M14	50/0.5

Table 2.2: Parameters of the circuit shown in figure 2.4

Parameter	Mostafa and Soliman OTRA [3]
Input current dynamic range	-50 to 50 μA
Offset current	1.25 μA
DC open loop transresistance gain	82 dBΩ
Gain bandwidth product	372 GHzΩ
Input resistance	15.5 Ω
Power dissipation	0.9 mW
Parasitic capacitance	22pF

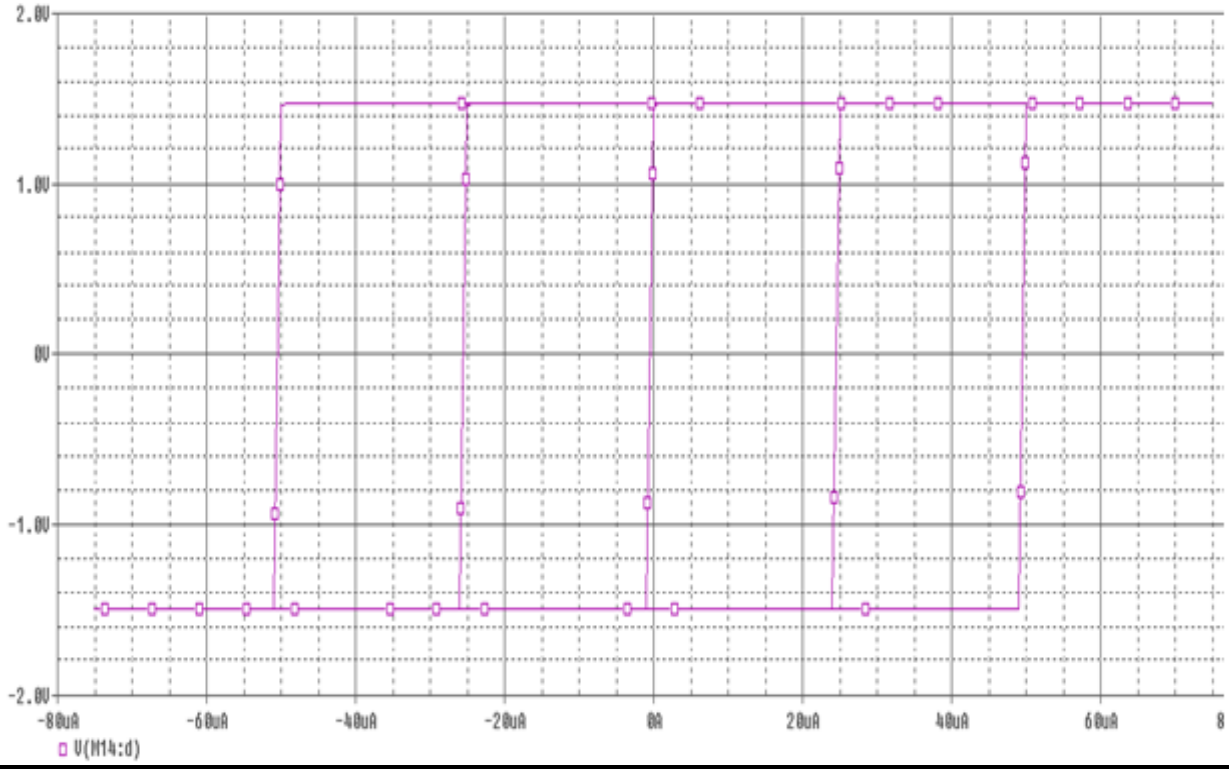

Fig 2.6. Non-inverting DC Transfer Chatacteristic of OTRA[3]

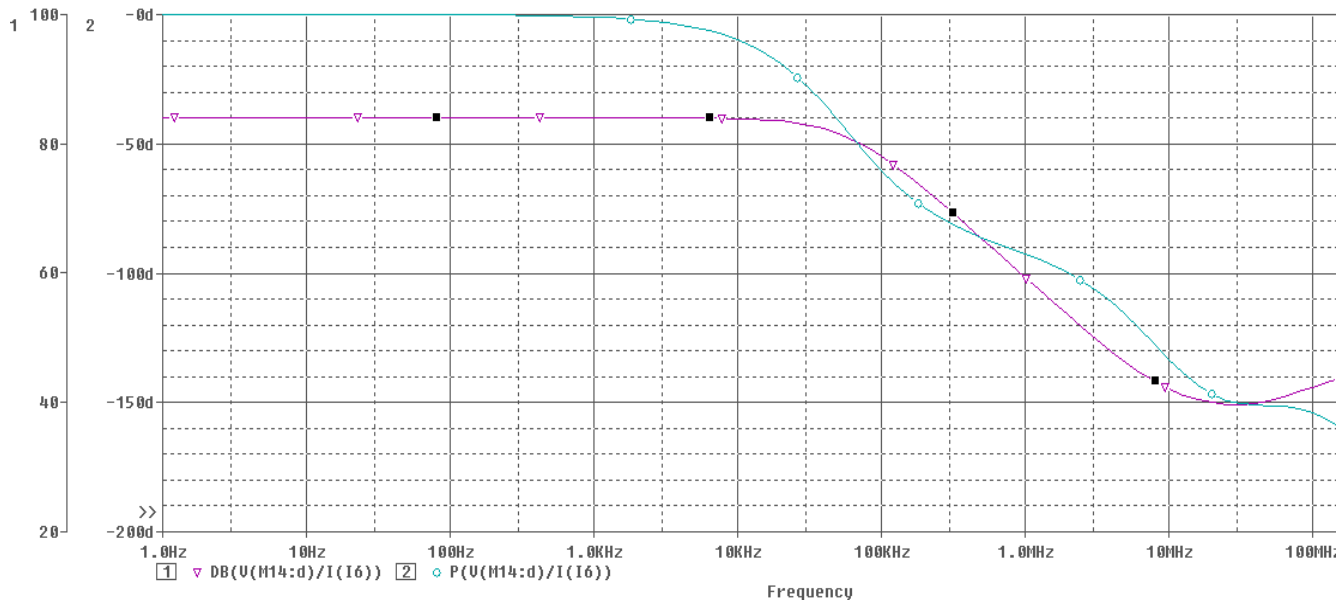

Fig. 2.7 Frequency response of Differential OTRA

References

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CHAPTER: 3

OTRA BASED FILTERS

The OTRA is a new active building block in industry and it has extensive applications in the field of telecommunication, control, instrumentation, measurement, and signal processing. OTRA is a high gain, current-input, voltage-output device. Using this device in a negative feedback loop should make it possible to obtain very accurate transfer functions **.** Both input and output terminals of the OTRA are characterized by low impedance, thereby eliminating response limitations incurred by capacitive time constants. The input terminals are internally grounded leading to circuits that are insensitive to the stray capacitances.

. The transfer function *H(s)* of a filter is the ratio of the output signal *Y(s)* to that of the input signal *X(s)* as a function of the complex frequency s:

$$H(s) = \frac{Y(s)}{X(s)}$$

With $s = \sigma + j\omega$

The transfer function of all linear time-invariant filters, when constructed of discrete components, will be the ratio of two polynomials in s, i.e. a rational function of s. The order of the transfer function will be the highest power of s encountered in the denominator.

standard transfer equation of the filter can be given by:

$$H(s) = \frac{a_m s^m + a_{m-1} s^{m-1} + \cdots a_1 s + a_0}{b_n s^n + b_{n-1} s^{n-1} + \cdots b_1 s + b_0}$$

Therefore, H(s) is a rational function of s with real coefficients with the degree of m for the numerator and n for the denominator. The degree of the denominator is the order of the filter. Solving for the roots of the equation determines the poles (denominator) and zeros (numerator) of the circuit. Each pole will provide a –6 dB/octave or –20 dB/decade response. Each zero will provide a +6 dB/octave or +20 dB/decade response. These roots can be real or complex. When they are complex, they occur in conjugate pairs. These roots are plotted on the s plane (complex plane) where the horizontal axis is σ (real axis) and the vertical axis is ω (imaginary axis). How these roots

are distributed on the s plane can tell us many things about the circuit. In order to have stability, all poles must be in the left side of the plane.

3.1 Second Order analog Filters

Transfer function of Second order filter is given as:

$$H(s) = \frac{Y(s)}{bs^2+cs+d}$$

Where $s = \sigma + j\omega$ and a,b,c,d are constants.

In second order filter there are always two poles which lie on the left half of the s plane for a system to be stable. Implementation of second order filters (LPF, BPF, HPF, BSF) using OTRA has been discussd in following subsection.

3.1.1 Low Pass Filter

A low pass filter is a filter that passes low-frequency signals and attenuates signals with frequencies higher than the cutoff frequency. The actual amount of attenuation for each frequency varies depending on specific filter design. It is sometimes called a high-cut filter, or treble cut filter in audio applications. Low-pass filters exist in different forms, including electronic circuits (such as a *hiss filter* used in audio), anti-aliasing filters for conditioning signals prior to analog-to-digital conversion, digital filters for smoothing sets of data, acoustic barriers, blurring of images, and so on. Low-pass filters provide a smoother form of a signal, removing the short-term fluctuations, and leaving the longer-term trend.

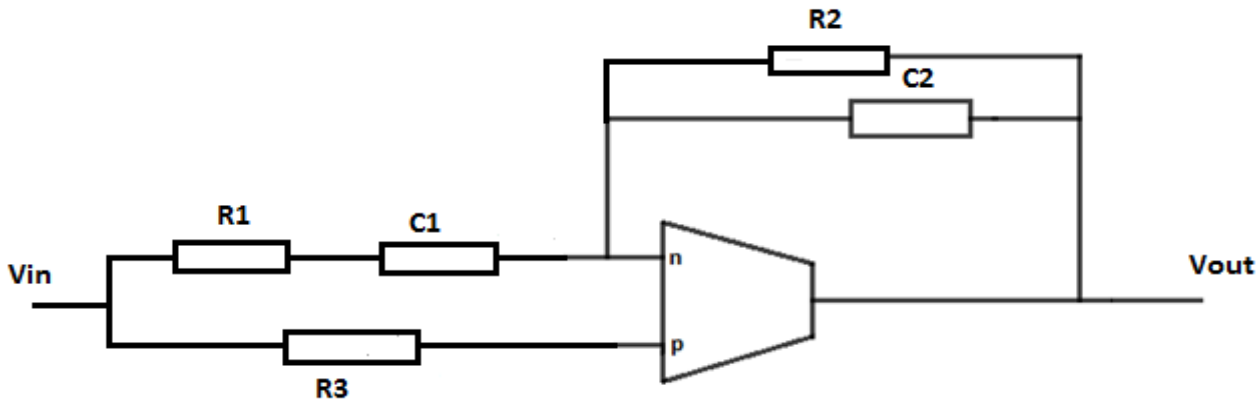

Fig. 3.1 Low Pass Filter configuration of OTRA

Transfer function of Low Pass Filter in fig 3.1 is given by:

$$\frac{V_0}{V_{in}} = \frac{G_1 - {}^{1}\Big/\left(\frac{1}{G_1}+\frac{1}{SC_1}\right)}{G_3+SC_3} \tag{3.1}$$

The resonant angular frequency (ω0), the quality factor (Q0) and filter Gain (H0) are given by equations (3.2), (3.3) and (3.4) respectively

$$\omega_0 = \frac{\sqrt{G_1 G_3}}{\sqrt{C_1 C_3}} \tag{3.2}$$

$$Q_0 = \frac{\sqrt{G_1 G_3 C_1 C_3}}{(G_1 C_3 + G_3 C_1)} \tag{3.3}$$

$$H_0 = \frac{G_1}{G_3} \tag{3.4}$$

3.1.1.1 PSPICE Schematic and Simulation results of LPF

Results of LPF of fig 3.1 are verified through PSPICE simulations using the CMOS implementation of the OTRA [3].The schematic of LPF is given in Fig. 3.2. Component values chosen for LP response are C1=10pF, C2=10pF, R1 = R3 = 1K, R2=10K.

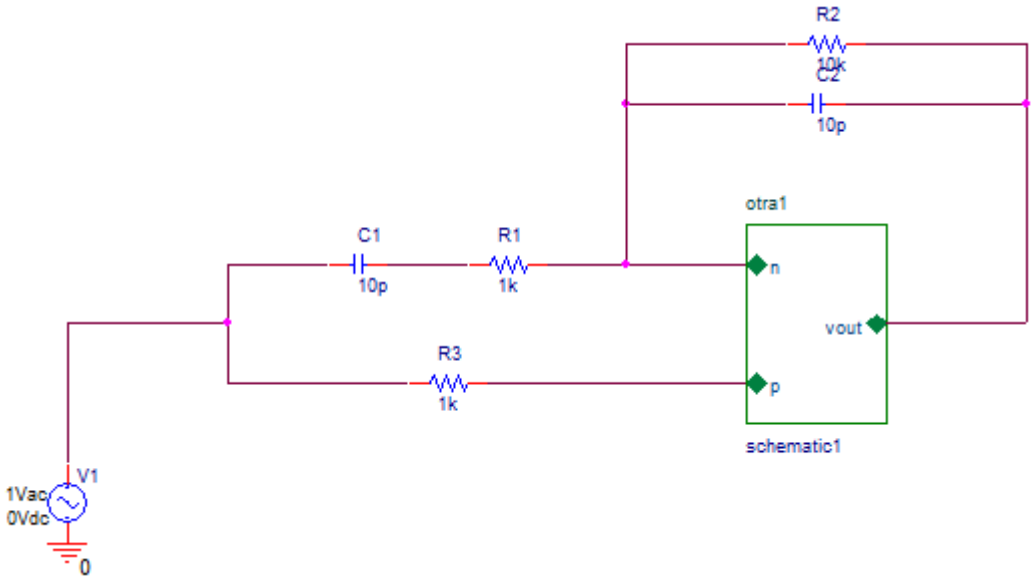

Fig 3.2 PSPICE schematic of LPF

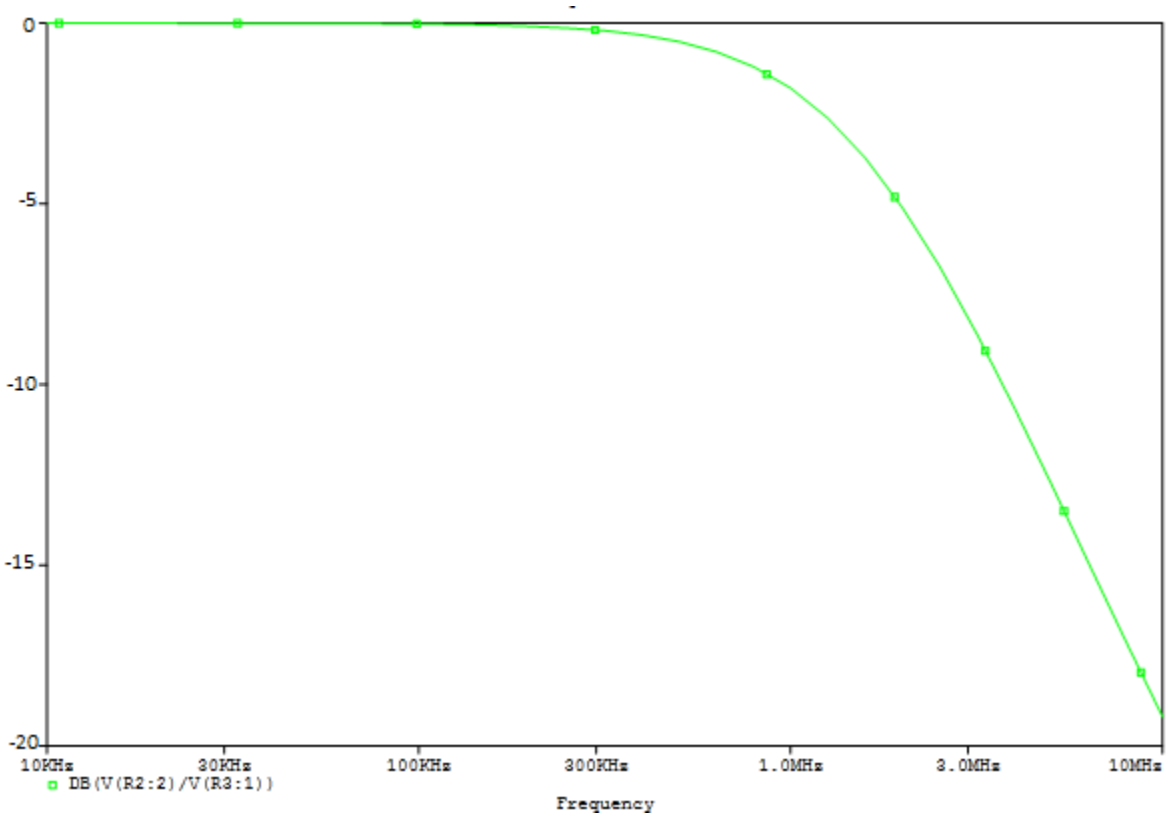

Fig. 3.3 Frequency response of LPF

3.1.2 High Pass Filter

A high-pass filter (HPF) is an electronic filter that passes high-frequency signals but attenuates (reduces the amplitude of) signals with frequencies lower than the cutoff frequency. The actual amount of attenuation for each frequency varies from filter to filter. A high-pass filter is usually modeled as a linear time-invariant system. It is sometimes called a low-cut filter or bass-cut filter.

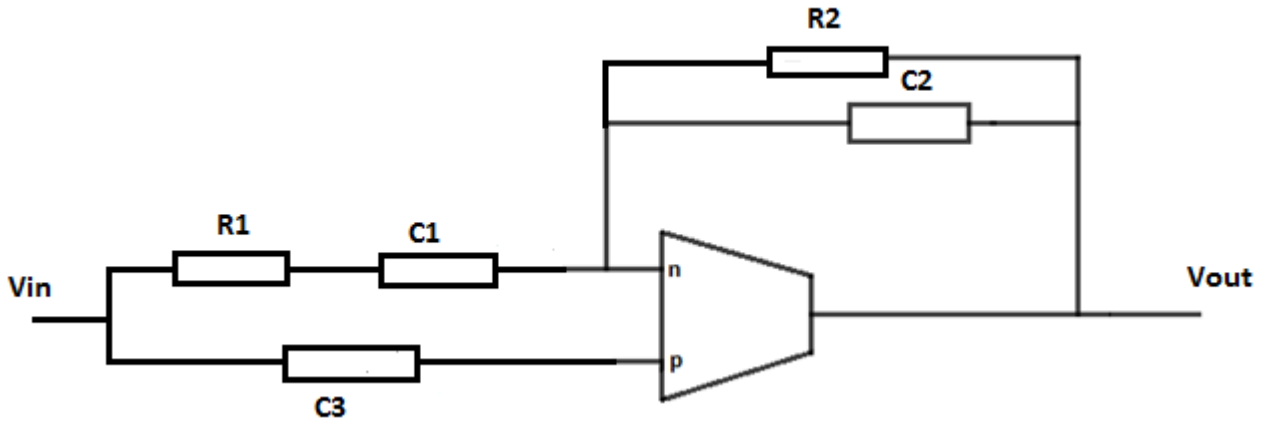

Fig. 3.4 High Pass Filter configuration of OTRA

Transfer function of High Pass Filter in Fig 3.4 is given by:

$$\frac{V_0}{V_{in}} = \frac{sc_1 - 1 \Big/ \left(\frac{1}{G_1} + \frac{1}{SC_1}\right)}{G_3 + SC_3} \tag{3.5}$$

Where ω0, Q0 and H0 are given by equations (3.6), (3.7) and (3.8) respectively.

$$\omega_0 = \frac{\sqrt{G_1 G_3}}{\sqrt{C_1 C_3}} \tag{3.6}$$

$$Q_0 = \frac{\sqrt{G_1 G_3 C_1 C_3}}{(G_1 C_3 + G_3 C_1)} \tag{3.7}$$

And $$H_0 = \frac{C_1}{C_3} \quad (3.8)$$

3.1.2.1 PSPICE schematic and simulation result of HPF

Results of HPF of fig 3.4 are verified through PSPICE simulations using the CMOS implementation of the OTRA [3].The schematic of HPF is given in Fig. 3.5. Component values chosen for HP response are C1 = C3= 10pF, C2=1nF and R1=R2= 1KΩ.

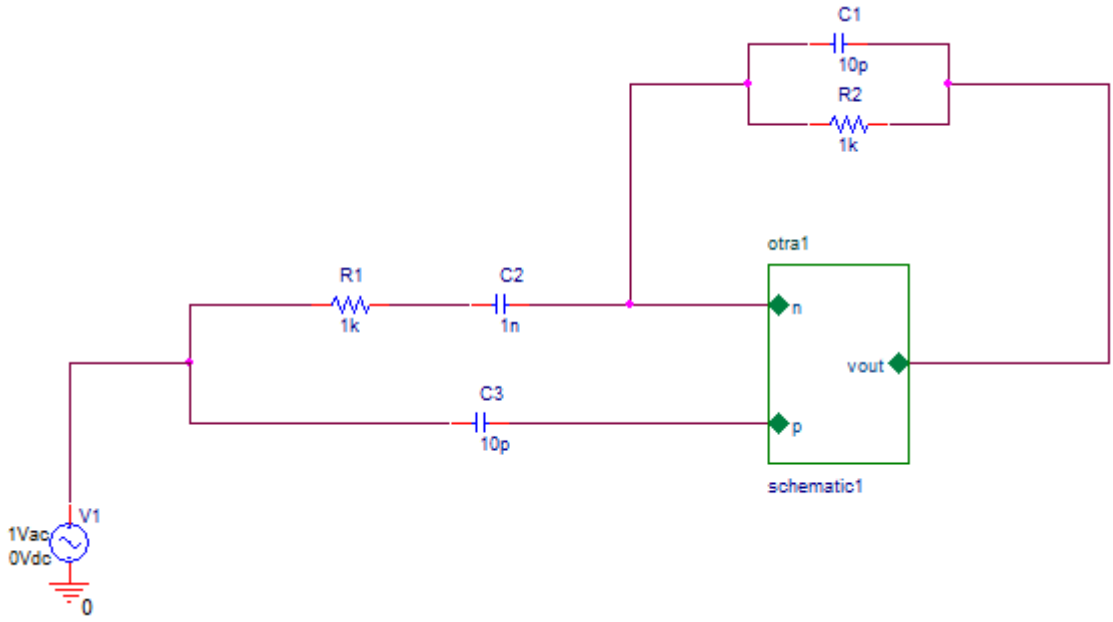

Fig 3.5 PSPICE schematic of HPF

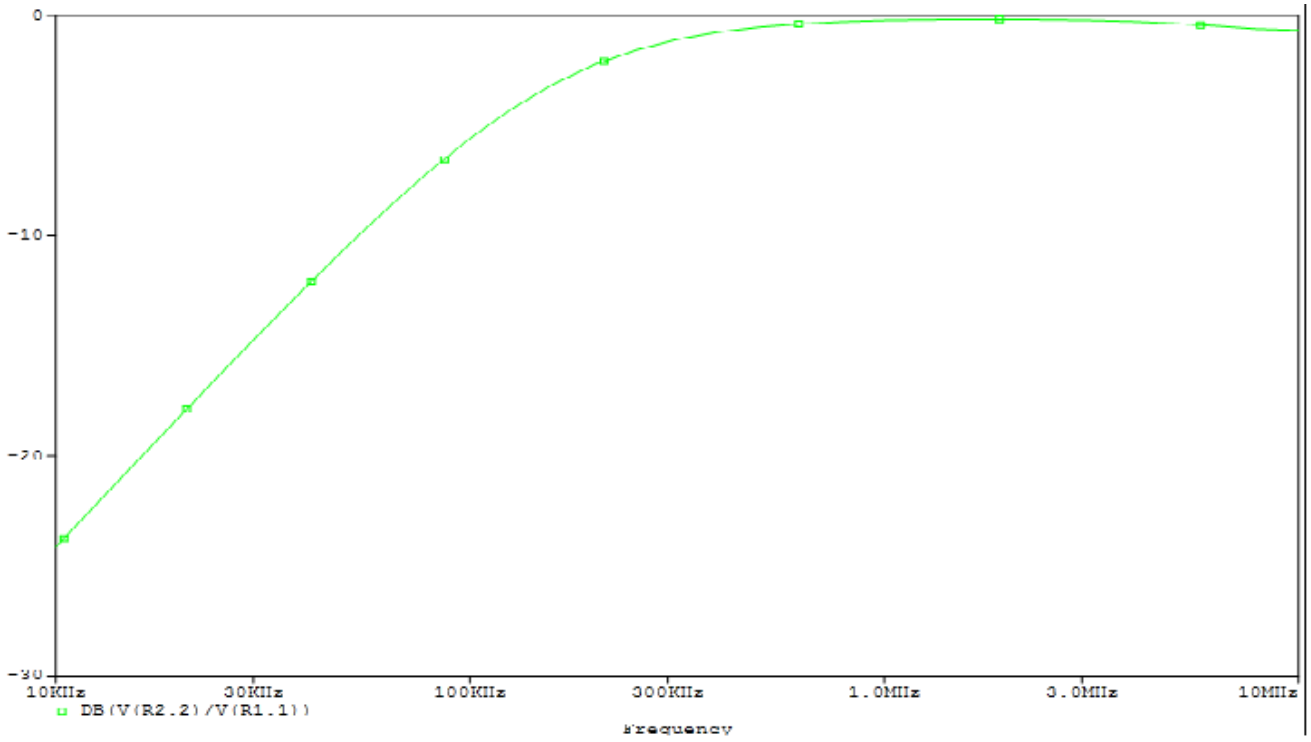

Fig. 3.6 Frequency response of HPF

3.1.3 Band Pass filter

A band-pass filter is a device that passes frequencies within a certain range and rejects (attenuates) frequencies outside that range. *Bandpass* is an adjective that describes a type of filter or filtering process; it is to be distinguished from pass band, which refers to the actual portion of affected spectrum. Hence, one might say "A dual bandpass filter has two passbands." Abandpass *signal* is a signal containing a band of frequencies not adjacent to zero frequency, such as a signal that comes out of a bandpass filter. An ideal bandpass filter would have a completely flat passband (e.g. with no gain/attenuation throughout) and would completely attenuate all frequencies outside the passband. Additionally, the transition out of the passband would be instantaneous in frequency.

In practice, no bandpass filter is ideal. The filter does not attenuate all frequencies outside the desired frequency range completely; in particular, there is a region just outside the intended passband where frequencies are attenuated, but not rejected. This is known as the filter roll-off, and it is usually expressed in dB of attenuation per octave or decade of frequency.

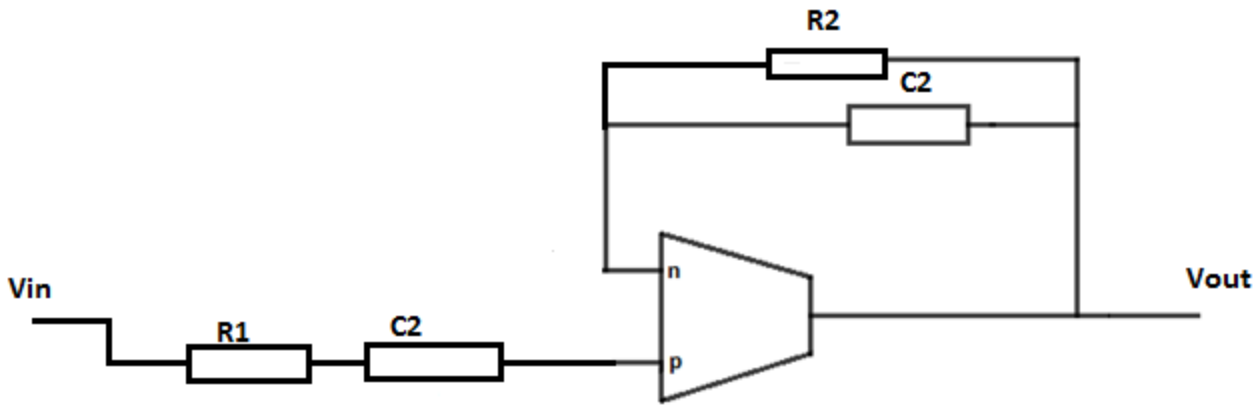

Fig. 3.7 Band Pass Filter configuration of OTRA

Transfer function of Band Pass Filter in Fig 3.7 is given by :

$$\frac{V_0}{V_{in}} = \frac{{}^{1}\Big/\left(\frac{1}{G_1}+\frac{1}{SC_1}\right)}{G_3+SC_3} \tag{3.9}$$

equations (3.10), (3.11) and (3.12) respectively give the value of ω0, Q0and H0 for the filter.

$$\omega_0 = \frac{\sqrt{G_2 G_3}}{\sqrt{C_2 C_3}} \tag{3.10}$$

$$Q_0 = \frac{\sqrt{C_2 C_3 G_2 G_3}}{(C_3 G_2 + C_2 G_3)} \tag{3.11}$$

And $$H_0 = \frac{G_2 C_3}{G_2 C_3 + G_3 C_2} \tag{3.12}$$

3.1.3.1 PSPICE Schematic and Simulation results of BPF

Results of BPF of fig 3.7 are verified through PSPICE simulations using the CMOS implementation of the OTRA [3].The schematic of BPF is given in Fig. 3.8.. The component values chosen are R1 = R2 = 0.9KΩ, R3= 20KΩ, C1 = 0.1Nf, C2 = 3nF.

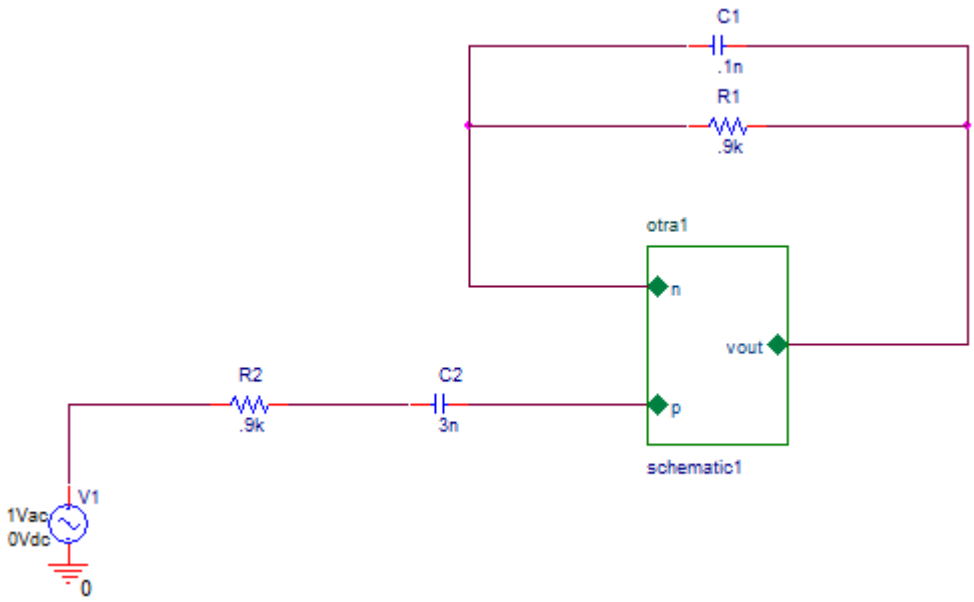

Fig. 3.8 PSPICE Schematic of BPF

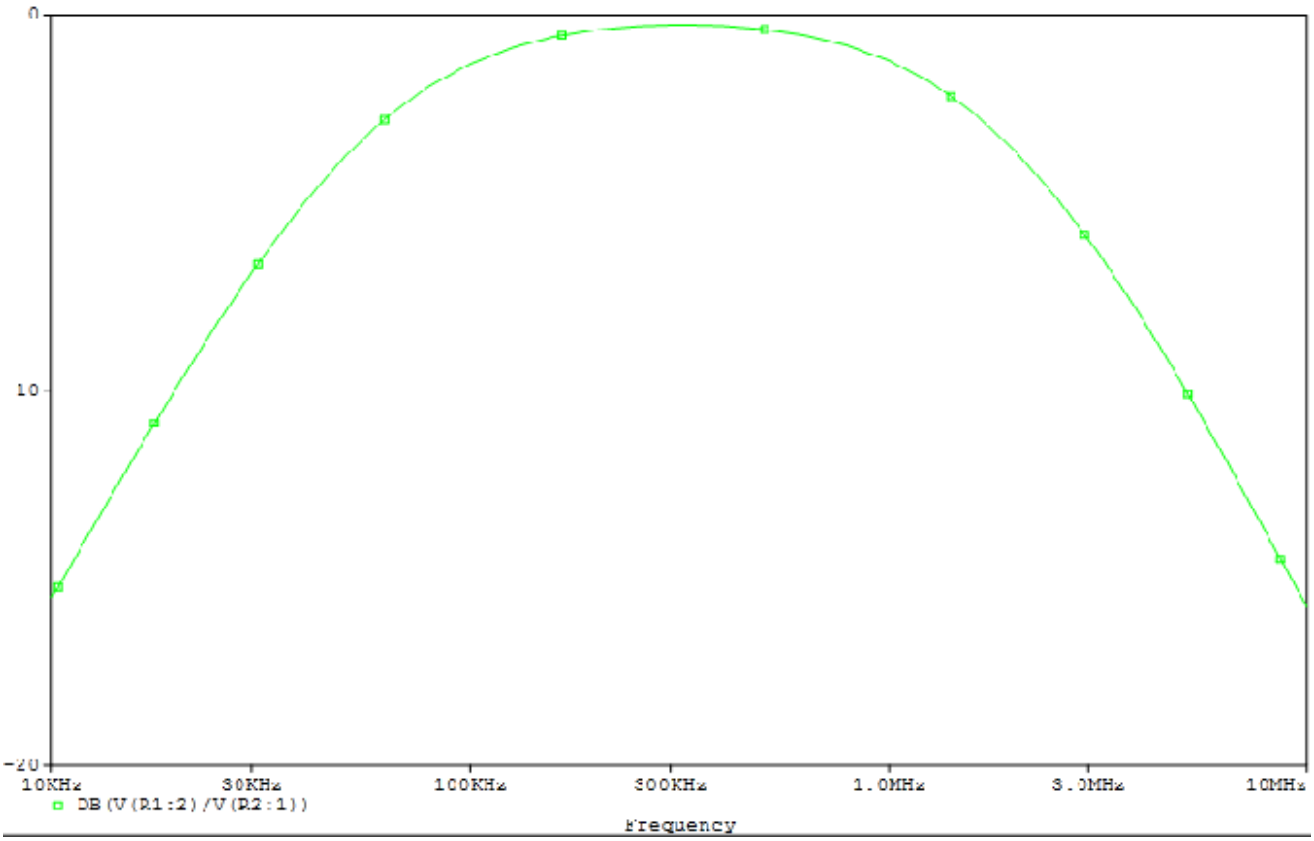

Fig. 3.9 Frequency response of BPF

3.1.4 Band Stop Filter

Band stop filter is Also called band-elimination, band-reject, or notch filters, this kind of filter passes all frequencies above and below a particular range set by the component values. It's function is opposite of band pass filter which allows to pass a particular band of frequencies.

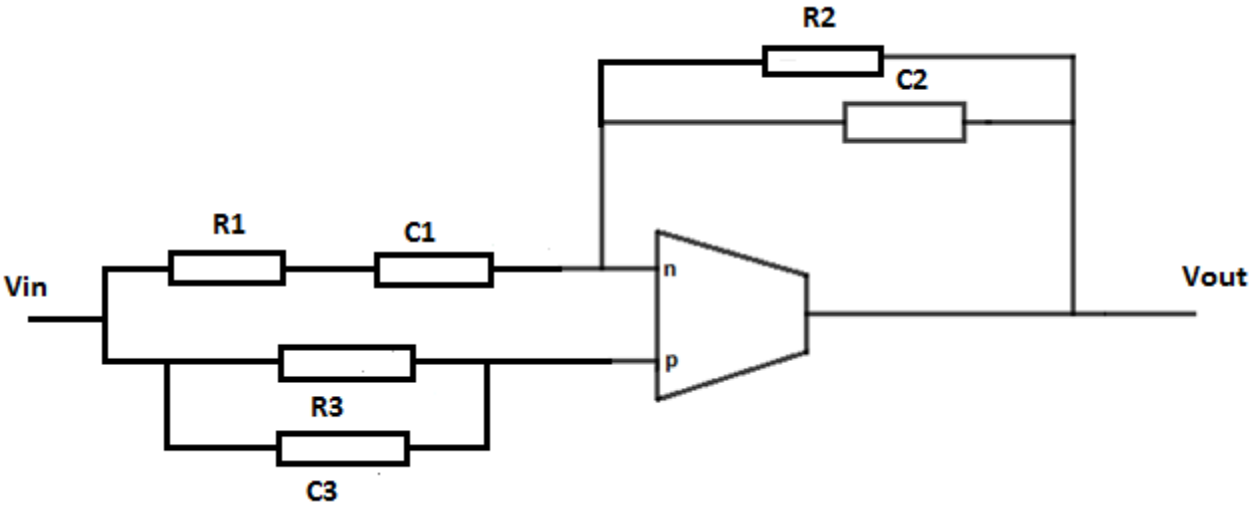

Fig. 3.10 Band Stop Filter configuration using OTRA

Transfer function of Band Pass Filter in Fig 3.10 is given by :

$$\frac{V_0}{V_{in}} = \frac{G_2 - SC_2 - 1 \Big/ \left(\frac{1}{G_1} + \frac{1}{SC_1}\right)}{G_3 + SC_3} \tag{3.13}$$

equations (3.14), (3.15) and (3.16) respectively give the value of ω0, Q0and H0 for the filter.

$$\omega_0 = \frac{\sqrt{G_1 G_2}}{\sqrt{C_1 C_2}} \tag{3.14}$$

$$Q_0 = \frac{\sqrt{C_1 C_2 G_1 G_2}}{(C_1 G_2 + C_2 G_1)} \tag{3.15}$$

And $$H_0 = 1 \tag{3.16}$$

3.1.4.1 PSPICE schematic and simulation results of BSF

Results of BSF of fig 3.10 are verified through PSPICE simulations using the CMOS implementation of the OTRA [3].The schematic of BSF is given in Fig. 3.11.The component values chosen are R1 = R2 = 1KΩ, R3= 1KΩ, C1 = 5pf, C2 = 1nf, C3=10pf.

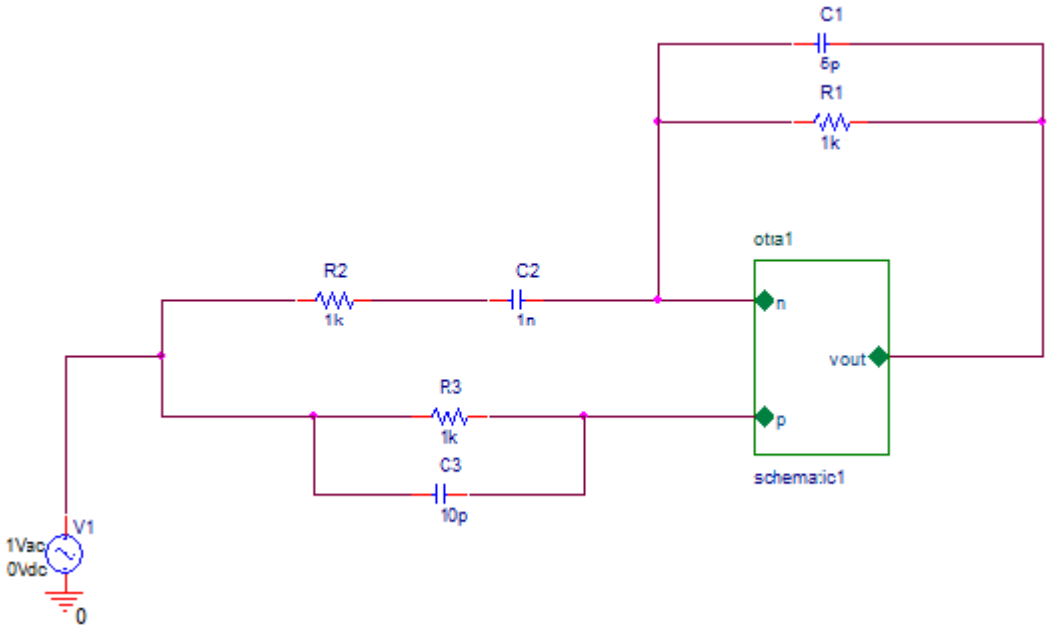

Fig. 3.11 PSPICE schematic of BSF

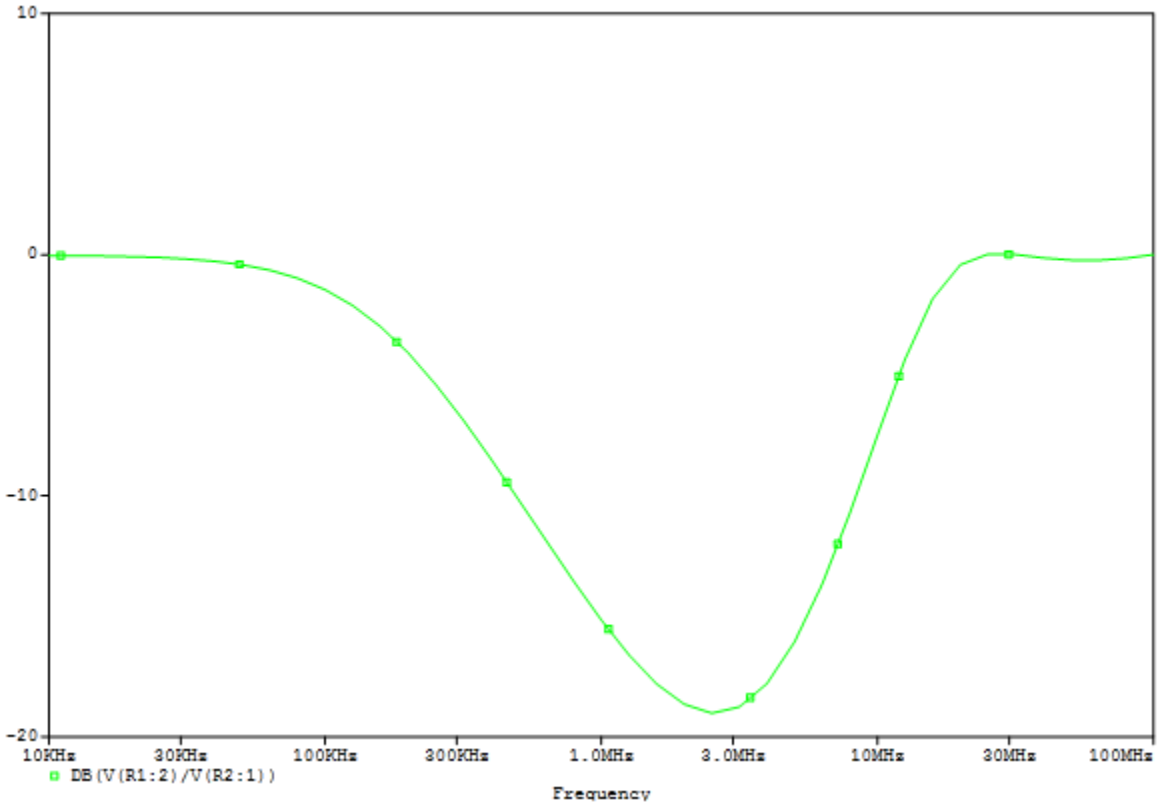

Fig. 3.12 Frequency response of BSF

3.2 Voltage Mode Biquadratic Filters

Biquad filter is a second-order recursive linear filter, containing two poles and two zeros. In this section, a single OTRA based biquadratic filter configuration is presented which is based on Sallen Key approach. It realizes the low pass (LP), high pass (HP), and band pass (BP) filter functions by appropriate admittance selection.

3.2.1 Low Pass Filter

A low pass filter is a filter that passes low-frequency signals and attenuates (reduces the amplitude of) signals with frequencies higher than the cutoff frequency. The actual amount of attenuation for each frequency varies depending on specific filter design.

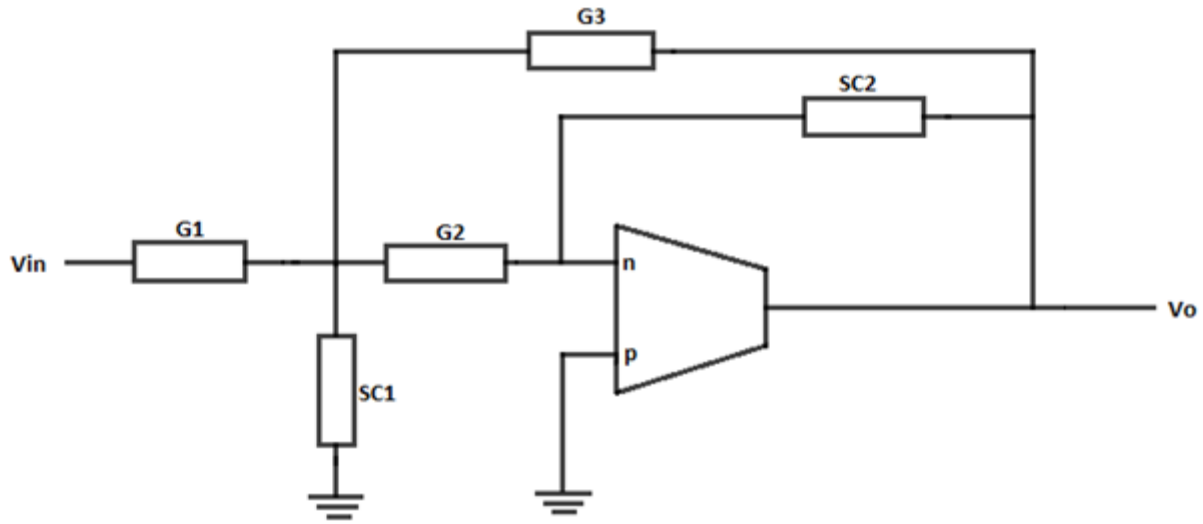

Fig. 3.13 Biquad LPF configuration using OTRA

Transfer function of biquadratic Low Pass Filter in fig 3.13 is given by:

$$\frac{V_0}{V_{in}} = \frac{-G_1G_2}{\{SC_2(G_1+SC_1+G_2+G_3)+G_2G_3\}} \quad (3.17)$$

Or $$\frac{V_0}{V_{in}} = \frac{-G_1G_2/C_1GC_2}{S^2+S+G_2G_3/C_1C_2} \quad (3.18)$$

The resonant angular frequency (ω0), the quality factor (Q0) and filter Gain (H0) are given by equations (3.19), (3.20) and (3.21) respectively

$$\omega_0 = \frac{\sqrt{G_2G_3}}{\sqrt{C_1C_2}} \quad (3.19)$$

$$Q_0 = \frac{\sqrt{G_2G_3C_1}}{(G_1+G_2+G_3)\sqrt{C_2}} \quad (3.20)$$

$$H_0 = \frac{-G_1}{G_3} \quad (3.21)$$

Result of LPF in fig 3.13 are verified through simulations using the CMOS implementation of the OTRA [3] as given in Fig. 3.14. The SPICE simulation was performed using 0.5 µm CMOS process parameters provided by MOSIS (AGILENT). The LP and filter configuration was designed to give Butterworth response for an f0 of .7 MHz. Component values chosen for LP response are C1=450pF, C2=100pF, R1 = R2 = R3 = 0.5KΩ..

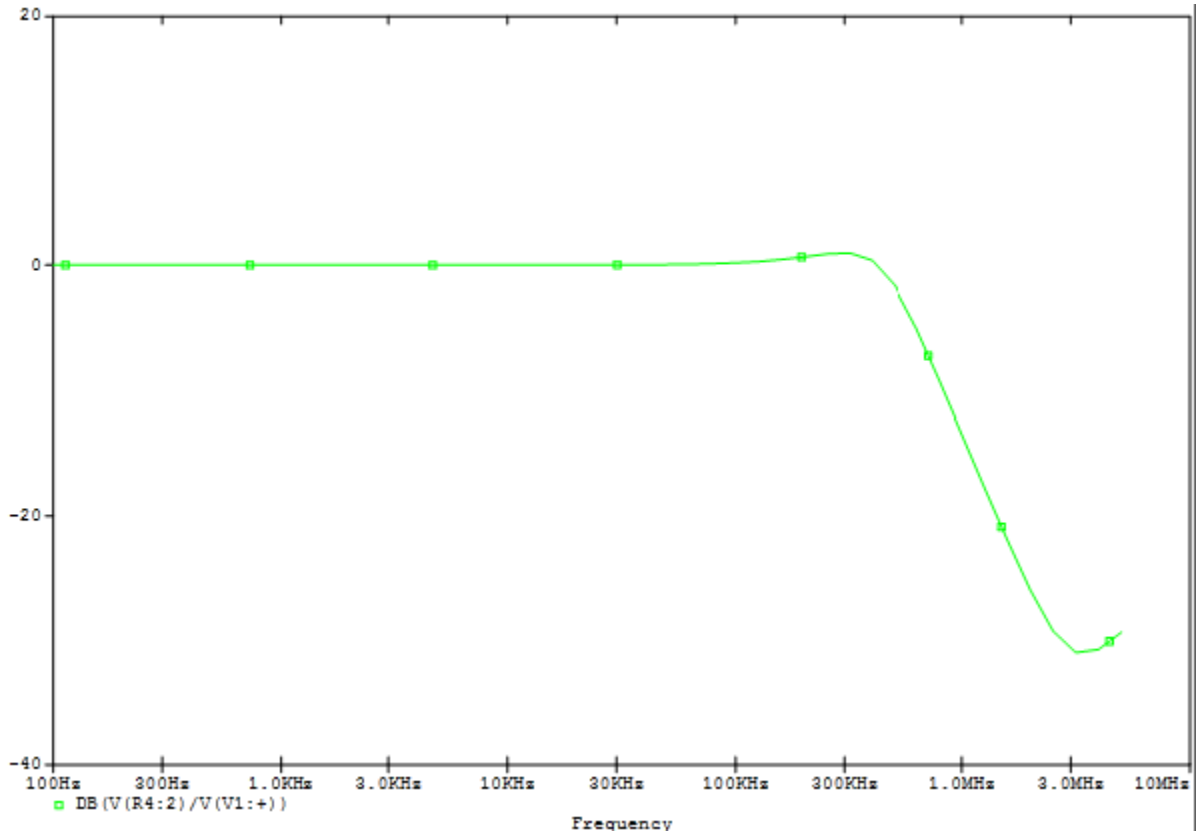

Fig 3.14 LP response for f_0 of .7 MHz

3.2.2 High Pass Filter

A high-pass filter (HPF) is an electronic filter that passes high-frequency signals but attenuates (reduces the amplitude of) signals with frequencies lower than the cutoff frequency. The actual amount of attenuation for each frequency varies from filter to filter. A high-pass filter is usually modeled as a linear time-invariant system. It is sometimes called a low-cut filter or bass-cut filter.

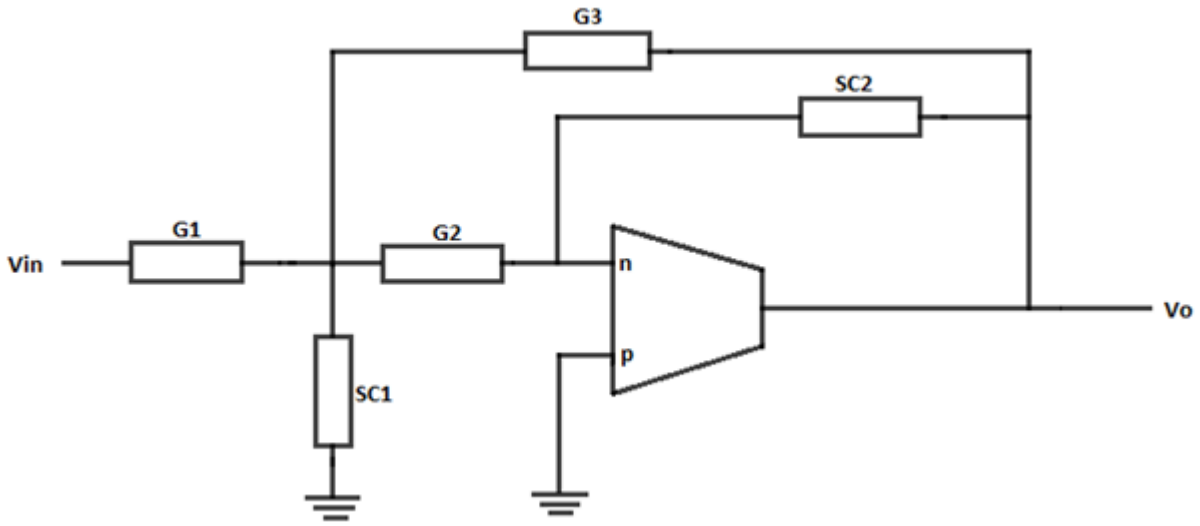

Fig. 3.15 Biquad HPF configuration using OTRA

Transfer function of High Pass Filter in Fig 3.15 is given by:

$$\frac{V_0}{V_{in}} = \frac{-S^2 {}^{C_1}/_{C_2}}{S^2 + S\left\{G_2 (C_1 + C_2 + C_3) {}^{1}/_{C_2 C_3}\right\} + {}^{G_1 G_2}/_{C_2 C_3}} \tag{3.22}$$

Where ω0, Q0 and H0 are given by equations (3.23), (3.24) and (3.25) respectively.

$$\omega_0 = \frac{\sqrt{G_1 G_2}}{\sqrt{C_2 C_3}} \tag{3.23}$$

$$Q_0 = \frac{\sqrt{G_1 C_2 C_3}}{(C_1 + C_2 + C_3)\sqrt{G_2}} \tag{3.24}$$

And $$H_0 = \frac{-C_1}{C_3} \tag{3.25}$$

The High Pass filter circuits is verified through simulations using the CMOS implementation of the OTRA [3] as given in Fig. 3.15. The SPICE simulation was performed using 0.5 µm CMOS process parameters provided by MOSIS (AGILENT). The HP filter configuration was designed to give

Butterworth response for an f0 of .7 MHz. Component values chosen for HP response are C1 = C2 = C3= 100pF,R1= 0.5KΩ, R2= 2.25KΩ.

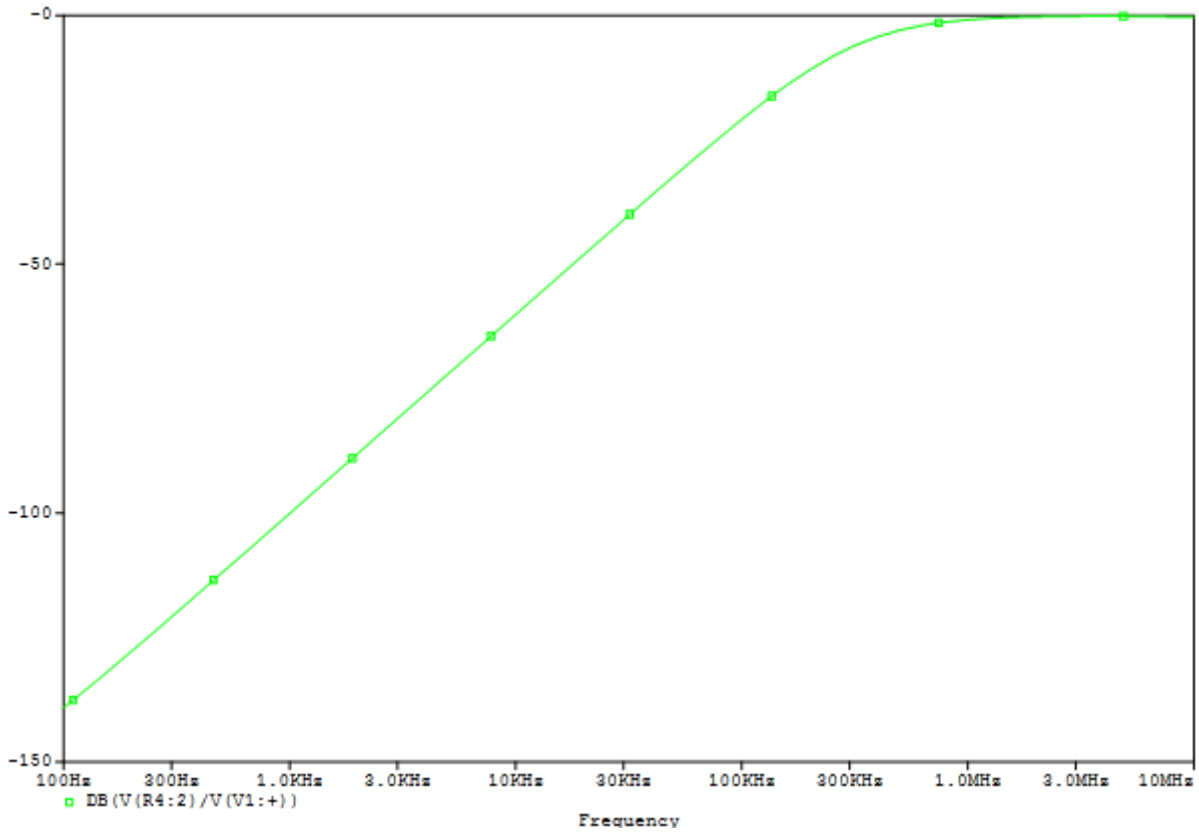

Fig 3.16 High Pass response for f_0 of .7 MHz

3.2.3 Band Pass filter

A band-pass filter is a device that passes frequencies within a certain range and rejects (attenuates) frequencies outside that range. Bandpass is an adjective that describes a type of filter or filtering process; it is to be distinguished from pass band, which refers to the actual portion of affected spectrum. Hence, one might say "A dual bandpass filter has two passbands." Abandpass *signal* is a signal containing a band of frequencies not adjacent to zero frequency, such as a signal that comes out of a bandpass filter.

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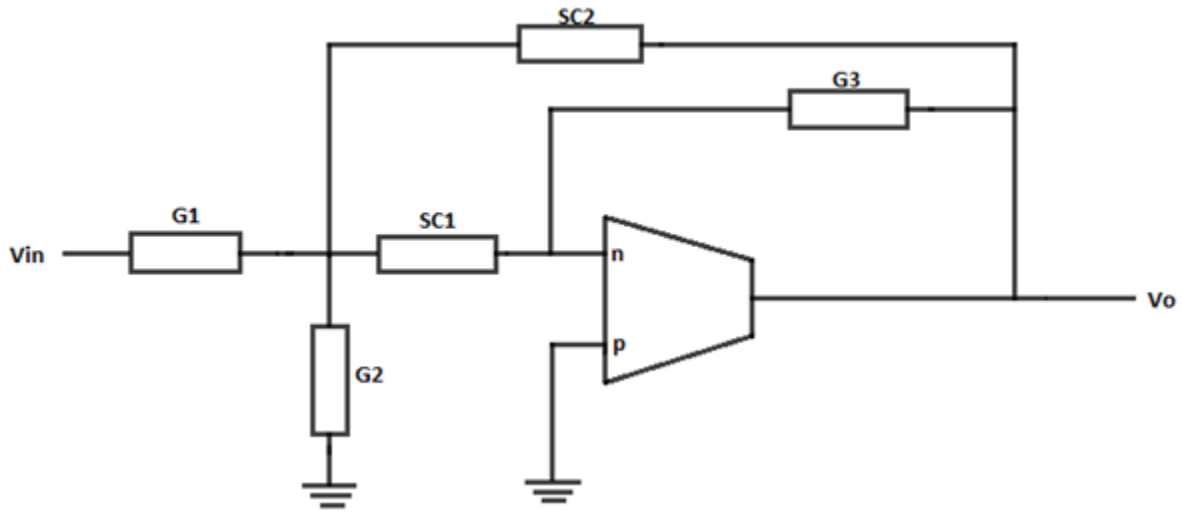

Fig. 3.17 Biquad BPF configuration using OTRA

Transfer function of Band Pass Filter in Fig 3.17 is given by :

$$\frac{V_0}{V_{in}} = \frac{-SG_1/C_2}{S^2 + S\left(G_3(C_1+C_2)\right)/C_1C_2 + G_3(G_1+G_2)/C_1C_2} \tag{3.26}$$

equations (3.27), (3.28) and (3.29) respectively give the value of ω0, Q0and H0 for the filter.

$$\omega_0 = \frac{\sqrt{(G_1+G_2)G_3}}{\sqrt{C_2C_3}} \tag{3.27}$$

$$Q_0 = \frac{\sqrt{C_1C_2(G_1+G_2)}}{(C_1+C_2)\sqrt{G_3}} \tag{3.28}$$

And $$H_0 = \frac{-G_1C_1}{G_3(C_1+C_2)} \tag{3.29}$$

The Band Pass filter circuit is verified through simulations using the CMOS implementation of the OTRA [3] as given in Fig. 3.18. The SPICE simulation was performed using 0.5 µm CMOS process parameters provided by MOSIS (AGILENT). The band pass response having f0 of .5 MHz and Q0 = 1 is shown in Fig. 3.18 for which the component values chosen are R1 = R2 = 10KΩ, R3= 20KΩ, C1 = C2 = 10pF.

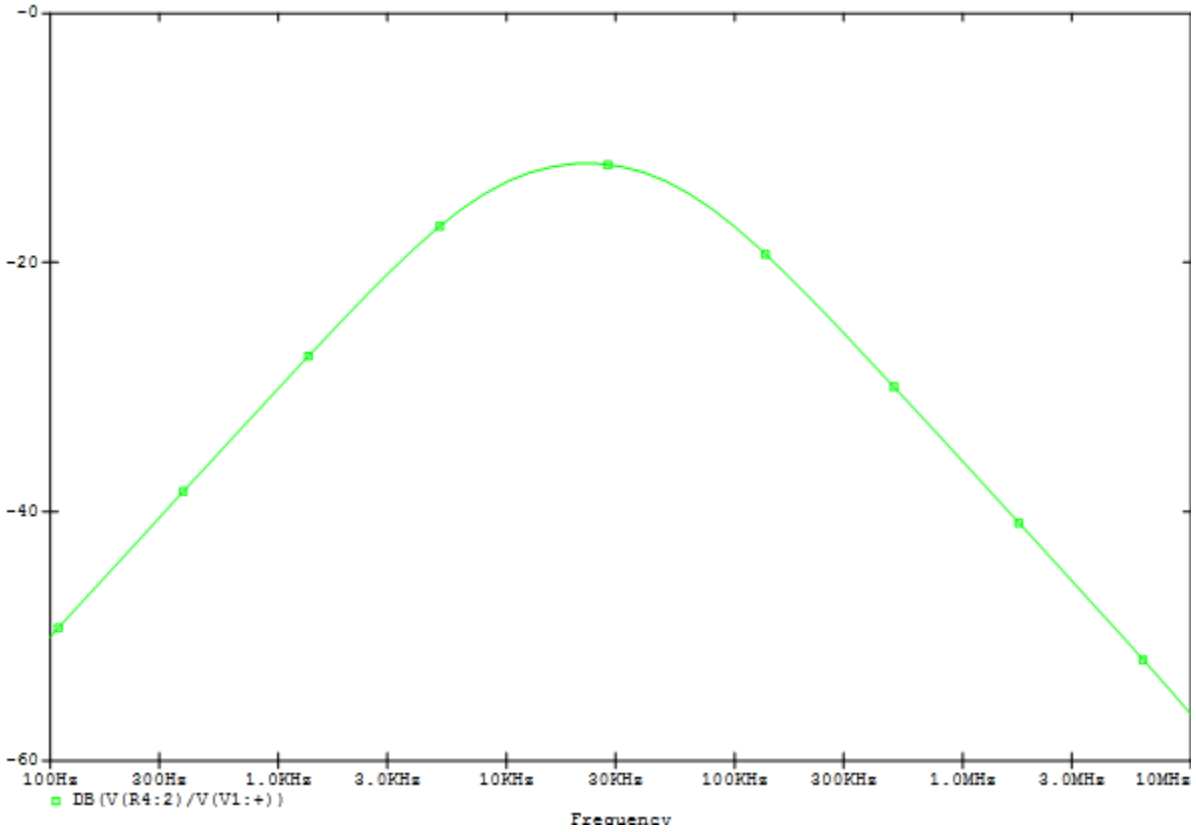

Fig. 3.18 BPF response at f_0 of .4 MHz

Reference

[l] J. Chen, H. Tsao, and C. Chen, “Operational transresistance amplifier using CMOS technology”, Electron. Lett., vol. 28, no. 22, pp. 2087- 2088, Oct. 1992..

[2] K.N. Salama and A.M. Soliman, “CMOS operational transresitance amplifier for analog signal processing applications”, Microelectronics Journal, vol. 30, pp. 235-245, 1999.

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CHAPTER 4

OTRA BASED OSCILLATORS

4.1 INTRODUCTION

Oscillators are circuits that produce periodic waveforms. In oscillators, the only input requirement is of DC power supply which is required for operation of the active device. The frequency of the generated waveforms may vary from a few Hz to several KHz. It may be used to generate AC waveforms such as sinusoidal, rectangular or sawtooth depending upon the type of oscillators used.

Oscillators works on a principle of positive feedback. It is well known that positive feedback amplifier consists of amplifier having gain of 'A' and feedback circuit with gain of 'β'. Here, a part of output is fed back to input through feedback circuit. The signal which is fed back is added to the input signal using summer 'Σ' and output of the summer acts as an actual input signal to the amplifier. The Fig.4.1 shows the block diagram of the oscillator. The difference between positive feedback amplifier and oscillator is that, in oscillator, there is no need of external input signal. To start the oscillations, output signal must be fed back in proper magnitude and phase.

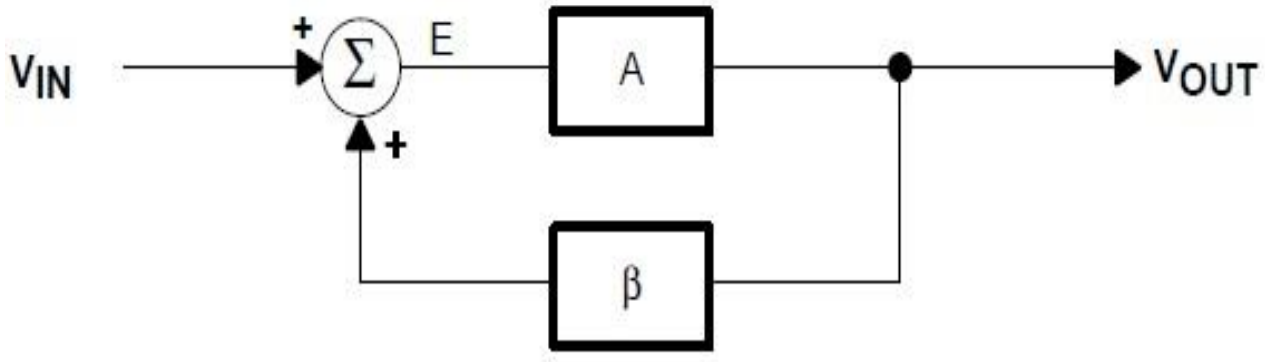

Fig. 4.1 Basic block of oscillator with feedback

The corresponding classic expression for a feedback system is derived as follows. Equation (4.1) is the defining equation for the output voltage; equation (4.2) is the corresponding error:

$$V_{OUT} = E \times A \tag{4.1}$$

$$E = V_{IN} + \beta V_{OUT} \tag{4.2}$$

Eliminating the error term, E, from these equations gives

$$\frac{V_{OUT}}{A} = V_{IN} - \beta V_{OUT} \tag{4.3}$$

and collecting the terms in V_{OUT} yields

$$V_{IN} = V_{OUT}\left(\frac{1}{A} + \beta\right) \tag{4.4}$$

Rearrangement of the terms produces equation (4.5), the classical form of feedback expression:

$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{1 + A\beta} \tag{4.5}$$

Oscillators do not require an externally-applied input signal; instead, they use some fraction of the output signal created by the feedback network as the input signal.

Oscillation results when the feedback system is not able to find a stable steady-state because its transfer function cannot be satisfied. The system goes unstable when the denominator(in 4.5) becomes zero, i.e., when 1 + Aβ = 0, or Aβ = –1. The key to designing an oscillator is ensuring that Aβ = –1. This is called the **Barkhausen criterion**. Satisfying this criterion requires that the magnitude of the loop gain is unity with a corresponding phase shift of 180^0as indicated by the minus sign. An equivalent expression using the symbology of complex algebra is Aβ = 1∠–180° for a negative feedback system. For a positive feedback system, the expression is Aβ = 1∠0° and the sign of the Aβ term is negative (in 4.5).

As the phase shift approaches 180° and |Aβ| → 1, the output voltage of the now-unstable system tends to infinity but, of course, is limited to finite values by an energy-limited power supply. When the output voltage approaches either power rail, the active devices in the amplifiers change gain. This causes the value of A to change and forces Aβ away from the singularity; thus the trajectory towards an infinite voltage slows and eventually halts. At this stage, one of three things can occur: (i) Nonlinearity in saturation or cutoff causes the system to become stable and lock up at the current power rail. (ii) The initial change causes the system to saturate (or cutoff) and stay that way for a long time before it becomes linear and heads for the opposite power rail. (iii) The system stays

linear and reverses direction, heading for the opposite power rail. The second alternative produces highly distorted oscillations (usually quasi-square waves), the resulting oscillators being called relaxation oscillators. The third produces a sine-wave oscillator.

4.1.1 Phase Shift in the Oscillator

The 180^0 phase shift in the equation Aβ = 1∠–180° is introduced by active and passive components. Like any well-designed feedback circuit, oscillators are made dependent on passive-component phase shift because it is accurate and almost drift-free. The phase shift contributed by active components is minimized because it varies with temperature, has a wide initial tolerance, and is device dependent. Amplifiers are selected so that they contribute little or no phase shift at the oscillation frequency. These constraints limit the op-amp oscillator to relatively low frequencies.

A single-pole RL or RC circuit contributes up to 90° phase shift per pole, and because $180^0$of shift is required for oscillation, at least two poles must be used in the oscillator design. An LC circuit has two poles, thus it contributes up to 180 phase shift per pole pair. But LC and LR oscillators are not considered here because low frequency inductors are expensive, heavy, bulky, and highly nonideal. LC oscillators are designed in high frequency applications, beyond the frequency range of voltage feedback op amps, where the inductor size, weight, and cost are less significant. Multiple RC sections are used in low frequency oscillator design in lieu of inductors.

Phase shift determines the oscillation frequency because the circuit oscillates at whatever frequency accumulates a 180° phase shift. The sensitivity of phase to frequency, dϕ/dω, determines the frequency stability. When buffered RC sections (an op amp buffer provides high input and low output impedance) are cascaded, the phase shift multiplies by the number of sections, n as shown in Fig. 4.2.

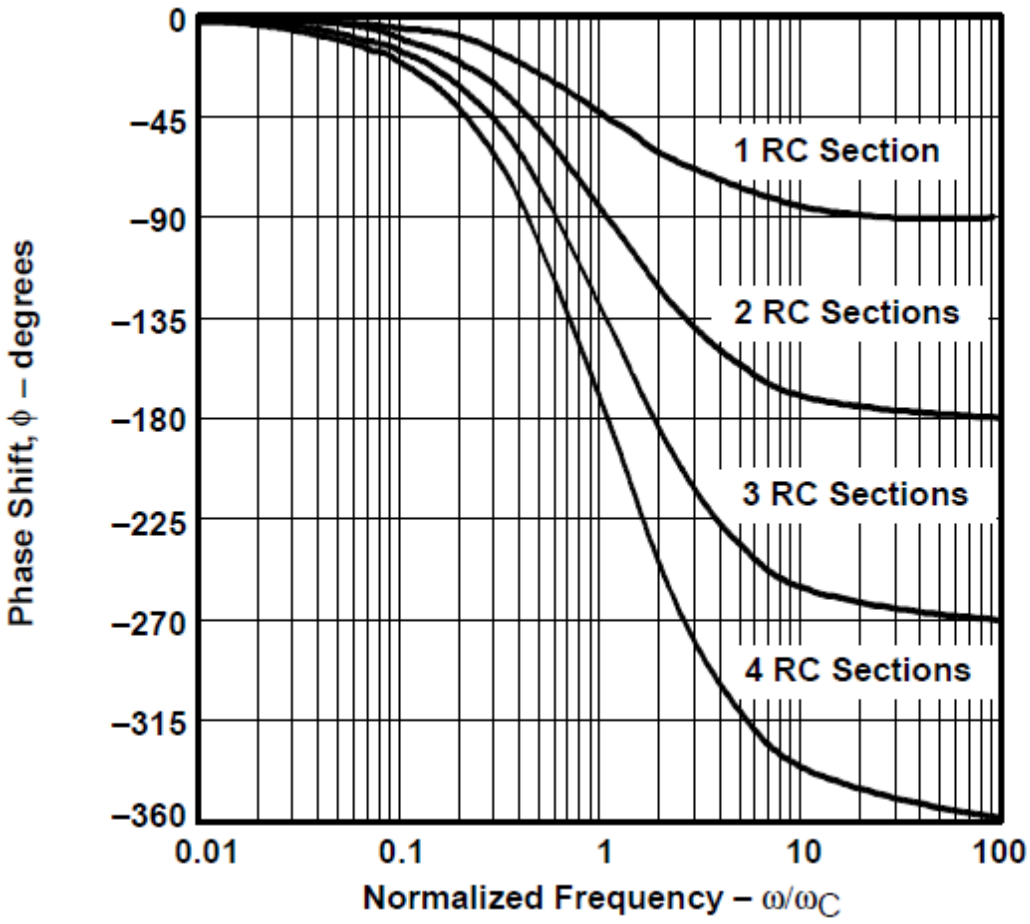

Fig. 4.2 Phase Plot of RC Sections

In the region where the phase shift is 180°, the frequency of oscillation is very sensitive to the phase shift. Thus, a tight frequency specification requires that the phase shift, dϕ, be kept within exceedingly narrow limits for there to be only small variations in frequency, dω, at 180°. Figure 4.2 demonstrates that, although two cascaded RC sections eventually provide 180° phase shift, the value of dϕ/dω at the oscillator frequency is unacceptably small. Thus, oscillators made with two cascaded RC sections have poor frequency stability. Three equal cascaded RC filter sections have a much higher dϕ/dω (see Figure 4.2), and the resulting oscillator has improved frequency stability. Adding a fourth RC section produces an oscillator with an excellent dϕ/dω (see Figure 2); thus, this is the most stable RC oscillator configuration. Four sections are the maximum number used because op amps come in quad packages, and the four-section oscillator yields four sine waves 45° phase

shifted relative to each other. This oscillator can be used to obtain sine/cosine or quadrature sine waves.

4.1.2 Gain in the Oscillator

The oscillator gain must be unity ($A\beta = 1\angle -180°$) at the oscillation frequency. Under normal conditions, the circuit becomes stable when the gain exceeds unity, and oscillations cease. However, when the gain exceeds unity with a phase shift of –180°, the nonlinearity of the active device reduces the gain to unity and the circuit oscillates. The nonlinearity becomes significant when the amplifier swings close to either power rail because cutoff or saturation reduces the active device (transistor) gain. The paradox is that worst-case design practice requires nominal gains exceeding unity for manufacturability, but excess gain causes increased distortion of the output sine wave.

When the gain is too low, oscillations cease under worst case conditions, and when the gain is too high, the output wave form looks more like a square wave than a sine wave. Distortion is a direct result of excessive gain overdriving the amplifier; thus, gain must be carefully controlled in low-distortion oscillators. Phase-shift oscillators have distortion, but they achieve low-distortion output voltages because cascaded RC sections act as distortion filters. Also, buffered phase-shift oscillators have low distortion because the gain is controlled and distributed among the buffers.

4.2 OTRA BASED OSCILLATORS

Different types of sinusoidal oscillators using the operational amplifier (op amp) as the active element are available in the literature [1]. It is well known that the finite gain bandwidth product of the op amp affects both the condition and frequency of oscillation [1,2]. To overcome this problem, several oscillators have been introduced in the literature using the current conveyor as the active element [3–6] or the current feedback operational amplifier [7,8].

Oscillator circuit using OTRA can be realized by various configurations of which some depicted below proposed by K.N. salama and A.M. Soliman.

4.2.1 The Single OTRA Oscillators

Fig. 4.3 represents the generalized configuration of the single OTRA oscillator.

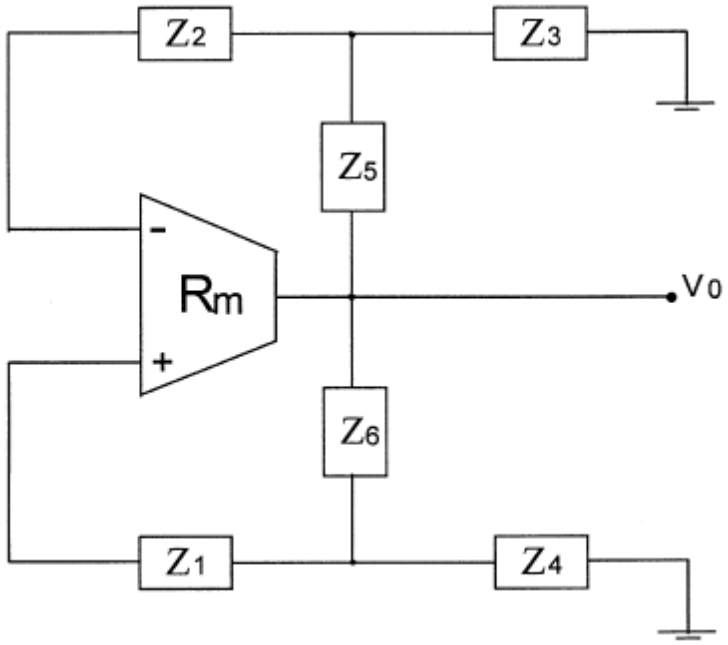

Fig. 4.3 Single OTRA Generalized Oscillator

Assuming an ideal OTRA the characteristic equation is given by:

$$z_2 + z_5\left(1 + \frac{z_2}{z_3}\right) = z_1 + z_6\left(1 + \frac{z_1}{z_4}\right) \tag{4.6}$$

Several oscillator circuits can be generated based on the generalized configuration of Fig. 4.3. One special case is given in Fig. 4.4 and is described in this section.

In order to achieve independent control on the condition of oscillation without affecting the frequency of oscillation, the circuit shown in Fig. 4.4 is derived from the general configuration of Fig. 4.3. For this circuit, the condition of oscillation is given by:

$$\frac{R_1}{R_2} + \frac{C_2}{C_1} = 1 + \frac{R_3}{R_2} \tag{4.7}$$

Fig. 4.4 represents a non canonic single OTRA oscillator. The radian frequency of oscillation is given by:

$$\omega_0 = \frac{1}{\sqrt{C_1 C_2 R_1 R_2 \left(1-\frac{R_3}{R_1}\left(1+\frac{c_3}{c_2}\right)\right)}} \tag{4.8}$$

It is seen that ω_0 can be independently controlled by varying c_3 without affecting the condition of oscillation.

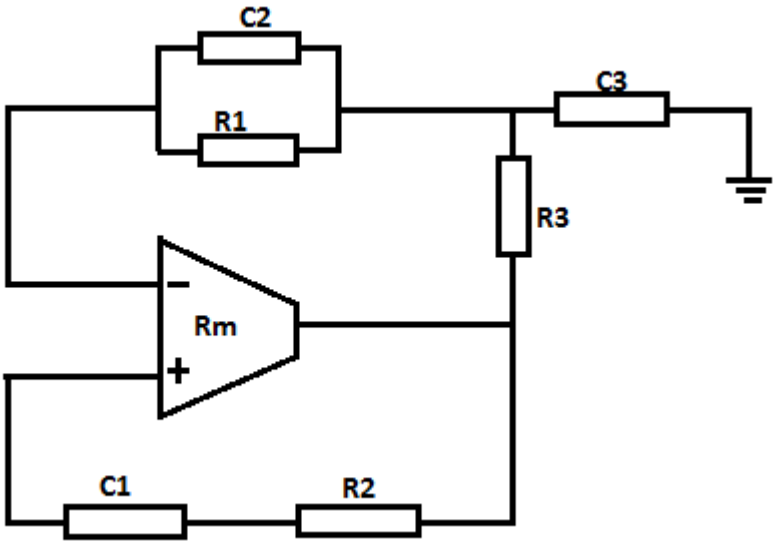

Fig. 4.4 Single OTRA oscillator

4.2.1.1 PSPICE Schematic and Simulation results of single OTRA oscillator

Results of single OTRA oscillator of fig 4.4 are verified through PSPICE simulations using the CMOS implementation of the OTRA [9].The schematic of single OTRA oscillator is given in Fig. 4.5.. The component values chosen are R1=R2=20K, R3=5K and C1=40pF, C2=20Pf.

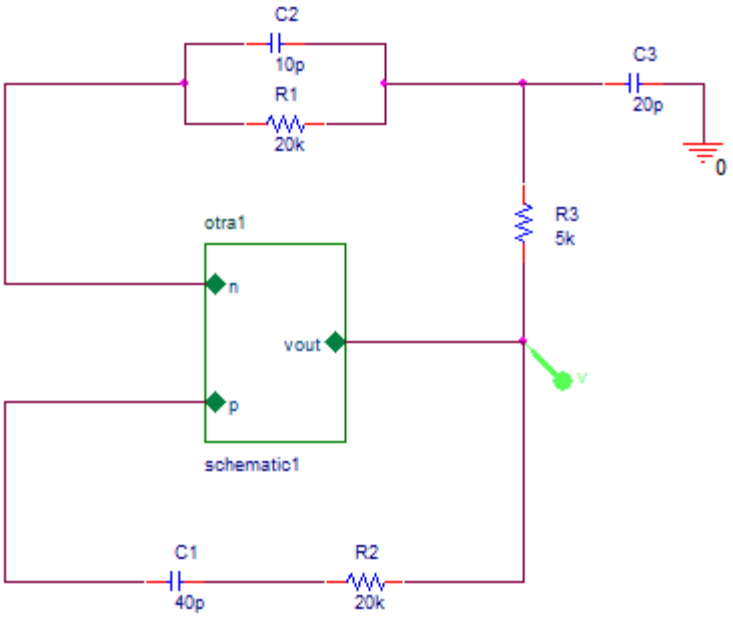

Fig. 4.5 PSPICE schematic of single OTRA oscillator

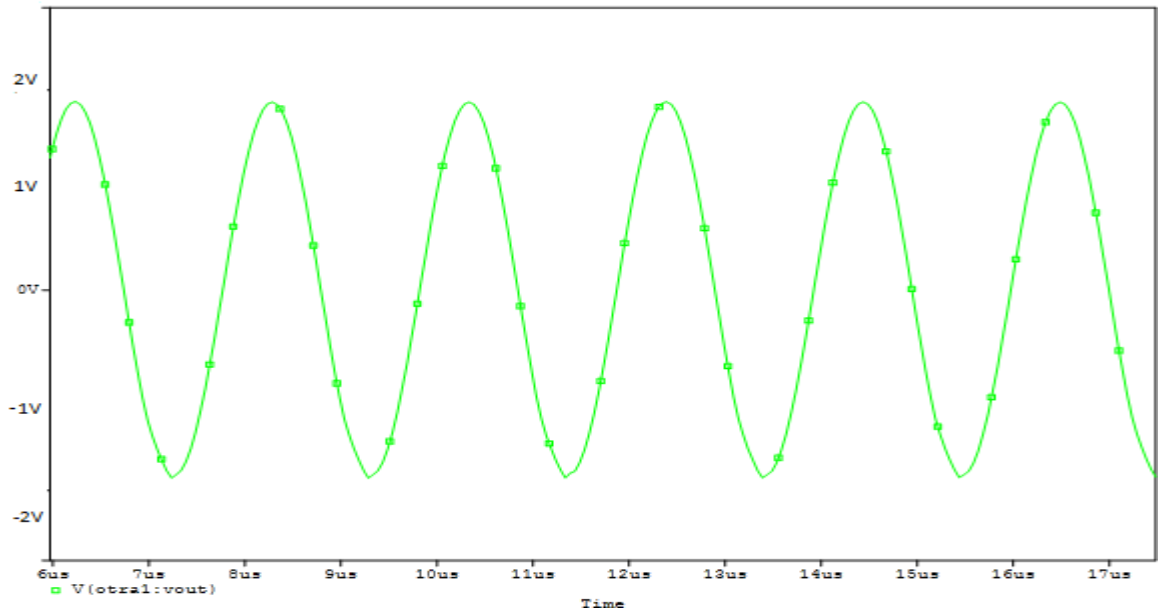

Fig. 4.6 transient response of single OTRA oscillator

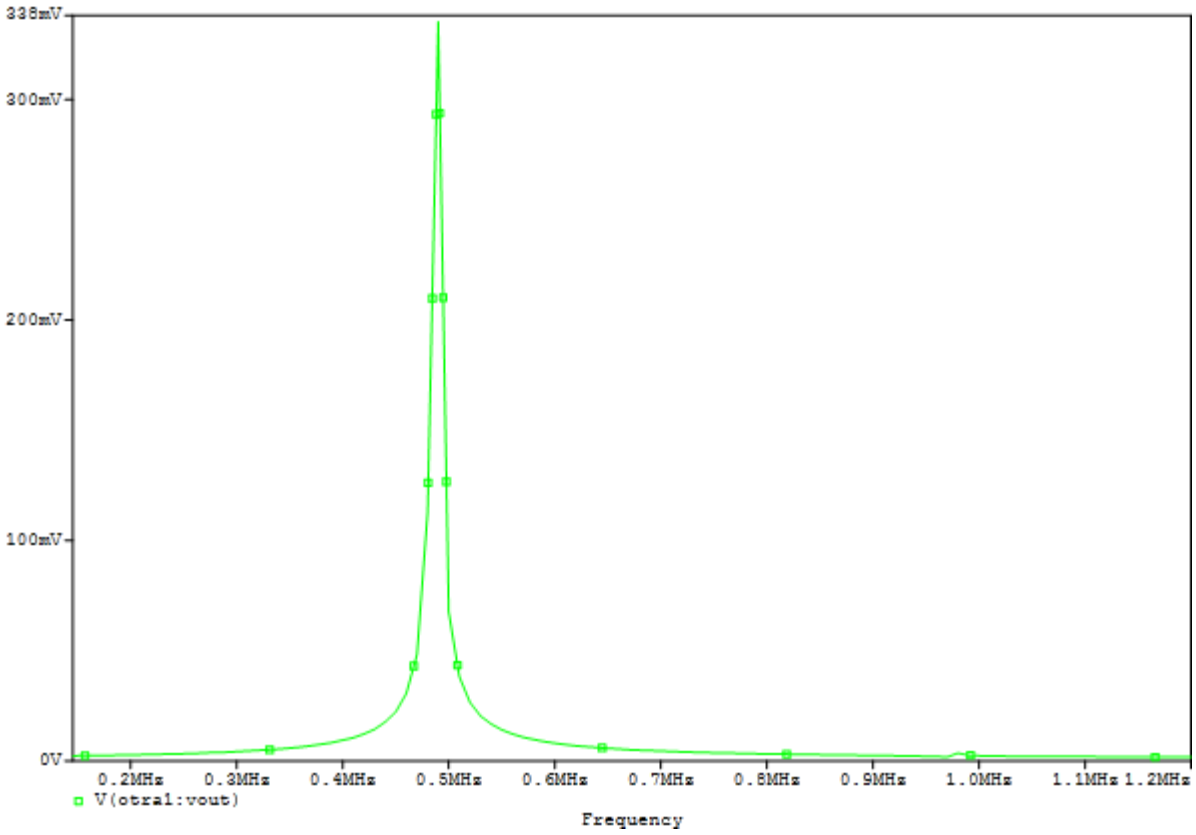

Fig. 4.7 Frequency spectrum of single OTRA oscillator

4.2.2 The Quadrature Oscillator

In this section novel quadrature oscillator using two OTRAs is shown. This oscillator employs the minimum number of capacitors, namely two plus four or five resistors.

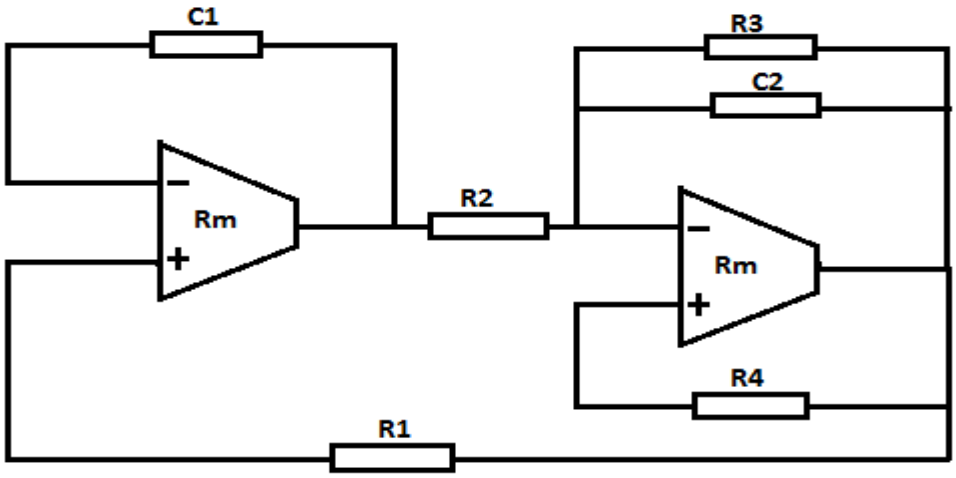

Fig. 4.8 Configuration of quadrature oscillator

The state matrix equation for the oscillator shown in Fig.4.8 is given by:

$$\begin{bmatrix} \frac{dv_1}{dt} \\ \frac{dv_2}{dt} \end{bmatrix} = \begin{bmatrix} 0 & \frac{1}{C_1R_1} \\ -\frac{1}{C_2R_2} & \frac{1}{C_2}\left(\frac{1}{R_4} - \frac{1}{R_3}\right) \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \tag{4.9}$$

The frequency of oscillation (ω_0) and condition of oscillation is given by:

FO: $$\omega_0 = \sqrt{\frac{1}{C_1C_2R_1R_2}} \tag{4.10}$$

CO: $$R_3 = R_4 \tag{4.11}$$

It is seen that either *R*3 or *R*4 can be adjusted to control the condition of oscillation without affecting v_0. Also v_0 can be adjusted by varying *R*1 or *R*2 without disturbing the condition of oscillation. This circuit is considered to be a two-phase oscillator or quadrature oscillator.

4.2.2.1 PSPICE Schematic and Simulation results

Results of two OTRA quadraure oscillator of fig 4.4 are verified through PSPICE simulations using the CMOS implementation of the OTRA [9].The schematic of two OTRA quadrature oscillator is given in Fig. 4.5.. The component values chosen are R1=R3=10K, R2=R5=5K and C1=C2=45Pf.

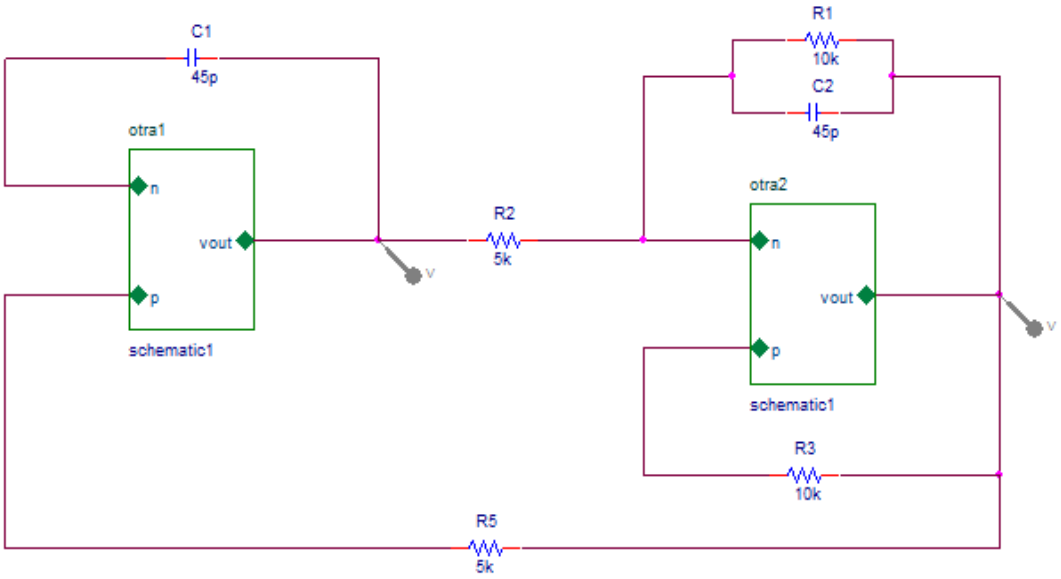

Fig. 4.9 PSPICE schematic of Quadrature oscillator

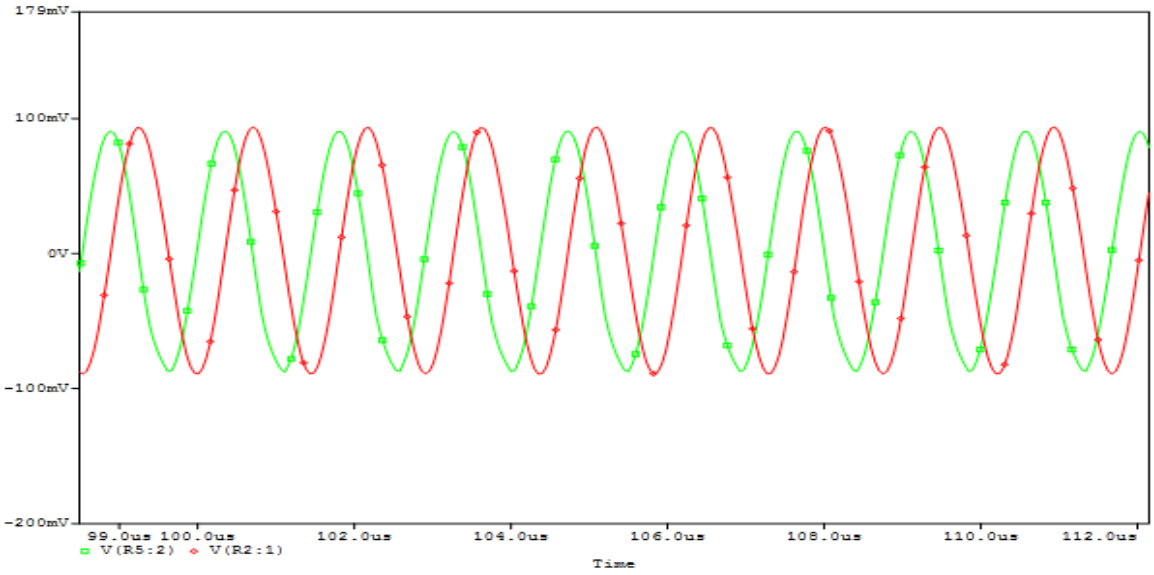

Fig. 4.10 transient response of quadrature oscillator

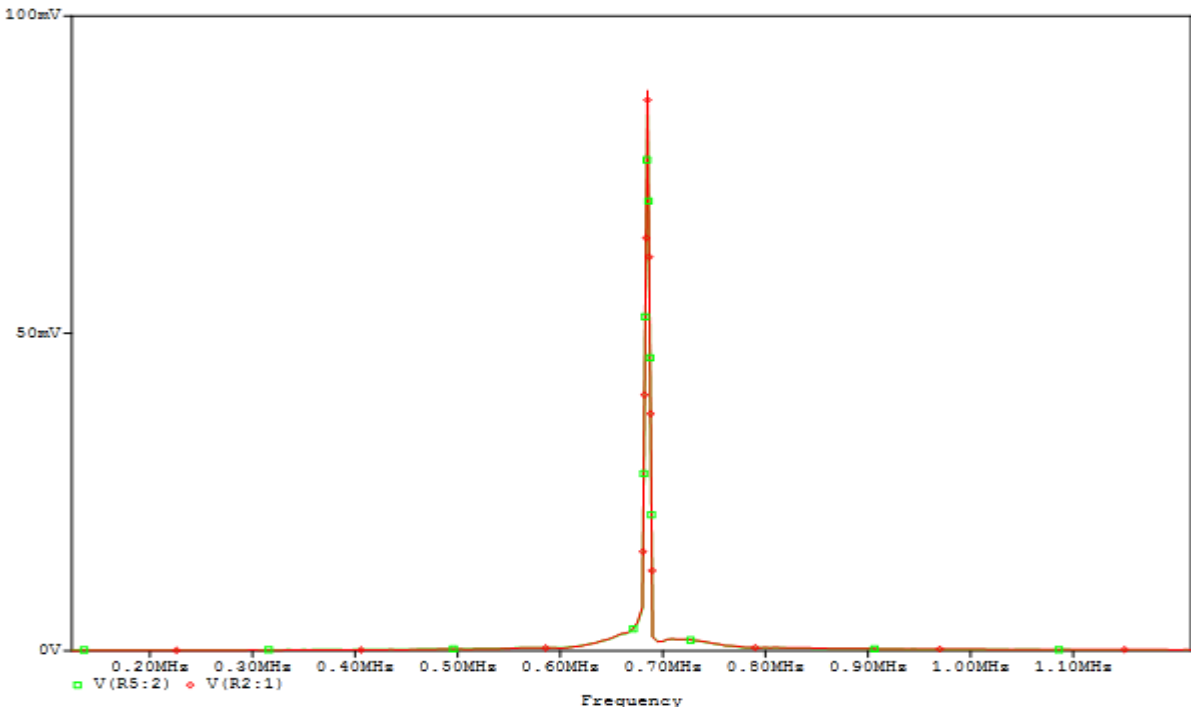

Fig. 4.11 Frequency spectrum of Quadrature oscillator

4.3 OSCILLATOR USING OTRA WITH NON INTERACTIVE CONTROL

The oscillator configuration is shown in Fig. 4.12 which makes use of two lossless integrator, connected in non inverting mode and inverting mode respectively.

The characteristic equation of this oscillator can be deduced as:

$$s^2C_1C_2 + s(C_1G_3 - C_2G_1) + G_1G_2 = 0 \quad (4.12)$$

The frequency of oscillation (FO) and condition of oscillation (CO) are derived as:

FO: $$f = \frac{1}{2\pi}\sqrt{\frac{G_1G_2}{C_1C_3}} \quad (4.13)$$

CO: $$C_1G_3 = C_2G_1 \quad (4.14)$$

From (4.12) it is clear that the circuit Fig. 4.12 is stable and it will always produce oscillations.

The frequency of oscillations can be adjusted by proper selection of resister and capacitor values.

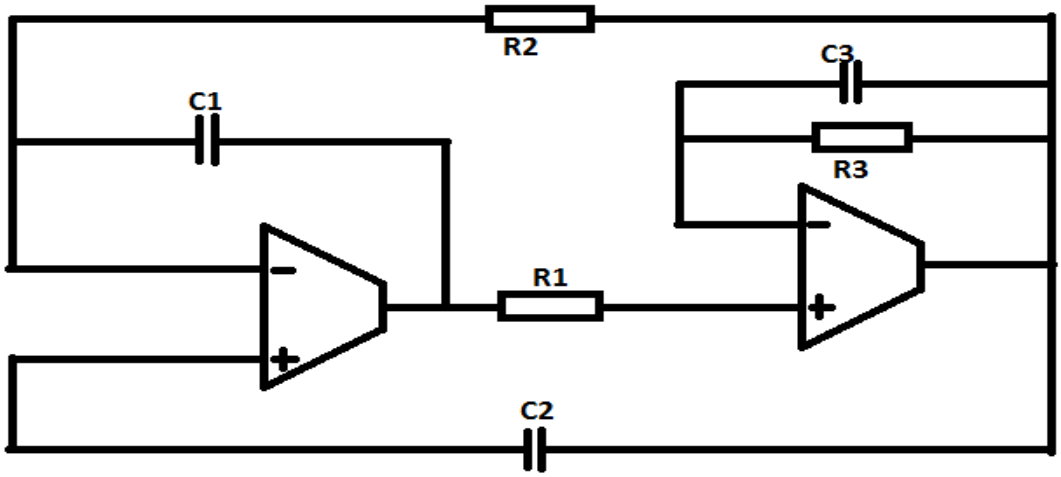

Fig. 4.12 oscillator using OTRA with non interactive control

The current differencing property of the OTRA makes it possible to implement the resistors connected to the input terminals of OTRA, using MOS transistors with complete non linearity cancellation [14]. Each resistor requires two matched n-MOSFETs connected in a manner as shown in Fig 4.13 which represents a typical MOS implementation of resistance connected at negative input of OTRA.

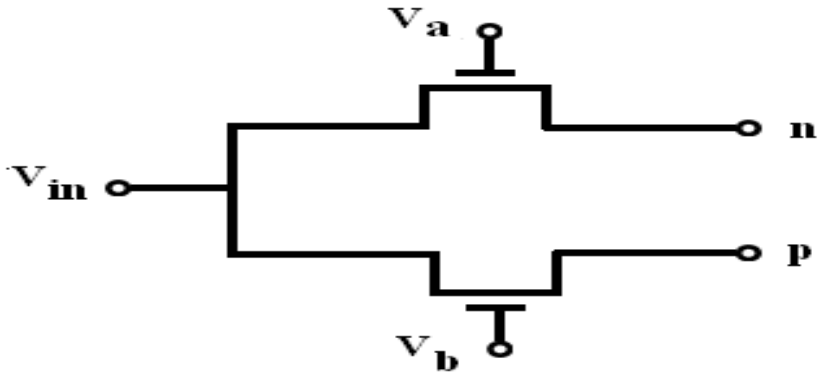

Fig. 4.13 The MOS based Resistor

Symbols 'p' and 'n' represent the non-inverting and the inverting terminals of the OTRA. As can be seen from the figure, the voltages at the drain and the source terminals for both MOSFETs are equal. On taking the difference of the currents flowing in the two transistors, the non linearity gets cancelled out. The resistor value realized can be expressed as:

$$R = \frac{1}{K_N(V_a - V_b)} \tag{4.15}$$

Where

$$K_N = \mu\, C_{OX}\, \frac{W}{L} \tag{4.16}$$

K_N needs to be determined for the transistors being used to implement the resistors and μ, C_{OX} and W/L represent standard transistor parameters.

4.3.1 PSPICE Schematic and Simulation results

The sinusoidal oscillator is verified through simulations using the CMOS implementation of the OTRA [8]. The PSPICE simulations are performed using 0.5 μm CMOS process parameters provided by MOSIS (AGILENT). Supply voltages taken are ±1.5V. The resistor and capacitor values are taken as R_1=2K, R_2=50K, R_3=30K, C_1=20p, C_2=30p, C_3=200p. The Proposed Oscillator is designed for an FO of 159 KHz and the simulated value was observed to be 160KHz. The simulated transient output and corresponding frequency spectrum for Oscilllator are depicted in Fig. 4.15 and Fig. 4.16.

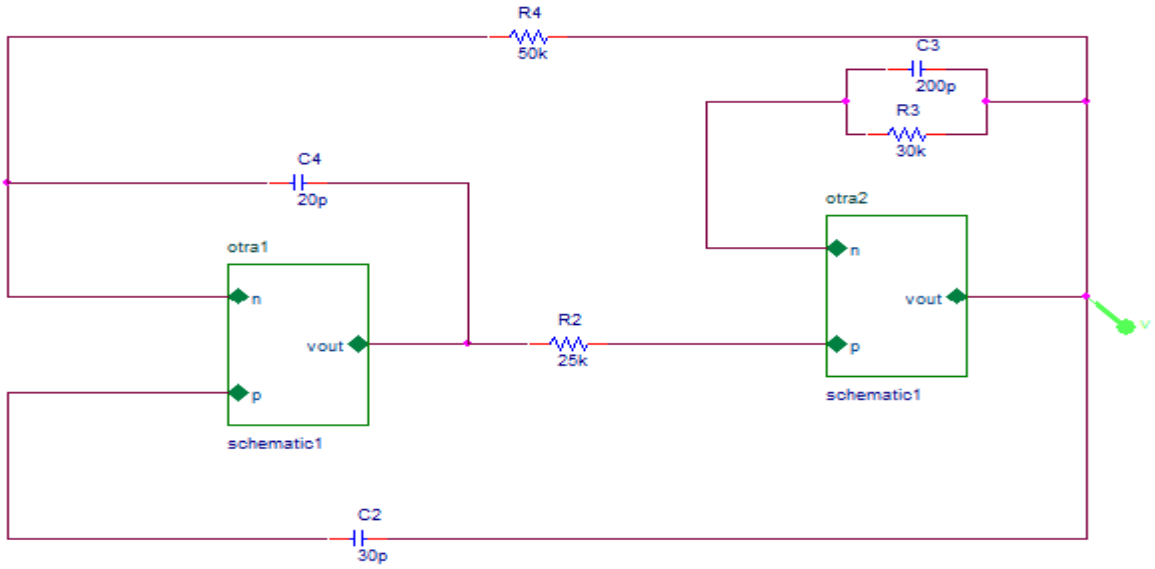

Fig. 4.14 PSPICE schematic of oscillator

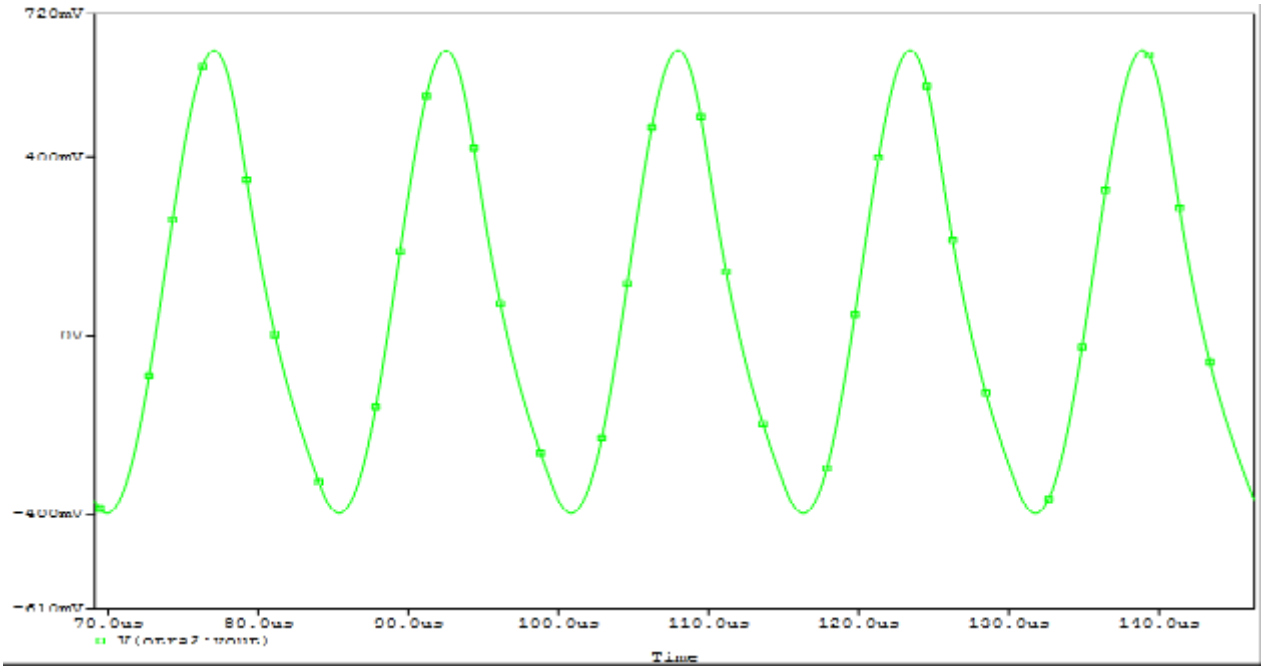

Fig. 4.15 Transient output of oscillator

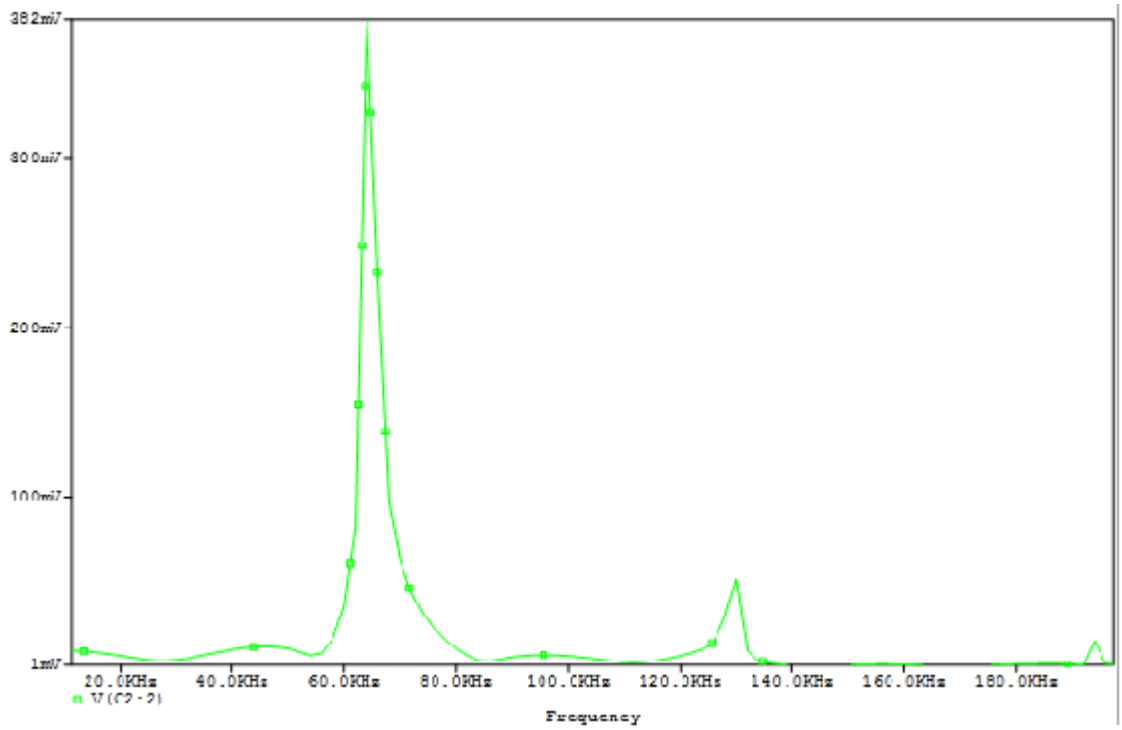

Fig. 4.16 Frequency spectrum of oscillator

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CHAPTER 5

OTRA BASED NON-LINEAR APPLICATIONS

5.1 Introduction

Electrical devices are built from nonlinear components. In order to understand the design of these devices, a fundamental understanding of nonlinear circuits is necessary. Moreover, non-linear circuit is where the real engineering comes in. That is, there are no hard and fast rules to analyze most non-linear circuits. To analyze non-linear circuits, the approach used depends on the type of circuit, generally the simplest approach is utilized.

It is easy to understand the difference between a linear and a nonlinear circuit by looking at the difference between a linear and a nonlinear equation:

$$y = x \tag{5.1}$$

$$y = x + 3 \tag{5.2}$$

$$y = x^2 \tag{5.3}$$

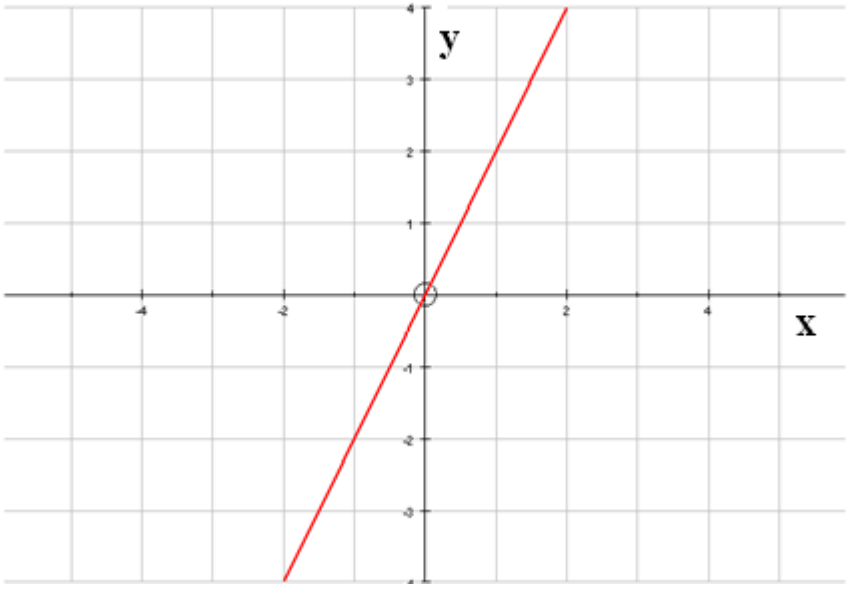

Figure 5.1 graph for equation 5.1 showing linear characteristic

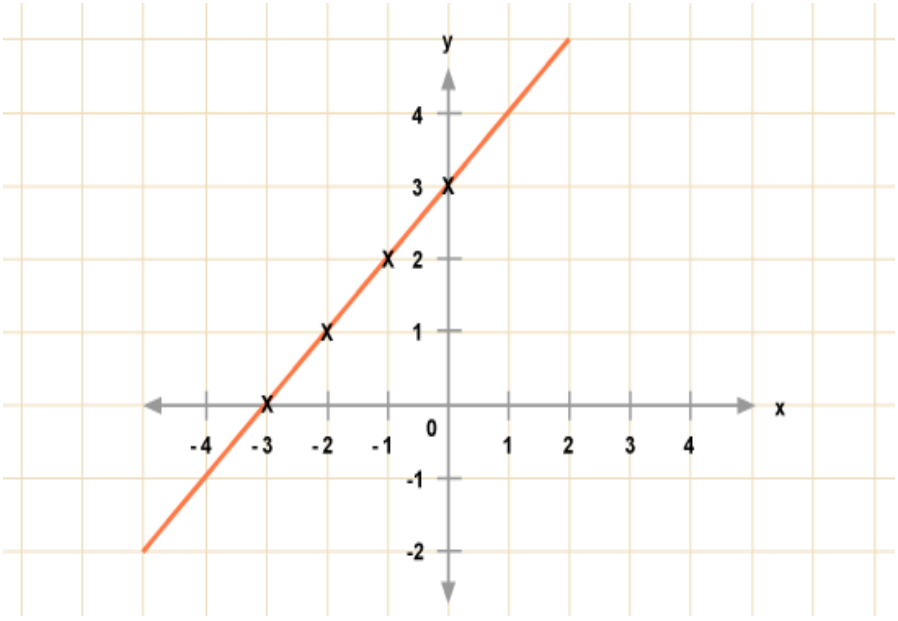

Figure 5.2 graph for equation 5.2 showing non linear characteristic

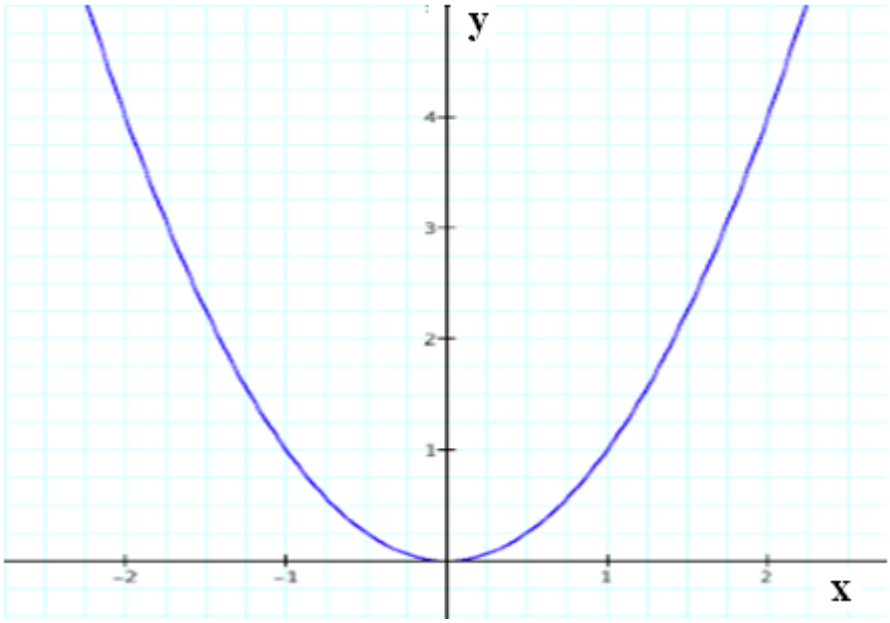

Figure 5.3 Graph for equation 5.3 showing non linear characteristic

Analog Integrated Circuit Design using CMOS non linear circuit become increasingly important with growing opportunities. Coupled with the various technological improvements such as the continuously shrinking feature size of the devices on IC's and the most attractive reduction of power

supply voltages and power dissipation. This has led to creation of alternate analog design techniques. Some nonlinear applications i.e analog multiplier, squarer, monostable multivibrator using OTRA has been implemented and simulated in the following sections using PSPICE model.

5.2 Analog Multiplier Circuit

Analog multipliers find extensive application in the field of telecommunication, control, instrumentation, measurement, and signal processing . A number of circuits are reported in literature relating to analog multipliers [1-4]. Circuits presented in [1-3] are based on Gilbert multiplier [5] and are suitable for CMOS integrated technology. Recently the OTRA has emerged as an alternate analog building block [6-9] which inherits all the advantages of current mode techniques. The OTRA is a high gain current input voltage output device. The input terminals of OTRA are internally grounded, thereby eliminating response limitations due to parasitic capacitances and resistances at the input. Several non-linear circuits use single active element such as classical voltage op-amp, current conveyor, current feedback amplifier or a four terminal floating nullor. A novel operational transresistance amplifier based analog multiplier with CMOS devices is presented here. It uses single OTRA, and few CMOS devices. The multiplier circuit provides its output as the multiplication of its two inputs.

5.2.1 Circuit Description

The circuit of OTRA [8] based basic multiplier is shown in Fig.5.4. The transistors M1, M2 M3, and M4 are matched transistors and operate in the linear region. v_1 and v_2 represent small signals, whereas V_{c1}, V_{c2}, and V_{DC} are the bias voltages. OTRA inputs keep the sources of the two transistorsM1 and M2 virtually grounded. The drain current for the MOS transistor operating in triode region is given by [10].

$$I_D = k\frac{W}{L}\left((V_{GS} - V_T) - \frac{V_{DS}}{2}\right)V_{DS} \tag{5.4}$$

where *k* is transconductance; *W* and *L* respectively represent the channel width and length of the of the MOSFET. The other terms have their usual meaning.

Using (5.4) the currents through *p* and *n* terminals of OTRA, that is, i_p and i_n respectively, can be expressed as:

$$i_p = K_n\frac{W}{L}\left(((V_{DC} + v_1) - V_T) - \frac{v_2}{2}\right)v_2 + K_n\frac{W}{L}\left(V_{C1} - V_T) - \frac{v_o}{2}\right)v_o \tag{5.5}$$

$$i_n = K_n\frac{W}{L}\left(V_{DC} - V_T) - \frac{v_2}{2}\right)v_2 + K_n\frac{W}{L}\left(V_{C2} - V_T) - \frac{v_o}{2}\right)v_o \tag{5.6}$$

As R_m approaches infinity the input currents are forced to be equal resulting in

$$v_o = \frac{v_1 v_2}{(V_{C2} - V_{C1})} = Kv_1v_2 \tag{5.7}$$

where *K* is a proportionality constant and is the inverse differences of gate voltage of M_3 and M_4.

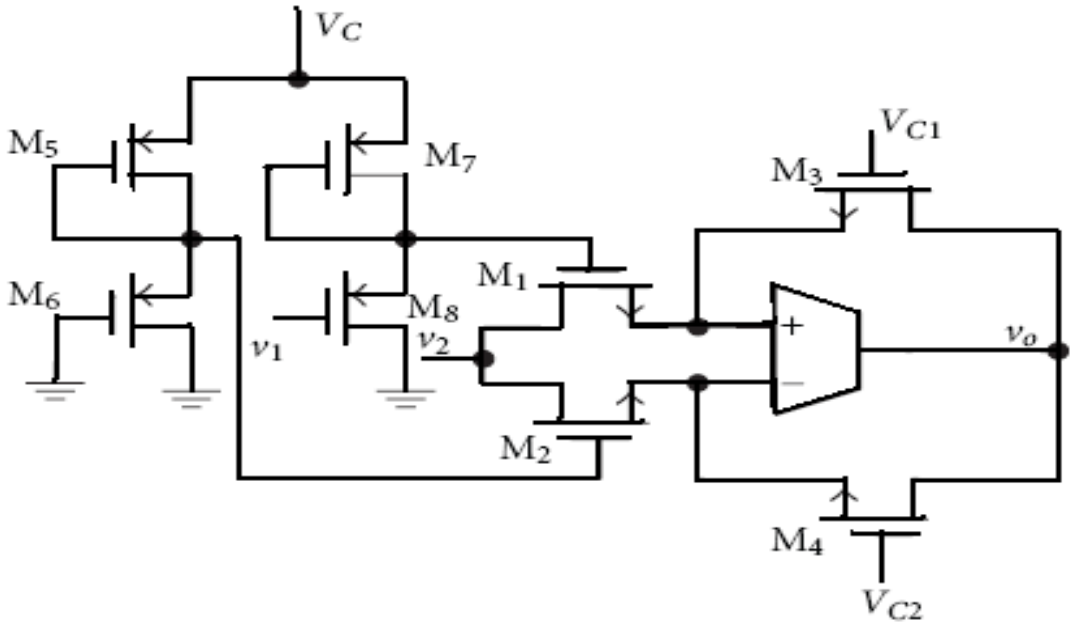

Fig. 5.4 Complete Analog Multiplier circuit using OTRA

5.2.2 Simulation Results

The OTRA multiplier results is shown using OTRA [8]. The PSPICE schematic of the multiplier is shown in Fig 5.5.

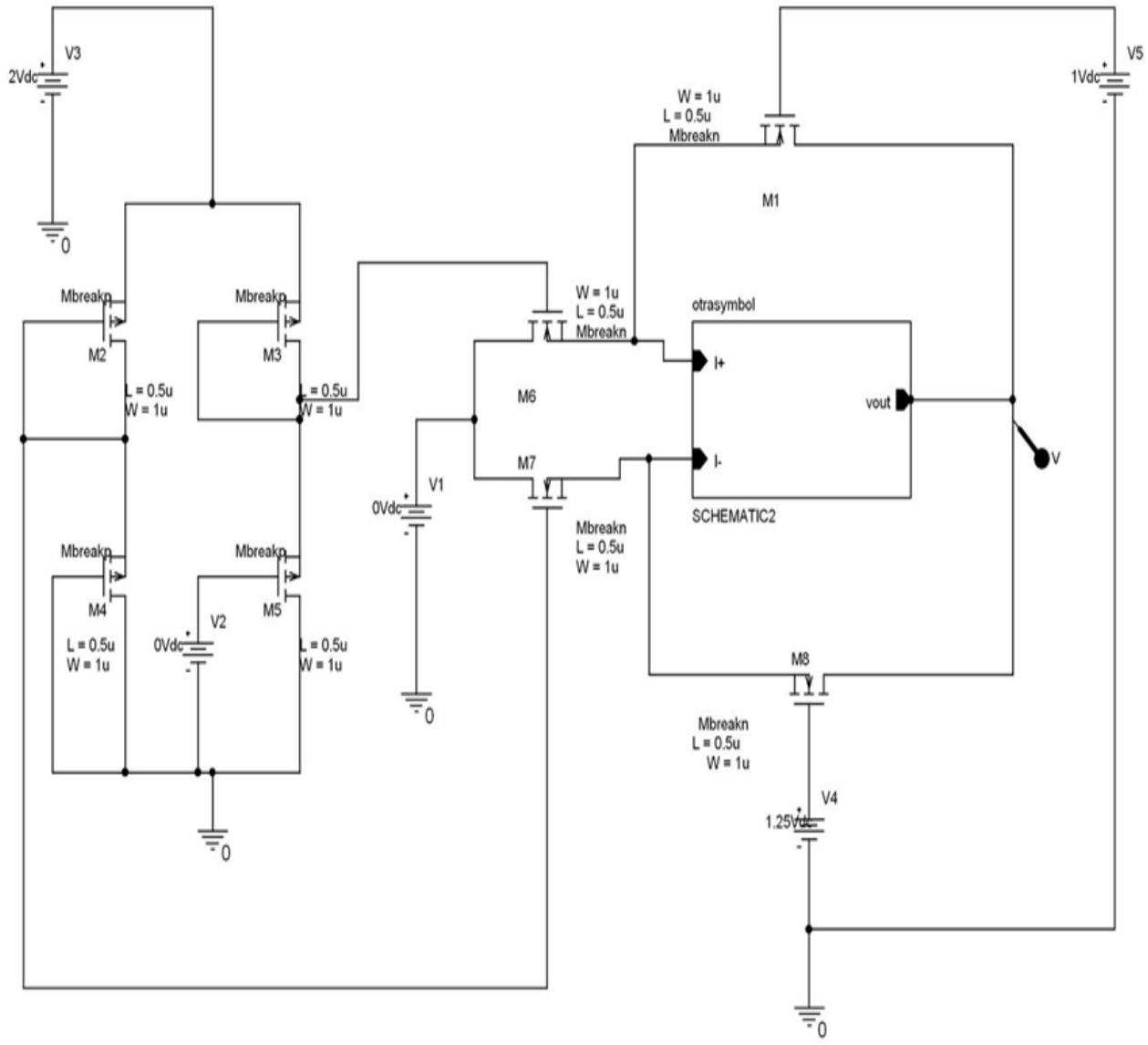

Fig. 5.5 PSPICE Schematic of complete Multiplier circuit using OTRA

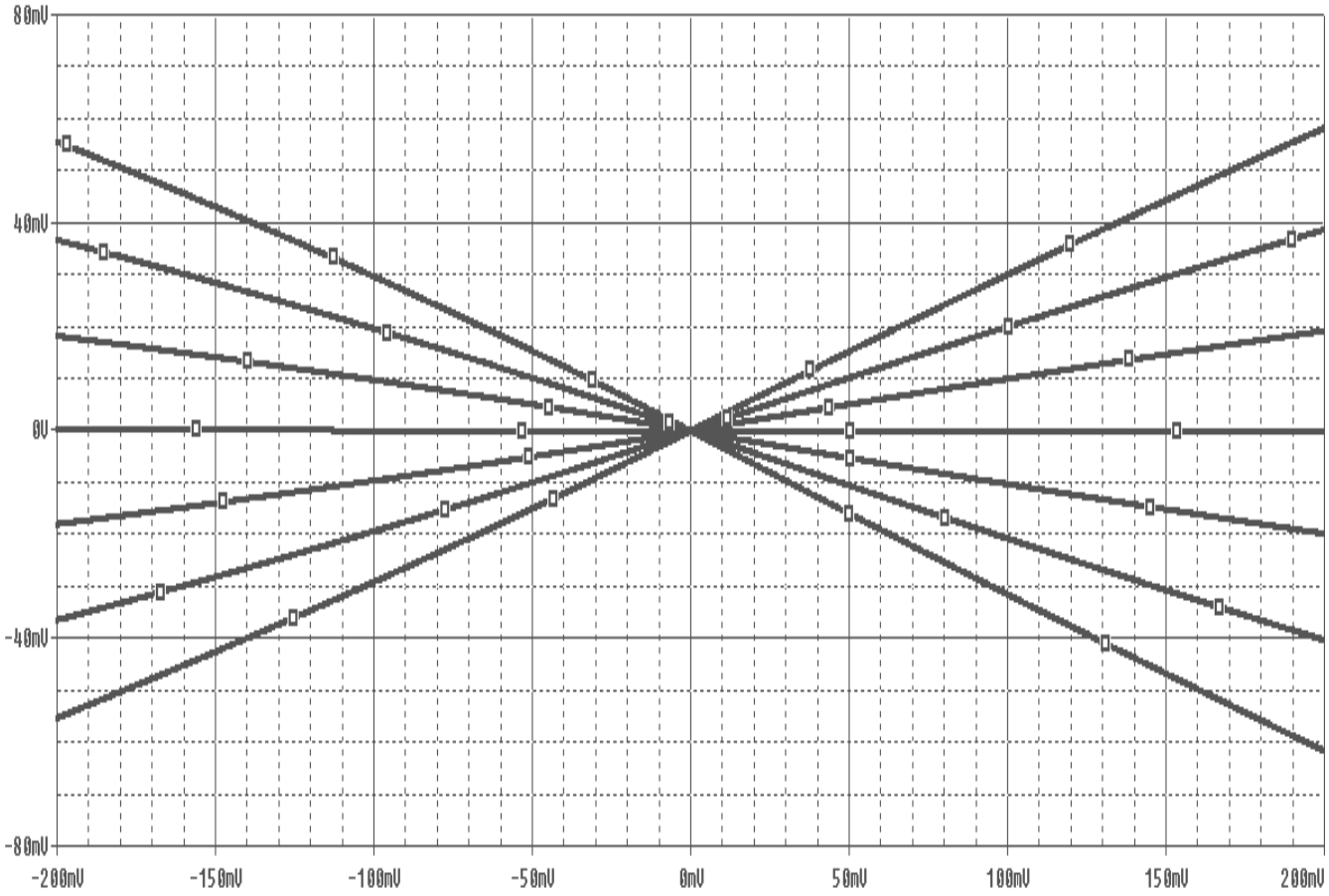

Fig 5.6 DC Characteristic of Complete Multiplier using OTRA

5.3 Squarer Circuit

Squarer circuit can be implemented using OTRA with minor change in input voltage (if V1=V2) in analog multiplier circuit shown above. The multiplier can be used as a squarer circuit if v1 = v2 = vin.

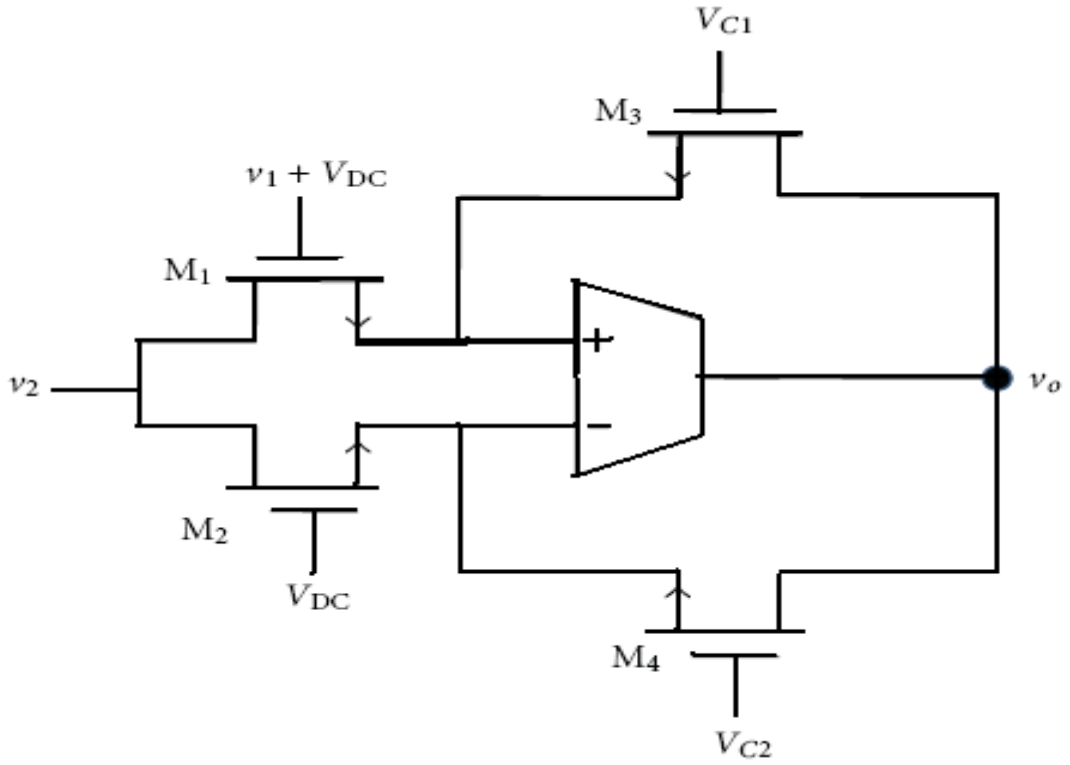

Fig 5.7 Basic Multiplier circuit using OTRA

OTRA inputs keep the sources of the two transistors M1 and M2 virtually grounded. The transistors M1, M2 M3, and M4 are matched transistors and operate in the linear region. V_1 and V_2 represent small signals, V_{C1},V_{C2}, and V_{DC} are the bias voltages.

The drain current for the MOS transistor operating in triode region is given by [10]:

$$\mathrm{I_d} = k\frac{w}{L}\left(\left(V_{gs} - V_t\right) - \frac{Vds}{2}\right)Vds \tag{5.8}$$

Where *k* is transconductance; *W* and *L* respectively represent the channel width and length of the of the MOSFET. The currents through *p* and *n* terminals of OTRA, that is, $I_p$and I_n respectively, can be expressed as:

$$\mathrm{I_p} = k_n \frac{w}{L}\left((V_{DC} + v_1) - V_t) - \frac{V_2}{2}\right)V_2 + k_n \frac{w}{L}\left((V_{C1} - V_t) - \frac{v_0}{2}\right)V_0 \quad (5.9)$$

$$\mathrm{I_n} = k_n \frac{w}{L}\left((V_{DC} - v_t) - V_t) - \frac{V_2}{2}\right)V_2 + k_n \frac{w}{L}\left((V_{C2} - V_t) - \frac{v_0}{2}\right)V_0 \quad (5.10)$$

As *Rm* approaches infinity the input currents are forced to be equal resulting in

$$V_0 = \frac{v_1 v_2}{(Vc1 - Vc2)} = k v_1 v_2 \quad (5.11)$$

where *K* is a proportionality constant and is the inverse of difference of gate voltages of M3 and M4.

For a Squarer circuit V1= V2= Vin then output of the multiplier is given by :

$$v_0 = k\ vin^2 \quad (5.12)$$

5.3.1 Simulation results

Schematic of complete multiplier using OTRA [8] is shown in Fig 5.8. Here V1=V2=Vin.

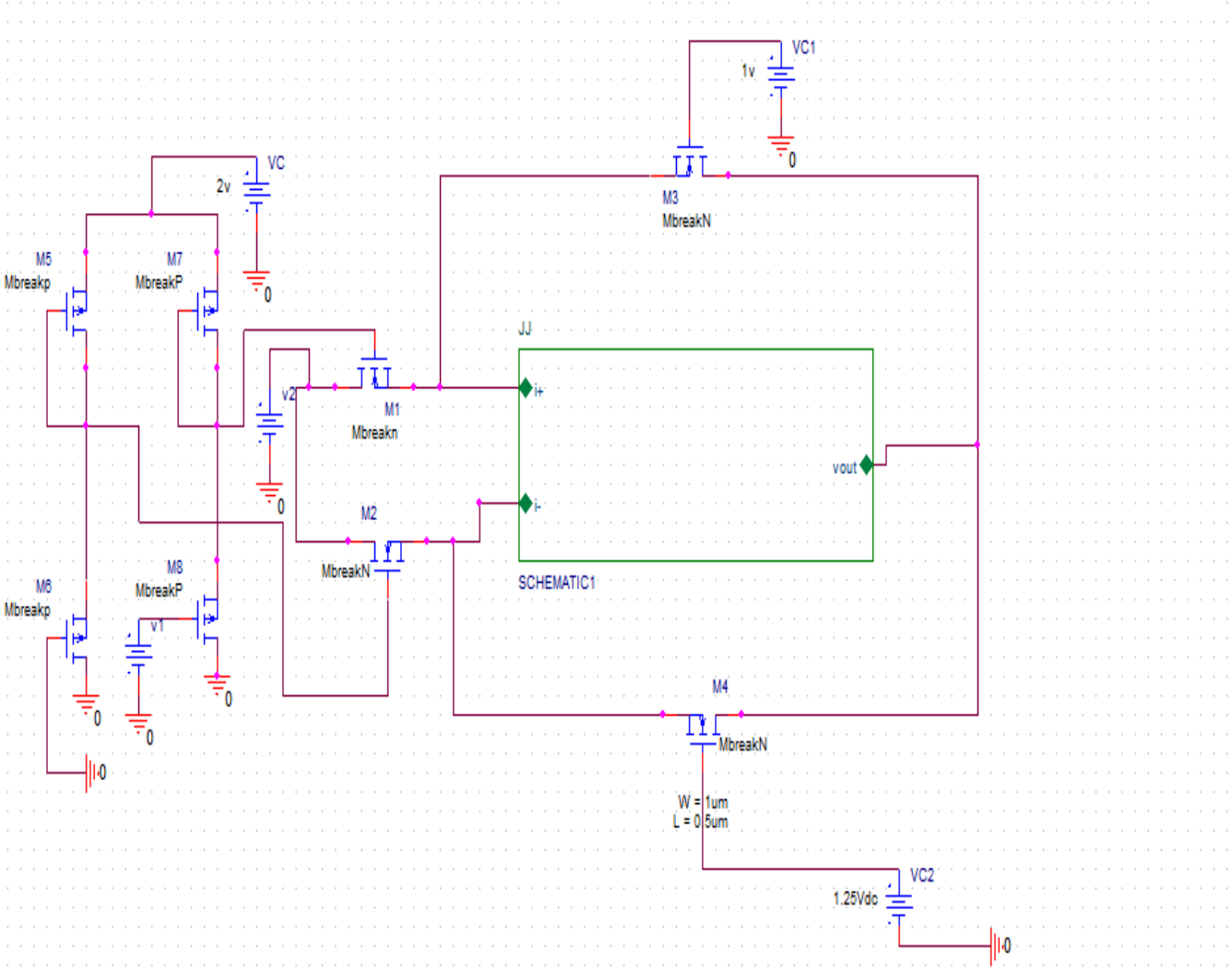

Fig 5.8 PSPICE Schematic of Squarer circuit using OTRA

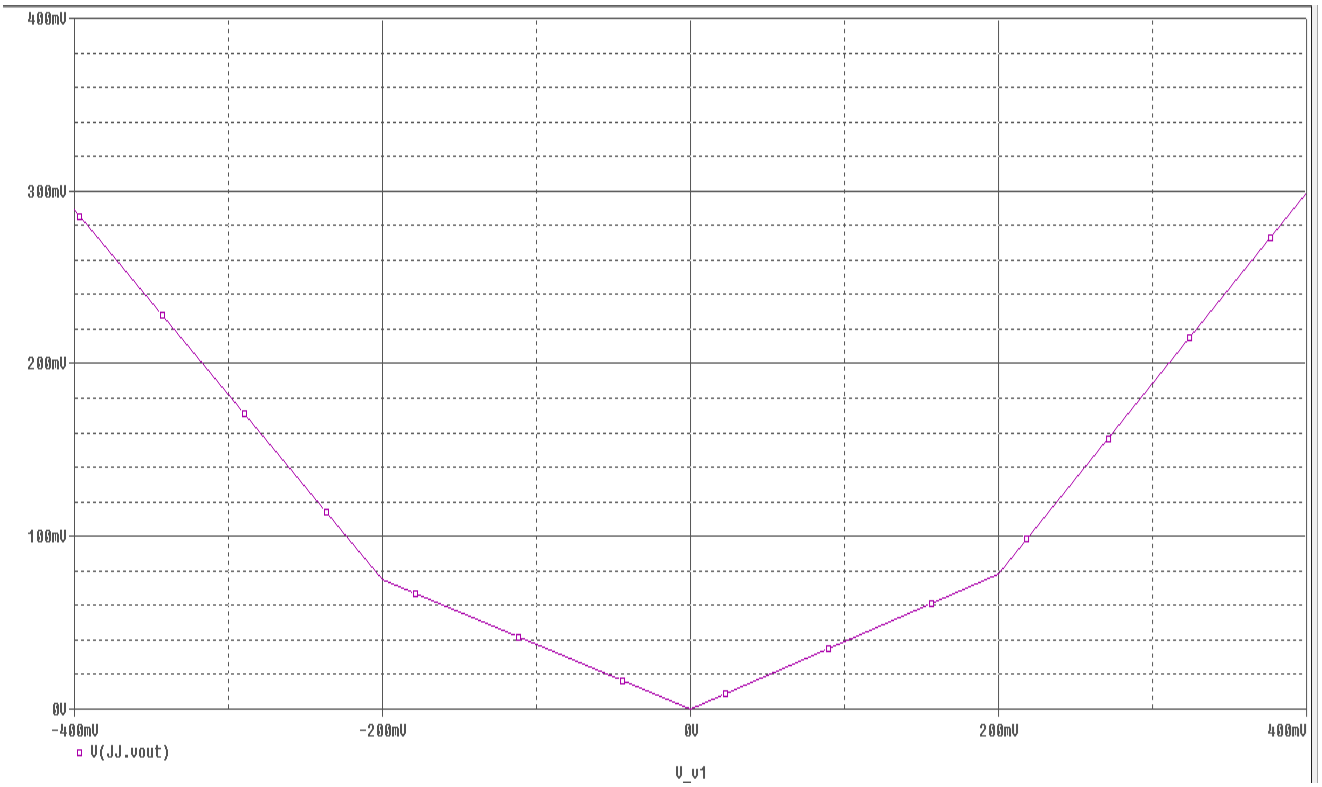

Fig 5.9 PSPICE Simulation of Squarer circuit using OTRA

5.4 Monostable Multivibrator using OTRA

5.4.1 Introduction

A multivibrator is an electronic circuit used to implement a variety of simple two-state systems such as oscillators, timers and flip-flops. It is characterized by two amplifying devices (transistors, electron tubes or other devices) cross-coupled by resistors or capacitors. The name "multivibrator" was initially applied to the free-running oscillator version of the circuit because its output waveform was rich in harmonics. There are three types of multivibrator circuits depending on the circuit operation:

- **astable**, in which the circuit is not stable in either state —it continually switches from one state to the other. It functions as a relaxation oscillator.
- **monostable**, in which one of the states is stable, but the other state is unstable (transient). A trigger pulse causes the circuit to enter the unstable state. After entering the unstable state, the circuit will return to the stable state after a set time. Such a circuit is useful for creating a timing period of fixed duration in response to some external event. This circuit is also known as a **one shot**.
- **bistable**, in which the circuit is stable in either state. It can be flipped from one state to the other by an external trigger pulse. This circuit is also known as a flip flop. It can be used to store one bit of information.

Multivibrators find applications in a variety of systems where square waves or timed intervals are required. For example, before the advent of low-cost integrated circuits, chains of multivibrators found use as frequency dividers. A free-running multivibrator with a frequency of one-half to one-tenth of the reference frequency would accurately lock to the reference frequency. This technique was used in early electronic organs, to keep notes of different octaves accurately in tune. Other applications included early television systems, where the various line and frame frequencies were kept synchronized by pulses included in the video signal.

5.4.2 Monostable multivibrator using OTRA

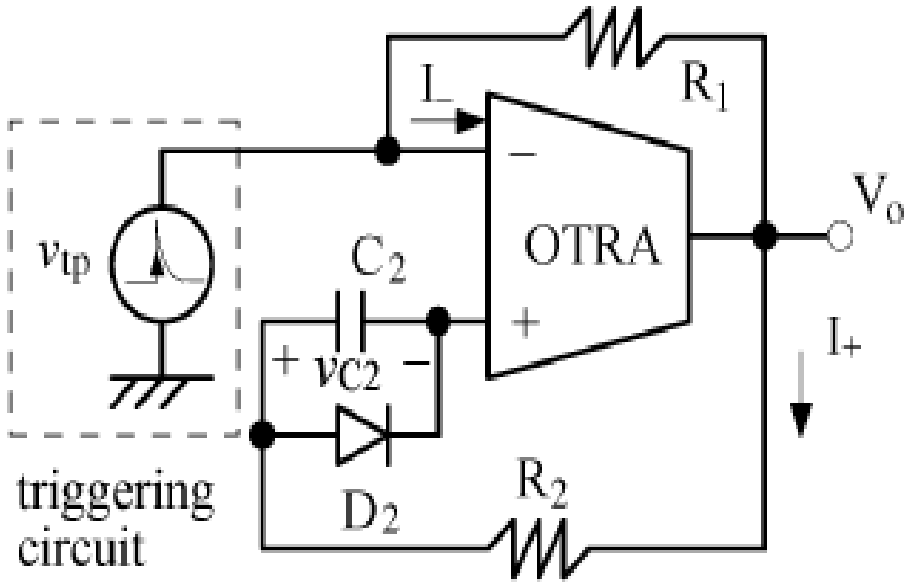

Fig. 5.10 Monostable Multivibrator with positive triggering signal using OTRA

The circuit diagram of the current-mode monostable is shown in Fig. 5.11. The circuit depicted in Fig. 5.11 uses only one OTRA and four passive elements (two resistors, one capacitor, and one diode). This circuit is triggered via a rising-edged signal to produce an output pulse with a predetermined width. Fig. 5.12 shows the corresponding waveforms of the proposed circuits in Fig. 5.11. There are two saturation levels of $V_0, +V_{sat}\ and\ -V_{sat}\ where\ +V_{sat} = |-V_{sat}|$. The initial capacitor voltage is clamped at V_{D2} , the forward conduction voltage drop of the diode. In Fig. 5.12, T is the pulse width, and T_r is the recovery time. The operations of the circuits are divided into stable and quasi-stable states.

A. Quasi stable state

Assuming that the circuit is at its steady state for a long time, C_2 is open circuited, and v_{c2} is clamped by D_2 . Let R_1 be greater than R_2 . Then, I_+ is more positive than I_-. Thus, V_0 is guaranteed to be at the positive saturation level $+V_{sat}$ at the stable states. A triggering signal is

applied at $t = 0$. Since now I_- is more positive than I_+, V_0 jumps from $+V_{sat}$ to $-V_{sat}$. As soon as the triggering signal is removed, the inverting input terminal is grounded. Thus, I_- remains at a dc value of

$$I_-(t) = \frac{-V_{sat}}{R_1}, \qquad \text{for } 0 < t < T \tag{5.13}$$

Since V_0 is equal to $-V_{sat}$, C_2 starts to discharge through R_2 from $t = 0$. The initial and final values of v_{c2} are V_{D2} and $-V_{sat}$, respectively. The capacitor voltage in the quasi-stable state can be expressed as

$$v_{c2}(t) = \left(V_{D2} - (-V_{sat})\right)e^{\frac{-t}{R_2C_2}} + (-V_{sat}) \tag{5.12}$$

Define K as the ratio of V_{D2} to $|-V_{sat}|$, i.e

$$K = \frac{V_{D2}}{|-V_{sat}|} = \frac{V_{D2}}{+V_{sat}} \tag{5.13}$$

By substituting (5.12) in (3.24) $v_{c2}(t)$ can be modified to

$$v_{c2}(t) = (-V_{sat})\left[1 - (K+1)e^{\frac{-t}{R_2C_2}}\right] \tag{5.14}$$

The current into the non inverting input node of the OTRA is

$$I_+(t) = \frac{(-V_{sat}) - v_{c2}(t)}{R_2} = \frac{(-V_{sat})(1+K)}{R_2}e^{\frac{-t}{R_2C_2}} \tag{5.15}$$

As v_{c2} drops toward $-V_{sat}$, I_+ increases until I_+ is more positive (or less negative) than I_-. Then V_0 changes from $-V_{sat}$ to $+V_{sat}$. The period of the quasi-stable state T can thus be determined from the instant that $I_+ = I_-$. From (5.11) and (5.15)

$$I_+(t) = \frac{(-V_{sat})(1+K)}{R_2}e^{\frac{-t}{R_2C_2}} = \frac{-V_{sat}}{R_1} \tag{5.16}$$

$$T = R_2 C_2 ln\left[\frac{R_1}{R_2}(1+K)\right] \quad (5.17)$$

At $t = T$, v_{c2} drops to a lower threshold of V_{TL}. Substituting (5.17) into (5.14) and rearranging the equation can derive

$$V_{TL} = v_{c2}(T) = \left(1 - \frac{R_2}{R_1}\right)(-V_{sat}) \quad (5.18)$$

B. Stable State

From $t = T$, V_0 stays at $+V_{sat}$, and C_2 begins to charge through R_2 from V_{TL} toward its final value $+V_{sat}$. Thus, from (5.14), the capacitor voltage in the stable state is expressed as

$$v_{c2}(t) = \left(V_{TL} - (-V_{sat})\right)e^{\frac{-(t-T)}{R_2 C_2}} + (+V_{sat})$$

$$= (+V_{sat})\left[\left(\frac{R_2}{R_1} - 2\right)e^{\frac{-(t-T)}{R_2 C_2}} + 1\right] \quad \text{For } T < t < T_r \quad (5.19)$$

From (5.19), it can be seen that v_{c2} increases with time. At $t = T + T_r$, v_{c2} grows above V_{D2} and is clamped at that level. Thus

$$V_{D2} = K(+V_{sat}) = v_{c2}(T + T_r) = (+V_{sat})\left[\left(\frac{R_2}{R_1} - 2\right)e^{\frac{-T_r}{R_2 C_2}} + 1\right] \quad (5.20)$$

From (5.20), the recovery time is calculated as

$$T_r = R_2 C_2 ln\left(\frac{2 - {}^{R_2}/_{R_1}}{1-K}\right) \quad (5.20)$$

In the period from T to $(T + T_r)$ the two input currents of the OTRA can be derived, respectively, as

$$I_-(t) = \frac{+V_{sat}}{R_1} \quad (5.21)$$

$$I_+(t) = \frac{(+V_{sat}) - v_{c2}(t)}{R_2}$$

$$= \frac{+V_{sat}}{R_2}\left(2 - \frac{R_2}{R_1}\right) e^{\frac{-(t-T)}{R_2 C_2}} \quad (5.22)$$

From (5.21) and (5.22), it is observed that I_+ is always more positive than I_- in the stable state. V_0 will remain at $+V_{sat}$. Then, if the next triggering signal is applied, the circuits will enter the quasi-stable state again. However, if the circuit illustrated in Fig. 5.11 is triggered during the recovery period, will start to discharge from a voltage level lower than V_{D2}. The result is an immature pulse with a width less than . That is why these proposed monostable multivibrators are non retriggerable. The minimum period between two consecutive triggering signals is ($T + T_r$), which in terms of the circuit components is

$$T + T_r = \mathrm{R_2 C_2 ln}\left(\frac{1+\mathrm{K}}{1-\mathrm{K}} \frac{2\mathrm{R_1} - \mathrm{R_2}}{\mathrm{R_2}}\right) \quad (5.23)$$

Usually V_{D2}, is much less than the saturation values of V_0 . Thus, K can be considered negligible. Then from (5.23), the expression is further simplified to

$$T + T_r = \mathrm{R_2 C_2 ln}\left(\frac{2\mathrm{R_1}}{\mathrm{R_2}} - 1\right) \quad (5.24)$$

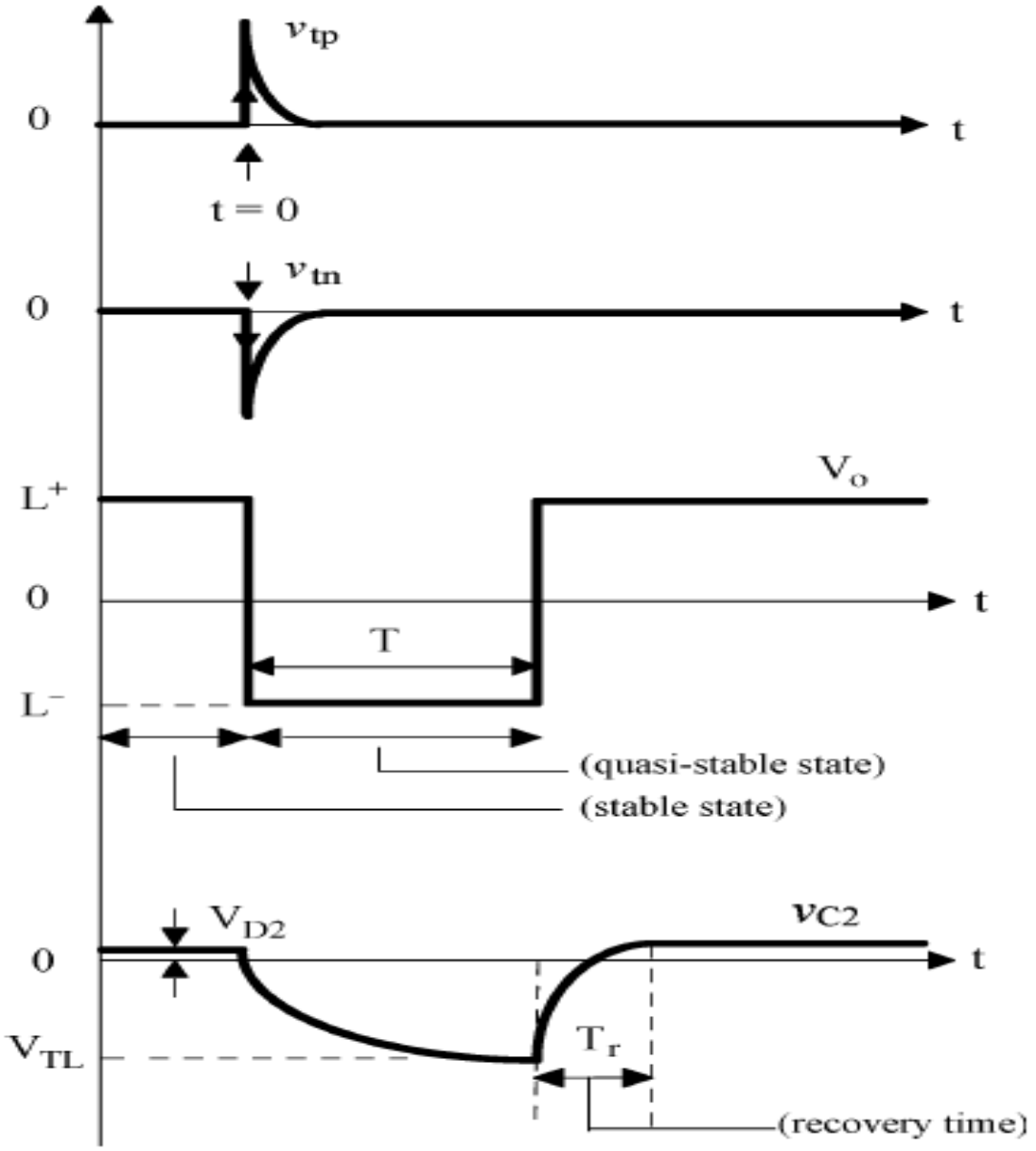

Fig.5.11 Waveforms of the monostable multivibrator using OTRA

5.4.3 Simulation Results

PSpice simulated results of monostable multivibrator using OTRA is shown below.

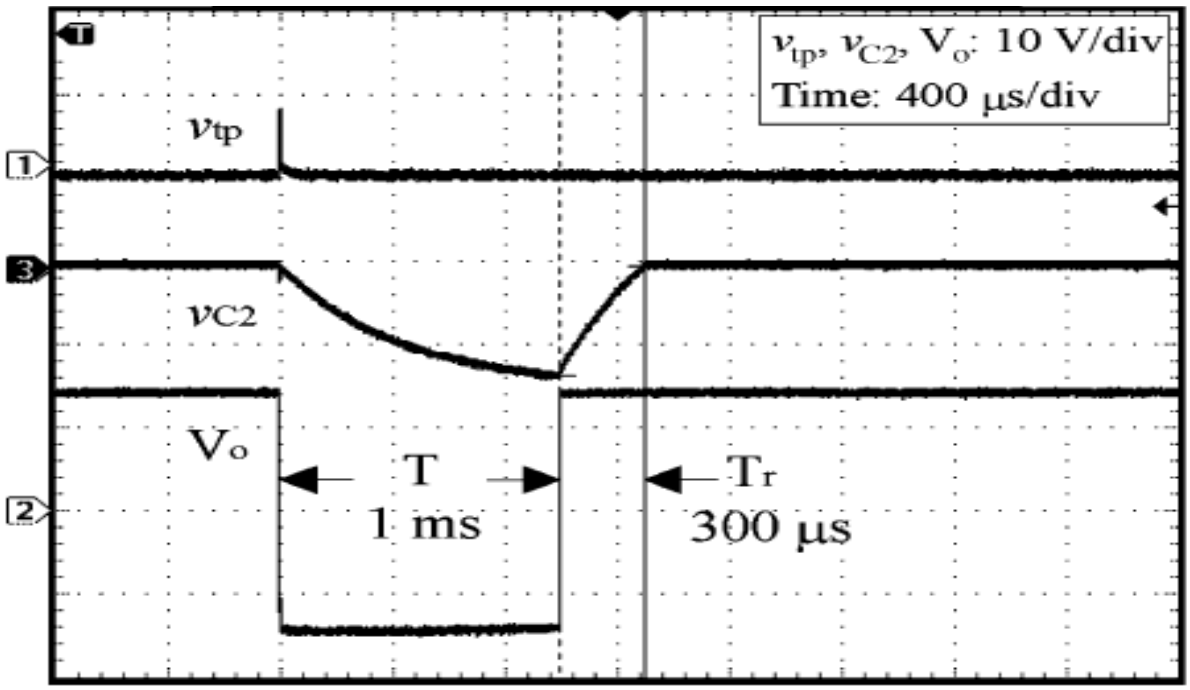

Fig 5.13 PSPICE simulated waveforms of monostable multivibrator using OTRA

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Chapter 6

CONCLUSION AND FUTURE SCOPE

6.1 CONCLUSION

Operational Trans-resistance Amplifier (OTRA) is a high gain current input, voltage output amplifier . it is clear that both input and output terminals are characterized by low impedance, thereby eliminating response limitations incurred by capacitive time constants. The input terminals are virtually grounded leading to circuits that are insensitive to stray capacitances .

OTRA has found significant importance in analog signal processing in recent years due to its useful features. This work presents a review of available literature in OTRA. In chapter 2 basics of OTRA along with its chronological evolvement has been discussed. A CMOS realization of OTRA proposed by Mostafa and Soliman has been characterized using PSPICE 0.5 µm technology model parameters. This building block has been used for simulating all OTRA based structures studied and implemented in this work. In chapter 3 OTRA based filters available in literature are implemented. Two generic biquadratic filter configurations have been studied which can be used to design LP,HP and BP filters by appropriate choices of admittances. These biquadratic filters have been simulated using PSPICE to verify their functionalities. In chapter 4 design of sinusoidal oscillators based on OTRA are discussed and implemented. In chapter 5 nonlinear applications of OTRA has been shown which find extensive applications in analog signal processing.

The simulations are performed using PSPICE and it is observed that the simulation results are in close agreement with theoretical results. The effect of non ideal behaviour of OTRA has also been included [3].

6.2 APPENDIX

Simulations have been performed using SPICE at 0.5um technology and the model files provided by MOSIS (AGILENT) used have the following parameters:

.MODEL MBREAKN nmos
+ LEVEL=3
+ UO=460.5
+ TOX=1E-8
+ TPG=1
+ VTO=.62
+ JS=1.8E-6
+ XJ=.15E-6
+ RS=417
+ RSH=2.73
+ LD=4E-8
+ ETA=0
+ VMAX=130E3
+ NSUB=1.71E17
+ PB=.761
+ PHI=.905
+ THETA=.129
+ GAMMA=.69
+ KAPPA=0.1
+ AF=1
+ WD=1.1E-7
+ CJ=76.4E-5
+ MJ=.357
+ CJSW=5.68E-10

+ MJSW=.302

+ CGSO=1.38E-10

+ CGDO=1.38E-10

+ CGBO=3.45E-10

+ KF=3.07E-28

+ DELTA=0.42

+ NFS=1.2E11

+ W=90U

+ L=4U

.MODEL MBREAKP pmos

MBREAKP

+ LEVEL=3

+ UO=100

+ TOX=1E-8 + TPG=1

+ VTO=-.58

+ JS=.38E-6

+ XJ=.1E-6

+ RS=886

+ RSH=1.81

+ LD=3E-8

+ ETA=0

+ VMAX=113E3

+ NSUB=2.08E17

+ PB=.911

+ PHI=.905

+ THETA=.12

+ GAMMA=.76

+ KAPPA=2

+ AF=1

+ WD=1.4E-7

+ CJ=85E-5

+ MJ=.429

+ CJSW=4.67E-10

+ MJSW=.631

+ CGSO=1.38E-10

+ CGDO=1.38E-10

+ CGBO=3.45E-10

+ KF=1.08E-29

+ DELTA=0.81

+ NFS=.52E11

+ W=200U

+ L=4U