CHAPTER-1

INTRODUCTION

The dissertation deals with implementation of current conveyor and its applications in filter design and simulated immittances. Analog integrated circuit design is becoming increasingly important with growing opportunities. Coupled with the various technological improvements are the ever shrinking feature size of the devices on ICs and the consequent reduction of power supply voltages. During the last couple of decades, modern applications of analog signal processing has followed the trends of current mode approach, where the signals representing the information are in the form of electric current. Current conveyors are among the main building block used in current mode circuits.

In [1] an excellent review of all the active building blocks used in analog signal processing till 2008 along with a catalogue of new building blocks has been given. Two approaches have been suggested for developing new active building blocks. The first approach suggests that by modifying the basic elements such as Voltage Feedback Amplifier (VFA), Operational Transconductance Amplifier (OTA), Current Feedback Amplifier (CFA) and Current Conveyors new building blocks can be developed. These elements should have a simpler internal structure in order to maintain low power consumption and high-speed operation. The second approach is characterized by entirely new elements which extend the original VFA-CFA-OTA-CC set.

In the following we present a very brief review of current mode signal processing and some of the active building blocks used in analog signal processing.

1.1 Evolution of current mode approach

The advancement in the field of analog IC design has been given by the process technologies that are built mostly for digital applications. With the growth of submicron technologies like 0.13 and 0.18 micron, the supply voltages have been reduced to 3.3 volts and even lower [2].This makes it difficult to design a voltage mode CMOS circuit with high linearity and wide dynamic range. With respect to future applications the current mode circuits have become a viable alternative due to its inbuilt features and advantages over the voltage mode circuits.

Advantages of current mode circuits

- The current mode circuits are faster in comparison to the voltage mode circuits. The parasitic capacitances which are inherent in the analog circuits must be charged and discharged with the changing voltage levels [3]. In the case of current mode circuit it is not mandatory that any change in current level is followed by the change in voltage level. Thus, the parasitic capacitances will not affect the operating speed of the circuit in huge amount.
- They do not require specially processed resistors or capacitors.
- They are also more compatible with digital CMOS technology making combination of mixed signal circuits more feasible.
- The number of components required to perform a signal processing function is less compared to voltage mode circuits.

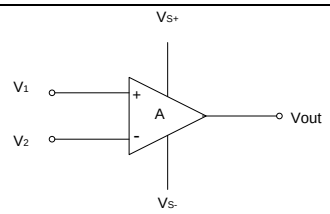
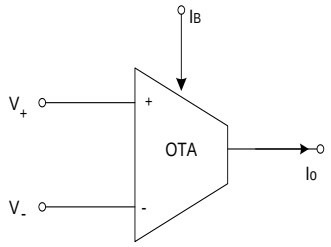
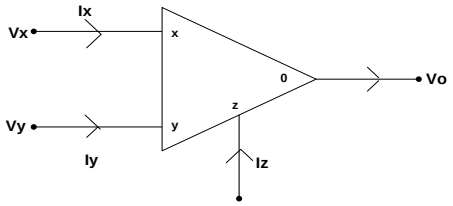
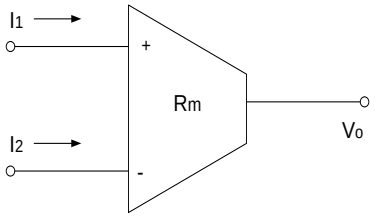
1.2 Various active building blocks used in Analog Signal Processing

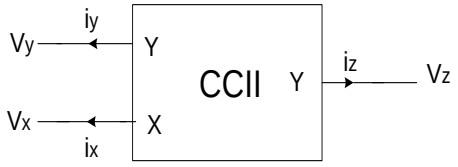
A very large number of active building blocks have been proposed by different research groups. These research groups have proposed either a fundamental active building block or modified the existing building block by overcoming its limitations or made it more versatile by adding new features to it. Table 1.1 summarizes these fundamental building blocks. We have not included the

different derivatives of the current conveyors in this table. These derivatives of current conveyors have been tabulated elsewhere. We call them as fundamental building blocks because these blocks have been used to synthesize most of the synthetic active building blocks suggested in [1].

Table 1.1

Active building blocks used in analog signal processing

BLOCK	SYMBOL	TRANSFER FUNCTION MATRIX
Operational Amplifier (OP-AMP)		$\begin{bmatrix} V_1 \\ V_2 \\ V_0 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ A & -A & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_0 \end{bmatrix}$
Operational Transconductance Amplifier (OTA)		$\begin{bmatrix} I_1 \\ I_2 \\ I_0 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ g_m & -g_m & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_0 \end{bmatrix}$
Current Feedback Operational Amplifier (CFOA)		$\begin{bmatrix} V_x \\ I_y \\ I_z \\ V_o \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} I_x \\ V_y \\ V_y \\ I_o \end{bmatrix}$
Operational Transresistance Amplifier (OTRA)		$\begin{bmatrix} V_1 \\ V_2 \\ V_0 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_0 \end{bmatrix}$

Current Conveyor (CC)		$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix}$

1.3 Current Conveyors and their various versions

Current conveyor is the most basic building block in the field of current mode analog signal processing. In the most fundamental form the second generation current conveyor CCII, which is the most widely used variant is a three terminal device which has a high input impedance terminal (y), a low input impedance terminal (x) and a high output impedance terminal (z). With signal ground as the fourth terminal it is a four terminal device which can perform many useful signal processing functions when they are arranged in particular circuitry with other passive components [4]. The current conveyor can simplify the circuit design in the same manner as the conventional operational amplifier does. Current conveyor has proved itself to be functionally flexible and accomplished and now it has been quickly acquiring acceptance as the practical building block in manner as the theoretical building block. Their gain depends only on the absolute value of a single circuit element whereas it is not dependent upon the matching of pairs of external components, as in the case of instrumentation amplifier. The principle of the first generation current conveyor was published in 1968 by K. C. Smith and A. S. Sedra and which was followed by the introduction of the second generation current conveyor in 1970 by A. S. Sedra and K. C. Smith [5]. Soon after, a number of authors have suggested improved implementation of the current conveyor to strengthen the performance and utility of this building block. Unfortunately, there is still a shortage of available current conveyors in the form of an IC. Many manufacturers do not use this block in their advanced applications and systems due to the absence of its IC. If it is available as an IC then the manufacturer will get the chance to be more familiar with the current conveyor and its usability. There is only one monolithic IC of "pure" current conveyor i.e. CCII01. Tremendously, many novel constructions of modern wideband and high-speed operational-amplifiers are

based on current conveyor (OPA660, AD840). It has many applications due to current mode, when the current flows into the low-impedance input X, is applied by a simple current mirror into the z output and its input voltage Y is grounded. In 1995 the third-generation current conveyor was proposed by Fabre [6]. A Current Conveyor IC, named as PA630, was introduced by Wadsworth in the year 1989, produced by Phototronics Ltd. of Canada. During that time only, the now a days well-known AD844, operational trans impedance amplifier generally known as a current feedback op-amp was introduced. It was known to be internally a CCII+ accompanied by voltage follower. A very comprehensive review of the current mode circuits prior to 1990 was given by Wilson. In 1995, authorization of many continuous variations and generalizations of basic principle of CCII was done in order to use this circuit element more effectively in various applications [7].

1.3.1 First Generation Current Conveyor (CCI)

The CCI is a three terminal device and the terminals are named as X, Y and Z. Originally the current conveyor was introduced, as a 3-port device whose block representation is as shown in figure below

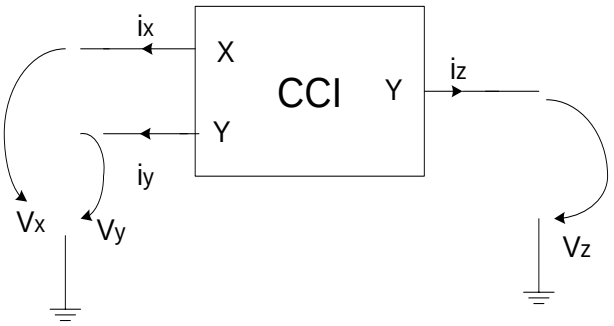


Fig 1.1 Representation of CCI

The CCI's operation is such that if a voltage is applied to Y, input terminal an equal potential will be generated on the input terminal X. In the same way, an input current I being pushed into terminal X will produce an equal amount of current flowing into terminal Y. Furthermore the current I will be send to the output terminal Z such that

terminal Z has the characteristics that current source having the value I, with high output impedance. It can also be seen, the X's potential has been set by the help of Y and it is independent of the current being applied into port X. In a similar manner, the current through input Y, being fixed by that of X, and it is independent of the voltage applied at the terminal Y. Hence, the device shows the virtually short circuit input characteristics at port X and a dual virtually open-circuit input characteristics at the port Y.

The matrix given below forms the equation which helps to express the input-output characteristics of CCI

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_X \\ I_X \\ V_Z \end{bmatrix}$$

Where the variables I_Y, V_X and I_Z provides the total instantaneous quantities. In CCI+, the current i.e. supplied to Y produces current into Z and in a CCI-, current into Y produces an equivalent current out of Z. The + sign applies for the CCI in which both I_Z and I_X flow into the conveyor and it is denoted by CCI+. The – sign applied in the case of opposite polarity denoted by CCI-, in which I_Z and I_X flows out of the conveyor.

To anticipate the interaction of the port voltages and currents shown by the above matrix equations the nullator-norator representation given in Fig 1.2 may be used

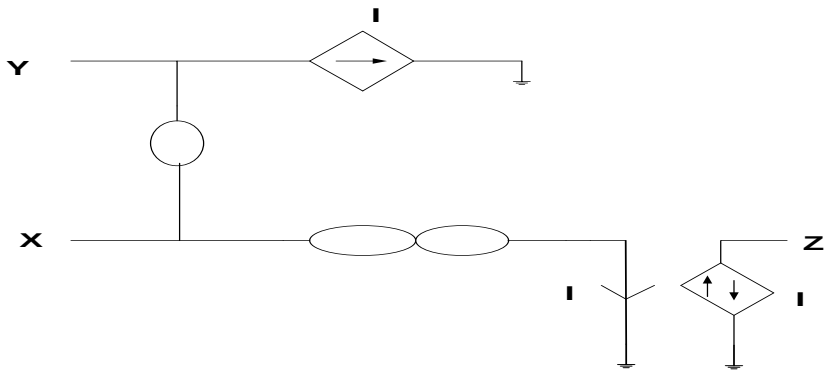


Fig 1.2 Nullator Norator representation of CCI

In the fig 1.2 that is shown above, the nullator element is represented by single ellipse and norator element is represented by the two intersecting ellipses. The nullator element has the equation V=0 and I=0 whereas the norator has an random current-voltage relationship [8]. Clearly the nullator element is used to represent the virtual short circuit condition between the X and Y terminals. Two dependent current sources are also included in the circuit. These are used in the circuit in order to transmit the current at port X to ports Y and Z.

1.3.2 The Second Generation Current conveyor (CCII)

In CCII, no current flows through terminal Y, in order to increase the flexibility of current conveyors. The ideal CCII appeared as an ideal transistor, with the perfect characteristics [5, 9-11]. At the gate or base no current flows through them, which is represented by terminal Y. The emitter or source voltage (appeared at terminal X) follows the voltage at terminal Y, as there was no base-emitter or gate-source voltage drop. There is infinite input impedance at gate or base (terminal Y) whereas the emitter or source (X) has zero input impedance. The current that comes out of the emitter or source (terminal X) that reflects as a current in at the collector or drain (Z), but with an infinite output impedance.

Fig 1.3 Circuit symbol of CCII

The $\pm$ sign shows the flow of current in the same direction or opposite direction respectively among the nodes X and Z. The current that is applied to terminal X is then passed to the output terminal Z which is at high impedance level where it is provided with either positive polarity (means in CCII+) or negative polarity (means in CCII-). The Current conveyor is named as negative current conveyor when the current

flowing into the terminals Z and X is in the opposite direction. The current conveyor is named as positive current conveyor when the current flowing in the terminals Z and X are in the same direction.

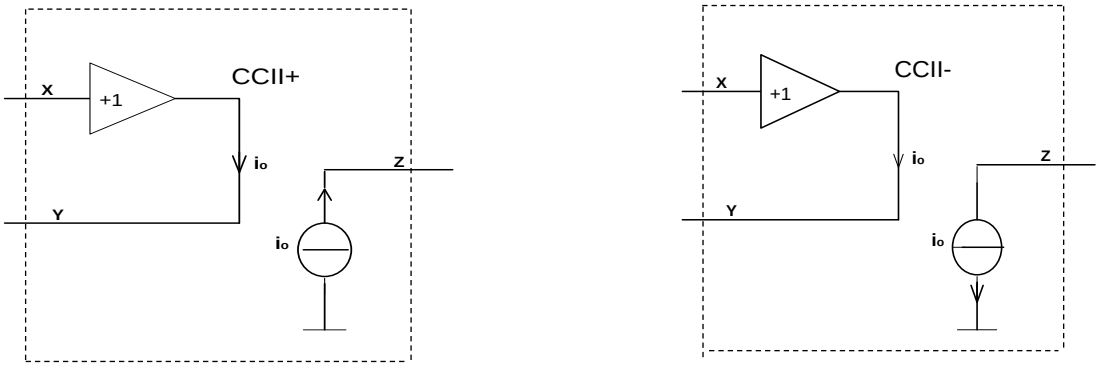


Fig 1.4 Principle of second generation current conveyor (CCII)

This building block of current conveyor has proved to be more useful than CCI. Utilizing the same block diagram representation, CCII can be expressed with a matrix as

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix}$$

The nullor representation of second generation current conveyor (positive or negative in Fig 1.4) has been illustrated in Fig 1.5 given below.

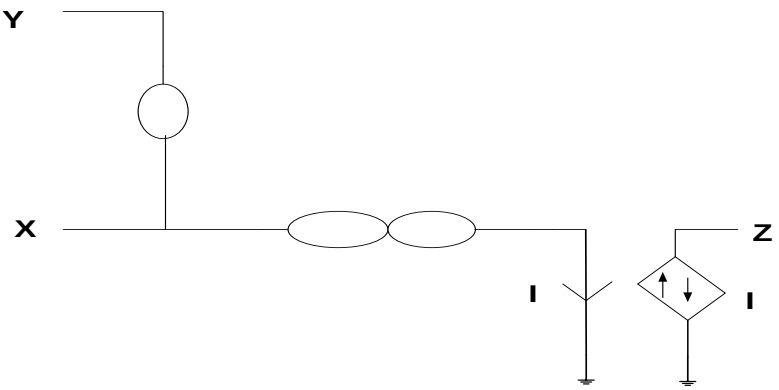


Fig 1.5 Nullator Norator representation of a CCII

In the case of a CCII-, it is not necessary to have dependent current source, the only thing is current that flows into the terminal X must also flows out of terminal Z. Thus the equivalent circuit of CCII- can be represented with a single nullor element as shown in Fig 1.6.

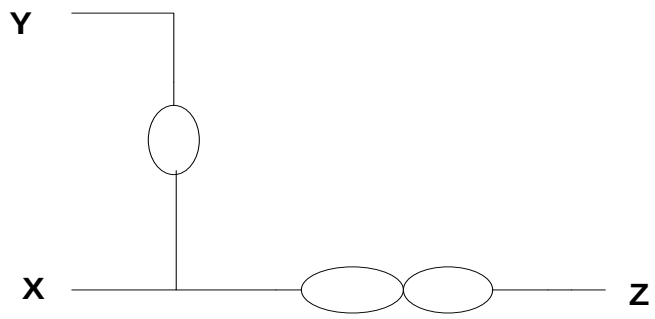


Fig 1.6 A simplified representation of CCII-

In the current conveyor family types, CCII has proven itself to be so far the most advantageous. A wide range of applications of CCII are present in literature. It is a much suitable building block for the designing of active RC filters or number of special admittance converters [8]. In the last few decades a number of high-speed and wide-range of op-amps was presented that were based on current conveyor structure. And also in case of the low voltage applications CCII is going to prove itself to be very much powerful building block. The most widely well-known applications of CCII were in the realization of controlled sources, impedance inverters, impedance converters, gyrator and other analog computation devices.

1.3.3 The Third Generation Current Conveyor (CCIII)

The third generation current conveyor is similar to the first generation Current conveyor apart from the only difference that the current in terminal X is reversed [2,6]. The current in terminal X and Y flow in opposite directions hence in a CCIII whatever current flows into terminal Y , the same current should also flows out of terminal X. This is defined clearly by push-pull topology. Current measurement is one

of the main applications of third generation current conveyor. This structure was given in 1995 by Fabre.

Block diagram representation of CCIII is shown in fig 1.7 and the equations are given by the matrix below-

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_X \\ I_X \\ V_Z \end{bmatrix}$$

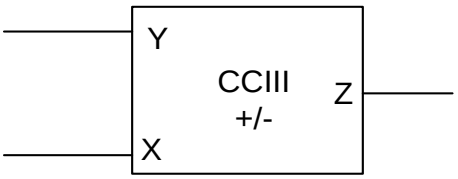
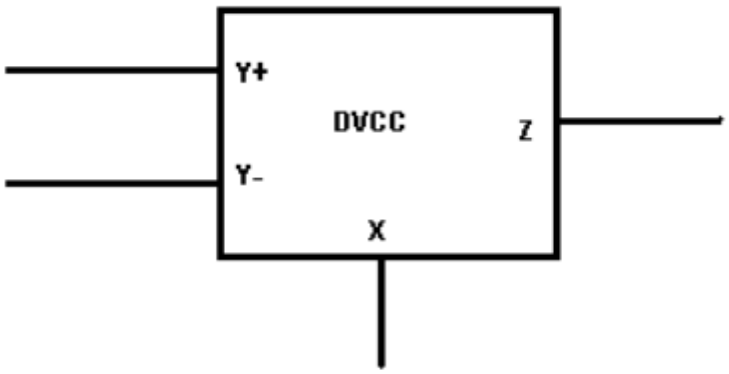
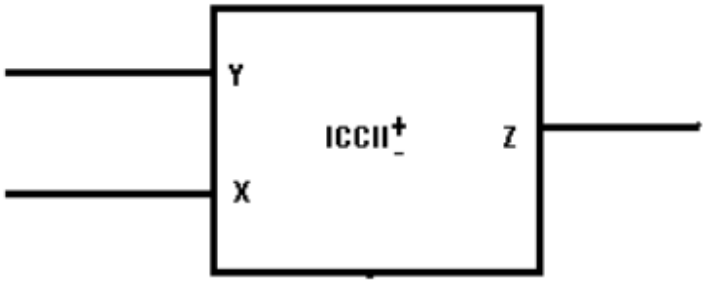
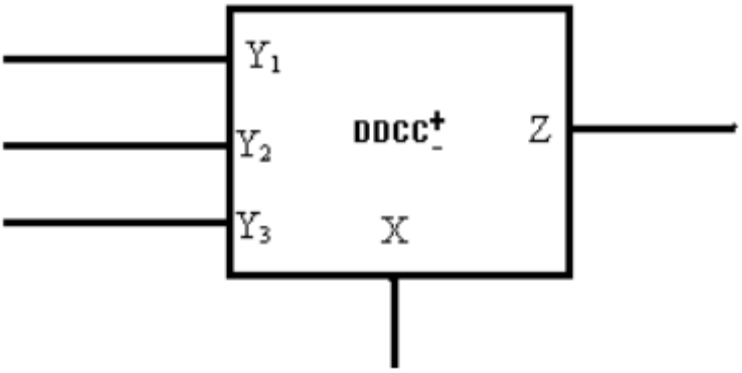
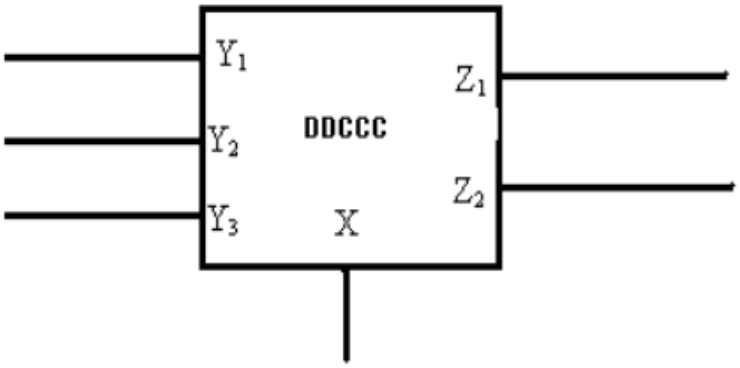
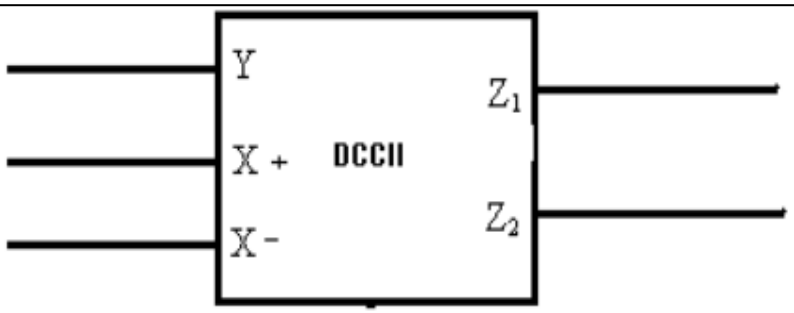


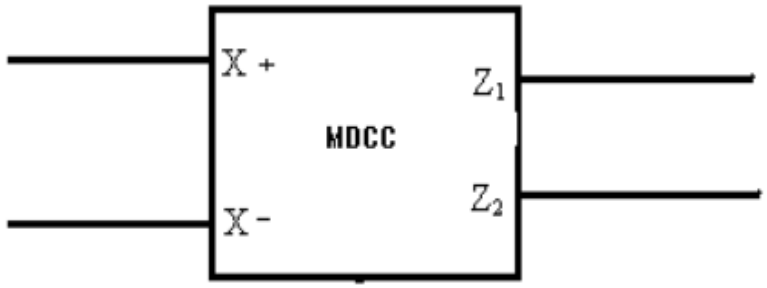
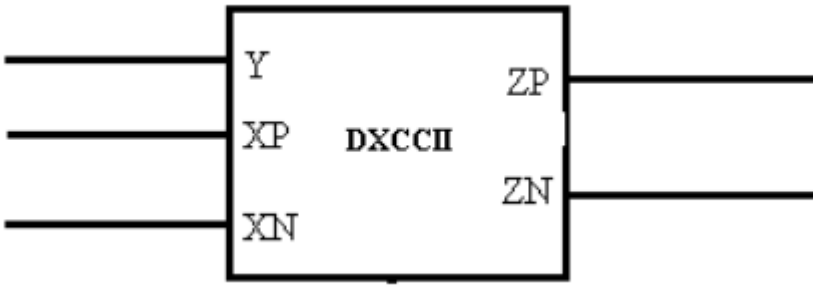
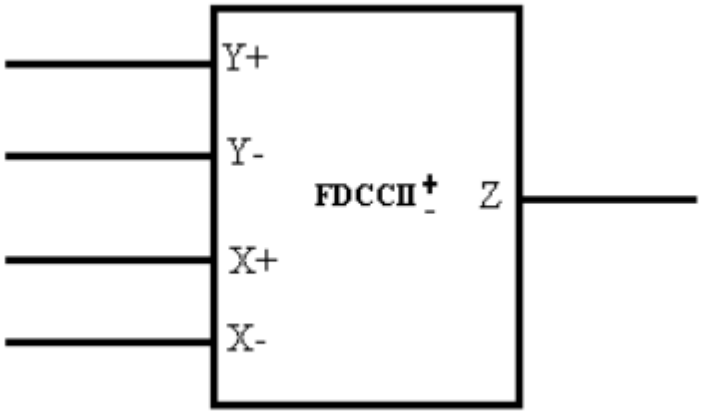
Fig 1.7 Block diagram representation of CCIII

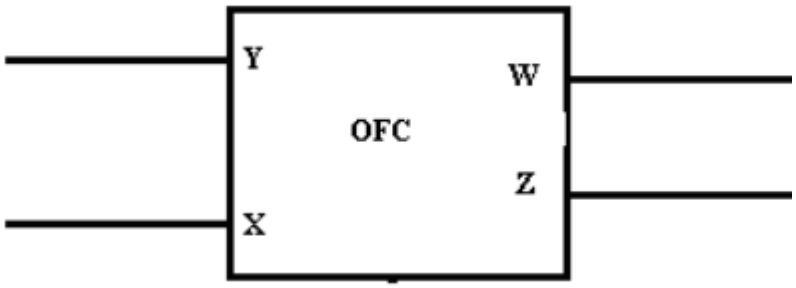
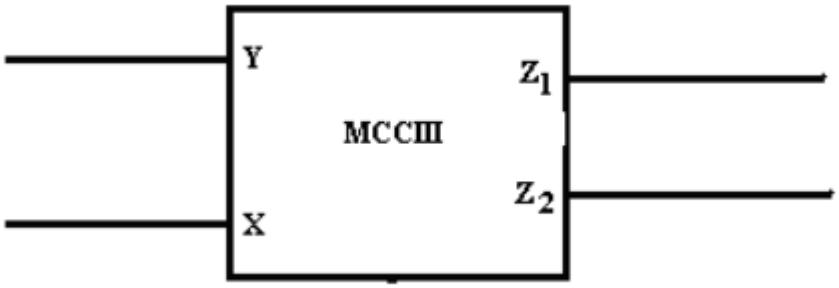
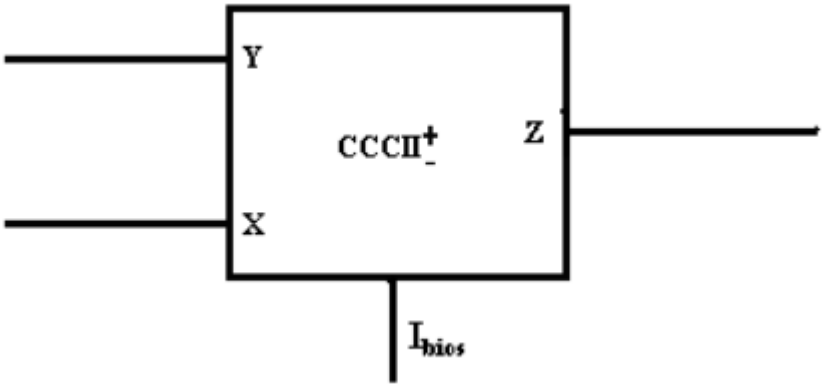
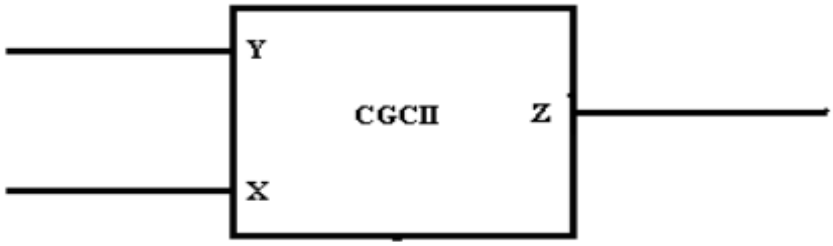
1.3.4 A brief summary of the behavioural models of selected conveyors

Some of the basic blocks of Current Conveyor derivatives and their port relationships of are given in [12] and represented in Table 1.2.

	Differential voltage current conveyor $I_{Y+} = I_{Y-} = 0$ $V_X = V_{Y+} - V_{Y-}$ $I_Z = I_X$

	Inverting current conveyor II $I_Y = 0$ $V_X = - V_Y$ $I_Z = +/- I_X$
	Differential difference current conveyor $I_{YI} = I_{Y2} = I_{Y3} = 0$ $I_X = V_{Y1} - V_{Y2} + V_{Y3}$ $I_Z = \pm I_X$
	Differential Difference Current Controlled Conveyor $I_{Y1} = I_{Y2} = I_{Y3} = 0$ $I_X = V_{Y1} - V_{Y2} + V_{Y3}$ $I_{Z1} = I_X$ $I_{Z2} = -I_X$
	Differential Current Conveyor II $I_Y = 0$ $V_{X+} = V_{X-} = V_Y$ $I_{Z1} = -I_{Z2} = I_{X+} - I_{X-}$

	Modified Differential Current Conveyor $V_{X+} = V_{X-} = 0$ $I_{Z1} = -I_{Z2} = I_{X+} - I_{X-}$
	Dual-X Current Conveyor $I_Y = 0$ $V_{XP} = -V_{XN} = V_Y$ $I_{ZP} = I_{XP}$ $I_{ZN} = I_{XN}$
	Fully Differential Current Conveyor II $I_{Y+} = I_{Y-} = 0$ $V_{X+} = V_{X-} = V_{Y+} - V_{Y-}$ $I_Z = \pm(I_{X+} - I_{X-})$

	Operational Floating Conveyor $I_Y = 0$ $V_X = V_Y$ $V_W = Z_T I_X$ $I_Z = - I_W$
	Modified Current Conveyor III $I_Y = I_X$ $V_Y = V_X$ $I_{Z1} = -2I_X$ $I_{Z2} = I_X$
	Current Controlled Conveyor II $I_Y = 0$ $I_Z = \pm I_X$
	Current Gain conveyor $I_Y = 0$ $V_X = V_Y$ $I_Z = A I_X$

- The requirement of multiple output current conveyor had given rise to the Dual output CCII (DO-CCII), which produces current Iz in multiple directions, hence it can combine both the positive and negative CCII in a single device. If both currents are of same polarity either both positive or both negative, then the resulting conveyors are of the CFCCIIp or CFCCIIn types CCII, where p or n stands for positive or negative current conveyor.

- The another generalization can be represented by the Differential Voltage Current Conveyor (DVCC), in which the original input voltage Y breaks into 2 inputs Y_1 and Y_2. Voltage at the X terminal is then given by the voltage difference of the voltage inputs. It provides too much flexibility during the design of voltage mode and mixed mode applications.

- DVCC provided with the complementary pair of terminals Z_1 and Z_2 is known as Differential Voltage Complementary Current conveyor (DVCCC). A special case of DVCC in which the terminal Y_1 grounded, is called ICCII, which is inverting CCII. On the other hand, Differential Difference CCII (DDCC) is given which is an extension of DVCC. Voltage at the X terminal is given by the combination of voltages at three terminals Y_1, Y_2 and Y_3. Breaking the terminal Z of DDCC into the pair of Z terminals with currents $I_Z = I_X$ gives the Differential Difference Complementary Current Conveyor (DDCCC).

- The other generalization of CCII is Differential Current Conveyor (DCC), in which the input X can be replaced by the pair of inputs X_1 and X_2. The current through the terminal Z is given by the difference of currents through the terminals X_1 and X_2.

- The Modified Differential Current Conveyor (MDCC) is the simplified form of DCC which assumes that signal voltage at the Y terminal is zero.

- Dual-X second generation current conveyor (DXCCII) which is the combination of CCII and ICCII. DXCCII has two terminals that are Xp and Xn. The copy of currents at terminals Xp and Xn are provided at terminals Zp and Zn.

- Fully Differential CCII (FDCCII) is an important generalization of the conventional CCII. The terminals X, Y and Z are in pairs. FDCCII is created for the applications with fully differential architecture for fast signal processing. Such a type of current conveyor is known as Fully Balanced CCII (FBCCII).

- The special internal structure of MCCII provides such an operation that the current through the Z terminal does not depends on the direction of current Ix, i.e. Iz = abs (Ix). The full wave rectifiers can be economically implemented using this feature [13].

- Joining the two current conveyors (CCII-) produces another conveyor named as Floating Conveyor (OFC). OFC is a universal differential input differential output building block, which permits the current mode, voltage mode and mixed mode applications.

- An utmost example of universality is the Universal Current Conveyor (UCC). By using this circuit all the above types of current conveyor can be very easily implemented. However, such integrality is at the cost of non-optimal parameters for a specific application.

- The modifications in the third generation current conveyor, named as Modified CCIII (MCCIII). It is equipped with a pair of terminals Z_1 and Z_2. Currents out of these terminals are in opposite directions and holds the following inequalities $I_{Z1} = -2I_X$, $I_{Z2} = I_X$. The unequal values of the currents allow the design to be of some interesting applications.

- The non-zero impedance of X terminal is one of the important parasitic parameter of the current conveyor, which negatively affects its behavior especially in the case of filtering applications. However, this phenomenon is complicatedly utilized in a new type of conveyor which is called as Current Controlled Conveyor (CCCII), where the resistance of terminal X is controlled electronically by the help of bias current. It can be seen that this active device can be used in filters whose parameters may be controlled electronically. Such a feature is necessary in the so called gmC filters, i.e. filters that consist only of OTAs and capacitors.

- The other method to control electronically the parameters of the current conveyor is based on the conveyors with variable gain i.e. Iz/Ix. This type of conveyor called as CGCCII (current gain CCII). The variable gain is applied through transforming current Iz into the voltage by means of resistors, and also through transforming voltage into current by means of electronically gm-controlled OTA. The updated solution can be differentiated by the help of digital control of the gain, utilizing the Current Division Network (CDN) and Digitally Controlled Current Follower (DCCF).

1.4 Objectives of the work

1.4.1 Implementation of different structures of current conveyors.

1.4.2 Implementation of simulated immittances using different realizations of current conveyors.

1.4.3 Realization of RC Active filters using different architectures of current conveyors.

1.4.4 Higher order filters realization using different realizations of current conveyors.

1.5 Conclusion

This thesis work is divided into 5 chapters. Chapter 1 gives a brief introduction and description about the current conveyors. Chapter 2 gives the various implementation of second generation current conveyor. Chapter 3 shows the realization of grounded inductor, floating inductor and capacitance multiplier through second generation current conveyor. Chapter 4 gives the realization of voltage mode and current mode universal filter using CCII+. Chapter 5 introduces a fourth order high pass Butterworth filter design using CCII by element replacement method. Chapter 6 concludes the thesis with the results, conclusion and future scope of the project.

CHAPTER-2

CMOS REALIZATION OF CURRENT CONVEYOR II

In analog computation and circuit synthesis, the application of second generation Current Conveyors as a circuit building block was given by Smith and Sedra. In the present chapter we discuss some of the integrable realizations and realization of CCII using off-the shelf available components.

2.1 CCII+ available off-the shelf available components

2.1.1 CCII+ using OA and OTA

Though the transistor based realization of the first generation and the second generation current conveyor was given in 1968 and 1970 by Smith and Sedra, these blocks started getting due attention from the academic community and research fraternity only when practical realizations of these blocks using off-the shelf available components like operational amplifiers, operational transconductance amplifies and transistor arrays started appearing. In 1980, a new active circuit was proposed by Senani [14] for implementing current conveyors, which consists of operational amplifier (OA), operational transconductance amplifier (OTA) and resistors. This circuit is a simple implementation of second generation current conveyor as the IC of OA and OTA was easily available. The three port active R circuit is shown in the figure given below.

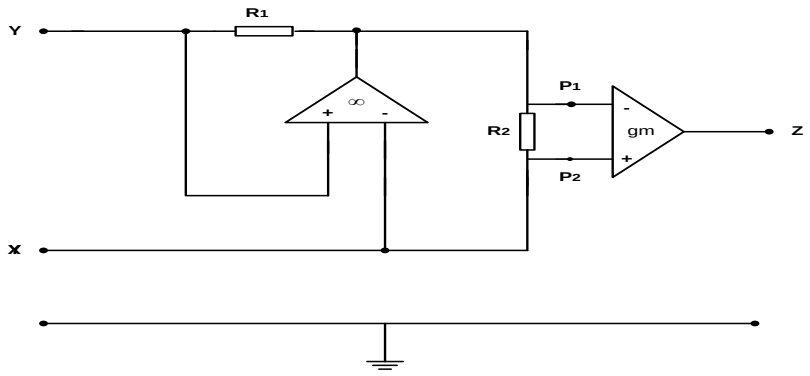


Fig 2.1 Circuit capable of implementing Current Conveyor

Let us consider that operational amplifier has infinite input impedance, zero output impedance and voltage gain equal to A and operational transconductance amplifier has infinite input impedance and transconductance equal to gm. The hybrid matrix of this three port active R circuit is given as

$$[H] = \begin{bmatrix} \frac{1}{R_1(1+A)} & \frac{AR_2}{R_1(1+A)} & 0 \\ \frac{A}{(1+A)} & \frac{R_2}{(1+A)} & 0 \\ 0 & g_m R_2 & 0 \end{bmatrix}$$

As $A \rightarrow \infty$, the above matrix reduces to

$$[H] = \begin{bmatrix} 0 & \frac{R_2}{R_1} & 0 \\ 1 & 0 & 0 \\ 0 & g_m R_2 & 0 \end{bmatrix}$$

Now if R_1 is deleted and $R_2 = 1/g_m$, then the above H matrix of the circuit reduce to the equation of CCII+ and CCII- would be realizable by interchanging the input terminal of OTA.

2.1.2 CCII+ using 741 in supply current sensing mode

IC 741 is a very cheap easily available and functionally very simple integrated circuit which is the circuit implementation of a differential voltage controlled

voltage source. The remarkable ac and dc performance of this op-amp makes its relevant for active filter applications. The internal architecture of this IC does not contain signal ground and as a result the output current of this amplifier is equal to the difference of the currents drawn by the two supply leads. This fact has been used by several researchers to realize a current conveyor with the help of current mirrors and this IC. This technique of realizing CCII was first reported by B. Wilson in 1984 and then developed as a current mode amplifier [15]. Figure 2.2 gives the schematic realization of the CCII+ whereas Figure 2.3 gives the actual realization with the current mirrors realized with the mixed transistor arrays.

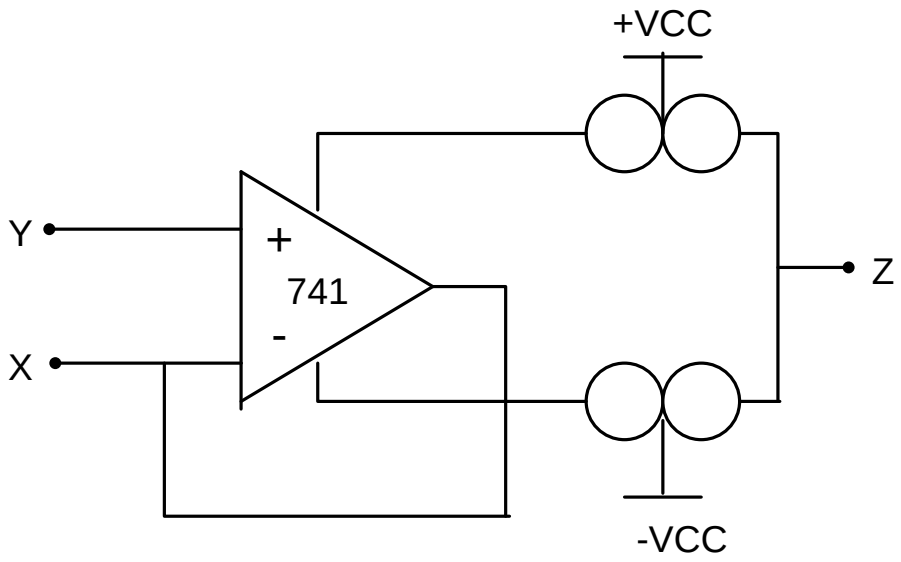


Fig 2.2 CCII+ using IC 741

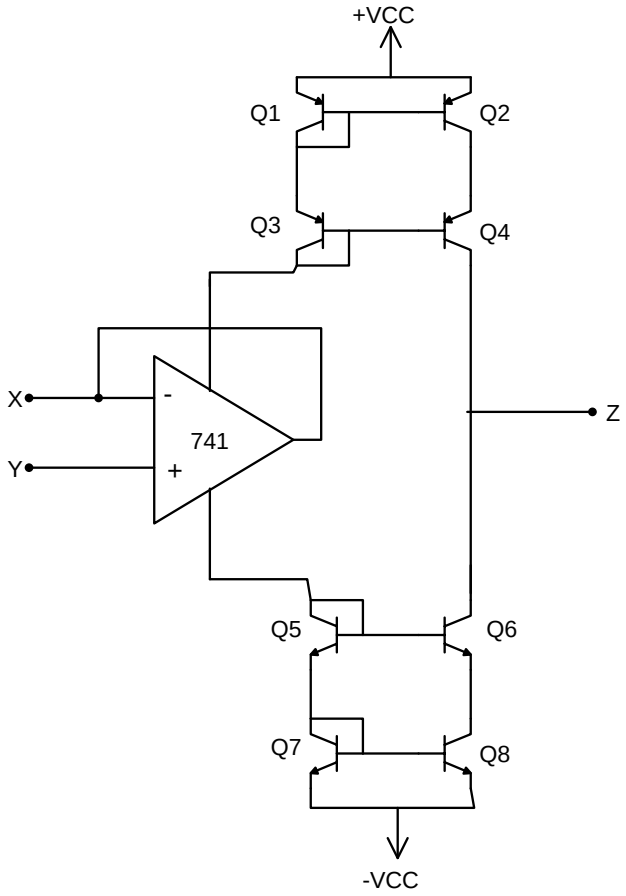


Fig 2.3 CCII+ using IC 741 in supply current sensing mode

2.1.3 Second Generation Current Conveyor based on CFOA

CFOA (current feedback operational amplifier) is a novel active building block which offers wider signal bandwidth and higher linearity compared to conventional op-amps. It is a versatile, low cost component that provides an excellent combination of ac and dc performance [16-18].

The functional block diagram of CFOA is shown in fig 2.4 and its terminal characteristics are given as

$$\begin{bmatrix} V_x \\ I_y \\ I_z \\ V_o \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} I_x \\ V_y \\ V_y \\ I_o \end{bmatrix}$$

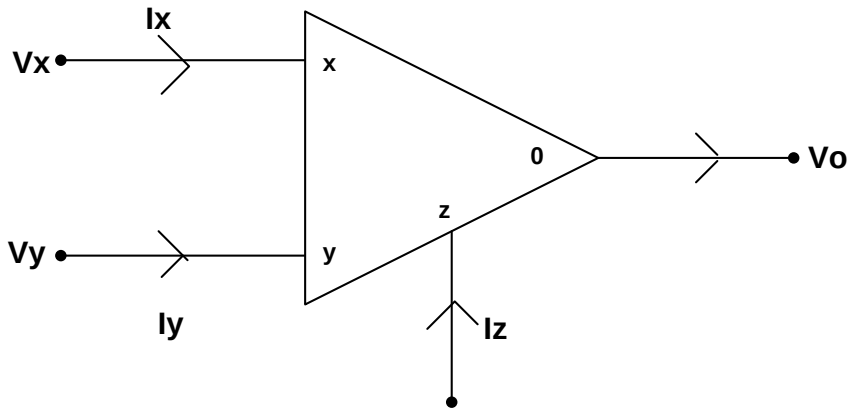


Fig 2.4 Functional Block Diagram of CFOA

It is clear from the terminal characteristics of CFOA that it consists of a current conveyor of second generation along with a voltage buffer. It is also available in the form of IC AD-844. It is a high speed monolithic operational amplifier, which can provide high bandwidth and very fast large signal response with excellent dc performance [19]. It can be used in many non-inverting applications and also be used for current to voltage applications. It provides a closed-loop bandwidth that is determined by the feedback resistor and does not depend on the closed loop gain. It is free from the slew rate limitations. The rise and fall times are essentially independent of output level. It can be operated from ±4.5 V to ±18 V power supplies and is capable of driving loads down to 50 Ω, as well as driving very large capacitive loads.

When we apply the input at Y terminal i.e. V_Y and then we check the voltage at X terminal i.e. V_X, the relationship between X and Y is shown below

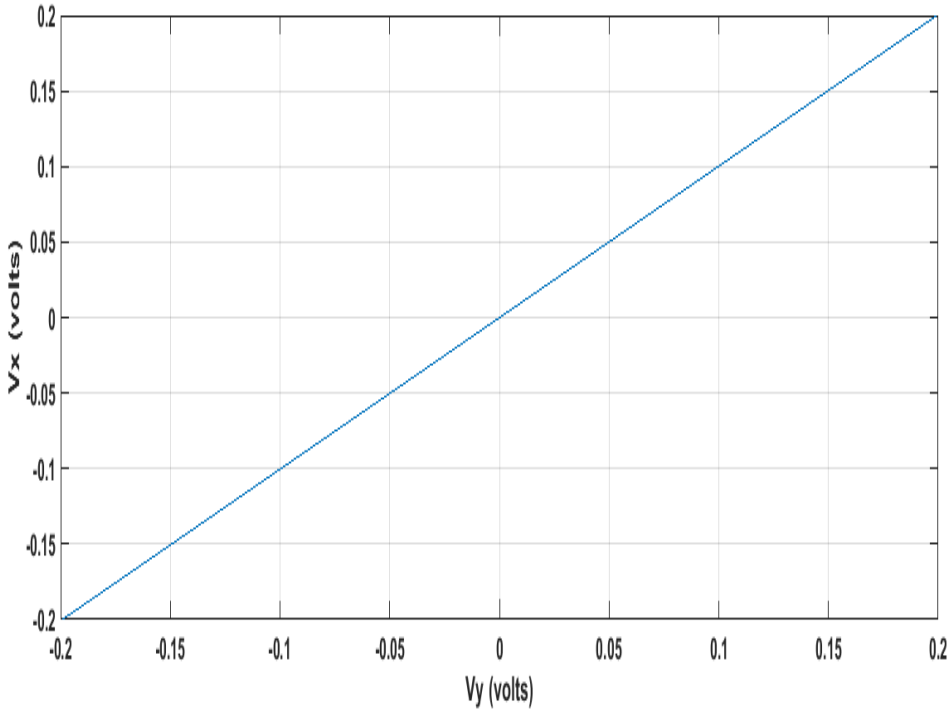


Fig 2.5 Port relationship between V_X and V_Y when we applied input dc sweep at Y terminal

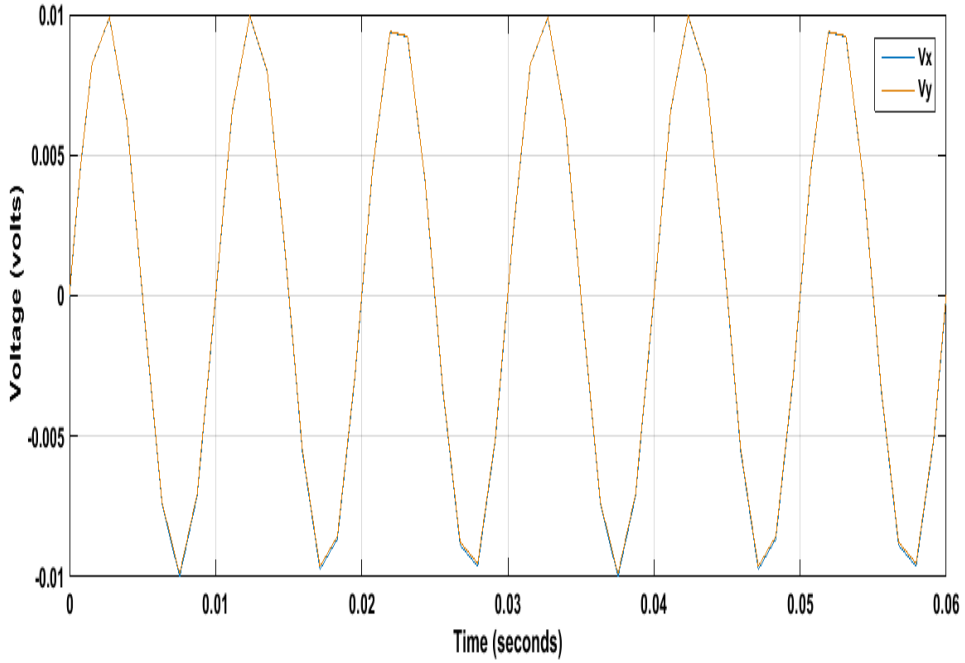


Fig 2.6 Port relationship between V_X and V_Y when we applied sinusoidal input voltage at Y terminal

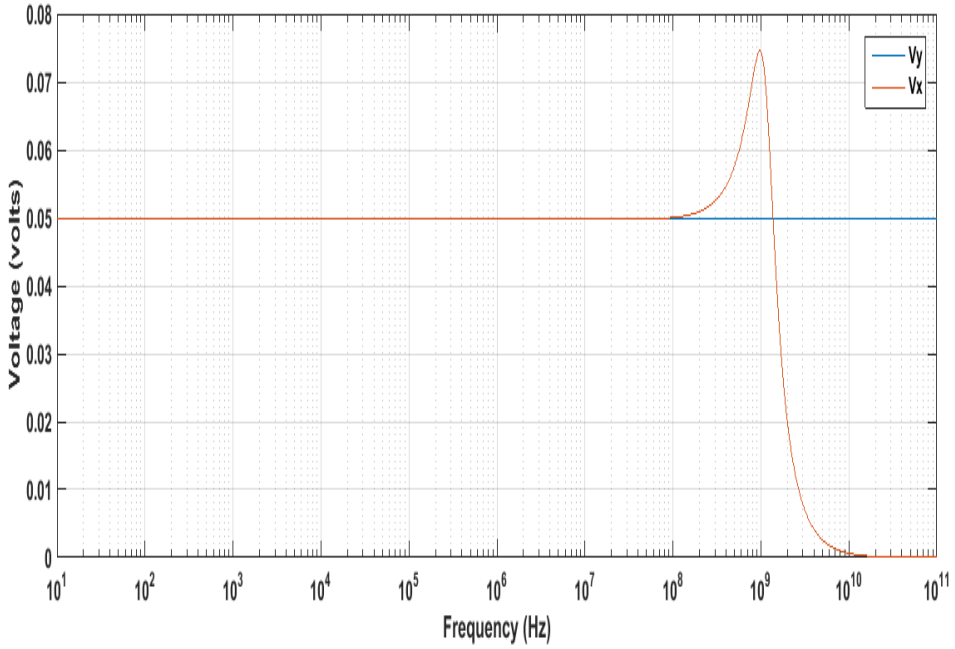


Fig 2.7 Port relationship between V_X and V_Y when we applied AC input voltage at Y terminal

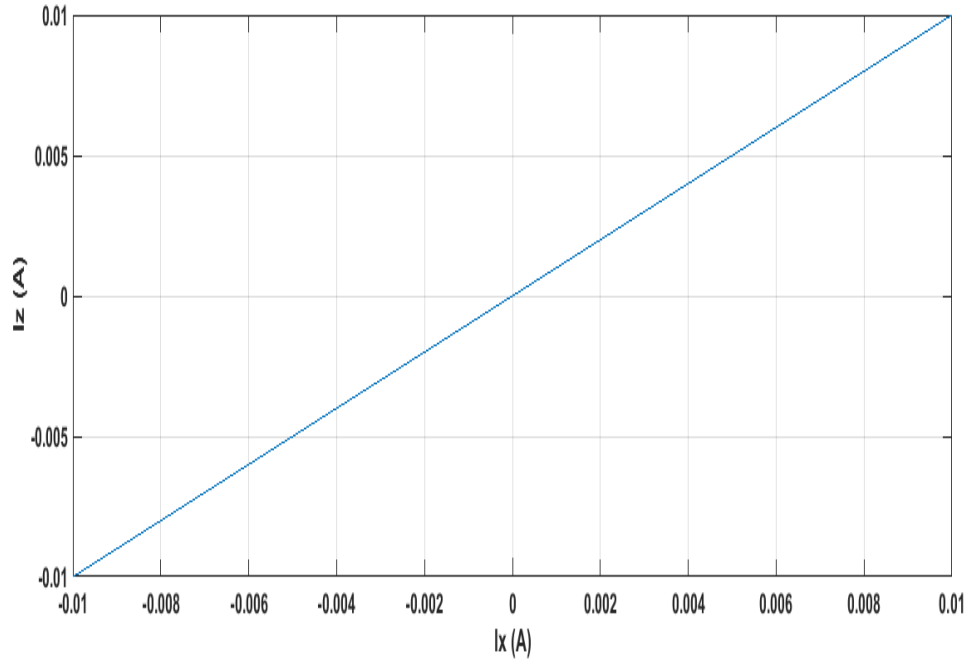


Fig 2.8 Port relationship between I_X and I_Z when we applied input dc sweep at X terminal

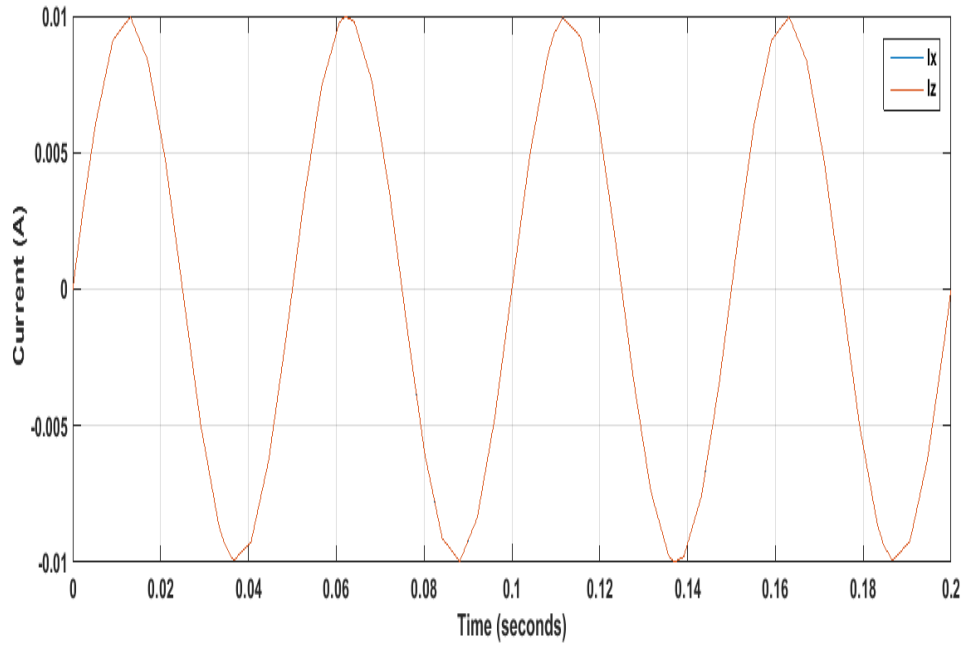


Fig 2.9 Port relationship between I_X and I_Z when we applied sinusoidal input current at X terminal

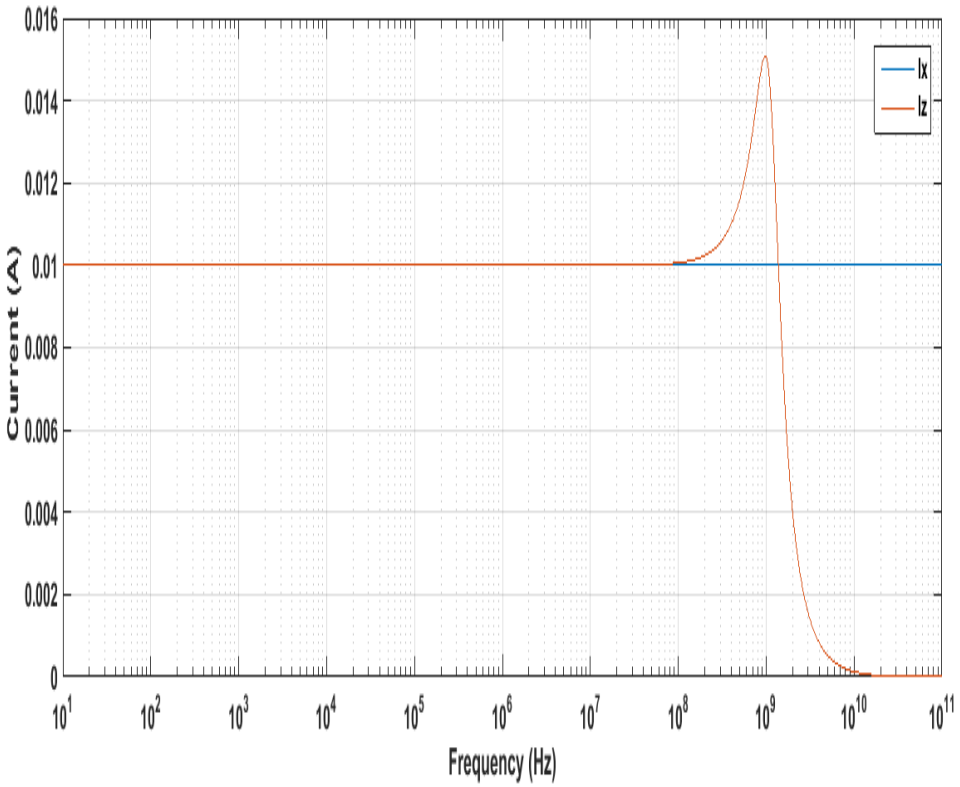


Fig 2.10 Port relationship between I_X and I_Z when we applied AC input current at X terminal

2.2 Integrable realizations of CCII+

2.2.1 Trans linear Second Generation Current Conveyor

The conventional translinear configuration is a very attractive implementation of CCII which is tunable and very simple. It has been used in many circuit designs and has proved its good performances [20, 21]. Owing to the translinear loop carried in this configuration, nearly ideal CCII behaviour can be observed at its three terminals. The considered circuit achieves the function of voltage follower between ports X and Y by means of one mixed translinear loop (M7,M8,M11,M12 Fig. 2.11). If a voltage is applied to terminal Y, an equal potential will appear on the input terminal X. The current flow through Y is Zero (ideally). The current will be conveyed to output terminal Z such that Z has the characteristics of a current source with high output impedance. Potential of X is set by that of Y, which is independent of the current applying at port X.

Whereas, the port X can be used as a voltage output or as a current input port. Therefore, this current conveyor can be used to process both voltage and current signals [8,22].

There are two types of second generation current conveyors:

• Positive current conveyor (CCII+) in which the currents I_X and I_Z have the same direction as in a current mirror.

• Negative current conveyor (CCII-) in which currents I_X and I_Z has the different direction as in current buffer.

The translinear CCII+ is shown in figure 2.11 which satisfies all the equations of second generation current conveyor.

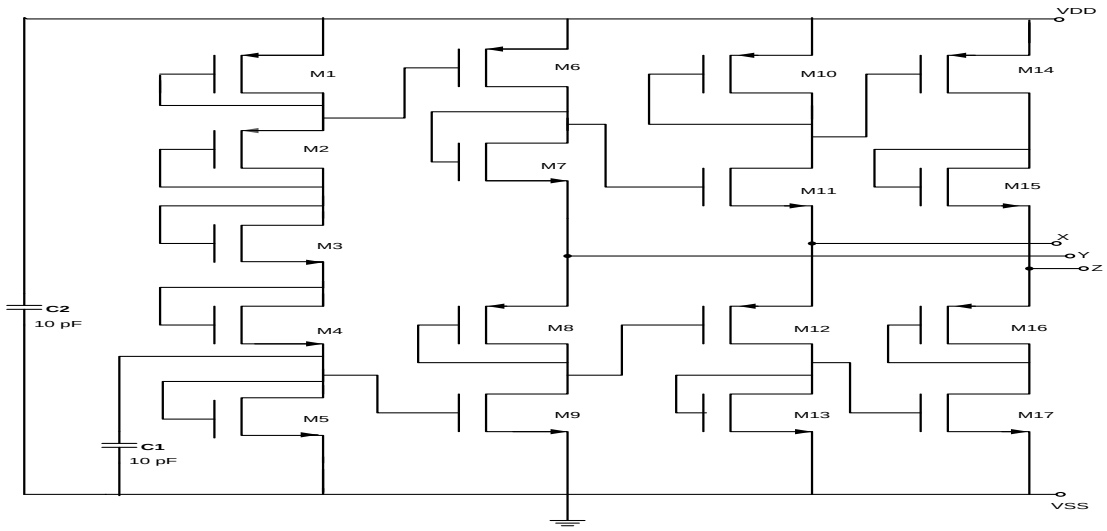


Fig 2.11 Translinear second generation current conveyor (CCII+) [9]

Table 2.1

Aspect ratio for the CCII+ in translinear mode

Transistors	W (um)	L (um)
All pMOS	100	0.5
All nMOS	50	0.5

CCII+ that is shown in Fig. 2.11 uses 0.5 micron CMOS technology. When we apply the input at Y terminal i.e. V_Y and then we check the voltage at X terminal i.e. V_X, the relationship between X and Y is shown in fig 2.12.

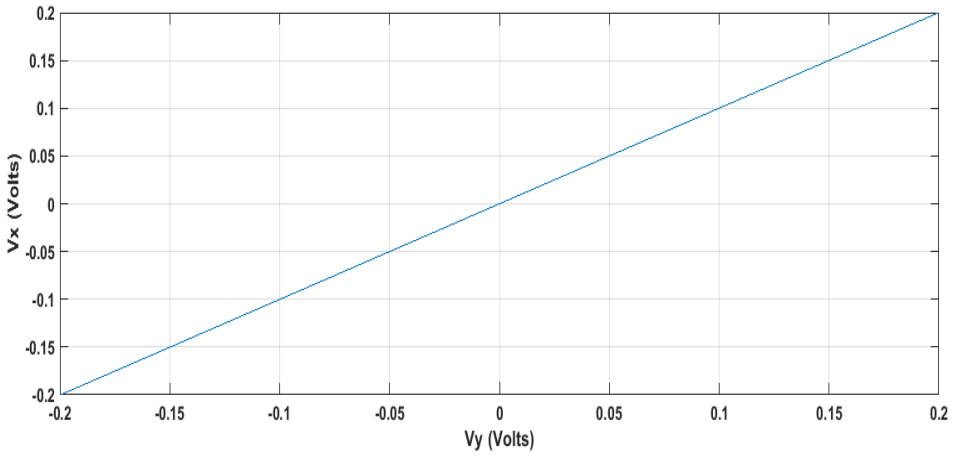


Fig 2.12 Port relationship between V_X and V_Y when we applied input dc sweep at Y terminal

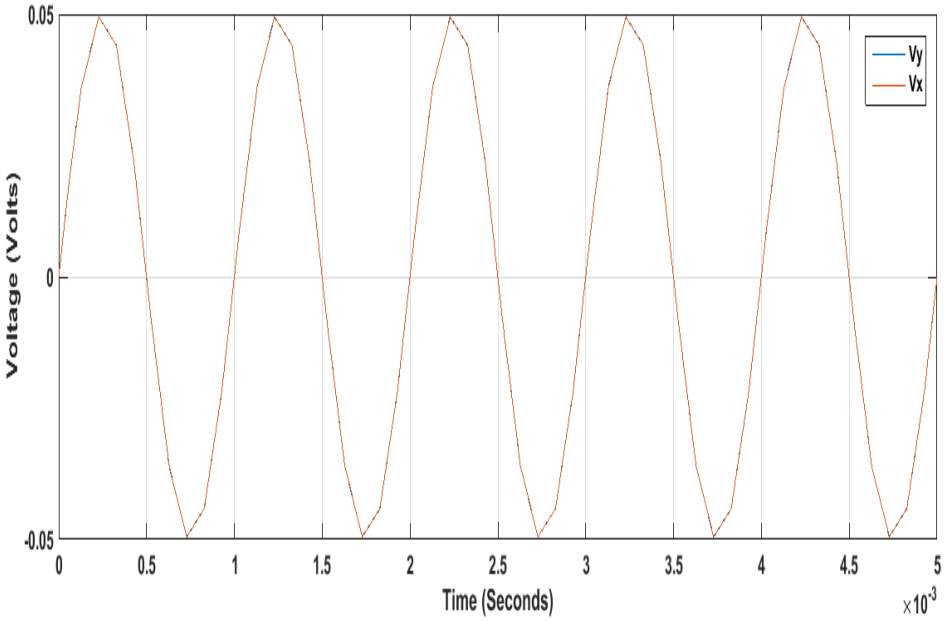


Fig 2.13 Port relationship between V_X and V_Y when we applied sinusoidal input voltage at Y terminal

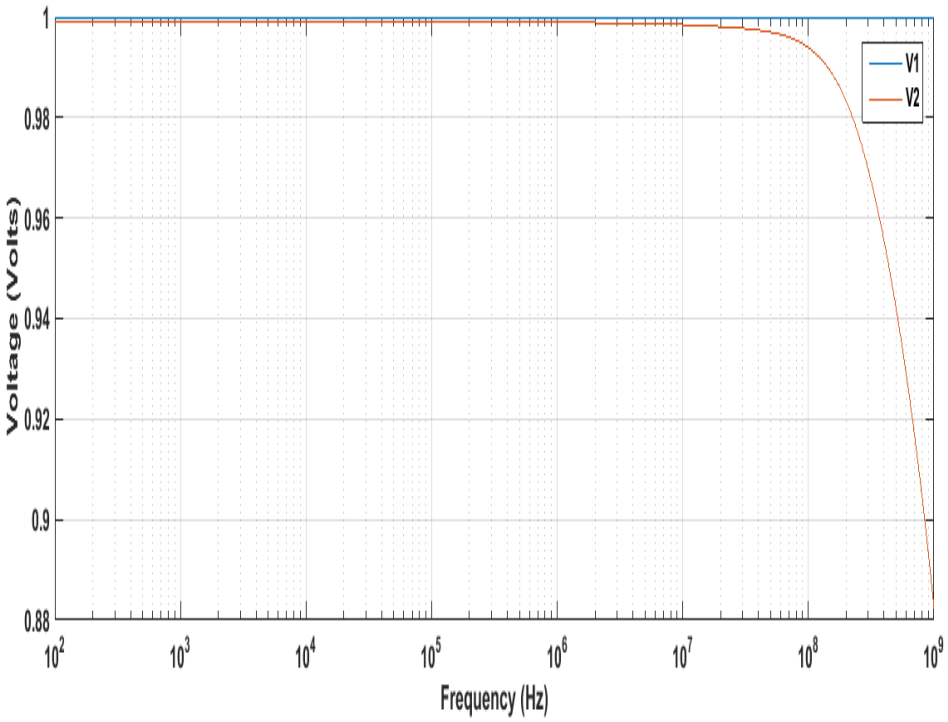


Fig 2.14 Port relationship between V_X and V_Y when we applied AC input voltage at Y terminal

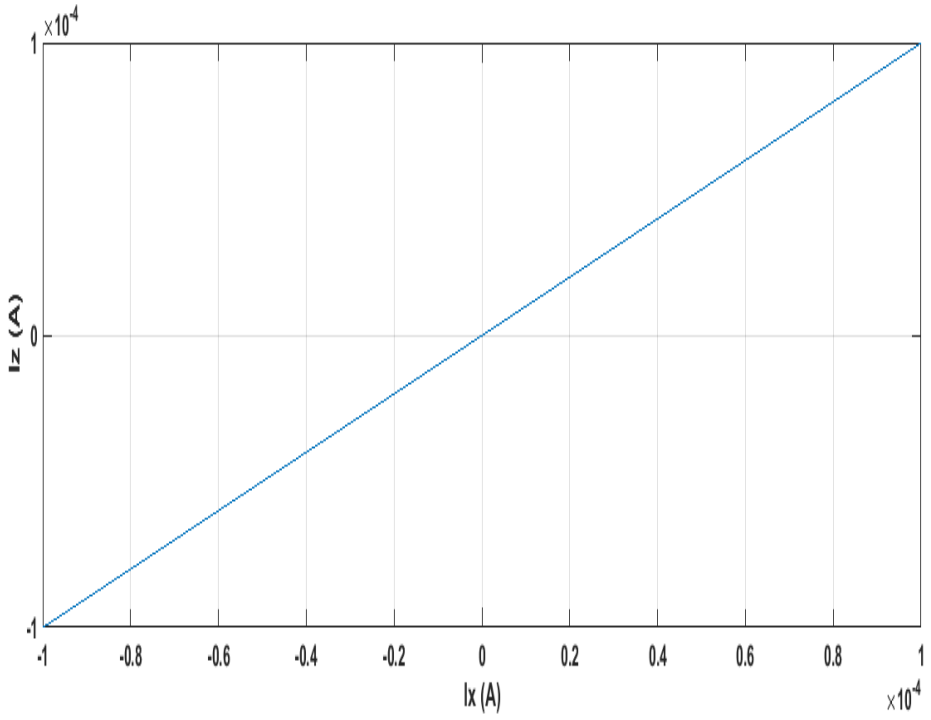


Fig 2.15 Port relationship between I_X and I_Z when we applied input dc sweep at X terminal

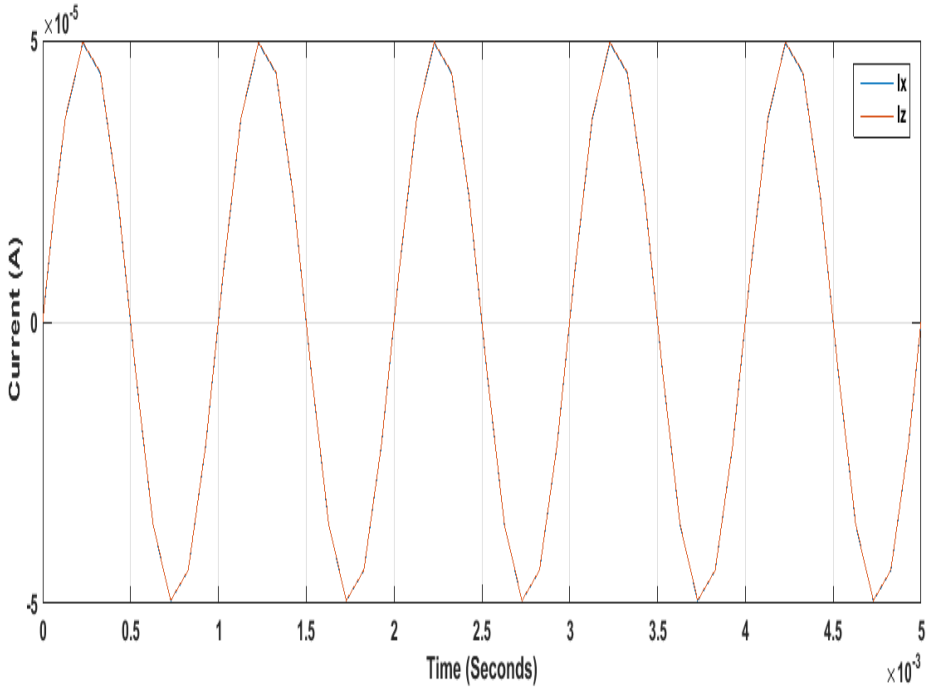


Fig 2.16 Port relationship between I_X and I_Z when we applied sinusoidal input current at X terminal

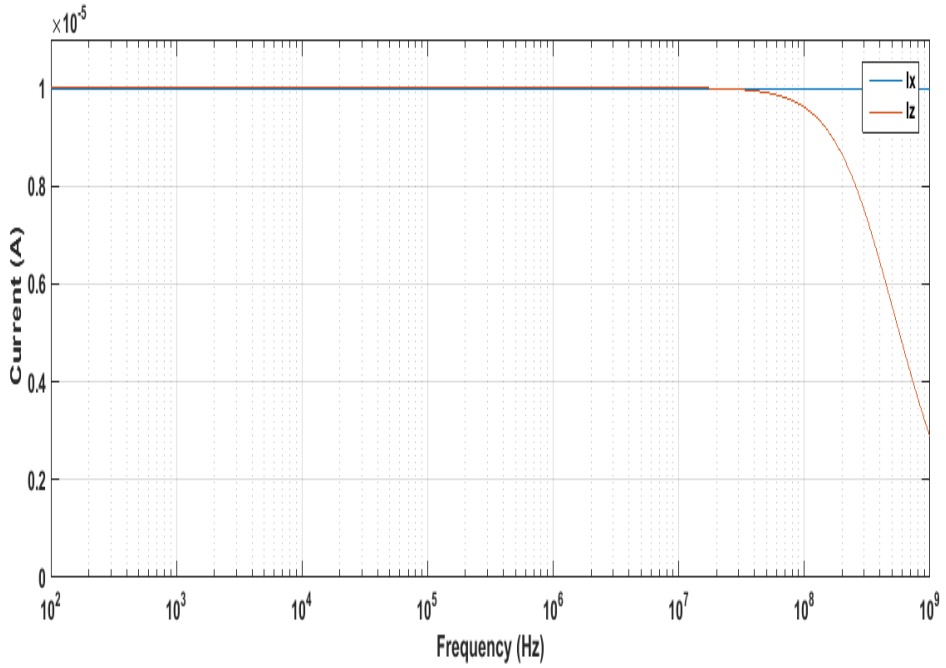


Fig 2.17 Port relationship between I_X and I_Z when we applied AC input current at X terminal

2.2.2 Second Generation Current Conveyor based on flipped voltage follower

A cell for low voltage low power analog design is known as Flipped Voltage Follower (FVF). It provides very accurate voltage following action and also it is capable to operate at low supply voltage levels. The flipped voltage follower is an improved version of conventional voltage follower i.e. common drain amplifier [23,24].

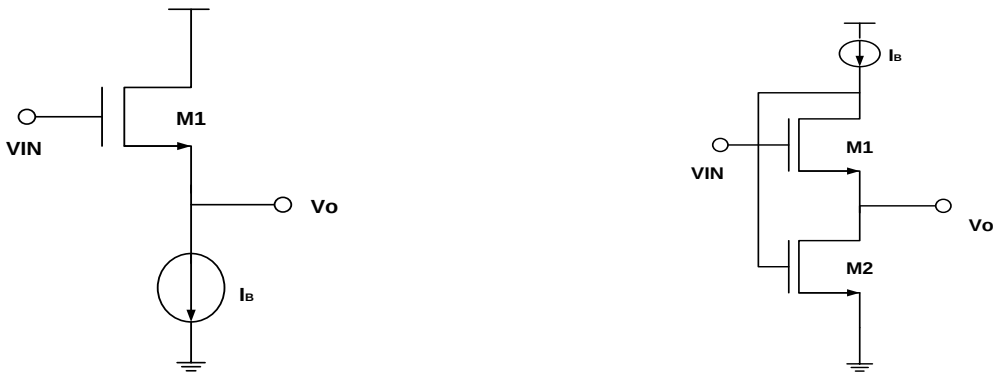


Fig 2.18 (a) Common drain amplifier circuit (b) Flipped voltage follower

The main advantages of flipped voltage follower over conventional voltage follower are

a. The current across the transistor M1 is constant and equal to the biasing current I_B. Hence, the voltage difference between the gate and source of M1(V_{GSM1}) is also constant and the small signal gain between V_O and V_{IN} is unity and it does not depend on the output current.

$$V_O = V_{IN} - V_{GSM1} \tag{2.1}$$

b. The output resistance is reduced by

$$r_o^{FVF} = \frac{1}{g_{m1} g_{m2} r_{o2}} \tag{2.2}$$

Where g_m is the transconductance and r_o is the output resistance of MOSFET transistors.

The negative feedback between the gate of M2 and the drain of M1 adjusts the voltage V_{GSM2} according to the output current. Though M2 can draw large currents, but the current sourcing capability is limited to I_B.

Flipped voltage follower is used for low-voltage design as it requires only a supply voltage of $V_{TH} + V_{eff}$, where V_{TH} is the threshold voltage and V_{eff} is the effective gate voltage equals to $V_{GS} - V_{TH.}$ The CCII structure using flipped voltage follower is shown in fig 2.19. The output of the flipped voltage follower is shifted by V_{GSM9} (Eq. 2.1), M5 connected as a diode is used as dc level shifter. It is biased by two identical current sources formed by M1 and M7 providing the high impedance input at node Y.
As $I_{DM5} = I_{DM9}$ then,

$$V_X = V_Y + V_{GSM9} - V_{GSM5} = V_Y \tag{2.3}$$

The low voltage cascode current mirror is formed by the transistor M6, M7 and M8. This current mirror copies the current through M2 to M7. The current through M2 is equal to the current through M1. The minimum operating voltage of such current mirror is $V_T + V_{Dsat}$, which is half as compared to conventional cascade current mirror.
The flipped voltage follower is formed by the transistors M9 and M10. The output

swing of flipped voltage follower is controlled by the threshold voltage V_T,

$$V_O=V_T–V_{DsatM10} \quad (2.4)$$

Where V_{Dsat} is the drain-source saturation voltage ($V_{Dsat} = V_{GS} – V_T$). M17 is used as the level shifter of V_{GSM17} in the feedback branch in order to extend the dynamic range by same quantity. Its biasing current is provided by the current source formed by M18.

In order to minimize the power consumption, the FVF must be modified for class-AB operation i.e. to be able to sink and source relatively large currents, while maintaining the output node at a constant voltage with respect to the input. Comparing the current $I_B = I_{DM3}$, which is used to bias the FVF, with the drain current I_{DM10} is used. It adjusts the voltage V_{GSM11} so that M11 sources the required current at output node. $V_{GSM10}=V_{GSM12}$, so the current through M10 is copied to M12. Respectively, $I_{DM3} = I_{DM4}$. So if current tends to flow out of node X, the drain current I_{DM10} will tend to decrease and be less than the biasing current, $I_B = I_{DM3} = I_{DM4}$.

The voltage at the gate of M11is adjusted by the high impedance node at the drain of M12, which will source current if required, keeping $I_{DM9} = I_{DM10} = I_B$valid, otherwise it will enter the cut off region. Therefore M10 can sink current from node X while M11 can source current to node X achieving class-AB operation. Further V_X depends only on the gate voltage of M9 which in turn depends on the input voltage at node Y. The current through M11 is copied to M13 using a current mirror formed by M13 and M16. Also the drain current of M10 is copied to M14. M15 is used to compensate the biasing current I_B flowing through M10 at node Z, so that $I_X = I_Z$.

Thus, by the use of flipped voltage follower as the input stage of CCII, we can have high accuracy, high speed, wider bandwidth, low output impedance, lower voltage supply requirements and low power consumption [25-27].The realization of second generation current conveyor using flipped voltage follower is shown in fig 2.19.

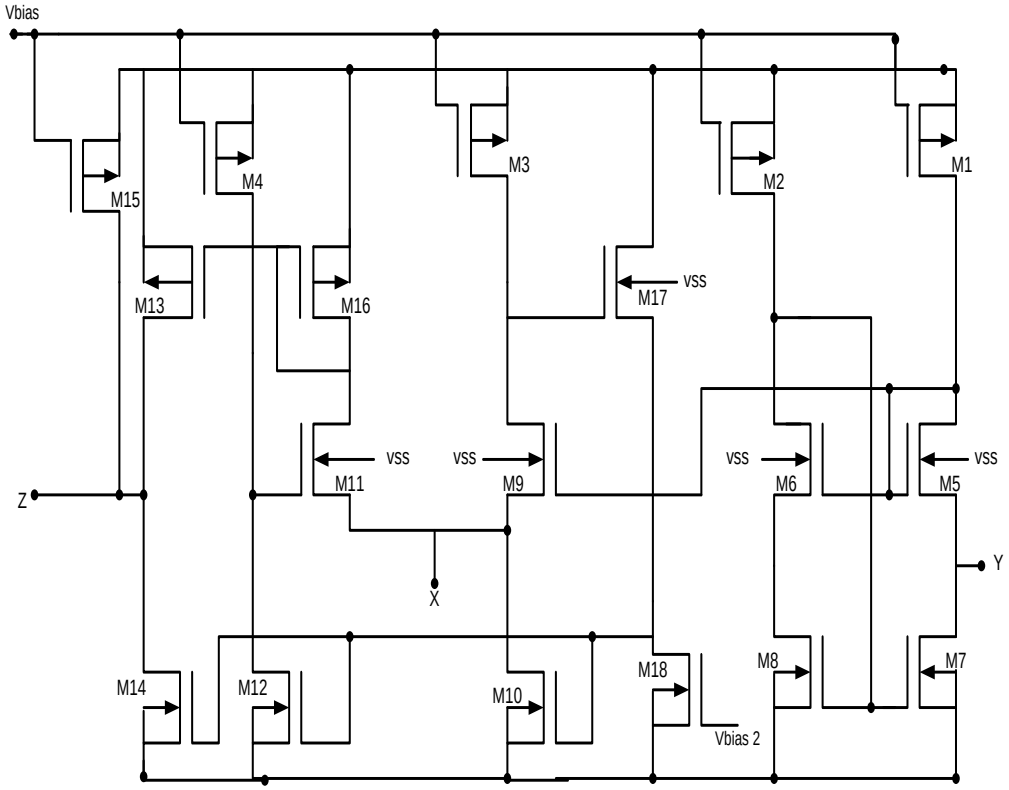


Fig 2.19 Second generation current conveyor (CCII+) using Flipped voltage follower [23]

Table 2.2

Aspect ratio for the CCII+ based on flipped voltage follower

Transistors	W (um)	L (um)
M1-M4 M10-M16	10	1
M5-M9 M17, M18	5	1

The circuit is simulated using 0.35 um CMOS technology. When we apply the input at Y terminal i.e. V_1 and then we check the voltage at X terminal i.e. V_2, the relationship between X and Y is shown below

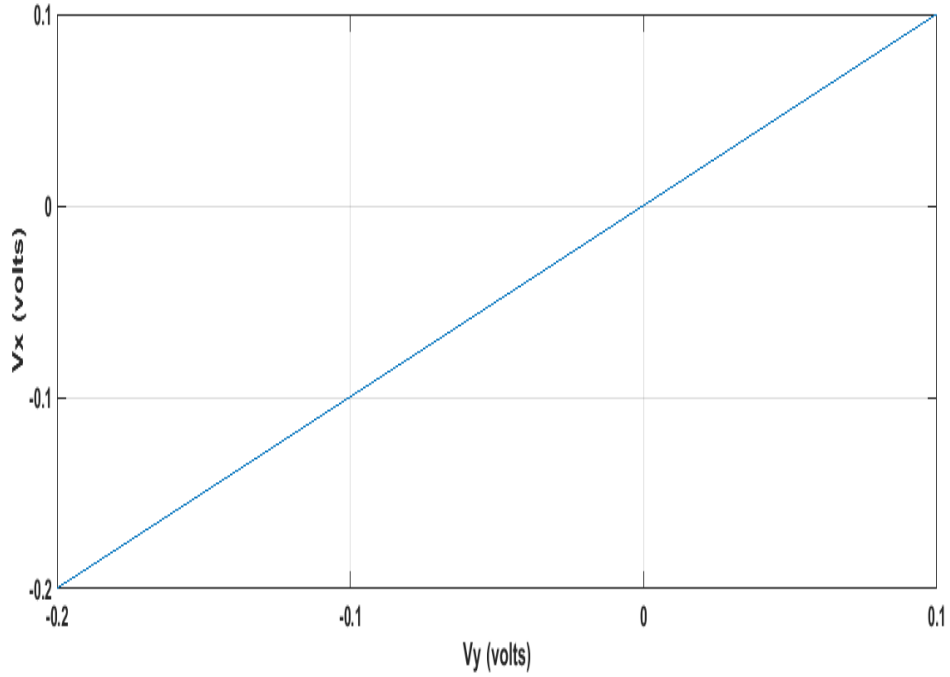


Fig 2.20 Port relationship between V_X and V_Y when dc sweep is applied at Y terminal

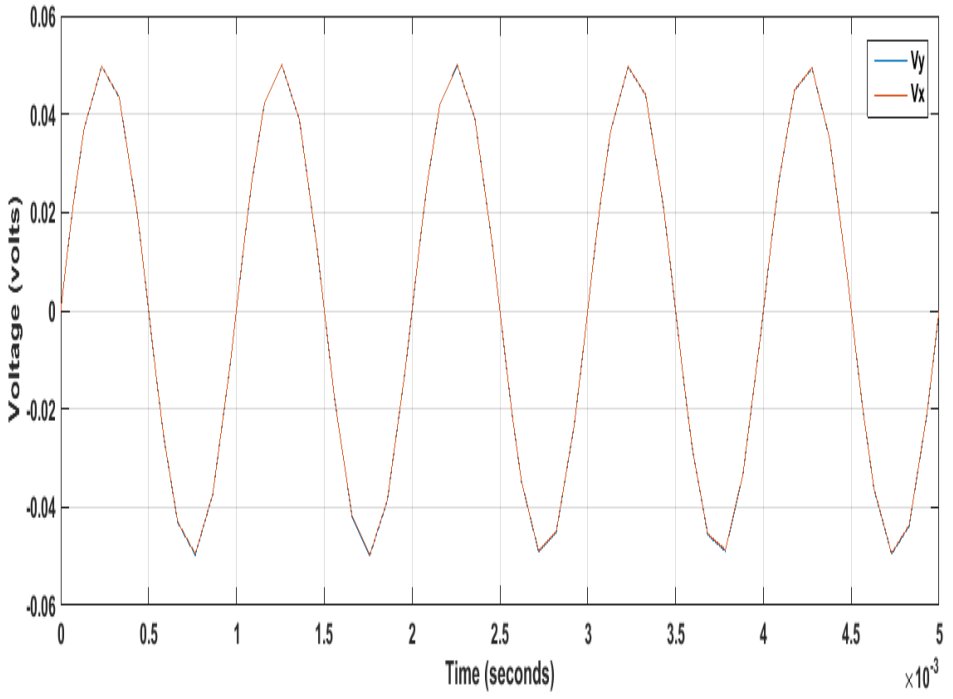


Fig 2.21 Port relationship between V_X and V_Y when sinusoidal input voltage is applied at Y terminal

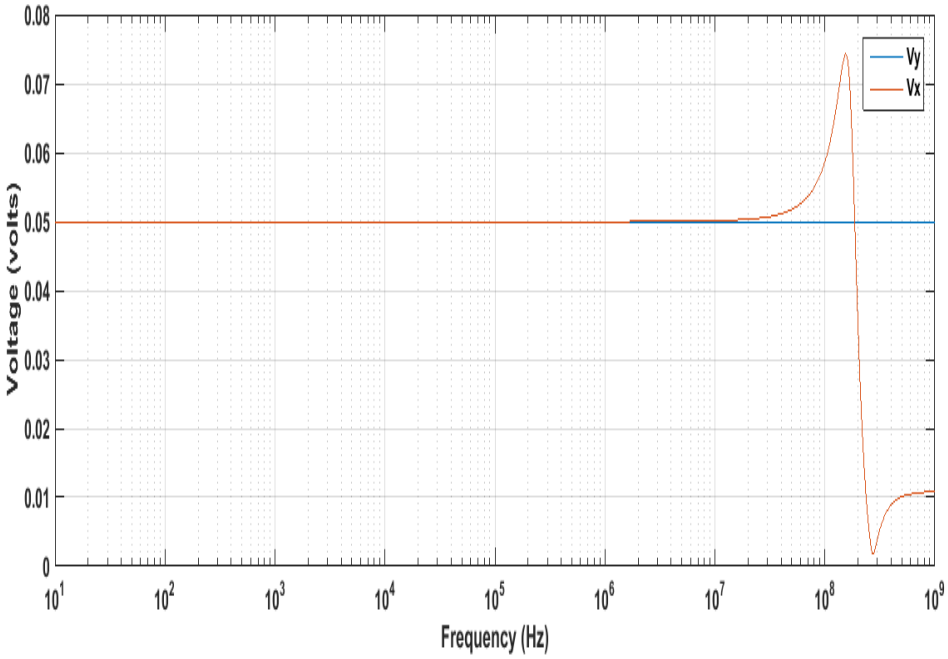


Fig 2.22 Port relationship between V_X and V_Y whenAC input voltageis applied at Y terminal

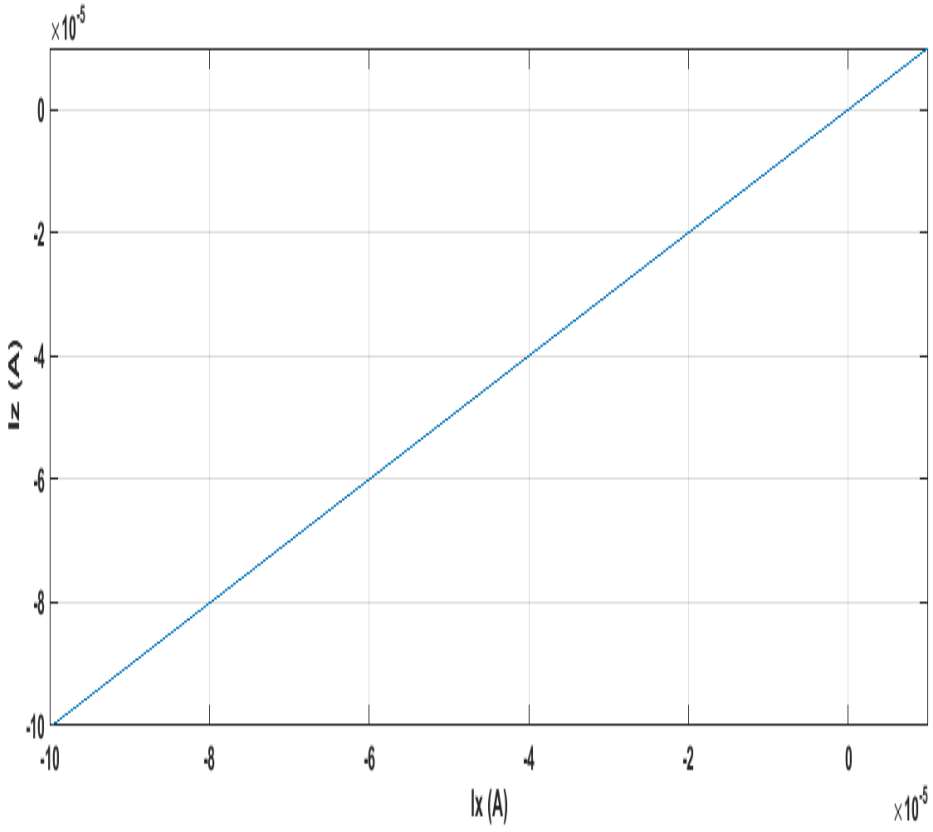


Fig 2.23 Port relationship between I_X and I_Z when dc sweep is applied at X terminal

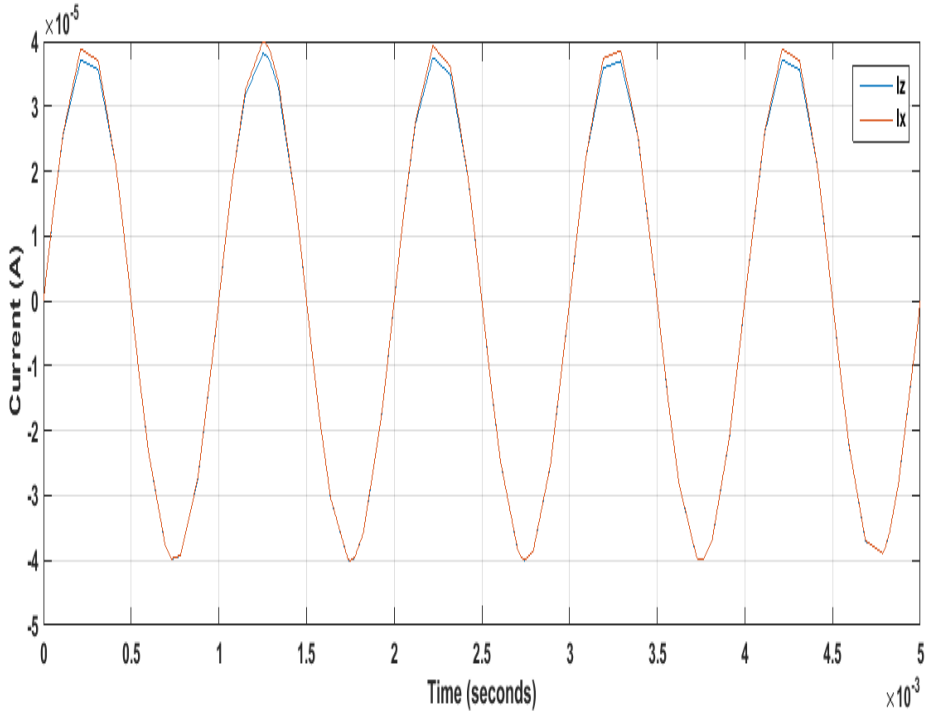


Fig 2.24 Port relationship between I_X and I_Z when sinusoidal input current is applied at X terminal

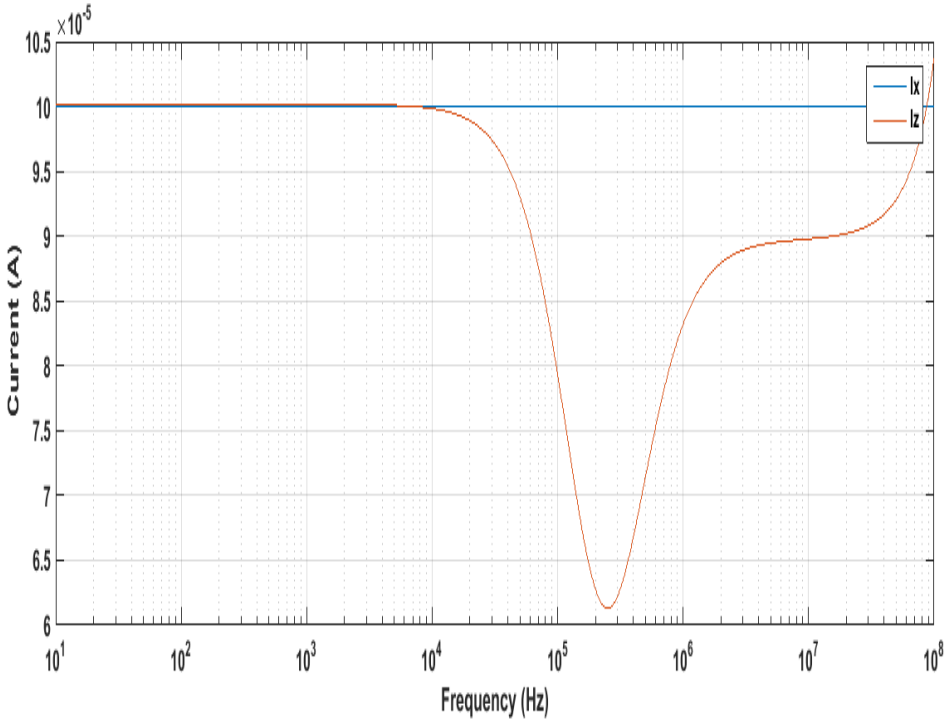


Fig 2.25 Port relationship between I_X and I_Z whenAC input current is applied at X terminal

2.3 Measurement of parasitic effects

The parasitic effects are caused due to parasitic elements, which cause imperfection in our work. Parasitic elements are the circuit elements that exist in the electrical network that can be resistance, capacitance and inductance. They are undesirable in the circuit for its intended purpose but they are unavoidable. Manufacturer of components strive to minimise these parasitic elements but they are unable to completely eliminate them. Parasitic resistances and capacitances of the active elements in a circuit cause certain limitations at low and high frequencies [20, 28, and 29]. Due to various stray capacitances and resistances involved with the MOSFETs/BJT used in any amplifier configuration the actual behaviour of the amplifier differs from the ideal behaviour as defined by the ideal terminal characteristics. Furthermore the frequency responses of the individual transistors also limit the various current transfers and voltage transfers involved in any integrated circuit. In case of current conveyors the voltage transfers and the current transfers are also characterized by deviations from their ideal value. A general model of the current conveyor where various non-idealities observed in the actual behaviour has been modelled in terms of parasitic impedances was proposed by Fabre [30]. The relationship of terminal voltages and currents is given by the matrix shown below

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} \frac{1}{R_Y // C_Y} & 0 & 0 \\ \beta & R_X & 0 \\ 0 & \alpha & \frac{1}{R_Z // C_Z} \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix}$$

Here α and β are the current and voltage transfer ratio of CCII. R_Y and C_Y are parasitic resistances on port Y and R_Z and C_Z are the parasitic resistances on port Z.

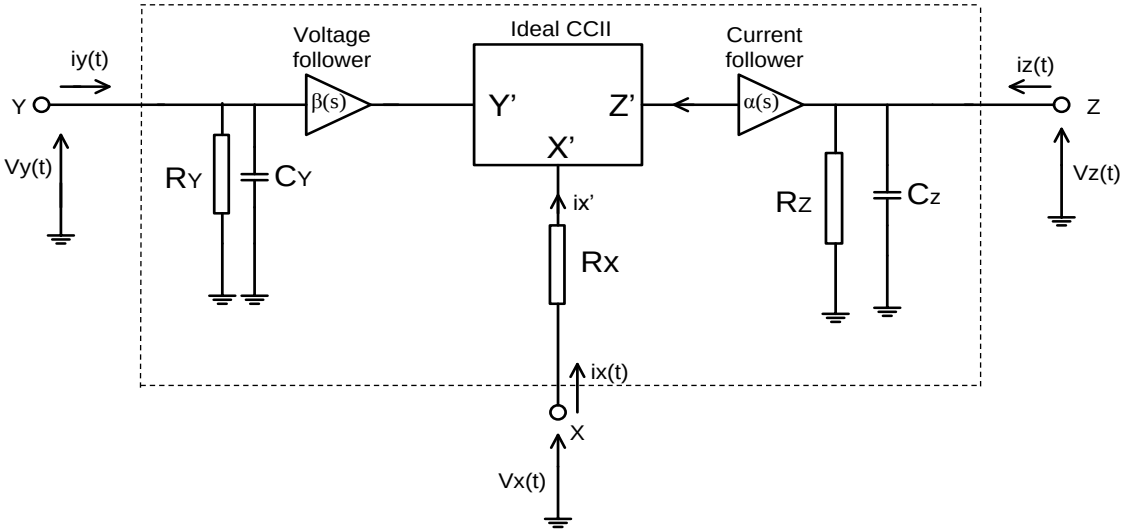


Fig 2.26 The ideal CCII with its parasitics [30]

2.3.1 Characterization by simulation

We have determined the various parasitics associated with the translinear CCII shown in Fig. 2.11 using the method suggested in [30]. $\beta(s) = V_X/V_Y$,is the voltage transfer between port X and port Y of the current conveyor. It is determined as a function of frequency, by applying infinite load R_L at port X and voltage generator with zero output resistance is applied at port Y. Port Z is grounded.

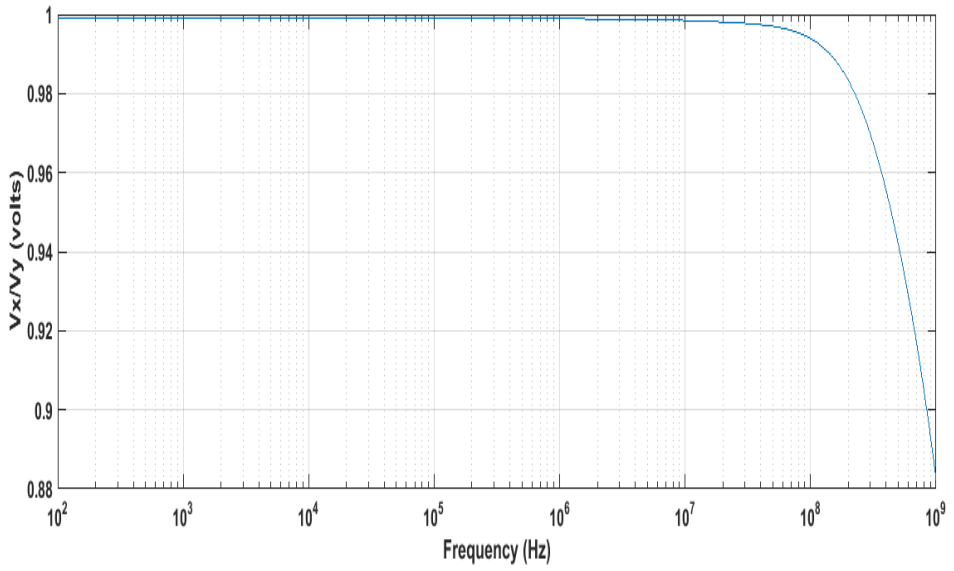


Fig 2.27 Voltage transfer ratio with respect to frequency

So, $\beta(s) = V_X/V_Y = 0.9989$

$\alpha(s) = I_Z/I_X$, It is the current transfer between port Z and port X of the current conveyor. It is determined by applying input current at port X and I_Z is the current that flows through port Z grounded. Port Z is also grounded.

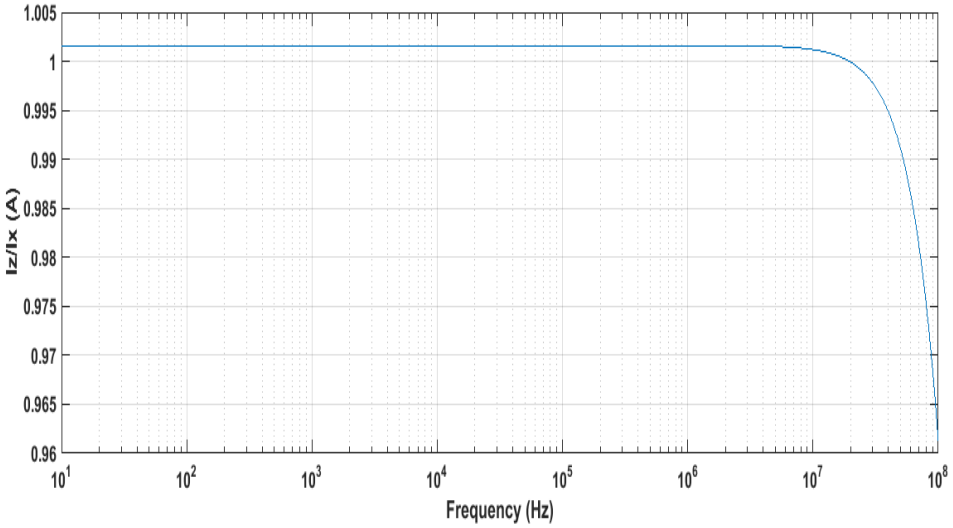


Fig 2.28 Current transfer ratio with respect to frequency

So, $\alpha(s) = I_Z/I_X = 1.0016$

The value of R_Y and C_Y is determined by applying infinite impedance at port X and port Z is grounded. AC input voltage is applied at port Y. Thenthe graph of V_Y/I_Y is plotted with respect to frequency.

$$Z_Y = V_Y/I_Y = R_Y//C_Y \qquad (2.5)$$

R_Y is the value at low frequency. C_Y is then determined by -3 dB cutoff frequency, i.e.

$$C_Y = \frac{1}{2\pi f_Y R_Y} \qquad (2.6)$$

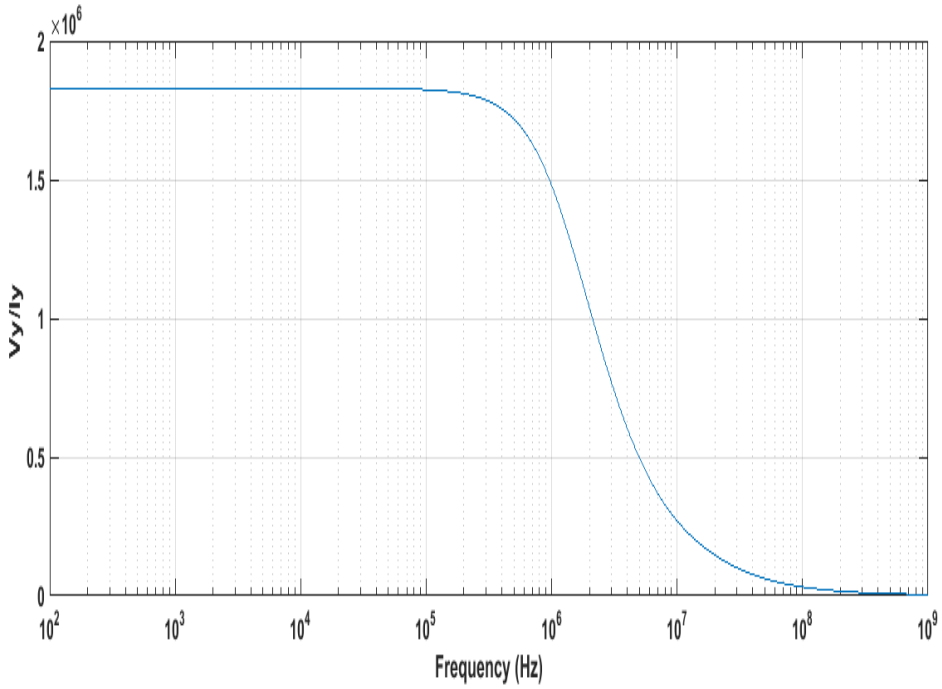


Fig 2.29 Simulation Response of V_Y/I_Y with respect to frequency

R_Y = 1.8293 Mohm, f_Y= 1.37324 MHz, C_Y = 0.063388 pF

The value of R_Z and C_Z is determined by applying infinite impedance at port Z and port Y is grounded. AC input voltage is applied at port Y. then the graph of V_Z/I_X is plotted with respect to frequency.

R_Z is the value at low frequency. C_Z is then determined by -3 dB cutoff frequency, i.e.

$$C_Z = \frac{1}{2\pi f_Z R_Z} \tag{2.7}$$

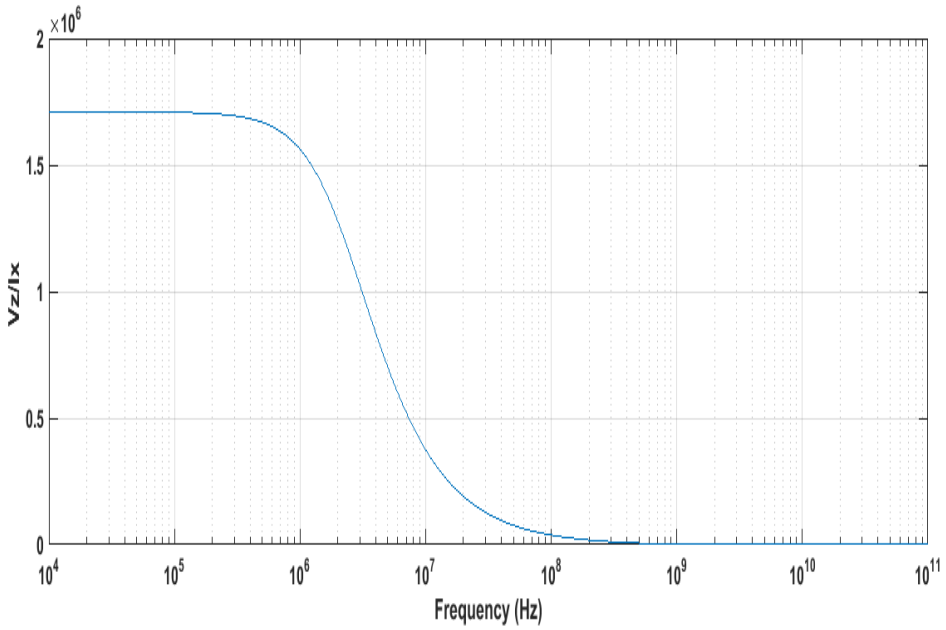


Fig 2.30 Simulation Response of V_Z/I_X with respect to frequency

R_Z = 1.7095 M ohm, f_Z= 2.2433 MHz, C_Z = 0.04152 pF

R_X is determined by applying infinite impedance at port Z and ac input voltage at port Y. R_X is that value of resistance applied at port X when voltage at port X is half of voltage at port Y.

R_X = 580 ohms.

2.4 Conclusion

In the present chapter we have reviewed some of the realizations of the CCII+ using off-the shelf available components and integrable realizations of CCII+. Complete characterizations of these realizations have been carried out in PSPICE.

CHAPTER-3

COMPONENT REALIZATION USING CCII

3.1 Grounded Inductor

Sedra and Smith introduced current conveyors as an active building block.. Current conveyors offer many advantages like wider bandwidth, greater linearity and better dynamic range over operational amplifier. Simulated immittances find lot of applications in analog signal processing because integrated circuit inductors at for low- to medium frequency applications are not economical in terms of the space requirement on the IC and poor quality factors. Grounded/floating inductor simulation using active elements like operation amplifiers very common. Recently due to availability of integrable versions of CCII+, lot of work has been carried out in the area of simulated inductances (both in the grounded as well as floating form) using them. [31, 32, 33]. In the present chapter we present some of these immittances. PSPICE simulations has been carried out to characterize these immittances. Different realizations of the same immittances using different structures of the CCII+ have been presented.

3.1.1 Lossy Grounded Inductor

The lossy grounded inductor is also called as non-ideal grounded inductor. The grounded inductor can be realized through single second generation current conveyor, single capacitor and by using one or two resistors. The grounded inductor shown in the figure below can realize a frequency dependent type of inductance i.e. series inductance.

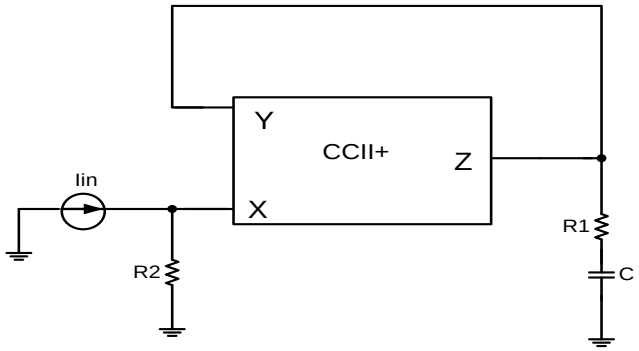


Fig 3.1 Grounded inductor using CCII+ [34]

For the circuit given in fig 3.1 the input impedance is given by

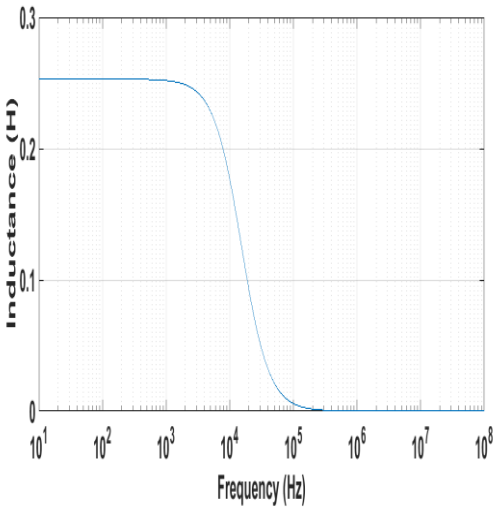
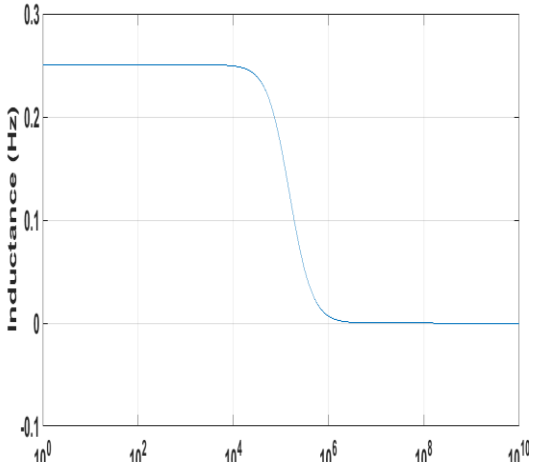
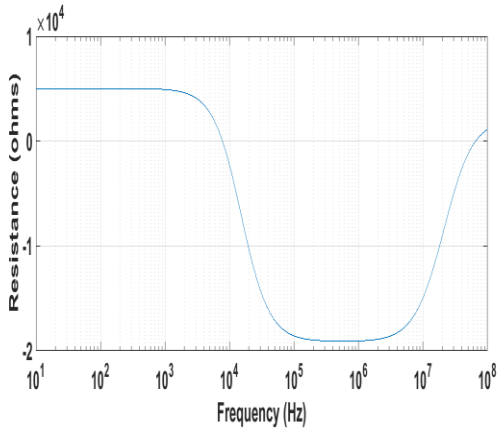
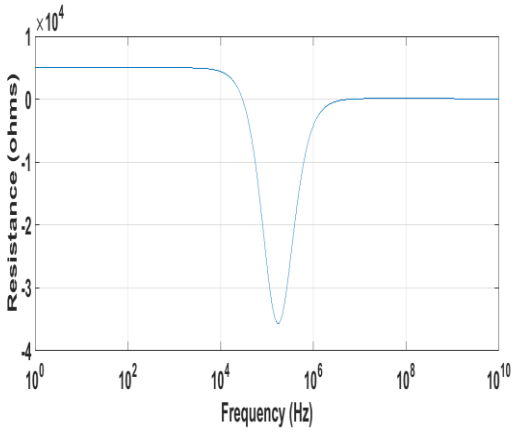
$$Z_{in} = \frac{R_2 + sCR_1R_2}{1 + sCR_1(1 - R_2/R_1)} \tag{3.1}$$

At $R_1 = R_2 = R$, the value of inductance can be given as $L = CR^2$, which can simulate the series RL impedance. Thus it can be seen that in order to simulate series RL impedance equal valued matched resistors are used [34,35].

Taking C= 10 nF, $R = R_1 = R_2 = 5$ Kohms, we get $L = CR_1R_2 = 250$ mH, which we have analysed through PSPICE simulations i.e. shown below

Table 3.1

Lossy grounded inductor realization from CCII+

	
Evaluation of inductance using CCII+ in Translinear mode	Evaluation of inductance from CCII+ using AD844
	
Evaluation of resistance using CCII+ in Translinear mode	Evaluation of resistance from CCII+ using AD844

3.1.2 Lossless Grounded Inductor

The lossless grounded inductor is also called as ideal grounded inductor which gives us the value of pure inductance. The lossless grounded inductor shown in fig 3.6 consists of two second generation current conveyor (CCII+ and CCII-), two resistance and a capacitor.

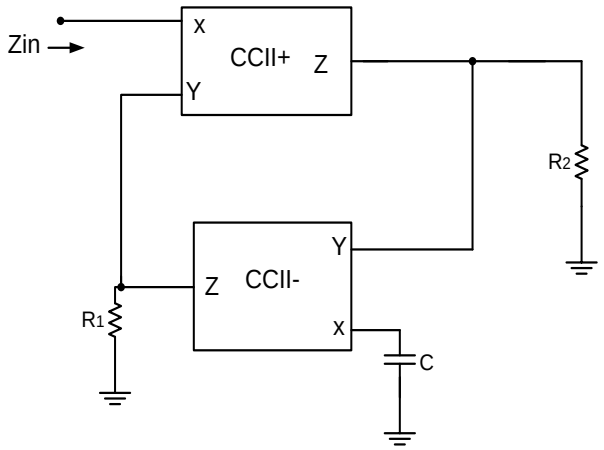


Fig 3.2 Lossless grounded inductor using CCII+ and CCII- [36]

The input impedance for the circuit given in fig 3.6 is given by

$$\text{Zin} = \frac{\text{Vin}}{\text{Iin}} = -\text{sCR}_1\text{R}_2 \tag{3.2}$$

Here, $L_{eq}= CR_1R_2$. We have realized CCII- from CCII+ as shown in figure below [37].

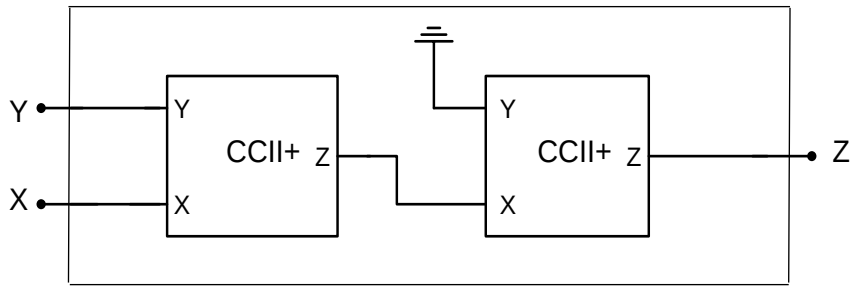
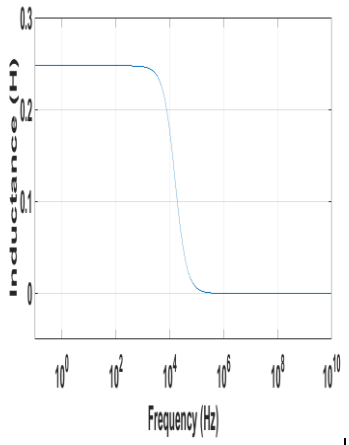
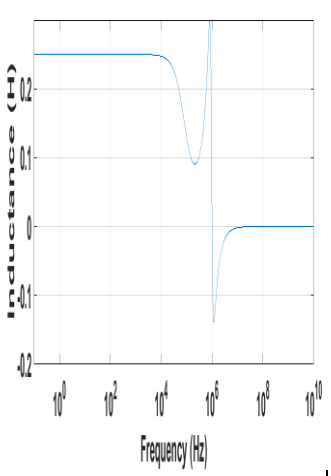
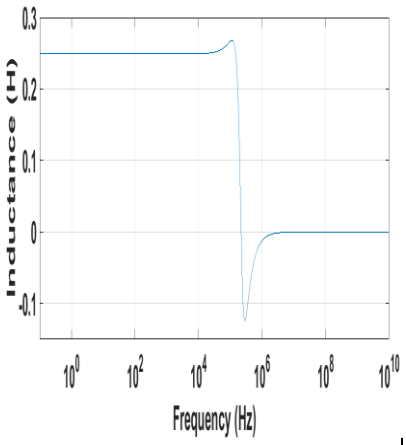


Fig 3.3 Realizing CCII- from CCII+

We have chosen $R_1 = R_2 = 5$ kohms and C = 10 nF, then as $L_{eq} = CR_1R_2 = 250$ mH, for this we have done the analysis using PSPICE simulations by evaluating the value of inductance i.e. shown below

Table 3.2

Lossless grounded inductor realization from CCII+

		
Evaluation of inductance using CCII+ in Translinear mode	Evaluation of inductance through CCII+ using flipped voltage follower	Evaluation of inductance through CCII+ using AD844

3.2 Floating Inductor

The existing methods of lossy/lossless floating inductance require two or four current conveyors and require exact matching of some components. In [38] a floating inductor is shown as lossy as well as lossless.

3.2.1 Lossy Floating Inductor

Lossy floating inductor is also known as non-ideal floating inductor as it does not gives the value of pure inductor. The lossy floating inductor which we have considered consists of two second generation current conveyor, two resistors and a single capacitor [39].

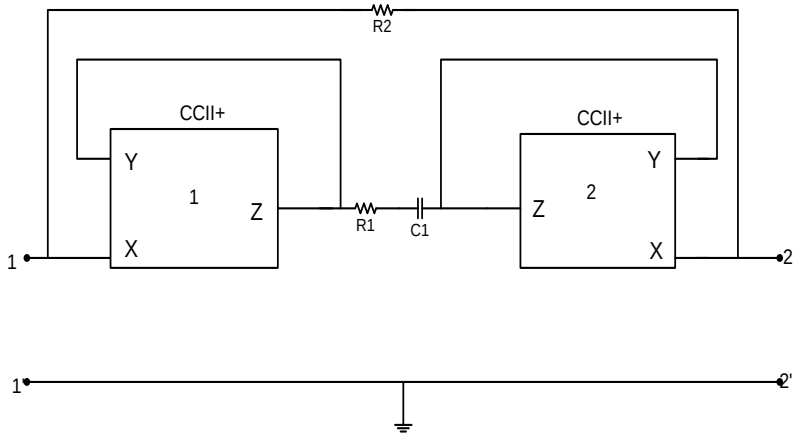


Fig 3.4 Lossy Floating Inductor using two CCII+ [34]

The short circuit admittance matrix of this two port network is given by

$$[Y] = \frac{1 + sC(R_1 - R_2)}{R_2(1 + sCR_1)} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \tag{3.3}$$

Thus, it represents a floating impedance Z(s) between terminals 1 and 2, given by

$Z(s) = R+sCR^2 = R + sL$, provided that $R_1 = R_2 = R$.

We have chosen $R= R_1 = R_2 = 5$ kohms and C = 10 nF, hence we get $L = CR^2 = 250$ mH. Using this series RL impedance we have realized second order RLC low pass filter with cut off frequency as 2.25 kHz and quality factor as 0.707, with specifications as R= 5 kohms, L= 250 mH and C = 20 nF. We have analysed this LPF filter using PSPICE simulations.

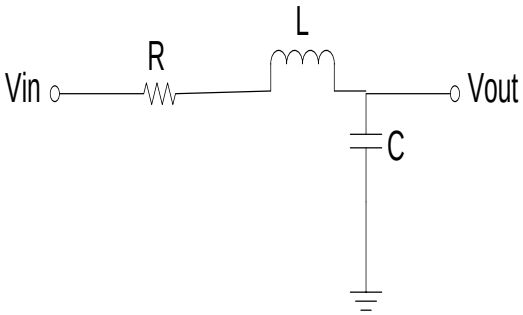


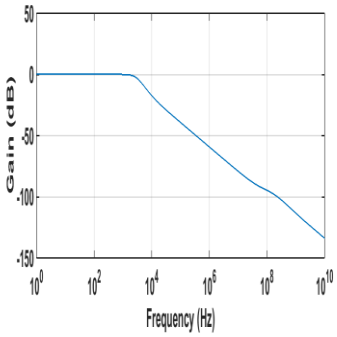
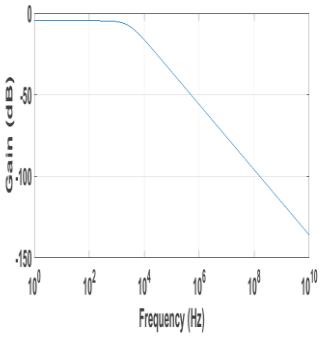
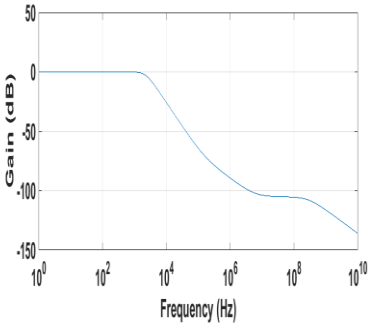
Fig 3.5 Second order RLC low pass filter

Transfer function is

$$\frac{V_o}{V_{in}} = \frac{1/LC}{s^2 + \frac{R}{L}s + \frac{1}{LC}} \tag{3.4}$$

Table 3.3

LPF realization using Lossy floating inductor realized from CCII

		
Simulation result of LPF using lossy floating inductor. This provides the LPF with cut off frequency of 3 kHz	Simulation result of LPF using lossy floating inductor. This provides the LPF with cut off frequency of 2.68 kHz	Simulation result of LPF using lossy floating inductor.This provides the LPF with cut off frequency of 2.269 kHz.

3.2.2 Lossless Floating Inductor

Lossless floating inductor is also known as ideal floating inductor as it gives the value of pure inductor. The lossless floating inductor which we have considered consists of four second generation current conveyor, two resistors and a single capacitor [40].

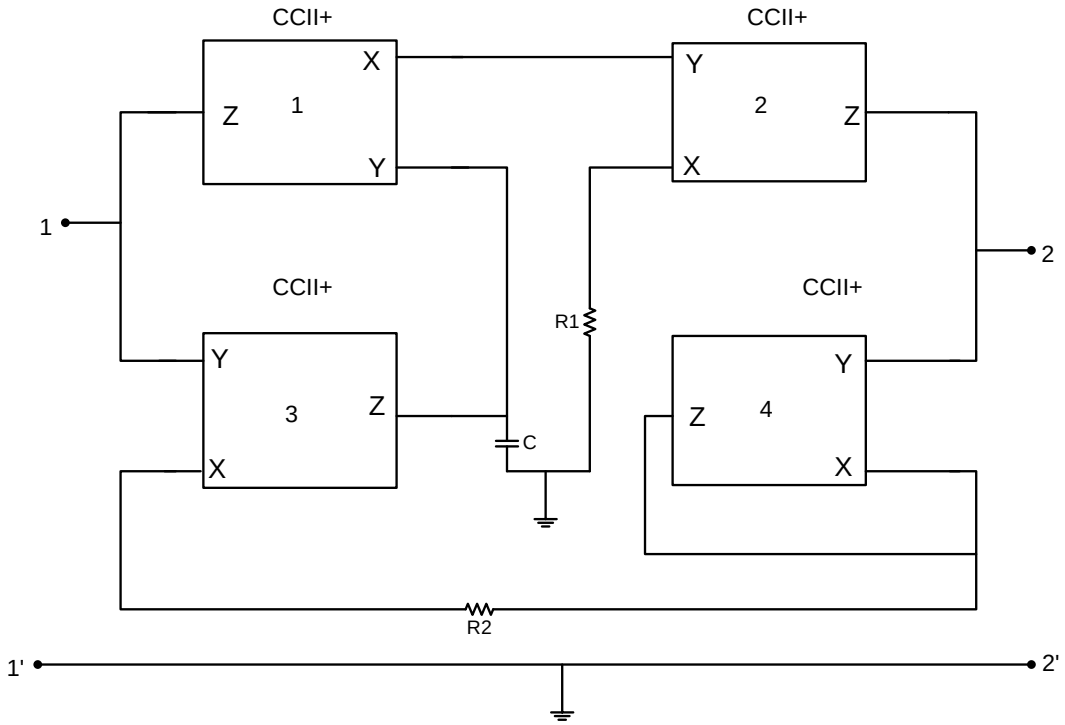


Fig 3.6 Lossless Floating Inductor using four CCII+ [41]

The Y matrix of the circuit is given by

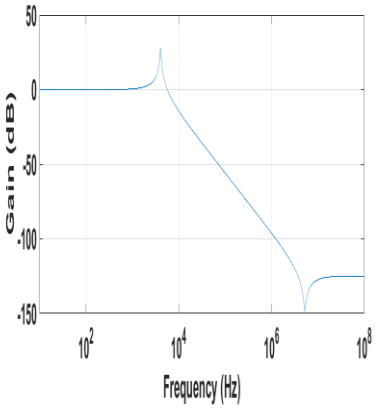
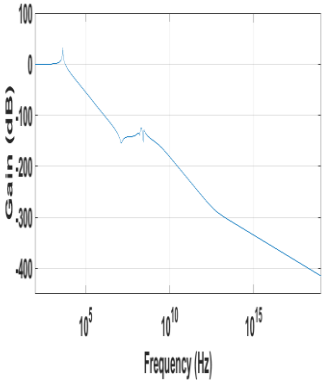
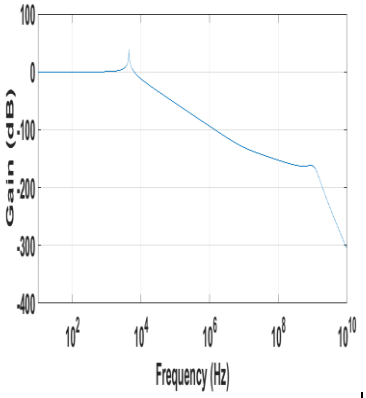
$$[Y] = \frac{1}{sCR_1R_2}\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \tag{3.5}$$

The circuit simulates lossless floating inductor $L_{eq} = sCR_1R_2$.

We have chosen R= R_1 = R_2 = 11.18 kohms and C = 10 nF, then we get L = CR^2 = 125 mH. Using this lossless floating inductor we have realized second order RLC low pass filter with cut off frequency of 4.5 kHz and quality factor as 0.707, with specifications as R= 5 kohms, L= 125 mH and C = 10 nF. We have analysed the RLC LPF (fig 3.12) using lossless floating inductor through PSPICE simulations.

Table 3.4

LPF Realization using Lossless floating inductor realized from CCII+

		
Simulation result of LPF using lossless floating inductor. This provides the LPF with cut off frequency of 4.13 kHz.	Simulation result of LPF using lossless floating inductor. This provides the LPF with cut off frequency of 4.5 kHz.	Simulation result of LPF using lossless floating inductor. This provides the LPF with cut off frequency of 4.49 kHz.

3.3 Lossless floating Capacitive Multiplier

Lossless floating capacitor provides the value of pure capacitor by using four second generation current conveyors, two resistors and a capacitor. In fig 3.16 when we interchange the position of R_1 and C, then the circuit would simulate a lossless floating capacitor [42, 43].

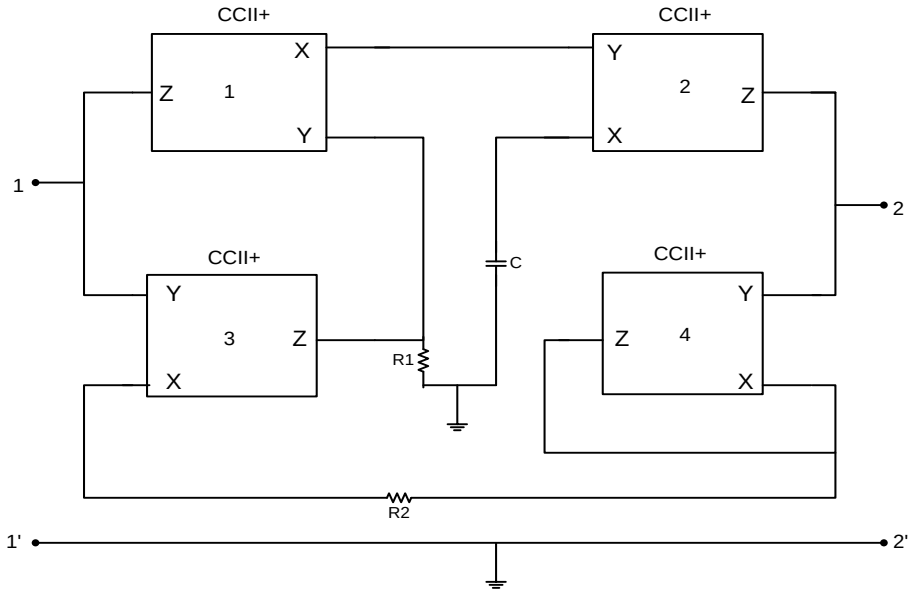


Fig 3.7 Lossless Floating Capacitor using four CCII+ [41]

The circuit simulates lossless floating capacitor with C_{eq} as

$$C_{eq} = \frac{CR_1}{R_2} \tag{3.6}$$

We have chosen R_1=5 kohms, R_2 =10 kohms and C=1 nF, then we get $C_{eq} = \frac{CR_1}{R_2} =$ 0.5 nF . Using this lossless floating capacitor we have realized second order RLC high pass filter with cut off frequency of 31.85 kHz and quality factor as 0.707, with specifications as R= 14.14 kohms, L= 50 mH and C = 0.5 nF. We have analysed this HPF filter using PSPICE simulations using Fig 3.20.

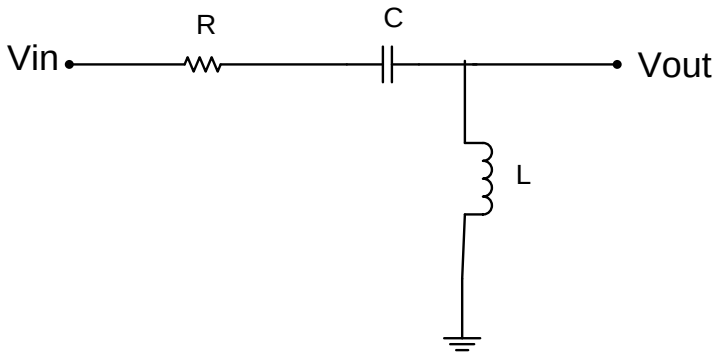


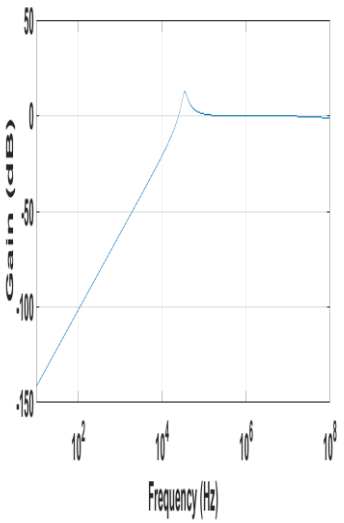
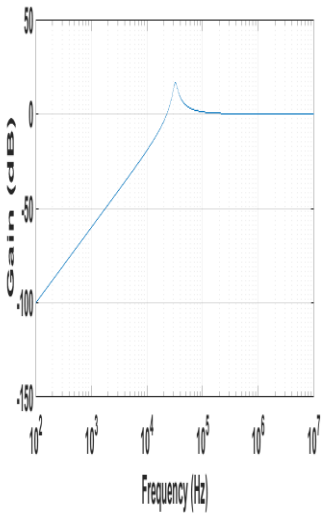
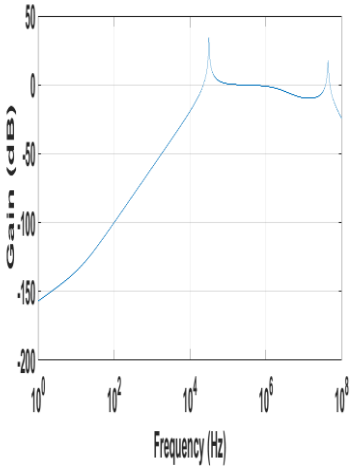
Fig 3.8 Second order RLC high pass filter

Transfer function is

$$\frac{V_o}{V_{in}} = \frac{s^2}{s^2 + \frac{R}{L}s + \frac{1}{LC}} \tag{3.7}$$

Table 3.5

HPF realization using Lossless floating capacitor realized from CCII+

		
Simulation result of HPF using lossless floating capacitor. This provides the HPF with cut off frequency of 31.18167 kHz.	Simulation result of HPF using lossless floating capacitor. This provides the HPF with cut off frequency of 30.14309 kHz.	Simulation result of HPF using lossless floating capacitor. This provides the HPF with cut off frequency of 31.41698 kHz.

3.4 Conclusion

In the current chapter we have presented simulated immittances using different realizations of the second generation current conveyor. The validity of the simulated immittances has been tested using different first order and second order filters. PSPICE simulations were carried out to verify the workability of these simulated immittances.

CHAPTER-4

FILTER DESIGNING USING CCII

In this chapter a comparative study of biquad realizations using different realizations of the second generation current conveyor is presented. The current conveyor circuit provides high frequency range of operation as compared to conventional operational amplifiers [44-46].Two circuit configurations have been chosen. One of the configurations belongs to the single input multiple output type filter category while the other configuration belongs to the Multiple input and multiple output category. The first circuit is a current mode universal filter using two CCII+ and the second circuit is a voltage mode filter using three CCII+s. Both the filters have been simulated with all the realization of the current conveyors presented in Chapter-2 and a comparison has been done in respect of input range, bias voltage and cut-off frequency. PSPICE results of time response and frequency response of all the circuits have been presented.

4.1 Current Mode Universal Filter

Figure 4.1 shows a current mode universal filter [47].

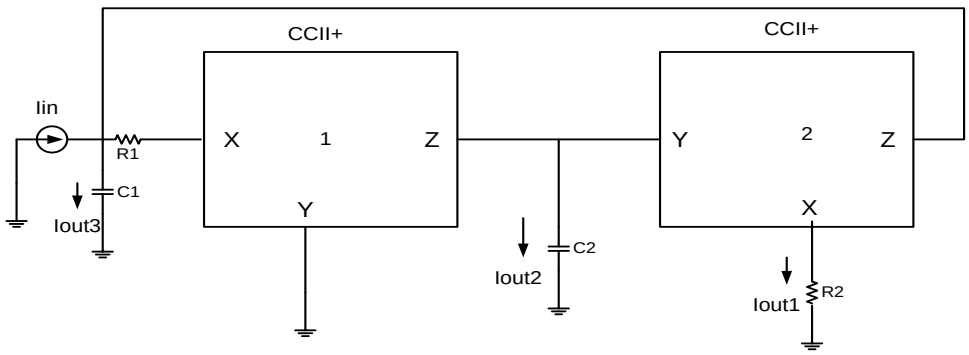


Fig 4.1 Current mode universal filter

It may be noted that the three output currents are flowing through grounded elements and additional current followers will be required to drive the loads. The various transfer functions are as given below

$$T_1(s) = \frac{I_{out1}(s)}{I_{in}(s)} = -\frac{1}{R_1R_2C_1C_2\,s^2 + R_2C_2s + 1} \tag{4.1}$$

$$T_2(s) = \frac{I_{out2}(s)}{I_{in}(s)} = -\frac{R_2C_2s}{R_1R_2C_1C_2\,s^2 + R_2C_2s + 1} \tag{4.2}$$

$$T_3(s) = \frac{I_{out3}(s)}{I_{in}(s)} = +\frac{R_1R_2C_1C_2s^2}{R_1R_2C_1C_2\,s^2 + R_2C_2s + 1} \tag{4.3}$$

The three transfer functions are respectively of low pass filter ($T_1(s)$), band pass filter ($T_2(s)$) and high pass filter ($T_3(s)$) with unity gain. These transfer functions are characterized by

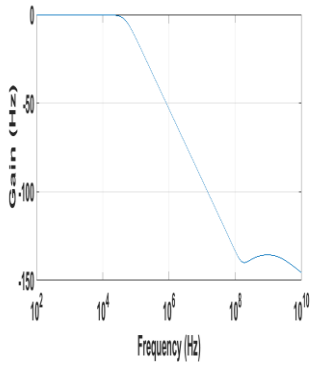
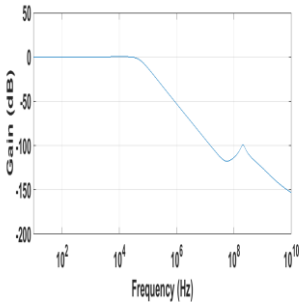
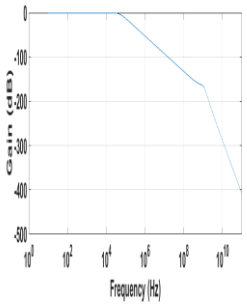
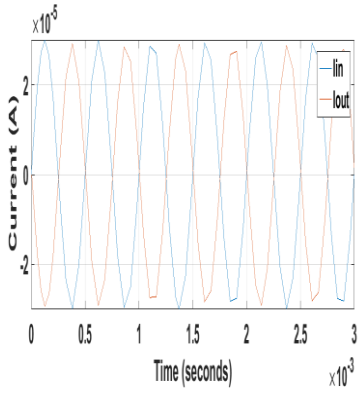
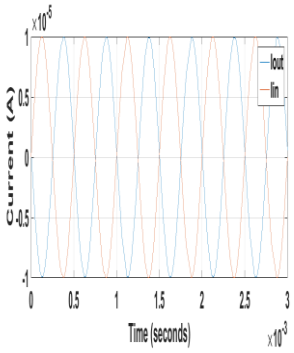
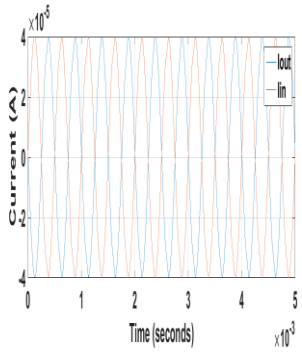
$$w_o = \frac{1}{\sqrt{R_1R_2C_1C_2}} \tag{4.4}$$

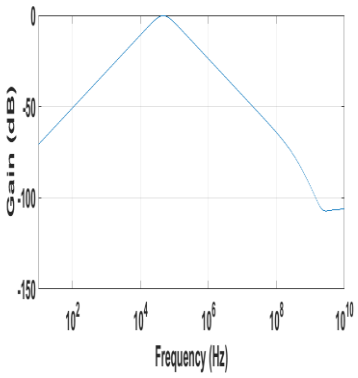
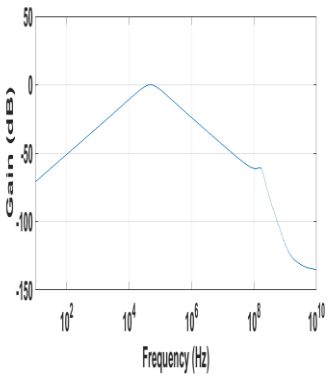
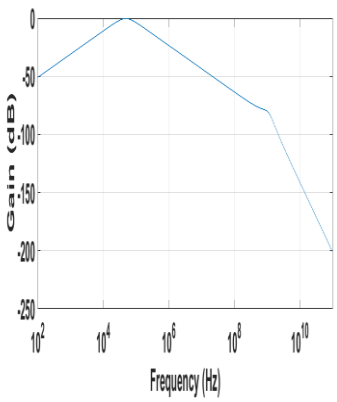
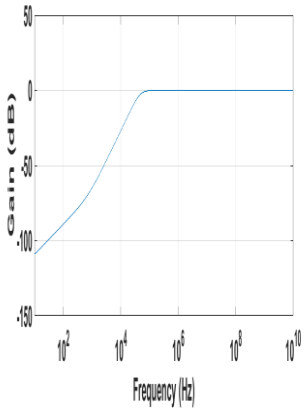
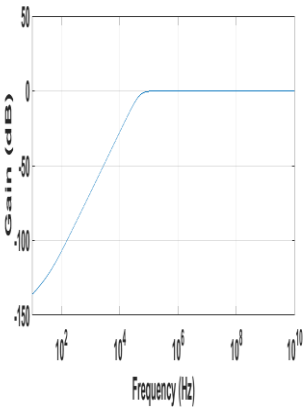
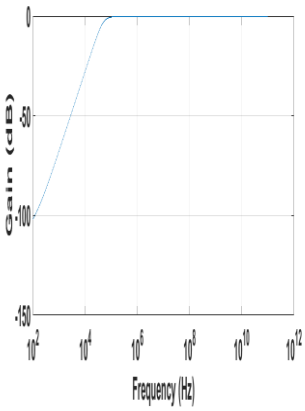
$$Q = \sqrt{\frac{R_1C_1}{R_2C_2}} \tag{4.5}$$

The above universal filter is designed using translinear implementation of CCII+, CCII+ using flipped voltage follower and CCII+ using AD844. Designed for f_o = 50 KHz and Q = 0.707, with R_1 = 10 KOHM, R_2 = 20 KOHM, $C_1 = C_2$ = 0.225 nF.

Table 4.1

Realization of current mode filter from CCII+

 Low pass filter response from translinear CCII+ with a cut off frequency of 46.43 KHz.	 Low pass filter response from CCII+ using flipped voltage follower with a cut off frequency of 49 KHz.	 Low pass filter response from CCII+ using AD844 with a cut off frequency of 48.4 KHz.
 Transient response of Low pass filter realized from translinear CCII+ when I_{in} = 30uA Sin(2π*2KHz)t	 Transient response of Low pass filter realized from CCII+ using flipped voltage follower when I_{in} = 10uA Sin(2π*2KHz)t	 Transient response of Low pass filter realized from CCII+ using AD844 when I_{in} = 40uA Sin(2π*2KHz)t

		
Band pass filter response from translinear CCII+ with a cut off frequency of 46.32 KHz.	Band pass filter response from CCII+ using flipped voltage follower with a cut off frequency of 48.8 KHz.	Band pass filter response from CCII+ using AD844 with a cut off frequency of 50.4 KHz.
		
High pass filter response from translinear CCII+ with a cut off frequency of 46.8 KHz.	High pass filter response from CCII+ using flipped voltage follower with a cut off frequency of 47.86 KHz.	High pass filter response from CCII+ using AD844 with a cut off frequency of 48.9 KHz.

From the above responses we have analysed the highest frequency, lowest supply voltage and lowest input current for low pass filter, band pass filter and high pass filter. Table 4.2-4.4 summarize these comparisons for the LP, BP and HP filters.

Table 4.2

Evaluation for Low pass filter

CCII+ configurations	**Highest Frequency**	**Lowest supply voltage**	**Lowest input current**
Trans linear CCII+	20 MHz	+/- 1.2 V	1 uA
CCII+ using AD844	100 KHz	+/- 4.5 V	0.5 uA
CCII+ using flipped voltage follower	50 MHz	+1.1 V/-0.25 V	0.05 uA

Table 4.3

Evaluation for Band pass filter

CCII+ configurations	**Highest Frequency**	**Lowest supply voltage**	**Lowest input current**
Trans linear CCII+	20 MHz	+/- 1.2 V	0.2 uA
CCII+ using AD844	100 KHz	+/- 4.5 V	0.01 pA
CCII+ using flipped voltage follower	50 MHz	+1.1 V/-0.25 V	0.002 uA

Table 4.4

Evaluation for High pass filter

CCII+ configurations	**Highest Frequency**	**Lowest supply voltage**	**Lowest input current**
Trans linear CCII+	20 MHz	+/- 1.2 V	0.1 uA
CCII+ using AD844	100 KHz	+/- 4.5 V	0.01 pA
CCII+ using flipped voltage follower	50 MHz	+1.1 V/-0.3 V	1 uA

4.2 Voltage mode universal filter

Figure 4.12 shows a multiple input single output type voltage mode multifunction voltage mode filter and employs three second generation current conveyor [48,49].

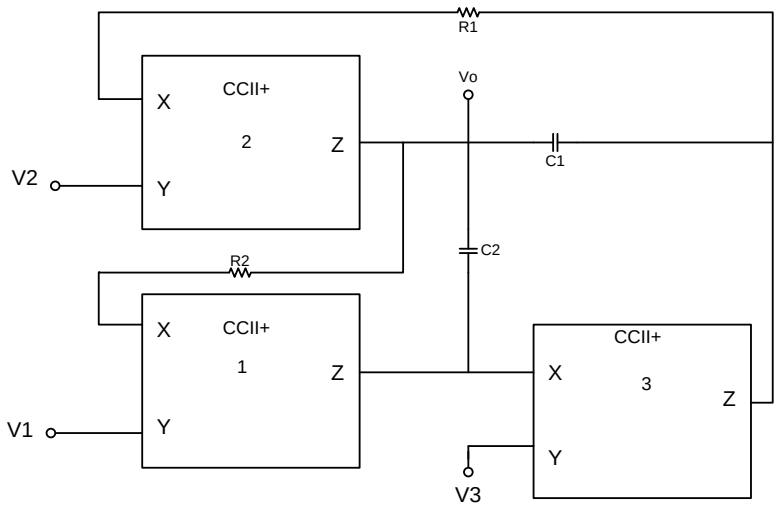


Fig 4.2 Voltage Mode Universal Filter

The output voltage V_0 can be expressed as

$$V_O = \frac{s^2C_1C_2V_3 + sC_1G_1V_2 + G_1G_2V_1}{s^2C_1C_2 + sC_1G_1 + G_1G_2} \tag{4.6}$$

From equation (4.6) we can see

If $V_2 = V_3 = 0$ i.e. grounded, a second order low pass filter can be obtained with the transfer function of V_o/V_1.

If $V_1 = V_3 = 0$ i.e. grounded, a second order band pass filter can be obtained with the transfer function of V_o/V_2.

If $V_1 = V_2 = 0$ i.e. grounded, a second order high pass filter can be obtained with the transfer function of V_o/V_3.

Thus the circuit is capable of realizing low pass, high pass and band pass filter.

The transfer functions can realize low pass filter, band pass filter and high pass filter with unity gain. This transfer functions are characterized by

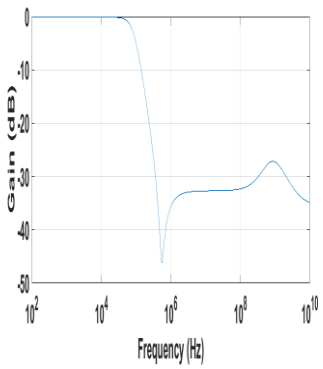
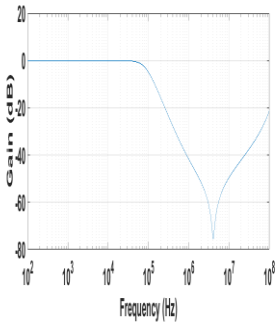
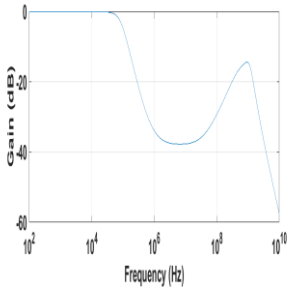
$$w_o = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}} \tag{4.7}$$

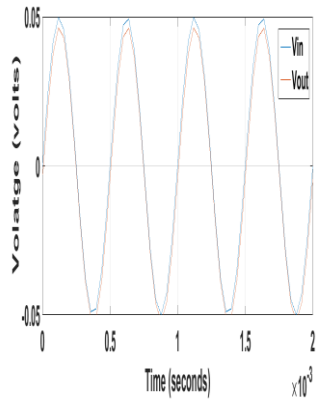
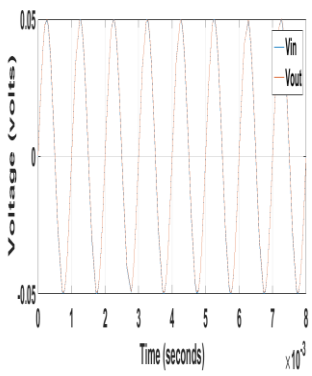
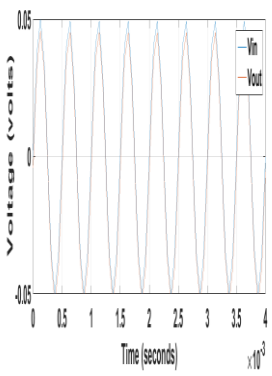
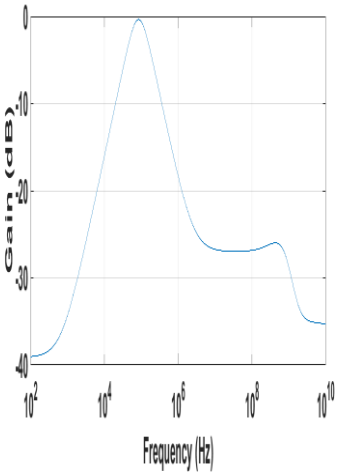
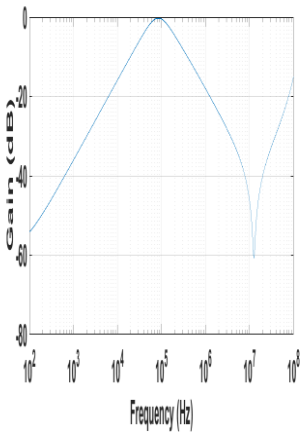
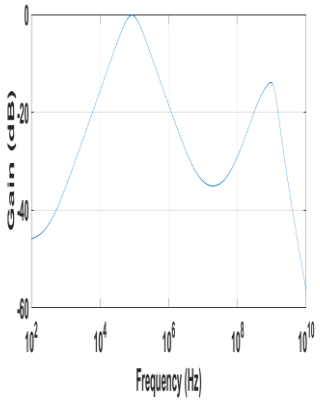
$$Q = \sqrt{\frac{R_1 C_2}{R_2 C_1}} \tag{4.8}$$

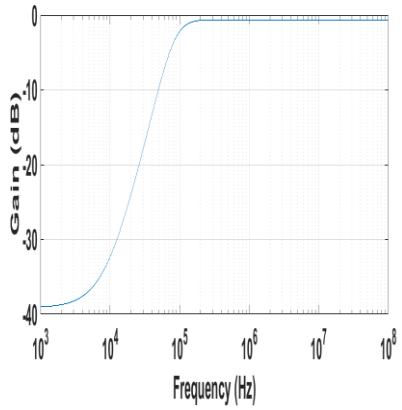
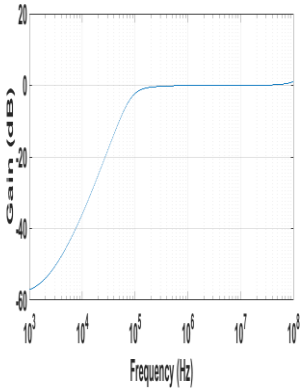
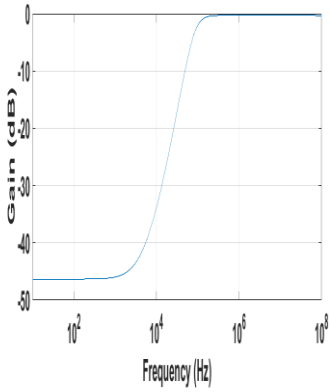
The above multifunction filter is designed using trans linear implementation of CCII+, CCII+ using flipped voltage follower and CCII+ using AD844. Designed for f_o = 90 KHz and Q = 0.707, with R_1 = 20 KOHM, R_2 = 40 KOHM, C_1 = C_2 = 0.0625 nF.

Table 4.5

Realization of voltage mode filter from CCII+

 Low pass filter response from translinear CCII+ with a cut off frequency of 83.8 KHz.	 Low pass filter response from CCII+ using flipped voltage follower with a cut off frequency of 82.8 KHz.	 Low pass filter response from CCII+ using AD844 with a cut off frequency of 85.38 KHz.

		
Transient response of Low pass filter realized from CCII+ in Translinear mode when V_{in} = 50mV Sin (2π*2KHz)t	Transient response of Low pass filter realized from CCII+ using flipped voltage follower when V_{in} = 50mV Sin (2π*1KHz)t	Transient response of Low pass filter realized from CCII+ using AD844 when V_{in} = 50mV Sin (2π*2KHz)t
		
Band pass filter response from translinear CCII+ with a cut off frequency of 85.114 KHz.	Band pass filter response from CCII+ using flipped voltage follower with a cut off frequency of 85.114 KHz.	Band pass filter response from CCII+ using AD844 with a cut off frequency of 85.114 KHz.

		
High pass filter response from CCII+ in Translinear mode with a cut off frequency of 82.34 KHz.	High pass filter response from CCII+ using flipped voltage follower with a cut off frequency of 89 KHz.	High pass filter response from CCII+ using AD844 with a cut off frequency of 84.37 KHz.

From the above responses we have analysed the highest frequency, lowest supply voltage and lowest input voltage for low pass filter, band pass filter and high pass filter and the results are summarized below.

Table 4.6

Evaluation for Low pass filter

CCII+ configurations	**Highest Frequency**	**Lowest supply voltage**	**Lowest input voltage**
Trans linear CCII+	10 MHz	+/- 0.5 V	10 mV
CCII+ using AD844	200 KHz	+/- 3 V	20 mV
CCII+ using flipped voltage follower	150 KHz	+1 V/-0.06 V	3 mV

Table 4.7

Evaluation for Band pass filter

CCII+ configurations	**Highest Frequency**	**Lowest supply voltage**	**Lowest input current**
Trans linear CCII+	10 MHz	+/- 0.5 V	15 mV
CCII+ using AD844	150 KHz	+/- 3 V	40 mV
CCII+ using flipped voltage follower	150 KHz	+1.1 V/-0.2 V	3 mV

Table 4.8

Evaluation for High pass filter

CCII+ configurations	**Highest Frequency**	**Lowest supply voltage**	**Lowest input voltage**
Trans linear CCII+	10 MHz	+/- 0.5 V	10 mV
CCII+ using AD844	150 KHz	+/- 4 V	35 mV
CCII+ using flipped voltage follower	1 MHz	+1.1 V/-0.2 V	5 mV

4.3 Conclusions

In the present chapter we have carried out a comparative study of different realizations of one current mode and one voltage mode universal filter circuit in respect of input current/voltage range, cut-off frequency, bias voltages. We have used three different implementations of the simulated grounded inductors based on the flipped voltage follower topology, translinear loops and the bipolar current conveyor available in the current feedback amplifier AD844. Frequency response and transient response of all the filters have been presented. The translinear CCII based filter circuits have highest

cut-off frequencies while the lowest input voltage is possible with the flipped voltage follower based CCII+. For the current mode filter circuit the highest cut-off frequency is possible with flipped voltage follower based circuit and the lowest input current is possible with the translinear CCII based circuit.

CHAPTER-5

HIGHER ORDER FILTER DESIGN USING CURRENT CONVEYOR

5.1 Introduction

Current conveyors have been used to design biquad and higher order filters.. In the present chapter we present the application of current conveyors in the design of higher order filters.

A filter whose order is 3 or more than 3 is known as higher order filter. Generally, a third-order filter is characterised by a slope of 60 db/decade, a fourth-order filter produces 80 db/decade and so on at the edge of the passband. The transfer function of higher order filter is given as

$$H(s) = \frac{V_0}{V_{in}} = \frac{N(s)}{D(s)} = \frac{a_m s^m + a_{m-1} s^{m-1} + \ldots + a_1 s + a_0}{s^n + b_{n-1} s^{n-1} + \ldots + b_1 s + b_0} \qquad (5.1)$$

Where $n \geq m$ and $n > 2$. The higher order filter can be realized basically through three methods described below [50]:

5.1.1 The Cascade Method

Here the higher order filter is formed by cascading the lower order filters. This method uses modular approach. The high order function is factorized in low order functions formed into the form of sub networks.

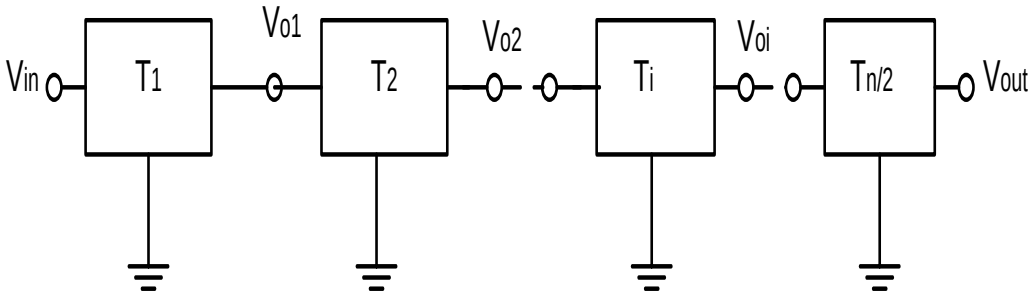


Fig 5.1 Cascade realization of nth order filter

This method is most widely used in industry as it is very easy to understand, to implement and a very efficient method. It is the simplest way to build a third-order low-pass filter by cascading a first order filter with a second-order. Similarly a fourth-order low-pass filter can be formed by cascading two second-order low-pass filters. Although there is no limit to the order of the filter that can be formed, as the order of the filter increases, so does its size. Also the accuracy declines, in that the difference between the actual stop band response and the theoretical stop band response increases with an increase in the order of the filter.

5.1.2 Element Substitution Method

Ladder simulation can be done through element replacement method. In this method, all inductors are replaced by the circuit of gyrators or generalised impedance converters, whose input impedance over the appropriate frequency range is inductive. Then the resulting active components are inserted into the LC filter topology. The element substitution method does not allow itself very easily to signal level scaling for dynamic range optimization. It realizes ideally

$$Z_{in}(jw) = jwCR_1R_2 = jwL_o \qquad (5.2)$$

5.1.3 Leap Frog (LF) Method

This topology has low sensitivity to component tolerances, low noise and reduced complexity. This design is simple as the element values can be calculated

directly from the transfer functions coefficients. It is a more robustway to simply extend the concepts of operational simulation to higher order passive networks. Filters designed using leapfrog method are called as leapfrog filters. Leapfrog filters are built up stage by stage, simulating the V-I characteristics of each passive component.

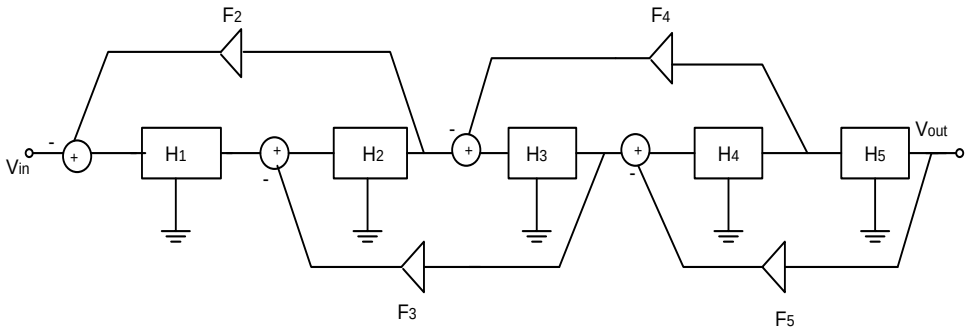


Fig 5.2 Leap frog topology of high order active filters

5.2 Fourth Order High Pass Butterworth Filter Design

We have designed a fourth order High Pass Butterworth filter using element replacement method i.e. replacing grounded inductors with the lossless grounded inductor using CCII+ that we have simulated in earlier chapter (fig 3.6). Fourth order High Pass Butterworth filter of 5 kHz cut off frequency and quality factor of 0.707 is designed with specifications as $L_1 = L_2 = 24.36$ mH, $C_1 = 55.37$ nF, $C_2 = 15.616$ nF, $R_s = R_L = 1$ Kohms.

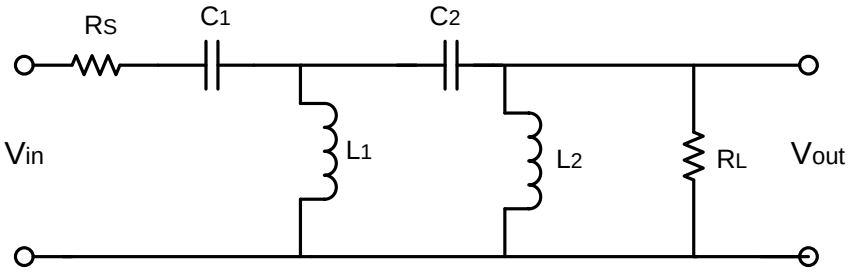


Fig 5.3 4thorder High Pass Butterworth filter design

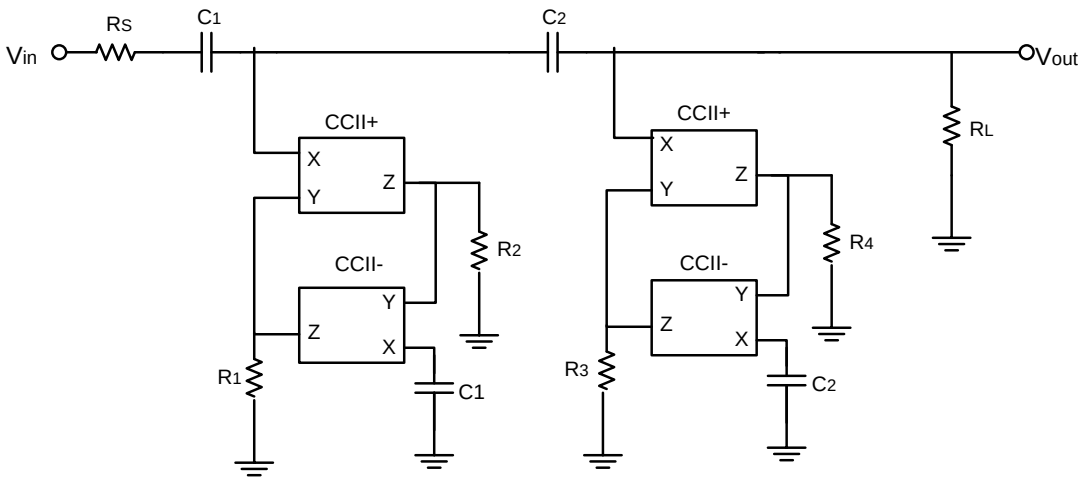


Fig 5.4 4th order High Pass Butterworth filter design using element replacement method

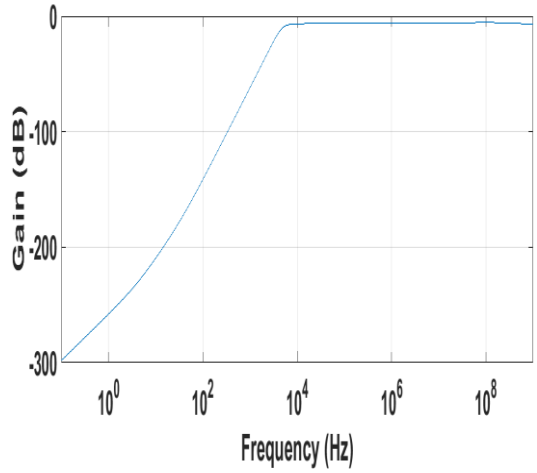
The transfer function is given as

$$\frac{V_o}{V_{in}} = \frac{s^4}{s^4\left(1+\frac{R_s}{R_L}\right) + s^3\left(\frac{R_s}{L_1}+\frac{R_s}{L_2}+\frac{1}{C_1R_L}+\frac{1}{C_2R_L}\right) + s^2\left(\frac{1}{L_1C_1}+\frac{1}{L_2C_1}+\frac{1}{L_2C_2}\right) + s\left(\frac{1}{L_1C_1R_LC_2}+\frac{R_s}{L_1L_2C_2}\right) + \frac{1}{L_1L_2C_1C_2}}$$

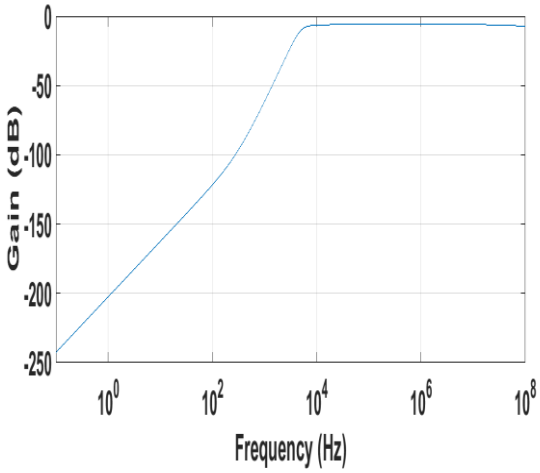
..... (5.3)

Table 5.1

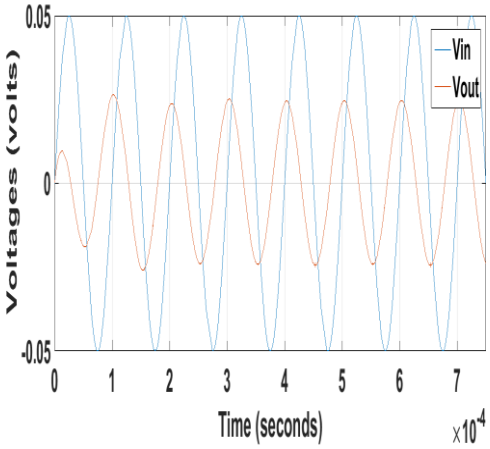
4rth order Butterworth filter design using CCII+



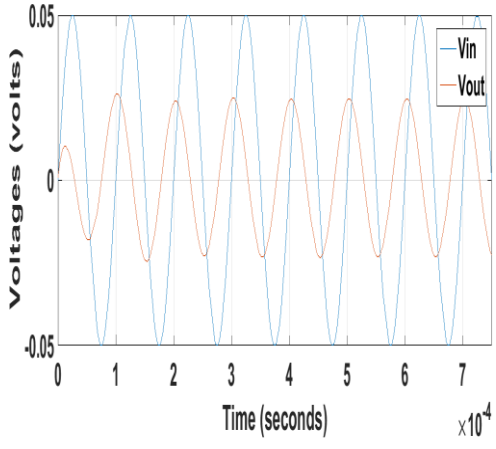
4rthorder Butterworth filter response using CCII+ using flipped voltage follower with a cut off frequency of 5.2 kHz.



4rthorder Butterworth filter response using CCII+ using AD844 with a cut off frequency of 5.4 kHz.



Transient response of 4rth order Butterworth filter using CCII+ using flipped voltage follower when V_{in} = 50mV Sin (2π*10KHz)t



Transient response of 4rth order Butterworth filter using CCII+ using AD844 when V_{in} = 50mV Sin 2π*10KHz)t

5.3 Conclusions

In the present chapter we have presented the design and implementation of a fourth order voltage mode Butterworth highpass filter base on the element replacement approach of designing highpass filter. We have used two different implementations of the simulated grounded inductors based on the flipped voltage follower topology and the bipolar current conveyor available in the current feedback amplifier AD844. Frequency response and transient response of the fourth order high pass filter have been presented. As the flipped voltage follower based inductor can operate with reduced bias levels the filter circuit is suitable for low voltage applications.

CHAPTER-6

CONCLUSION AND SCOPE IN THE FUTURE

6.1 Conclusion

The second generation current conveyor is one of the most versatile current mode building block as it has been used in wide range of applications. Several circuit realizations have been presented for its circuit implementations. Current conveyors provide a substitute method for implementation of an analog system in an impressive manner. The adaptability of the device permits its production in the integrated form. Three versions of the current conveyor were proposed over a period of three decades. During the last two decades numerous derivative of the basic current conveyor and their versions have been proposed in the literature.

Although the block diagram of second generation current conveyor is similar to the first generation current conveyor except the only change that is there no current flows in terminal ‘y’. Hence, infinite input impedance exists at terminal ‘y’. The terminal ‘x’ shows zero input impedance as the voltage at terminal ‘x’ follows the voltage that is applied to terminal ‘y’. The current that is provided to ‘x’ terminal is carried to high impedance output terminal ‘z’ where it is provided with either positive polarity (CCII+) or negative polarity (CCII-). The current conveyor can provide finer gain bandwidth products than comparable op-amps under small and large signal processing conditions. In case of Instrumentation amplifiers, their gain does not depend on the matching of pairs of external components, whereas it depends only on the absolute value of single circuit element. Due to its low power and low voltage characteristics current conveyors are most widely known in analog signal processing. CCII can be used as a voltage buffer as well as current buffer.

In the chapter -2 we have described several circuit realizations of the current conveyor using OPAMPS and OTAs, supply current sensing, translinear mode, flipped voltage follower-based and using AD844 IC.

In Chapter -3 of the dissertation we have presented the application of the current conveyors in the realization of simulated immittances. Some earlier works on simulated immittances have been reviewed. We have characterized these immittances using different realizations of the current conveyor given in chapter-2. Workability of these simulated immittances have been verified using different realizations of the current conveyors.

In Chapter-4 we have presented a comparative study of two multifunction second order filters realized with different structures of the second generation current conveyor. The limitations of different realizations in terms of input range, cut-off frequency, bias voltages/currents have been presented.

In Chapter-5 the applications of current conveyors in the design of higher order filters using the element substitution method has been presented. A fourth order high pass filter with Butterworth characteristics has been designed in which the grounded inductor of the prototype passive structure has been replaced with the simulated inductors presented in Chapter-2.

6.2 Scope for further work in future

In [1] many active building blocks have been proposed in which current conveyor is acting as a core element. The input/output terminals of the current conveyors are connected to current/voltage differencing units resulting in new active building blocks with additional functionalities. The work carried out in this dissertation can be extended to examine the best configuration of the current conveyor for a particular realization of the combined block. In addition a comparative study of various realizations of the current conveyor in other signal processing applications namely, signal generation may also be carried out.

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APPENDICES

APPENDIX 1

PSPICE model file used for process and electrical parameters CMOS 0.5 um from TSMC Technology

```
.MODEL nmos_transistor NMOS (LEVEL=3
+ UO=460.5 TOX=1E-8 TPG=1 VTO=.62
+ JS=1.8E-6 XJ=.15E-6 RS=417 RSH=2.73
+ LD=4E-8 ETA=0 VMAX=130E3 NSUB=1.71E17
+ PB=.761 PHI=.905 THETA=.129 GAMMA=.69
+ KAPPA=0.1 AF=1 WD=1.1E-7 CJ=76.4E-5
+ MJ=.357 CJSW=5.68E-10 MJSW=.302
+CGSO=1.38E-10 CGDO=1.38E-10 CGBO=3.45E-10
+ KF=3.07E-28 DELTA=0.42 NFS=1.2E11)


.MODEL pmos_transistor PMOS (LEVEL=3
+ UO=100 TOX=1E-8 TPG=1 VTO=-.58
+ JS=.38E-6 XJ=.1E-6 RS=886 RSH=1.81
+ LD=3E-8 ETA=0 VMAX=113E3 NSUB=2.08E17
+ PB=.911 PHI=.905 THETA=.12 GAMMA=.76
+ KAPPA=2 AF=1 WD=1.4E-7 CJ=85E-5
+ MJ=.429 CJSW=4.67E-10 MJSW=.631
CGSO=1.38E-10 CGDO=1.38E-10 CGBO=3.45E-10
+ KF=1.08E-29 DELTA=0.81 NFS=.52E11)
```

APPENDIX 2

PSPICE model file used for process and electrical parameters CMOS 0.35 um from TSMC Technology

```
.MODEL nmos_transistor NMOS (LEVEL = 3,
+TOX = 7.9E-9 NSUB = 1E17 GAMMA=0.5827871
+PHI=0.7 VTO=0.5445549 DELTA=0 UO = 436.256147
+ETA = 0 THETA = 0.1749684 KP =2.055786E-4
+VMAX=8.309444E4 KAPPA=0.2574081
+RSH = 0.0559398 NFS = 1E12 TPG = 1 XJ = 3E-7
+LD=3.162278E-11 WD=7.046724E-8 CGDO=2.82E-10,
+CGSO = 2.82E-10 CGBO = 1E-10 CJ = 1E-3 PB = 0.9758533,
+MJ =0.3448504 CJSW=3.777852E-10 MJSW=0.3508721)

.MODEL pmos_transistor PMOS (LEVEL = 3
+TOX = 7.9E-9 NSUB = 1E17 GAMMA=0.4083894
+PHI=0.7 VTO=-0.7140674 DELTA=0 UO =212.2319801
+ETA=9.999762E-4 THETA=0.2020774 KP = 6.733755E-5
+VMAX = 1.181551E5 KAPPA = 1.5 RSH = 30.0712458
+NFS = 1E12 TPG=-1 XJ = 2E-7 LD=5.000001E-13
+WD=1.249872E-7 CGDO=3.09E-10 CGSO = 3.09E-10
+CGBO = 1E-10 CJ = 1.419508E-3 PB=0.8152753
+MJ=0.5 CJSW=4.813504E-10 MJSW=0.5)
```