Implementation of Various Filters Using OTRA

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CERTIFICATE

This is to certify that the ***Mr. Aman Harsh, Roll no. 2k14/cCi/15****, student of* ***M.Tech, Control & Instrumentation, Department of Electrical Engineering, Delhi Technological University,*** *has submitted the dissertation entitled "****Implementation of various filters using OTRA****" under my supervision in partial fulfilment of the requirement for the award of the degree of Master of Technology in Electrical Engineering (Control & Instrumentation). This dissertation is a record of his work carried out by him under my guidance and supervision and has not been presented earlier for the award of any degree/diploma.*

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Aman Harsh

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LIST OF SYMBOLS

S. No.	Symbols	Descriptions
1	Q	Quality factor
2	S	Stability factor
3	BW	Band width
4	W	Cut off Frequency
5	OTRA	Operational Transresistance Amplifier
6	K_P	Proportional Coefficient
7	K_I	Integral Coefficient
8	K_D	Derivative Coefficient
9	g_m	Trans-conductance
10	Z_i	Input Impedance
11	Z_o	Output Impedance
12	V_{ss}	Source Supply Voltage
13	V_{DD}	Drain Supply Voltage
14	I_o	Bias Current
15	I_b	Bias Current
16	OTA	Operational Trans-conductance Amplifier
17	CC	Current Conveyor
18	CFA	Current Feedback Amplifier
19	CFOA	Current Feedback Operational Amplifier
20	CMOS	Complementary Metal Oxide Semiconductor
21	OA	Operational Amplifier

22	SFG	Signal Flow Graph
23	VLSI	Very Large Scale Integration
24	VCVS	Voltage Controlled Voltage Source
25	VCCS	Voltage Controlled Current Source
26	CCVS	Current Controlled Voltage Source
27	L	Inductor
28	LP	Low pass filter
29	HP	High pass filter
30	W/L	Transistor Aspect Ratio
31	C_{OX}	Gate Oxide Capacitance Per Unit Area
32	BJT	Bipolar Junction Transistor
33	CCCII	Second Generation Current Controlled Current Conveyor
34	$H_i(s)$	Transfer Function For Current Mode
35	$H_v(s)$	Transfer Function For Voltage Mode

ABSTRACT

The low-voltage and low-power mixed mode circuit design has gained importance with the advent of the portable electronic and mobile communication systems. More and more mixed mode circuit blocks, are being integrated onto a single chip in an effort to reduce overall cost and space and to improve system performance. This requires the scaling of CMOS technology. The reliability and density factors associated with technology scaling demand for downsized supply voltages. This trend of continuous reduction of the supply voltage poses serious challenges to the analog designers. To circumvent this conflict instead of using costly CMOS technologies with lower thresholds, it is desirable to use low voltage circuit techniques that are compatible with standard CMOS processes. In the last few decades the current-mode processing has emerged as an alternative design technique. Ever shrinking feature size of devices on ICs and consequential reduction of power supply voltage can be handled by operating in the current domain, as current mode circuits are designed for lower voltage swings. While fundamentally any design techniques is limited by device characteristics, there may be specific applications where current-mode circuits provide one or more of the following advantages: higher bandwidth, better signal linearity, higher slew rates, lower power consumption, and better accuracy. Additionally, current-mode circuits are often less complex than the voltage-mode circuits, which may lead to significant chip area savings. Emergence of various current-mode analog building blocks is outcome of the considerable progress in current-mode analog signal processing. Operational trans-resistance amplifier (OTRA) among those is of relatively recent origin.

Keywords : CFOA, OTRA,CC,

CHAPTER I

INTRODUCTION

1.1 Introduction

This dissertation presents a study on OTRA its internal structure and its characteristic equations.OTRA is one of the current mode active building block with current as input and voltage as output.

The low-voltage and low-power mixed mode circuit design has gained importance with the advent of the portable electronic and mobile communication systems. More and more mixed mode circuit blocks, are being integrated onto a single chip in an effort to reduce overall cost and space and to improve system performances [1]. This require the scaling of CMOS technology. The reliability and density factors associated with technology scaling demand for downsized supply voltages. This trend of continuous reduction of the supply voltage poses serious challenges to the analog designers. To circumvent this conflict instead of using costly CMOS technologies with lower thresholds, it is desirable to use low voltage circuit techniques that are compatible with standard CMOS processes.

In last few decades the current-mode processing has emerged as an alternative design technique. Ever shrinking feature size of devices on ICs and consequential reduction of power supply voltage can be handled by operating in the current domain, as current mode circuits are designed for lower voltage swings [2]. While fundamentally any design techniques is limited by device characteristics there may be specific applications where current-mode circuits provide one or more of the following advantages higher bandwidth, better signal linearity, higher slew rates, lower power consumption, and better accuracy. Additionally, current-mode circuits are often less complex than the voltage-mode circuits, which may lead to significant chip area savings.

1.2 Dissertation Outline

In this dissertation, the first chapter covers the introduction of OTRA as a building block in various applications. In second chapter various literature has been presented which are available and various applications are discussed in brief. The third chapter covers implementation of OTRA by CMOS technology and various characteristics of OTRA and some basic circuits of OTRA like summer, adder etc. In the fourth chapter voltage mode filters are obtained and their Pspice simulations are obtained. In the sixth chapter current mode filter has been implemented using OTRA and simulated in Pspice. In the sixth chapter leap frog low pass filter has been implemented and simulated.

CHAPTER II

OPERATIONAL TRANSRESISTANCE AMPLIFIER

2.1 Introduction

From the very beginning op-amp is an integral part of signal processing and electronics circuits. It can be used as a voltage mode (output is voltage) device for different applications. But at high frequencies the performance specifications of these circuits gets detoriated due to constant gain bandwidth product and slow slew rate op op-amps. The limitations of Op-amp has led to the development of current-mode (CM) signal processing. Current is used instead of voltage in current mode(CM) device throughout the circuit or through a specific area. One can achieve a considerable improvement in system performance like bandwidth, signal linearity, slew rate and power consumption using CM techniques [3]. Consequently, CM signal processing has progressed considerably in past few decades and resulted in emergence of various CM analog building blocks and OTRA is of recent origin [4]. OTRA is a high gain current input and output voltage device. The input and output terminals of OTRA [1] has low impedences thus results in the circuit which are insensitive to the stray capacitances thus making it suitable for high frequency applications.

It is necessary to convert the input and output signals of current-mode circuits to voltage by trans-conductors and trans-resistors to maintain the compatibility with existing voltage processing circuits. This thus has a disadvantage of increasing chip area and power dissipation. However, circuits utilizing OTRA as the dynamic component advantage from the present preparing abilities at the information terminals, and can straight forwardly drive the current VM signal preparing circuits accordingly killing the prerequisite of extra hardware and related force utilization, at the yield.

In this chapter OTRA has been dealt with detail. The OTRA realized here with MOSFET.

2.2 The ideal OTRA

Circuit symbol representation of an OTRA [1] is shown in fig 2.1(a). It has a two input terminal and one output terminal. An ideal OTRA amplifies the difference of current between the positive terminal and negative terminal and multiplies it by Rm i.e gain and results into the output voltage at the output terminal. Both the input terminal voltage of an OTRA is zero. The output voltage of an OTRA is independent of the load connected to it or should be independent of the load current. The OTRA characteristic equation is given by equation (2.1) and the equivalent circuit is represented in fig 2.1(b). For an ideal OTRA the trans-resistance gain (Rm) approaches infinity thus making the input currents to be equal.

$$\begin{bmatrix} V_p \\ V_n \\ V_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ I_o \end{bmatrix} \qquad (2.1)$$

The above idealized condition does not apply in practice but the idealized condition can be used to simplify mathematical analysis of OTRA circuits.

In spite of the fact that the above glorified conditions cannot be acknowledged by and yet the utilization of such a perfect OTRA model rearranges the numerical investigation of OTRA circuits. OTRA circuits are made to approximate the glorified idealized characteristics. The proportionate circuit model of a OTRA is presented in Fig. 2.2 where Rp and Rn represents to terminal resistances of p and n ports separately.

If we are using OTRA in open loop configuration then due to its high gain i.e ideally infinity output voltage saturates either at positive or negative saturation level. Thus it has a limited application. So OTRA is used in negative feedback configuration which forces the output in linear region instead of saturation region. As OTRA is a current fed voltage source it is used as a shunt-shunt feedback configuration as a result the feedback network and amplifier are placed in parallel [5]. A parallel setup is appropriate for low voltage operations as it minimizes

stacking of transistors along these lines giving more make a bee line for sign swing. Additionally, utilizing OTRA in current feedback techniques leads to bandwidth which is almost independent of closed loop gain.

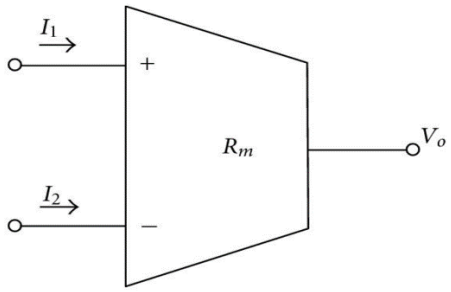


Fig 2.1(a) Symbol of OTRA [1]

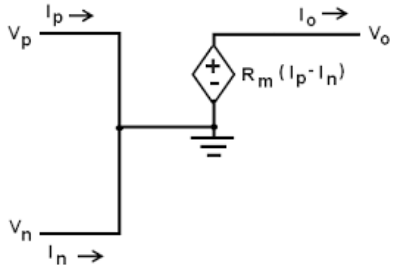


Fig 2.1(b) Eqivalent circuit of OTRA [1]

2.3 Non Ideal model of OTRA

For an ideal OTRA the trans-resistance gain R_m should be ideally infinity but in practical its value is finite and thus its effect must be taken into consideration [2].

Considering the single-pole model $R_m$is given as

$$R_m(s) = \left(\frac{R_0}{1+{}^{s}/_{w_0}}\right) \qquad (2.2)$$

Where, R_0 =DC open loop transresisance gain.

For the application of high frequency range the equation changes to

$$R_m(s) \approx \frac{R_0}{s/w_0} = \frac{1}{s/R_0 w_0} = \frac{1}{sc_p} \qquad (2.3)$$

Thus, $C_p = \frac{1}{R_0 w_0}$

C_p is called parasitic capacitance of OTRA.

2.4 Implementation of OTRA

In this section method of implementation of OTRA is obtained based on the literature available.

According to existing literature OTRA can be implemented by two ways,

(i) Using IC AD844(CFOA) [2].

(ii) Using integrated circuit using MOSFET [6].

2.4.1 Realization of OTRA using CFOA

CFOAs are commercially called as IC AD844.Symbolically it is represented as shown in fig.2.2 and the terminal equations of CFOA [2] is characterized by

$$V_x = V_y;\ I_y = 0\ ; I_z = I_x;\ V_w = V_Z \qquad (2.4)$$

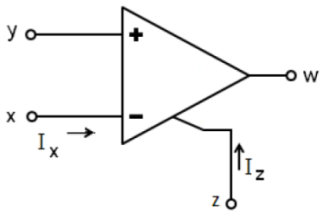


Fig.2.2 Symbol of CFOA

The OTRA can be realized using two CFOA(AD844) [2] ICs as shown below in the fig.2.3 below and from the terminal characteristics of CFOA [7] various currents can be calculated as

$$I_{z1} = I_p \tag{2.5}$$

$$I_{x2} = I_n - I_{z1} \tag{2.6}$$

$$I_{Z2} = I_{x2} \tag{2.7}$$

Using equations (2.5) and (2.6) the current through Z_2 *is given by*

$$I_{z2} = I_n - I_p \tag{2.8}$$

The voltages at different terminal is given by equation (2.9)

$$V_p = V_{1-} = V_{1+} = 0 \tag{2.9}$$

$$V_0 = V_{z2} = -I_{z2}R_{z2} = (I_p - I_n)R_{z2} \tag{2.10}$$

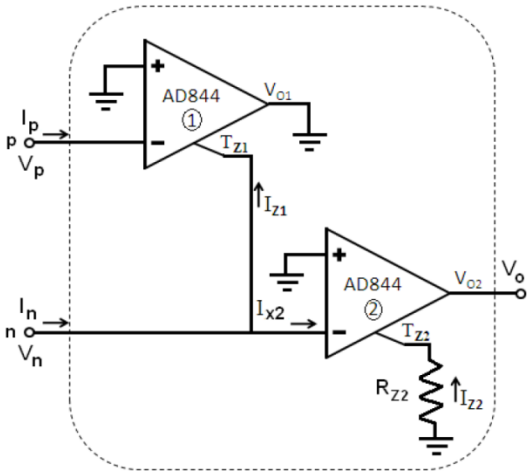


Fig.2.3 CFOA(AD844) based OTRA [8]

Ideally terminal x provides infinite input resistance and thus at the terminal z.But the input resistance at x terminal of AD844 is around 50Ω and at the z terminal is around 3MΩ.

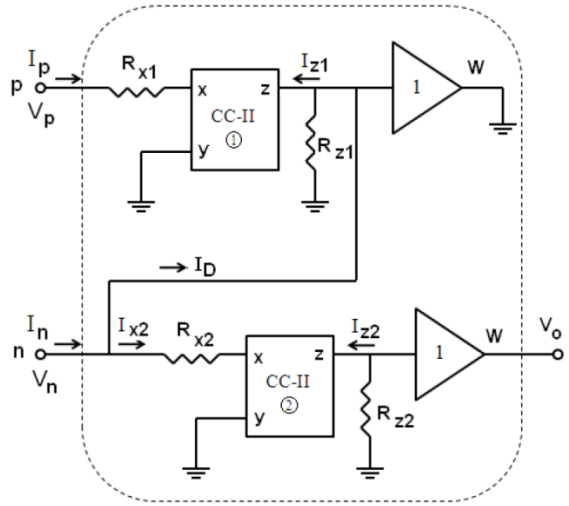


Fig.2.4 Equivalent circuit of OTRA constructed with AD844 [8].

To know the effect of R_x andR_z i.e the parasitic resistances the CFOAs are replaced with the current conveyers which are having finite input resistances (R_x) and finite z terminal resistance(R_z) as shown in the fig.2.3 and the analysis of the equivalent circuit model with parasitic for the case of non-ideality is presented in fig.2.4 and the computation of various currents are done as below

$I_{z1}=I_p$ (2.12)

$$I_D = I_{z1}\left(\frac{R_{z1}}{R_{x2}+R_{z1}}\right) \quad (2.13)$$

$I_{x2}=I_n - I_D$ (2.14)

$$I_{z2} = I_{x2} \quad (2.15)$$

Ideally I_D should be equal to I_{z1}, which can be valid only when $R_{z1} \gg R_{x2}$ which is the case for AD844. Also it can be concluded that the input terminals are virtually grounded only when the external resistance connected at the input terminal of the OTRA is much larger than R_x. If the above conditions are satisfied then only the OTRA constructed with AD844 closely follows the ideal OTRA. The output equation for the above OTRA can be written as

$$V_0 = (I_p - I_n)R_{z2} \quad (2.16)$$

Where R_{z2} represents the trans-resistance gain of the OTRA.

2.4.2 Integrable model of OTRA

Different types of integrated circuit implementations of OTRA [1], [6], [8] are available in literature and are briefly described in this section. The OTRA implementation consists of a differential current controlled current source followed by a voltage buffer. The OTRA proposed is based on cascaded connection of the modified differential current conveyor and a common source amplifier [3]. The MDCC [9] facilitates the current differencing operation and the common source amplifier facilitates the high gain stage. The OTRA consists of a low voltage cascode current mirror [8] along with a low voltage cascode load as the core of the circuit, consisting of common source amplifiers gain boost stage and level shifters followed by common source output stage. The OTRA structure is similar [1] to Salama model but uses less

number of current mirrors than that [8]. This reduces the transistor mirror mismatch and also increases the frequency capabilities of the circuit. Due to smaller number of transistors the power dissipation gets reduced. The CMOS OTRA [8] realization uses same input stage as in [4] while a differential gain stage is used instead of the single common source amplifier. This differential stage decreases the DC offset current and increases the DC open loop gain (R_m). Another differential OTRA structure is also proposed in [10]. It consists of two symmetrically placed basic input cells having four transistors each. Each cell forms two Class AB current mirror connections. This basic input unit is followed up by four similar basic cells to reduce the process variation effects. Gain is provided by using three stages of differential amplifier. The non-buffered, dual differential outputs are buffered through unity gain configurations which are designed using CMOS op-amps [4]. This structure is complete differential design.

2.5 Implementation of OTRA using CMOS technology

Here we will discuss the OTRA implementation using CMOS technology and verify the function of all the circuit structures. The CMOS based OTRA [1] structure is shown in fig.2.4. The circuit operation is based on the fact that all the MOSFETs ($M_1 - M_{14}$) operates in the saturation region and the transistors groups $(M_1 - M_3), (M_5 - M_6)(M_8 - M_{11})\ and\ (M_{12} - M_{13})$ are perfectly matched. Transistors ($M_8 - M_{11}$) forms the current mirrors where M_8 sets the reference current I_B which is repeated by M_9–M_{11} which forces equal currents in the transistors $M_1, M_2\ and\ M_3$ .This makes equal voltages of gate to source voltage and consequently forces the two input terminal to be equal to zero(virtually grounded).The current mirrors formed by the transistor pairs M_{10}-M_{11} and $M_{12} - M_{13}$provide the current differencing operation, thus developing gate to source voltage for which is connected as common source amplifier and provides the high gain.

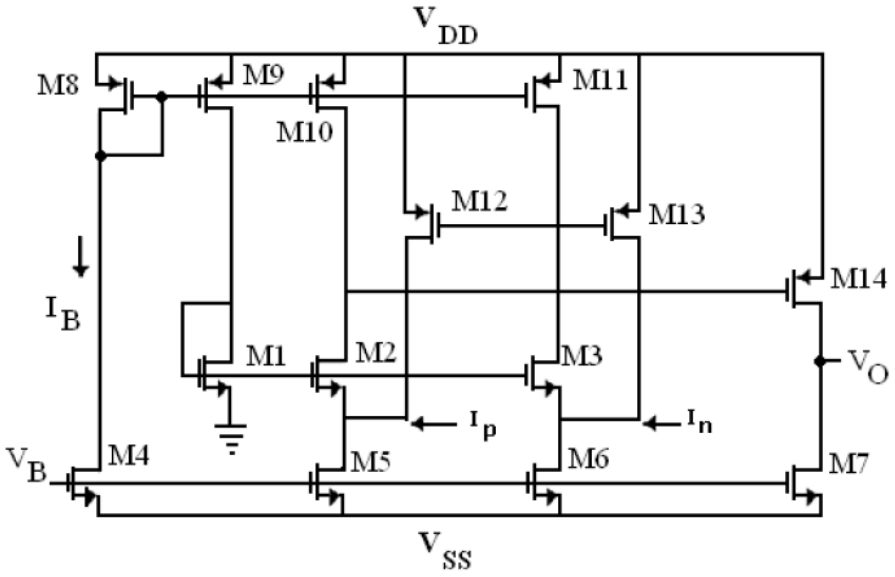


Fig.2.5 CMOS realization of OTRA [1]

The DC characteristic and gain characteristic for the OTRA implemented is obtained and shown in fig.2.5.1.

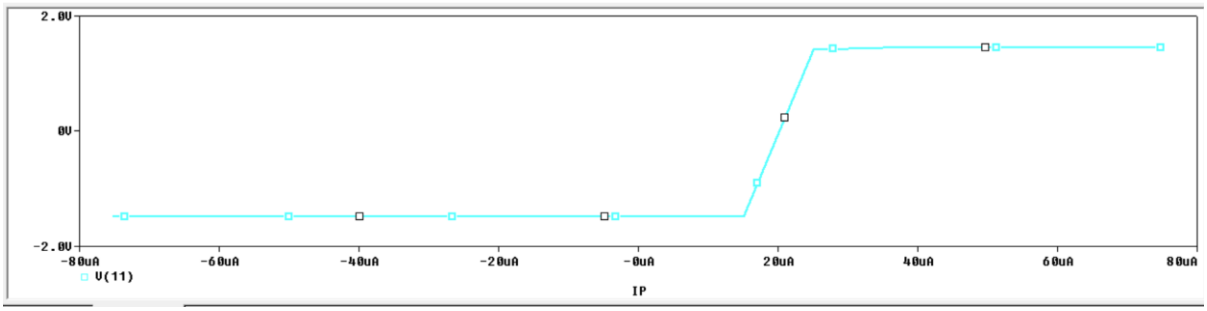


Fig.2.5.1 DC characteristic of OTRA with I_N = 20nA

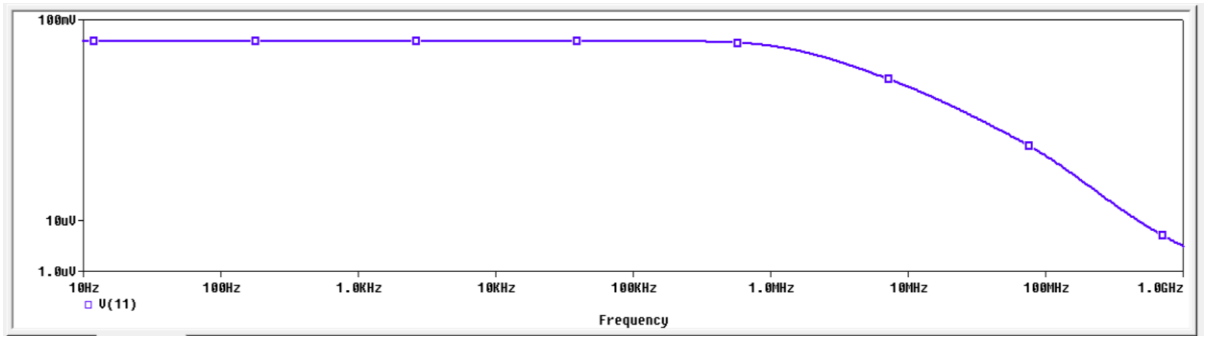


Fig.2.5.2 AC characteristic of OTRA

The supply voltage V_{DD} and V_{SS} are taken as 1.5V and bias voltage V_B is taken as -0.5V.

2.6 OTRA characterization

The SPICE simulation has been performed using 0.5µm, CMOS process parameters provided by MOSIS (AGILENT) as listed in Table 2.1. Supply voltages for simulations are kept as ± 1.5 V. Aspect ratios used for different transistors are same as in [6] and are given in Table 2.2.

Table 2.1 Device Model parameters.

Device Type	Model parameter
NMOS	LEVEL=2 PHI=0.6000 TOX=4.3500E-08 XJ=0.200000U TPG=1 + VTO=0.8756 DELTA=8.5650E+00 LD=2.3950E-07 KP=4.5494E-05 + UO=573.1 UEXP=1.5920E-01 UCRIT=5.9160E+04 RSH=1.0310E+01 + GAMMA=0.4179 NSUB=3.3160E+15 NFS=8.1800E+12 VMAX=6.0280E+04 + LAMBDA=2.9330E-02 CGDO=2.8518E-10 CGSO=2.8518E-10 CGBO=4.0921E-10 + CJ=1.0375E-04 MJ=0.6604 CJSW=2.1694E-10 MJSW=0.178543 PB=0.800000

PMOS	LEVEL=2 PHI=0.6000 TOX=4.3500E-08 XJ=0.200000U TPG=1 + VTO=0.8756 DELTA=8.5650E+00 LD=2.3950E-07 KP=4.5494E-05 + UO=573.1 UEXP=1.5920E-01 UCRIT=5.9160E+04 RSH=1.0310E+01 + GAMMA=0.4179 NSUB=3.3160E+15 NFS=8.1800E+12 VMAX=6.0280E+04 + LAMBDA=2.9330E-02 CGDO=2.8518E-10 CGSO=2.8518E-10 CGBO=4.0921E-10 + CJ=1.0375E-04 MJ=0.6604 CJSW=2.1694E-10 MJSW=0.178543 PB=0.800000

Table 2.2 Aspect ratio(W/L) of transistors in OTRA circuit

Transistors	W(um)/L(um)
$M_1 - M_3$	100/2.5
M_4	10/2.5
M_5, M_6	30/2.5
M_7	10/2.5
$M_8 - M_{11}$	50/2.5
M_{12}, M_{13}	100/2.5
M_{14}	50/2.5

The DC transfer characteristic of the above OTRA circuit has been obtained using PSPICE simulation as shown in fig.2.5 with the input differential current range from -50µA to 50µA. AC characteristic obtained from PSPICE is plotted in fig.2.6.

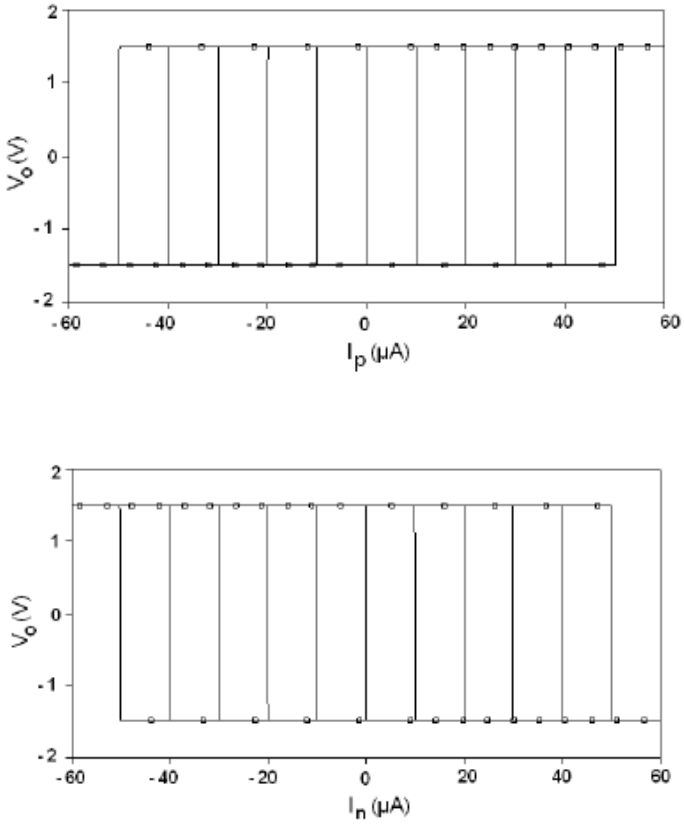


Fig.2.6 DC transfer characteristic

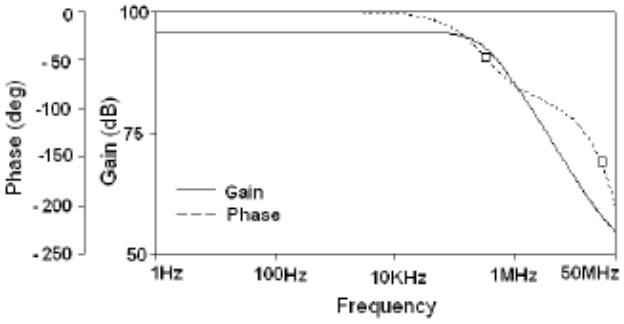


Fig.2.7 Frequency response of open loop trans-resistance gain

As from the observation in fig.2.6 the frequency response is decreasing with the increase in frequency this is due to the presence of parasitic impedances which becomes dominant at higher frequency range. Different parameters obtained from PSPICE simulation is tabled in table 2.3.

Table 2.3 OTRA parameters

Parameters	Results
Input current dynamic range	-50 to 50μA
Input resistances Rp, Rn	15Ω
DC open loop trans-resistance gain	99.2dBΩ
Gain bandwidth product	23.43GHzΩ

2.7 Basic circuit applications

2.7.1 Inverting Voltage Amplifier

An inverting mode amplifier is shown in the fig.2.8. It consists an OTRA and two resistors connected from output to the negative terminal of the OTRA making it negative feedback. The current at the terminal can be calculated as

$$i_n = \frac{v_n}{R_1} + \frac{V_0}{R_2} \tag{2.17}$$

The current at the positive terminal can be given as

$$i_p = 0$$

Assume that the OTRA is idea and the overall voltage gain can be computed by solving the currents at positive and negative terminal

$$\frac{V_{in}}{R_1} + \frac{V_0}{R_2} = 0 \tag{2.18}$$

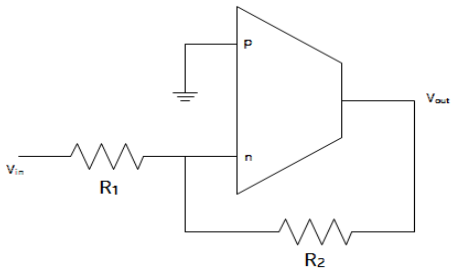


Fig.2.8 Inverting mode OTRA amplifier

Thus from the above equations closed loop inverting gain can be computed as

$$\frac{v_0}{v_{in}} = -\frac{R_2}{R_1} \tag{2.19}$$

2.7.2 Non inverting voltage amplifier

A non-inverting mode amplifier consisting of an OTRA with two resistors R_1 and R_2 as shown in the figure

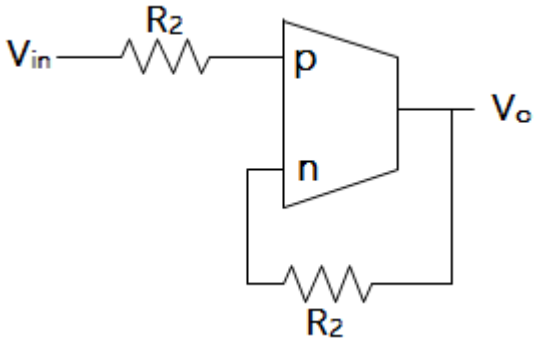


Fig.2.9 Non inverting mode OTRA implementation

Current at both the terminal p and n can be calculated as

$$i_n = \frac{v_0}{R_2} \tag{2.20}$$

$$i_p = \frac{v_{in}}{R_1} \tag{2.21}$$

Considering the OTRA is ideal voltage gain of the given amplifier can be calculated as

$$\frac{v_{in}}{R_1} = \frac{v_O}{R_2} \tag{2.22}$$

This results in the voltage gain of

$$\frac{v_o}{v_{in}} = \frac{R_2}{R_1} \tag{2.23}$$

2.7.3 OTRA as a summer

A summer amplifier can be made through OTRA as shown in the fig.2.10. The circuit uses the single OTRA with a feedback resistor R_F and other resistors ($R_1 to\ R_N$) by which the input signals are applied for which summing has to be done.

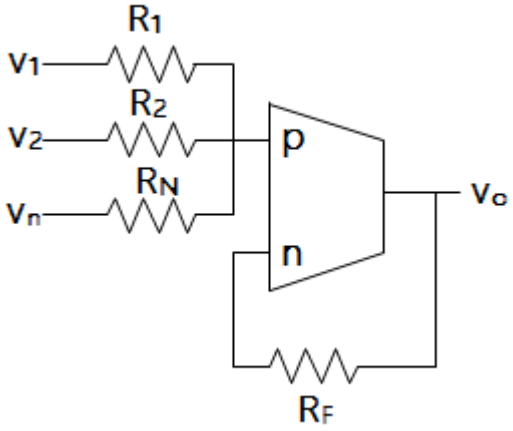


Fig.2.10 The summing amplifier

Equating the currents at non inverting terminal and the inverting terminal, the voltage at the output can be calculated as

$$v_o = \frac{R_F}{R_1} v_1 + \frac{R_F}{R_2} V_2 + \cdots + \frac{R_F}{R_N} v_N \tag{2.24}$$

If $R_F = R_1 = R_2 = R_N$

$$v_o = v_1 + v_2 + \cdots + v_n \tag{2.25}$$

2.7.4 OTRA as a difference amplifier

Some applications require the output as a function of differential input voltages. Circuit diagram of difference amplifier using OTRA is shown in fig.2.11.

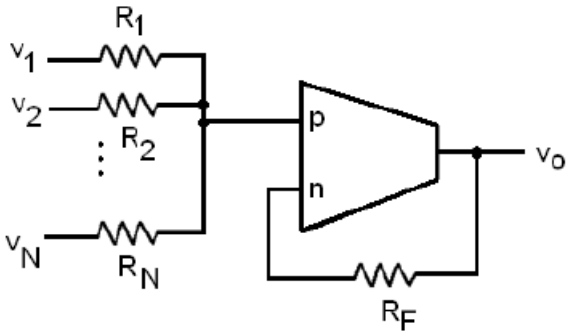


Fig.2.11 OTRA as difference amplifier

Assuming the OTRA is ideal then the output voltage for the circuit isgiven by

$$v_o = \frac{R_F}{R_1} v_1 - \frac{R_F}{R_2} v_2 \tag{2.26}$$

If $R_1 = R_2 = R$ then the output equation becomes

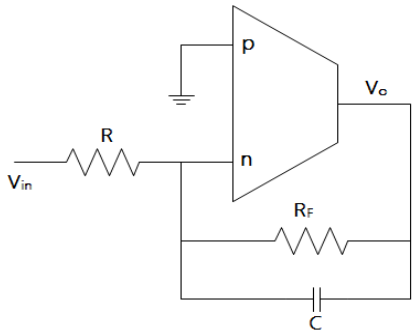
$$v_0 = \frac{R_F}{R}(v_1 - v_2) \tag{2.27}$$

Also if $R_1 = R_2 = R_F$ then the output voltage equation changes to

$$v_o = (v_1 - v_2) \tag{2.28}$$

2.7.5 Lossy Integrator using OTRA

OTRA can be used to implement inverting and non-inverting lossy integrator as shown below. Fig.2.12 represents inverting lossy integrator and fig.2.13 represents non inverting lossy integrator.



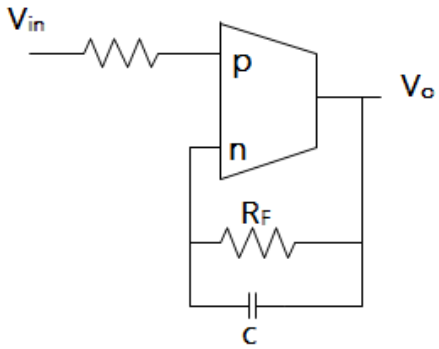


Fig.2.12 Inverting lossy integrator **Fig.2.13** Non inverting lossy integrator

Using the terminal equations of OTRA and applying KCL and KVL the transfer function is given by

$$\frac{v_o}{v_{in}} = -\frac{(R_F/R)}{1+SCR} \tag{2.29}$$

Where K=$\frac{R_F}{R}$

Applying input at the p terminal the transfer function can be obtained as

$$\frac{v_o}{v_{in}} = \frac{R_F/R}{1+sCR} \tag{2.30}$$

Where K=R_F/R represents the DC gain.

2.8 Applications of OTRA

Emergence of various current-mode analog building blocks is outcome of the considerable progress in current-mode analog signal processing. Operational transresistance amplifier (OTRA) among those is of relatively recent origin.

It is a high gain current input voltage output device which provides advantages of current mode design techniques and can readily be used for voltage-mode applications.

A wide variety of OTRA based system applications, ranging from filters, oscillators, multivibrators through general analog interfacing, are available in literature [2]. In this research work design and development of signal generating and processing circuits using OTRA as building block is presented. The prime concern of the design is to provide better quality response, introduce versatility and modularity, and to develop circuits which could be better implemented in integrated circuit form.

.

2.9 Conclusion

In the present chapter OTRA characteristics and its terminal equations are presented. Non-idealities of OTRA has been taken into consideration which will help in the performance evaluation of OTRA circuits and a summary on the literature review is presented. The OTRA internal circuit is obtained using CMOS technology [1] and simulated on PSPICE. Some basic circuits of OTRA is also realized which will be helpful for OTRA circuits.

Chapter III

Literature Review

3.1 Introduction

Now-a-days OTRA are being implemented in many signal processing circuits due to the advantage of internally grounded impedance, high slew rate and large bandwidth than op-amp. Some of its applications which are present in literatures will be discussed in this chapter. Now a days, scientists are focusing more on current mode device than voltage mode device due to advantage of current mode devices. The OTRA [1] used in all the circuits presented here are implemented using CMOS technology as presented in chapter 2.

3.2 Filters

An all pass filter [11] is a filter which passes all the signal through it but modifies the phase of the signal according to the frequency of the signal. Here a new voltage mode configuration has been proposed which uses a single operational trans-resistance amplifier and then a first order all pass filter is realized. The proposed filter [11] is insensitive to the parasitic impedances due to the internally grounded input terminals. Low output impedance at the output enables it to be used in cascade without the use of buffers.

In [13] a voltage mode band pass filter is implemented using OTRA in high frequency domain is simulated using Cadence Virtuoso UMC 180 nm technology. The CMOS OTRA based on the cascaded connection of modified differential current conveyer (MDCC) [9] and a CS amplifier. All the transistors are operated in saturation region. The center frequency of the designed band pass filter is which works actually in high frequency domain.

A fourth order filter structure [14] has been implemented using OTRA. OTRA [1] based second order low pass filter and high pass filter is verified and fourth order band pass and notch filter topologies are also obtained.

The resulting filters are simulated by 0.18μm CMOS process through Orcad Unison Suite.

High order linear transformation MOSFET C filters [15] using operational transresistance amplifiers (OTRAs) is simulated. The systematic method is developed to realize LT OTRA-based filters efficiently. Based on the proposed design procedures, we can synthesize high order filters with OTRAs along with MOSFET [16] resistor circuits (MRCs) and capacitors. A third-order Chebychev low pass filter is demonstrated.

High-order OTRA-based LT MOSFET-C [17] filters with reduced parasitic capacitance effects are presented. Signal processing circuits implemented employing OTRAs have almost constant bandwidths because of the use of current-feedback configurations. The nth-order Chebychev filter can be realized by using n OTRAs along with n capacitors and n+1 MRCs. Proposed filter has the following merits: efficient design procedures, simple design equations and systematic circuit architectures. The proposed filter is suitable for integration. Furthermore, it can be extended to higher-order filters.

The research paper [18] introduces a new voltage mode first order multifunction filter using three operational transresistance amplifier (OTRA) and some passive components. A single topology is used for the implementation of first order low pass(LP), high pass(HP) and all pass(AP) filter functions. One can tap all the three filter functions simultaneously form the proposed topology. It is simulated using PSPICE with 0.5μm CMOS process parameters provided by MOSIS (AGILENT).

All the passive components of the topology are grounded as the inputs of an OTRA are virtually grounded. Hence effect of parasitic elements are minimised and also suitable for IC design.

The %THD of the output responses with respect to the input reveals that %THD is very low even for a comparatively high input signal.

In [23] shadow filter configuration is implemented using operational transresistance amplifier (OTRA). In shadow filters an external amplifier is added in the feed-back loop of the basic filter and by controlling the gain of this amplifier the characteristics of the resulting filter can be tuned. Depending upon the value of A the filter characteristics can be varied from very low to very high values.

An another method of electronic tuning of filter parameters has been introduced in a recently proposed family of second-order filters [24] termed as shadow filters. In these filters an external amplifier is added in the feedback loop and the characteristics of the resulting filter can then be tuned by controlling the gain (A) of this amplifier. Depending upon the value of A the filter characteristics can be varied theoretically from zero to infinity[25].

In [27] a multi input single output (MISO) third order voltage mode (VM) universal filter using only one operational transresistance amplifier (OTRA) is presented. The proposed circuit realizes low pass, high pass, all pass, bandpass and notch responses from the same topology.

The performance of the proposed universal filter is evaluated with CMOS implementation of OTRA as given in [26], DC power supply voltages V_{DD} =- V_{SS} =1.5 V and bias voltage V_B=0.5V. The simulations are performed using based on 0.5μm MOSIS (AGILENT) CMOS technology parameters.

This research article contains two new voltage-mode third order asymmetric band pass filter structures [1], [29], [30] using single operational transresistance amplifier (OTRA) and passive components.

3.3 Oscillator

In [31], single-op-amp sinusoidal oscillators are synthesized using genetic algorithms. The motivation is to evolve new topologies of oscillators using different active building blocks (ABBs) and automate the study of their properties. A new fitness evaluation scheme by analyzing transfer function of the circuits is used and a learning scheme loosely inspired from Lamarckian search is also suggested. A new problem specific crossover operator is tested and a comparative study of different crossover operators is done. On comparison of results of the GA with existing results, it was found that the GA rediscovered all the twelve canonic single op-amp based SFOs.

In this paper [32] Operational Trans-Resistance Amplifier (OTRA) based multiphase sinusoidal oscillator circuits are presented. The first circuit produces n odd phase oscillations of equal amplitudes and equally spaced in phase. The second circuit is capable of producing n odd or even phase oscillations equally spaced in phase. An alternative approach is discussed in the third circuit, which utilizes a single phase tunable oscillator circuit which is used to inject signals into a phase shifter circuit [33-34]. An automatic control (AGC) circuit has been implemented for the second and third circuit. The circuits are simple to realize and have a low component count.

Two new topologies of OTRA based sinusoidal oscillators [35] are presented. The first topology makes use of lossless integrators. whereas the second topology is designed using a second order all pass section. The proposed topologies can be made fully integrated by implementing the resistors using matched transistors operating in linear region, which facilitates electronic tuning of oscillation frequency [36]. The total harmonic distortion (THD) for both the designs is found to be quite low.

The first topology makes use of lossless integrators, whereas the second topology is designed using a second order all pass section [37].

Quadrature oscillator [38] based on the operational transresistance amplifier (OTRA) is presented in this paper. The proposed quadrature circuit uses two OTRAs as main active building blocks and a few external passive components to generate the oscillations. The circuit provides independent control over the condition of oscillation and frequency of oscillation. A prototype circuit is implemented on a laboratory breadboard [39] using commercially available current feedback operational amplifier ICs (AD844 AN) and passive components are connected externally and tested for waveform generation.

This paper [41] presents a new third-order quadrature oscillator using operational transresistance amplifiers as active elements. The proposed circuit provides high precision of the frequency of oscillation. The frequency of oscillation can be controlled using a single passive component and the condition of oscillation can be controlled orthogonally by setting the circuit components [42]. Also two quadrature voltage output terminals possess low

impedance level which can be directly connected to the load. Simulation results verifying the theoretical analysis are also included.

This paper [43] illustrates two sinusoidal oscillators based on single Operational Transresistance Amplifier (OTRA). The proposed circuits require a single OTRA and a few passive components to generate the oscillations. The proposed circuit's frequency of oscillation and condition of oscillation are given. The proposed circuits have been examined using Cadence 180 nm CMOS model parameters. These circuits have been constructed using commercially available current feedback amplifier (AD844 AN) [2] and later on passive components were connected externally and tested for waveform generation. The results obtained demonstrate excellent agreement with theoretical values.

These circuits use only one OTRA and few passive components, the proposed circuits are simpler than the conventional waveform generators. The proposed circuits require two capacitors and three resistors to generate the oscillations.

3.4 Inductor

This paper [44] deals with an operational transresistance amplifier (OTRA) based grounded CMOS active inductor architecture and implementation of bandpass filter in the high frequency domain. The whole configuration is simulated using Cadence Virtuoso UMC 180 nm Technology.

In this paper OTRA based grounded active inductor has been simulated with BPF implementation. There is much other process to test the active inductor like linearity checking of impedance vs frequency plot, phase change across inductor, etc. One can also choose IP3, noise, PSS analysis for complete circuit realization. One can change the bandwidth by modifying R and C by using poly resistors and poly capacitor to a large extent of value.

This paper [45] deals with Inductance simulator which find numerous applications in the field of electronics, instrumentation, measurement and signal processing. The negative inductance [28] finds some special applications in areas such as generation for chaotic

oscillator, cancellation of parasitic inductance, impedance matching, and to minimize reflection at the antenna so that a better radiation patterns is obtained. Unfortunately, negative inductance is not physically available. However, it may be designed using active network. Already a number of inductor simulators are available using an analog building blocks namely operational transresistance amplifier (OTRA).

It is also found that the non-linearity error may be eliminated at high frequency by passive compensation.

3.5 Multivibrator

Three non retriggerable current-mode monostable multivibrators [46] constructed of one operational transresistance amplifier (OTRA) and a few passive elements are presented in this brief. Two of these circuits are operated respectively under positive and negative triggering modes. However, the recovery time cannot be adjusted once the pulse width is decided. The third topology, which can work in either triggering mode, features a tunable recovery time. The proposed current-mode monostable are simpler compared to their counterparts composed of operational amplifiers. The circuit operations are described in detail. Experimental results are in good agreement with the theoretical analysis**.**

This paper [47] presents a new Analog Timer circuit which is used to design Astable and Monostable multivibrators. The circuit employs comparators designed using OTRA and flip flops implemented using Nand gates. Astable multivibrator designed using this Timer circuit generates a periodic waveform of variable time period and duty cycle. Monostable multivibrator uses a current trigger pulse to produce the output. The proposed circuits are insensitive to parasitic capacitances and resistances due to internally grounded input terminals of OTRA and can operate at very low power supply voltage. The performance of the proposed Timer circuits is verified through PSPICE simulation using 0.5 µm CMOS process parameters provided by MOSIS (AGILENT).

Chapter IV

IMPLEMENTATION OF OTRA AS A VOLTAGE MODE FILTER

4.1 Introduction

In this thesis OTRA has been implemented in various current mode(CM) and voltage mode (VM) filters. OTRA has been implemented using CMOS technology and its various characteristics is presented in chapter 2.

4.2 Implementation of OTRA in voltage mode filter

Most of electronic circuits process data than energy, so they act as data converters. For some reason, the voltage is used more frequently than the current to carry the data (analog or digital); so, the most electronic circuits act as voltage-to-voltage converters.

4.2.1 Voltage mode low pass filter

A voltage mode low pass filter [2] using OTRA has been implemented in the fig.4.6 as shown. Different values of Resistance, Capacitance and Inductance are connected and circuit analysis is done as below and transfer function is obtained.

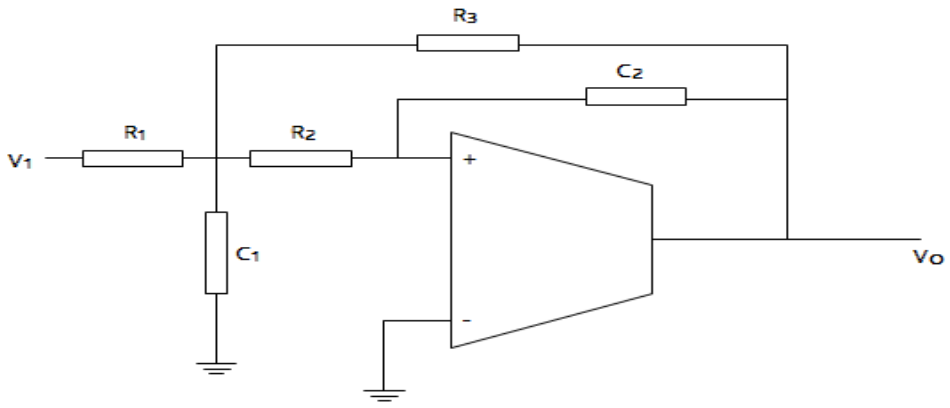


Fig.4.6 Voltage mode low pass filter [8]

Assuming the OTRA to be ideal its terminal equations to be written as

$$V_p = 0 \tag{4.1}$$

$$V_n = 0 \tag{4.2}$$

As the gain (R_m) of the transresistance amplifier is ideally infinity, this concludes

$$i_p = i_n = 0 \tag{4.3}$$

Applying KCL

$$\frac{v_1 - v_i}{R_1} + \frac{v_1 - 0}{1/sc_1} + \frac{v_1 - v_o}{R_3} + \frac{v_1 - 0}{R_2} = 0 \tag{4.4}$$

Applying KCL

$$\frac{0 - v_1}{R_2} + \frac{0 - v_0}{1/sc_2} = 0 \tag{4.5}$$

Solving equations

$$-\frac{v_1}{R_2} = v_o s c_2 \tag{4.6}$$

$$v_1 = -R_2 c_2 s \tag{4.7}$$

$$\frac{v_1}{R_1} + v_1 s c_1 + \frac{v_1}{R_3} + \frac{v_1}{R_2} = \frac{v_i}{R_1} + \frac{v_0}{R_3} \tag{4.8}$$

Putting the value of v_1 in equation

$$-R_2 s c_2 v_o \left(\frac{1}{R_1} + s c_1 + \frac{1}{R_3} + \frac{1}{R_1}\right) = \frac{v_i}{R_1} + \frac{v_o}{R_3} \tag{4.9}$$

Solving the equations we get the transfer function as

$$\frac{v_o}{v_i} = \frac{-{}^{G_1 G_2}/_{c_1 c_2}}{s^2 + s\left(\frac{G_1 G_2 G_3}{c_1}\right) + \left(\frac{G_1 G_2}{c_1 c_2}\right)} \tag{4.10}$$

Where,

$$G_1 = \frac{1}{R_1}, G_2 = \frac{1}{R_2}, \; G_3 = \frac{1}{R_3}$$

From the equation it is clear that

Resonance frequency $w_o = \sqrt{\frac{G_1 G_2}{c_1 c_2}}$

Quality factor $Q_o = \frac{\sqrt{G_1 G_2 G_3}}{\sqrt{c_2(G_1+G_2+G_3)}}$

Filter gain $H_O = -\frac{G_1}{G_3}$

The above filter is simulated using C_1 = 450pF, C_2 =100pF, R_1= R_2 = R_3 =0.5KΩ and the resonant angular frequency is found to be f_o=1.5Mhz. Quality factor Q_o comes to be 115.47.The value of filter gain comes to be -1. Simulation results of the filter is shown in fig.4.6.1. Input and output of the filter is shown with gain characteristic in fig.4.6.2.

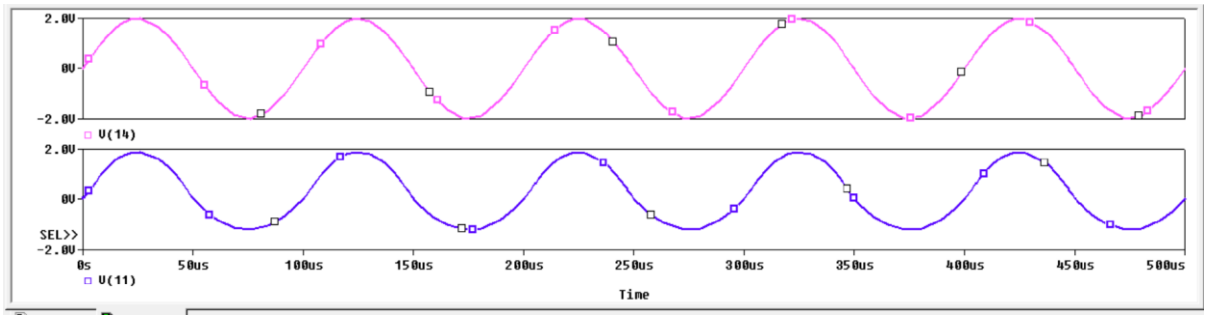


Fig.4.6.1 Input and output of low pass filter

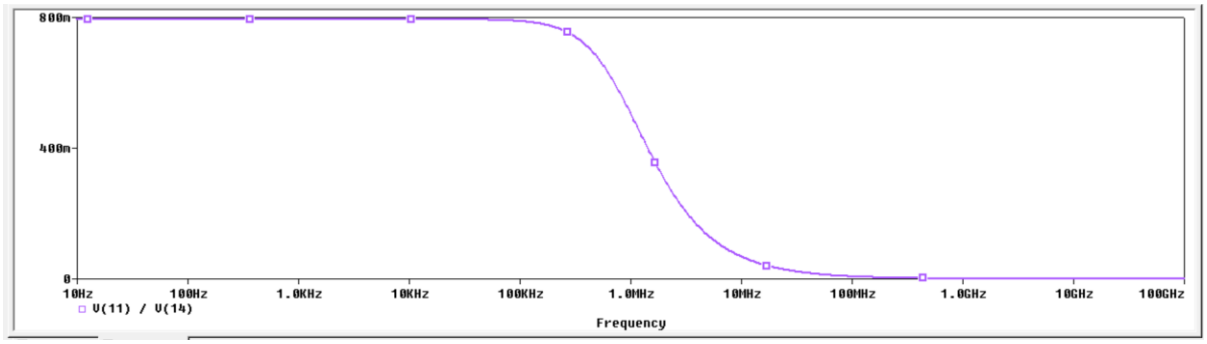


Fig.4.6.2 Gain characteristic of low pass filter

4.2.2 High Pass filter using single OTRA

A voltage mode high pass filter [6] using OTRA [1] has been implemented in the fig.4.7 as shown. Different values of Resistance, Capacitance and Inductance are connected and circuit analysis is done as below and transfer function is obtained.

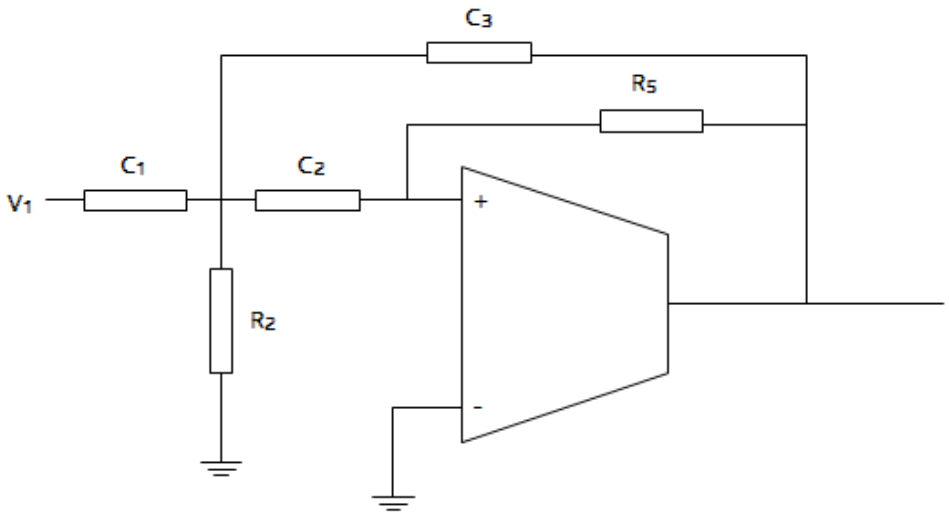


Fig.4.7 Voltage mode high pass filter [6]

Assuming the OTRA to be ideal its terminal equations to be written as

$$V_p = 0 \tag{4.11}$$

$$V_n = 0 \tag{4.12}$$

As the gain (R_m) of the transresistance amplifier is ideally infinity,this concludes

$$i_p = i_n = 0 \tag{4.13}$$

Applying KCL

$$\frac{v_1 - v_i}{\frac{1}{sc_1}} + \frac{v_1}{R_1} + \frac{v_1}{\frac{1}{sc_2}} + \frac{v_1 - v_o}{\frac{1}{sc_3}} = 0 \tag{4.14}$$

$$v_1\left(sc_1 + \frac{1}{R_1} + sc_2 + sc_3\right) = v_i(sc_1) + v_o sc_3 \tag{4.15}$$

Applying KCL at n terminal

$$\frac{0-v_1}{\frac{1}{sc_2}} + \frac{0-v_0}{R_2} = 0 \quad (4.16)$$

$$-v_1 sc_2 = \frac{v_o}{R_2} \quad (4.17)$$

$$v_1 = \frac{-v_o}{c_2 R_2} \quad (4.18)$$

$$\frac{-v_0}{sc_2 R_2}\left(sc_1 + \frac{1}{R_1} + sc_2 + sc_3\right) = v_i(sc_1) + v_o sc_3 \quad (4.19)$$

$$\frac{v_o}{v_i} = \frac{-\frac{s^2 c_1}{c_2}}{s^2 + s\left(G_2(c_2+c_2+c_3/c_2c_3)\right) + {(G_1G_2)}/{(c_2c_3)}} \quad (4.20)$$

Where,

$G_1 = \frac{1}{R_1}, G_2 = \frac{1}{R_2}, G_3 = \frac{1}{R_3}$

From the equation it is clear that

Resonance frequency $w_o = \sqrt{\frac{G_1 G_2}{c_1 c_2}}$

Quality factor $Q_o = \frac{\sqrt{G_1 G_2 G_3}}{\sqrt{c_2(G_1+G_2+G_3)}}$

Filter gain $H_O = -\frac{c_1}{c_3}$

Simulation results of the filter is shown in fig.4.7.1. Input and output of the filter is shown with gain characteristic in fig.4.7.2. Above filter is simulated with a value C_1=C_2=C_3= 100pF, R_1=0.5KΩ, R_2 = 2.25KΩ. The value of resonance frequency comes to be 9.428 Mhz and quality factor is 3.16 with filter gain H_o=1.

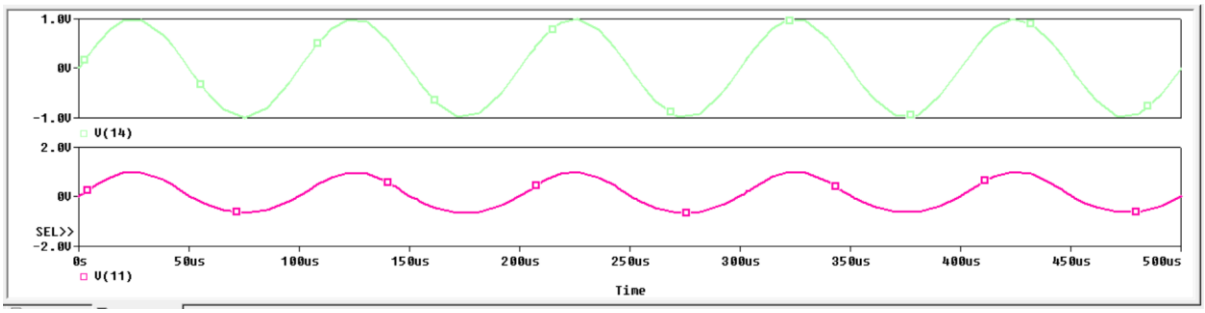


Fig.4.7.1 Input and output of high pass filter

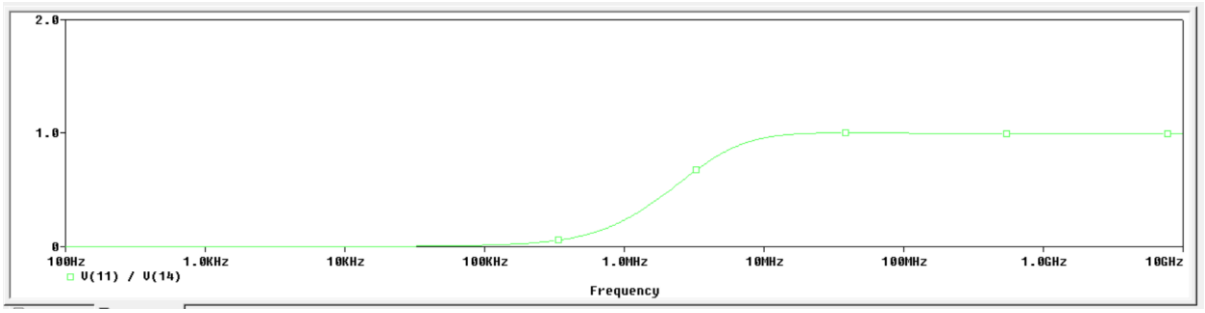


Fig.4.7.2 Gain characteristic of high pass filter

4.2.3 Band pass filter using Single OTRA

A voltage mode band pass filter [6] using OTRA [1] has been implemented in the fig.4.8 as shown. Different values of Resistance, Capacitance and Inductance are connected and circuit analysis is done as below and transfer function is obtained. PSPICE simulation results are obtained for the filter.

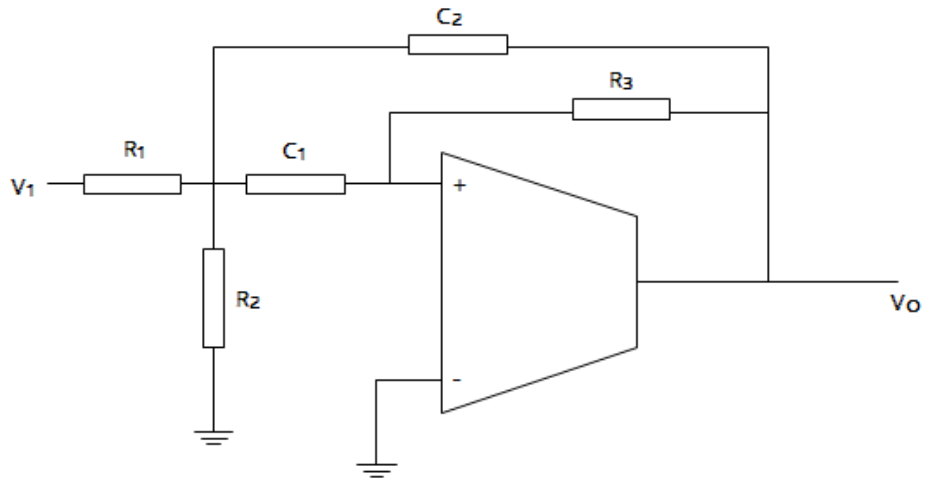


Fig.4.8 Voltage mode band pass filter [6]

Assuming the OTRA [2] to be ideal its terminal equations to be written as

$$V_p = 0 \tag{4.21}$$

$$V_n = 0 \tag{4.22}$$

As the gain (R_m) of the transresistance amplifier is ideally infinity, this concludes

$$i_p = i_n = 0 \tag{4.23}$$

Applying KCL at node 1

$$\frac{v_1 - v_{in}}{R_1} + \frac{v_1}{R_2} + \frac{v_1 - 0}{1/sc_1} + \frac{v_1 - v_0}{1/sc_2} = 0 \tag{4.24}$$

$$v_1 \left\{ \frac{1}{R_1} + \frac{1}{R_2} + sc_1 + sc_2 \right\} = \frac{v_{in}}{R_1} + v_o sc_2 \tag{4.25}$$

Applying KCL at node 2

$$\frac{0 - v_1}{1/sc_1} + \frac{0 - v_0}{R_3} = 0 \tag{4.26}$$

$$-v_1 sc_1 = \frac{v_0}{R_3} \tag{4.27}$$

$$v_1 = -\frac{v_0}{R_1 sc_1} \tag{4.28}$$

Putting the value of v_1 in equation

$$-\frac{v_0}{R_3 sc_1}\left\{\frac{1}{R_1}+\frac{1}{R_2}+sc_1+sc_2\right\}=\frac{v_{in}}{R_1}+v_o sc_2 \tag{4.29}$$

From the equation transfer function can be obtained as

$$\frac{v_o}{v_{in}}=\frac{{}^{G_1}/_{c_2}}{s^2+s(G_2(c_1+c_2)(c_1c_2)+(\frac{G_3(G_1+G_2)}{c_1c_2})} \tag{4.30}$$

This completes the voltage mode filter analysis.

Simulation results of the filter is shown in fig.4.8.1. Input and output of the filter is shown with gain characteristic in fig.4.8.2.The above filter is simulated with a value of C_1=C_2=10PF, R_1=R_2=10KΩ and R_3=20KΩ.The value of resonance frequency obtained is 1.6MHz.The value of quality factor is 1.

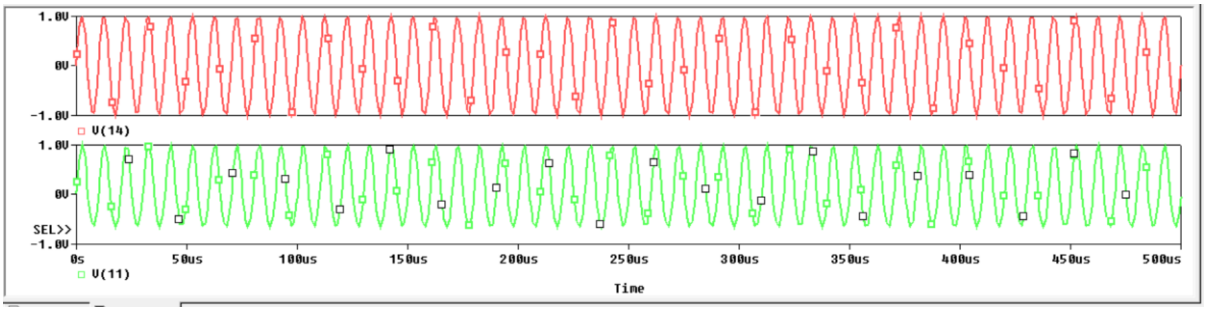


Fig.4.8.1 Input and output of band pass filter

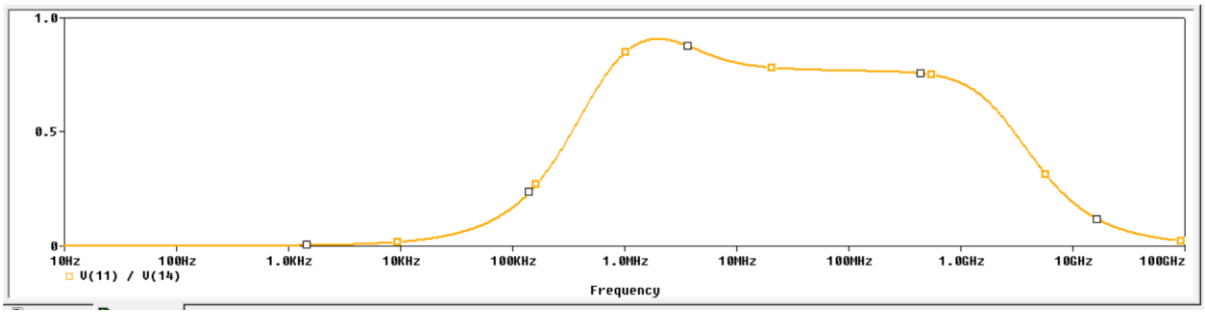


Fig.4.8.2 Gain characteristic of Band pass filter

4.3 Conclusion

All the voltage mode filters Pspice simulation has been executed and the results are obtained. The results obtained are matched with the theoretical data and values are found to be correct. OTRA as a voltage mode filter can be used in the signal processing devices to obtain the desired results.

Chapter V

Current Mode filters using OTRA and Shadow filter

5.1 Introduction

Now-a-days current mode filters are gaining importance due to its simplicity in implementing operations such as addition/subtraction, multiplication by a constants and the potential to operate at higher signal bandwidths and their capability to be used as voltage mode analogous [48]. Some of the applications in signal processing devices have requirement of current and their we require current mode filters as building blocks.

Here three different configuration of current mode all pass filter using OTRA will be discussed in details with the circuit analysis and PSPICE simulation is obtained. All the three mode topologies uses single OTRA.

A first order all pass filter is widely used for the place where input signal varies from 0 to π or π to 0 where the amplitude of the signal remains constant over all the frequency range and phase of the signal varies according to the frequency of the applied signal and it just act as a phase modifier.

5.2 Different Configuration of All pass filter using OTRA

a) This filter uses single OTRA with two resistors and a capacitor [12].The circuit analysis is done using characteristics equations of OTRA and applying KCL and KVL at its terminal node and the results are verified using Pspice.The circuit diagram representing an All Pass Filter [11],[21] is shown in fig.5.1.

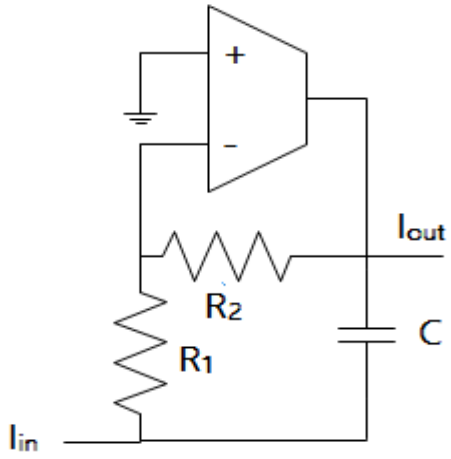


Fig. 5.1 (a) All pass filter using OTRA [12]

Applying node terminal equations and KVL and KCL we get the transfer function as given by equation as

$$\frac{I_{out}}{I_{in}} = \frac{1-sCR}{1+sCR} \tag{5.1}$$

Where $R_1 = R_2 = R \; and \; C_1 = C$

The phase equation is given by

$$\Phi = \pi - 2\tan^{-1} wRC \tag{5.2}$$

The simulations results are obtained for the all pass filter is shown in fig.5.1.1 represents input and output of the filter and fig.5.1.2 represents gain characteristic.

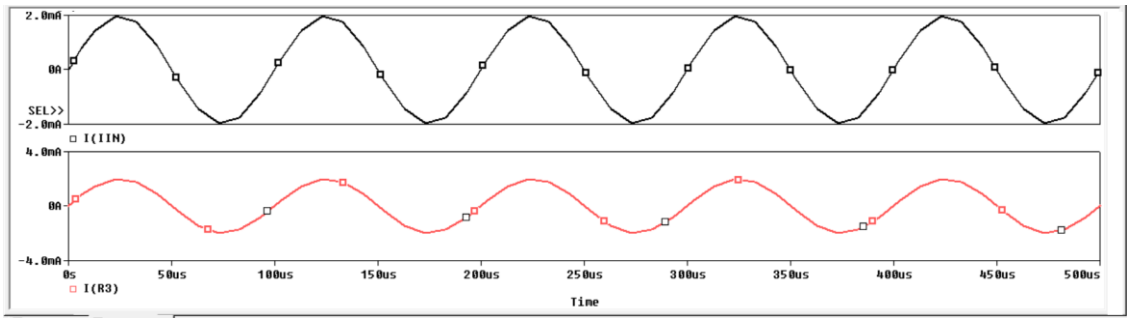


Fig.5.1.1 Input and output current of All pass filter.

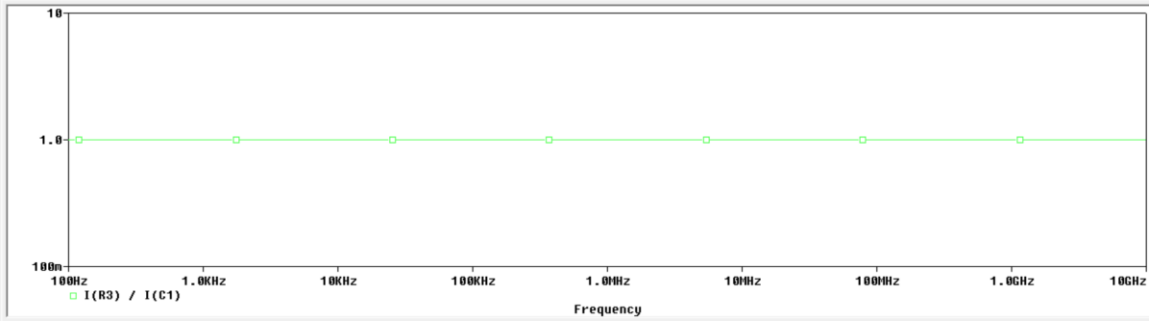


Fig.5.1.2 Gain characteristic of All pass filter

The above filter is simulated for R_1=R_2=10KΩ and C_1=10uf.The gain is found to be unity as observed in the result.

b) This filter uses single OTRA with one resistors and a capacitor [12].The circuit analysis is done using characteristics equations of OTRA and applying KCL and KVL at its terminal node and the results are verified using Pspice.The circuit diagram representing an All Pass Filter [11],[21] is shown in fig.5.2.

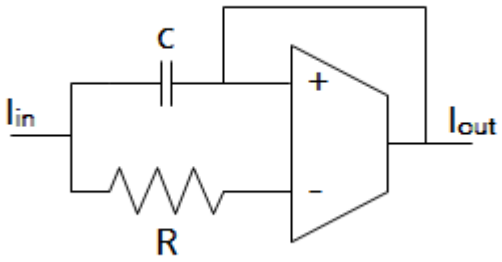


Fig.5.2 (b) All pass filter [12]

Applying node terminal equations and KVL and KCL we get the transfer function as given by equation as

$$\frac{I_{out}}{I_{in}} = \frac{1-sCR}{1+sCR} \qquad (5.3)$$

Where $R_1 = R_2 = R \; and \; C_1 = C$

The phase equation is given by

$$\Phi = \pi - 2\tan^{-1} wRC \qquad (5.4)$$

The simulations results are obtained for the all pass filter is shown in fig.5.2.1 represents input and output of the filter and fig.5.2.2 represents gain characteristic.

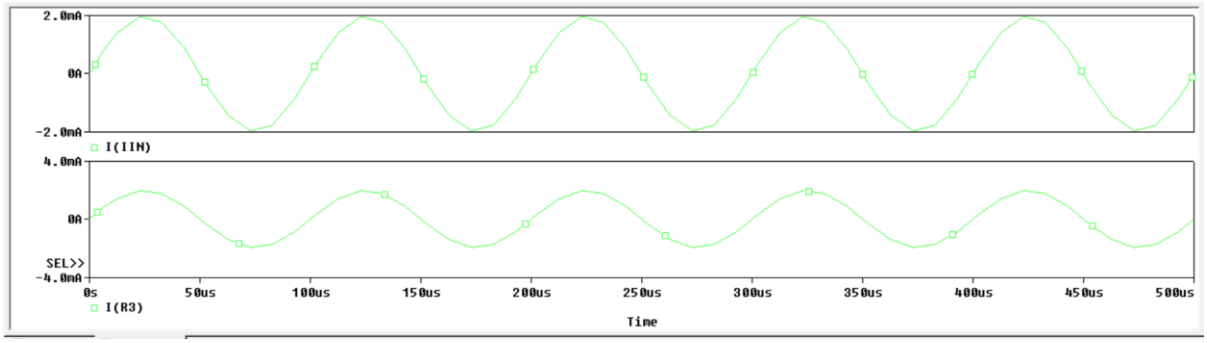


Fig.5.2.1 Input and output current of All pass filter

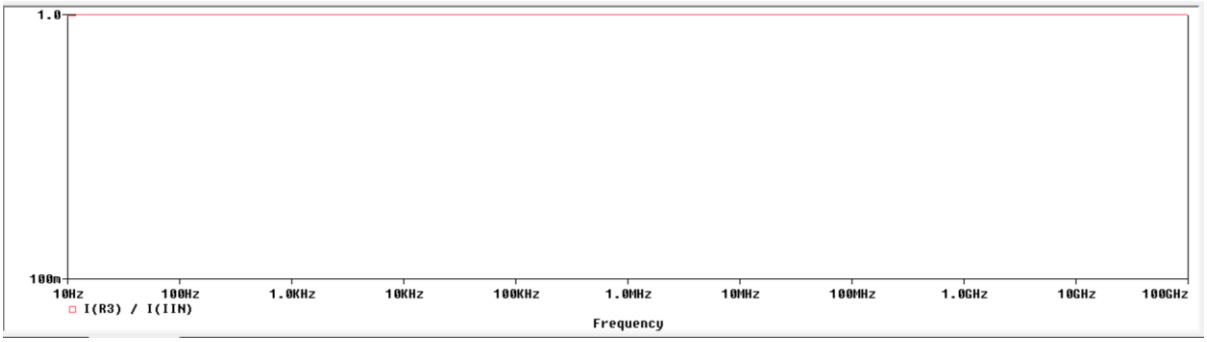


Fig.5.2.1 Gain characteristic of All pass filter

The filter is simulated for a value R=10KΩ and C = 10UF.The gain is observed to be 1 at all frequency as observed from the results.

c) This filter uses single OTRA with one resistors and a capacitor [12].The circuit analysis is done using characteristics equations of OTRA and applying KCL and KVL at its terminal node and the results are verified using Pspice.The circuit diagram representing an All Pass Filter [11],[21] is shown in fig.5.3.

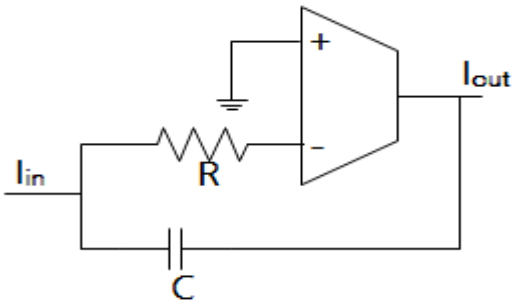


Fig.5.3 (c) All pass filter [12]

Applying node terminal equations and KVL and KCL we get the transfer function as given by equation as

$$\frac{I_{out}}{I_{in}} = \frac{1-sCR}{1+sCR} \tag{5.5}$$

Where $R_1 = R_2 = R \; and \; C_1 = C$

The phase equation is given by

$$\Phi = \pi - 2\tan^{-1} wRC \tag{5.6}$$

The simulations results are obtained for the all pass filter is shown in fig.5.3.1 represents input and output of the filter and fig.5.3.2 represents gain characteristic.

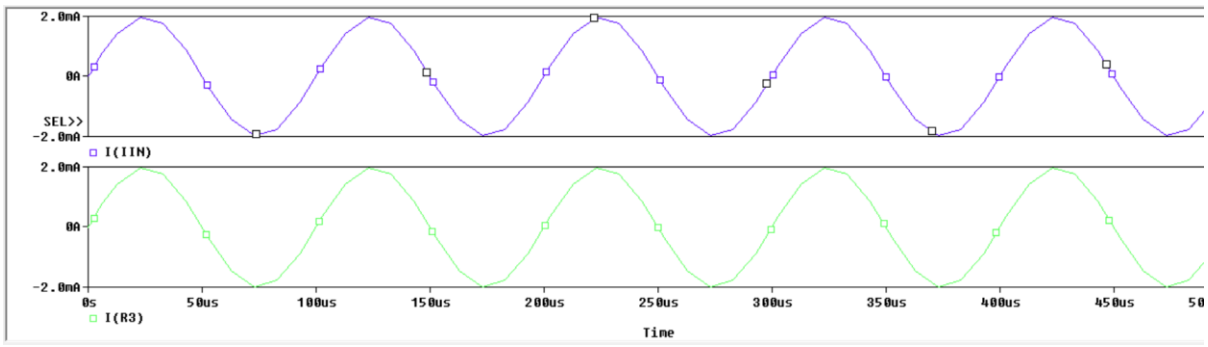


Fig.5.3.2 Input and output current of All pass filter

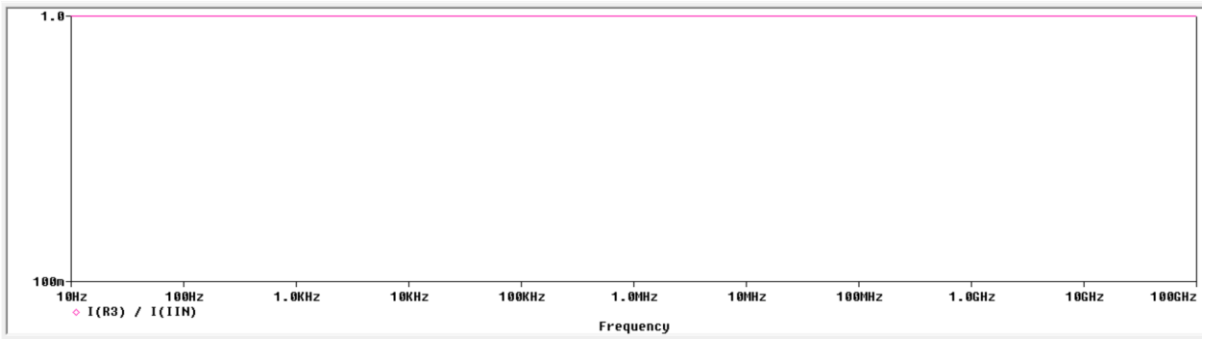


Fig.5.3.1 Gain characteristic of All pass filter

Above filter is simulated for R=10KΩ and C=100UF.The gain of the filter is observed to be 1 for all the frequency as observed in the results.

5.3 OTRA based shadow filters

A shadow filter [23] is a filter which can be tuned by varying its gain. An external amplifier is used in the feedback loop of the basic filter and by controlling its gain the resulting filter is tuned. By varying the value of gain A, the filter characteristics can be varied from very low to very high values.

Electronic channel is a direct two port recurrence specific system which permits signals in a predetermined recurrence reach to be passed, while dismissing frequencies outside this extent. The channel qualities, for example, characteristic frequency (W_o), quality component (Q_o) and bandwidth (Δω) should be tuned to a particular quality for an objective application. The channel qualities can be tuned either by changing the estimation of uninvolved parts used to plan the channel or can be electronically balanced by making those attributes subject to a few DC voltage or current. A yet another strategy for electronic tuning of channel parameters has been presented in an as of late proposed group of second-request channels termed as shadow channels [25]. In these channels an outside amplifier is included the food back circle and the attributes of the subsequent channel can then be tuned by controlling the addition of this amplifier. Contingent on the estimation of A the channel attributes can be differed

hypothetically from zero to boundlessness while practically speaking from low to high values. In writing this methodology of electronic recurrence tuning has additionally been adjusted to plan dynamic recurrence nimble channels. A broad survey demonstrates that a set number of topologies of shadow channels are accessible in writing. The plan of shadow channels is presented in anyway it doesn't give orthogonal tuning of channel attributes. This confinement is forestalled in the work displayed in by putting two parallel enhancers in criticism circle and in this way giving orthogonal tunability. The hypothesis of shadow channels is further stretched out in to nth request channels known as class n shadow channels. Current mode building pieces are utilized for functional confirmation of the channels exhibited in as these squares are not slew restricted and are preferred to design wide bandwidth, high speed systems.

5.4 Block diagram of shadow filter

Block diagram of a shadow filter is represented in fig.5.4. The H(s) and H1(s) are considered to be second order band pass (BP) and low pass (LP) transfer functions, respectively, having same denominators. When the low pass output is amplified and added to the externally applied voltage Vin, the equivalent BP and LP filter functions so obtained (H'(s) and H1'(s)) retains their filter function type but with varied characteristics. A generalized analysis of this concept has been presented in, showing that H(s) and H1(s) can represent any of the four filter functions LP, BP, high pass (HP), or band reject (BR) filter.

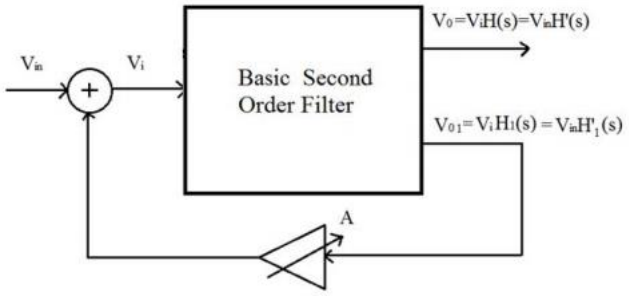


Fig.5.4 Block diagram of shadow filter [23]

Circuit diagram representing the shadow filter is represented in fig.4.5 as shown below.Considering the second order filter block in fig.4.4 is helpful in realizing the all four characteristics of LP,HP,BP and Band reject filter.

$$H(s) = \frac{d+es+fs^2}{s^2+\frac{w_o}{Q_o}s+w_o^2} \tag{5.7}$$

$$H_1(s) = \frac{a+bs+cs^2}{s^2+\frac{w_o}{Q_o}s+w_o^2} \tag{5.8}$$

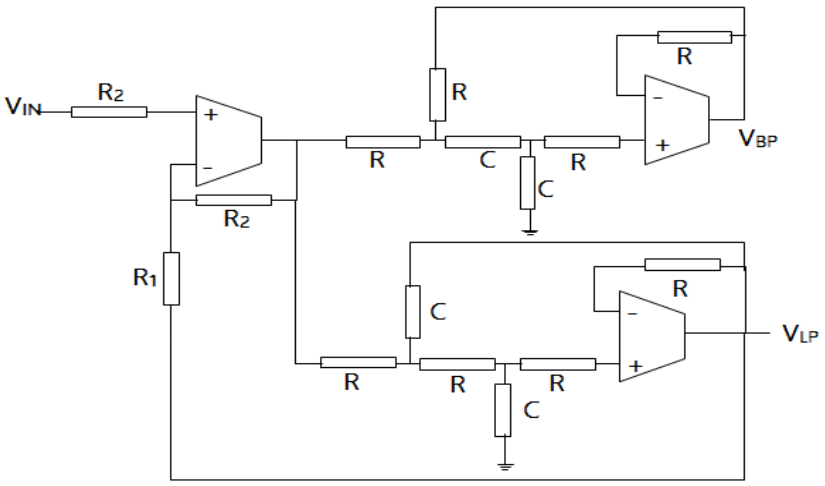


Fig.5.5 Shadow filter using multiple OTRA [23]

From fig 5.4

$$H'(s) = \frac{H(s)}{1-AH_1(s)} \tag{5.9}$$

Substituting H(s) and $H_1(s)$

$$H'(s) = \frac{d+es+fs^2}{s^2(1-Ac)+\left(\frac{w_o}{Q_o}-Ab\right)s+w_o^2-A\alpha} \tag{5.10}$$

The coefficients W_o and Q_O respectively represent the characteristic frequency and quality factor of the shadow filter. If the feedback is taken from LP then,

$$W_o' = w_0\sqrt{1-\frac{A\alpha}{w_o^2}}; \qquad Q_O' = Q_0\sqrt{1-\frac{A\alpha}{w_o^2}}$$

This shows that the center frequency and Q change proportionately and the bandwidth remains same as the previous value.

If H_1(s) is considered to be HP output of the second order cell then,

$$w_0' = \frac{w_o}{\sqrt{1-A_c}}; Q_O' = Q_O\sqrt{1-A_c}$$

From above it is clear that the product of quality factor and characteristic frequency remains constant and higher quality factor at lower frequency and vice versa can be obtained.

If the feedback signal is taken from the BP output, then

$$w_0' = w_o; Q_O' = \frac{Q_O}{1-\frac{AbQ}{w_0}}$$

Simulation result for the shadow filter is shown in fig.5.5.1 which shows the input and output. Fig.5.5.2 shows gain of the low pass shadow filter.

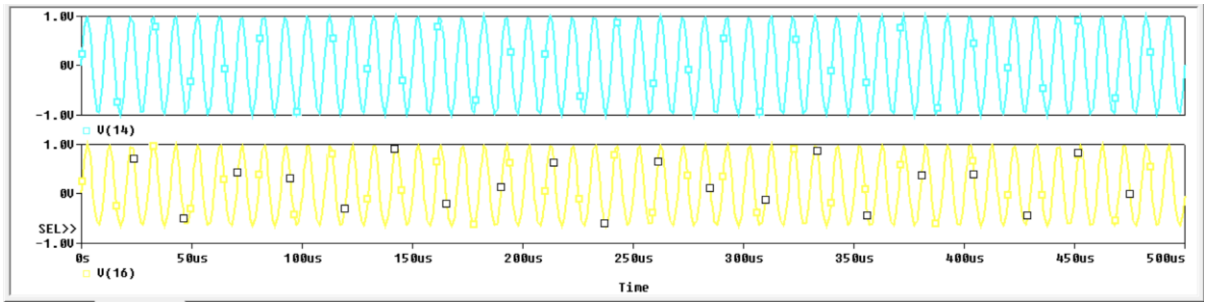


Fig.5.5.1 Input and output of shadow filter

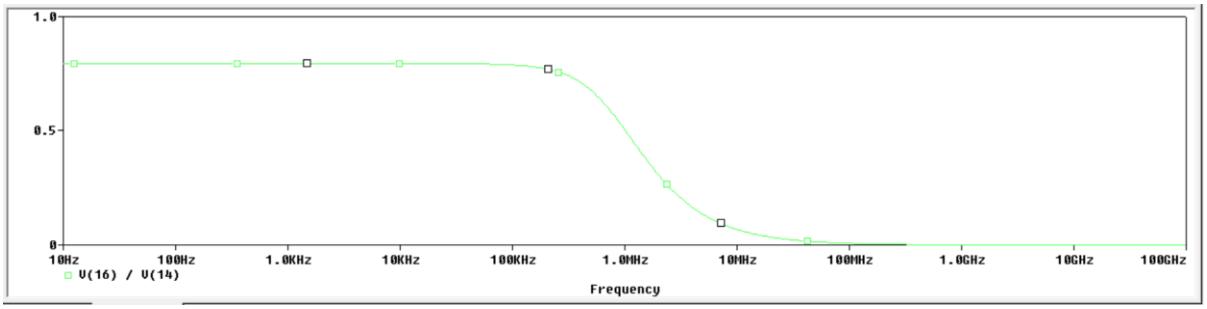


Fig.5.5.2 Gain characteristic of low pass shadow filter

The above is simulated using R_1=20KΩ, R_2=20KΩ, R_3=20KΩ, R4=4KΩ R_5=4KΩ, C_6=0.1Nf, R_7= R_8= R_9 = R_{10}= R_{11}= R_{12}= 4KΩ.

The above values give the bandwidth to be 92 MHz.

The gain of the filter is -1.

From the above it is clear that quality factor varies with fixed center frequency.

The OTRA based complete shadow filter realizing LP controlled BP structure is shown in Fig.5.5. The BP and LP responses are obtained through OTRA 1 and OTRA 2 respectively. The OTRA 3 performs the function of an inverting amplifier and adder where in the amplified LP output gets added with applied input. The gain A of the inverting amplifier ($A = -R_2/R_1$) can be varied by changing value of R_2. The BP controlled BP and HP controlled BP configurations may be obtained by using component selections.

5.5 Conclusion

Simulation result is obtained for various current mode filters and shadow filters. Current mode filters are getting more importance now a day in signal processing circuits.

Chapter V1

Leap Frog Filter

6.1 Introduction

A leap frog filter of order two is an active filter having electronic circuit which simulates the passive electronic ladder. Active-ladder or multiple feedback filter are the other names of the leap frog filter [49]. The arrangement of feedback loops in the signal flow-graph of simulated ladder filter inspired the name leapfrog filter. The leap frog filter has the low component sensitivity of the passive ladder filter that it simulates.

A low pass ladder filter is represented in fig.6.1. Its signal flow graph is also drawn as shown in fig.6.2 below.

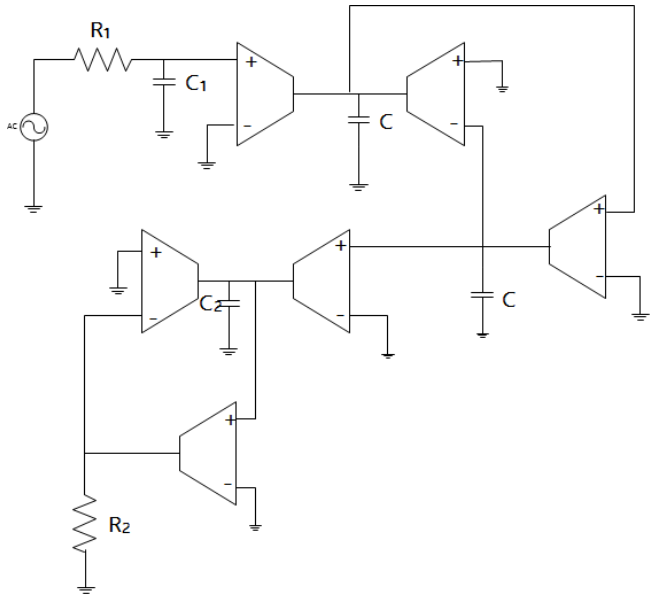


Fig.6.1 Low pass filter(Leap frog)

The above circuit consists of a grounded inductor implemented using OTRA and parallel series connection of resistance, capacitance and inductance.Output is taken across resistor R_2.

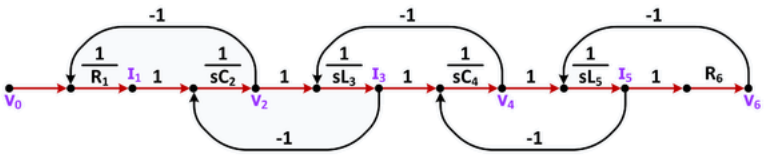


Fig.6.2 Signal flow graph of low pass filter

Simulation results for the leap frog filter is shown in fig.6.1.1 as below.

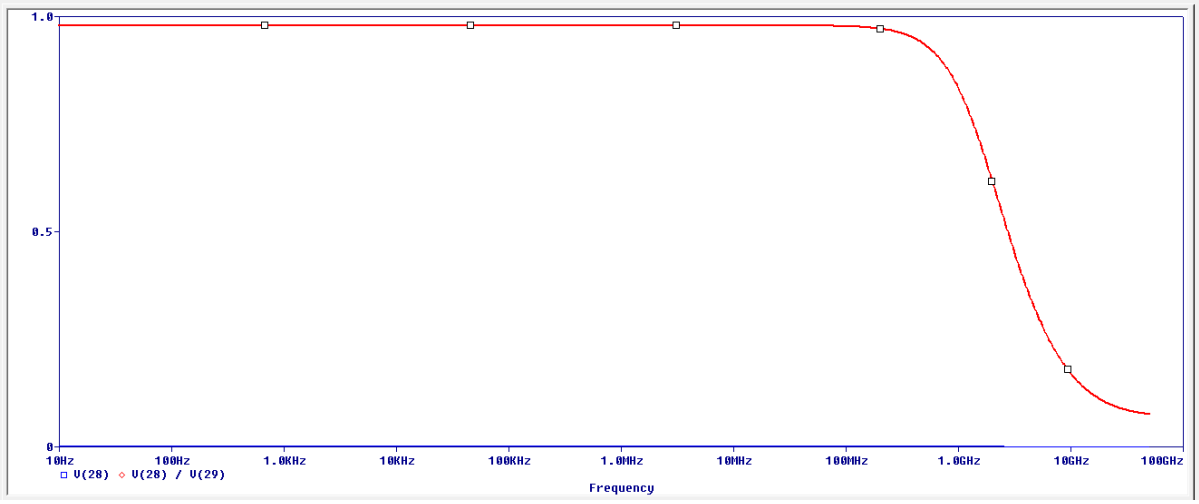


Fig.6.1.1 Gain characteristic of leap frog low pass filter.

The above circuit is simulated using R_1= R_2= 1kΩ, C_1=300pf, C_2=100pf. The value of inductance comes to be 0.208mH .The bandwidth of this filter comes to be 6.8Mhz.The gain is decreasing with increase in frequency as observed in the simulation result.

6.2 Synthesis of leap frog filters

The definition and synthesis of leapfrog filters is described by Temes and LaPatra Chen and Wait, Huelsman and Korn.

Following are the steps which are typically followed in the synthesis of Leapfrog filters

a) Determination of a prototype passive ladder filter having desired frequency response. Normally a doubly terminated prototype is used.

b) All the voltage(KVL) and current equations(KCL) related to the elements are written for the formation of signal flow graph.

c) Signal flow graph is obtained and the nodes of the signal flow graph includes voltages and currents. The branch gains include the impedances and the admittances.

d) Now all the nodes of the signal flow graph are converted into voltages and all the impedances are converted into dimensionless transmittances. This is accomplished by multiplying all the impedances with 1/R an arbitrary resistance and dividing all admittance elements by 1/R. This scaling will not change the frequency response.

e) Manipulate the SFG in such way that gains feeding each summing node have the same signs. This step has to be don for implementation convenience. After the execution of this step all the feedback gains in the SFG will be converted into +1 and the signs of the gain block will be reversed.AS a consequence some of the nodes which also includes the main output may get 180 degree phase reversed. This has normally no consequence.

f) The gain blocks used are implemented with active filters and they are interconnected as indicated in the signal flow graph. Sometimes state variables filters are also used in gain blocks.

g) The final circuit obtained will have more components than the prototype passive filter which means that the final circuit obtained has degree of freedom which can be used to optimize the circuit for dynamic range and practical values of components.

6.3 Generic Filter

The design of generic filter [17] starts with a known ladder filter of one of the topologies shown in the fig.6.3. Usually all the ladder filters are lossless except the last filter which is lossy. The figure shows a four element ladder filter with voltage input and voltage output.

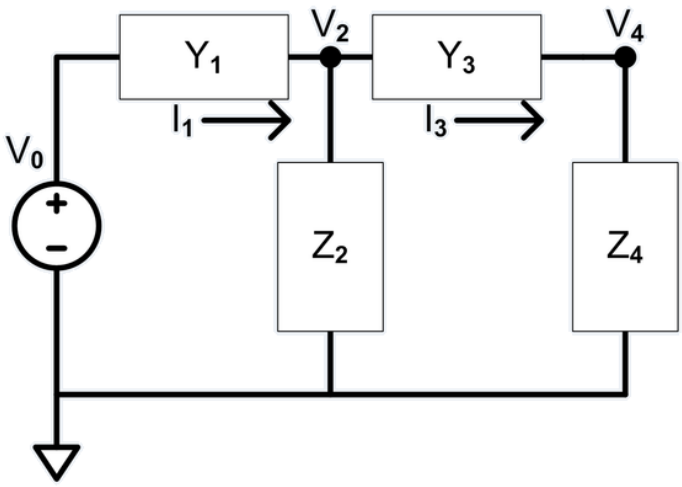


Fig.6.3 Four element ladder with voltage input and voltage output [49]

$$I_1 = (V_O - V_{2)}Y_1 \tag{6.1}$$

$$V_2 = (I_{2-} I_3)Z_2 \tag{6.2}$$

$$I_3 = (V_2 - V_{4)}Y_3 \tag{6.3}$$

$$V_4 = (I_{3)}Z_4 \tag{6.4}$$

The signal flow graph equations are represented above.The name leapfrog filter is assigned due to the arrangement of the feedback loops in the signal flow graph.Manipulation in the signal flow graph is done to convert all the current node into voltage nodes and all the admittances and impedances into dimensionless transmittances.This represents the manipulation in the equations either by multiplying one side by R/R and distributing the *R* terms across the subtraction operation or multiplying both sides by R.This manupultion changes the equation in following ways

$$V_1 = (V_O - V_2)H_1 \tag{6.5}$$

$$V_2 = (V_1 - V_3)H_2 \tag{6.6}$$

$$V_3 = (V_2 - V_4)H_3 \tag{6.7}$$

$$V_4 = (V_3)H_4 \tag{6.8}$$

Where

$$H_1 = RY_1,\ H_2 = GZ_2, H_3 = RY_3, H_4 = GZ_4, G = \frac{1}{R}, V_1 = RI_1, V_3 = RI_3$$

The manupulation in signal flow graph is done so as to make the gains into each summing node is +1.The results of all manipulation is shown in fig. below.The resultant equations of the resultant signal flow graph are as follows:

$$-V_1 = (V_O - V_2)(-H_1) \tag{6.9}$$

$$-V_2 = (-V_1 + V_{43})(H_2) \tag{6.10}$$

$$V_3 = (-V_2 + V_4)(-H_3) \tag{6.11}$$

$$V_4 = (V_3)H_4 \tag{6.13}$$

The negative sign before $V_1\ and\ V_2$as label of nodes in the signal flow graph indicates that these nodes represent a 180 degree phase difference with respect to the signals in the prototype filter.

Simple steps are followed for the manipulation as given in steps below

i) All the odd numbered or all the even numbered transmittances are made negative.If the total numbers of inversions are even then the overall phase shift with respect to the prototype is o degree.

ii) All feedback gains are changed to +1.

iii) The number of inversions to that node from input are counted which determines the sign of each node.

iv) The node is labeled negative if the number of inversions is odd.

The signal flow graph is most suitable for its implementation.State variables filters that are available in both inverting mode and non-inverting topologies are often used.

6.4 Band pass filter

The ciruit diagram of a band pass passive filter is determined first.The individual components in series or parallel can be combined in general impedences or admittances.

The schematic diagram for a passive band pass electronic filter using OTA and OTRA is shown in fig.6.4. The above circuit consists of two inductors,one floating inductor with OTA [50] as building block.Another grounded inductor is simulated using OTRA as building block. OTA is simulated using C-MOS technology [51].

Inductor through OTA is simulated using the value of C = 0.1µF, R_L= 64Ω I_{B1}=I_{B2}=I_{B3}=50µA.Grounded inductor simulated throug OTRA has an inductance value L = 0.208µH found through simulated results.

With these values the inductance value is found to be L= 0.166mH.

Its signal flow graph is shown below in the fig.6.5.Different values of resistors,capacitors used here in this circuit has value as R_1=100KΩ, R_2 = R_3 = R_4 = R_5 = R_6 = R_7 =R_8 =R_9=R_{10}=R_{16} = 10KΩ.C_1 = 1µF,C_2 = 300nF ,C_3 = 0.1 µF , C_4 = C_5 = C_8 = 0.1nF.

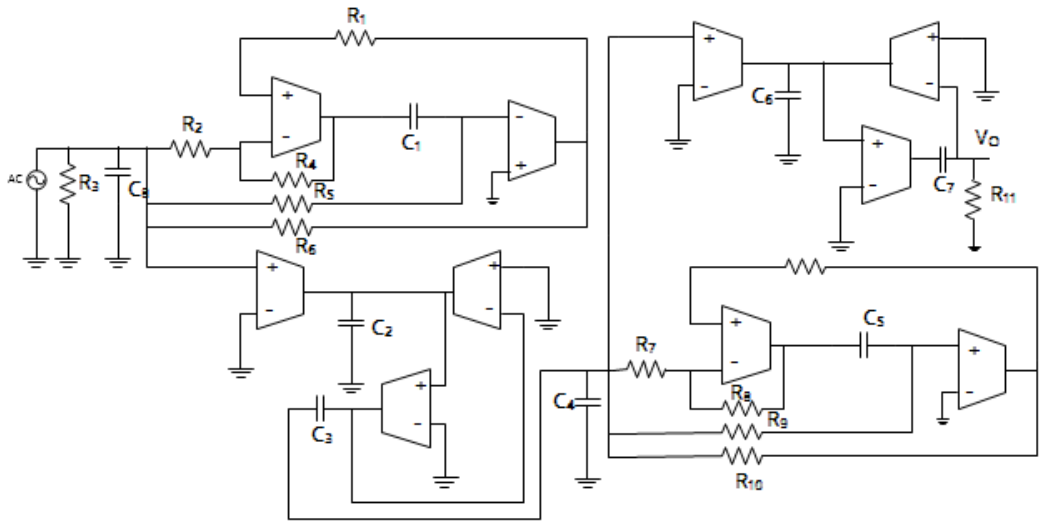


Fig.6.4 Band pass filter using leap frog technique

For the above circuit diagram

$$Z_1 = \frac{sL_1}{s^2C_1L_1 + s\frac{L_1}{R_1} + 1} \tag{6.14}$$

$$Y_2 = \frac{sC_2}{s^2C_2L_2 + 1} \tag{6.15}$$

$$Z_3 = \frac{sL_3}{s^2C_3L_3 + 1} \tag{6.16}$$

$$Y_4 = \frac{sC_4}{s^2C_4L_4 + sC_4R_4 + 1} \tag{6.17}$$

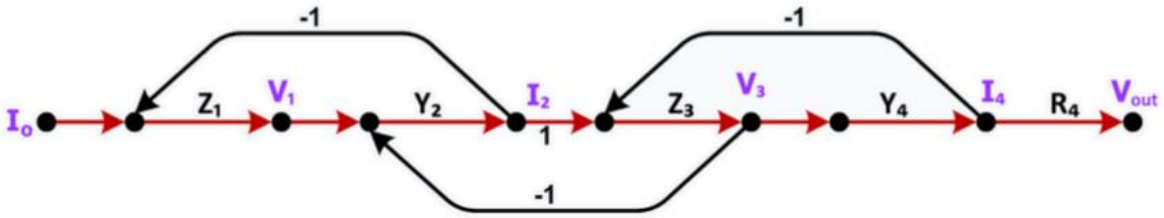


Fig.6.5 The signal flow graph representation of the ladder filter equations

The equation representing the relation between voltage and current is given by the equations as below

$$V_1 = (I_O - I_2)Z_1 \tag{6.18}$$

$$I_2 = (V_1 - V_3)Y_2 \tag{6.19}$$

$$V_3 = (I_2 - I_4)Z_3 \tag{6.20}$$

$$I_4 = V_3Y_4 \tag{6.21}$$

$$V_4 = I_4R_4 \tag{6.22}$$

Fig. 6.4.1 shows the simulation results of the leap frog band pass filter.

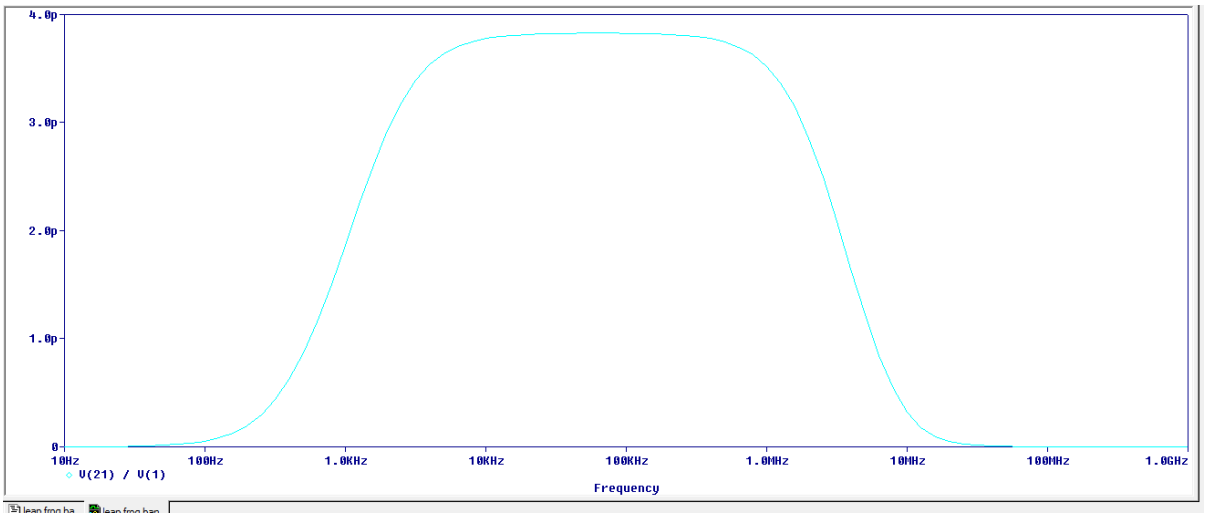


Fig.6.4.1 Gain characteristic of band pass filter

6.5 Scaled signal flow graph

The current variables is multiplied by an arbitrary resistance to convert into voltage variables which converts all the gains into dimensionless values.All the currents are multiplied by R,this is accomplished by multiplying R/R one side and then the R term is distributed over the currents.Below fig.6.6 representsthe signal flow graph of the ladder filter equations with inpedences scaled by R,which is an arbitrary resistance.

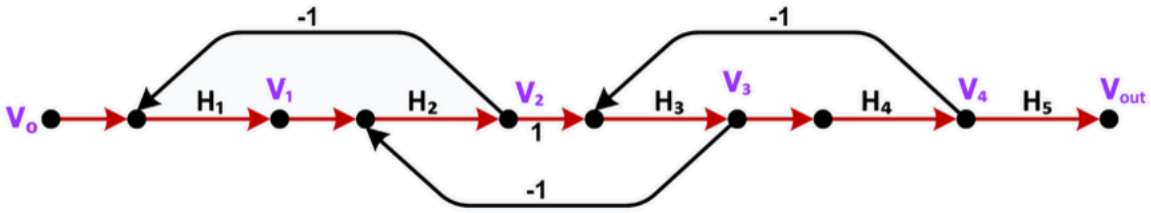


Fig.6.6 Signal flow graph representation with impedences scaled by an arbitrary resistance R

Equations obtained for the above signal flow graph are given by

$$V_1 = (V_0 - V_2)H_1 \quad (6.23)$$

$$V_2 = (V_1 - V_3)H_2 \quad (6.24)$$

$$V_3 = (V_2 - V_4)H_3 \quad (6.25)$$

$$V_4 = (V_4)H_4 \quad (6.26)$$

$$V_{out} = (V_4)H_5 \quad (6.27)$$

Where

$$H_1 = GZ_1, H_2 = RY_2, H_3 = GZ_3, H_4 = RY_4, H_5 = GR_4, G = \frac{1}{R}, V_2 = RI_2 \ and \ V_4 = RI_4$$

6.7 Conclusion

Leap frog filter analysis is done and it is simulated using Pspice and results are obtained. It is difficult to tune a leapfrog filter because of the complicated feedback.One of the method to tune it is to open the feedback loops so that the remaining filter structure becomes a simple cascade design.Each cascaded section is then tuned independently.The inner sections $H_2 \ and \ H_3$ have finite value of Q and it may become unstable when the feedback loops re opened.So these stages are designed with large value of Q but should have finite value such that it remains stable when the feedback loops are open.

CHAPTER VII

SUMMARY AND CONCLUSION

7.1 Summary

In this dissertation we have presented a study on designing and implementation of different types of filters using OTRA. Filters are a very important part of signal processing which is used to eliminate unnecessary frequency components. In the following we present a summary of the work done in this project.

In chapter I, the general description of OTRA is presented. Some background material on various current mode and voltage mode active buildings blocks used for the implementation of OTRA has also been presented.

In chapter II, history, characteristics, terminal equations, applications and CMOS implementation of the OTRA is briefly discussed. Some basic circuits like adder, subtractor, integrators etc has been discussed.

In chapter III, various papers on filters, oscillators, multivibrators and inductors using OTRA has been discussed in brief.

In chapter IV, a brief discussion on the voltage mode filters using OTRA has been presented. Low pass filter, high pass filter and band pass filter has been implemented using OTRA.

In chapter V, different modes of first order all pass filter using OTRA and shadow filter using OTRA is presented and simulated using PspicE.

In chapter VI, low pass and band pass leap frog filter has been implemented using OTRA.

7.2 Future scope

In this project emphasis was on using OTRA as a building block in leap frog filter implementation. The work presented in this project may be extended to implement higher order leap frog filters using OTRA. Furthermore we have not carried out high pass filter and all pass filter using leap frog technique. These studies may be carried out to give the complete quantitative characterization of these filters. Thus there is ample scope for extending this work.

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