Investigation of Leakage Power in DCVS Logic Family

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by

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CERTIFICATE

This is to certify that the dissertation titled "**Investigation of Leakage Power in DCVS Logic Family**" is a bonafide record of work done by **Pratibha Bajpai, Roll No. 2K14/VLS/15** at **Delhi Technological University** for partial fulfilment of the requirements for the award of degree of Master of Technology in VLSI and Embedded systems Engineering. This project was carried out under my supervision and has not been submitted elsewhere, either in part or full, for the award of any other degree or diploma to the best of my knowledge and belief.

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ABSTRACT

Rapid scaling of transistor dimensions in accordance with Moore's law due to brisk demand of high speed portable electronic device has led to drastic upsurge in leakage currents in the device leading to unnecessary leakage power dissipation. The research in this thesis unfolds the rising gravity of the issue with continuous technology advancement and explores different ways to curtail the problem. Of late, a shift of trend from conventional CMOS logic to differential logic styles has been witnessed due to their in-built features of lower power consumption and high speed. DCVSL which is one of the differential logic families is an efficacious blend of the advantages of traditional CMOS logic and pseudo NMOS logic and offers a high speed, area effective and rail to rail swing logic design option. Henceforth, DCVS logic family has been explored in this thesis to exploit its inherent advantages and moreover its leakage power aspect has been dealt deeply to introduce low power DCVS logic which works well at lower technology nodes.

This thesis includes in depth study of causes of leakage power in devices and techniques to regulate leakage current at circuit level for CMOS logic circuits. Trends followed by leakage current with variation in supply and technology are studied and verified. LECTOR technique used for CMOS logic has been adapted and aptly applied to static, dynamic and enhanced DCVS logic which achieves a significant saving in leakage loss for DCVS logic circuits. Various basic logic circuits are implemented using DCVSL style and their low power versions are proposed by adapting studied methodologies which are leakage power efficient. Hybrid configurations involving combination of transmission gate logic and DCVS logic are proposed for two input and three input XOR gates for static, dynamic and enhanced DCVS logic. Hybrid configuration proves to be more efficient in terms of leakage power saving. Furthermore, LECTOR incorporated versions of hybrid configurations are introduced which achieves even more leakage saving when compared to basic DCVSL configuration. The functionality and effectiveness of all proposed architectures are confirmed through intensive simulations on SYMICA Development Environment at 90nm, 65nm and 45nm technology parameters (leakage effect is more predominant below 180nm). All the above introduced circuits are simulated with VDD=1.8V and 1.2V to analyse the pattern followed with supply variation. Similarly, temperature variation is performed for temperature values of -25°C, 27°C and 100°C at 45nm technology and VDD=1.2V. Effect of proposed configurations on the delay of the circuit has been analysed as well.

Chapter 1

Introduction

1.1 MOTIVATION

Earlier chief design constraints in VLSI design used to be the area, delay and cost of the device or system being designed. In recent years this trend has changed vividly and minimal power dissipation has been witnessed to emerge as the greatest challenge for designers relatively to other design metrics to avoid heating up and degradation of device [1]. Low power design has become the need of the hour of semiconductor industry due to steep increase in the demand of power efficient portable electronic devices. Portable devices have two modes of operation –active mode and standby mode. Cell phones, PCs and laptops sit in idle state most of the times and have burst mode type integrated circuits i.e. their idle time is quite higher than the time for which they are active[2]. There is a leakage power dissipation which takes place when the device is non-operational and drains out the battery worth of no use. This leakage power has come into main focus since the VLSI design industry has entered into deep submicron regime.

The demand of reduced overall power dissipation, higher speed and denser integration has commenced the scaling of MOS devices in every technology generations. Well known Moore's Law which is a phenomenological observation that every two years the number of transistors on an IC doubles is the practical realisation of scaling theory. A corollary of Moore's law is Dennard's Scaling Law [3]: as transistors shrink, they become speedier, consume less power, and are cheaper to manufacture. The multiplication in Transistor count in Intel microprocessors is shown in fig 1.1[3]

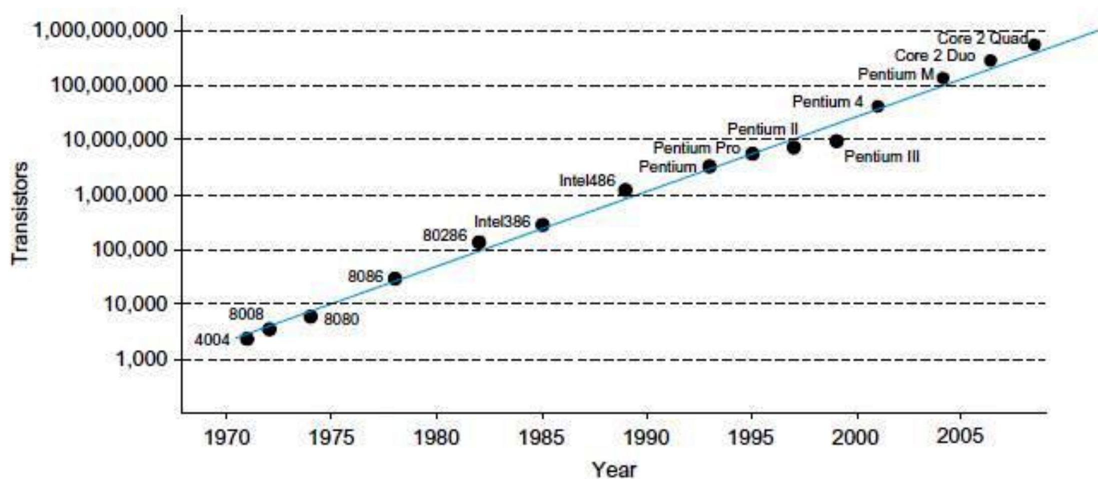


Fig 1.1 Transistors in Intel microprocessors[3]

Undoubtedly progressing towards lower technology nodes is fulfilling above mentioned gainful features but unfortunately has resulted in a drastic increase in leakage currents while the device is inactive which gets even worse when multiplied with millions of transistors count on chip. The reasons behind the same are explained in the following chapters. We can observe the pattern followed by leakage power dissipation with decreasing channel length from fig 1.2[4]. It is an estimation based upon the present scenario that leakage power is going to increase 32 times per device as we touch year 2020 [5] . Fig 1.2 shows the percentage contribution of leakage power and active power in total power dissipated at various technology generations [4]. It should be noted that with every technology advancement leakage power share in overall power dissipation increases manifold and has even exceeded active power for below 45nm technologies. Consequently, it has become extremely crucial to regulate the increasing leakage loss with shrinking device geometries.

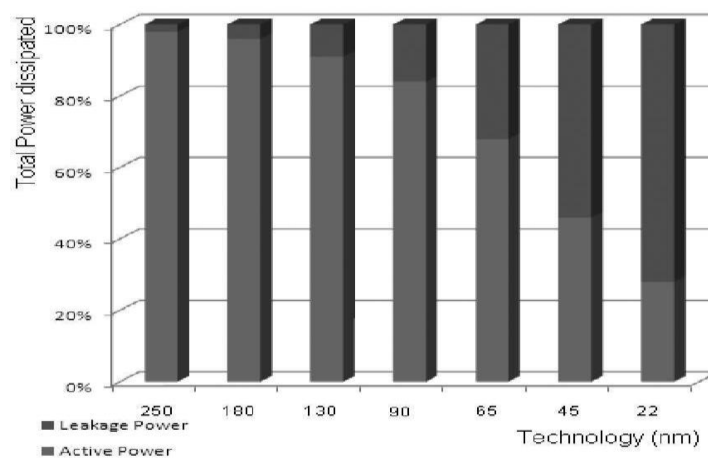


Fig 1.2 Power dissipated in various technologies [4]

Design styles and logic family play a significant role in deciding the performance and

efficiency of the circuit based on various design constraints like area, speed, power dissipation, threshold voltage and supply voltage scalability of the circuit**.** Differential logic styles are gaining attention of researchers rapidly as they offer some very promising features like superior noise immunity, compact structure and implementation of both complemented and non-complemented functions together. There are several differential logic styles available like CPL, MCML etc. Differential cascode voltage switch logic or DCVSL is one of them which successfully combines the advantages of both conventional CMOS logic and pseudo NMOS logic and thereby provides a high speed, area efficient and rail to rail swing slogic design alternative. Our motive is to first to study various leakage reduction techniques available for CMOS logic circuits. Secondly, analyse DCVSL logic family in terms of its leakage power loss at various technology generations and develop a self-controlled circuit level methodology to minimise leakage currents for the same. Choice of logic family proves to be very crucial in accordance with what all design constraints are to be met and hence is a challenging task for VLSI designers.

1.2RESEARCH OBJECTIVE

The basic motivation to proceed with this particular research is to perform a profound study of circuit level techniques to counteract the increasing leakage power losses with finer technologies and come up with a low power differential logic style by aptly applying those to DCVSL family. DCVSL being a differential logic style offers certain advantages over logic implementation using conventional CMOS logic style and hence is a part of high speed digital circuit designing. A lot of research has been performed in the field of leakage power reduction for traditional CMOS logic but leakage power aspect of DCVSL style is yet to be explored. This thesis is an attempt to unfold the leakage power losses in DCVSL logic circuits and propose different new low power structural configurations for the most frequently used logic circuit in digital VLSI design i.e. XOR gate which has minimal leakage power dissipation. The objectives of carrying out this research work are:

- To carefully study the trends followed by leakage power dissipation with rapid technology advancements.
- Study of various components contributing to leakage current and in depth analysis of several circuit-level leakage reduction techniques to gain control over it.
- Appropriately applying the knowledge of studied techniques to achieve DCVSL configuration incorporated with a self-controlled leakage reduction facility.
- Simulating basic static DCVSL, dynamic DCVSL and EDCVSL circuits along with proposing their low power, leakage controlled versions and comparing their leakage currents.
- To introduce new hybrid static and hybrid dynamic DCVSL architectures for two input and three input XOR gates and their reduced leakage configurations.
- To introduce new special structures (NP mixed DCVSL and DSCL) for two input XOR gate.
- Verification of proposed structures by performing intensive simulations on SYMICA development environment at 180nm, 90nm, 65nm and 45nm technologies.
- Performing voltage supply and temperature variations for the proposed structures.

1.3 STRUCTURE OF THESIS

This thesis is framed in five chapters. First chapter discusses the basic motivation behind this work which explains that why this research has been taken up accompanied by the objectives of this thesis and also the literature regarding the leakage power reduction techniques in CMOS logic and in DCVS logic has been reviewed. Chapter 2 delineates about the trends followed by leakage power with scaling down of technology, types of power dissipation and different components of leakage current. It also discusses the various circuit level techniques to regulate leakage current through a CMOS logic circuit. Moreover, towards end it presents a comparison between various techniques. Chapter 3 is dedicated to static DCVSL which explains the advantages of DCVS logic style over traditional CMOS logic. It discusses the

operation of basic DCVSL, throws a light over existing leakage reduction techniques for DCVSL and proposes a new LECTOR incorporated structure of DCVSL which provides a self-controlled leakage reduction facility in DCVS logic circuits. It also presents an overview of transmission gate logic and finally proposes new hybrid configurations for 2 input and 3 input static DCVSL XOR gates combining transmission gate logic and DCVS logic which are then compared with existing fully stacked DCVSL structure of XOR gates for leakage currents. Chapter 4 describes the dynamic counterpart of DCVSL along with enhanced DCVSL. Hybrid dynamic DCVSL and EDCVSL architectures for 2 input and 3 input XOR gates have been proposed. In conjunction with this two special structures namely NP mixed DCVSL and LECTOR incorporated DSCL have been proposed. Voltage and temperature variations also have been performed for existing and proposed structures and the comparison is drawn. Chapter 5 comprises conclusion drawn from varied study and simulation, in accordance with the thesis objectives.

Chapter 2

Leakage Power Minimization Techniques

2.1 INTRODUCTION

With perpetual scaling of devices dimensions to stay on Moore's law is leading the electronics industry towards the path of denser and speedier integration. Henceforth it has provided a provision for catering the demand of complex functions with higher performance and lower power dissipation. Along with minimising device sizes supply voltage needs to be scaled as well to avoid high electric field effects (second order effects) and maintain the acceptable system functioning. Moreover voltage scaling is the most effective method to save dynamic power ($C_{load}*F_{clk}*V_{dd}^2$) because of its square law dependence on supply voltage plus the reduction in parasitic capacitance due to scaling of device leads to lesser load capacitance and hence reduced dynamic power. Unfortunately voltage scaling degrades the performance of the circuit by reducing its speed due to decrease in overdrive voltage (V_{gs} -V_{th}). Generally, the ratio of the supply voltage to the threshold voltage of the device should be at least 5, in order to ensure that the performance of CMOS circuits is least affected [6]. Therefore, to counteract the performance degradation due to voltage scaling, we scale down threshold voltage of transistor to lessen the gate delays. Scaling V_{th} is followed by an exponential increase in sub threshold leakage current. There are several other components as well contributing to leakage power dissipation in deep submicron and nanoscale technologies explained later in the chapter. But the most dominant phenomenon is subthreshold leakage which outdoes other leakage components.

Threshold voltage of transistors needs to be adjusted in digital circuits design for maximum saving in leakage loss while maintaining the desirable performance. Circuit level methodologies have a very important role to play in the motive of regulating the subthreshold leakage power dissipation in both active and sleep modes. Hence it has turned out to be indispensable for circuit designers to concede the importance of controlling leakage power consumption and saving energy efficiently at all levels of the design hierarchy, starting from the lower levels of abstraction. Various leakage minimisation techniques have been discussed in detail in the chapter.

2.2. POWER DISSIPATION IN CMOS CIRCUITS

Average power dissipation (P_{avg}) of CMOS digital circuits can be expressed as the sum of three key components which are given in the following equation, as

$$\mathbf{P_{avg} = P_{short\text{-}circuit} + P_{leakage} + P_{dynamic}}$$

2.2.1 Short-Circuit Power: Short-Circuit Power is the power dissipation which takes place from stacked P and N device in a CMOS logic gate which get ON simultaneously. This happens for a brief period of time during which the input of the circuit switches. The most prominent way to control this type of power dissipation is the minimization of the transition times on nets. It typically accounts for 15%-20% of the overall power dissipation.

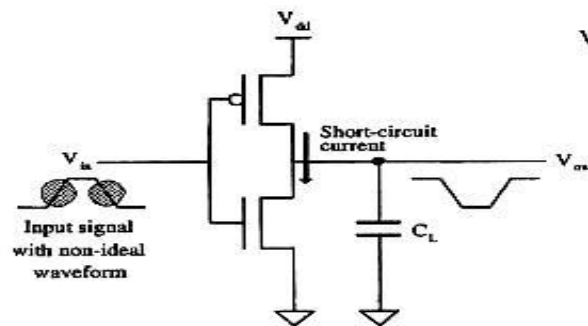


Fig 2.1 Short-circuit power

As the frequency of operation is being increased with every technology generation, the transition time signals are also getting reduced thus resulting in reduction of static power. Figure 2.2 shows that Intel microprocessor clock frequencies have doubled approximately every 34 months [4].

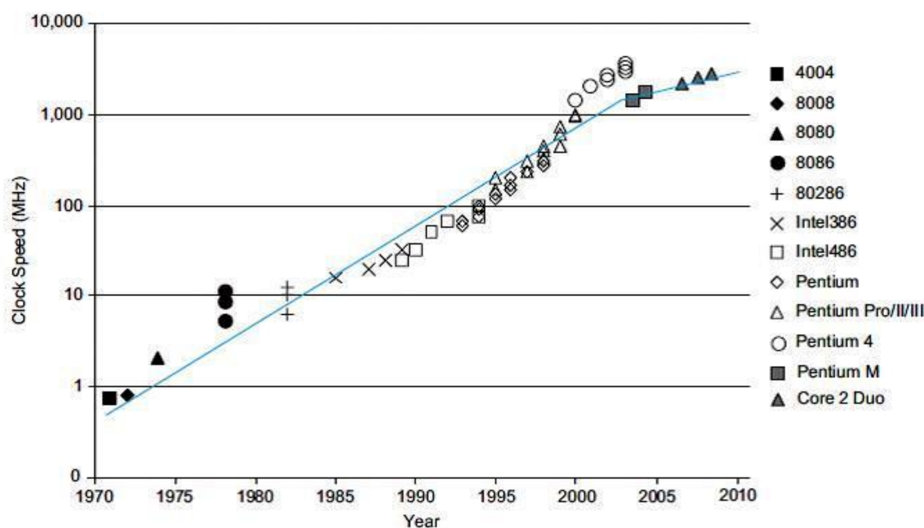


Fig 2.2 Clock frequencies of Intel microprocessors [4]

2.2.2 Dynamic Power: is the dynamic power dissipation, also called the switching power. This is the dominant source of power consumption in CMOS system-on-chip (SoC), accounting for roughly 75% of the total. It is generally represented by the following approximation,

$$P_{dynamic} = \alpha . C_{Load} . V_{dd}^{2} . f_{clk}$$

where'α' is the switching activity factor (also called transition probability) and it tends to increase as the need for bandwidth increases, 'C_{Load}' is the overall capacitance to be charged and discharged in a reference clock cycle.

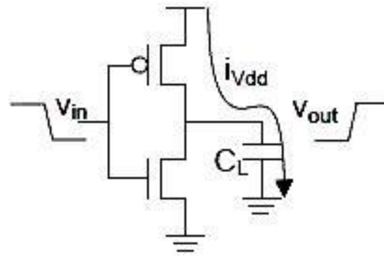


Fig 2.3 Dynamic switching power

The power dissipation that results from switching activity proves to be the dominant component for technology processes having feature size greater than 1um [6]. The minimum dimension of a transistor that can be unfailingly manufactured is denoted by the feature size of a CMOS manufacturing process. With maturation of technology processes toward the deep-submicron and nanotech regime, the feature sizes of the transistors are getting reduced, and consequently reducing the load capacitances. Figure 2.4 shows the feature sizes for different process generations [4]. The reduction in feature size puts a constraint on supply voltage to avoid high electric field effects and hence forces its reduction. The voltage scaling technique taking the prominent benefit of the quadratic dependence of switching power on supply voltage contributes to dynamic power savings. It can be concluded that with reduction in feature size dynamic power dissipation is losing its dominance due to minimisation of parasitic capacitances and supply voltage.

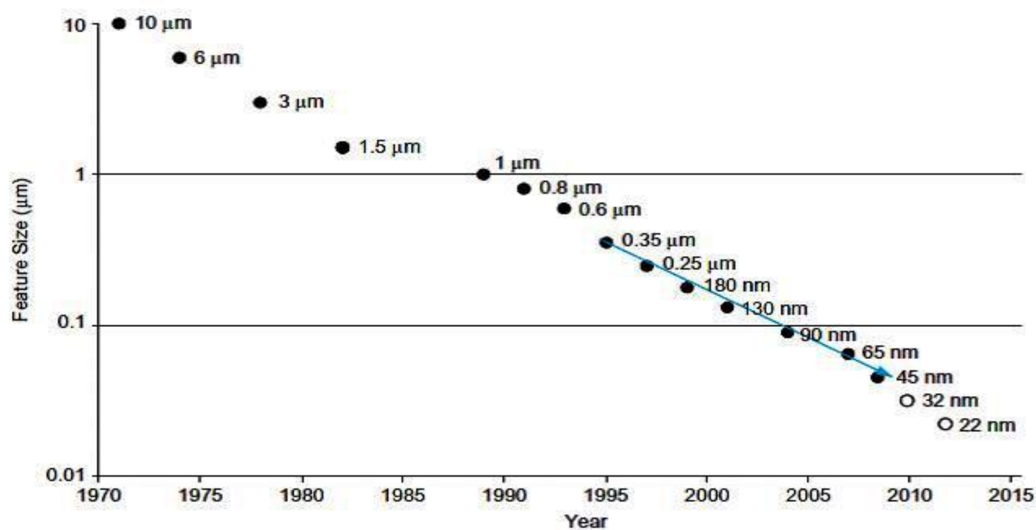


Fig 2.4 Process generations [13]

2.2.3 Leakage Power: A small amount of current is leaked even when transistors are supposedly OFF. Different leakage mechanisms comprise subthreshold conduction between source and drain, gate leakage from the gate to body, and junction leakage from source to body and drain to body, as shown in Fig 2.5. Thermal emission of carriers over the potential barrier set by the threshold causes subthreshold conduction. Tunnelling of charge carriers through the extremely thin gate dielectric causes a quantum mechanical effect called gate leakage. Junction leakage is the result of current through the reverse biased p-n junctions between the source/drain diffusions and the body. In technology with feature sizes greater than 180 nm, leakage was typically insignificant except in very low power applications. For 90 and 65 nm technologies, threshold voltage got reduced to the level that subthreshold leakage is raised from the levels of 1s to 10s of nA per transistor, which becomes significant when collectively seen for millions or billions of transistors on a chip. For 45 nm process technology, oxide thickness gets reduced to the extent that gate leakage becomes comparable to subthreshold leakage. Gate leakage can be reduced if high-k gate dielectrics are employed. On the whole, leakage has become a significant design concern in deep sub-micron and nanometre processes [3].

Leakage power also increases with increasing die area which means an increase in transistor count over the chip indicating the multiplication of leakage current.

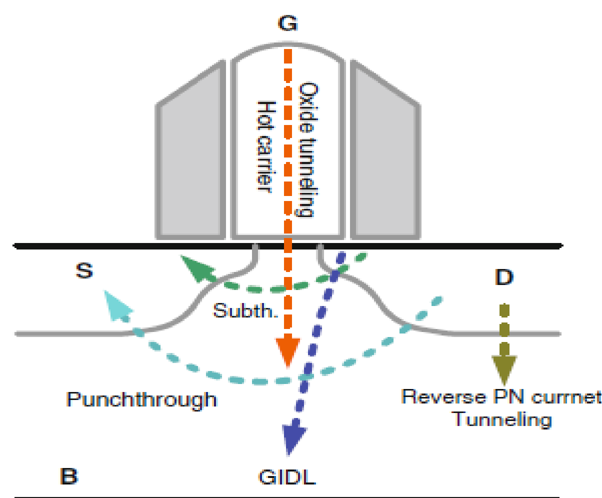


Fig 2.5 Leakage current components in an NMOS transistor.

Major Components of Leakage Power Dissipation

The four major sources of leakage current flow in a MOS transistor are:
i. Reverse-biased junction leakage current (I_{REV})
ii. Gate induced drain leakage (I_{GIDL})
iii. Gate direct-tunnelling leakage (I_G)
iv. Subthreshold (weak inversion) leakage (I_{SUB})
which are discussed below.

i. Reverse-biased junction leakage current (*IREV*)

The reverse biased *junction leakage* current originates from the source or drain to the substrate through the reverse biased diodes formed between source/drain and substrate when a transistor is OFF. For instance, considering the case of an inverter with logic low input voltage, NMOS turns OFF, the PMOS turns ON, and the output voltage is logic high. Consequently, the drain-to-substrate voltage of the NMOS which is OFF transistor is equal to the supply voltage. As a result of it leakage current flows from the drain to the substrate through the reverse-biased diode (junction). The diode's leakage current magnitude depends on the drain diffusion area and the leakage current density, which is decided by the concentration of doping. The p-n junction leakage is dominated by band-to-band tunnelling (BTBT) if both n and p regions are heavily doped [7]. Junction reverse-bias leakage components are usually insignificant relating to the other three leakage components.

ii. Gate-Induced Drain Leakage

High field effect in the drain junction of MOS transistors causes gate induced drain leakage (GIDL). For an NMOS transistor having gate at ground potential and drain at VDD potential, band bending takes place in the drain which is very significant and allows electron-hole pair generation through avalanche multiplication and band-to-band tunnelling. A deep depletion condition arises as the holes are swiftly swept out to the substrate and simultaneously electrons get collected by the drain which results in GIDL current. This leakage mechanism even worsens by high drain to body voltage and high drain to gate voltage. Transistor scaling leads to progressively sharp halo implants, where the substrate doping at the junction interfaces is made higher, whereas the channel doping is kept low. This has been done primarily to avoid or control punch-through and drain-induced barrier lowering while having a very less effect on the carrier mobility in the channel. BTBT currents are increased as a result of steep doping profile at the drain edge, particularly as VDB is increased. GIDL current gets increased with thinner oxide and higher supply voltage [8].

iii. Gate Direct Tunnelling Leakage

The current flowing from the gate through the "leaky" oxide insulation to the substrate is the gate leakage current. For low Si-oxide thicknesses (typically in 0.15um and even lower technology nodes), leading effect causing gate leakage is the direct tunnelling through the silicon oxide layer due to high electric field across the gate substrate for a high potential difference . There are several Mechanisms for direct tunnelling which include electron tunnelling in the conduction band (ECB), electron tunnelling in the valence band (EVB), and hole tunnelling in the valence band (HVB) and among all ECB proves to be the dominant one. The amount of the *gate direct tunnelling current gets* increased exponentially with the decrease in gate oxide thickness T_{ox} and increase in supply voltage V_{DD}. As a fact, for comparatively thin oxide thicknesses (of the order 2-3 nm), at a gate to source voltage (V_{GS}) of 1V, every 0.2nm reduction in T_{ox} results in a tenfold increase in gate leakage current I_G [8]. It should be noted that the gate leakage for a NMOS device is

typically one order of magnitude higher than that of an PMOS device having identical T_{ox} and V_{DD} when using SiO_2 as the gate dielectric. To maintain effective gate control over the channel region gate oxide thickness must also be reduced as transistor length and supply voltage are scaled down. As a consequence of it there is an exponential upsurge in the gate leakage due to direct tunnelling of electrons through the gate oxide [8]. An effective method to combat the gate leakage currents and maintaining excellent gate control as well is the replacement of the now used silicon dioxide gate insulator with high-K dielectric material such as TiO_2 and Ta_2O_5.

iv. Subthreshold (weak inversion) leakage (*I_{SUB}*)

There is a current flow between source and drain region in a MOS transistor when gate voltage, V_{GS} is below the threshold voltage, V_{TH} of the MOS transistor which is known as Subthreshold or weak inversion conduction current. It results due to the minority carrier drift from the drain to the source region through the channel in weak inversion region. The flow of subthreshold leakage current in an NMOS transistor has been shown in fig 2.6[5], when V_{GS} is less than V_{TH} of the transistor. The minority carriers' concentration in weak inversion region is rather small, but not actually zero. Subthreshold leakage power has become dominant among other leakage power components because of the inevitability to use low threshold voltage transistors in order to maintain the desired speed of the device. New and improved circuit design techniques should be devised to minimise this leakage power which is undesirable in digital circuit design.

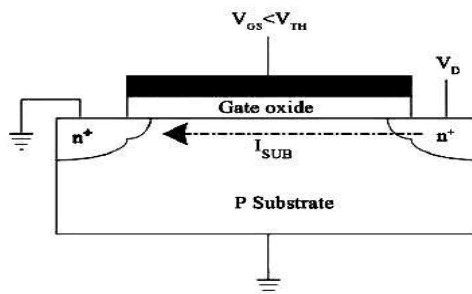


Fig 2.6 Subthreshold leakage current in an NMOS transistor [5]

According to BSIM4 MOSFET model, the equation governing this subthreshold leakage current [5] can be expressed as

$$I_{SUB}=I_0 e^{\frac{VGS-VTH0-\eta VDS+\gamma VBS}{nVT}}\left\{1-e^{\frac{-VDS}{VT}}\right\}\text{.........................(1.1)}$$

where,

$$I_o = \mu C_{ox}\left(\frac{W}{L}\right)V_T^2 e^{1.8} \text{ and } V_T = \frac{KT}{q}$$

Here VGS, VDS and VBS are the gate to source, drain to source, and bulk to source voltages respectively, μ denotes the carrier mobility, Cox is the gate oxide capacitance per

unit area, W and L denote the channel width and channel length of the transistor, K is the Boltzmann constant, T is the absolute temperature, q is the electrical charge of an electron, VT is the thermal voltage, VTH0 is the zero biased threshold voltage, γ is body effect coefficient, η denotes the drain induced barrier lowering coefficient, and n is the subthreshold swing coefficient. Table 2.1 [9] shows the dependence of subthreshold leakage current on MOS device parameters. Increasing the threshold voltage of the MOS transistor is an effective way to reduce sub- threshold leakage power dissipation.

TABLE 2.1 [9]
DEPENDENCE OF SUBTHRESHOLD LEAKAGE CURRENT ON MOS TRANSISTOR PARAMETERS.

TRANSISTOR PARAMETER	DEPENDENCE OF SUBTHRESHOLD LEAKAGE
Transistor width (W)	Directly proportional
Transistor length (L)	Inversely proportional
Temperature (T)	Exponential increase
Transistor threshold voltage (VTH)	Increases by an order of magnitude with 100 mV decrease
Input voltage (VGS)	Exponential increase

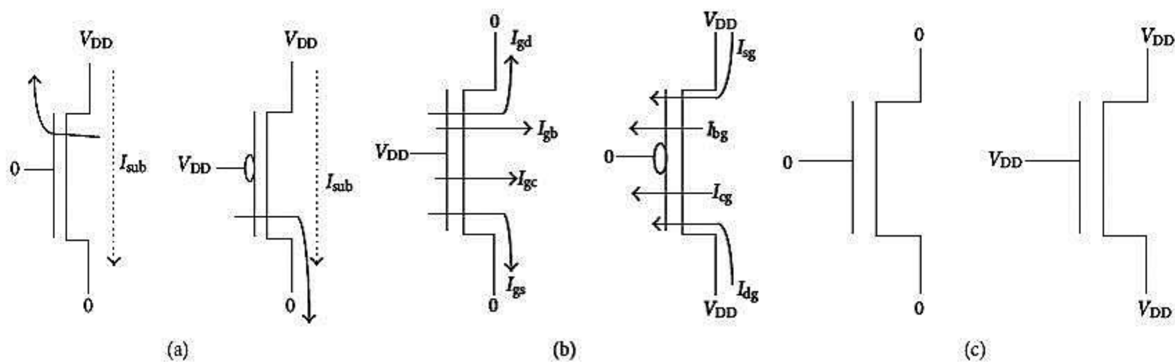


Fig 2.7 (a)Maximum subthreshold leakage current state. (b)Maximum gate oxide leakage current state. (c)Condition to avoid both subthreshold and gate oxide leakage current[10]

2.3 LEAKAGE REDUCTION TECHNIQUES

Continuous scaling down of CMOS technology has made leakage power comparable to dynamic switching power. Threshold voltage of transistors needs to be adjusted in digital circuits design for maximum saving in the leakage power dissipation while maintaining the desirable performance. To counteract the excessive leakage in CMOS circuit, many

architectural techniques have been proposed over the years which achieve a significant saving in subthreshold leakage.

Various leakage power reduction techniques have been discussed below briefly:

2.3.1 Power Gating (Sleep Approach) with MTCMOS: Sleep transistor technique [11] is the most widely known and conventional approach to achieve efficient leakage regulation in CMOS circuits. Sleep approach does two small changes in the basic circuitry of CMOS circuit (i) placement of an additional "sleep" PMOS transistor between power supply (V_{dd}) and the pull-up network of a circuit and (ii) placement of an additional "sleep" NMOS transistor between the pull-down network and Gnd.

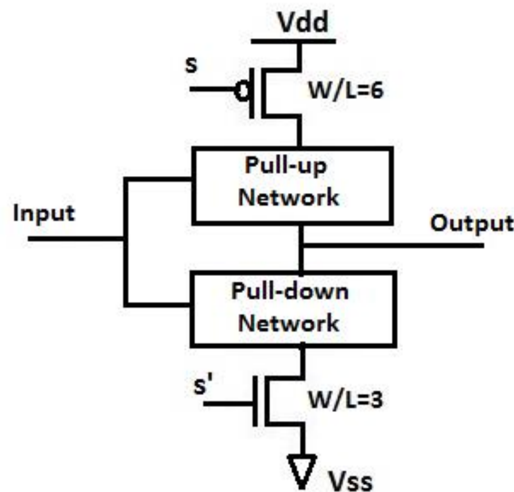


Fig 2.8 Sleep Approach

In standby mode when the circuit is sitting idle and is not supposed to work these sleep transistors turn off the circuit by cutting off the power rails. The circuit loses its connection from ground and V_{dd}. The structure is shown in Fig 2.8 where transistors with input S and S' are sleep transistors. The sleep transistors are turned on when the circuit is active so that PUN is transparently connected to V_{dd} through PMOS sleep transistor and PDN is connected to ground through NMOS sleep transistor so that normal operation takes place. And when the circuit is idle, the sleep transistors are turned-off. The power cut-off done by sleep transistor approach can reduce leakage power effectively. However, sleep technique results in some worth noticing drawback which are output destruction of state plus a floating output voltage after sleep mode. State-destructive techniques use sleep transistor to achieve cutting off of transistor (pull-up or pull-down or both) networks from supply voltage or ground. These techniques are also known as gated-V_{dd} and gated- Gnd. Sleep transistors used are usually having high Vth to achieve effective leakage reduction. This technique is MTCMOS where sleep transistors are made high Vth while for maintaining fast switching speeds, transistors used in logic design are low-Vth. High Vth transistors suppress leakage manifold as compared to low Vth ones. Moreover, the state loss and floating values of the pull-up and pull-down networks during sleep mode has a

significant impact on the wake up time and energy of the sleep technique because of the necessity to recharge transistors which suffered state loss during sleep.

2.3.2 Zigzag Approach: One of the drawbacks of sleep technique was the floating state of output in sleep mode due to loss of connection from both V_{dd} and ground. The zigzag technique [11] shown in fig 2.9 is somewhat similar to sleep technique except it uses only one sleep transistor in each logic stage either in the pull-up or pull-down network depending upon a particular input pattern. Input pattern is a data vector which can achieve the lowest possible leakage power consumption for the concerned circuit. Sleep transistor is assigned to the pull-down network if the output of the circuit for the input vector corresponding to the lowest power is "1" so that the output node remains connected to V_{dd} in sleep mode or else sleep transistor is assigned to the pull-up network if the output is "0" so that the output node remains connected to ground rail in sleep mode. For Fig 2.9, we have assumed that the output of the first stage turns out to be "1" and the output of the second stage turns out to be "0" when there is an assertion of minimum leakage inputs. Therefore, we insert a pull-down sleep transistor for the first stage between PDN and ground and a pull-up sleep transistor for the second stage between power supply and ground. Like the sleep transistor technique, here also size of the sleep transistors is determined by the size of the largest transistor in the network (pull-up or pull-down) connected to the sleep transistor. The configuration can be made dual-Vth with high-Vth transistors being used as are the sleep transistors and others as low Vth. The zigzag technique has been introduced in order to reduce the wake-up cost of the sleep transistor technique. The wake-up overhead is reduced by the zigzag technique by picking a particular circuit state (e.g., corresponding to a "reset") and then, for the specific circuit state chosen, the pull-down network for each gate whose output is high is turned off while on the other hand the pull-up network for each gate whose output is low are turned off. Henceforth the application of predetermined input pattern corresponding to lowest power dissipation, prior going to sleep, which directs the circuit output in sleep mode to some reset value and thus preventing the floating output problem.

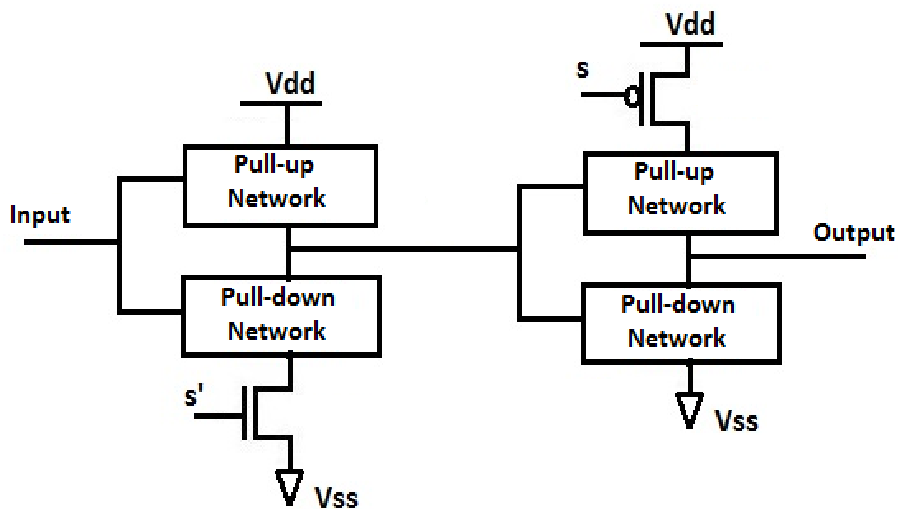


Fig 2.9 Zigzag Approach

2.3.3 Forced Stack Approach: It has been observed that **"**a state with more than one transistor OFF in a path from supply voltage to ground is far less leaky than a state with only one transistor OFF in any supply to ground path"[9]. Another conventional technique to achieve leakage power reduction is the stacking of transistors approach. Stack effect or we can say Self-Reverse bias effect is the phenomenon where subthreshold leakage current diminishes due to series connection of two or more turned off transistors in the path from V_{dd} to ground. The process of stacking of transistor is done by replacement of transistor of width W with two series connected transistors of width W/2 thus maintaining equivalent input capacitance [12]. Two input NAND gate is an example of natural stacking of NMOS transistors in pull down network as shown in Fig.2.10. Suppose both NMOS transistors Q1 and Q2 are off corresponding to some input, then the intermediate node voltage, VQ is at a non-zero value due to the presence of a small drain current because of leakage. However, divided transistors adversely lead to increase in the delay and could impose a limitation on the usefulness of the approach.

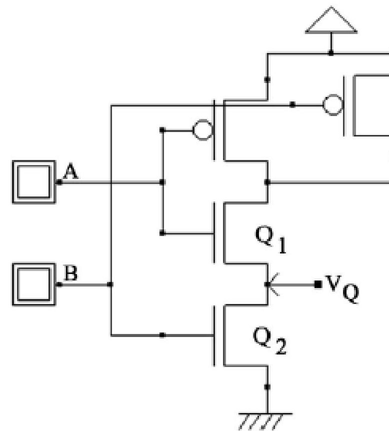


Fig 2.10 Natural stacking of NMOS transistors in a two input NAND gate [5]

There are certain effects [5] of Positive potential Q at the intermediate node between two turned off stacked transistors which are discussed below:
1) VS for Q1 is positive, therefore VGS of Q1 becomes negative;
2) VBS of Q1 becomes negative, consequently causing a rise in threshold voltage of Q1 as body effect for Q1 comes in picture (relatively higher threshold transistor reduces leakage effectively);
3) VDS of Q1 decreases, which favourably aids in lessening the drain induced barrier lowering.
From the expression of subthreshold leakage current in chapter one, it can be observed that a negative VGS, an increase in the body effect (negative VBS), and a reduction in VDS (less drain induced barrier lowering) collectively reduce the subthreshold leakage current exponentially in standby mode.
Basic idea of the stacking approach for a generalised CMOS circuit is shown below in Fig2.11 where each of the transistors in PDN and PUN is replaced by two half sized transistors. From above discussion it can be inferred that stacking is an effective technique

which reduces leakage by increasing the effective threshold voltage of the stacked transistors but it has a serious drawback of delay overhead due to decrease in effective aspect ratio and due to the increased resistance offered by now two transistors in series rather than one. One of the advantages of stacking over sleep technique is that it is state saving.

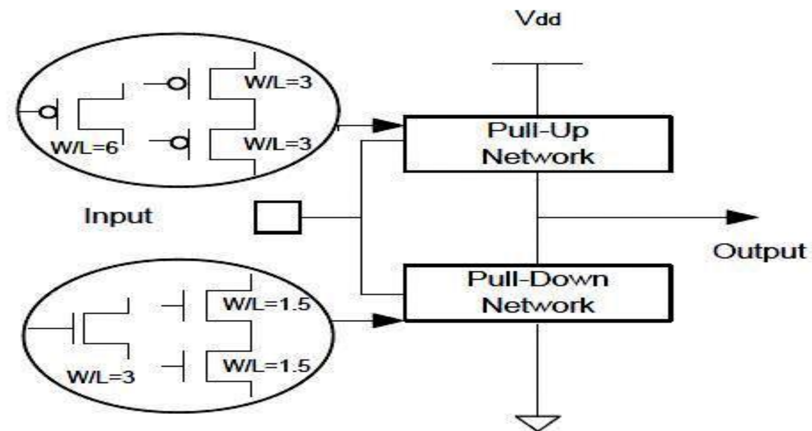


Fig 2.11 Stack Approach [11]

2.3.4 Sleepy Stack Approach: The sleepy stack structure is basically a combination of structure of the forced stack and the sleep transistor techniques. The sleepy stack technique involves splitting up of existing transistors into two half size transistors similar to the stack technique. Then sleepy stack is finally obtained by addition of sleep transistors in parallel to one of the divided transistors. The structure is shown in fig 2.12. The sleep transistors of the sleepy stack have similar operation as that of the sleep transistors used in the sleep transistor technique in which sleep transistors turn on during active mode and turn off during sleep mode. This sleepy stack structure potentially cuts down circuit's delay in two possible ways. First, since the sleep transistors remain always on during active mode, the sleepy stack structure manages to have speedier switching time than the forced stack structure; the drain and source of each sleep transistor are virtually connected since sleep transistors remain on in active mode so, the value of voltage at the sleep transistor source is always readily existing at the sleep transistor drain, and thus, current flow can be immediately achieved to the low-Vth transistors which are connected to the gate output irrespective of the status of each transistor in parallel to the sleep transistors.

While in sleep mode, sleep transistors remain turned off and stacked transistors accomplish leakage current suppression along with state retention. Even though the sleep transistors are in off state, the sleepy stack structure preserves the exact logic state. The leakage reduction by sleepy stack structure is attained in two ways. First, leakage power is diminished by high-Vth sleep transistors and the transistors parallel to the sleep transistors. Second, series of stacked turned off transistors prompt the stack effect, which also causes

suppression of leakage power consumption. A reduction in delay during active mode is achieved due to reduced resistance of the path offered because of parallel arrangement of each sleep transistor to one of the stacked transistors [12]. However, area penalty to be paid for this approach is a noteworthy matter since each transistor has to be replaced by three transistors and extra controls wires are to be added for S and S'', which are sleep signals**.**

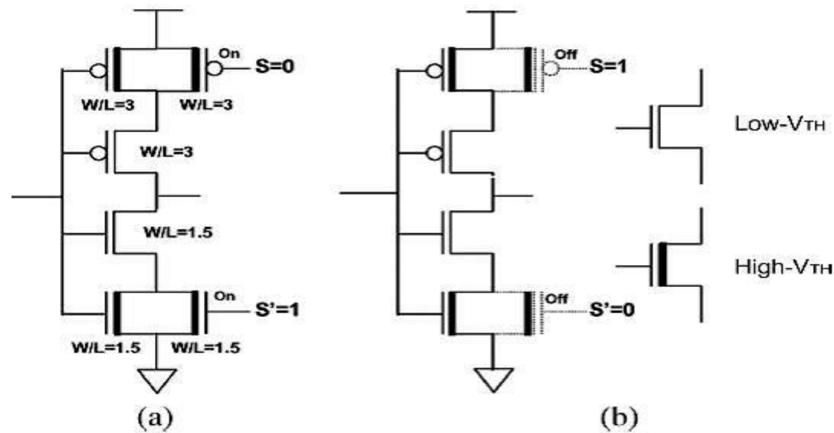


Fig 2.12 (a) Sleepy stack inverter with W=L of each transistor and active mode S, S' assertion. (b) Sleep mode S, S' assertion [12]

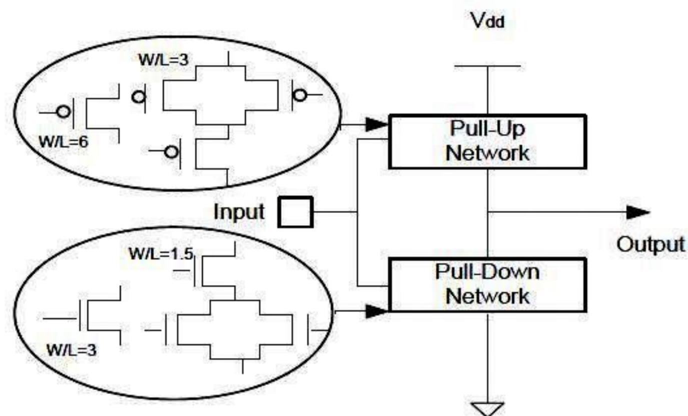


Fig 2.13 Sleepy Stack Approach for general CMOS circuit [11]

RC equivalent circuits for both forced stack and sleepy stack are shown below in Fig 2.14 and Fig 2.9 respectively. We can observe from the figures below that resistance experienced by the current in forced stack is $4R_1$ for either side i.e. from Vdd to output node or output node to ground whereas for sleepy stack when same path resistance observed it comes out to be $3R_1$ due to parallel combination of sleep transistor and one of the stacked transistors. This lower resistance through the path in sleepy stack enables the designer to use high Vth for sleep transistors as well as one of the stacked transistors parallel to it thereby achieving higher leakage suppression having the same performance.

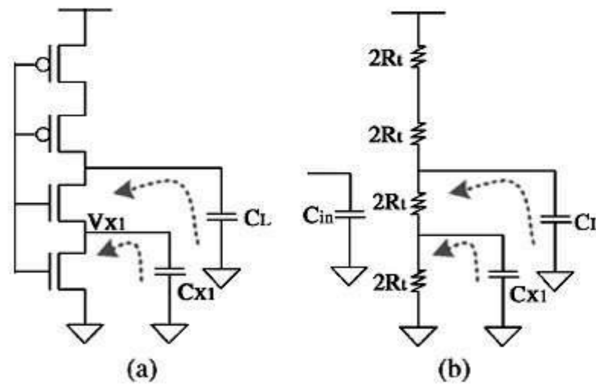


Fig 2.14 (a) Forced stack technique inverter circuit schematic. (b) RC equivalent circuit [12]

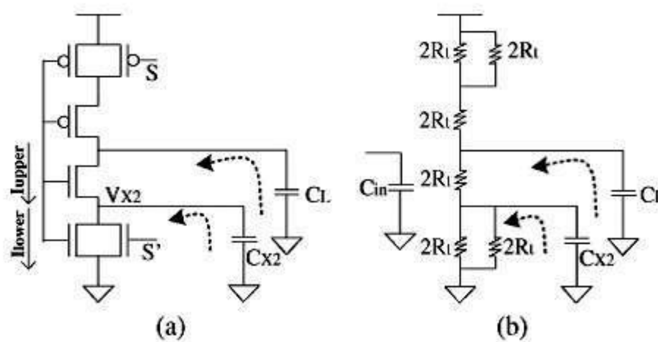


Fig 2.15 (a) Sleepy stack technique inverter schematic. (b) RC equivalent circuit [12]

2.3.5 Leakage Feedback Approach: The leakage feedback technique is typically based on the sleep approach except the fact that leakage feedback approach makes use of two additional transistors to preserve the logic state during sleep mode, and the output of an inverter drives the two transistors which is in turn driven by output of the circuit implemented utilizing leakage feedback [11]. As shown in Fig 2.16,there is a PMOS transistor placed in parallel to the sleep transistor (S) in PUN and a NMOS transistor which is placed parallel to the sleep transistor (S') in PDN. These two transistors are being driven by the output of the inverter which is in turn being driven by the output of the implemented logic circuit. So while the circuit is in sleep mode, sleep transistors get turned off but one of the transistors in parallel to the sleep transistors either in PDN or PUN maintains the connection with the apt power rail to retain the exact logic. Dual Vth (multi threshold) technology can be applied for the sleep, zigzag, sleepy stack and leakage feedback approaches to gain higher leakage power reduction. High-Vth results in less leakage but lowers performance. Therefore high Vth is used just for sleep transistors and logic design transistors are kept low Vth to maintain the performance.

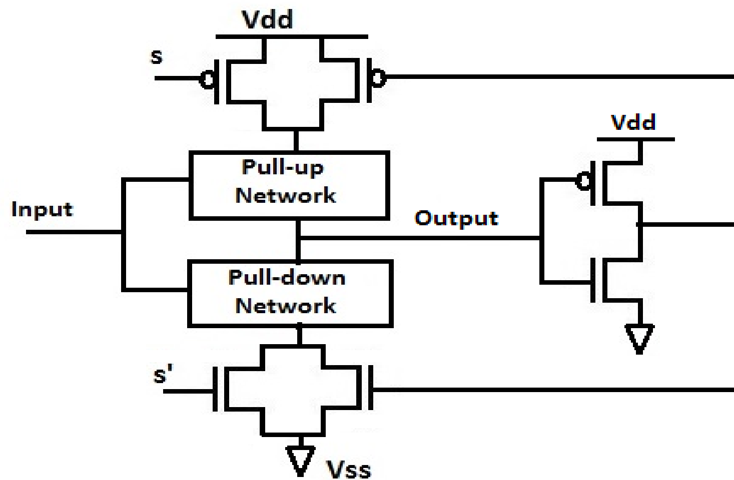


Fig 2.16 Leakage feedback approach

2.3.6 Sleepy Keeper Approach: Sleepy keeper [11] is basically a modification of leakage feedback technique. The structure of sleepy keeper as shown in Fig 2.17 is same as that of leakage feedback except that the inverter is not used at the output node to feed inverted output to the state retaining transistors instead PMOS parallel to PMOS sleep transistor in PUN is replaced by an NMOS and NMOS parallel to NMOS sleep transistor in PDN is replaced by a PMOS transistor. So when the output logic state just before going to sleep mode is '1', NMOS parallel to PMOS sleep transistor driven by the output turns on and output node is maintained at logic high state in sleep mode. Similarly when output is zero, PMOS parallel to NMOS sleep transistor turns on and connects the output node to ground to retain the logic in sleep mode. Hence the state is preserved in sleepy keeper along with effective leakage power reduction.

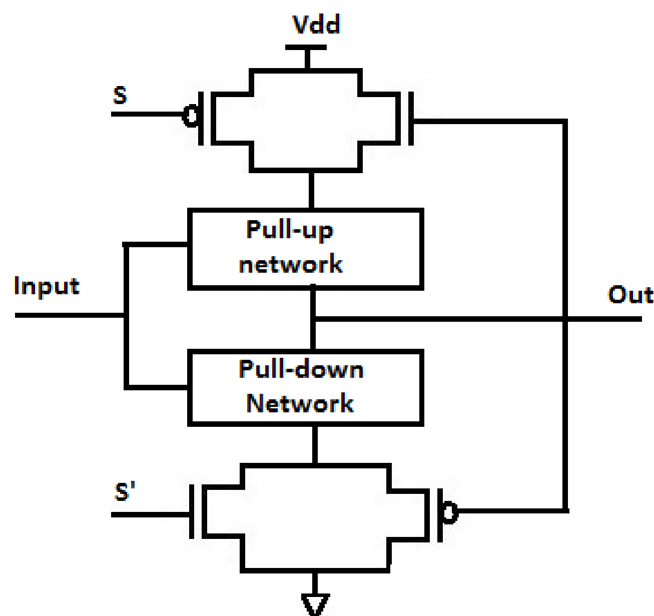


Fig 2.17 Sleepy Keeper Approach

2.3.7 LECTOR Technique: The basic concept behind LECTOR technique for minimising leakage currents achieving effective stacking of transistors in the path from V_{dd} to ground. Above approach is based on the observation that "a circuit state with more than one turned OFF transistor in a path from supply voltage to ground is much less leakier than a circuit state with only one OFF transistor in any supply to ground path [9]".

LECTOR introduces two leakage control transistors (a PMOS and a NMOS) in between the PUN and PDN of the logic gate where the gate terminal of each of the leakage control transistor (LCT) is controlled by the source of the other. This arrangement ensures that one of the LCTs is always in "near cut-off region" for any possible input combination. This results in effective increase in the resistance of the path from V_{DD} to ground, leading to substantial drop in leakage currents through the path [6]. The most noteworthy feature of LECTOR is that it manages to have leakage suppression in both active and idle states of the circuit effectively. Making LCTs high Vth contributes in achieving much more leakage control as high Vth transistors are far less leaky that low Vth transistors. This approach can be called as "dual Vth LECTOR technique".

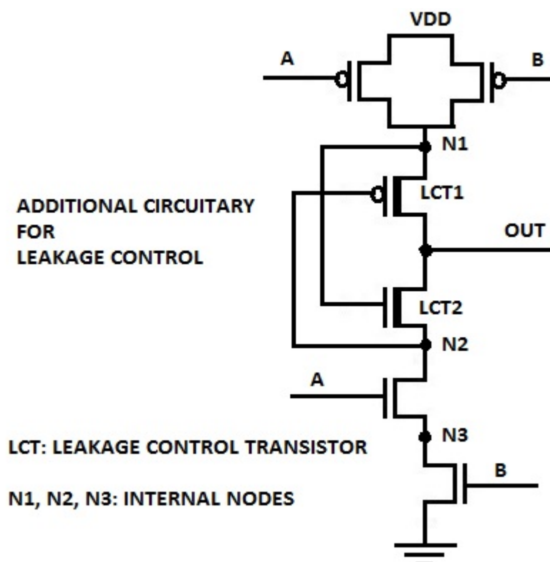


Fig 2.18 Lector Technique Implementing NAND GATE

A CMOS NAND gate with the addition of two leakage control transistors LCT1 and LCT2 is shown in fig 2.18. Consider inputs (A, B) = (1, 0), M1 and M4 are turned OFF; M2 and M3 are turned ON. Status of LCT1 and LCT2 is determined by the voltages at nodes N1, N2, Out and N3. For input combination (1, 0) N1 is at VDD since M2 is on and PMOS passes strong VDD. Similarly LCT1 which is a PMOS passes good VDD to Output node so that Out is raised to VDD as well. LCT2 is an NMOS therefore it passes weak VDD and hence node N2 is at voltage VDD-Vth. Now voltage at node N2 (source voltage of LCT2) drives the gate of LCT1. VSG=Vth for LCT1 but the transistor is in "near cut-off" state because of no voltage difference between its drain (node N1) and source (output node). Similarly the voltage at node N1 (source voltage of LCT1) drives the gate of LCT2. LCT2 turns on as its VGS=Vth and VDS is also equal to Vth so there is a potential difference to allow current to flow through it turning it ON comfortably. Circuit can

analysed for other input combinations in the similar manner. Table 2.2[6] shown below gives the status of all the transistors for different input combinations.

TABLE 2.2 [6]
STATE MATRIX OF TWO-INPUT LCT NAND GATE

TRANSISTOR REFERENCE	INPUT VECTOR-(A_{in}, B_{in})			
	(0,0)	(0,1)	(1,0)	(1,1)
M_1	On state	On state	Off state	Off state
M_2	On state	Off state	On state	Off state
LCT_1	Near cut-Off state	Near cut-Off state	Near cut-Off state	On state
LCT_2	On state	On state	On state	Near cut-Off state
M_3	Off state	Off state	On state	On state
M_4	Off state	On state	Off state	On state

It can be very apparently observed from Table 2.2 that one of the leakage control transistor is always in near cut-off state. This cuts down the leakage by increasing resistance through the path.

2.3.8 GALEOR Technique:

GALEOR technique [13] has the exactly same structure as that of LECTOR except the fact that the locations of extra leakage control transistors (also known as Gated Leakage Transistors (GLTs)) are swapped. N-type GLT is placed between pull-up network and output and P-type GLT is placed between pull-down network and output. GLTs are usually made high Vth. GALEOR is also a self-controlled technique like LECTOR but has a limitation of one Vth drop in the logic high output and one Vth rise in logic low output.

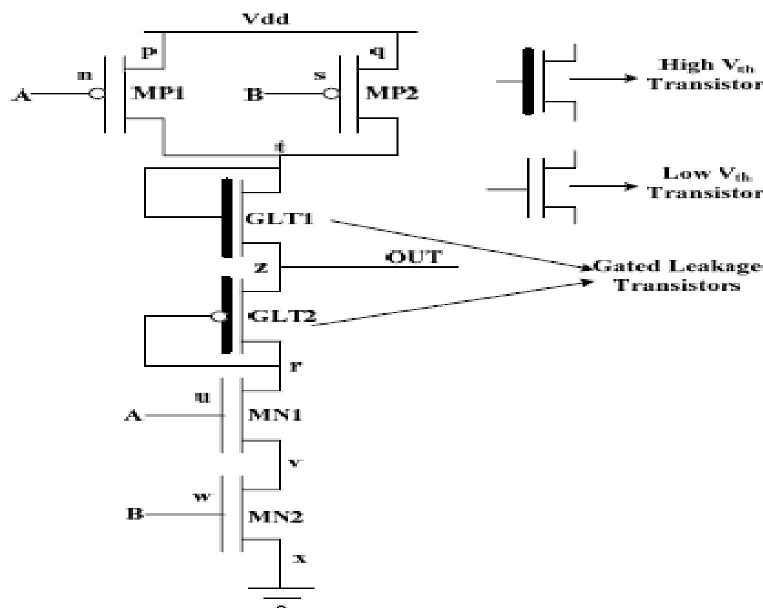


Fig 2.19 GALEOR Technique Implementing NAND Gate [13]

2.4 COMPARISON OF VARIOUS TECHNIQUES

TECHNIQUE	ADVANTAGES	DISADVANTAGES
• **Sleep transistor Approach (power gating)**	• drastic reduction in leakage current due isolation from power supply in sleep mode	• Additional signal required to drive sleep transistors • Area and delay increased due to sleep transistors • Unknown floating state in sleep mode • High wake up time • Energy requirement to recharge lost state
• **Zigzag technique**	• Circuit doesn't go into unknown state as connection is maintained either with Vdd or ground even in sleep mode. • Wake up cost reduced	• Area and delay increased due to sleep transistors • Actual state still lost
• **Leakage feedback And Sleepy keeper Technique**	• Actual state preserved	• Additional circuitry is needed to monitor the circuit state and control sleep transistors despite the fact that the circuit is in idle state
• **Forced stack**	• Actual state preserved	• every transistor is replaced by two transistors • Higher delay due to increase in resistance
• **Sleepy stack**	• Higher reduction in leakage current than forced stack • state retention with smaller delay	• Area penalty is a significant matter for this approach since every transistor is replaced by three transistors • additional wires are added for Sleep control signal
• **LECTOR and GALEOR**	• Self-controlled • No additional circuitry required to control the LCTs and GLTs. • Less area ,less power consumption	• Vth drop in logic high output signal ($V_{high}=V_{dd}-V_{th}$) and logic Low output signal is Vth higher than ground level ($V_{low}=V_{th}$) for GALEOR. • Slight increase in delay for both LECTOR and GALEOR.

2.5 SUMMARY

We can conclude from the above comparison table that maximum power saving is achieved in the case of sleep transistor approach but with a disadvantage of state loss and the need of external control signal (sleep signal). Forced stack provides reasonable power saving along with an advantage of state retention but increases the delay by breaking every transistor into half sized transistors and hence increasing the overall resistance of the path with significant transistor overhead. Sleepy stack technique somewhat tries to diminish the delay increased in forced stack by using high Vth sleep transistor in parallel to one of the stacked transistors which itself is taken as high Vth. Thus being able to use one of the transistors in stack as high Vth due to presence of parallel high Vth sleep transistors (parallel transistors reduce the resistance through the path thus using high Vth stack transistor would not affect delay much) further reduces the leakage current in addition stacking effect. Sleepy stack possess the same limitation of significant area and transistor count overhead along with the requirement of a sleep signal. Sleepy keeper is also a technique providing reasonable power saving along with state retention but still requires external signal to control the circuit. Finally we have a look at LECTOR technique which provides though low comparatively but sufficient leakage power saving has a lot of advantages which all the above techniques lack like state retention, low increase in delay, self-controlled (i.e. doesn't require external control signal to drive the circuit for leakage control) and requirement of only two extra stacked transistors for any circuit we wish to reduce leakage for. Thus, each technique has its own advantages and drawbacks. So it depends on our requirement which technique we use which suits the purpose best. Leakage increases with technology scaling hence the techniques will show even better performance efficiency as we move towards lower technology.

LECTOR proves to be an impressive approach for leakage regulation for logic circuits in terms of the advantages it offers, especially its self-controlled feature which makes it function efficiently both in active and standby mode. Leakage power loss aspect in DCVSL logic family and its variant configurations has been profoundly studied in the following chapters and careful application of LECTOR methodology has been done to achieve notable leakage power saving.

2.6 SIMULATION RESULTS AND DISCUSSIONS

Simulations have been performed here for CMOS inverter to ascertain the effectiveness of application of LECTOR technique to CMOS logic circuits with lowering down of technology, supply voltage variation and temperature variation.

CMOS INVERTER: Basic and LECTOR CMOS inverters as shown in fig.2.20 and fig.2.21 respectively were designed and simulated to authenticate the efficacy of LECTOR technique in leakage current reduction on application to basic CMOS inverter.

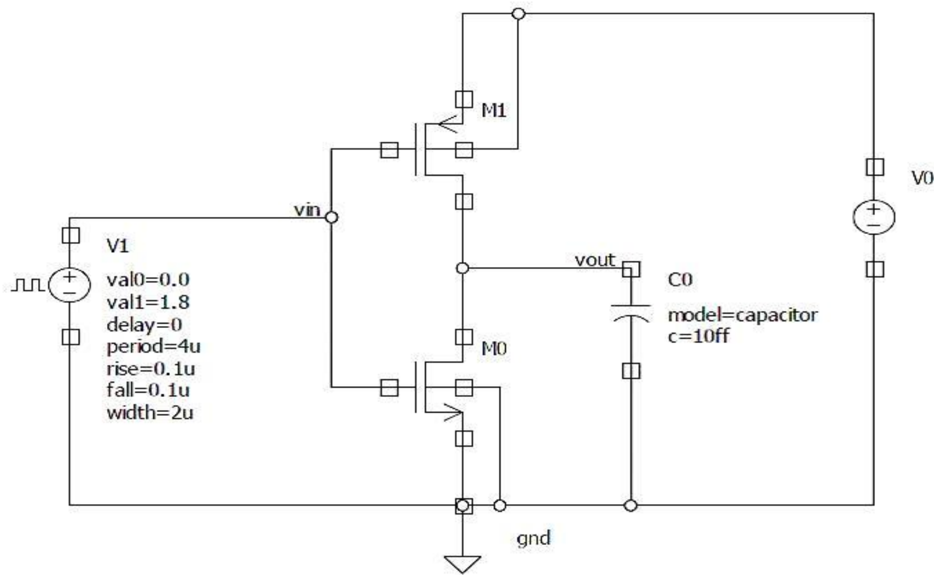


Fig. 2.20 Basic CMOS inverter

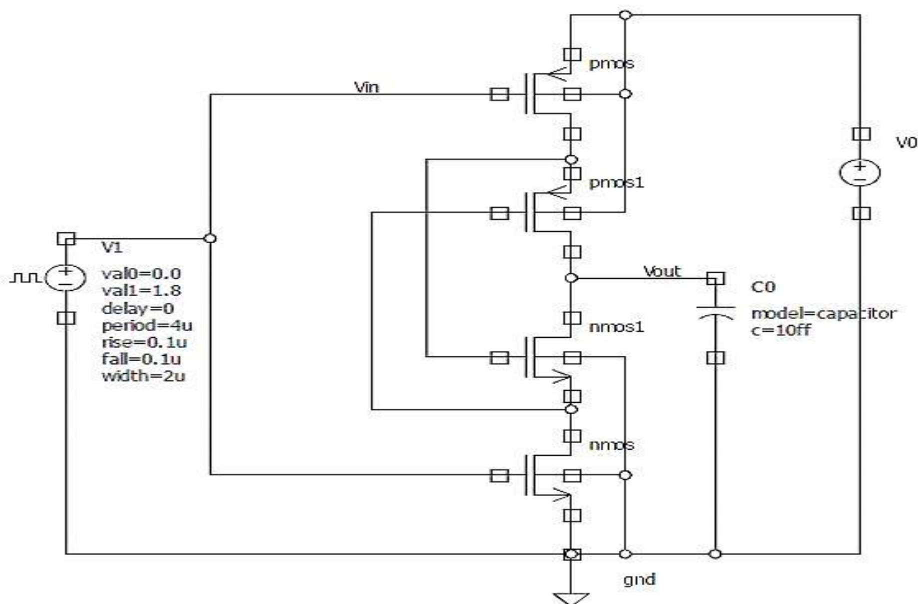


Fig. 2.21 LECTOR CMOS inverter

Table 2.3 given below shows the trend followed by leakage current with supply voltage and technology node variation. It can easily inferred from the table that for a given threshold voltage, leakage current decreases with decreases in operational supply voltage from 1.8V to 0.9V. Moreover, leakage current increases with scaling down of technology from 180nm to 45nm. One can observe that leakage effect is negligible for 180nm (in pA) and is predominant only below 180nm technology.

TABLE 2.3

BASIC CMOS INVERTER LEAKAGE CURRENT AT VARIOUS POWER SUPPLIES

Technology	Leakage current (nA) at Supply voltage		
	1.8V	**1.2V**	**0.9V**
180nm	0.172	-	-
90nm	30.52	3.73	1.69
65nm	64.70	5.13	1.96
45nm	154.74	8.74	2.56

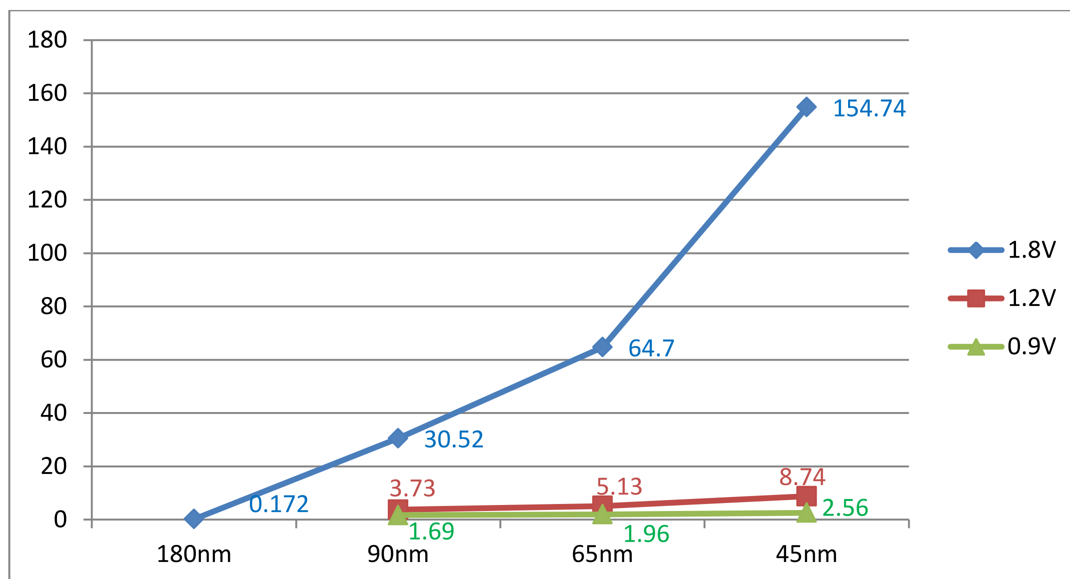


Fig. 2.22 Leakage current comparison for different supply voltages for basic DCVSL inverter

Figure 2.22 is a graphical comparison of leakage current for different voltage supplies and various technology nodes which evidently picturises the pattern followed in Table 2.3.

Leakage control transistors used in LECTOR technique can be made high Vth to achieve even more saving in leakage current. Table 2.4 shows leakage current for basic and LECTOR CMOS inverter at various technologies for VDD=1.8V. LECTOR technique with both high and standard Vth is considered and percentage saving is shown for both of them. High Vth LCTs achieve better saving by almost 12.8% taking an average of all technologies. It can be seen that maximum saving (almost 90%) is obtained for 45nm technology and minimum (around 60%) for 180nm. This shows that effectiveness of leakage control technique improves with each technology advancement towards lower node.

TABLE 2.4

LEAKAGE CURRENT MEASUREMENT FOR BASIC AND LECTOR CMOS INVERTER AT VDD=1.8

Technology	Leakage current(nA)				
	Basic	Lector		Percentage saving	
		Without high V_T	With high V_T	Without high V_T	With high V_T
180nm	0.172	0.096	0.070	43.76%	59.30%
90nm	30.52	6.92	5.61	77.32%	81.16%
65nm	64.70	9.25	7.42	85.70%	88.53%
45nm	154.74	18.8	14.09	87.80%	90.89%

Figure 2.3 graphically represents the leakage current reduction obtained by LECTOR technique when applied to basic inverter. High Vth LCTs in LECTOR provide better saving than standard Vth ones as shown in Table 2.4. Therefore, we'll consider high Vth LCTs for all the following discussions and proposed configurations.

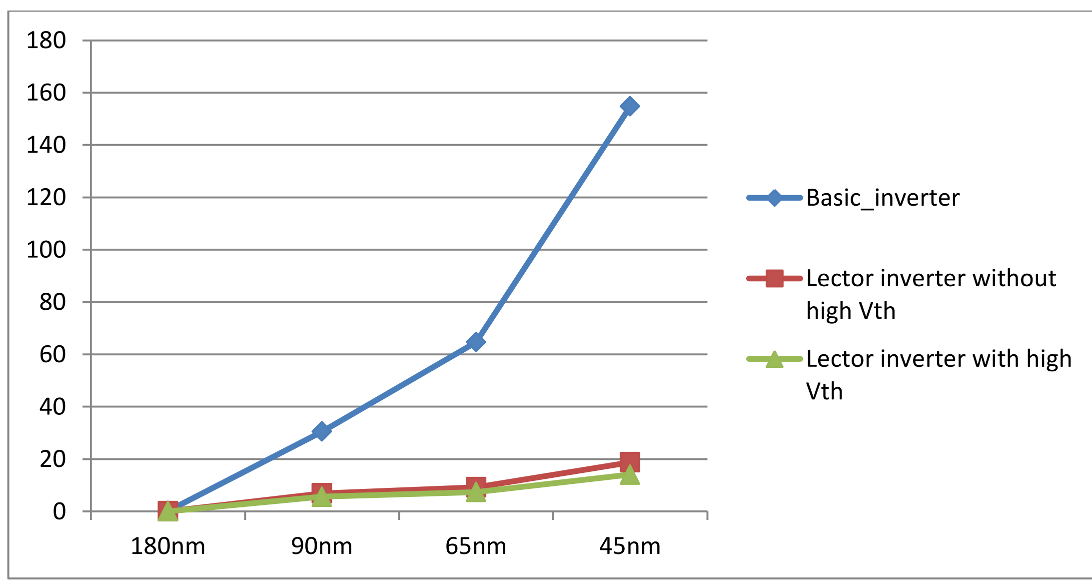


Fig. 2.23 Leakage current in CMOS inverter (in nA) at different technologies at 1.8V

Table 2.5 presents leakage current measurement for basic and LECTOR CMOS inverter at various technologies at VDD=1.2. An obvious cut down of leakage current corresponding to OFF states can be observed from VDD=1.8V to VDD=1.2V. Moreover, there is a drastic reduction in static current corresponding to ON states (i.e. when input=1 and inputs and outputs have stabilised after transition) as can be seen from the Table 2.5.

TABLE 2.5
LEAKAGE CURRENT MEASUREMENT FOR BASIC AND LECTOR CMOS INVERTER
AT VDD=1.2

Technology	Leakage current(nA)		
	Basic	Lector (With high V_T)	Percentage saving (With high V_T)
90nm	3.74	1.55	58.55%
65nm	5.13	1.69	67.05%
45nm	8.74	2.02	76.88%
	Static current		
90nm	6.04	2.16	64.23%
65nm	8.61	2.30	73.28%
45nm	16.50	2.51	84.78%

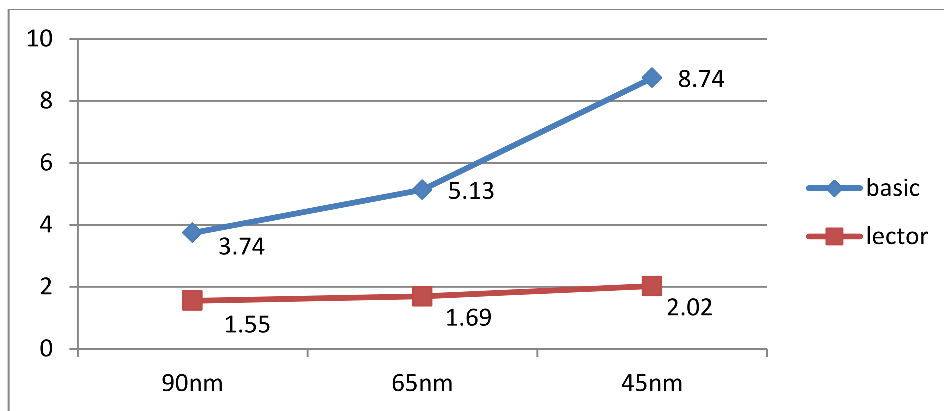


Fig. 2.24 Leakage current in CMOS inverter (in nA) at different technologies at 1.2V

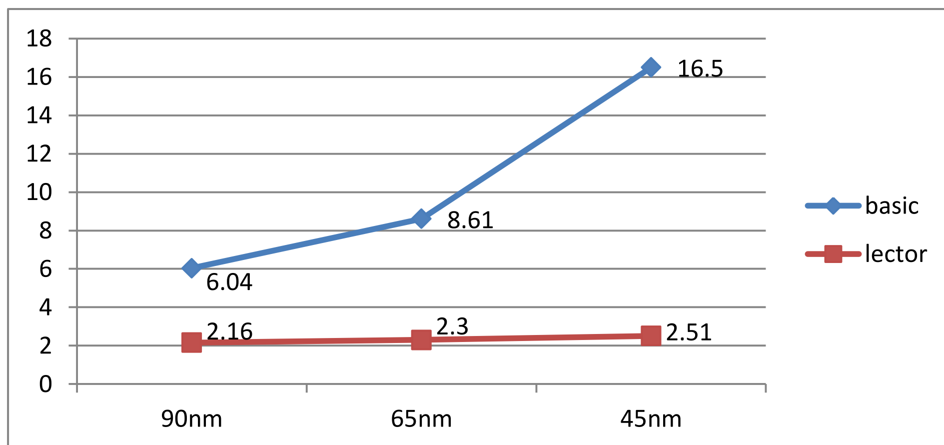


Fig. 2.25 Static current in CMOS inverter (in nA) at different technologies at 1.2V

Figure 2.24 and fig. 2.25 graphically represent leakage current and static current of CMOS inverter respectively at VDD=1.2. Reduction of leakage current achieved by LECTOR can be easily observed from the graph.

Temperature Variation for CMOS inverter has been performed at 45nm technology and power supply=1.2.

TABLE 2.6

TEMPERATURE VARIATION FOR CMOS INVERTER

Temperature	**Leakage current**	
	Basic	**Lector**
-25°C	3.16	0.587
27°C	8.74	2.02
100°C	23.96	6.95

The pattern followed in Table 2.6 verifies that leakage current increases with temperature. Leakage current is directly proportional to temperature.

Chapter 3

Leakage Power Reduction in Differential Cascode Voltage Switch Logic Family

3.1. INTRODUCTION

Design styles and logic family play a significant role in deciding the performance and efficiency of the circuit based on various design constraints like area, speed, cost, power dissipation, threshold and supply voltage scalability of the circuit**.** Several logic styles are existing and many are being proposed in an attempt to minimise the power consumption and enhance the performance of the logic. Differential cascode voltage switch logic (DCVSL) is a widely known logic design style. Implementation of CMOS random logic with DCVSL style proves to be advantageous over the conventional static CMOS logic design approach. Transistor count in CMOS logic to implement a 'N' input logic is '2N'. Subsequently, the number of transistors required to implement a complex logic would be immense. Ratioed logic style [14] was proposed as an alternative to decrease the required transistor count. However, ratioed logic suffers a major drawback of static power dissipation and reduced logic swing since pull up transistor is unconditionally on. Nonetheless, we can create a potential ratioed logic style that totally eliminates static currents and offers rail-to-rail swing. Above mentioned logic design style is a combination two concepts: *differential logic* and *positive feedback*. A differential gate receives complementary inputs and generates complementary outputs. Through feedback mechanism it is ensured that the load device gets turned off when not required. *Differential Cascode Voltage Switch Logic* (or DCVSL) is an example of such a logic family [14]. A lot of research on Leakage power reduction in CMOS logic approach has been undergone. But study on leakage power aspect of DCVSL family is somewhat limited till date. Therefore, an attempt has been made to explore the leakage power loss facet for DCVSL here in this thesis.

3.2. STATIC DCVSL

One of the earliest realization of static differential CMOS logic well-known as the differential cascode voltage switch logic was introduced in 1984 [15]. Logic function in DCVSL is implemented by using PDN only. As complementary pull-up network is not required, therefore reduction in parasitic capacitances at the output node provides a speedier response. In contrast to pseudo NMOS, static power loss is eliminated and rail to rail swing can be achieved.

3.2.1 Operation of DCVSL

The pull-down networks PDN1 and PDN2 are implemented using NMOS transistors only and are mutually exclusive (i.e. both are never on at the same time), such that the desired logic function and its complement are simultaneously realized. Initially assuming Out and Outbar at 1 and 0 respectively. When inputs are activated both PDN1 and PDN2 evaluate. Suppose input combination applied is such that PDN1 turns on and provides a discharge path to Out. Outbar which is at '0' initially is keeping M1 turned on. So there is a contention between M1 and PDN1 and Out is not able to discharge completely during this phase. Still discharging of Out starts yet at slower pace. As soon as Out falls below V_{DD} -$|V_{TP}|$, M2 turns on which is driven by Out. Now M2 provides a charging path to Outbar. Since PDN1 and PDN2 are mutually exclusive and implement differential logic functions. Therefore PDN2 is OFF and there is no discharge path for Outbar. Thus M2 successfully charges Outbar to $V_{DD.}$ As Outbar exceeds V_{DD}-$V_{T,}$ M1 turns off cutting the path between V_{DD} and ground and hence eliminating any static power loss. Now PDN1 can efficiently complete the discharge process for Out. Eventually both Out and Outbar attain correct logic state.

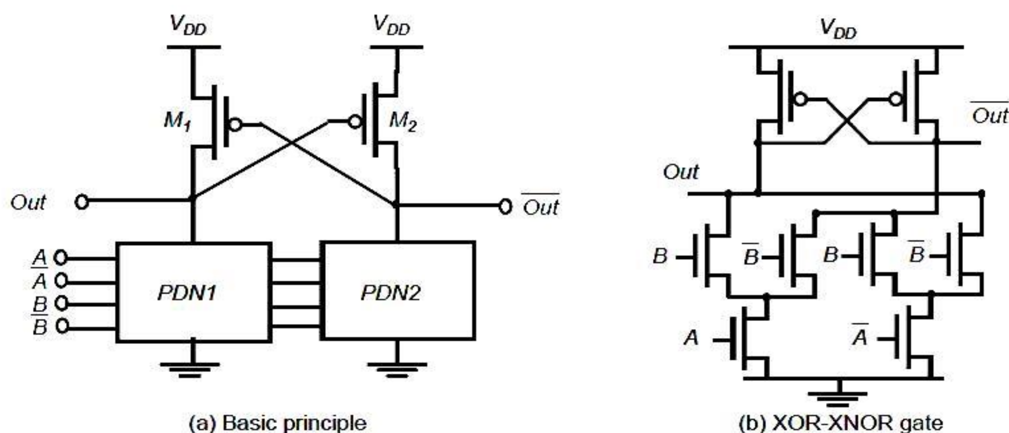


Fig.3.1. DCVSL logic gate

It should be noted that provision of sharing of the common transistors among the two differential pull-down networks when some complex logic function is realized lessens the implementation overhead. The resultant circuit shows a rail-to-rail swing, and there is an elimination of static power dissipation: in steady state, none of the stacked pull-down networks and load devices is in conduction mode simultaneously. However, the circuit is still ratioed logic since sizing of pull up transistors relatively to pull down devices critically affects the performance as well as the functionality of the circuit.

3.2.2 Advantages of DCVSL Logic Family over Conventional CMOS Logic:

i. There is a speed improvement in DCVSL as achieved in case of domino circuit. There is a reduction in the parasitic capacitances at the output nodes since logic function is

implemented using only pull down network consisting exclusively NMOS transistors provides a quicker response.

ii. Elimination of static power consumption is achieved by employing positive feedback provided by two cross-connected PMOS transistors which ensures that pull up transistor and PDN are never on simultaneously.

iii. DCVSL allows sharing of the common transistors in the logic network for both the differential outputs when some complex logic function is implemented. Requiring only PDN to implement logic function and provision for sharing of transistors provides significant saving of area as compared to conventional CMOS logic.

iv. This logic style generates differential outputs i.e. output and its complement both, therefore results in the elimination of inverting stage. We need not require an additional inverter to generate the complement of the output signal. This eliminates the problem of clock skew. When clock and clockbar are needed simultaneously, usage of an inverter to complement the clock signal would result in clock skew problem due to inverter delay. DCVSL circuit deals with this concern well.

Therefore, the attractive features of DCVSL design style are lesser circuit delays, higher logic flexibility and its differential mode of operation. But as every design style has its own advantages and drawbacks likewise DCVSL is also accompanied by certain disadvantages. Above mentioned advantages are achieved at the expense of additional area overhead and complexity associated with differential logic networks which involve complementary signals. Moreover during the transition, there is a period of time where there is a state of contention as mentioned above in the operation of the circuit when both PMOS and PDN are turned on simultaneously, producing a short circuit path. It might be possible that static DCVS circuits consume slightly more power, however, than conventional CMOS circuits because there is a dependence of charging and discharging times on the turn-on and the turn-off paths within the DCVS tree and these are usually asymmetrical. This asymmetry in rise and fall times extends the period of time for which current flows through the latch of the DCVSL circuit during the transient state, thereby causing an increase in the power dissipation. Thus we need to employ some circuit level power minimisation techniques in DCVSL circuits to take up the opportunity to realise faster circuits offered by DCVSL and spending less power for that.

3.3. IDEA OF LEAKAGE IN DCVSL

As DCVSL is a differential logic therefore one of the differential branches would not conduct and the other would conduct foe any given input combination applied. The branch not conducting would be having some amount of leakage current flowing through it due to off transistors in the path which would result in leakage power. Leakage power is the power dissipation owing to false currents when the transistors in the off branch of DCVSL are in the state of non-conduction.

3.4. APPLICATION OF LOW POWER TECHNIQUES TO DCVSL CIRCUITS

3.4.1 Existing methodologies:

a) MT-DCVS Design Methodology [16]: In this section, MTCMOS technique discussed in previous chapter has been modified to generate multi-threshold DCVS (MT-DCVS) circuits for leakage power reduction and high performance for DCVSL circuits in deep-submicron regions. These MT-DCVS logic circuits integrate low-V_T and regular high-V_T MOS devices. A mixed V_T methodology enables to achieve higher performance and at the same time keeping up a low leakage power for DCVS circuits.

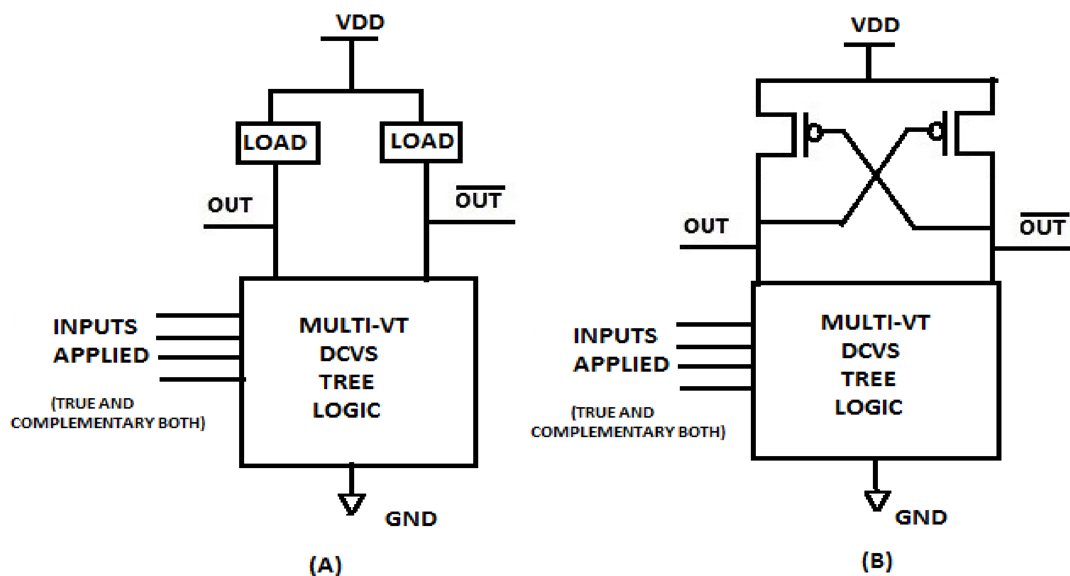


Fig 3.2 Schematic diagrams of (a) basic (b) static MT-DCVS circuit.

An MT-DCVS circuit schematic has been illustrated in figure3.2. The MT-DCVS circuit basically comprises of a multi threshold DCVS tree logic block and a load circuitry. Differential outputs are generated i.e. both true and complement output (Q and Q'). One of the most significant characteristics of the multi-V_T DCVSL block is the mixture of both low-V_T and high-V_T devices being used. Low-V_T devices are meant for gaining higher speed and high-V_T devices are meant for maintaining low leakage current. By means of a mixture of low V_T and high V_T devices we exploit the advantage of attainment of high speed while keeping the leakage current low.

b) Sleep Embedded DCVSL Methodology [2]: Sleep transistor approach was discussed in the previous chapter in context of CMOS circuits. Likewise, the sleep transistor concept has been adapted and reformed to be applied to DCVSL circuits in an attempt to obtain leakage current suppression. Combinations of high-VT and standard-VT sleep transistors have been used in order to maintain a proper-balance of the trade-off between high speed and leakage loss.

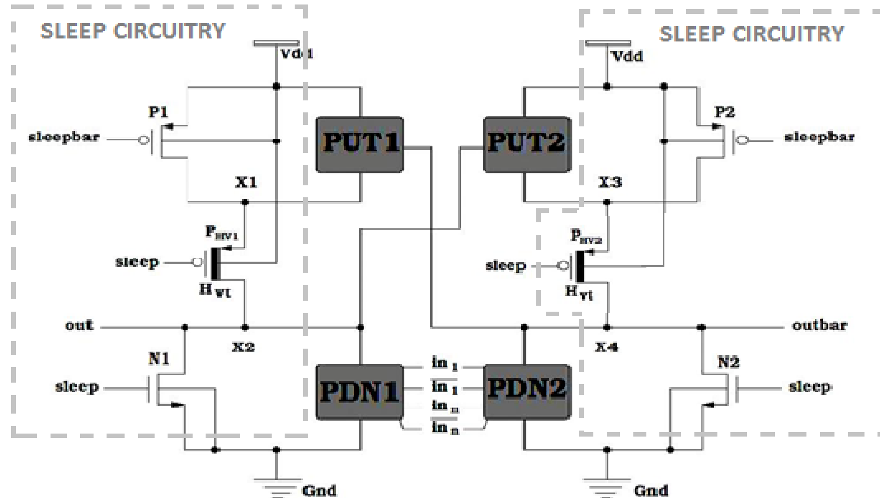


Fig.3.3 Generic sleep embedded DCVSL circuit [2]

Operation

A generic sleep embedded differential cascode voltage switch logic circuit has been shown in fig 3.3. During normal operation (i.e. active mode), 'sleep' signal is logic low and 'sleepbar' is logic high. This results in turning off of transistors {P1, P2, N1 and N2} and turning on of transistors {PHV 1 and PHV 2}. Behaviour of circuit in active mode is exactly same as that of a normal DCVSL circuit in normal mode of operation. The sleep or standby mode operation is slightly more intricate. During sleep mode, 'sleep' is logic high and 'sleepbar' is logic low. Therefore, transistors {P1, P2, N1 and N2} get turned on whereas transistors {PHV 1 and PHV 2} get turned off. P1 turns on so that the common point X1 is also grows to voltage V_{DD}. This brings PUT1 now between two equipotential (V_{DD}) points and henceforth there should not be any leakage current flowing through the PUT1. Similarly, N1 turns on and drives common point X2 to ground. The PDN1 comes now amid two equipotential (ground) points and hence there should not be any leakage current flowing through the PDN1. The same happens to PUT2 and PDN2 and there should not be any leakage current through them as well. The only path for leakage loss happening during the sleep (standby) mode will be through high threshold transistors PHV 1 and PHV 2 which are turned off, but, having their both end terminals connected at different potentials. Transistor PHV 1 is connected between points X1 and X2 and transistor PHV 2 is connected between points X3 and X4. Output values are always going to be '0' while the circuit is in sleep mode since 'out' and 'outbar' are connected to X2 and X4 respectively.

3.4.2 Proposed Methodology

Sleep embedded DCVSL approach achieves a significant reduction in leakage current but requires an external signal to drive the sleep transistors. Moreover, an additional serious limitation is the loss of state i.e. the circuit loses its actual state in sleep mode. Another approach to achieve the motive of leakage of suppression was MTDCVS which involves a combination of high V_T and low V_T devices in logic implementation. But proper selection of dual threshold transistors is critical to achieve balance between performance and leakage

reduction. In contrast to above delineated techniques, proposed technique is fully self-controlled technique which acts well in both active and idle modes. No area overhead since requires only two extra transistors for any logic implementation and properly retains the state of circuit.

"Modified LECTOR incorporated DCVSL approach": The leakage control transistor concept in [6] was adapted and modified to work for leakage current regulation in DCVSL circuits. Two high V_T leakage control transistors i.e. LCT1(PMOS) and LCT2(NMOS) are fitted between PUT and PDN on both the differential branches as shown in fig 3.4 below.

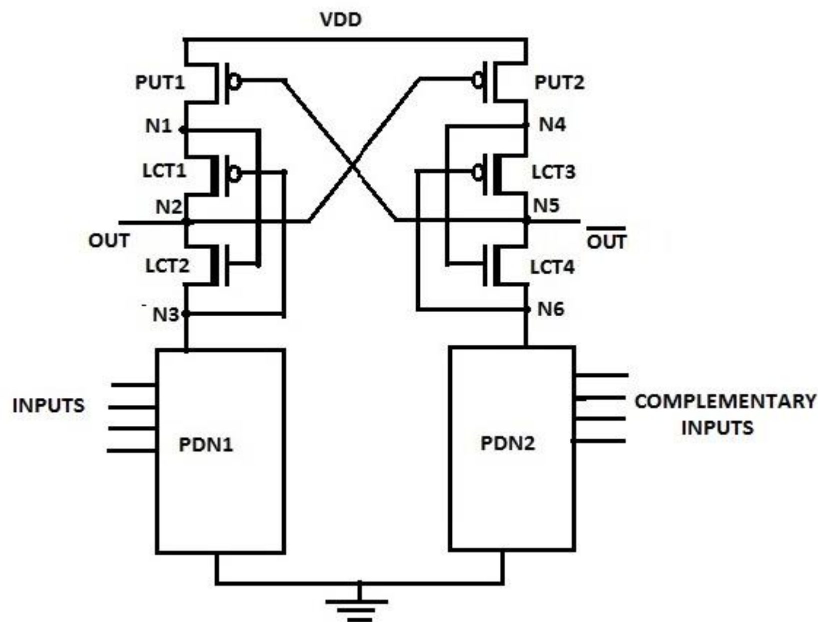


Fig 3.4 Modified LECTOR incorporated generic DCVSL circuit

a) Concept behind the above mentioned technique is that one of the two LCTs in the path from V_{DD} to ground in either of the differential branches is in near cut-off state for any input combination applied. This increases the overall resistance offered to the current flow along the path and thereby reducing the leakage current through the path. The use of high V_T LCTs cuts off the leakage further as high V_T transistors are far less leaky than standard V_T transistors. One of the most significant advantage of this technique is that it works well in both active and stand-by mode. Thus in active mode the technique very efficiently reduces the static current through the circuit as well when discharging has already taken place for the input combination applied which turns on the PDN causing output to discharge and still there is a static current through the path when the input is stable.

b) Architecture: The proposed leakage controlled network is exactly similar to basic DCVSL except the incorporation of two high V_T PMOS and NMOS leakage control transistors in both the true logic and complementary logic branches as leakage control circuitry. LCT1 and LCT2 are inserted between PUT1 and PDN1; likewise LCT3 and LCT4

are inserted between PUT2 and PDN2. PDN1 is meant for logic implementation of desired function and PDN2 implements differential logic.

c) Leakage control mechanism in modified DCVSL circuit: As we know PDN1 and PDN2 are mutually exclusive. Therefore will not be active simultaneously i.e. one of the branches will be OFF (no discharge path available to ground) and other would be ON (discharge path available to ground). Here the OFF branch corresponding to OFF PDN would experience leakage loss. OFF transistors would offer a subthreshold leakage current to flow through the branch when current through OFF branch should ideally be zero. Incorporation of leakage control transistors diminish the leakage current flowing through the branch when PDN is OFF as well as the static current when PDN is on. Suppose initially Out and Outbar are at '1' and '0' respectively. Consider a case where input combination is such that PDN 1 is OFF and provides no discharge to Out. Since Outbar is at logic '0', it keeps PUT1 turned ON so that node N1 is at $V_{DD.}$ LCT1 passes strong '1' so that Out is also at V_{DD}. LCT2 which is an NMOS passes weak '1' leads node N3 to voltage 'V_{DD}-V_T'. So by analysing the voltages at the terminals of LCT1 and LCT2, it can be figured out that LCT2 is ON and LCT1 is in near cut off state. Subsequently offering more impedance to leakage current flowing while there should be no current ideally, it reduces the leakage loss. Similarly the case of static current reduction can be analysed when the given input combination is such that it turns on the PDN1. In context of figure shown above, static current is the current flowing from V_{DD} to ground when PDN1 is ON and Out has stabilised itself at logic low after discharging process. So when PDN1 turns ON, Out starts discharging and PUT1 is still ON since Outbar is at still 0. As Out reaches below V_{DD}-$V_{T,}$ it turns ON PUT2 which in turn charges Outbar to V_{DD} and thus PUT1 turns OFF. Since PDN1 is ON, N3 falls to logic '0' and as LCT2 (NMOS) passes strong '0' therefore Out is also completely discharges to '0'. Taking into consideration that LCT1 is a PMOS, it passes weak '0' and node N1 is at 'V_{DD}-V_T'. In this case LCT2 comes out to be in near cut off state and contributing in reduction of unnecessary power loss because of static currents flowing. Hereby it can be comprehended that LECTOR incorporated DCVSL circuitry proves to be an effective approach to regulate unnecessary power loss in both active and standby modes.

d) Examples: CMOS XOR gates are used as an essential fundamental building unit in quite a lot of VLSI applications like adders and microprocessors for instance. CMOS XOR gates are characterised by high power consumption, lesser speed and bigger layout area because of the complex pull up and pull down networks they possess [10].DCVSL XOR implements logic function with pull down network only and more over allows sharing of common transistors in PDN to implement both logic function and its complement. So wherever both the XOR signal and its complement are required, DCVSL consumes smaller layout area and proves to be better choice over CMOS XOR. Reduction in transistor count improves the speed of the gate as well as compared to CMOS XOR. Because of the superior performance offered by DCVSL XOR, it finds its usage in numerous VLSI applications. To make these gates more efficient at lower technologies, their leakage aspect is being explored and tried to be dealt effectively.

The leakage control efficiency of LECTOR technique has been applied and verified on various differential cascode voltage switch logic gates. Basic and LECTOR incorporated configurations for 2-input and 3-input XOR gates are shown below.

i) Basic DCVSL 2-input XOR gate (2-level stacking)

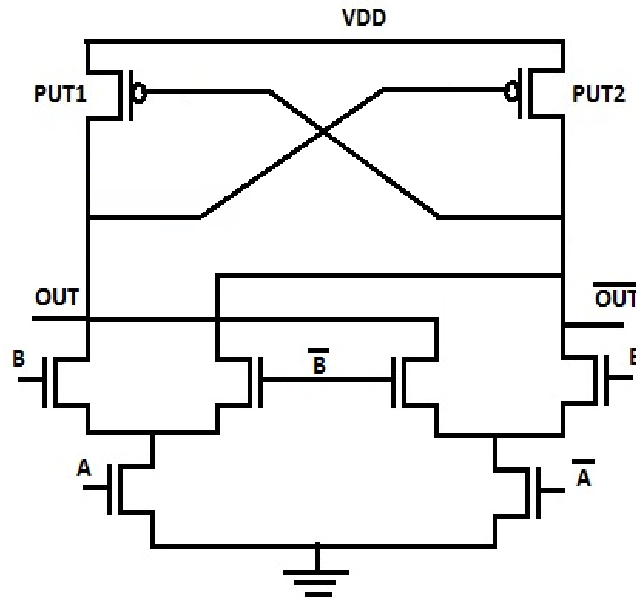


Fig.3.5 Two-input XOR gate

ii) LECTOR incorporated DCVSL 2-input XOR gate (2-level stacking)

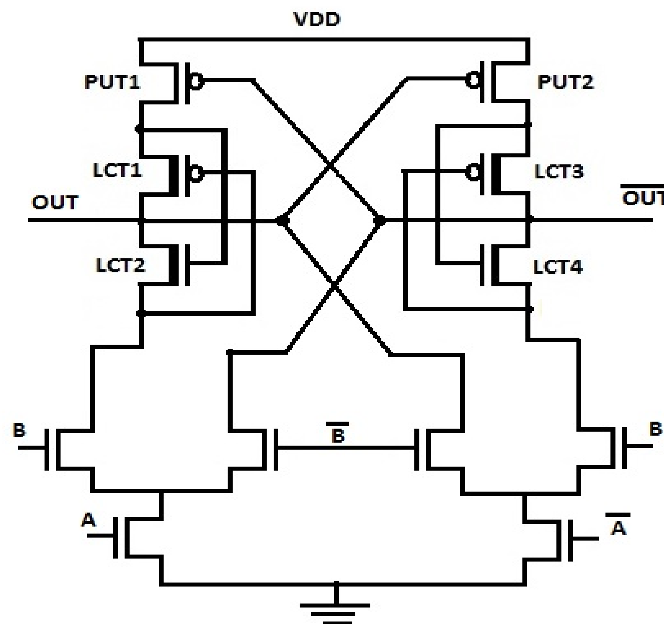


Fig.3.6 Two-input LECTOR XOR gate

iii)Basic DCVSL 3-input XOR gate (3-level stacking)

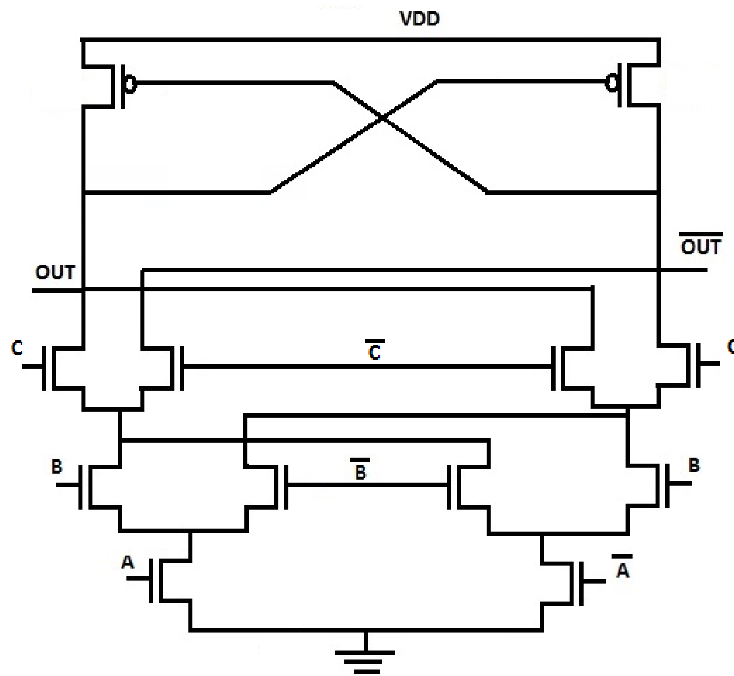


Fig3.7 Three input XOR gate (all stacking)

iv)LECTOR incorporated DCVSL 3-input XOR gate (3-level stacking)

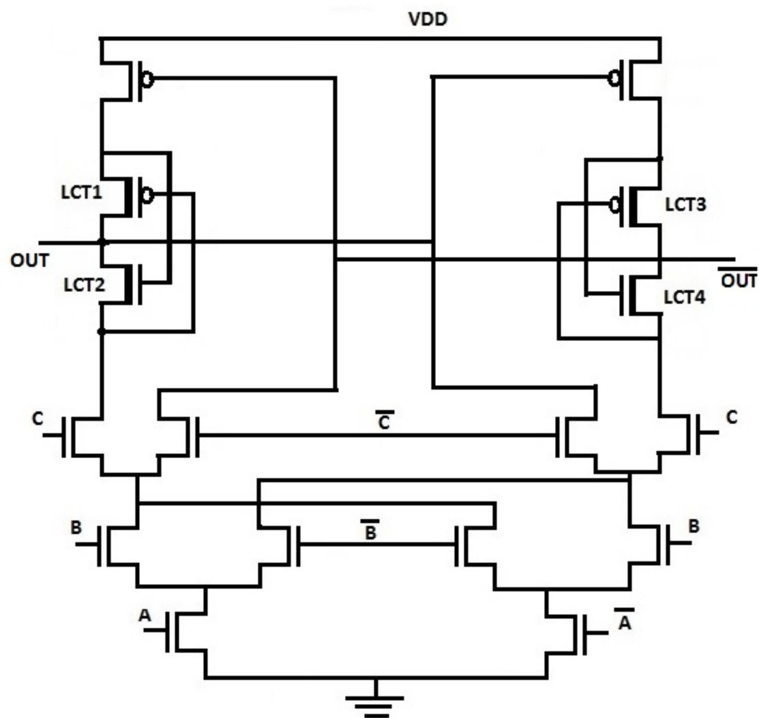


Fig.3.8 Three-input LECTOR XOR gate

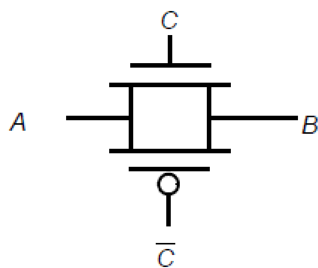
3.5 HYBRID STATIC DCVSL (Hy-DCVSL)

Hybrid static DCVSL technique has been proposed as an alternative to differential cascode voltage switch logic (DCVSL) style for digital circuit design. The Hy-DCVSL presents the usage of transmission gates with basic DCVSL for digital logic implementation. Interestingly it results in reduction of the stacked source-coupled transistor pair levels when compared to the present DCVSL style. Reduction in stacked transistor pair levels lessens the leakage current through the path. A static logic design style using the transmission gates for implementation of the logic functions has been proposed.

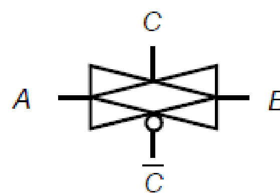
3.5.1 What Are Transmission Gates?

CMOS transmission gate (TG) or pass gate can be considered as a basic switch circuit. A new category of logic circuits has been presented which makes use of Transmission Gates as their basic building units. A CMOS transmission gate is a parallel connection of an NMOS and a PMOS transistor as shown in figure 3.9. Complementary pass transistor logic could be thought as possibly the first choice for hybrid approach but they have a serious drawback of threshold voltage drop in logic high input (as NMOS passes weak 1). Transmission gates are extensively used to deal with the problem of voltage-drop in complementary pass transistor logic [14]. It is built by utilising the complementary properties of NMOS and PMOS transistors i.e. NMOS transistors pass a good 0 while a weak 1, while PMOS transistors pass a good 1whereas a weak 0. Thus the perfect approach would be to use an NMOS for pull-down operation and a PMOS to perform pull-up operation. The transmission gate is a clever blend of the best essences of both the devices by forming a parallel combination of NMOS device and a PMOS device. Complementary control signals are given to the gate terminals of the transmission gate (C and Cbar). The transmission gate typically behaves as a bidirectional switch whose functionality is controlled by the gate signal C. When C = 1, both MOSFETs are turned on which allows the signal to pass through the gate. In short,

$$A = B \text{ if } C = 1$$



(a) Circuit



(b) Symbolic representation

Fig 3.9 CMOS transmission gate

On the other hand, C = 0 brings both the transistors in cut-off state and thus resulting in an open circuit between the nodes A and B.

3.5.2 Proposed Hybrid Configuration

The circuit diagrams of various basic DCVSL XOR gates are being shown in fig.3.5 and fig.3.7. It can be observed that the PDN consist of multiple levels of source-coupled transistor pairs which add to the leakage of the gate. It could be thought that stacking of transistors should reduce leakage as was explained in forced stack technique in previous chapter. But the condition for stacking to reduce leakage is that all the stacked transistors should be in off-state simultaneously. Here in the case of n-input XOR gate which is one of the basic building unit for many digital designs does not have the case of all stacked transistors OFF in the path. Either of the transistors in the path is bound to be ON and is going to add up its slight ON current to the leakage of the branch and hence increasing the leakage current when there should be no current through the path overruling the stacking effect.

Therefore an alternative configuration has been proposed to cut down the leakage loss of the gates because of the numerous source-coupled transistor pair levels in N-input XOR gate. The novel gates are constructed with an intention to lessen these source-coupled transistor pair levels in the Pull down network. The basic structural design of a Hy-DCVSL gate has been shown in Fig. 3.10. The only difference lies in the approach to implement the logic function. A part of logic functionality is realised using transmission gates (TG) while residual part implemented in PDN itself.

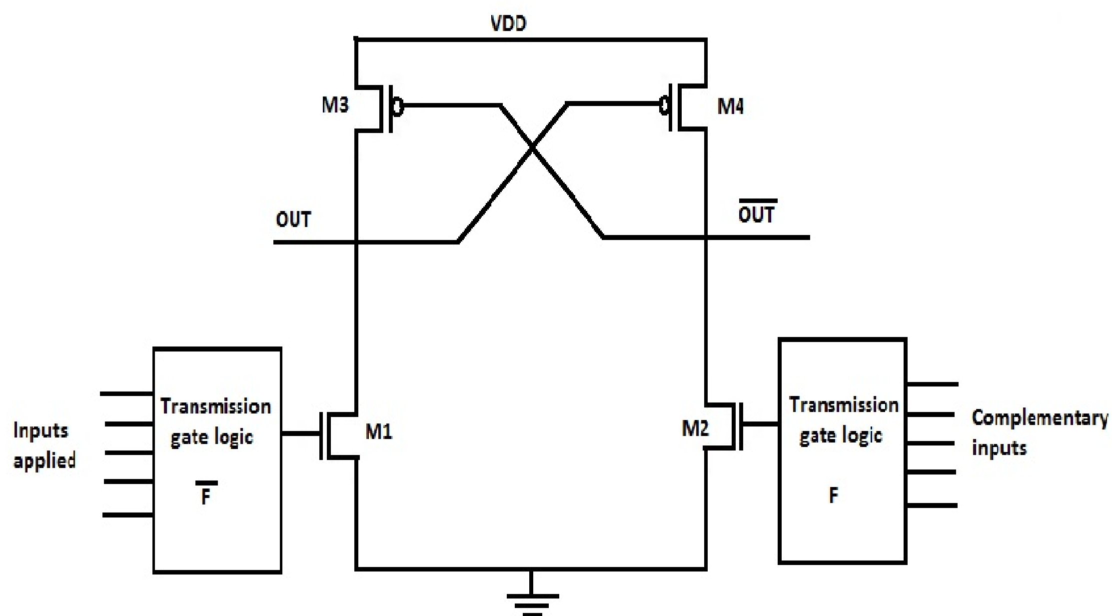


Fig. 3.10 Basic architecture of a generic Hy-DCVSL circuit

The output of the transmission gate logic and the complementary transmission gate logic is applied to input of the transistors M1 and M2 respectively. Initially there is an evaluation of the output of TGL (transmission gate logic) and then it is aptly reflected at the output node of DCVSL circuit. The reduction in the source coupled levels reduces the leakage loss offered by the circuit. Hybrid configurations for 2-input and 3-input XOR gates have been proposed along with their LECTOR incorporated configurations as shown below.

a) 2-Input XOR DCVSL Gate

Hybrid configuration of 2-input XOR involves implementing $A \odot B$ and $A \oplus B$ using transmission gate logic and applying them to the gates of M1 and M2 respectively as shown in Fig. 3.11. TGL is evaluated on both the sides then M1 and M2 invert their respective TG logics and appropriately reflect the input at the output nodes.

i) Proposed hybrid DCVSL(all TG)

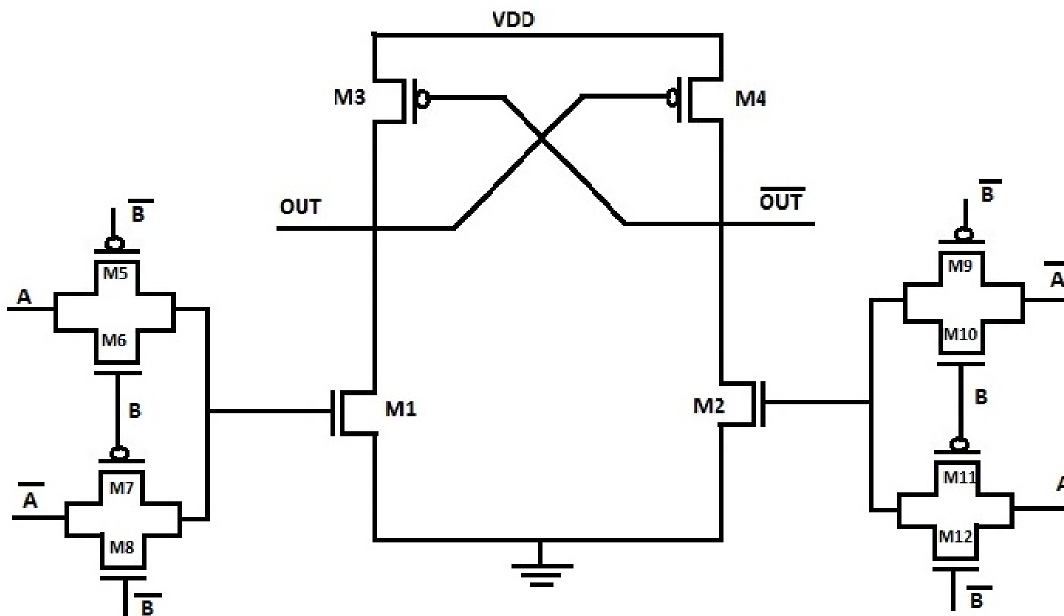


Fig.3.11 Proposed hybrid DCVSL 2-input XOR gate

ii) LECTOR hybrid DCVSL (all TG)

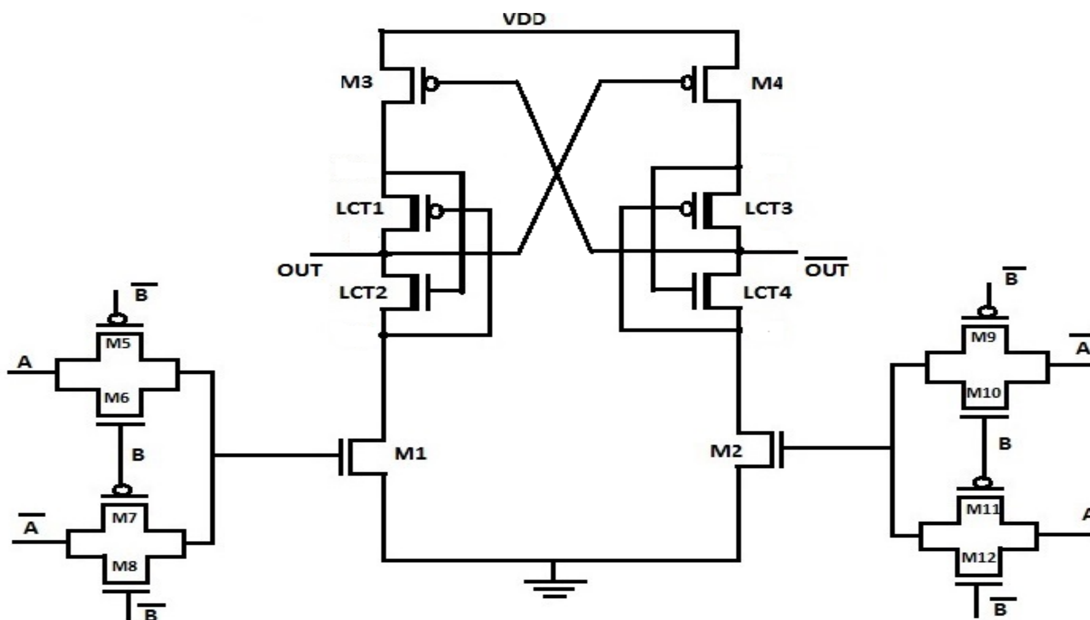


Fig.3.12 LECTOR hybrid DCVSL 2-input XOR gate

b) 3-Input XOR DCVSL Gate

Hybrid realization of the three input XOR DCVSL gate can be achieved in two possible types-

TYPE1 realises 3-input XOR with only two stacked source-coupled transistor pair levels in contrast to the three level stacking as in the case of basic fully stacked DCVSL gate. The XOR of two inputs is realised by the TGL logic and is fed to the input to the lowest stack level and the upper stack level is then formed by following the same approach as earlier for basic DCVS logic.

TYPE2 realises complete logic for 3-input XOR gate with transmission gate logic. TGL output is then fed to the input of DCVS logic circuit which is now a kind of inverter/buffer configuration whose input is driven by the output of the TGL logic implemented. This greatly reduces the leakage current through the path as there are no more stacked source coupled transistors pairs left.

i) **Proposed Hybrid DCVSL TYPE 1 (TG+ two level stacking)**

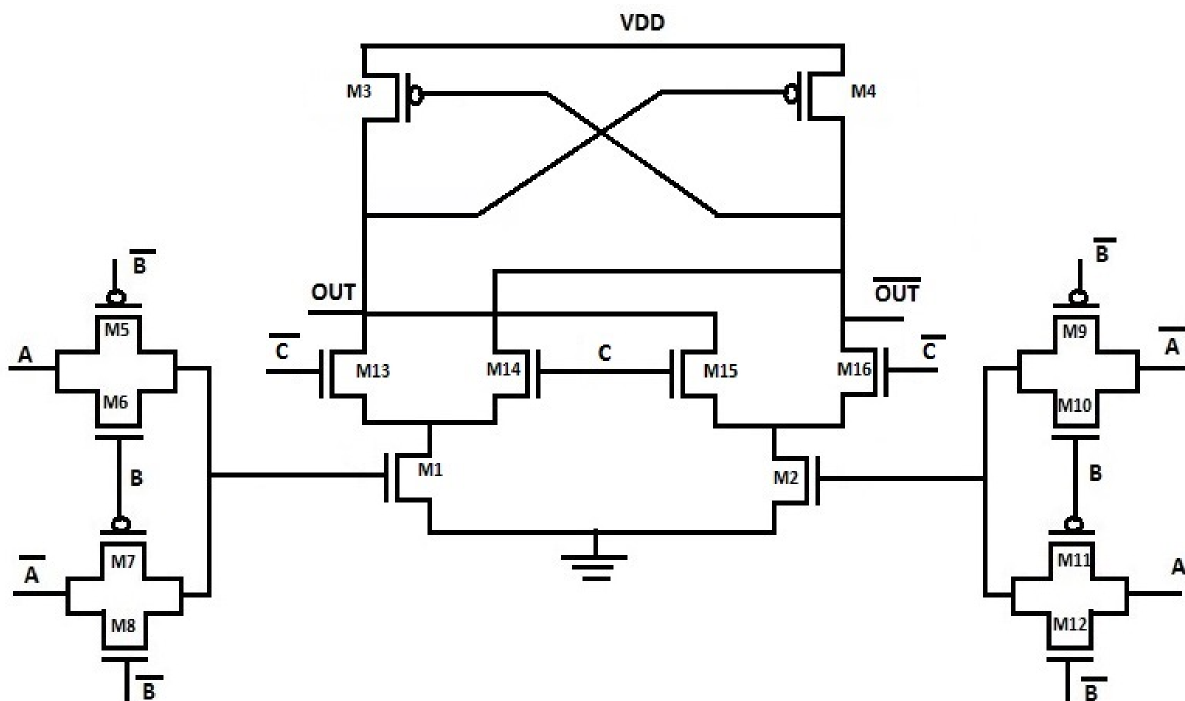


Fig.3.13 Proposed Hybrid DCVSL 3-input XOR TYPE1

ii) LECTOR Hybrid DCVSL TYPE 1 (TG+ two level stacking)

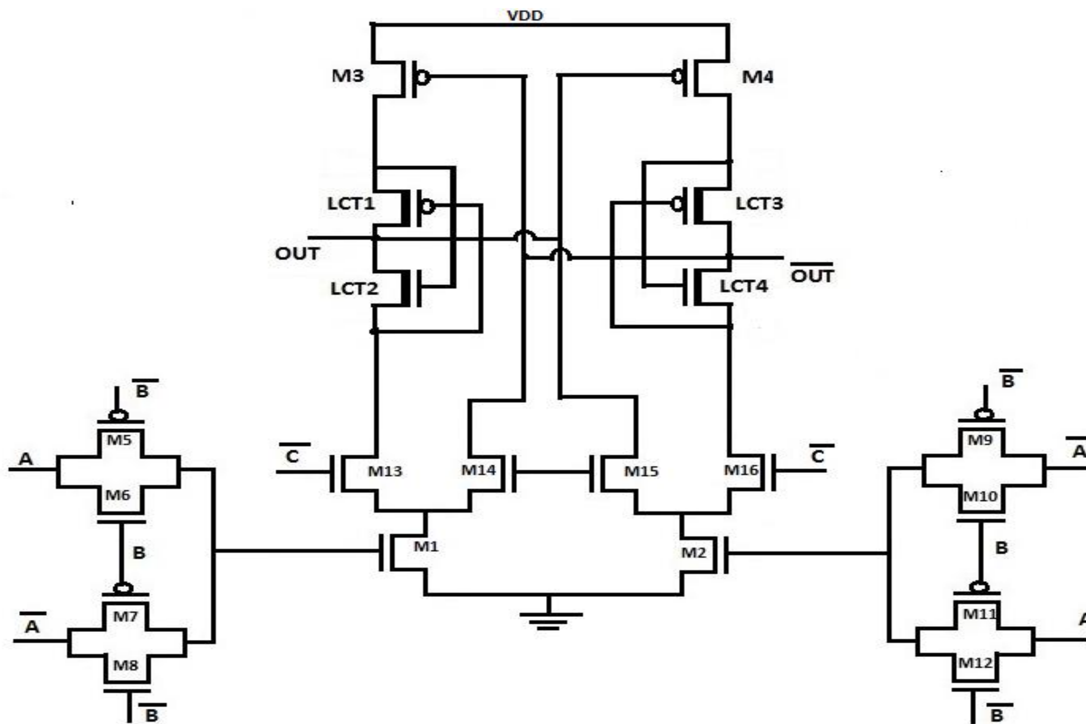


Fig.3.14 LECTOR Hybrid DCVSL 3-input XOR TYPE1

iii) Proposed Hybrid DCVSL TYPE 2 (All TG)

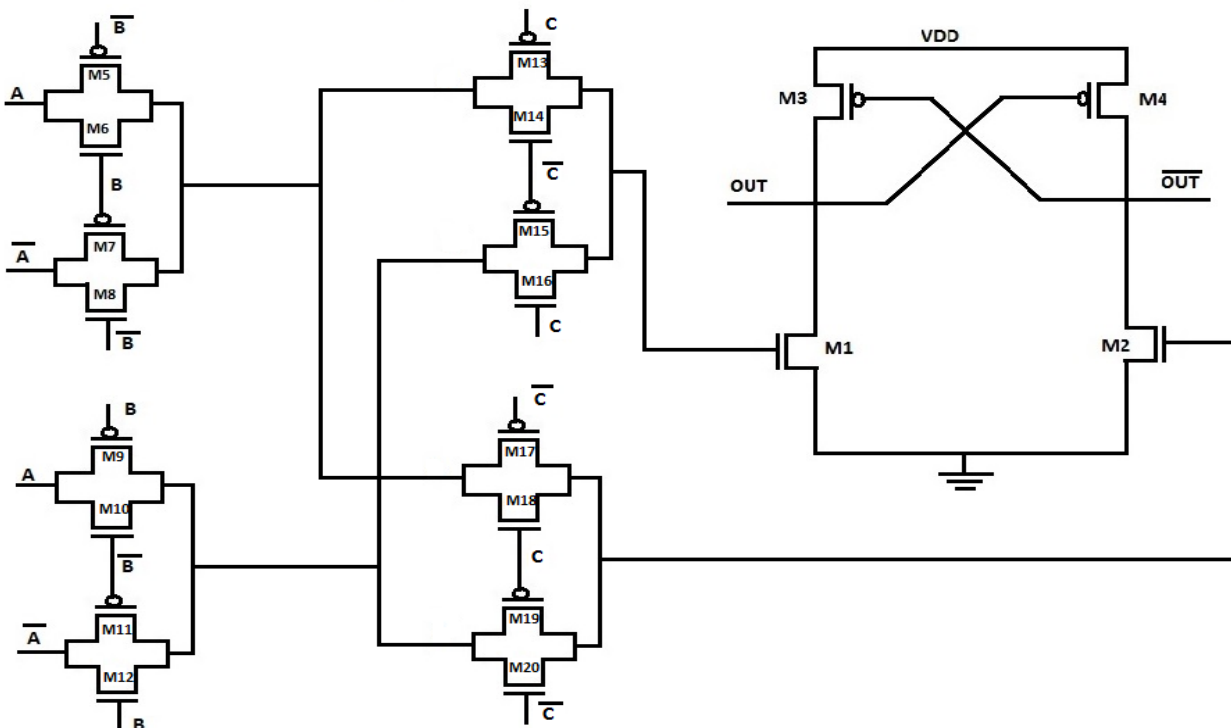


Fig.3.15 Proposed Hybrid DCVSL 3-input XOR TYPE2

iv) LECTOR Hybrid DCVSL TYPE 2 (all TG)

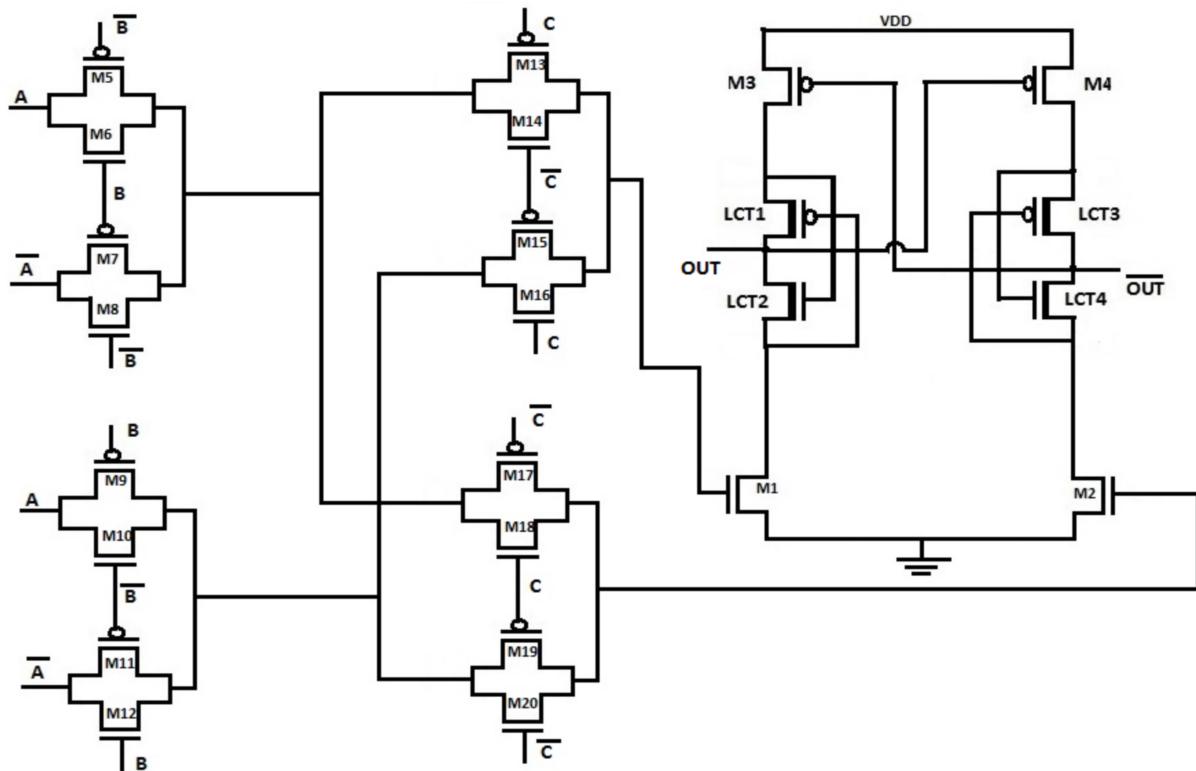


Fig.3.16 LECTOR Hybrid DCVSL 3-input XOR TYPE2

3.6 SIMULATION RESULTS AND DISCUSSIONS

All the proposed static DCVSL configurations in the above chapter were designed and simulated in order to find out the saving achieved in leakage current. Simulations have been performed at 90nm, 65nm and 45nm technology nodes on SYMICA design platform. Supply voltage variation and temperature variation have been performed as well to study the pattern followed by leakage current.

1. BASIC DCVSL INVERTER

Basic DCVSL inverter shown in fig.3.18 was designed and simulated. Figure 3.19 shows LECTOR incorporated DCVSL inverter designed and simulated to authenticate the effectiveness of LECTOR technique in leakage current reduction when applied to basic DCVSL inverter.

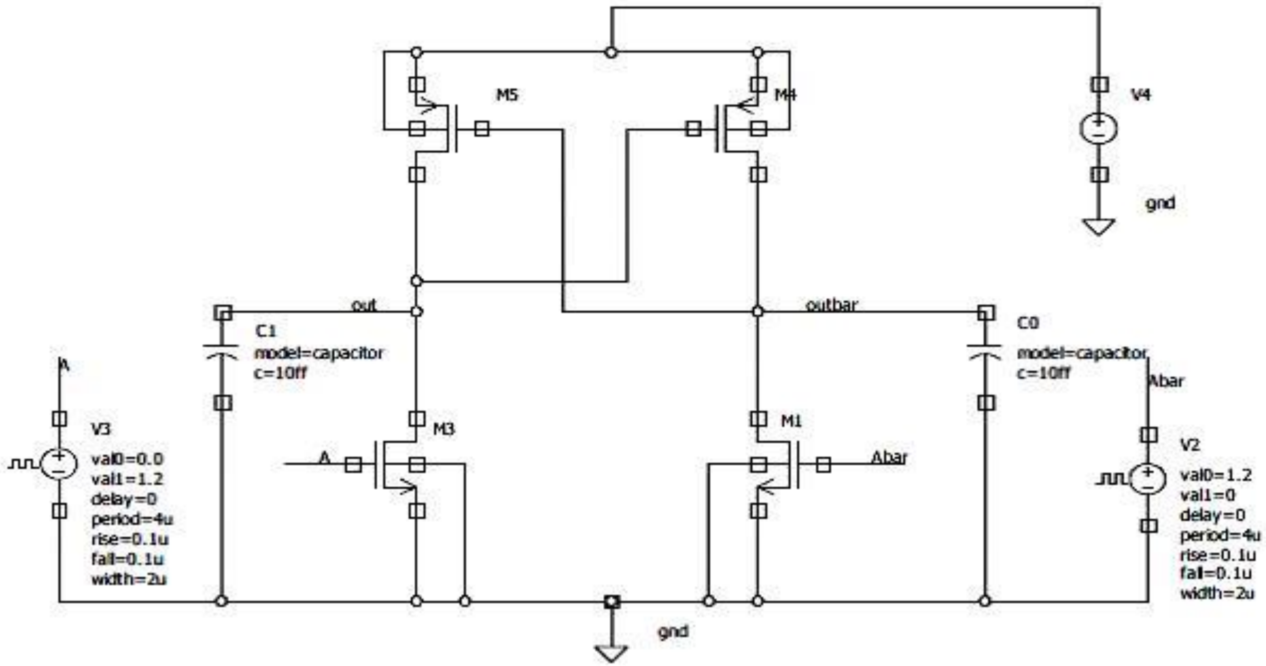


Fig. 3.17 DCVSL inverter basic

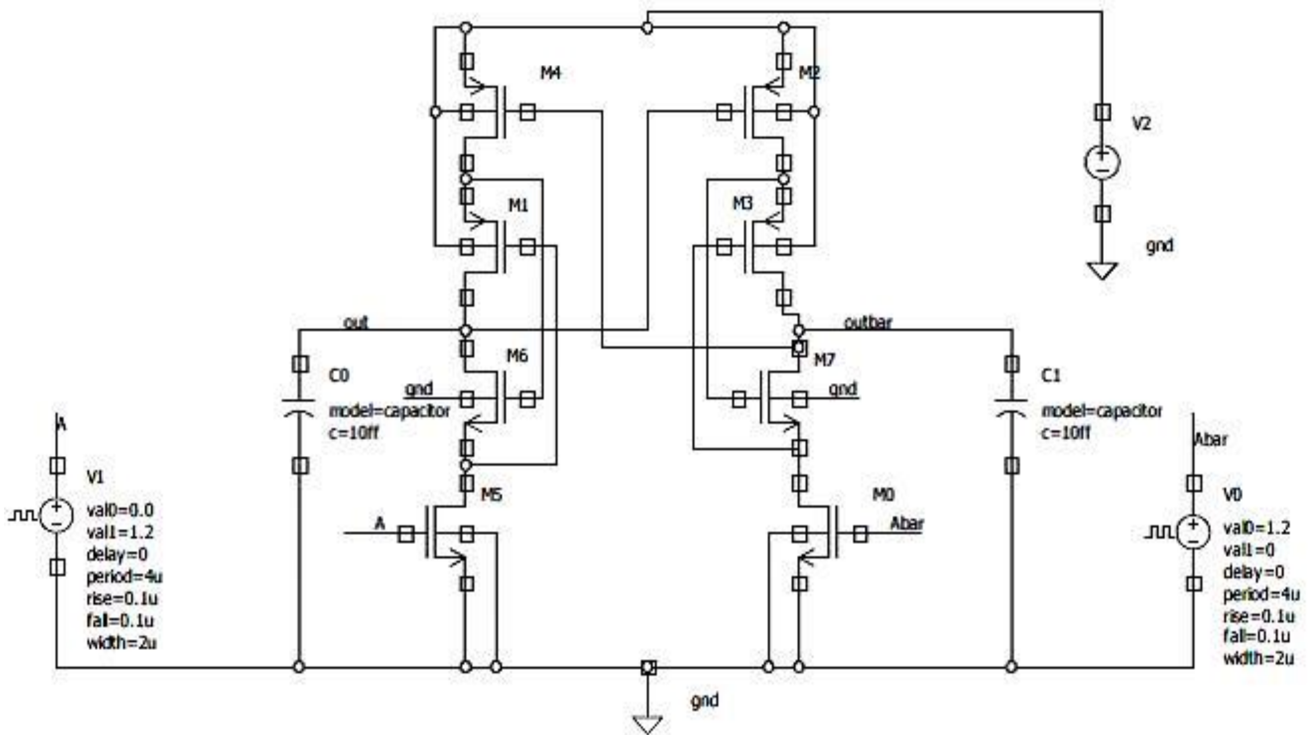


Fig. 3.18 LECTOR incorporated DCVSL inverter

TABLE 3.1
LEAKAGE CURRENT MEASUREMENT FOR BASIC AND LECTOR DCVSL INVERTER AT VDD=1.8V

Technology	Leakage current (nA)		
	Basic	Lector (With high V_T)	Percentage saving (With high V_T)
180nm	0.172	0.070	59.30%
90nm	30.52	5.61	81.16%
65nm	64.70	7.92	88.53%
45nm	154.74	14.09	90.89%
	Static current (nA)		
90nm	52.23	10.58	79.74%
65nm	144.19	16.37	88.64%
45nm	672.21	33.02	95.08%

TABLE 3.2
LEAKAGE CURRENT MEASUREMENT FOR BASIC AND LECTOR DCVSL INVERTER AT VDD=1.2V

Technology	Leakage current (nA)		
	Basic	Lector (With high V_T)	Percentage saving (With high V_T)
90nm	3.73	1.55	58.44%
65nm	5.13	1.69	67.05%
45nm	8.74	2.02	76.88%
	Static current (nA)		
90nm	6.04	2.22	63.24%
65nm	8.63	2.40	72.19%
45nm	16.55	2.81	83.02%

Table 3.1 and Table 3.2 represent the leakage current values for basic DCVSL inverter and LECTOR incorporated DCVSL inverter for supply voltage of 1.8V and 1.2V respectively. It can be observed that percentage saving achieved is 59%-95% for VDD=1.8V and 58%-83% for VDD=1.2V where efficiency of the proposed LECTOR configuration increases with lowering down of technology from 90nm to 45nm.

2. DCVSL NAND/AND

DCVSL NAND/AND consists of two stacked NMOS transistors implementing NAND logic and two parallel NMOS transistors driven by complementary inputs implementing differential AND logic.

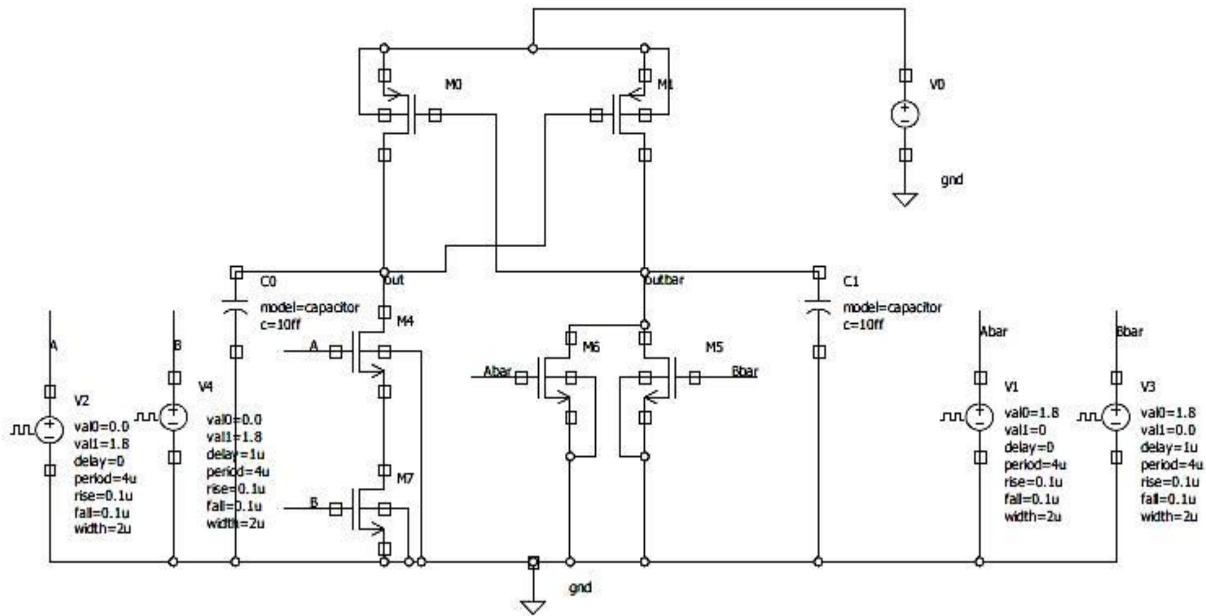


Fig. 3.19 DCVSL NAND/AND

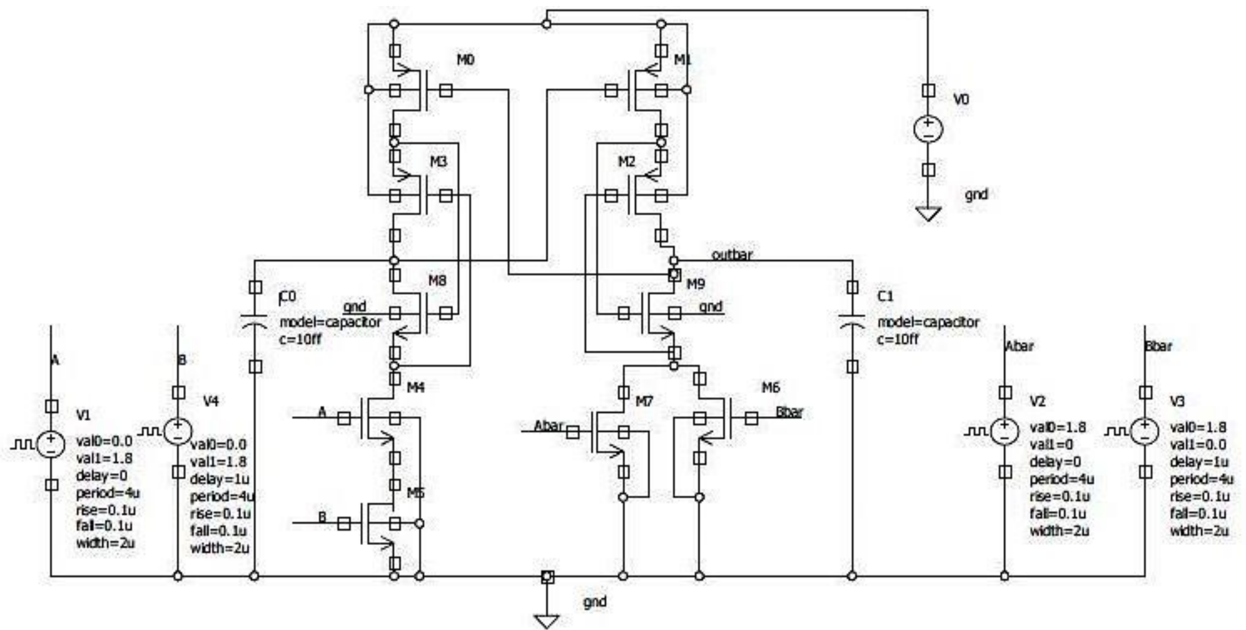


Fig. 3.20 LECTOR incorporated DCVSL NAND/AND

Table 3.3 and Table 3.4 tabulate the leakage current values for basic and LECTOR incorporated DCVSL NAND/AND gates for VDD=1.8 and VDD=1.2 respectively. It is quite clear that leakage current decreases with reduction in supply voltage for a given threshold voltage. LECTOR configuration of DCVSL NAND/AND gate achieves significant saving in leakage current as compared to its basic configuration. Ideally, PDN1 should not conduct any current for input combination (1,0), (0,1) and (0,0) but leakage current shows its presence there. Input combination (1,1) turns on PDN1 and allows output node to discharge. After discharging when the output has stabilised to value '0', there

should be no current through PDN1 but there flows a static current through it which is undesirable. LECTOR incorporated configuration notably reduces both of these undesirable currents as can be observed from the tables given below.

TABLE 3.3
LEAKAGE CURRENT MEASUREMENT FOR BASIC AND LECTOR DCVSL NAND/AND GATE AT VDD=1.8V

Technology/ Input states(A,B)	Basic	Lector (With high V_T)	Percentage saving (With high V_T)
90nm			
Leakage current(nA)			
(1,0)	14.70	11.20	23.8%
(0,1)	63.80	11.27	82.33%
(0,0)	26.12	1.56	94.00%
Static current(nA)			
(1,1)	52.32	10.64	79.66%
65nm			
Leakage current(nA)			
(1,0)	22.07	15.94	27.70%
(0,1)	136.69	16.11	88.21%
(0,0)	60.23	2.45	95.90%
Static current(nA)			
(1,1)	144.81	16.51	88.59%
45nm			
Leakage current(nA)			
(1,0)	43.12	28.59	34.00%
(0,1)	337.90	29.23	91.30%
(0,0)	73.14	2.35	96.78%
Static current(nA)			
(1,1)	684.62	33.82	95.06%

TABLE 3.4
LEAKAGE CURRENT MEASUREMENT FOR BASIC AND LECTOR DCVSL NAND/AND GATE AT VDD=1.2V

Technology/ Input states(A,B)	Basic	Lector (With high V_T)	Percentage saving (With high V_T)
90nm			
Leakage current(nA)			
(1,0)	3.99	3.11	22.05%
(0,1)	7.94	3.13	60.57%
(0,0)	0.792	0.431	45.51%
Static current(nA)			

(1,1)	6.04	2.24	62.91%
65nm			
Leakage current(nA)			
(1,0)	4.64	3.42	26.29%
(0,1)	11.18	3.46	69.05%
(0,0)	1.17	0.435	62.78%
Static current(nA)			
(1,1)	8.63	2.43	71.84%
45nm			
Leakage current(nA)			
(1,0)	6.15	4.17	32.19%
(0,1)	19.95	4.24	78.74%
(0,0)	1.10	0.358	67.36%
Static current(nA)			
(1,1)	16.57	2.88	82.61%

It can be observed from Table 3.3 and Table 3.4 that percentage saving achieved in leakage and static current for VDD=1.8V is 23%-94% for 90nm, 27%-95% for 65nm and 34%-96% for 45nm. For VDD=1.2V, percentage saving achieved is 22%-62% for 90nm, 26%-72% for 65nm and 32%-82% for 45nm. Table 3.4 shows that the leakage current is minimum for the condition where both transistors are off. It's because inherent stacking comes into picture.

3. Two input DCVSL XOR/XNOR gate (all stacking)

Basic structure of fully stacked 2-input DCVSL XOR gate shown in fig. 3.5 is simulated with input conditions given as – load capacitances = 10ff, inputs A and B with period=4us, rise time (fall time) = 0.1us, width=2us and delay of 0.5us between different inputs, for different technologies. From both the output nodes two discharging paths are branching out. Output node discharges if any of those paths is turned ON. There should be no current from "out" to ground for input combinations (1,0) and (0,1) (known as OFF states). Nonetheless, leakage current makes its path to ground through off transistors for these inputs. Similarly, for input combinations (1,1) and (0,0) (known as ON states) PDN1 turns on and discharges "out" to logic "0". Current flow through PDN after output stabilisation is static current which is undesirable.

LECTOR incorporated configuration of 2-input DCVSL XOR gate shown in fig. 3.6 is simulated with same input conditions as mentioned above. It successfully reduces the leakage currents and static currents in basic configuration which can be observed from Table 3.5 and Table 3.6 for supply voltage of 1.8V and 1.2V respectively.

TABLE 3.5

LEAKAGE CURRENT MEASUREMENT FOR BASIC AND LECTOR DCVSL 2-INPUT XOR/XNOR GATE AT VDD=1.8V

Technology/ Input states(A,B)	Basic	Lector (With high V_T)	Percentage saving (With high V_T)
90nm			
OFF STATES	**Leakage current (nA)**		
(1,0)	91.34	30.93	66.13%
(0,1)	91.34	30.93	66.13%
ON STATES	**Static current(nA)**		
(1,1)	52.42	10.83	79.33%
(0,0)	52.42	10.83	79.33%
65nm			
OFF STATES	**Leakage current(nA)**		
(1,0)	176.00	43.21	75.44%
(0,1)	176.00	43.21	75.44%
ON STATES	**Static current(nA)**		
(1,1)	145.00	17.00	88.27%
(0,0)	145.00	17.00	88.27%
45nm			
OFF STATES	**Leakage current(nA)**		
(1,0)	397.00	75.42	81.00%
(0,1)	397.00	75.42	81.00%
ON STATES	**Static current(nA)**		
(1,1)	689.50	36.47	94.71%
(0,0)	689.50	36.47	94.71%

TABLE 3.6

LEAKAGE CURRENT MEASUREMENT FOR BASIC AND LECTOR DCVSL 2-INPUT XOR/XNOR GATE AT VDD=1.2V

Technology/ Input states(A,B)	Basic	Lector (With high V_T)	Percentage saving (With high V_T)
90nm			
OFF STATES	**Leakage current(nA)**		
(1,0)	15.55	8.68	44.18%
(0,1)	15.55	8.68	44.18%
ON STATES	**Static current(nA)**		
(1,1)	6.05	2.29	62.14%
(0,0)	6.05	2.29	62.14%

65nm			
OFF STATES	**Leakage current(nA)**		
(1,0)	19.94	9.42	52.75%
(0,1)	19.94	9.42	52.75%
ON STATES	**Static current(nA)**		
(1,1)	8.64	2.51	70.94%
(0,0)	8.64	2,51	70.94%
45nm			
OFF STATES	**Leakage current(nA)**		
(1,0)	31.32	11.18	64.30%
(0,1)	31.32	11.18	64.30%
ON STATES	**Static current(nA)**		
(1,1)	16.61	3.11	81.27%
(0,0)	16.61	3.11	81.27%

It can be observed from Table 3.5 and Table 3.6 that percentage saving obtained in leakage and static current for VDD=1.8V is 66%-79% for 90nm, 75%-88% for 65nm and 81%-94% for 45nm. For VDD=1.2V, percentage saving achieved is 44%-62% for 90nm, 52%-71% for 65nm and 64%-81% for 45nm.

4. Two input hybrid DCVSL XOR gate (all TG)

Hybrid configuration of two input DCVSL XOR/XNOR gate represented by fig. 3.11 is simulated with input conditions given as – load capacitances = 10ff, inputs A and B with period=4us, rise time (fall time) = 0.1us, width=2us and delay of 0.5us between the two inputs, for different technologies. Similarly, LECTOR incorporated version of 2-input hybrid DCVSL XOR/XNOR gate represented by fig. 3.12 is simulated with same input conditions as mentioned above. Leakage and static current values obtained are tabulated in Table 3.7 and Table 3.8 for both the configurations at VDD=1.8V and VDD=1.2V respectively.

TABLE 3.7
LEAKAGE CURRENT MEASUREMENT FOR PROPOSED AND LECTOR HYBRID 2-INPUT DCVSL XOR/XNOR GATE AT VDD=1.8V

Technology/ Input states(A,B)	Proposed	Lector (With high V_T)	Percentage saving (With high V_T)
90nm			
OFF STATES	**Leakage current(nA)**		
(1,0)	30.57	5.68	81.41%
(0,1)	30.57	5.68	81.41%
ON STATES	**Static current(nA)**		
(1,1)	52.23	10.58	79.74%

(0,0)	52.23	10.58	79.74%
65nm			
OFF STATES	Leakage current(nA)		
(1,0)	64.93	7.99	87.69%
(0,1)	64.93	7.99	87.69%
ON STATES	Static current(nA)		
(1,1)	144.20	16.37	88.64%
(0,0)	144.20	16.37	88.64%
45nm			
OFF STATES	Leakage current(nA)		
(1,0)	159.00	14.70	90.75%
(0,1)	159.00	14.70	90.75%
ON STATES	Static current(nA)		
(1,1)	672.56	33.13	95.07%
(0,0)	672.56	33.13	95.07%

TABLE 3.8

LEAKAGE CURRENT MEASUREMENT FOR PROPOSED AND LECTOR HYBRID 2-INPUT DCVSL XOR/XNOR GATE AT VDD=1.2V

Technology/ Input states(A,B)	Proposed	Lector (With high V_T)	Percentage saving (With high V_T)
90nm			
OFF STATES	Leakage current(nA)		
(1,0)	3.74	1.55	58.55%
(0,1)	3.74	1.55	58.55%
ON STATES	Static current(nA)		
(1,1)	6.04	2.22	63.24%
(0,0)	6.04	2.22	63.24%
65nm			
OFF STATES	Leakage current(nA)		
(1,0)	5.13	1.69	67.05%
(0,1)	5.13	1.69	67.05%
ON STATES	Static current(nA)		
(1,1)	8.63	2.40	72.19%
(0,0)	8.63	2.40	72.19%
45nm			
OFF STATES	Leakage current(nA)		
(1,0)	8.75	2.03	76.80%
(0,1)	8.75	2.03	76.80%
ON STATES	Static current(nA)		

(1,1)	16.55	2.80	83.08%
(0,0)	16.55	2.80	83.08%

It can be observed from Table 3.7 and Table 3.8 that percentage saving obtained in leakage and static current for VDD=1.8V is 79%-81% for 90nm, 87%-88% for 65nm and 90%-95% for 45nm. For VDD=1.2V, percentage saving achieved is 58%-63% for 90nm, 67%-72% for 65nm and 77%-83% for 45nm.

5. THREE input DCVSL XOR/XNOR gate (all stacking)

Basic structure of fully stacked 3-input DCVSL XOR/XNOR gate presented by fig. 3.7 and LECTOR incorporated configuration of 3-input DCVSL XOR/XNOR gate (all stacking) presented by fig. 3.8 are simulated with input conditions given as – load capacitances = 10ff, inputs A, B and C with period=4us, rise time (fall time) = 0.1us, width=2us and delay of 0.5us between different inputs, for different technologies. Three level stacking of NMOS transistors is done to implement the required function. Input states which correspond to "out=1" are the OFF states which should not allow any current flow through PDN1. Similarly, input states which correspond to "out=0" are the ON states which should not allow any current flow through PDN1 after the output node has completely discharged. Leakage currents and static currents for some of the corresponding input states are shown in Table 3.9 and Table 3.10 for supply voltage 1.8V and 1.2V respectively.

TABLE 3.9
LEAKAGE CURRENT MEASUREMENT FOR BASIC AND LECTOR 3-INPUT DCVSL XOR/XNOR GATE AT VDD=1.8V

Technology/ Input states(A,B,C)	Basic	Lector (With high V_T)	Percentage saving (With high V_T)
90nm			
OFF STATES	**Leakage current(nA)**		
(1,0,0)	173.68	72.69	58.14%
(1,1,1)	173.68	72.69	58.14%
(0,0,1)	173.68	72.69	58.14%
ON STATES	**Static current(nA)**		
(1,1,0)	52.68	11.17	78.79%
(0,1,1)	52.68	11.17	78.79%
(0,0,0)	52.68	11.17	78.79%
65nm			
OFF STATES	**Leakage current(nA)**		
(1,0,0)	315.81	100.08	68.31%
(1,1,1)	315.81	100.08	68.31%

(0,0,1)	315.81	100.08	68.31%
ON STATES	**Static current(nA)**		
(1,0,0)	146.48	17.78	87.86%
(0,1,1)	146.48	17.78	87.86%
(0,0,0)	146.48	17.78	87.86%
45nm			
OFF STATES	**Leakage current(nA)**		
(1,0,0)	671.48	170.60	74.59%
(1,1,1)	671.48	170.60	74.59%
(0,0,1)	671.48	170.60	74.59%
ON STATES	**Static current(nA)**		
(1,1,0)	708.65	40.70	94.25%
(0,1,1)	708.65	40.70	94.25%
(0,0,0)	708.65	40.70	94.25%

TABLE 3.10
LEAKAGE CURRENT MEASUREMENT FOR BASIC AND LECTOR DCVSL 3-INPUT XOR/XNOR GATE AT VDD=1.2V

Technology/ Input states(A,B,C)	Basic	Lector (With high V_T)	Percentage saving (With high V_T)
90nm			
OFF STATES	**Leakage current(nA)**		
(1,0,0)	33.82	20.68	38.85%
(1,1,1)	33.82	20.68	38.85%
(0,0,1)	33.82	20.68	38.85%
ON STATES	**Static current(nA)**		
(1,1,0)	6.06	2.36	61.05%
(0,1,1)	6.06	2.36	61.05%
(0,0,0)	6.06	2.36	61.05%
65nm			
OFF STATES	**Leakage current(nA)**		
(1,0,0)	41.85	22.24	46.85%
(1,1,1)	41.85	22.24	46.85%
(0,0,1)	41.85	22.24	46.85%
ON STATES	**Static current(nA)**		
(1,0,0)	8.67	2.62	69.78%
(0,1,1)	8.67	2.62	69.78%
(0,0,0)	8.67	2.62	69.78%
45nm			
OFF STATES	**Leakage current(nA)**		
(1,0,0)	62.31	25.99	58.28%
(1,1,1)	62.31	25.99	58.28%

(0,0,1)	62.31	25.99	58.28%
ON STATES	Static current(nA)		
(1,1,0)	16.71	3.42	79.53%
(0,1,1)	16.71	3.42	79.53%
(0,0,0)	16.71	3.42	79.53%

It can be observed from Table 3.9 and Table 3.10 that percentage saving obtained in leakage and static current for VDD=1.8V is 58%-79% for 90nm, 68%-87% for 65nm and 74%-94% for 45nm. For VDD=1.2V, percentage saving achieved is 39%-61% for 90nm, 47%-69% for 65nm and 58%-79% for 45nm.

6. Three input hybrid DCVSL XOR/XNOR gate (TYPE1=>TG+ stacking)

Three input hybrid DCVSL XOR/XNOR gate of TYPE 1 is a combination of transmission gate logic (TGL) and stacking. XOR/XNOR of inputs A and B is realised using TGL and applied to the input of lowest stack. Upper stack is driven by the third input C. Structure of proposed 3-input Hybrid DCVSL XOR/XNOR gate (TYPE 1) shown in fig.3.13 and LECTOR incorporated configuration of 3-input Hybrid DCVSL XOR/XNOR gate (TYPE 1) shown in fig.3.14 are simulated with input conditions given as – load capacitances = 10ff, inputs A, B and C with period=4us, rise time (fall time) = 0.1us, width=2us and delay of 0.5us between different inputs, for different technologies.

Leakage currents corresponding to OFF states and static currents corresponding to ON states for different technologies and for proposed and LECTOR configuration are tabulated in Table 3.11 and Table 3.12 for VDD=1.8V and VDD=1.2V respectively.

TABLE 3.11
LEAKAGE CURRENT MEASUREMENT FOR PROPOSED AND LECTOR 3-INPUT HYBRID DCVSL XOR/XNOR GATE (TYPE 1) AT VDD=1.8V

Technology/ Input states(A,B,C)	Proposed	Lector (With high V_T)	Percentage saving (With high V_T)
90nm			
OFF STATES	Leakage current(nA)		
(1,0,0)	91.38	30.96	66.11%
(1,1,1)	91.38	30.96	66.11%
(0,0,1)	91.38	30.96	66.11%
ON STATES	Static current(nA)		
(1,1,0)	52.43	10.83	79.34%
(0,1,1)	52.43	10.83	79.34%
(0,0,0)	52.43	10.83	79.34%

65nm			
OFF STATES	**Leakage current(nA)**		
(1,0,0)	176.55	43.33	75.45%
(1,1,1)	176.55	43.33	75.45%
(0,0,1)	176.55	43.33	75.45%
ON STATES	**Static current(nA)**		
(1,1,0)	145.25	17.00	88.29%
(0,1,1)	145.25	17.00	88.29%
(0,0,0)	145.25	17.00	88.29%
45nm			
OFF STATES	**Leakage current(nA)**		
(1,0,0)	399.18	76.33	80.87%
(1,1,1)	399.18	76.33	80.87%
(0,0,1)	399.18	76.33	80.87%
ON STATES	**Static current(nA)**		
(1,1,0)	689.68	36.52	94.70%
(0,1,1)	689.68	36.52	94.70%
(0,0,0)	689.68	36.52	94.70%

TABLE 3.12
LEAKAGE CURRENT MEASUREMENT FOR PROPOSED AND LECTOR 3-INPUT HYBRID DCVSL XOR/XNOR GATE (TYPE 1) AT VDD=1.2V

Technology/ Input states(A,B,C)	**Proposed**	**Lector (With high V_T)**	**Percentage saving (With high V_T)**
90nm			
OFF STATES	**Leakage current(nA)**		
(1,0,0)	15.56	8.68	44.21%
(1,1,1)	15.56	8.68	44.21%
(0,0,1)	15.56	8.68	44.21%
ON STATES	**Static current(nA)**		
(1,1,0)	6.05	2.29	62.14%
(0,1,1)	6.05	2.29	62.14%
(0,0,0)	6.05	2.29	62.14%
65nm			
OFF STATES	**Leakage current(nA)**		
(1,0,0)	19.95	9.42	52.78%
(1,1,1)	19.95	9.42	52.78%
(0,0,1)	19.95	9.42	52.78%
ON STATES	**Static current(nA)**		
(1,1,0)	8.64	2.51	70.94%
(0,1,1)	8.64	2.51	70.94%

(0,0,0)	8.64	2.51	70.94%
45nm			
OFF STATES	Leakage current(nA)		
(1,0,0)	31.33	11.19	64.28%
(1,1,1)	31.33	11.19	64.28%
(0,0,1)	31.33	11.19	64.28%
ON STATES	Static current(nA)		
(1,1,0)	16.66	3.11	81.33%
(0,1,1)	16.66	3.11	81.33%
(0,0,0)	16.66	3.11	81.33%

It can be observed from Table 3.11 and Table 3.12 that percentage saving obtained in leakage and static current for VDD=1.8V is 66%-79% for 90nm, 75%-88% for 65nm and 81%-95% for 45nm. For VDD=1.2V, percentage saving achieved is 44%-62% for 90nm, 53%-71% for 65nm and 64%-81% for 45nm.

7. Three input hybrid DCVSL XOR/XNOR gate (TYPE2=> complete TG)

Three input hybrid DCVSL XOR/XNOR gate of TYPE 2 uses transmission gate logic (TGL) for desired logic implementation which is applied as input to DCVSL circuit. Proposed 3-input Hybrid DCVSL XOR/XNOR gate (TYPE2) shown in fig.3.15 and LECTOR incorporated version of 3-input Hybrid DCVSL XOR/XNOR gate (TYPE2) shown in fig.3.16 are simulated with input conditions given as – load capacitances = 10ff, inputs A, B and C with period=4us, rise time (fall time) = 0.1us, width=2us and delay of 0.5us between different inputs, for different technologies. Leakage currents arise in cases where output is supposed to be at logic '1' and PDN is OFF allowing no current flow through it. Such input combinations are OFF states. Similarly, ON states correspond to static current. Table 3.13 and Table 3.14 give leakage and static current values for Proposed and LECTOR configuration of 3-input Hybrid DCVSL XOR/XNOR gate (TYPE 2) for VDD=1.8V and VDD=1.2V respectively.

TABLE 3.13

LEAKAGE CURRENT MEASUREMENT FOR PROPOSED AND LECTOR 3-INPUT HYBRID DCVSL XOR/XNOR GATE (TYPE 2) AT VDD=1.8V

Technology/ Input states(A,B,C)	Proposed	Lector (With high V_T)	Percentage saving (With high V_T)
90nm			
OFF STATES	Leakage current(nA)		
(1,0,0)	30.71	5.68	79.74%
(1,1,1)	30.71	5.68	79.74%
(0,0,1)	30.71	5.68	79.74%

ON STATES	Static current(nA)		
(1,1,0)	52.23	10.00	80.85%
(0,1,1)	52.23	10.00	80.85%
(0,0,0)	52.23	10.00	80.85%
65nm			
OFF STATES	Leakage current(nA)		
(1,0,0)	65.58	8.16	87.75%
(1,1,1)	65.58	8.16	87.75%
(0,0,1)	65.58	8.16	87.75%
ON STATES	Static current(nA)		
(1,1,0)	144.20	15.20	89.45%
(0,1,1)	144.20	15.20	89.45%
(0,0,0)	144.20	15.20	89.45%
45nm			
OFF STATES	Leakage current(nA)		
(1,0,0)	168	15.72	90.64%
(1,1,1)	168	15.72	90.64%
(0,0,1)	168	15.72	90.64%
ON STATES	Static current(nA)		
(1,1,0)	673.34	30.48	95.47%
(0,1,1)	673.34	30.48	95.47%
(0,0,0)	673.34	30.48	95.47%

TABLE 3.14

LEAKAGE CURRENT MEASUREMENT FOR PROPOSED AND LECTOR 3-INPUT HYBRID DCVSL XOR/XNOR GATE (TYPE 2) AT VDD=1.2V

Technology/ Input states(A,B,C)	Proposed	Lector (With high V_T)	Percentage saving (With high V_T)
90nm			
OFF STATES	Leakage current(nA)		
(1,0,0)	3.74	1.55	58.55%
(1,1,1)	3.74	1.55	58.55%
(0,0,1)	3.74	1.55	58.55%
ON STATES	Static current(nA)		
(1,1,0)	6.04	2.16	64.23%
(0,1,1)	6.04	2.16	64.23%
(0,0,0)	6.04	2.16	64.23%
65nm			
OFF STATES	Leakage current(nA)		
(1,0,0)	5.18	1.69	67.37%
(1,1,1)	5.18	1.69	67.37%

(0,0,1)	5.18	1.69	67.37%
ON STATES	**Static current(nA)**		
(1,1,0)	8.68	2.30	73.50%
(0,1,1)	8.68	2.30	73.50%
(0,0,0)	8.68	2.30	73.50%
45nm			
OFF STATES	**Leakage current(nA)**		
(1,0,0)	8.80	2.04	76.81%
(1,1,1)	8.80	2.04	76.81%
(0,0,1)	8.80	2.04	76.81%
ON STATES	**Static current(nA)**		
(1,1,0)	16.55	2.80	83.08%
(0,1,1)	16.55	2.80	83.08%
(0,0,0)	16.55	2.80	83.08%

It can be observed from Table 3.13 and Table 3.14 that percentage saving obtained in leakage and static current for VDD=1.8V is 80%-81% for 90nm, 88%-89% for 65nm and 91%-95% for 45nm. For VDD=1.2V, percentage saving achieved is 58%-64% for 90nm, 67%-73% for 65nm and 77%-83% for 45nm.

Figure 3.21 shows the comparison between leakage current of basic DCVSL 2-input XOR (i.e. all stacking) and hybrid DCVSL configuration for 2-input XOR/XNOR at 1.2V. It can be easily observed that hybrid configuration has reduced leakage currents than the basic fully stacked configuration.

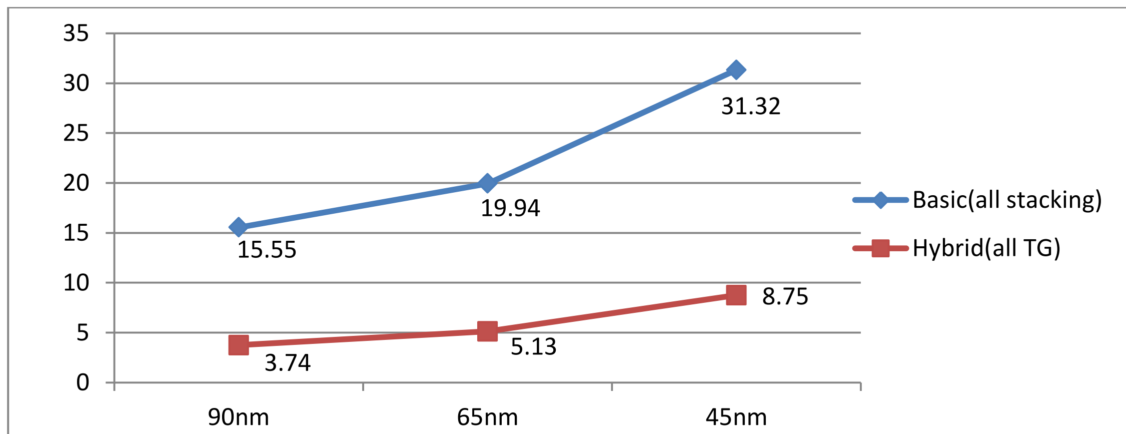


Fig. 3.21 Leakage current (nA) comparison between Basic and Hybrid DCVSL configurations for 2-input XOR/XNOR at 1.2V

Figure 3.22 shows that leakage current is minimum for Type 2 (all TG) configuration of hybrid DCVSL 3 input XOR/XNOR gate. Type 1 (TG+stacking) configuration is having slightly greater leakage current than Type 2 and basic (all stacking) structure is having the highest of all. Effectiveness of inclusion TG in gate configuration in leakage current reduction can be observed from fig. 3.22.

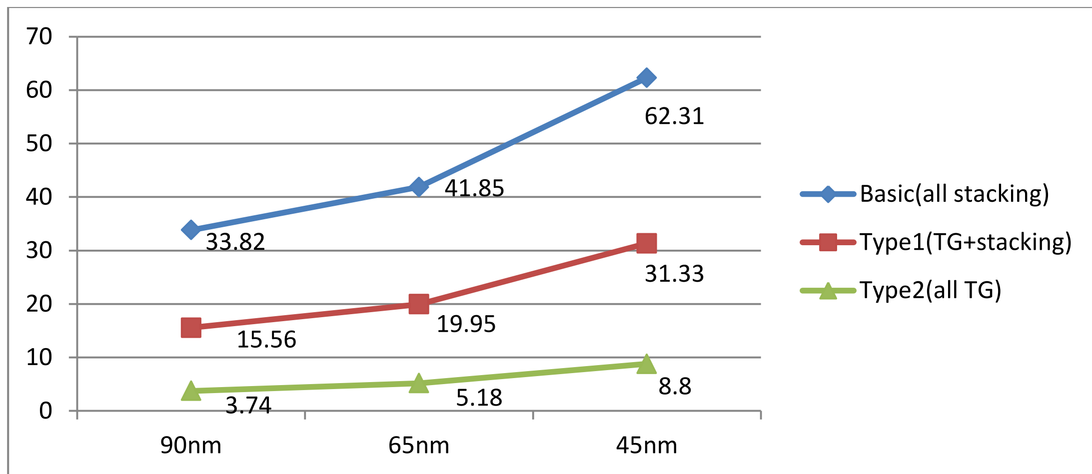


Fig. 3.22 Leakage current (nA) comparison between Basic, Hybrid type1 (TG+stacking) and hybrid Type2 (all TG) DCVSL configurations for 3-input XOR/XNOR at 1.2V

TEMPERATURE VARIATION

(At 45nm technology and power supply=1.2)

The pattern followed by leakage current with variation in temperature has been studied via performing temperature variation on the circuits simulated above for temperature values -25°C, 27°C and 100°C.

- **DCVSL inverter**

Temperature	Leakage current(nA)	
	Basic	Lector
-25°C	3.16	0.587
27°C	8.74	2.02
100°C	23.96	6.95

- **Basic DCVSL 2 input XOR gate (all stacking)**

OFF STATES	Leakage current at temperature(nA)		
	-25°C	27°C	100°C
(1,0)	10.67	31.32	91.31
(0,1)	10.67	31.32	91.31

- **LECTOR DCVSL 2 input XOR gate (all stacking)**

OFF STATES	Leakage current at temperature (nA)		
	-25°C	27°C	100°C
(1,0)	3.27	11.18	37.59
(0,1)	3.27	11.18	37.59

- **Proposed Hybrid DCVSL 2 input XOR gate (all TG)**

OFF STATES	Leakage current at temperature (nA)		
	-25°C	27°C	100°C
(1,0)	3.16	8.75	24.09
(0,1)	3.16	8.75	24.09

- **LECTOR Hybrid DCVSL 2 input XOR gate (all TG)**

OFF STATES	Leakage current at temperature(nA)		
	-25°C	27°C	100°C
(1,0)	0.587	2.03	6.99
(0,1)	0.587	2.03	6.99

- **Proposed Hybrid DCVSL 3 input XOR gate (one level TG + stacking)**

OFF STATES	Leakage current at temperature (nA)		
	-25°C	27°C	100°C
(1,0,0)	10.67	31.33	91.50
(1,1,1)	10.67	31.33	91.50
(0,0,1)	10.67	31.33	91.50

- **LECTOR Hybrid DCVSL 3 input XOR gate (one level TG + stacking)**

OFF STATES	Leakage current at temperature(nA)		
	-25°C	27°C	100°C
(1,0,0)	3.27	11.20	37.36
(1,1,1)	3.27	11.20	37.36
(0,0,1)	3.27	11.20	37.36

- **Proposed Hybrid DCVSL 3 input XOR gate (all TG)**

OFF STATES	Leakage current at temperature(nA)		
	-25°C	27°C	100°C
(1,0,0)	3.17	8.80	24.44
(1,1,1)	3.17	8.80	24.44
(0,0,1)	3.17	8.80	24.44

- **LECTOR Hybrid DCVSL 3 input XOR gate (all TG)**

OFF STATES	Leakage current at temperature(nA)		
	-25°C	27°C	100°C
(1,0,0)	0.588	2.04	7.07
(1,1,1)	0.588	2.04	7.07
(0,0,1)	0.588	2.04	7.07

DELAY CALCULATIONS

The output nodes in DCVSL circuits generally have unequal rise and fall times due to an in-built asymmetry in NMOS tree (pull down network) and PMOS load (pull up transistor). Considering the DCVSL circuit given in fig 3.1(a), the voltage at the drain node of NMOS transistor (which is also connected to the gate of PMOS transistor of the differential branch) falls slowly. This results in a situation where the low-to-high switching time (T_{PLH}) (the delay from the input signal dropping from logic high to logic low to the output signal rising from logic low to logic high) is greater than the high-to-low switching propagation delay (T_{PHL}) [21].

Proposed LECTOR incorporated and Hybrid structures are investigated for their timing parameters to study the trade-off occurring between leakage power and delay due to newly introduced circuitry for the purpose of leakage control. Following tables are the results of delay calculations performed for the basic and proposed configurations of two input and three input XOR gates.

- ## Two input XOR DCVSL gate (all stacking)

Input conditions: VDD=1.8V, Technology =45nm, Period=200ns, Width=100ns, t_r=2ns, t_f =2ns, t_d=50ns

TABLE 3.15

DELAY MEASUREMENT FOR BASIC DCVSL 2-INPUT XOR GATE

A	B	Output	Delay
0->1	**0**	0->1	400ps
1->0	**0**	1->0	160ps
0->1	**1**	1->0	148ps
1->0	**1**	0->1	416ps
0	**0->1**	0->1	290ps
0	**1->0**	1->0	250ps
1	**0->1**	1->0	240ps
1	**1->0**	0->1	304ps

It can be observed from Table 3.15 that DCVSL has unequal rise and fall delays. The low to high transition is greater than the high to low transition due to the reason discussed in section 3.6.

TABLE 3.16

DELAY MEASUREMENT FOR LECTOR INCORPORATED DCVSL 2-INPUT XOR GATE

A	B	Output	Delay
0->1	**0**	0->1	682ps
1->0	**0**	1->0	68ps
0->1	**1**	1->0	57ps

1->0	**1**	0->1	680ps
0	**0->1**	0->1	583ps
0	**1->0**	1->0	81ps
1	**0->1**	1->0	80ps
1	**1->0**	0->1	533ps

It can be inferred from Table 3.16 that average delay ((rise time + fall time)/2) increases for LECTOR incorporated DCVSL configuration as compared to the basic DCVSL structure. But when we observe closely we can see that low to high transition duration increases whereas high to low transition time decreases.

- **Two input hybrid DCVSL XOR gate (all TG)**

Input conditions: VDD=1.8V, Technology =45nm, Period=200ns, Width=100ns, t_r=2ns, t_f=2ns, t_d=50ns

TABLE 3.17
DELAY MEASUREMENT FOR 2-INPUT BASIC HYBRID DCVSL XOR GATE

A	B	Output	Delay
0->1	**0**	0->1	560ps
1->0	**0**	1->0	520ps
0->1	**1**	1->0	396ps
1->0	**1**	0->1	510ps
0	**0->1**	0->1	590ps
0	**1->0**	1->0	560ps
1	**0->1**	1->0	550ps
1	**1->0**	0->1	590ps

TABLE 3.18
DELAY MEASUREMENT FOR 2-INPUT LECTOR INCORPORATED HYBRID DCVSL XOR GATE

A	B	Output	Delay
0->1	**0**	0->1	690ps
1->0	**0**	1->0	350ps
0->1	**1**	1->0	342ps
1->0	**1**	0->1	700ps
0	**0->1**	0->1	850ps
0	**1->0**	1->0	610ps
1	**0->1**	1->0	600ps
1	**1->0**	0->1	860ps

It can be observed from Table 3.18 that hybrid configuration slightly increases the delay of the basic DCVSL circuits. Table 3.17 shows the delays for 2-input basic hybrid DCVSL XOR Gate which when compared to delay for basic DCVSL in Table 3.15 shows that hybrid configuration pays delay overhead for reduced leakage current. But the

percentage leakage saving achieved is comparatively greater than the percentage increase in delay. As we can see from Table 3.18 that LECTOR technique increases the low to high delay and decreases high to low delay for input A transiting.

- **Three input DCVSL XOR gate (all stacking)**

Input conditions: VDD=1.8V, Technology =45nm, Period=200ns, Width=100ns, t_r =1ns, t_f =1ns, Td=50ns

Calculating delay for only worst cases

Worst case discharging happens when all intermediate (internal node) capacitances are charged and they all need to be discharged. This can happen when the input to the lowest transistor close to ground makes a transition from 0 to 1. And since there is only one pull up transistor, it is difficult to find the worst cases among all for charging.

TABLE 3.19
DELAY MEASUREMENT FOR 3-INPUT BASIC DCVSL XOR GATE (ALL STACKING)

A	B	C	Output	Delay
0->1	**1**	**0**	1->0	46ps
1->0	**0**	**0**	1->0	45ps
1->0	**1**	**1**	1->0	49ps
0->1	**0**	**1**	1->0	48ps

TABLE 3.20
DELAY MEASUREMENT FOR 3-INPUT LECTOR INCORPORATED DCVSL XOR GATE (ALL STACKING)

A	B	C	Output	Delay
0->1	**1**	**0**	1->0	77ps
1->0	**0**	**0**	1->0	114ps
1->0	**1**	**1**	1->0	77ps
0->1	**0**	**1**	1->0	114ps

Table 3.21 gives the delay values for the worst cases of 3-input basic DCVSL XOR gate. Table 3.22 gives the delay values for the worst cases of 3-input LECTOR incorporated DCVSL XOR gate and shows that LECTOR slightly increases the delay of basic EDCVSL configuration.

- **Three input Hybrid DCVSL XOR gate (TYPE1=>TG+ stacking)**

Input conditions: VDD=1.8V, Technology =45nm, Period=200ns, Width=100ns, t_r=1ns, t_f =1ns, Td=50ns

TABLE 3.21

DELAY MEASUREMENT FOR 3-INPUT BASIC HYBRID DCVSL XOR GATE (TYPE1=>TG+ STACKING)

A	B	C	Output	Delay
0->1	**1**	**0**	1->0	124ps
1->0	**0**	**0**	1->0	149ps
1->0	**1**	**1**	1->0	124ps
0->1	**0**	**1**	1->0	148ps

TABLE 3.22

DELAY MEASUREMENT FOR 3-INPUT LECTOR INCORPORATED HYBRID DCVSL XOR GATE (TYPE1=>TG+ STACKING)

A	B	C	Output	Delay
0->1	**1**	**0**	1->0	192ps
1->0	**0**	**0**	1->0	196ps
1->0	**1**	**1**	1->0	193ps
0->1	**0**	**1**	1->0	198ps

Comparing delay values for 3-input XOR gate for fully stacked and hybrid configuration TYPE1 given by Table 3.21 and Table 3.23 respectively shows that TG configuration increases the delay of the circuit. Incorporation of LECTOR further increases the delay of hybrid DCVSL slightly.

- **Three input Hybrid DCVSL XOR gate (TYPE2=> COMPLETE TG)**

Input conditions: VDD=1.8V, Technology =45nm, Period=200ns, Width=100ns, t_r=1ns, t_f =1ns, Td=50ns

TABLE 3.23

DELAY MEASUREMENT FOR 3-INPUT BASIC HYBRID DCVSL XOR GATE (TYPE2=> COMPLETE TG)

A	B	C	Output	Delay
0->1	**1**	**0**	1->0	358ps
1->0	**0**	**0**	1->0	358ps
1->0	**1**	**1**	1->0	361ps
0->1	**0**	**1**	1->0	358ps

TABLE 3.24
DELAY MEASUREMENT FOR 3-INPUT LECTOR INCORPORATED HYBRID DCVSL XOR GATE (TYPE2=> COMPLETE TG)

A	B	C	Output	Delay
0->1	**1**	**0**	1->0	350ps
1->0	**0**	**0**	1->0	348ps
1->0	**1**	**1**	1->0	351ps
0->1	**0**	**1**	1->0	347ps

Comparing delay values for 3-input XOR gate for fully stacked, hybrid configuration TYPE1 and TYPE2 given by Table 3.21, Table 3.23 and Table 3.25 respectively shows that delay increases from basic all stacking to complete TG hybrid configuration. TG configuration increases the delay of the circuit. Integration of LECTOR adds up to the delay of hybrid DCVSL slightly.

Chapter 4

Enhanced Differential Cascode Voltage Switch Logic (Dynamic DCVSL) and Special Structures

4.1 INTRODUCTION

DCVS logic tree is greatly simplified by Enhanced Differential Cascode Voltage Switch Logic [17] which results in dramatic reduction in the interconnect count by elimination of the complementary inputs required for the differential branch and still retains the attributes of basic DCVSL. EDCVSL indicates reduced power consumption when compared to the conventional DCVSL design while preserving all advantages of basic DCVSL. The chapter gives an insight to the dynamic DCVS logic and enhanced DCVS logic, explores their advantages over the conventional DCVSL and ascertains the ways to control leakage loss using different approaches and structures.

4.2 DYNAMIC DCVSL

Various clocked versions of DCVSL have been brought in light over the years in order to enhance the performance and minimise the power consumption of the logic circuit. One of the dynamic circuits is shown in figure 4.1(b). It consists of two complementary pull down networks and has positive feedback in the form of the two cross-coupled PMOS pull-up transistors. When clock signal is low, OUT and OUTB are pre-charged to V_{DD}. This is called pre-charge phase. When CLK raises to logic high; NMOS logic tree evaluates to attain its true and complementary output state upon assertion of input signals. Proper switching of the logic gate is achieved by the positive feedback which is being applied to PMOS pull-up transistors (M3 and M4). Additional accelerating circuitry in the form of NMOS transistors M5 and M6 are employed to improve the performance of the dynamic DCVSL gate. Dynamic DCVSL has a significant advantage of reduced power consumption over conventional static DCVSL logic designs. The state of contention which used to take place while switching in case of static DCVSL is now eliminated.

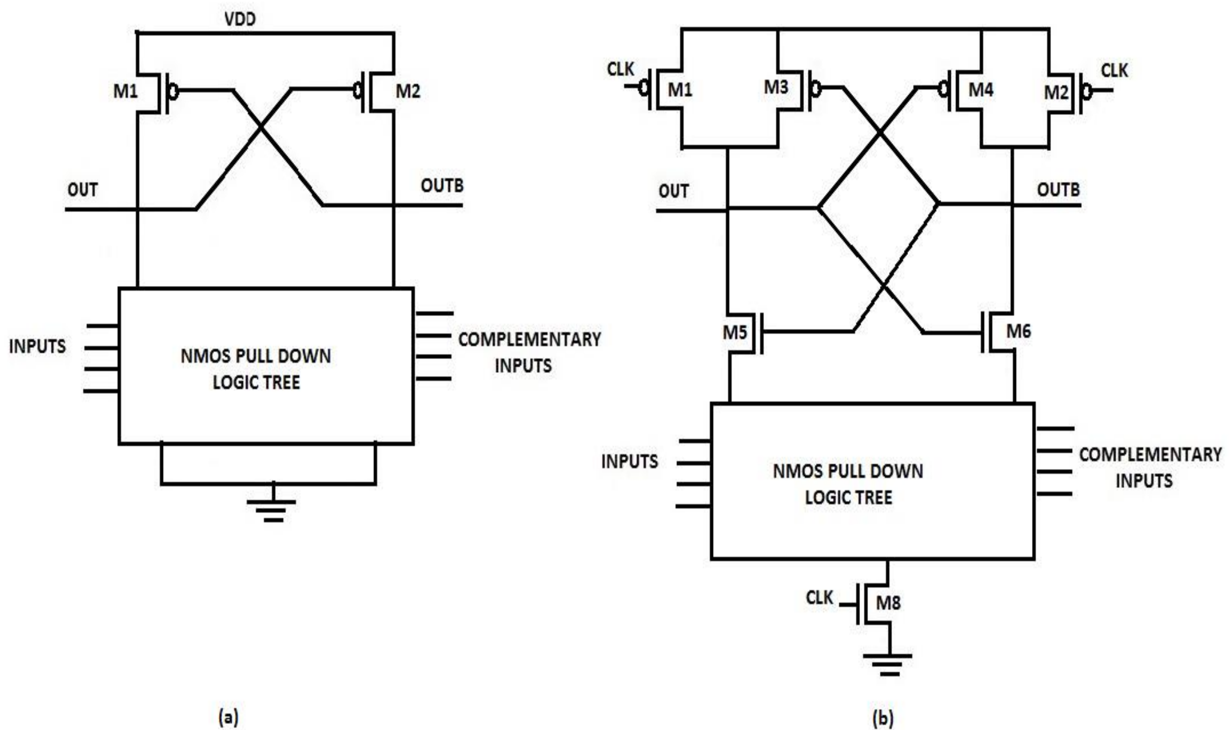


Fig. 4.1 DCVSL: (a) Static version, and (b) Dynamic version

In case of static DCVSL, gate of either of the PUTS is at logic '1' and other one is at logic '0' as they are connected to complementary output nodes. Looking at figure 3.1 let us consider the case where the output node (OUT) has to switch from '1' to '0' which indicates that complementary output node (OUTbar) has to make a switch from '0' to '1'. As inputs are asserted, PDN1 turns ON and tries to discharge OUT. But the task of discharging is made difficult by PUT1 which is still ON since OUTbar is at logic '0'. This raises a state of conflict between PUT and PDN where PDN tries to pull down and PUT tries to pull up. Consequence of contention is static power dissipation within that duration. Now if we analyse the case of dynamic DCVSL, OUT and OUTbar are both charged to V_{DD} during pre-charge cycle. This indicates that PUT1 and PUT2 both are initially in OFF state. PUTs get turned ON conditionally depending upon inputs asserted. This drives away the problem of contention since none of the PUT is ON initially.

4.3 ENHANCED DIFFERENTIAL CASCODE VOLTAGE SWITCH LOGIC

Enhanced differential cascode voltage switch logic is an improved version of dynamic DCVSL. EDCVSL interestingly eliminates the transistors required for complementary inputs. Reduction in transistor count increases the speed of the gate as well.

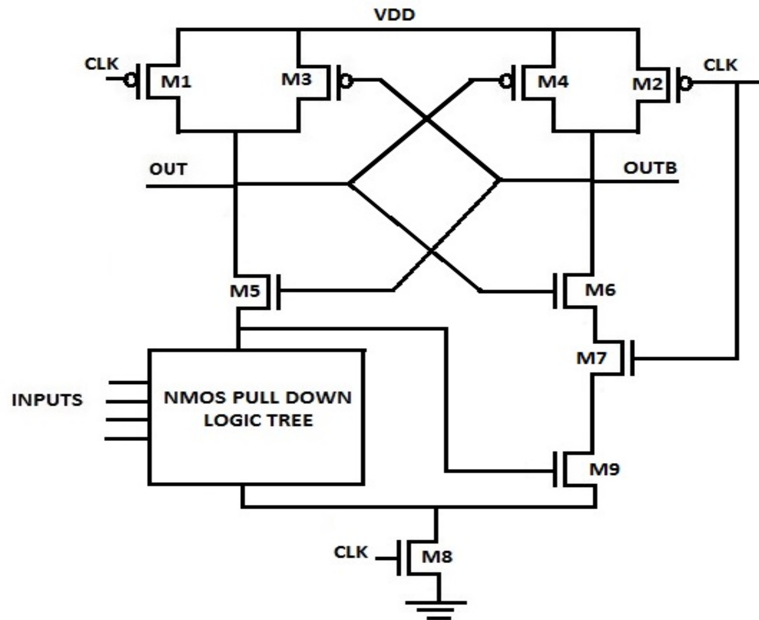


Fig.4.2 Basic architecture of EDCVSL

4.3.1 Architecture and Operation

Basic architecture of EDCVSL is shown in figure 4.2. Operation of EDCVSL can be divided into two phases- i) pre-charge ii) evaluation. In pre-charge phase nodes OUT and OUTB are charged up to V_{DD} with the help of PMOS pre-charge transistors M1 and M2 which get turned on when CLK=0. The feedback transistors M3 and M4 are during pre-charge phase since gate voltages driving them are logic high at that moment. When CLK=1, the circuit is in the phase of evaluation, the pre-charge transistors Ml and M2 get turned OFF, whereas transistors M7 and M8 driven by CLK signal get turned ON building a path for current from the two pre-charged output nodes OUTB and OUT to ground via EDCVS logic tree depending upon the inputs asserted. The feedback transistors M3 and M4 are for speeding up the evaluation and maintaining the correct logic levels. The complete complementary input network is replaced by a single transistor M9 which is controlled by voltage at the intermediary output node (which is the source terminal of M5) of the other differential rail which retains logic high when there is no path for current flow or logic low when the EDCVS tree turns on and allows current to flow during evaluation phase. The complementary output in case of EDCVSL is generated by pulling a wire out of intermediate output node (source terminal of M5) and feeding it to the gate terminal of NMOS transistor M9 which inverts the applied signal to generate its complement.

4.3.2 Advantages of EDCVS logic design

EDCVSL possess all the good features of DCVS logic and in addition to those have certain advantageous features over DCVSL. Some of them are discussed below-

1. Simplification of logic tree eliminates the complementary input signals and efficiently lessens the total number of interconnects of the logic circuit. This improves the speed of the circuit.

2. Charge sharing problem in a dynamic logic circuit is proportional to the depth of logic tree since a deep logic tree has a lot of intermediate nodes which share charge from the output node. Charge sharing problem at the output loses its severity when parallel structure is used for logic tree realisation. Proposed EDVSL enables the utilisation of only parallel structure for evaluation logic tree implementation whereas it is a necessity for conventional DCVSL to employ both series and parallel structures.

4.3.3 Modified LECTOR incorporated EDCVSL approach

Enhanced DCVS logic designs have also been seen to suffer leakage power loss, though less due to dynamic configuration. Since feedback transistors in EDCVSL maintain the connection between V_{DD} and output node, there are chances of leakage currents along the path from VDD to ground. Therefore, a LECTOR incorporated EDCVSL structure has been proposed to combat the leakage currents flowing from V_{DD} to ground when there should be no current at all. Leakage control mechanism of LECTOR for DCVSL has already been discussed in the previous chapter how it cuts off leakage currents through the path. Exactly same concept applies to EDCVSL for leakage regulation.

Fig 4.3 Modified LECTOR incorporated generic EDCVSL circuit

a) Architecture

Basic structure of LECTOR incorporated modified EDCVSL is exactly same as that of basic EDCVSL except the inclusion of four leakage control transistors (LCT1, LCT2, LCT3, and LCT4), two on each branch (true logic and complementary).

b) Leakage conditions and control mechanism

Leakage currents are those currents which flow through the branch when PDN doesn't conduct and output node is supposed to be at logic high. These situations arise in both pre-charge and evaluation phases. Consider figure 4.2, during pre-charge phase, the output is supposed to be at logic high irrespective of the input conditions since NMOS transistor M8 driven by clock is OFF for CLK=0. Turned off M8 transistor blocks the path for current to ground and hence the current should ideally be zero in such condition. But the subthreshold leakage currents through OFF transistors along the path manage to flow and reach the ground terminal. During evaluation phase, for input conditions which don't turn ON the PDN, the output node is preserves its logic high state as there is no current path provided by the logic tree. Nevertheless, there is a leakage current flow through OFF transistors in the evaluation logic tree. Henceforth, LECTOR configuration has been adapted for EDCVSL as well which efficiently controls the leakage current flow.

4.4 Proposed Hybrid dynamic DCVSL and EDCVSL Configurations

Hybrid configuration for DCVSL was discussed in the previous chapter in section 3.5.2. The same concept is applied to dynamic DCVSL and EDCVSL. Reduction in number of source coupled stacked transistors pairs reduces the leakage current as explained earlier. To take advantage of this concept, hybrid configurations for dynamic DCVSL and EDCVSL have been built. In hybrid technique of logic realisation transmission gates are used to implement a part of logic and the rest of it is realised by dynamic DCVS or EDCVS logic.

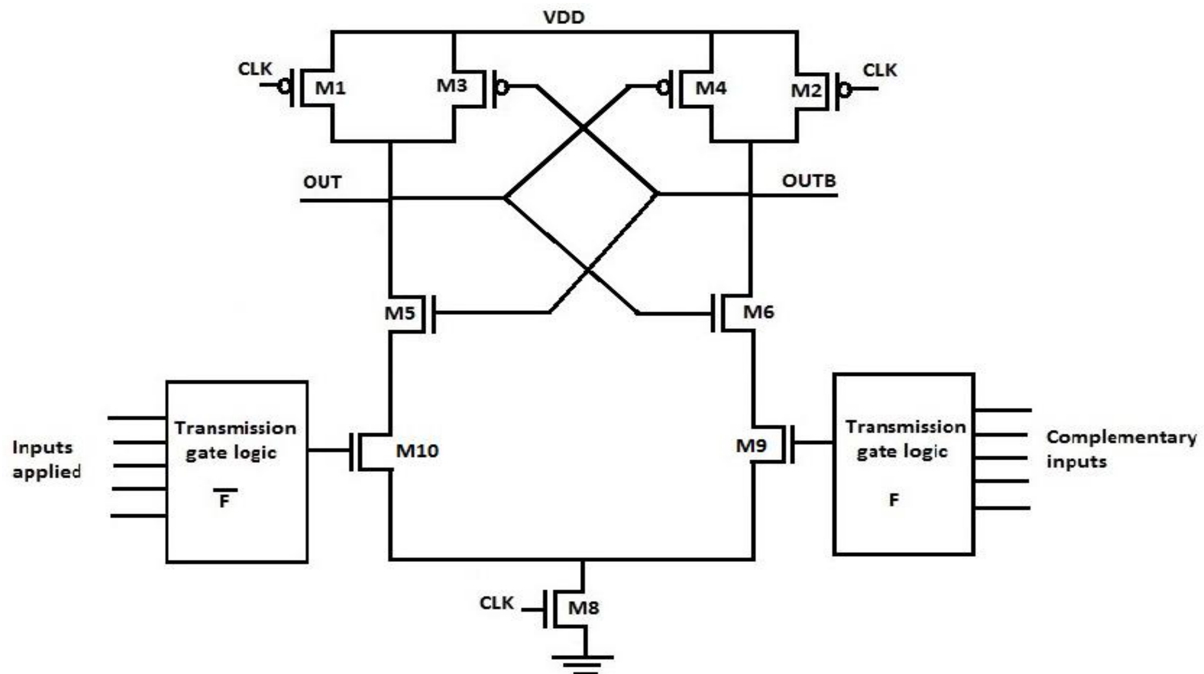


Fig.4.4 Basic architecture of a generic Hy-DyDCVSL circuit

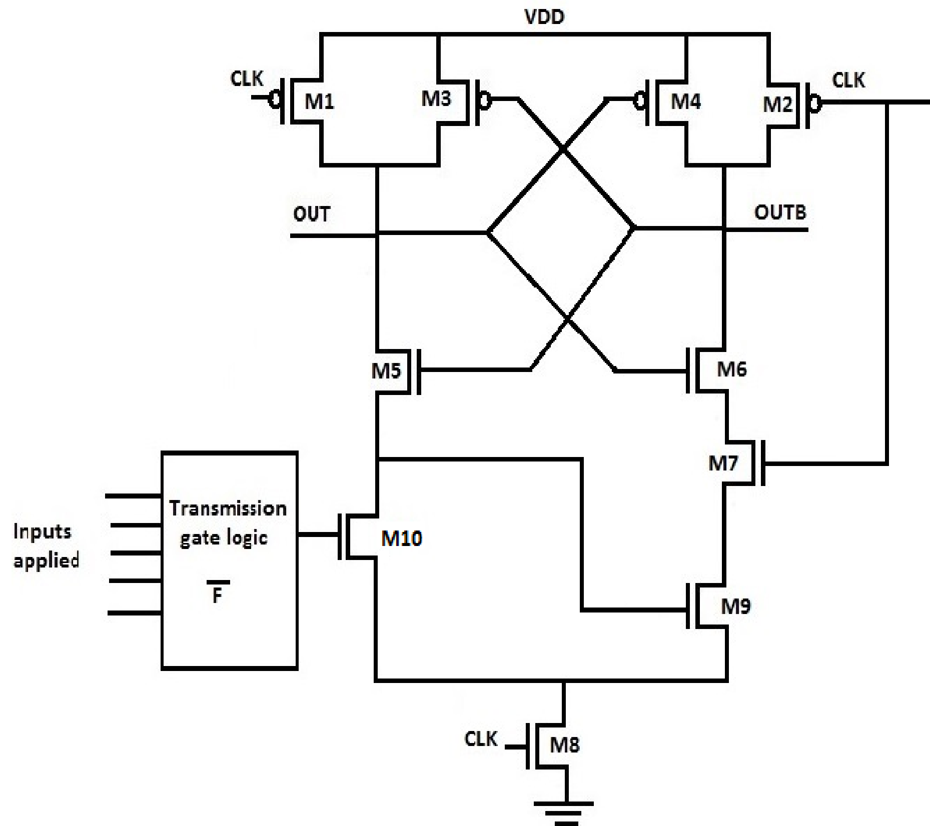


Fig.4.5 Basic architecture of a generic Hy-EDCVSL circuit

The generic architectures of hybrid dynamic DCVSL (referred to as Hy-DyDCVSL) and hybrid EDCVSL (referred to as Hy-EDCVSL) are shown above in Fig 4.4 and Fig 4.5 respectively.

Hybrid configurations for 2-input and 3-input XOR gates for dynamic DCVS/EDCVS logic have been proposed along with their LECTOR incorporated configurations as shown below.

4.4.1 2-Input XOR EDCVSL Gate

Hybrid configuration of 2-input XOR involves realisation of XNOR of the two inputs using transmission gate logic and feeding it to the input of basic EDCVS logic circuit. First TGL is evaluated and the evaluated logic is applied to the input transistor M1 which then inverts the fed logic to produce the required XOR functionality. The intermediate output at the source of M10 is fed to transistor M9 on the differential branch to produce its desired complemented logic as shown in Fig 4.6.

a) **Basic hybrid EDCVSL**

Fig.4.6 Basic hybrid EDCVSL 2-input XOR gate

b) **LECTOR hybrid EDCVSL**

Fig.4.7 LECTOR hybrid EDCVSL 2-input XOR gate

4.4.2 3-Input XOR dynamic DCVSL Gate

3-input XOR is realised using hybrid dynamic DCVSL configuration which consists of only two-level stacking instead of three level stacking in case of conventional design. One of the source coupled transistor pair level is reduced by realising XOR of two inputs using

TGL and applying it to the lowest level stack. The upper level stack is constructed by using the same approach as earlier for conventional design.

a) **Basic Hybrid dynamic DCVSL (TG+ two level stacking)**

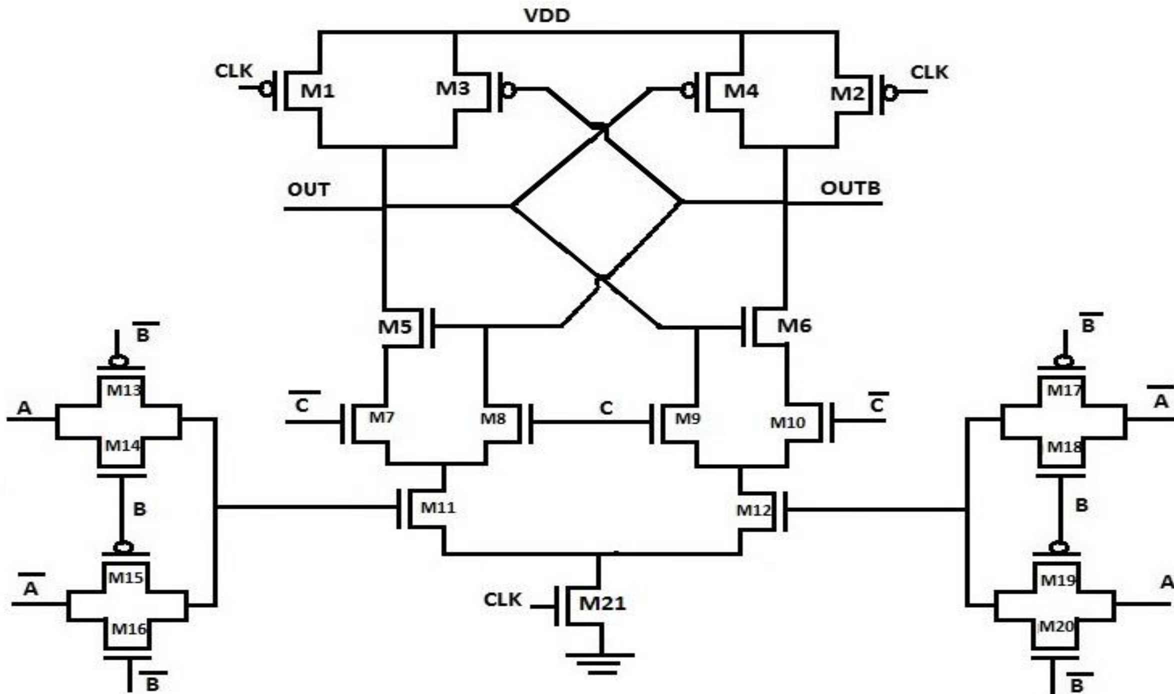


Fig.4.8 Basic Hybrid dynamic DCVSL 3-input XOR

b) **LECTOR Hybrid dynamic DCVSL (TG+ two level stacking)**

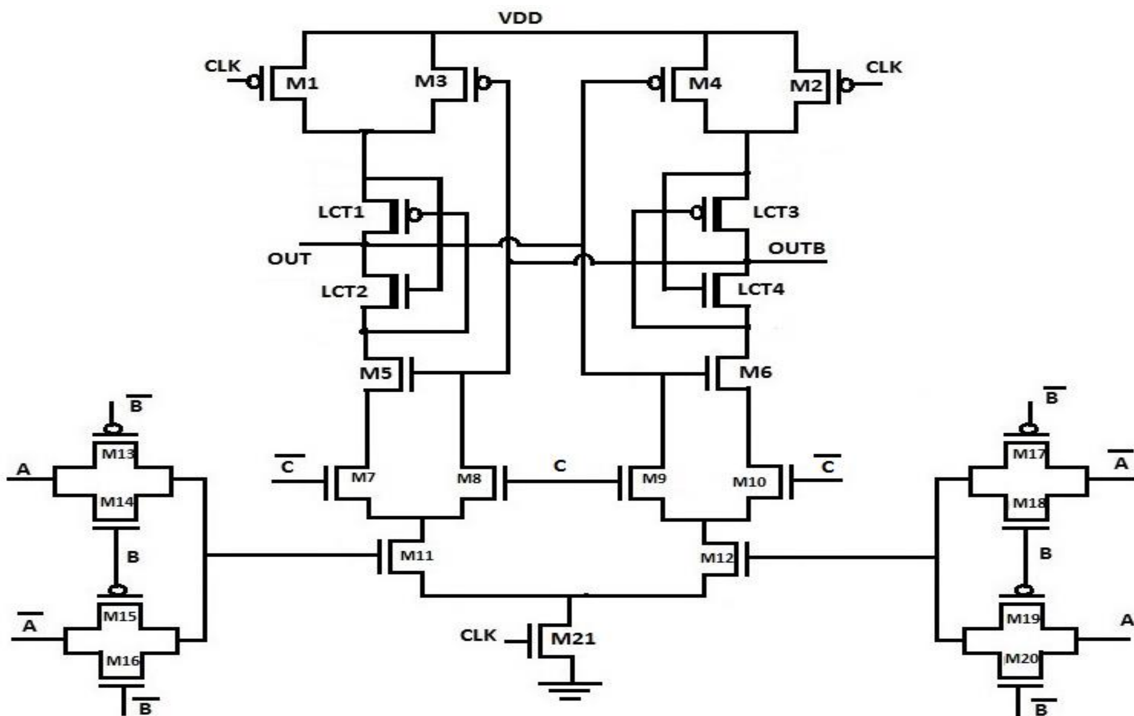


Fig.4.9 LECTOR Hybrid dynamic DCVSL 3-input XOR

4.5 SPECIAL CONFIGURATIONS FOR DCVSL

4.5.1 NP mixed DCVSL

NP mixed DCVSL technique adopts both N and P type transistors to build pull down network or we can say DCVS logic tree. The concept behind this approach is that PMOS transistors have comparatively lesser subthreshold and gate oxide leakage currents [18]. A comparison of normalised values of gate oxide and subthreshold leakage currents for high Vt and low Vt PMOS and NMOS transistors has been tabulated for different temperatures in Table 4.1.

TABLE 4.1
NORMALIZED GATE OXIDE AND SUBTHRESHOLD LEAKAGE CURRENTS OF THE HIGH-VT AND LOW-VT TRANSISTORS AT DIFFERENT TEMPERATURES [18]

Subthreshold and gate oxide leakage current	NMOS		PMOS	
	Low-Vt	High-Vt	Low-Vt	High-Vt
I_{sub} (110°C)	22.3	2.6	16.01	1.0
I_{gate}(110°C)	3.3	0.05	0.097	0.0003
I_{sub} (25°C)	3.7	1.9	3.1	1.0
I_{gate}(25°C)	9.4	0.15	0.31	0.001

From comparison Table 4.1 it can be inferred that PMOS transistors are far less leaky than NMOS transistors in every condition as it suppresses subthreshold and gate oxide leakage effectively but at the expense of speed. N-type DCVS logic tree has higher speed and higher leakage power consumption whereas NP mixed DCVS logic tree has lesser leakage currents and higher delays. A conventional DCVSL can be converted into NP mixed DCVSL by replacing those NMOS transistors with PMOS who have complementary inputs and using true signal input for these PMOS instead of its complement. This eliminates the extra inverters required to obtain complement of the original signals thus reducing power consumption due to these inverters. Basic architecture proposed for a 2 input XOR gate using NP mixed DCVS logic design approach is shown below in the Fig 4.10. The circled transistors shown in Fig 4.10 are the PMOS transistors in pull down network which have replaced NMOS transistors which were driven by complementary input signals. Now those complementary inputs are replaced by true inputs to PMOS transistors.

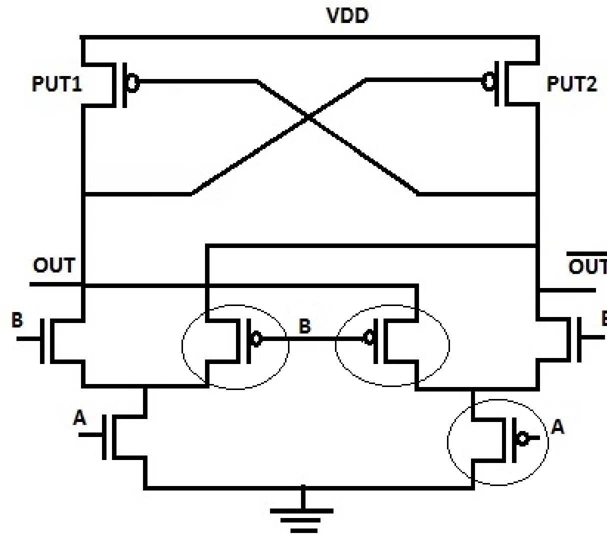


Fig.4.10 NP mixed DCVSL 2 input XOR gate

4.5.2 Differential Static CMOS Logic (DSCL)

a) Problem with conventional DCVSL: A DCVSL gate rather than having a complete pull up logic tree consists of two back to back connected pull up PMOS transistors forming a feedback latch which is used to transmute the logic 0 on one rail to logic 1 on its complementary rail.

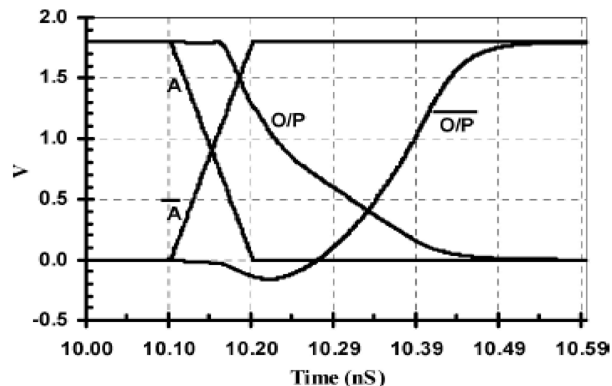


Fig. 4.11 Input and output waveforms for DCVSL gate [25]

This indicates that the output transition from low-to-high (L-H) is always going to trail behind the output transition from high-to-low (H-L) as can be seen in Fig. 4.11. Besides the output undergoing a switching from logic high-to-low suffers through a situation of contention between the pull down network (DCVS logic tree) and the pull-up PMOS transistor which remains ON initially. This contention results in slower last portion of high-to-low output transition which can be evidently seen in Fig. 4.11. This leads to performance degradation of DCVSL gate in the form of-

1. A lower speed as the low-to-high edge is always trailing behind the high-to-low edge. Moreover, since the high-to-low transition is commenced by the low-to-high transition at the input, this effect gets added up for multi stage DCVS logic.
2. High momentary static power dissipation due to the initial contention between PDN and PUT.

b) DSCL configuration

DSCL configuration is a remedy for the problems discussed above. DSCL gate can be obtained from DCVS logic gate by adding a PMOS logic tree pull up network in parallel to the existing PMOS feedback transistors [19] as shown in Fig. 4.13. Considering a two input XOR/XNOR gate structure, DSCL implementation requires only 14 transistors as compared to the requirement of 18 transistors in [20]. DSCL thereby shows 22% reduction in transistor count for 2-input XOR/XNOR gate and even more for higher fan-in gates (e.g. approximately 45% saving for 3-input XOR/XNOR gate). The output Low-to-high transition would now be starting in unison with high-to-low transition on the other rail due to the addition of PMOS pull up logic tree as shown in Fig.4.12. Cross-coupled PMOS pull-up latch is still preserved to provide assistance while pulling up action though the size of PMOS latch has been made smaller since pull up process is now not its sole responsibility as it was in DCVSL. In DSCL, it is PMOS logic tree which majorly performs the pull up action. This helps in reducing the contention between PUT and PDN to a great extent. The positive consequence of this effect can be seen in the form of almost equalisation of low-to-high and high-to-low transition times [19].

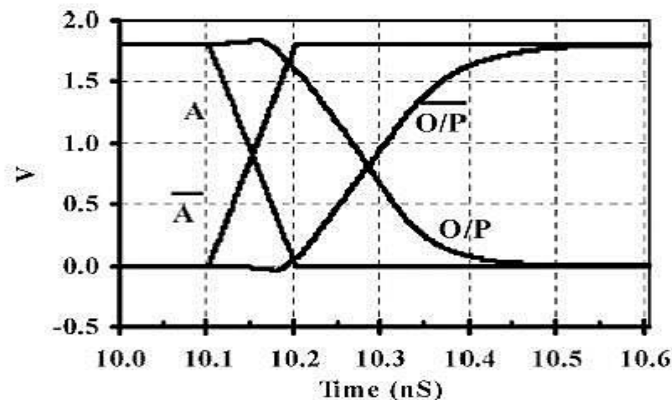


Fig. 4.12 Input and output waveforms for DSCL gate [19]

DSCL shows a great saving in terms of peak supply current drawn while switching. Figure 4.13 shows peak supply current for DSCL is nearly one third of that for DCVSL.

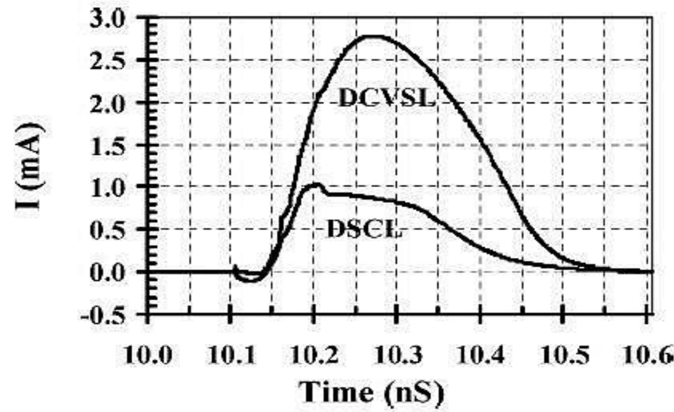


Fig. 4.13 Peak supply currents for the DCVSL and the new DSCL While output switching [19]

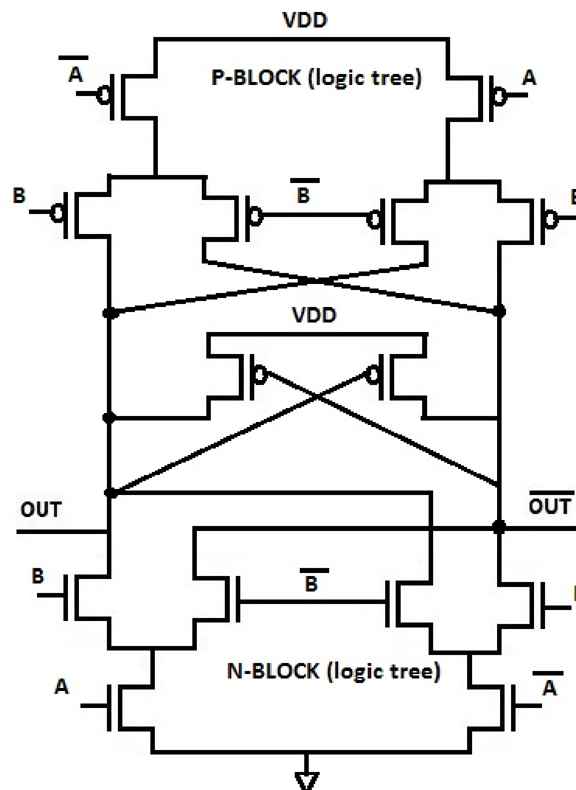


Fig. 4.14 Basic architecture for a 2-input XOR/XNOR DSCL gate [19]

c) Proposed LECTOR incorporated DSCL configuration

Figure 4.15 presents the proposed low power configuration of DSCL i.e. LECTOR incorporated DSCL. Leakage control transistors inserted in between P-logic tree and N-logic tree perform the leakage control mechanism as was explained in previous chapters and provides the above discussed advantages over conventional DCVSL along with leakage control facility.

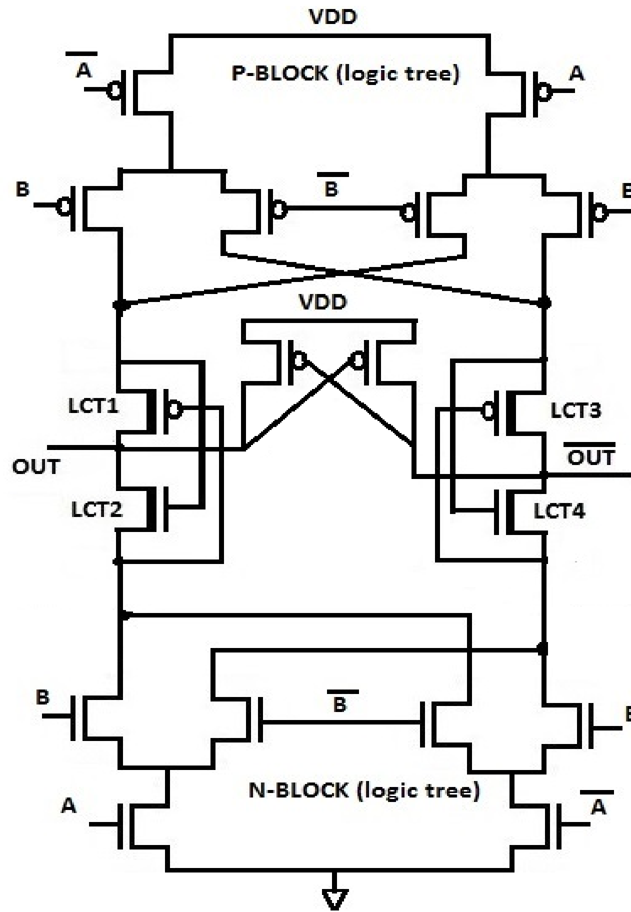


Fig 4.15 Architecture of LECTOR incorporated 2-input XOR/XNOR DSCL gate

4.6 SIMULATION RESULTS AND DISCUSSIONS

Simulations for all proposed and existing dynamic DCVSL circuits have been performed at different technology nodes (90nm, 65nm and 45nm) for different power supplies and comparison in terms of leakage current has been drawn and percentage saving is obtained.

1. EDCVSL inverter/buffer

Figure 4.16 shows the structure of basic EDCVSL (enhanced differential cascode voltage switch logic) inverter/buffer. This represents enhanced dynamic version of DCVSL inverter/buffer. Being a dynamic circuit it has two modes of operation-i)pre-charge and ii)evaluation. Leakage current may occur in both pre-charge and evaluation phase. During pre-charge phase, evaluation transistor (nmos6) is OFF allowing no path for current through PDN and thereby the output should remain at logic one for any input combination. But leakage current makes its path to the ground during pre-charge phase which is undesirable. During evaluation phase, input combinations which turn the PDN

OFF correspond to leakage current. However, ON states during evaluation phase turn ON the PDN and correspond to static current.

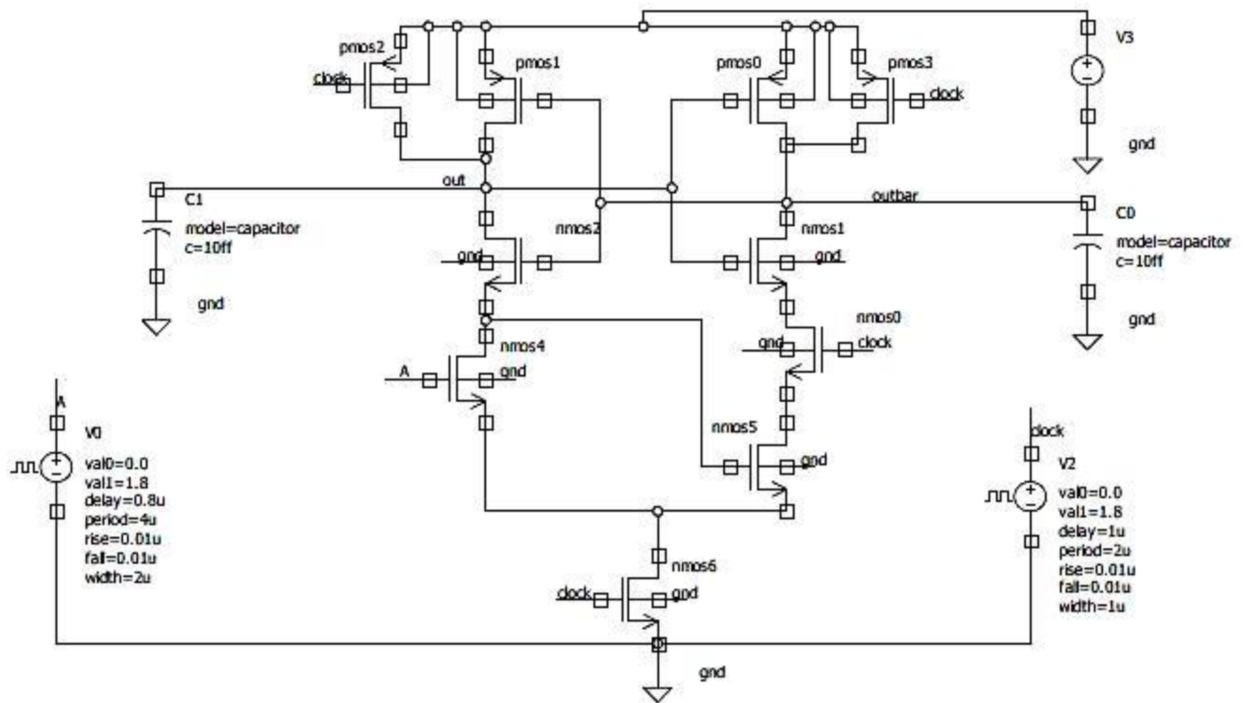


Fig. 4.16 Basic EDCVSL Inverter/Buffer

Figure 4.17 shows the LECTOR incorporated configuration of EDCVSL Inverter/Buffer used for leakage current reduction. Leakage current and static current values for different phases of operation of the circuit and the percentage savings are given by Table 4.2 and Table 4.3 for VDD=1.8V and VDD=1.2V respectively.

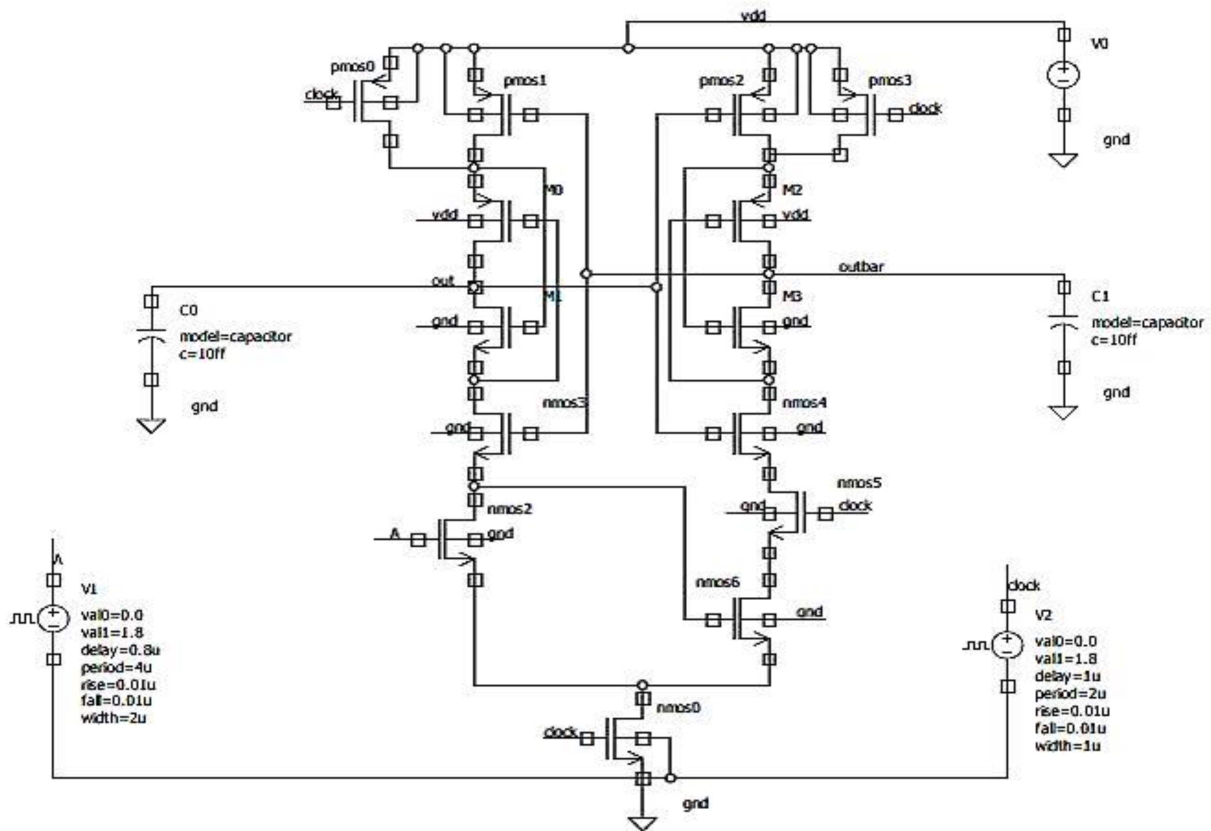


Fig. 4.17 LECTOR incorporated EDCVSL Inverter/Buffer

TABLE 4.2
LEAKAGE CURRENT MEASUREMENT FOR BASIC AND LECTOR EDCVSL INVERTER/BUFFER AT VDD=1.8V

Technology/ Input states(A,B)		Basic	Lector (With high V_T)	Percentage saving (With high V_T)
90nm				
OFF STATES		**Leakage current**		
Precharge	**0**	0.883	0.570	35.49%
	1	6.50	5.59	15.38%
Evaluation	**0**	0.288	0.266	7.6%
ON STATES		**Static current**		
Evaluation	**1**	130.42	42.48	67.42%
65nm				
OFF STATES		**Leakage current**		
Precharge	**0**	1.55	1.01	34.80%
	1	9.15	7.82	14.53%
Evaluation	**0**	0.258	0.226	12.09%
ON STATES		**Static current**		
Evaluation	**1**	323.46	65.97	79.6%

45nm				
OFF STATES		Leakage current		
Precharge	0	1.45	0.955	34.30%
	1	15.56	13.17	15.36%
Evaluation	0	0.239	0.180	24.68%
ON STATES		Static current		
Evaluation	1	1220	95.60	92.20%

TABLE 4.3

LEAKAGE CURRENT MEASUREMENT FOR BASIC AND LECTOR EDCVSL INVERTER/BUFFER AT VDD=1.2V

Technology/ Input states(A,B)		Basic	Lector (With high V_T)	Percentage saving (With high V_T)
90nm				
OFF STATES		Leakage current		
Precharge	0	0.100	0.095	5.00%
	1	1.77	1.54	12.99%
Evaluation	0	0.236	0.192	18.64%
ON STATES		Static current		
Evaluation	1	13.04	5.12	60.73%
65nm				
OFF STATES		Leakage current		
Precharge	0	0.123	0.105	14.63%
	1	1.96	1.67	14.79%
Evaluation	0	0.193	0.155	19.68%
ON STATES		Static current		
Evaluation	1	19.21	5.03	73.81%
45nm				
OFF STATES		Leakage current		
Precharge	0	0.140	0.086	38.57%
	1	2.38	1.94	18.48%
Evaluation	0	0.210	0.122	41.90%
ON STATES		Static current		
Evaluation	1	34.73	7.54	78.28%

It can be observed from Table 4.2 and Table 4.3 that percentage saving obtained in leakage and static current for VDD=1.8V is 8%-67% for 90nm, 12%-79% for 65nm and 25%-92% for 45nm. For VDD=1.2V, percentage saving achieved is 5%-61% for 90nm, 14%-74% for 65nm and 18%-78% for 45nm.

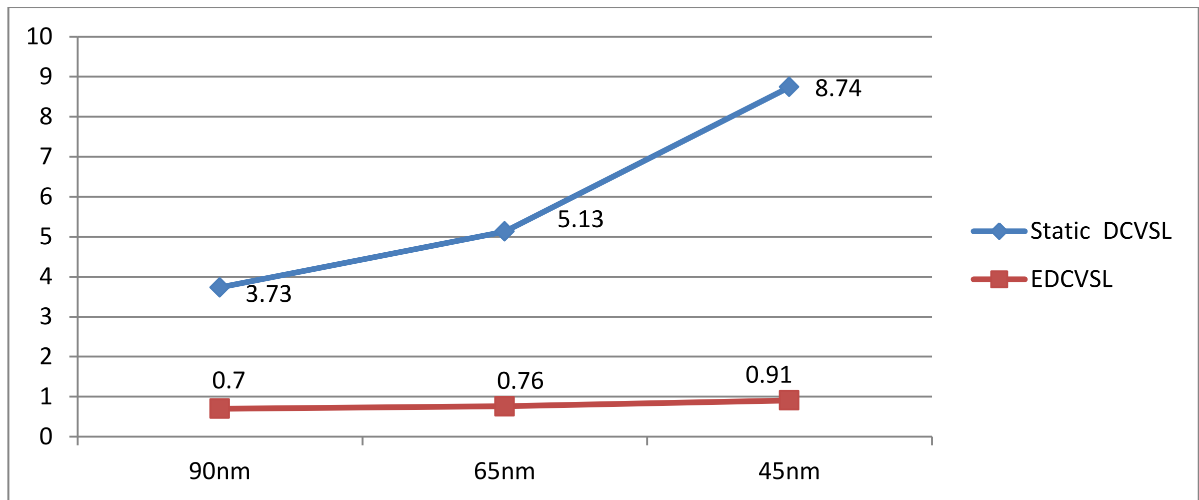


Fig. 4.18 Average leakage current comparison for static DCVSL and dynamic EDCVSL inverter

Figure 4.18 shows that leakage current is significantly less in case of dynamic DCVSL as compared to static DCVSL.

2. Two input XOR /XNOR EDCVSL gate (all stacking)

Figure 4.19 and fig. 4.20 present the basic and LECTOR incorporated configurations of EDCVSL 2-input XOR gate.

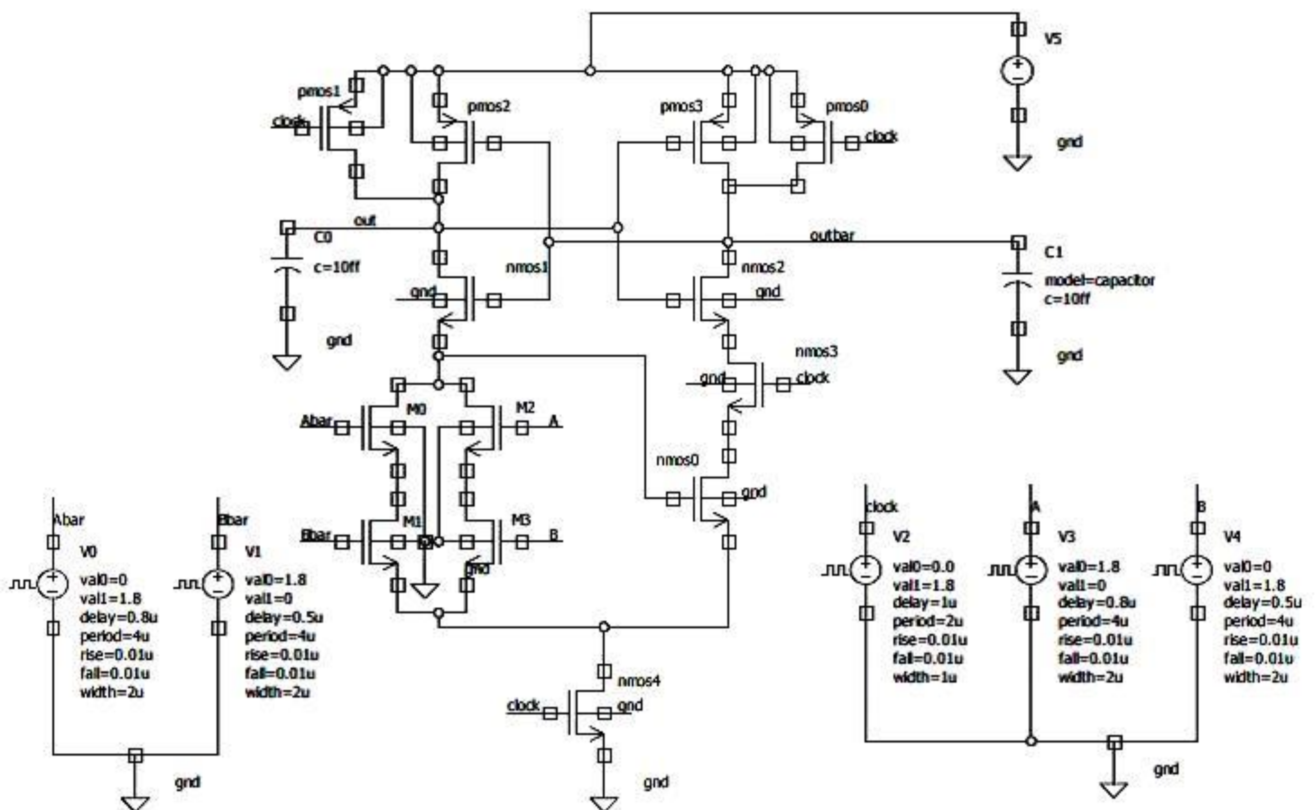


Fig. 4.19 Basic EDCVSL 2-input XOR gate (all stacking)

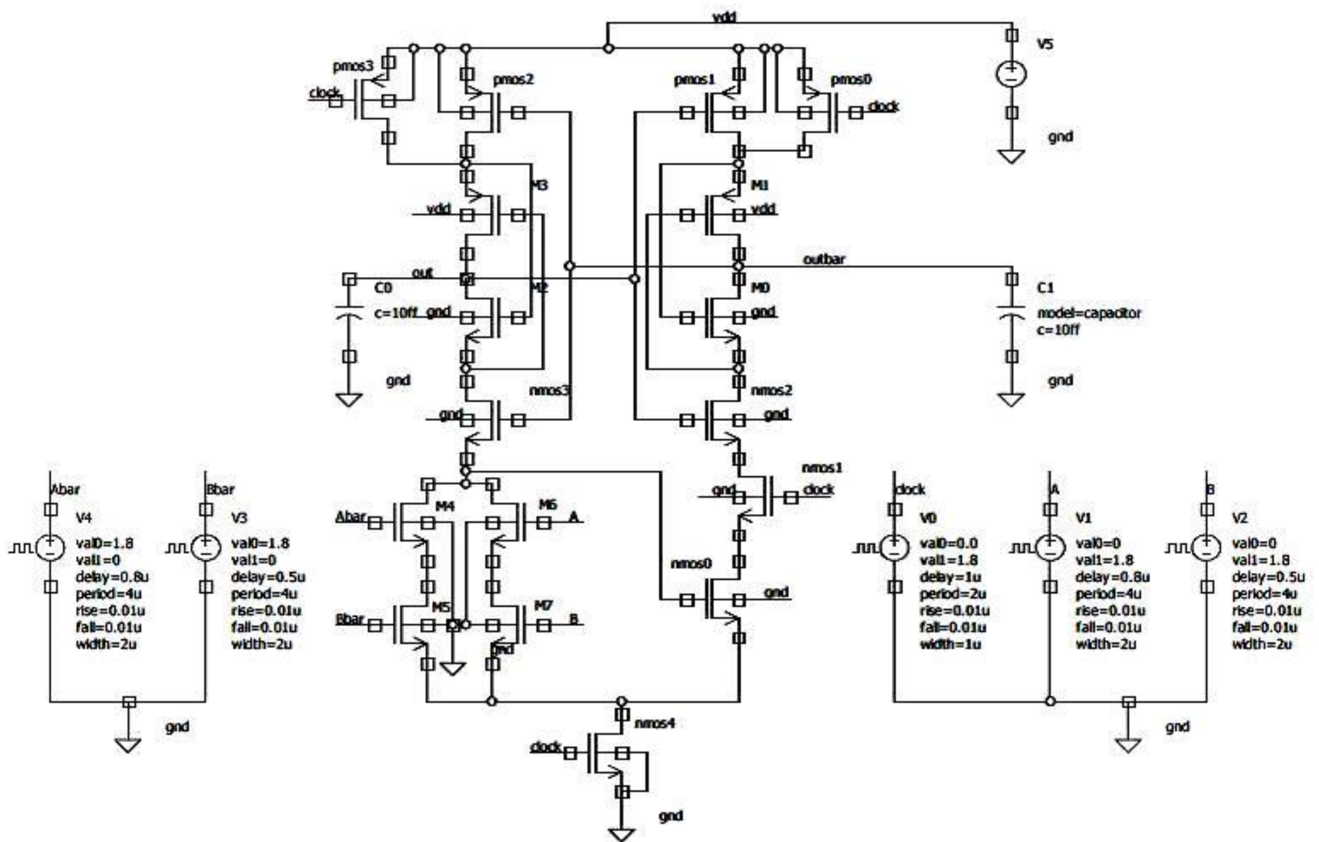


Fig. 4.20 LECTOR incorporated EDCVSL 2-input XOR gate (all stacking)

Table 4.4 and Table 4.5 give the leakage and static current values for corresponding ON and OFF states in pre-charge and evaluation phases for basic and LECTOR configuration with VDD=1.8V and VDD=1.2V respectively. Percentage saving for each input state is also given in the tables.

TABLE 4.4
LEAKAGE CURRENT MEASUREMENT FOR BASIC AND LECTOR EDCVSL 2-INPUT XOR GATE (ALL STACKING) AT VDD=1.8V

Technology/ Input states(A,B)		Basic	Lector (With high V_T)	Percentage saving (With high V_T)
90nm				
OFF STATES		**Leakage current**		
Precharge	**(0,0)**	8.89	7.20	19.01%
	(0,1)	3.13	2.11	32.58%
	(1,1)	8.89	7.20	19.01%
	(1,0)	3.13	2.11	32.58%
Evaluation	**(1,0)**	0.028	0.010	64.28%
	(0,1)	0.028	0.010	64.28%
ON STATES		**Static current**		
Evaluation	**(1,1)**	130.20	42.44	67.40%
	(0,0)	130.20	42.44	67.40%

65nm				
OFF STATES		**Leakage current**		
Precharge	**(0,0)**	13.50	10.74	20.44%
	(0,1)	5.50	3.78	31.27%
	(1,1)	13.50	10.74	20.44%
	(1,0)	5.50	3.78	31.27%
Evaluation	**(1,0)**	0.041	0.041	-
	(0,1)	0.041	0.041	-
ON STATES		**Static current**		
Evaluation	**(1,1)**	322.30	65.81	79.58%
	(0,0)	322.30	65.81	79.58%
45nm				
OFF STATES		**Leakage current**		
Precharge	**(0,0)**	19.5	15.76	19.17%
	(0,1)	5.32	3.67	31.01%
	(1,1)	19.5	15.76	19.17%
	(1,0)	5.32	3.67	31.01%
Evaluation	**(1,0)**	0.040	0.038	5.00%
	(0,1)	0.040	0.038	5.00%
ON STATES		**Static current**		
Evaluation	**(1,1)**	1225	95.31	92.21%
	(0,0)	1225	95.31	92.21%

TABLE 4.5

LEAKAGE CURRENT MEASUREMENT FOR BASIC AND LECTOR EDCVSL 2-INPUT XOR GATE (ALL STACKING) AT VDD=1.2V

Technology/ Input states(A,B)		**Basic**	**Lector (With high V_T)**	**Percentage saving (With high V_T)**
90nm				
OFF STATES		**Leakage current**		
Precharge	**(0,0)**	1.93	1.62	16.06%
	(0,1)	0.229	0.144	37.11%
	(1,1)	1.93	1.62	16.06%
	(1,0)	0.229	0.182	37.11%
Evaluation	**(1,0)**	0.128	0.045	64.84%
	(0,1)	0.120	0.046	61.66%
ON STATES		**Static current**		
Evaluation	**(1,1)**	13.04	5.16	60.42%
	(0,0)	13.04	5.16	60.42%
65nm				
OFF STATES		**Leakage current**		
Precharge	**(0,0)**	2.28	1.87	17.98%
	(0,1)	0.445	0.297	33.25%

	(1,1)	2.28	1.87	17.98%
	(1,0)	0.445	0.297	33.25%
Evaluation	**(1,0)**	0.015	0.005	66.67%
	(0,1)	0.016	0.005	66.68%
ON STATES		**Static current**		
Evaluation	**(1,1)**	19.20	6.52	66.04%
	(0,0)	19.20	6.52	66.04%
		45nm		
OFF STATES		**Leakage current**		
Precharge	**(0,0)**	2.66	2.14	19.54%
	(0,1)	0.452	0.306	32.30%
	(1,1)	2.66	2.14	19.54%
	(1,0)	0.452	0.306	32.30%
Evaluation	**(1,0)**	0.020	0.007	65.00%
	(0,1)	0.020	0.007	65.00%
ON STATES		**Static current**		
Evaluation	**(1,1)**	34.72	7.48	78.45%
	(0,0)	34.72	7.48	78.45%

It can be observed from Table 4.4 and Table 4.5 that percentage saving obtained in leakage and static current for VDD=1.8V is 19%-67% for 90nm, 20%-79% for 65nm and 19%-92% for 45nm. For VDD=1.2V, percentage saving achieved is 16%-64% for 90nm, 18%-66% for 65nm and 19%-78% for 45nm.

3. Proposed hybrid EDCVSL two input XOR/XNOR gate (all TG)

Proposed hybrid EDCVSL 2-input XOR/XNOR of A and B is realised using TGL and applied to basic EDCVSL circuit as shown in fig. 4.21. gate and LECTOR incorporated configuration of hybrid EDCVSL 2-input XOR/XNOR gate represented by fig.4.6 and fig 4.7 are simulated for different technologies with input conditions given as – load capacitances = 10ff, inputs A and B with period=4us, rise time (fall time) = 0.1us, width=2us, delay of 0.8us for A and 0.5us for B, Clock period=4us, clock width=1us, clock rise time (fall time)= 0.1us and initial clock delay of 1us.

Table 4.6 and Table 4.7 show the leakage current and static current values for different input combinations for proposed and LECTOR configuration and the percentage saving achieved by LECTOR incorporated structure. Measurement has been done on two supply voltages i.e. VDD=1.8V given by Table 4.6 and VDD=1.2V given by Table 4.7.

TABLE 4.6
LEAKAGE CURRENT MEASUREMENT FOR PROPOSED AND LECTOR HYBRID EDCVSL 2-INPUT XOR/XNOR GATE (ALL TG) AT VDD=1.8V

Technology/ Input states(A,B)		Proposed	Lector (With high V_T)	Percentage saving (With high V_T)
90nm				
OFF STATES		**Leakage current**		
Precharge	**(0,0)**	6.41	5.59	12.79%
	(0,1)	0.866	0.575	33.60%
	(1,1)	6.42	5.59	12.79%
	(1,0)	0.866	0.575	33.60%
Evaluation	**(1,0)**	0.308	0.263	14.61%
	(0,1)	0.308	0.263	14.61%
ON STATES		**Static current**		
Evaluation	**(1,1)**	130.41	42.49	67.41%
	(0,0)	130.41	42.49	67.41%
65nm				
OFF STATES		**Leakage current**		
Precharge	**(0,0)**	8.97	7.81	12.93%
	(0,1)	1.50	1.02	32.00%
	(1,1)	8.97	7.81	12.93%
	(1,0)	1.52	1.02	32.00%
Evaluation	**(1,0)**	0.292	0.229	21.57%
	(0,1)	0.292	0.229	21.57%
ON STATES		**Static current**		
Evaluation	**(1,1)**	323.47	65.97	79.60%
	(0,0)	323.47	65.97	79.60%
45nm				
OFF STATES		**Leakage current**		
Precharge	**(0,0)**	14.49	13.12	9.45%
	(0,1)	1.34	0.947	29.32%
	(1,1)	14.49	13.12	9.45%
	(1,0)	1.35	0.950	29.32%
Evaluation	**(1,0)**	0.337	0.188	44.21%
	(0,1)	0.337	0.188	44.21%
ON STATES		**Static current**		
Evaluation	**(1,1)**	1220	95.61	92.16%
	(0,0)	1220	95.61	92.16%

TABLE 4.7
LEAKAGE CURRENT MEASUREMENT FOR PROPOSED AND LECTOR HYBRID EDCVSL 2-INPUT XOR/XNOR GATE (ALL TG) AT VDD=1.2V

Technology/ Input states(A,B)		Proposed	Lector (With high V_T)	Percentage saving (With high V_T)
90nm				
OFF STATES		**Leakage current**		
Precharge	**(0,0)**	1.77	1.53	13.55%
	(0,1)	0.055	0.037	32.72%
	(1,1)	1.78	1.53	13.55%
	(1,0)	0.055	0.036	32.72%
Evaluation	**(1,0)**	0.244	0.185	24.18%
	(0,1)	0.249	0.182	26.90%
ON STATES		**Static current**		
Evaluation	**(1,1)**	13.04	5.15	60.50%
	(0,0)	13.04	5.15	60.50%
65nm				
OFF STATES		**Leakage current**		
Precharge	**(0,0)**	1.96	1.67	14.79%
	(0,1)	0.119	0.075	36.97%
	(1,1)	1.96	1.67	14.79%
	(1,0)	0.118	0.075	36.97%
Evaluation	**(1,0)**	0.195	0.172	11.79%
	(0,1)	0.196	0.172	11.79%
ON STATES		**Static current**		
Evaluation	**(1,1)**	19.21	6.52	66.05%
	(0,0)	19.21	6.52	66.05%
45nm				
OFF STATES		**Leakage current**		
Precharge	**(0,0)**	2.34	1.96	16.23%
	(0,1)	0.117	0.077	34.18%
	(1,1)	2.34	1.96	16.23%
	(1,0)	0.117	0.077	34.18%
Evaluation	**(1,0)**	0.151	0.122	19.20%
	(0,1)	0.151	0.120	20.52%
ON STATES		**Static current**		
Evaluation	**(1,1)**	34.73	7.57	78.20%
	(0,0)	34.73	7.57	78.20%

It can be observed from Table 4.6 and Table 4.7 that percentage saving obtained in leakage and static current for VDD=1.8V is 13%-67% for 90nm, 13%-79% for 65nm and 9%-92% for 45nm. For VDD=1.2V, percentage saving achieved is 13%-60% for 90nm, 13%-66% for 65nm and 16%-78% for 45nm.

4. Two input XOR/XNOR dynamic DCVSL gate (all stacking)

Figure 4.21 and fig. 4.22 show the basic and LECTOR incorporated configuration of dynamic DCVSL two input XOR/XNOR gate (all stacking). It is similar to static DCVSL 2-input XOR/XNOR gate (all stacking) except the inclusion of pre-charging transistors parallel to pull up transistors.

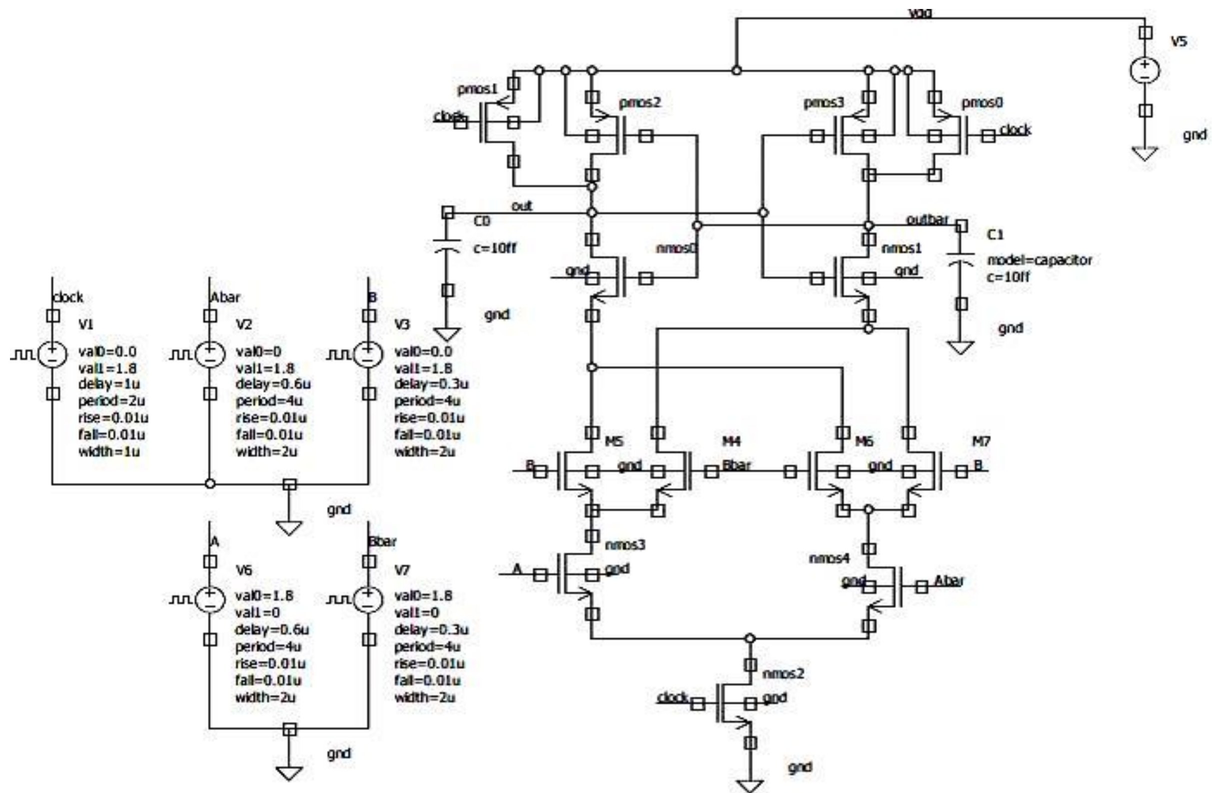


Fig. 4.21 Basic Dynamic DCVSL 2-input XOR/XNOR gate (all stacking)

LECTOR configuration shown in fig. 4.22 achieves reduction in leakage current and static current when compared to basic configuration. Leakage current and static current values for different input combinations, technologies, phase of operation and configurations (basic and LECTOR) are given in Table 4.8 and Table 4.9 for VDD=1.8V and VDD=1.2V respectively. Percentage saving achieved by LECTOR configuration is mentioned in the tables as well.

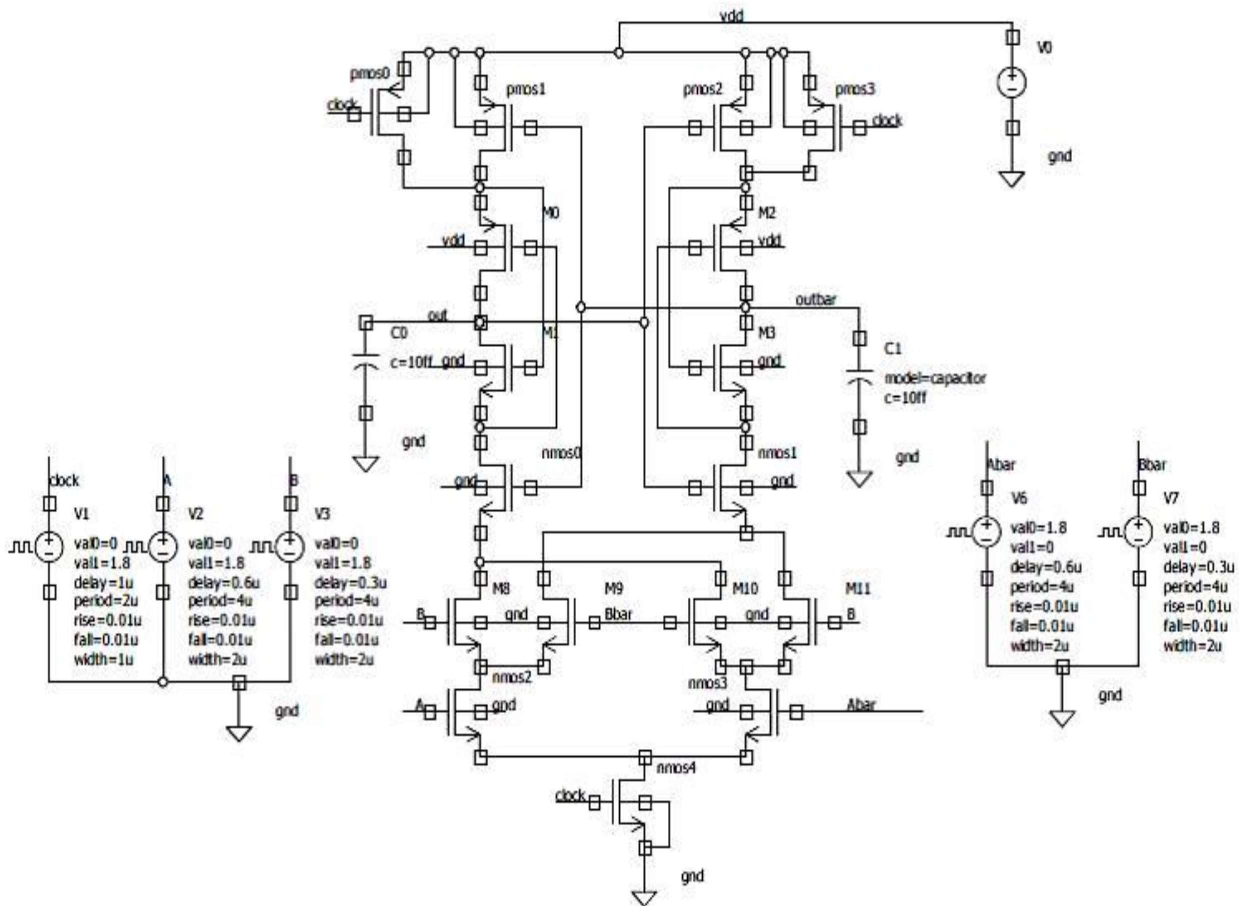


Fig. 4.22 LECTOR incorporated Dynamic DCVSL 2-input XOR/XNOR gate (all stacking)

TABLE 4.8
LEAKAGE CURRENT MEASUREMENT FOR BASIC AND LECTOR INCORPORATED DYNAMIC DCVSL 2-INPUT XOR/XNOR GATE (ALL STACKING) AT VDD=1.8V

Technology/ Input states(A,B)		Basic	Lector (With high V_T)	Percentage saving (With high V_T)
90nm				
OFF STATES		Leakage current		
Precharge	(0,0)	9.84	7.85	20.22%
	(0,1)	4.36	2.99	31.42%
	(1,1)	9.84	7.85	20.22%
	(1,0)	4.36	2.99	31.42%
Evaluation	(1,0)	0.030	0.004	86.66%
	(0,1)	0.030	0.004	86.66%
ON STATES		Static current		
Evaluation	(1,1)	130.19	42.43	67.40%
	(0,0)	130.19	42.43	67.40%

65nm				
OFF STATES		**Leakage current**		
Precharge	**(0,0)**	15.20	11.96	21.31%
	(0,1)	7.64	5.36	29.84%
	(1,1)	15.20	11.96	21.31%
	(1,0)	7.64	5.36	29.84%
Evaluation	**(1,0)**	0.006	0.007	-
	(0,1)	0.006	0.007	-
ON STATES		**Static current**		
Evaluation	**(1,1)**	322.24	65.77	79.58%
	(0,0)	322.24	65.77	79.58%
45nm				
OFF STATES		**Leakage current**		
Precharge	**(0,0)**	21.01	16.83	19.89%
	(0,1)	7.33	5.19	29.19%
	(1,1)	21.01	16.83	19.89%
	(1,0)	7.33	5.19	29.19%
Evaluation	**(1,0)**	0.007	0.007	-
	(0,1)	0.007	0.007	-
ON STATES		**Static current**		
Evaluation	**(1,1)**	1225	95.27	92.22%
	(0,0)	1225	95.27	92.22%

TABLE 4.9
LEAKAGE CURRENT MEASUREMENT FOR BASIC AND LECTOR INCORPORATED DYNAMIC DCVSL 2-INPUT XOR/XNOR GATE (ALL STACKING) AT VDD=1.2V

Technology/ Input states(A,B)		**Basic**	**Lector (With high V_T)**	**Percentage saving (With high V_T)**
90nm				
OFF STATES		**Leakage current**		
Precharge	**(0,0)**	1.96	1.65	15.81%
	(0,1)	0.31	0.20	35.48%
	(1,1)	1.96	1.65	15.81%
	(1,0)	0.31	0.20	35.48%
Evaluation	**(1,0)**	0.082	0.069	15.85%
	(0,1)	0.082	0.069	15.85%
ON STATES		**Static current**		
Evaluation	**(1,1)**	13.05	5.05	61.30%
	(0,0)	13.05	5.05	61.30%
65nm				
OFF STATES		**Leakage current**		
Precharge	**(0,0)**	2.38	1.94	18.48%
	(0,1)	0.62	0.43	30.64%

	(1,1)	2.38	1.94	18.48%
	(1,0)	0.62	0.43	30.64%
Evaluation	**(1,0)**	0.006	0.003	50.00%
	(0,1)	0.006	0.003	50.00%
ON STATES		**Static current**		
Evaluation	**(1,1)**	19.24	6.51	66.16%
	(0,0)	19.24	6.51	66.16%
45nm				
OFF STATES		**Leakage current**		
Precharge	**(0,0)**	2.76	2.21	19.92%
	(0,1)	0.63	0.43	31.74%
	(1,1)	2.76	2.21	19.92%
	(1,0)	0.63	0.43	31.74%
Evaluation	**(1,0)**	0.005	0.002	60.00%
	(0,1)	0.005	0.002	60.00%
ON STATES		**Static current**		
Evaluation	**(1,1)**	34.72	7.45	78.54%
	(0,0)	34.72	7.45	78.54%

It can be observed from Table 4.8 and Table 4.9 that percentage saving obtained in leakage and static current for VDD=1.8V is 20%-67% for 90nm, 21%-79% for 65nm and 20%-92% for 45nm. For VDD=1.2V, percentage saving achieved is 16%-61% for 90nm, 18%-66% for 65nm and 20%-78% for 45nm.

5. Proposed Hybrid Dynamic DCVSL Three input XOR/XNOR gate (TG + stacking)

Proposed hybrid dynamic DCVSL 3-input XOR/XNOR gate and its LECTOR incorporated configuration shown in fig.4.8 and fig.4.9 respectively are simulated with inputs conditions given as – load capacitances = 10ff, inputs A, B and C with period=4us, rise time (fall time) = 0.1us, width=2us, delay of 0.6us for A, 0.3us for B and 0.8us for C, Clock period=4us, clock width=1us, clock rise time (fall time)=0.1us and initial clock delay of 1us.

LECTOR incorporated configuration achieves notable reduction in leakage and static currents as mentioned in Table 4.10 for VDD=1.8V and Table 4.11 for VDD=1.2V. Percentage saving achieved is also mentioned in the tables.

TABLE 4.10

LEAKAGE CURRENT MEASUREMENT FOR PROPOSED AND LECTOR INCORPORATED HYBRID DYNAMIC DCVSL 3-INPUT XOR/XNOR GATE (TG+STACKING) AT VDD=1.8V

Technology/ Input states(A,B)		Proposed	Lector (With high V_T)	Percentage saving (With high V_T)
90nm				
OFF STATES		**Leakage current**		
Precharge	**(0,0,0)**	9.84	7.85	20.22%
	(0,1,0)	4.36	2.96	32.11%
	(1,1,0)	9.84	7.85	20.22%
	(1,1,1)	4.36	2.96	32.11%
Precharge	**(1,0,1)**	9.84	7.85	20.22%
	(0,0,1)	4.36	2.96	32.11%
	(1,0,0)	4.36	2.96	32.11%
	(0,1,1)	9.84	7.85	20.22%
Evaluation	**(1,1,1)**	0.0008	0.0008	-
	(0,1,0)	0.0009	0.0008	-
ON STATES		**Static current**		
Evaluation	**(1,0,1)**	130.19	42.43	67.40%
	(0,0,0)	130.28	42.48	67.40%
65nm				
OFF STATES		**Leakage current**		
Precharge	**(0,0,0)**	15.18	11.95	21.27%
	(0,1,0)	7.64	5.36	29.84%
	(1,1,0)	15.18	11.95	21.27%
	(1,1,1)	7.64	5.36	29.84%
	(1,0,1)	15.18	11.95	21.27%
	(0,0,1)	7.64	5.36	29.84%
	(1,0,0)	7.64	5.36	29.84%
	(0,1,1)	15.18	11.95	21.27%
Evaluation	**(1,1,1)**	0.006	0.006	-
	(0,1,0)	0.006	0.006	-
ON STATES		**Static current**		
Evaluation	**(1,0,1)**	322.25	65.78	79.58%
	(0,0,0)	322.25	65.78	79.58%
45nm				
OFF STATES		**Leakage current**		
Precharge	**(0,0,0)**	20.88	16.80	19.54%
	(0,1,0)	7.31	5.17	29.27%
	(1,1,0)	20.88	16.80	19.54%
	(1,1,1)	7.31	5.17	29.27%
	(1,0,1)	20.88	16.80	19.54%
	(0,0,1)	7.31	5.17	29.27%

	(1,0,0)	7.31	5.17	29.27%
	(0,1,1)	20.88	16.80	19.54%
Evaluation	(1,1,1)	0.007	0.007	-
	(0,1,0)	0.007	0.007	-
ON STATES		Static current		
Evaluation	(1,0,1)	1220	95.22	92.19%
	(0,0,0)	1220	95.22	92.19%

TABLE 4.11
LEAKAGE CURRENT MEASUREMENT FOR PROPOSED AND LECTOR INCORPORATED HYBRID DYNAMIC DCVSL 3-INPUT XOR/XNOR GATE (TG+STACKING) AT VDD=1.2V

Technology/ Input states(A,B)		Proposed	Lector (With high V_T)	Percentage saving (With high V_T)
90nm				
OFF STATES		Leakage current		
Precharge	(0,0,0)	1.95	1.65	15.38%
	(0,1,0)	0.355	0.250	29.57%
	(1,1,0)	1.95	1.65	15.38%
	(1,1,1)	0.355	0.250	29.57%
	(1,0,1)	1.95	1.65	15.38%
	(0,0,1)	0.355	0.250	29.57%
	(1,0,0)	0.355	0.250	29.57%
	(0,1,1)	1.95	1.65	15.38%
Evaluation	(1,1,1)	0.168	0.110	34.52%
	(0,1,0)	0.168	0.110	34.52%
ON STATES		Static current		
Evaluation	(1,0,1)	13.05	5.07	61.14%
	(0,0,0)	13.05	5.07	61.14%
65nm				
OFF STATES		Leakage current		
Precharge	(0,0,0)	2.38	1.94	18.48%
	(0,1,0)	0.622	0.424	31.83%
	(1,1,0)	2.38	1.94	18.48%
	(1,1,1)	0.622	0.424	31.83%
	(1,0,1)	2.38	1.94	18.48%
	(0,0,1)	0.622	0.424	31.83%
	(1,0,0)	0.622	0.424	31.83%
	(0,1,1)	2.38	1.94	18.48%
Evaluation	(1,1,1)	0.013	0.004	69.23%
	(0,1,0)	0.013	0.004	69.23%
ON STATES		Static current		
Evaluation	(1,0,1)	19.20	6.51	66.09%
	(0,0,0)	19.20	6.51	66.09%

45nm				
OFF STATES		**Leakage current**		
Precharge	**(0,0,0)**	2.76	2.21	19.92%
	(0,1,0)	0.632	0.434	31.32%
	(1,1,0)	2.76	2.21	19.92%
	(1,1,1)	0.632	0.434	31.32%
	(1,0,1)	2.76	2.21	19.92%
	(0,0,1)	0.632	0.434	31.32%
	(1,0,0)	0.632	0.434	31.32%
	(0,1,1)	2.76	2.21	19.92%
Evaluation	**(1,1,1)**	0.006	0.002	66.67%
	(0,1,0)	0.006	0.002	66.67%
ON STATES		**Static current**		
Evaluation	**(1,0,1)**	34.72	7.54	78.28%
	(0,0,0)	34.72	7.54	78.28%

It can be observed from Table 4.10 and Table 4.11 that percentage saving obtained in leakage and static current for VDD=1.8V is 20%-67% for 90nm, 21%-79% for 65nm and 19%-92% for 45nm. For VDD=1.2V, percentage saving achieved is 15%-61% for 90nm, 18%-66% for 65nm and 20%-78% for 45nm.

5. DSCL Two Input XOR/XNOR gate

Basic DSCL (differential static CMOS logic) for 2-input XOR/XNOR gate and LECTOR incorporated version of DSCL 2-input XOR/XNOR gate presented in fig.4.14 and fig.4.15 respectively are simulated with inputs conditions given as – load capacitances = 10ff, input A with period=400ns and B with period=200ns, rise time (fall time) = 2ns, width of A=200ns and width of B=100ns, delay of 50ns for A. Table 4.12 and Table 4.13 tabulate the leakage and static current values for different technologies, input states and configurations at VDD=1.8V and VDD=1.2V respectively.

TABLE 4.12
LEAKAGE CURRENT MEASUREMENT FOR BASIC AND LECTOR INCORPORATED DSCL 2-INPUT XOR/XNOR GATE AT VDD=1.8V

Technology/ Input states(A,B)	Basic	Lector (With high V_T)	Percentage saving (With high V_T)
90nm			
OFF STATES	**Leakage current**		
(1,0)	90.94	30.86	66.06%
(0,1)	90.94	30.86	66.06%
ON STATES	**Static current**		
(1,1)	178.22	73.11	58.97%
(0,0)	178.22	73.11	58.97%

65nm			
OFF STATES	Leakage current		
(1,0)	174.42	43.00	75.34%
(0,1)	174.42	43.00	75.34%
ON STATES	Static current		
(1,1)	430.45	134.47	68.76%
(0,0)	430.45	134.47	68.76%
45nm			
OFF STATES	Leakage current		
(1,0)	372.93	74.06	80.14%
(0,1)	372.93	74.06	80.14%
ON STATES	Static current		
(1,1)	1650	394.22	76.10%
(0,0)	1650	394.22	76.10%

TABLE 4.13

LEAKAGE CURRENT MEASUREMENT FOR BASIC AND LECTOR INCORPORATED DSCL 2-INPUT XOR/XNOR GATE AT VDD=1.2V

Technology/ Input states(A,B)	Basic	Lector (With high V_T)	Percentage saving (With high V_T)
90nm			
OFF STATES	Leakage current		
(1,0)	15.54	8.61	44.59%
(0,1)	15.54	8.61	44.59%
ON STATES	Static current		
(1,1)	25.91	13.51	47.85%
(0,0)	25.91	13.51	47.85%
65nm			
OFF STATES	Leakage current		
(1,0)	19.92	9.43	52.66%
(0,1)	19.92	9.43	52.66%
ON STATES	Static current		
(1,1)	33.65	14.85	55.86%
(0,0)	33.65	14.85	55.86%
45nm			
OFF STATES	Leakage current		
(1,0)	31.22	11.32	63.74%
(0,1)	31.22	11.32	63.74%
ON STATES	Static current		
(1,1)	55.74	18.14	67.45%
(0,0)	55.74	18.14	67.45%

It can be observed from Table 4.12 and Table 4.13 that percentage saving obtained in leakage and static current for VDD=1.8V is 59%-66% for 90nm, 69%-75% for 65nm and 76%-80% for 45nm. For VDD=1.2V, percentage saving achieved is 45%-48% for 90nm, 53%-56% for 65nm and 64%-67% for 45nm.

6. NP Mixed 2-input XOR/XNOR gate (all stacking)

Figure 4.10 gives the basic structure of NP mixed 2-input XOR/XNOR gate fully stacked. NP mixed structure is obtained from conventional DCVSL circuit by just replacement of those NMOS transistors in PDN which are driven by complementary inputs with PMOS transistors driven by true inputs signals. Leakage current and static current values for different input states and supply voltages at 45nm technology are given by Table 4.14.

TABLE 4.14
LEAKAGE CURRENT MEASUREMENT FOR NP-MIXED 2-INPUT XOR/XNOR GATE

Technology/ Input states(A,B)	Leakage current (nA)
45nm	**Power supply=1.8 V**
OFF STATES	**Leakage current**
(1,0)	170.81nA
(0,1)	4.50nA
ON STATES	**Static current**
(1,1)	722.60nA
(0,0)	34.27nA
45nm	**Power supply=1.2 V**
OFF STATES	**Leakage current**
(1,0)	2.87nA
(0,1)	2.96nA
ON STATES	**Static current**
(1,1)	16.66nA
(0,0)	3.43nA

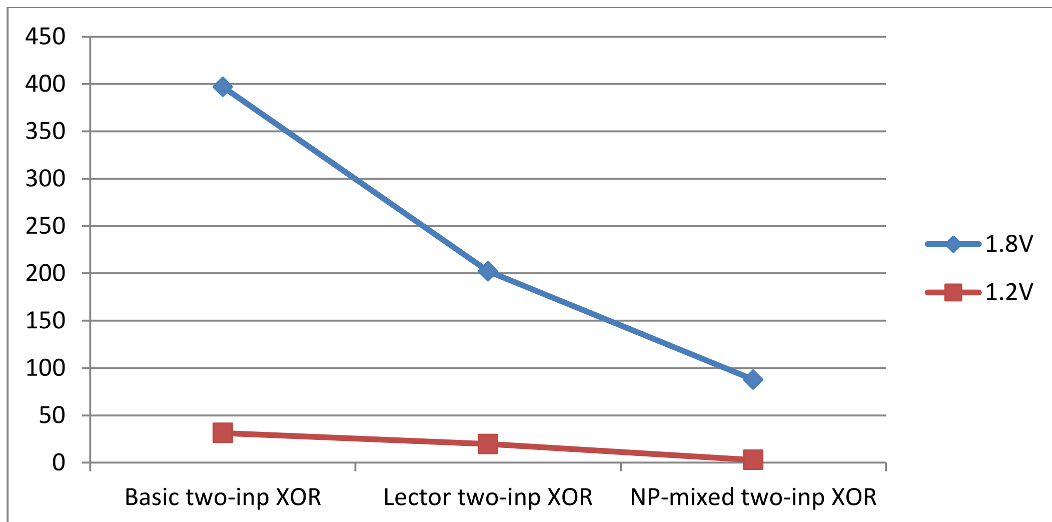


Fig. 4.23 Leakage current comparison between basic, LECTOR incorporated and NP mixed DCVSL 2-input XOR gate

Figure 4.23 shows the comparison between the leakage for basic DCVSL, LECTOR incorporated DCVSL and NP mixed DCVSL. Graph shows that NP mixed style achieves the lowest leakage current even below LECTOR incorporated configuration. But it is accompanied with the speed and threshold voltage drop limitations.

TEMPERATURE VARIATION

(At 45nm technology and power supply=1.2)

The pattern followed by leakage current with variation in temperature has been studied via performing temperature variation on the circuits simulated above for temperature values -25°C, 27°C and 100°C.

- **Basic EDCVSL inverter**

OFF STATES		Leakage current at temperature(nA)		
		-25°C	27°C	100°C
Precharge	**0**	0. 100	0.119	0.340
	1	0.713	2.34	7.78
Evaluation	**0**	0.036	0.150	0.810

- **LECTOR EDCVSL inverter**

OFF STATES		Leakage current at temperature (nA)		
		-25°C	27°C	100°C
Precharge	**0**	0.067	0.086	0.313
	1	0.585	1.94	6.54
Evaluation	**0**	0.032	0.119	0.668

- **Basic EDCVSL 2 input XOR gate (all stacking)**

OFF STATES		Leakage current at temperature(nA)		
		-25°C	27°C	100°C
Precharge	**(0,0)**	1.01	2.66	8.14
	(0,1)	0.45	0.51	0.62
	(1,1)	1.01	2.66	8.14
	(1,0)	0.45	0.51	0.62
Evaluation	**(1,0)**	0.001	0.003	2.43
	(0,1)	0.001	0.003	2.43

- **LECTOR EDCVSL 2 input XOR gate (all stacking)**

OFF STATES		Leakage current at temperature (nA)		
		-25°C	27°C	100°C
Precharge	**(0,0)**	0.783	2.14	6.76
	(0,1)	0.271	0.314	0.393
	(1,1)	0.783	2.14	6.76
	(1,0)	0.271	0.314	0.393
Evaluation	**(1,0)**	0	0.004	1.50
	(0,1)	0	0.004	1.50

- **Basic Hybrid EDCVSL 2 input XOR gate (all TG)**

OFF STATES		Leakage current at temperature(nA)		
		-25°C	27°C	100°C
Precharge	**(0,0)**	0.712	2.34	7.74
	(0,1)	0.100	0.117	0.285
	(1,1)	0.712	2.34	7.74
	(1,0)	0.100	0.117	0.285
Evaluation	**(1,0)**	0.030	0.150	0.826
	(0,1)	0.030	0.150	0.826

- **LECTOR Hybrid EDCVSL 2 input XOR gate (all TG)**

OFF STATES		Leakage current at temperature (nA)		
		-25°C	27°C	100°C
Precharge	**(0,0)**	0.584	1.95	6.55
	(0,1)	0.068	0.079	0.151
	(1,1)	0.584	1.95	6.55
	(1,0)	0.068	0.079	0.151
Evaluation	**(1,0)**	0.020	0.122	0.673
	(0,1)	0.020	0.122	0.673

- **Basic Hybrid EDCVSL 3 input XOR gate (one level TG+ stacking)**

OFF STATES		Leakage current at temperature		
		-25°C	27°C	100°C
Precharge	**(0,0,0)**	1.13	2.76	8.22
	(0,1,0)	0.535	0.631	0.798
	(1,1,0)	1.13	2.76	8.22
	(1,1,1)	0.535	0.631	0.798
	(1,0,1)	1.13	2.76	8.22
	(0,0,1)	0.535	0.631	0.798
	(1,0,0)	0.535	0.631	0.798
	(0,1,1)	1.13	2.76	8.22
Evaluation	**(1,1,1)**	0.0004	0.006	1.56
	(0,1,0)	0.0004	0.006	1.56

- **LECTOR Hybrid EDCVSL 3 input XOR gate (one level TG+ stacking)**

OFF STATES		Leakage current at temperature		
		-25°C	27°C	100°C
Precharge	**(0,0,0)**	0.862	2.21	6.80
	(0,1,0)	0.394	0.449	0.558
	(1,1,0)	0.862	2.21	6.80
	(1,1,1)	0.394	0.449	0.558
	(1,0,1)	0.862	2.21	6.80
	(0,0,1)	0.394	0.449	0.558
	(1,0,0)	0.394	0.449	0.558
	(0,1,1)	0.862	2.21	6.80
Evaluation	**(1,1,1)**	0.0003	0.001	1.06
	(0,1,0)	0.0003	0.001	1.06

From above tables we can conclude that the pattern followed verifies that leakage current is directly proportional to temperature. Leakage current increases with temperature.

DELAY CALCULATIONS

- **Two input hybrid EDCVSL XOR gate (all TG)**
  Input conditions: VDD=1.8V, Technology =45nm, Period=200ns, Width=100ns, t_r=2ns, t_f=2ns, Td=50ns

TABLE 4.15
DELAY MEASUREMENT FOR 2-INPUT BASIC HYBRID EDCVSL XOR GATE (ALL TG)

Mode of Operation	A	B	Output	Delay
Evaluation	**1**	**1**	1->0	300ps
	0	**0**	1->0	299ps
precharge	**1**	**1**	0->1	184ps
	0	**0**	0->1	187ps

Here t_{plh} (0->1) delay is lesser than t_{phl} (1->0) delay because there are two parallel paths available for charging the output node during pre-charge phase.

TABLE 4.16
DELAY MEASUREMENT FOR 2-INPUT LECTOR INCORPORATED HYBRID EDCVSL XOR GATE (ALL TG)

Mode of Operation	A	B	Output	Delay
Evaluation	**1**	**1**	1->0	345ps
	0	**0**	1->0	344ps
precharge	**1**	**1**	0->1	598ps
	0	**0**	0->1	598ps

Here t_{plh} (0->1) delay is increased due to near cut-off high Vth PMOS LCT present between the pre-charging transistors and the output node.

- **Three input hybrid dynamic DCVSL XOR gate (TG + stacking)**

Input conditions: VDD=1.8V, Technology =45nm, Period=200ns, Width=100ns, t_r=1ns, t_f=1ns

TABLE 4.17
DELAY MEASUREMENT FOR 3-INPUT BASIC HYBRID DYNAMIC DCVSL XOR GATE (TG + stacking)

Mode of Operation	A	B	C	Output	Delay
Evaluation	**0**	**0**	**0**	1->0	243ps
	1	**1**	**0**	1->0	243ps
	1	**0**	**1**	1->0	243ps
	0	**1**	**1**	1->0	243ps
precharge	**0**	**0**	**0**	0->1	167ps
	1	**1**	**0**	0->1	167ps
	1	**0**	**1**	0->1	167ps
	0	**1**	**1**	0->1	167ps

Here t_{plh} (0->1) delay is lesser than t_{phl} (1->0) delay because there are two parallel paths available for charging the output node during pre-charge phase.

TABLE 4.18
DELAY MEASUREMENT FOR 3-INPUT LECTOR INCORPORATED HYBRID DYNAMIC DCVSL XOR GATE (TG + stacking)

Mode of Operation	A	B	C	Output	Delay
Evaluation	**0**	**0**	**0**	1->0	362ps
	1	**1**	**0**	1->0	362ps
	1	**0**	**1**	1->0	362ps
	0	**1**	**1**	1->0	362ps
precharge	**0**	**0**	**0**	0->1	394ps
	1	**1**	**0**	0->1	394ps
	1	**0**	**1**	0->1	394ps
	0	**1**	**1**	0->1	394ps

Here t_{plh} (0->1) delay is increased due to near cut-off high Vth PMOS LCT present between the pre-charging transistors and the output node.

- **DSCL (Differential static CMOS logic)**

Two input XOR DSCL gate (all stacking)

Input conditions: VDD=1.8V, Technology =45nm, Period=200ns, Width=100ns, t_r=2ns, t_f=2ns, Td=50ns

TABLE 4.19

DELAY MEASUREMENT FOR 2-INPUT BASIC DSCL XOR GATE (all stacking)

A	**B**	**Output**	**Delay**
0->1	**0**	0->1	207ps
1->0	**0**	1->0	179ps
0->1	**1**	1->0	166ps
1->0	**1**	0->1	208ps
0	**0->1**	0->1	141ps
0	**1->0**	1->0	163ps
1	**0->1**	1->0	158ps
1	**1->0**	0->1	138ps

TABLE 4.20

DELAY MEASUREMENT FOR 2-INPUT LECTOR INCORPORATED DSCL XOR GATE (all stacking)

A	**B**	**Output**	**Delay**
0->1	**0**	0->1	516ps
1->0	**0**	1->0	312ps
0->1	**1**	1->0	302ps
1->0	**1**	0->1	516ps
0	**0->1**	0->1	397ps
0	**1->0**	1->0	346ps
1	**0->1**	1->0	345ps
1	**1->0**	0->1	398ps

DSCL configuration reduces 0 -> 1 delay as was discussed in section 4.5.2 and makes low to high and high to low delays comparable due to its special configuration.

Chapter 5

Conclusion and Future Work

5.1 CONCLUSION

This thesis majorly focusses on two aspects. Firstly, in depth analysis of increasing leakage power dissipation in VLSI circuits with scaling down of technology and various methodologies existing for CMOS logic for reducing leakage currents in the device. Secondly, discussing benefits of DCVS logic family and proposing new DCVS configurations for reducing leakage power in basic structures.

Simulations have been performed for 90nm, 65nm and 45nm technologies where leakage current increases with lowering down of the technology. LECTOR technique has been adapted for DCVS logic structure for leakage power reduction and thereby proposing LECTOR incorporated DCVSL circuits firstly for static 2 input and 3 input XOR/XNOR gates. These newly introduced LECTOR incorporated DCVSL XOR/XNOR gates achieve around 60%-95% saving in leakage current for power supply of 1.8V and around 40%-80% for supply voltage of 1.2V where percentage saving increases with lowering down of technology from 90nm to 45nm. Leakage current decreases with scaling down of supply voltage for a given threshold voltage. Moreover, hybrid configurations for these circuits have also been proposed which experience significantly less leakage currents than basic structures. LECTOR incorporated versions of Hybrid structures for 2-input DCVSL XOR/XNOR gate achieve 81%-95% saving in leakage current for supply voltage of 1.8V and 59%-83% for supply voltage of 1.2V. For LECTOR incorporated 3-input hybrid DCVSL XOR/XNOR gate (TYPE1 and TYPE2) saving achieved is 66%-95% for supply of 1.8V and 44%-83% for supply voltage of 1.2V where saving increases with scaling down of technology from 90nm to 45nm. Leakage current for 3-input DCVSL XOR/XNOR reduces in the order of first basic structure then TYPE1 hybrid structure followed by Type2 hybrid structure.

Similarly, reduced leakage power versions of dynamic DCVSL and EDCVSL circuits have also been proposed. Leakage currents are inherently less in dynamic DCVSL circuits which are further reduced by incorporation of LECTOR circuitry and hybrid structures. LECTOR incorporated 2-input EDCVSL XOR/XNOR gate achieves approx. 19%-33% saving in leakage current VDD=1.8V and 1.2V. Hybrid structure of 2-input EDCVSL XOR gate suffers lesser leakage than basic structure which is further reduced by LECTOR incorporation so that a saving of around 10%-36% is achieved for VDD=1.8V and 1.2V. Hybrid structure of 3-input dynamic DCVSL XOR/XNOR gate upon LECTOR incorporation shows a percentage saving of 15%-32% for VDD=1.8V and 1.2V. Further LECTOR incorporated DSCL configuration has been proposed where DSCL proves to be an improvement of

DCVSL in terms of achieving equality in rise and fall times of the circuit which also achieves 66%-76% saving in leakage current. A yet another variation of DCVSL proposed is NP mixed DCVSL which tremendously reduces the leakage current as compared to basic structure but at the cost of increased delay. Temperature variations have also been performed for all the above proposed circuits which indicate that leakage current is directly proportional to the temperature. And it is worth mentioning that advantage of leakage current saving achieved by LECTOR configurations and hybrid structures is at the cost of slight delay overhead.

5.2 FUTURE WORK

This work was an attempt to explore the necessity to control leakage power dissipation with growing technology and the advantages of differential logic family DCVSL over conventional CMOS logic. Various configurations for the fundamental DCVSL circuits have been devised here which have efficiently controlled the leakage currents through basic structures. Thus a pathway has been paved for future researchers to exploit the inherent benefits of DCVSL along with the leakage current regulation mechanism and build bigger structures utilising these proposed low power basic structures which are least affected by the advancement of technology in terms of leakage power loss.

REFERENCES

[1] P. Kalyani, Dr. P. Satishkumar and Dr. K. Ragini, “Various Low Power Techniques for CMOS Circuits”, Int. Journal of Engineering Research and Applications www.ijera.com ISSN : 2248-9622, Vol. 3, Issue 6, Nov-Dec 2013, pp.330-333

[2] P. Lakshmikanthan and A. Nunez, “A Novel Methodology to Reduce Leakage Power in Differential Cascode Voltage Switch Logic Circuits”, 3rd International Conference on Electrical and Electronics Engineering, 2006

[3] N.H.E. Weste and D.M. Harris “CMOS VLSI Design: A Circuits and Systems Perspective”, Pearson Education, Copyright c 2011, 2005, 1993, 1985

[4] S.L. Narayan, R. Korah and N.K. Kumar, “A novel sleepy stack 6-T SRAM cell design for reduced leakage power in submicron technologies”, International Conference on Communication and Signal Processing, April 3-5, 2013

[5] M. Kumar, Md. A. Hussain and S. K. Paul, “New Hybrid Digital Circuit Design Techniques for Reducing Subthreshold Leakage Power in Standby Mode”, Scientific Research, Circuits and Systems, 2013, 4, 75-82

[6] N. Hanchate and N. Ranganathan, “LECTOR: A Technique for Leakage Reduction in CMOS Circuits”, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol.12, No. 2, February 2004

[7] Y. Taur and T. H. Ning, “Fundamentals of Modern VLSI Devices”, New York: Cambridge Univ. Press, 1998, ch. 2, pp. 94–95.

[8] F. Fallah , M. Pedram ,“Standby and Active Leakage Current Control and Minimization in CMOS VLSI Circuits”, IEICE transactions on electronics, 2005

[9] S. Narendran', S. Borkar', V. De', D. Antoniadisn, and A. Chandrakasann,“Scaling of Stack Effect and its Application for Leakage Reduction”, International Symposium on Low Power Electronics and Design (ISLPED) '01, August 6-7,2001.

[10] A. K. Pandey, R. A. Mishra, and R. K. Nagaria,“Leakage Power Analysis of Domino XOR Gate”, Hindawi Publishing Corporation ISRN Electronics Volume 2013

[11] H. malviya, S. Nayar and C.M Roy ,"A NEW APPROACH FOR Leakage Power Reduction Techniques in Deep Submicron Technologies in CMOS CIRCUIT for VLSI Applications", International Journal of Advanced Research in Computer Science and Software Engineering, Volume 3, Issue 5, May 2013

[12] J. C. Park and V. J. Mooney III, "Sleepy Stack Leakage Reduction" IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 14, No. 11, November 2006

[13] I. S. Rao, D.Srinivas, B.R. Paramesh, V.M. Rao, "Leakage Current Reduction "GALEOR & LECTOR" Techniques", International Journal of Communication Engineering Applications, Vol 02, Issue 02; May 2011

[14] J. M. Rabaey, "Digital Integrated Circuits: A Design Perspective", New York: Prentice Hall, l996.

[15] V. Motallebzadeh, Md. R. Alamdar, S. I. Tous and A. Golmakani, "Design of a novel hybrid-CMOS full adder with low power consumption, high speed and full swing outputs", Majlesi Journal of Telecommunication Devices, Vol. 2, No. 2, June 2012

[16] W. Chen, W. Hwang, P. Kudva, G.D. Gristede, S. Kosonocky and R.V.Joshi "Mixed MuIti ThreshoId DifferentiaI Cascode VoItage Switch (NIT- DCVS) Circuit Styles and Strategies for Low Power VLSI Design" , International Symposium on Low Power Electronics and Design, 2001

[17] D. W. Knng, Y.B. Kim, "Design of Enhanced Differential Cascode Voltage Switch Logic (Edcvsl) Circuits for high fan-in Gate", 15th Annual IEEE International Conference on ASIC/SOC, 2002

[18] Z. Liu and V. Kursun, "PMOS-only sleep switch dual-threshold voltage domino logic in sub-65-nm CMOS technologies," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol.15, no. 12, pp. 1311–1319, 2007.

[19] Md. E.S. Elrabaa, "A New Static Differential CMOS Logic with Superior Low Power Performance", Proceedings of the 10th IEEE International Conference on Electronics, Circuits and Systems, (Volume:2) , 2003.

[20] C. Tretz, et.al., "Performance comparison of differential static CMOS circuit topologies in SOI technology," in Proc. IEEE International SOI Conference, 1998, pp. 123–124.

[21] A. Srinivasulu, M. Rajesh “ULPD and CPTL Pull-Up Stages for Differential Cascode Voltage Switch Logic”, Hindawi Publishing Corporation Journal of Engineering Volume, 2013