REALIZATION OF ANALOG CIRCUITS USING ANALOG BUILDING BLOCK: CDBA

Dissertation submitted in
Partial fulfilment of the requirement
For the award of the degree of

Master of Technology

in

VLSI and Embedded System Design

by

Kashif Khan

University Roll No. 2K14/VLS/13

Under the guidance of

Mr. A.K. Singh
Assistant Professor,
Electronics and Communication Engineering Department, DTU

2014-2016

ELECTRONICS AND COMMUNICATION ENGINEERING DEPARTMENT

DELHI TECHNOLOGICAL UNIVERSITY

DELHI-110042, INDIA

Department of Electronics and Communication Engineering

Delhi Technological University

Delhi-110042

www.dce.edu

CERTIFICATE

This is to certify that the dissertation titled **"Realization of Analog Circuits using Analog Building Block: CDBA "** is a bonafide record of work done by **Kashif Khan , Roll No. 2K14/VLS/13** at **Delhi Technological University, Delhi** for partial fulfilment of the requirements for the degree of Master of Technology in VLSI and Embedded System Design. This project was carried out under my supervision and has not been submitted anywhere else, either in part or full, for the award of any other degree or diploma to the best of my knowledge and belief.

Date: _____

(Mr. A.K. Singh)
Assistant Professor
Department of Electronics and Communication Engineering
Delhi Technological University

ACKNOWLEDGEMENT

This work would have not been possible without the support of many. First, it is my duty to thank God Almighty for making the completion of this research possible. Next, I would like to express my gratitude to my parents and my family for their continued support.

I would like to express my deep sense of respect and gratitude to my project supervisor **Mr. A.K. Singh ,** Assistant Professor, Electronics and Communication Engineering Department, DTU for providing the opportunity of carrying out this project and being the guiding force behind this work. I am deeply indebted to her for the support, advice and encouragement she provided without which the project could not have been a success.

I am also grateful to **Prof. Prem R. Chadha**, HOD, Electronics and Communication Engineering Department, DTU for his immense support.

I would also like to acknowledge Delhi Technological University for providing the right academic resources and environment for this work to be carried out.

Last but not the least I would like to express sincere gratitude to my friends and my colleagues for constantly encouraging me during the completion of work.

Kashif Khan

University Roll no: 2K14/VLS/13

M.TECH. (VLSI Design and Embedded System)

Department of Electronics & Communication Engineering

Delhi Technological University

Delhi – 110042

ABSTACT

In the recent decades, with the demand of low power supply and low area requirement due to miniaturization, a large number of Analog Building Block (ABB) has been introduce for analog signal processing. These Analog Blocks offer significant advantage over conventional op-amp. With development in this area using current mode concept having notable features like high gain, high bandwidth, simple circuit structure, high slew rate and reduce power supply voltage, these Blocks are very reliable and there performance is much better then conventional op-amp. Current mode design technique offer voltage independent, high bandwidth in analog circuits with properties of accuracy and versatility in a wide range of application. One of such analog block is Current difference buffered amplifier CDBA, on which recently a lot of research work is done. Here I have presented a study on various implementation of CDBA topology. I have also analysis Flipped Voltage Follower circuits and compare various parameter with normal source follower. Using the concept of Flipped voltage follower I have also study and implemented a CDBA[19] which is based on this concept. Using FVF based CDBA, implementation of filter and rectifier is performed and various properties of these analog circuits are studied.

TABLE OF CONTENT

LIST OF FIGURES

LIST OF TABLES

ABBREVIATIONS

OA	Operational Amplifier
CC	Current Conveyors
OTA	Operational Transconductance Amplifier
CDBA	Current Difference Buffered Amplifier
VMC	Voltage Mode Circuits
CM	Current Mode
IC	Integrated Circuits
RF	Radio Frequency
CFA	Current Feedback Amplifier
FVF	Flipped Voltage Follower
FVFCS	Flipped Voltage Follower Current Source
ABB	Analog Building Block
CDU	Current Difference Unit
BU	Buffered Unit
LPF	Low Pass Filter
HPF	High Pass Filter
BPF	Band Pass Filter
APF	All Pass Filter
AC	Alternating Current
DC	Direct Current

CHAPTER 1

INTRODUCTION

1.1 MOTIVATION

This is one of the most popular misconceptions today; that the world has gone digital and analog is being passes away. But in actual it is not truth. The main motivation behind digital computation is speed and precision with in a smaller circuit area. However, these are achieved at the cost of higher power consumption and higher circuit complexity. Portable devices which are used today such as mobile phones, tablet computers, and medical prosthetic devices have a limited power budget. It is clearly having an all-digital design in such applications would be disadvantageous. Secondly, these devices interact with the real world which is analog thus their interface must be analog in nature. In general, all data-acquisition systems require an analog interface, both at the input and the output. To exploit the advantages of both, digital and analog processing, the best possible solution is to stay within the analog domain as long as possible to minimize power consumption and only perform the most important computations digitally in order to ensure higher speed and greater precision. This design methodology ensures that analog ICs still play a significant role in the design of electronic systems.

Going deeper into this scenario, it becomes apparent that in certain applications, it became very difficult or even impossible to replace analog functions with their digital counterparts, regardless of advances in technologies. For instance, at low-to-moderate levels of precision (such as medical prosthetic devices), analog implementation of certain computations can be vastly more efficient in terms of power dissipation, circuit area, or both than its digital equivalent design. This efficiency of any circuit is achieved by performing most of the processing in analog domain. In such designs, usually, only a small subset of internal computations is performed using a digital signal processing system. Pre- and post-processing is performed in the analog domain. Such designs provide the right balance of power efficiency, and computational accuracy. Therefore, analog circuits will continue to be a significant part of larger VLSI digital systems.

In the last few decades, a huge number of active building blocks [9] were introduced for analogue signal processing. Currently a large number of analog processing circuits are developed using these analog blocks [1] which having advantage of current mode concept [4] having better tradeoff between speed and bandwidth. Here I have derived motivation of my work from the work done on one such active block which is based on flipped voltage follower technique (CDBA) having very low power dissipation.

1.2 Basic Analog Processing Module

There are a number of analog signal processing modules having a wide variety of applications. Out of these, some modules which are relevant to the work carried out within this thesis are discussed in the following paragraphs.

1.2.1 Filter

Filters [2] play a significant role in almost any electronic system, having widespread applications found in telecommunication, radar, consumer electronics, instrumentation systems etc. Radio and television are good examples of everyday use of filters. When a channel is changed on an analog television set or radio, an analog filter is used to pick out the carrier frequency on the input signal. Once it's isolated, the television or radio information being broadcast is used to form the picture and/or sound. Filters were designed and developed early in the twentieth century. During that time, their primary application was in telephony. Continuous progress in the design of filters was largely done in the 1930's and 1940's. As of today, there exist a number of approaches to implement filters. They can be termed as passive, active and switched capacitors.

Passive Filters

From early 20th century till the late 1960s [2], filters were constructed from resistors, capacitors and inductor. Since these components are passive in nature hence the designed filters were termed as passive filters. Such filters do not have any amplifying elements (Transistors, operational amplifiers (OA), current conveyors (CC) etc.). Passive filters have a number of advantages. Since they do not contain any active component, they do not require any power supply. They are not restricted by the bandwidth limitations of active devices; they can work well at very high frequencies. For example, Passive LC filters work well at high frequencies, however in low frequency applications. The required inductors are large, physically bulky and their characteristics are non-ideal. Furthermore, such inductors are impossible to fabricate in monolithic form and are incompatible with any of the techniques for assembling a modern electronic system. Therefore, there has been a considerable interest in finding filter realization that do not require inductors. Use of passive components allows such filters to be used in applications involving larger current or voltage levels than can be handled by active devices. Passive filters also generate lesser noise when compared to circuits using active gain elements.
The noise they produce is simply thermal noise from resistive components and, with careful design; the amplitude of this noise can be very low. However, passive filters exhibit significant drawbacks when employed in certain applications. Since they do not use any active elements, they cannot provide a signal gain. Input impedances can be lower than desirable, and output impedances can be higher than optimum, hence buffer amplifiers maybe needed.

Active Filters:

In the 1950's it was recognized that substantial size and cost reduction could be achieved by replacing large and expensive passive inductors with active circuitry [2]. However, high quality active components such as operational amplifiers became commercially available only in the mid 1960's. Filters based on active devices are accordingly termed as active filters. Such filters also use other amplifying elements such as operational transconductance amplifiers (OTA), current conveyors (CC) etc. with resistors and capacitors in their feedback loops, so as to synthesize the desired filter characteristics. Active filters can have high low input impedance, high/low output impedance, and virtually any arbitrary gain. They are also usually easier to design than passive filters. Their most significant advantage is that they do not contain inductors, thereby reducing the problems associated with such components. Nonetheless, problems of accuracy and value spacing also affect capacitors, although to a lesser degree. Performance at high frequencies is limited by the gain-bandwidth product of the amplifying elements. However, within the amplifier's operating frequency range, active filter can achieve very good accuracy, provided that

low tolerance resistors and capacitors are used [3]. However, it needs to be pointed out that active filters will generate noise due to inherent amplifying circuitry. But this can be minimized by the use of low-noise amplifiers and careful circuit design. Inductor-less filters can also be designed and are termed as active RC filters. Thin-film and thick-film techniques have been used to produce hybrid microcircuits using active RC techniques. These, however, need precise capacitors and laser trimming of resistors to achieve the desired specifications

1.2.2 Precision Rectifier

Precision rectifiers are also considered to be important modules in the area of non-linear analog signal processing. Simple diode-based rectifier circuits are capable of rectification above the threshold voltage of a diode. These rectifiers find applications in RF demodulators, piecewise linear function generators, DC voltage power supplies etc. However, there are some applications such as detection of an RF signal where small voltages of the order of 100mV are required. In such cases, it is not possible to employ a conventional rectifier as the voltage drop across the diode cannot be ignored. For such applications, a precision rectifier is more appropriate. The full-wave rectifiers based on operational amplifiers (OAs) and diodes, while generally faster than other rectifier circuits, suffer from a major disadvantage. The finite small-signal rate of change of voltage of the OAs results in the distortion of the rectified signal during the zero-crossing of the input signal in which the non-conduction/conduction transition of the diodes occurs. Nonetheless, the use of the high slew-rate OAs does not solve this drawback because of its small signal transient problem. This problem is overcome by using various analog active block like CDBA, which show a very high slew rate and bandwidth as compared to traditional OA based circuits.

1.2.3 Oscillators

Oscillators were discovered by Edwin Howard Armstrong in 1912 [3] using vacuum tubes. His discovery went to revolutionize radio, and today, these circuits find widespread acceptance in applications such as modern telecommunications equipment. Oscillations start off with their poles in the right-half plane (which is an unstable condition) but as the amplitude of oscillation grows, the loop-gain of the circuit drops due to non-linear effects and the systems pushes its poles towards the left-half plane until they reach the steady-state condition in which the poles lie on the imaginary axis. To obtain sustained oscillation, the Barkhausen criteria must be satisfied. Oscillators can be used to perform a very basic operation called frequency synthesis wherein a given range of frequencies can be generated using a single oscillator. This feature is utilized in cellular applications where multiple users placing calls require precise frequency control in order to ensure efficient utilization of available bandwidth. Oscillators can be utilized as analog interface circuits for resistive and capacitive sensors. In such an interface setup, for instance, the oscillators' output period is proportional to the resistive/capacitive value. Today, oscillators are used in almost all electronic circuitry be it digital or analog. These are widely employed as carrier generators for radio systems and as clock generators for digital circuitry. Timing information plays an essential role in information processing. To provide these systems with timing information, usually oscillators are used, which generate periodic signals. Each system imposes a different requirement on the oscillations produced by the oscillator, depending on the type and performance of that specific system. Thus it is clear that the number of oscillators per

system has significantly grown over time due to their immense utility in almost all electronic applications

1.3 VOLTAGE MODE VERSUS CURRENT MODE

All conventional analog circuits are voltage mode circuits (VMCs) where the circuit performance is determined in terms of voltage level at various nodes including the input and the output nodes. But these circuits suffer from the following disadvantages:

(i) Output voltage cannot change instantly when there is a sudden change in the input voltage due to stray and other circuit capacitances
(ii) Bandwidth of op-amp based circuits is usually low because of finite unity-gain bandwidth.
(iii) Slew rate is dependent on the time constants associated with the circuit.
(iv) Circuits do not have high voltage swings.
(v) Require higher supply voltages for better SNR.

Clearly, VMCs are not suitable for use in high frequency applications. This unsuitability is due to the fact that in voltage-mode circuits, the high-valued resistors with parasitic capacitances create a dominant pole at a relative low frequency, which limits the bandwidth. Current mode (CM) circuits offer a better alternative to VMC in high-frequency applications. Early circuit design principles and techniques for CM processing, such as the trans-linear circuit principal introduced by Barrie Gilbert in 1972, are becoming powerful tools for the development of high performance analog circuits and systems. A further consequence of the development of CM analog signal processing has been the emergence of new analog building blocks ranging from the current-conveyor and current-feedback op-amps to sampled-data current circuits, such as dynamic current-mirrors and analog neural networks. In the CM approach [4], the circuit description is presented in terms of current. This implies that both, the input and the output, are taken in current form rather than in voltage form. Hence CM signal processing techniques can be defined as the processing of current signals in an environment where voltage signals are irrelevant in determining circuit performance. The advancements in IC technologies together with the demand for smaller and low-power devices have ushered in the era of IC filters [5]. While the initial goal of microminiaturization was to produce filters for audio frequency applications, the focus has progressively changed toward higher-than-audio frequency filters. The advent of submicron IC technological processes (0.5μm and smaller) has facilitated realization of filters in the VHF frequency band (30-300MHz). Together with higher frequency of operation, reduction in power consumption by various electronic devices has also been of concern to present-day researchers. In view of this, attention is being paid toward signal processing in terms of currents rather than voltages. This new type of signal processing is known as current-mode (CM) [6] signal processing. CM signal processing lead to a higher frequency of operation, since the signal current is delivered into a small (ideally short circuit) load resistance. The parasitic pole frequency, due to such a small resistance (pole frequency being inversely proportional to the resistance), will be very high and hence, a high-frequency signal can be

processed without substantial impairment due to the presence of such a high-frequency parasitic pole. In summary, the following are the advantages of the CM approach [6]:

(i) Extended bandwidth.
(ii) Easy addition, subtraction and multiplication of signals.
(iii) Higher dynamic range.
(iv) Suitability of operation in reduced power supply environment.
(v) Simpler circuit structure.
(vi) Low-power consumption.
(vii) Low-voltage operation.
(viii) Micro-miniaturization.

1.4 THESIS ORGANIZATION

In order to assist the reader in understanding the workflow involved in the development of analog signal processing modules within this thesis, it becomes imperative to outline its layout. The following paragraphs explain the organization of this thesis from Chapter 2 onwards.

Chapter 2 discuss with the literature survey of CDBA which gave us a exposure of development of CDBA at various stage, in same chapter we also discuss about various filter application using CDBA and also Nonlinear application of CDBA like rectifier.

Chapter 3 deal with the Flipped voltage follower concept in which we discuss advantage of FVF cell, its type and simulation and comparison of this technique is done with voltage follower.

In Chapter 4, we realize a CDBA block which is based on FVF cell having very low input impedance, low power dissipation and used only 14 transistors. All simulation is done on PSPICE using 0.18um CMOS technology parameter and various parameter of CDBA are analyses.

In Chapter 5 We have implement some filter using CDBA and in Chapter 6 a nonlinear application of CDBA is done in which we implemented a rectifier. Conclusion is presented in chapter 7 which highlight the contribution made within this work.

CHAPTER 2

LITERATURE SURVEY

The demand for electronic circuit having extremely low supply voltage and low power consumption [8] is increasing day by day due to miniaturization. Voltage-mode and current mode circuits such as current conveyors and current feedback operational amplifiers are getting much attention as compared to other active elements due to wider bandwidth, simple circuitry, low power consumptions and dynamic ranges. In the last decade, a huge number of active building blocks were introduced for analogue signal processing. In the present days, a number of trends can be noticed in the area of analogue filter and oscillator design, namely reducing the supply voltage of integrated circuits and transition to the current-mode. On the other hand, current-, voltage- and mixed-mode analog circuits design still receives considerable attention of many researches. During the last two decades, research in the field of analog CMOS circuits has gained a lot of interest. Continuous improvements in CMOS technology [5] enabled the integration of complete electronic systems on a single chip. Usually, analog and mixed analog-digital circuits are now found at the interface of such systems with the 'analog real world. Furthermore, analog signal processing can be favorable in terms of speed, chip area and power dissipation, especially for low and moderate precision circuits. Linear circuits, like amplifiers and filters, are indispensable analog building blocks.

In order to increase the speed of circuits for analog signal processing and to decrease the supply voltages of integrated circuits, designers devote their attention to the so-called current mode. It means simply speaking that the individual circuit elements should interact by means of currents, not voltages. In practice, we can only approach the current mode because a current flowing through circuit element necessarily causes a voltage drop. Choosing proper impedance levels, sufficiently small voltages can be achieved with the aim to eliminate the influence of Miller's capacitances and other non-idealities. The circuits based on current-mode technique are suited for these applications. Presently, there is a growing interest in synthesizing the current-mode circuits because of more their potential advantages such as larger dynamic range, higher signal bandwidth, greater linearity, simpler circuitry and lower power consumption [8].

2.1 CURRENT DIFFERENCE BUFFERED AMPLIFIER (CDBA)

As we know due to closed loop voltage gain the conventional op-amp suffer from gain bandwidth limitation, a technique used to overcome this is current mode concept. AD844 a current feedback op-amp IC is commercially without suffering from gain bandwidth and slew rate limitation. With trend of evaluation of current mode concept from CCI (Smith and Sedra, 1968) CCII (Sedra and Smith 1970) and a lots of CC block have been observed and adopted in last decade. A new versatile multi terminal active analog building block, current difference buffered amplifier (CDBA) was proposed by Acar and Ozoguz in 1999 [10]. Its flexibility to operate in both current and voltage mode and low parasitic make it suitable for wide band application. It has an attractive feature which is requirement of less no of passive component and

better cascadablity for various analog circuit implementations. A number of modifications are also proposed like CCCDBA, ZC-CDBA etc.

CDBA is a four terminal analog block its characteristic is given by below matrix

$$\begin{vmatrix} Iz \\ Vw \\ Vp \\ Vn \end{vmatrix} = \begin{vmatrix} 0 & 0 & 1 & -1 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{vmatrix} \begin{vmatrix} Vz \\ Iw \\ Ip \\ In \end{vmatrix}$$

The block diagram of CDBA is shown in figure 2.1

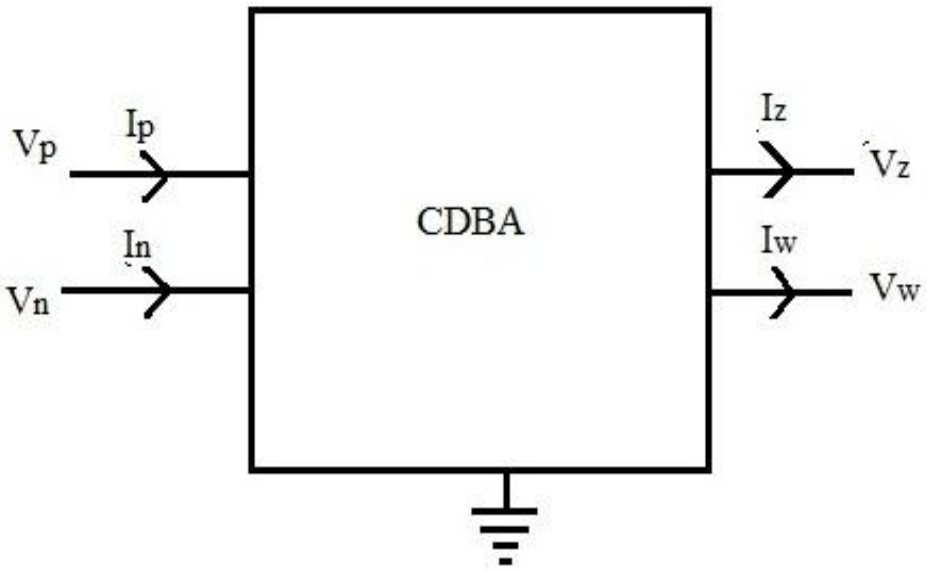


Figure 2.1 CDBA Block diagram [10]

I_p and I_n are current mode input terminal, V_w is voltage mode output terminal, Ideally the input impedance of I_p and In should be zero, practically it should be very low.

The first CDBA was implemented using commercially available CFA AD844 having two input two output by Acar and Ozoguz (1999) [10]. The realization circuit is shown in figure 2.2.

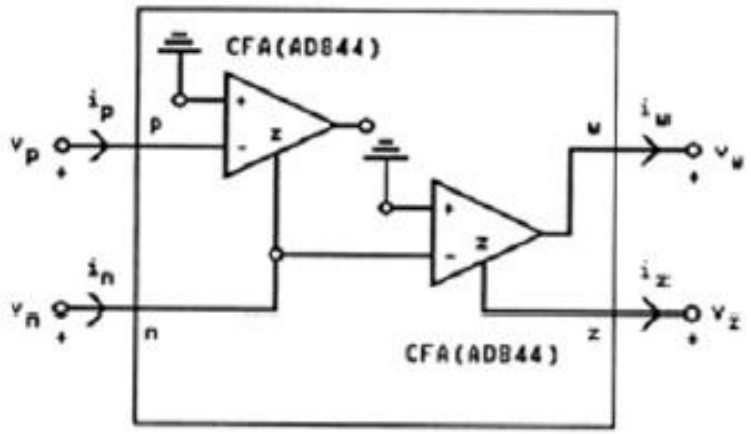


Figure 2.2 Implementation of CDBA with CFAs (Acar and Ozoguz, 1999).

Conventional implementation of CDBA with two AD844 has raised a noisy w-terminal voltage output (Acar and Ozoguz, 1999)[10]. Due to this reason, a new implementation of CDBA is proposed using three AD844 in Figure 2.3 (Koksal, Oner and Sagbas, 2009) [11].

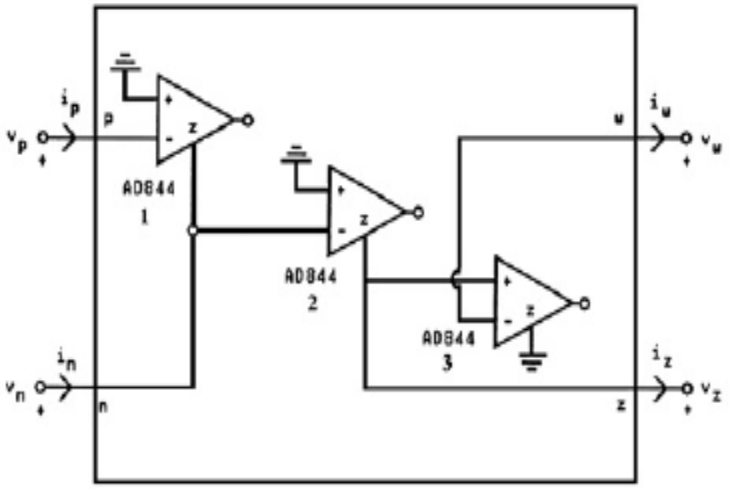


Figure 2.3 Three-AD844 CDBA Realization (Koksal, Oner and Sagbas, 2009).

This new implementation transfers second AD844- Z terminal voltage into the P terminal of the third AD844. As $V_p = V_n$, n-terminal of the third AD844 is used as noise free w-terminal voltage output. Three AD844 CDBA shows good agreement between simulated and experimental results at frequency lesser than 3 MHz but over this frequency range discrepancies arise because of stray capacitances of AD844s which roots affective attenuations at high frequencies

In 2000 a simplified CMOS implementation of CDBA was given by Toker, ozoguz, cicekoglu, and Acar [13]

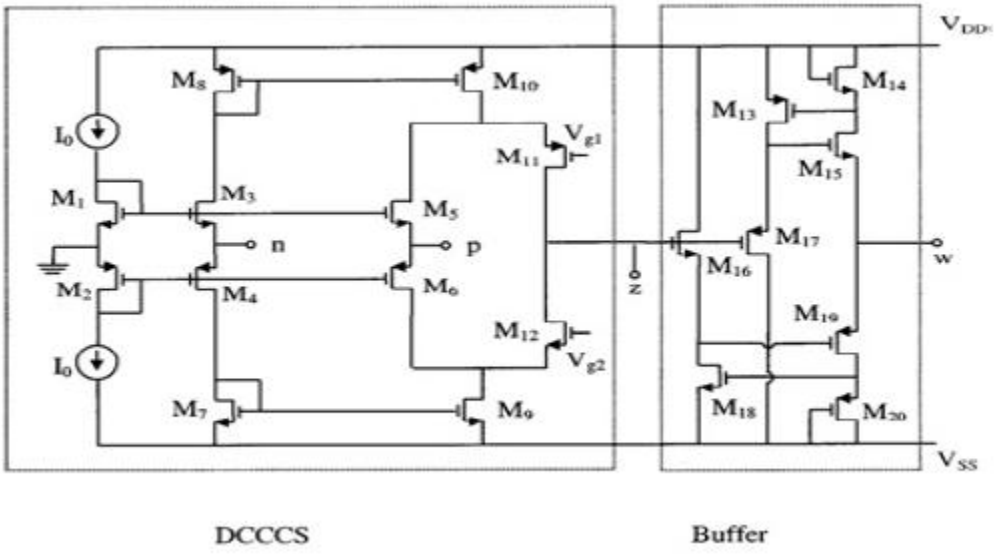


Figure 2.4 Simplified Implementation of CMOS CDBA (Toker *et al.*, 2000).

In Figure 2.4, the aspect ratio of the transistor M_3 (M_4) should be twice as large as to those of M_1 (M_2) and M_5 (M_6). This circuit can be converted to the well-known CFOA by removing the transistor M_5 and M_6. This shows that CDBA is a less complicated circuit compare to some other current mode active element. CDBA offers the advantages of the CFA and CCII, such as high slew-rate, wide bandwidth and simple implementation.

In 2001, Tarim and Kuntman presented a current differencing buffer amplifier employing two CCII and a voltage buffer. It is apparent that overall performance is determined by the performance of CCII and voltage buffer blocks. Tangsrira T, Fujii and Surakampontorn proposed a CDBA in low voltage operation (Tangsrirat, Fujii and Surakampontorn, 2002). The difference of current I_p I_n, is converted to the output voltage V_w, through an impedance connected at the terminal *z*. A CDBA is basically a combination of a current subtracted (current differencing circuit) and a voltage follower [13].

CMOS based CDBA shows quite high (of several hundred ohm) terminal resistance (Ozoguz, Toker andAcar, 1999), (Tarim and Kuntman, 2001) and voltage gain, $\beta \approx 0.7$. This limits the CDBA application and need to include methods to compensate these effects. Thus a low supply operated CDBA with low input terminal resistance are the natural choice for analog signal processing circuits. In order to achieve that, a low-voltage CDBA using only NMOS transistors proposed by W. Tangsrirat, K. Klahan, T. Dumawipata and W. Surakampontorn in 2006 (Tangsrirat *et al.* 2006) [14]. The proposed CDBA has low resistance value at both current-input terminal (p, n) and at the output-voltage terminal (w). A low impedance current conveyor (CCII+) is used with some modification for current differencing circuit realization. In the realization of CDBA, a negative current mirror using only NMOS is employed to achieve the

high frequency response as signal has an all NMOS signal path. Since the unity gain bandwidth depends on transconductance, All NMOS path is used due to the superiority of NMOS over PMOS(1) For a typical n-well process, unity gain frequency of NMOS devices is approximately twice that of PMOS devices which is due to the higher saturation velocity of electron compared to holes. (2) Gate length of PMOS must be three times wider than NMOS to obtain the same transconductance in view of the fact that the junction capacitance per unit area is approximately two times larger for PMOS as that of for NMOS.

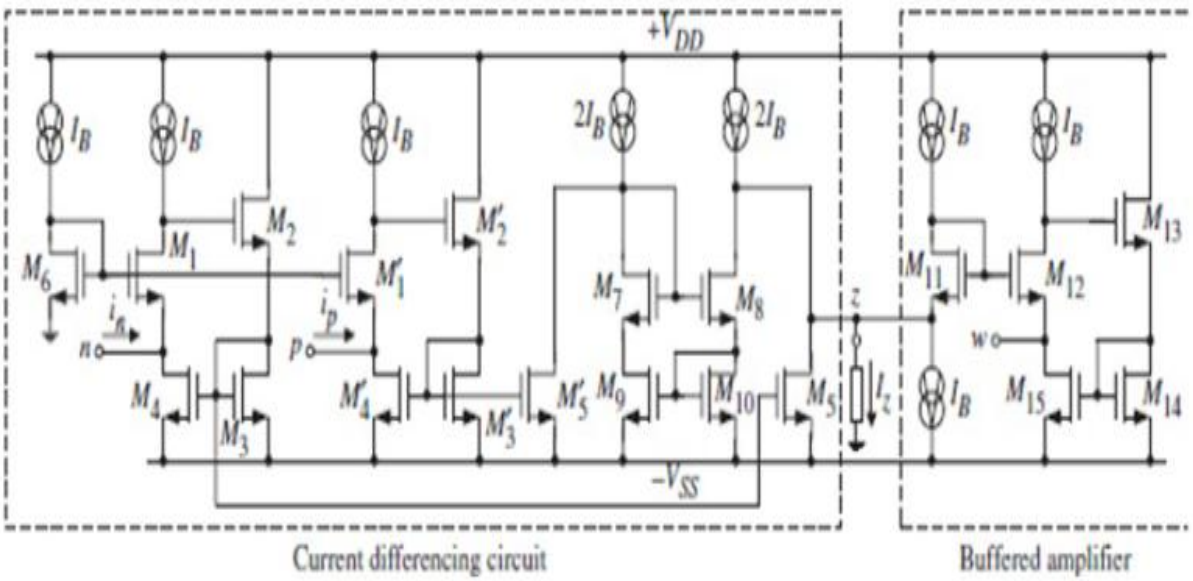


Figure 2.5 Low-Voltage NMOS CDBA [14]

In 2006 Sawangaroml, Tangsrirat and Surakampontom proposed NPN transistor based CDBA in 2006 (Sawangaroml, Tangsrirat and Surakampontom, 2006) [15]. The proposed and designed CDBA can operate with low voltage supply of ±1 volts. In order to achieve the high frequency response, the presented CDBA is designed such that the signal has an all NPN transistor signal path. The circuit in Figure2.6, the current differencing block is functioned by two unity gain current amplifiers composed of Q_1-Q_5 and Q_7-Q_{11} in addition with a current mirror by Q_{12}-Q_{15}, whose output current is the difference of I_p and I_n (I_p-I_n). Buffer voltage amplifier block is given by Q_{16}-Q_{20} which forces the *w* terminal voltage (V_w) to that of the *z* terminal (V_z). This circuit can operate at low supply voltage as only one current source and two transistors are connected between the positive and negative supply rails. The bias current is chosen to be 200 μA for the simulation and the cutoff frequencies of I_z/I_p and I_z/I_n plots are approximately at 126 MHz and 119 MHz respectively. The simulated frequency response of the voltage transfer between the port z and W, with a resistor of 1 kΩ connected from port Z to ground, is observed with -3dB frequency of about 200 MHz [16].

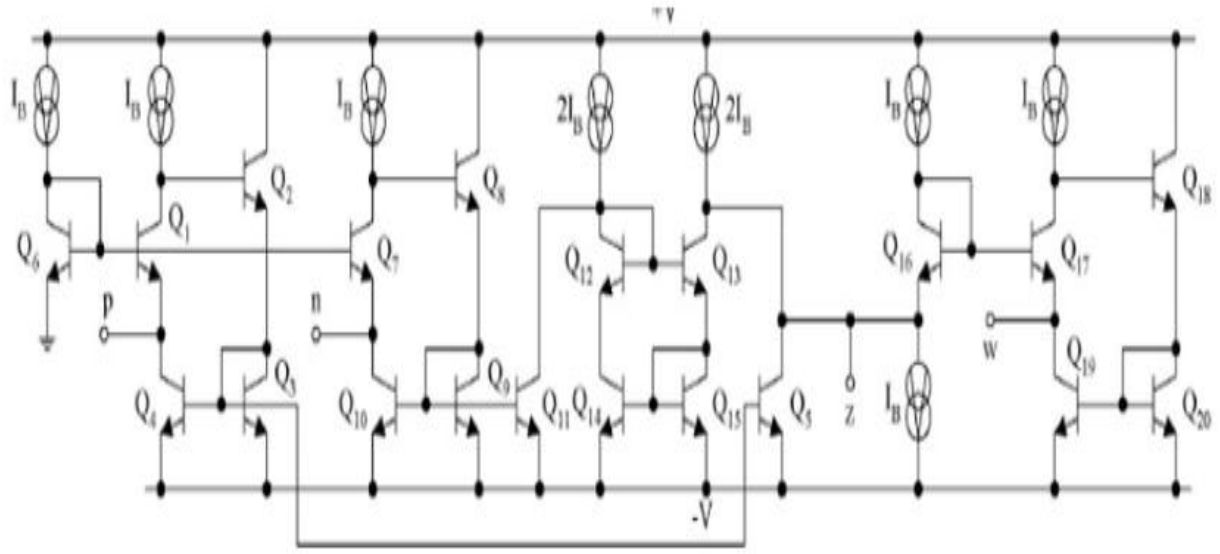


Figure 2.6 NPN Based CDBA (Sawangaroml, Tangsrirat and Surakampontom, 2006).

A low power high performance CDBA is proposed by Cakir and Cicekoglu (Cakir and Cicekoglu, 2008) [17]. The circuit is realized by current differencing circuit (M_1-M_{10}) and voltage buffer (M_{11}-M_{18}) Figure 2.7. This current differencing circuit is based on the flipped voltage follower current sources (FVFCS) which is responsible for the low input resistance at the input ports. The proposed CDBA operates at VSS = ± 0.75 V. The output stage is designed with a differential FVF (DFVF) topology based class AB voltage buffer. This stage offers moderate swing and low output impedance. The simulation result shows that the impedance of port p, n, z and w are 50 Ω, 50 Ω, 102 kΩ and 158 Ω respectively for wide frequency range with current and voltage gain, $\alpha = 0.978$ and $\beta = 0.970$. The power consumption is 1.2 mW and the offset current at port z is 0.14 μA.

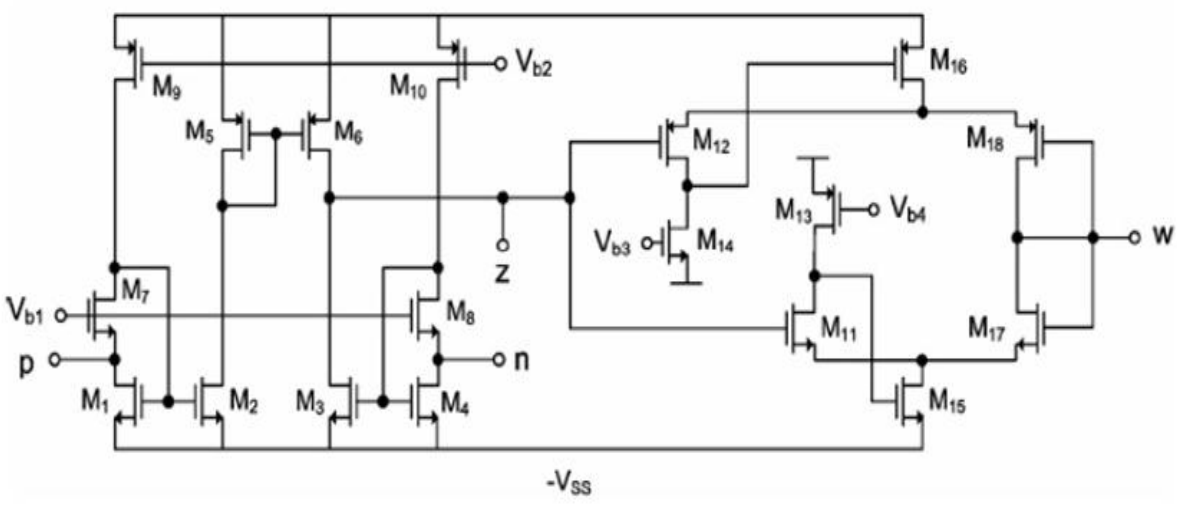


Figure 2.7 Low Power High Performance CDBA (Cakir and Cicekoglu, 2008).

2.2. Comparative analysis of characteristic of various CDBA circuits

The improvement in performance parameters with the development of CDBA from Table 2.1 confirms the suitability of this element in various analog signal processing circuits at low voltage. Also the result claims as a suitable candidature for low voltage low power circuits with a wide frequency range.

Table 2.1 Comparison of Various CDBA circuits

Reference	**Supply (V)**	**Terminal impedance Ω)**				**-3 dB frequency**
		P	**N**	**Z**	**W**	
Toker etal 2000	±2.5	710	390	NA	NA	NA
Tarim and kuntman 2001	±5	645	645	678M	49	70
Tangsrirat, fujii,surakamportorn 2002	±1	NA	NA	1k	10k	100
Tangsrirat et al 2006	±1.25	13	13	290k	13	500
Sawangaromi,tangsrirat, surakamportorn 2006	±1	NA	NA	NA	NA	200
Cakir and cicekoglu 2008	±0.75	50	50	102k	158	NA
Cakir,minaei, and cicekoglu 2009	±0.75	46.9	46.9	185	25.1	158
Cakir,minaei, and cicekoglu 2010	±0.6	56.4	56.4	157k	270	25
Kanjanop and kasemsuwan 2011	±0.7	16.89	15.99	102.4k	15.56	460

CHAPTER 3

FLIPPED VOLTAGE FOLLOWER

The flipped voltage follower (FVF) [23] is just an enhanced type buffer cell having low power and low voltage operation. In last few years use of FVF cell and its application are increasing continuously because of its low voltage and power consumption in deep sub micrometer CMOS technology. The main aim of this chapter is to just understand the basic operation of this cell so that we can utilize the cell and its modification version in analog circuit design.

3.1 Source Follower

Since to achieve a high gain with limited power supply voltage, load impedance should be as large as possible, for these a buffer can be placed after the amplifier so that there is negligible loss of signal level. The source follower (common drain configuration) can be used as a Buffer. The basic source follower configuration is shown in figure 3.1, where the input signal is applied at gate of MOSFET and output is taken from the source. It basically sense the input signal at gate which derive the load at source, thus source potential follow the gate potential , that's why it is called as a source follower.

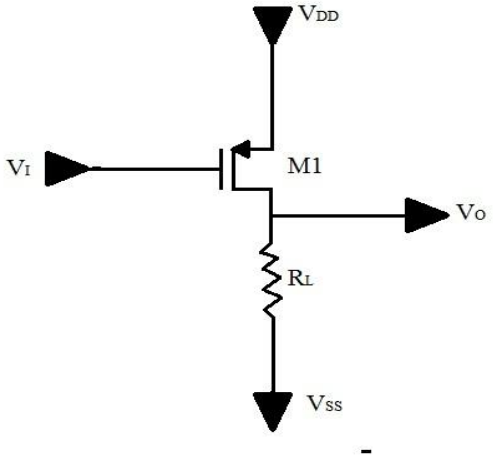


Figure 3.1 Source Follower [23]

With the large signal analysis, when input applied voltage $V_i < V_{th,}$ Transistor M1 is off and $V_o=0$, But on increase the input voltage such that $V_i > V_{th}$ M_1 is ON and goes in saturation and output voltage V_0 is difference of input applied voltage & voltage between gate to source.

$$V_i = V_o + V_{GS} \tag{3.1}$$

Output follow input with a difference level shift of V_{GS}. Since the gate to source voltage is consist of threshold voltage and overdrive voltage. If both of these are constant only then the output follow input and the gain would be unity.

But in practical because of body effect the threshold voltage V_{th} is effected and not remain constant also the overdrive voltage also not remain constant as it depend on drain current which change with output voltage. To study all this effect we will analysis its small signal model. Small signal model of source follower is shown in figure3.2. here the body terminal is connected to lowest supply potential (here it is ground) so that source body junction is reversed bias as a result of these when output voltage V_o changes then V_{BS} also change as output is taken from source terminal.

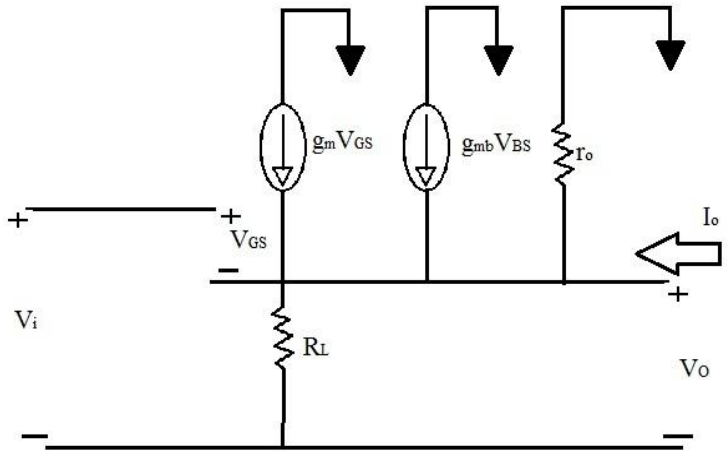


Figure 3.2 Small Signal Model of Source Follower

Applying KCL at output node such that $I_o=0$

$$g_m V_{GS} + g_{mb} V_{BS} + \frac{V_{BS}}{r_o} = \frac{V_o}{R_L} \tag{3.2}$$

But,

$$V_{BS} = -V_o \tag{3.3}$$

Using equation 3.1, 3.3, in 3.2 and rearranging them we can get

$$g_m V_i - g_m V_o - g_{mb} V_o - \frac{V_o}{r_o} - \frac{V_o}{R_L} = 0$$

Again rearranging the terms,

$$\frac{V_o}{V_i} = \frac{g_m}{g_m + g_{mb} + \frac{1}{r_o} + \frac{1}{R_L}} \tag{3.4}$$

If load resistance $R_L = \infty$, (with ideal current source),

Above equation will be modified as

$$\frac{V_o}{V_i} = \frac{g_m r_o}{1 + (g_m + g_{mb}) r_o} \tag{3.5}$$

Equation (3.4) shows that the open circuit gain of source follower is less then unity. On replacing the resistive load with an ideal current source having $R_L=\infty$, we get gain equation (3.5) which shows that the gain is less then unity.

As drain current and g_m increases, $r_{o=}\infty$ the gain equation for source follower will be

$$\frac{V_0}{V_i} = \frac{1}{1 + \frac{g_{mb}}{g_m}} = \frac{1}{1 + \eta} \tag{3.6}$$

Above equation (3.6) also show that the gain of source follower is less then unity, which depend on η, having value in between 0.1 to 0.3. The output resistance of source follower can be calculated from small signal model (figure 3.2) of source follower.

Putting V_i=0, and drive the circuit with output voltage source V_o

Then V_{GS}=-V_o and output current is given by

$$I_O = \frac{V_o}{R_L} + \frac{V_o}{r_o} + g_m V_o + g_{mb} V_o$$

(3.7)

Rearranging equation (3.7) we can get

$$R_o = \frac{V_o}{V_i} = \frac{1}{g_m + g_{mb} + {}^1/_{r_o} + {}^1/_{R_L}}$$

(3.8)

From above equation (3.8), we can see that the body effect reduce is output resistance, which is desirable here as output is voltage. As R_L =∞ and r_o=∞, the new equation for outpour resistance is given by

$$R_o = \frac{V_o}{V_i} = \frac{1}{g_m + g_{mb}}$$

(3.9)

Thus source follower has high input impedance and moderate output impedance.

The nonlinearity of source follower due to body effect can be eliminated if bulk is tied to source, but this technique only possible for PMOS only because all NMOS share the same substrate. From figure 3.3 it can be shown that PMOS source follower having different n-well, thus eliminated the body effect of M1. Source follower also shifts the dc level of input signal by V_{GS} thus limit the voltage swing.

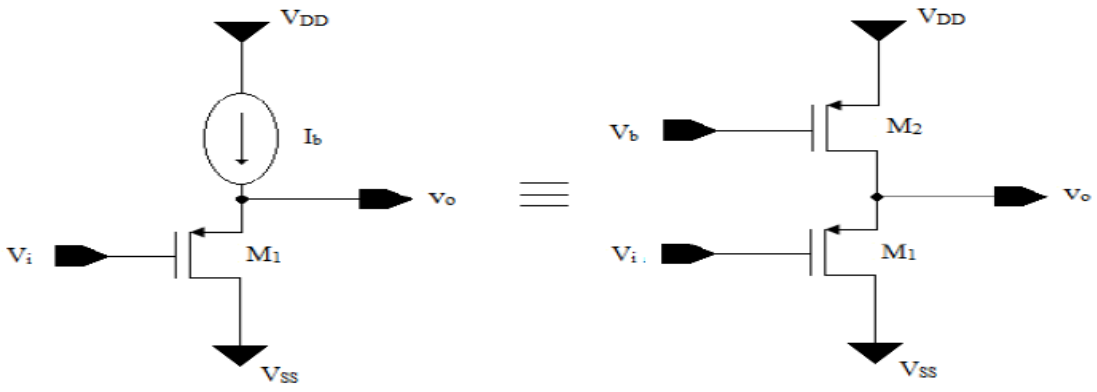


Figure 3.3 PMOS as a Source Follower without Body effect [23]

Thus we can conclude that because of various drawback of source follower like nonlinearity due to body effect, voltage headroom consumption because of level shift due to V_{GS}, poor driving capability limits the use of this topology.

3.2 Flipped Voltage Follower cell

The common drain amplifier shown in figure 3.3 is basically used as a buffer. As we have already discussed it is also call as Source follower. If body effect is neglected output of circuit follow the input with a dc shift of gate to source voltage and which are not constant as current through M_1 depend on output current. The circuit is capable to sink a large current from load but its sourcing capability is limited due to bias current I_b. Thus for large signal as well as small signal behavior, the gain of the common drain (source follower) is less then unity.

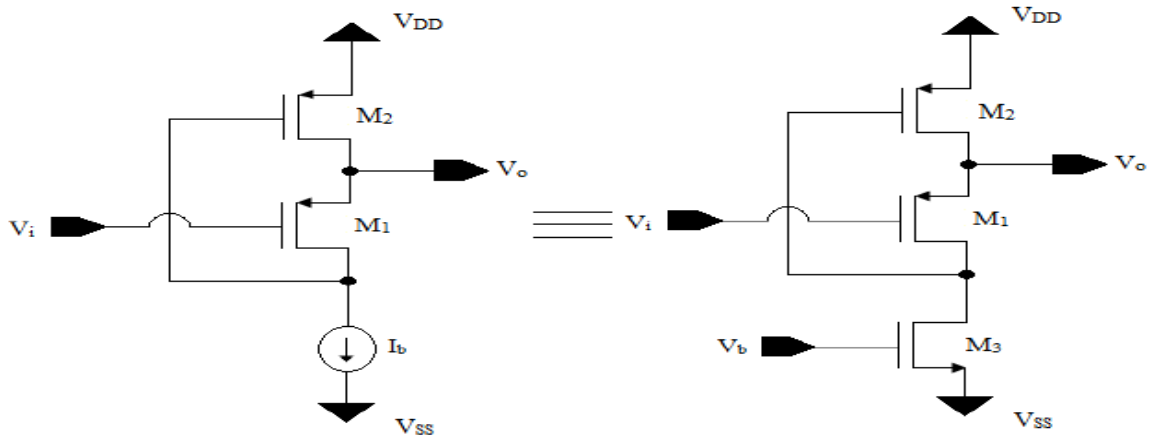


Figure 3.4 Flipped Voltage Follower [23]

Flipped voltage follower is a source follower with a local shunt feedback. The circuit diagram of flipped voltage follower is shown in figure 3.4. It is also called as voltage follower with shunt feedback as shown from circuit a local feedback exist. The current through transistor M_1 is constant, independent to output current. If we neglect short channel effect, V_{SG1} remain constant and the gain of the voltage follower is unity. The circuit shown in figure 3.4 is able to source large amount of current, unlike to basic source follower (figure 3.1) but its sinking capability is limited due to biasing current I_b. The large sourcing capability of FVF is due to its low resistance given by ($R_o= 1/g_{m1}g_{m2}r_{o1}$), which is in order of 20-100 ohm.

In circuit diagram transistor M_2 provide a shunt feedback whereas M1 and M2 provide two pole negative feedback loops. The open loop gain of circuit is given by $A_{OL}=-g_{m2}Ro$.

The FVF cell can be operated at a very low voltage supply, this operating condition is of great advantage as currently in the present world of miniaturization we can use this technique.

From figure 3.4 we can write the following relation

$$V_{SD2}=V_{S2}-V_{D2}= V_{DD}-V_{S1} \tag{3.10}$$

Transistor M_1 is operating in saturation mode, condition of saturation of M_2 is given by blow analysis (Neglecting second order effect)

We can write V_{S1} as

$$V_{S1} = V_{G1}+|V_{TP}|_1+(V_{S1}-V_{G1})-|V_{TP}|_1$$

$$V_{S1} = V_i + |V_{TP1}| + \sqrt{\frac{2I_o}{k_p(W/L)_1}} \tag{3.11}$$

Where Io is Drain current (here I_b), $k_p=\mu_pC_{ox}$, and V_{TP} is threshold voltage of transistor M_1. For saturation of M_2

$$V_{SD2}>V_{SG2}-|V_{TP}|_1$$

Also

$$V_{S1}=V_{D2}$$

$$V_{DD} - \left(V_i + |V_{TP1}| + \sqrt{\frac{2I_o}{k_p(W/L)_1}} \right) > \sqrt{\frac{2I_0}{k_p(W/L)_1}}$$

(3.12)

Now condition for saturation of M_1 assuming that M_2 is in saturation (ignoring second order effect) is given by the following analysis.

$$V_{SG1}\text{-}V_{SD1} < |V_{TP}|_1$$

(3.13)

Also,

$$V_{SG1}\text{-}V_{SD1}=V_{D1}\text{-}V_{G1}$$

$$=V_{D1}\text{-}V_{G1}+V_{DD}\text{-}V_{S2}$$

$$=V_{G2}\text{-}V_1+V_{DD}\text{-}V_{S2}$$

$$=V_{DD}\text{-}V_{SG2}\text{-}V_1$$

$$=V_{DD}\text{-}(|V_{TP}|_2+V_{SG2}\text{-}|V_{TP}|_2)\text{-}V_1$$

$$=V_{DD} - \left(V_i - |V_{TP2}| - \sqrt{\frac{2I_o}{k_p(W/L)_2}} \right)$$

(3.14)

From equation (3.13) and equation (3.14)

$$V_{DD} - \left(V_i - |V_{TP2}| - \sqrt{\frac{2I_o}{k_p(W/L)_2}} \right) < |V_{TP1}|$$

(3.15)

From equation (3.12) and equation (3.15) we can get the range of input signal, which is given by

$$V_{DD} - \left(|V_{TP2|} - |V_{TP1}| - \sqrt{\frac{2I_o}{k_p(W/L)_2}} \right) < V_i$$
$$< V_{DD} - \left(|V_{TP1}| - \sqrt{\frac{2I_o}{k_p(W/L)_2}} - \sqrt{\frac{2I_o}{k_p(W/L)_1}} \right)$$

(3.16)

Equation 3.16 show the range relation of input signal applied to FVF, it can also observed from above relation that valid input signal range decreased with threshold voltage.

3.3 Property of basic FVF Cell

- Since the current through M1 is constant, which give more precise copy of input signal to that at output thus the gain is almost truly unity, which was less then unity in conventional source follower.
- Its operating potential is very low.
- FVF cell is capable to source large amount of current, which is not possible in simple source follower.
- It provides very low output impedance.
- It can be implemented as active DC level shift.

3.4 Basic structures of Flipped voltage follower

3.4.1 Flipped Voltage Follower Current sensor (FVFCS)

When FVF cell is used as a current sensing, it is called as Flipped voltage follower current sensor (FVFCS) [23].The circuit diagram of FVFCS is shown in figure 3.5. Assume node X as input current sensing node and all transistor are biased such that they all operate in saturation mode. As we know due to shunt feedback due to M_2, impedance at node X is very low. The current flowing through this node does not change the value of its voltage and thus node X can source a large current variation at input. The FVF cell translate them as voltage variation on output node Y.As show in circuit, this voltage can be used to generate replica of input using transistor M_5.The output and input current are related as

$$I_O=I_{in}+I_b$$

Where I_b is the bias current, and can be removed by various technique if needed. FVFCS can be operated at a very low voltage supply. The relation for supply voltage is given by

$$V_{DD}^{MIN} = V_{TP} + 2V_{DSat}$$

Where V_{TP} is threshold voltage and V_{DSat} is minimum drain to source voltage so that transistor are in saturation mode.

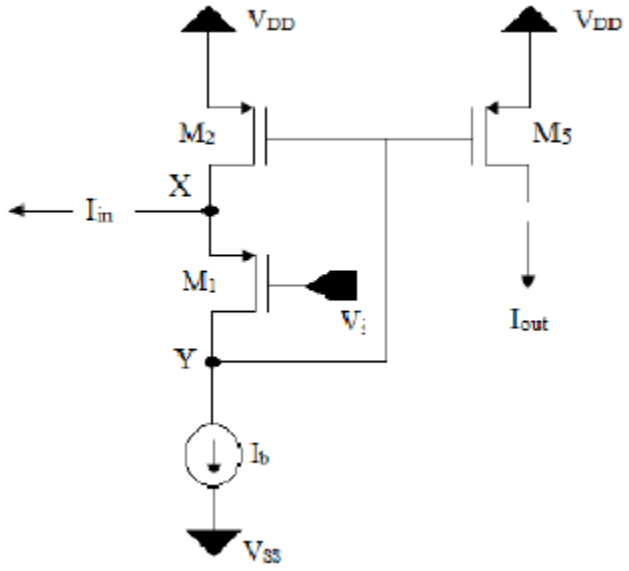


Figure 3.5 Flipped Voltage Follower Current Source (FVFCS) [23]

3.4.2 Flipped voltage follower differential structure (DFVF)

The first differential structure based on FVF cell can be built by adding a transistor M_3 at node X. The structure that forms is called as FVF differential structure (DFVF) [23]. The circuit of DFVF is shown in figure 3.6.

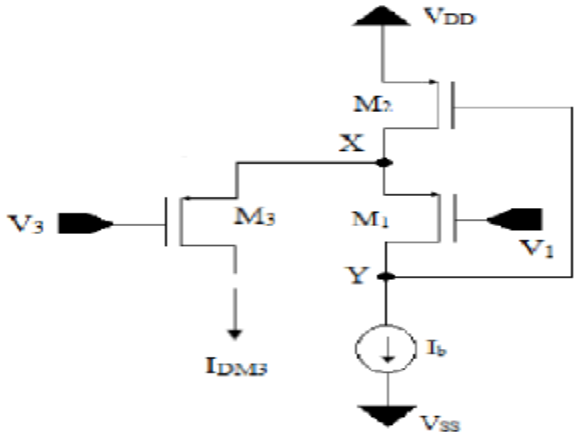


Figure 3.6 Differential Flipped Voltage Follower (DFVF) [23]

As we know the impedance at node X is very low due to shunt feedback, thus its voltage remains almost constant for a large current from M_3. Under quiescent condition, if $V_1=V_2$ and M_1, M_2 are of same size, then it satisfied $I_{DM1}=I_{DM3}=I_b$. Differential voltage V_1-V_3 generates a typical current variation in transistor M3 which follow MOS square law. One of important property of this circuit is that the maximum output current could be much larger then quiescent current. Another advantage of DFVF is that output is available both as current and voltage. The minimum supply voltage is given by

$$V_{DD}^{MIN} = V_{TP} + 2V_{DSat}$$

Where V_{TP} is threshold voltage and V_{DSat} is drain to source voltage so that all transistors operate in saturation mode.

3.4.3 FVF Pseudo-Differential Pair (FVFDP)

We can easily construct a pseudo differential pair from DFVF just by adding an extra transistor M_4 at node X. The structure will call as FVF pseudo differential pair (FVFDP) [23] as shown in figure 3.7.

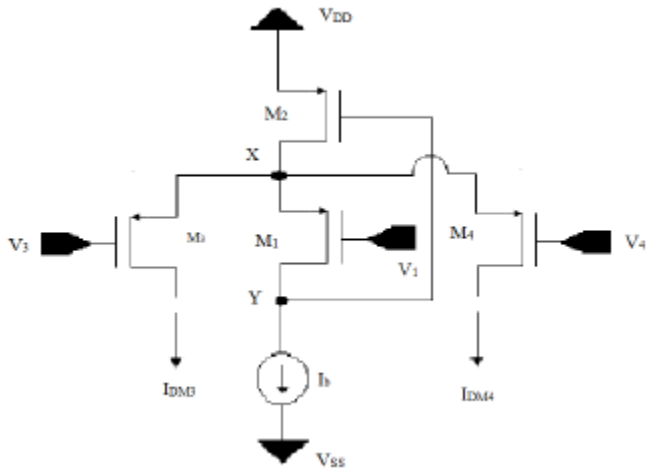


Figure 3.7 Flipped Voltage Follower Differential Pair FVFDP [23]

Under quiescent condition, $V_1=V_3=V_4$, and assuming M_1, M_3, M_4 are perfectly matched, the voltage at gate of M_1 is $V_1=(V_3+V_4)/2=V_{CM}$.

The difference between DFVF and FVFDP is that FVFDP is true differential output. The output current of DFVF is large if V_1-V_3 is positive but if V_1-V_3 in negative it is zero, while in case of FVFDP it could be positive or negative depending on value of input differential voltage. The minimum supply voltage for FVFDP is same as that of FVFCS and DFVF.

3.5 Simulation Result

3.5.1 Source Follower

From circuit diagram of figure 3.2, PSPICE simulation of source follower is done using 0.18 um CMOS technology. The transistor dimension is listed in Table 3.1.The value of input voltage is 0.25V, bias voltage is 0.35V, supply voltage is 0.9V and source voltage is zero.

Table 3.1 Transistor dimension of voltage follower

Transistor	W (µm)	L (µm)
M_1	15	0.2
M_2	13.9	0.2

The DC transfer characteristic of voltage follower is shown in figure 3.8. Here input voltage V_i is varied from 0 V to 0.6 V with an increment of 0.01 V. It is observed that output of voltage follower varies linearly with input from 0 V to 0.3 V. The total power consumption of voltage follower is 21.1 µwatt.

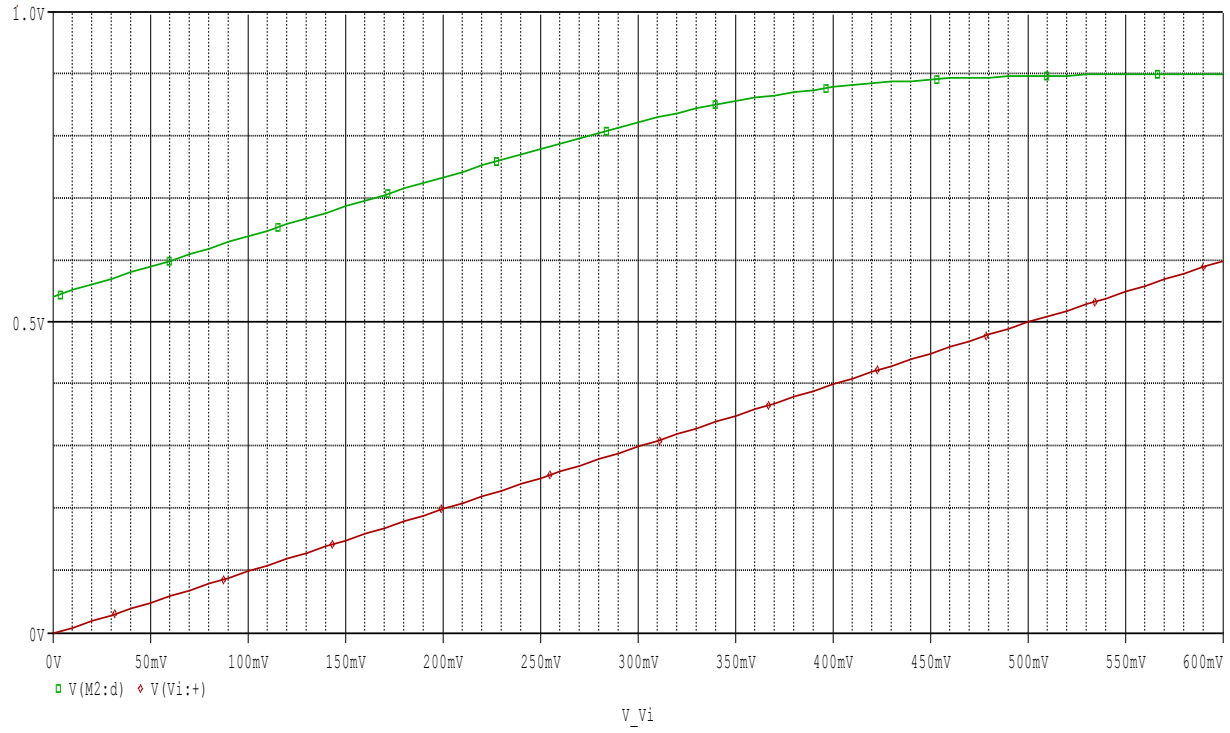


Figure 3.8 DC transfer curve of voltage follower

3.5.2 Flipped Voltage follower (FVF)

The circuit diagram of FVF cell shown in figure 3.3 is simulated on PSPICE using 0.18µm CMOS technology. The transistor dimension is listed in table 3.2. The input applied voltage (Vi), bias voltage (V_b), supply voltage (V_{dd}), and source voltage (V_{ss}) are chosen as 0.12 V, 0.7V, 0.9V, and 0V respectively.

Table 3.2 Transistor dimension of FVF cell

Transistor	W(um)	L(um)
M_1	110	2
M_2	17.8	2
M_3	0.5	0.5

The DC transfer curve of FVF cell is shown in figure 3.9 where input voltage Vi is varied from 0 V to 0.4 V with an increment of 0.01V. It can be seen from DC response that the output of FVF follow input from 0V t0 0.3 V linearly. Figure 3.10 show the transient response which show output follow input.

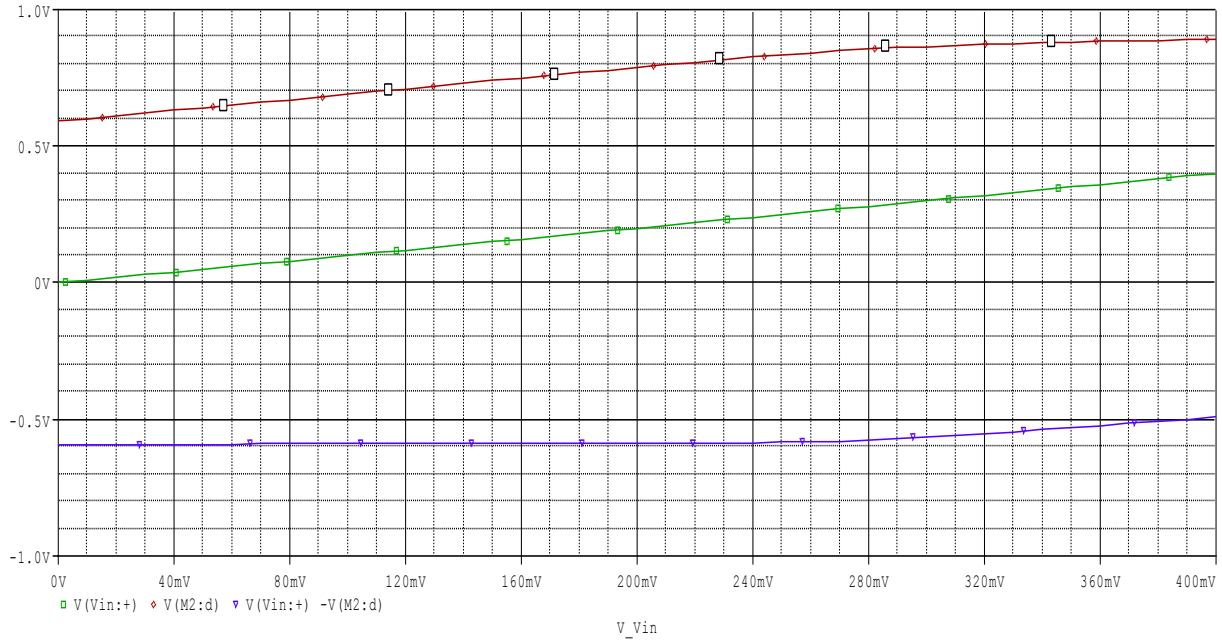


Figure 3.9 DC response of FVF cell

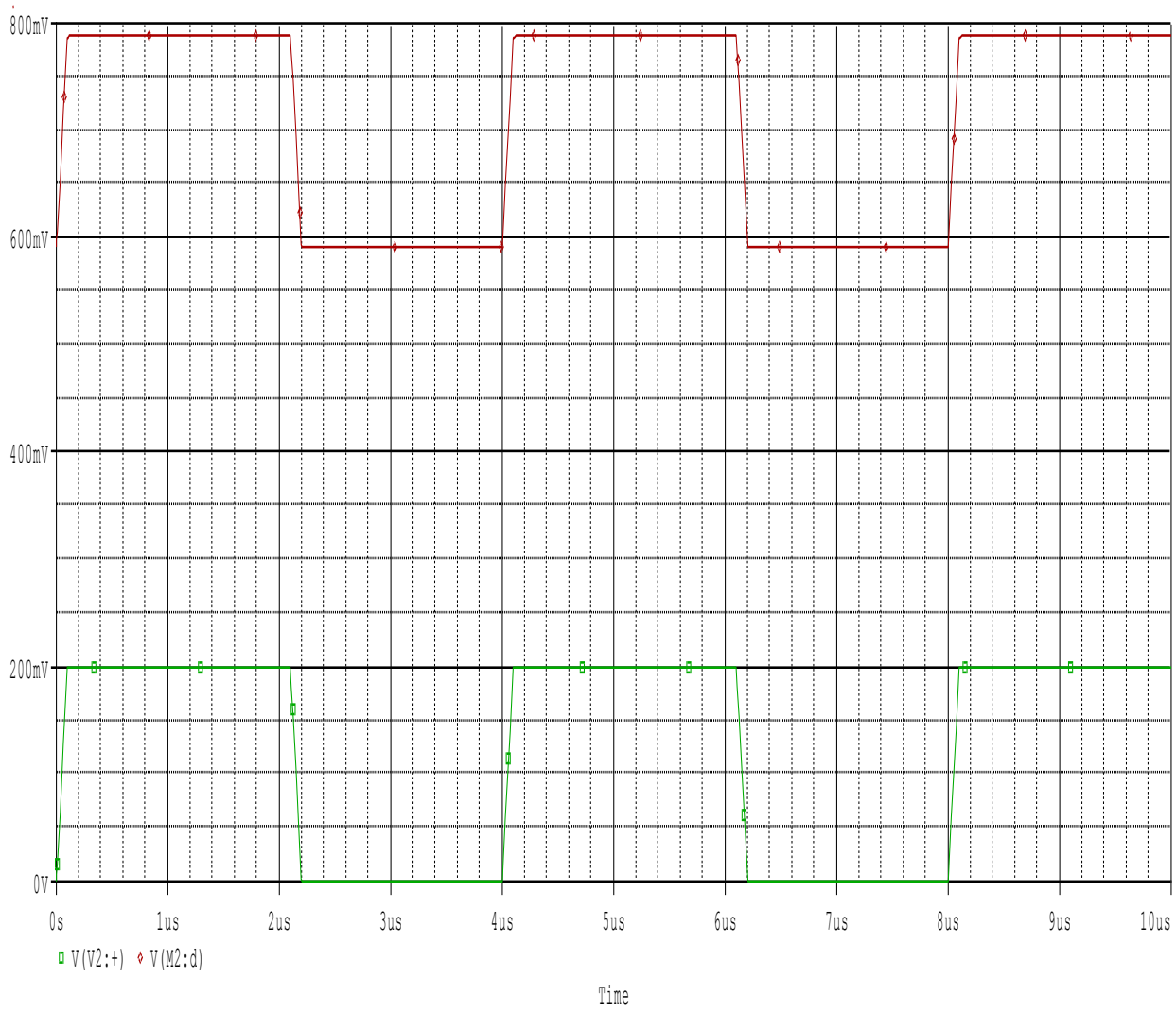


Figure 3.10 Transient response of FVF cell

The frequency response of FVF cell is shown in figure 3.11 which show that the bandwidth of FVF cell is about 30 MHz. The power consumption of flipped voltage follower cell is about 7.89 µwatt.

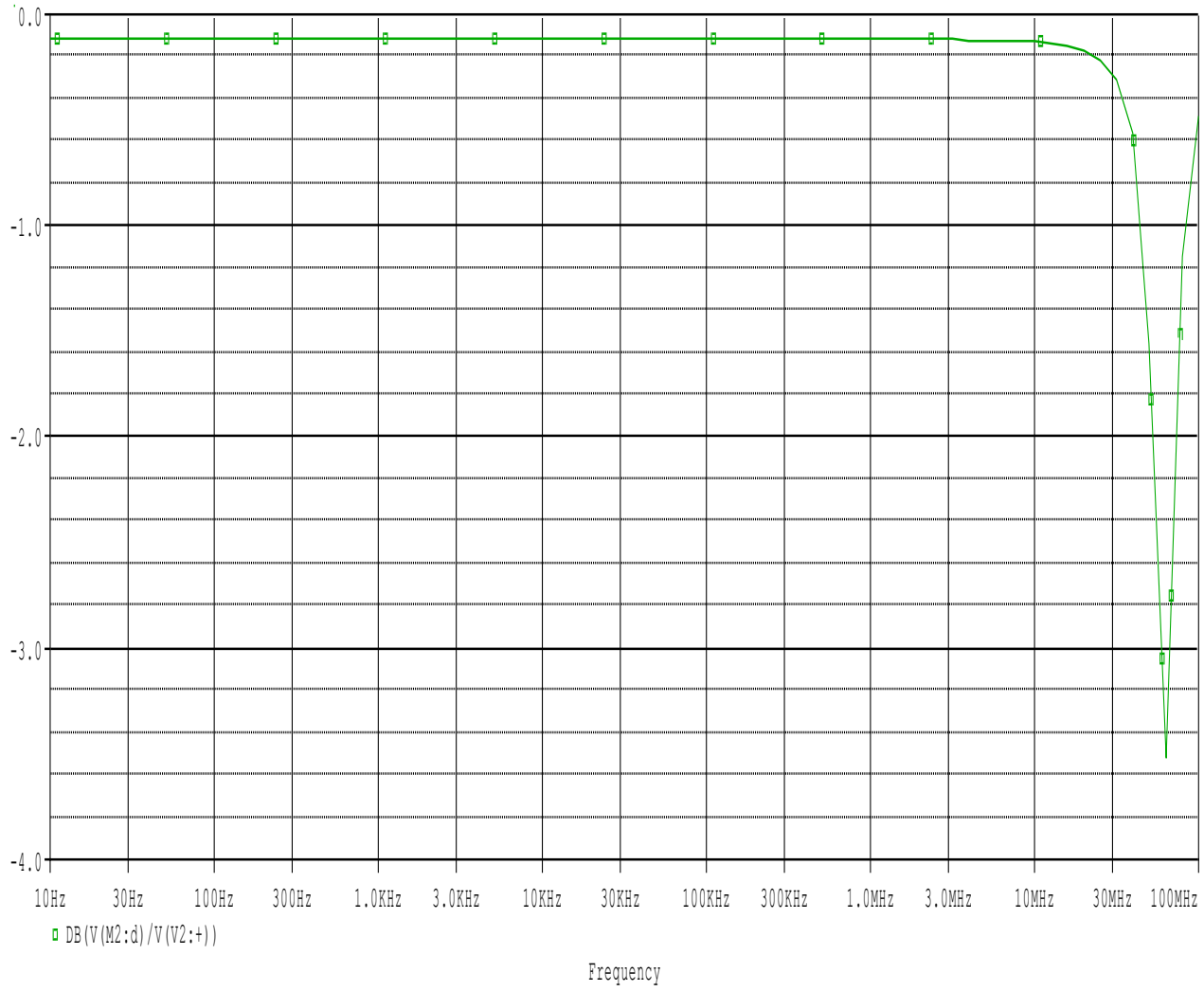


Figure 3.11 Frequency response of FVF cell

Thus from simulation of source follower and FVF cell we analyses that while using same power supply the power consumption of FVF cell is very low in comparison to source follower, this potential of FVF can be exploited to design various Analog building block (ABB) having low power consumption.

CHAPTER 4

CURRENT DIFFERENCE BUFFERED AMPLIFIER (CDBA)

The first CDBA was introduced by Acar & Ozoguz [10], which can operate both in current as well as voltage mode. There were also many other implementation of CDBA using bipolar technology and CMOS technology reported in literature survey. In present chapter we will realize a FVF based CDBA [17] on PSPICE using 0.18µm parameter.

4.1 Basic Block Diagram and Circuit Description

CDBA is consists of two fundamental block, Current difference unit also called as current subtractor followed by a voltage buffer. The block diagram of CDBA [10] is shown in figure 4.1

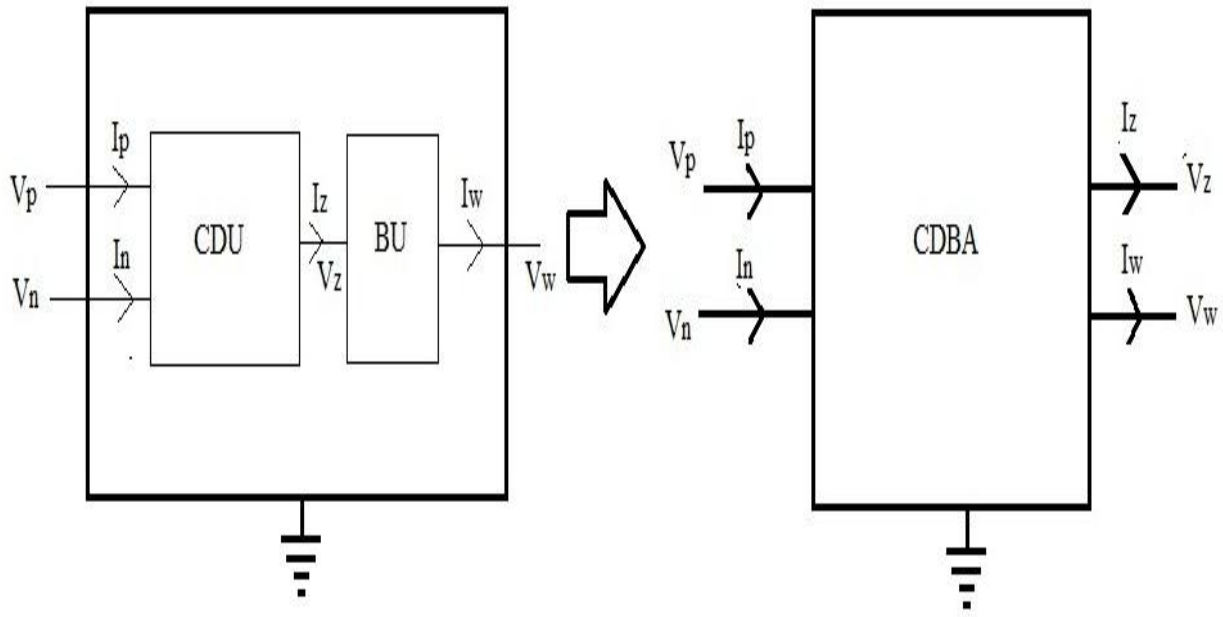


Figure 4.1 Block diagram of CDBA [10]

Input is applied to two different terminal of subtractor, the difference of applied Input is obtained at output of CDU which is fed to input terminal of buffered unit whose output terminal just followed the input applied to it. Thus the complete unit is current difference buffered amplifier. The equivalent circuit of CDBA is shown in figure 4.2 [10].

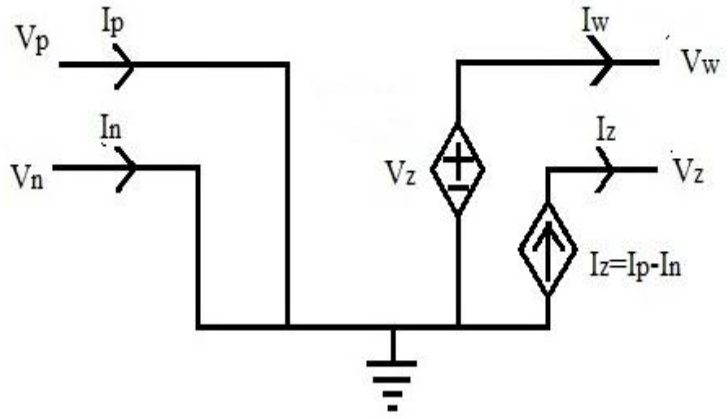


Figure 4.2 Equivalent circuit of CDBA [10]

The Characteristics of Voltage and current of CDBA can be describe by the following current and voltage equation:-

$$I_z = \alpha_p I_p - \alpha_n I_n$$

$$V_w = \beta_v V_z$$

$$V_P = V_N = 0$$

Where parameter αp & αn are current gain and βv is the voltage gain.
Under ideal condition the value of all above parameter should be unity and ideal current and voltage equation would be written as:-

$$I_z = I_p - I_n$$

$$V_w = V_z$$

$$V_P = V_N = 0$$

From above diagram it is clear that p and n are current mode input terminal whose impedance should be minimum and under ideal condition it should be zero. The current at output terminal z is difference of Ip and In and its impedance should be high ideally infinite. The voltage of terminal W follows to that of terminal Z.
The port relation of CDBA can also characterized by following matrix

$$\begin{vmatrix} Iz \\ Vw \\ Vp \\ Vn \end{vmatrix} = \begin{vmatrix} 0 & 0 & 1 & -1 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{vmatrix} \begin{vmatrix} Vz \\ Iw \\ Ip \\ In \end{vmatrix}$$

4.2 Current Difference Unit (CDU)

The current difference unit of CDBA is based on flipped voltage follower current source (FVFCS) having very low input impedance as well as very low power dissipation. The circuit of CDU [17] is shown in figure 3 consisting of transistor M1 to M8. From circuit it can be seen that current at terminal Z is the difference of input terminal current Ip and Iz. Thus terminal z is output terminal of subtractor. Assuming transistor pair M_1-M_4, M_7-M_8, M_5-M_6 are perfectly matched and operated in saturation region.

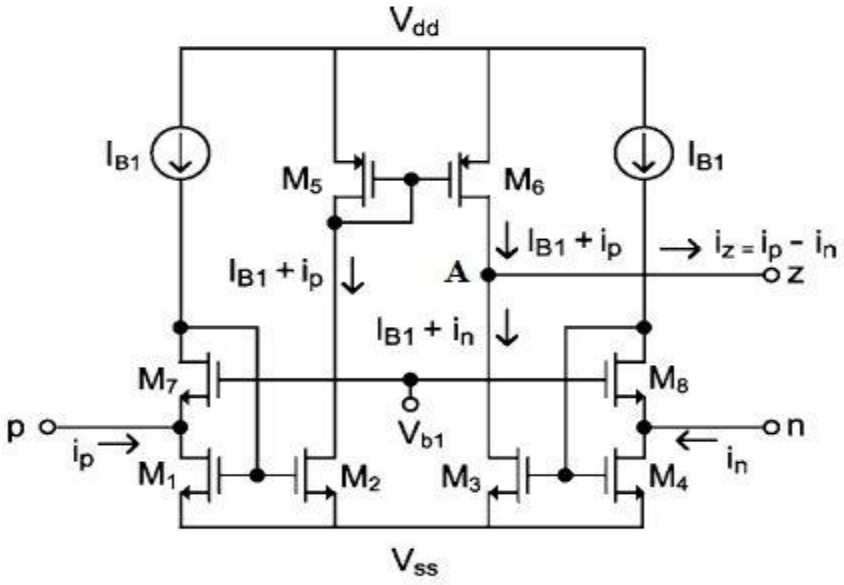


Figure 4.3 Current difference unit (CDU) of CDBA [19]

Biasing current I_{B1} is applied as shown in circuit. Transistor M_5 and M_6 are perfectly matched and constitute a simple current mirror, so the current equation will be

$$I_{D(M5)}=I_{D(M6)}$$

$$I_{B1}+I_p=I_{B1}+I_p$$

Applying KCL at node “A” we get the current equation as

$$I_z=I_{DM6}-I_{DM3}$$

But,

$$I_{DM3}= I_{B1}+I_n$$

So,

$$I_z= I_{B1}+I_p-(I_{B1}+I_n)$$

$$I_z= I_p-I_n$$

(4.1)

Thus the above equation show that current at output terminal Z is the difference of current applied at input.

4.2.1 Calculation of input impedance

In CDBA the applied signal is current so ideally its input impedance should be zero and practically it should be low. Since in input stage of CDU is a FVFCS, so to find the expression of input impedance we have to perform small signal analysis [23].

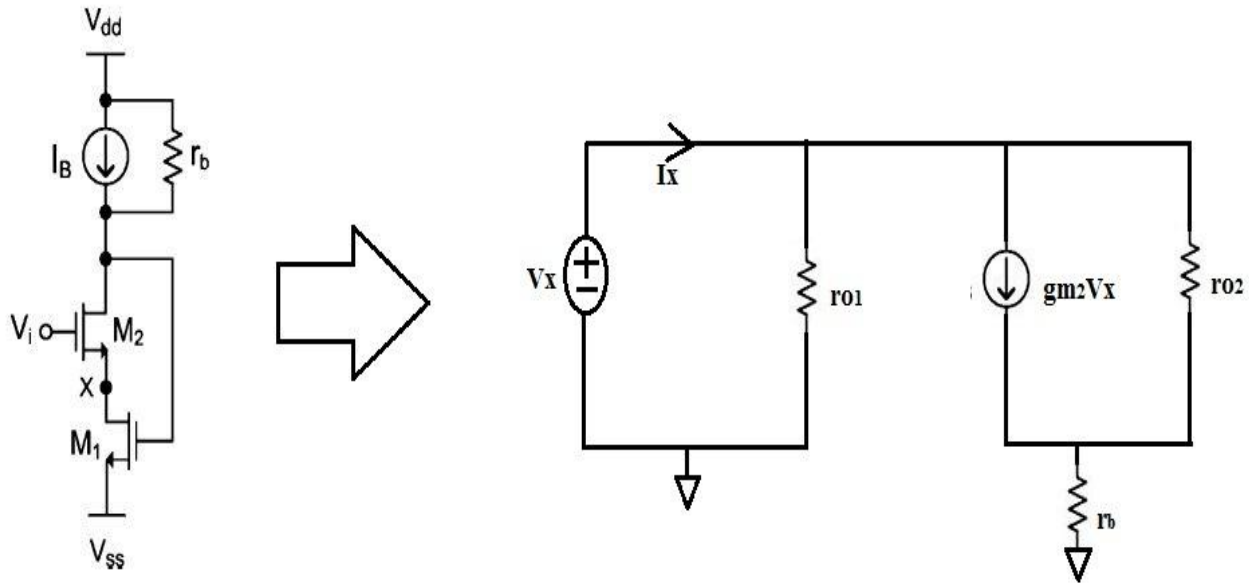


Figure 4.4 Small signal model of input terminal of CDBA [23]

Applying KCL at node X

$$I_X = \frac{V_x}{r_{o1}} + g_{m2}V_x + \left(\frac{V_x - V_D}{r_{02}}\right)$$

(4.2)

$$g_{m2}V_x + \left(\frac{V_x - V_D}{r_{02}}\right) = \frac{V_D}{r_b}$$

(4.3)

$$V_D = \frac{(g_{m2}r_{o2} + 1)\left(\frac{r_b}{r_{o2}}\right)}{1 + \left(\frac{r_b}{r_{o2}}\right)} V_x$$

(4.4)

Rearranging equation (4.2) and (4.3), we get

$$\frac{V_x}{I_x} = \frac{r_{o1}\left(1 + \frac{r_b}{r_{o2}}\right)\frac{1}{g_{m2}}}{r_{o1}\left(1 + \frac{1}{g_{m2}r_{o2}}\right) + \left(1 + \frac{r_b}{r_{o2}}\right)\frac{1}{g_{m2}}}$$

Using approximation $g_{m2}r_{02} \gg 1$

$$R_{OLX} = r_{o1} || \left(1 + {}^{r_b}/_{r_{o2}}\right)\frac{1}{g_{m2}}$$

(4.5)

Close loop gain is given by

$$R_{CLX} = \frac{R_{OLX}}{1 + |A_{OL}|}$$

But,

$$A_{OL} = \frac{V_r}{V_t} = -g_{m1}(r_b || g_{m2} r_{o1} r_{o2})$$

So,

$$R_{CLX} = \frac{r_{o1} || \left(1 + {}^{r_b}/_{r_{02}}\right) {}^{1}/_{g_{m2}}}{1 + g_{m1}(r_b || g_{m2} r_{01} r_{02})} \tag{4.6}$$

If,

$$r_b \cong r_{01}$$

Then,

$$R_{CLX} = \frac{2\left({}^{1}/_{g_{m2}} || r_{01}\right)}{g_{m1}(r_{02} || g_{m2} r_{01} r_{02})} \tag{4.7}$$

Using approximation $g_{m2} r_{02} \gg 1$

$$R_{CLX} = \frac{{}^{2}/_{g_{m2}}}{g_{m1}\left(\frac{r_{02} g_{m2} r_{01} r_{02}}{(r_{02}(1 + g_{m2} r_{01}))}\right)} \tag{4.8}$$

$$R_{CLX} \cong \frac{2}{g_{m1} g_{m2} r_{02}} \tag{4.9}$$

From equation (4.9), the input impedance of both the terminal of CDU is very low.

4.2.2 Buffered Unit (BU)

The output stage of CDBA, Which is a Buffered unit [17] consist of transistor consist of 6 transistor M_9 to M_{14} having two biasing current I_{B1} and $I_{B2.}$ The output is based on differential flipped voltage follower (DFVF), which we have already discuss earlier.one of the advantage of DFVF is that it can operate at very low voltage.

Thus the complete circuit diagram of realized CDBA is shown in figure 4.5

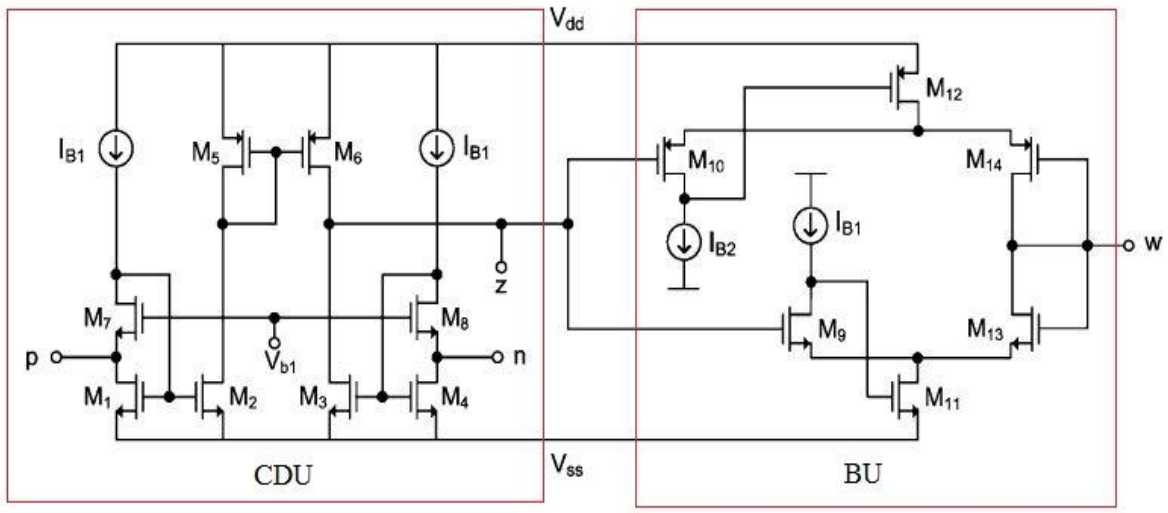


Figure 4.5 FVF based CDBA [19]

The circuit is consists of only 14 transistor, having very low input impedance, low power dissipation. The aspect ratio of transistor is shown in table 4.1

Table 4.1 Transistors dimension of CDBA

Transistor	W (µm)	L(µm)
M_1, M_2, M_3, M_4	27	4
M_5, M_6,	90	1.8
M_7,M_8	180	0.90
M_9	6	0.24
M_{10}	18	0.24
M_{11}, M_{13}	30	0.24
M_{12}, M_{14}	99	0.24

4.3 Simulation Result of CDBA

The simulation of above CDBA circuit is done on ORCAD PSPICE using 0.18µm parameter. The transistor dimensions are reported in table 4.1 and the biasing current used is 56µA and 84µA. The following result have been analysis from above simulation

4.3.1 Current Transfer Characteristic

On performing DC analysis of CDU via varying input current from -80µA to 80µA, it is observed the current at terminal Z is difference of I_p and I_z from -60µA.

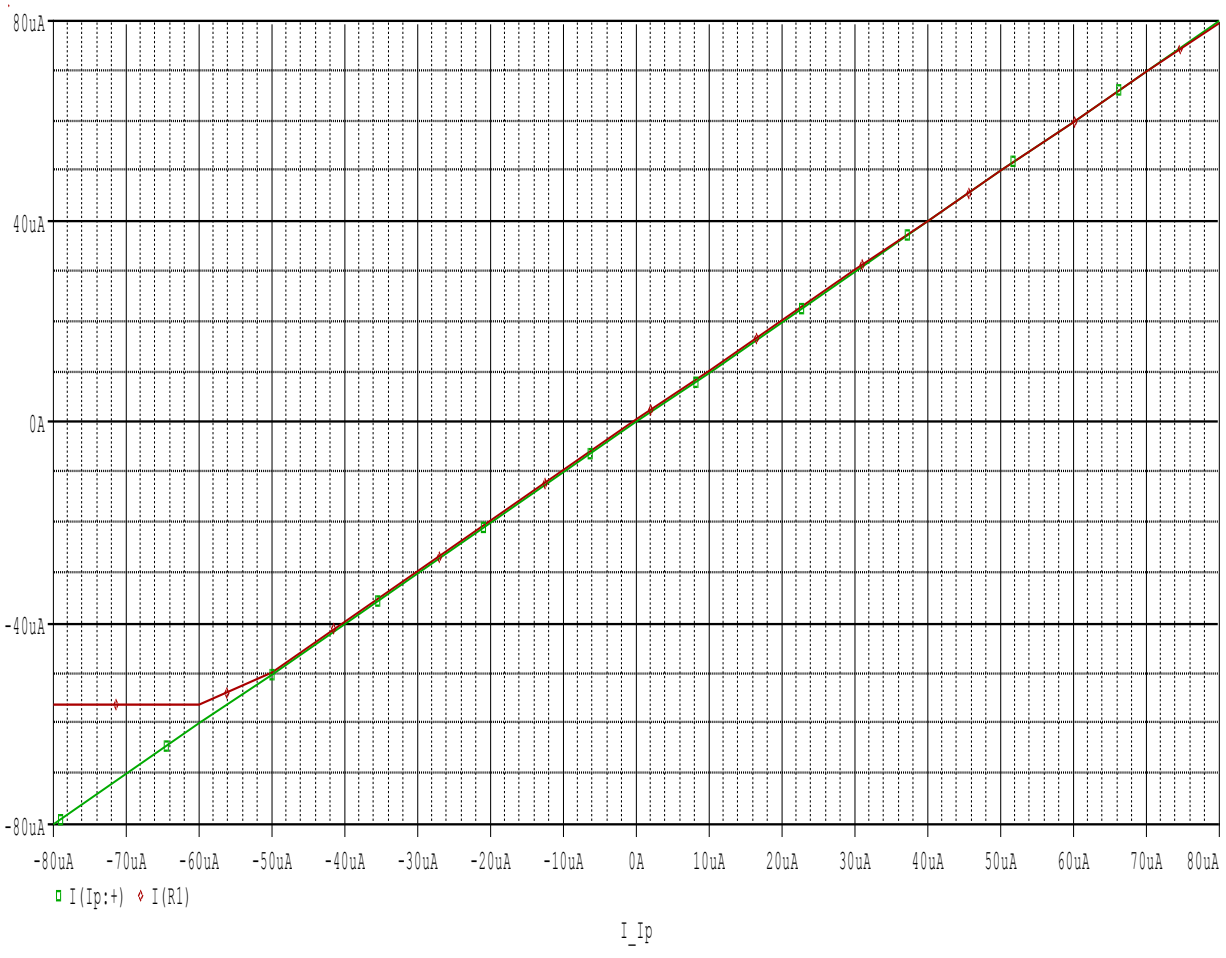


Figure 4.6 Current Transfer Characteristic

4.3.2 Input Impedance

The input impedance is defined as voltage at that terminal divided by current at that terminal. The mathematical expression for input impedance of CDBA is already derived which show that it should be very low. On simulation the circuit on PSPICE the input impedance is found to be very low about 76 ohm which is very low

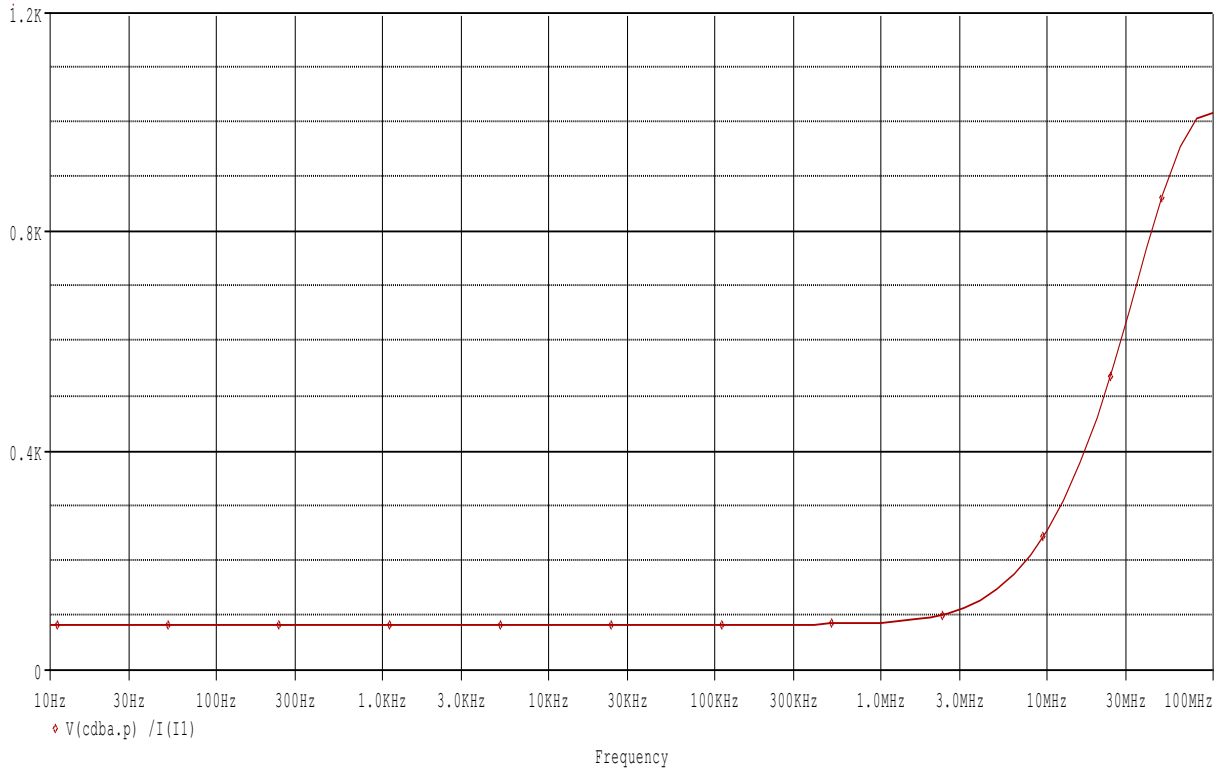


Figure 4.7 Input terminal impedance

4.3.3 Terminal Z impedance variation with frequency

Z is the output of CDU where we get difference of applied input at I_p and I_z. Since CDU is current mode circuit so its output impedance should be high. On observing from graph is the found that its output impedance is about 135 KΩ.

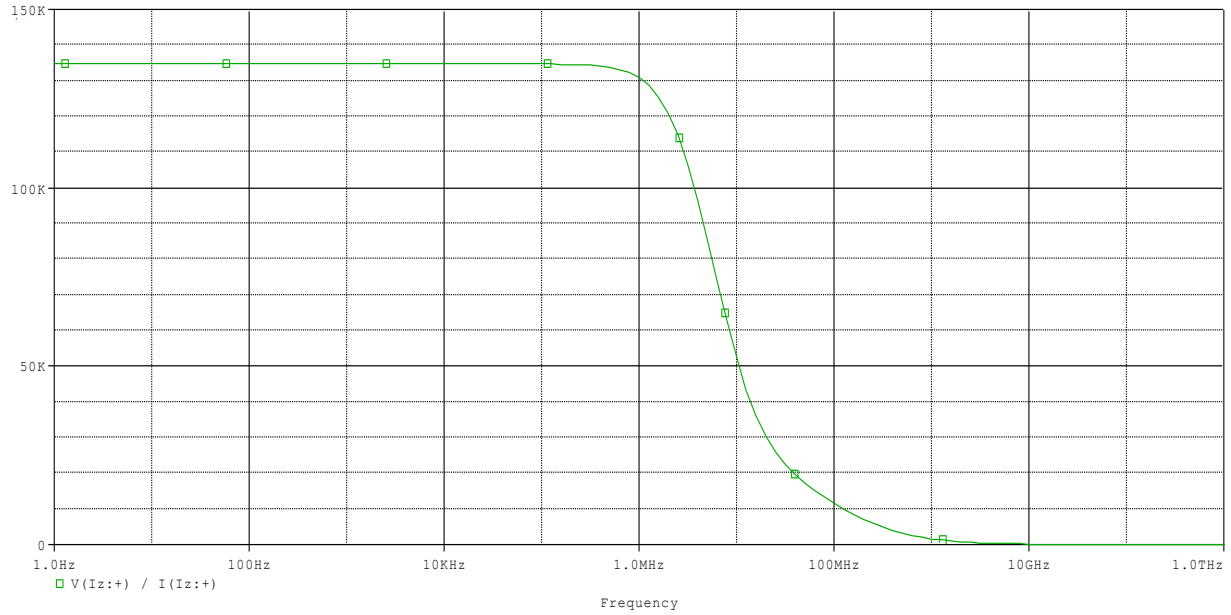


Figure 4.8 Terminal Z impedance Magnitude with Frequency Variation

4.3.4 Voltage transfer characteristic (VTC)

The voltage transfer characteristic is shown in figure 4.9, it is graph between output voltage Vw against voltage Vz. From simulation it is observed that Vw follow Vz from -100mV to 100mV and the error increases for Vz value greater then ± 100mV

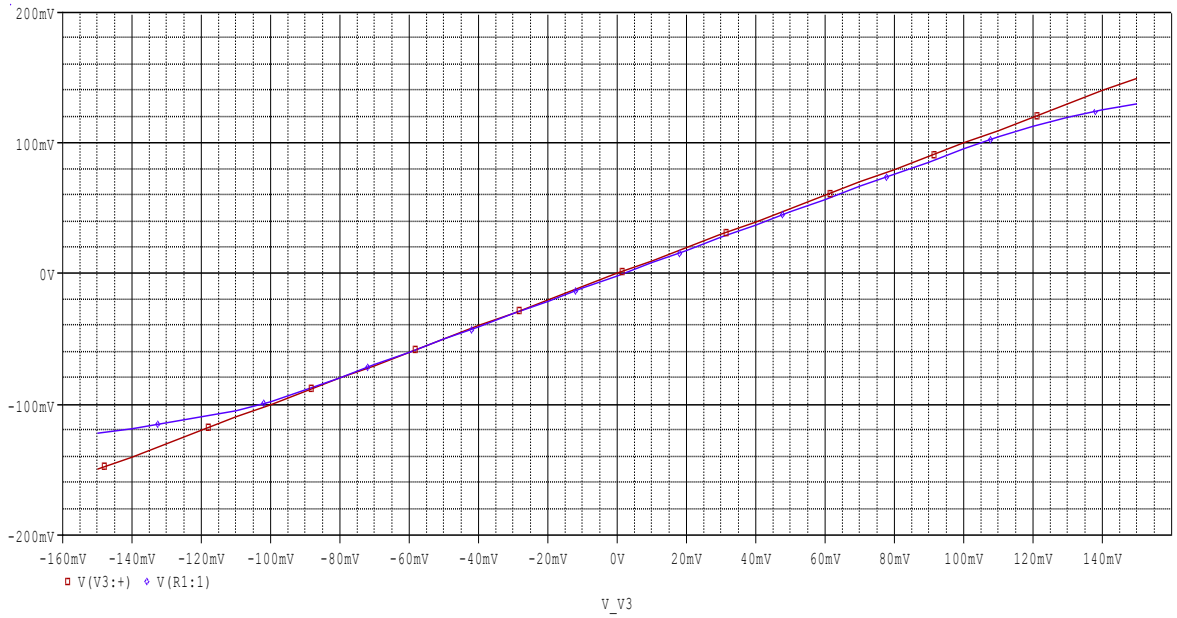


Figure 4.9 Voltage Transfer Curve of CDBA

4.3.5 Frequency response of voltage transfer ratio

On performing the frequency analysis of output stage of CDBA the frequency response is shown in figure 4.10

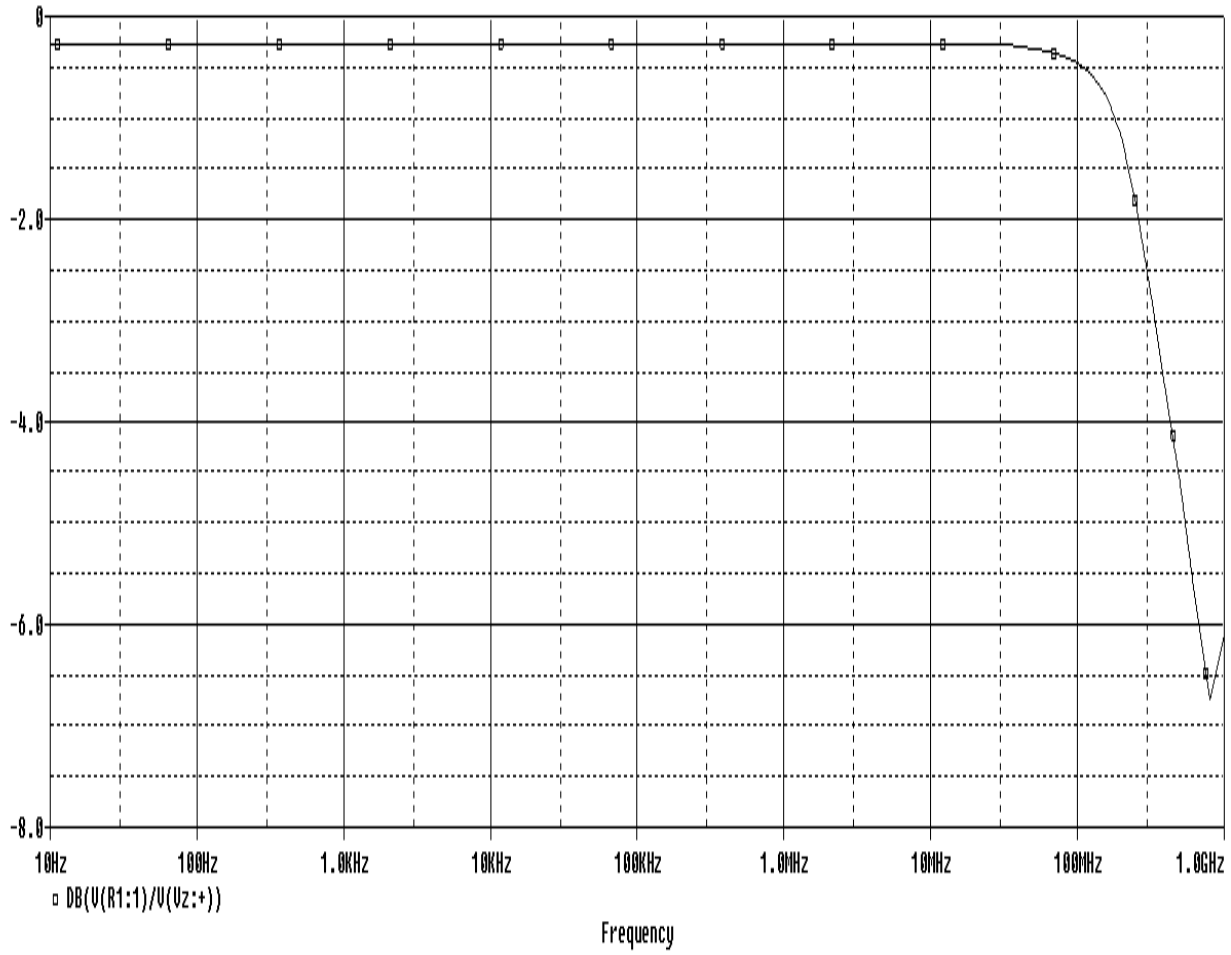


Figure 4.10 Frequency response of voltage transfer ratio of CDBA

CHAPTER 5

REALIZATION OF FILTER USING CDBA

Filters are one of most important and widely used in analog signal processing to select a particular frequency. I recent years because of advantage of current mode a large number of analog active blocks (ABB) [6] are used for designing of filter. In this chapter we used Flipped voltage follower based CDBA having very low input impedance and low power consumption for implementation of various filter. All simulations within this chapter are performed on PSPICE using 0.18µm model parameter.

5.1 Filter

It is some time desirable to have a circuit capable of selection one frequency or a range of frequency from a mixture of different frequency in a circuit. A circuit which is design to perform this frequency selection is called as Filter [26]. Thus a filter is nothing but just a frequency selecting circuit. Ideally a filter does not add any new frequency to a signal and also does not change any of its component but it change the relative amplitude of varies frequency component or there phase relationship. Filters are used in electronic system to emphasize the signals in a particular range and reject in other range. Consider a situation in which a useful signal at frequency f1 is effected with unwanted signal at f2, if the effected signal is passed a circuit having low gain at f2 compare to f1 then unwanted signal can be removed . The circuit which used for this purpose is basically a filter [26].

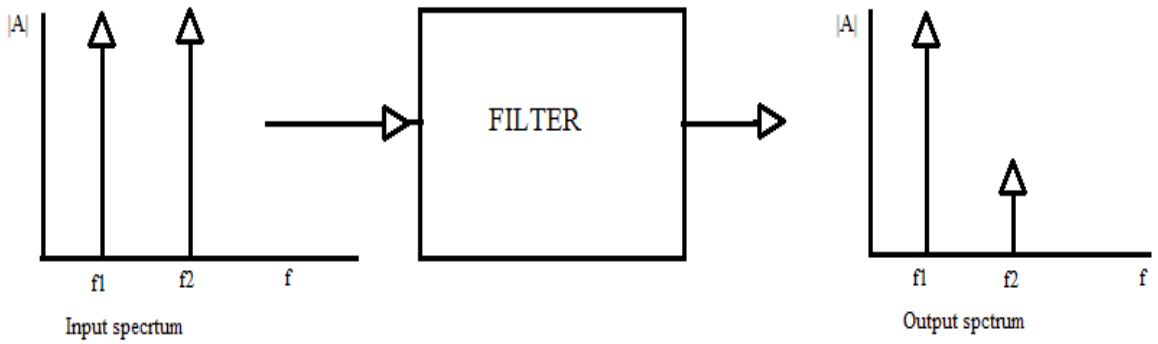


Figure 5.1 Effect of Filter to remove unwanted Signal [26]

On the basis of frequency range, filters are divided into five basic types.

5.1.1 Low Pass Filter (LPF)

A low pass filter [2] is a circuit which allows passing low frequency signal but rejecting the higher frequency signals. LPF are used where a high frequency component need to be removed completely from a signal. For example in a photo diode, it is mainly placed at the output of amplifier to reduce the overall level of noise. Figure 5.2 [26] show the possible amplitude response (ideal and practical) of a low pass filter. Under ideal condition it pass signal completely in pass band and attenuate the signal completely in stop band, the width of transition region is zero.

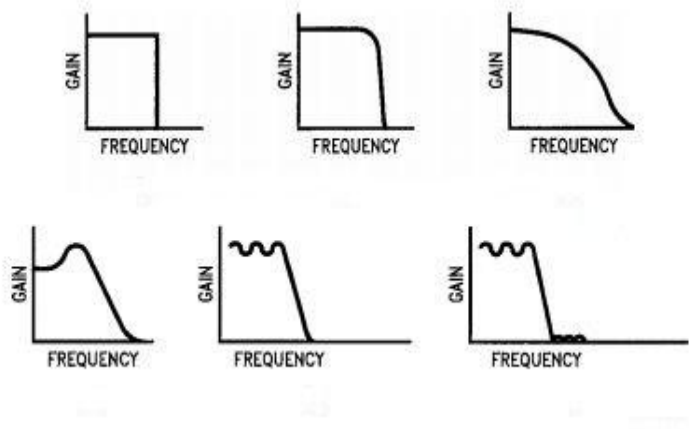


Figure 5.2 Amplitude response of LPF [26]

5.1.2 High Pass Filter (HPF)

The opposite of low pass filter (LPF) is high pass filter (HPF) [3], which reject the signal below its cutoff frequency and allow passing signal above its cut off frequency. The amplitude response (ideal and practical) of HPF is shown in figure 5.3 [26], which is just the mirror image of low pass filter.

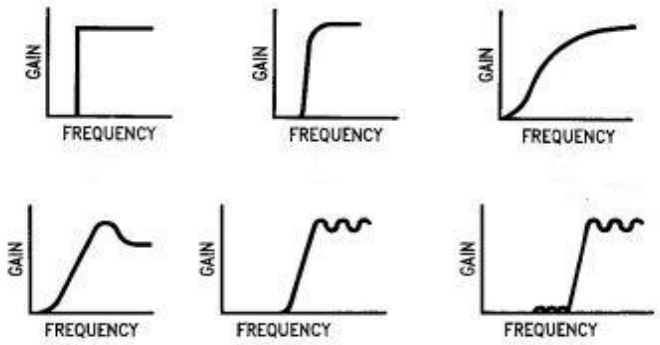


Figure 5.3 Amplitude responses of HPF [26]

High pass filter is used in the application where lower frequency signal needed to be rejected like in a loudspeaker. Under ideal condition HPF reject the signal completely below its cut of frequency and that band call as stop band while passes complete signal in pass band.

5.1.3 Band Pass Filter (BPF)

A band pass filter [2] is a circuit which allow to pass signal in a particular set of frequency band and reject the signal completely below and above that frequency band.it has three band such as STOP BAND- PASS BAND-STOP BAND. A band pass filter is a combination of LPF and HPF as shown in figure 5.4.

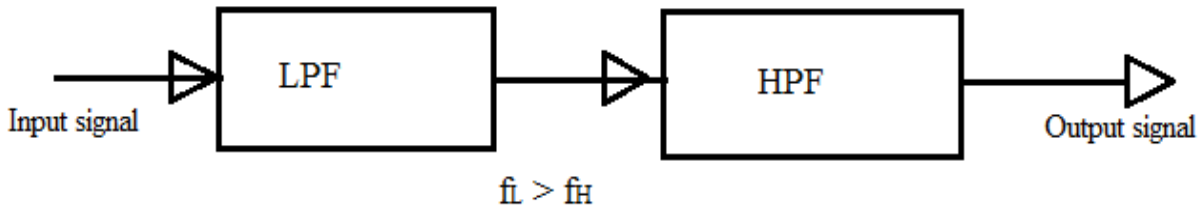


Figure 5.4 Block diagram BPF [2]

The input signal is applied to LPF which pass the signal below f_L, and then the output of LPF is applied to HPF, which passes the signal above cut of frequency f_H. To get output signal response the following condition should satisfied

$$f_L > f_H$$

BPF is used in electronic system where we need to separate signal at a particular frequency or band of frequency from signal of other frequency. Amplitude response of a BPF (ideal and practical) is shown in figure 5.5 [26]

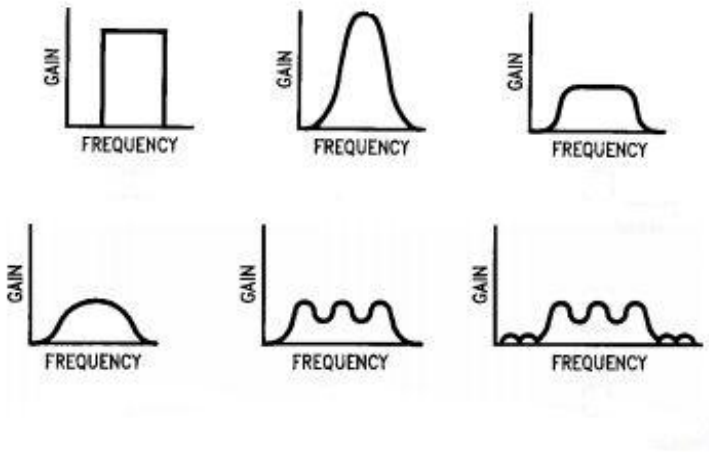


Figure 5.5 Amplitude response of BPF [26]

Under ideal condition the width of transition region is zero, and signal get attenuated on both the side of pass band.

5.1.4 Band Reject Filter or Notch Filter

It is just opposite to band pass filter (BPF) [3], it is a circuit which pass all the frequency signal only attenuate in a particular band. The amplitude response of band reject filter is mirror image of band pass filter (BPF) as shown in figure 5.6 [26].

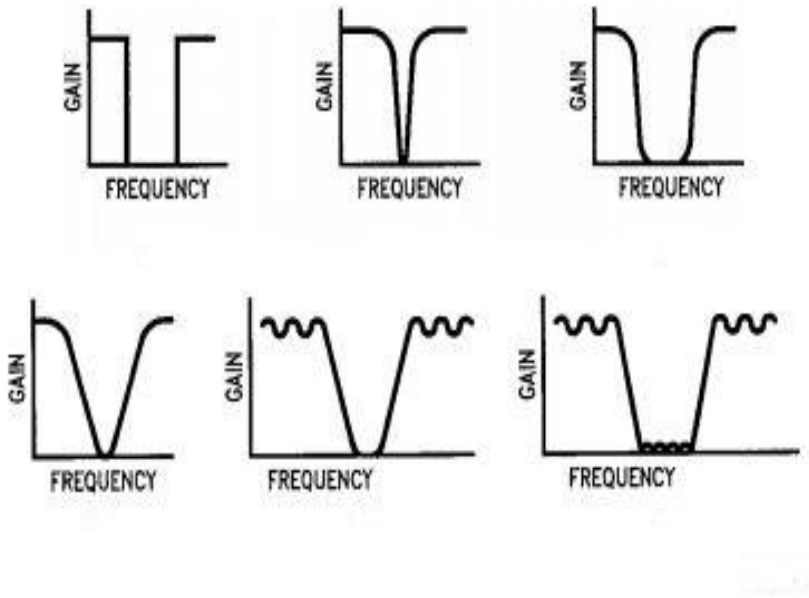


Figure 5.6 Amplitude responses of Band reject filter [23]

Band reject filter can be realized using LPF and HPF as shown in figure 5.7 in parallel to each other. Input signal is applied to both LPF and HPF. LPF passes the signal up to cut off frequency that is f_L. While high pass filter (HPF) passes signal after cut off frequency f_H. Satisfying the condition:-

$$f_L < f_H$$

The output signal is a band rejected signal, in which the signal is completely attenuated between f_L to f_H.

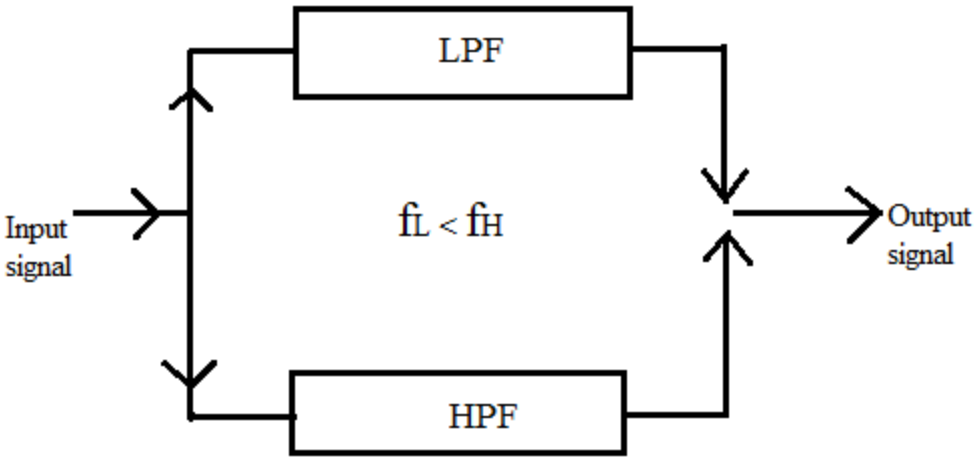


Figure 5.7 Block diagram of band reject filter [3]

The amplitude frequency response of ideal band reject filter consists of PASS BAND-STOP BAND-PASS BAND. The width of transition region under ideal condition is zero.

5.1.5 All Pass Filter (APF)

An APF[3] is a filter which can pass all the frequency signal without effecting the amplitude but there is a change in its phase, that why it is also called as phase shifter. The main application of this type filter is to change the phase of signal in order to cancel any previous imposed unwanted phase shift. The amplitude frequency response of an ideal all pass filter is shown in figure 5.8.

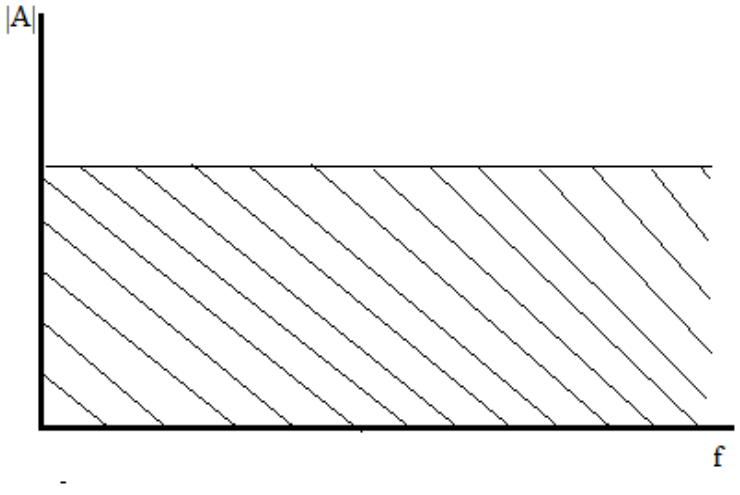


Figure 5. 8 Amplitude response of APF [2]

5.2 Realization of All pass filter and notch filter using CDBA

The block diagram of second order filter is shown in figure 5.9[17]. The general voltage transfer function is given by

$$\frac{V_0}{V_i} = \frac{s^2 + s\left(\frac{1}{R_2C_2} - \frac{1}{R_1C_1}\right) + \frac{1}{c_1C_2R_2R_3}}{s^2 + s\left(\frac{1}{R_2C_2} + \frac{1}{C_1R_3}\right) + \frac{1}{C_1C_2R_2R_3}} \tag{5.1}$$

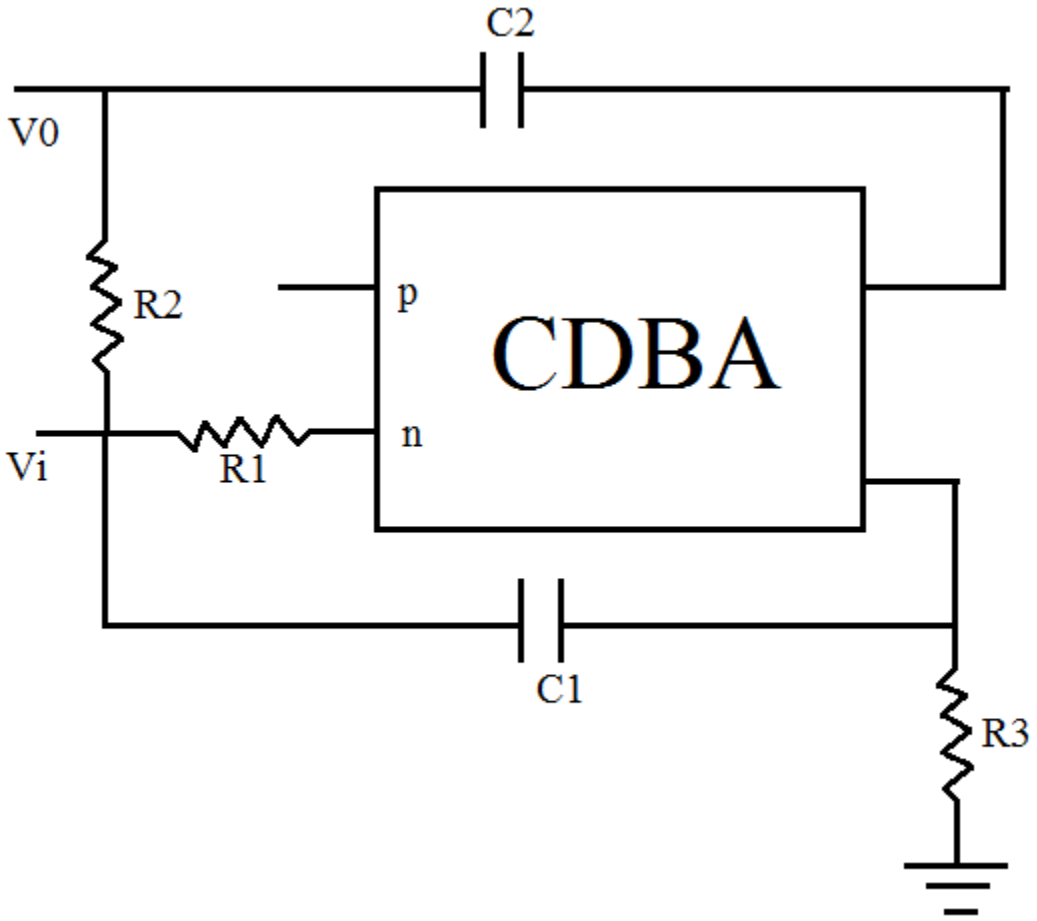


Figure 5.9 Block diagram of Second order APF/Notch filter using CDBA [19]

Here we have used three resistors and two capacitors. All simulation is done on PSPICE Orcad using 0.18µm CMOS technology. On choosing component value as R_1=2kΩ, R_2=6kΩ, R_3=6kΩ,

C_1=C_2=25pf a second order all pass filter response is obtain having center frequency about 1.08MHz

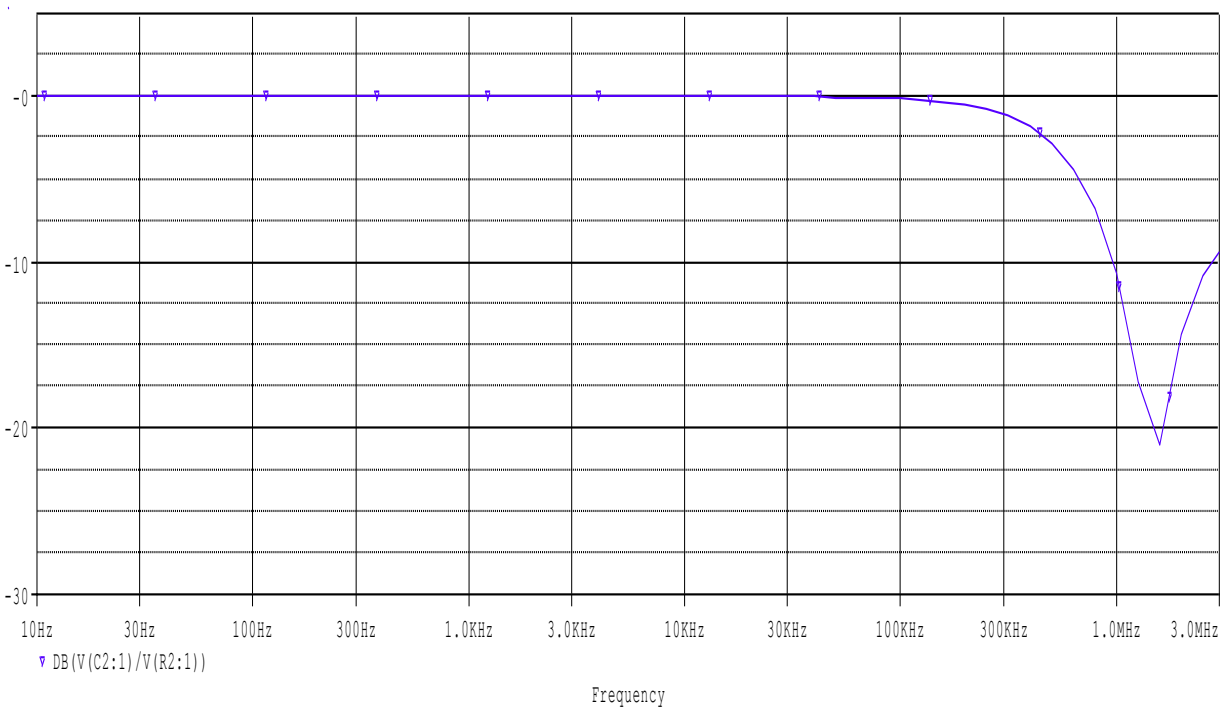


Figure 5.10 All pass filter using CDBA

If matching condition is obtain R_1C_1=R_2C_2, then the transfer function of equation 5.1 will be

$$\frac{V_o}{V_i} = \frac{S^2 + \frac{1}{C_1C_2R_2R_3}}{S^2 + s\left(\frac{1}{R_2C_2} + \frac{1}{C_1R_3}\right) + \frac{1}{C_1C_2R_2R_3}} \tag{5.2}$$

If component value is chosen as R_1=10kΩ, R_2=10kΩ, R_3=2kΩ, C_1=C_2=20pf a second order notch filter response is obtain as shown in figure 5.11

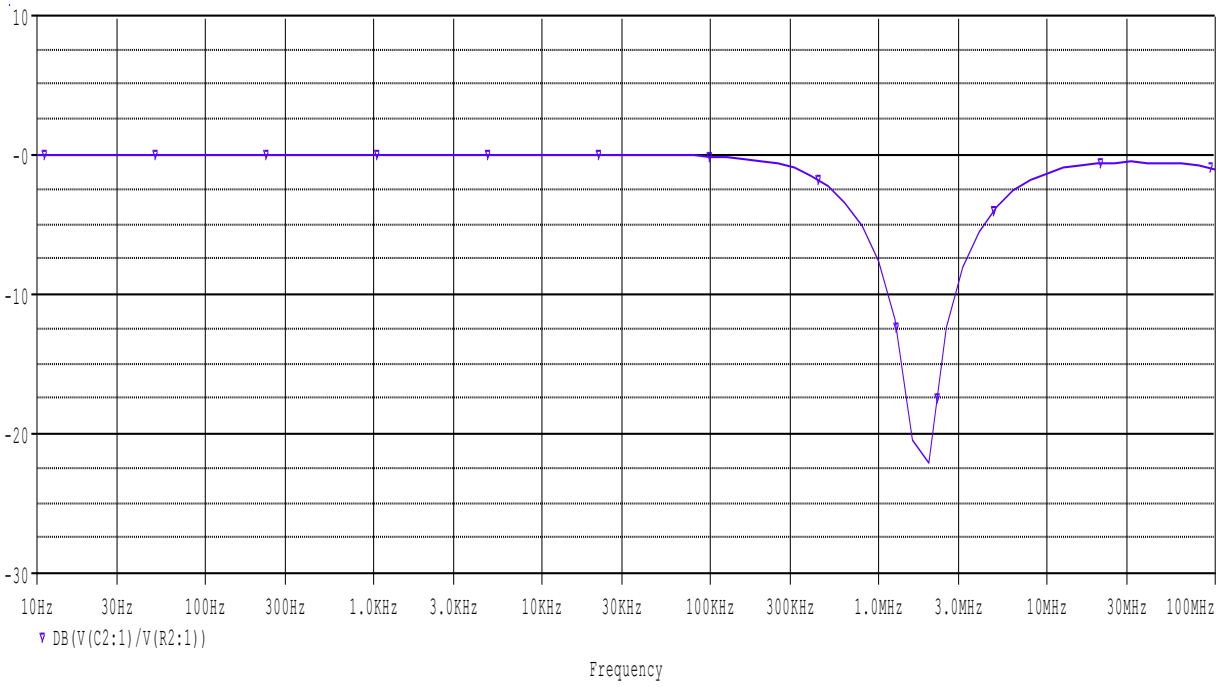


Figure 5.11 Notch filter using CDBA

CHAPTER 6

REALIZATION OF FULL WAVE RECTIFIER USING CDBA

Full wave rectifier [27] is one of the most important nonlinear analog circuit which is widely used in telecommunication, measurement and instrumentation area. It is also used in DC convertors, wattmeter, AC voltmeter, demodulator, linear function generator and various types of nonlinear signal processing circuits. Because of threshold voltage of diode and low frequency range of op amp the classical diode rectifier have very narrow usage area. The concept of current mode circuit having various advantages like better linearity, high dynamic range, low power consumption, low temperature sensitivity and simple structure open a way for development of rectifier using various available analog active blocks (ABB). In this chapter we will implement a inverting and non-inverting full wave rectifier using an analog building block called as CDBA. The CDBA block which we are using here is based on flipped voltage follower. All simulation are performed on PSPICE using 0.18µm CMOS model parameter.

6.1 Classical diode Rectifier

A rectifier is an electrical device that converts alternating current (AC) to direct current which flow in only one direction. This process called as rectification. Rectifier has many uses in electrical as well as electronic field. Because of the alternating nature of input AC sine wave, the process of rectification alone produce DC current that through unidirectional consist of pulses of current. Many application of rectifier such as power supplies for radio, television and computer equipment require steady constant DC current.

Before the development of silicon semiconductor rectifiers, vacuum tube and copper oxide- or selenium-based metal rectifier stacks were used with the introduction of semiconductor electronics; vacuum tube rectifiers became obsolete, except for some enthusiasts of vacuum tube. For power rectification from very low to very high current, semiconductor diodes of various types junction diode are widely used.

Other devices that have control electrodes as well as acting as unidirectional current valves are used where more than simple rectification is required where variable output voltage is needed. High-power rectifiers, such as those used in high voltage direct current power transmission, employ silicon semiconductor devices of various types. These are thyristor or other controlled switching solid-state switches, which effectively function as diodes to pass current in only one direction.

(a) Half wave rectifier

(b) Full wave rectifier

6.2 Full wave rectifier using CDBA

In this section we will simulate full wave rectifier using two diodes and one CDBA [28]. The inverting and non-inverting full wave rectifier are shown in figure 5.1 (a) and 5.1 (b)

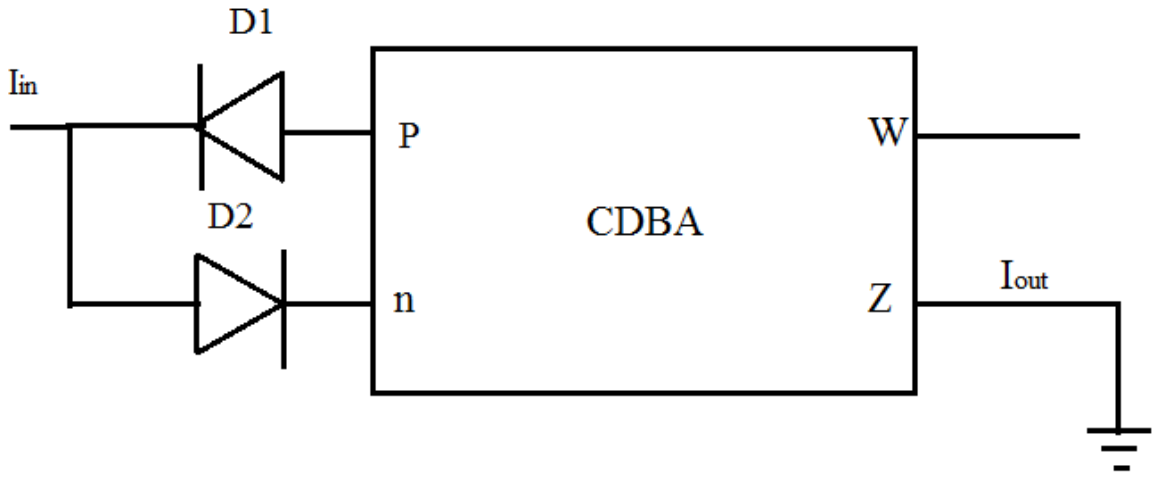


Figure 5.1 (a) Inverting full wave rectifier using CDBA [28]

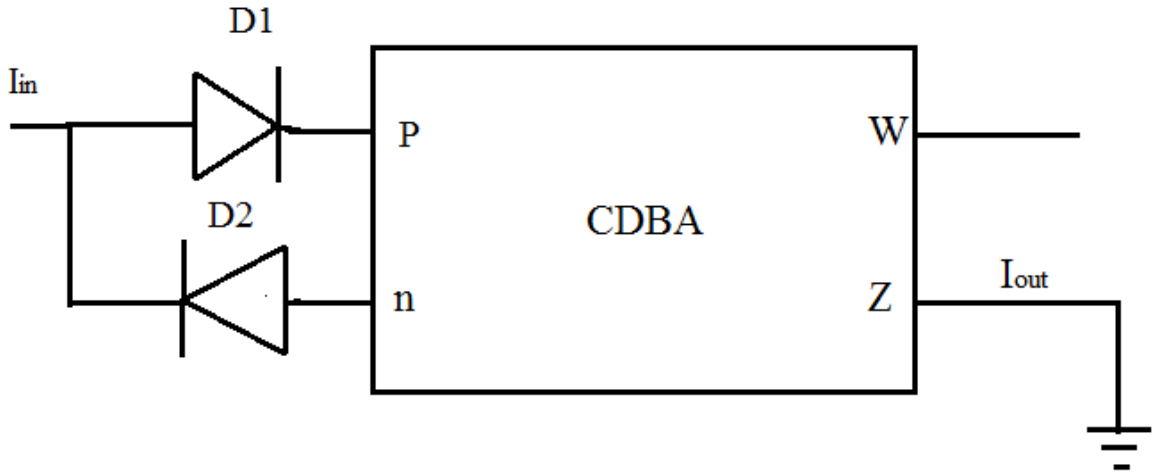


Figure 5.1 (b) Non inverting full wave rectifier using CDBA [28]

In figure 5.1 (a) when current is applied then for positive input current diode D1 is in off state and diode D2 is in on state the result of current Ip is zero thus

$$I_{out} = -I_n = -I_{in} \quad (1)$$

For negative input current, diode D1 is on and diode D2 is in off state, thus the current at In port will be zero

$$I_{out} = I_p = I_{in} \tag{2}$$

Thus ,

$$I_{out} = I_z = -|I_{in}| \tag{3}$$

Thus corresponding to equation 4 inverting type full wave rectifier is obtained. For non-inverting type rectifier the direction of diode is change as shown in figure 5.1(b)

$$I_{out} = I_z = |I_{in}| \tag{4}$$

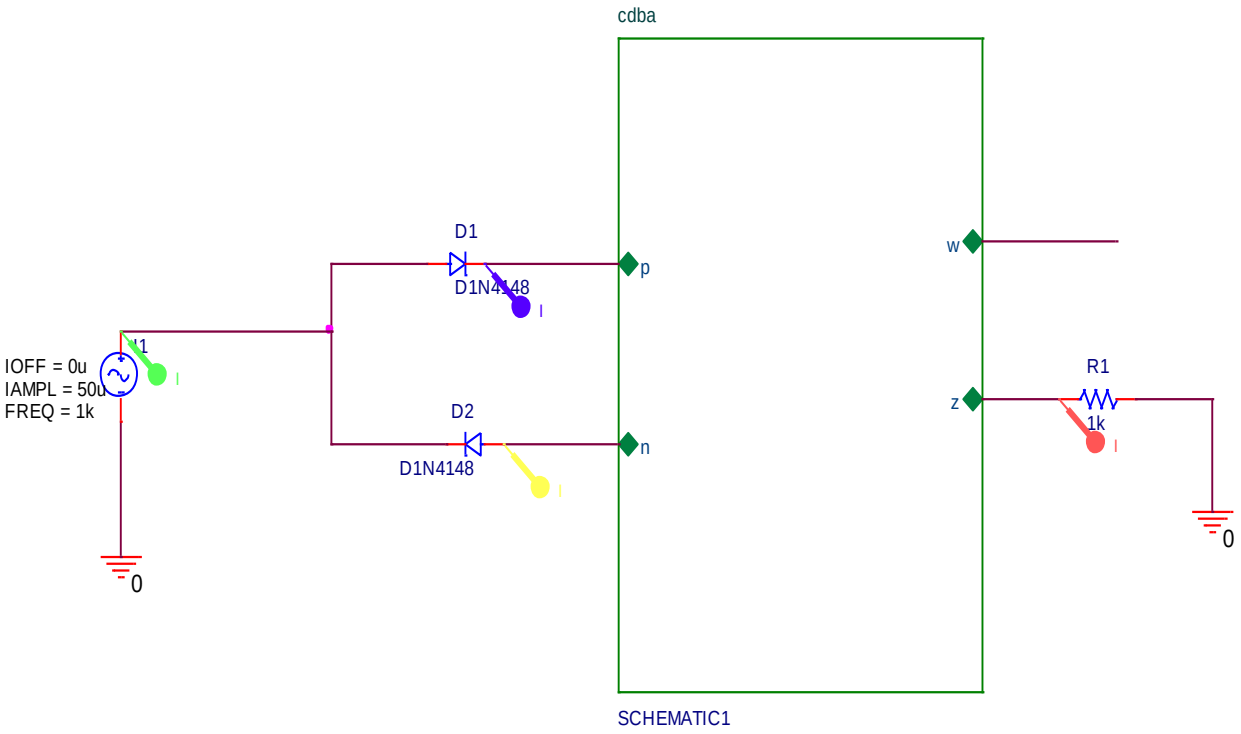
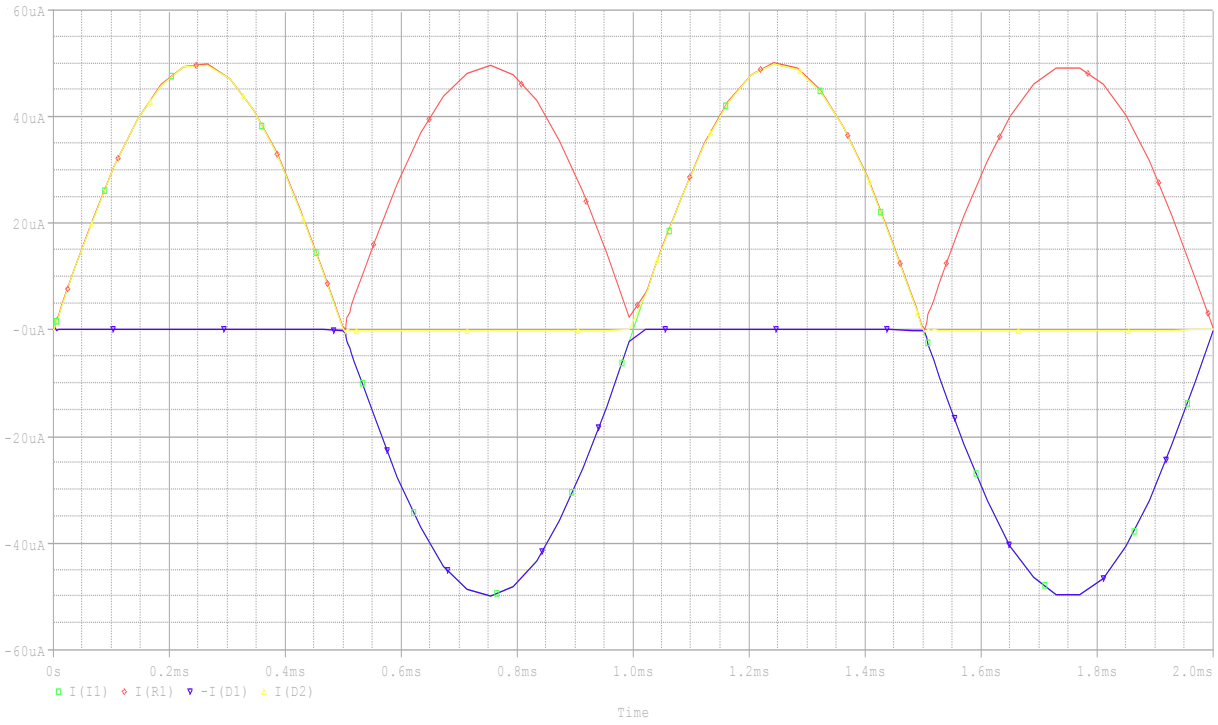
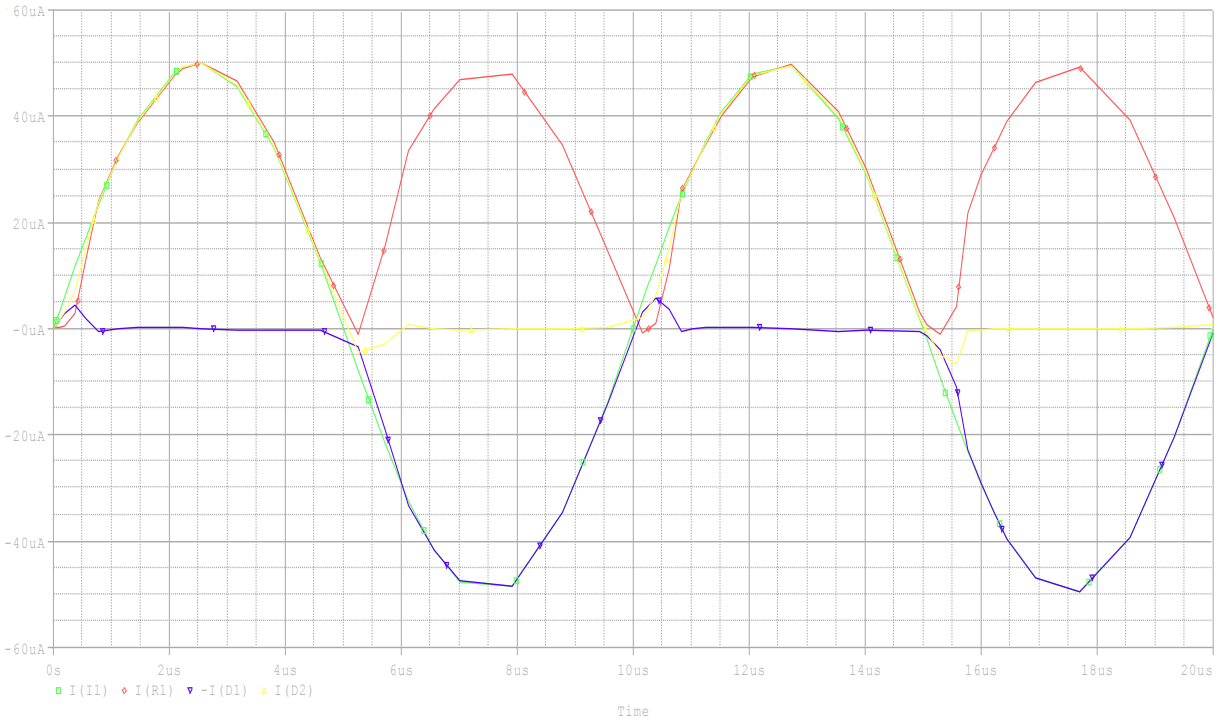


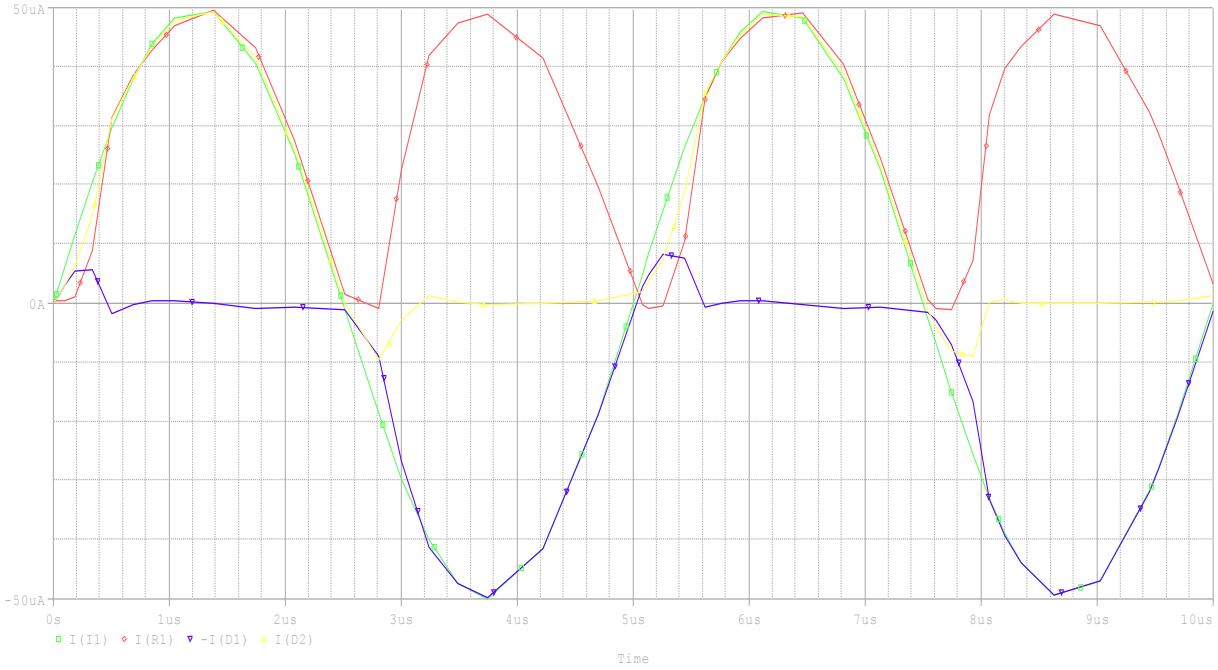
Figure 5.2 Schematic of full wave rectifier using CDBA


60uA
40uA
20uA
-0uA
-20uA
-40uA
-60uA
0s
0.2ms
0.4ms
0.6ms
0.8ms
1.0ms
1.2ms
1.4ms
1.6ms
1.8ms
2.0ms
I(I1)
I(R1)
-I(D1)
I(D2)
Time

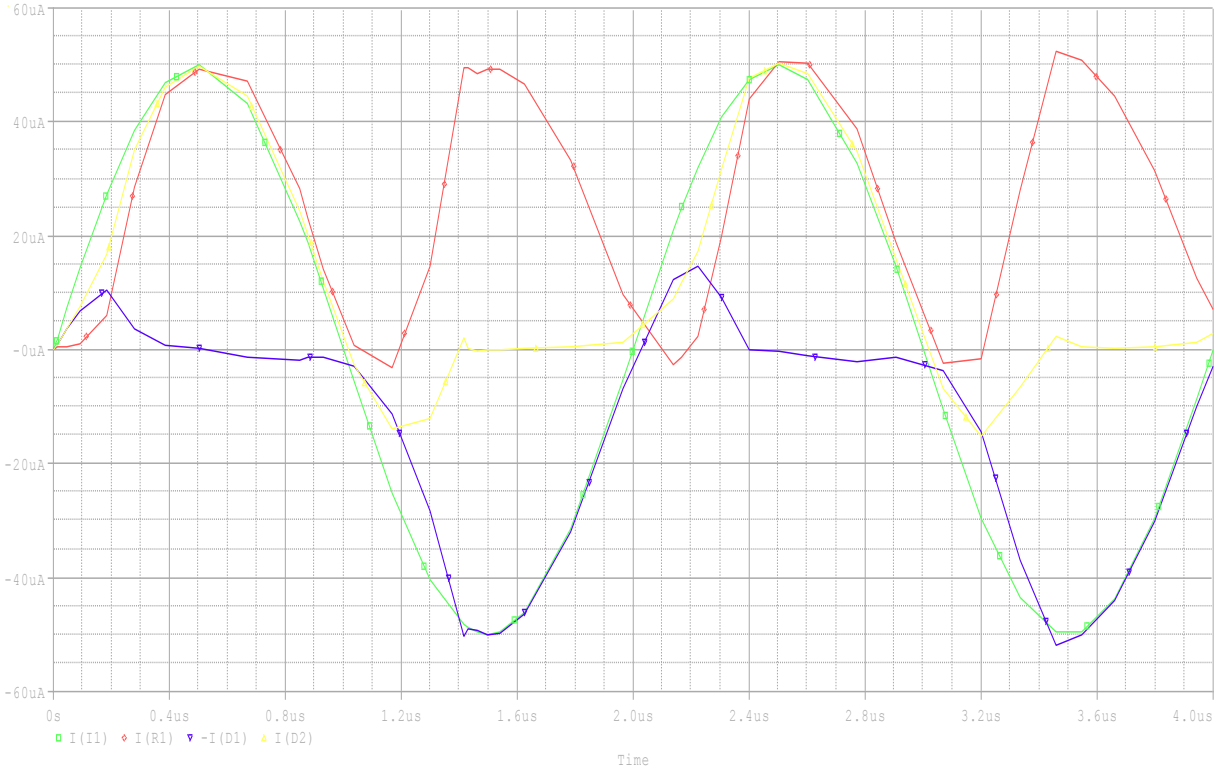
(a)


60uA
40uA
20uA
-0uA
-20uA
-40uA
-60uA
0s
2us
4us
6us
8us
10us
12us
14us
16us
18us
20us
I(I1)
I(R1)
-I(D1)
I(D2)
Time

(b)



(c)



(d)

Figure 5.3 Time domain response of full wave rectifier using CDBA for sinusoidal input with varying frequency (a) 1 KHz (b) 100 KHz (c) 200 KHz (d) 1 MHz

Figure 5.2 shows the schematic of CM full wave rectifier using CDBA and figure 5.3 shows the response for applied sinusoidal input signal at various frequencies. It is observed from analysis that as frequencies is increases the non-linearity also increases. The output waveform is as per theoretical one only at low frequency, but at higher frequency there is deviation in result. This deviation can be improved up to certain extent if we use better diode (1PS79SB17 or BAS516) whose performance is better at higher frequencies but the cost will be increases.

CHAPTER 7

CONCLUSION

In last two decade, for analog signal processing a large number of Analog building blocks (ABB) [9] have been introduce due to various limitation of conventional voltage mode op-amp. The various benefits such as low power dissipation, high bandwidth, and low supply voltage of current mode concept are used by these active blocks via which we can implement various analog circuits.

In this thesis firstly we study basic of current mode concept, its advantage in analog circuits then using concept of flipped voltage follower we implemented a very important active analog block call as CDBA and study various of its characteristic and then using this block we implemented a linear analog circuit filter, which is used widely in electronic and electrical industry and also as an important building block of various circuit in telecommunication. We also implemented a nonlinear circuit, full wave rectifier which is also very important part of analog circuits.

Thus with the demand of miniaturization of area and low power dissipation without compromises with quality, these active analog block are replacing conventional op-amp in various application.

REFERENCES

1. C. Toumazou J.lidgey B.Wilson " current mode signal processing circuits" IEEE circuit device and system Vol 137 No 2 1990"
2. R. Schaumann and M. E. V. Valkenburg, Design of Analog Filters, 2nd ed. New York, USA: Oxford University Press, 2004.
3. R. Raut and M. N. S. Swamy, Modern Analog Filter Analysis and Design: A Practical Approach, 1st ed. Weinheim, Germany: Wiley-VCH, 2010.
4. J. Mahattanakul and C. Toumazou, "Current-mode versus voltage-mode-biquad filters," IEEE Transaction on Circuits and Systems—II: Analog and Digital Signal Processing, vol. 45, No.2, pp. 173-186, 1998.
5. B. Razavi, Design of analog CMOS integrated circuit new york McGraw Hill 2001
6. R.S. Zebulum D. Keymeulen, T. Daud " Current mode circuits: Increasing the chance of evolution to find a way " IEEE 2002
7. Hanspeter schmid "Why the term current mode neither divide nor qualify circuit" 3018 bern, Switzerland IEEE 2002.
8. S. yan, E.S. Sinencio "Low voltage analog circuit design techniques: A tutorial" IEICE Trans Analog integrated circuit and system, Vol Eoo A No 2 february 2000.
9. D.Biolek, R. Senani, V.Biolkova, Z.kolka "Active element for analog signal processing: Classification, review, and new proposal" Radio engineering Vol 17 No 4, 2008.
10. Acar C. and Ozoguz S. 1999 A new versatile building block : Current difference buffered amplifier suitable for analog signal processing filter" Microelectronic journal 30 pp 157-160.
11. Acar C. and Sedef H. 2003 " Realization of nth- order current transfer function using CDBA" Int J. Electronic Vol 90 No 4 pp 277-283.
12. Ozoguz S. Toker A and Acar C. 1999 " Current mode continuous time fully integrated universal filter using CDBA" Electronic letter Vol 35 No 2 pp 97-98.
13. Tarim N. and kuntman H. 2001 " A high performance CDBA" 13th international conference on Microelectronic pp 153-156
14. Tangsrirat W.,Klahan K. Dumawipata T. and Surakampontorn W. 2006 " Low voltage NMOS based current difference buffered Amplifier and its application to current mode ladder filter design" International journal of Electronic Vol 93 No 11 pp 777-791.
15. Dumawipata T. Tangsrirat W. and surakampontorn W. 2007 " Low voltage CDBA using only NMOS transistor" International Symposium on integrated circuit pp 123-126.
16. Sawangaroml V. Tangsrirat W. and Surakampontorn W. 2006 " NPN based current difference buffered amplifier and its application" SICE-ICASE International joint conference.
17. Cakir C. and Cicekoglu O. 2008 " Low voltage high performance current difference buffered amplifier" Istanbul pp37-40.
18. Cakir C. Minaei S. and Cickoglu O. 2009 " Low voltage low power high swing current difference buffered amplifier" Circuit and system and TAISA conference pp1-4.

19. Cakir C. Minaei S. and cickoglu O. 2010 " Low voltage low power CMOS current difference buffered amplifier" Analog integrated circuit and signal process springer Vol 62 No 2 pp237-244.
20. Kanjanop A. and Kasemsuwan V. 2011 " A low voltage class AB current difference buffered amplifier (CDBA)" International Symposium on Intelligent signal processing and communication system pp1-5.
21. Maheshwari S. and khan I.A. 2004 " Current contro current difference buffered amplifier : Implementation and application" Active and passive electronic components No 4 pp 219-227.
22. " Special issue on low voltage low power analog design" IEEE Trans circuit and systems I, fundam theory appl Vol 42 No 11 1995.
23. R. G. Carvajal, J.R. Angulo, A.J. Lopez-Martin, A. Torralba, J.A. Gomez Galan, A. Carlosena and F. Munoz Chavero " The Flipped voltage follower : A usefull Cell for low voltage low power circuit design" IEEE transactions on Circuit and Systems-I Vol 52 No 7 july 2005.
24. Uygur A. and Kuntman H. (2006) " Low voltage current difference buffered amplifier in a novel all pass configuration" In MELECON 06 proceeding of 13th IEEE Mediterranean electro technical conference spain pp 23-26.
25. Torralba A. Carvajal R.G. Galan J. and Ramfrez angulo J. (2002) " Compact low power high slew rate CMOS buffered for large capacitive load" electronic letter, 38(22) 1348-1349.
26. Application note 779 A basic introduction to filter Texas Instrumnt.
27. Montree Kumngern " Precission Full wave rectifier using two DDCC" Circuits and Systems, 2011, 2, 127-132
28. Suleyman Erkan, Umut Engin Ayten, and Mehmet Sagbaş "Current-Mode Full-Wave Rectifier Circuits Using Current Differencing Buffered Amplifie" IEEE2015.