“MODEL PARAMETER EXTRACTION OF AlGaN/GaN HEMT AT MICROWAVE FREQUENCY”

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IN

Microwave and optical Communication Engineering

BY

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CERTIFICATE

It is certified that project report entitled "**MODEL PARAMETER EXTRACTION OF AlGaN/GaN HEMT AT MICROWAVE FREQUENCY**" submitted by **Mr. Pragyey Kumar Kaushik** for partial fulfilment of the requirements of the degree "**Master in Technology in Microwave & optical communication engineering**" is bona fide dissertation work carried out under the supervision of the undersigned scientist at solid state physics laboratory New Delhi and to the best of our knowledge this work has not been submitted anywhere else for any other degree or diploma. He is sincere, intelligent and hardworking. I wish all the best for his bright future.

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I hereby declare that this submission is my own work and that, to the best of my knowledge and belief, it contains no material previously published or written by another person nor material which to a substantial extent has been accepted for the award of any other degree or diploma of the university or other institute of higher learning, except where due acknowledgment has been made in the text.

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PREFACE

It is the requirement of the M.Tech (Microwave & optical communication Electronics) degree that a student has to undergo project training at the forth semester of two year course. In this time period he has to acquire the work experience in any organization in public sector, private sector or government departments. Along with working exposure the student has to develop an application or module of it.

I underwent my project training in **campus** of **Solid State Physics Laboratory, New Delhi India (SSPL)** situated at **Timarpur, Lucknow Road, New Delhi.** During project training I have worked on the AlGaN/GaN HEMT with the project named **"MODEL PARAMETER EXTRACTION OF AlGaN/GaN HEMT AT MICROWAVE FREQUENCY"** at MMIC lab in SSPL. This project is developed for the scientific purpose. This report briefly describes the systematic approach taken to develop this project. The project development report contains information about organization, hardware, software, its implementation and testing.

ACKNOWLEDGEMENT

This six months project work carried out at **Solid state physics laboratory, New Delhi** has been an enlightening experience in pursuit of my academic excellence. The successful completion of this project work starting with initial search and collection relevant reference materials, calculation, theoretical analysis and finally simulation of result and comparison it with measured data and Microwave Standards section speaks about the professional acumen and excellence of scientists and all staff members of SSPL. I am sincerely thankful to **Dr R. K. Sharma, Director, SSPL, New Delhi** for giving me an opportunity to work at this esteemed organization. I am profoundly grateful to **Dr Meena Mishra** and **Dr. Seema Vinayak** for her guidance in understanding of the project work, coordination in the development process, finally carrying out measurements and analysis of the measured parameters. They took keen interest in my training, beckoning me to learn more and more, and get wonderful and enriching experience in the Microwave world. My special thanks to **Mr Umakant Goyal** and to all members of the MMIC, Fabrication and measurment Department for extending their support and making the experience enriching & informative.

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This dissertation would not become reality without my family support; my **Maa** and **Brother** encourage me time to time. Finally I would like to thank **Ms. Manali Saxena** for her moral support and suggestion to improve my work.

I wish to convey my sincere gratitude to Department of Electronics & Communication and Applied Physics department of Delhi Technological University for their immense contribution for my academic development.

ORGANIZATIONAL PROFILE

Solid State Physics Laboratory (SSPL) is one of the pioneer establishments in the electronic cluster of laboratories under the Defence R&D Organization (DRDO), Ministry of Defence, Government of India. The history of SSPL started in 1960 with a nucleus of scientists and with the broad objective of development of an R & D base in the field of solid-state materials, devices and subsystems. It was the first such institute in the country that started work in this vital area. From a small beginning, the laboratory has grown into a premier research and development establishment in the field of solid state materials and devices, and is well known both within the country and abroad. The nature of activities in SSPL is interdisciplinary involving a fusion of solid state physicists, chemists, system designers, engineers (electronics, computer, mechanical) and material technologists. The strength of the laboratory is the pool of well qualified scientists and engineers from various disciplines. It is the workplace of around 500 people, 170 of them being scientists. Over the past 46 years, their has been an explosion in the development of almost all the aspects of the laboratory. The laboratory made a humble beginning with discrete devices based on silicon. Over the years it has reached greater heights and the work has reached its present day level based on compound semiconductors and advanced materials. During its long history, SSPL has worked successfully in many areas including growth of Si crystals, bipolar and MOS based ICs, Charge Coupled Devices, Variable Time fuses, silicon solar cells to name just a few. On the materials front SSPL works on electroceramics, ferrites, CZT, MCT, GaAs, Ge, Bi2Te3, CNTs. SSPL has the sophisticated test and characterization facilities to analyse these materials and the devices made from them. To keep pace with the international development in the area of solid state materials and devices SSPL has initiated activities in the emerging technologies like nanotechnology and polymer electronics. The laboratory has also constantly updated itself with new facilities like the state-of-the art Mask Fabrication facility and the Digital Library for storing and retrieving of digital information as well as the various sophisticated equipments required for R&D. There are many divers area and facility available at SSPL listed below.

(1) ELECTRON PROBE MICRO ANALYSER (EPMA)

This probe is use to determine

Elemental segregation at grain boundaries, Compositional uniformity in S.C. alloys, Elemental imaging of S.C. surfaces.

(2) SECONDARY ION MASS SPECTROMETER (SIMS)

This is used for surface contamination studies, Depth profiling, Interface analysis of multilayer structures.

(3) SECONDARY ELECTRON MICROSCOPE (SEM)

This is used for surface morphology & Structural analysis, Critical dimension measurements, Elemental analysis of precipitates, Failure analysis of fractured surfaces.

(4) FOURIER TRANSFORM INFRARED SPECTROMETER (FTIR)

It is used for determining thickness estimation of epitaxial layers, Purity of chemicals, Compositional determination in variable band gap semiconductors.

(5) DEEP LEVEL TRANSIENT SPECTROSCOPE (DLTS)

It is used for optical characterization of minority carrier traps in semiconductors, Determination of interface states in Schottky contacts.

(6) MOLECULAR BEAM EPITAXY (MBE)

The deposition of sub-micron thick N and P doped and un-doped layers of epitaxial silicon with sharp transition at the junction can be obtained at low temperature of operation and at low growth rate under UHV conditions using MBE. electron beam mask fabrication (EBMF).

(7) ELECTRON BEAM MASK FABRICATION (EBMF)

The system is used for -Writing sub-micron and sub-100-nanometer patterns directly on a selected substrate. To write Mushroom Gate / T-Gate with foot length of 0.25μm or better on GaAs / any other semiconductor substrate.

(8) LIQUID PHASE EPITAXY (LPE) GROWTH REACTOR

Liquid Phase Epitaxy (LPE) Epitaxy is a phase transition process which leads to formation of single crystal solids. In LPE non equilibrium is intentionally created, by supersaturating of the melt, to drive the system towards formation of single crystal solid.

(9) ION IMPLANTER

The equipment is capable of implanting ions of any element in the periodic table. Silicon is implanted for n-type layers, often with heavily doped (n+) layer for contact at the surface using this system.

(10) MASK FABRICATION FACILITY

The facility is capable of fabricating photo mask up to minimum feature size of 1μm. The facility is self-contained with class-100, 1000 and 10,000 clean rooms.

(11) CLEANROOM FACILITY

A clean room facility was setup and commissioned in June 2004. This facility consists of a Class 100 process area, Class 10 K utility area and Class 1 K gowning and storage area. The variety of equipment required for the requisite work, including LPG writing System, dry and wet process equipments and mask design centre have been installed and are being used routinely. Up till now 418 good quality photo masks have been fabricated, which include 208 user masks (SSPL and outside) and 210 test masks.

MONOLITHIC MICROWAVE INTEGRATED CIRCUITS GROUP

MMIC circuit

Monolithic microwave integrated circuits (MMICs) are widely used in a variety of defence, space and commercial applications. Solid State Physics Laboratory has already developed MMIC technologies upto 18 GHz for applications such as medium power amplification and switching. This technology is based on MESFET (Metal semiconductor field effect transistor) as the active device for the design of MMICs. GaAs MESFET devices for C-Band power applications have also been developed. These technologies have been transferred to GAETEC, Hyderabad and are in regular production. Several of these MMICs have been supplied in chip form or custom

specific modules to DRDO labs (RCI, DLRL, DEAL, LRDE) and also sold to BEL, ISRO, SAC. The commercial value of these MMICs for the period 2002 and 2003 is more than 5 crores.

Presently SSPL is developing 40 GHz -MMIC technology along with high power devices to be used by system laboratories of DRDO working in EW and radar communications. As there is requirement of Low noise circuit as well as high power amplifier in current scenario, hence SSPL is committed to deliver the best Low noise Circuit operating in the wide range of operating frequency of L-band to Ka –band. For achieving such high performance circuits 0.5um and 0.25um p-HEMT (P-High Electron Mobility Transistor) technology is being developed. Once these technologies are developed they will be transferred to GAETEC, Hyderabad for regular production. These all module level components are Space qualified and are being deployed in satellite communication. Around 64 MMIC module level commencements (Designed and fabricated – in house) deployed in CARTOSAT-I, working in good condition is one of the many success story of SSPL-MMIC Activity.

LIST OF FIGURE

1.1 Basic element of power amplifier and basic configuration of PA 3

2.1 Thickness growing one by one layer 5

2.2 Overview of high speed devices 6

2.3 Parasitic capacitor 8

2.4 ON resistance slope of current voltage curve 8

2.5 Relative energy band diagram & mobility of different material 11

2.6 MESFET diagram 12

2.7 Mobility Vs Doping concentrations 13

3.1 Formation of potential well and electron trapping in the well 15

3.2 Population of 2DEG for different bias of gate 16

3.3 Basic structure of HEMT & corresponding band diagram 16

3.4 Complete basic structure of HEMT with spacer layer 17

3.5 Unity current gain curves (a) Ft = 16.8 GHz at Vg = 0V, Vd = 10V (b) Ft = 21 GHz at Vg = -1V, Vd = 10V (c) Ft = 24.05 GHz at Vg = -2V, Vd = 10V (d) Ft = 26.55 GHz at Vg = -3V, Vd = 10V (e) Ft = 28.1 GHz at Vg = -4V, Vd = 10V (f) Ft = 27.95 GHz at Vg = -5V, Vd = 10V (g) Ft = 3.5 GHz at Vg = -6V, Vd = 10V 21

3.6: Variation of F_t with respect to V_g 22

3.7 Variation of F_{max} with respect to Vg 22

4.1 Illustration of the importance of microwave transistor modelling as helpful feedback for device fabrication and as a valuable tool for circuit design 24

4.2 Interdisciplinary knowledge required in microwave device modelling 25

4.3 Data measurement setup 27

4.4 Wafer testing probe and wafer probe station 28

4.5 DUT measurement setup process of De embedding 29

4.6 Open and short structure used for de embedding 30

4.7 Without de embedding and with de embedding 31

5.1 Small signal equivalent circuit for AlGaN/GaN HEMT 33

5.2 Physical meaning of parameter associated with AlGaN/GaN HEMT 34

5.3 Procedure to extract the intrinsic Y parameter from measured S parameter 37

5.4 Distributed RC network under the gate region 38

5.5 Flow of current across the gate pad 39

5.6 Simplified small signal circuit of HEMT for situation V_d = 0V and V_g < pinch off 41

5.7 Simulated Y-Parameter with respect to frequency of 0.8× 100 μm AlGaN/GaN HEMT device 42

5.8 Consistency of Cpd and Cpg value throughout the frequency range of 0.8× 100 μm AlGaN/GaN HEMT device 42

5.9 Extracted intrinsic parameter values form “a to g” for 0.8× 100 μm AlGaN/GaN HEMT device 45

5.10 Extracted Intrinsic parameter define and measured S-parameter called for Vd = 10V and Vg = -1.2V in ADS for 0.8× 100 μm AlGaN/GaN HEMT device 46

5.11 Measured (blue line) and simulated (red line) S- parameter for Vd =10V and Vg = -1.2V of 0.8× 100 μm AlGaN/GaN HEMT device 47

5.12 Extraction based magnitude and phase of measured (Blue Line) and simulated (Red line) data of 0.8× 100 μm AlGaN/GaN HEMT device for Vg = -1.2V and Vd = 10V 49

5.13: Measured (blue line) and simulated (red line) S- parameter for Vd =10V and Vg = -3V of 0.8× 100 µm AlGaN/GaN HEMT device 50

5.14: Extraction based magnitude and phase of measured (Blue Line) and simulated (Red line) data of 0.8× 100 µm AlGaN/GaN HEMT device for Vg = -3 V and Vd = 10V 53

6.1 IV characteristics of 0.8× 100 µm HEMT 55

6.2 Gate voltage Vs current of 0.8× 100 µm HEMT 56

6.3 Drain current (Ipk) and gate voltage (Vpk) 57

6.4 Effect of parameter on I_g Vs V_g curve 58

6.5 g_m and its derivatives 59

6.6 Effect of parameter α_s, α_r and λ on I_d Vs V_d graph 60

6.7 Output trans conductance g_d and its derivatives g_{d2} and g_{d3} 61

6.8: Extracted non linear parameters define in ADS for 0.8× 100 µm AlGaN/GaN HEMT device 63

6.9: Simulated (Blue line) and measured (Red line) Id Vs Vg curve 64

6.10: Simulated (Blue line) and measured (Red line) of (a) g_m (b) g_{m1} (c) g_{m2} 66

6.11: Simulated (Blue line) and measured (Red line) Id Vs Vd curve 67

6.12 Simulated (Blue line) and measured (Red line) of (a) g_d (b) g_{d1} (c) g_{d2} 69

6.13 Operated region of Id Vs Vg curve show the error of only 4.94044 % only 70

6.14 Operated region of I_d Vs V_d curve show the error of only 3.68914 % only 71

6.15 Input and output trans conductance accuracy (a) less than 9 % of error (b) less than 10 % of error 73

LIST OF TABLE

3.1 Comparison list of semiconductor material 17

3.2 Physical property of some promising substrate material for GaN HEMT 19

5.1: Extracted extrinsic parasitic resistance and inductance values of 0.8× 100 µm AlGaN/GaN HEMT device 43

5.2: Extracted extrinsic parasitic capacitance values of 0.8× 100 µm AlGaN/GaN HEMT device 43

5.3: Extracted intrinsic parameter values for different bias point of 0.8× 100 µm AlGaN/GaN HEMT device 44

6.1: Extracted non linear parameters values for .8× 100 µm AlGaN/GaN HEMT device 62

LIST OF ABBREVIATION

2-DEG	Two-Dimensional Electron Gas
3G	Third Generations
4G	Fourth Generations
5G	Fifth Generations
ADS	Advanced design Simulation
AlGaN	Aluminium Gallium Nitride
BJT	Bipolar junction transistor
DUT	Device under test
FET	Field effect transistor
GaAs	Gallium arsenide
GaN	Gallium Nitride
HBT	Heterojunction bipolar transistor
HEMT	High electron mobility transistor
IC-CAP	Integrated Circuit Characterization and Analysis Program
MOSFET	Metal oxide semiconductor field effect transistor
MESFET	Metal semiconductor field effect transistor
PA	Power Amplifier
SiC	Silicon carbide

ABSTARCT

Development of microwave power devices plays a crucial role in modern communicating world. From the point contact diode to the modern HBT's and HEMT's are the fascinating example of this marathon technological achievement. As said that "necessity is the mother of invention", in science community is was well known that as time will pass we will have to develop more precise and more fast technology to fulfil the need of corresponding world demand, Resulting the HBT's and HEMT's comes into existence. Although the journey of getting these super fast devices was not so easy and it take 4 to 5 decade to become the reality. Discussion of this dissertation is based on latest technology called HEMT device.

The main objective of this dissertation to take the suitable model for HEMT which suites the device performance up to 10 GHz. Then extract all parameter which belongs to the model and simulate these result and compare to the measured one. Small signal model and large signal model parameter extraction also carried out up to some limit and it is shown that good agreement between simulated result and measured data.

In chapter 1 deal with introduction of what is high speed devices where it can be used and what is the objective of this dissertation work.

Chapter 2 discussed the whole classical development of FET devices. Introducing the little bit idea of fabrication process of substrate of devices. Then the discussion about journey of high speed devices from the Si technology to the HEMT technology is carried out. What are those parameters which affect the device speed is also discussed in this chapter.

Chapter 3 deals with AlGaN/GaN HEMT exclusively. This chapter deals with the formation of hetero – junction with two different band gap materials which finally lead to the development of HEMT. Then the comparison between different semiconductor materials, are use in making of FET's. Substrate plays important role in FET's so this chapter also discuss the material which is most suitable to the AlGaN/GaN HEMT and why. What are the advantages to take the GaN as a material is also cover at the end of the chapter 3.

Chapter 4 cover the basic idea of modelling and data measurement. This chapter it is also mention what are those challenges which encountered at the time of modelling. S-Parameter measurement and De-embedding of measured data also give us some useful steps which are necessary for the modelling of HEMT devices.

Chapter 5 come up with small signal modelling insight. The model which is used in this work (As the device which is used in this work having transit frequency 7-8 GHz) is suitable for parameter extraction. Then generate the mathematical equation by putting some legal approximation who does not affect the model performance. Simulated and measured data comparison given at the end of this chapter, which tells us that parameter extraction is quite good enough.

Chapter 6 deal with large signal model parameter extraction, in particular the angelov model is taken to extraction procedure because in ADS and in IC-CAP use this model. Finally DC-IV parameter extraction and transfer characteristics parameter is extracted in IC-CAP and result is simulated in ADS to compare measured curve with simulated curve. Only 4.6% error comes in to the simulated curve with respect to measured one which is good agreement.

Finally in the 6th chapter future scope and discussion carried out.

Overall, successfully parameter extraction done and good agreement between simulated and measured data come.

TABLE OF CONTENT

a) Declaration *i*

b) Preface *ii*

c) Acknowledgement *iii*

d) Organizational Profile *iv*

e) List of Figure *viii*

f) List of Table *xi*

g) List of Abbreviations *xii*

h) Abstract *xiii*

1. Introduction **1**

1.1 high speed transistors 2

1.2 main objective of this dissertation work 3

2. Development of FET devices **4**

2.1 Fabrication process 5

2.2 Journey of high speed devices 5

2.2.1 Si based devices (mainly MOSFET) 6

2.2.2 Parameter affects the operation of high speed device 7

2.2.2.1 Device capacitance (Junction capacitance) 7

2.2.2.2 Routing capacitance (Parasitic capacitance)` 7

2.2.2.3 ON state resistance of devices 8

2.2.2.4 Characteristics frequency 9

2.2.2.4.1 Cut off frequency 9

2.2.2.4.2 Transit frequency 9

2.2.3 Compound semiconductor 10

2.2.3.1 Binary compound 10

2.2.3.2 Ternary compound 10

2.2.3.3 Quaternary compound 10

2.2.4 GaAs based device (MESFET) 11

2.2.4.1 MESFET 12

3. *AlGaN/GaN* HEMT 14

3.1 Hetero junction formation in AlGaN/GaN HEMT 15

3.2 Structure of HEMT 16

3.2.1 Substrate 19

3.2.2 Technical advantage of AlGaN/GaN HEMT 19

3.2.3 RF characteristics of AlGaN/GaN HEMT 20

4. Basic idea of modelling and data measurement of active devices 23

4.1 Modelling 24

4.2 Approaches for device modelling 25

4.2.1 Physics based modelling 26

4.2.2 Empirical modelling 26

4.3 Modelling challenges 27

4.4 Data measurement of devices 27

4.4.1 Measurement of IV characteristics 28

4.4.1.1 DC IV measurement 28

4.4.1.2 Pulsed IV measurement 28

4.4.2 S-Parameter measurement 28

4.5 Actual measured data of device 29

4.5.1 De – embedding of data 29

5. Small signal parameter extraction of *AlGaN/GaN* HEMT **32**

5.1 Model for small signal parameter extraction 33

5.2 Intrinsic parameter extraction procedure 35

5.3 Extrinsic parameter extraction procedure 37

5.3.1 Extraction of parasitic resistance and inductance 37

5.3.2 Parasitic capacitance extraction 41

5.4 Extracted parameter value 43

5.5 Comparison of simulated and measured s-parameter 46

6. **Non linear characteristics parameter extraction** **54**

6.1 Non – Linearity 55

6.2 Modelling of drain current 56

6.2.1 Mathematical equation for drain current modelling 57

6.2.2 Meaning of different parameter 57

6.2.2.1 Meaning of I_{pk} and V_{pk} 57

6.2.2.2 Meaning of α_s, α_r and λ 59

6.3 Extracted parameter values 62

6.4 Simulation and comparison with measured data 63

7. Conclusion and Future work **74**

Reference

CHAPTER 1

INTRODUCTION

Fourth generation (4G) & Fifth generation (5G) wireless communication have planned to serve human kind for fetch the information and services at very high speed and at very high frequency with enormous bandwidth. So to achieve this requirement we need the devices that can stand with high speed data and can process accordingly. These devices called high speed devices.

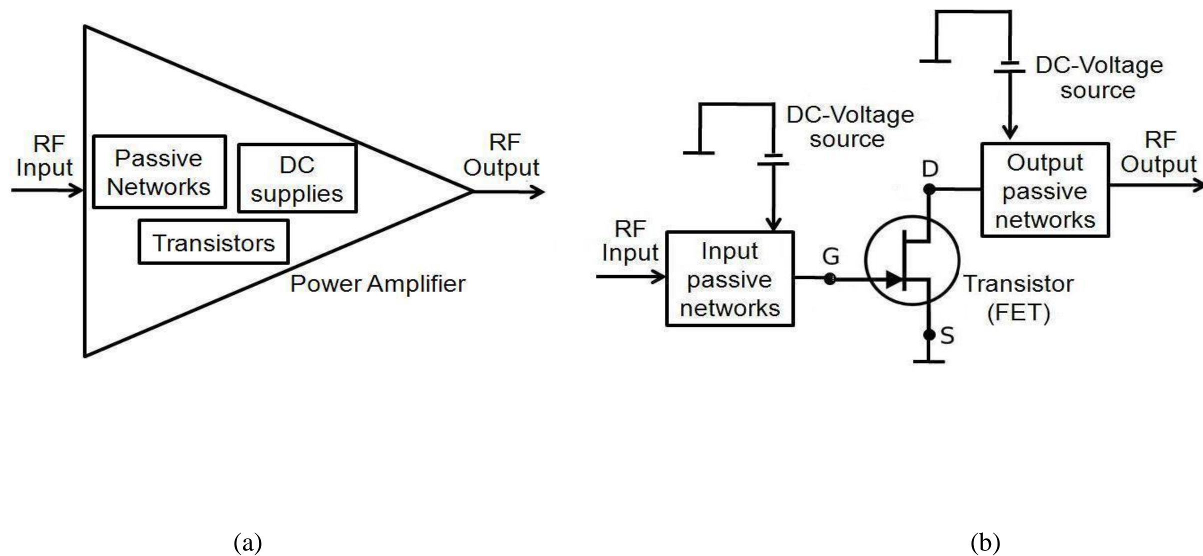
1.1 HIGH SPEED TRANSISTOR

The high speed devices used frequently in mobile communication where large amount of data coming per second, in satellite communication, in radar application etc. In past there were so many developments regarding high speed devices. In this Dissertation work we are going to make an attempt regarding AlGaN/GaN High electron mobility transistor which is high speed device. The idea of HEMT is firstly put forward by Takashi Mimura [1] who belongs to Fujitsu laboratories Japan in 1979. He proposed how to create a separate region for electron motion in field effect transistor. There are so many application of high speed transistor.

1. Small signal Amplifiers
2. Power Amplifiers
3. Mixers
4. Oscillators
5. Attenuators

Apart from all these application most important application is power amplifiers. The main component of power amplifier is transistor.

There are three terminal of FET known as Gate (G), Source (S) and Drain (D) and signal applied between gate and source. The gate terminal (V_{gs}) also known as controlling terminal in that sense it control the current flowing through the channel. As it is important to know that if we apply the gate to source voltage Vgs then how much amount of drain current going to be change that is (dIds/dVgs) is known as trans conductance of device and its give the information regarding the ability of transistor to amplify the signal.



(a) (b)

Fig. 1.1 (a) Basic element of PA **(b)** And basic configuration of PA [2].

1.2 MAIN OBJECTIVE OF THIS DISSERTATION WORK

To design Power amplifier with AlGaN/GaN we require accurate small and large signal model of transistor. There are so many researcher [3-7] who proposed small signal model and large signal model of these devices, but we have to choose the appropriate model for our device so that we will able to produce the accurate parameter extraction by which we can conclude the best match of device model. As we investigate parameter extraction of AlGaN/GaN HEMT it should contain:

1. Right selection of model to extract the parameter
2. Go through mathematical operation for extraction
3. S – Parameter measurement for different frequencies and for different bias
4. De-embedding of DUT (Device under test)
5. Some curve fitting of data if needed
6. Extract the parameter
7. Simulate the result & match it with measured data

Now simulated result & measured data should be match.

CHAPTER 2

DEVELOPMENT OF FET DEVICES

Before use of devices there is a long journey like material selection then wafer fabrication then device growing on wafer then dyeing and so on.

2.1 FABRICATION PROCESS

Modern transistors fabricate layer by layer process. First the layer who supports the foundation called substrate then semiconductor layer on to that substrate then metallic electrode on to semiconductor. All active layer growing is also a process of layer by layer.

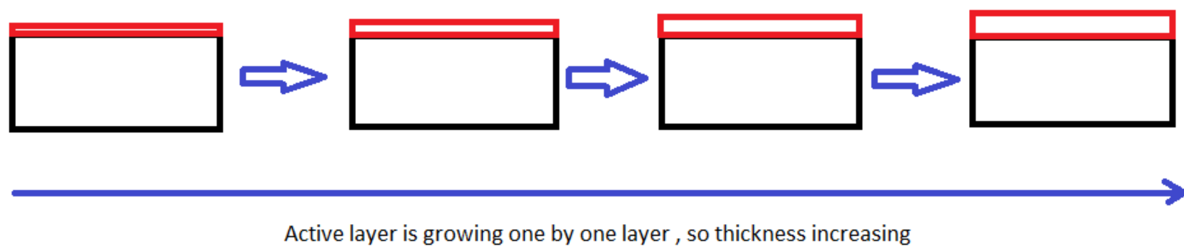


Fig. 2.1: Thickness growing one by one layer

Substrate layer found in the form of wafer. On single wafer there are thousand transistors fabricate so that manufacturing cost can be reduce. After 1947, BJT transistor put forward by Schockley, Bardeen & Brattain, there is a lots of correction and improvement regarding material selection and technology to implement those material into the form of device have been done. Firstly BJT then FET and more recently scientists come with another device called HEMT (High mobility electron transistor) , which can stand for high frequency , high power handling capacity, High mobility, high thermal conductivity, high saturated velocity of electron & high band gap. As lots of work had been done in the past we need to look development of those work.

2.2 JOURNEY OF HIGH SPEED DEVICES

As we know higher temperature handling capacity and higher mobility are the key factor of high speed devices. Here is short summery of material & model development for semiconductor devices. More or less Ge (Germanium) was first semiconductor material which is used for device fabrication, but as it band gap energy ≈ 0.67eV, so maximum operating temperature is around 75°C and it replaced by Silicon very soon (In 1950-60).

2.2.1 SILICON BASED DEVICE (MAINLY MOSFET)

Silicon becomes most dominating semiconductor material ever. Why silicon become so dominating? Here are the main four reasons.

I. Silicon is the most abundant semiconductor material which is found in earth's crust (0.238 weight fraction of earth's crust).

II. Chemical stability of silicon is extremely high (By Deeping in HCl & HNO_3 it does not affect on Si).

III. Silicon surface can be oxidized to SiO_2, Which is used for Gate dielectric, masking layer and in passivation.

IV. Its band gap energy is 1.1eV, so it can operate up to 150^oC, which is for better than Ge.

Due to long journey of research in Silicon technology it becomes mature technology as well. Due to these merits of Si high speed devices & circuits broadly categorise in two groups [9].

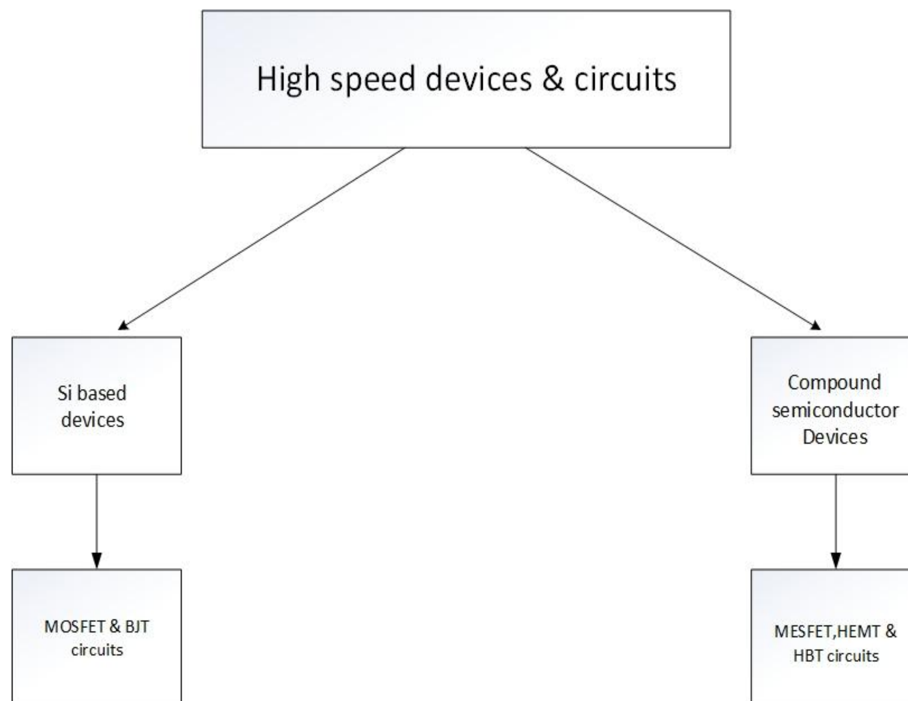


Fig. 2.2: Overviwe of high-speed devices [9].

MOSFET, MESFET, HEMT, HBT's are ues as high speed opration.

2.2.2 PRAMETER AFFECT THE OPRATION OF HIGH SPEED DEVICES

High speed opration or performace limited by four factor.

2.2.2.1 Device Cpacitance (Jn. Cpacitance)

It should be low

For example Gate capacitance

$$w_t = \frac{1}{\tau_t} = 2\pi f_t = \frac{\mu_n (V_{gs} - V_{th})}{L^2} \quad (2.1)$$

L.W.C_{ox} is called total gate capacitance = C_i = i/p capacitance

$$w_t = \frac{\mu_n.(C_{ox}.W).(V_{gs} - V_{th})}{L.(L.C_{ox}.W)} \quad (2.2)$$

$$I_{ds} = \frac{\mu_n.C_{ox}.W}{2L}(V_{gs} - V_{th})^2 \quad (2.3)$$

$$So,\ g_m\left(\text{Transconductance}\right) = \frac{\partial(I_{ds})}{\partial(V_{gs})} = \frac{\mu_n.C_{ox}.W}{L}(V_{gs} - V_{th}) \quad (2.4)$$

$$Now \qquad w_t = \frac{g_m}{C_i} \quad (2.5)$$

This is called "figure of merit".

For better performance or for high speed operation w_t should be high, for that either g_m should be high or C_i should be low.

2.2.2.2 Routing Capacitance (Paracitic Capacitance)

The routing or paracitic capacitance added to junction capacitance & bring down f_t & f_{max}. This paracitic capacitance generate because of pad of drain & source to the substrate. If we can increase thickness of substrate by simply adding insulator (SiC for GaN) the paracitic

capacitance will decrease.If we choose the substrate material with low permitivity then also we are able to decrease the paracitic capacitance.

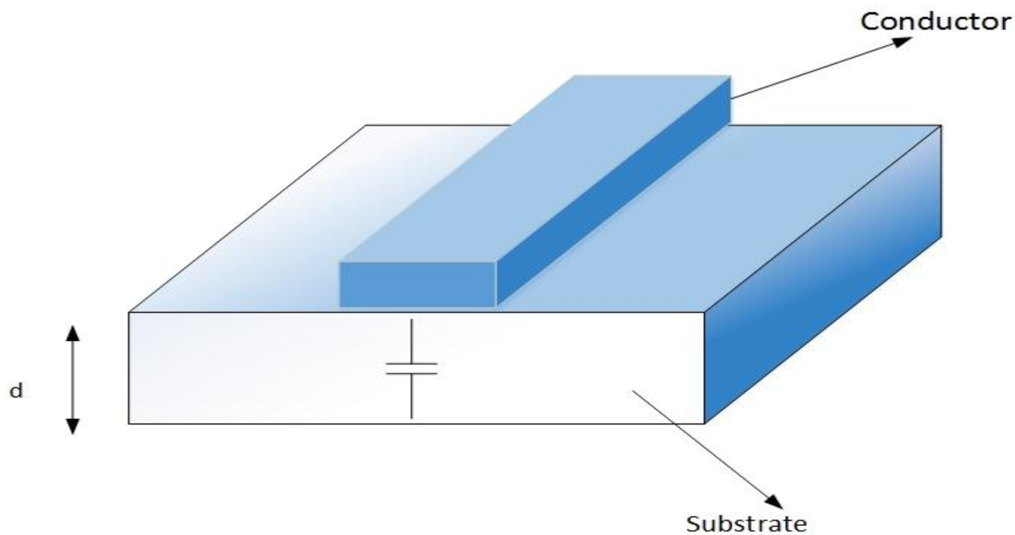


Fig. 2.3: Paracitic capacitance.

2.2.2.3 ON state resistance of devices

R_{on} is the slope of I_D & V_{DS} which show that how fast device come into on state. If R_{on} is small it means that device come into on state early.

For $V_{DS} << (V_{gs} - V_{th})$

So
$$R_{on} = \frac{\partial V_{ds}}{\partial I_d} = \frac{L}{\mu_n . C_{ox} . W . (V_{gs} - V_{th})} \quad (2.6)$$

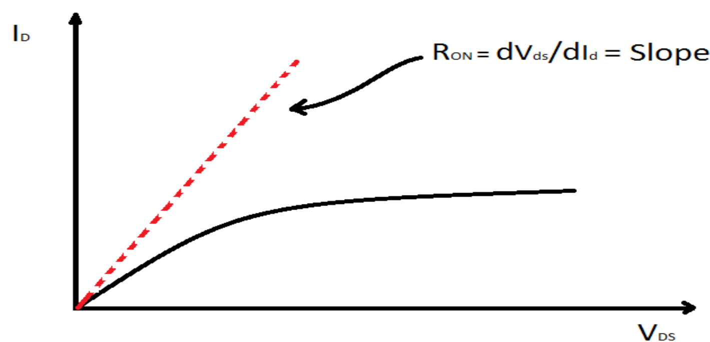


Fig. 2.4: On resistance slope of current voltage curve [9].

From equetion we can say that for small value of L & large value of mobility keep on resistance low, this is benificial for higher switching speed due to faster charging of next stage.

2.2.2.4 Characteristics Frequencies:-

2.2.2.4.1 Cutoff frequency

At power fall to the 50%. This frequency should be high so that device can handle large power which is key thingh of high speed devices.

2.2.2.4.2 Transit frequency

It is related to transit time τ_t, is the time taken by carrier to reach drain from the source. Transit frequency should be high means transit time should a low as possible.

$$w_t = \frac{1}{\tau_t} = 2\pi f_t = \frac{\mu_n (V_{gs} - V_{th})}{L^2} \qquad (2.7)$$

Where L is gate lenth & μ_n is mobility of charge carrier.

From the equation 1 we can see that to get lower transit time there is two option

1. L should be low.
2. μ_n should be high.

So we can coclude that for high speed circuits we need

- ✓ High transconductance
- ✓ Low ON resistance
- ✓ Low transit time
- ✓ High mobility
- ✓ Low Gate length
- ✓ Higher cut-off frequeny

As from above discussion we can see that there is two main aspect who are responsible for high speed opration of device. First one is mobility and second one is shorter gate length.

If any how we are able to manage the larger band gap energy material then those material can stand for high temprature and high frequency opration.

To fulfill all these requirnment we must move towards compound semiconductor.

2.2.3 COMPOUND SEMICONDUCTOR

Compound semiconductor are the best option for higher speed devices. Mainly we are having three type of compound semiconductor.

2.2.3.1 Binary Compound

It is alloys of two element.
For example III-VI compound
III-V compound
IV-IV compound

2.2.3.2 Ternary Compound

It is alloys of three element.

2.2.3.3 Quaternary Compound

It is alloys of Four elements.

Besically people use binary and ternary compound for fabrication of high speed devices.Commonaly GaAs, InP & GaN are used. The mobility and band gap energy of compound semiconductor are shown in figure.

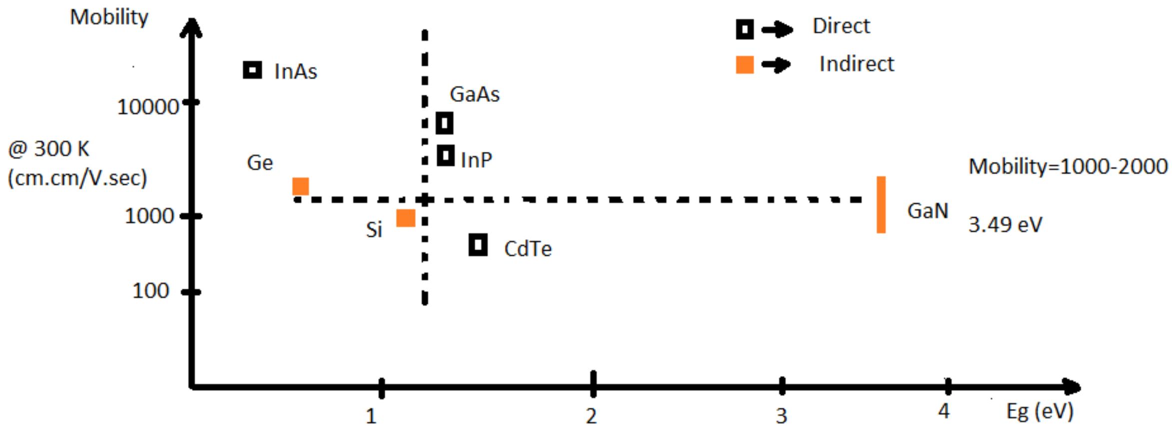


Fig. 2.5: Relative energy band diagram and mobility of different material.

2.2.4 GaAs BASED DEVICE (MAINLY MESFET)

As we know MOSFET is fabricated by Si because it is easy to prepare native oxide of Si which is used for dielectric of gate, but the question is can we make the MOSFET by using compound semiconductor like GaAs ?

Answer is NO. Because it is difficult to make oxide of compound semiconductor. As & Ga As having different oxidation rate, resulting compound semiconductor exhibit very poor interface properties.As MOSFET needs excellent gate dielectric material so realization of MOSFET are not possible with compound semiconductor so Si is the best option for fabricating of MOSFET.

So if we want to fabricate FET device with compound semiconductor we should use MESFET (Metal oxide semiconductor field effect transistor) in which people remove the oxide layer.

2.2.4.1 MESFET

In MESFET

$$g_m = \frac{\mu_n.C_s.W}{L}(V_{gs} - V_{th}) \tag{2.8}$$

$C_s >>> C_{ox}$ because ε_r for GaAs is 12.80 & for Si it is 3.9.

Mobility of GaAs (8500 cm^2/V.sec) is much higher than Si (1500 cm^2/V.sec), so g_m in the case of MESFET with GaAs is 10 to 15 times larger than Si MOSFET.

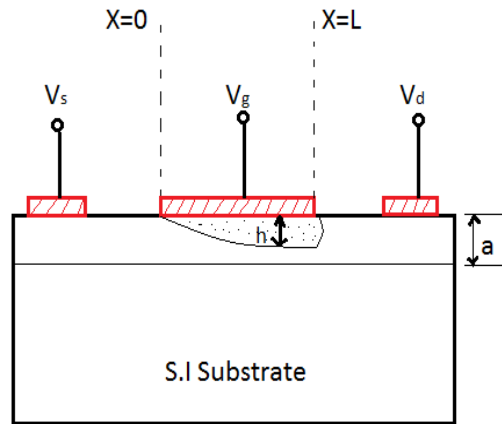


Fig. 2.6 MESFET diagrame.

Current density $J = q.n.v = q.N_d.v$

So current $I_d = J.A = J.W.(a - h) = q.N_d.v.W.(a - h) = q.N_d.\mu.E_s.a.W(1 - h/a)$

$$I_{ds} = \frac{2.C_s.W.v_s}{V_{po}}(V_{gs} - V_{th})^2 \text{, for } V_{po} << L.E_s \tag{2.9}$$

As we decrease L corresponding I_{ds} will independent of L & dependes on saturation velocity, but it hold good when $L > 2.a$.

If $L < a$ then I_d will depends on L. As L start decreasing then 1D assumption of deplition layer will convert in to 2D effect. If we want to reduce L, which is essential for high speed opration, to keep 1D effect we should also decrease ‘a’.

Current I_d will independent of L if ratio of L over 'a' will approximate 3.

As $V_{th} = V_{po} - V_{bi}$, $V_{bi} << V_{po}$, then for $V_{gs} = 0$

Drain current become $I_{ds} = K.V_{po}$ Where K is constant.

$$V_{po} = \frac{q.N_D.a^2}{2.\varepsilon_r.\varepsilon_o} \tag{2.10}$$

Now if we decrease 'a', V_{po} will go down resulting I_{ds} will fall, so one option is that we may increase N_D (Doping concentration) but when we increase doping concentration beyond some extent ($10^{18}/cm^3$) rectifying contact will convert into ohmic contact and mobility will fall [9]. This is the problme with MESFET model.

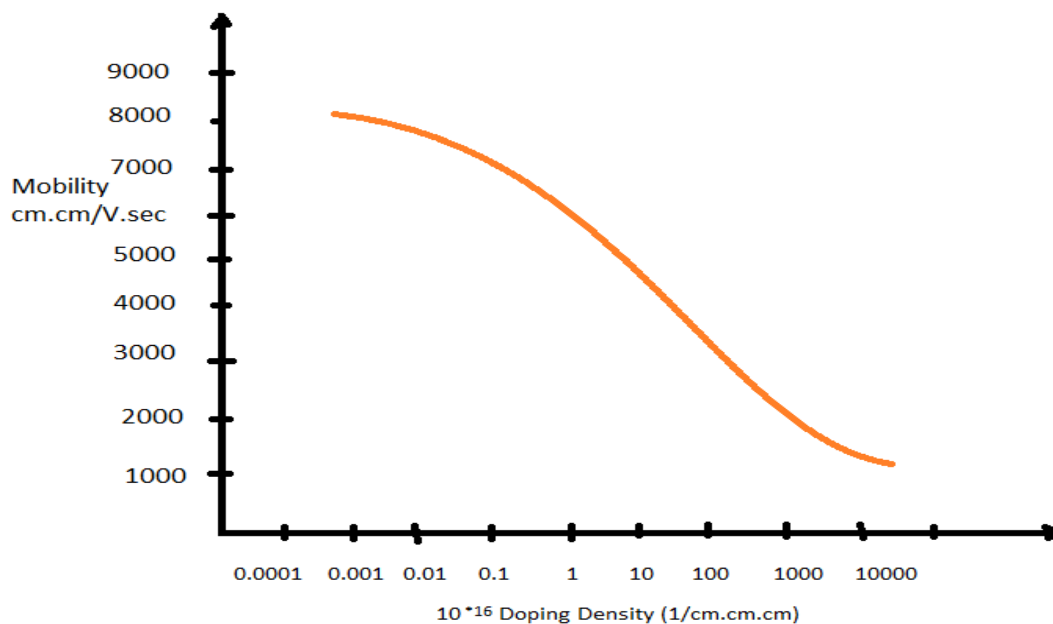


Fig. 2.7: Mobility Vs Doping concentration [10].

So from this point of view we need to separate the doping region & region where electron are present.

Here we are having is different type device called HEMT. In which people create a different region for electron movement called 2-DEG (2 dimensional electron gas) region.

CHAPTER 3

AlGaN/GaN HEMT

3.1 HETERO JUNCTION FORMATION IN AlGaN/GaN HMET

As we have seen in last chapter discussion that when we reduce the gate length (Lg) to maintain 1-Dimensional effect we need to reduce the channel height (a) but when we reduce the "a" pinch off voltage reduce, so we got the idea that is we increase the doping concentration (N_D) we are able to maintain the pinch off constant, but when we increase the doping, mobility of electron decrease significantly because ion impurity scattering, which cause the reduction of current and lower the trans conductance (g_m). In 1979 Mimura [1] in Japan come with outstanding idea of HEMT in which he proposed that if we put to different energy band gap material into contact then we are able to form a hetero junction. Due to formation of hetero junction of two different material there is a potential well formed at the junction in which electron gets trapped, so no electron which cause the current are in doping region resulting no electron face ion impurity scattering, so that mobility increases.

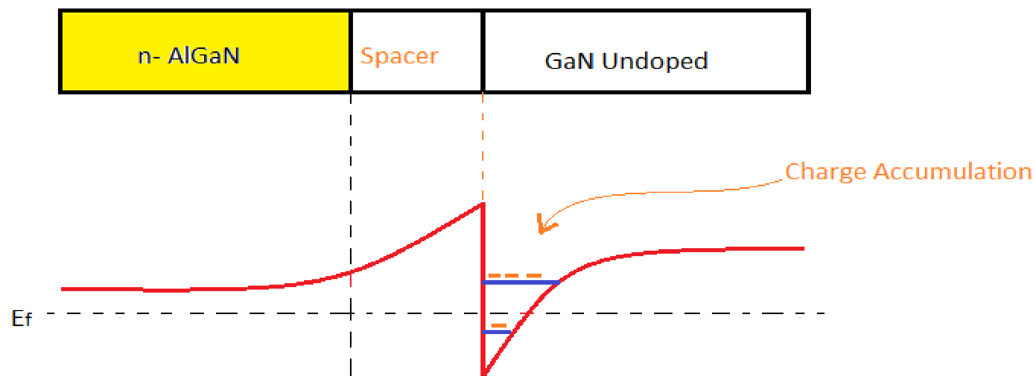


Fig. 3.1: Formation of potential well and electron trapping in the well

As shown in figure n- doped region and un-doped region when come into contact there is a formation of potential well and electron gets trapped in this potential well. This potential well are the order off 10 to 20 A^o , so that it seems to be like 2- dimensional channel that is why it is called 2-DEG (two dimensional electron gas) channel. The most important feature of 2DEG channel is it is free from ion impurity scattering so that mobility of electron increases. High mobility and corresponding high trans conductance due to 2DEG makes HEMT great candidate for high frequency and high power application. Gate voltage controls the carrier density into the potential well so that current gets control.

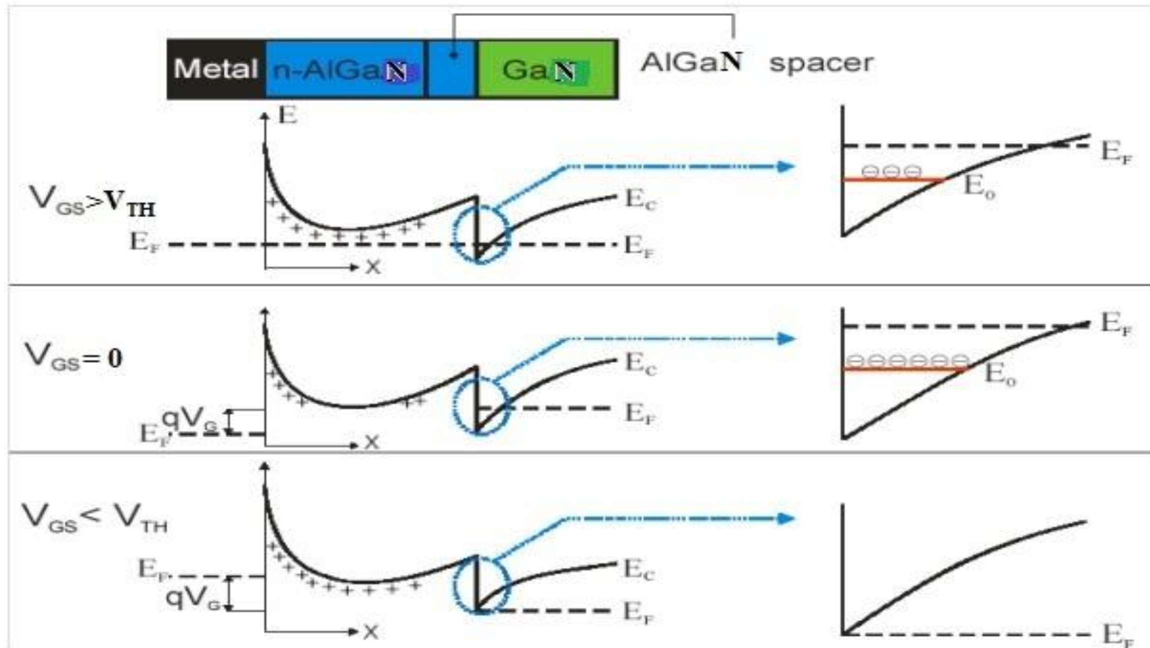


Fig. 3.2: Population of 2DEG for different bias of gate

We alter the population of 2DEG in spite of channel width modulation in MESFET. So that for different bias of gate there is different amount of charge carrier in 2DEG which turns into corresponding drain current.

3.2 STRUCTURE OF HEMT

The main basic structure of HEMT and corresponding band diagram are shown in figure 3.3

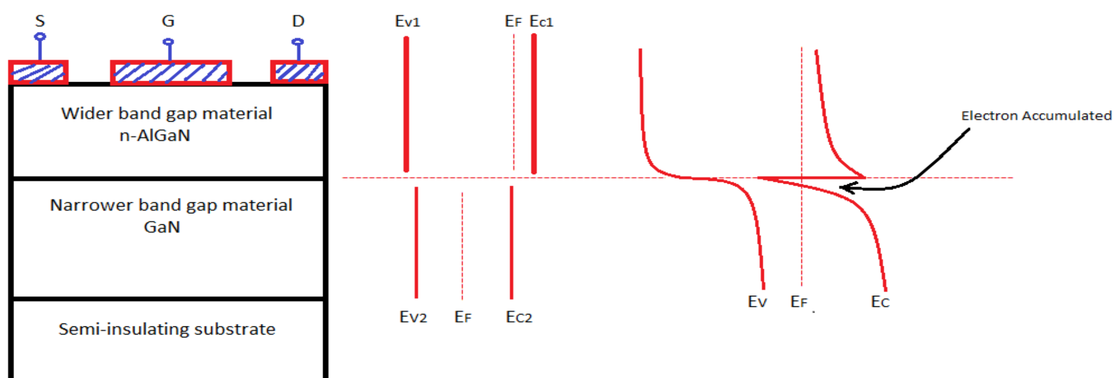


Fig. 3.3: Basic Structure of HEMT and corresponding band diagram

Most of the time we introduce a spacer layer (of un-doped AlGaN) in between the un-doped GaN and n doped AlGaN. By using spacer layer we prevent the electron motion which gets influenced

by doping in AlGaN region. Without such layer electron in the 2DEG are scattered as they pass close to the ionized donors so this scattering reduces electron mobility.

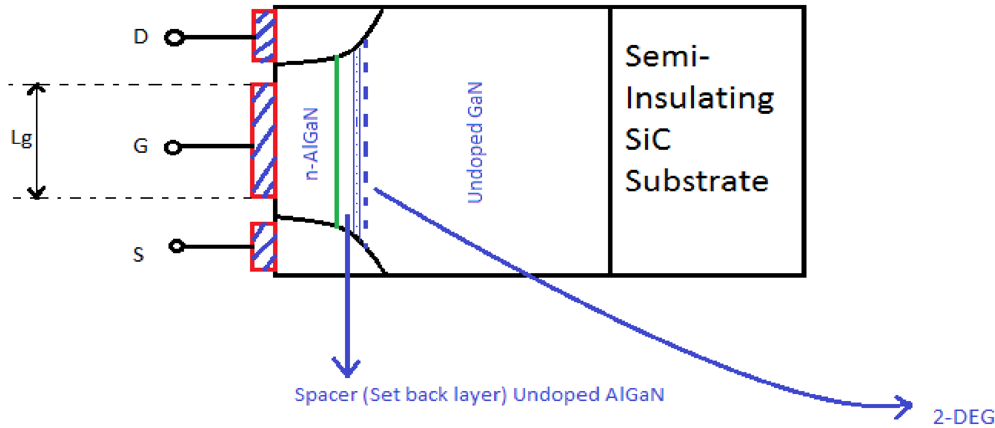


Fig. 3.4: Complete basic structure of HEMT with spacer layer

The most bottom layer of HEMT is Substrate. Commonly people use SiC and Sapphire for GaN based HEMT. Selection of substrate in GaN HEMT is key issue. The advantage of Si compare to the other is low (≈ 10% of sapphire or ≈1% of SiC), availability of lager wafer size and better thermal conductivity than sapphire. But the disadvantages of Si substrate on GaN device in lattice mismatch and low thermal conductivity in compare to the SiC.

Comparison between some important semiconductor material are listed in table 1

Semicondutors ➔	Sapphire	Si	GaAs	InP	GaN	SiC
Band gap (eV)	0.64	1.1	1.43	1.35	3.49	3.26
µ at 300K	-	1500	8500	1450	1000-2000	700
Peak saturation velocity(10 cm/sec)	-	1.0	2.1	2.3	2.1	2.0
Criticle Breakdown Field (MV/cm)	0.2	0.3	0.4	0.5	3.0	3.0
Thermal Conductivity(W/cmK)	0.49	1.5	0.5	0.7	>1.5	4.5
Relative Dielectric	8.9-11.1	11.8	12.8	12.5	10.0	9.0

Table 3.1: Comparison list of semiconductor material

Lattice mismatch of sapphire with GaN is about 14%.

As seen from table 1 GaN & GaAs, InP, SiC are wide band gap material which can stand with high power handling capacity. But due to ease of availability of Si and due to improved technology of GaAs these two candidates commonly used for amplification purpose. GaN are wide band gap semiconductor so it can stand with high temperature (≈500°K) and due to this noise performance of GaN is better than GaAs or InP. Due to so many use of GaN it become main focused for R&D in semiconductor.

In 2001 Cornell University and University of California at Santa Barbara both achieve the transistor based on GaN who can support the power densities above 10W/mm of gate width. The power handling capacity of a transistor are usually define as the watt per unit width of gate that transistor can handle. Researchers at Astralux tested transistor based on GaN in high surrounding temperature of about 300°C with a gain of about 100. Currently researchers spend time on Diamond devices but it is in early stage. As high cost and complex technology it is not very promising candidate for everyone to do research on it [10].

There is possibility to manufacture device with high mobility by GaAs & GaN called HEMT device so as seen in table the low value of mobility of GaN is not a problematic thing. As GaN not having its substrate so that SiC are used with GaN as a substrate material because it having low lattice mismatch (about 4%) and high thermal conductivity (ability to flow the heat into ambient) about 4.5 W/cm.K [10].

High breakdown field of GaN make it to operate at high power. High breakdown field made GaN to stand higher voltage over low dimension. As high band gap material GaN it is so clear and transparent. If one day substrate of GaN become possible then device fabricated by GaN will be total transparent. As we can see that mobility (It is the ability of charge carrier to move into the semiconductor under applied electric field) of electron in bulk GaN (1000-2000) is lower than GaAs (8400).

Si technology is only 10% efficient, 90% power goes wasted as heat in transistor, this heat blast away from the amplifier with the help of powerful fans so that complex circuitry be cool. It is hard to imagine that any internet user at any place in the word download a full HD movie by just clicking the button of their system so one can imagine how we pushed the Si based technology to their limits. As GaN based transistor used in system it might be possible that we can converge

the entire base station of internet to the size of a refrigerator. We can also compare the ability of GaN material to the SiC that SiC cannot form hetero junctions so that SiC cannot used to make HEMT it can be used to fabricate only MESFET. So that there are so many advantage of GaN based devices so that we use it latest technology. There is a major concern regarding GaN substrate selection.

3.2.1 SUBSTRAT

As we discus earlier that selection of suitable material for substrate is most technical issue in case of GaN HEMT for the researchers. As we have discuss earlier that Si is better in terms of wafer cost (10% of sapphire and 1% of SiC), and availability of large wafer size and better thermal conductivity than sapphier, but the major issue with Si is large mismatch to GaN devices. We can see from table1 and table 2 that SiC substrate is most appropriate material for GaN devices in terms of highest thermal conductivity and low mismatch (3-4%). SiC comes currently in 4 inch diameter size by Cree incorporation. Sapphire is also a strong contender regarding inexpensive but having lower thermal conductivity. There are some thermal management which we use for making GaN devices on sapphire called flip-chip mounting technology, but this technology increases cost and complexity of fabrication of devices. So in totality SiC in the best option for substrate for GaN based devices [2].

Attribute	Si (111)	Sapphire (c-plane)	4H-SiC
Thermal conductivity (W/cm·K)	1.5	0.42	4.9
Lattice mismatch with GaN (%)	~ -17	~ -16	~ +3.5
Currently available wafer size (inch)	12	6	4
Cost (compared to Si)	Low	Low	High
Resistivity (Ω cm)	Max 10^4	> 10^6	$10^5 - 10^8$

Table 3.2: Physical property of some promising substrate material for GaN HEMT [3].

3.2.2 TECHNICAL ADVANTAGE OF AlGaN/GaN HEMT

GaN, as a material having some remarkable electronic property that makes it outstanding candidate for high power microwave devices. It having wide band gap (Eg =3.4eV) from table 1, so it is having high electric breakdown (> 2 MV/cm). As resulting it can operate for high drain voltage (> 50V). It also sustain high saturation velocity approximately 2×10^7 cm/sec. GaN device can also stand up to 300°C of channel temperature.

As we know $I_{max} \propto q.\eta_{s}.v_s$ (3.1) where q is charge of electron 1.6×10^{-19}C.

η_s = sheet carrier density (10^{13} cm^{-2}) and v_s is electron saturation velocity.

So when saturation velocity is high in GaN device then current will also be high.

We also know that $f_T \propto v_s/L_{eff}$, As L_{eff} is low in GaN and saturation velocity is high in GaN than overall unit gain frequency is very high in GaN devices.

3.2.3 RF CHARACTERISTICS OF AlGaN/GaN HEMT

There are two main parameters by which one can know the maximum limit of performance, first one is unit current gain frequency (f_t) and second one is max oscillation frequency (F_{max}). Unit current gain frequency is that frequency on which h_{21} is 1. Unit current gain frequency can be extracted from S- Parameter measurement. S-Parameter measurement then converted into h-Parameter and then h_{21} (In dB) plotted in ADS with respect to frequency, plot where cut the 0dB line that frequency is f_t. To calculate h_{21} from S-Parameter we use the following equation

$$h_{21}(dB) = 20\log\left(\frac{-2S_{21}}{(1-S_{11})(1+S_{22})+S_{12}S_{21}}\right) \quad (3.2)$$

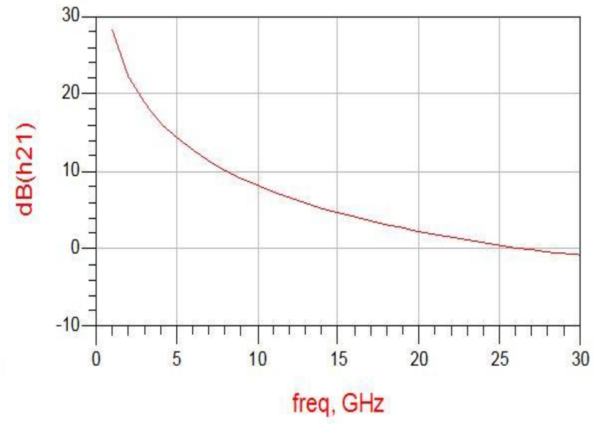
F_{max} is frequency over which maximum unilateral gain is 1. It also can be calculated by S-Parameter measurement by following equation

$$MUG(dB) = 10\log\left[\left(\frac{1}{1-|S_{11}|^2}\right)|S_{21}|^2\left(\frac{1}{1-|S_{22}|^2}\right)\right] \quad (3.3)$$

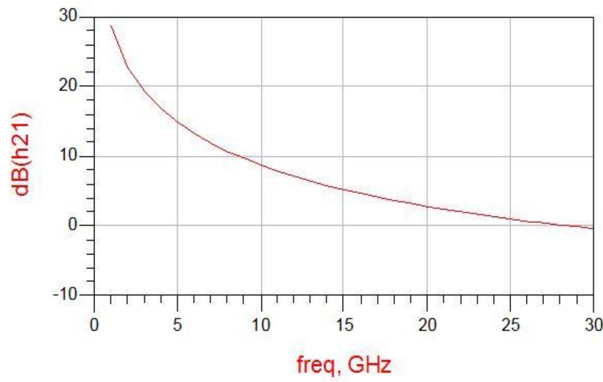
(a)

(b)

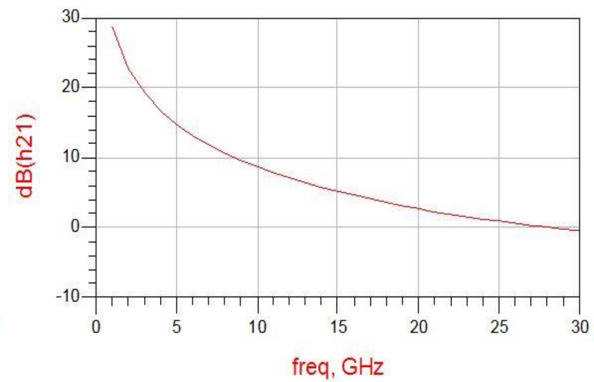
(c)



(d)



(e)



(f)

(g)

Fig. 3.5: Unity current gain curves **(a)** Ft = 16.8 GHz at Vg = 0V, Vd = 10V **(b)** Ft = 21 GHz at Vg = -1V, Vd = 10V **(c)** Ft = 24.05 GHz at Vg = -2V, Vd = 10V **(d)** Ft = 26.55 GHz at Vg = -3V, Vd = 10V **(e)** Ft = 28.1 GHz at Vg = -4V, Vd = 10V **(f)** Ft = 27.95 GHz at Vg = -5V, Vd = 10V **(g)** Ft = 3.5 GHz at Vg = -6V, Vd = 10V.

We can see from figure 3.5, that as we move towards pinch off then f_t decreases. This similar trend follows by the graph of figure 3.6.

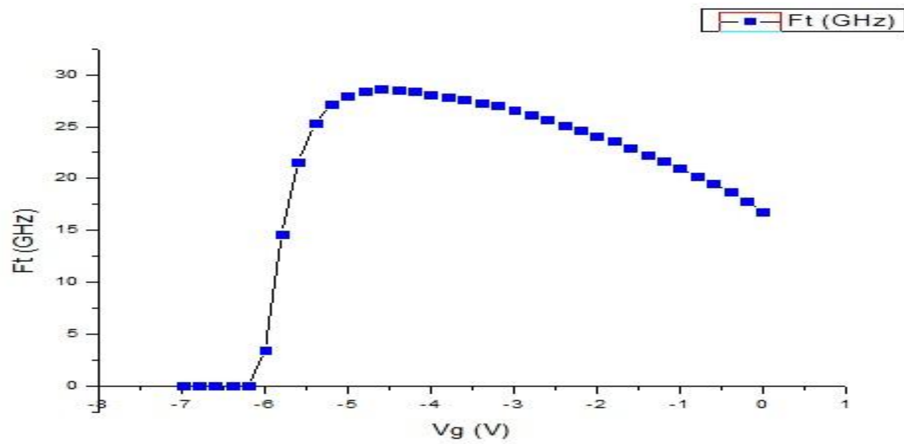


Fig. 3.6: Variation of F_t with respect to V_g

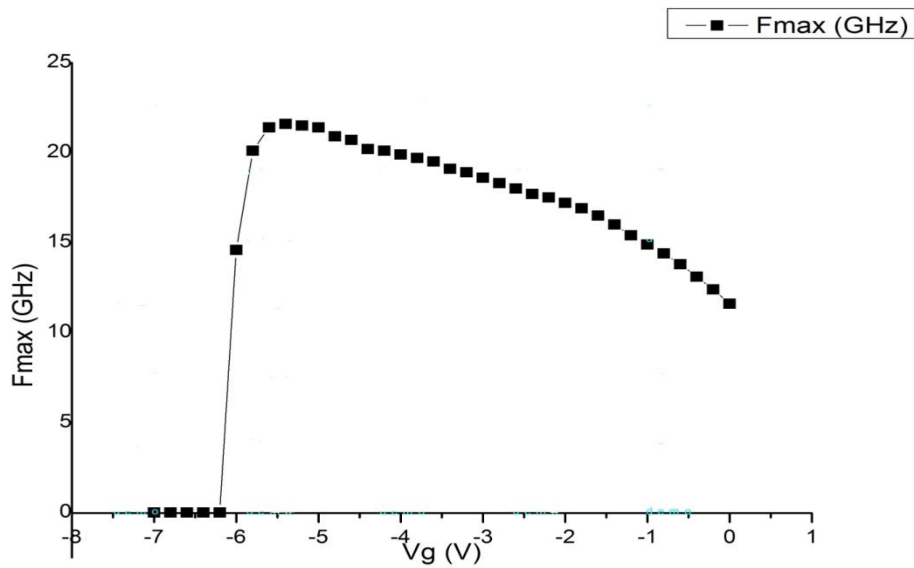


Fig. 3.7: Variation of F_{max} with respect to Vg

Generally for good and healthy operation of device we choose 1/3rd of unit current gain frequency so typically we select 7-8 GHz as an operating frequency. So when we are using a device for modelling purpose with operating range of 7-8 GHz then it is sufficient to use reference [3-5].

CHAPTER 4

BASIC IDEA OF MODELLING AND DATA MEASUREMENT OF ACTIVE DEVICES

In this chapter basic idea of active devices will be presented. Before going to idea and technique of modelling, we should know what is modelling and why it is so important in device characterization.

4.1 MODELLING

Modelling is the basically art of making equivalent circuit and corresponding mathematical equation who govern the behaviour of device as a whole with certain approximation. For simple model we use large number of approximation and for complex model we prefer to use small number of approximation. In other word we can say that device model is the representation of the characteristics of the device in the form of an equation, an equivalent circuit or in the form of diagram/graph/table. Device model is used in analysis, simulation & design of device and circuit. Simulation always cut down the fabrication cost. A device modelling give us a direct relation between terminal quantity like current verses voltage, which is useful for analysis and simulation of a general circuit and quick simulation of particular device [12].

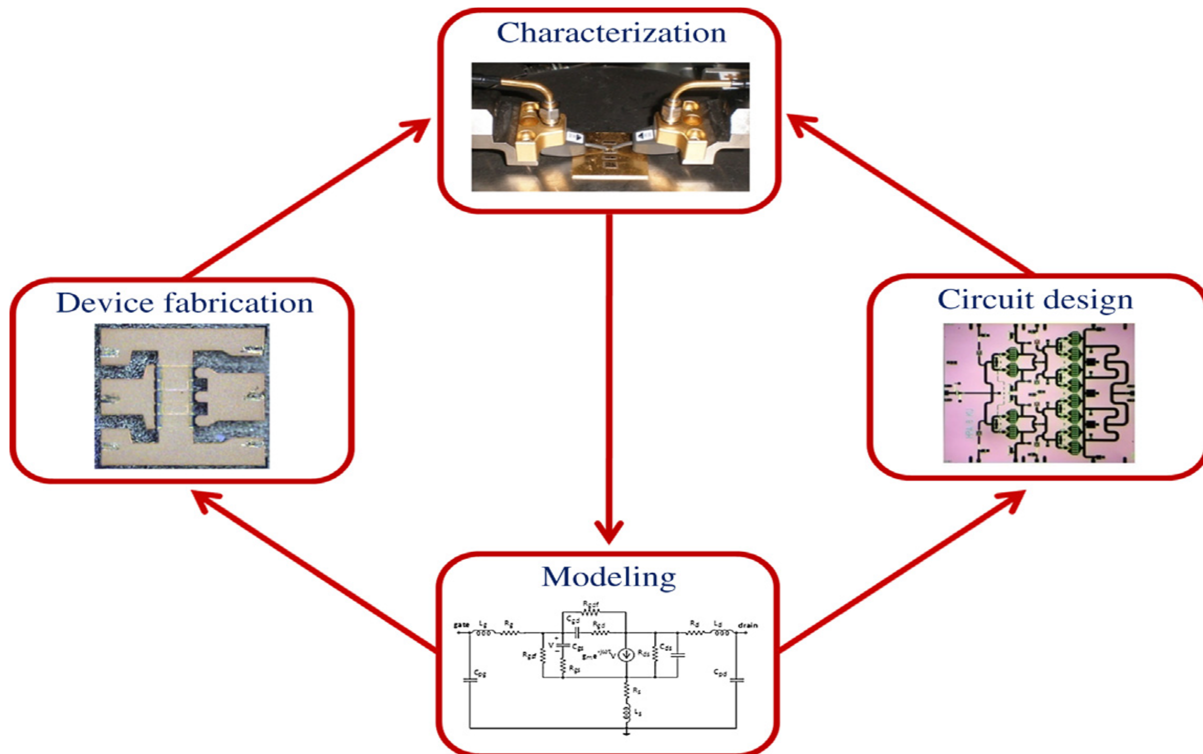


Fig. 4.1: Illustration of the importance of microwave transistor modelling as helpful feedback for device fabrication and as a valuable tool for circuit design [13].

To get the measured data knowledge of microwave measurement setup is good thing. As in this Dissertation we use AlGaN/GaN HEMT then it is mandatory to know about semiconductor physics in sub detail so that so we can link the model to the physical stricture. A good knowledge of circuit theory is essential part of modelling because it is use in selection of network topology.

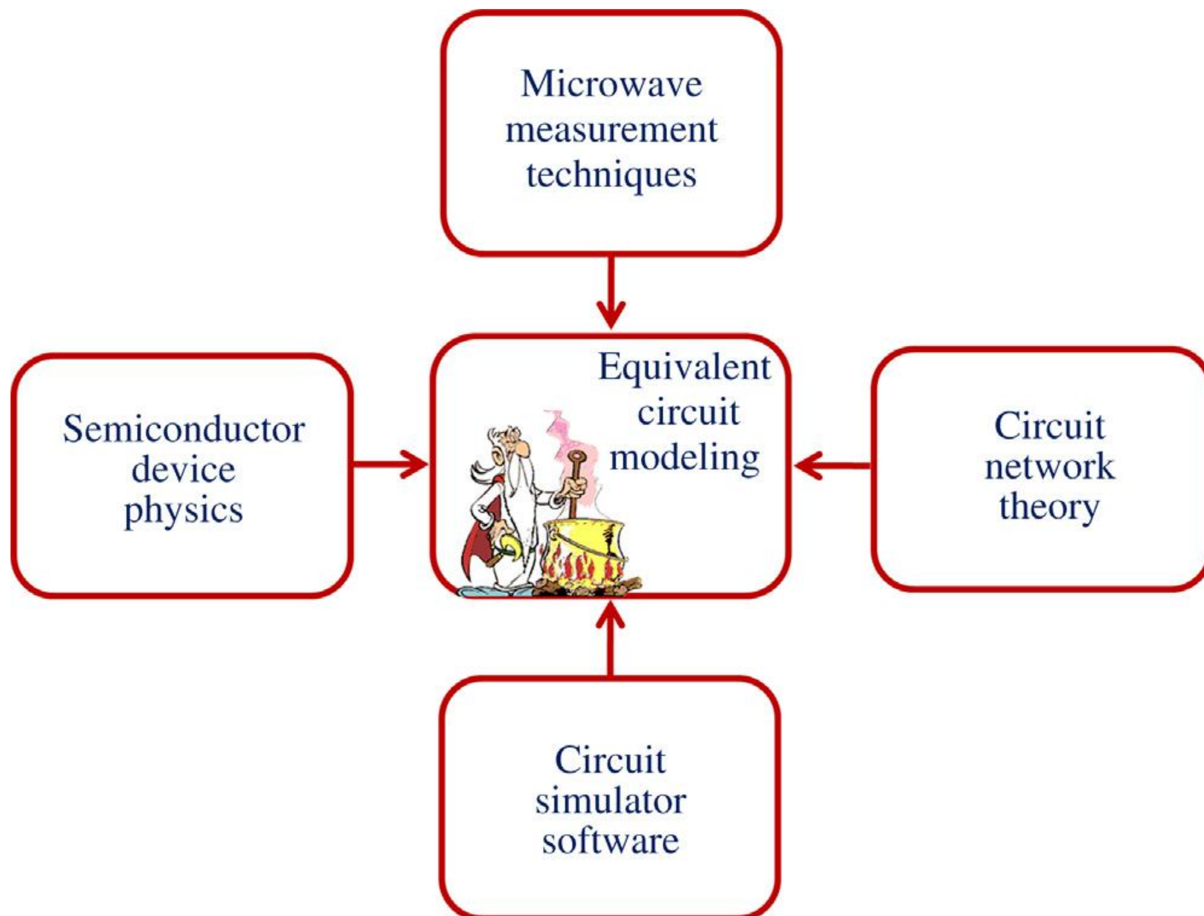


Fig. 4.2: Interdisciplinary knowledge required in microwave device modelling [13].

4.2 APPROACHES FOR DEVICE MODELLING

Mainly there are two approaches for device modelling which is being extensively used. The first one approach is physical modelling; it is based on physics based parameter extractions, which define the geometry and technology of devices. Another is empirical approach for modelling. This approach deals with measurement based characteristics which is being used to describe the device behaviour.

4.2.1 PHYSICS BASED MODELLING

In this modelling approach we use the physics based property like carrier concentration, mobility, conductivity, band gap, thermal conductivity etc to describe the behaviour of devices. The device designer or circuit designers who are having some control on fabrication process get benefited with this approach. The device response is calculated in this process is by solving the some nonlinear differential equation which described the internal electric field of devices and carrier who are responsible for transportation mechanism of device. These nonlinear equations are most of the time become so complex so that to solve these equations we need numerical technique. The main problem with this approach is that we need information regarding technology, assumption and approximations etc which reduces the device model accuracy.

4.2.2 EMPIRICAL MODELLING

This modelling approach is mainly based on measurement based modelling. In this idea we use large amount of data to describe the behaviour of device. This modelling approach is also called "analytical modelling approach" because in empirical modelling we use the analytical equation for the calculation of measured data which finally turns in to the behaviour of device. A lookup table constructed by measured data and this model is based on that lookup table so it is also called "table based modelling". In empirical modelling approach the model accuracy depends on the accuracy of measurement of data has taken. Non-linearity of device come into account solve by some fitting and mathematical optimization [14]. The main advantage of this approach is its simplicity, ability to simulate the measurement data for various ranges, its computational efficiency, so that we are able to compare between different ranges of measured data. The main disadvantage of this model is while we are taking the simplified version of analytical equation it will give us the limited accuracy of device model. As in this model we develop the relation between input and output of device we are able to calculate the output for different input. This modelling approach does not tell us any physics of device. This approach is also having some validity range for which we need to take the data for analytical equation.

In this Dissertation we used this approach for modelling of AlGaN/GaN HEMT for data used from frequency range of 1 GHz to 16 Ghz.

4.3 MODELLING CHALLENGES

As data acquisition is so large in this Dissertation so that to manipulate the parameter with these data is quite difficult because some time for some range of measured data the value of parameter come absurd value at this time we have to take care of it. While we are calculating the average value of parameter for the whole range of frequency we need to take care of those absurd values which come at some specific range of frequency. If we do not take care of those values, the outcome will be very destructive which will lead the offset outcome between measured value and simulated values.

In non linear modelling if we do not take in to account that the particular parameter or constant affect which area of IV curve and transfer curve then achieving good result is quiet difficult. In non linear modelling also we need some clarity of parameter otherwise doing optimization, tuning or curve fitting lead the result far away from the desired results.

4.4 DATA MEASUREMENT OF DEVICES

Data measurement of device is most important work which is used for characterization of device and accuracy and reliability of devices. The reliability of small signal modelling and large signal modelling strongly depend upon the measurement uncertainty. As data acquisition is so important in device modelling therefore this section deals with data measurement.

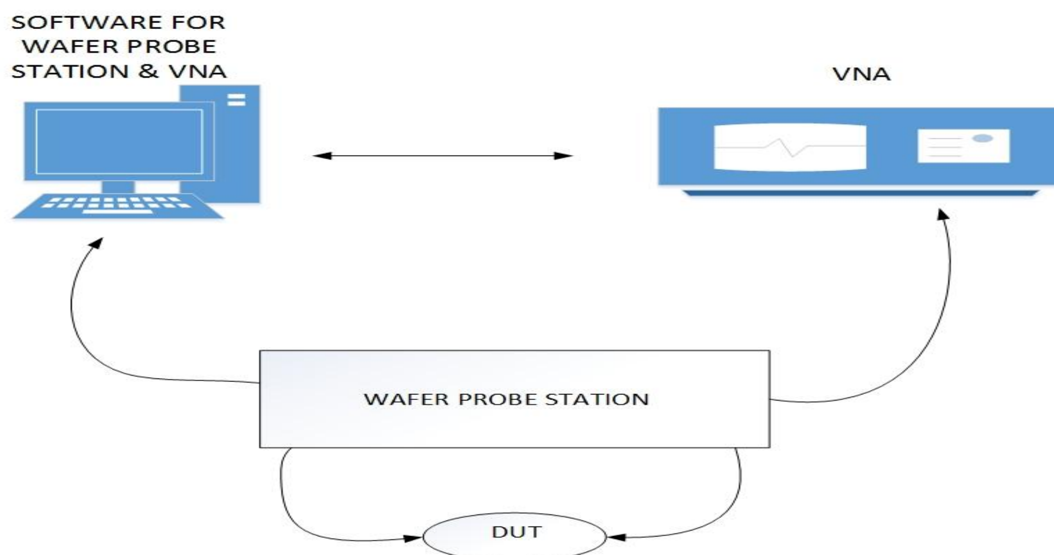


Fig. 4.3: Data measurement setup

4.4.1 MEASUREMENT OF IV CHARACTERISTICS

4.4.1.1 dc IV measurement

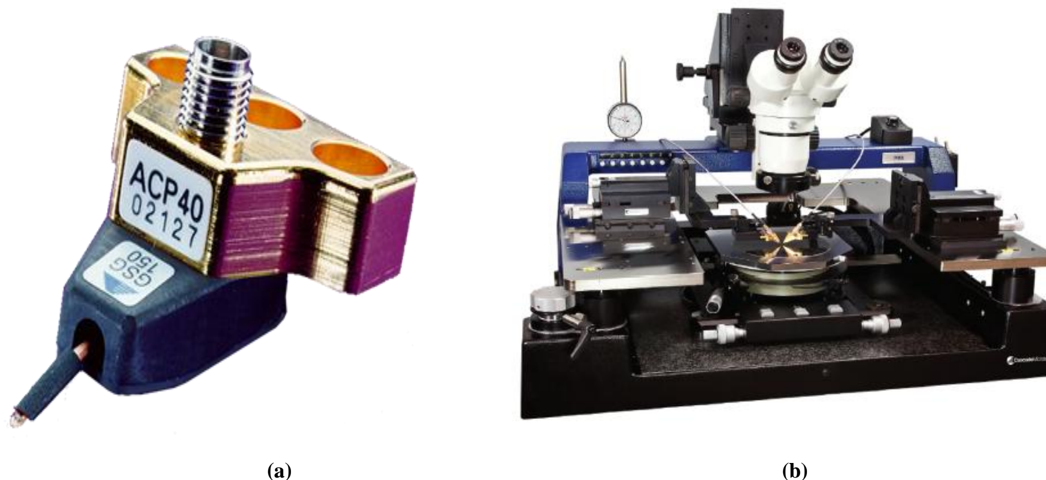
In device modelling the DC IV measurement is most important things. For active device DC IV measurement we use different Ig and Id current for different bias point (For different Vg & for different Vd). In these measurements self heating is key thing so that while doing measurement we should put some time delay between successive measurements so that device can cool down enough. If we follow this process then we will get uncorrelated measurements. Safe operating voltage, current and power take into account so that measurement does not lead the local destruction (like burning of pad) of device.

4.4.1.2 Pulsed IV measurement

It overcomes the disadvantage of DC IV measurement. In pulsed IV measurement we provide isothermal condition to the device. Under appropriate quiescent bias condition and thermal temperature the pulsed IV measurement is used.

4.4.2 S – PARAMETER MEASUREMENT

For small signal modelling the S–parameter measurement is the most common and important measurement. For different frequency range (1 GHz to 16 GHz for our device) and for different bias point (Vg = -7 to 0V with Vd = 0V, Vg = -15 to 0V with Vd = 10V) S - parameter measurement done. These S-parameter measurements taken with help of wafer probe station, VNA, Cables and Probes.



(a) (b)

Fig. 4.4: **(a)** Wafer testing probe, **(b)** Wafer probe station

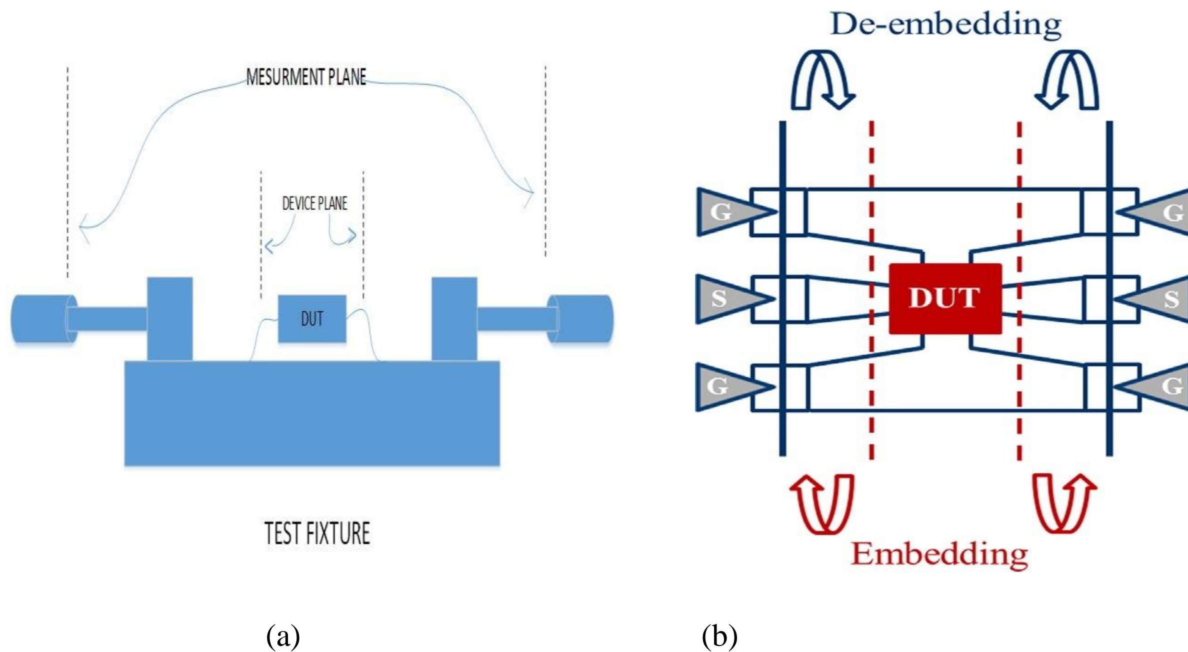
For the best measurement the knowledge of these devices and calibration procedure need to know. From these S – Parameter we are also able to calculate f_t & F_{max} which decide the maximum operational region of AlGaN/GaN HEMT.

4.5 ACTUAL MEASURED DATA OF DEVICE

When we take the measurement of device with the help of wafer testing probe there is some parasitic effect come into the account which lead the extraction out of the way consequently simulation give the result with great off set. So for getting the accurate simulated result with respect to the measured result, we need to de-embed those parasitic effects which come into measured data.

4.5.1 DE-EMBEDDING OF DATA

DE-embedding is the process in which we remove the losses, occur due to coaxial cable, due to wafer probe, pads, metal interconnection etc. Actually VNA measured the S-Parameter up to measurement plane; if we want to know the actual S-Parameter of DUT then we need to perform de-embedding operation so that measurement plane can shift to the device plane which contains actual S-Parameter of DUT. This shifting of plane is also known as mathematical shift of electrical reference plane [13].



(a) (b)

Fig. 4.5: **(a)** DUT with measurement setup **(b)** process of de embedding and embedding [13]

The process of shifting the electrical reference plane closer to the DUT is called De-embedding and if electrical reference plane shifting away from the DUT is called embedding as in fig 4.5. As transistor cannot be probed directly, there is a requirement of pad and interconnection. If we increase the operating frequency the parasitic effect of these pads and interconnection significantly increases.

In this Dissertation, proposed de embedding process is two- step de embedding. In two step de embedding process we use open structure and short structure of DUT.

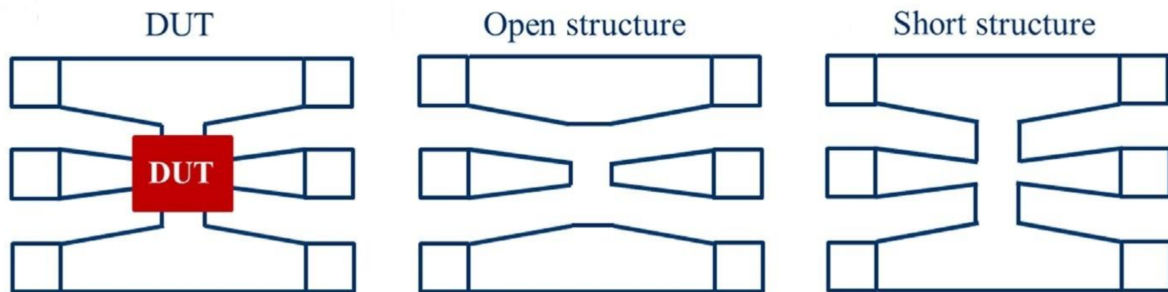
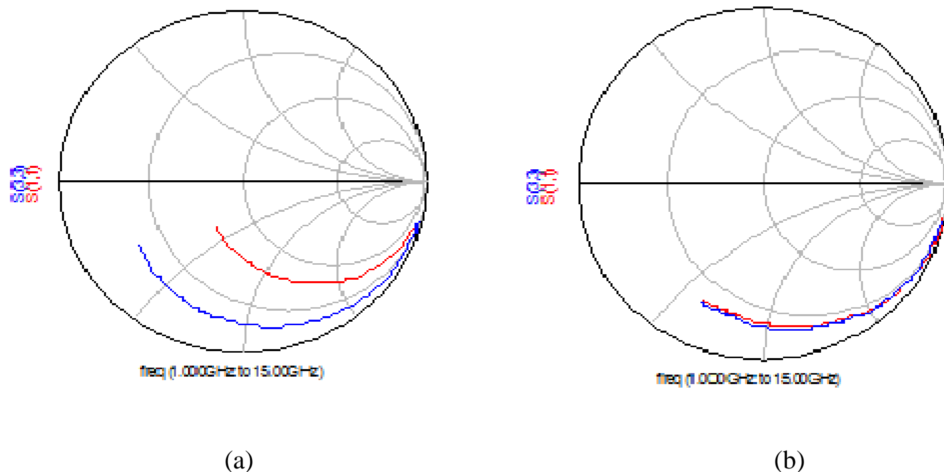


Fig. 4.6: open and short structure used for de embedding [13].

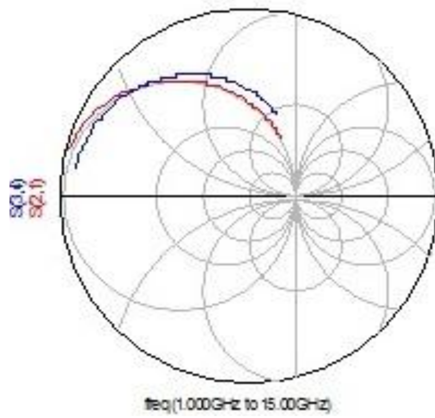
The fundamental approach to de embed the data consist three steps-

1. Y- Parameter of measured data
2. Y- Parameter of open and short structure
3. Remove Y- Parameter of these structure from the measured data
4. Remaining Y-Parameter will belong to the pure DUT

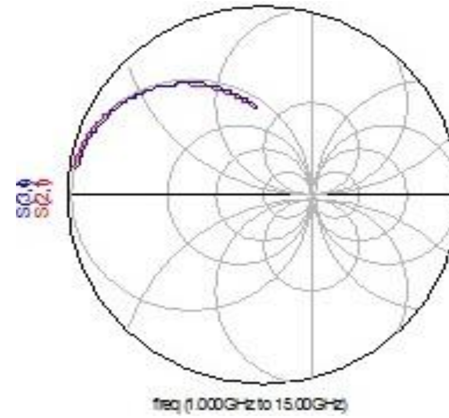
One can clearly see the difference between without de embedded simulated data and measured data with without de embedded simulated data and measured data in fig. 4.7.



(a) (b)



(c)



(d)

Fig. 4.7: (a) & (c) Without de embedding **(b) & (d)** With de embedding

Magnitude and phase will also not match without de embedding along with S parameter mismatch. So it is essential to perform the de embedding process before modelling and parameter extraction.

CHAPTER 5

SMALL SIGNAL PARAMETER EXTRACTION OF *AlGaN/GaN* HEMT

As we see in chapter 2 the f_t and f_{max} of AlGaN/GaN HEMT is 7-8 GHz so proposed strategy for small signal parameter extraction is based on Damberin, Berroth and Miras model [4-6]. As we discussed earlier that empirical modelling is based on measured data, so small signal parameter extraction will also use the measured data to extract the small signal parameter.

So in this Dissertation we will discuss model and relative mathematical formulation first then extracted parameter second then simulated the result and comparison of simulated result with measured data finally.

The parameter extraction will be divided in to two part first is extrinsic parameter and second is intrinsic parameter. Combine these two types of parameter will give the complete behaviour of a device, which we will see in comparison and discussion sub chapter.

5.1 MODEL FOR SMALL SIGNAL PARAMETER EXTRACTION

The model which is used in this dissertation is taken from Damberin model and correction from Berroth and Miras [4-6]. The model is divided in to two part extrinsic parameter and extrinsic parameter. There are 7 parameters related to the intrinsic model and 8 parameters related to extrinsic model so complete number of parameter is 15.

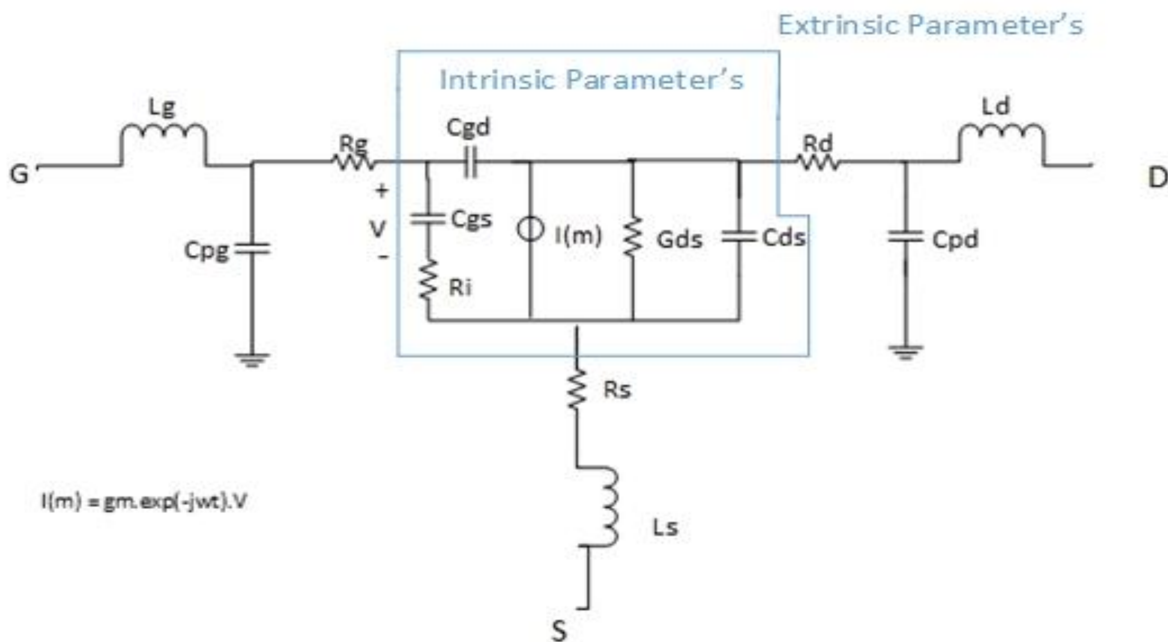


Fig. 5.1: Small signal equivalent circuit for AlGaN/GaN HEMT

The parasitic effect is related to the extrinsic parameter and these parameters are independent to the bias point of gate and drain and frequency. The extrinsic parameters are basically belongs to the active layer of device and these parameters are dependent of bias point of gate and drain but these are also independent of frequency of RF input signal.

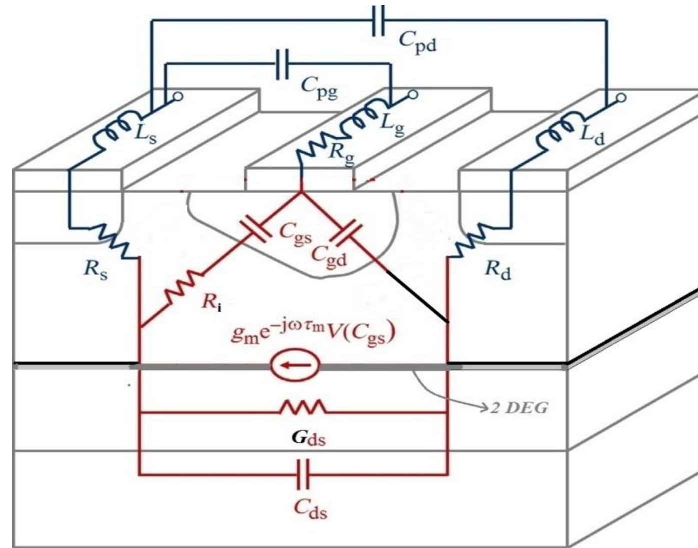


Fig. 5.2: Physical meaning of parameter associated with AlGaN/GaN HEMT

As seen in figure 5.2 current is related to the 2-DEG region, τ is transit time, the time taken by electron to reach the drain from source. R_s, R_d and R_g are the ohmic and rectifying contact resistance respectively these are responsible for current reduction flowing throw the 2-DEG layer. Similarly L_s, L_d, and L_g are the inductance which is arises due to bias of drain, source and gate. The parameter C_{gs} and C_{gd} are charge storage effect between gate-source and 2DEG and between gate-drain and 2DEG region. These charge storing capacity take some finite time to store in between the electrode and 2DEG with time constant R_iC_{gs} and $R_{dg}C_{gd}$ (R_{gd} is not shown in figure 5.2), this is the concept for origin of these parameters. The 2DEG responsible for current flow in the potential well, so the parameter I_m and R_{ds} (=1/G_{ds}) are related to the flow of current and this current is controlled by voltage across the C_{gs}, and proportional to the trance conductance g_m. C_{ds} is the capacitance related to the geometrical region of 2DEG.

These all parameter will govern the basic small signal behaviour. As we discuss earlier we have taken some approximation but these approximation will not affect greatly to the extracted value of parameter.

5.2 INTRINSIC PARAMETER EXTRACTON PROCEDURE

If we consider only intrinsic part of the model we can easily say that this portion of model having π- topology, so that this part can easily characterize by admittance parameter, so that these parameter can be relate to the Y-Parameter. The Y- Parameter can be write as [15].

$$Y_{11} = \frac{Ri.Cgs^2.w^2}{D} + jw\left(\frac{Cgs}{D} + Cgd\right) \quad (5.1)$$

$$Y_{12} = -jw.Cgd \quad (5.2)$$

$$Y_{21} = \frac{g_m.e^{-jwt}}{1 + jRi.Cgs.w} - jwCgd \quad (5.3)$$

$$Y_{22} = G_{ds} + jw(Cds + Cgd) \quad (5.4)$$

Where $D = 1 + w^2.Cgs^2.Ri^2$

As HEMT is a high speed and low noise device, many experiment shows that for high speed and low noise device the second term of "*D*" that is $(w.Cgs.R_i)^2$ is less than one so that we can assume that "D" ≈ 1.

And For HEMT type devices $\tau \approx 0.1$ to 1ps

Let's take w = 5 and 10 GHz

For 5 GHz $\quad w.\tau = 0.03$

For 10 GHz $\quad w.\tau = 0.06$

In both cases $w.\tau$ is very less than one so that Y_{21}-Parameter of intrinsic model will converge into following equation

$$Y_{21} = g_m - jw.(C_{gd} + g_m(Ri.C_{gs} + \tau)) \quad (5.5)$$

All other equetions will remain same by putting D = 1, only equetion no (5.3) convert into equetion no (5.5).

Now all intrinsic parameter can be extracted form these equetions written on next page.

$$C_{gd} = -\frac{\mathrm{Im}(Y_{12})}{w} \tag{5.6}$$

$$C_{gs} = \frac{\mathrm{Im}(Y_{11})}{w} - C_{gd} \tag{5.7}$$

$$G_{ds} = \mathrm{Re}(Y_{22}) \tag{5.8}$$

$$C_{ds} = \frac{\mathrm{Im}(Y_{22})}{w} \tag{5.9}$$

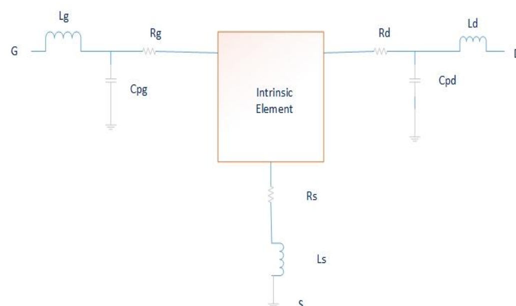
$$R_i = \frac{\mathrm{Re}(Y_{11})}{(C_{gs} \times w)^2} \tag{5.10}$$

$$g_m = \mathrm{Re}(Y_{21}) \tag{5.11}$$

$$\tau = \left(-\frac{\mathrm{Im}(Y_{21})}{(w \times g_m)} - \frac{C_{gd}}{g_m} - (R_i.C_{gs}) \right) \tag{5.12}$$

But the million dollar question is that how we will get these equations from the S-Parameter, when the S-Parameter is totally belong to the device as a whole, when the measured S-Parameter contain intrinsic as well as extrinsic parameter.

The procedure to get the Y- Parameter is taken from the Dambrine [4]. Suppose we know the parasitic element or parameter values then



$$\begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix}$$

S➔Z

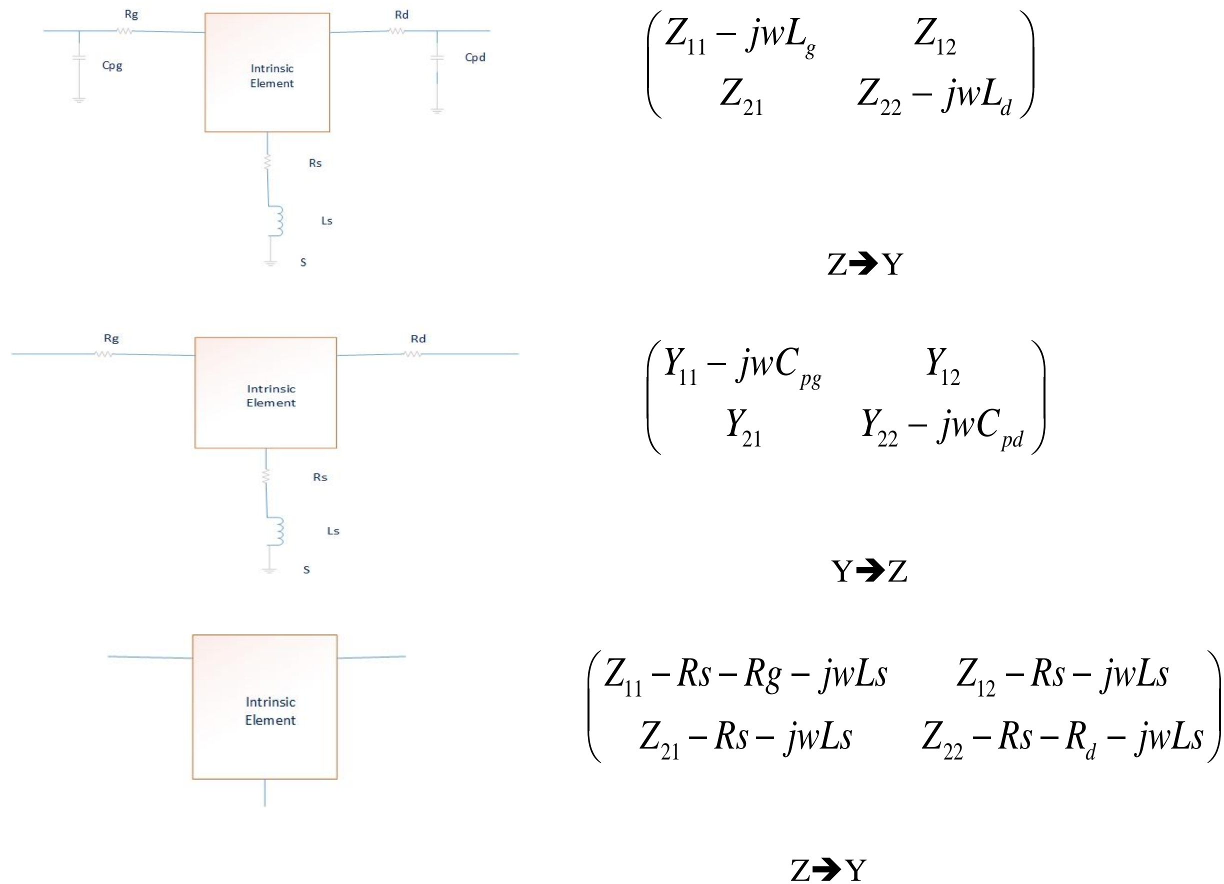


Fig. 5.3: Procedure to extract the intrinsic Y parameter from measured S parameter [3].

Finally the conversion of Z-Parameter to Y-Parameter will give the desired parameter. But again the big question is how we are able to know the extrinsic parameter values?

Our next task should be how to extract the extrinsic parameter so that we can find the intrinsic one.

5.3 EXTRINSIC PARAMETER EXTRACTION PROCEDURE

5.3.1 EXTRACTION OF PARASITIC RESISTANCE AND INDUCTANCE

When we do not apply the drain and gate voltage with respect to source that means Vgs = 0 and Vds = 0 [16-17], then there is no current flow in the 2DEG region and in this condition device can be treated as without intrinsic parameters.

There is additional $Z_{11,}$ requires the contribution of C_{gch} (Parasitic capacitance under gate) parallel with R_{gch} (Schottky Resistance of the gate). And R_{ch} is the resistance of the channel under the gate [24].

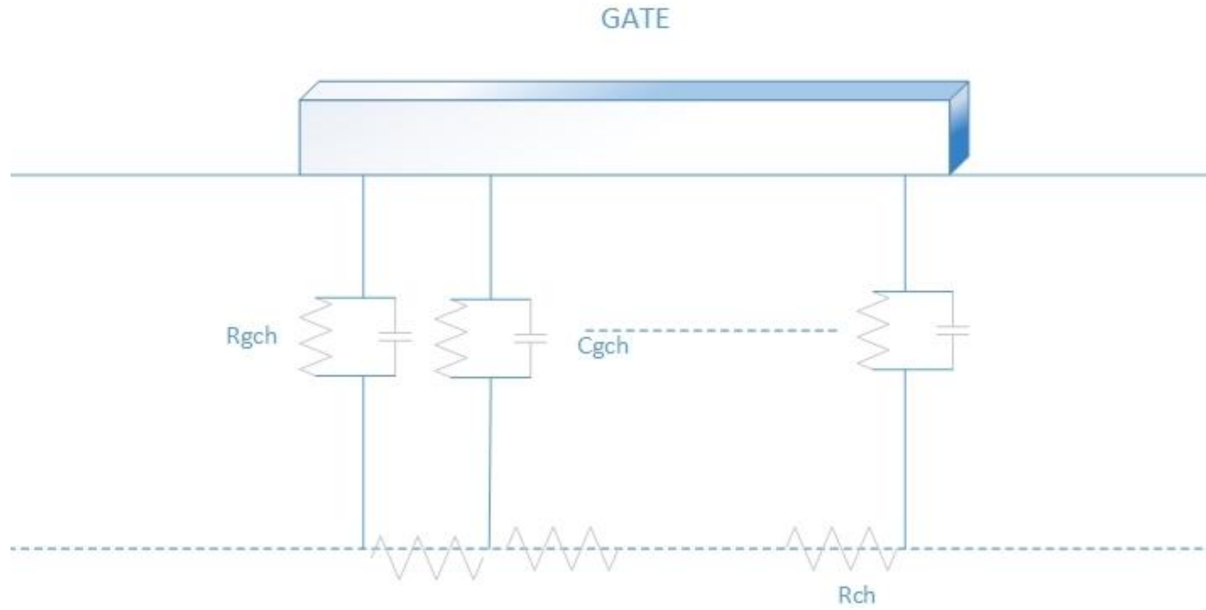


Fig. 5.4: Distributed RC network under the gate region

As we have taken that V_{ds} = 0V, then Z_{gch} (Parallel combination of C_{gch} and R_{gch}) can be written as [15]

$$Z_{gch} = \frac{R_{gch}}{1 + j.w.C_{gch}.R_{gch}} \tag{5.13}$$

Now the all Z-Parameter can be written as below

$$Z_{11} = \frac{R_{gch}}{3} + Z_{gch} \tag{5.14}$$

$$Z_{12} = Z_{21} = \frac{R_{ch}}{2} \tag{5.15}$$

$$Z_{22} = R_{ch} \tag{5.16}$$

$$R_{gch} = \frac{nKT}{qI_g} \tag{5.17}$$

Where R_{ch} calculation is crucial and it need to be carried out .

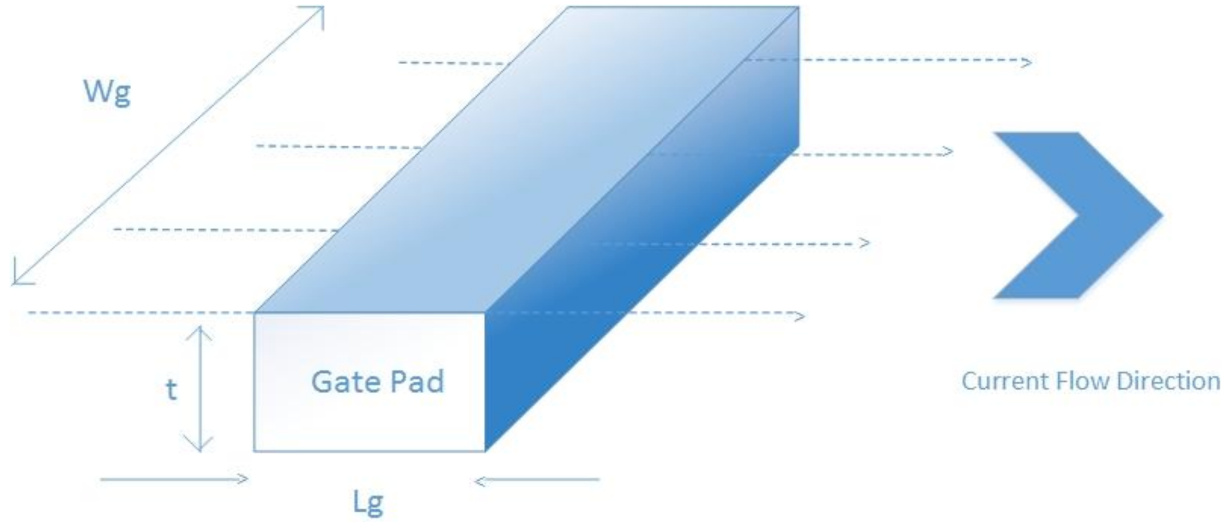


Fig. 5.5: Flow of current across the gate pad

So, for this configuration the calculation of R_{ch} deals with these dimensions of the gate. In general R_{ch} in known as 2 DEG technological parameter resistance. This resistance strongly depends on sheet resistance (η_s). Sheet resistance can be calculated by a numerical method called transmission line method [4]. This is hard part to calculate the R_{ch}, because calculation of sheet resistance itself is a rigours process. In this Dissertation 0.8×100 µm and sheet resistance 300Ω AlGaN/GaN HEMT is used. This data provided by SSPL fabrication lab DRDO New Delhi.

So
$$R_{ch} = \rho \frac{L_s}{A}$$

$$A = W_g \times t$$

$$R_{ch} = \left(\frac{\rho}{t}\right)\left(\frac{L_g}{W_g}\right)$$

$$R_{ch} = \eta_s \left(\frac{L_g}{W_g}\right) \tag{5.18}$$

Where η_s is equal to the (ρ/t).

For 0.8× 100 micrometer with gate finger 2 the R_{ch} will be 1.2Ω. This value of R_{ch} will be used for rest of the calculation.

As we are not giving large forward bias to the gate then Z-Parameter can be written as below

For $V_{ds} = V_{gs} = 0$ V.

$$Z_{11} = R_s + R_g + \frac{R_{ch}}{3} + \frac{R_{gch}}{1+(R_{gch}.C_{gch}.w)^2} + jw\left[L_s + L_g - \frac{R_{gch}{}^2.C_{gch}}{1+(R_{gch}.C_{gch}.w)^2}\right] \quad (5.19)$$

$$Z_{12} = Z_{21} = R_s + R_{ch} + jwL_s \quad (5.20)$$

$$Z_{22} = R_s + R_d + R_{ch} + jw(L_s + L_d) \quad (5.21)$$

In case of "cold" condition which is $V_{ds} = V_{gs} = 0\ V$, C_{pd} and C_{ds} are negligible and C_{pg} is included in C_{gch}.

From equations we can find out the extrinsic parameters as from equation 5.22 to 5.25.

$$L_s = \frac{\mathrm{Im}(Z_{12})}{w} \quad (5.22)$$

$$L_d = \frac{\mathrm{Im}(Z_{22})}{w} - L_s \quad (5.23)$$

$$R_s = \mathrm{Re}(Z_{12}) - \frac{R_{ch}}{2} \quad (5.24)$$

$$R_d = \mathrm{Re}(Z_{22}) - R_s - R_{ch} \quad (5.25)$$

The value of L_g and R_g can be calculeted by equetion (5.19), but as we can analyse the equetion (5.19) there is two more unknown call R_{gch} and C_{gch} and both these euation can not be directely obtain by simple mathametic. So we need to fit the measured data value of Z_{11} by any function who can take care of these two unknown. In this dissertation curve fitting analysis is done by MATLAB curve fitting tool.

5.3.2 PARASITIC CAPACITANCE EXTRACTION

Researchers throughout the world use V_d = 0V and gate voltage below to the pinch off to find out the parasitic capacitance value [4 and 16]. When we use this situation V_d = 0V and V_g < pinch off then small signal equivalent gets simplified and converted into

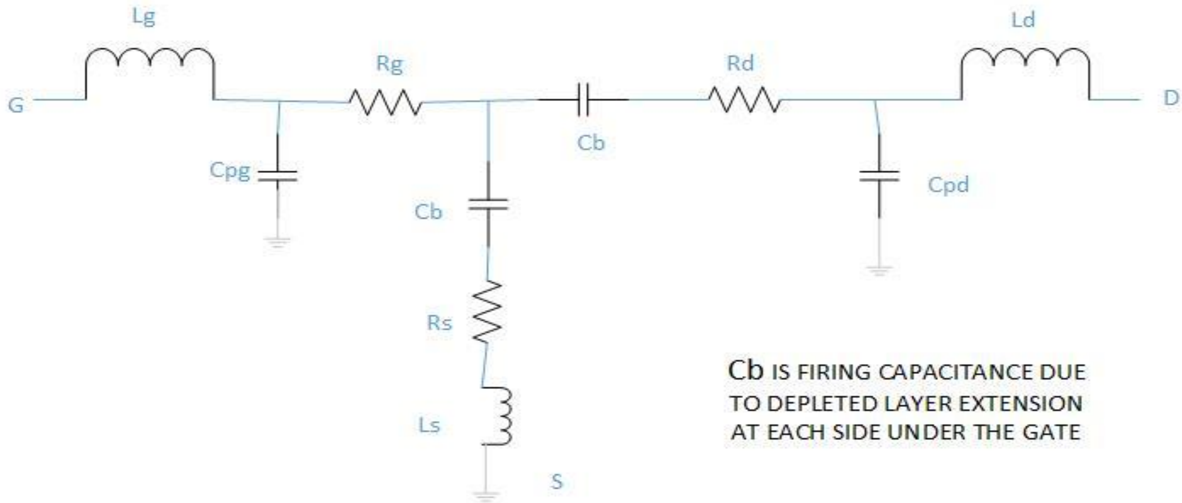


Fig. 5.6: Simplified small signal circuit of HEMT for situation V_d = 0V and V_g < pinch off [2].

Gate parasitic and drain parasitic capacitance can be calculated with pinch off S- parameter measured data.

Y-parameter can be estimated as

$$Y_{11} = jw(C_{pg} + 2C_b) \tag{5.26}$$

$$Y_{12} = Y_{21} = -j.w.C_b \tag{5.27}$$

$$Y_{22} = j.w(C_{pd} + C_b) \tag{5.28}$$

So,

$$C_b = -\frac{\mathrm{Im}(Y_{12})}{w} = -\frac{\mathrm{Im}(Y_{21})}{w} \tag{5.29}$$

$$C_{pd} = \frac{\mathrm{Im}(Y_{22})}{w} - C_b \tag{5.30}$$

$$C_{pg} = \frac{\mathrm{Im}(Y_{11})}{w} - 2C_b \tag{5.31}$$

From equation 5.26 to 5.28 one can say that imaginary part of Y_{11}, Y_{12}, Y_{21} and Y_{22} are linear function of frequency and it can verified from measured imaginary Y parameter in figure 5.7.

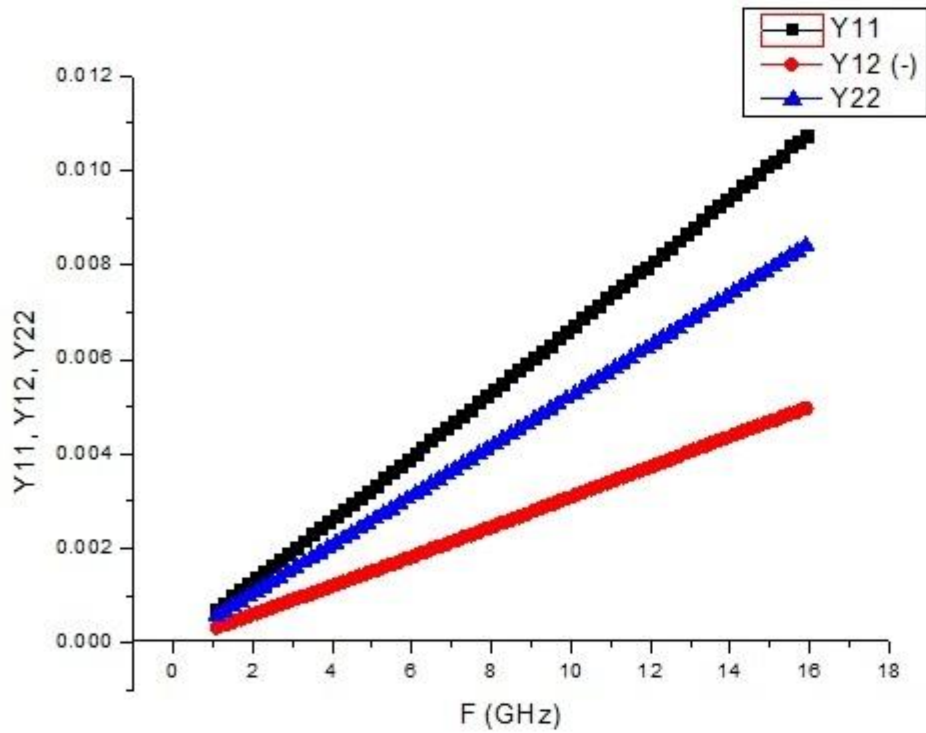


Fig. 5.7: Simulated Y-Parameter with respect to frequency of 0.8× 100 µm AlGaN/GaN HEMT device

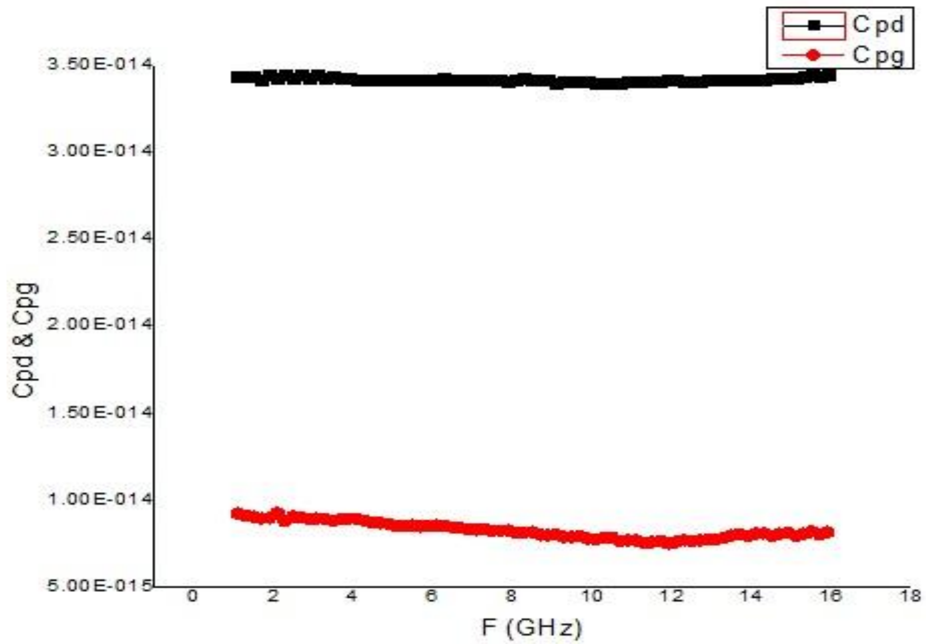


Fig. 5.8: Consistency of Cpd and Cpg value throughout the frequency range of 0.8× 100 µm AlGaN/GaN HEMT device .

5.4 EXTRACTED PARAMETER VALUES

With Vds = 0 V, Vgs = 0 V,

Ls = 0.00576 (nH)	**Rs** = 2.9621 (Ω)
Lg = 0.00576 (nH)	**Rg** = 5.5769 (Ω)
Ld = 0.00423 (nH)	**Rd** = 5.1847 (Ω)

Table 5.1: Extracted extrinsic parasitic resistance and inductance values of 0.8× 100 μm AlGaN/GaN HEMT.

With Vds = 0 V, Vgs = -Vp = -7 V,

Cb = 48.9 (fF)	**Cpd** = 34.14 (fF)	**Cpg** = 8.25 (fF)

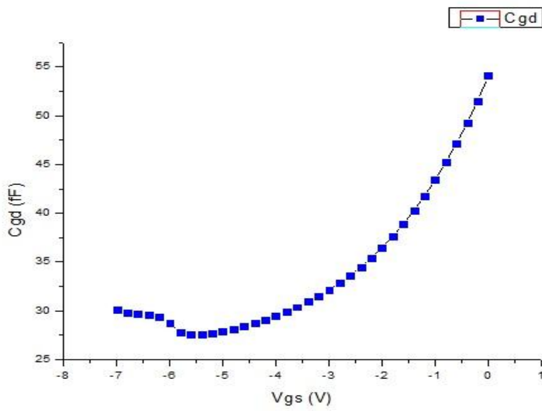
Table 5.2: Extracted extrinsic parasitic capacitance values of 0.8× 100 μm AlGaN/GaN HEMT device

With Vds = 10V,

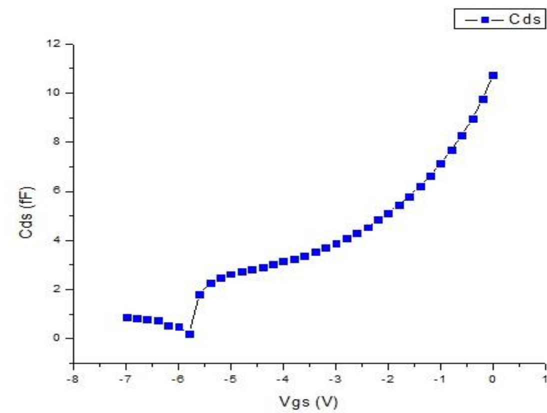
Vgs	Cgd (fF)	Cds (fF)	Cgs (fF)	Gds (mS)	Ri (Ω)	Gm (mS)	T (nsec)
0.0	54.083	10.745	247.12	3.5	8.5454	33	0.001166
-0.2	51.526	9.7542	245.55	3.3	7.8592	34.6	0.001136
-0.4	49.243	8.938	244.56	3.2	7.2268	36	0.001100
-0.6	47.166	8.2751	244.12	3.1	6.6630	37.4	0.001065
-0.8	45.219	7.6757	244.42	3.1	6.0655	38.8	0.001049
-1.0	43.419	7.1312	245.35	3.0	5.4842	40.2	0.001039
-1.2	41.774	6.6391	246.76	2.9	4.9182	41.5	0.001036
-1.4	40.266	6.2100	248.50	2.9	4.3962	42.8	0.001032
-1.6	38.880	5.8050	250.53	2.8	3.9300	44.1	0.001023
-1.8	37.631	5.4600	252.68	2.8	3.5640	45.4	0.0010007
-2.0	36.487	5.1244	254.89	2.7	3.1373	46.6	0.000999
-2.2	35.453	4.8360	257.13	2.7	2.7221	47.8	0.001006
-2.4	34.498	4.5360	259.37	2.7	2.2946	49.0	0.00102
-2.6	33.635	4.3070	261.56	2.6	1.9324	50.1	0.00102
-2.8	32.850	4.0840	263.64	2.6	1.5323	51.2	0.001053
-3.0	32.143	3.8913	265.57	2.6	1.1906	52.3	0.00107
-3.2	31.499	3.7017	267.30	2.5	0.8447	53.2	0.001094
-3.4	30.914	3.5356	268.77	2.5	0.5295	54.1	0.001094
-3.6	30.380	3.3840	269.94	2.4	0.2213	54.9	0.0011468
-3.8	29.898	3.2540	270.73	2.4	0.0822	55.6	0.0011810
-4.0	29.464	3.1483	271.00	2.3	0.3159	56.1	0.00120
-4.2	29.070	3.0250	270.66	2.3	0.5351	56.4	0.001236
-4.4	28.716	2.9220	269.52	2.2	0.7575	56.4	0.001280
-4.6	28.40	2.8341	267.31	2.1	0.9023	55.9	0.0013198
-4.8	28.12	2.752	263.59	2.0	0.9889	54.8	0.001363
-5.0	27.884	2.634	257.77	1.9	0.9825	52.8	0.001418
-5.2	27.693	2.486	248.71	1.8	0.8035	49.3	0.001483
-5.4	27.57	2.2759	234.26	1.5	0.3466	43.5	0.00159
-5.6	27.54	1.814	210.22	1.2	0.7168	33.8	0.001797

Vgs	**Cgd (fF)**	**Cds (fF)**	**Cgs (fF)**	**Gds (mS)**	**Ri (Ω)**	**Gm (mS)**	**τ (n-sec)**
-5.8	27.763	0.1956	167.55	0.66	3.5573	18.3	0.002309
-6.0	28.71	0.497	102.28	0.1478	9.85	2.8	0.00398
-6.2	29.414	0.546	68.68	0.0585	14.633	0.052	0.006977
-6.4	29.618	0.736	58.74	0.0557	20.1443	0.0321	0.02548
-6.6	29.709	0.808	54.91	0.05542	23.414	0.0336	0.02083
-6.8	29.82	0.845	52.88	0.0549	25.766	0.0355	0.02144
-7.0	30.10	0.859	51.88	0.0533	27.1326	0.0455	0.0303

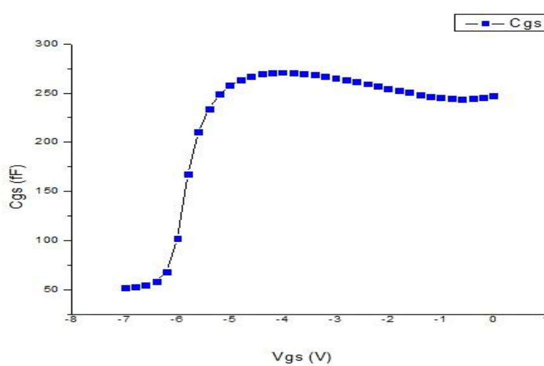
Table 5.3: Extracted intrinsic parameter values for different bias point of 0.8× 100 μm AlGaN/GaN HEMT device.



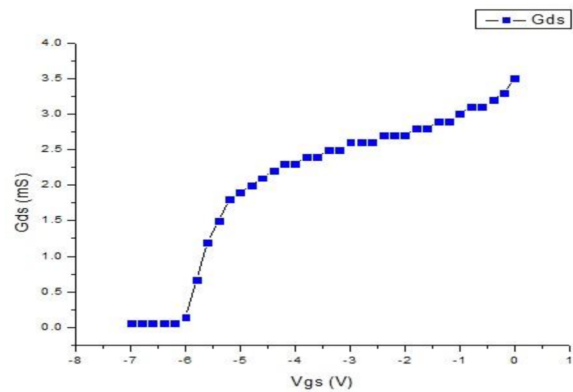
(a) Cgd



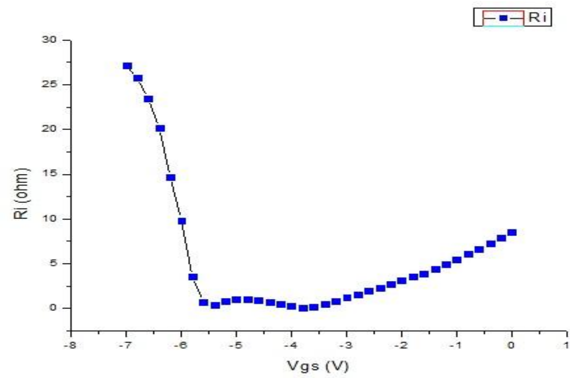
(b) Cds



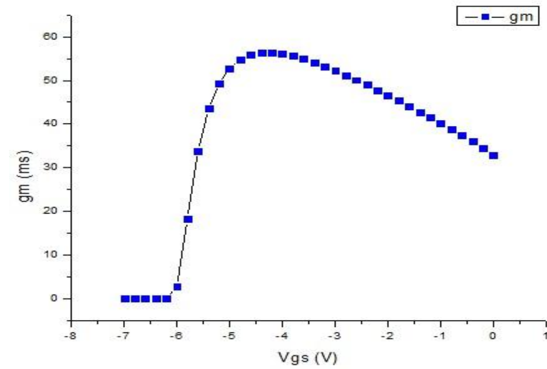
(c) Cgs



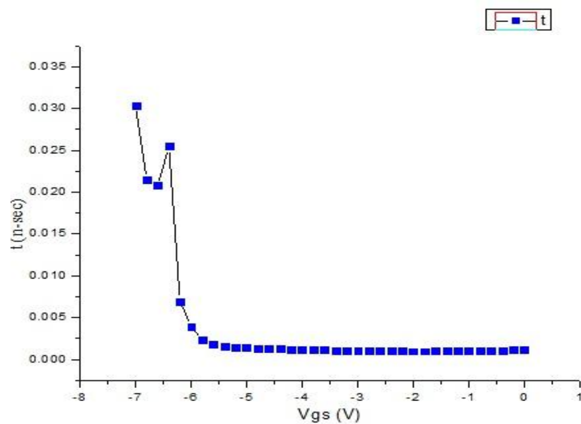
(d) Gds



(e) Ri



(f) gm



(g) τ

Fig. 5.9: Extracted intrinsic parameter values form "a to g" for 0.8× 100 μm AlGaN/GaN HEMT device

Finally the intrinsic parameters were extracted in table 5.1, 5.2 and 5.3 respectively which is shown in fig. 5.9. The extracted parameter clearly shows there transition in pinch off region from the normal region of operation. Position of C_{gs} is in between gate contact and channel carrier density, charge of channel is make capacitance effect, if gate voltage increases above pinch off the charge get closer to the gate so C_{gs} increases. C_{gd} and C_{ds} at close to the pinch off are showing negligible value and it is quiet intuitive because in pinch off region C_{gd} and C_{ds} extended into the depletion region.

5.5 COMPARISON OF SIMULATED AND MEASURED S-PARAMETER

Simulated result is now needed to verify with the measured data for any particular bias point to validate the value of extracted intrinsic parameter values. Then checking of simulated parameter values in ADS with measured S- parameter has been done. We have seen that extracted model is having good agreement with measured S- parameter over the wide range of frequency.

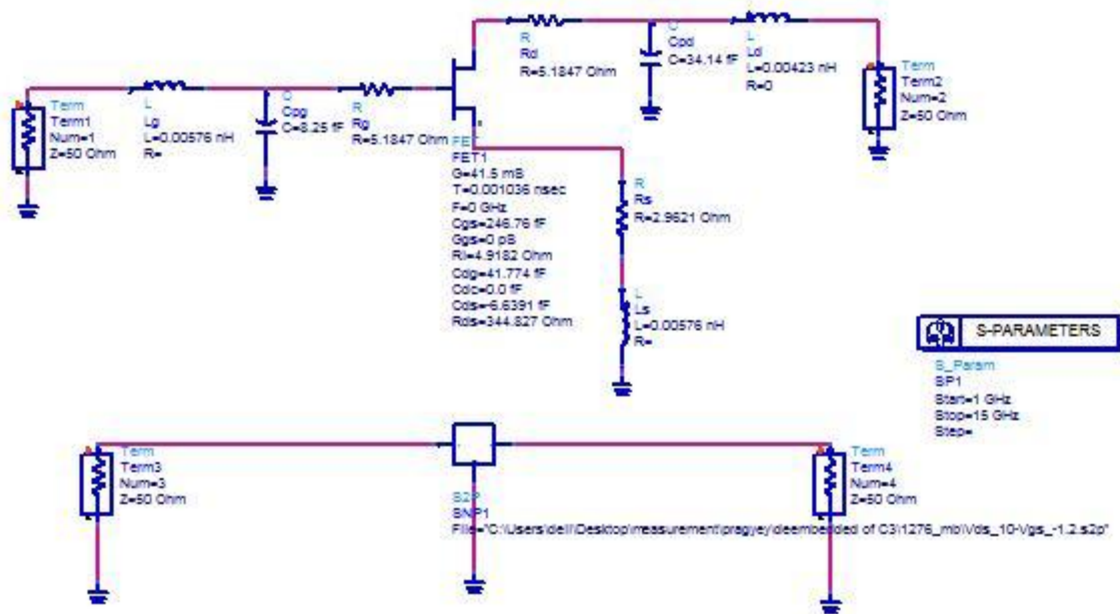
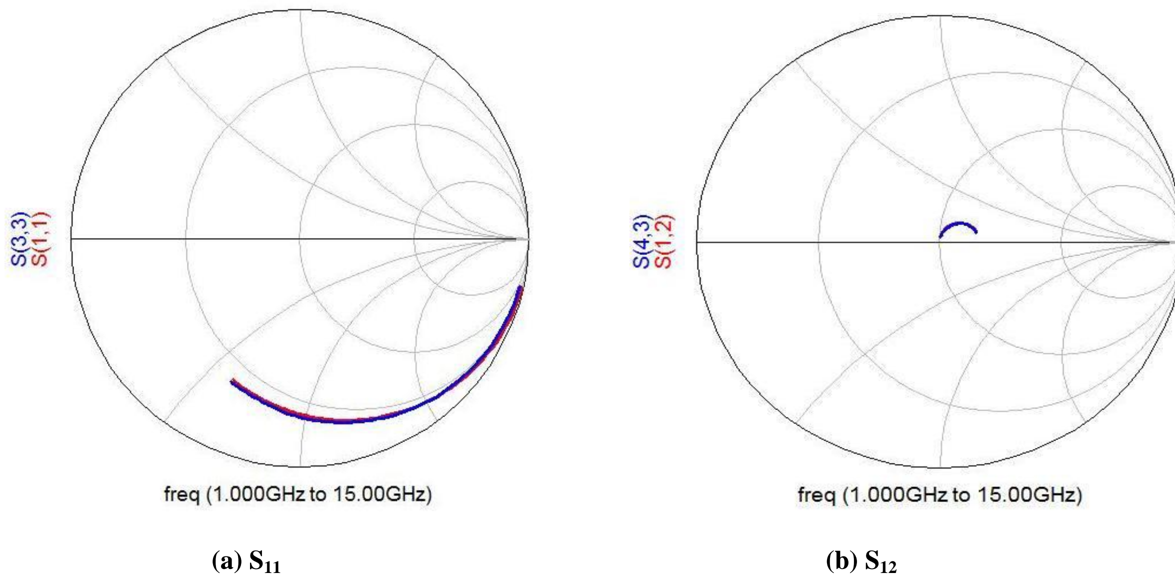
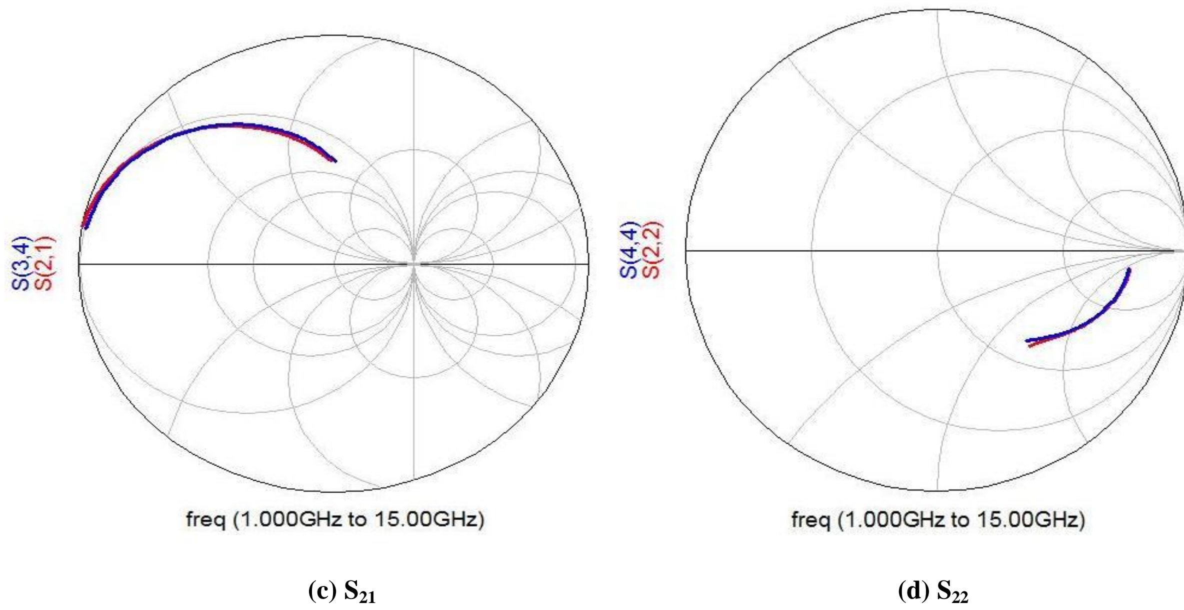


Fig. 5.10: Extracted Intrinsic parameter define and measured S-parameter called for Vd = 10V and Vg = -1.2V in ADS for 0.8× 100 µm AlGaN/GaN HEMT device.

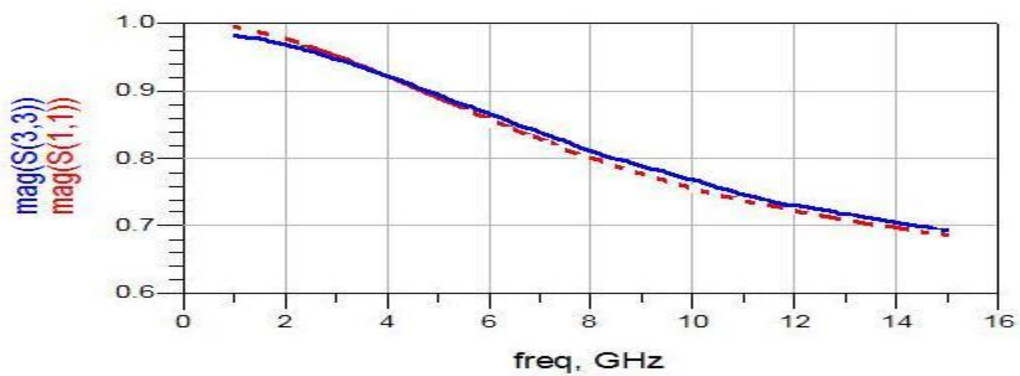


(a) $\mathbf{S_{11}}$ **(b)** $\mathbf{S_{12}}$

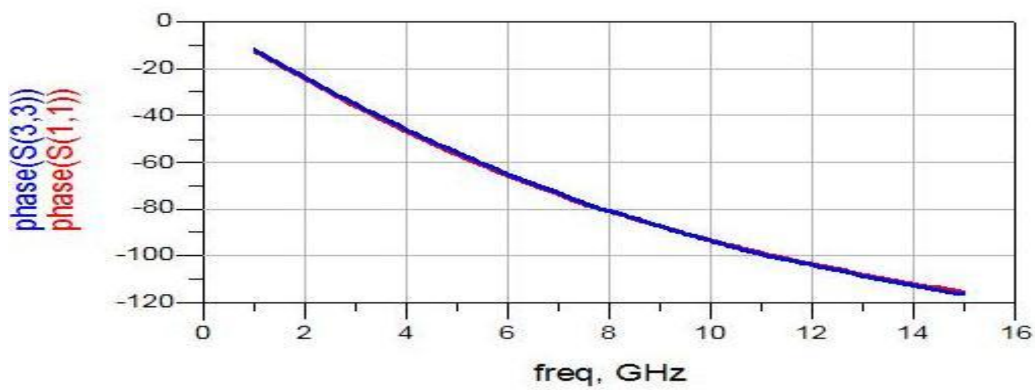


(c) S_{21} **(d) S_{22}**

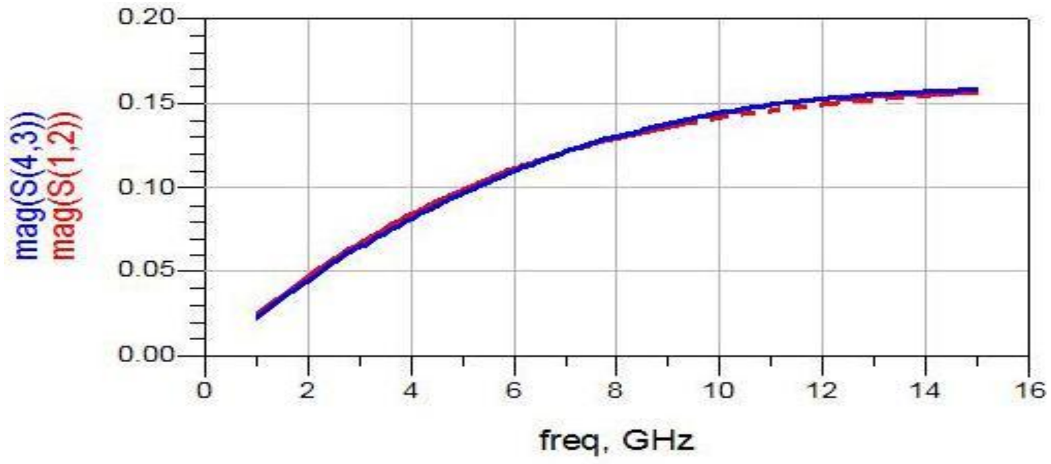
Fig. 5.11: Measured (blue line) and simulated (red line) S- parameter for Vd =10V and Vg = -1.2V of 0.8× 100 μm AlGaN/GaN HEMT device.



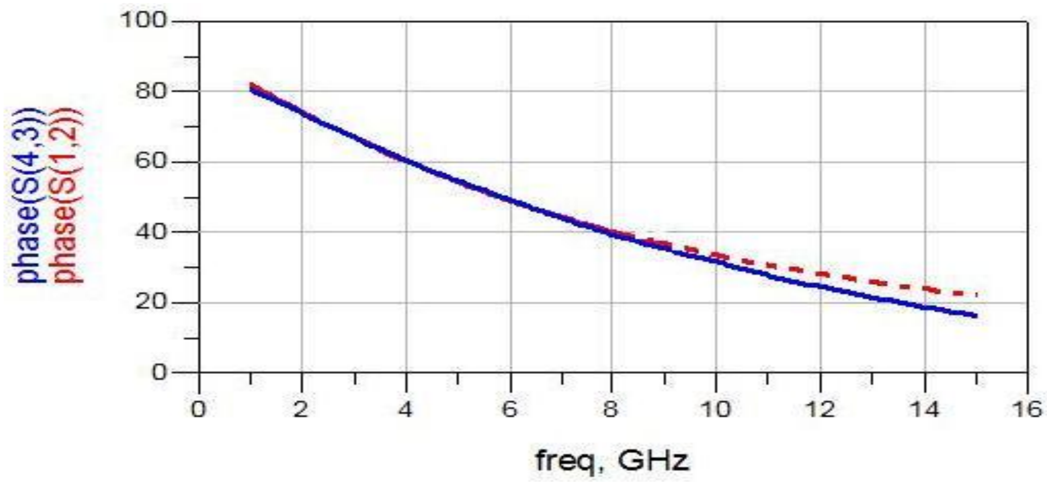
(a) Magnitude of S_{11}



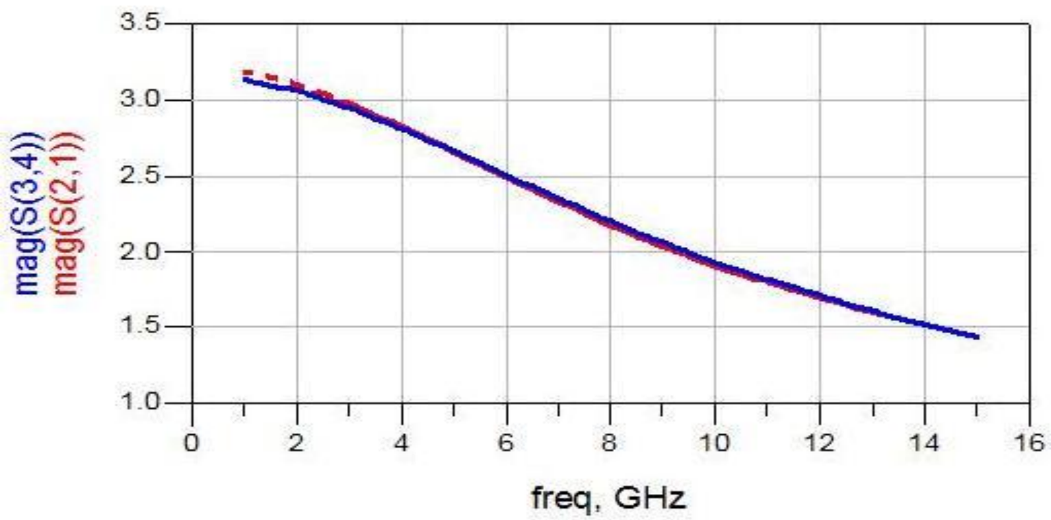
(b) Phase of S_{11}



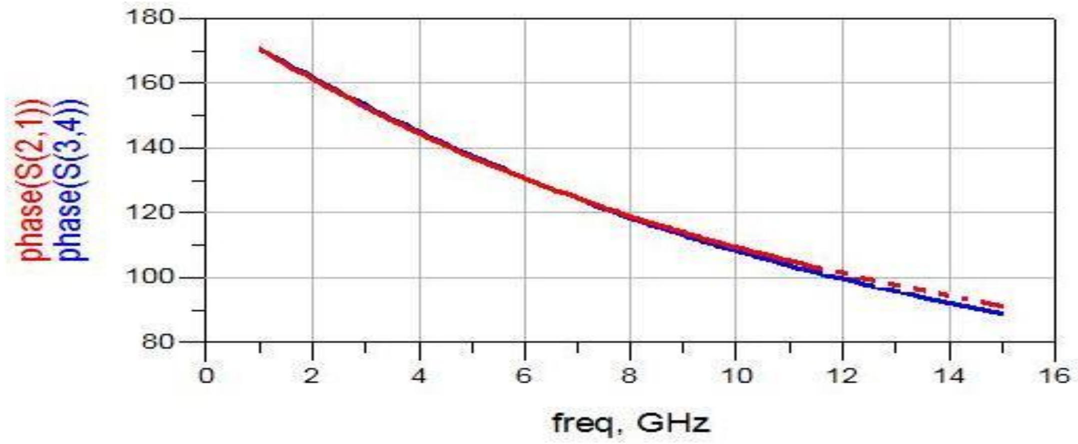
(c) Magnitude of S_{12}



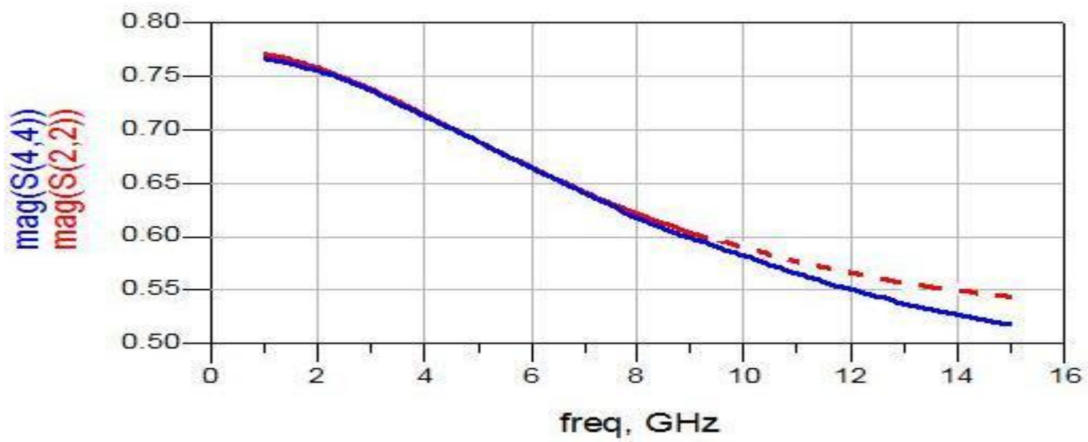
(f) Phase of S_{12}



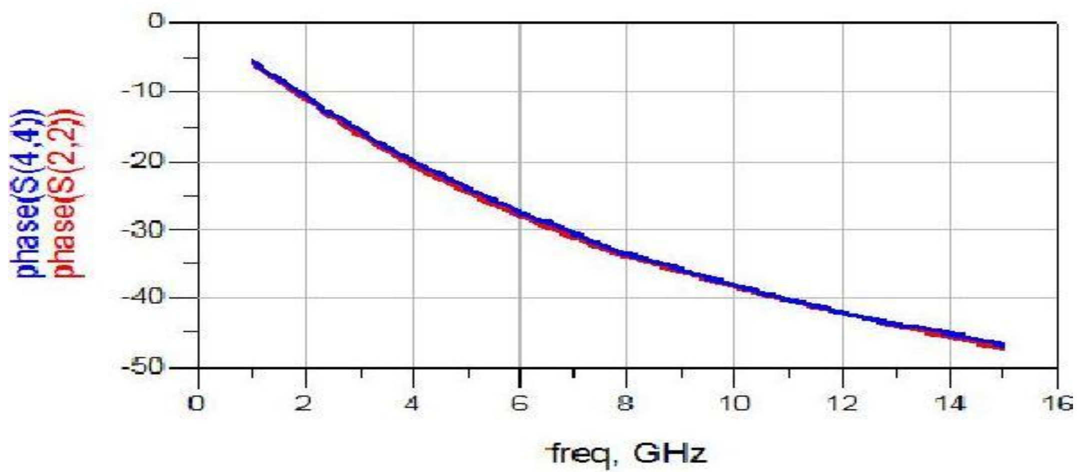
(c) Magnitude of S_{22}



(d) Phase of S_{21}

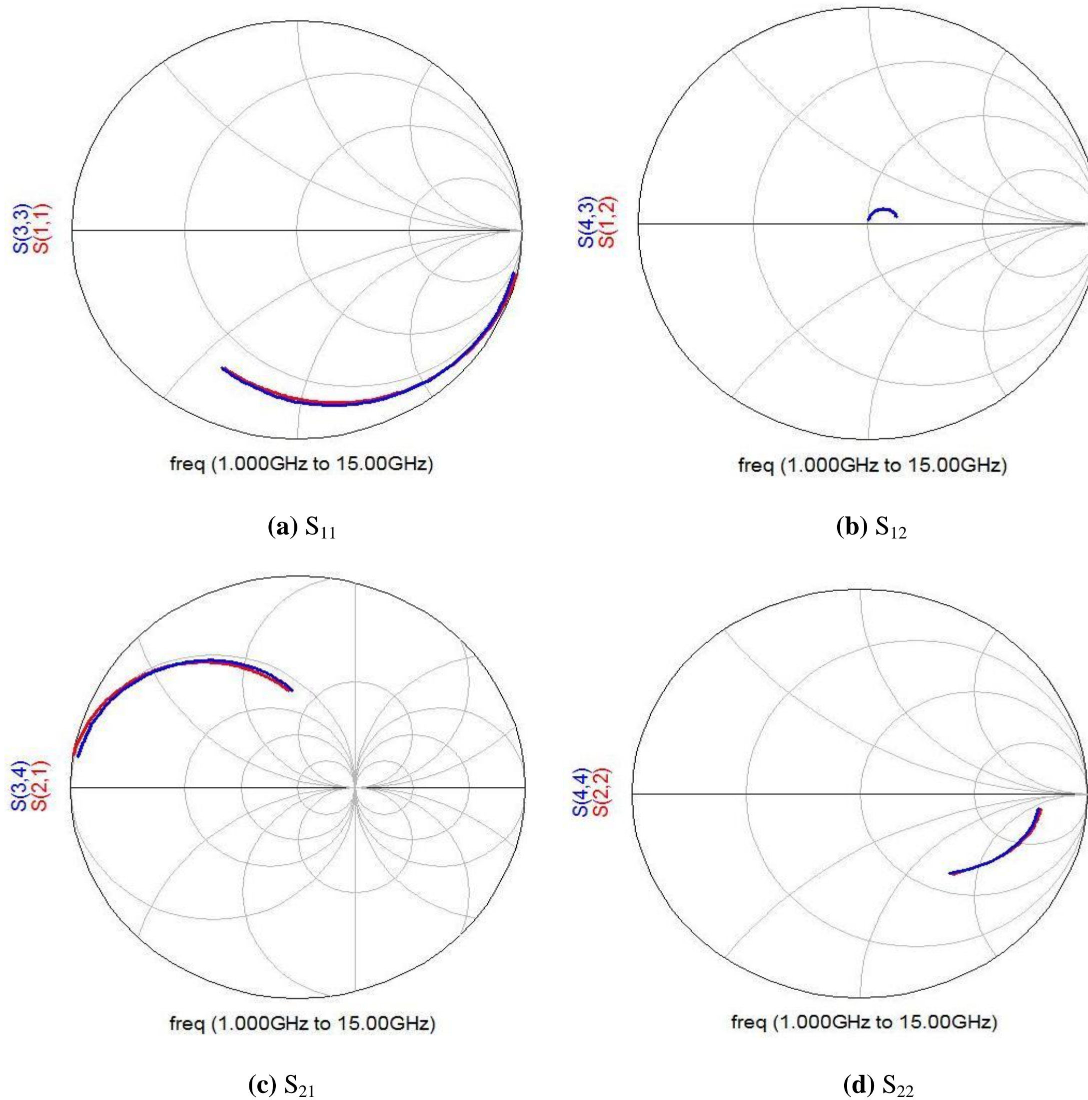


(e) Magnitude of S_{22}



(f) Phase of S_{22}

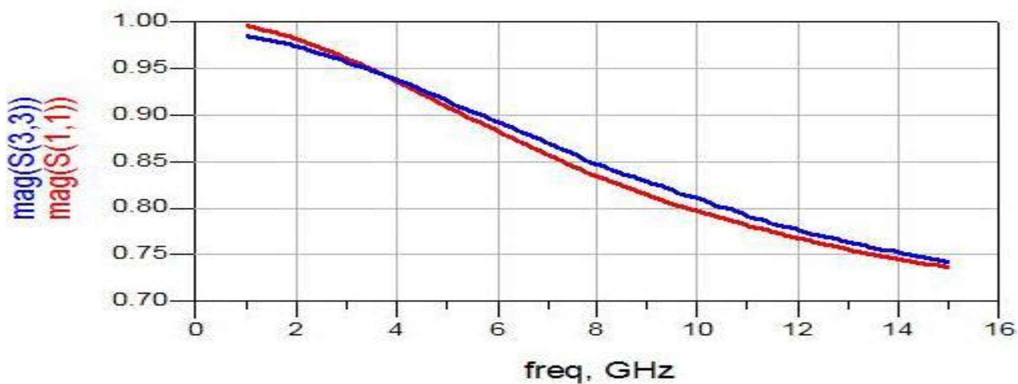
Fig. 5.12: Extraction based magnitude and phase of measured (Blue Line) and simulated (Red line) data of 0.8× 100 μm AlGaN/GaN HEMT device for Vg = -1.2 V and Vd = 10V



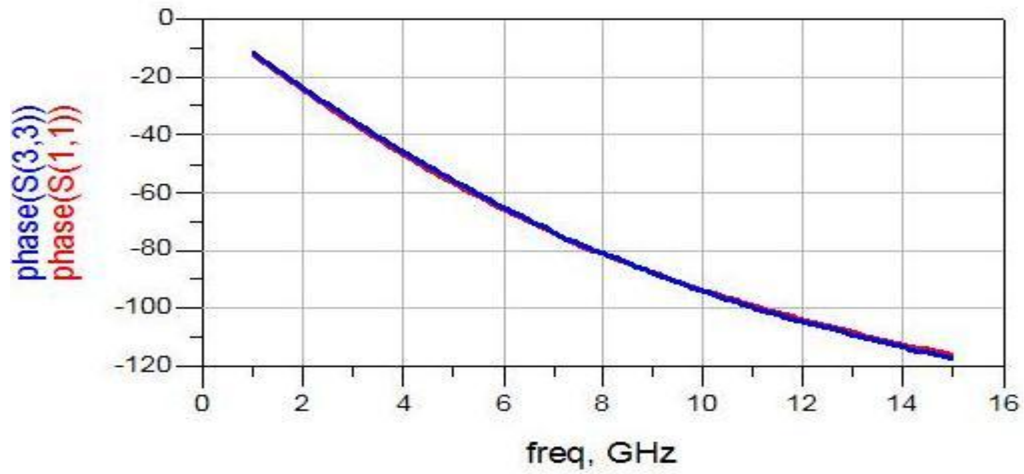
(a) S_{11} **(b)** S_{12}

(c) S_{21} **(d)** S_{22}

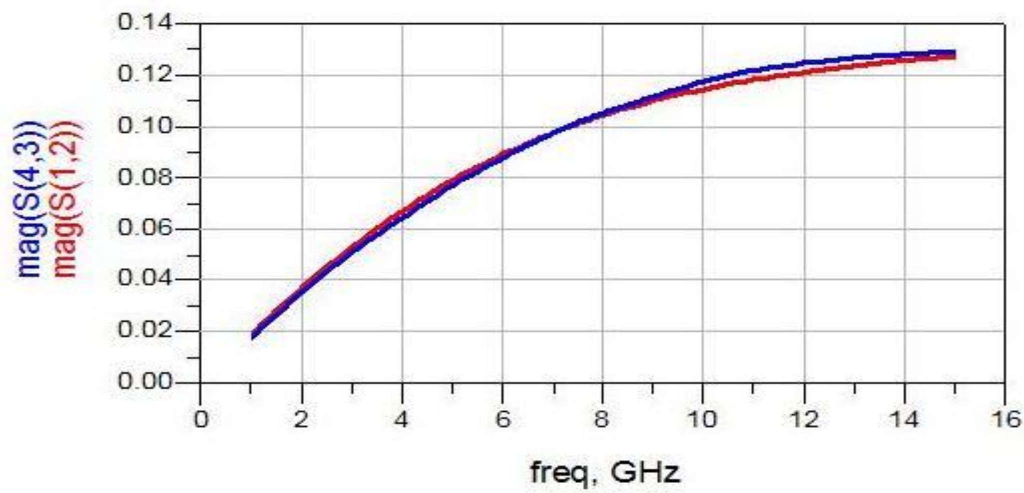
Fig. 5.13: Measured (blue line) and simulated (red line) S- parameter for Vd =10V and Vg = -3V of 0.8× 100 μm AlGaN/GaN HEMT device.



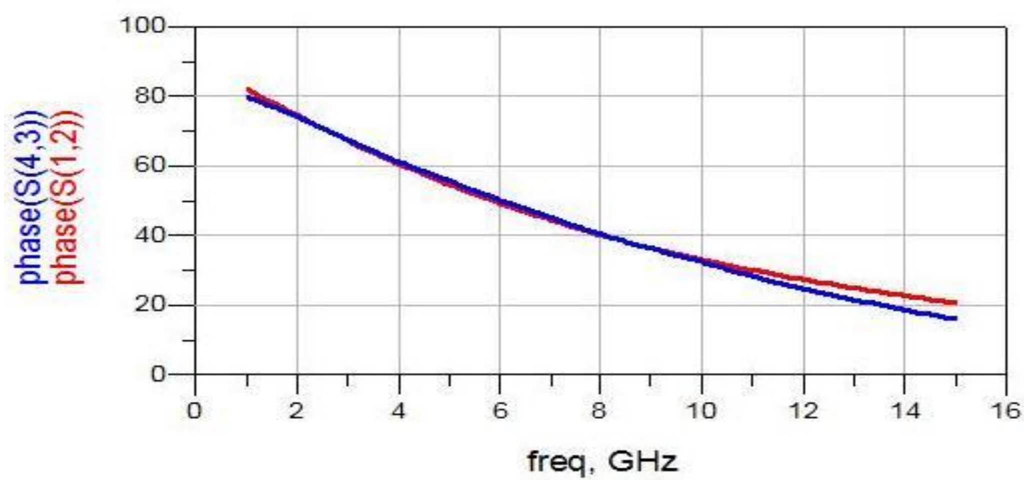
(a) Magnitude of S_{11}



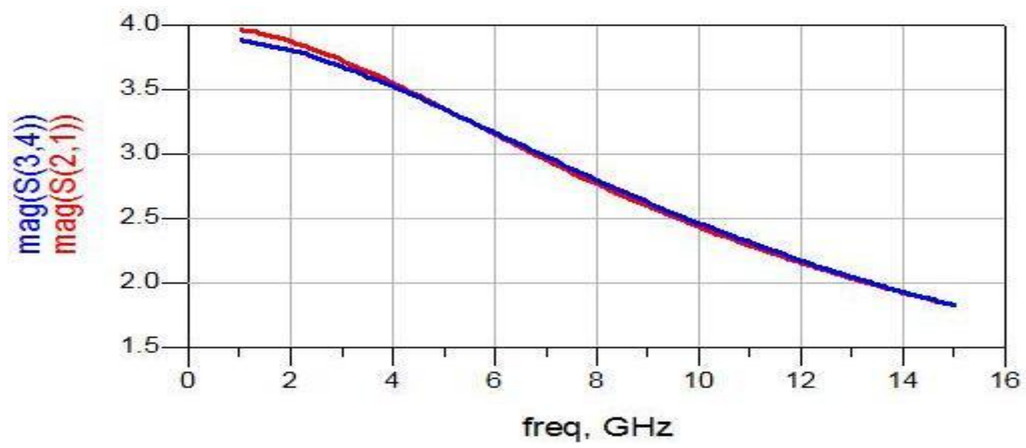
(b) Phase of S_{11}



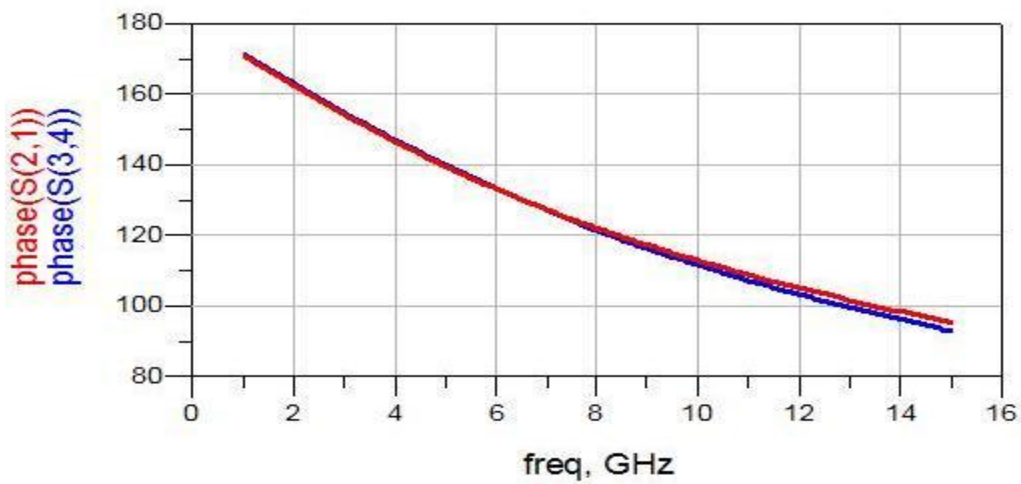
(c) Magnitude of S_{12}



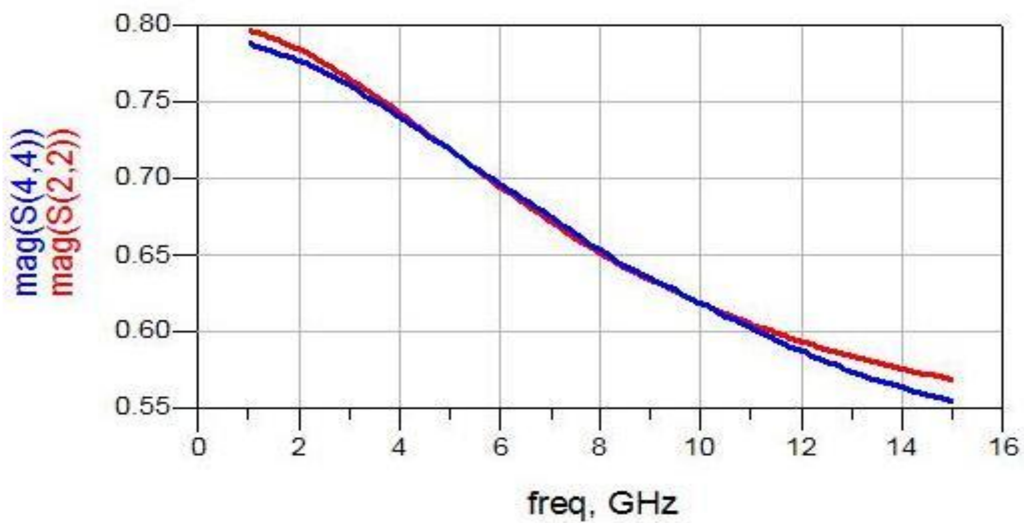
(d) Phase of S_{12}



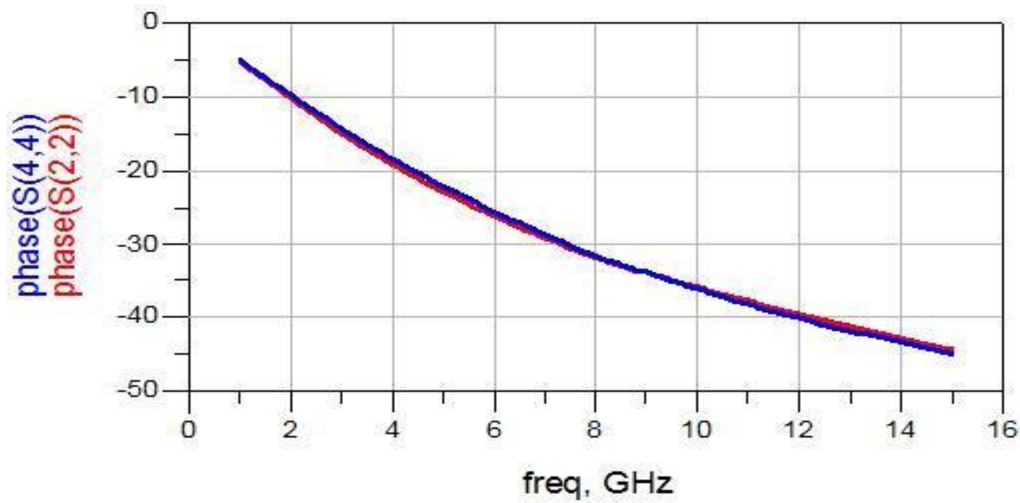
(e) Magnitude of S_{12}



(f) Phase of S_{21}



(g) Magnitude of S_{22}



(h) Phase of S_{22}

Fig. 5.14: Extraction based magnitude and phase of measured (Blue Line) and simulated (Red line) data of 0.8× 100 μm AlGaN/GaN HEMT device for Vg = -3 V and Vd = 10V

For both bias points that is Vg = -1.2 and -3 V we can see that matching between simulated and measured data which validate the mathematical model. On the behalf of calculated parameters one can say that there is quiet remarkable agreement found in between simulated result and measured data for fig. 5.11 to 5.14.

CHAPTER 6

NON-LINEAR CHARACTERISTICS PARAMETER EXTRACTION

6.1 NON - LINEARITY

Non linear model include the relationship between cause and effect of the device at the respective terminals. If the cause is done at the drain (in the form of voltage by keeping gate cause constant) then effect will be in the form of current at the drain terminal called DC IV effect. If the cause is done at gate by keeping drain cause constant then the effect will be in the form of current at the drain terminal called transfer characteristics effect. Both these effects can be model in non linear manner as the drain current is not linear function of either drain voltage or gate voltage as shown in fig 6.1.

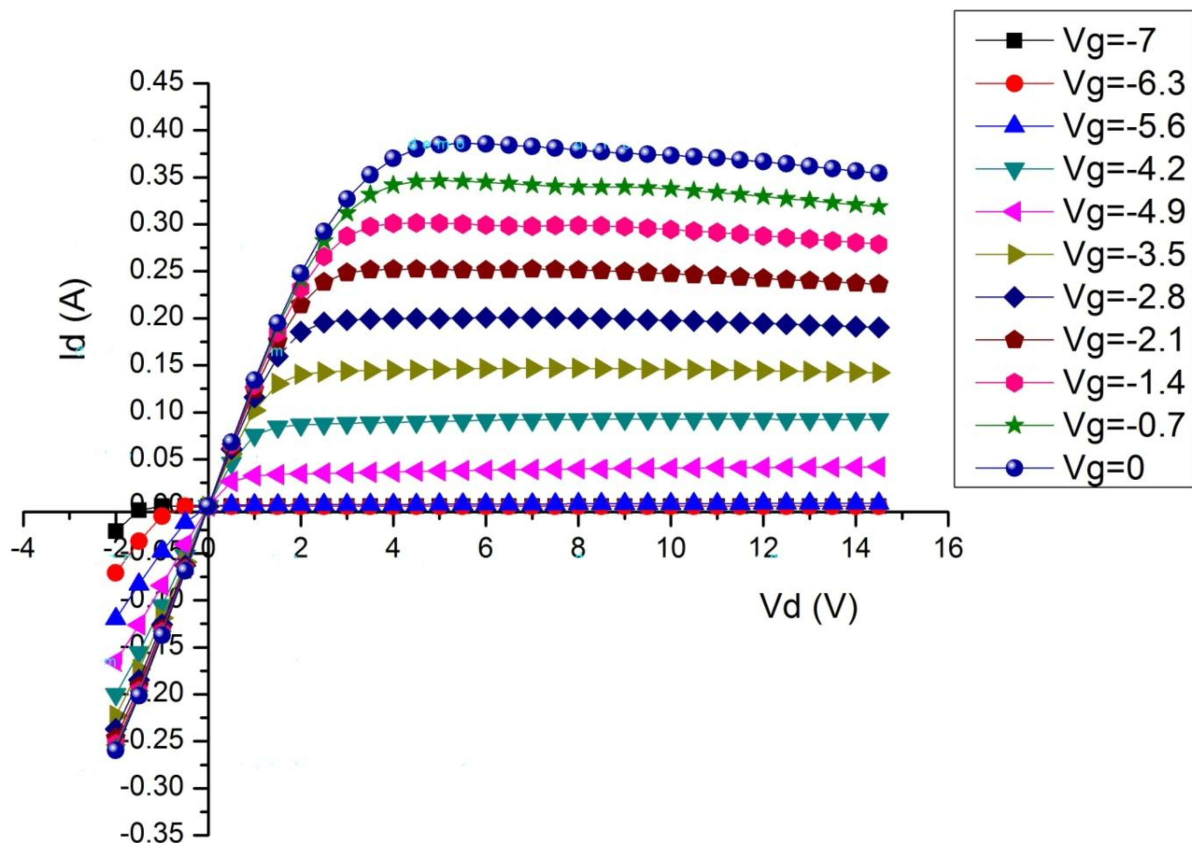


Fig. 6.1: IV characteristics of 0.8× 100 μm HEMT.

If we can analyse the fig 6.1 we can clearly see that drain current (at higher gate voltage) is linear approximately up to 3.8 V of drain voltage and similarly for different gate voltage drain current is linear up to some specific voltage. But after that specific voltage at gate terminal it get sub linear and then it get saturated. Overall we can say that drain current is nonlinear to the voltage applied to the drain terminal. Similarly for gate terminal voltage, drain current is again nonlinear

as shown in fig 6.2. In this chapter we will discuss the mathematical equation who can govern this nonlinearity.

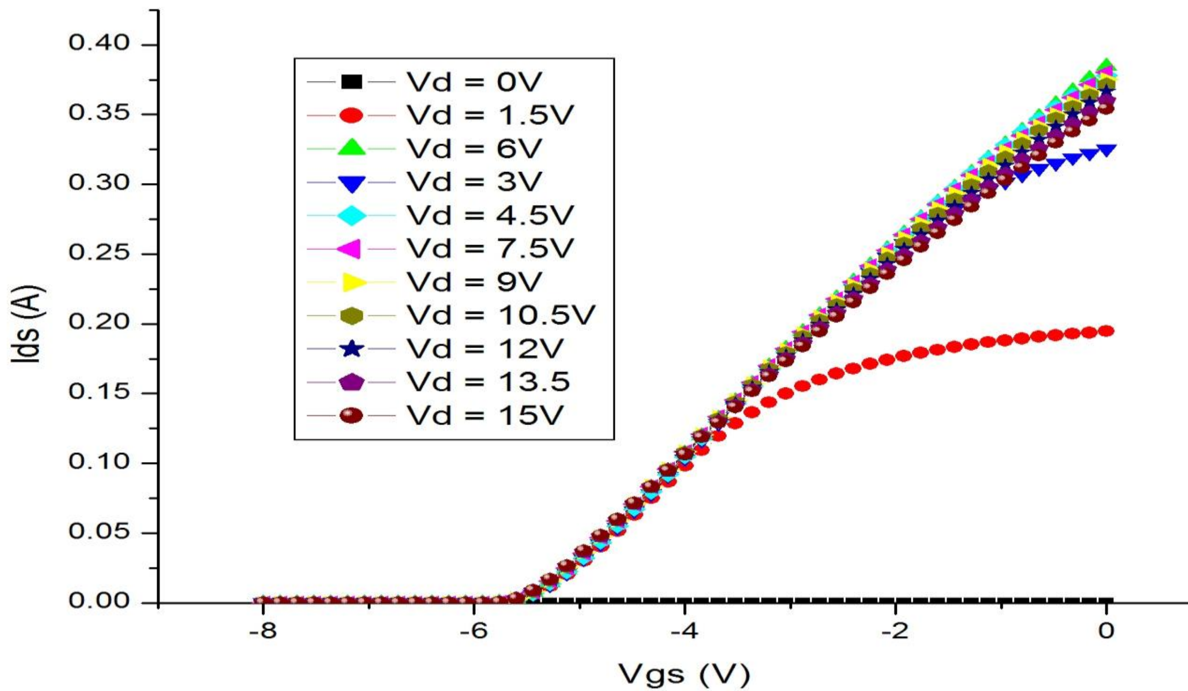


Fig. 6.2: Gate voltage verses current of $0.8\times\ 100\mu m$ HEMT device.

To create the model of these nonlinear properties of the device we use Angelov model [7-8] mainly because this model in incorporated in ADS and IC-CAP software and this model is quiet accurate also.

6.2 MODELLING OF DRAIN CURRENT

There are so many effort has been done in the past regarding nonlinear modelling of metal semiconductor field effect transistor (MESFET) and for high electron mobility transistor (HEMT) [18]. “Curtice model” was well known model in the field of MESFET modelling.“Angelov model” become more authentic model for modelling of HEMT devices [7-8,18-20]. The mathematical equation define by Angelov govern the whole nonlinearity of drain current for both dependency. There are 18 parameter will come in to the drain equation who will model the non linear phenomena. The task of this chapter in this dissertation is to calculate these parameters and then simulated result compare with measured one who validate the accuracy of mathematical model taken for the device.

6.2.1 MATHEMATICAL EQUATION OF DRAIN CURRENT MODELLING

The equation for drain current is define in "Angelov model" [8] is as below

$$I_{ds} = I_{pk}(1+\tanh(\psi))\tanh(\alpha V_{ds})(1+\lambda V_{ds}) \tag{6.1}$$

Where $$\psi = P_1(V_{gs}-V_{pk}) + P_2(V_{gs}-V_{pk}) + P_3(V_{gs}-V_{pk}).... \tag{6.2}$$

$$P_1(V_{ds}) = P_{1s}\left[1+\left(\frac{P_{10}}{P_{1s}}-1\right)\frac{1}{\cosh^2(B_2V_{ds})}\right] \tag{6.3}$$

$$B_1 = \left(\frac{P_{10}}{P_{1s}}-1\right) \tag{6.4}$$

And $$\alpha = \alpha_r + \alpha_s(1+\tanh(\psi)) \tag{6.5}$$

In equation (6.1) we see another parameter called α *and* λ which stands for variation in nonlinear graph in figure 6.1 at different bias voltage and for different current. This variation we called in mathematical language "slope of graph" at different point. There is different parameter which include into the main drain current equation I_{pk}, V_{pk}, P_1, P_2, P_3 *etc* will be discussed in subsequent paragraph.

6.2.2 MEANING OF DIFFERENT PARAMETER

6.2.2.1 Meaning of I_{pk} and V_{pk} .

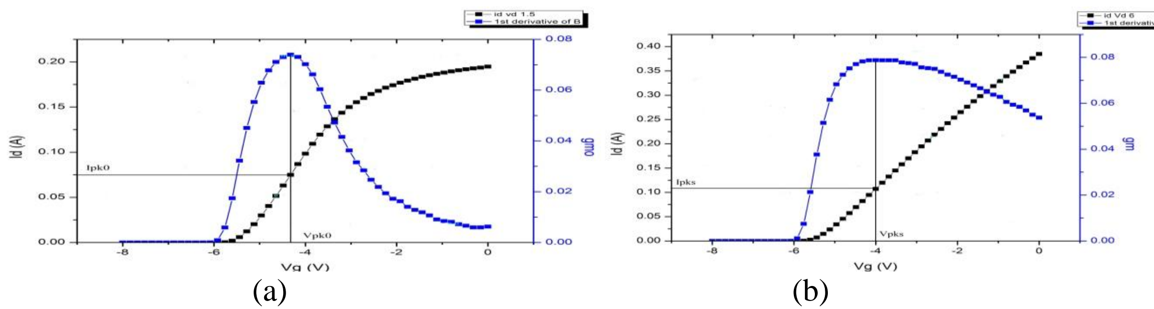


Fig. 6.3: Drain current (Ipk) and gate voltage (Vpk) at **(a)** below knee for Vd =1.5V **(b)** Beyond knee for Vd =6V (Saturation region).

In fig 6.3 I_{pk0}, V_{pk0} and I_{pks}, V_{pks} are the drain current and gate voltage at the maximum trans conduction for V_d *1.5V* and V_d *6V* respectively. Trans conductance (g_m) is the first derivative of transfer characteristics. In [8], gate voltage at maximum trans conductance define as a function of V_{ds} and ΔV_{pk}.

$$V_{pk}(V_{ds}) = V_{pko} + (V_{pks} - V_{pko})\tanh(\alpha V_{ds}) \tag{6.6}$$

The dependency of gate voltage on drain current and ΔV_{pk} is quite obvious because when we move from below knee to beyond knee, maximum trans conductance shifted but once we enter into saturation region then the maximum trans conductance get fixed so that this variation in gate voltage at maximum g_m is important key in equation 6.6. V_{pks} control the shift in I_d *Vs* V_g curve like in figure 6.4.

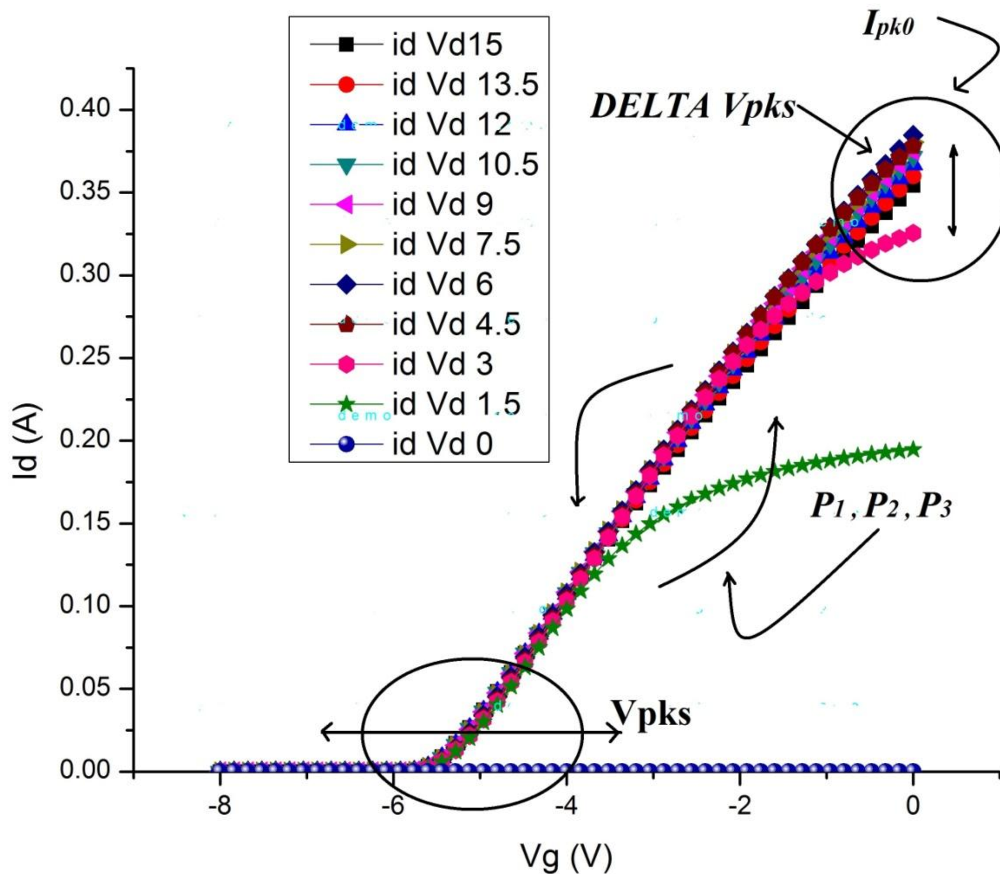
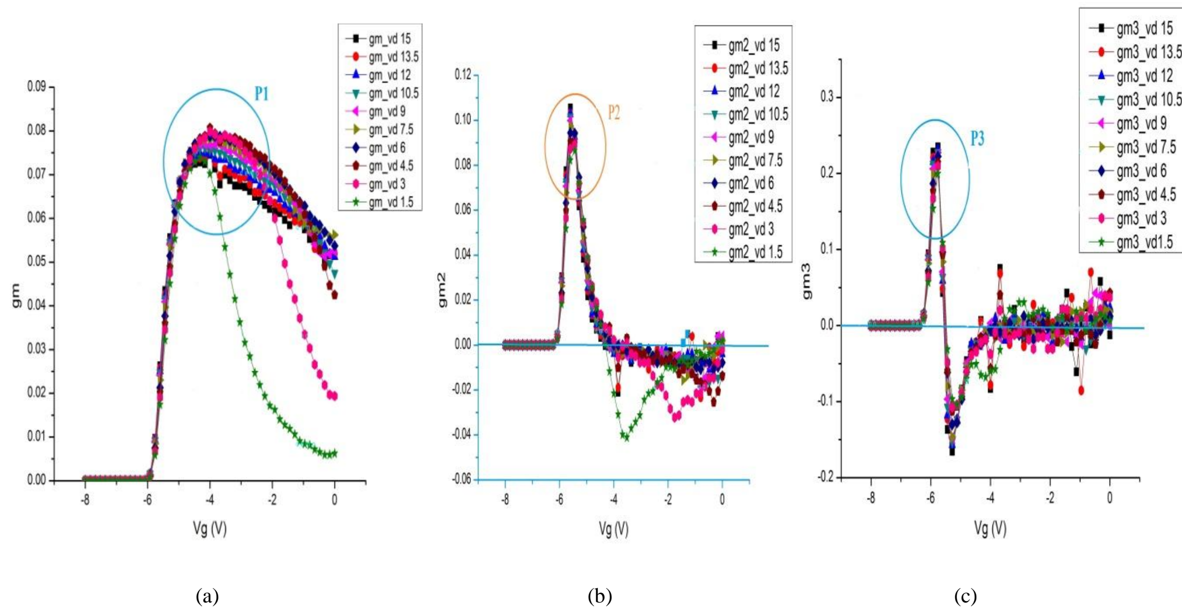


Fig. 6.4: Effect of different parameter on Ig Vs Vg curve [21].

In equation 6.2, three terms completely define the drain current verses gate voltage characteristics. If trans conductance is completely bell shaped then second and third term need not define but if trans conductance is not symmetrical then it is necessary to define second and third term. As our device having non symmetrical phenomena then it is necessary to include the second and third term. If we talk in term of effect of P_1, P_2 and P_3 then we can say that P_1 belongs to g_m, P_2 belongs to derivative of g_m called g_{m2} and P_3 belongs to derivative of g_m called g_{m3}. In short one can say that if we can define the first and second derivative of trans conductance then we are able to define the drain current and gate voltage characteristics completely.



(a) (b) (c)

Fig. 6.5: **(a)** gm Vs Vg **(b)** gm2 Vs Vg **(c)** gm3 Vs Vg, and P_1, P_2 and P_3 represent the effect region in derivatives graphs.

6.2.2.2 Meaning of α_s, α_r and λ

In I_d *Vs* V_d characteristic α_r define as slope of current of graph at lower drain voltage, in practice researchers says below knee voltage. Similarly α_s define as slope of current of graph at higher V_d, in general it is beyond voltage.

λ define in I_d *Vs* V_d characteristics as it changes complete current slope for the higher V_d. In general for V_d greater than knee voltage.

In HEMTs at higher voltage and at higher current there is self heating process get dominate and it reduce the current which turns into negative slope of I_d *Vs* V_d graph. This region of graph can be modelled by parameter R_{th} thermal resistance parameter. To find this R_{th} in this dissertation we use IC-CAP CAD tool. Although all others parameter having some mathematical feel but R_{th} find out with the help of CAD tool rather than mathematical evidence for thermal resistance parameter. There are some others parameters which we say derived parameter namely B_1 and B_2, from equation 6.4 it can observe that B_1 is some function of the region of either side of knee voltage. In the I_d *Vs* V_d curve B_1 create effect in such a way that it suppresses the current below the knee but does not having any significant change in current for drain voltage greater than knee. B_2 is approximately $1.5\ \alpha$ and it is having variation of current slowly for lower value of drain voltage and having some short of sinusoidal variation when we make B_2 higher and all this process happen at lower drain voltage, typically lower than knee voltage.

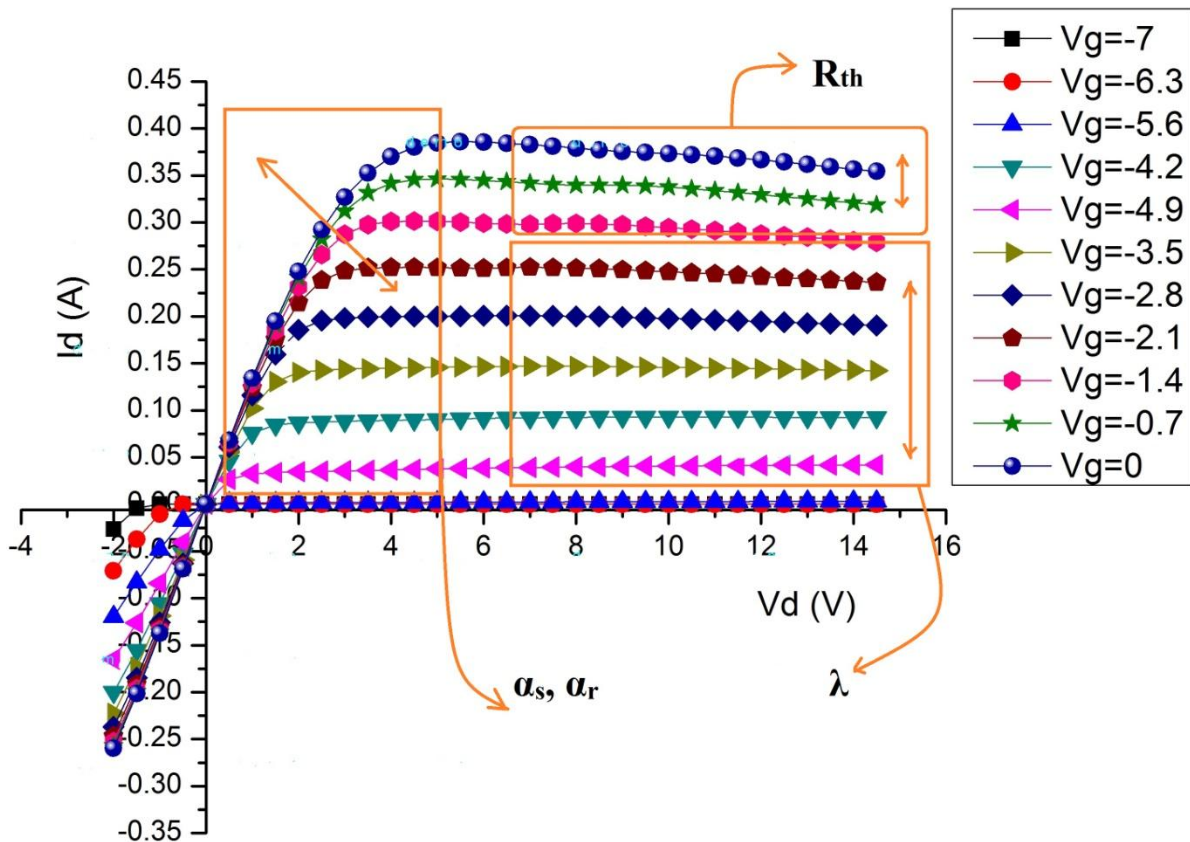


Fig. 6.6: Effect of different parameter mainly α_s, α_r, λ and R_{th} on I_d Vs V_d graph [21-22].

Linear region of I_d Vs V_d curve slop also control by another IC-CAP CAD tool parameter called R_D. ΔV_{pk} also set and control the variation in linear region.

As we have define the parameter effect in input trans conductance and on its derivative, if we can found the parameter effect on output tans conductance and on its derivative then the accuracy of simulated result based on parameter values and measured result will be with great agreement. Fig 6.7 shows the effect of parameter on output trans conductance and its derivatives.

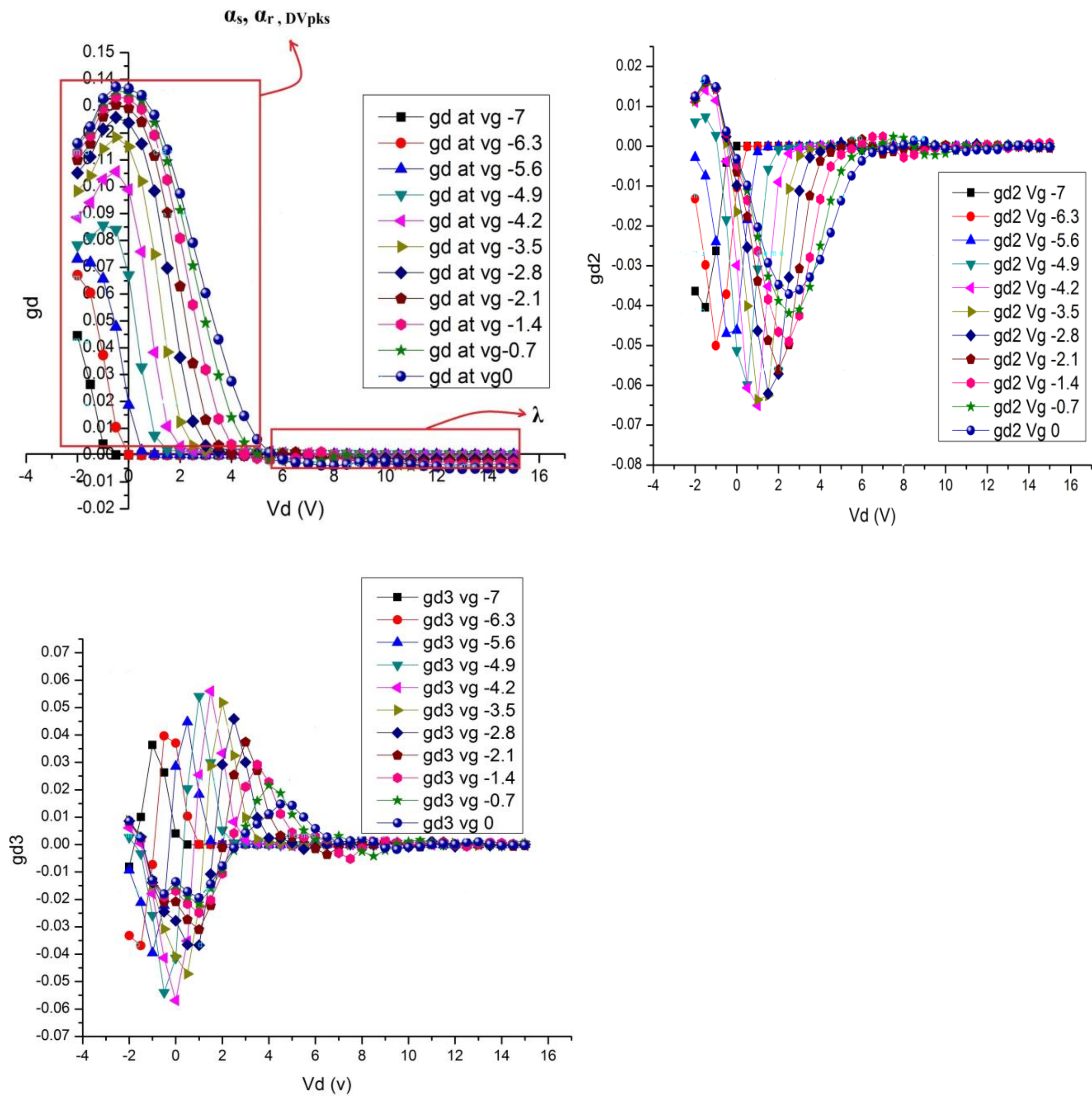


Fig. 6.7 Output trans conductance gd and its derivatives gd2 and gd3.

α_s, α_r and ΔV_{pk} change the output trans conductance below knee voltage and λ create effect after knee voltage. While doing tuning and optimization on IC-CAP CAD tool we need to be careful that if we tune or optimize any parameter for I_d Vs V_d graph, it may cause the change on trans conductance or its derivative. So while performing tuning and optimization we should be very careful.

6.3 EXTRACTED PARAMETER VALUES

After performing all essentially required step the extracted parameters for angelove model is listed in table 6.1. The meaning of non linear parameters shown in table 6.1 has been discussed in previous sections and sub sections.

Parameter	Value
I_{pk0}	0.332 A
V_{pks}	-3.596 V
ΔV_{pks}	-0.0912 V
P_1	0.3598
P_2	-0.2512
P_3	0.2138
B_1	0
B_2	0.1
λ_1	$89.13\times10^{-9} \approx 0$
λ	0.00005495
L_{vg}	$444.1\times10^{-10} \approx 0$
V_{kn}	1.035 V
R_D	0.3311 Ω
R_S	7.3110 Ω
R_{th}	0.4909 Ω

α_s	0.07656
α_r	2.128

Table 6.1: Extracted non linear parameters values for .8× 100 μm AlGaN/GaN HEMT device.

From the IC-CAP CAD tool either we can call the net list file into ADS to simulate or export .ds file to ADS. This net list file and .ds file contains all these extracted non linear parameters values which can be read by ADS. The schematic and simulation done on the basis of parameter values is given and discussed in the next section.

6.4 SIMULATION AND COMPARISON WITH MEASURED DATA

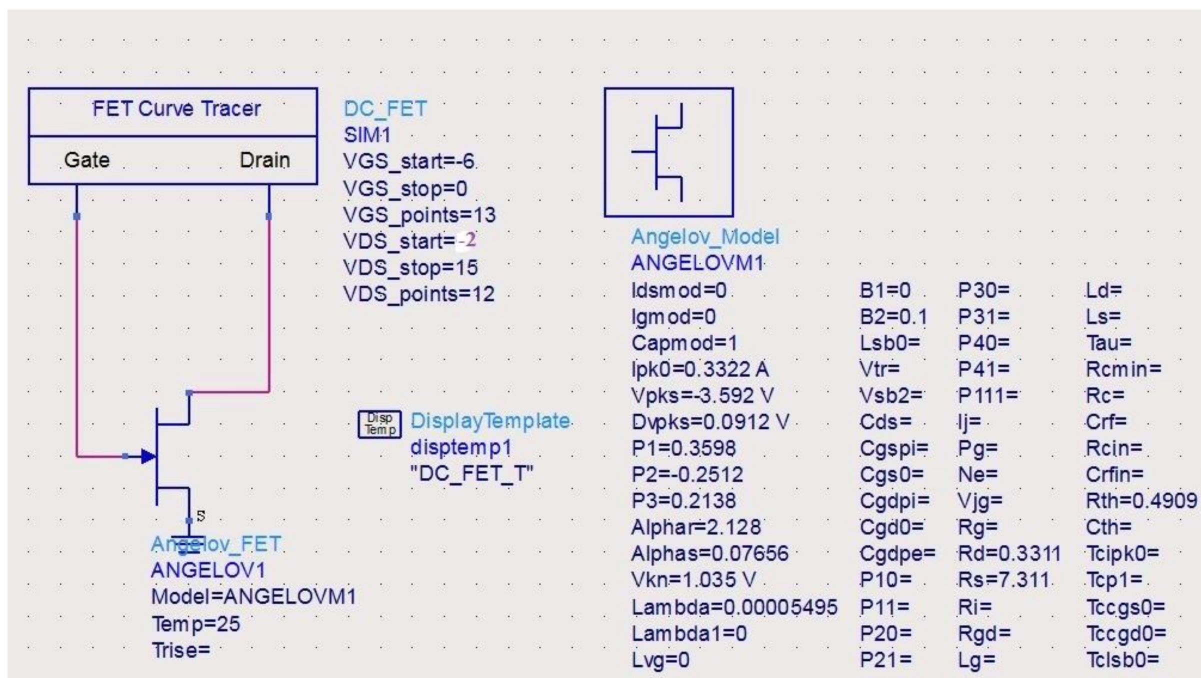


Fig.6.8: Extracted non linear parameters define in ADS for 0.8× 100 μm AlGaN/GaN HEMT device

Based on simulated result and measured data the outcome appears with great agreement (with less than 5% error in saturation region). Although the input trans conductance and output trans conductance (the first derivative of Id Vs Vg and Id Vs Vd respectively) also having good error

of less than 10% which show the mathematical beauty of angelove model which is taken in the non linear modelling. At the last in this chapter we will conclude by saying that we get that less than 5 % of error for I_d Vs V_g and I_d Vs V_d curve and less than 10 % of error for I_d Vs V_g and I_d Vs V_d curves derivatives. This whole procedure validates the accuracy of measurement and modelling.

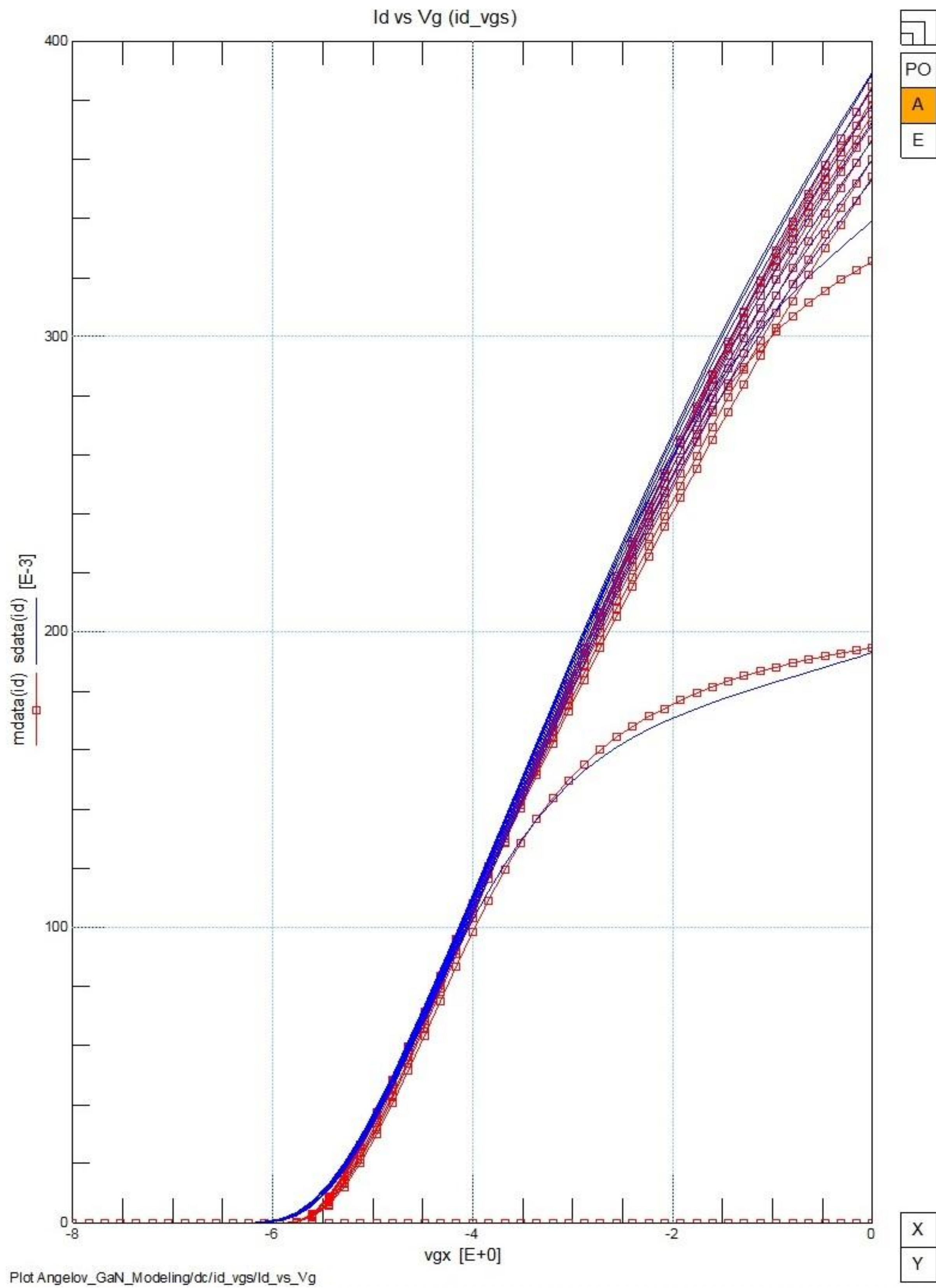
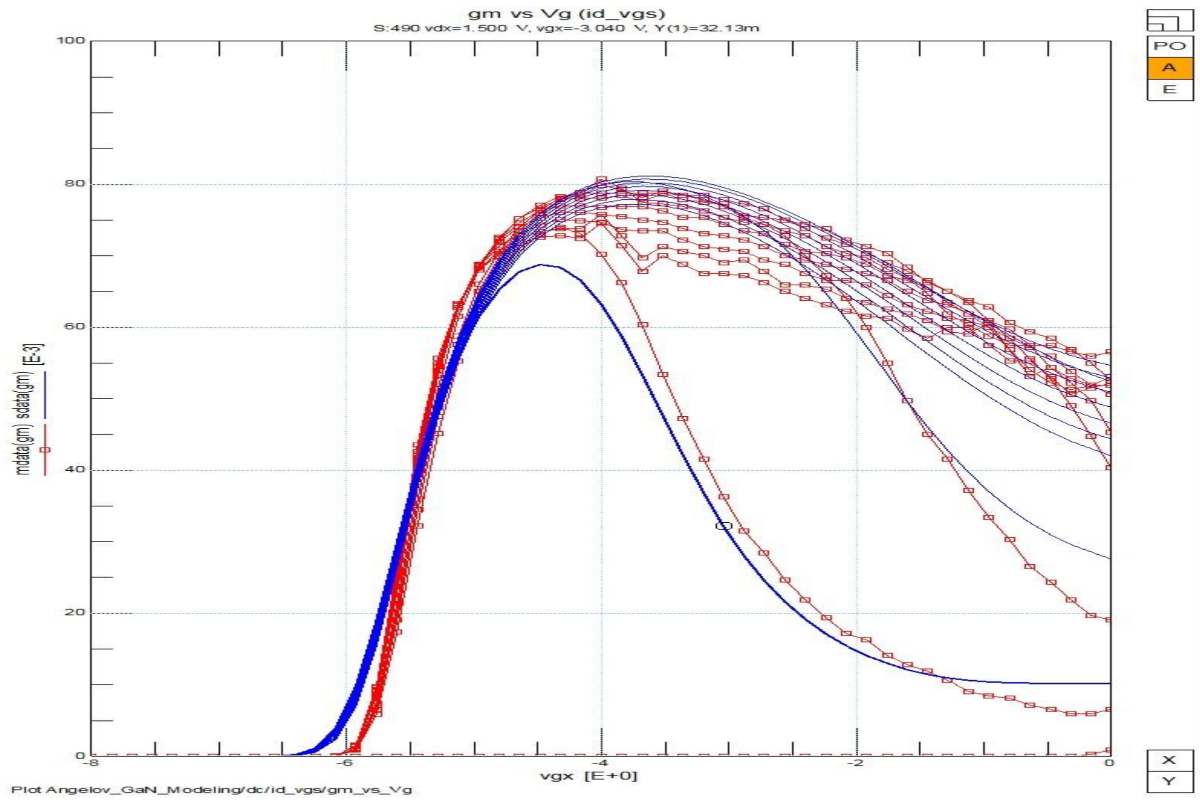
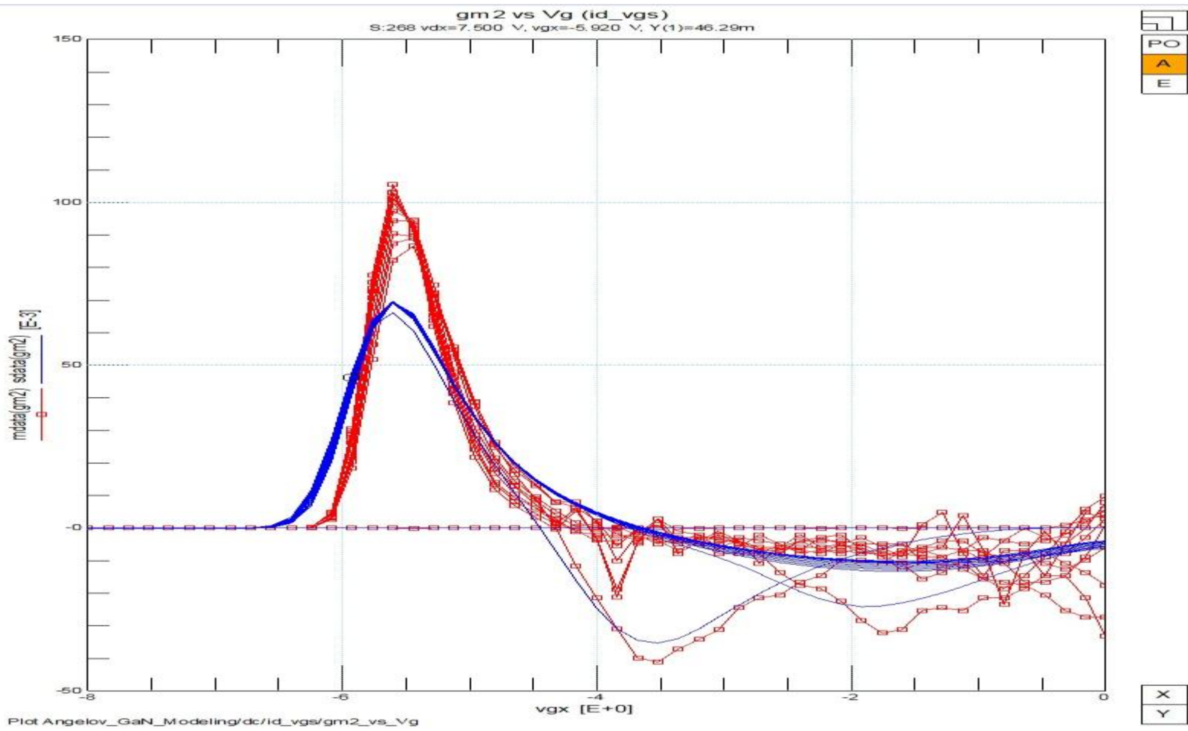


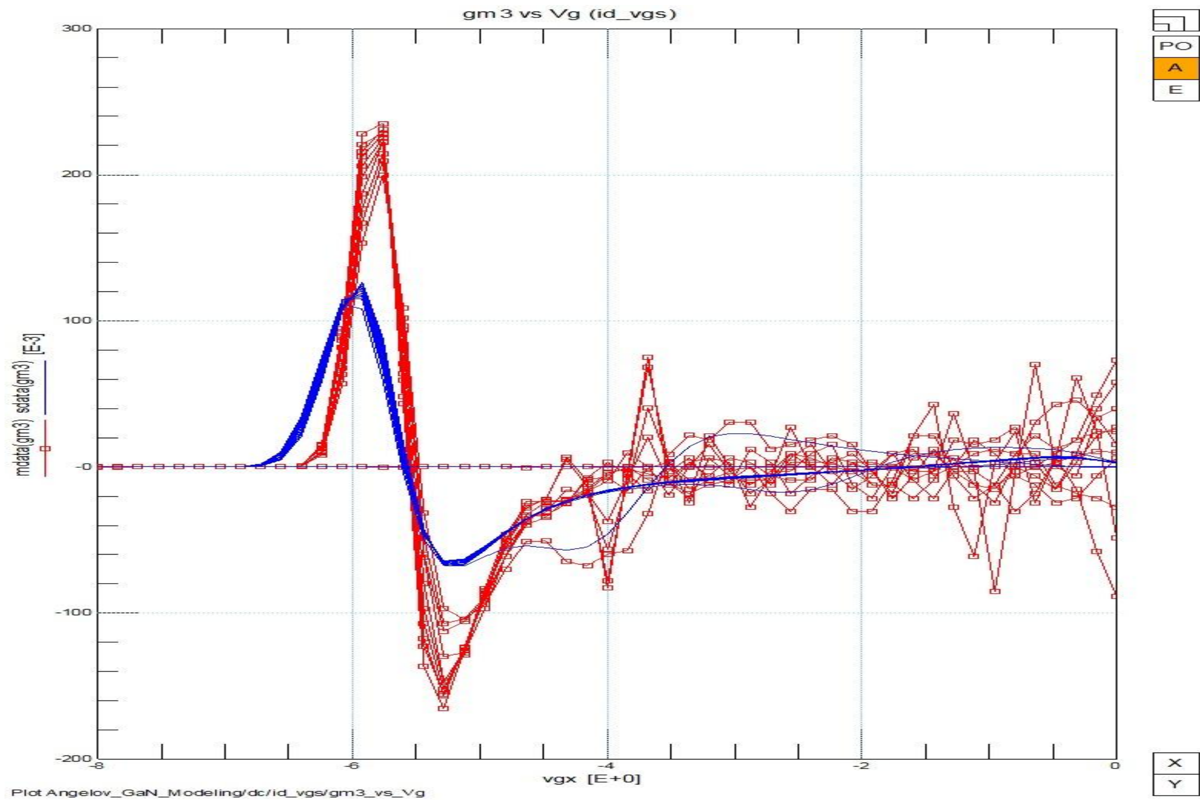
Fig. 6.9: Simulated (Blue line) and measured (Red line) Id Vs Vg curve.



(a) g_m



(b) g_{m2}



(c) g_{m2}

Fig. 6.10: Simulated (Blue line) and measured (Red line) of **(a) g_m (b) g_{m1} (c) g_{m2}.**

As we can see here that the derivatives (First (g_m), second (g_{m2}), third derivative (g_{m3})) of Id Vs Vg also having good agreement between simulated and measured data, which shows that models mathematical ability and accuracy. As we have extracted 17 non linear parameters and there is very good matching occurs. The second and third derivatives need to fallow the measured data.

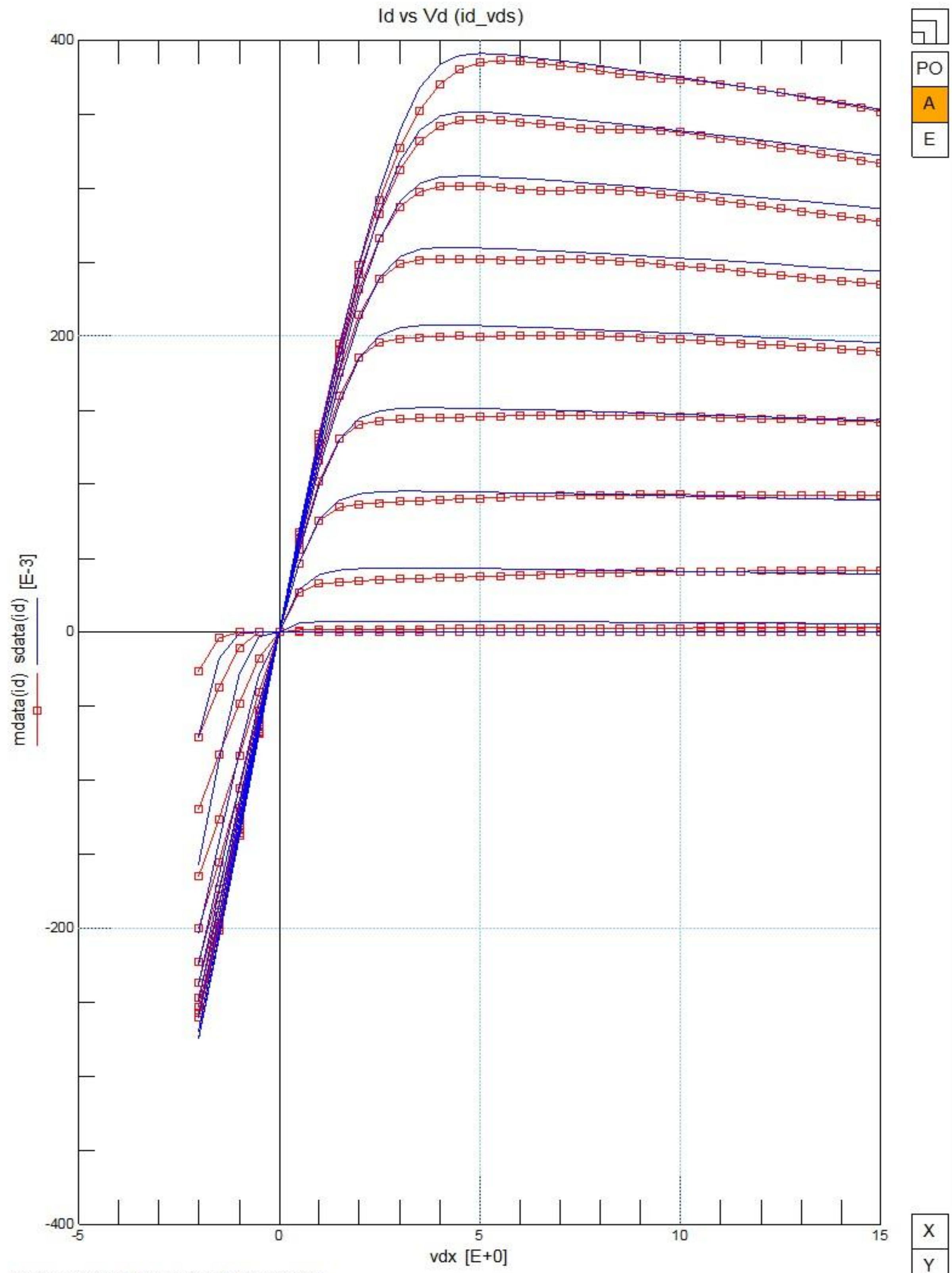
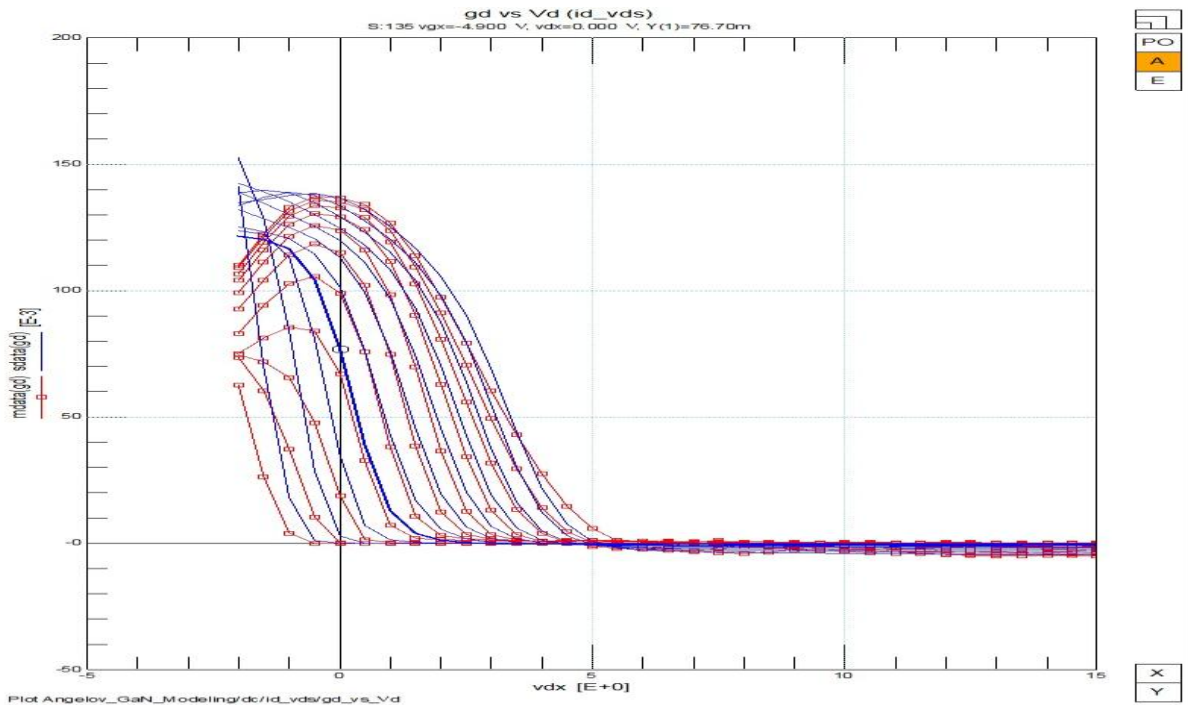
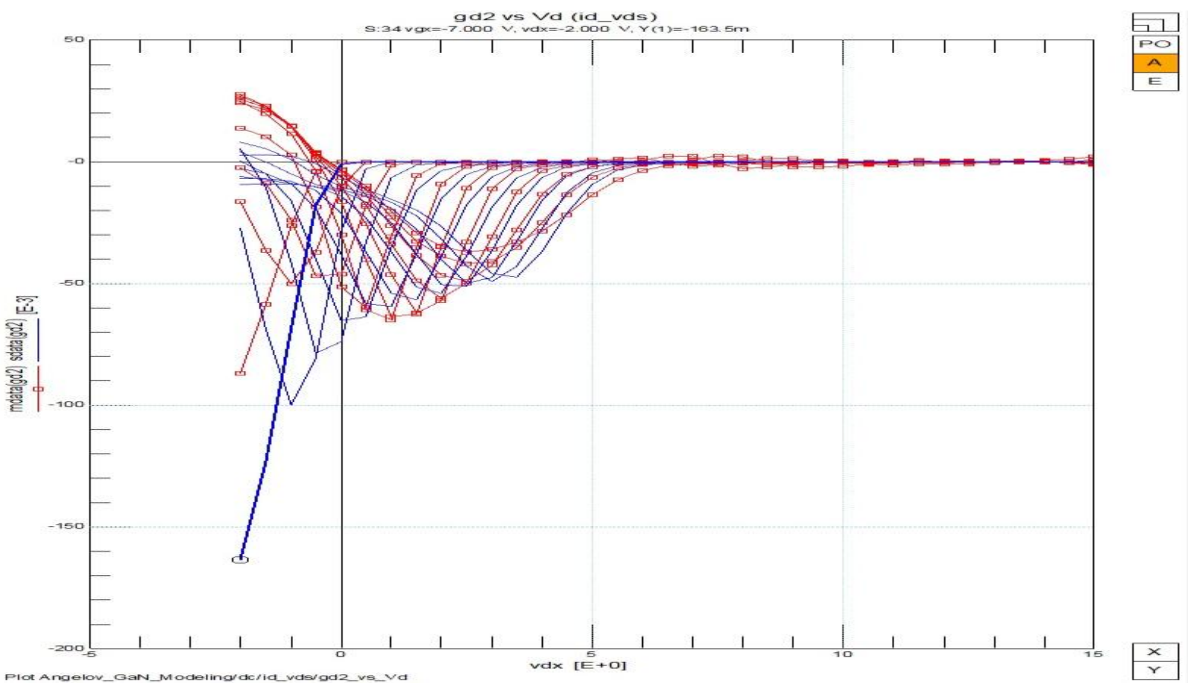


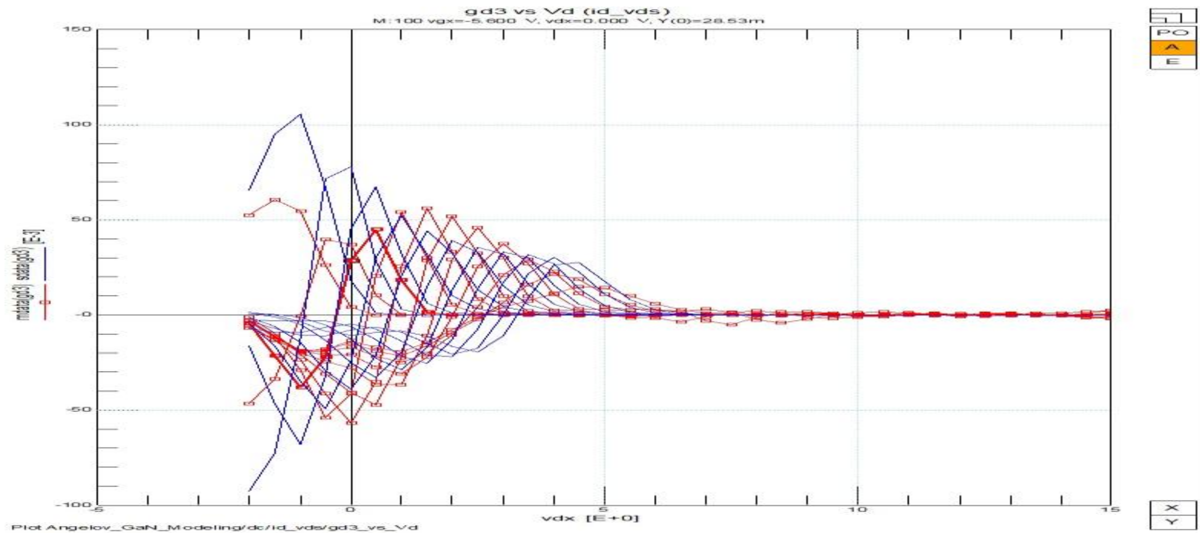
Fig. 6.11: Simulated (Blue line) and measured (Red line) Id Vs Vd curve.



(a) g_d



(b) g_{d1}



(c) g_{d2}

Fig.6.12 Simulated (Blue line) and measured (Red line) of **(a)** $\mathbf{g_d}$ **(b)** $\mathbf{g_{d1}}$ **(c)** $\mathbf{g_{d2}}$

In fig 6.11 we take Vd value from -2V to 15 V. As taking negative value of Vd turn it easy to model the linear region. Mathematical equations find the suitable trend and also correct slop correspondingly of linear region and model it accurately. Fig 6.12 show he modelling of output trans conductance and up to its second derivative. As we have done the modelling up to third derivative of I_d Vs V_g and I_d Vs V_d then suitability of mathematical model is much more accurate because its deal with how the change will occur in I_d Vs V_g and I_d Vs V_d curve. In fig 6.9 to 6.12 it can easily say that the simulated result follow correctly the measured data which also validate the data measurement accuracy as well as modelling procedure.

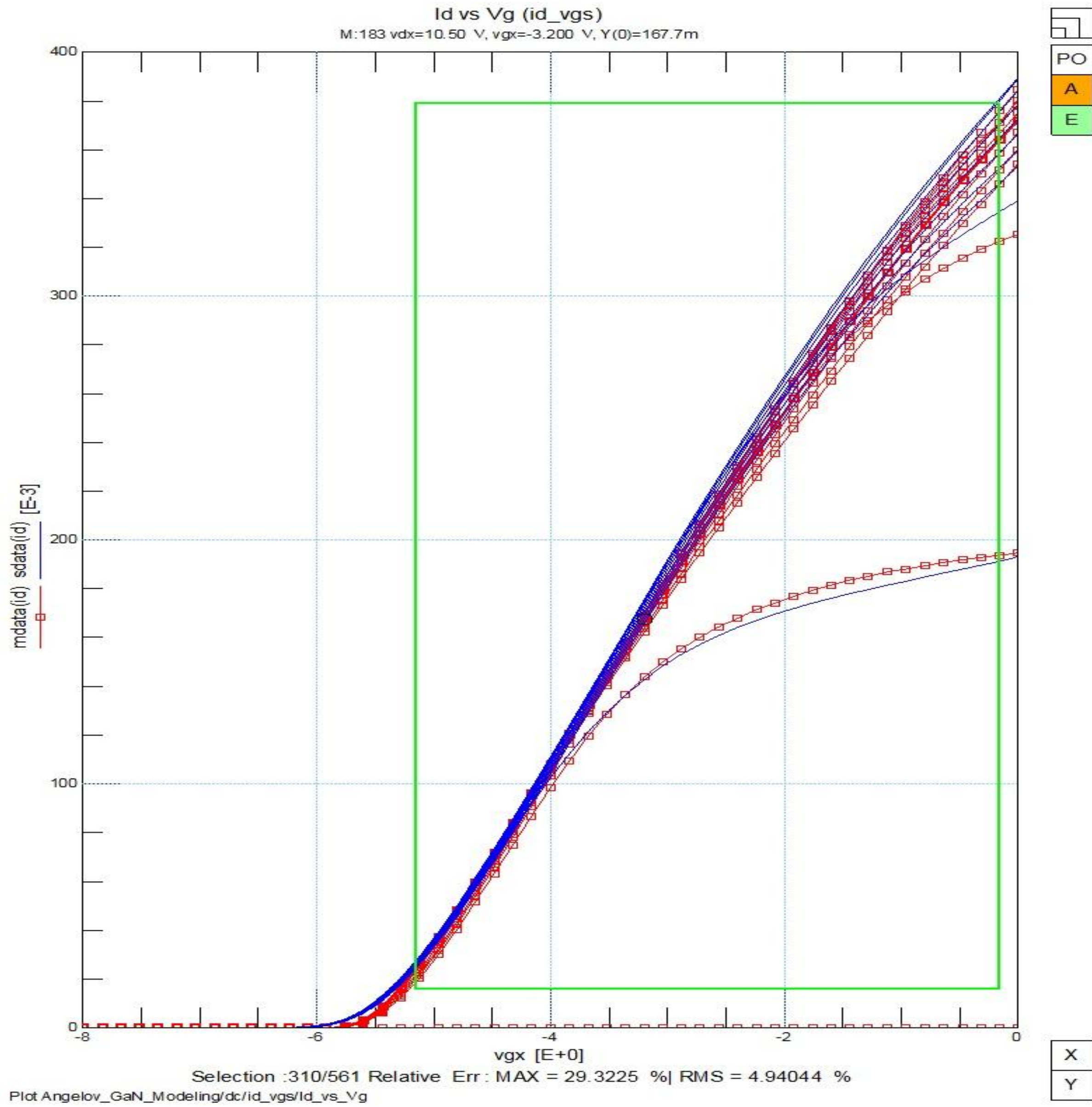


Fig.6.13 Operated region of Id Vs Vg curve show the error of only 4.94044 % only.

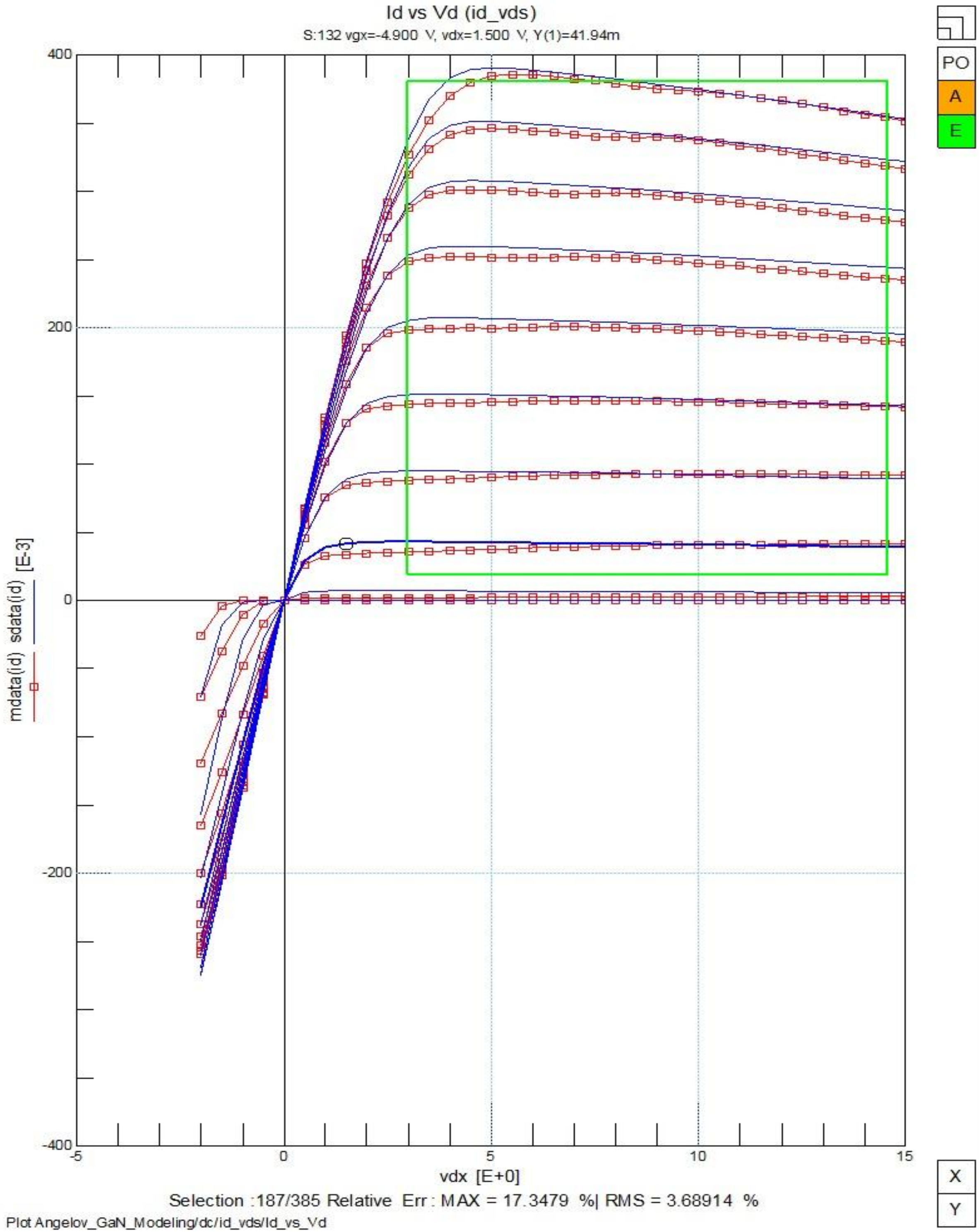
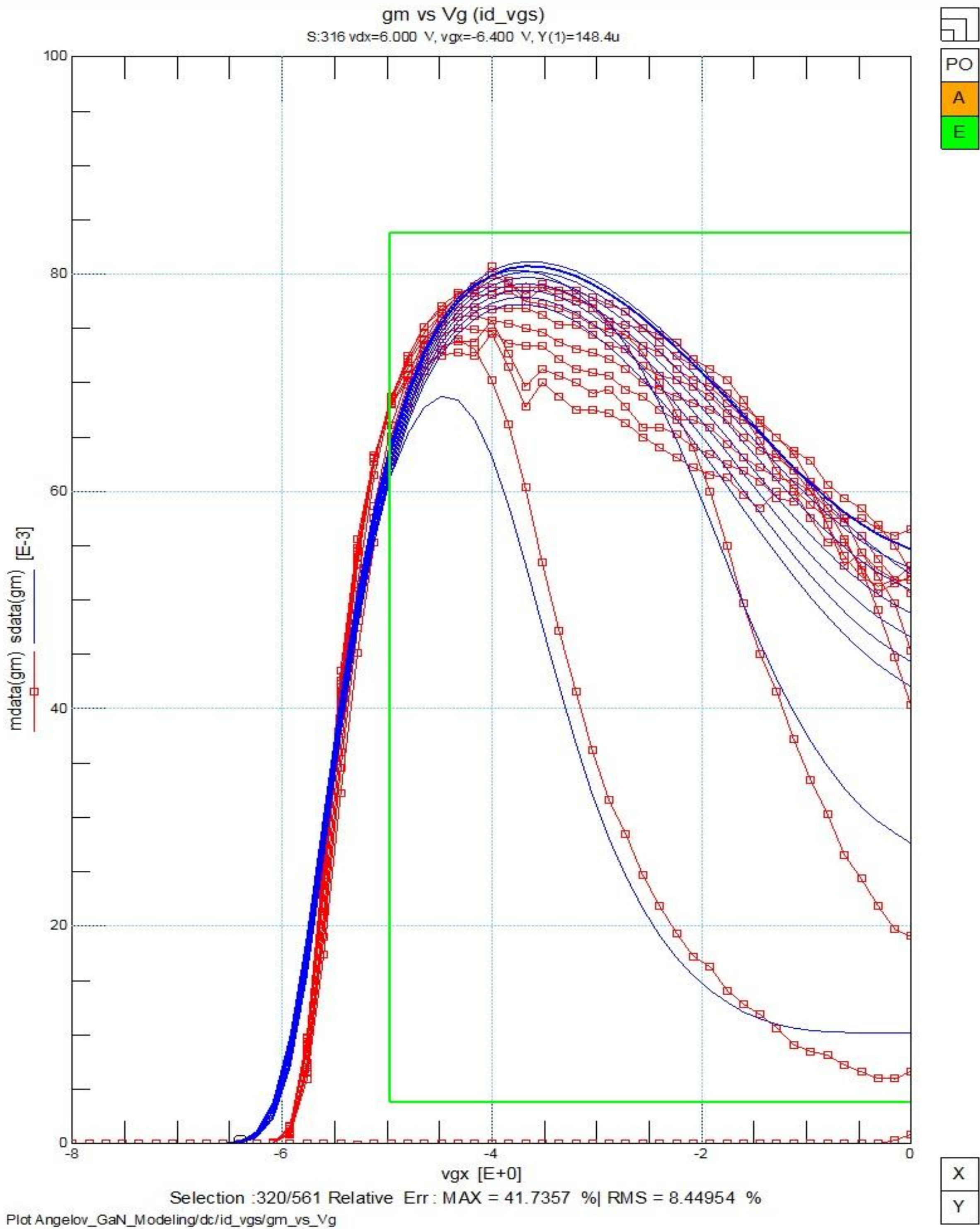
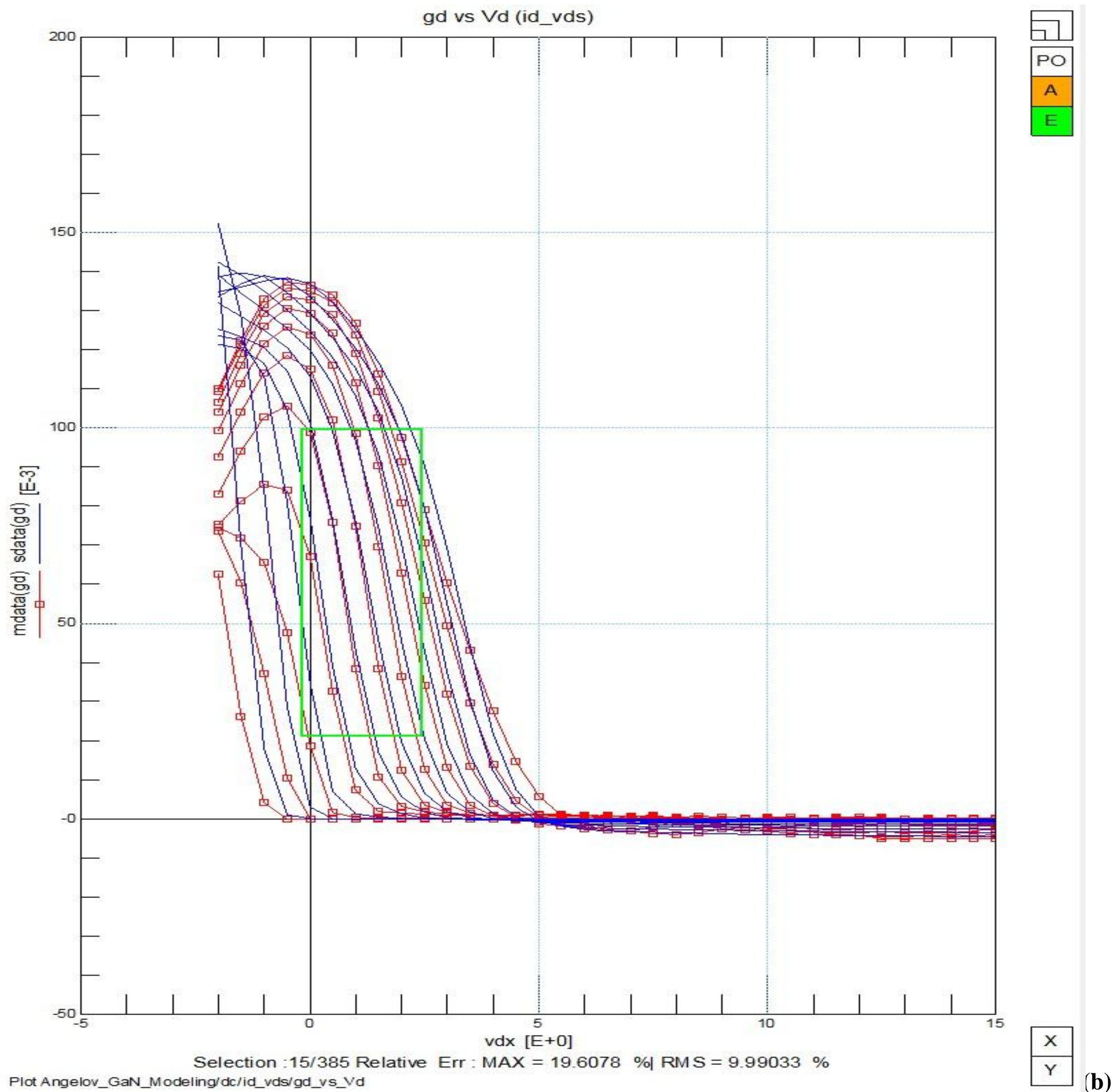


Fig. 6.14 Operated region of I_d Vs V_d curve show the error of only 3.68914 % only.

The yellow region of I_d Vs V_g and I_d Vs V_d curve show the error of 4.94044 % and 3.68914 % only. The yellow region show the saturation region where device operated most of the time as an amplifier. So that accuracy of this region is important in non linear modelling process.



(a) gm having the accuracy of around less than 9 % of error.



(b)

$\mathbf{g_d}$ having the accuracy of around less than 10 % of error.

Fig. 6.15 Input and output trans conductance accuracy (a) less than 9 % of error (b) less than 10 % of error.

Fig 6.15 shows the accuracy of derivative of I_d Vs V_g and I_d Vs V_d curve. We find the error of less than 9 % for input tans conductance and less than 10 % for output trans conductance which is very good matching for first derivative also.

Finally we get that less than 5 % of error for I_d Vs V_g and I_d Vs V_d curve and less than 10 % of error for I_d Vs V_g and I_d Vs V_d curves derivatives. This whole procedure validates the accuracy of measurement and modelling.

CHAPTER 7

CONCLUSION AND FUTURE WORK

This dissertation contains linear as well as non linear DC modelling approach. The good agreement found between simulated results based on extracted parameter and the measured data. This matching would not become possible without proper measurement process and without perfect modelling approach. We have also seen that there is key thing in model parameter extraction called de-embedding process which removes parasitic phenomena in the device. Without de-embedding there will be off set in the result found.

Curve fitting, optimization and tuning were the key factor in parameter extraction. Curve fitting done in matlab and optimization and tuning done in IC-CAP CAD tool which turns into better result in parameter extraction. In this dissertation we use eight transaction paper which show the level of work of this dissertation.

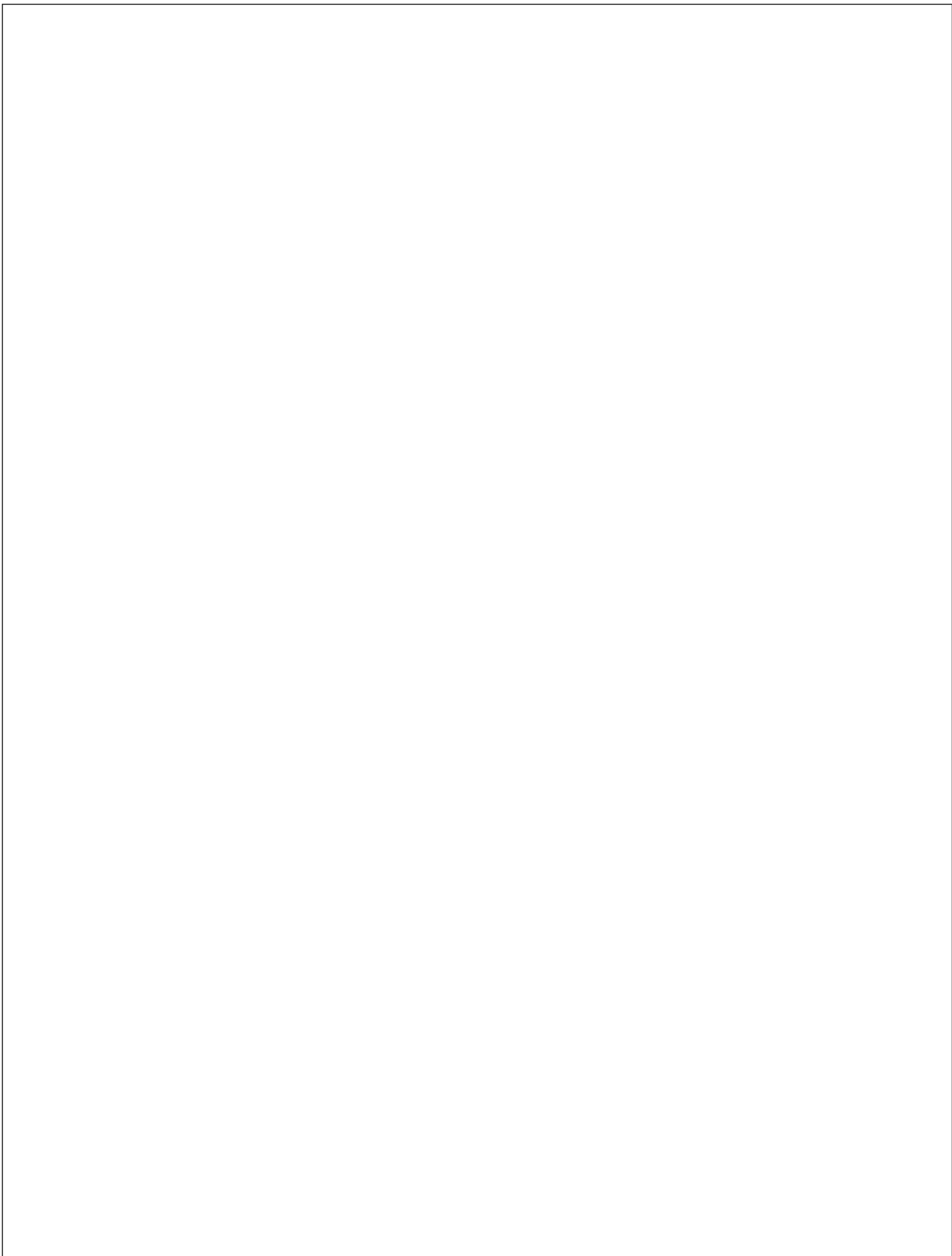
As device maximum operating frequency is about 7 to 8 GHz so we prefer to impose Dambrin, berroth and Miras paper which is fundamental paper for linear parameter extraction. In non linear parameter extraction we prefer most recent and advanced parameter extraction procedure based on Angelov model. ADS also use the Angelov model in its directory.

We have taken 15 parameters in linear modelling and 17 parameters in non linear modelling one could go beyond 15 and 17 parameter but the complexity will also increase exponentially. [2, 3, 14] have taken more parameter but extraction procedure become more tedious simultaneously.

In this dissertation we have done up to DC nonlinear modelling (In non linear modelling we got less than 5 % error).

The future work could be the modelling of device by application of RF signal called RF modelling. RF modelling along with linear modelling and non linear modelling called complete modelling. Capacitance value depends on bias voltages as well so by including the capacitor depends on bias voltages, modelling will be again become accurate but difficult. As HEMT devices are power devices so that they suffer by heating effect. So that we should include the heating effect in the mathematical model.

Once we increase the parameter and there dependency on bias voltages, then complexity becomes more and more but the same time we will get more precise model for device which could give better results than current one.



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