ADAPTIVELY BIASED CMOS VOLTAGE FOLLOWER

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by

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This work is dedicated to my parents for supporting and encouraging me throughout my life.

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Abstract

A novel CMOS adaptive biasing technique has been proposed for low power applications which can be applied to any CMOS circuit having differential current at one of its node. This technique gives an output current proportional to input differential voltage. The proposed technique can be used in low voltage high speed operational amplifiers. The dynamic bias current saves power and also improve slew rate, delay. A modified NMOS topology technique is also applied to a conventional operational amplifier to improve the slew rate. A SPICE simulation for proposed technique and modified NMOS topology technique in 0.18um CMOS technology is reported.

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CHAPTER 1

NEED FOR LOW POWER DESIGN

1.1 Motivation

With the continuous growth of market for portable devices operated by battery such as mobile phones, laptops and many consumer electronic devices, low power design has become very important in integrated circuits. Among several other available technologies such as bipolar junction transistor (BJT), gallium arsenide (GaAs), complementary metal-oxide-semiconductor (CMOS), bipolar CMOS, the CMOS technology has played an important role in the development of low power portable devices for various applications.

For more than ten years, several low power CMOS design techniques have been investigated that include basic circuit design modification, architecture changes for implementing desired functions using low threshold voltage devices, power down strategies, optimization of transistor size, supply voltage scaling along with other possible techniques.

Need for Low-power design started in 1990 with expansion in portable electronic market. Power dissipation in CMOS circuits has been increased due to increased clock frequency. Power dissipation peaked in 1990-1991. After 1991, power dissipation of CMOS chips is reduced due to the emergence of low power design. Increase in demand of large number of portable devices such as notebook computers and mobile phones where very low power dissipation is a primary requirement, low power design has gained importance.[10]-[15]

1.2 Introduction

In the past, the major concerns of the VLSI circuit designers were area, speed and cost. In recent years, this has changed dramatically and power dissipation is being given significant weightage in comparison to area and speed. Power consumption is a clear concern in the semiconductor industry. The production of portable and hand-held electronic devices combined with increasing packaging costs is forcing circuit designers to adopt low power design techniques. Low power design of application specific integrated circuits (ASIC) result in increased battery life and better reliability [17].

Semiconductor Industry Association has identified low power design techniques as a critical technological need. Hence it becomes dominating for circuit designers to acknowledge the importance of controlling power consumption at all levels of the design hierarchy, starting from the lower levels of abstraction.

1.2.1 Effects of Power Dissipation

When power is dissipated, it consistently leads to rise in temperature of the chip. This increase in temperature affects the device even when the device is off [26]. When the device is off, it leads to rise in the number of intrinsic carriers, by the following relation

$$\eta_i = \varepsilon^{\frac{EG}{KT}} \tag{1.1}$$

From the above relation it can be observed that as temperature increases, the number of intrinsic carriers in the semiconductor increases. The majority carriers, contributed by the doping atoms, are less affected by rise in temperature. Therefore the device becomes more intrinsic. As temperature increases, leakage current, which is directly proportional to minority carrier concentration [26], increases which further increases the temperature. Eventually, the device might get permanently damaged, if the increase in temperature is not controlled by removal of the dissipated heat. A device in ON state won't be affected much by minority carrier increase, but will be affected by threshold voltage which decrease with increase in temperature and lead to change in current. Hence the device performance degrades. Power dissipation is more precarious in battery powered applications as the power dissipation increases, the battery life reduces [22][23].

We now discuss some prevailing low power CMOS techniques that are used in different levels of abstraction.

1.3 Low Power Techniques in CMOS Circuits

In most low power techniques conservation and trade-off are the important factors. The conservation tries to reduce the power that is wasted in the circuit. The designer needs to identify and prevent the leakage power. Another way of low power technique is to discover alternate designs that reduces power dissipation. This requires complex trade-off decisions involving a designer's skill. Thorough analysis and understanding of the design specification, operating environment are means to propose new low power techniques [16]-[18].

1.3.1 Forward Body Bias Method

In low power design, voltage scaling is a straightforward technique and becomes more effective due to the quadratic dependence with the supply voltage. But, with low supply voltage, gate to source voltage of a MOS transistor reduces. Thus, low threshold MOSFETs are required for operation at the low power supply voltage. To obtain low threshold voltage transistors using present CMOS technologies, circuit design techniques must be developed that reduces device threshold values. Forward body-bias technique is used for designing low threshold voltage transistors. As threshold voltage is a function of source-bulk potential, threshold voltage can be controlled. By increasing the body potential, threshold voltage can be reduced. However, there is a limit to the amount of VSB, which can be applied since large VSB may trigger CMOS latch up.

The dependence of threshold voltage on body bias is given in equation 1.1

$$V_{TN} = V_{TN0} + \gamma(\sqrt{|2\emptyset_f + V_{SB}|} - \sqrt{|2\emptyset_f|}) \quad (1.1)$$

Where $V_{TN}$is the threshold voltage of NMOS and V_{TN0} is the zero-bias threshold voltage with V_{SB}= 0. γ is called the body-effect coefficient.

When $V_{B} > 0$, more holes move away from the substrate region leaving a small negative charge in the depletion region. As threshold voltage is a function of total charge in the depletion region, threshold voltage decreases. Thus, an NMOS can be designed to operate at a reduced voltage.

1.3.2 Dynamic Threshold Technique

The forward body biased method, MOSFET has been used for designing a low power CMOS circuits. However, this technique has a drawback. When the transistor is turned-off, the leakage current rises due to reduced threshold voltage. With increase in forward body-bias, the leakage current increases significantly. This leakage current can be reduced using a dynamic body bias technique.

The dynamic threshold MOSFET (DTMOS) technique is used to overcome the drawback in the forward biased MOSFET. It operates in two modes. In the ON mode of the transistor, the source and body of MOSFEET is in forward bias. The threshold voltage of the transistor is reduced. In the OFF mode, the transistor has source body voltage (V_{SB}= 0) which increases the threshold voltage. Thus, it reduces the leakage current and turns off the transistor completely. This DTMOS method with the forward source-body biased MOSFETs is used for the low voltage operation of CMOS circuits.

1.3.3 Dynamic Voltage Scaling Technique

Dynamic voltage scaling technique (DVS) has been an effective low power design technique in digital systems. In this technique, a higher supply voltage is applied to a digital integrated circuit (IC) when it is operating at a high speed and a lower supply voltage is applied when it is not in its peak performance such as standby mode. In DVS technique, a smart power supply generator is needed which generates adaptive supply voltage according to operational frequency of the IC. Thus, the problem which the chip designers are facing, is the development of a portable, cost effective adaptive power supply. DC/DC converter is found to be the best solution in adaptive supply voltage generation.

1.4 Limitations of Low Power Design

1.4.1 Practical limits

A number of difficulties or technological limitations are there to address and these limits are called as practical circuits:

i) Capacitors increase the power dissipation to attain a required bandwidth. This is acceptable only if the presence of capacitor reduces the noise power by the same amount by decreasing the noise bandwidth. Hence, parasitic capacitors contributes to increase in power consumption.

ii) The power used in bias circuitry is a wastage and efforts should be taken to minimize. However, poor biasing structures may increase the noise and therefore a proportionate increase in power.

iii) According to [8], power consumption is increased if the signal at any node corresponding to a pole inside bandwidth has a peak-to-peak voltage amplitude smaller than the supply voltage. Thus, measures has to be taken to amplify the signal to its maximum possible value, and to sustain this all over the path. Using current-mode circuits with limited voltage swings is no more a good tactic to reduce power, as long as the energy is supplied by a voltage source. It only becomes worthy when voltage companding techniques are used.

iv) Due to the presence of additional noise sources, there will be an increase in power consumption. This comprise 1/f noise, and noise coming from the power supply.

v) When capacitive loads are present for example parasitic capacitance, the current required to attain a given bandwidth is inversely proportional to the trans-conductance of the active device. The small value of trans-conductance in MOS transistors may consequently cause an increase in power consumption.

vi) The prerequisite for accuracy usually leads to the use of larger dimensions for active and passive devices, with a subsequent increase in parasitic capacitors and thus power.

vii) All switched capacitors must be clocked at a frequency higher than twice the signal frequency. The power consumed by the clock itself may be dominant in some applications.

Methods to reduce the effect of these limits can be found at various levels of abstraction in analog design ranging from device to system.

1.4.2 Other difficulties to low-power design

Other than the practical limitations discussed before, there are also historical or psychological barriers to the design of low power analog circuits. The most important obstacles that a designer need to know are listed below

a) Analog blocks are frequently be taken from predefined libraries with bias currents in the range of milli amps and with architectures that are not well-suited with low voltage or low current.
b) The use of low bias currents is sometimes not acceptable due to a lack of adequate transistor models and correct description of transistors parameters and also leakage currents.

1.5 Key Contributions

The work in this dissertation can be summarized as follows:

1. Design and simulate the two stage CMOS operational amplifier.

2. Design and simulate adaptive biased CMOS operational amplifier.

3. Design and simulate adaptive biased CMOS operational amplifier using modified NMOS topology.

4. Design and simulate proposed adaptive biased CMOS operational amplifier.

In the dissertation, a novel adaptive biased CMOS op-amp is proposed. The slew rate and delay in the proposed adaptive biased CMOS op-amp has been improved. All the circuits have been simulated using TSMC 0.18μm CMOS process technology parameters and the simulation results have been presented to show the effectiveness of the circuits. The performance parameters of the proposed adaptive biased CMOS op-amp has been compared with the existing techniques discussed in chapter 3 and the comparison shows that the proposed adaptive biased CMOS op-amp has high slew rate with minimum additional circuitry. The proposed circuit can be used for various analog applications where better high frequency performance is demanded.

1.6 Organization of Thesis

The organization of thesis is as follows:
CHAPTER 2: The chapter addresses the basics of adaptive biasing and some of the existing prevalent techniques. The need for adaptive biasing techniques are discussed.

CHAPTER 3: In this chapter, the basic functioning of operational amplifier and its application as a voltage follower is discussed. The CMOS configuration of op-amp, its working and simulation results are analysed. The working and analysis of adaptively biased op-amp and modified NMOS topology is also discussed.

CHAPTER 4: The chapter proposes the novel structure of adaptive biasing. The performance is analysed through SPICE simulations.

CHAPTER 5: The pros and cons of the methods discussed in above chapters and comparison of proposed circuit with existing methods have been presented in this chapter.

CHAPTER 2

ADAPTIVE BIASING

2.1 Introduction

The design of digital and analog circuits with low power consumption is attaining more importance in present days. This is due to the increase in usage of battery operated devices, for which it is essential to reduce the weight and the size and to improve its operation life. Other important reasons are the heat generated on chip, growing cost of power supplies and cooling mechanisms. As we all know, the CMOS technology is obviously the best for micro power constraints. It offers low stand by currents and transistors with good performance at very low bias currents [21]. In specific, the quiescent current of the circuit stages has to be decreased to reduce the power consumption of the operational amplifiers (op-amp) [19]. The reduction of biasing current limits the transient characteristics, in specific slew-rate and gain bandwidth product. In coming chapters, some CMOS adaptive biasing circuits have been discussed in low power applications to give low quiescent current without reducing the circuit driving capability.

There are many adaptive biasing techniques available. But each technique has its own advantages and disadvantages. There will be trade-off between power consumption, slew rate and delay parameters. Depending on the application, suitable adaptive biasing technique can be adopted. These techniques are not generalised i.e., a technique can be implemented only to a particular block like differential amplifier, operational trans-conductance amplifier etc. The same cannot be used for other analog blocks. Generalised techniques are not popular in the CMOS adaptive biasing because some techniques concentrate on improving the slew rate, gain and delay parameters and some techniques concentrate on reducing leakage by not effecting other parameters. Depending on the application suitable technique is used. Various adaptive biasing techniques are discussed and compared in the coming chapters.

2.2 Need for Biasing

When the transistor is used as a linear amplifier, it has to amplify signals which swing in both ways, such as sine waves. For this to happen, the operating point of the transistor has to be in the middle of the active region, where it presents the (almost) linear amplification behaviour. The process of forcing the transistor into the active region is called biasing, and is done commonly with DC power supply. When biased, DC currents flow in the transistor and non-zero DC voltages develop at its terminals. Biasing has also to be done to other amplifying devices, such as field effect transistors (FETs).

We try to place the transistor in the middle of the active region, such that it amplifies linearly either negative or positive swings of the AC signal which is supposed to be amplified. If the incoming signal forces the transistor to leave the active region (either entering into cut off or saturation) due to an improper bias point in the active region, then there is distortion in the amplified AC signal, which is something an electronic designer always wants to avoid. It is about this Operating point or quiescent point (which is set by the circuit designer via biasing)

so care has be taken so that the operating point should be placed in such a way that the output will not exceed the voltage or current ratings of the circuit. Otherwise this will lead to distortions to the signal output such as clipping etc.

2.2.1 Types of Biasing

The common problem in the working of a transistor amplifier is maintaining stable quiescent current and quiescent voltage (operating point). This is done by using proper biasing conditions and maintaining them stable irrespective of variations in temperature which causes distortion at the output [26]. Thus, there is requirement for a method to stabilize the operating point and to maintain it exactly at the middle of the load line. There are many methods available but only three basic types are popular.

2.2.2 Fixed Bias

It is also called gate bias, was shown in fig 2.1. It consists of a resistor R_G connected between the gate supply voltage and the gate terminal. But unfortunately, this method is somewhat thermally unstable. If the temperature of the transistor increases for any reason (due to a rise in ambient temperature or due to current flow through it), drain current will increase. This increase in current also causes the operating point or quiescent point, to move away from its desired position. This variation to temperature is undesirable because it affects the linearity of the amplifier and results in distortion.

Since voltage drop across R_G is zero volts, gate to source voltage is V_{GG} and R_D is selected in such a way that transistor operates in saturation region. The main drawback of this circuit is it requires two supply voltages. This method is more sensitive to variation in temperature when compared to others.

In the fig 2.1

V_{DD} is drain supply which provides drain current

V_{GG} - Gate supply used for channel accumulation in case of enhancement MOSFET

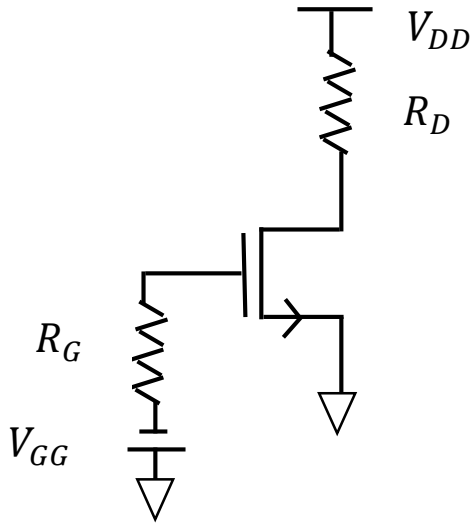


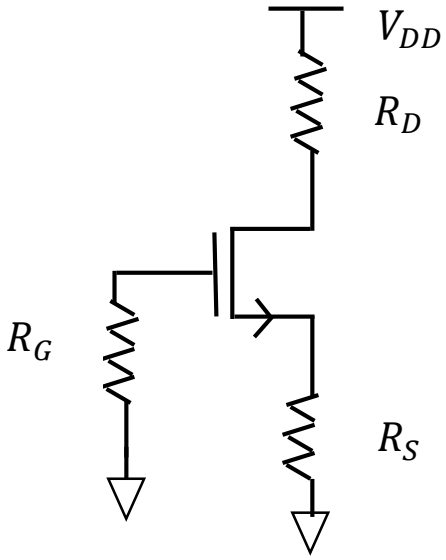
Fig 2.1 fixed bias circuit

2.2.3 Self-Bias

Much better method of biasing is achieved by introducing the bias resistor directly at the source terminal, as shown in fig 2.2. It is also called as source self-bias. Increase of temperature causes an increase in drain current, the drain voltage will fall due to the increase of voltage produced across the load resistor.

Voltage drop across source resistor causes reverse biasing of gate channel junction. This method of maintaining gate channel junction in reverse biasing through voltage drop across source resistance is known as self-biasing. For the reverse biasing of gate junction fixed bias uses power supply at gate terminal. Here no supply at gate terminal is required. Drain resistance should be selected in such a way that transistor works in saturation region.

Increase in drain current due to temperature (generally ambient temperature) leads to increase in voltage drop across source resistance. This implies increase in reverse biasing of gate channel junction. Due to more reverse voltage across gate junction channel width decreases which finally reduces drain current. The increase in drain current due to temperature is compensated by reduction in channel width. Source resistance is called self-biasing resistor.



$$V_{GS} = -I_D R_S$$

Fig 2.2 self-bias circuit

The main drawback of this technique is the source resistance creates negative feedback in the amplifier analysis. This negative feedback severely effects the voltage gain. To overcome this problem a bypass capacitor is connected in parallel to source resistance. So during amplifier analysis (ac analysis) the bypass capacitor is short circuited thus nullifying the effect of negative feedback on gain of the amplifier.

2.2.4 Voltage Divider Bias

A combination of fixed and self-bias can be used to improve stability and to overcome some of the drawbacks of the other two biasing methods. One of the most commonly used combination-bias method is the voltage divider type shown in fig 2.3. Fixed bias is provided in this circuit by connecting voltage divider consisting of$R_{1,}$ R_2 and the supply voltage V_{DD}. The dc current flowing through the voltage divider network bias the gate terminal. Source resistor, which is connected in series with the source, provides the source with self-bias. When the drain current increases, the voltage drop across source would also increase, increasing reverse voltage at gate terminal, thus reduces drain current. However, to provide long-term or dc thermal stability, and at the same time, allow minimal ac signal degeneration.

Voltage divider network biasing makes the transistor circuit independent of changes in temperature as the voltages at the transistors are dependent on external circuit values.

To calculate the voltage developed across gate terminal, we simply use the voltage divider formula for resistors in series.

Generally the voltage drop across resistor R_2 is much less than for resistor R_1. Then clearly the transistors gate voltage with respect to ground, will be equal to the voltage across R_2.

The aim of **Transistor Biasing** is to establish a known operating point for the transistor to work efficiently and produce an undistorted output signal.

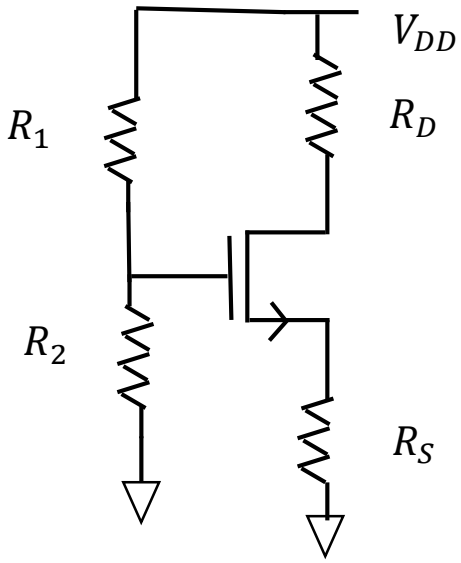


Fig 2.3 voltage divider bias circuit

Here gate to source voltage is difference between the voltage at R2 and voltage at source resistance.

Voltage at R2 can be calculated using voltage divider rule.

$$V_{GS} = \frac{V_{DD}R_2}{R_1 + R_2} - I_D R_S$$

Self-bias cannot be used for enhancement mode MOSFET. In that case voltage divider biasing is used for stable operating point. Drain and source resistors are selected in such a way that transistor is working in saturation region.

2.3 Need for Adaptive Biasing

The current trend for low power design is mainly driven by the rising demand for long battery life portable devices, and the technological restrictions of high performance VLSI circuits. Low power is the main objective for which speed and dynamic range have to be sacrificed due to scaling of supply voltage. The efficient way to reduce the power dissipation is to reduce the supply voltage, since the average power of CMOS digital circuits (is proportional to the square of the supply voltage), generally dominant in modern VLSI circuits. Although the supply voltage has dropped from 5 V in the early 90's down to 1.2 V at present, most analog circuits can still be designed. However, a further drop in supply voltages is expected to cause serious blockades for analog designer, because the signal swing becomes too small to design circuits with sufficient signal integrity at sensible power consumption levels [7]. From a circuit point of view, it is difficult to implement analog circuits with the reduced supply voltage, since many circuit techniques like stacking and cascading become no longer possible. Due to this, analog designers are diverting from conventional circuit architectures. Novel techniques for the design of low voltage, low power high performance analog circuits are required for the new generations of deep sub-micron CMOS technologies.

The process of introducing dependence of bias current (from supply voltages) on the input voltage is called as adaptive biasing. In analog circuits normally the bias current is independent of input voltage. Due to this there is leakage of power especially in CMOS differential circuits.

To understand the discussion, consider the case of differential amplifier. It consists of two inputs and the output is the difference of input voltages with a gain. When both the inputs are zeros the current in the two differential paths is zero. When one of the input is zero and other has some input voltage, the current flowing in that path contributes to the output voltage. But when both the inputs are same, current flows in both the paths with equal magnitude. As the output is difference of the inputs, it will become zero. Even though the output is zero, the input transistors are in ON state due to the input voltages. So bias current flows in both the paths i.e. there is current flow in the circuit from supply to the ground even though the output is zero. This current flowing in the circuit is considered as leakage current because it is unwanted or undesired. Thus the power dissipation caused by the flow of leakage current is known as leakage power dissipation.

For reducing that leakage power, several adaptive biasing techniques are adopted. There many ways to bring adaptive nature for the bias current. One among them is to connect a controlling circuit. Other one is to introduce some transistors to the basic architecture to bring the dependence nature for bias current [1]. We will discuss some adaptive biasing techniques to acquire knowledge on the concept of adaptive biasing.

2.3.1 Current Feedback Adaptive Biasing

This technique is used in Operational Trans-conductance Amplifiers. They gained important role as basic building blocks for filters, multistage amplifier circuits. To meet low power and high output current specifications at a time, class-AB operation mode is essential. The conventional class-AB differential amplifier based on cross coupled pair of input transistors is not suitable with more demanding low voltage requirements. Many resolutions that involve modification of the basic differential pair architecture are either duplicating the input transistors, or adding extra elements to the simple mirror based current source. Other methodologies that uses positive feedback are not suitable to obtain large quiescent currents.

In this method [28], class AB operation is obtained from basic OTA cells protecting the original topology. In this way, the output current driving capabilities of cells are improved for low voltage operation. This method can be applied to a conventional wide swing OTA cell. Maximum quiescent current can be certainly controlled by setting a few current mirror gains. The input and output rail-to-rail voltage ranges are preserved, with the additional advantages of a substantial reduction of the Trans conductance dependence on the input common mode voltage.

2.3.1.1 Principle and Working

In simple OTA cell the maximum output current is equal to twice the quiescent current. Increase in the maximum output current causes rise in the quiescent power consumption. Applying a differential input voltage, means to increase the fraction of I0 flowing into one of the two branches of the input differential amplifier while reducing the fraction that flows into the other branch. Ultimately, for an appropriate high input voltage, tail current is completely directed to one branch and the corresponding drive of the output transistor cannot be increased further.

The basic idea of this method is to prevent both currents in the input branches from getting smaller than a fixed value, by means of a proper feedback loop. In this manner, as the differential input voltage increases beyond a certain threshold, the smaller branch current tends to be stable, while the larger continues to increase and so does the drive of the corresponding output transistor.

In this method, the upper part is organised by a conventional OTA, while the lower part consists of control circuit that produces the adaptive biasing of the OTA, to allow class AB operation. The control circuit makes a replica of the current in the output transistors. These output currents are subtracted to the reference current the results are summed up and sent back to top (original) circuit.

When a differential voltage is applied, the tail currents remain constant. The tail current is controlled only by the differential current, that, getting smaller and smaller, produces a proportional increase of the tail currents, and consequently, in the output current of the stage. The critical point of the control circuit is the path between VDD and ground. By Reducing VDD, the tail current also reduces, affecting the large signal performance of the circuit. Small

signal functionality remains immune until the quiescent current start decreasing. This occurs when the VDD is as very low. The minimum supply voltage is given to the control circuit to ensure proper functionality.

2.3.2 Low Voltage Power Efficient Adaptive Biasing

In modern applications very stern requirements are enforced to the adaptive biasing block of Fig. 1. They are ability to set low and controlled quiescent currents, low output resistance and large driving capability, large output currents in order not to limit slew rate, low voltage operation, reduction in number of transistors due to noise, bandwidth and silicon area considerations[13]. This technique will be applied to the design of low power differential input stages as shown in fig 2.4

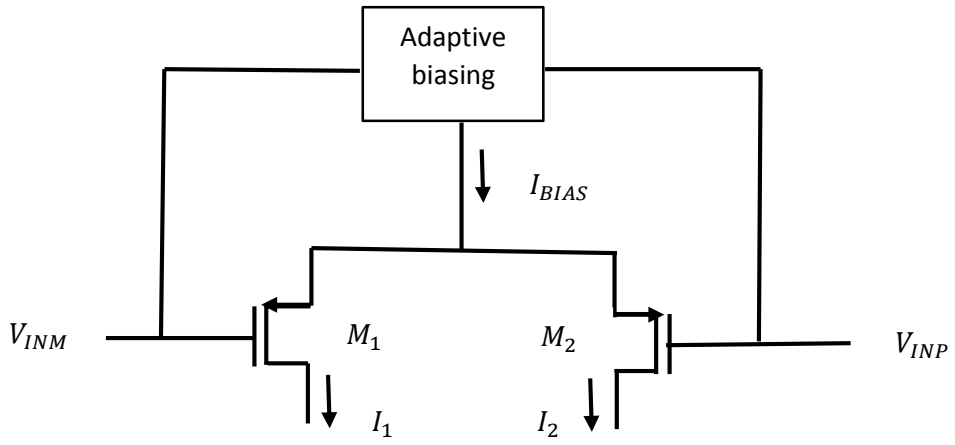


Fig 2.4 adaptive biasing topology

To meet these requirements, adaptive biasing technique shown in Fig 2.4 is used. The aim is to set a controlled voltage at the common source node of M1 and M2.

When $V_{INP} = V_{INM} = V_{CM}$, i.e. under quiescent conditions, the adaptive biasing network forces $V_{GS1} = V_{GS2} = V_B$. Hence, quiescent current through M1 and M2 is perfectly set by V_B and do not depend on V_{CM}. Selecting V_B slightly larger than V_{TH} very low quiescent current can be achieved. However, when a differential input is applied, an unbalance in $V_{GS1}$and V_{GS2} is created which leads to different currents in M1 and M2 the maximum value of which is not limited by the quiescent current. Note that under dynamic conditions operation is also independent of V_{CM}, and a large CMRR can be obtained.

The adaptive biasing circuitry consists of CMS circuit and a buffer unit which are explained briefly below

2.3.2.1 CMS Circuit

A new CMS circuit that achieves the above mentioned necessities. To provide high input resistance and to level shift the input voltage, two simple and efficient level shifter buffers that we call as flipped voltage followers (FVFs) are engaged. Remember that if classic source followers were employed, input deviations would lead to different drain currents in the source follower transistors, and therefore to non-symmetrical DC level shifts.

2.3.2.2 Buffer Circuit

Buffer used here consists basically on an FVF, consists of a level shifter. The FVF cell has all the above mentioned desirable features, such as a very low output resistance and large current driving capability. The FVF output is shifted up with respect to the input, and therefore an identical input down shifting is required. This is achieved by a source follower. There is an alternative execution that avoids the requirement for the level shifter. It is a PMOS transistor driven by a NMOS differential pair in negative feedback. The feedback provides an accurate voltage copy and low output resistance. It leads to a significant increase in slew rate and fast settling, low noise and low static power consumption. It can find application in low voltage low power CMOS operational amplifiers and buffers.

CHAPTER 3

ADAPTIVELY BIASING OF CMOS OPERATIONAL AMPLIFIER

3.1 Introduction

Operational amplifier (op-amp) plays an important role in analog circuit design. It is widely used building block in analog circuit design. It was designed by John R. Ragazzini in 1947 to represent a unique type of amplifier. It is used to perform operations such as addition, subtraction, integration, differentiation and amplification. The first application of Op-amp was in analog computer. Op-amps are the amplifiers that have high open loop gain, so that when op-amps are used in negative feedback, the overall close loop transfer function becomes independent upon the forward path gain of the op-amp. This feature has been much advantageous in designing analog circuits. The prime requirement of an op-amp is to have a very high open loop gain to implement the negative feedback concept, very high resistance at the input and low output impedance. In recent times, the CMOS Op-amp circuits are often used in Integrated circuits. A two stage CMOS Op-amp is very popular among all design techniques. This thesis focuses mainly on various adaptive biasing techniques that can be implemented to CMOS Op-amps.

3.2 Fundamentals of Operational Amplifier

Mainly, in an Op-amp the input is a differential signal which is applied to a differential amplifier as the input stage and the output stage is a single ended output, which amplifies the difference of the two input given at the input stage of the Op-amp, hence there is a differential to single ended conversion circuit must exist in an Op-amp circuit. As the output impedance of the Op-amp is very low and requires a high output voltage swing a buffered stage is used at the output. The Fig 3.1 shows the basic block diagram of an Operational amplifier.

The input stage of the Op-amp is differential amplifier. As the name suggests it performs the difference between the two input signals. It rejects the common mode voltage applied at the input terminals. As, it cancels the common voltage at the input, hence, noise and bias voltages are cancelled out. Wide range of electronic circuits use differential amplifiers. But, practically some amount of common mode voltage factor is always exists at the output of the differential amplifier.

The output of the differential amplifier is stated as

$$V_{OUT} = A_C\left(\frac{V_1 + V_2}{2}\right) + A_d(V_1 - V_2)$$

Where A_C is the common mode gain and A_d is differential mode gain of the op-amp.

By using a differential amplifier it is possible to eliminate noise and bias voltages that appear on both inputs so a small common-mode gain is usually considered acceptable [9]. The common mode rejection ratio is simply the ratio between differential-mode and common mode

gain and it represents the efficiency of the amplifier in rejecting voltages that are common to both inputs from affecting the output.

Common-mode rejection ratio (CMRR) is given by

$$CMRR = \frac{A_d}{A_C}$$

For an ideal differential amplifier common mode gain should be zero and CMRR should be infinite. The differential amplifier used in CMOS technology gives a single ended output. The out stage of two stage CMOS Op-amp is a common source which gives one more gain stage in cascade with the differential gain stage. For designing an Op-amp with very low output impedance a source follower output stage is used which is considered as buffer stage. The block diagram of op-amp is shown in fig 3.1

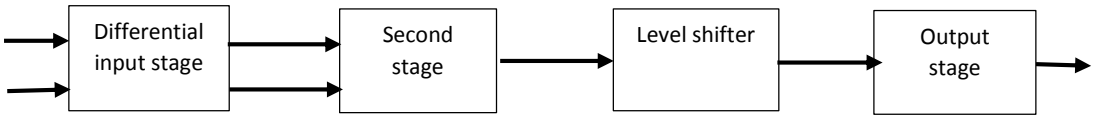


Fig 3.1 Block diagram of op-amp

From [25], input stage is dual input balanced output differential amplifier. Second stage is dual input unbalanced output differential amplifier. Two differential stages are used to obtain high voltage gain and common mode rejection. Since second stage has unbalanced output, DC biasing voltage will also be present in it. If this DC biasing voltage reaches output stage, its biasing conditions gets distorted which causes distortion in the final output. Therefore level shifter has been used to remove the DC biasing voltage present in unbalanced output. Power amplifier is used as output stage so that op-amp can supply greater power to the load.

Symbol of op-amp is given in fig 3.2

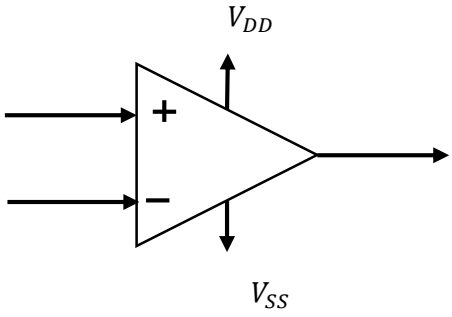


Fig 3.2 symbol of op-amp

Two input terminals are used for applying differential input signals, the negative input is known as inverting terminal of the input and positive input is the non-inverting terminal. The Op-amp gives a single ended output and the output terminal is shown in the symbol as output pin. The pins VDD and VSS are shown in the symbol generally used as the terminals for the supply voltages. The op-amp is a dual power supplies component in which the VDD terminal is used for positive power supply and VSS is used for negative power supply. Sometimes ground signal is applied at the VSS terminal.

Table 1 Ideal and practical parameters of op-amp

Parameters	Ideal	Practical
Open loop gain	Infinite	10^6
Input resistance	Infinite	1-2M ohms
Output resistance	0	50-100 ohms
Open loop bandwidth	Infinite	5Hz
Offset	0	Non zero
CMRR	Infinite	10^6
Slew rate	Infinite	0.5-1V/us

From the above mentioned parameters, we concentrate on increasing slew rate by using adaptive biasing in this thesis. Slew rate directly represents how fast the device is responding. Thus by improving slew rate and reducing power consumption at the same time, adaptive biasing has a crucial role in op-amp design.

3.2.1 Op-amp as a voltage follower

In this thesis op-amp is configured as a voltage follower by providing negative feedback from output to inverting terminal at input as shown in fig 3.3

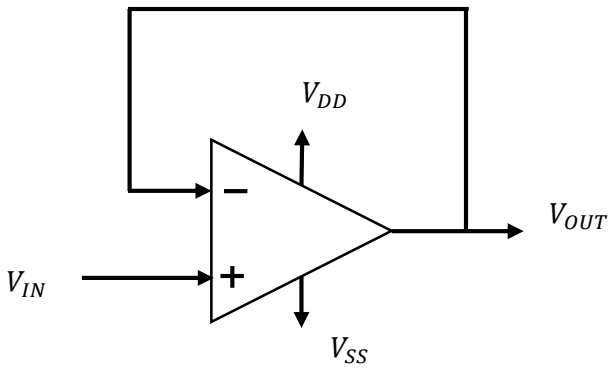


Fig 3.3 op-amp as voltage follower

The configuration shown in the Fig 3.3 is a simple diagram of unit gain configuration. This is used to find the slew rate, delay time of Op-amp by applying a step signal at non inverting input of the Op-amp. Observing output waveform of the Op-amp after a transient analysis we can find the SR and the delay time. From the slope of the output signal during rise or fall time of output waveform we can determine the slew rate.

3.2.2 Working

When an input is applied to the non-inverting terminal, by the concept of virtual short the voltage at non-inverting terminal appears at inverting terminal. As the output terminal is directly connected to inverting terminal, output voltage is equal to input applied at non-inverting terminal thus becoming voltage follower. It is very useful in giving effective isolation of the output from the input signal source because of its high input impedance. It will draw very low power from the signal source avoiding loading effects. It is often used in the construction of buffers in logic circuits.

Slew rate is determined by measuring slope from 20% to 80% of maximum value [27]. SR^+ is obtained during rising edge of the input. SR^- is obtained during falling edge. Average of both will give the overall slew rate of the device.

T_d is the time taken by output to reach 50% of its maximum value. Both T_{DLH} and T_{DHL} are measured and average is taken to get the overall delay.

Now we will see the architecture of a conventional two-stage CMOS op-amp and its operation as a voltage follower.

3.3 Conventional Two Stage CMOS Operational Amplifier

As the name suggests that conventional two stage op-amp consists of two stages. First one is differential input stage and the second one is common source stage. As the single stage op-amp has a drawback of low gain, common source stage is cascaded to first stage to increase gain. As we know common source stage is a tans-conductance amplifier that gives output current proportional to the input voltage. The output current is allowed to pass through a resistor or a diode connected load to generate output voltage. The conventional two stage op-amp works as voltage follower when one of its input is connected to output terminal. A step signal is applied at input to calculate the slew rate of the operational amplifier. Power consumption, delay and input bias current also observed from the simulations.

3.3.1 Working

A conventional two stage CMOS Op-amp is shown in the Fig 3.4 [2]. The first stage of this Op-amp is consist of M1 –M6 transistors, the second stage is consist of M7-M8 transistors. All transistors used in this conventional Op-amp operates in saturation region. The first stage is a differential stage, the differential signal is applied into the pin and the gate terminals of the transistor M1 and M2 respectively. These transistor M1 and M2 are two NMOS driver transistors used to convert the differential voltage to differential current, these differential

currents are given to the current mirrored load transistor M3 and M4. The transistor M5 and M6 are used to provide the biasing current to the differential stage.

The following is the circuit diagram of conventional op-amp

3.3.2 Circuit Diagram

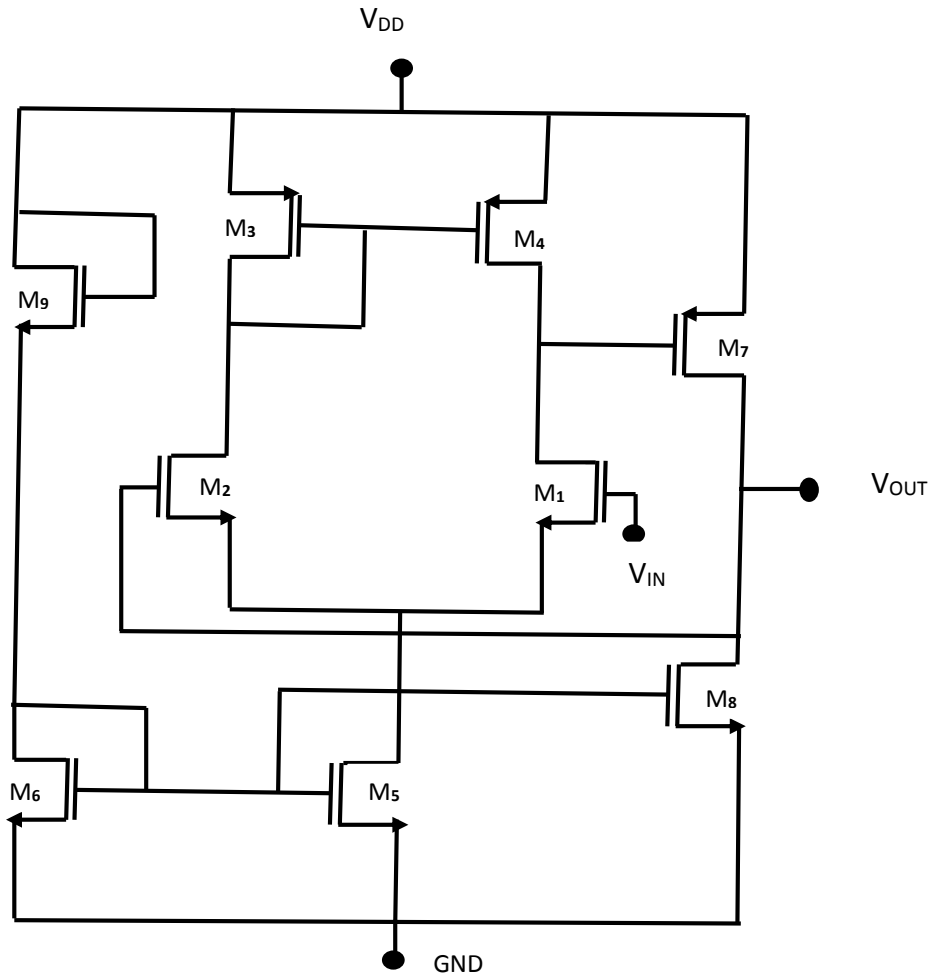


Fig 3.4 conventional two stage CMOS op-amp

The output of the differential stage is a single ended output signal and it gives the difference of the input signals with a constant gain. The second stage is a common source gain stage, the output of the first stage is applied to the gate of transistor M7. M8 is used to provide the bias current to the second stage and the output is taken from the drain terminal of the M8.

When a step signal of certain frequency is applied at the non-inverting terminal of op-amp, the voltage difference between inverting and non-inverting terminal is equal to input because initial

voltage at output is considered to be zero. Due to input voltage current I1 flows through the drain of M1 and it is proportional to square of the input because transistor is operating in saturation region. The voltage at inverting input is zero therefore transistor M2 is OFF and no current flows through it. Due to current I1 in M1-M4 branch, voltage develops at the output port. At this condition the voltage difference is maximum thus output current is also maximum as a result, output voltage rises rapidly.

As the voltage at the inverting terminal increases (due to rise in output), transistor M2 is ON and operates in saturation region. Current I2 starts flowing in M2-M3 path which is proportional to square of the output voltage. As I2 increases, the differential input voltage reduces thus limiting the rapid growth of the output. When output voltage reaches input, the differential input voltage becomes zero and no there will be no further increase in the output. In this way output reaches the input after certain time. The bias current which is the sum of the currents I1 and I2 are supplied through current mirror from the supply voltage. It is to be observed that even though output reaches input voltage, transistors M1 and M2 are in ON state thus allowing bias currents to flow through them. In this case the bias current through the current mirror is considered as leakage current. The power dissipation caused by leakage current is known as leakage power.

DC gain of first stage

$$\boldsymbol{A_1 = \frac{-g_{m1}}{g_{ds1} + g_{ds4}}}$$

DC gain of second stage

$$\boldsymbol{A_2 = \frac{-g_{m7}}{g_{ds7} + g_{ds8}}}$$

Overall gain

$$A_V = A_1 A_2$$

Slew rate

$$SR \propto I_5$$

Power dissipation (leakage)

$$PD = I_5^2 t$$

Interestingly slew rate and power dissipation are both proportional to bias current [2]-[4]. But if we can reduce the duration of the current flow, power consumption can be reduced without effecting slew rate. This analysis is useful in the coming adaptive biasing techniques that mainly focus on reducing the time duration of bias current flow through current mirror.

3.4 Simulation Results of Two Stage Conventional Op-Amp

The conventional CMOS Op-amp shown in the Fig 3.4 is designed in TSMC 180 nm technology with supply voltage of 1.8 V. The simulation of this Op-amp is done by PSPICE circuit simulator. Here we applied a square input signal of 1.65V at a frequency of 200Hz at the non-inverting input of Op-amp. The power consumption of the Op-amp found out from the transient analysis is 550 uW.

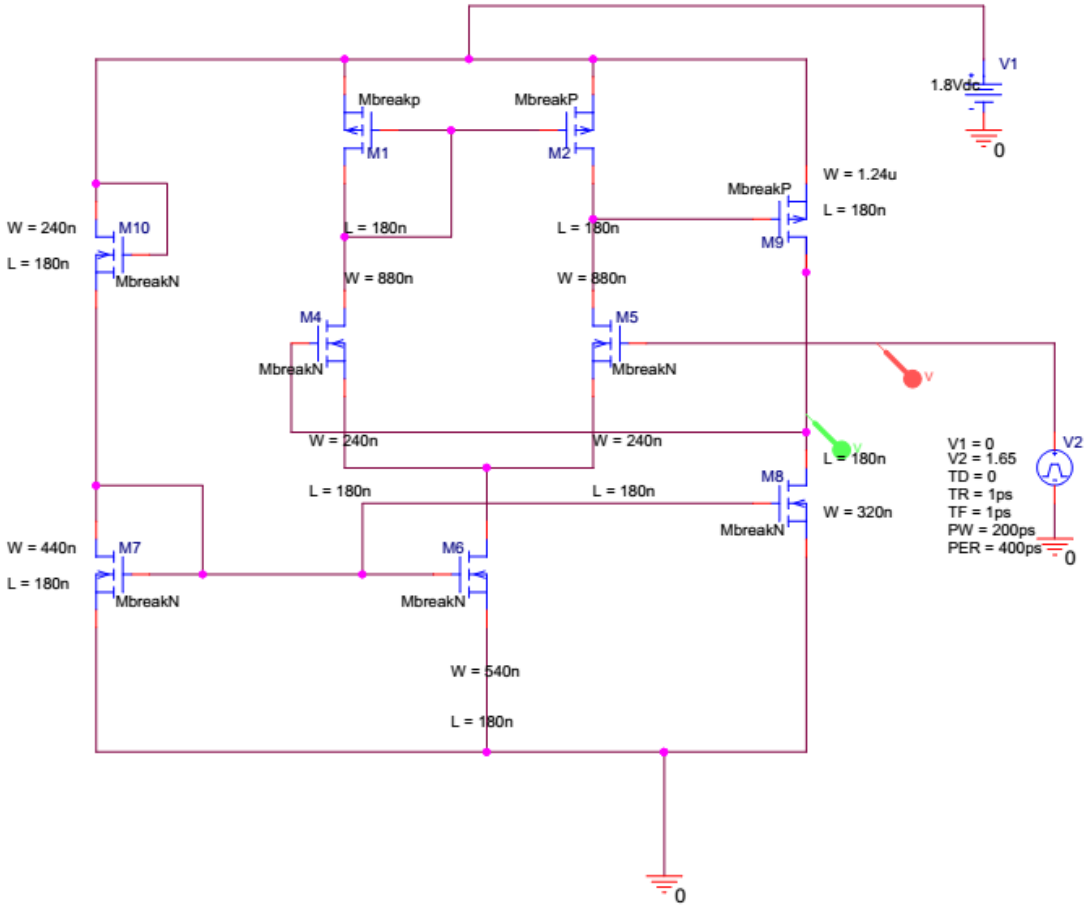


Fig 3.5 Schematic of two stage conventional op-amp

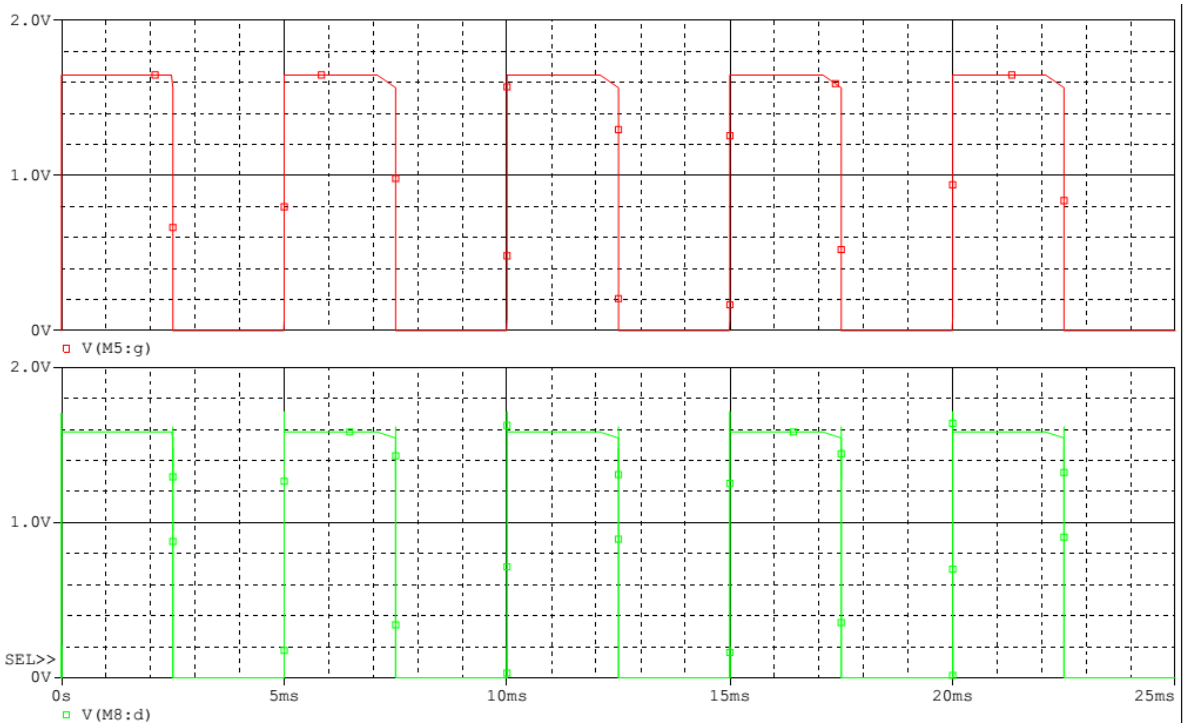


Fig 3.6 input and output of conventional op-amp at 200Hz input

Figure 3.6 shows the output of the conventional op-amp when a 200Hz square wave is given as input. This allow us to observe the response of the circuit at lower frequencies. From this we observe that the output is following input justifying the functioning of voltage follower. In this case slew rate, delay cannot be obtained. A much higher frequency input is required to estimate exact slew rate and delay.

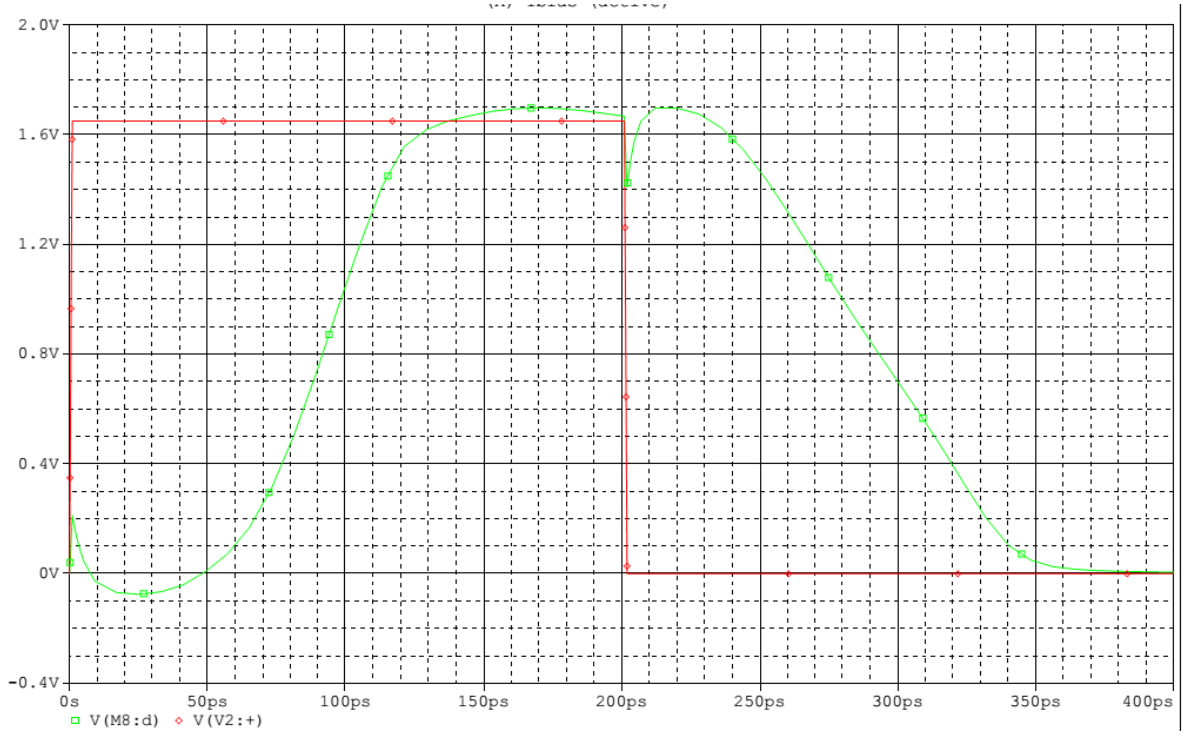


Fig 3.7 input and output of conventional op-amp at 2.5GHz

Figure 3.7 shows the output of the conventional op-amp when a 2.5GHz square wave is given as input. This allow us to observe the response of the circuit at higher frequencies. From this we observe that the output is following input justifying the functioning of voltage follower but with a certain rise and fall time. In this case slew rate, delay can be obtained. Higher slew rate specifies the ability of the circuit to work at higher frequencies.

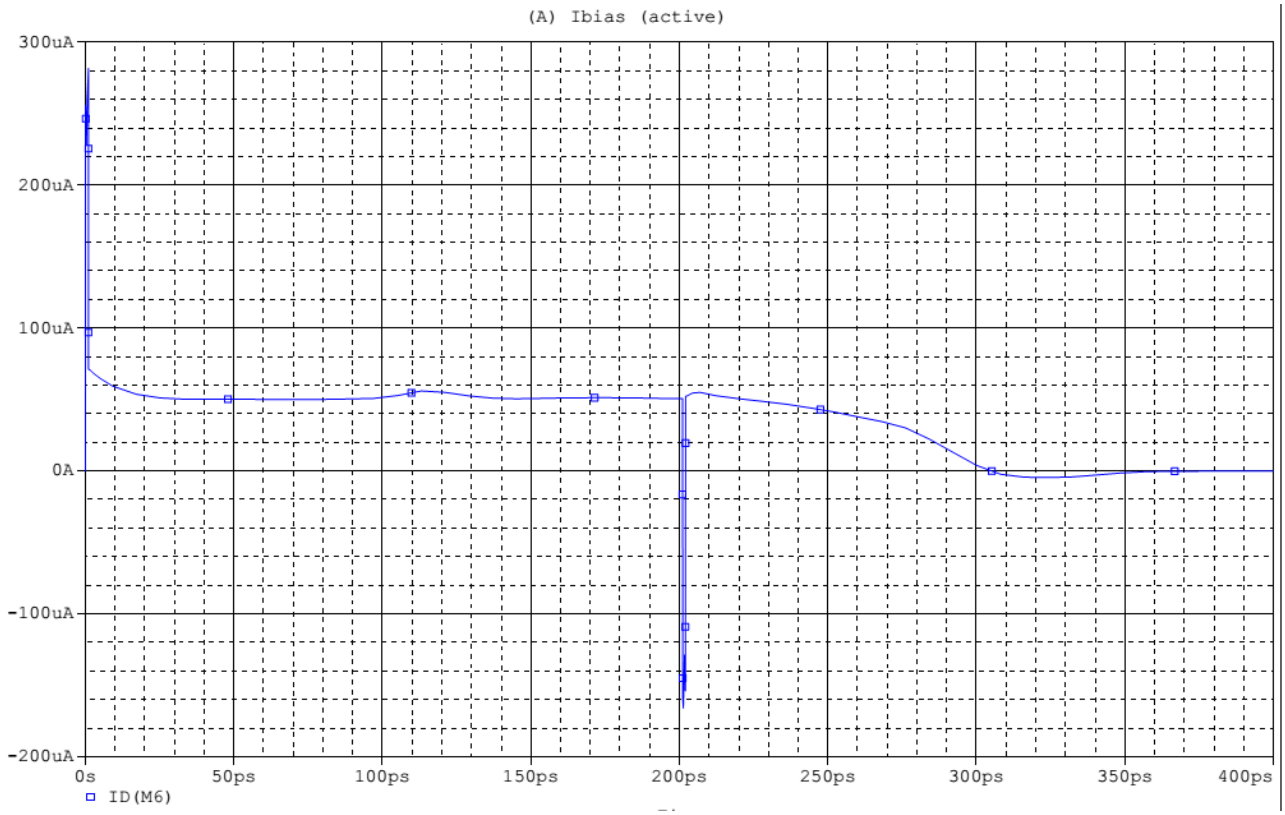


Fig 3.8 Bias current of conventional op-amp

Figure 3.8 gives the variation of bias current with respect to time. It is clearly seen that even though output reaches input voltage, still the bias current is flowing in the circuit. This is the main source of leakage power consumption.

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 ****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C


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(N22091)    1.7679 (N22099)    1.7679 (N22103) 4.999E-09 (N22125)    1.8000

(N22191)    0.0000 (N22219) 19.95E-09



    VOLTAGE SOURCE CURRENTS
    NAME         CURRENT

    V_V1        -3.058E-04
    V_V2         0.000E+00

    TOTAL POWER DISSIPATION   5.50E-04  WATTS



          JOB CONCLUDED

**** 05/04/16 00:04:35 ****** PSpice 16.5.0 (April 2011) ****** ID# 0 ********

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6

Fig 3.9 Power consumption of conventional op-amp

Figure 3.9 gives the total power dissipation of CMOS op-amp. From the bias current plot, majority contribution of total power is leakage power and it is due to leakage current. Efforts should be taken to minimize the leakage current and at the same time slew rate has to be improved. Power dissipation is obtained from the simulation output file.

3.4.1 Observations

The parameters obtained from the simulations performed are tabulated below

Table 2 parameters obtained for conventional op-amp

	Slew rate V/ns	I_{BIAS}(max) uA	Delay (ps)	P.D (W)
Conventional op-amp	8.65	240	123	$5.5x10^{-4}$

3.5 Adaptively Biased Two Stage CMOS Operational Amplifier

In [2], author demonstrates a method which uses an Adaptive biased differential amplifier stage for biasing. When operational amplifier is designed as a Buffer, the output signal gets distorted even at low frequencies and it does not follow the input signal. To resolve this issue the designers need to go for alternative biasing schemes. When the operational amplifier is designed using this adaptive biasing technique and pulse input is given it, the new circuit provides a distortion-less output even at higher frequencies [3]. This improves the Slew-Rate of the operational amplifier. The input/output characteristic of the design is discussed.

As we have discussed through different kind adaptive biasing techniques and came to know their advantages and disadvantages, in this adaptive biasing technique, methodology is simple and easily implementable to the many of the operational amplifier circuits. In [3], author presents a high slew-rate CMOS operational amplifier. It uses an external circuit to shoot up large bias current into the conventional CMOS differential input stage, in the presence of large differential input signals. This measure considerably increases the slew-rate of the operational amplifier for a given quiescent current. In [4], the author explains the programmable slew-rate operational amplifier which uses digital signals to control the range of the slew-rate. To implement [3] and [4], large number of transistors are required, which consumes more power and thus more area.

To achieve higher Slew-Rate, we have discussed several design techniques [3] [4] [5]. All the designed techniques use more number of additional transistors, which in turn results more complex circuits. When compared to its counterparts this design [2] has the following advantages, like simple circuitry, less area(less number of components) and higher Slew-Rate.

3.5.1 Adaptive Biasing Circuitry

The adaptive biasing circuitry is shown in fig 3.10

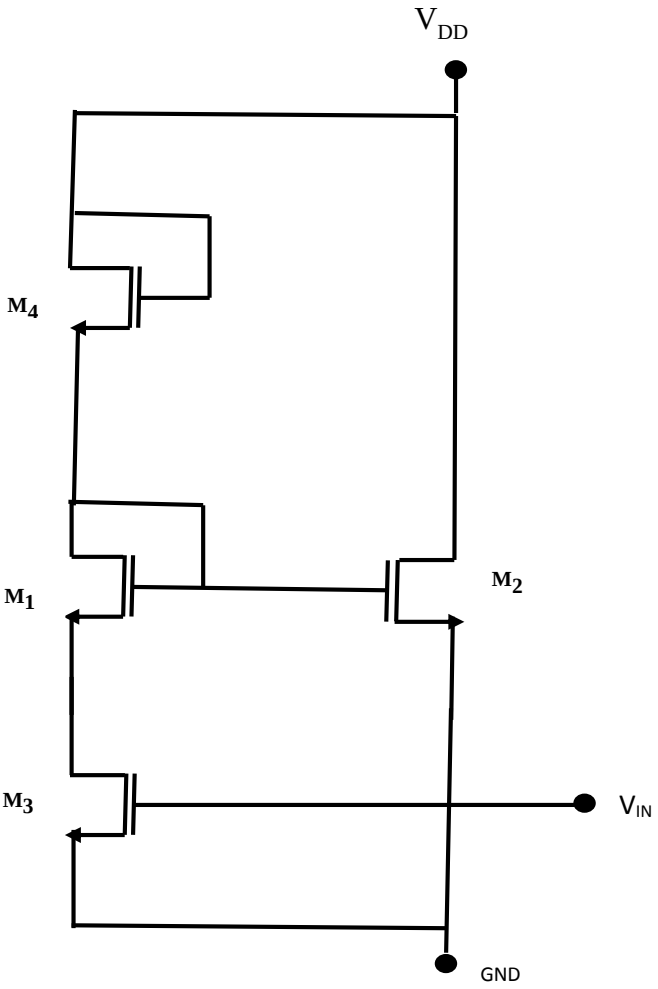

Fig 3.10 Adaptive biasing circuitry

If we observe the above fig, an additional transistor M3 is connected to the current mirror part of the op-amp. This additional transistor is responsible for the dependence of bias current on the input signal. The input signal of op-amp buffer is given to gate of M3.

Main objective of this method is to improve slew rate. For that, bias current has to be increased because slew rate is directly proportional to bias current. To increase bias current there is a need of additional circuitry in the current mirror path. In this regard, M3 is added to the current mirror path. When input is applied to the op-amp, M3 transistor operates in saturation region (input to op-amp is connected to gate of M3) maximum bias current flows through the op-amp. When input is zero, transistor M3 comes to OFF state and no current flows in the path. This is

called adaptive biasing as bias current becomes variable to input signal amplitude. This provides high biasing current when input is high.

The drawback in this method is even though output reaches the input voltage, still the bias current flows in the circuit. That means leakage current is not reduced in this method. It concentrates mainly on improving slew rate. The adaptively biased op-amp is shown below in fig 3.11

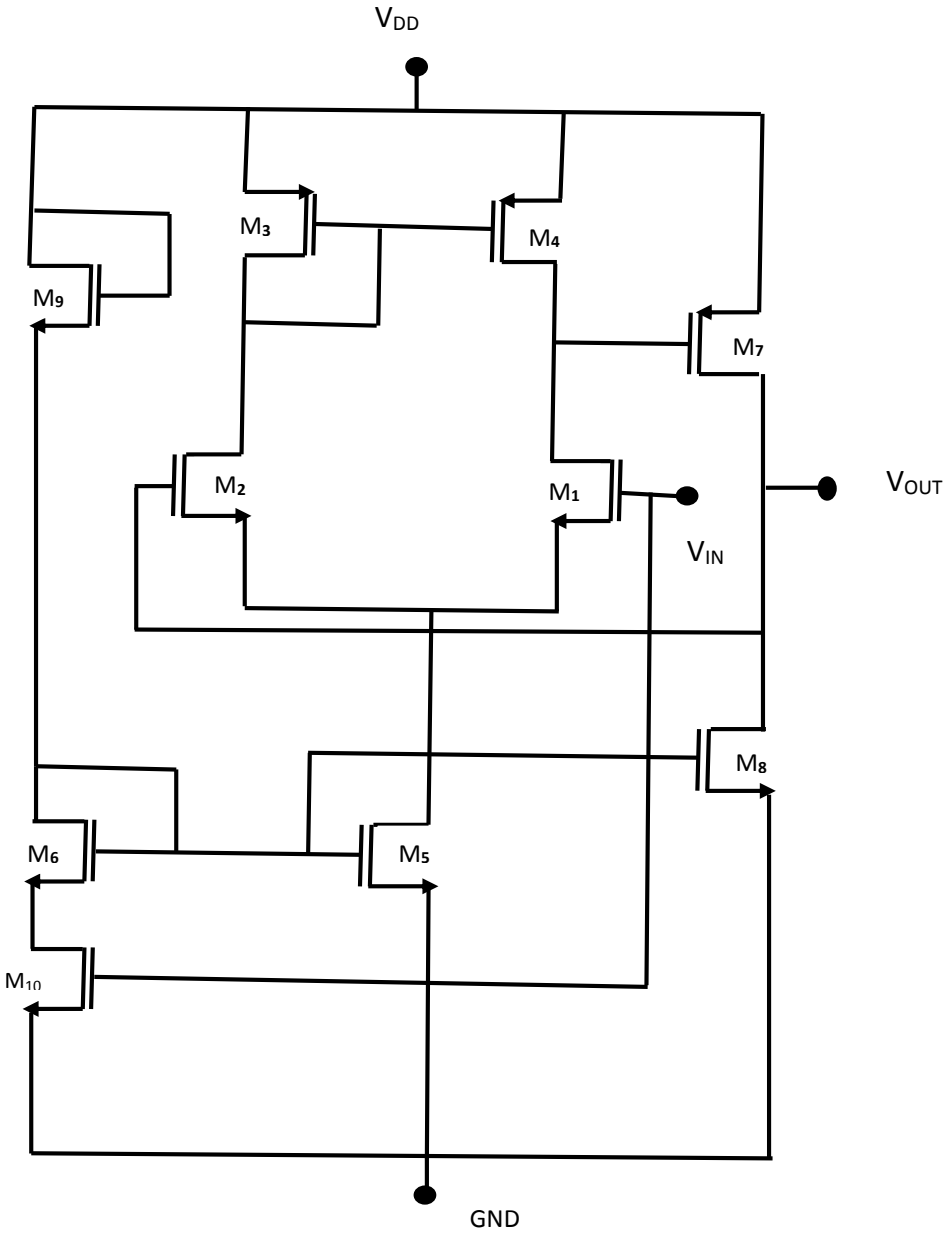

Fig 3.11 Adaptively biased conventional two stage CMOS op-amp

The above discussed additional circuitry is connected to the conventional op-amp is shown in fig 3.11

The standard equation of reference current (bias current) is given by

$$I_{ref} = \frac{1}{2} K_n' \frac{W}{L} (V_{gs} - V_t)^2$$

Where W=width of the MOS

L=channel length of the MOS

V_{gs}=gate to source voltage

V_t=threshold voltage

K_n'= Trans-conductance parameter

3.6 Simulation Results of Adaptively Biased Op-Amp

The adaptively biased CMOS Op-amp shown in the Fig 3.11 is designed in TSMC 180 nm technology with supply voltage of 1.8 V. The simulation of this Op-amp is done by PSPICE circuit simulator. Here we applied a square input signal of 1.65V at a frequency of 200Hz at the non-inverting input of Op-amp. The power consumption of the Op-amp will be found out from the transient analysis.

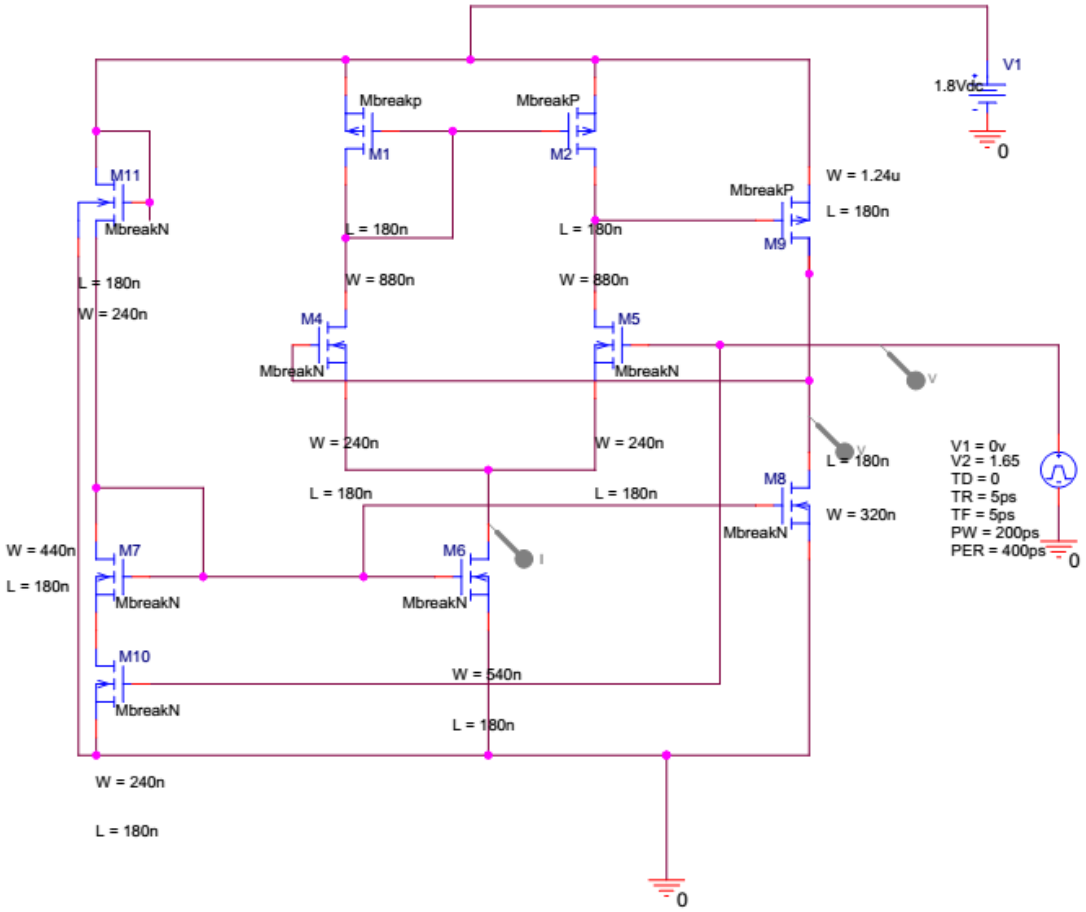

Fig 3.12 schematic of adaptively biased CMOS op-amp

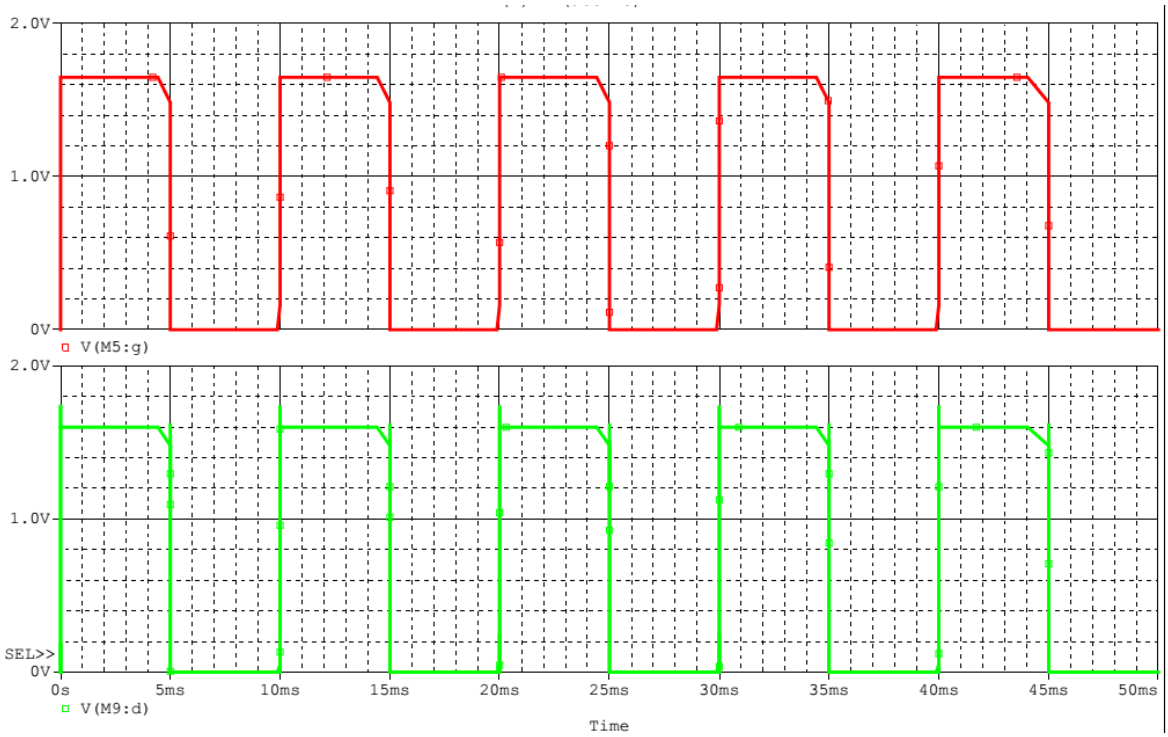

Fig 3.13 input and output of adaptively biased CMOS op-amp at 100Hz

Figure 3.13 shows the output of the adaptively biased op-amp when a 100Hz square wave is given as input. This allow us to observe the response of the circuit at lower frequencies. Input is applied with a small rise and fall times of 5ps and a negligible delay.

From this we observe that the output is following input justifying the functioning of voltage follower. In this case slew rate, delay cannot be obtained. A much higher frequency input is required to estimate exact slew rate and delay.

The main intention is to study the adaptive biased design technique for the CMOS Operational Amplifiers. Compared to the Slew-Rate of the conventional CMOS Operational Amplifier, this new configuration gives an improved Slew-Rate.

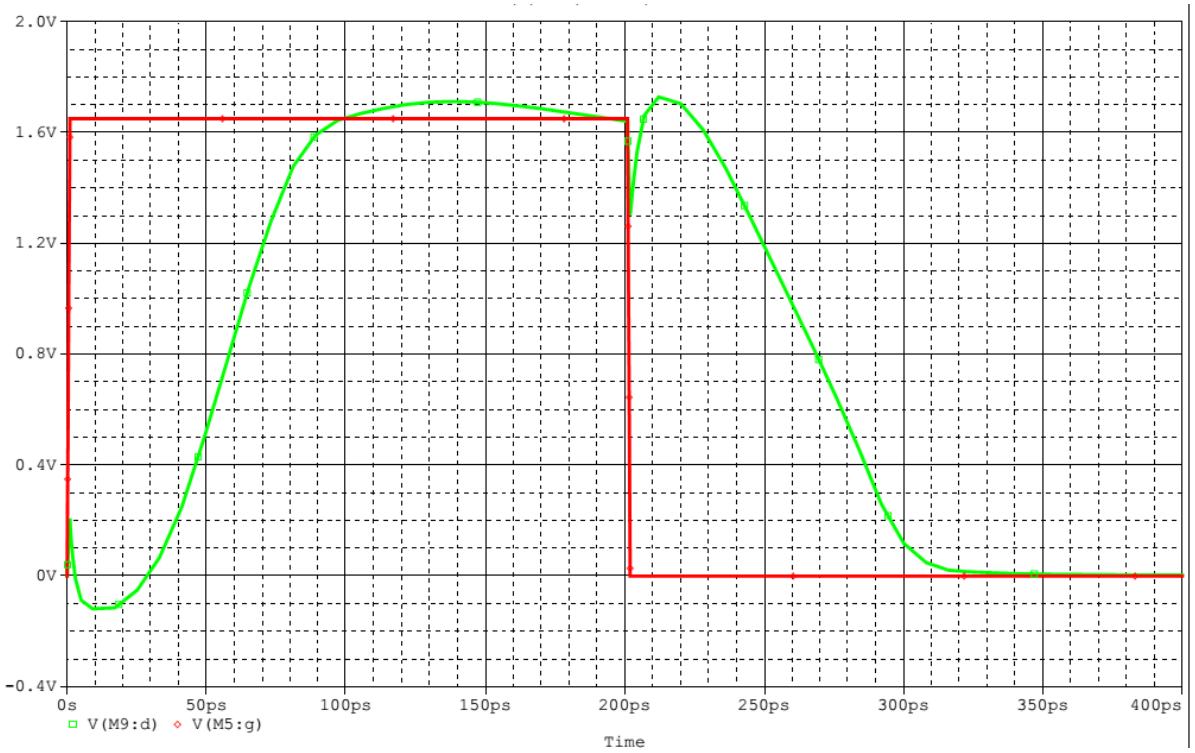

Fig 3.14 input and output of adaptively biased CMOS op-amp at 2.5GHz

Figure 3.14 shows the output of the adaptively biased op-amp when a 2.5GHz square wave is given as input. This allow us to observe the response of the circuit at higher frequencies. The maximum Slew-Rate achieved by this design is 13V/nS, which is 40% more than the conventional op-amp. Also it uses less number of MOS transistors and less Area.

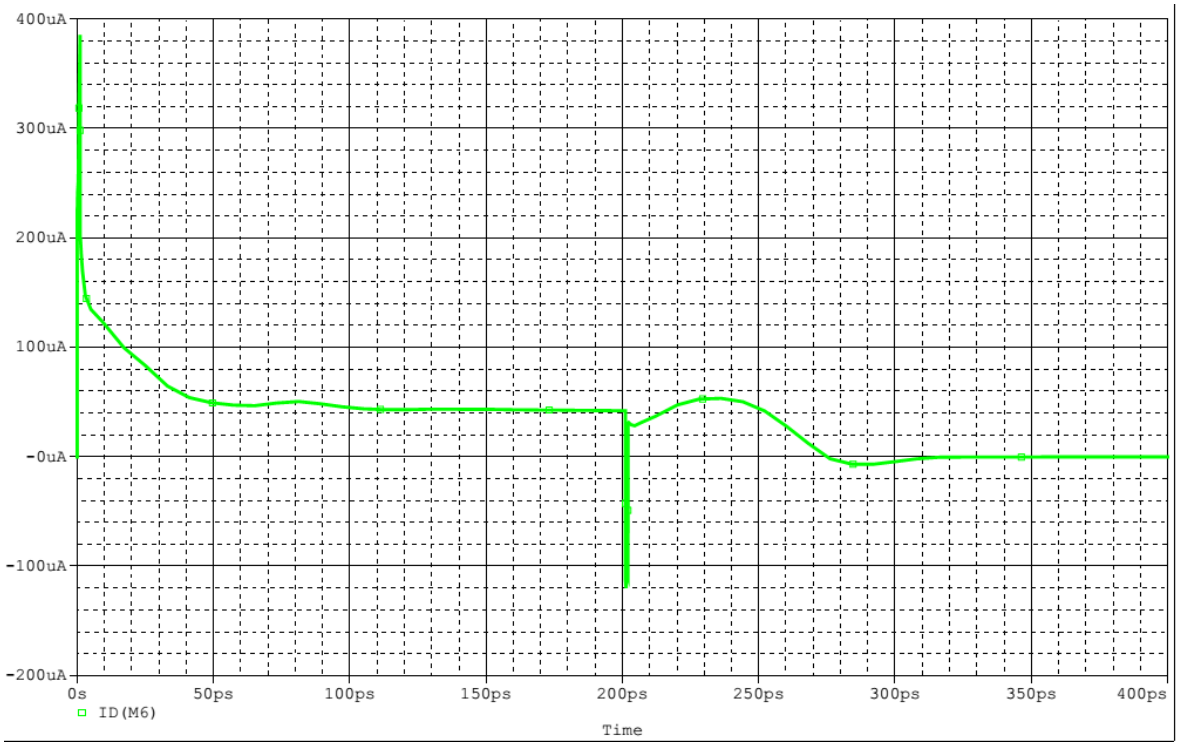

Fig 3.15 Bias current of adaptively biased CMOS op-amp

Figure 3.15 gives the variation of bias current with respect to time. It is clearly seen that even though output reaches input voltage, still the bias current is flowing in the circuit. This is the main source of leakage power consumption.

This happens due to conduction of transistor M10 even though output reaches input in the time period between 0 to 200ps.

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 ****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C


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(N02438)    1.8000 (N04978) 15.22E-09 (N08191)    0.0000 (N022700)    1.3851



    VOLTAGE SOURCE CURRENTS
    NAME         CURRENT

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    V_V2         0.000E+00

    TOTAL POWER DISSIPATION   3.58E-11  WATTS


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 ****     JOB STATISTICS SUMMARY


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Fig 3.16 Total power consumption of adaptively biased CMOS op-amp

Figure 3.16 gives the total power dissipation of CMOS op-amp. From the bias current plot, majority contribution of total power is leakage power and it is due to leakage current. Efforts should be taken to minimize the leakage.

3.6.1 Observations

The parameters obtained from the simulations performed are tabulated below

Table 3 parameters obtained for adaptively biased op-amp

	Slew rate V/ns	I_{BIAS}(max) uA	Delay (ps)	P.D (W)
Adaptively biased op-amp buffer	13	390	66	3.58×10^{-11}

3.7 Modified NMOS Topology for Adaptive Biasing

In this technique [4], a CMOS adaptive biasing NMOS topology for low power applications is presented. The circuit gives an output current which is dependent on the applied input differential voltage. This method can be employed in low power operational amplifiers, where a dynamic bias current helps to save power dissipation.

Some of the CMOS adaptive biasing circuits have been proposed for low power applications to give low bias current without reducing the driving capability of the circuit [2] [3] [6] [7]. In [5] [6], the differential stage has a current source contributed by two terms. One is constant term, and the second term depends on the input differential voltage. The adaptive biasing circuitry is instituted by a pair of current mirrors that perform the difference between the currents that flow through the two branches of the differential pair. This process allows to obtain good performance in linearity, sensitivity and slew rate. In [2], the adaptive biasing operation is acquired by introducing a replica of the differential input stage.

The currents generated in this stage are used to adaptively change the bias current of the input stage of the op-amp. This method yields good transient performance but it works only when large signals are applied at the input. The main disadvantage of the above techniques is they need additional quiescent current therefore, additional static power dissipation.

In this section, NMOS adaptive biasing structure is presented [4]. In principle, no additional quiescent current is required, except if there is need to improve sensitivity of the circuit. This can be done by using a very small biasing current used also to compensate the threshold voltages. This circuit can be used as a basic building block where a low power consumption is necessary. In fact, the low power characteristic can be obtained by implementing a suitable topology that delivers current only if there is a differential input signal.

3.7.1 NMOS Adaptive Biasing Topology

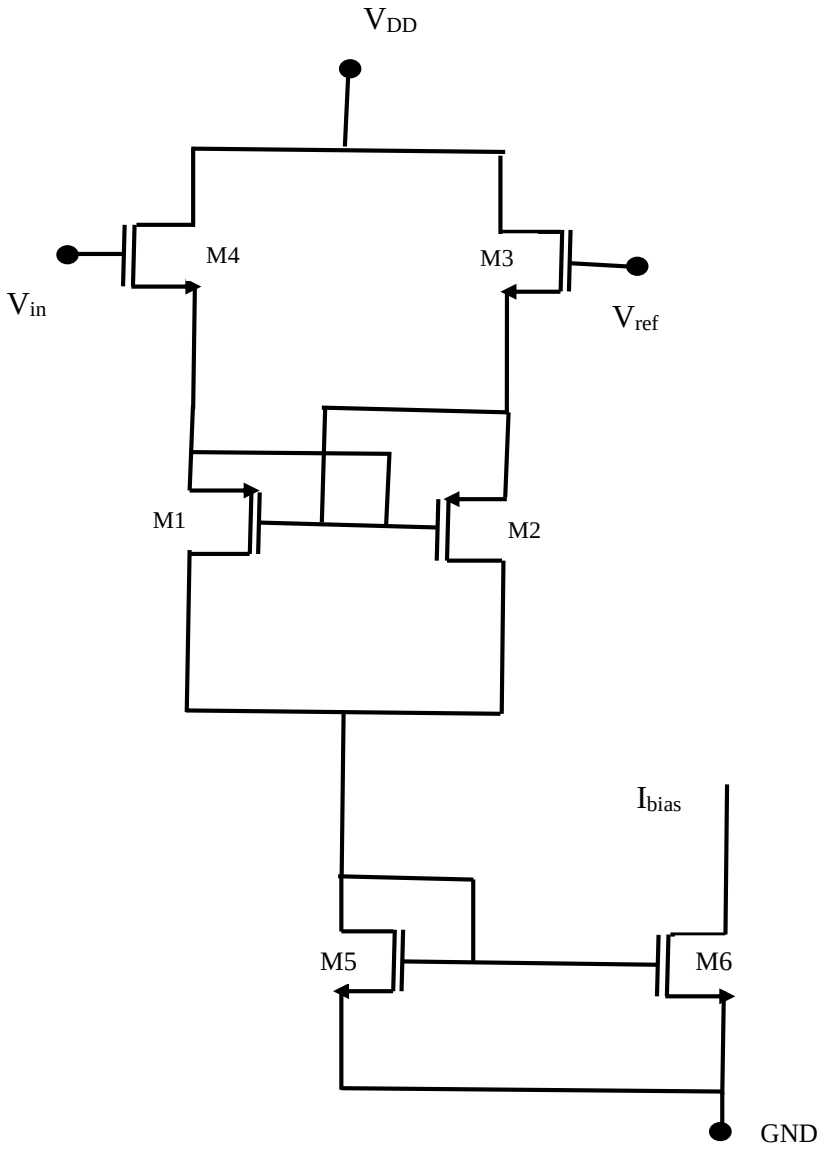

Fig 3.17 NMOS adaptive biasing topology

Figure 3.17 shows the basic NMOS topology of the circuit. It is based on the conventional NMOS input stage, but its topology has been varied in order to have output as tail current.

It is formed by an input NMOS differential pair M3, M4, two controlling transistors M1, M2 and a current mirror M5, M6 which provides the output tail current. The circuit has two inputs, voltage applied to the gate of M4 is considered as the input voltage, while a constant voltage is applied to the gate of transistor M3. In order to understand the working of above circuit, we have to study the following three cases:

1. When $V_{in}=V_{ref}$, the input transistors M3 and M4 have the same source voltage therefore gate to source voltages of M1 and M2 are equal to zero. This means that M1 and M2 are both in cut-off state, and zero output current will flow in the current mirror circuit.

2. $V_{in} < V_{ref}$ in particular $V_{ref} - V_{th,}$ we have that M1 is OFF and M2 is in ON state. In this situation, the current flowing in M5 will be given by the contribution of the current flowing through M2, which is constant because V_{ref} is constant external voltage.
3. $V_{in} > V_{ref}$ in particular $V_{ref} + V_{th}$ M1 and M4 are in ON state and the output current is given by current flowing through M1, which is proportional to square of the input voltage.

This circuit shows some drawbacks. Firstly, the fact that M1 and M2 are ON for a range of $2V_{th}$. This specifies that there is a central region of about $2V_{th}$. Where the output current is about zero. Secondly, the different biasing of M3 and M4 leads to an uneven behaviour of the output tail current that can induce an intolerable distortion.

3.7.2 Modified NMOS Adaptive Biasing Topology

To solve the distortion problem faced in NMOS topology, the circuit is modified by introducing some alterations as shown in fig 3.18. A voltage polarization of V_{TH} has given to the transistors M1 and M2. This can be done by connecting additional transistors M7 and M8 as shown in fig 3.18. The working of modified circuit is given as

1. In this case, for $V_{in}=V_{ref}$, the output current is non-zero and given by current sources, whose value can be fixed as low as possible to maintain the transistors at the edge of the cut-off region. This eliminates the distortion problem faced in NMOS topology
2. $V_{in} < V_{ref}$ we have that M1 is OFF and M2 is in ON state. In this situation, the current flowing in M5 will be given by the contribution of the current flowing through M2, which is constant because V_{ref} is constant reference voltage.
3. $V_{in} > V_{ref}$, M1 and M4 are in ON state and the output current is given by current flowing through M1, which is proportional to square of the input voltage.

The minimum value of the output current can be set from the current mirrors by adjusting the mirror ratios.

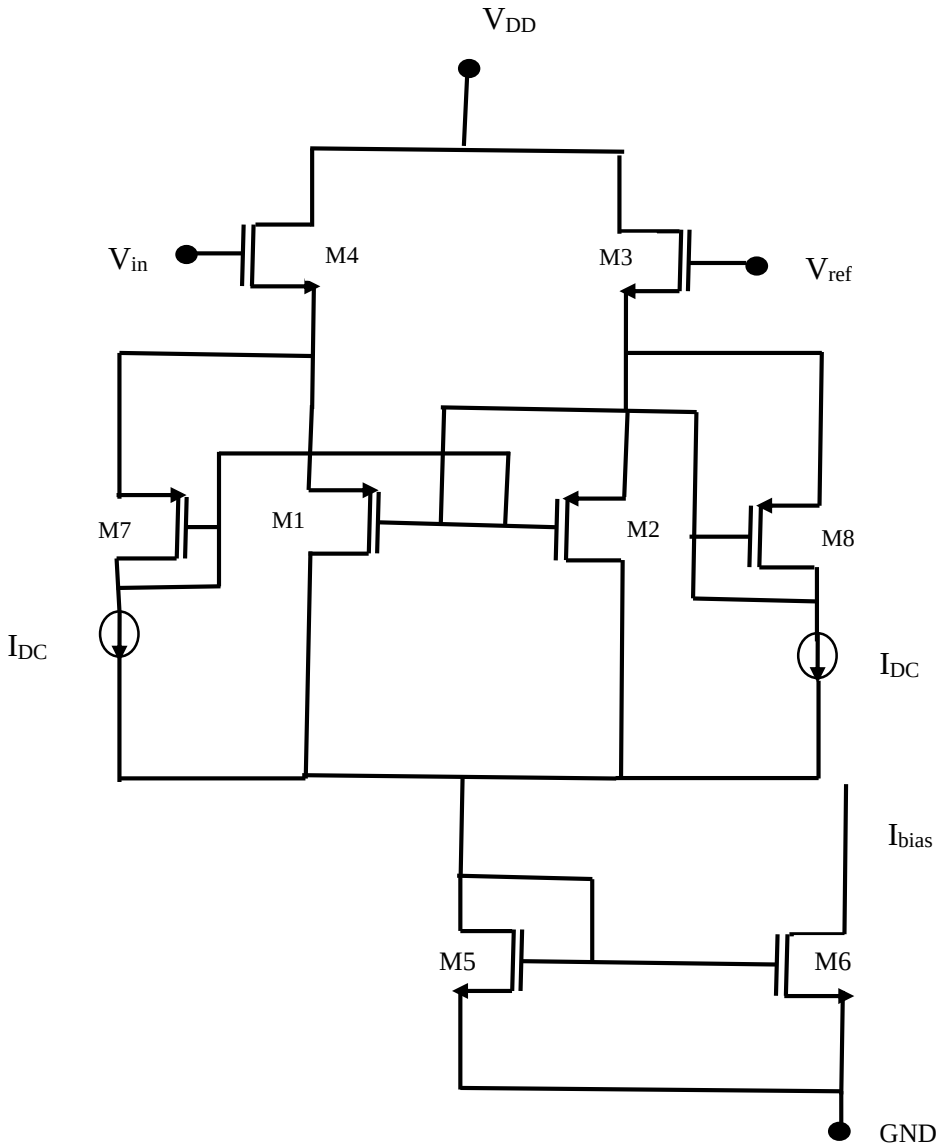

Fig 3.18 modified NMOS adaptive biasing

3.8 Simulation Results of Modified NMOS Adaptive Biasing Topology

The schematic of modified NMOS adaptive biasing topology is shown in the Fig 3.19 is designed in TSMC 180 nm technology with supply voltage of 3V. The simulation of this topology is done by PSPICE circuit simulator. Here we applied a reference input of 1.2V and V_{in} is varied from 0V to 1.8V.

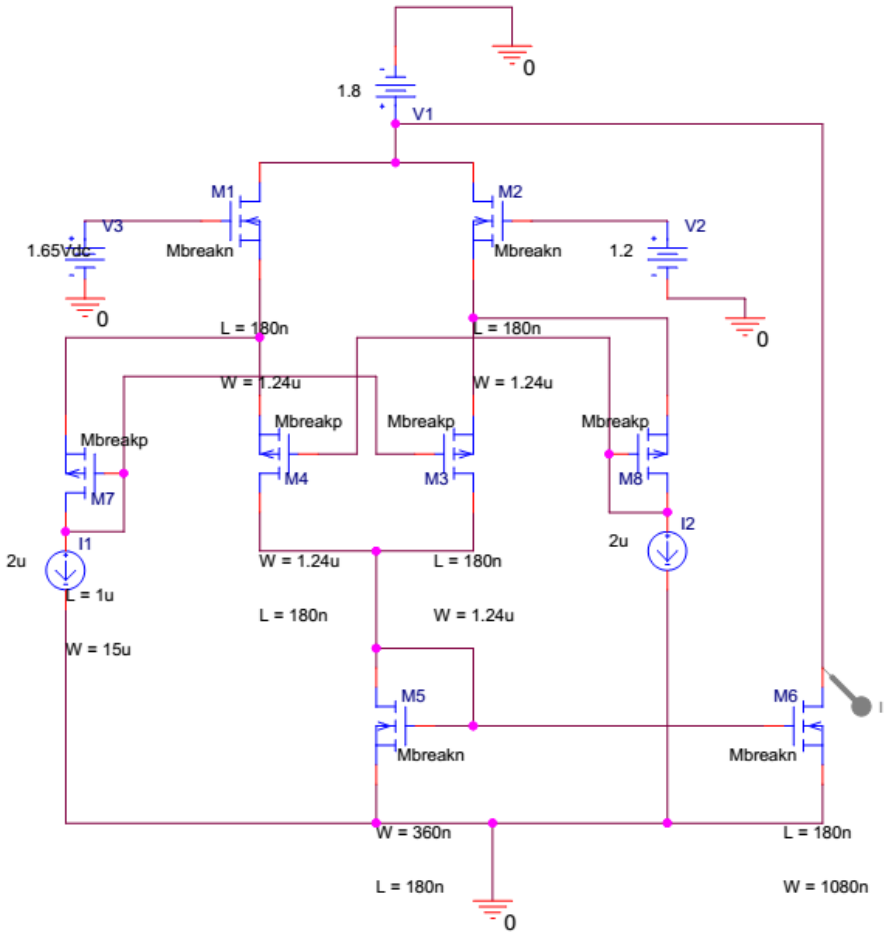

Fig 3.19 schematic of modified NMOS adaptive biasing topology

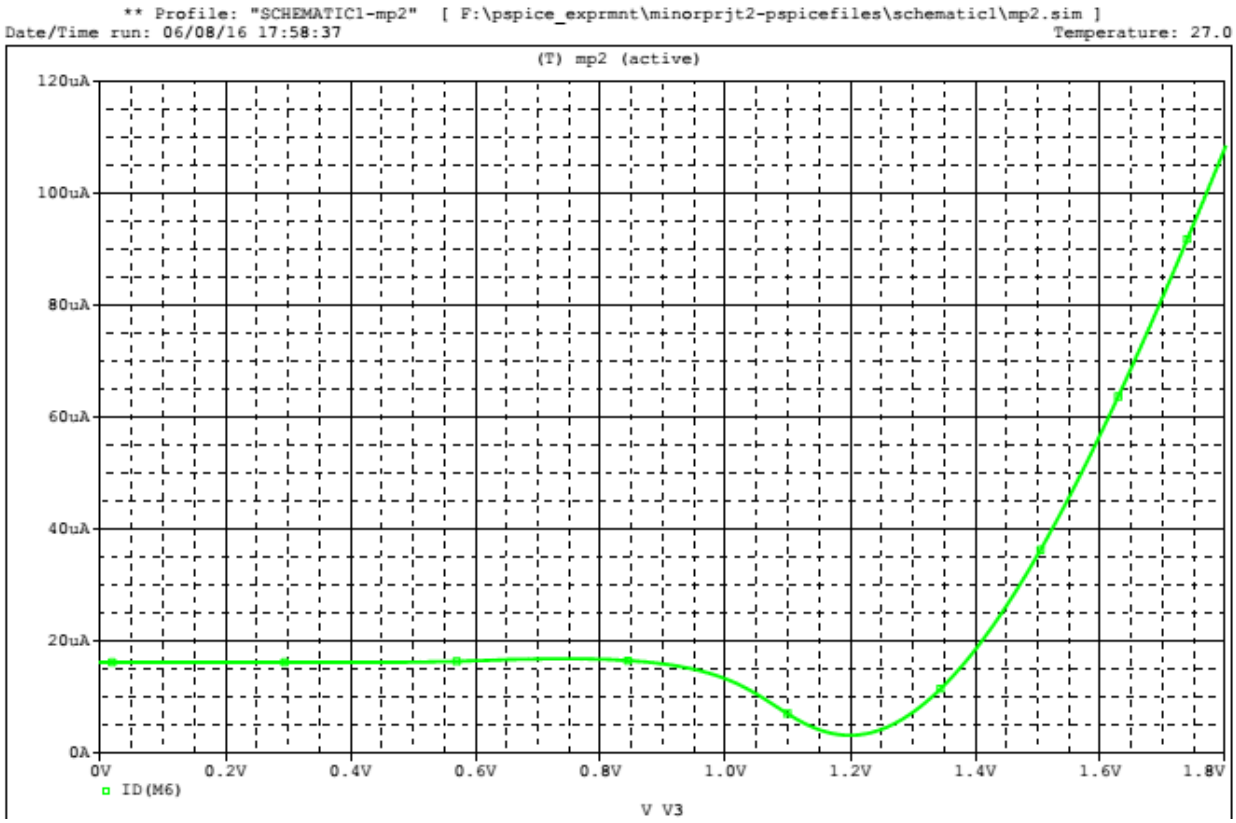

Fig 3.20 output bias current of modified NMOS adaptive biasing topology

The three cases discussed in working of modified NMOS topology (3.7.2) is justified from the fig 3.20. It shows the variation of bias current with input voltage.

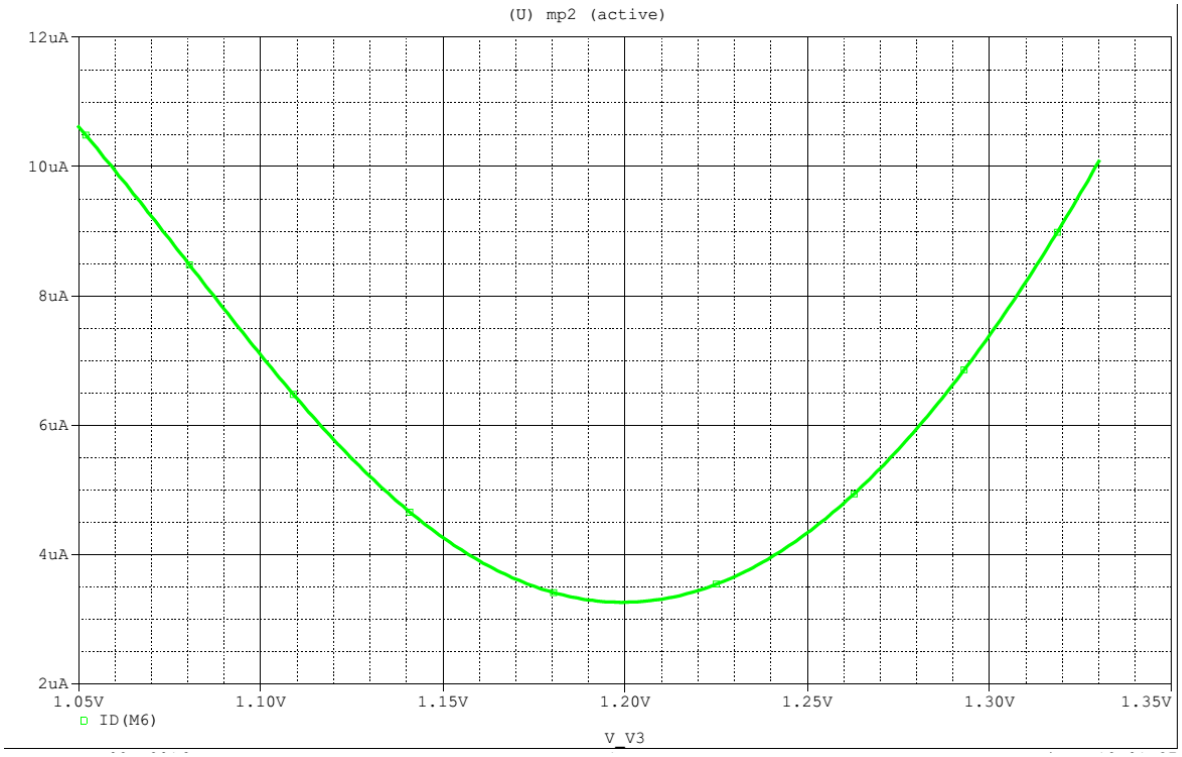

Fig 3.21 variation of output bias current with input differential voltage

As we clearly observe in fig 3.21, the current through the transistor M8 (output of current mirror) never becomes zero. Even though input signals are same, minimum amount of current flows through the current mirror to operate M1 and M2 near to cut-off region. The DC current sources prevents transistors M1 and M2 from going into deep cut-off region. This property of modified NMOS topology solves the problem of distortion.

3.9 CMOS Op-amp Using Modified NMOS Adaptive Biasing Topology

Modified NMOS topology is used in analog CMOS circuits specifically in circuits having differential input stage. The input of the analog block iso given as inputs to the input terminal of NMOS topology and a DC voltage is given as reference input of NMOS topology. The output bias current of NMOS topology is given as bias current to the analog block. Here we are connecting this modified NMOS topology to a CMOS voltage follower.

3.10 Simulation Results

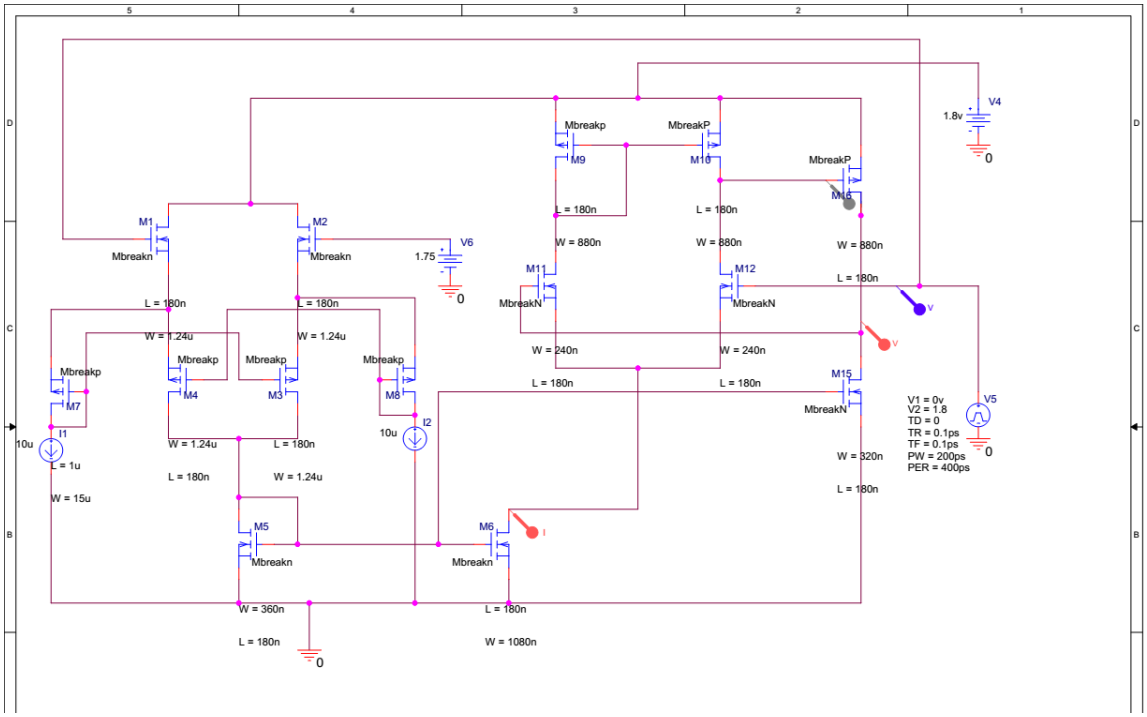

Fig 3.22 schematic of op-amp using modified NMOS AB topology

Here reference voltage is given to supply voltage of 1.8v. When input is zer0, the difference between the inputs of NMOS topology is 1.8V. So a huge amount of current flows in the circuit. When the output of op-amp reaches 1.8V, the differential input applied to NMOS topology becomes zero and no current flows in the circuit although negligible current is allowed to flow to avoid distortion.

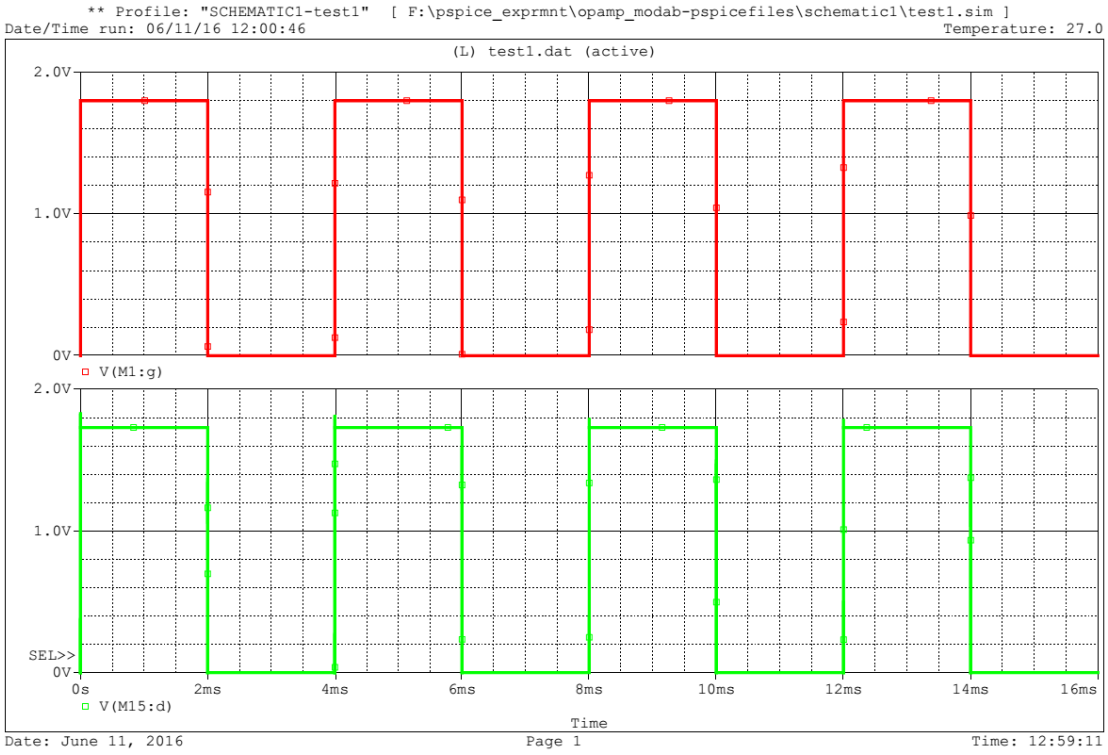

Fig 3.23 input output characteristics

Figure 3.23 shows the output of the adaptively biased op-amp using NMOS topology when a 250Hz square wave is given as input. This allow us to observe the response of the circuit at lower frequencies. Input is applied with a small rise and fall times of 0.1ps and a negligible delay.

From this we observe that the output is following input justifying the functioning of voltage follower. In this case slew rate, delay cannot be obtained. A much higher frequency input is required to estimate exact slew rate and delay.

The main intention is to study the adaptive bias using modified NMOS topology for the CMOS Operational Amplifiers. Compared to the Slew-Rate of the conventional CMOS Operational Amplifier, this new configuration gives an improved Slew-Rate.

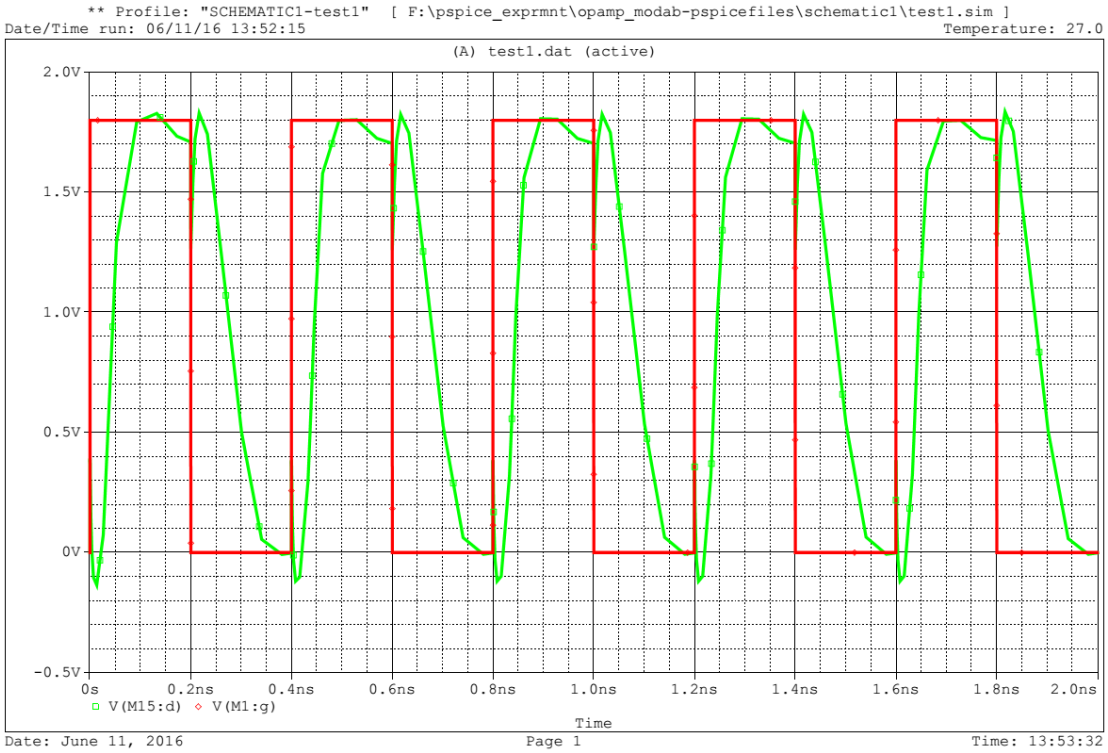

Fig 3.24 input output characteristics at 2.5GHz

Figure 3.24 shows the output of the adaptively biased op-amp when a 2.5GHz square wave is given as input. This allow us to observe the behaviour of the circuit at higher frequencies.

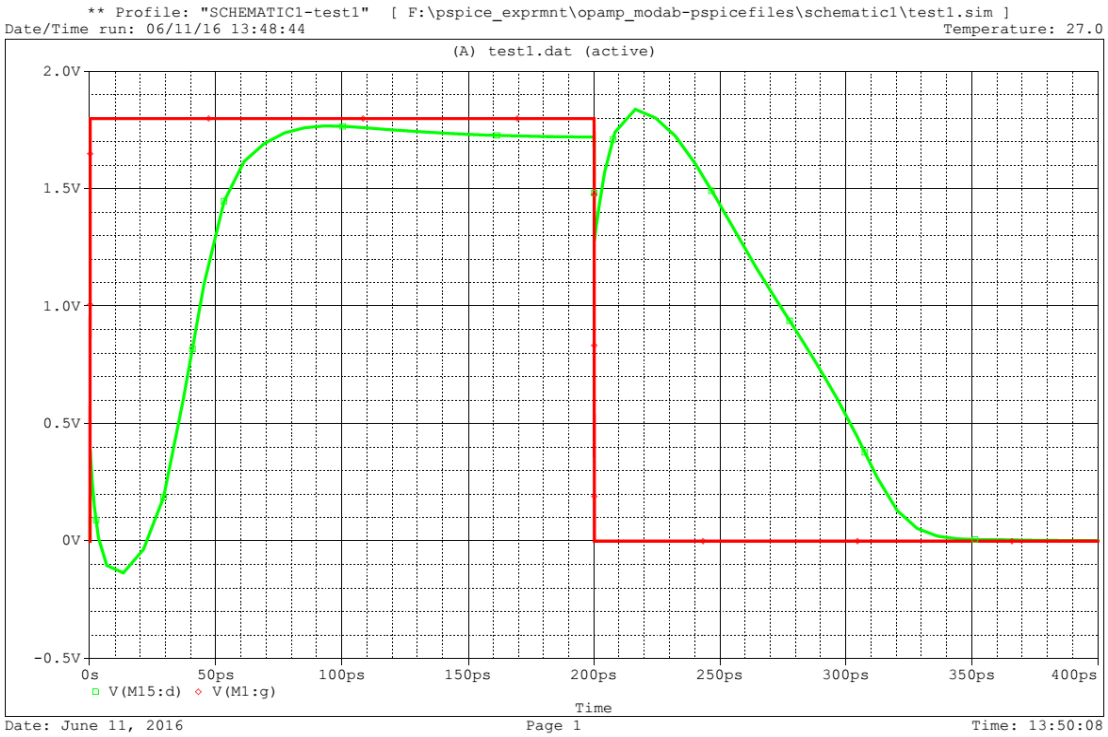

Fig 3.25 waveform for calculation of slew rate

Figure 3.25 is the magnified version of fig 3.24 which is used for calculating the transient parameters like slew rate, delay, rise time and fall time.

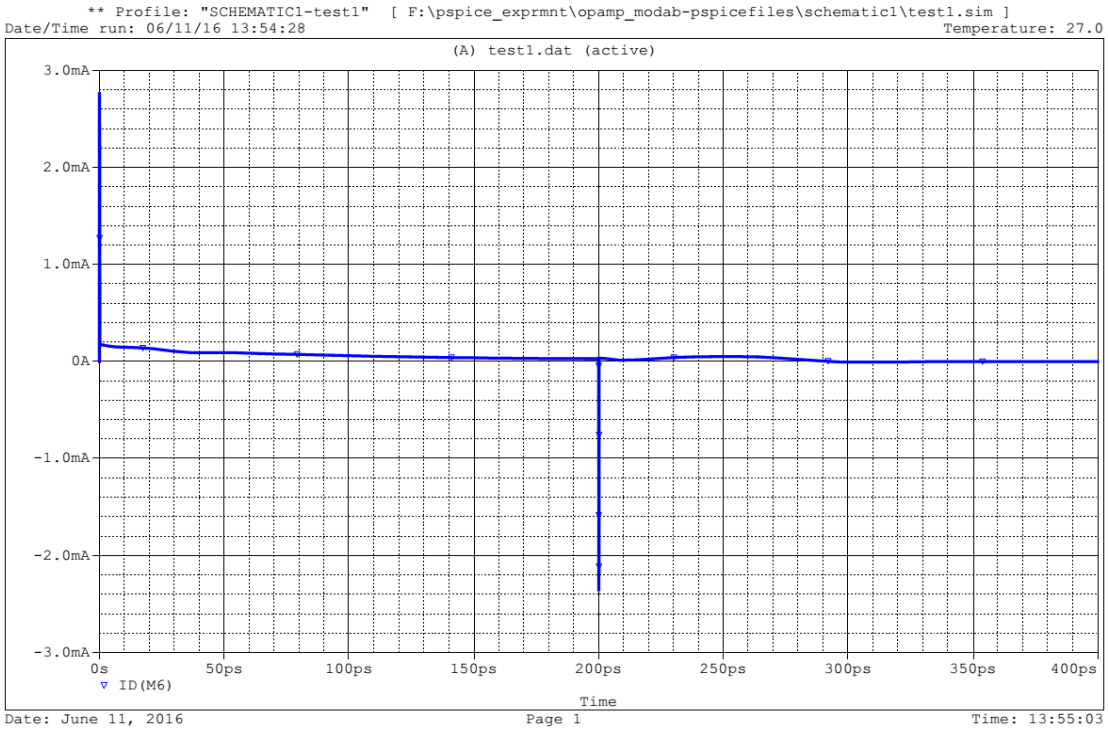

Fig 3.26 bias current

Figure 3.26 gives the variation of bias current with respect to time. It is clearly seen that when output reaches input voltage, the bias current is negligible in the circuit. This is the main reason for reduction in leakage current when output reaches input voltage.

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                                F:\pspice_exprmnt\opamp_modAB-PSpiceFiles\SCHEMATIC1\test1\test1.out

 ****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C


 ********************************************************************************


 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(N19012)    1.7679 (N19020) 7.222E-09 (N19072)    1.8000 (N19080)    1.7679

(N19188)    0.0000 (N19200) 28.65E-09 (N21278)     .8878 (N30968)     .4661

(N30972)    1.0471 (N30976)    -.2255 (N30984)     .3555



     VOLTAGE SOURCE CURRENTS
     NAME         CURRENT

     V_V4        -6.519E-05
     V_V5         0.000E+00

     TOTAL POWER DISSIPATION   1.17E-04  WATTS



          JOB CONCLUDED
```

Fig 3.27 power dissipation

Power dissipation is increased considerably because large amount of bias current flows within a short span of time. This leads to increase in power consumption at the cost of improved transient parameters.

3.10.1 Observations

The parameters obtained from the simulations performed are tabulated below

Table 4 parameters obtained for adaptively biased op-amp using modified NMOS topology

	Slew rate V/ns	I_{BIAS}(max) mA	Delay (ps)	P.D (W)
CMOS voltage follower using modified NMOS adaptive biasing topology	31.4	2.8	60.5	1.17×10^{-4}

CHAPTER 4

PROPOSED ADAPTIVELY BIASED CMOS OPERATIONAL AMPLIFIER

4.1 Introduction

The circuit of proposed op-amp consists of two parts. First one is differential input stage and the second one is common source stage. As the single stage op-amp has a drawback of low gain, common source stage is cascaded to first stage to increase gain [20]. As we know common source stage is a tans-conductance amplifier that gives output current proportional to the input voltage. The output current is allowed to pass through a resistor or a diode connected load to generate output voltage. But the only difference between the conventional CMOS voltage buffer and the proposed model is biasing of current mirror. Instead of drawing the required current from the power supply, the current mirror draws current from the drain terminal of input transistor. The significance of this will be explained in the working.

The proposed CMOS op-amp works as voltage follower when one of its input is connected to output terminal. A step signal is applied at input to calculate the slew rate of the operational amplifier. Power consumption, delay and input bias current also observed from the simulations.

4.1.1 Working

A proposed two stage CMOS adaptively biased Op-amp is shown in the Fig 4.1. The first stage of this Op-amp is consist of M1 –M6 transistors, the second stage is consist of M7-M8 transistors. All transistors used in this Op-amp operates in saturation region. The first stage is a differential stage, the differential signal is applied into the pin and the gate terminals of the transistor M1 and M2 respectively. These transistor M1 and M2 are two NMOS driver transistors used to convert the differential voltage to differential current, these differential currents are given to the current mirrored load transistor M3 and M4. The transistor M5 and M6 are used to provide the biasing current to the differential stage.

Instead of drawing the required current from the power supply, the current mirror draws current from the drain terminal of input transistor. This idea of biasing came by observing the currents at the drain terminal of M6 and at the gate terminal of M16 in fig 3.22.These current waveforms are shown in fig 4.2 for convenience.

As the M3-M4 current mirror network provides differential current through the gate of source follower stage, there is also another way of adaptive biasing. Instead of using a separate network to generate differential current corresponding to the input voltages, it is already available at the gate terminal of second stage. This available differential current is given as reference current to the current mirror.

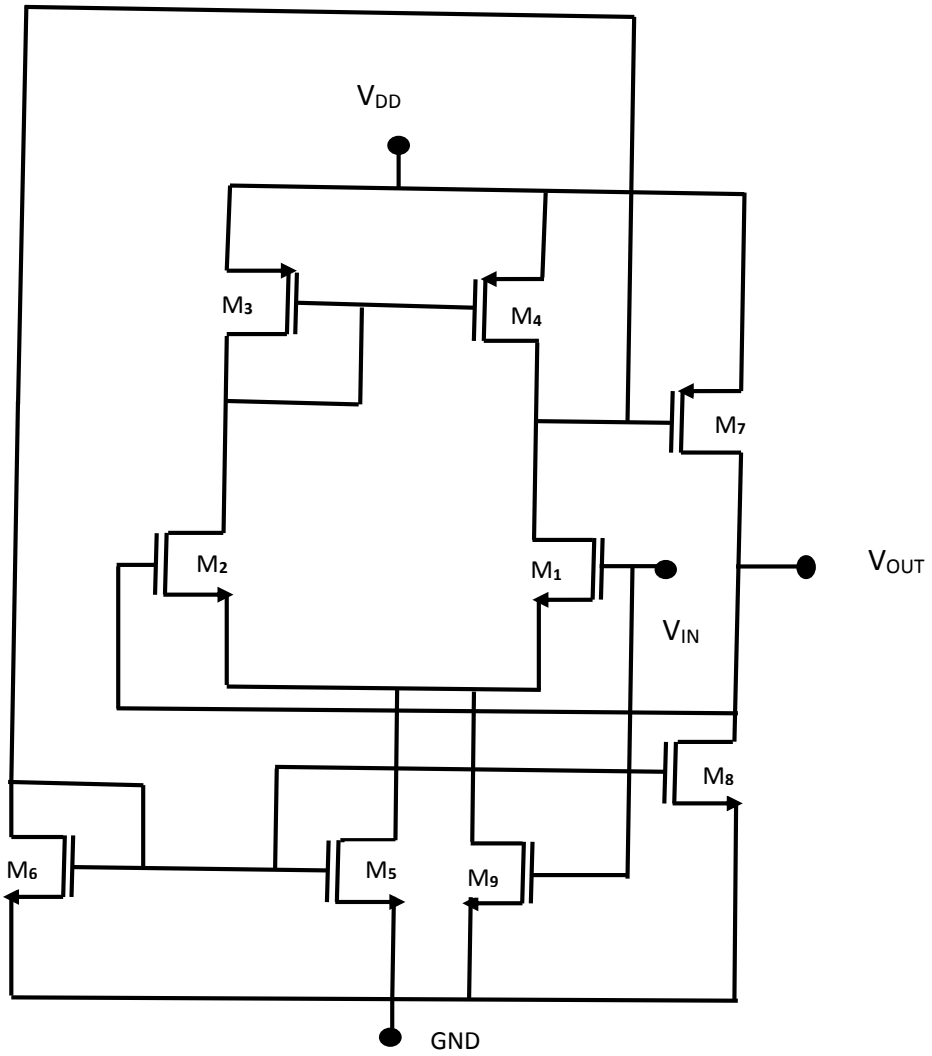


Fig 4.1 proposed adaptively biased CMOS op-amp

Here as the differential current from the input of second stage is not sufficient to achieve higher slew rate, an additional transistor M9 is included in parallel to the bias current path. The input of op-amp is given as input to M9. As it is connected in parallel, it increases the biasing current and slew rate. But the disadvantage of this additional transistor is it increases power dissipation.

When input is applied at gate of M1 in fig 4.1

i. When V_{IN} is high, the difference in the paths of M1, M2 is high. This differential current is given as input bias current through current mirror. At the same time, transistor M9 operates in saturation region and it contributes to bias current. The current through current mirror and the current through M9 constitutes bias current. This bias current drives the output towards input.

ii. When output reaches input (V_{IN} = V_{OUT}), the differential current is zero because the current generated in the path of M1, M2 are same. Therefore reference current of the current mirror is zero. Thus no bias current flows through current mirror. But as the transistor is still in saturation, there will be current flow which is called as leakage current. This current is the source of power dissipation.

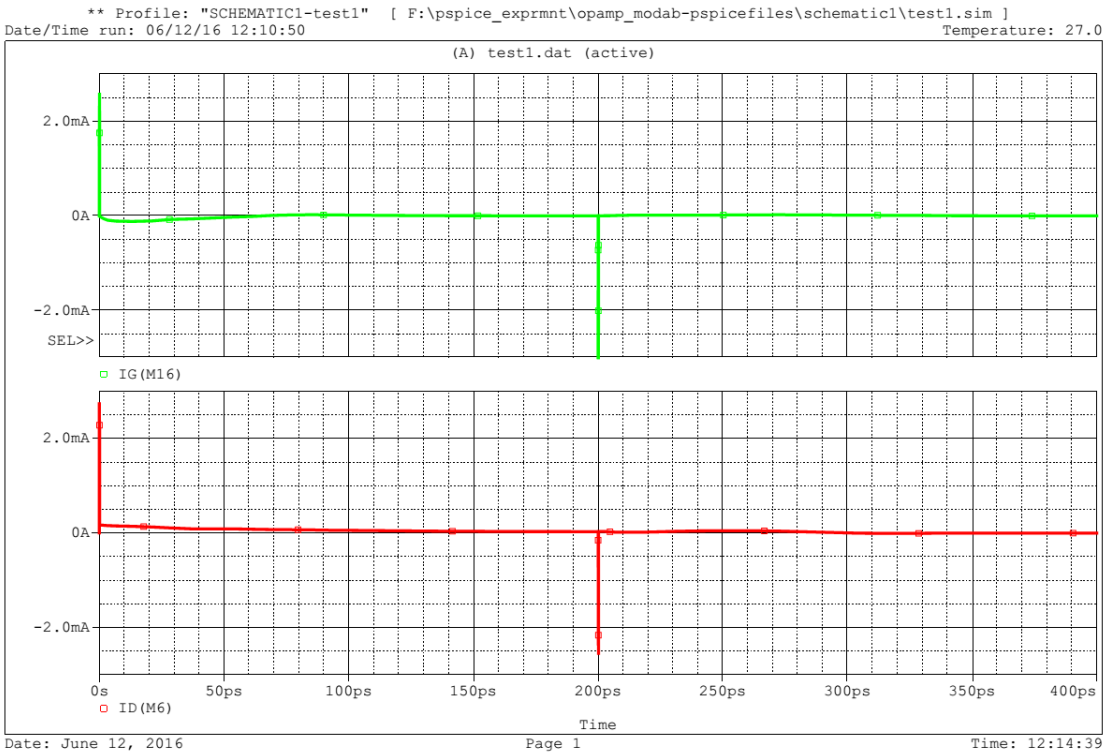


Fig 4.2 current waveforms

The idea of proposed adaptive biasing technique is developed by observing the pattern of currents from the fig 4.2. It gives the variation of the currents at the drain terminal of M6 and at the gate terminal of M16 in fig 3.22.

4.2 Simulation Results

The proposed adaptively biased CMOS Op-amp shown in the Fig 4.1 is designed in TSMC 180 nm technology with supply voltage of 1.8 V. The simulation of this Op-amp is done by PSPICE circuit simulator. Here we applied a square input signal of 1.8V at a frequency of 250Hz at the non-inverting input of Op-amp. The power consumption and slew rate are observed from the transient analysis.

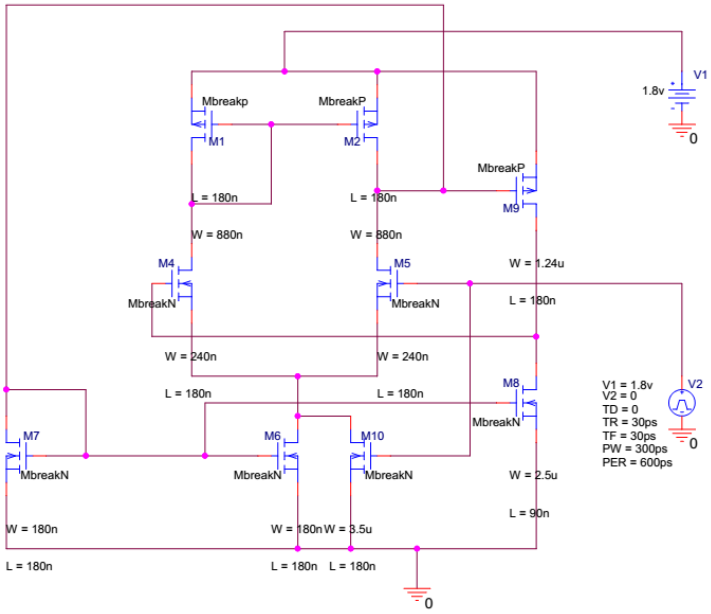


Fig 4.3 schematic of proposed CMOS op-amp

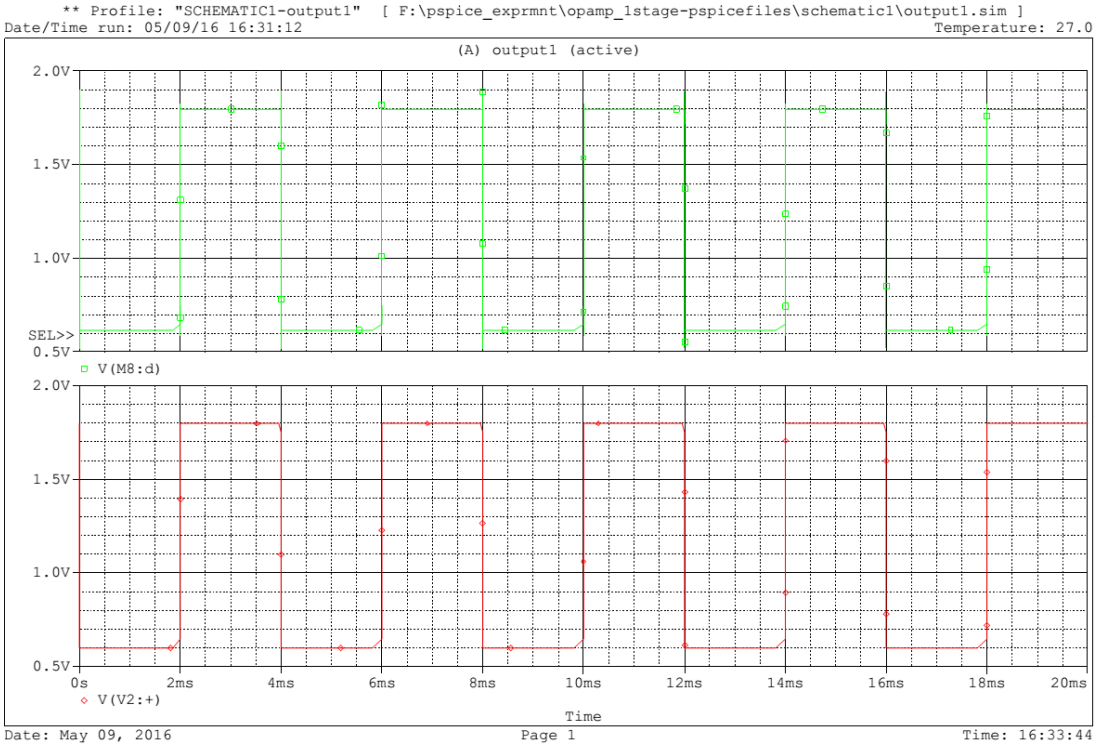


Fig 4.4 input-output characteristics of proposed CMOS op-amp at 250Hz

Figure 4.4 shows the output of the proposed adaptively biased op-amp when a 250Hz square wave is given as input. This allow us to observe the response of the circuit at lower frequencies. Input is applied with a small rise and fall times of 30ps and a negligible delay.

From this we observe that the output is following input justifying the functioning of voltage follower. In this case slew rate, delay cannot be obtained. A much higher frequency input is required to estimate exact slew rate and delay.

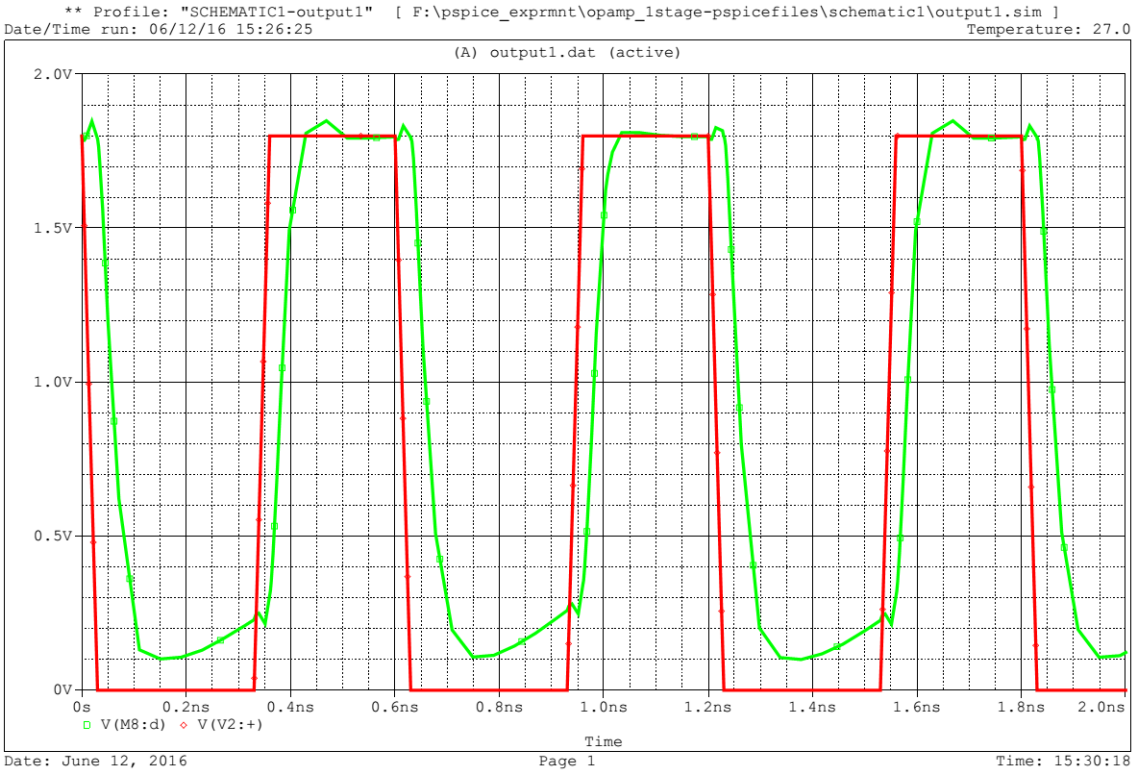


Fig 4.5 input-output characteristics of proposed CMOS op-amp at 1.66GHz

Figure 4.5 shows the high frequency behaviour of proposed adaptively biased op-amp. From this we can observe that the output closely follows input compared to other techniques that are discussed above.

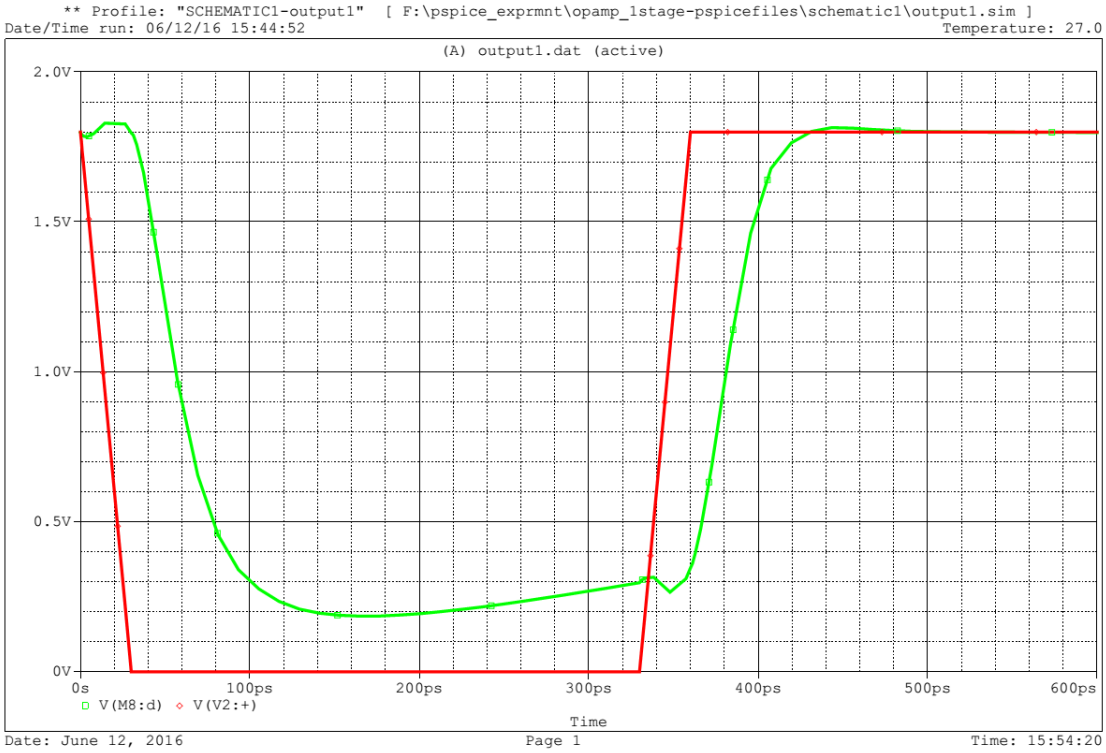


Fig 4.6 waveform for calculation of slew rate and delay

Figure 4.6 gives the slew rate and delay parameters of proposed design. It is the magnified version of fig 4.5 which is used for calculating the transient parameters like slew rate, delay, rise time and fall time.

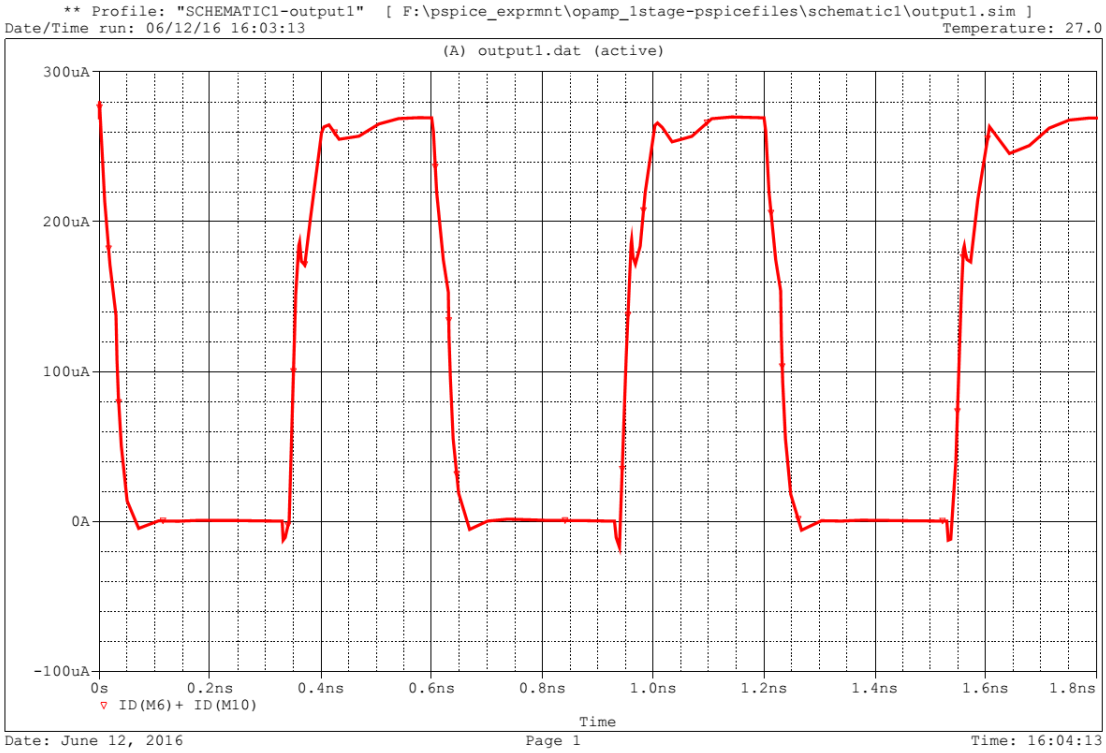
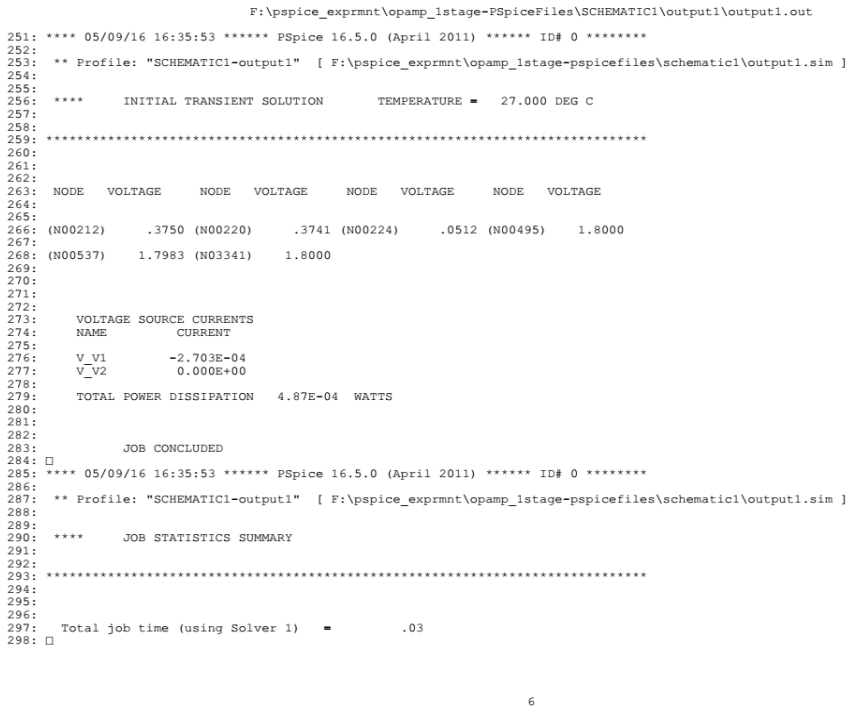


Fig 4.7 biasing current of proposed adaptively biased CMOS op-amp

From fig 4.7 we can clearly see that bias current in non zero when both input and output are high. This is due to additional transistor M9. This causes power dissipaton. In any application if there is requirement of high slew rate, then the power dissipation should be compromised. But still it is very much superior over conventonal op-amp and some other adaptive biasing techniques.



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**** 05/09/16 16:35:53 ****** PSpice 16.5.0 (April 2011) ****** ID# 0 ********

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 ****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C


 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(N00212)     .3750 (N00220)     .3741 (N00224)     .0512 (N00495)    1.8000

(N00537)    1.7983 (N03341)    1.8000


    VOLTAGE SOURCE CURRENTS
    NAME          CURRENT

    V_V1         -2.703E-04
    V_V2          0.000E+00

    TOTAL POWER DISSIPATION   4.87E-04  WATTS


          JOB CONCLUDED

**** 05/09/16 16:35:53 ****** PSpice 16.5.0 (April 2011) ****** ID# 0 ********

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 ****     JOB STATISTICS SUMMARY


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Fig 4.8 power dissipation of proposed adaptively biased CMOS op-amp

4.2.1 Observations

The parameters obtained from the simulations performed are tabulated below

Table 5 parameters obtained for proposed adaptively biased op-amp

	Slew rate V/ns	I_{BIAS}(max) uA	Delay (ps)	P.D (W)
Proposed Adaptively biased op-amp buffer	28.275	280	47	$4.8x10^{-4}$

CHAPTER 5

CONCLUSION

Analog CMOS amplifiers are extensively used in electronic devices and the design of CMOS amplifiers has a well-defined procedure involving the use of small signal models under a fixed biasing point. The expansion of electronic systems offers new applications for analog amplifiers, and the signals to be amplified that may not necessarily to have a fixed DC bias, which requires an automatic shifting of biasing point in the amplifier. The established design procedure may not be helpful to achieve better characteristics.

The objective of the work presented in the thesis is to develop a design method for adaptive analog blocks such as op-amp and OTA. An adaptive amplifier can adjust itself automatically to suit the DC level of the input voltage and the bias current is variable according to the DC level. To design such an amplifier, one needs to define the characteristics of the circuit according to the given input and the required output. One should expect a great diversity of the characteristics of amplification, as each application has different requirements. Hence, a generalised design method is well appreciated. The proposed design method is developed based on the analysis of the circuit characteristics of modified NMOS topology.

To conclude the thesis, we first discuss the advantages and disadvantages of three different adaptive biasing techniques that are presented in chapter 3 and 4. After that a comparison table is presented by tabulating the values of power dissipation, slew rate, delay and maximum biasing current of all the three adaptive biasing techniques. By observing it the significance of each technique is clearly distinguished. Each technique has its own advantage and depending on the designers application the best technique can be adopted.

5.1 Pros and Cons of Adaptive Biasing Techniques

In 3.2, conventional op-amp is simulated and it is observed that a slew rate of 9V/ns is achieved. Power dissipation is also considerably high. This is a drawback in both high frequency applications and low power applications.

5.1.1 Adaptively Biased CMOS Op-Amp

An adaptive biasing technique is discussed in 3.4 to improve the transient behaviour of conventional op-amp. An additional transistor is used to adaptively vary the biasing current. A slew rate of 13V/ns is achieved. i.e, a growth of 50% is achieved compared to conventional operational amplifier. A remarkable decrease in power dissipation is also seen.

This method is used in applications where improvement of slew rate is not important and reducing power consumption is the primary criteria. So this technique is well suitable in low power applications.

5.1.2 Modified NMOS Topology

In 3.8, an adaptively biased op-amp using modified NMOS topology is presented. This technique uses a separate network having 6 transistors and two DC current sources to adaptively vary the biasing current. It achieves a remarkable slew rate of 31.4V/ns. i.e, a growth of 260% achieved when compared to conventional op-amp and a growth of 140% when compared to adaptive biasing technique in 3.5. This slows that this technique is well-suited for high frequency applications. But at the same time a huge increase in power dissipation when compared to technique in 3.5 is observed. But still it is less when compared to conventional op-amp. One more advantage is this technique is more generalised when compared to others techniques discussed in this thesis. It can be applied to a wide range of analog blocks.

This method mainly concentrated on slew rate. So, this technique is preferred in high frequency applications where good transient performance is demanded. The drawback in this method is not the power dissipation because it is less than the conventional op-amp. But the actual drawback is area. As this technique requires additional six transistors and two current sources, more chip area is required during fabrication. Here there is a trade-off between slew rate and area. This modified NMOS topology is used in applications where chip area is not a concern and demands high slew rate.

5.1.3 Proposed Adaptive Biasing Technique

The proposed adaptive biasing technique is presented in chapter 4. This is a novel method that is developed by observing the NMOS topology. This technique achieves a remarkable slew rate of 28.275V/ns. i.e, a growth of nearly 200% when compared to conventional op-amp and a growth of nearly 100% when compared to technique in 3.5. But it is 1% less than the slew rate achieved by using modified NMOS topology. This is not a major issue because the gap between them is negligible. The power dissipation of both these methods also approximately same. This shows that the transient behaviour of both these techniques is almost same.

The upper hand of the proposed technique comes in case of chip area. This method conceives less area because additionally only one transistor is used to adaptively vary the bias current. Note that this technique also gives high slew rate. So, this can be used as alternate technique to the NMOS topology where area is a concern.

But the disadvantage of this technique is, it is not as generalised as NMOS topology method. It doesn't have application for wide range of analog blocks. The blocks which generate differential current at one of their nodes are only allowed to use this method which are quite less in number.

5.2 Comparison Table

	Slew rate (V/ns)	I_{BIAS} (max) uA	Delay (ps)	Power dissipation
Conventional op-amp	**8.65**	**240**	**123**	**$5.5x10^{-4}$**
Adaptively biased op-amp	**13**	**390**	**66**	**$3.58x10^{-11}$**
Modified NMOS adaptive biasing topology	**31.4**	**2800**	**60.5**	**$1.17x10^{-4}$**
Proposed Adaptively biased op-amp buffer	**28.275**	**280**	**47**	**$4.8x10^{-4}$**

Table 6 comparison table

5.3 Future Scope

The proposed adaptive biasing technique can be used in operational trans-conductance amplifiers, CDTA and in some of the current mode analog blocks. The adaptive biasing can be used to suppress the leakage current in testing of sub-micron/deep sub-micron CMOS integrated circuits. Leakage current is one of the important issues in current CMOS design. The adaptive NMOS topology can be used in circuits having differential input stage. These low power techniques can be easily applied to designs of ultra-low power analog, digital and mixed-signal circuits in deep submicron CMOS process.

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