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"AN INVESTIGATING ON CDBA BASED CONTINOUS TIME CIRCUITS"

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VLSI DESIGN & EMBEDDED SYSTEMS

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CERTIFICATE

This is to certify that the major project entitled **"AN INVESTIGATION ON CDBA BASED CONTINUOUS TIME CIRCUITS"** is submitted by **Mr. Vikash Jarwal (2K13/VLSI/23) ,** in partial fulfilment of the requirements for the award of degree of **Masters in Technology** in **VLSI Design and Embedded Systems,** Delhi Technological university, Delhi**.**

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I, hereby, further declare that in case of any legal dispute in relation to my M.Tech. Major Project, will be solely responsible for the same.

Date:

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ABSTRACT

Over the year of time, the evolution of modern application of signal processing has followed the trends of so called current mode, when signals, representing the information being processed, are in the form of current. In contrast to the conventional mode which utilized electric voltage, the current mode circuit can exhibit higher bandwidth, better signal linearity, higher slew rate and lower power consumption. Since they are designed for lower voltage swings, smaller supply voltage can be used. The current differencing buffered (CDBA) amplifier can operate in both current mode and voltage mode, which provides flexibility.

This project discusses implementation of lossless grounded negative inductor circuits (and application thereof), and oscillator circuit, using single CDBA. CDBA is designed using AD844 IC.

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ABBREVIATIONS

Abbreviations	Full - Form	Abbreviations	Full – Form
CMOS	Complementary Metal Oxide Semiconductor	LPF	Low Pass Filter
NI	Non-inverting	CFA	Current Feedback Amplifier
CML	Current Mode Logic	FTFN	Four Terminal Floating Nullor
QO	Quadrature Oscillator	CDTA	Current Difference Trans conductance Amplifier
SO	Sinusoidal Oscillator	CDBA	Current differencing buffered amplifier
MSO	Multiphase Sinusoidal Oscillator	CCII	Current Conveyor II
SSB	Single Side Band	VM	Voltage mode

CHAPTER 1: INTRODUCTION

1.1 Overview

Demand of low power microelectronic circuits requiring low supply voltage constitute long-term trends while developing advanced microelectronic design technologies. Speed and accuracy of data processing are very important factors to be considered. While satisfying one necessity another may have to be traded off which leads to non-fulfilment of all parameters at the same time. To overcome this problem a trade-off solution is utilized as a part of practice.

Over a span of time, the development of advanced applications of signal processing has accompanied the tendency of current mode [1], when signals, containing the useful information being refined, are in the form of electric currents. Counterpoint to the formal voltage mode, which utilizes electric voltages, the current mode microelectronic circuits can expose under particular conditions better linear signal and higher bandwidth. One more benefit is that they require low supply voltage as they are intended for lower voltage swings [1]. While developing advanced current mode applications, mixed mode microelectronic circuits are also examined to optimize the interface between sub-blocks which are playing different roles.

As the microelectronic circuit technology is getting advanced from the last two decades, circuit designers have become able to increase the efficiency of current-mode analog methodologies for producing refined and accurate solutions to several microelectronic circuit design problems. As a result, the current-mode signal processing methodology is always expected to offer one or more of the following benefits: consumption of less average power, higher operating frequency range, better linearity, higher slew rates and improved accuracy [2].

To overcome this problem of selecting either current mode or voltage mode technology, scientists Acar and Ozoguz have developed a current differencing buffered amplifier [3] which can work efficiently in both current-mode and voltage-mode technology for the flexible operation. This amplifier can operate at high frequency range and does not display many parasitic capacitances.

1.2 Motivation

Digital signal processing is a rapidly developing field and it is getting advanced further, as growth in microelectronic circuits technology demands dense and effective application of its algorithmic programs on silicon chips. Even though many digital techniques and circuits are available to process various forms of signal, but still many complex and high performance advanced devices require analog circuits. We know that analog signals occur naturally. That's why, analog circuits act as an interface between the actual world and the digital domain. Analog VLSI can deal with nearly all real world issues and has extended its range for new information processing applications in numerous fields like hand writing acknowledgement, integrated sensors, speech acknowledgement, image processing and so on.

As a result interest has been increased in the evolution process of active elements which are used for analog signal processing. The adaptation involved in their development included modification in basic circuits like current conveyors, Voltage Feedback Amplifier, Operational Trans-conductance Amplifier, Current Feedback Amplifier etc. Another direction of evolution is by inserting an entirely new element in the circuit which expands the original CC, VFA, OTA, CFA etc. The key motivation for performing such modifications is an attempt to raise the application prospective of active blocks. Concurrently, the internal structure of the element must be simple while consuming less power and operating at higher speed [4].

Advancement in IC technology in past two decades motivated VLSI designers to increase the efficiency of current mode methodologies. The CM provides various advantages over VM. CM approach includes high slew rates, better linearity, enhanced accuracy, broader bandwidth and reduced power consumption [4]. The traditional analog circuits are VM circuits wherein the voltage levels at various points along with the input and the output points determines the circuit parameters and performance, a simple example of such circuit is an operational amplifier. All these circuits cannot change its output voltage instantly in accordance with the abrupt transition occurred due to stray and parasitic capacitances in the input voltage. Due to the finite unity gain bandwidth product, bandwidth of circuits based on op amp becomes low. They require higher supply voltages to achieve better SNR and time constants of the circuits effect the slew rate. In this way, VM circuits are not fitting for their utilization at high frequency applications. In CM circuits, current form is used to display the input/output signals and the whole circuit

analysis is done in currents. Here, the voltage levels are not utilized for obtaining the circuit performance. CM circuits have low impedance internal nodes and voltage swings are small. The bandwidths of these circuits are higher and become low time constant circuits due to their low impedance. Higher slew rate can be obtained with the help of the higher rate of change in output signal. An easy architecture is used to design Current mode circuits and power supply voltage does not make any effect in the operation of these circuits.

The advantages of current mode has increased the evolution of many current-mode active building blocks for example, Differential Voltage Current Conveyor, Operational Trans-conductance Amplifiers, Differential Difference Current Conveyor, Current-Feedback Op-Amps, Current Controlled Current Conveyors, Dual X Current Conveyors, Voltage Differencing Trans-conductance Amplifier, Current Differencing Trans-conductance Amplifier. An advanced active building block named Current Differencing Buffered Amplifier incorporating the benefits of current mode was introduced in 1999 [3]. This block has gained popularity in past decade due to wide dynamic range and broad bandwidth. Also, it is suitable for high frequency operation as its internally grounded input terminals makes the circuit free from parasitic capacitances.

The growing interest in CDBA is mainly because of the flexibility and ease of implementation offered by this block. The block can be easily implemented by CMOS technology. Hardware implementation using IC AD844N can also be accomplished. Also, it offers broad range of linear and non-linear applications. These features of CDBA have captured the interest of analog designers towards it, thus motivating the designers to further explore this block to obtain satisfactory results through simulations and develop new applications using this active block.

1.2.1 Development of Active Blocks

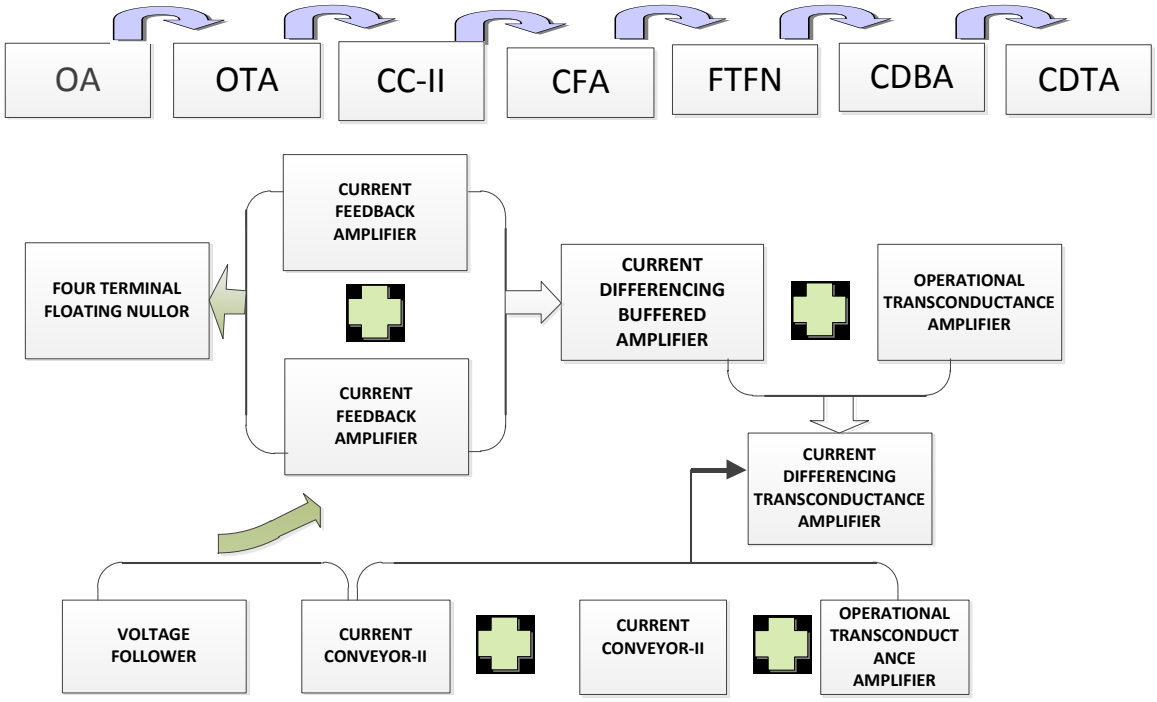

Fig.1.1 Development of Active Blocks [4]

Advancement in fundamental blocks like VFA, OTA, CC, CFA (full names are in fig.1.1) is being carried out for the development of active blocks. The internal structure of these element should be simple in order to have high-speed operation and low power consumption. Except the advancement in current ones, introducing of new elements is being carried out for the development of active elements, which expands the original VFA--OTA-CC-CFA active set.

A specialized pattern is followed in the process of development which has been going on.

1.2.1.1 Development of Current Feedback Amplifier from Current Conveyor II:

Current Feedback Amplifier (CFA) [4] was introduced over traditional voltage - feedback amplifier to enhance the limited finite gain-bandwidth product. Its functions are: to produce constant bandwidth unaffected by closed loop gain and to provide high slew rate capability. CFA acts as an operational Trans impedance amplifier and its internal structure contains a CCII+ followed by a voltage follower. CFA can be demonstrated as shown in fig 1.2

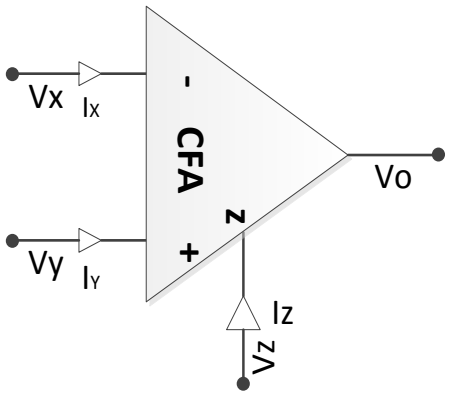

Fig.1.2 symbol Current feedback amplifier [4]

1.2.1.2 Four Terminal Floating Nullor (FTFN)

FTFN was evolved after the development of Current Feedback amplifier. Due to its features of more flexibility and more versatility than operational amplifier or current conveyor, it was developed for the advancement in continuous-time circuits. It is designed by cascading CFAs.

1.2.1.3 Generation of Current Differencing Buffered Amplifier:

Current Differencing Buffered Amplifier (CDBA), advantages of current-mode circuit includes [3] absence of stray and parasitic capacitances, high slew rate, broad bandwidth, and easy implementation. It is used in current and voltage mode signal processing applications. CDBA comprises of a unity-gain voltage amplifier and a unity-gain current differential amplifier. Structure of CDBA is shown in Fig-1.3

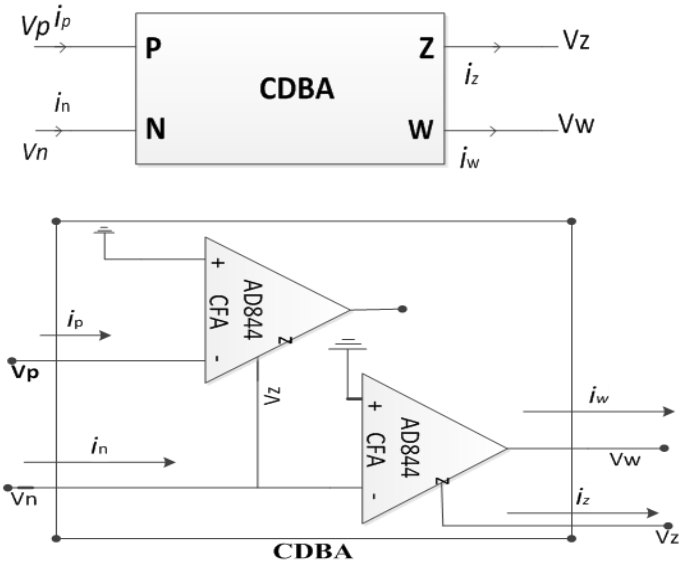

Fig.1.3 (a) CDBA symbol (b) CDBA structure using AD844 [3]

1.2.1.4 Design of Current Difference Trans conductance Amplifier (CDTA)[4]

Current Difference Trans conductance Amplifier being compatible to the CDBA consists of different current inputs *n* and *p* [4]. Outside load obtains the difference of these currents from terminal *z*. We get voltage signal at the *z* terminal of CCII+ then this voltage is passed through the trans-conductance *g* block which is known as trans-conductance operational amplifier (OTA). Then we obtain the current pair at *x* terminals. The fact is, the trans-conductance can be controlled electronically through an auxiliary port. Output current pair at *x* terminals can flow in three combinations of directions:

1. Both currents flowing out of CDTA block.
2. The currents have opposite directions.
3. Both currents flowing inside the CDTA block.

In fig. 1.4 we can see that outside flow of current is shown by '+' and inside flow is shown by '–'sign. Therefore we can design three types of CDTA components viz. CDTA+-, CDTA-- and CDTA++.

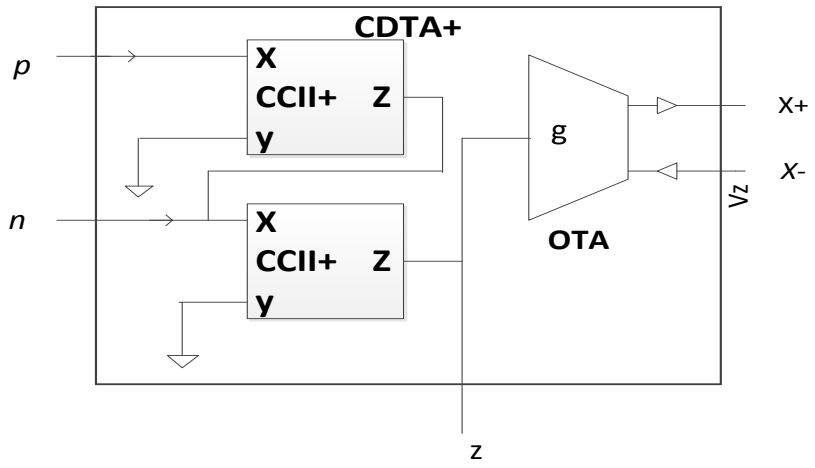

Fig. 1.4 Structure of CDTA [4]

1.3 Research objective

The objectives of the research are listed below,

- To study and analyse the different methods of realizing CDBA active block.
- Comparative analysis of CDBA realizations in terms of various performance parameters.
- To study and analyse various applications based on CDBA
- To propose new circuit configurations which offer better performance.

- Verification of proposed circuits by functional simulations and/or by experimentation.

Initially the literature related to CDBA [3] and applications proposed using CDBA is reviewed which suggested the areas which could be explored to propose new designs. Signal generators such as oscillators and multi-vibrators are an important class of circuits and find wide application in electronic system design. It was observed that though, a large number of sinusoidal oscillators are available in literature, yet there is scope of further investigations. As a result two new negative inductor structures using single CDBA and two oscillator configurations are proposed. The first one is a second order sinusoidal oscillator (SO) configuration, designed using proposed negative inductor. Second proposition is a second order oscillator using single CDBA for minimizing chip area with better THD performance as compared to its second order counterpart. All the proposed designs are simulated using PSPICE to test their functionality.

1.4 Thesis organization

The thesis is organized in 7 chapters as follows:

Chapter2:

Chapter 2 reviews the history and developments through the years in the block realization of CDBA and applications made out using the CDBA active block.

Chapter 3:

It describes the theory and various realizations of CDBA. Further for verification of CDBA active block simulation results, such as DC and AC analyses, are presented.

Chapter 4:

It describes theory of filters with all standard second order filters implementations using CDBA and their simulation results are verified.

Chapter 5:

It describes theory of oscillators and implementation of different configuration of QO and MSO using CDBA. The PSPICE simulations for functional verification of these implemented configurations are also presented.

Chapter 6:

Chapter 6 presents the CDBA based new propositions and their simulation results showing conformity with the proposed theory. This includes negative inductor using

single CDBA and its application, second order sinusoidal oscillator. Additionally, yet another second order sinusoidal oscillator using single CDBA is also proposed.

Chapter 7:

Chapter 7 summarizes the work presented in this dissertation followed by a concluding remark highlighting the objective achieved through this work.

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CHAPTER 2: LITERATURE REVIEW

In past years, there has been trending shift to current mode design due to its various advantages over voltage mode. This lead to the development of various current mode active devices like second generation Current Conveyors (CCII), Operational Trans-conductance Amplifier (OTA), Current-Feedback Operational-Amplifiers (CFOA), Differential Voltage Current Conveyors (DVCC), third-generation Current Conveyors (CCIII), Differential Difference Current Conveyors (DDCC) etc. In 1999, a new building block called CDBA was proposed [1]. The block inherits all the properties of current mode circuits and therefore is suitable for high frequency applications. Designing of analog signal processing devices using CDBA has been an attractive task for many scholars and researchers and therefore a wide range of applications employing CDBA have been proposed in [2, 4, 8-28]. Numerous papers have been reported on CDBA in past one and a half decade. This includes various realizations of CDBA and broad range of signal processing and generation applications such as filters, oscillators, immitance simulator, multi-vibrator, multiplier, etc.

2.1. Reported work on CDBA realization

C. Acar and S. Ozoguz in 1999 proposed a CDBA realization using CFOA (IC AD844) [1]. Two AD844IC's were used to design CDBA block and then filters were realized using it. In the same year, S. Ozoguz and C. Acar along with A. Toker, M. A. İbrahim also proposed CMOS realization of CDBA [2].

After two years, Kuntman and Tarim [3] presented a low power high performance CDBA using a voltage buffer and cascading of 2 second generation current conveyors (CCII). This configuration was implemented in CMOS technology incorporating only MOS transistors in it.

CDBA based on NPN transistor was proposed in 2006 by Sawangarom, Tangsrirat and Surakampontom [4] proposed. This CDBA could work at the power supply range of 2 to 5 volts. CDBA based on NPN transistors has been designed using two blocks called voltage follower and current differencing circuit. Cascading of 2 unity gain current amplifier is used to design the current differencing circuit and to reflect the current to output port, current mirror is used in the circuit. This circuit had the added advantage of using only NPN transistors which help to gain a maximum high frequency response which was earlier limited because of the use of PNP transistors.

In the same year, K. Klahan, W.Tangsrirat, W. Surakampontorn and K. Kaewdang [5] presented a low supply voltage wide band NMOS based CDBA, which shows low resistance at the output-voltage node (w) and at the current-input nodes (p, n). The presented NMOS based CDBA could work more efficiently at the certain range of supply voltage and frequency. It can operate at minimum power supply voltage of ±1.25 volts. This NMOS based CDBA was designed by altering low impedance second generation current conveyor circuit (CCII+) so that it can work as a voltage buffer circuit and a current differencing circuit also.

The existing CDBAs work on comparatively high supply voltage due to that they produce high input resistance, consume more average power and shows the problem of limited output voltage swing. To overcome this problem, scientists Oguzhan Cicekoglu and Cem Cakir [6] in 2008 introduced a high performance low voltage CDBA. Proposed circuit could work effectively consuming less average power at a maximum voltage of ±0.75V. A new approach based on flipped voltage follower current sources (FVFCS) used in the CDBA makes it more advantageous as it offers very low resistance at the input and output terminals. Moderate output voltage swing has been obtained from the output stage of this CDBA.

At that point after a year, Oguzhan Cicekoglu, Cem Cakir and Shahram Minaei [7] in 2009 invented an efficient low power low voltage CDBA based on CMOS. The circuit can function efficiently at the power supply voltage of ±0.6 volts. This Low power CMOS CDBA circuit is made up of voltage buffer and current differencing circuit. It provides very low input resistance at n and p nodes and consumes less average power as compared to the other CDBA circuit designs existing in literature.

2.2. Reported work on CDBA Applications

2.2.1 Linear Applications

2.2.1.1 Filters

A design methodology to implement continuous-time current-mode filters employing CDBAs using minimum active components was presented by Worapong Tangsrira, Nobuo Fujii and Wanlop Surakampontorna [8] in 2002. They also implemented fifth-order Butterworth low-pass filter & a sixth-order Chebyshev band pass filter to describe the functionality of the techniques.

Visawa Sawangarom, Worapong Tangsrirat and Wanlop Surakampontom in 2006 proposed NPN based CDBA and realized all pass filter using it [4]. Likewise, in 2008

they realized Voltage mode universal biquad filter based on six passive components and two CDBA [9]. The configuration could realize all five types of filter with the same topology.

A. U. Keskin in 2008 presented voltage mode band pass filter based on single CDBA [10]. The filters were of High quality factor and used minimum number of components.

M. Sagbas, M. Koksal and S.E. Oner in 2009 presented another design of second order multi-function multi-mode filter [11]. This design utilizes one CDBA block and four to five passive components. Proposed topology was useful in implementing current, voltage, transadmittance and transconductance modes. It was also used in designing of band pass, low pass and high pass filters.

Fırat Kacard and Yasin ozcelep in 2011 proposed five new configurations of first order all pass filter based on voltage mode using CDBA [12]. They used four to five passive elements while realizing the filter.

A current-mode linear transformation filter based on CDBA for realizing higher order filters was presented by Wen-Ta Lee, Yuh-Shyan Hwang, Jiann-Jong Chen and Zhao-Hong Huang [13] and also third order chebychev low pass filter was proposed by them to prove the functionality.

Shahram Minaei, Cem Cakir and Oguzhan Cicekoglu in 2010 presented a new CMOS realization of CDBA that operate at low voltage [14]. The circuit also consumed low power and offered high performance. Then they analyzed all pass and notch filter using the proposed topology to verify the performance of the new circuit. Also, ZC-CDBA performance was demonstrated on a new current mode filter topology proposed by Ersin Alaybey, Arda Güney and Hakan Kuntman in 2013 [15].

2.2.1.2 Oscillators

CDBA based resistance controlled sinusoidal oscillators were first proposed in 2000 by S. O zcana, A. Tokera, C. Acara, H. Kuntmana and O. Cicekoglu [16]. They gave six configurations to design sinusoidal oscillator (SO). These oscillators are suitable for VCO implementations.

Another oscillator called multiphase sinusoidal oscillator employing CDBA as an active element was proposed by Sumaytee Pisitchalermpong, Worapong Tangsrirat and Wanlop Surakampontom in 2006 [17]. The circuit includes inverters and n cascaded

blocks of lossy integrators based on CDBA. N sinusoidal waves of phase difference $\frac{180^{\circ}}{n}$ are obtained at the output of such oscillator.

A Quadrature oscillator (QO) consists of 2 capacitors and 3 CCCDBAs which is appropriate for IC architecture is proposed by Montree Siripruchyanum, Winai Jaikla and Phamorn Silapa in 2007 [18]. Here input bias current is used to electronically control the condition and frequency of oscillation.

CDBA based QO designed by 2 capacitors, 4 resistors and 2 CDBA blocks [9] is proposed in 2008 by Worapong Tangsrirat, Tattaya Pukkalanun, and Wanlop Surakampontorn. The virtually grounded resistors used in the circuit provide controllability on condition and frequency of oscillation independently.

In 2010, J.K. Pathak, R. Senani and A.K. Singh proposed a systematic approach to realise CDBA based QO [19]. They presented a general configuration designed using an integrator and low pass filter that yielded 12 different Quadrature oscillator circuits.

Abhirup Lehiri in 2011 also proposed a low frequency quadrature sinusoidal oscillator using CDBA [20]. His proposed circuits use reduced number of components and low frequency is obtained due to difference term in the oscillator's frequency.

Winyu Sonjoi, Worapong Tangsrirat and Wanlop Surakampontorn proposed another electronically tunable Quadrature oscillator made up of two CCCDBA and two grounded capacitors in 2009 [21]. This configuration provides two sinusoidal output having phase difference of 90°. Later in 2013, the performance of this oscillator was improved by using high performance CCCDBA by [22].

Ali Umit Keskin [23] proposed a design of CDBA based minimum Component Oscillators (MCO) in which Negative Impedance (NIC) approach was used. The steps in synthesis of NIC based oscillator are as follows: a) Initially a grounded NIC circuit structure of a particular type of active element is formed, b) then NIC is connected with a shunt branch so that, any real term can be eliminated from the complex plane & a symmetric pair of pole can be placed on the imaginary axis.

2.2.1.3 Immitance Simulator

Ali Ümit Keskin and Erhan Hancioglu in 2005, proposed synthetic floating inductance circuits based on CDBA [24]. They presented two different configurations which uses grounded capacitor. The circuits were fully integrable and also electronically tunable.

Worapong Tangsrirat and Wanlop Surakampontorn in 2006 [25] proposed an electronically tunable lossless floating inductance simulator. The floating inductance circuit uses only three current controlled CDBAs (CC-CDBA) and a grounded capacitor. Equivalent inductance of this simulator can be adjusted by varying the external bias current of the current controlled CDBA. This floating inductance simulator is very useful in microelectronic circuit design as there is no requirement of external resistors.

2.2.1.4 Inverse filter

CDBA based universal inverse filter configuration [26] was proposed by Rajeshwari Pandey, Neeta Pandey, Tushar Negi and Vivek Garg in 2013. The topology was use to design all five inverse filters namely inverse high pass, inverse low pass, inverse all pass, inverse band pass and inverse band reject filter.

2.2.1.5 Nth order current transfer function realization

Cevdet Acar and Herman Sedef in 2003 proposed CDBA based two new configurations to realize high order current mode transfer function [31, 27]. One configuration was made of one CDBA block and four passive components and the other was designed with two CDBA blocks and four passive components. These topologies had reduced number of active elements in their realization.

2.2.2. Non-linear Applications

2.2.2.1 Multivibrators

Sajal K. Paul, Rajeshwari Pandey, Kashish Anand, Kranti Ghosh Gautam and Neeta Pandey [28] proposed three voltage mode astable multivibrator microelectronic circuit based on single CDBA. In this multivibrator design, first circuit outputs the square wave of fixed duty cycle and other two offer duty cycle controllability. One of the controllable square wave generators employ resistance to control the duty cycle, whereas the other makes use of voltage source to electronically control it.

2.2.2.2 Multiplier

A new fully integrable fourth quadrant analog multiplier based on CDBA [29] was proposed by Ali Umit Keskin in 2003. The circuit gave good performance and featured reduce number of component and ease of implementation.

In 2007, Montree Siripruchyanun [30] designed an analog multiplier and divider using CCCDBA block. The circuits need only two CCCDBA for its construction and no passive element. The circuit also behaves as gain-controllable current amplifier. In same

year, multiplier/divider circuit was designed using high performance Bi-CMOS CCCDBA [31]. The circuit can be used for analog signal processing based applications.

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CHAPTER 3: CDBA ACTIVE BUILDING BLOCK

3.1. CDBA Terminal Characteristics

CDBA block can be designed using two fundamental blocks which are voltage follower block and current subtractor block. The symbol for the CDBA active block circuit is represented in Figure 3.1. The equivalent structure of circuit to the CDBA consists of dependent current and voltage sources and is shown in figure 3.2.

Fig. 3.1 Symbol of CDBA [1]

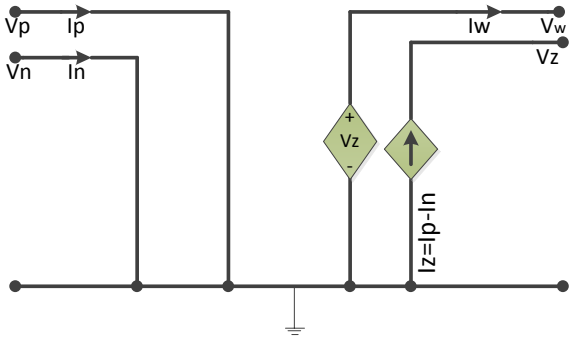

Fig. 3.2 Equivalent circuit of CDBA [2]

The characteristics of the ideal CDBA block can be modelled as [2]:

$$\begin{bmatrix} i_z \\ V_w \\ V_p \\ V_n \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 & -1 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_z \\ i_w \\ i_p \\ i_n \end{bmatrix} \tag{3.1}$$

And for practical CDBA equation become

$$I_Z = \alpha_p I_P - \alpha_n I_n, V_W = \beta_v V_Z, V_P = V_n = 0 \tag{3.2-3.4}$$

Where current gains are denoted by α_p and α_n, and voltage gain by β_v , which in the ideal case should be equal to unity.

In practice, they are expressed as

$$\alpha_p = 1 - \varepsilon_p, \alpha_n = 1 - \varepsilon_n, \beta_v = 1 - \varepsilon_v \tag{3.5-3.7}$$

With

$$|\varepsilon_p| \ll 1, |\varepsilon_n| \ll 1, |\varepsilon_v| \ll 1$$

Here current-tracking errors are denoted by ε_p and ε_n and voltage-tracking error is denoted by ε_v .

If we observe the equivalent circuit and the above describing equations, we find that the z- terminal of circuit is showing the divergence of current through p terminal from current through n terminal that's why we name z as the current output node, which has typically infinite resistance. In this block p-terminal is called non-inverting terminal and n-terminal is called inverting terminal. These p and n terminals which act as inputs to the block are grounded thereby ideally having zero input impedances at these terminals internally. The w-terminal is termed as voltage output, as the voltage occurring at the w-terminal is always same as that of the z-terminal due to the appearance of the voltage follower circuit between the two terminals. As w-terminal is used as a voltage output hence it should ideally have zero impedance.

3.2. Realizations of CDBA

3.2.1. IC AD844 based Realization

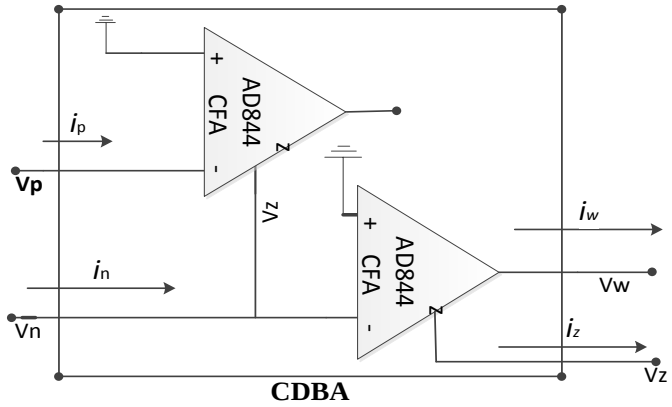

Fig. 3.3 Implementation of CDBA using CFOA (AD844 IC) [1]

Figure 3.3 presents the implementation of CDBA using two AD844 CFOA IC's (see Appendix A). The current at the compensation node v_z of the CFOA is ideally equal to the difference of the current applied to the non-inverting and inverting terminals of the CFOA. Hence the current at the compensation node for first IC is given by:

$$i_{z1} = -i_p \tag{3.8}$$

thereby giving a resultant current of i_{n2} at the inverting terminal of second IC.

$$i_{n2} = i_n + i_{z1} \text{ Or } i_{n2} = i_n - i_p \quad (3.9)$$

Therefore the current at the z-terminal (output node) of second IC is given by:

$$i_{z2} = i_p - i_n \quad (3.10)$$

Which is the required current at the z-terminal of CDBA, also the voltage at the w-terminal called output voltage of the CFOA is same as that of the voltage at the z-terminal using a voltage follower circuit attached between the two terminals as can be seen in the CMOS implementation of the CFOA. The voltage at the z-terminal is formed by i_{z2} current and the impedance at the z-terminal.

3.2.2. NPN Transistor based Realization[3]

Various CDBA blocks has been proposed in literatures which are implemented using different technologies however, every implementation has some of its own limitations. There are certain limitations due to the use of PNP transistors in the implementation as they limit the high frequency operation of the circuit and this leads to a conclusion that CDBA should be designed in such a way that signals only pass through NPN transistors. Also due to the advances in large scale integration and increased use of complicated circuit systems and portable consumer electronics equipments, there has being a gradual increase in the need of a low voltage low power technique.

3.2.2.1. Block Architecture

In this section, a simple NPN based CDBA proposed in [3] is described which can work efficiently at power supply voltage up to 2 volts DC, and since the signal has only NPN transistors in its signal path this helps in achieving a maximum high frequency response. As shown in figure 3.4, the NPN based CDBA consists of two sub-circuits namely the current differencing circuits and a buffer voltage amplifier. We find from the circuit that when we traverse the path between the negative and positive supply voltages, the path has only one biased current source and two transistors. As a result this circuit can work at a low power supply voltage compared to other implementations with a minimum power supply voltage of ($2\ V_{be}+V_{cesat}$) = 2 V (or +1 V to -1 V).

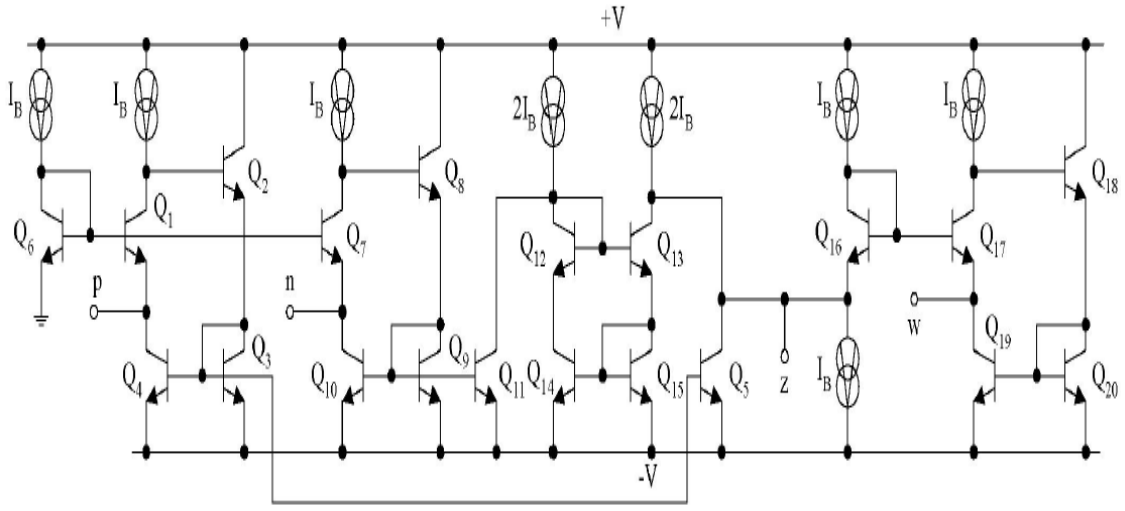

Fig. 3.4 NPN transistors based CDBA circuit [3]

3.2.2.2. Circuit Description

3.2.2.2.1. Current Differencing Circuit

This circuit can be designed by connecting 2 unity gain current amplifiers. Now if we consider figure 3.5 which depicts the circuit diagram of the unity gain current amplifier we can see that Q1 through Q4 transistors form a feedback loop. Let us assume that the emitter current passing through the Q1 transistor is i_e, then the emitter current passing through the Q2 transistors will be equal to $\beta_2 i_e$ which is also the emitter current for the Q3 transistor. Q3-Q4 transistors together form a current mirror and hence the current $\beta_2 i_e$ is reflected to the collector of Q4 transistor. Therefore following relation can be obtained:

$$i_{in} = i_e + \beta_2 i_e \tag{3.11}$$

Or

$$i_e = \frac{i_{in}}{\beta_2 + 1} \tag{3.12}$$

Where,

i_{in} - the input signal current

β_2 - the current gain of transistor Q2

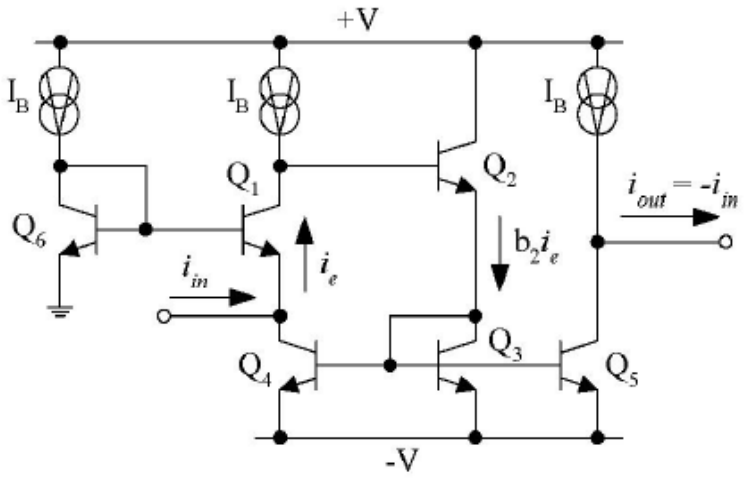

Figure 3.5 Unity gain current amplifier [3]

For the circuit output current i_{out} can be given by:

$$i_{out} = -\beta_2 i_e = -\frac{\beta_2}{\beta_2+1} i_{in} \quad (3.13)$$

Generally the current gain β_2 of the circuit is in several hundreds and is high enough to obtain the ratio $(\beta_2/\ \beta_2+1)$ nearly equal to 1; hence the output current of the circuit can be represented by:

$$i_{out} = -i_{in} \quad (3.14)$$

Because of the negative feedback applied Between the Q1 through Q4 transistors, the value of the input resistance r_{in} of the unity gain circuit is very low and is given by the following expression below:

$$r_{in} = \frac{r_{e1}}{\beta_2} \quad (3.15)$$

Where,

$r_{e1} = V_T / I_B$ - the small signal emitter resistance

V_T - the thermal voltage.

The two groups of transistors namely Q1-Q5 and Q7-Q11 form two current amplifiers which combine together to form the current differencing circuit as depicted in figure 3.6. Transistors Q1 through Q5 reflect current $-i_n$ to the output port and second current amplifier Q7 through Q11 along with current mirror circuit Q12-Q15 represents i_p at the output terminal, Therefore the relation obtained for the output terminal of the circuit is:

$$i_{out} = i_p - i_n \quad (3.16)$$

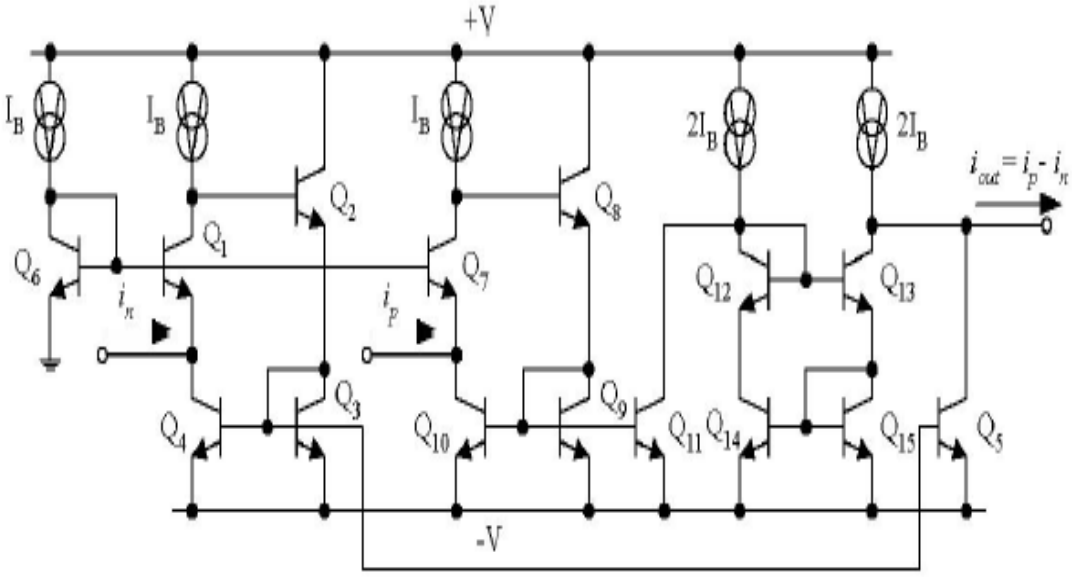

Fig. 3.6 Current differencing circuit [3]

3.2.2.2.2. Buffered Voltage Amplifier

The voltage at terminal W (V_w) is forced to be equal to the voltage at terminal Z(V_Z) with the help of transistors Q16 through Q20 which together form the buffer voltage amplifier as shown in figure 3.7, i.e. $V_w = V_Z$.

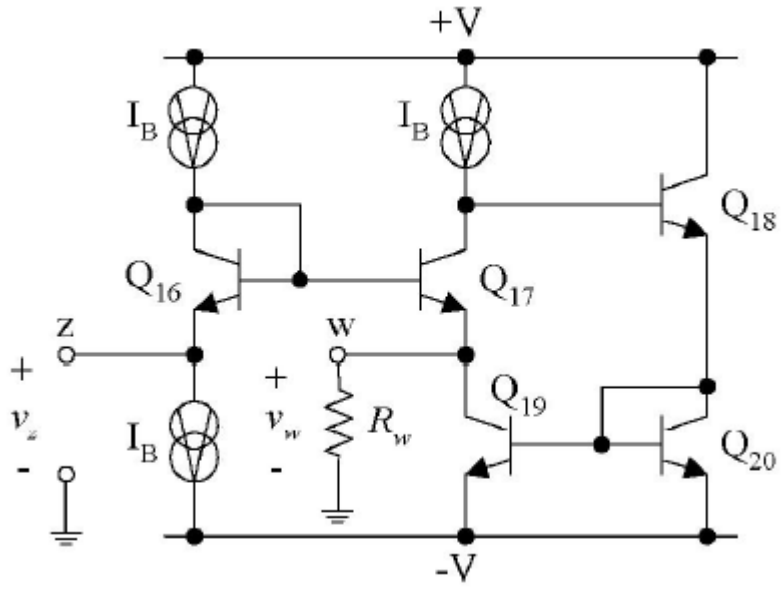

Figure 3.7 Buffer Voltage amplifier [3]

3.2.3. CMOS based Realization[4]

The DCCCS block which acts the current differencing circuit, followed by the voltage follower [5] block combine together to form the CMOS implementation of the CDBA active block as depicted in figure 3.8.

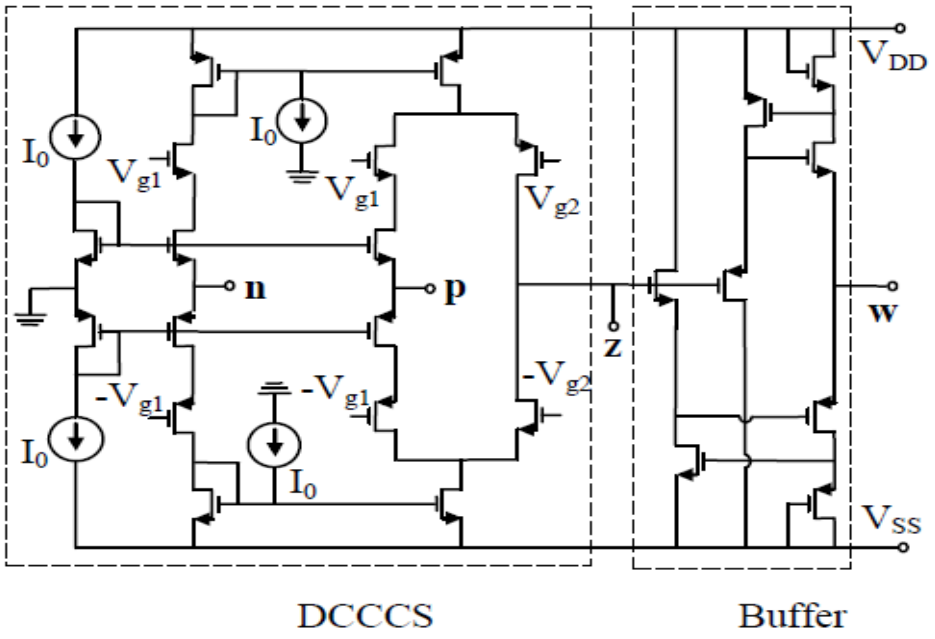

Fig. 3.8 CMOS implementation of CDBA **[4]**

The CCII configuration implemented by Bruun [6] is slightly modified to reach to the required DCCCS circuit which is used in current CDBA block.

3.2.4. Low Voltage Low Power CMOS based CDBA (LVLP CDBA) [2]

In the recent scenario, what we observe is a shift in the interest of researchers to low voltage circuit designs due to the advent of mobile communication systems and portable electronics and thus efforts are made to decrease the supply voltage of the circuit designs and hence minimize the power consumption. These low power capabilities were missing in the previously discussed implementations of CDBA.

Also in CMOS based CDBA, the terminal resistances are of the order of hundreds (high) of ohms and their transfer ratios for current and voltage are smaller than one. Hence, the main aim of discussing this implementation of CDBA based on the FVF technique is to overcome the disadvantages mentioned above.

3.2.4.1. Block Architecture

The low power low voltage CDBA circuit implementation can be separated into two blocks: first is the voltage buffer block and second is the current differencing block. Where first block works as a buffer between z and w terminals and second block replicates the divergence between the current passing through the P and N terminal obtained at z terminal and second block acts as a buffer between the Z and W terminals.

The complete schematic of the block can be seen in figure 3.9, where M1-M8 transistors make up the current differencing block and M9-M14 make up the voltage buffer block.

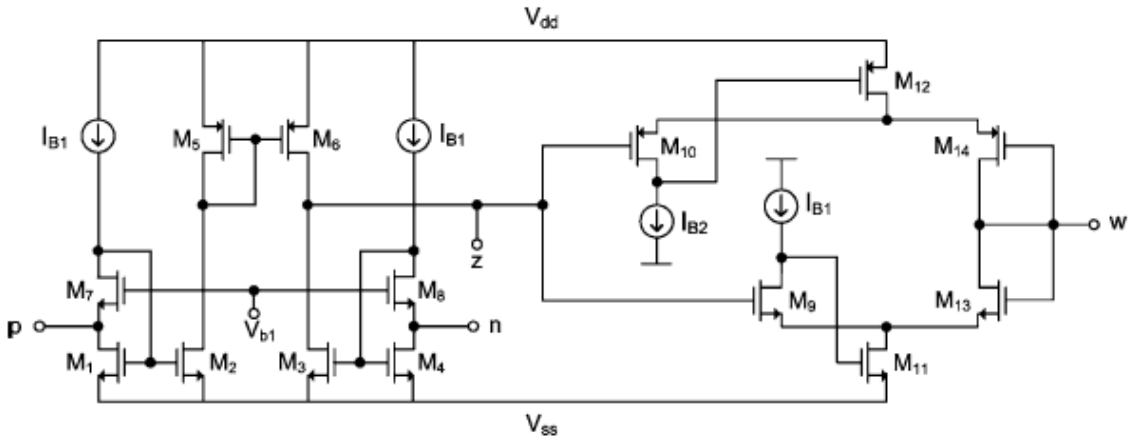

Fig. 3.9 Low Power CMOS implementation [2]

3.2.4.2. Circuit Description

The resistances occurring at the input terminals (p & n) of the implemented CDBA block can be made very low by using FVFCS, hence the current subtraction circuit is so implemented thereby removing one of the disadvantage of other implementations.

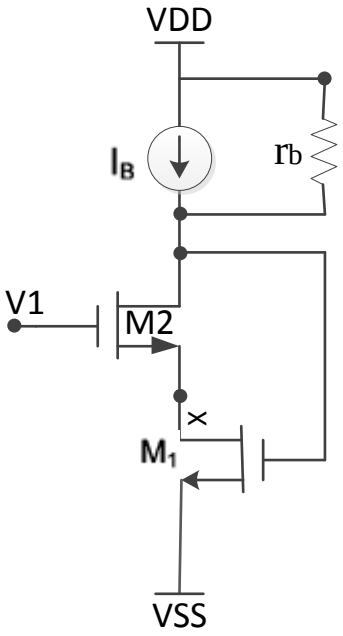

Fig. 3.10 Flipped voltage follower current source (FVFCS) [2]

The resistance occurring at input terminal of the FVFCS is shown in fig. 3.10, when seen at the node X can be found to be;

$$R \cong \frac{\frac{1}{g_{m2}}\left(1+\frac{r_b}{r_{02}}\right)//r_{01}}{g_{m1}(r_b//g_{m2}r_{01}r_{02})} \quad (3.17)$$

Where,

r_b - Output resistance of the current source

r_o- Output resistance of the transistors

g_m - trans conductance of the transistors

For a basic current source having $r_b = r_{o2}$, the node resistance can be found to be;

$$R \cong \frac{2}{g_{m1}g_{m2}r_{02}} \quad (3.18)$$

The current subtraction circuit comprises of M1 to M8 transistors is shown in fig. 3.11. The circuit can basically be understood as comprising of three current mirrors respectively constructed out of M1-M2, M3-M4 and M5-M6 transistors. Due to current mirror between M1-M2 the current flowing through M2 is $I_{B1} + i_p$ and $I_{B1} + i_n$ flows through M3 due to current mirror between M3-M4. Also the current mirror between M5-M6 leads to a current $I_{B1} + i_p$ flowing through M6, thereby replicating the difference of the currents at the P and N terminals of the CDBA to the Z terminal.

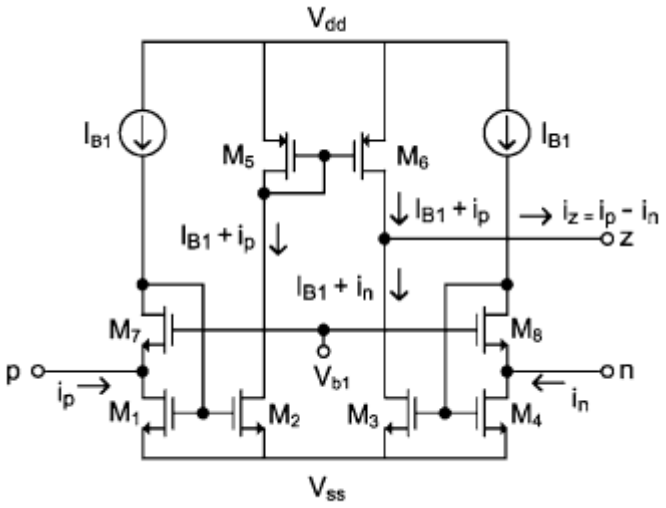

Fig. 3.11 Current subtractor circuit [2]

Hence, terminal-z is labelled as current output node. The current at the output node can be represented as follows:

$$i_z = I_{B1} + i_p - (I_{B1} + i_n) = i_p - i_n \quad (3.19)$$

For the current implementation of CDBA, the output stage is based on DFVF. The circuit for DFVF is shown in figure 3.12, where for large currents through transistor M3 the voltage at node Y remains approximately constant and also the impedance of this node is very low.

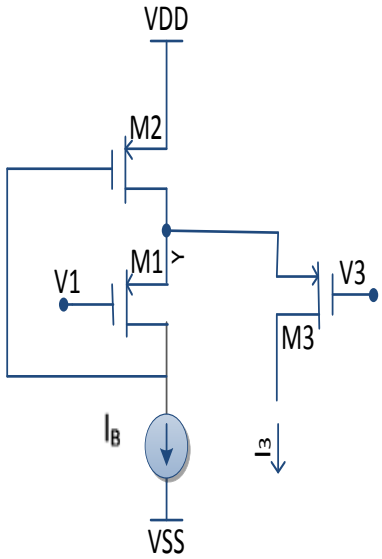

Fig. 3.12 Differential flipped voltage follower (DFVF) [2]

This condition of constant voltage and very low impedance can be achieved if the transistors M1 and M3 are assumed to be of same sizes and the quiescent condition of V1=V3 is observed. DFVF has another important characteristic i.e. it can operate even for very low supply voltages. The supply voltage can be reduced up to a minimum level for satisfactory performance of the circuit given by,

$$V_{dd}(\text{Min}) = V_{Tp} + 2\,V_{ds,sat} \qquad (3.20)$$

The output stage circuit is a class AB voltage buffer, where M10, M12 and M9, M11 respectively form two complementary DFVF cells with current sources I_{B1} and I_{B2} as can be seen in figure 3.9. This circuit offers moderate output swing and low output impedance.

3.3. Simulation Results

3.3.1. IC AD844 based Realization

The proposed circuit is operated at the supply voltage of ±5 V. To do the simulations, the PSPICE model file of AD844 IC (see Appendix A) supplied by Analog Devices is used.

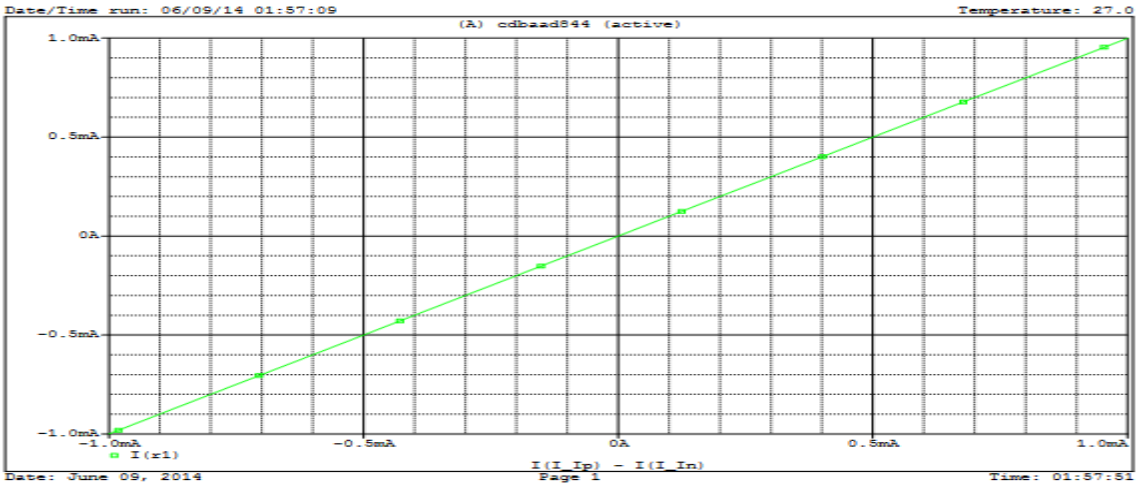

Fig. 3.13 Current transfer characteristics I_z VS $I_p - I_n$ (AD844)

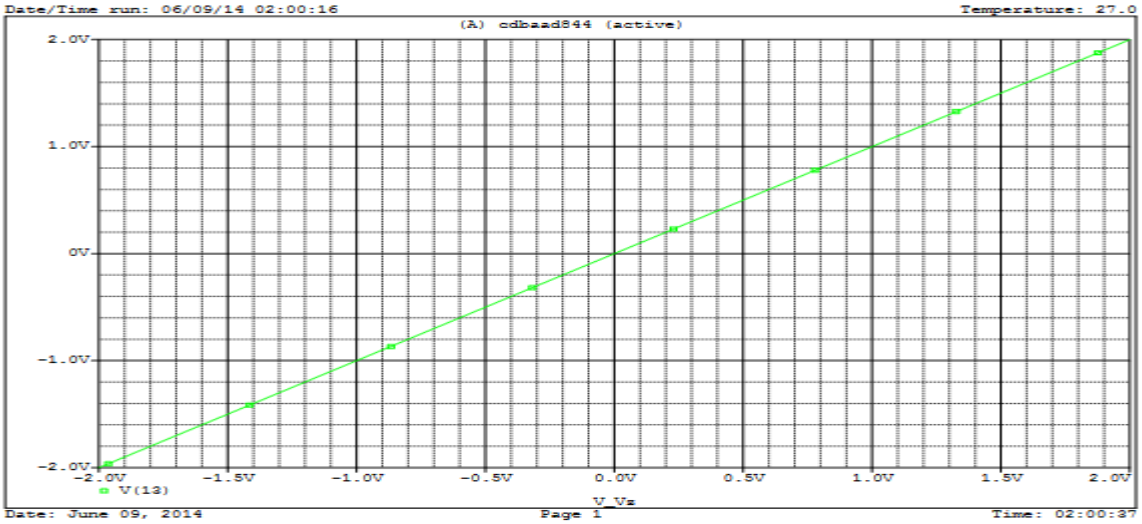

Fig. 3.14 Voltage transfer characteristics V_w VS V_z (AD844)

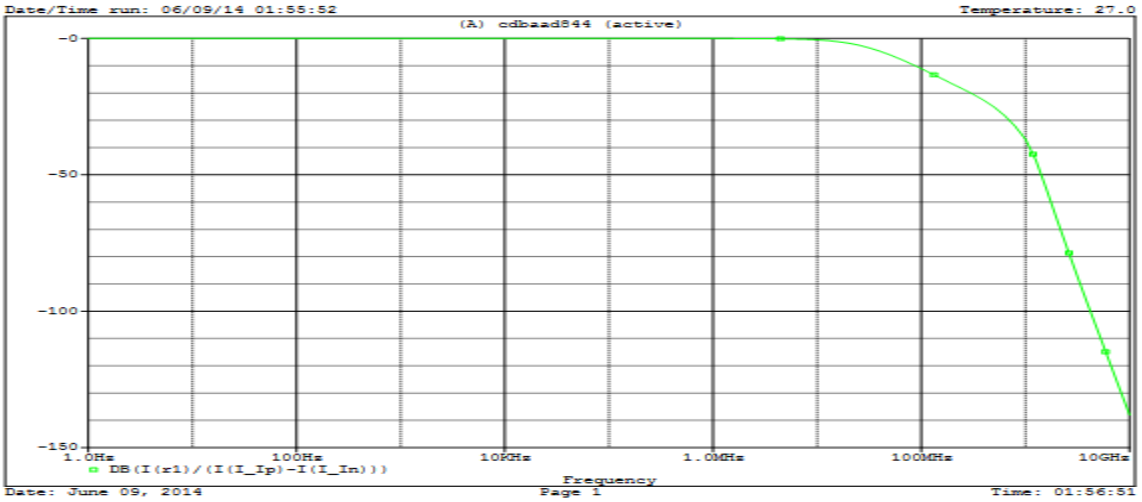

Fig. 3.15 Current transfer ratio frequency response (AD844)

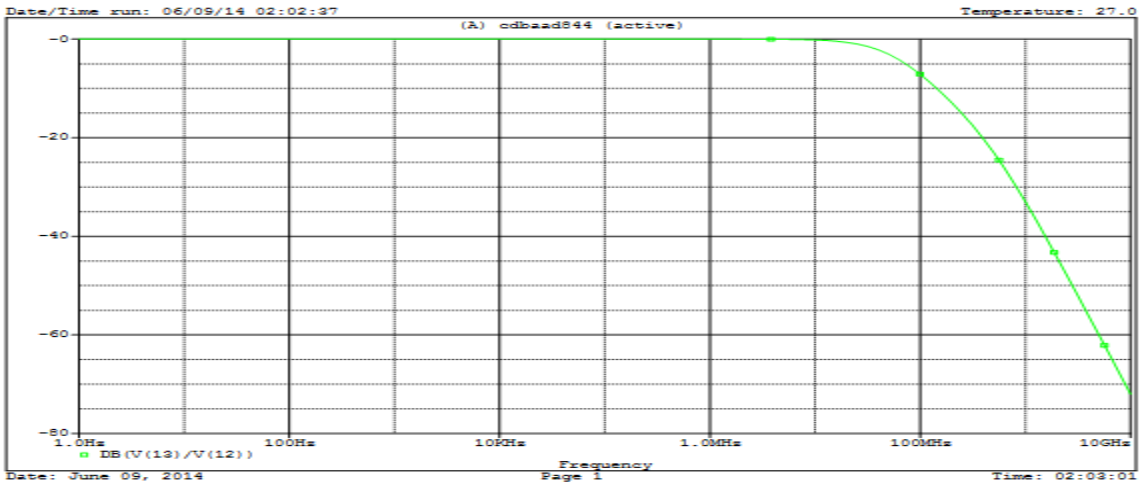

Fig. 3.16 Voltage transfer ratio frequency response (AD844)

The DC current characteristics and voltage transfer characteristics to realize the current are depicted in figure 3.13 and 3.14 respectively. It can be seen that these characteristics are linear for a large range. The current and voltage follow the given input current and voltages for as high as 1mA and 2V respectively and hence are found to be highly linear.

3.3.2. The LVLP CDBA

The supply voltage and the technology parameters used for the CDBA realization and its simulation are ±0.8 V and TSMC 0.18µm respectively. The bias currents of 56 µA and 84 µA are chosen respectively for I_{B1} and I_{B2} and dimension of the gate channel of the transistors used are mentioned in Table 3.1.

Transistor	W/L ratio (µm/ µm)
M1, M2, M3, M4	0.36/0.18
M5, M6	0.18/0.18
M7, M8	0.18/0.18
M9	0.45/0.36
M10	0.24/0.36
M11	0.72/0.36
M12	0.24/0.36
M13	0.72/0.36
M14	0.24/0.36

Table 3.1 MOS Transistor dimensions

For the current CDBA realization the DC current transfer characteristics are displayed in fig. 3.17. For the entire dynamic range at I_{B1} = 56µA the CDBA can be seen to be highly linear.

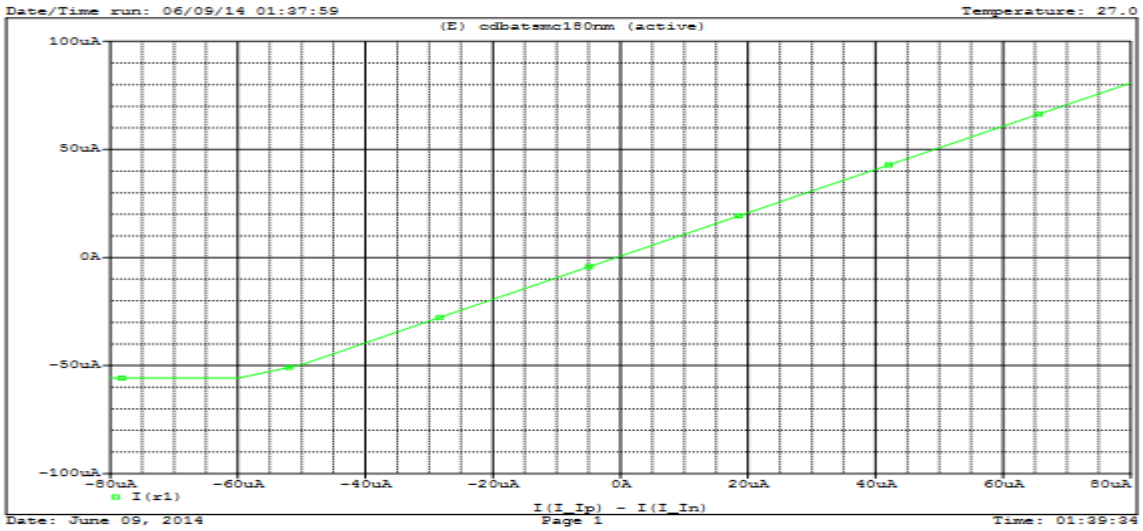

Fig. 3.17 Current transfer characteristics I_z VS $(I_p - I_n)$ (LVLP CDBA)

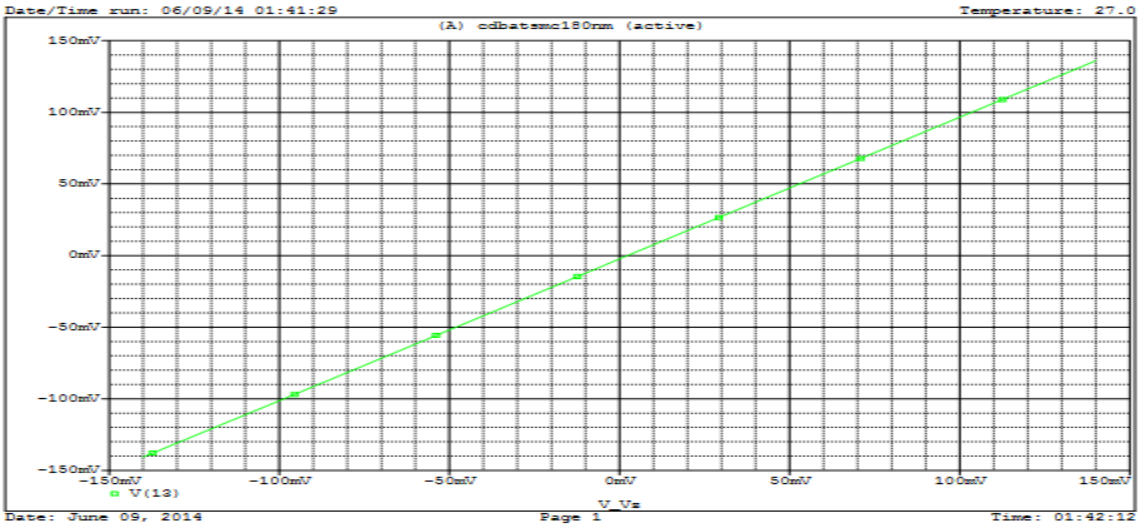

Fig. 3.18 Voltage transfer characteristics V_w VS V_z (LVLP CDBA)

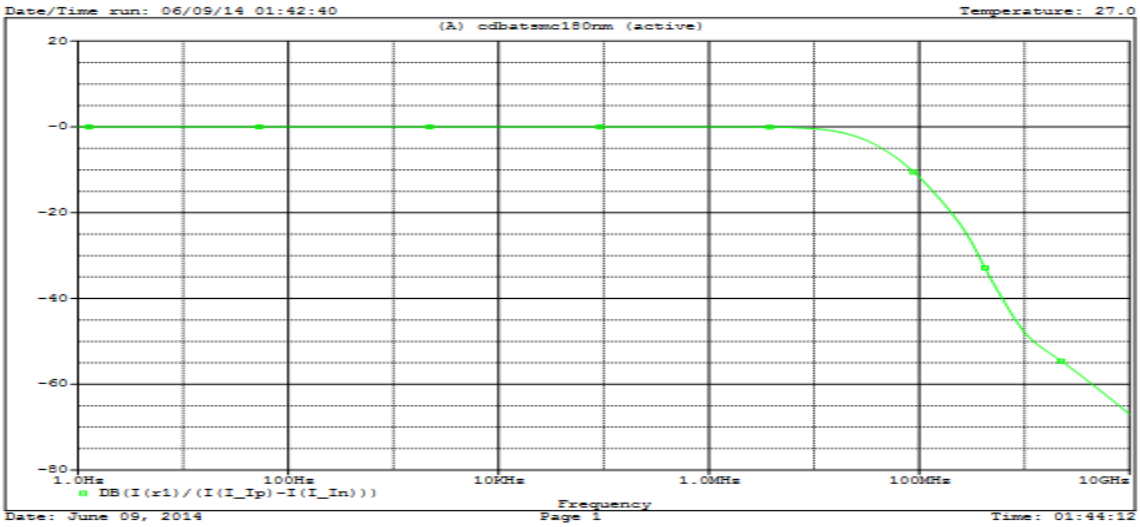

Fig. 3.19 Current transfer ratio frequency response (LVLP CDBA)

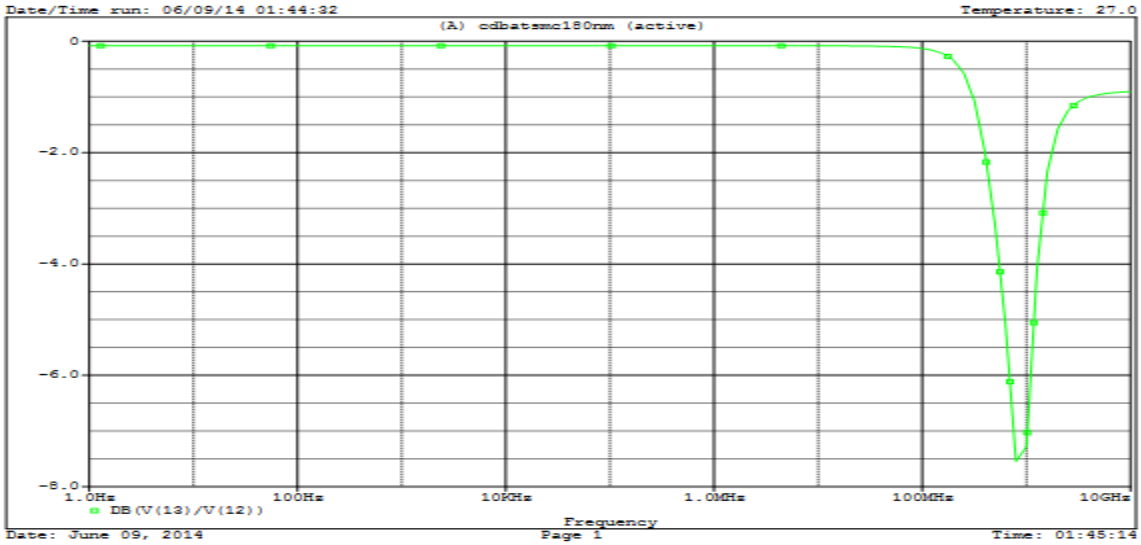

Fig. 3.20 Voltage transfer ratio frequency response (LVLP CDBA)

The output voltage, V_w which is proportional to V_z is shown by the DC voltage transfer characteristic, shown in figure 3.18. From figure 3.18 we can conclude that the voltage transfer error goes on increasing as the values of V_z starts to go beyond the range of ±100 mV.

Figure 3.19 and Figure 3.20 are representing the frequency response of current and voltage transfer ratio respectively as the AC transfer characteristics of the simulated LVLP CDBA.

3.3.3. Comparison

Various parameters of both the simulated realizations of the CDBA are shown in Table 3.2. It can be clearly seen from table 3.2 that in AD844 based realization the voltage and current follow the required values more closely but LVLP CDBA has very less power dissipation, better voltage and current transfer bandwidths and hence can be used for higher frequency range.

Parameter	**AD844 Realization**	**LVLP CDBA Realization**
Supply voltage (V)	±5	±0.8
Current transfer ratio, $\alpha = {I_z}/{(I_P - I_n)}$	0.9996	0.9861

Current transfer BW (MHz)	28.81	30.47
Voltage transfer ratio, $\beta = {V_w}/{V_z}$	0.9998	0.9310
Voltage transfer BW (MHz)	49	475
Power Dissipation (mW)	999.89	98.818

Table 3.2 Performance of the CDBA realizations

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CHAPTER 4: FILTER REALIZATIONS

4.1 Introduction

Filters are the electrical networks that process signal to modify its amplitude and/or phase characteristics in a frequency dependent manner. A filter never adds a new frequency neither it alters the component frequency of the input signal, it only varies the amplitude along with phase characteristics of the various frequency component present in the signal. Filters are often used in electronic systems to separate signals i.e. passing those of interest in certain frequency range and blocking the undesirable ones. The gain of such filters depends on signal frequency. Consider an example where the input signal comprises of desirable frequency F_1 along with an undesirable one F_2. A filter having a very low gain at F_2 and high gain at F_1 will attenuate the frequency F_2 and only useful frequency remains when the input signal is passed through it.

Analysis of filters is done in frequency domain, therefore to demonstrate its characteristics, generally phase vs. frequency and gain vs. frequency plots are used. Mathematically, Frequency domain behaviour of a filter is described with the term called Transfer Function which is represented as the ratio of the Laplace transform of the output signal to the input signal fed to the filter [1]. Therefore, the voltage transfer function is given by,

$$H(s) = \frac{V_{OUT}(s)}{V_{IN}(s)} \tag{4.1}$$

Where $V_{OUT}(s)$ and $V_{IN}(s)$ are the Laplace transform of the output and input signal voltages respectively.

The magnitude of the transfer function as a function of frequency is an important analysis as it shows the variation on the amplitudes of sinusoidal signals at different frequencies due to the presence of filter. The magnitude versus frequency of a transfer function is known as the amplitude response or frequency response. Also, the quantity of phase shift obtained in sinusoidal signals represented by a function of frequency is called its phase response. Since a variation in signal's phase also corresponds to a variation in time signal, hence the phase characteristics of a filter turn out to be essential while transacting with complex signals where the relationships between time and the signal components at different frequencies are critical. The effect of filter on the phase and magnitude of the input signal can be represented by replacing s with jω in the transfer function. The magnitude is obtained by taking its absolute value i.e.

$$\left|H(\mathrm{j}\omega) = \frac{V_{OUT}(\mathrm{j}\omega)}{V_{IN}(\mathrm{j}\omega)}\right| \tag{4.2}$$

And the phase is obtained as:

$$\arg H(\mathrm{j}\omega) = \arg \frac{V_{OUT}(\mathrm{j}\omega)}{V_{IN}(\mathrm{j}\omega)} \tag{4.3}$$

An ideal filter has its amplitude response equal to one for the particular range of frequencies (pass band frequencies) and zero for any other frequency range (stop band frequencies). The frequency at which the response transits from pass band frequencies to stop band frequencies is known as the cut-off frequency$\mathrm{f_c}$.

The two important parameters for consideration while designing filters are as follows: (i) 3 dB down frequency response from the pass band which is called cut-off frequency $\mathrm{f_c}$ (ii) quality factor (Q) which is shown as:

$$\alpha = \frac{1}{\mathrm{Q}} \tag{4.4}$$

The highest power of the variable s in the transfer function (Laplace transform format) of the designed filter is called its order. It defines the steepness of the designed filter. It can also be determined by calculating the number of poles (existing either on real or imaginary axis) in the transfer function which is in x/y pattern. A pole and a zero are the root of the denominator (y) and numerator (x) respectively. Basically the total number of inductors and capacitors connected in the circuit determines the order of the filter. The Higher-order filters are therefore more costly to build as they are complicated and require more number of components. But increasing the order the filter enhances its signal discriminating power at different frequencies.

4.2 CDBA based Filter Topologies

The ancient forms of electronic filter circuits designed using combinations of Resistor (R), Capacitor (C) and Inductor (L) only are called passive filters. However, active filters are constructed using passive elements and active components (like transistors). The filtering performances of modern active filters are better compared to passive ones; also they are smaller in physical size and more flexible in application. The op-amps are widely used for designing active filter. There are various other active blocks, available in literatures which are used to implement active filters. CDBA is one among of them [2]. There are many CDBA topologies used to construct active filters, we are focusing on two of them namely topology (A) and topology (B) which are explained in

further sections. Filters are also classified according to their response characteristics as low pass, high pass, all pass, band pass and notch. These are described in detail in the subsequent sections of the chapter and designed using the CDBA topologies.

4.2.1 Topology (A)

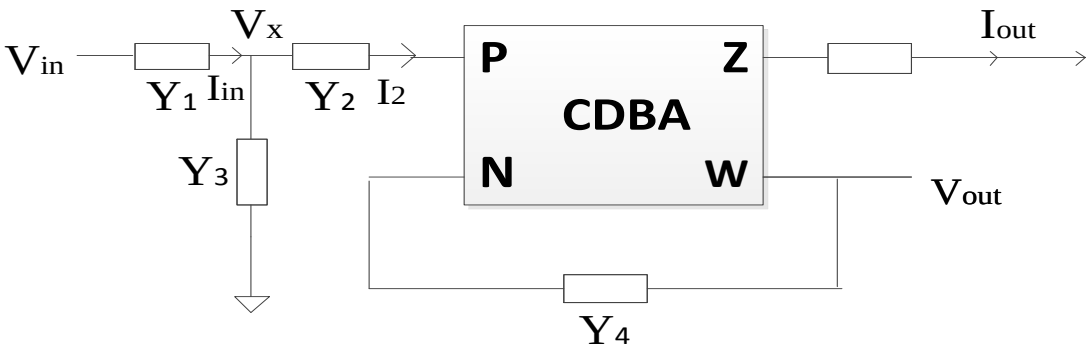

Fig. 4.1General filter topology (A) of CDBA [3]

Basic structure of multi-mode filter topology is shown in Fig.4.1 [3]. This structure consists of 4 or 5 passive elements and a single CDBA. Number of filter transfer functions calculated in CM, VM, TIM and TAM is 3 and is dependent on the passive elements used [3].

In the above topologies only VM topology is utilized to analyze the configuration for Filters. The voltage input V_{IN} is required to carry out VM analysis.

Using characteristic equations of CDBA given in chapter 3, the transfer function can be derived as follows:

Applying KCL at node V_X,

$$(V_{IN} - V_X)\, Y_1 = V_X Y_3 + V_X Y_2 \tag{4.5}$$

$$\frac{V_X}{V_{IN}} = \frac{Y_1}{(Y_1+Y_2+Y_3)} \tag{4.6}$$

Using characteristic equations of CDBA,

$$V_{OUT} Y_5 = V_X Y_2 - V_{OUT} Y_4 \tag{4.7}$$

$$\frac{V_{OUT}}{V_X} = \frac{Y_2}{(Y_4+Y_5)} \tag{4.8}$$

Multiplying $\frac{V_X}{V_{IN}}$ and $\frac{V_{OUT}}{V_X}$,

$$\frac{V_{OUT}}{V_{IN}} = \frac{Y_1 Y_2}{(Y_1+Y_2+Y_3)(Y_4+Y_5)} \tag{4.9}$$

Where Y_1, Y_2, Y_3, Y_4, Y_5 are the admittance in the CDBA filter topology

4.2.1.1 Low Pass Filter

It gives a smooth passage to low frequency signals and rejects the high frequency signals more than the filter's cut off frequency (f_c). They find their application in systems or part of the system where high frequency components are to be removed from the signal. In general the transfer function (in frequency domain) of the low pass filter is as follows,

$$H(s) = \frac{H_o}{s^2+\frac{\omega_0}{Q}s+{\omega_0}^2} \tag{4.10}$$

Where $H_o$is pass band gain and $\omega_0 = 2\,\pi\, f_c$

Low pass filter can be designed using topology (A) of CDBA by selecting the appropriate components. For that the following G and C replacements for the admittance of the transfer function given in section 4.2.1 are done,

$Y_1 = G_1,\ Y_2 = G_2, Y_3 = sC_3,\ Y_4 = G_4,\ Y_5 = sC_5$

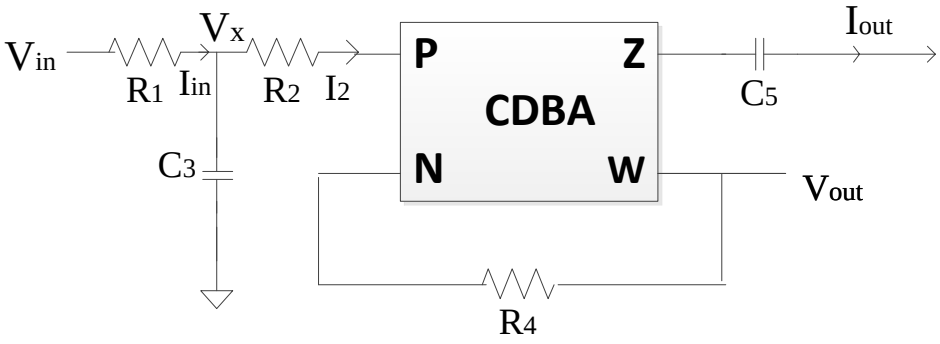

Fig. 4.2 Low pass second order filter design using CDBA [3]

By putting the above replacements transfer function of topology (A), we get transfer function for low power filter,

$$\frac{V_{OUT}}{V_{IN}} = \frac{G_1G_2}{(G_1+G_2+sC_3)(G_4+sC_5)}$$

$$= \frac{G_1G_2}{s^2C_3C_5+s(C_3G_4+C_5G_1+C_5G_2)+G_4(G_1+G_2)}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{\frac{G_1G_2}{C_3C_5}}{s^2+s\frac{(C_3G_4+C_5G_1+C_5G_2)}{C_3C_5}+\frac{G_4(G_1+G_2)}{C_3C_5}} \tag{4.11}$$

The natural frequency ω_0 and quality factor Q can be determined by the transfer function;

$$\omega_0 = \sqrt{\frac{G_4(G_1+G_2)}{C_3C_5}} \tag{4.12}$$

and

$$\frac{\omega_0}{Q} = \frac{(C_3G_4+C_5G_1+C_5G_2)}{C_3C_5} \tag{4.13}$$

So,

$$Q = \frac{\sqrt{C_3C_5G_4(G_1+G_2)}}{C_3G_4+C_5G_1+C_5G_2} \tag{4.14}$$

PSPICE simulations for the designed filters namely low pass, high pass and band pass made out of topology A is done to verify the behaviour and match them with that existing in theory.

CDBA active block used is realized using the commercially available AD844 IC and its macro PSPICE model is used for simulations with a power supply voltage of ±5V. The simulation results for each of the filter type is presented as and when each of them is analysed. The component values for low pass filter are chosen as R1 =100, R2 =1K, C3 =1nF, R4 =1K and C5 = 10nF. Frequency response of the gain of the designed low pass filter is depicted in figure 4.3.

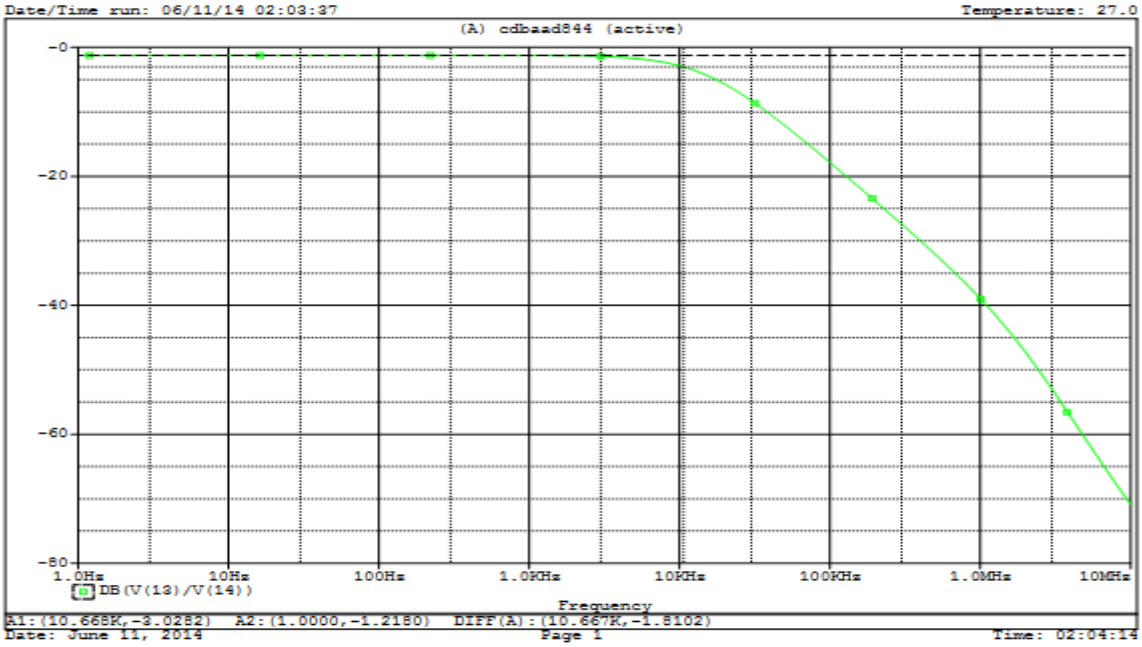

Fig. 4.3 Frequency response of the low pass filter

4.2.1.2 High Pass Filter

It passes the high frequency signals through it and rejects the signals below its cut of frequency (f_c). High pass filter can be applied to reject dc offset in the high gain amplifiers. The transfer function (in frequency domain) of high pass filter can be determined by adding a s^2 term in the numerator of the transfer function of the low pass filter and is shown as,

$$H(s) = \frac{H_o s^2}{s^2 + \frac{\omega_0}{Q} s + {\omega_0}^2} \tag{4.15}$$

High pass filter design using topology (A) of CDBA can be implemented by appropriate selection of components. To accomplish that the following G and C replacements for the admittance in transfer function given in section 4.2.1 are designed,

$Y_1 = sC_1,\ Y_2 = sC_2, Y_3 = G_3,\ Y_4 = G_4,\ Y_5 = sC_5$

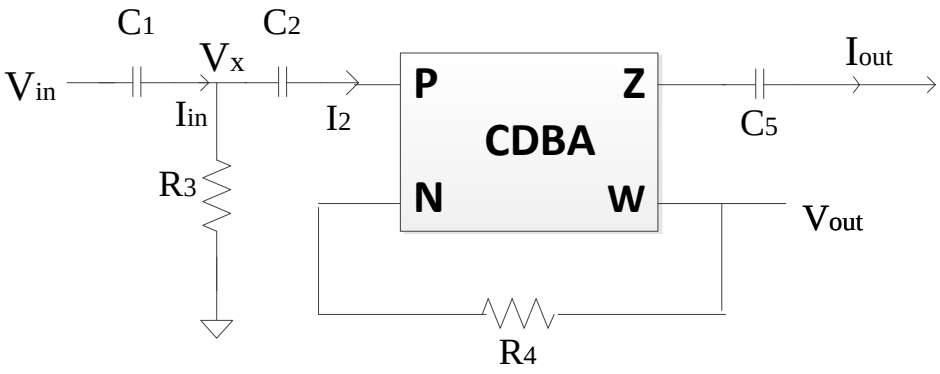

Fig. 4.4 High pass second order filter design using CDBA [3]

$$\frac{V_{OUT}}{V_{IN}} = \frac{s^2 C_1 C_2}{(sC_1 + sC_2 + G_3)(G_4 + sC_5)}$$

$$= \frac{sC_1 G_2}{s^2(C_1 + C_2)C_5 + s(C_1 G_4 + C_2 G_4 + C_5 G_3) + G_3 G_4}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{\frac{s^2 C_1 C_2}{(C_1 + C_2)C_5}}{s^2 + s\frac{(C_1 G_4 + C_2 G_4 + C_5 G_3)}{(C_1 + C_2)C_5} + \frac{G_3 G_4}{(C_1 + C_2)C_5}} \tag{4.16}$$

The natural frequency ω_0 and quality factor Q for high pass filter can be determined from the transfer function;

$$\omega_0 = \sqrt{\frac{G_3 G_4}{(C_1 + C_2)C_5}} \tag{4.17}$$

and

$$\frac{\omega_0}{Q} = \frac{(C_1 G_4 + C_2 G_4 + C_5 G_3)}{(C_1 + C_2)C_5} \tag{4.18}$$

So,

$$Q = \frac{\sqrt{C_5 G_3 G_4 (C_1 + C_2)}}{C_1 G_4 + C_2 G_4 + C_5 G_3} \tag{4.19}$$

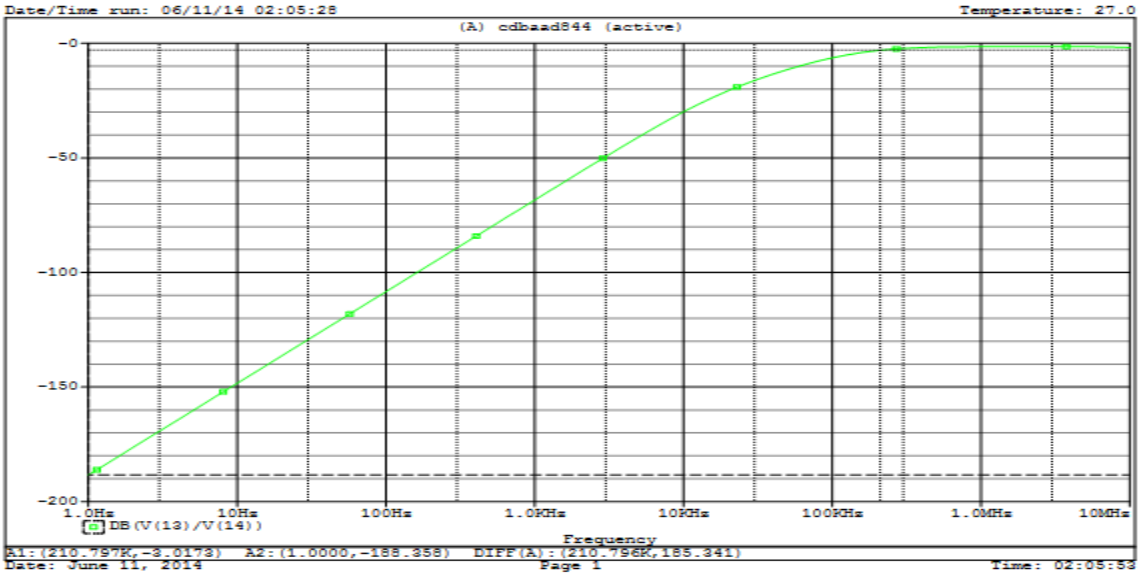

Fig. 4.5 Frequency response of the high pass filter

The values of capacitors and resistors used in high pass filter are chosen as C1 =1nF, C2 =0.1nF, R3 =1K, R4 =100K and C5 = 0.1nF.

4.2.1.3 Band Pass Filter

It passes a specific range of frequencies through it, while attenuating lower and higher frequencies lying outside the desired range of frequencies. The band pass filter is commonly used in audio signal processing, where a definite range of useful frequencies of sound are passed while others are blocked. Changing the numerator of low pass filter's transfer function will convert it to band pass filter given by,

$$H(s) = \frac{H_o \frac{\omega_0}{Q} s}{s^2 + \frac{\omega_0}{Q} s + {\omega_0}^2} \tag{4.20}$$

Suitable component selection in topology (A) of CDBA can lead to the construction of band pass filter. The admittance can be replaced with proper selection of these components i.e. proper G and C to get the band pass filter design,

$\boldsymbol{Y_1} = sC_1,\ \boldsymbol{Y_2} = G_2, \boldsymbol{Y_3} = sC_3,\ \boldsymbol{Y_4} = G_4,\ \boldsymbol{Y_5} = sC_5$

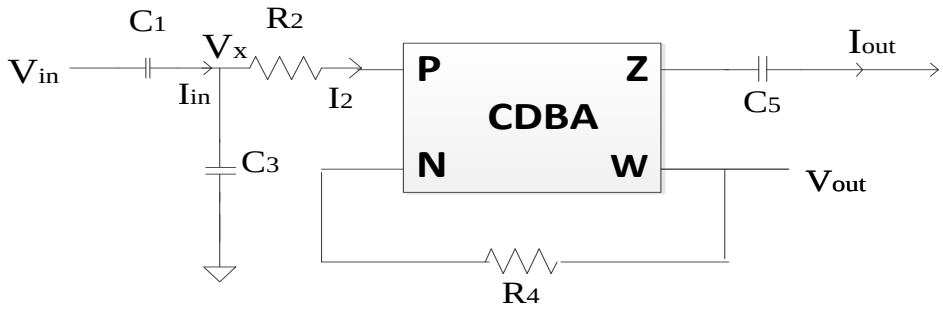

Fig. 4.6 Band pass second order filter design using CDBA [3]

$$\frac{V_{OUT}}{V_{IN}} = \frac{sC_1G_2}{(sC_1+G_2+sC_3)(G_4+sC_5)}$$

$$= \frac{sC_1G_2}{s^2(C_1+C_3)C_5+s(C_1G_4+C_3G_4+C_5G_2)+G_2G_4}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{\frac{sC_1G_2}{(C_1+C_3)C_5}}{s^2+s\frac{(C_1G_4+C_3G_4+C_5G_2)}{(C_1+C_3)C_5}+\frac{G_2G_4}{(C_1+C_3)C_5}} \quad (4.21)$$

The natural frequency ω_0 and quality factor Q for band pass filter can be determined from the transfer function;

$$\omega_0 = \sqrt{\frac{G_2G_4}{(C_1+C_3)C_5}} \quad (4.22)$$

and

$$\frac{\omega_0}{Q} = \frac{(C_1G_4+C_3G_4+C_5G_2)}{(C_1+C_3)C_5} \quad (4.23)$$

So,

$$Q = \frac{\sqrt{C_5G_2G_4(C_1+C_3)}}{C_1G_4+C_3G_4+C_5G_2} \quad (4.24)$$

The component values for band pass filter are chosen as C1 =2.2nF, R2 =470, C3 =10nF, R4 =4.7K and C5 = 1nF.

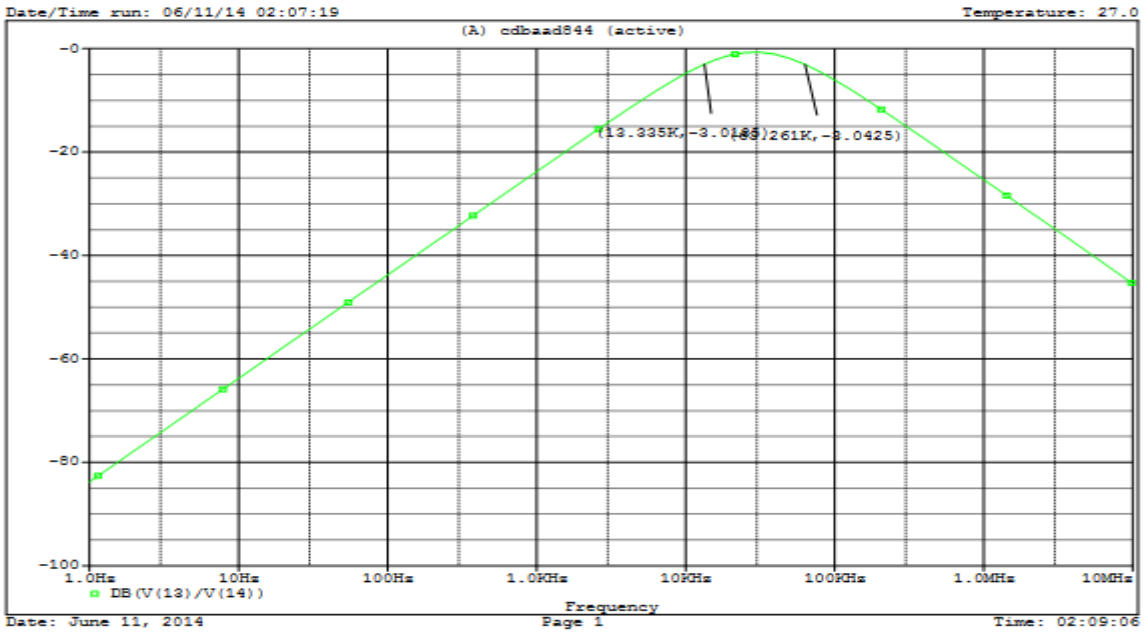

Fig. 4.7 Frequency response of the gain of band pass filter

4.2.2 Topology (B)

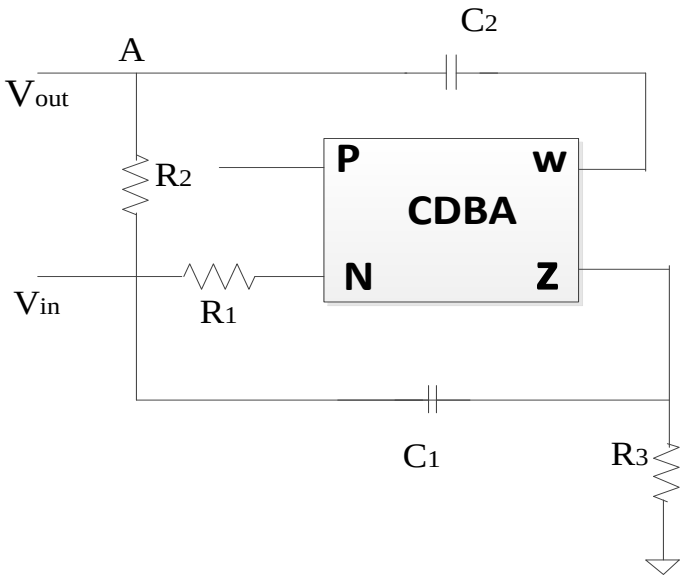

Fig. 4.8 Filter topology (B) of CDBA [4]

The topology (B) of filter design is shown in Fig. 4.8.This topology of CDBA comprises of 2 capacitors, 3 resistors and a CDBA block.

By using characteristic equations of CDBA given in chapter 3, the transfer function can be derived as follows:

$$I_p = 0,\ I_n = \frac{V_{IN}}{R_1},\quad I_z = -I_n = -\frac{V_{IN}}{R_1} \tag{4.25-4.27}$$

$$I_Z = \frac{V_z}{R_3} + (V_z - V_{IN})sC_1 \tag{4.28}$$

So,

$$V_z = \frac{sC_1 - \frac{1}{R_1}}{\frac{1}{R_3} + sC_1} V_{IN} \tag{4.29}$$

Applying KCL at node A and substituting value of V_z we get,

$$V_{OUT}\frac{(sC_2R_2+1)}{R_2}\frac{(sC_1R_3+1)}{R_3} = V_{IN}\left[sC_2\left(sC_1 - \frac{1}{R_1}\right) + \frac{sC_1R_3+1}{R_2R_3}\right]$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{s^2 + s\left(\frac{1}{C_2R_2} - \frac{1}{C_1R_1}\right) + \frac{1}{C_1C_2R_2R_3}}{s^2 + s\left(\frac{1}{C_2R_2} + \frac{1}{C_1R_3}\right) + \frac{1}{C_1C_2R_2R_3}} \tag{4.30}$$

4.2.2.1 All Pass Filter

An all pass filter does not affect the amplitude of the signal at different frequencies. It can be utilised to shift the phase of the input signal. Therefore it is also known as phase shift filter. They are used in pulsed circuits to provide phase equalization. Their application also includes Single side band-suppressed carrier modulation circuits. The transfer function (in frequency domain) of all pass filters is,

$$H(s) = \frac{s^2 - \frac{\omega_0}{Q}s + {\omega_0}^2}{s^2 + \frac{\omega_0}{Q}s + {\omega_0}^2} \tag{4.31}$$

An all pass filter using topology (B) is obtained by doing the following substitutions in transfer function obtained for topology B:

$$\frac{1}{C_1R_1} = \frac{2}{C_2R_2} + \frac{1}{C_1R_3} \tag{4.32}$$

Resulting transfer function obtained after the substitution is,

$$\frac{V_{OUT}}{V_{IN}} = \frac{s^2 - s\left(\frac{1}{C_2R_2} + \frac{1}{C_1R_3}\right) + \frac{1}{C_1C_2R_2R_3}}{s^2 + s\left(\frac{1}{C_2R_2} + \frac{1}{C_1R_3}\right) + \frac{1}{C_1C_2R_2R_3}} \tag{4.33}$$

The natural frequency ω_0 and quality factor Q for all pass filter can be determined from the transfer function;

$$\omega_0 = \sqrt{\frac{1}{C_1C_2R_2R_3}} \tag{4.34}$$

and

$$\frac{\omega_0}{Q} = \frac{1}{C_2R_2} + \frac{1}{C_1R_3} \tag{4.35}$$

$$\text{So, } Q = \frac{\sqrt{C_1C_2R_2R_3}}{C_1R_3 + C_2R_2} \tag{4.36}$$

PSPICE simulations for the all pass and notch filter derived from topology B is carried out to verify their functional behaviour. For simulation LVLP CDBA, designed using TSMC 0.18µm technology parameters with power supply of ±0.8V, is used.

The component values for all pass filter are chosen as R1 =2K R2 =6K R3 = 6K C1 =25pF and C2= 25pF. The magnitude frequency response of the all pass filter is shown in figure 4.9.

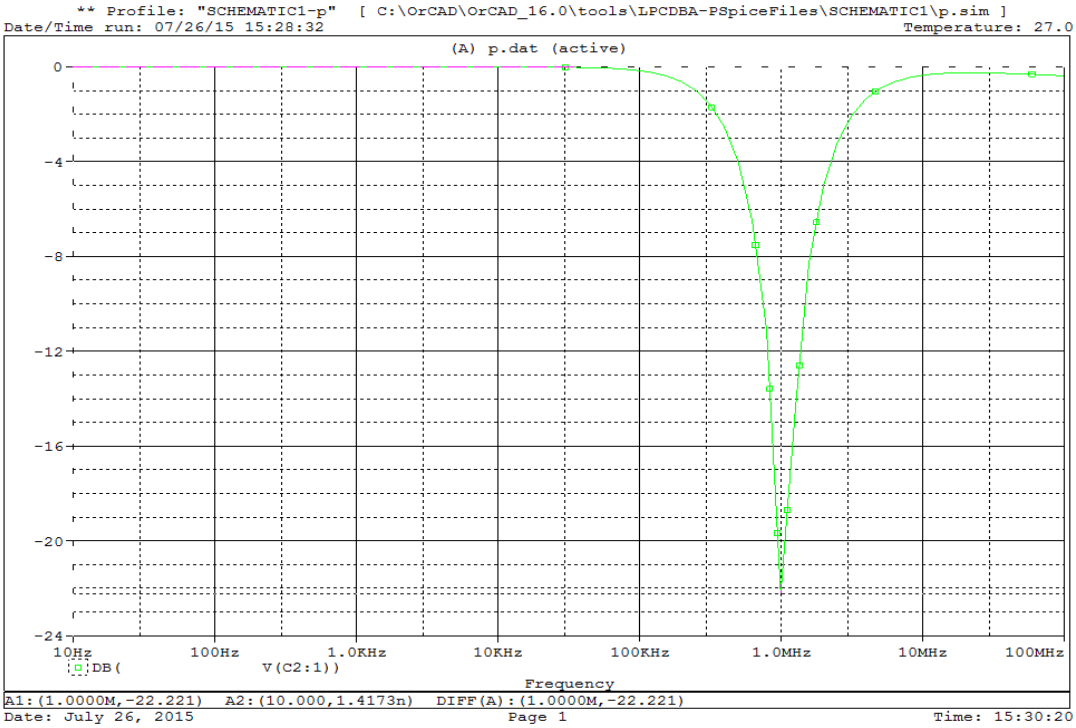

Fig. 4.9 Frequency v/s gain response of all pass filter

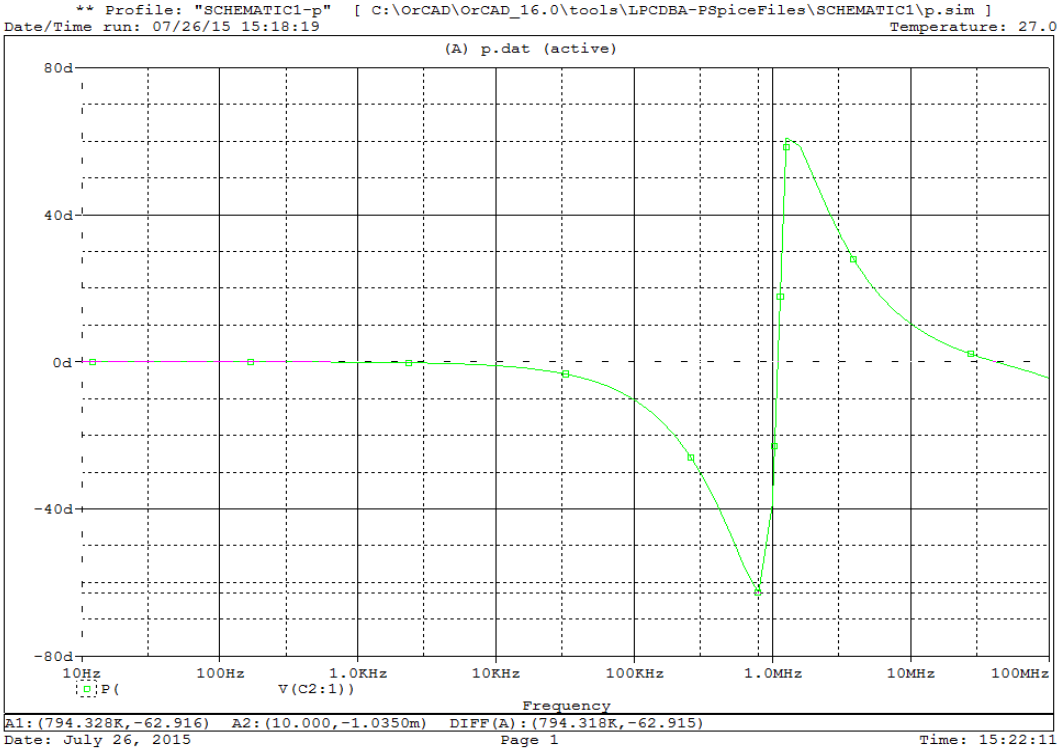

Fig. 4.10 phase response of the all pass filter

4.2.2.2 Notch Filter

It is also known as narrow band reject filter. The notch filter passes the entire frequency components lying outside its narrow stop-band. The transfer function is shown as:

$$H(s) = \frac{s^2+{\omega_0}^2}{s^2+\frac{\omega_0}{Q}s+{\omega_0}^2} \tag{4.37}$$

A second order notch filter based on topology (B) can be analysed by satisfying the following matching condition,

$$C_1R_1 = C_2R_2 \tag{4.38}$$

The transfer function is obtained by substituting the above equation in general transfer function of topology (B),

$$\frac{V_{OUT}}{V_{IN}} = \frac{s^2+\frac{1}{C_1C_2R_2R_3}}{s^2+s\left(\frac{1}{C_2R_2}+\frac{1}{C_1R_3}\right)+\frac{1}{C_1C_2R_2R_3}} \tag{4.39}$$

The natural frequency ω_0 and quality factor Q of notch filter is same as obtained for all pass filter;

$$\omega_0 = \sqrt{\frac{1}{C_1C_2R_2R_3}} \tag{4.40}$$

And

$$Q = \frac{\sqrt{C_1C_2R_2R_3}}{C_1R_3+C_2R_2} \tag{4.41}$$

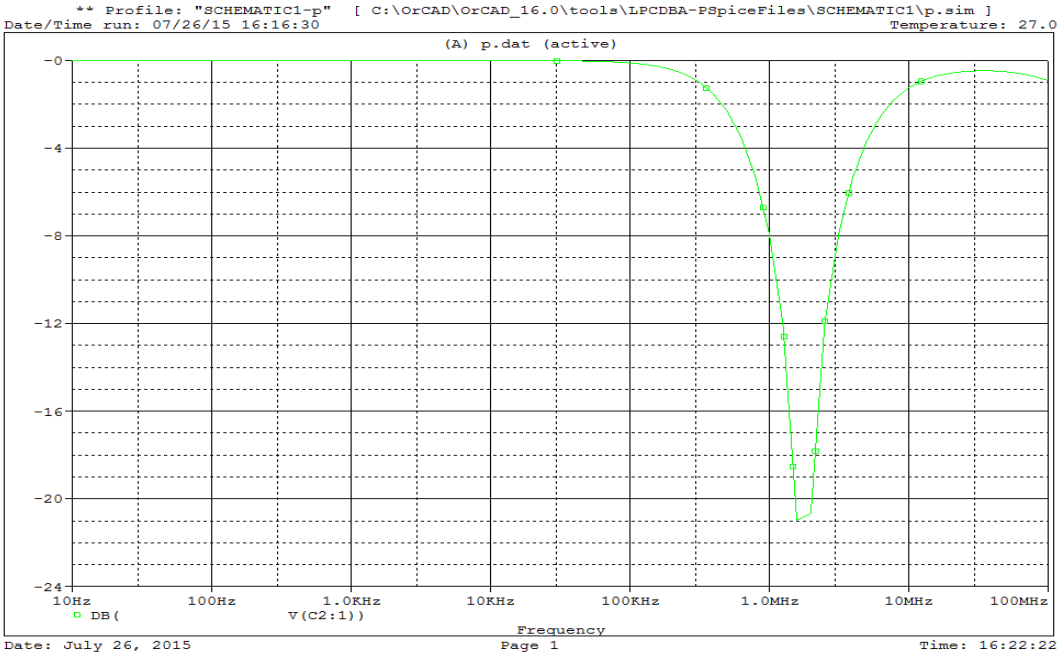

Fig. 4.11 Frequency v/s gain response of the notch filter

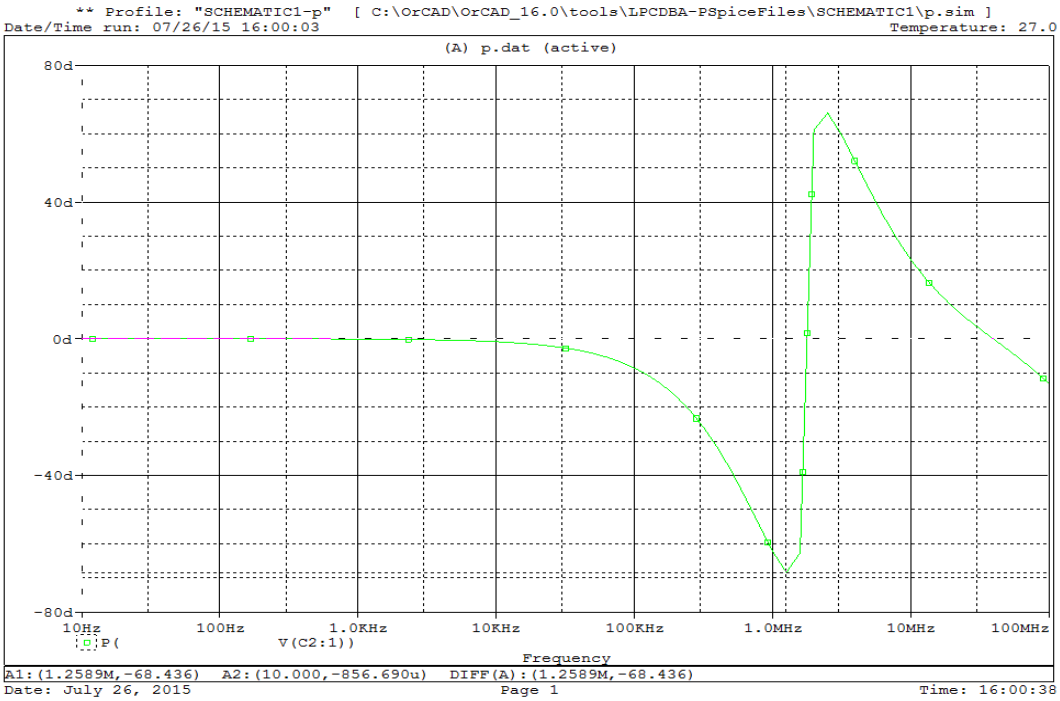

Fig. 4.12 phase response of the notch filter

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CHAPTER 5: CDBA BASED OSCILLATORS

5.1 Introduction

Signal generators are an important class of electronic circuits and find wide applications in communication, measurement, instrumentation and power electronics. Circuits, which generate sine waves utilizing resonance phenomena, are known as linear oscillators whereas those, generating square, triangular, pulse (etc.) waveforms, are called nonlinear oscillators or function generators. Nonlinear oscillators employ circuit building blocks known as multi-vibrators**.**

The basic structure of a sinusoidal oscillator consists of an amplifier and a RC or LC frequency selective network connected in a positive-feedback loop, such as that shown in block diagram form in Fig.5.1. Although in an actual oscillator circuit, input signal is not be present, which has been included in Fig. 5.1 to help explain the principle of operation.

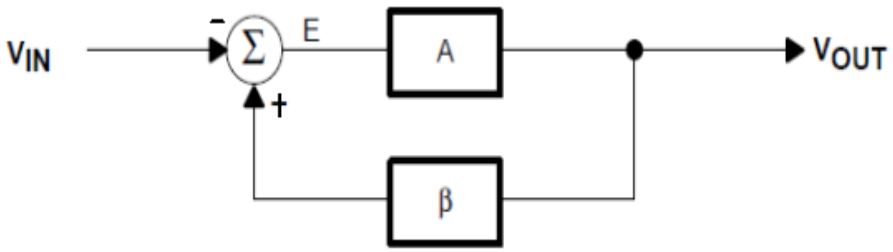

Fig.5.1 Basic structure of oscillator [1]

Considering Av as voltage gain of amplifier without feedback, βv as feedback fraction and Avf to be voltage gain of amplifier with feedback, the voltage gain of a positive feedback amplifier of Fig.5.1 is given by;

$$Avf = \frac{Av}{1 - \beta v\, Av}$$

If $\beta v\, Av = 1$ then $Avf \rightarrow$ infinity. It means that a vanishing small input voltage would give rise to finite (*i.e.*, a definite amount of) output voltage even when the input signal is zero. Thus once the circuit receives the input trigger, it would become an oscillator, generating oscillations with no external signal source. This condition is called the Barkhausen criterion [1].

The loop gain is given by

$$L(S) = A(S).\beta(S) \tag{5.1}$$

Characteristics equation gives rise to

$$1 - L(S) = 0 \tag{5.2}$$

We know that $S = j\omega_0$ where ω_0 is the frequency of oscillation

In order to produce continuous undamped oscillations at the output of an amplifier, the positive feedback should be such that

$$\beta v\ Av = 1$$

With total phase of loop should be 0^0 or 360^0

Once this condition is set in the positive feedback amplifier, continuous undamped oscillations can be obtained at the output immediately after connecting the necessary power supply.

The frequency of oscillation ω_0 is determined solely by the phase characteristics of the feedback loop, the loop oscillates at the frequency for which the phase is zero. It follows that the stability of the frequency of oscillation will be determined by the manner in which the phase Φ (ω_0) of the feedback loop varies with frequency. A "steep" function Φ (ω_0) will result in a more stable frequency [1].

5.2 Total Harmonic Distortion

The term harmonics referred to Power quality in ideal world would mean how pure the voltage is, how pure the current waveform is in its sinusoidal form. Power quality is very important to commercial and industrial power system designs. Ideally, the electrical supply should be a perfect sinusoidal waveform without any kind of distortion. If the current or voltage waveforms are distorted from its ideal form it will be termed as harmonic distortion. This harmonic distortion could result because of many reasons. In today's world, prime importance is given by the engineers to derive a method to reduce the harmonic distortion. Harmonic distortion was very less in the past when the designs of power systems were very simple and conservative. But, nowadays with the use of complex designs in the industry harmonic distortion has increased as well.

The harmful and damaging effects of harmonic distortion can be evident in many different ways such as electronics miss-timings, increased heating effect in electrical equipments, capacitor overloads, etc

Fig. 5.2: AC source and an electrical load

Fig 5.3: (a) Ideal Sine wave (b) Distorted Waveform

As can be observed from the waveform in Figure 5.3, waveform distortions can drastically alter the shape of the sinusoid. However, no matter the level of complexity of the fundamental wave, it is actually just a composite of multiple waveforms called harmonics. Harmonics have frequencies that are integer multiples of the waveform's fundamental frequency. For example, given a 60Hz fundamental waveform, the 2nd, 3rd, 4th and 5^{th} harmonic components will be at 120Hz, 180Hz, 240Hz and 300Hz respectively. Thus, harmonic distortion is the degree to which a waveform deviates from its pure sinusoidal values as a result of the summation of all these harmonic elements. The ideal sine wave has zero harmonic components. In that case, there is nothing to distort this perfect wave.

Total harmonic distortion, or THD, is the summation of all harmonic components of the voltage or current waveform compared against the fundamental component of the voltage or current wave:

$$THD=\frac{\sqrt{(V_2^2+V_3^2+V_4^2+\cdots\ldots V_n^2)}}{V_1} *100 \text{ [1]}$$

The formula above shows the calculation for THD on a voltage signal. The end result is a percentage comparing the harmonic components to the fundamental component of a signal. The higher the percentage, the more distortion that is present on the mains signal.

5.3 Second Order Quadrature Oscillator

Quadrature oscillators (QO) produce outputs having a phase difference of 90°. The phase-locked sine-cosine relationship of QO has useful applications in the field of talecommunications where the modulation scheme utilizes both in-phase and quadrature components, such as in single-sideband generators, and quadrature mixers [2]. The QOs are also used extensively in the field of instrumentation and power electronics [3]. For these applications low value of total harmonic distortion (THD) is an essential requirement as higher harmonics have detrimental effects on electrical equipment..

In [4] a systematic approach to realize QOs and to get 12 QO circuits which oscillate at same frequency, having quadrature phase difference, using CDBA has been presented. This approach has been given section 5.1.1 for ready reference.

The QO circuits derived in [4] have following attractive features:

(i) Minimum number of passive components are employed which also removes the need of component matching.

(ii) Very low passive and active sensitivities

(iii) Low harmonic distortion

(iv) Separate resistor pairs are used to control the CO and FO of the circuits hence enabling fully uncoupled control.

(v) Looking from the integrated circuit implementation perspective, the circuits have the added advantage, as resistors and capacitors are grounded/virtually grounded.

5.3.1 Systematic approach to realize QO circuits

A general scheme consists of a first order LPF block and an integrator bock out of which one of them is working in inverting configuration is used to realize a second order QO. The scheme is shown in Fig. 5.4.

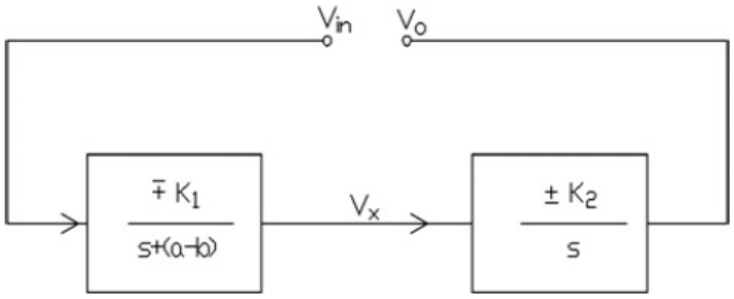

Fig. 5.4 General scheme for QO realization [4]

The voltage transfer functions of the first-order LPF $T_1(s)$ is of type:

$$T_1(S) = \frac{V_X}{V_{in}} = \frac{K_1}{S+(a-b)} \tag{5.3}$$

Where,

K_1 and K_2 the gain constants

a and b the pole frequency

And integrator's voltage transfer function $T_2(s)$ is assumed to be of the type:

$$T_2(s) = \frac{V_O}{V_X} = \frac{K_2}{S} \tag{5.4}$$

For the oscillator circuit the loop gain can be expressed as:

$$\frac{V_o}{V_{in}} = T_1(s)T_2(s) = \frac{K_1K_2}{s[s+(a-b)]} \tag{5.3}$$

The desired characteristic transfer function of the QO need to have the inverting configuration i.e. open loop gain of the LPF and integrator topology need to have a negative gain. This need gets us to a conclusion that one of LPF or integrators has a negative gain i.e. out of K_1 and K_2 one of them is negative. In either of the above two cases, we obtain

$$\frac{V_o}{V_{in}} = T_1(s)T_2(s) = \frac{-K_1K_2}{s[s+(a-b)]} \tag{5.5}$$

Hence the closed-loop characteristic equation is given by:

$$s^2 + s(a-b) + K_1K_2 = 0 \tag{5.5}$$

Therefore the CO is:

$$a = b$$

And the FO is found to be:

$$f_o = \frac{\sqrt{K_1 K_2}}{2\pi} \tag{5.6}$$

(In the above equation, only magnitudes of K1 and K2 are considered)

5.3.2 Generation of various QO configurations using CDBAs

The generalized scheme developed in the previous section is used to generate QOs. These QOs use two CDBA blocks each to realize the LPF and integrator block of the configuration.

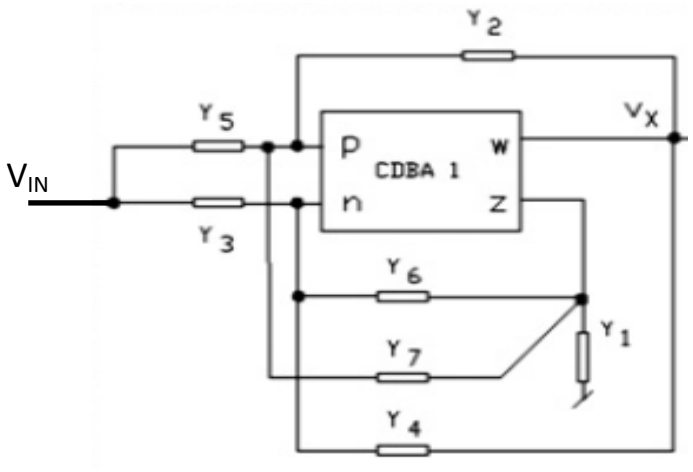

Fig. 5.5 General configuration for LPF block [4]

The generalized configuration for the LPF block is shown in Figure 5.5 and its transfer function is found to be:

$$\frac{V_X}{V_{in}} = \frac{(Y_5 - Y_3)}{(Y_1 + 2Y_6 + Y_4 - Y_2)} \tag{5.7}$$

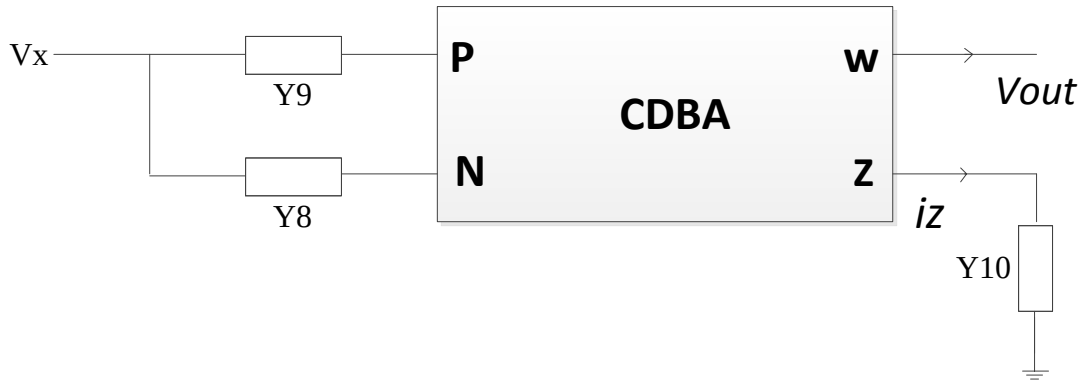

Fig. 5.6 General configuration for integrator block [4]

Figure 5.6 depicts the same for integrator block and its transfer function is given by:

$$\frac{V_o}{V_X} = \frac{Y_9 - Y_8}{Y_{10}} \tag{5.8}$$

S.No.	Low pass filter circuits							Integrator circuits			
	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	$T_1(S)$	Y_8	Y_9	Y_{10}	$T_2(S)$
1	sC_1	$\frac{1}{R_2}$	$\frac{1}{R_3}$	$\frac{1}{R_4}$	0	0	$\frac{-1}{C_1 R_3\left[s+\frac{1}{C_1}\left(\frac{1}{R_4}-\frac{1}{R_2}\right)\right]}$	0	$\frac{1}{R_9}$	sC_{10}	$\frac{1}{sC_{10}R_9}$
2	sC_1	$\frac{1}{R_2}$	$\frac{1}{R_3}$	0	0	$\frac{1}{R_6}$	$\frac{-1}{C_1 R_3\left[s+\frac{1}{C_1}\left(\frac{2}{R_6}-\frac{1}{R_2}\right)\right]}$	0	$\frac{1}{R_9}$	sC_{10}	$\frac{1}{sC_{10}R_9}$
3	sC_1	$\frac{1}{R_2}$	0	$\frac{1}{R_4}$	$\frac{1}{R_5}$	0	$\frac{1}{C_1 R_5\left[s+\frac{1}{C_1}\left(\frac{1}{R_4}-\frac{1}{R_2}\right)\right]}$	$\frac{1}{R_8}$	0	sC_{10}	$\frac{-1}{sC_{10}R_8}$
4	sC_1	$\frac{1}{R_2}$	0	0	$\frac{1}{R_5}$	$\frac{1}{R_6}$	$\frac{1}{C_1 R_5\left[s+\frac{1}{C_1}\left(\frac{2}{R_6}-\frac{1}{R_2}\right)\right]}$	$\frac{1}{R_8}$	0	sC_{10}	$\frac{-1}{sC_{10}R_8}$
5	$\frac{1}{R_1}$	$\frac{1}{R_2}$	$\frac{1}{R_3}$	sC_4	0	0	$\frac{-1}{C_4 R_3\left[s+\frac{1}{C_4}\left(\frac{1}{R_1}-\frac{1}{R_2}\right)\right]}$	0	$\frac{1}{R_9}$	sC_{10}	$\frac{1}{sC_{10}R_9}$
6	$\frac{1}{R_1}$	$\frac{1}{R_2}$	0	sC_4	$\frac{1}{R_5}$	0	$\frac{1}{C_4 R_5\left[s+\frac{1}{C_4}\left(\frac{1}{R_1}-\frac{1}{R_2}\right)\right]}$	$\frac{1}{R_8}$	0	sC_{10}	$\frac{-1}{sC_{10}R_8}$
7	$\frac{1}{R_1}$	$\frac{1}{R_2}$	$\frac{1}{R_3}$	0	0	sC_6	$\frac{-1}{2C_6 R_3\left[s+\frac{1}{2C_6}\left(\frac{1}{R_1}-\frac{1}{R_2}\right)\right]}$	0	$\frac{1}{R_9}$	sC_{10}	$\frac{1}{sC_{10}R_9}$
8	$\frac{1}{R_1}$	$\frac{1}{R_2}$	0	0	$\frac{1}{R_5}$	sC_6	$\frac{1}{2C_6 R_5\left[s+\frac{1}{2C_6}\left(\frac{1}{R_1}-\frac{1}{R_2}\right)\right]}$	$\frac{1}{R_8}$	0	sC_{10}	$\frac{-1}{sC_{10}R_8}$
9	0	$\frac{1}{R_2}$	$\frac{1}{R_3}$	$\frac{1}{R_4}$	0	sC_6	$\frac{-1}{2C_6 R_3\left[s+\frac{1}{2C_6}\left(\frac{1}{R_4}-\frac{1}{R_2}\right)\right]}$	0	$\frac{1}{R_9}$	sC_{10}	$\frac{1}{sC_{10}R_9}$
10	0	$\frac{1}{R_2}$	0	$\frac{1}{R_4}$	$\frac{1}{R_5}$	sC_6	$\frac{1}{2C_6 R_5\left[s+\frac{1}{2C_6}\left(\frac{1}{R_4}-\frac{1}{R_2}\right)\right]}$	$\frac{1}{R_8}$	0	sC_{10}	$\frac{-1}{sC_{10}R_8}$
11	0	$\frac{1}{R_2}$	$\frac{1}{R_3}$	sC_4	0	$\frac{1}{R_6}$	$\frac{-1}{C_4 R_3\left[s+\frac{1}{C_4}\left(\frac{2}{R_6}-\frac{1}{R_2}\right)\right]}$	0	$\frac{1}{R_9}$	sC_{10}	$\frac{1}{sC_{10}R_9}$
12	0	$\frac{1}{R_2}$	0	sC_4	$\frac{1}{R_5}$	$\frac{1}{R_6}$	$\frac{1}{C_4 R_5\left[s+\frac{1}{C_4}\left(\frac{2}{R_6}-\frac{1}{R_2}\right)\right]}$	$\frac{1}{R_8}$	0	sC_{10}	$\frac{-1}{sC_{10}R_8}$

Table 5.1 Various LPF realising T1(s) and integrator T2(s), which yield the required QOs [4]

Here, as can be seen from Figure 5.5 and 5.6 Y1 through Y7 admittances are used to realize the transfer function $T_1(s) = (V_x/V_{in}) = K_1/(s + (a - b))$ whereas Y8 through Y10 admittances are used to derive the transfer function $T_2(s) = (V_o/V_x) = (K_2/s)$. Either of $T_1(s)$ or $T_2(s)$ is negative which the required condition to be satisfied for QOs is. The QOs circuits thus derived from the transfer function are shown in Figure 5.7.

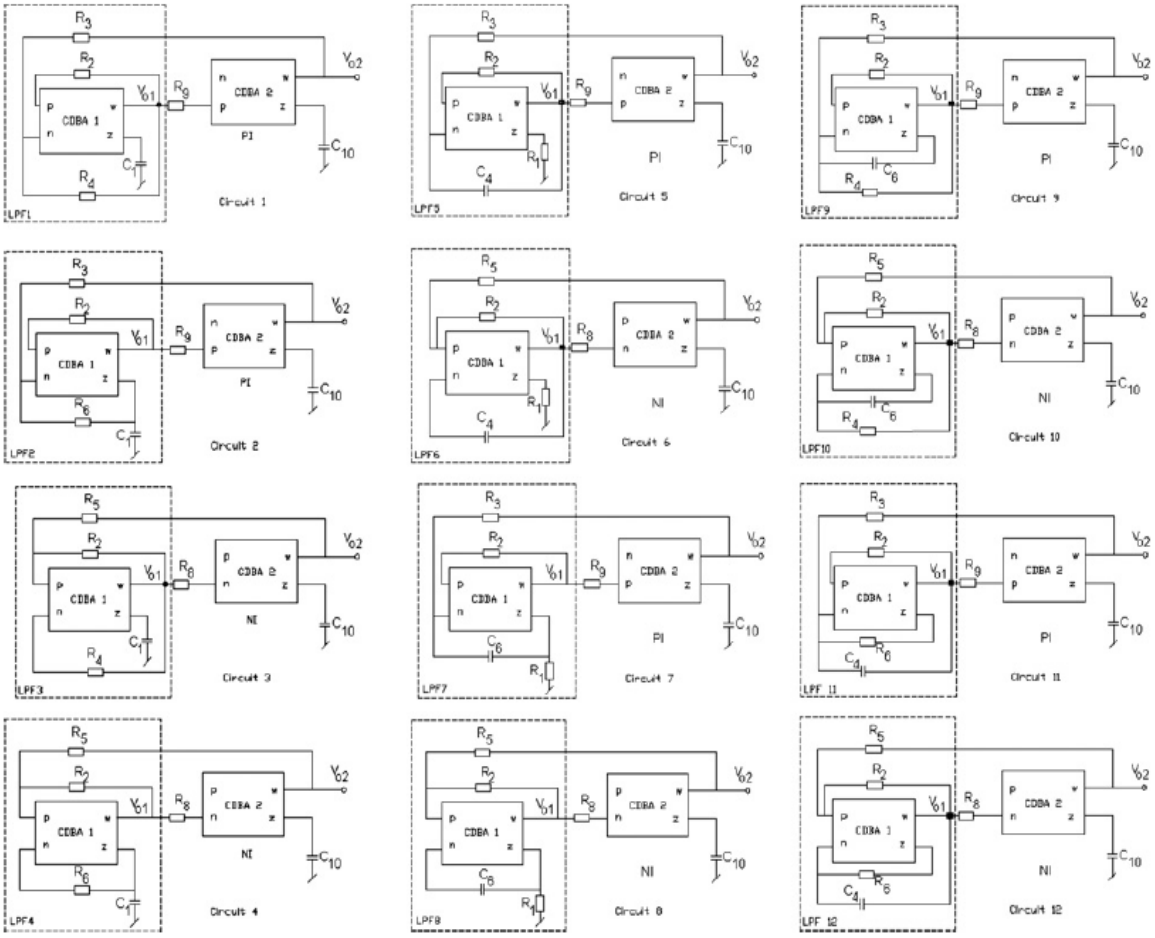

Fig. 5.7 Various CDBA-based QO circuits [4]

QO circuit	LPF	Integrator	CO[a=b]	FO$\left[\frac{\sqrt{K_1K_2}}{2\pi}\right]$
1	LPF1	NI	$R_2 = R_4$	$\frac{1}{2\pi\sqrt{C_1C_{10}R_3R_9}}$
2	LPF2	NI	$2R_2 = R_6$	$\frac{1}{2\pi\sqrt{C_1C_{10}R_3R_9}}$
3	LPF3	I	$R_2 = R_4$	$\frac{1}{2\pi\sqrt{C_1C_{10}R_5R_8}}$

4	LPF4	I	$2R_2 = R_6$	$\frac{1}{2\pi\sqrt{C_1C_{10}R_5R_8}}$
5	LPF5	NI	$R_2 = R_1$	$\frac{1}{2\pi\sqrt{C_4C_{10}R_3R_9}}$
6	LPF6	I	$R_2 = R_1$	$\frac{1}{2\pi\sqrt{C_4C_{10}R_5R_8}}$
7	LPF7	NI	$R_2 = R_1$	$\frac{1}{2\pi\sqrt{2C_6C_{10}R_3R_9}}$
8	LPF8	I	$R_2 = R_1$	$\frac{1}{2\pi\sqrt{2C_6C_{10}R_5R_8}}$
9	LPF9	NI	$R_2 = R_1$	$\frac{1}{2\pi\sqrt{2C_6C_{10}R_3R_9}}$
10	LPF10	I	$R_2 = R_1$	$\frac{1}{2\pi\sqrt{2C_6C_{10}R_5R_8}}$
11	LPF11	NI	$2R_2 = R_6$	$\frac{1}{2\pi\sqrt{C_4C_{10}R_3R_9}}$
12	LPF12	I	$2R_2 = R_6$	$\frac{1}{2\pi\sqrt{C_4C_{10}R_5R_8}}$

Note: NI-Non-inverting, I-inverting

Table 5.2: parameters of the various QO circuits [4]

Table 5.2 enlists various parameters of the circuits derived, it can be observed that CO and FO are respectively dependent on different set of resistors and can be set as needed independently of the other. This proves the uncoupled behaviour of the circuits thus derived, for e.g. QO circuit 1 has two resistances R2 and R4 appearing in the CO which do not appear in the FO and the rest of the two resistors namely R3 and R9 appear in the FO term. This fully uncoupled and independent control of CO and FO can be seen in all the other cases too.

The relationship between V01 and V02 as seen from configurations of Figure 5.7 can be expressed as:

$$\frac{V_{02}}{V_{01}} = \pm sC_{10}R_k \qquad (5.9)$$

Where,

For oscillators 3, 4, 6, 8, 10, 12 k = 8

For oscillators 1, 2, 5, 7, 9, 11 k = 9

This indicates that V01 and V02 are in quadrature phase i.e.in all the circuits thus derived the phase shift between V01 and V02 is equal to ±90˚.

5.3.2.1 PSPICE simulation results

All the derived CDBA based QO circuits are simulated using PSPICE to verify the theoretical results. The CDBA block is made out of commercially available AD844 IC's with supply voltages of ±12V and macro model of these IC's are used for PSPICE simulations. The component values chosen for circuit 1 are C1 = C10 = 100pF, R2 = 4KΩ, R4 = 5KΩ and R3 = R9 = 700Ω. And a simulated frequency was observed to be 2.01 MHz which was in accordance with theoretical calculations.

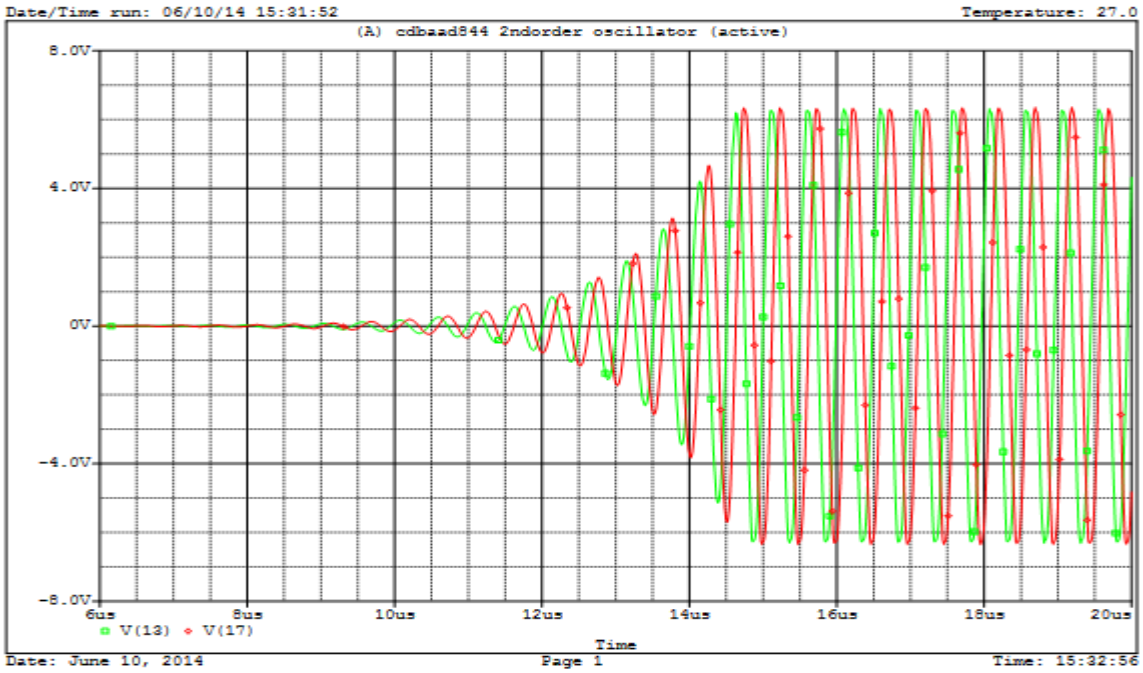

Fig. 5.8: Transient waveform for oscillator circuit 1

The output waveform for the oscillator derived from circuit 1 showing the build-up of oscillations is shown in Figure 5.5 and steady state output waveform is shown in Figure 5.6, which confirms the realization of QOs. Frequency spectrum of the outputs V01 and V02 is displayed in Figure 5.7 which shows that the circuit oscillates at 2.01 MHz, also for the two outputs the phase shift was found to be between 89.27˚ and 93.20˚.

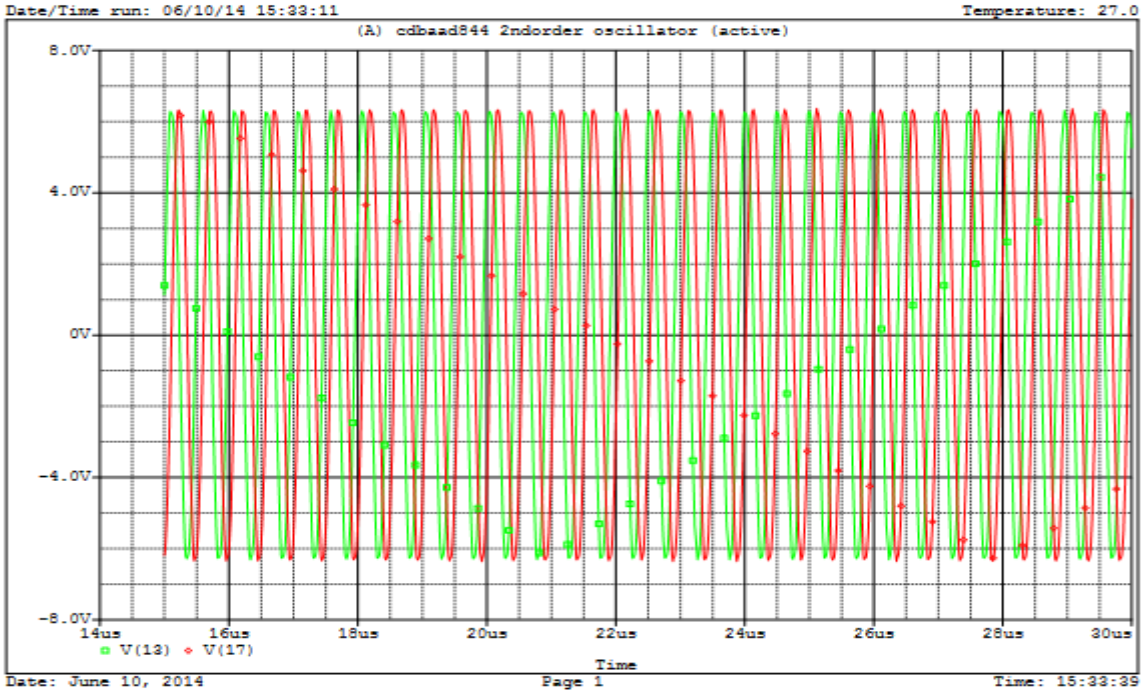

Fig. 5.9 Steady state waveform for oscillator circuit 1

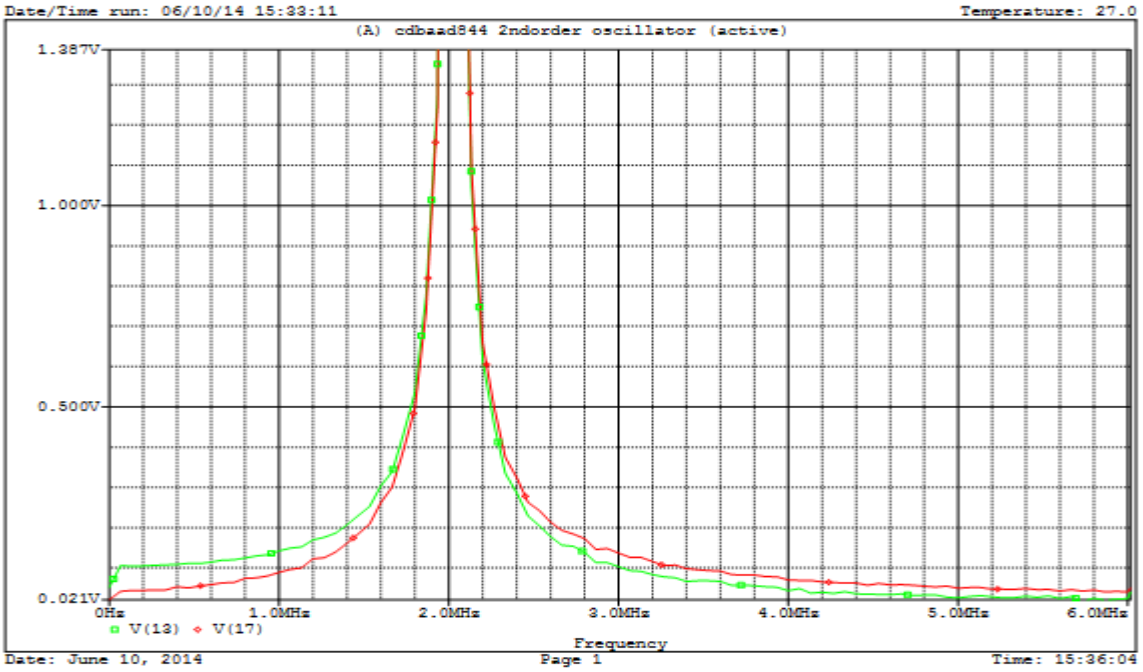

Fig. 5.10 Frequency spectrums for oscillator circuit 1

5.4 Multiphase sinusoidal Oscillator[5]

Multiphase sinusoidal oscillator (MSOs) is a type of oscillator circuit which is capable of producing multiple outputs i.e. multiple sinusoidal waves. These waves have some specific phase difference between them in time domain. MSO finds its extensive application in communication systems where they are used in SSB generators, quadrature

mixtures and phase modulators. Other areas of its usage include power electronics, measurement systems, signal processing [6-7] etc. In some literatures some works in MSOs has already been done based on operational amplifiers [6] and current conveyors [7]. From the research we found that bandwidth of all MSOs are less than 80 kHz.

Therefore a n-phase MSO circuit in [5] is discussed based on CDBA sub circuit blocks which are fit into predefined configurations discussed into various literatures [3,6-7] for realization of n-phase MSOs. PSPICE simulation results also discussed to verify working of MSO.

5.4.1 Approach to realize MSO Circuit

Fig 5.11 represents the circuit structure to analyse the MSO for n phase sinusoidal outputs. It consists of inverter based CDBA and cascade connection of the n lossy integrators. From Fig. 5.11, the voltage transfer function of the circuit between V_{on}, and V_{ox}, and V_{om} can be represented by:

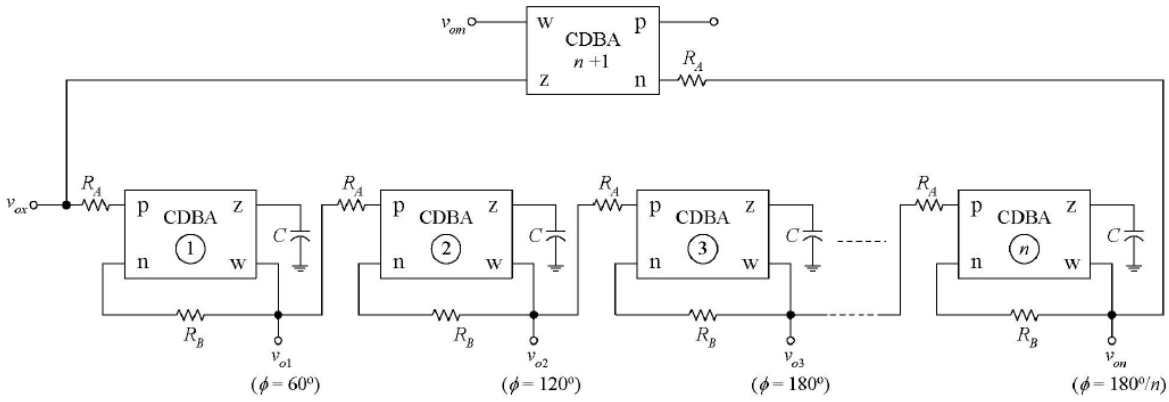

Fig. 5.11 Scheme for MSO [5]

$$\frac{Von}{Vox} = \left[\frac{K}{1+sT}\right]^n \tag{5.10}$$

And that of the inverter is assumed to be of the type,

$$\frac{Vom}{Von} = -1 \tag{5.11}$$

Where,

K= R_B/R_A represents the voltage gain of the lossy integrator based on CDBA, T = R_BC =$1/\omega_0$ and ω_0 is called internal-pole of the integrator. Therefore, if we substitute equation (5.10) into equation (5.11) mentioned above, the loop voltage gain (Vom/Vox) of the MSO circuit can be represented by:

$$\frac{Vom}{Vox} = -\left[\frac{K}{1+sT}\right]^n \tag{5.12}$$

At the oscillation frequency of $= \omega_0 = 2\pi f_o$, loop voltage gain(Vom/Vox) is adjusted to unity to fulfil the condition of oscillation. Equation (5.12) can then be represented as follows:

$$-\left[\frac{K}{1+sT}\right]^n = 1 \quad (5.13)$$

Or

$$(1+ST)^n + K^n = 0 \quad (5.14)$$

If we assume the value of real and imaginary terms in equation (5.14) to be zero then oscillation condition is satisfied for n ≥ 3. Shift of each Von in phase is 180°/n. For example let us assume n = 3, the real and imaginary terms of equation (5.14) can be represented by:

$$1 - 3(\omega oT)^3 + K^3 = 0 \quad (5.15)$$

And

$$3(j\omega oT) - j(\omega oT)^3 = 0 \quad (5.16)$$

In this case FO is,

$$f_o = \frac{\sqrt{3}}{2\pi CR\mathrm{B}} \quad (5.17)$$

where K= R_B/R_A = 2. It can be noticed that, for implementing the (n = 3) MSO i.e. it has 3 different phase shift sinusoidal output, the device should include seven virtually grounded resistors, three really grounded capacitors and four CDBAs. To satisfy the condition of oscillation there should be $R_B = 2R_A$

5.4.2 Simulation Using CDBA

MSO circuit design of Fig.6.14 has been analysed in PSPICE simulator. In this process CDBA was designed by 2 AD844 ICs as depicted in Figure 5.13. It is working at the power supply voltages of +5 V DC. Output waveforms have been obtained at the oscillation frequency, $f_o = \omega_0/2\pi$ = 26.76 kHz taking n = 3, the values of resistors and capacitors have been assumed as : R_A = 5 kΩ, R_B = 10.3 kΩ, C= 1 nF. To satisfy the condition of oscillation, the value of R_B = 10.3 kΩ is taken which is slightly greater than the ideal value of R_B = 10 kΩ for K= 2. Fig.6.16 represents the simulated output waveforms $Vo1$,$Vo2$, $Vo3$ and Vom of the presented MSO circuit of Fig.6.14. To analyse device, the frequency of oscillation f_o = 26 kHz has be calculated with error of 2.92% as compared to that obtained theoretically, and the phase shift of $Vo1$,$Vo2$ and $Vo3$ are

compared with Vom and obtained as: 60°, 121.4° and 180°, respectively. The simulation results are nearly equal to the theoretical design values.

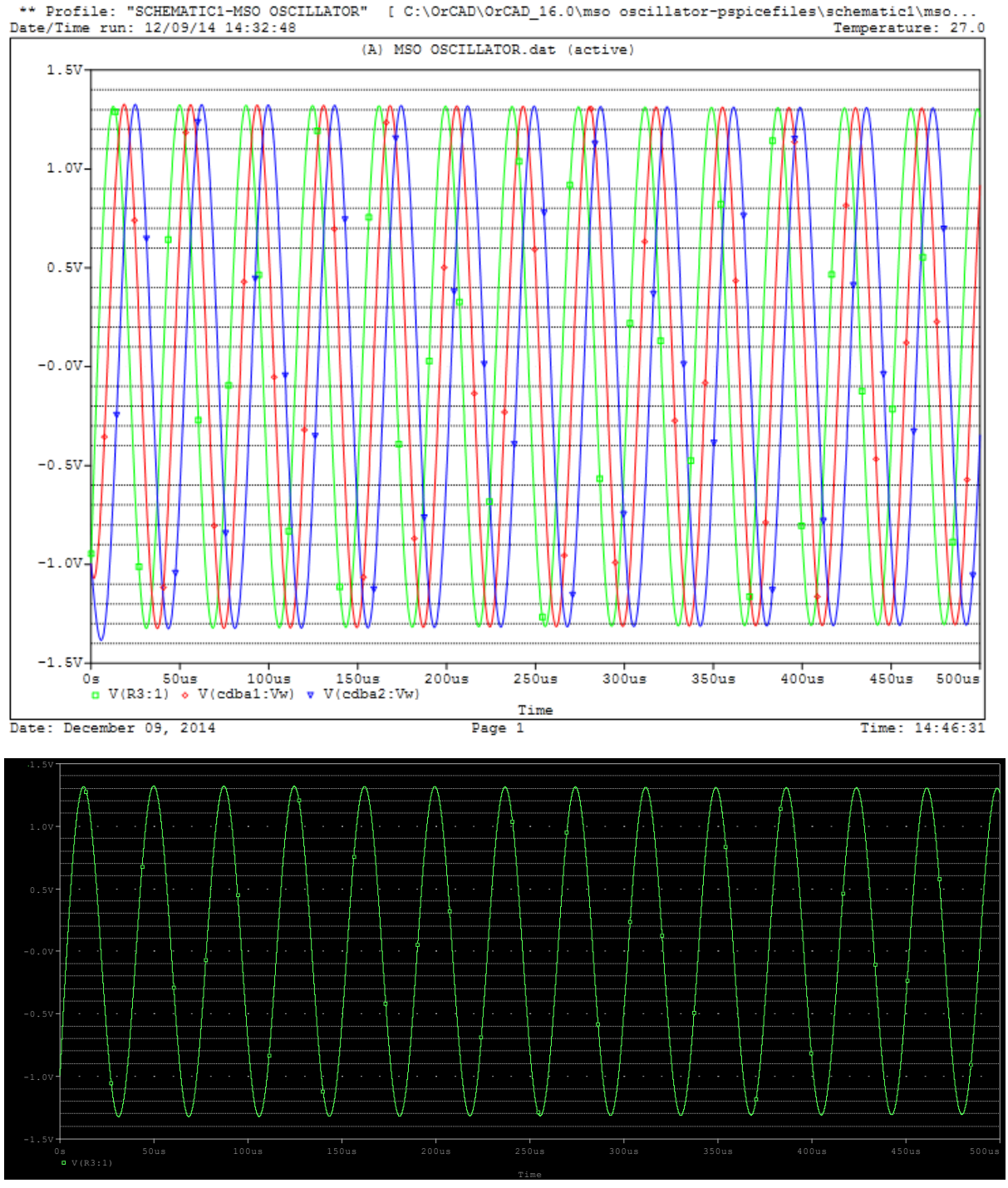

Fig. 5.12 Output waveforms for MSO

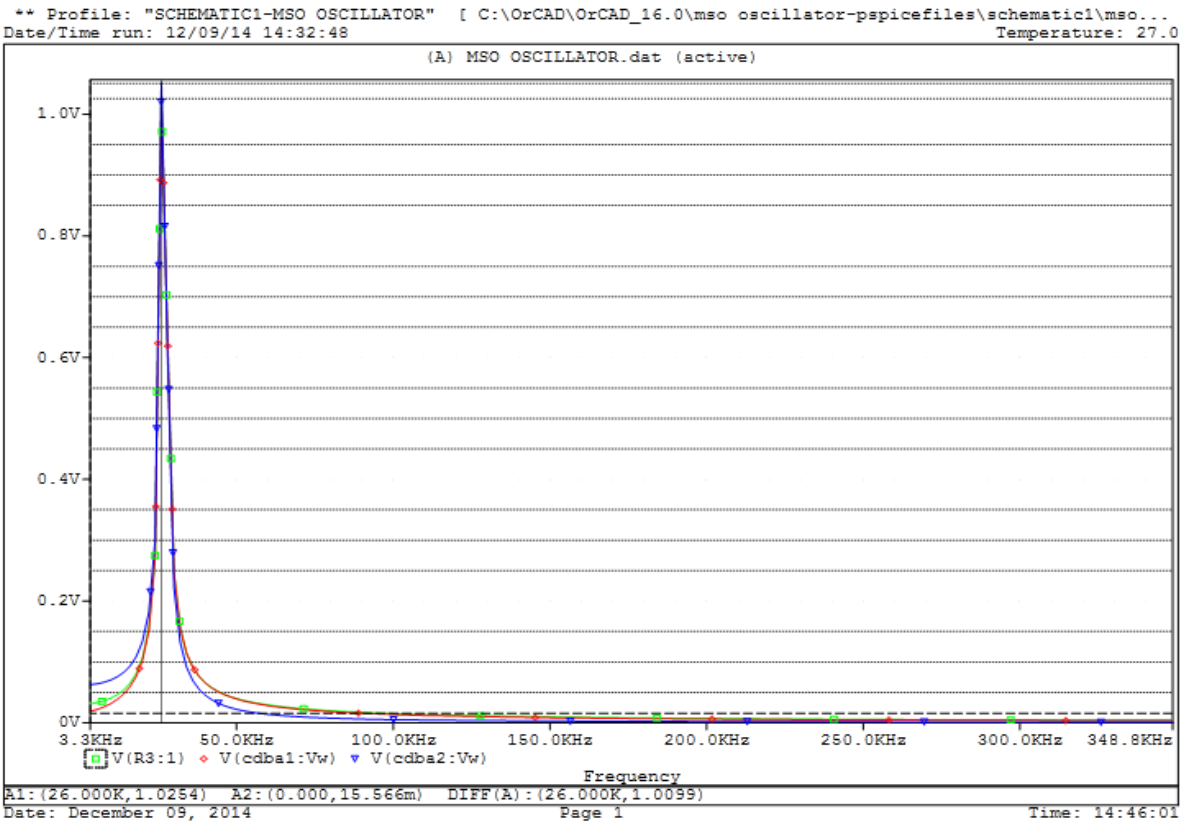

Fig. 5.13 Output spectrums for MSO

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CHAPTER 6 NEW PROPOSITIONS

6.1 New topologies of lossless grounded negative inductor using single CDBA:

Other than the positive inductance simulator circuit structures which are very important component in the circuit synthesis process mostly for analog signal processing devices like filters, analog phase shifters, chaotic oscillators and cancellation of parasitic capacitances, the negative inductance simulator circuits are also very useful components. It is observed that it is useful in numerous fields like designing of active filters, analog phase shifters and oscillators. It minimizes reflection at the input terminal of antenna (transmitter side), compensates bond wire inductance and cancels undesirable inductance**.**

There are various research papers published on the analysis of simulated inductance based on high performance active devices, for example operational transconductance amplifiers, current conveyors of second generation, current-feedback operational amplifiers, four terminal floating nullors, CDBA, DVCC, dual-X second generation current conveyors, fully differential second generation current conveyors etc. [1-20]. In [16] two active elements are used, first one is dual-output second-generation current-controlled current conveyor, and second one is operational amplifier. The circuit design of [17] consists of five passive elements and six current conveyors. 3 current conveyors (CCII+) and 2 external resistors are included in [18]. The circuit design of [19] comprises of three CDBAs and three MOS resistors. The circuit design of [20] represents a negative inductance simulator circuit.

In this work, two new types of lossless negative inductance simulator circuit topologies using single CDBA are proposed. The proposed topologies utilize some passive components. The first component is conditional and the second component is unconditional lossless negative inductor. At last, a second order sinusoidal oscillator circuit is constructed using the proposed lossless negative inductance simulator. Simulation results in PSPICE are compared with the theoretical values.

6.1.1 Topology 1

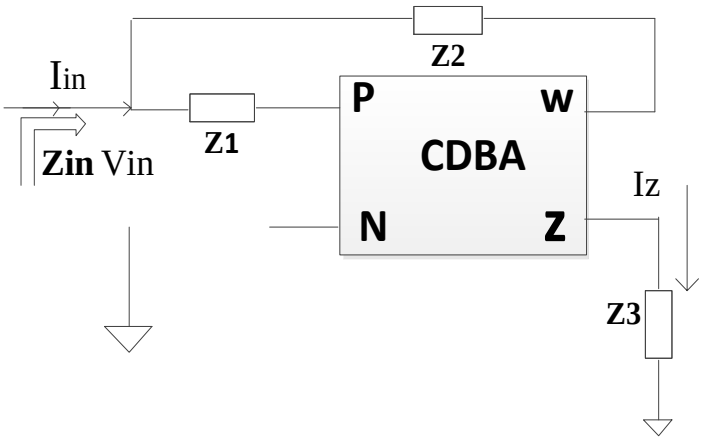

Fig 6.1: Proposed lossless negative inductor topology I

$$I_{in} + \frac{Vw - Vin}{Z2} = \frac{Vin}{Z1} = I_z \quad (6.1)\ (\text{as} I_z = I_p - I_n)$$

And $v_w = v_z = I_z z_3 = \frac{v_{in}}{z_1} z_3$ (6.2)

From equation 1 and 2

$$I_{in} + \frac{\frac{\text{Vin}}{\text{Z1}} Z3 - Vin}{Z2} = \frac{Vin}{Z1}$$

$$\Longrightarrow \quad I_{in} = v_{in}\left[\frac{1}{Z1} + \frac{1}{Z2} - \frac{Z3}{Z1Z2}\right]$$

$$\Longrightarrow \quad Z_{in} = \frac{v_{in}}{I_{in}} = \frac{Z1Z2}{Z1+Z2-Z3} \quad (6.3)$$

If $Z1 = R1$,

$$Z2 = R2,$$

And

$$\Longrightarrow \quad \text{Z3=R3 + (1/sc),}$$

Then

$$Z_{in} = \frac{v_{in}}{I_{in}} = \frac{R1R2}{R1 + R2 - R3 - \frac{1}{sc}}$$

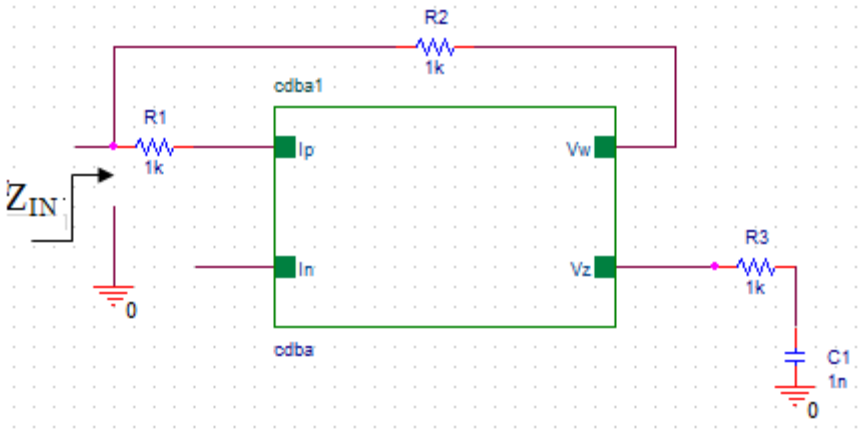

Fig. 6.2 negative inductor circuit using topology 1

If R1+R2=R3 (6.4)

$Zin = -\mathrm{R1R2}sC = -sL$ (6.5)

Where

L = $R1R2C$ is magnitude of the negative inductor

6.1.2 Topology 2

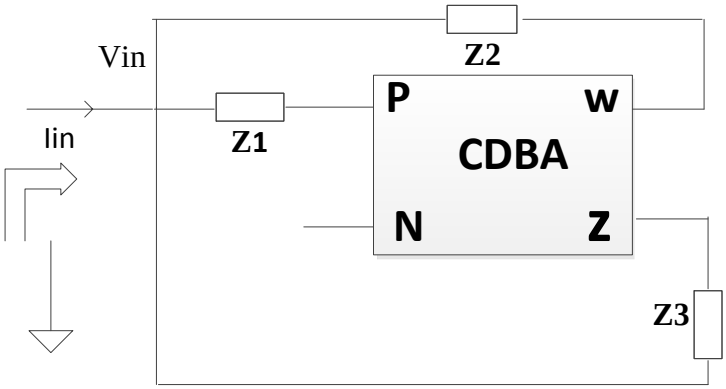

Fig. 6.3: Lossless negative inductor topology II

$$I_p = I_{in} + \frac{Vw-Vin}{Z2} + \frac{Vz-Vin}{Z3} = \frac{Vin}{Z1} = I_z \quad (6.6)$$

Also

$$I_z = \frac{Vz-Vin}{Z3} = \frac{Vin}{Z1} \quad (6.7)$$

And

$$Vz = Vw \quad (6.8)$$

From equations (6. 6), (6.7) and (6.8)

$$Zin = -\frac{Z1Z2}{Z3} \quad (6.9)$$

Taking $Z1 = R1, Z2 = R2, Z3 = \frac{1}{sC}$

$$Zin = -sCR1R2 = -sL \quad (6.10)$$

Where

L= $CR1R2$ (6.11)

6.1.3 simulations of proposed negative inductor

The CDBA is designed using the commercially available AD844/AD current feedback op-amp as shown in fig 3.3 and the circuit is supplied with symmetrical voltages of ±12V. Simulations are executed using the AD844 macro model supported by analog devices. Circuit for an inductance value of 10mH is shown in fig 6.4. The magnitude error found is within 10% (max) for inductive impedance from its ideal value for whole range of frequency taken and the phase is obtained from -93 to -87 degree is in the freq. range of 10 KHz to 80 KHz. The magnitude, transient and phase response are shown in fig. 6.5, 6.6, and 6.7 respectively.

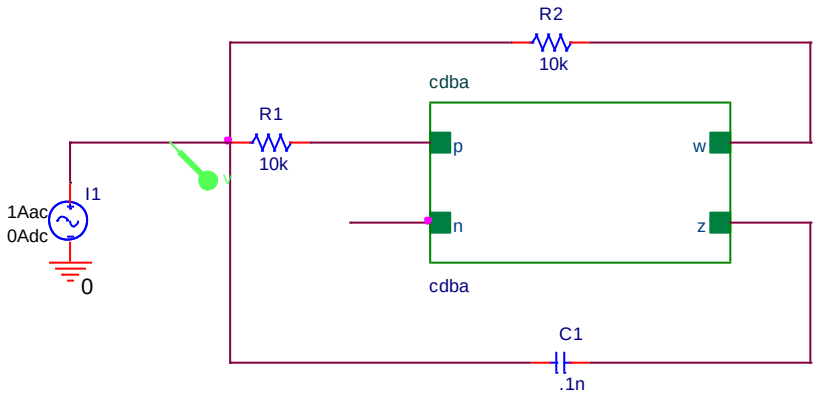

Fig 6.4 : circuit diagram of negative inductor for topology 2 using CDBA

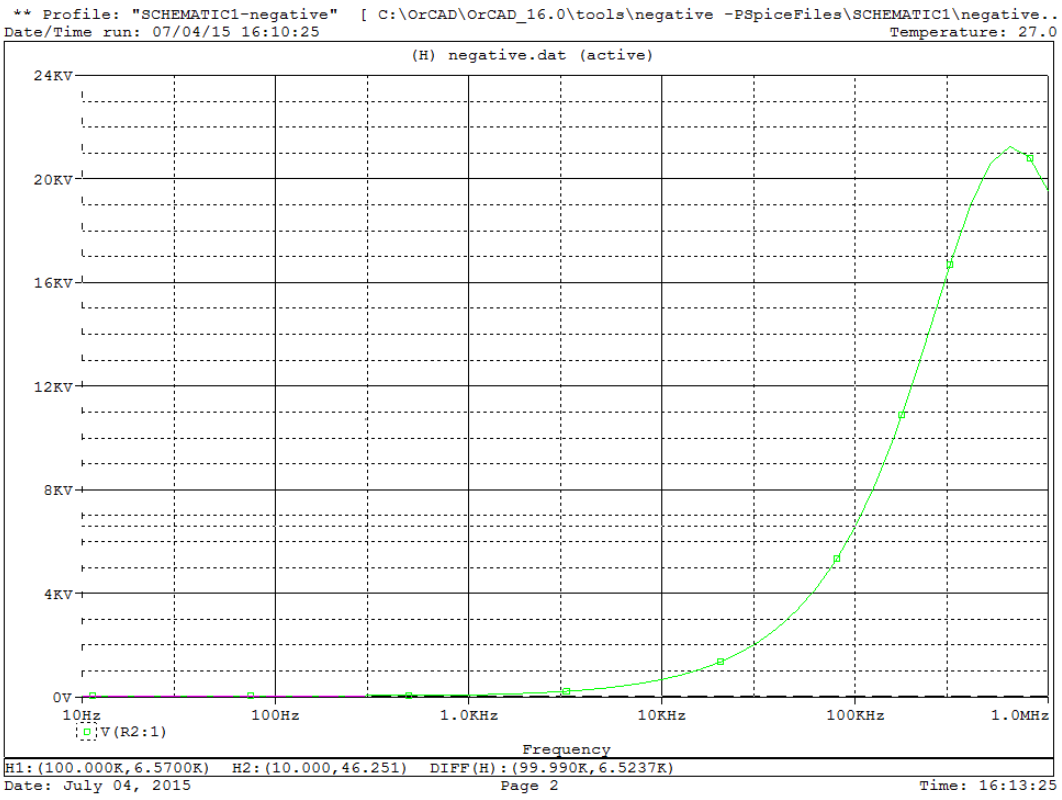

Fig. 6.5: Impedance versus frequency response of proposed negative inductor in kilo ohm = kilo volt

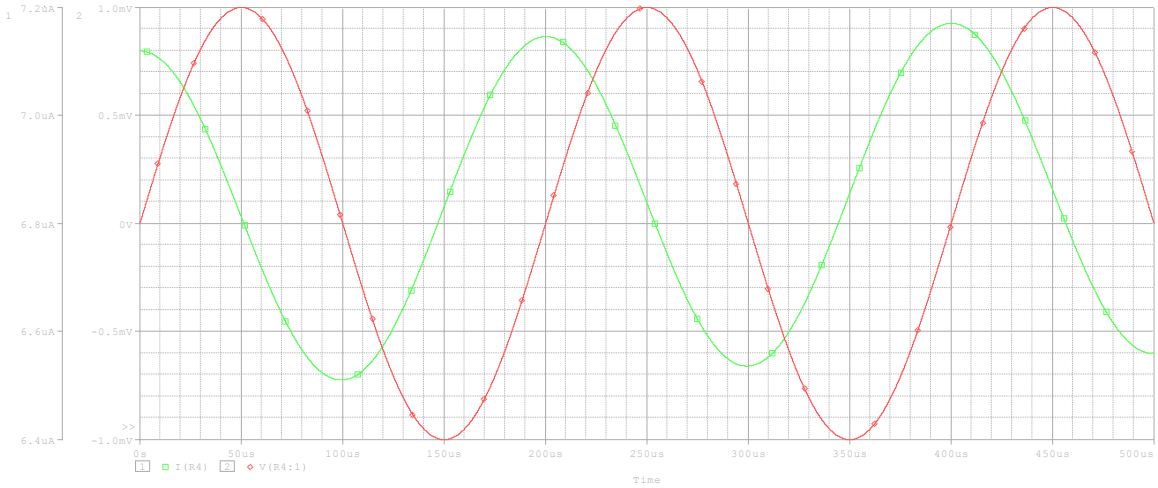

Fig. 6.6: Transient response for negative inductor for topology 2

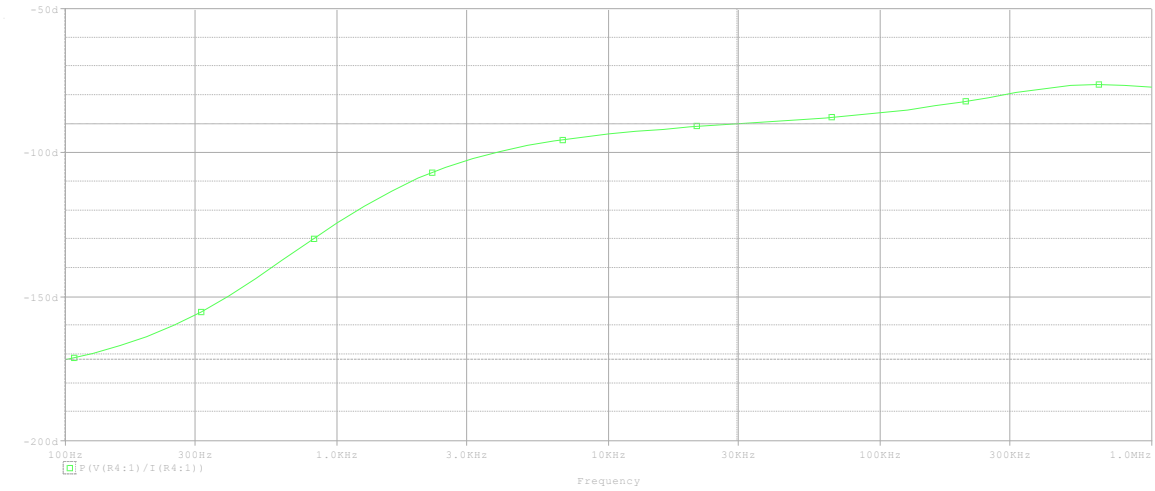

Fig. 6.7: phase response of negative inductor for topology 2

6.2 Application example of proposed negative inductor and simulations

6.2.1 Second Order Sinusoidal Oscillator using negative inductor

This section proposes a new configuration for the Sinusoidal oscillator circuit using proposed negative inductor. it doesn't have to satisfy any condition for the Barkhausen criteria [21], hence the name second order unconditional SO. The circuit is verified using Pspice simulations and the resulting output waveforms obtained are shown in sections to follow.

The importance of Sinusoidal oscillator was previously explained in section 5.1, also this configuration used for realizing SO has some added advantages which are:

(i) Number of passive components are employed are minimum which removes the need of matching of components.

(ii) High integrated circuit implementation capability, as the circuits have resistors and capacitors grounded/virtually grounded.

(iii) It doesn't have to satisfy any condition for the Barkhausen criteria.

6.2.1.1 Approach to realize SO Circuit using negative inductor

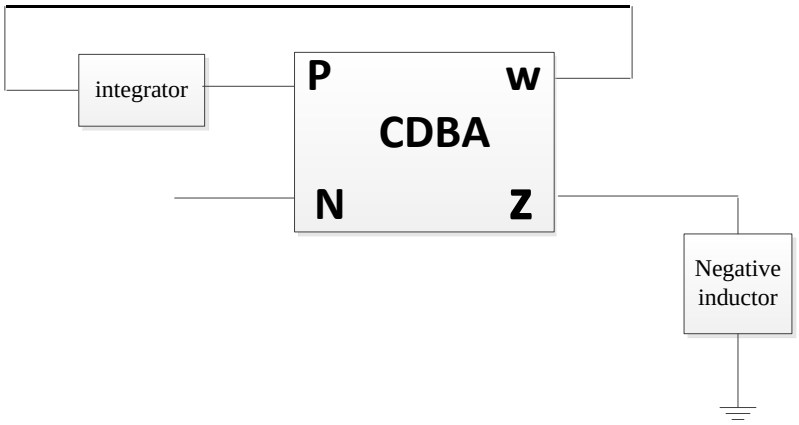

Fig. 6.8: Approach to realize SO Circuit using negative inductor

Here capacitor works as an integrator and negative inductor as an inverting differentiator. Then the current in the capacitor is of the type:

$$I_p = \frac{V_w}{X_C} = sCV_w \quad (6.12)$$

And

$$V_w = V_z = I_p X_{-L} = -sLI_p = -s^2CLV_w \quad (6.13) \quad \text{(from eq. 12)}$$

$$V_w = -s^2CLV_w$$

Hence the characteristics equation is

$$s^2CL+1=0 \quad (6.14)$$

Then FO is

$$\omega = 1/\sqrt{LC} \quad (6.15)$$

Where, $L = R_1R_2C_1$ If $R_1+R_2 = R_3$

Using the above equation it was found that the circuit is always oscillating and need not satisfy any condition for the oscillations to occur. The reason for this being the absence of the‘s’ term in the characteristic equation, hence the oscillator thus derived is called unconditional sinusoidal oscillator. The frequency of oscillation is given below.

$$f = \frac{1}{2\pi\sqrt{LC}}$$

FO: $f = \frac{1}{2\pi\sqrt{CC_1R_1R_2}}$ (Putting value of L)

If R1 =R2 =R then

FO: $f = \frac{1}{2\pi R\sqrt{CC_1}}$ (6.16)

6.2.1.2 Simulation results

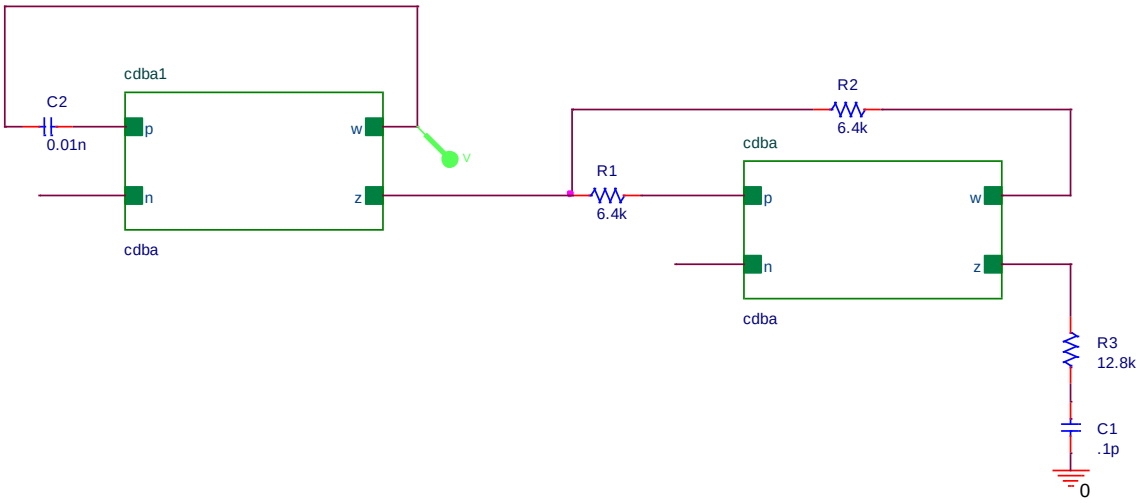

Fig. 6.9: Circuit for unconditional QO realization

Fig. 6.10: Output waveform of the unconditional QO circuit.

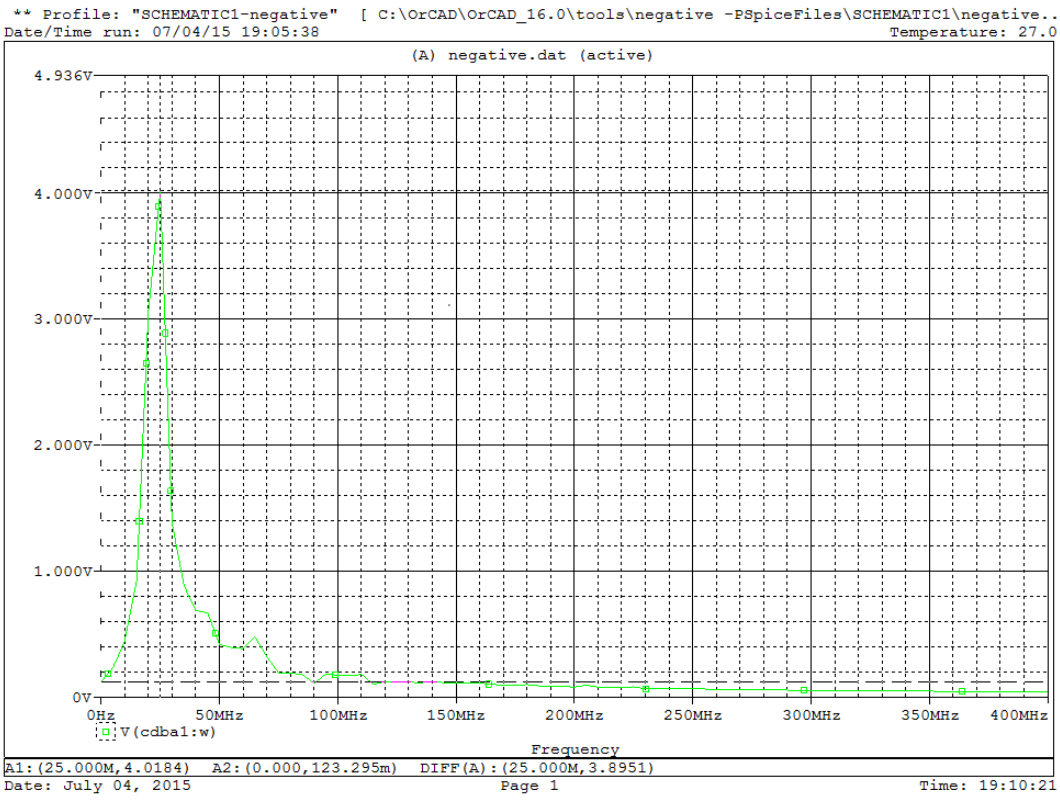

Fig. 6.11: frequency spectrum of circuit 6.12

TABLE.6.1 TOTAL HARMONIC DISTORTION FOR CIRCUIT 6.12

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE(DEG)
1	2.480E+07	5.407E+00	1.000E+00	-8.327E+01	0.000E+00
2	4.960E+07	1.430E-01	2.644E-02	-5.301E+01	1.135E+02
3	7.440E+07	4.229E-01	7.821E-02	9.864E+01	3.485E+02
4	9.920E+07	1.853E-02	3.426E-03	-1.210E+02	2.121E+02
5	1.240E+08	9.423E-02	1.743E-02	-1.191E+02	2.972E+02
6	1.488E+08	1.548E-02	2.862E-03	-6.771E+01	4.319E+02
7	1.736E+08	4.321E-02	7.992E-03	-4.032E+01	5.426E+02
8	1.984E+08	9.351E-03	1.729E-03	-5.758E+01	6.086E+02
9	2.232E+08	2.210E-02	4.087E-03	3.276E+01	7.822E+02

10	2.480E+08	6.238E-03	1.154E-03	-2.618E+01	8.065E+02
TOTAL HARMONIC DISTORTION = 8.499773E+00 PERCENT					

The circuit thus derived checked for its feasibility to obtain the desired oscillations For the Pspice circuit simulations of the circuit following component values was used:
C1 = .01nf, C2 = .1pf, R1 = R2 = 6.4 kΩ,
And a simulated frequency of 25 MHz was obtained with a percentage error of 0.53% as compared to that 24.86 MHz obtained theoretically. Frequency spectrum of the output V01 and is displayed in figure 6.11 which shows that the circuit oscillates at 25MHz and Total harmonic distortion obtained is 8.49% which is within acceptable limit.

6.3 new topologies of second order sinusoidal oscillator using single CDBA

The Sinusoidal oscillators have a wide range of applications in many electronic circuits such as communication, control-systems; signal processing, instrumentation and measurement. A variety of sinusoidal oscillators have been proposed using op-amp as an active element in the literature [22]. But the limitations in op-amp are due to slew rate and fixed gain bandwidth product that affect the condition of oscillation, frequency of oscillation and also that it does not operate at high frequencies [22- 24]. To overcome these drawbacks, several oscillators based on current conveyor (CCII) and current-feedback operational amplifier (CFOA) as an active element have been proposed in the literature [25-33]. These oscillators draw considerable attention due to their large frequency range, large dynamic range and wider bandwidth. In addition to these active devices, several other building blocks such as OTAs, CCCIIs, FTFNs, DDCC, DO-OTAs and CDBA [34-42] have also shot into prominence due to their advantages over voltage-mode op-amp based oscillators. However, most of the oscillators designed with the above active elements require more than one active element amongst them to control the frequency of oscillation with a grounded resistor or a capacitor [29-36]. More than one active element consumes more power and requires more chip area to fabricate IC.

This section represents two new configurations for the sinusoidal oscillator circuits based on CDBA. The proposed circuits require single CDBA and few passive

components to generate oscillations. The circuit is verified using Pspice simulations and the resulting output waveforms obtained are shown in sections to follow.

The importance of sinusoidal oscillator was previously explained in section 5.1, also this configuration used for realizing SO has some added advantages which are:

(i) Number of passive components are employed are minimum which removes the need of matching of components.

(ii) High integrated circuit implementation capability, as the circuits have resistors and capacitors grounded/virtually grounded.

(iii) Use only single CDBA block due to this it requires less chip area.

6.3.1 Approach to realize sinusoidal oscillator Circuit using single CDBA:

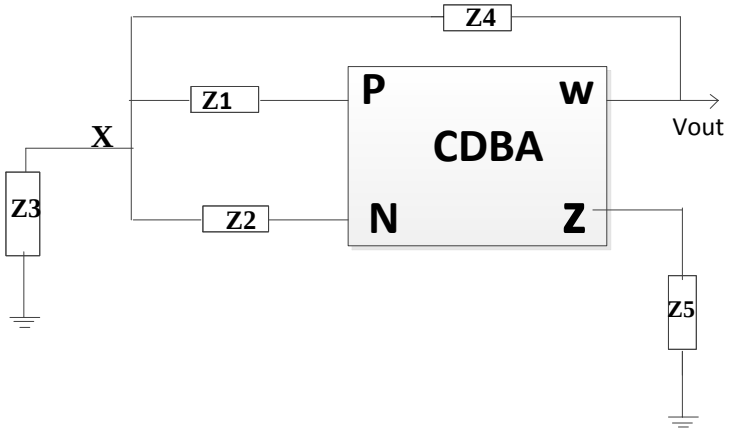

Fig. 6.12: Approach to realize sinusoidal oscillator Circuit using single CDBA

The characteristic equation of the circuit in Fig. 6.12 can be written by

$V_w = V_z = I_z Z_5$ (6.17)

And

$I_z = I_p - I_n$ (6.18)

$I_z = V_x \left(\frac{1}{Z_1} - \frac{1}{Z_2}\right)$ (6.19)

Now applying KCL at V_x

$\frac{V_i}{Z_3} + \frac{V_i}{Z_1} + \frac{V_i}{Z_2} + \frac{V_i - V_z}{Z_3} = 0$ (6.20)

Now solving equation 6.17, 6.18, 6.19, and 6.20 and then obtained characteristics eq. can be written as:

$Z_1 Z_2 Z_3 + Z_1 Z_3 Z_4 + Z_2 Z_3 Z_4 + Z_1 Z_2 Z_4 + Z_1 Z_3 Z_5 - Z_2 Z_3 Z_5$ (6.21)

Now to oscillate the circuit out of there must be two capacitive and three resistive components. In which for condition of oscillation any one of ($Z_2 or Z_3 or Z_5$) and (Z_1 or Z_4) must be capacitive components and remaining will be resistive components.

From the above conditions there will be two configurations of oscillator circuits as follow:

1) Z_1 and Z_5
2) Z_2 and Z_4 And remaining all are resistive components in both the cases.

To verify the proposed circuits taking topology 1 into consideration of above given:

$$Z_1 = \frac{1}{sC_1}, Z_2 = R_2, Z_3 = R_3, Z_4 = R_4, Z_5 = \frac{1}{sC_5}$$

Putting these values in eq. 6.21 and taking $s = j\omega$, the characteristics eq. is given as:

$$j\omega(C_5R_2R_3 + C_5R_4R_3 + C_5R_2R_4 - C_1R_2R_3) - C_5R_2R_3C_1R_5\omega^2 + R_3 = 0$$

Equating real and imaginary part equal to zero

$$CO: C_5R_2R_3 + C_5R_4R_3 + C_5R_2R_4 = C_1R_2R_3 \quad (6.22)$$

$$FO: \quad f = \frac{1}{2\pi\sqrt{C_5C_1R_4R_2}} \quad (6.23)$$

If $R_2 = R_4 = R_3 = R$

Then $C_5 + C_5 + C_5 = C_1$

$$CO: \ 3C_5 = C_1 \quad (6.24)$$

$$FO: \ f = \frac{1}{2\pi C_5 R\sqrt{3}} \quad (6.25)$$

The FO can be adjusted to desired value through R or proper selection of resistor R_2, R_3, R_4 and C_1, C_5 would satisfy the CO.

6.3.2 Simulation results:

The proposed SO is verified through simulations using the commercially available AD844 IC implementation of the CDBA which is shown in [2] in chapter 3. Supply voltages taken are ±8V.

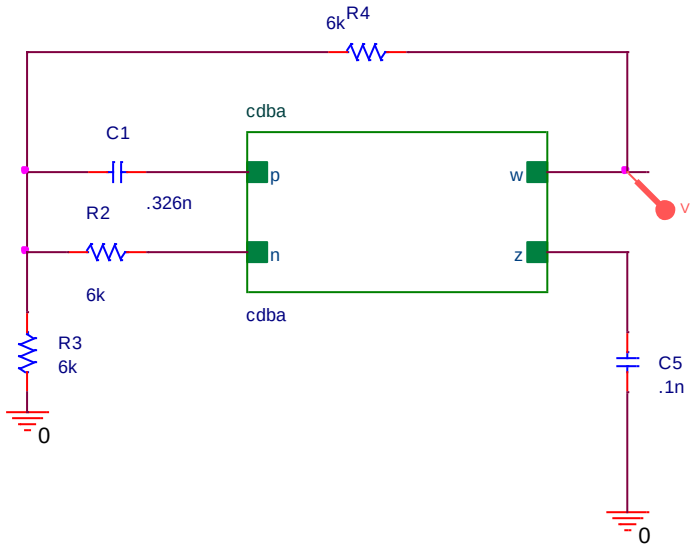

Fig 6.13: Configuration 1 to realize sinusoidal oscillator Circuit using single CDBA

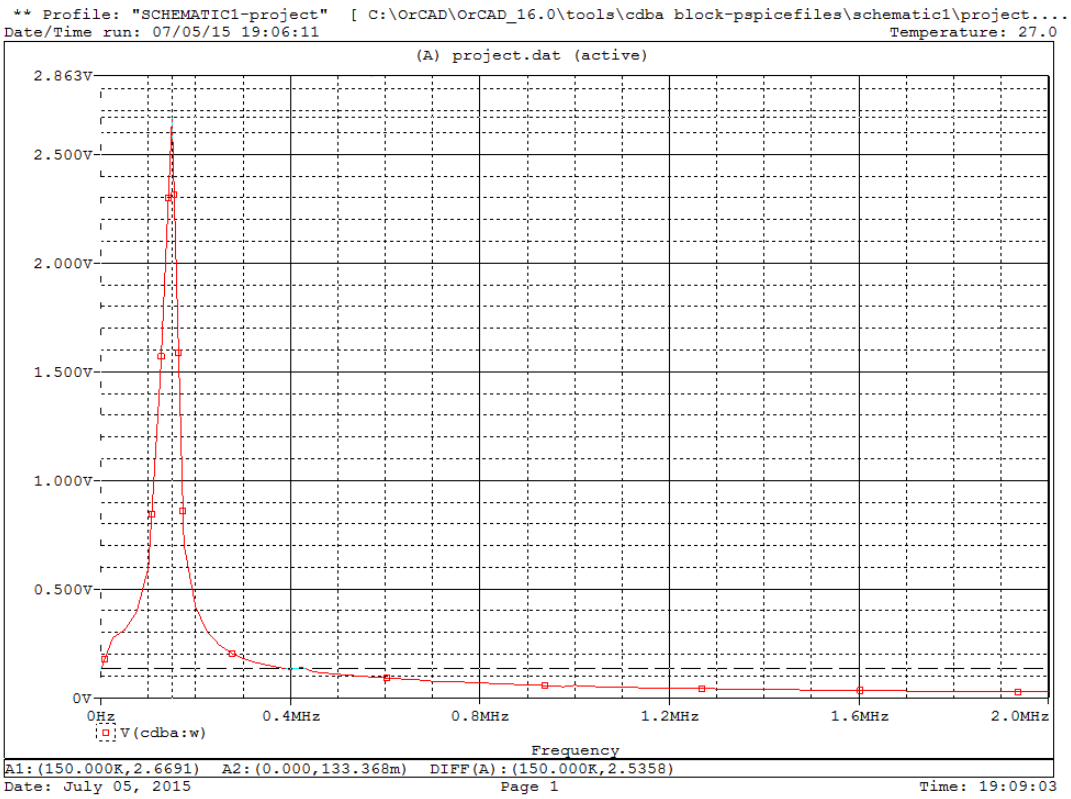

Fig. 6.14 frequency spectrum of circuit 6.16

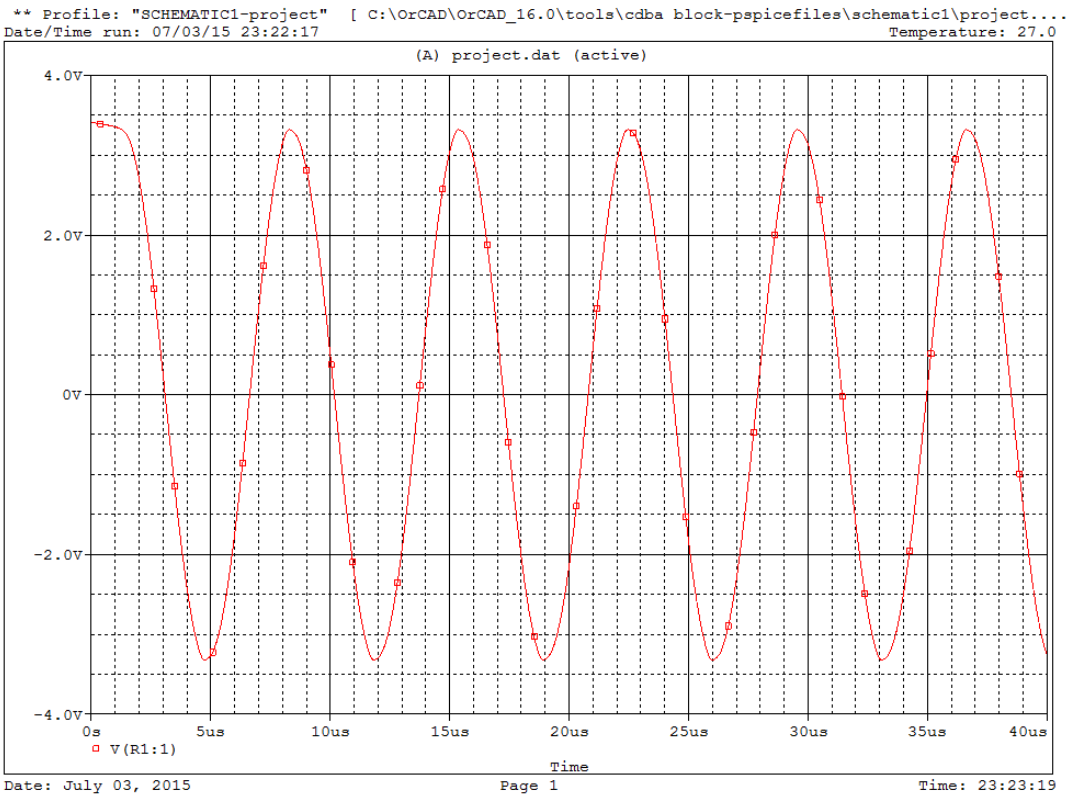

Fig. 6.15: transient response of circuit 6.16

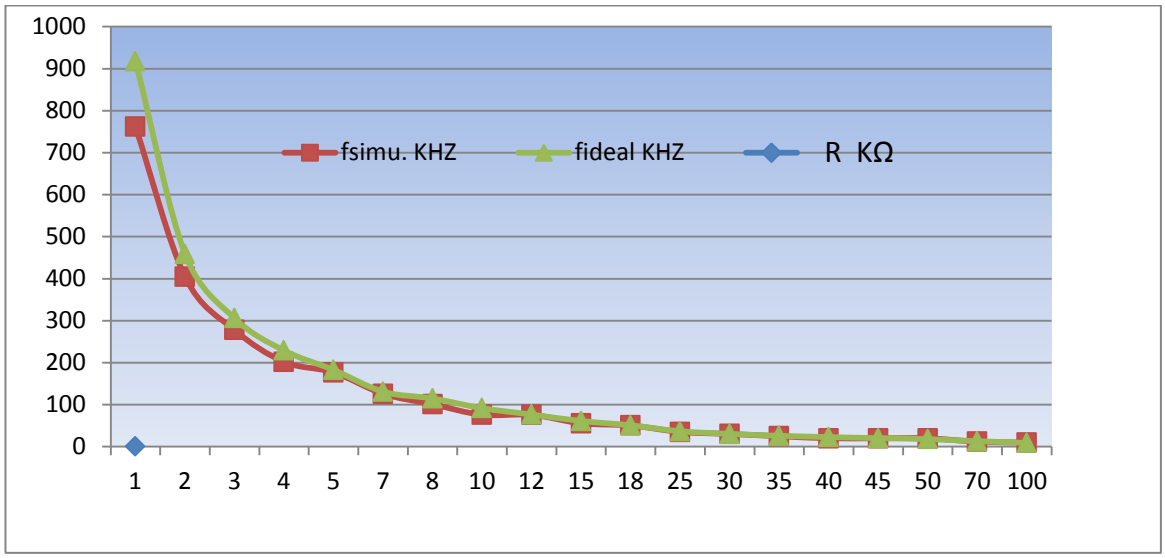

Fig. 6.16: freq. v/s R response of circuit 6.16 for C_5=0.1nf

TABLE.6.2 TOTAL HARMONIC DISTORTION FOR CIRCUIT 6.17

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE(DEG)

1	1.530E+05	3.147E+00	1.000E+00	-9.022E+01	0.000E+00
2	3.060E+05	1.468E-01	4.665E-02	-9.272E+01	8.772E+01
3	4.590E+05	6.521E-02	2.072E-02	-7.508E+01	1.956E+02
4	6.120E+05	3.220E-02	1.023E-02	-9.308E+01	2.678E+02
5	7.650E+05	2.192E-02	6.964E-03	-6.711E+01	3.840E+02
6	9.180E+05	1.465E-02	4.656E-03	-9.188E+01	4.494E+02
7	1.071E+06	1.097E-02	3.487E-03	-5.959E+01	5.720E+02
8	1.224E+06	8.729E-03	2.774E-03	-8.920E+01	6.326E+02
9	1.377E+06	6.503E-03	2.066E-03	-5.395E+01	7.580E+02
10	1.530E+06	5.931E-03	1.884E-03	-8.512E+01	8.171E+02
TOTAL HARMONIC DISTORTION = 5.298958E+00 PERCENT					

The circuit thus derived checked for its feasibility to obtain the desired oscillations For the Pspice circuit simulations of the circuit following component values are used:

C_1 = .326nf, C_5 = .1nf, R_2 = R_3 = R_4 =6 KΩ, C_1 is taken as slightly greater than $3C_5$ because of onset of nonlinearity produced in circuit and a simulated frequency of 150 KHz was obtained with a percentage error of 1.96% as compared to that 153 KHz obtained theoretically. The corresponding simulated frequency spectrum and transient output for topology 1 are shown in Fig. 6.14 and Fig. 6.15 respectively. The percentage total harmonic distortion (THD) is 5.29% for SO Circuit I. This is within acceptable limit. Variation of frequency with respect to R in equation 6.25 of section 6.3.1, also shown in fig 6.16 which show that obtained simulated frequencies are almost equal to ideal freq graph.

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CHAPTER 7 CONCLUSION

In this work ways to realize CDBA (a mixed mode active block) are studied. The block designed performed satisfactorily for both the realizations (AD844 IC and LVLP). Systematic approaches to synthesize three new circuits, which are lossless negative inductors, SO using proposed lossless negative inductor and sinusoidal oscillator using single CDBA, are presented. These approaches are used to yield the respective circuits using CDBA. The proposed circuits are verified for their working using PSPICE simulations, the error percentage and THD found in the frequency of oscillations were within 0.53% and 8.49% for section 6.2.2.2 and for section 6.3.2 were ±1.96% and 5.29% respectively. It is concluded that the results are approximately same as the theoretical propositioned and THD are also in acceptable limit.

The CDBA was implemented using the available AD844N IC (from Analog Devices Inc.). CDBA is not yet available commercially, AD844N was the only choice as CFOAs such as CLC-400/401 manufactured by National Semiconductors and MAX 4223-4228 manufactured by MAX Corporation does not have z-terminal as an accessible pin controlled externally which is very important for the implementation of CDBA using CFOA's. This can be taken as one of the limitations of the proposed circuits for the current being, as soon as the CDBA becomes available in the market (commercially) as an efficient microelectronic device it can be directly applied for the implementation of all the above proposed circuits and the required results can be obtained.

APPENDIX (A)

AD844 IC - 60 MHz, 2000 V/µs, Monolithic Op Amp

The AD844 is a high speed monolithic operational amplifier fabricated using Analog Device's junction isolated complementary bipolar (CB) process. It combines high bandwidth and very fast large signal response with excellent dc performance. Although optimized for use in current-to-voltage applications and as an inverting mode amplifier, it is also suitable for use in many non-inverting applications.

The AD844 can be used in place of traditional op amps, but its current feedback architecture results in much better ac performance, high linearity, and an exceptionally clean pulse response.

This type of op amp provides a closed-loop bandwidth that is determined primarily by the feedback resistor and is almost independent of the closed-loop gain. The AD844 is free from the slew rate limitations inherent in traditional op amps and other current-feedback op amps. Peak output rate of change can be over 2000 V/µs for a full 20 V output step. Settling time is typically 100 ns to 0.1%, and essentially independent of gain. The AD844 can drive 50 Ω loads to ±2.5 V with low distortion and is short circuit protected to 80 mA.

The AD844 is available in four performance grades and three package options. In the 16-lead SOIC (R) package, the AD844J is specified for the commercial temperature range of 0°C to 70°C.The AD844A and AD844B are specified for the industrial temperature range of –40°C to +85°C and are available in the CERDIP (Q) package. The AD844A is also available in an 8-lead PDIP (N). The AD844S is specified over the military temperature range of –55°C to +125°C. It is available in the 8-lead CERDIP (Q) package.

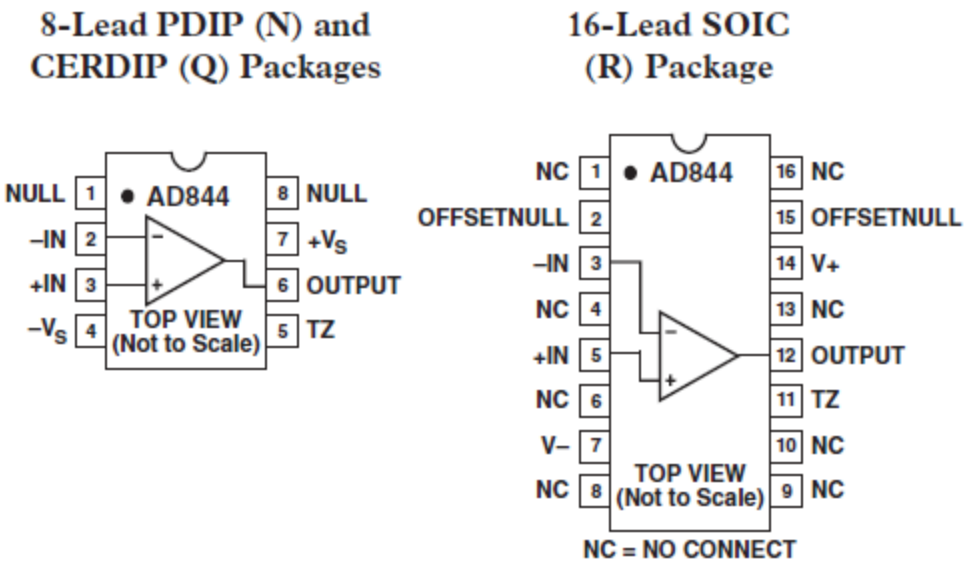

Fig. A Connection diagram [43] (ref given in chapter 6)

PRODUCT HIGHLIGHTS:

1. The AD844 is a versatile, low cost component providing an excellent combination of ac and dc performance.
2. It is essentially free from slew rate limitations. Rise and fall times are essentially independent of output level.
3. The AD844 can be operated from ±4.5 V to ±18 V power supplies and is capable of driving loads down to 50 Ω, as well as driving very large capacitive loads using an external network.
4. The offset voltage and input bias currents of the AD844 is laser trimmed to minimize dc errors; VOS drift is typically 1 μV/°C and bias current drift is typically equal to 9nA/°C.
5. The AD844 exhibits excellent differential gain and differential phase characteristics, making it suitable for a variety of video applications with bandwidths up to 60 MHz.
6. The AD844 combines low distortion, low noise, and low drift with wide bandwidth, making it outstanding as an input amplifier for flash A/D converters.

FEATURES:

Wide Bandwidth: 60 MHz at Gain of –1

Wide Bandwidth: 33 MHz at Gain of –10

Very High Output Slew Rate: Up to 2000 V/μs

20 MHz Full Power Bandwidth, 20 V p-p, R_L = 500Ω

Fast Settling: 100 ns to 0.1% (10 V Step)
Differential Gain Error: 0.03% at 4.4 MHz
Differential Phase Error: 0.158 at 4.4 MHz
Low Offset Voltage: 150 mV Max (B Grade)
Low Quiescent Current: 6.5 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ABSOLUTE MAXIMUM RATINGS:

Supply Voltage: ±18 V
Power Dissipation: 1.1 W for
8-Lead PDIP Package at θ_{JA} = 90°C/W.
8-Lead CERDIP Package at θ_{JA} = 110°C/W.
Output Short Circuit Duration: Indefinite
Common-Mode Input Voltage: ±VS
Differential Input Voltage: 6 V
Inverting Input Current
Continuous: 5 m Amp
Transient: 10 m Amp
Storage Temperature Range (Q): –65°C to +150°C
Storage Temperature Range (N, R): –65°C to +125°C
Lead Temperature Range (Soldering 60 sec): 300°C
ESD Rating: 1000 V

APPLICATIONS:

Flash ADC Input Amplifiers
High Speed Current DAC Interfaces
Video Buffers and Cable Drivers
Pulse Amplifiers

APPENDIX (B)

0.18 µm, level 7 parameters provided by TSMC for NMOS

```
LEVEL   = 7

+DSUB    = 0.0217897     + TNOM    = 27            TOX     = 4.1E-9
+XJ      = 1E-7                  NCH     = 2.3549E17       VTH0    = 0.3750766
+K1      = 0.5842025       K2      = 1.245202E-3     K3      = 1E-3
+K3B     = 0.0295587       W0      = 1E-7                  NLX     = 1.597846E-7
+DVT0W   = 0               DVT1W   = 0               DVT2W   = 0
+DVT0    = 1.3022984       DVT1    = 0.4021873       DVT2    = 7.631374E-3
+U0      = 296.8451012     UA      = -1.179955E-9    UB      = 2.32616E-18
+UC      = 7.593301E-11    VSAT    = 1.747147E5      A0      = 2
+AGS     = 0.452647        B0      = 5.506962E-8     B1      = 2.640458E-6
+KETA    = -6.860244E-3            A1      = 7.885522E-4     A2      = 0.3119338
+RDSW    = 105             PRWG    = 0.4826          PRWB    = -0.2
+WR      = 1                     WINT    = 4.410779E-9     LINT    = 2.045919E-8
+XL      = 0                     XW      = -1E-8                 DWG     = -2.610453E-9
+DWB     = -4.344942E-9          VOFF    = -0.0948017      NFACTOR = 2.1860065
+CIT     = 0                     CDSC    = 2.4E-4          CDSCD   = 0
+CDSCB   = 0               ETA0    = 1.991317E-3     ETAB    = 6.028975E-5
+DSUB    = 0.0217897       PCLM    = 1.7062594       PDIBLC1 = 0.2320546
+PDIBLC2 = 1.670588E-3           PDIBLCB = -0.1            DROUT   = 0.8388608
+PSCBE1  = 1.904263E10           PSCBE2  = 1.546939E-8           PVAG    = 0
+DELTA   = 0.01            RSH     = 7.1                   MOBMOD  = 1
+PRT     = 0                     UTE     = -1.5                  KT1     = -0.11
+KT1L    = 0                     KT2     = 0.022                 UA1     = 4.31E-9
+UB1     = -7.61E-18       UC1     = -5.6E-11                AT      = 3.3E4
+WL      = 0                     WLN     = 1                     WW      = 0
+WWN     = 1               WWL     = 0                     LL      = 0
+LLN     = 1                     LW      = 0                     LWN     = 1
+LWL     = 0                     CAPMOD  = 2               XPART   = 0.5
+CGDO    = 6.7E-10         CGSO    = 6.7E-10         CGBO    = 1E-12
+CJ      = 9.550345E-4     PB      = 0.8                   MJ      = 0.3762949
+CJSW    = 2.083251E-10            PBSW    = 0.8                   MJSW    = 0.1269477
+CJSWG   = 3.3E-10         PBSWG   = 0.8             MJSWG   = 0.1269477
+CF      = 0                     PVTH0   = -2.369258E-3            PRDSW   = -1.2091688
+PK2     = 1.845281E-3     WKETA   = -2.040084E-3            LKETA   = -1.266704E-3
+PU0     = 1.0932981       PUA     = -2.56934E-11    PUB     = 0
+PVSAT   = 2E3             PETA0   = 1E-4            PKETA   = -3.350276E-3    )
```

0.18 µm, level 7 parameters provided by TSMC for PMOS

```
  LEVEL   = 7

+ TNOM    = 27            TOX     = 4.1E-9
+XJ   = 1E-7                      NCH     = 4.1589E17             VTH0    = -0.3936726
+K1   = 0.5750728                 K2      = 0.0235926             K3      = 0.1590089
+K3B= 4.2687016                   W0      = 1E-6                  NLX     = 1.033999E-7
+DVT0W   = 0             DVT1W   = 0                     DVT2W   = 0
+DVT0 = 0.5560978                 DVT1    = 0.2490116             DVT2    = 0.1
+U0= 112.5106786                  UA      = 1.45072E-9    UB      = 1.195045E-21
+UC      = -1E-10        VSAT    = 1.168535E5    A0      = 1.7211984
+AGS     = 0.3806925     B0      = 4.296252E-7   B1      = 1.288698E-6
+KETA    = 0.0201833     A1      = 0.2328472     A2      = 0.3
+RDSW    = 198.7483291           PRWG    = 0.5                   PRWB    = -0.4971827
+WR      = 1                     WINT    = 0                     LINT    = 2.943206E-8
+XL      = 0                     XW      = -1E-8                 DWG     = -1.949253E-8
+DWB     = -2.824041E-9          VOFF    = -0.0979832    NFACTOR = 1.9624066
+CIT     = 0                     CDSC    = 2.4E-4        CDSCD   = 0
+CDSCB   = 0             ETA0    = 7.282772E-4   ETAB    = -3.818572E-4
+DSUB    = 1.518344E-3           PCLM    = 1.4728931     PDIBLC1 = 2.138043E-3
+PDIBLC2 = -9.966066E-6  PDIBLCB = -1E-3                 DROUT   = 4.276128E-4
+PSCBE1  = 4.850167E10           PSCBE2  = 5E-10         PVAG    = 0
+DELTA   = 0.01          RSH     = 8.2                   MOBMOD  = 1
+PRT     = 0                     UTE     = -1.5                  KT1     = -0.11
+KT1L    = 0                     KT2     = 0.022                 UA1     = 4.31E-9
+UB1     = -7.61E-18     UC1     = -5.6E-11      AT      = 3.3E4
+WL      = 0                     WLN     = 1                     WW      = 0
+WWN     = 1             WWL     = 0                     LL      = 0
+LLN     = 1                     LW      = 0                     LWN     = 1
+LWL     = 0                     CAPMOD  = 2             XPART   = 0.5
+CGDO    = 7.47E-10      CGSO    = 7.47E-10      CGBO    = 1E-12
+CJ      = 1.180017E-3   PB      = 0.8560642     MJ      = 0.4146818
+CJSW    = 2.046463E-10          PBSW    = 0.9123142     MJSW    = 0.316175
+CJSWG   = 4.22E-10              PBSWG   = 0.9123142     MJSWG   = 0.316175
+CF      = 0                     PVTH0   = 8.456598E-4           PRDSW   = 8.4838247
+PK2     = 1.338191E-3   WKETA   = 0.0246885             LKETA   = -2.016897E-3
+PU0     = -1.5089586    PUA     = -5.51646E-11  PUB     = 1E-21
+PVSAT   = 50            PETA0   = 1E-4          PKETA   = -3.316832E-3
```