A DISSERTATION ON

REALIZATION OF CURRENT CONTROLLED CONVEYOR MULTIMODE FILTERS

SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENT FOR THE AWARD OF THE DEGREE OF

MASTER OF TECHNOLOGY
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This is certified that the dissertation entitled "**Realization of current controlled conveyor multimode filters"** is a work of **Mandeep Sheoran** (University Roll No.-2K12/VLS/12) a student of Delhi Technological University. This work is completed under my direct supervision and guidance and forms a part of Master of Technology (VLSI and Embedded System Design) course and curriculum. He has completed his work with utmost sincerity and diligence.

The work embodied in this major project has not been submitted for the award of any other Institute / University for the award of any other degree to the best of my knowledge.

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ABSTRACT

Current mode circuits like current conveyors are getting significant attention in current analog ICs design due to their higher band-width, greater linearity, larger dynamic range, simpler circuitry, lower power consumption and less chip area. The second generation current controlled conveyor (CCCII) has the advantage of electronic tunability over the CCII . In CCCII adjustment of the X-terminal intrinsic resistance via a bias current is possible. The presented approach is based on the CMOS implementation of multiple output current controlled conveyor (MO-CCCII) which is used to generate multiple loop feedback filter structure in transresistance mode , transadmittance mode and voltage mode . The circuit is used for its application in designing universal filter .

All the circuits have been designed and simulated on PSPICE software with 0.35μm CMOS technology model parameters which is used to validate filter feasibility and operating frequency ranges using 2.5V supply voltage. Various simulations have been carried out to verify the valid filter expression . The outcomes show good agreement between expected and experimental results.

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CHAPTER 1

INTRODUCTION

The prime requirements in today's microelectronics technologies are low supply voltages and low power consumption [1] . In addition to the above demands , there are other factors which are needed to be fulfilled in some applications , among them speed of signal processing is the first and efficiency or accuracy with which signal is proceesed is second factor . But fulfillment of above all conditions simultaneously is problematic . So from the last two decades, there are various applications which are now using the new technique for the analog signal proceesing called as current mode [2] which has features of both low power consumption and high speed . Earlier technologies made use of voltage mode which has some demerits as compared to the current mode .

1.1 COMPARISON OF CURRENT MODE AND VOLTAGE MODE

When voltage mode and current mode are compared , it is found that current mode has many advantages over voltage mode. First one is higher bandwidth and better signal linearity. Lower power consumption in current mode circuits constitute the second advantage . Also current mode circuits are designed for low voltage swings such that smaller supply voltage can be used . In the past , voltage mode were used in almost every applications , but now , with the development of current mode applications , there is third type of mode known as mixed mode was introduced ,which can be used where there is requirement of interfacing between different sub blocks which are working in different modes [3] . Other than that , new circuits are developing for the processing of both analog and digital circuits which employs higher accuracy devices like current mirror , current copier and switched current filter . So the effect of these devices can only be calculated if system is working in current mode .

Higher slew rate and better accuracy is another merit of current mode . Also current mode circuits are not effected by noise and loop resistance which are present in long wire runs and

faulty connections. The only type of noise that can be present is electromagnetically induced noise which can be eliminated by employing shielded twisted pairs. Last but not the least, current-mode circuits does not need high voltage gain and high precision passive components, so they can be designed almost entirely with transistors. The only advantage of voltage mode signals over current mode signals is that they interface directly with D/A and A/D converters and analog multiplexing devices. So from above discussion it is clear that using current mode is more profitable and accurate choice over the voltage mode[3] .

1.2 CURRENT CONVEYOR :

Current mode circuits proved to be more advantageous than voltage mode circuits which lead to vast development of various types of current mode building blocks . The current conveyor (CCII) is one among such blocks which has received significant attention. It is hybrid block and has basic construction containing a voltage follower interconnected with either current mirror or current follower. Current conveyors were introduced in the late sixties or early seventies by Smith and Sedra[5] . They were considered to be used not only as current sources, impedance converters and inverters, etc., but also as function generators, amplifiers, filters, etc., in current processing circuits in instrumentation and measurement applications.

In the initial years of its development , the performance of current conveyors was limited , as technologies available at that time are inflexible and did not allow well-matched devices on fabricated chips. But as the technology begin to progress , the current conveyors attracted the attention of analog designers ,which makes it very useful building blocks of analog electronics in today's technology. They are parts of a number of very often used circuits, like active filters, current feedback operational amplifiers, voltage and current operational amplifiers among others and their main application areas are in high-speed, high-frequency circuits for both voltage and current signal processing[6]. Current Conveyors represent the emerging class of high performance analog circuit design based on current-mode approach. They have simple structure, wide bandwidth and capability to operate at low voltages.

1.2.1 ADVANTAGES :

Current conveyors are unity gain active elements exhibiting higher linearity, wider dynamic range and better high frequency performance.

Current conveyor has greater range of operating frequency which implies that higher voltage gain can be achieved at higher frequency also unlike OP-AMP which provide higher gain only at mid frequencies due to parasitic capictances at higher frequencies. So current conveyor has higher gain bandwidth product as compared to OP-AMP. If the comparison of its performance is done with the other active element like conventional bipolar operational transconductance amplifier (OTA) , it is found that , the transconductance of the CCCII will be much higher than that of the bipolar OTA [3].

Then after the improvement in Current conveyor devices represented by CCI , CCII & CCIII ., there is another type of current conveyor was introduced, which has the tuning capability such that parameters of current conveyor block can be tuned according to the bias current I_0 [8-9] , those current conveyor are called current controlled conveyor II (CCCII) . The only difference between normal current conveyor and current controlled conveyor is that , the later will have the biasing current which is used to modify the parameters of current conveyor such as parasitic resistance. Now with that device multiple filters can be designed by cascading CCCII .A device which is just the extension of CCCII is introduced ,which is called MO-CCCII stands for multiple output current controlled conveyor , which can be used for realization of multiple filter simultaneously .

MO-CCCII is same as CCCII but only difference is that , it has more than one output terminal unlike simple current controlled conveyor which has only one output terminal .Having multiple output has its benefits , that is , multiple output can be used for cascading one MO-CCCII with another , both feed forward and feedback at the same time which helps in realization of multiple filters simultaneously and if there is any modification required in feedback network for realization of different structure, it can be easily done without effecting the feed forward network . Input can be applied in form of both voltage and current , and there is common output which constitutes the connection from all the cascaded MO-CCCII .The node voltage and terminal currents at various points can be evaluated . Different node will have different transfer functions with respect to the input applied, which provides different filter expression simultaneously at every node , so that different filters can be realized at the same time . The detailed description of MO-CCCII are given in chapter 3 .

1.3 OBJECTIVE :

The circuit was proposed cascading three MO-CCCII and two grounded capacitances and general expression for current gain was calculated for the 12 possible structure in the reference[8] . So extension of the proposed circuit is the main aim of the thesis , which includes

1. Calculation of generalized expression of transresistance i.e ratio of node voltages to the applied input current, at every node and verifying the derived expression on some structures(structure explained in chapter 3 in detail) by putting the values of different coefficients in the expression (coefficients explained in chapter 4 in detail) and verifying the results using PSPICE simulation for valid filter expression .

2. Calculation of generalized expression of transconductance i.e ratio of I_{OUT} to the applied input voltages , by applying the input in the form of voltage , at 2^{ND} and 3^{RD} MO-CCCII block and removing the main input node of 1st MO-CCCII . Then in the derived expression , different coefficients ,whose value are structure dependent, are applied and checked for various valid filter expression and the result so obtained are verified using PSPICE simulation .

3. Calculation of generalized expression of transfer fuction in the form of V/V ratio i.e ratio of node voltages to the applied input voltages . The input voltages are applied at grounded terminal of 2^{nd} and 3^{rd} MO-CCCII block .The derived expression is applied on some structure and results are verified using PSPICE simulation

1.4 ORGANIZATION OF THESIS :

The thesis is organized as follows

Chapter 2: Literature survey of development of current conveyor including their history is described . The summary of different blocks of current conveyor and its derivatives including

current controlled conveyor (CCCII) which is used as basic active block for thesis , is introduced .

Chapter 3: This chapter describes the current controlled conveyor II in more detail with its internal circuit . Furthermore extension of CCCII , multiple output CCCII (MO—CCCII), is explained in detail with its equations and internal circuit . Different structures possible(as proposed in reference[8]) with feedback and feed forward network of cascaded MO-CCCII is described in brief . The defining equations of basic block of MO-CCCII are verified using schematic Ppsice .

Chapter 4: In this chapter the generalized expression of transresistance for circuit proposed in [8] has been derived .In the reference [8] , transfer fuction in the form of ratio of I_{OUT} to I_{IN} is calculated . In this chapter node voltages are considered . Furthermore different coefficient which are deciding factor in the realization of various filter are explained in detail . The derived generalized expression is verified on some structures of cascaded MO-CCCII using schematic Pspice.

Chapter 5: In this chapter generalized expression of transconductance i.e ratio of I_{OUT} to the applied input voltage , has been derived . The results are verified on structures of cascaded MO-CCCII using Pspice.

Chapter 6: In this chapter generalized expression of transfer function in the form of V/V ratio is derived . The results are verified on some structures of presented circuit using PSPICE simulation.

Chapter 7: In this section conclusion of the thesis work and future scope of the work are presented.

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CHAPTER 2

CURRENT MODE BUILDING BLOCKS

This chapter represents the literature survey of development of current conveyor from three decades . The hierarchy of current conveyor development are used in describing the application of the reference circuit . Various types of current conveyor building blocks are also discussed which includes current controlled conveyor II (CCCII) which is main active block of thesis..

2.1 INTRODUCTION

The growth of analog IC design has been delayed by the process technologies that are mostly optimized for digital applications only . With the evolution of submicron technologies such as .18 micron and .13 micron , the supply voltage has been reduced to 3.3 volts and lower . This makes it difficult to design a voltage mode CMOS circuits with high linearity and wide dynamic range . Recently , current mode circuits have become viable alternative for future applications because of their inherit advantages over voltage mode circuits.

The main advantage of using the current mode technologies is because of the non linear characteristic exhibited by most field effect transistor . A small change in the input or controlling voltage results in the much larger change in the output current . Thus for a fixed supply voltage , the dynamic range of current mode circuit is much larger than that of a voltage circuit . If voltage supply voltage is lowered , one can still get the required signals represented by the current.

A second advantage of the current mode circuit is that they are much faster as compared to voltage mode circuits . The parasitic capacitances present in the analog circuits must be charged and discharged with the changing voltage levels.In the current mode circuits , a change in the current level is not necessary accompanied by a change in the voltage

level.Hence , the parasitic capacitances will not effect the operating speed of the circuit by a significant amount . Other advantage of using the current mode circuits are that they do not require specially processed capacitances or resisitors , they are more compatible with digital CMOS technology making integration of mixed signal circuits more feasible.

2.2 CURRENT CONVEYOR :

The current conveyor (CCII) is one among such blocks which has received significant attention. It is hybrid block and has basic construction containing a voltage follower interconnected with either current mirror or current follower. It is basic building block of a number of applications in current mode , voltage mode and the mixed mode. The principle of the current conveyor of the first generation was published by K.C Smith and A . S Sedra[2] .Two years later , today ‘s widely used second generation CCII was described and in 1995 , third generation CCIII was introduced[3] . However , initially , during that time , the current conveyor did not find many applications because its advantages as compared to the classical operational amplifier (OP AMP) and were not widely appreciated. An IC current conveyor , namely PA630 , was introduced by Wadsworth in 1989 (mass produced by Phototronics Ltd . of Canada) and about the same time the now well known AD844 (operational trans impedance amplifier or more popularly known as current feedback op-amp) was recognised to be internally as CCII+ followed by the voltage follower[4] .

An excellent review of state of art of current mode circuits prior to the 1990 was provided by the Wilson[5]. Today, the current conveyor is considered a universal building block with wide spread applications in the current mode , voltage mode and mixed mode signal processing . It features most of the applications in the current mode , when it so called voltage input voltage y is grounded and the current , flowing into the low impedance input x , is copied by simple current mirror into the z output. Since 1995 in particular , many successive modifications have been witnessed and generalisation of basic principle of CCII in order to use this circuit element more efficiently in various applications .

2.2.1 FIRST CURRENT CONVEYOR (CCI) :

The current conveyor as initially introduced , is a 3-port device whose black box representation is as shown in fig 2.1.

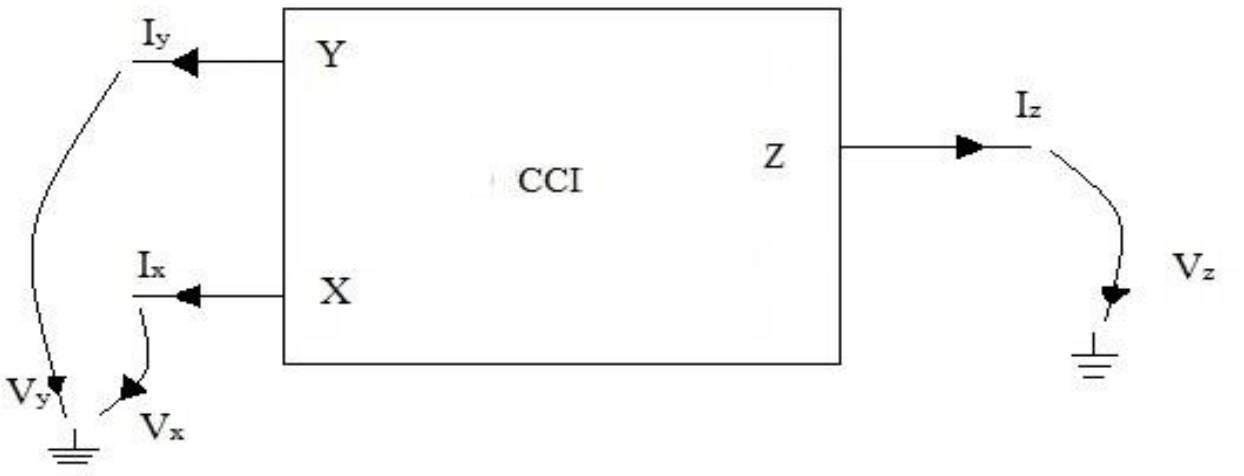

Fig 2.1 Basic block diagram of CCI

The operation of this device is such that if voltage is applied to the terminal Y, an equal potential will appear on the terminal X . In a similar manner , if an input current is forced into terminal X will result into an equal amount of current flowing into terminal Y .Also the same current I will be conveyed to the output terminal Z such that terminal Z has the characteristic of a current source of value I, with high output impedance[2].

As it can be seen , the potential of X being set up by that of terminal Y , is independent of current being forced into port X .Similarly , the current through input Y , being fixed by that of X , is independent of the voltage applied at Y. Thus , the device exhibits a virtual short circuit input characteristic at port X and dual virtual open circuited input characteristic at port Y.

Mathematically , the input – output characteristic of CCI can be described by the following equation

$$I_Y = 0$$
$$V_X = V_Y \qquad \text{eq. (2.1)}$$
$$I_Z = \pm I_X$$

Where the variables represents total instantaneous quantities . The + sign applies for the CCI in which both I_Z and I_X flow into the conveyor and it is denoted by CCI+ . The - sign applies for the opposite polarity case denoted by CCI-. To visualize the interaction of the port voltages and currents described by the above matrix equations the nullator-norator representation as shown in fig 2.2 .

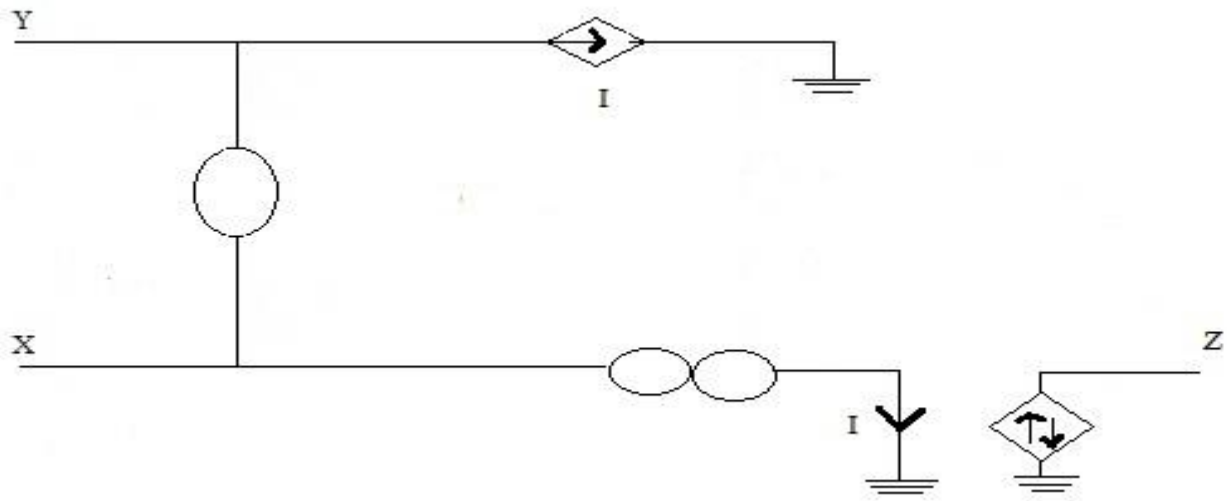

Fig 2.2 Nullator - Norator representation of CCI

In the figure 2.2 shown on the previous page , single ellipse is used to represent the nullator element and two intersecting ellipses to represent the norator element . The nullator element has constitutive equation V = 0 and I = 0 whereas the norator has an arbitrary current voltage relationship . Clearly the nullator element is used to represents the virtual short circuit apparent between the X and Y terminal. Also included in the circuit are two dependent current sources . These are used to convey the current at port X to port Y and Z.

2.2.2 NEGATIVE IMPEDANCE CONVERTER :

An early application of CCI was its use as a negative impedance converter (NIC). For this application terminal Z is grounded and the resistor is to be converted , is connected either between X and ground or between Y and ground . If resistor R is connected between X and ground , then looking into Y one sees a resistance –R that is short circuit stable[6] . Alternatively if R is connected between Y and ground then the input resistance at X is -R and is open circuit stable.

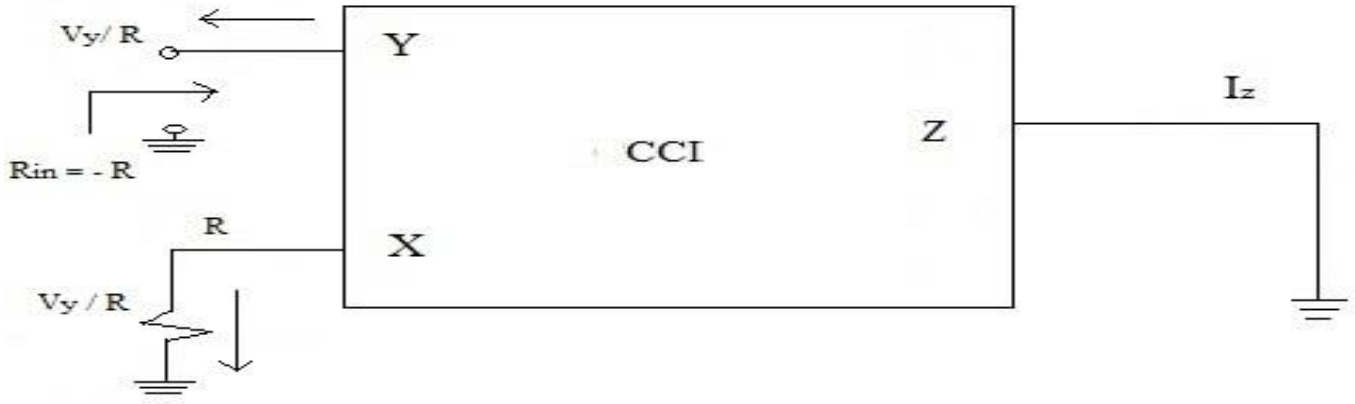

Fig 2.3 CCI implementation of Negative Impedance Converter(NIC) with -R at terminal Y

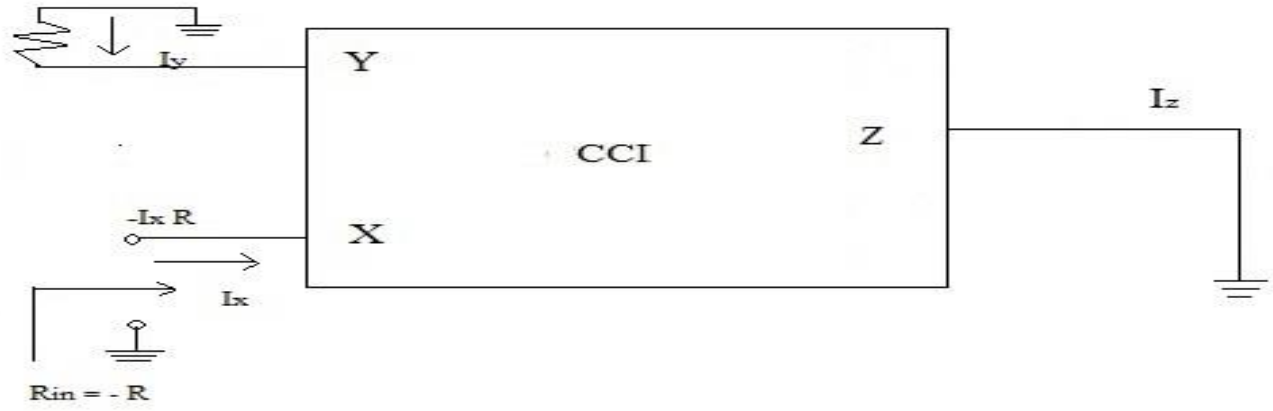

Fig 2.4 CCI implementation of Negative Impedance Converter(NIC) with –R at terminal X

The major problem that hindered the fabrication of the CCI in IC form in the 1960s is its use of high quality PNP devices . Since complimentary devices are available in CMOS technology , it is easy to fabricate a CMOS current conveyor

2.2.3 THE SECOND GENERATION CURRENT CONVEYOR (CCII) :

To increase the versatility of current conveyor , a second version of current conveyor was introduced in which no current flows in terminal Y .The CCII is three-terminal devices with the terminals designated X, Y and Z. The potential at X equals whatever voltage is applied to Y. Whatever current flows into X is mirrored at *Z* with a high output impedance. No current flows through terminal Y. The block diagram of CCII is shown in Fig 2.5 .

The ideal CCII can be seen as an ideal transistor, with perfected characteristics. No current flows into the gate which is represented by Y. There is no gate-source voltage drop, so the source voltage (at X) follows the voltage at Y. The gate has infinite input impedance (Y), while the source has zero input impedance (X). Any current out of the source (X) is reflected at the drain (Z) as a current in, but with infinite output impedance. Because of this reversal of sense between X and Z currents, this ideal field-effect transistor represents a CCII−[3]. If current

flowing out of X resulted in the same high-impedance current flowing out of Z, it would be a CCII+.

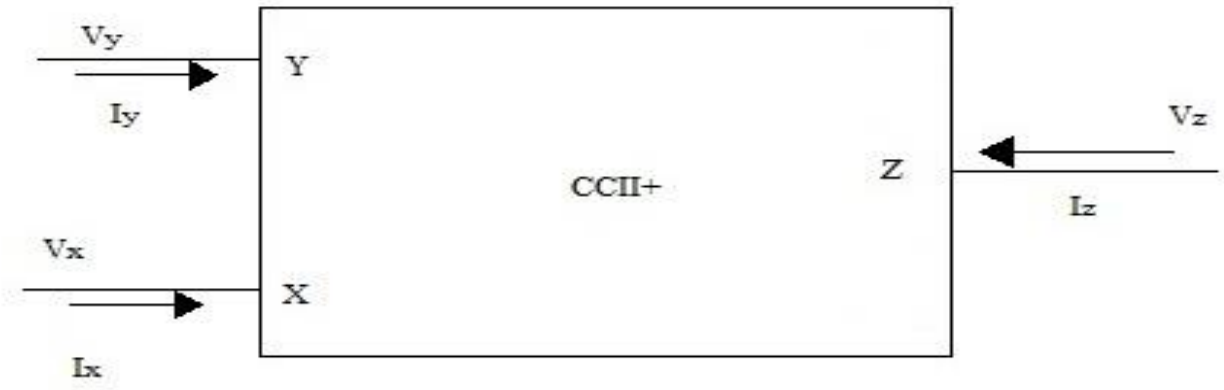

Fig 2.5 Block diagram of CCII

The relationship[3] between three terminals is defined as below:

$$I_y = 0$$

$$V_x = V_y \qquad \text{eq. (2.2)}$$

$$I_z = \pm I_x$$

The $\pm$ sign indicates the I_x and I_z are in same direction or opposite.

According to above equations, as it is known that an ideal CCII is a combination of a voltage follower and a current follower. The voltage follower between Y and X terminals and the current follower between X and Z terminals. An ideal voltage follower has infinite input impedance and zero output impedance, and an ideal current follower has zero input impedance and infinite output impedance. In terms of nullator the port behavior of second generation current conveyor (positive or negative) can be depicted as in fig 2.6 .

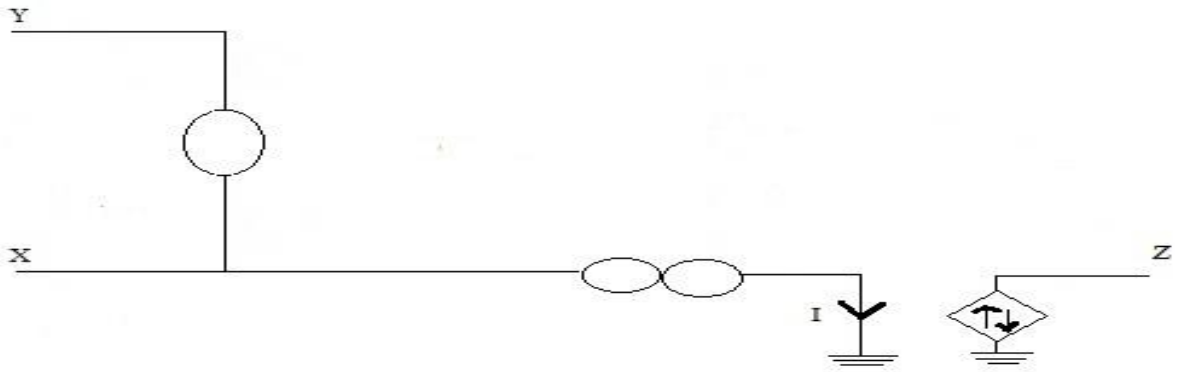

Fig 2.6 Nullator - Norator representation of CCII

The similarity and difference between CCI and CCII are clearly evident from their equivalent circuit . In the case of CCII- , the dependent current source is redundant , current flowing into terminal X must flow out of terminal Z . Hence the equivalent circuit of CCII- can be represented with single nullator element as shown in fig 2.7

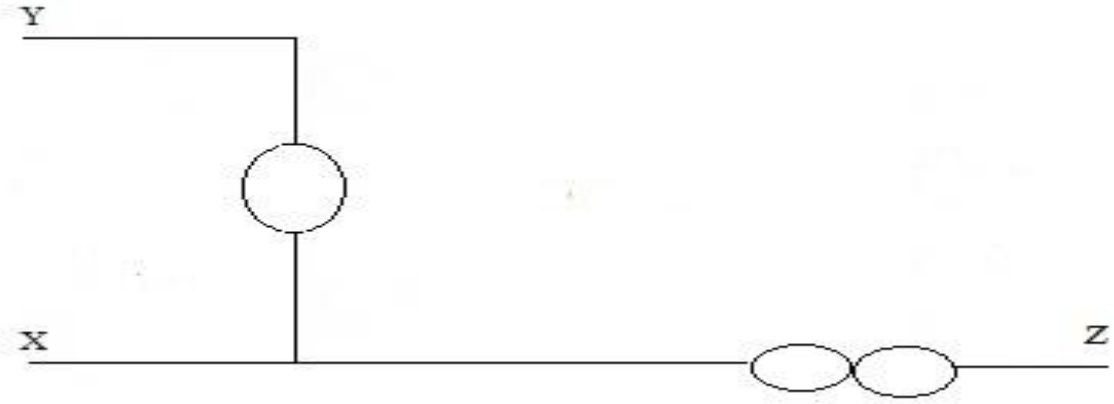

Fig 2.7 A Simplified representation of CCII-

The first widely recognized applications of CCII were in the realization of controlled sources , impedance converters , impedance inverters , gyrators and various computation devices.

2.2.4 THE THIRD GENERATION CURRENT CONVEYOR (CCIII) :

This structure was published by Fabre in 1995 . Structurally it is quiet similar to CCI with the exception that the current in port X and Y flow in the opposite direction . It is represented by push pull topology built from four simple CCIs . Its main application is current measurement[4].

Utilizing the same block diagram representation , CCIII is represented by

$$I_y = 0$$

$$V_x = V_y \qquad \text{eq. (2.3)}$$

$$I_z = \pm I_x$$

2.3 DIFFERENTIAL VOLTAGE CURRENT CONVEYOR (DVCC) :

In this type of current conveyor , original input voltage is split into two pair of inputs Y+ and Y- [8].There is another input terminal i.e X whose voltage is given by voltage difference of the voltages difference . This offers more freedom during the design of voltage and mixed mode applications[8] . The block diagram of DVCC is shown as below in fig 2.8.

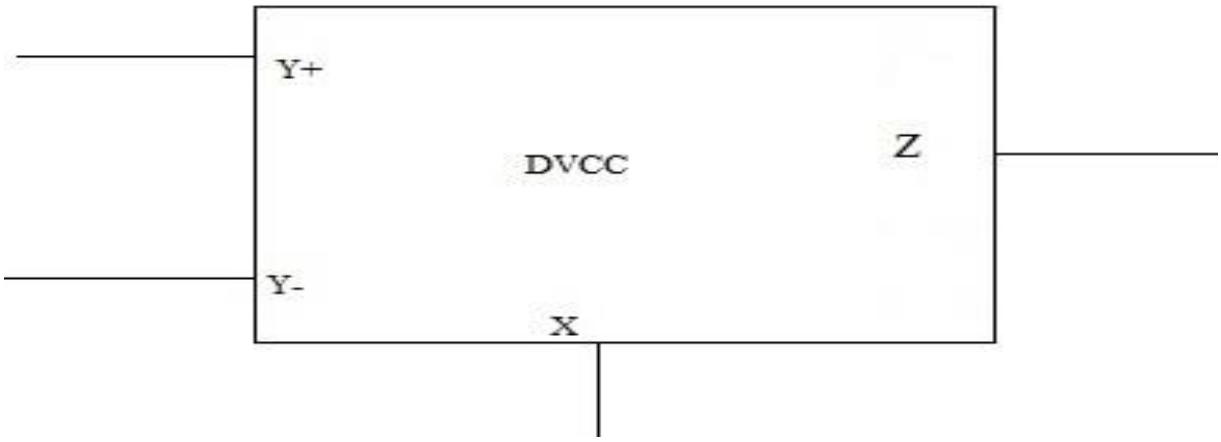

Fig 2.8 Block diagram of DVCC [8]

Equations[8] satisfied by the above active block are

$$I_{Y+} = I_{Y-} = 0$$

$$V_X = V_{Y+} - V_{Y-} \qquad \text{eq. (2.4)}$$

$$I_Z = I_X$$

2.4 INVERTING CURRENT CONVEYOR II (ICCII) :

In this current conveyor , the current at input terminal Y is zero and voltage at input terminal X and Y are equal but opposite in polarity . It is just the complementary type of current conveyor[9] whose block diagram is shown as fig 2.9

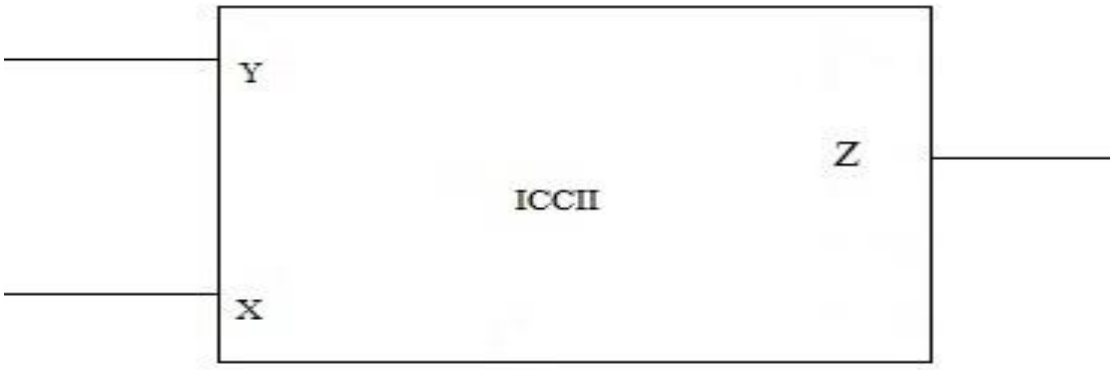

Fig 2.9 Block diagram of ICCII [9]

Equations[9] of above block can be represented as

$$I_Y = 0$$

$$V_X = - V_Y \qquad \text{eq. (2.5)}$$

$$I_Z = \pm I_X$$

2.5 DIFFERENTIAL DIFFERENCE CURRENT CONVEYOR (DDCC) :

In this current conveyor, the input terminal is split into three terminal naming Y_1, Y_2, Y_3 and input current at both the three terminal in zero[10] . There is another terminal X whose voltage is combination of three input terminal voltages of splited Y terminal .

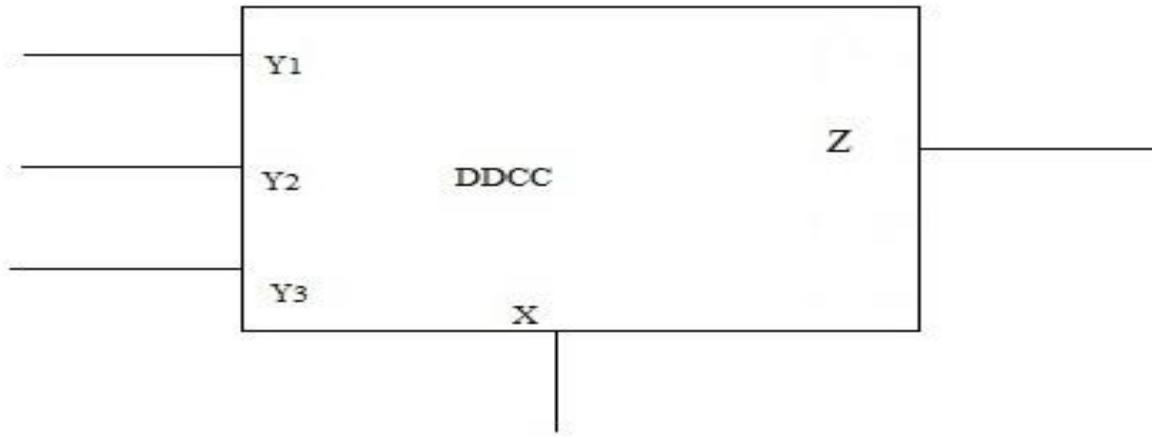

Fig 2.10 Block diagram of DDCC[10]

Equation[10] of above block are

$$I_{Y1} = I_{Y2} = I_{Y3} = 0$$

$$V_X = V_{Y1} - V_{Y2} + V_{Y3} \qquad \text{eq. (2.6)}$$

$$I_Z = I_X$$

2.6 DIFFERENTIAL DIFFERENCE CURRENT CONTROLLED CONVEYOR (DDCCC) :

This block is just extension of the previously described DDCC but only difference is just that , here, output terminal Z is also split into two terminal named as Z_1 and Z_2[11] which is as shown in block diagram fig 2.11 .

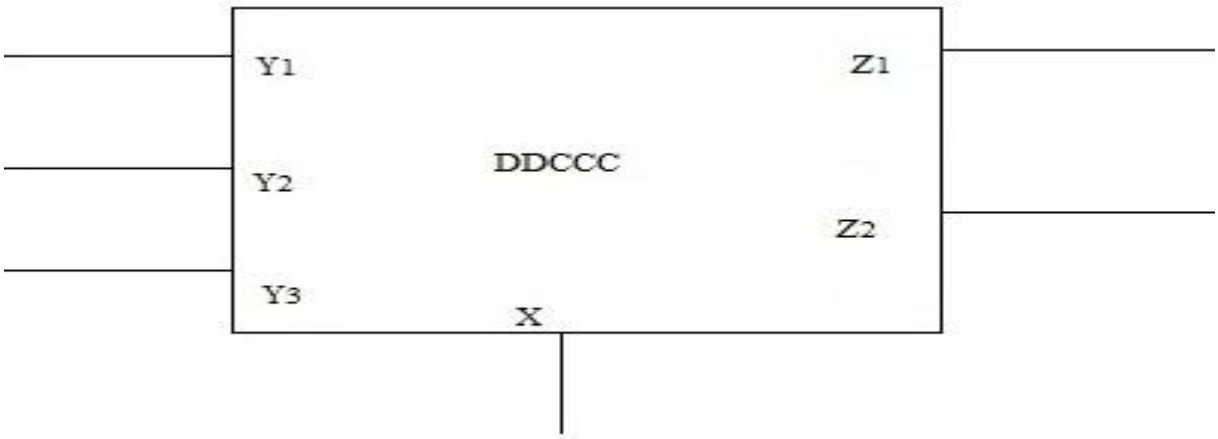

Fig 2.11 Block diagram of DDCCC [11]

Equations[11] representing the above blocks are

$$I_{Y1} = I_{Y2} = I_{Y3} = 0$$

$$V_X = V_{Y1} - V_{Y2} + V_{Y3} + I_X R_X \qquad \text{eq. (2.7)}$$

$$I_{Z1} = I_X$$

$$I_{Z2} = - I_X$$

2.7 DIFFERENTIAL CURRENT CONVEYOR II (DCCII) :

In this block of current conveyor[12] , X input terminal is split into two terminal as X+ and X- and Z terminal as Z_1 and Z_2 ,also in this current conveyor , the input terminal voltage at three terminal are equal and the output current at both terminal are equal but opposite in polarity and equivalent to the difference of current at terminal X+ and X-.

Fig 2.12 Block diagram of DCCII [12]

Equations[12] representing the above block are :

$$I_Y = 0$$

$$V_{X+} = V_{X-} = V_Y \qquad \text{eq. (2.8)}$$

$$I_{Z1} = -I_{Z2} = I_{X+} - I_{X-}$$

2.8 MODIFIED DIFFERENTIAL CURRENT CONVEYOR (MDCC) :

It is simplification of DCC on the assumption that signal voltage at terminal Y[12] , is zero which implies that voltage at both the X terminal is also zero as the voltage is equal in three terminal i.e two terminal of X and one terminal of Y .

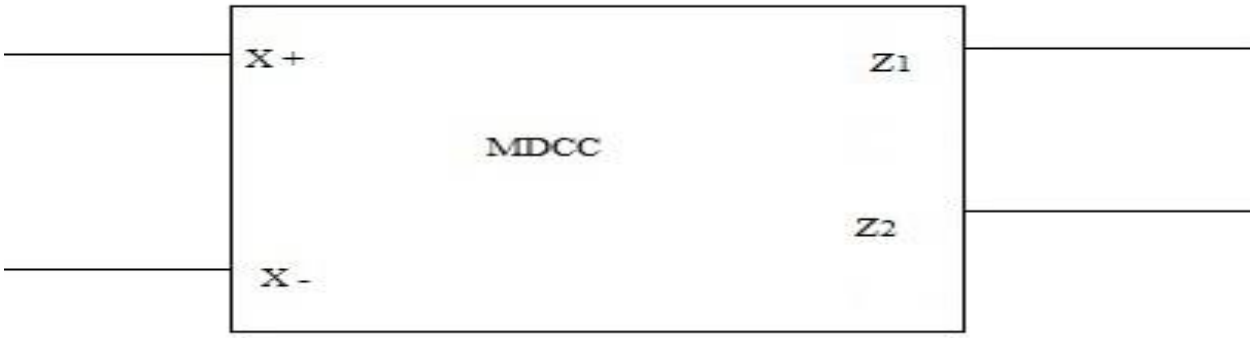

Fig 2.13 Block diagram of MDCC [12]

Equation[12] for the above defined block are :

$$V_{X+} = V_{X-} = V_Y = 0 \qquad \text{eq. (2.9)}$$

$$I_{Z1} = -I_{Z2} = I_{X+} - I_{X-}$$

2.9 DUAL –X CURRENT CONVEYOR (DXCCII) :

Dual –X current conveyor is proposed by Zeki and Toker[13] . It is combination of CCII and ICCII . Instead of single X terminal , DXCCII has two terminal X_P and X_N as outputs of non inverting and inverting unity gain amplifier with their inputs connected to y terminal[13] . Copies of X_P and X_N terminal currents are provided at Z_N and Z_P terminal[13]. The block diagram for above is as shown in fig 2.14

Fig 2.14 Block diagram of DXCCII [13]

Equation[13] representing the above block are :

$$I_Y = 0$$

$$V_{XP} = -V_{XN} = V_Y \qquad \text{eq. (2.10)}$$

$$I_{ZP} = I_{XP}$$

$$I_{ZN} = I_{XN}$$

2.10 FULLY DIFFERENTIAL CURRENT CONVEYOR II (FDCC II):

FDCC II is an important realization of the conventional CCII. The x, y, z terminal occurs here in pairs[14] . The basic circuit equation of CCII are now valid for differences of voltages or currents which corresponds to these pairs . It is thus designed for application with fully differential architecture for fast signal processing[15] . In this both X and Y terminal are splitted in two each which are shown as below in fig 2.15

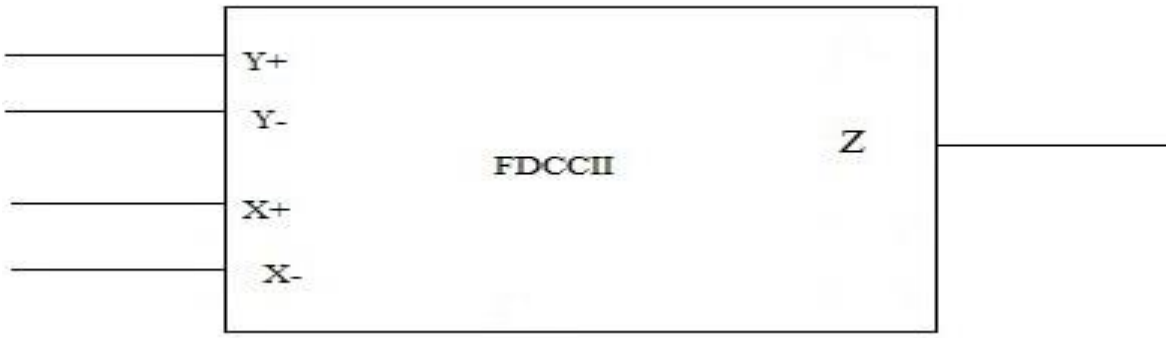

Fig 2.15 Block diagram of FDCCII [14]

Equation [14] for FDCC II are :

$$I_{Y+} = I_{Y-} = 0$$

$$V_{X+} = V_{X-} = V_{Y+} - V_{Y-} \qquad \text{eq. (2.11)}$$

$$I_Z = \pm (I_{X+} - I_{X-})$$

2.11 OPERATIONAL FLOATING CONVEYOR (OFC) :

It is conveyor which is formed from joining of two current conveyor (CCII-)[16] .It is a universal differential input ,differential output building block enabling current and voltage and mixed mode applications[20] . In this voltage at both terminal X and Y are equal and current at Y terminal is zero[16] , also the current at two output terminal W and Z are equal with opposite polarity which are shown as in fig 2.16

Fig 2.16 Block diagram of OFC [16]

Equations[20] are

$$I_Y = 0$$

$$V_X = V_Y \qquad \text{eq. (2.12)}$$

$$V_w = Z_T I_X$$

$$I_Z = - I_W$$

2.12 CURRENT GAIN CONVEYOR II (CGC) :

This is another type of current conveyor which electronically control the parameters of applications .It has variable current gain I_Z/I_X [19] . The current conveyor of such type , concretely CCII- , was formerly manufactured by Elantec under the code EL2717[19] . The variable gain is implemented via transforming current I_Z into voltage by means of resistor and via back transformation of voltage into current by means of electronically gm controlled OTA. The most recent solution is characterized by digital control of the gain , utilizing the so called CDN[23] (current division network) and DCCCF (digitally controlled current follower). In this type of current conveyor current at terminal voltage Y is zero , voltage at two terminal X and Y are equal and most importantly the output current at terminal Z is current gain times the input current at terminal X [19]. Block diagram of above defined current conveyor is defined as follows in fig 2.17.

Fig 2.17 Block diagram of CGCII [17]

Equation [19] representing the above defined current conveyor are :

$$I_Y = 0$$

$$V_X = V_Y , \; I_Z = A\, I_X \qquad \text{eq. (2.13)}$$

2.13 CURRENT CONTROLLED CONVEYOR II (CCCII) :

Current controlled conveyor was invented by Fabre in 1996 , it was extension of earlier current conveyor , in which the input resistance can be altered using the biased current (I_0) such that this current conveyor includes electronically tunable parameters and have high frequency range . In CCCII input impedance at terminal Y is very high such that no current flows through the terminal and at terminal X input impedance or value of parasitic resistance can adjustable according to the bias current so as value of resistance can be changed , so value of voltage at terminal X also indirectly depends on the biasing current[16] This can be shown , that this active device can be used in filters [18] whose parameters may be controlled electronically . Such a feature has been inherent in the so called g_mC filters i.e filters , compounded only of OTAs and capacitors. In this type of current controlled conveyor , current at Y terminal is zero[18] and current at output Z terminal is equal to $\pm I_X$.The CCCII based circuits doesnt require any external circuits , such that they can be used in the various analog applications ,its property of electronic tunability can be used in the filters , CCCII based circuits can work in high frequency range operation. The basic block diagram of CCCII can be shown as below in fig 2.18

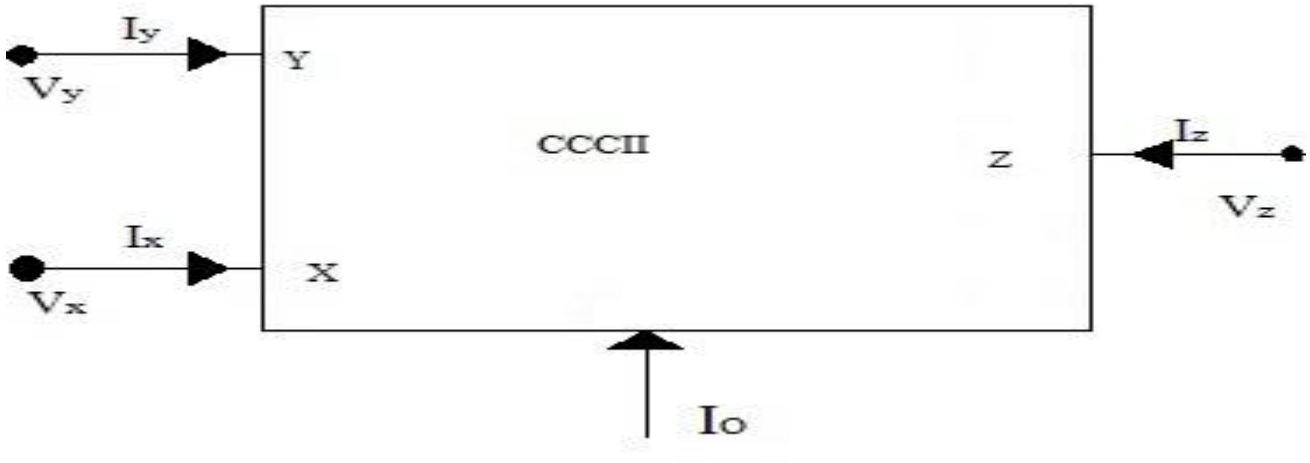

Fig 2.18 Basic block diagram of CCCII [21]

The defining equation for CCCII are

$$V_X = V_Y + I_X|R_X(I_0)|$$

$$I_Y = 0 , \; I_{Z-} = - I_X , \; I_{Z+} = I_X \qquad \text{eq. (2.14)}$$

Where $R_X = {}^{V_T}/_{2I_0}$ is bias current dependence resistance , V_T is thermal voltage , I_0 is bias current of CCCII[23].

If non idealities is taken into the consideration the defining matrix for CCCII can be[23]

$$V_X = \beta V_Y + I_X|R_X(I_0)|$$

$$I_Y = 0 , \; I_{Z-} = - \alpha I_X , \; I_{Z+} = \alpha I_X \qquad \text{eq. (2.15)}$$

where α and β are respectively current and voltage gains which are all equal to unity in the ideal case. In practice, they can be expressed as α =l- ε_i , $\beta = 1 - \varepsilon_V$ where $|\varepsilon_i| << 1$ and $|\varepsilon_v| << 1$. ε_i denotes the current tracking error and ε_v denotes voltage tracking error[3].
The current controlled current conveyor (CCCII) exhibits the features of the CCII plus the controllability. It has been realized in different technologies, BJT, CMOS, and BICMOS[23] . The internal circuitry of CCCII can be shown with two input terminal i.e X and Y and one output terminal Z using the CMOS can be shown as in fig 2.18 [21] .

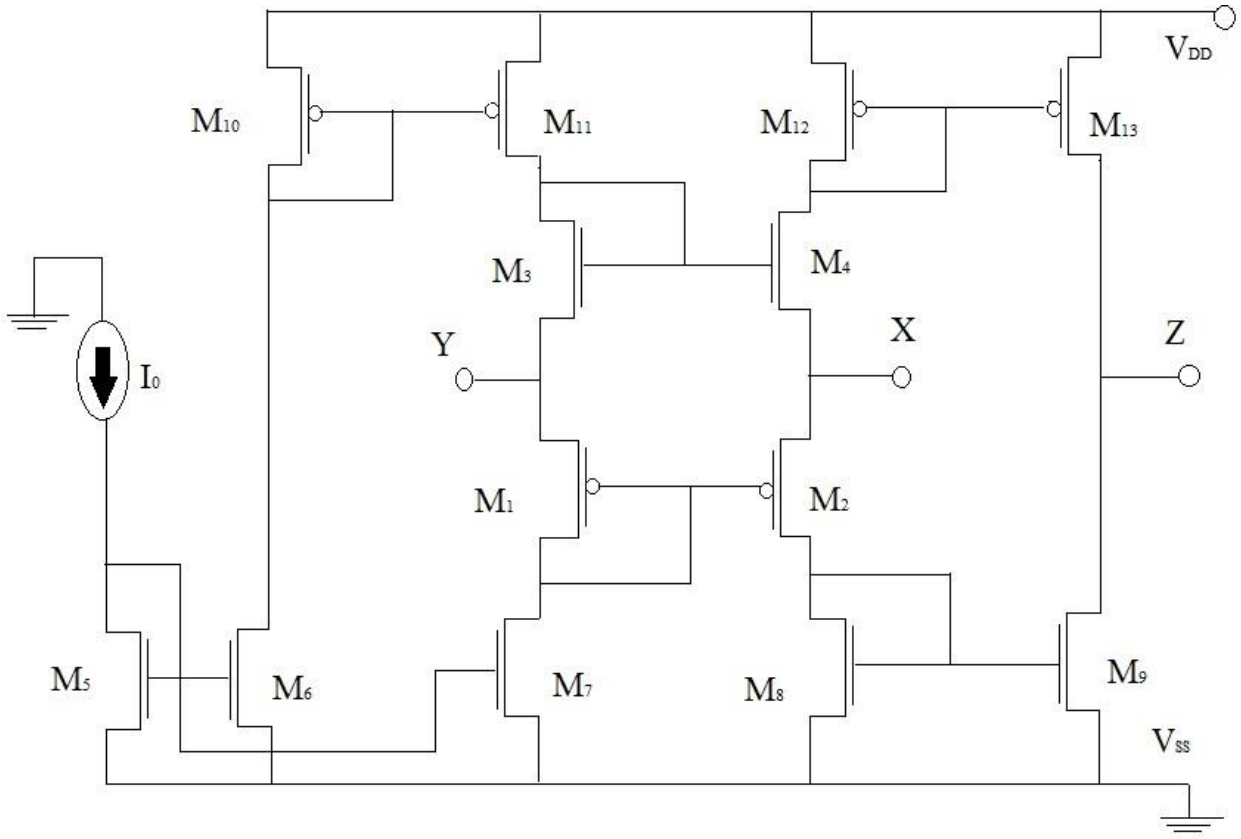

Fig 2.19 Internal Circuit of CCCII[18]

2.13.1 OPERATION :

The circuit in Fig 2.18 consists of one mixed trans-linear loop(transistors M1 to M4) as input cell. Two current mirrors (transistors M5, M7 and M10, M11) allow the mixed loop to be dc biased by the current I_0, the input cell present a high input impedance input port (Y) and a low impedance output port(X)[25]. This cell act as a voltage follower. The output Z that copies the current flowing through port X is realized in the conventional manner using two complementary mirror . A current controlled conveyor with negative current transfer (CCCII-) will be obtained easily, by only adding two cross coupled current mirrors in order to reverse the sign of the current through i_z[25] . Now it can be said that the current controlled conveyor (CCCII) is a translinear CCII to which the possibility of changing the value of the DC bias current Io will increase the additional properties. All the other characteristics of the CCIIs are preserved. The above discussed CCCII have two input terminal and one output terminal, such that, it

applications can be extended if it is modified to the multiple output current controlled conveyor or MO-CCCII which is discussed in next chapter in detail .

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CHAPTER 3

Multiple Output - Current Controlled Conveyor II (MO-CCCII)

This chapter describes the internal circuit of multiple output current controlled conveyor II (MO-CCCII). It uses additional current mirrors in CCCII to provide current terminals. The block diagram of MO-CCCII are verified through simulation. A generalized current mode filter is reviewed first , which is subsequently used for deriving the generalized expression for transresistance mode filters , transadmittance mode filters and voltage mode filters .

3.1THEORY: It is modified version of CCCII , as only difference between their block diagram is that MO-CCCII have multiple output i.e two output terminal for Z+ and two output terminal for Z- , where sign represents the direction of the current . Sign positive stands for in the same direction of the current at terminal at X and negative sign means the direction of output current will be opposite to the direction of the current at terminal X. The MO-CCCII can be designed using CCCII by just employing the extra current mirrors. The advantage of having multiple output is that using the multiple ports , CCCII can be used for multi functionalities . Another beneficial of using MO-CCCII is that it helps in reducing the required number of current conveyor at the cost of a pair of transistor (current mirror) . The block diagram of MO-CCCII is as shown in fig3.3.

Fig 3.1 Basic block diagram of MO-CCCII [2]

It uses additional current output terminals for developing current feedback connected together for achieving useful filter function and makes structure more versatile and flexible . The filter exhibit low input impedance and also does not require any matching component criteria and current inversion for obtaining any filter response . The structure is also capable of generating all standard response of universal filters at high output impedance i.e low pass filter , band pass filter , high pass filter , notch and all pass[2] . The internal circuit of multiple output current controlled conveyor II (MO-CCCII) is as shown in fig 3.2 .

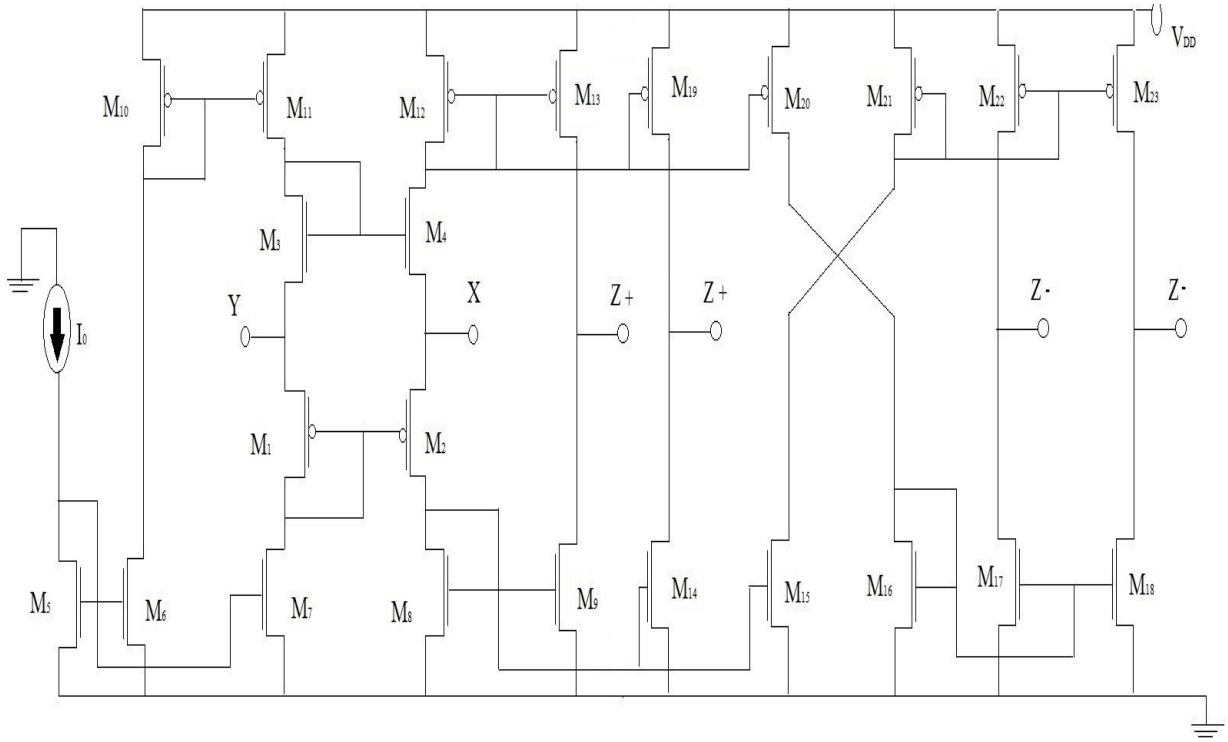


Fig 3.2 Internal Circuit of MO-CCCII [2]

Port relationship of current conveyor shown in Fig 3.2 are

$$V_X = V_Y + I_X|R_X(I_0)|$$

$$I_Y = 0 , \; I_{Z\pm} = \pm I_X$$

3.2 ADVANTAGES:

The MO-CCCII can be used for number of applications , when used as single block or when it is cascaded and there are multiple filters that can be generated , also it has many advantages over other current mode single input single output (SISO) structure[6] .

First one is , when more than one MO-CCCII is realized by cascading them , so as to realize universal filters i.e low pass , high pass, band pass , notch filter , less number of current conveyor are required as compared to other multiple filter circuit generator . Secondly it uses grounded capacitor which allows absorption of parasitic capacitance[7] and also helps in minimizing chip area ,making the structure suitable for monolithic integration . Third advantage is, its verstality , as there is no or very little modification required for the realization of multiple filter fuction[8] . Fourth one is it got advantages of electronic tunability which are required in many applications such that filter coefficients can be tuned according to the demand , such that , it increase its adaptability ,also there are many structure which uses different type of current conveyors for achieving tunability ,some being variable gain CCIIs and rest being CCIIs which is not considered good for integrated circuit layout viewpoint but in this system only one type of current conveyor are used .Last but not the least , is it exhibits low active and passive sensitivities[7].It is clear from above discussion that , MO-CCCII structure has many advantages and can be used for realization of filters , for which , more than one MO-CCCII are required and they should be cascaded so as to get multiple output at different node in the form of current or voltages

3.3 MULTIPLE LOOP FEEDBACK CURRENT MODE FILTER STRUCTURE:

The structure of multiple loop feedback current mode filter which employs three MO-CCCII and two grounded capacitors was proposed in [7] . The MO-CCCII blocks in the structure are cascaded by both feed forward and feedback network simultaneously such that their structure can be changed by modifying the feedback network . Feedback is defined by feedback coefficients.Therefore a new generalized circuit was proposed in [7] , which can be used for deriving the generalized expression for transresistance mode filters , transadmittance mode filters and voltage mode filters . A brief review is presented in the following subsection . The block diagram of discussed structure is shown in fig 3.3 .

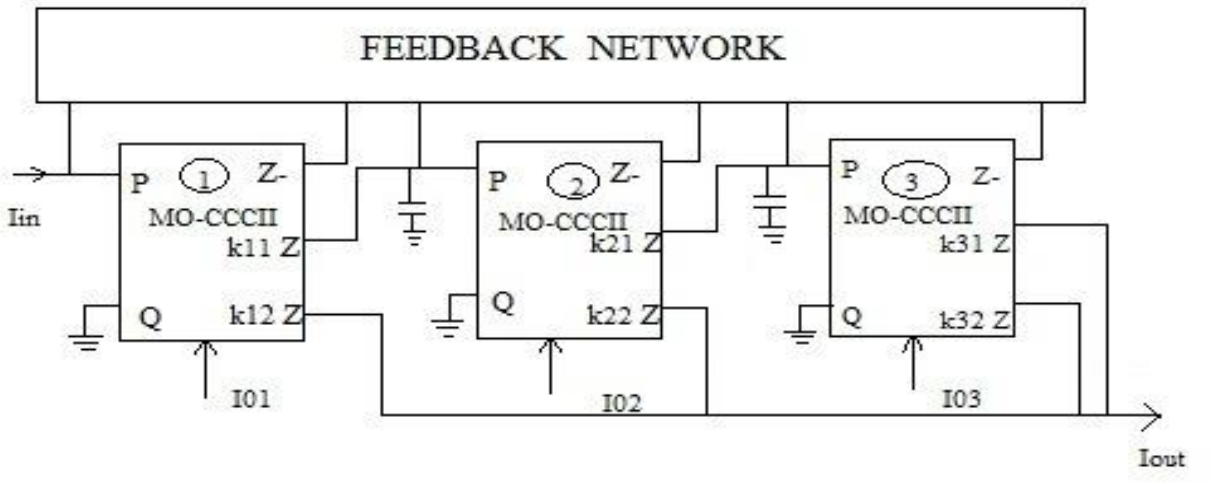


Fig3.3 Multiple loop feedback current mode filter structure[7]

Each block will satisfy the port relationship given below as

$$V_X = V_Y + i_X|R_{Xi}(I_{0i})|$$

$$i_Y = 0\ ,\ i_{Z-} = -i_X\ ,\ i_{K_{i1}} = k_{i1}i_X\ ,\ i_{k_{i2}} = k_{i2}i_X$$

where k_{i1} and $k_{i2} = \pm 1$ and $i = 1, 2, 3$ depending upon the number of block . $R_{Xi} = {}^{V_T}/_{2I_{0i}}$ is bias current dependence resistance , V_T is thermal voltage , I_{0i} is bias current of i^{th} MO-CCCII.

Apart from above port relationship , the above proposed structure will satisfy three feed forward equations also and depending on these three equations , different filters are realized by changing the value of different coefficients which will be defined in detail in next chapter.So three feed forward equation[7] are

$$i_i + i_{f1} = a_1 i_{x1} \qquad (1)$$

$$k_{11} i_{x1} + sC_2V_{P2}(i = 2) + a_2 i_{x2} = i_{f2} \qquad (2)$$

$$k_{21} i_{x2} + sC_3V_{P3}(i = 3) + a_3 i_{x3} = i_{f3} \qquad (3)$$

also there is one equation for node voltage also which is satisfied when either of terminal X or Y is grounded

$$V_{pi} = b_i i_{xi} R_{xi}$$

It is derived from equation

$$V_X = V_Y + i_X |R_{Xi}(I_{0i})|$$

Where f_{ij} is the current feedback coefficient from output of j^{th} MO-CCCII to the input of i^{th} MO-CCCII such that the value of f_{ij} can have zero or unity depending upon whether there is open circuited or direct feedback connection between i^{th} and j^{th} MOCCCII . It may be noted that $f_{21} = f_{31} = f_{32} = 0$, being non – feedback coefficients[7].

Notation a_i represents whether the current is flowing into the input of MO-CCCII or not So its value can be 0 or 1, zero if the input is Y terminal and 1 if the input terminal is X

Notation b_i can be either 1 or -1 depending on whether the input is connected to the X terminal or Y terminal which can be found out by the value of a_i.So if the value of $a_i = 1$ means input is connected to terminal X and $b_i = 1$ if $a_i = 0$ then input to the MO-CCCII is connected to Y terminal means $b_i = -1$[7].

Now by using the above three equations different structure can be formed , 12 such structures are possible and for each structure depending on the value of a_2 and a_3 , four different topologies are possible so total 48 expressions are possible . and then further taking different value of coefficient k , many filters expression are possible .

The transfer fuction of above structure in form of current gain can be expressed by[7]

$$\frac{I_{OUT}}{i_{in}} = -\frac{N(s)}{D(s)} \qquad (1)$$

Where

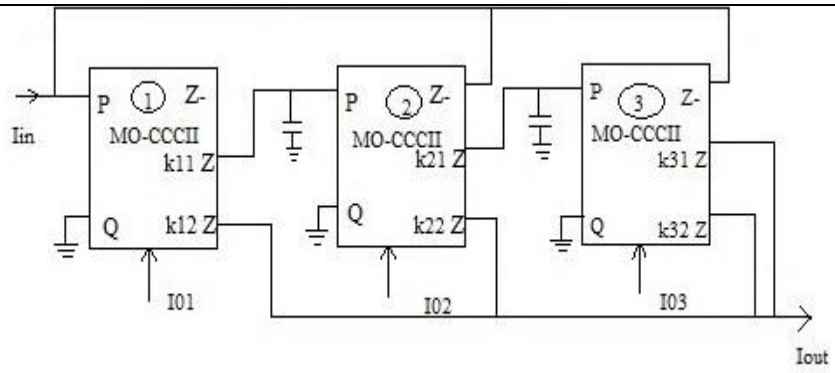
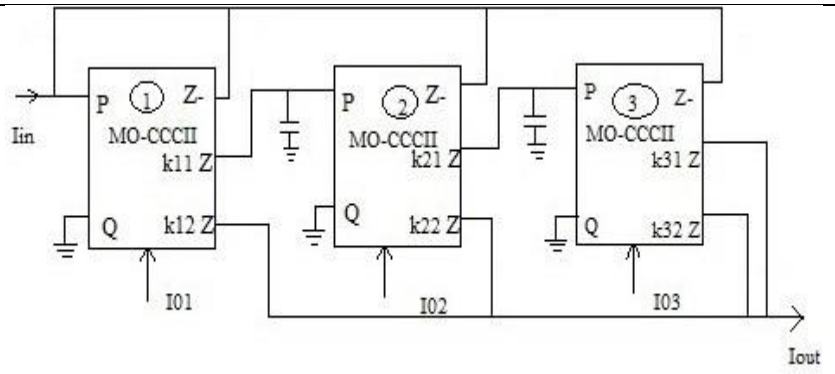
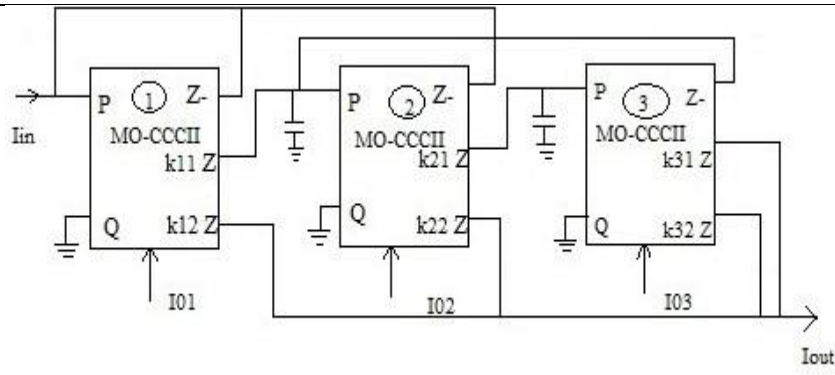
N(s)= $k_{12}[(f_{33} - a_3 - b_3\, sC_3R_{x3})\,(f_{22} - a_2 - b_2 sC_2R_{x3}) + f_{23}k_{21}] + k_{11}k_{22}(f_{33} - a_3 - b_3\, sC_3R_{x3}) + k_{12}k_{21}(k_{31} + k_{32})$

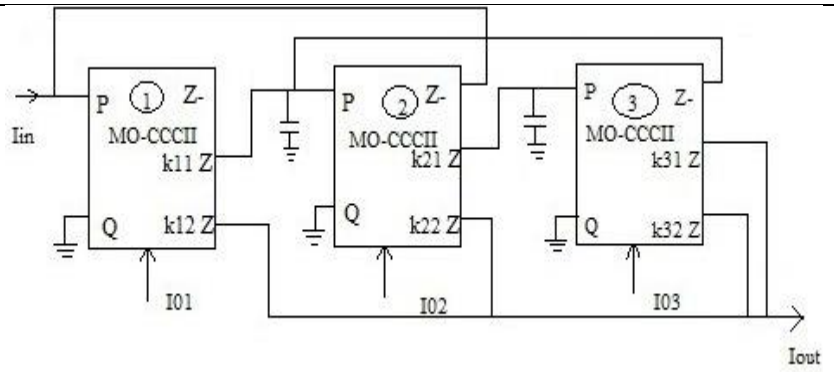
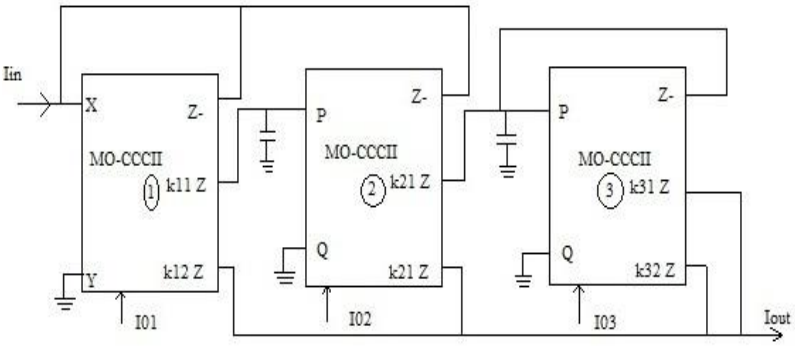
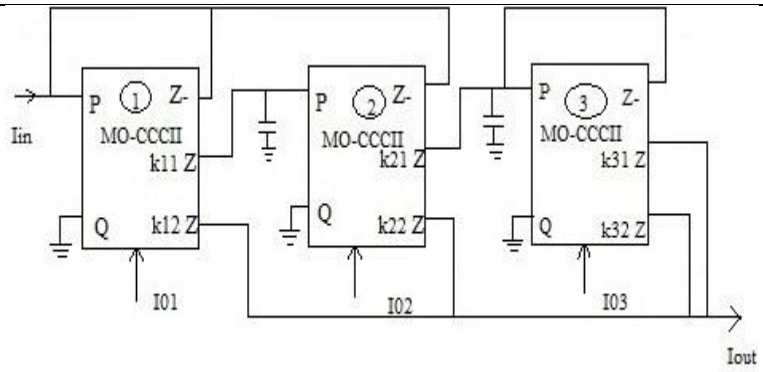
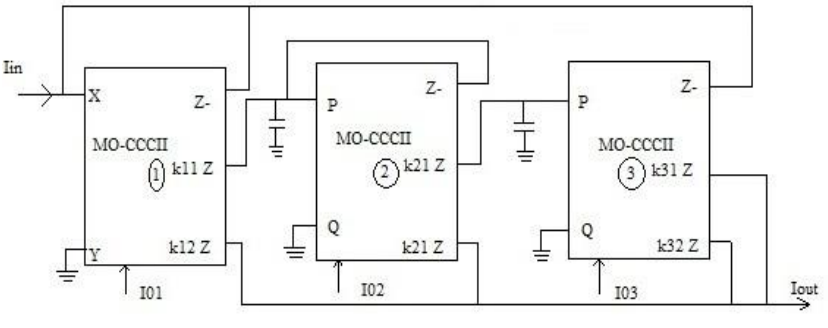
D(s)= $(f_{11} - a_1)[(f_{33} - a_3 - b_3\, sC_3R_{x3})\,(f_{22} - a_2 - b_2 sC_2R_{x3}) + f_{23}\, k_{21}]$

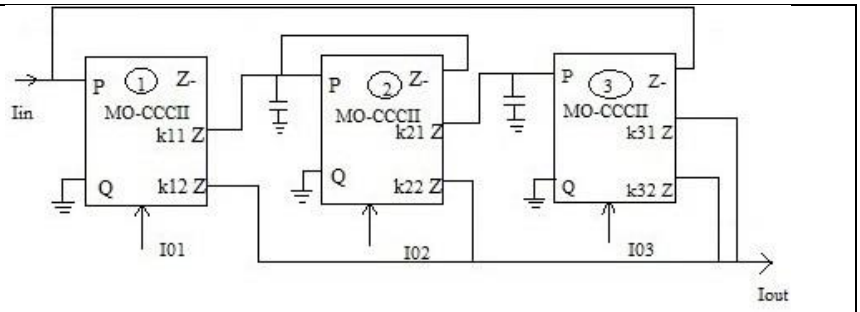
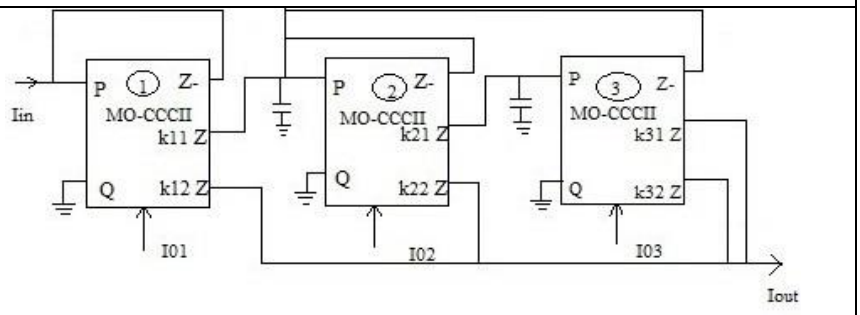
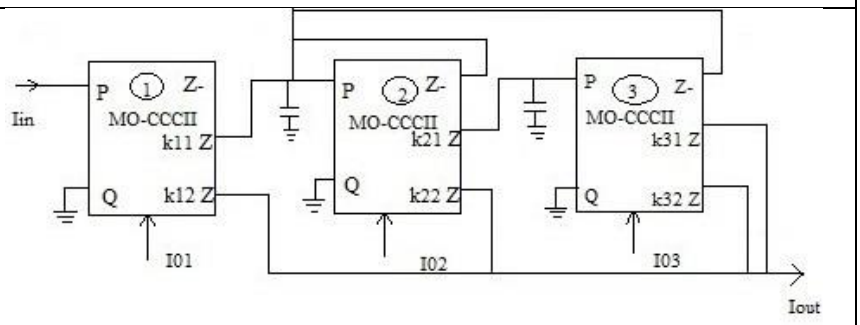
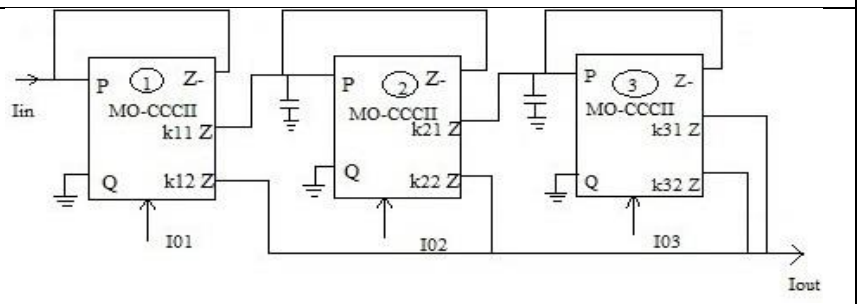
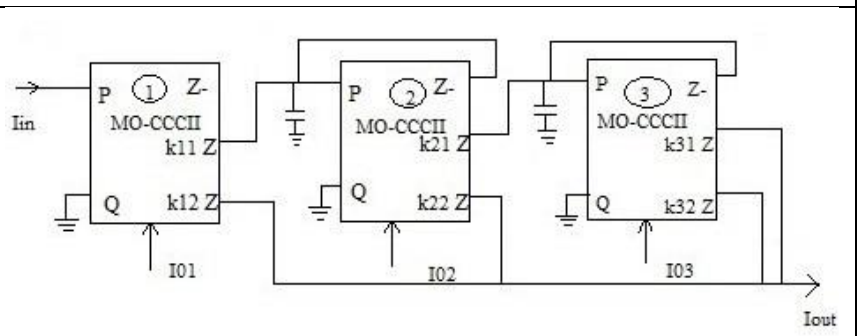
+ $f_{12}\; k_{11}(f_{33} - a_3 - b_3\, sC_3R_{x3})$ + $f_{13}\, k_{11}k_{21}$

So that by putting value of coefficients f_{ij} , a_i , b_i and k ,expression for different filters can be provided. The most important coefficients is feedback coefficient, which decides the feedback connection of the structure , also it should be noted that f_{11} and a_1 cannot be simultaneously zero or 1 as it will reduce the first feed forward equation to zero . . Value of f_{ij} can be found out by just observing the structure .So the 12 structure possible for the above multiple loop feedback current mode filter structure employing feedback and feed forward cascaded three MO-CCCII and two grounded capacitances shown in fig 3.3 which are taken from reference [7]. The below are the 12 structure possible ,each structure having four possible topologies making it 48 structure in total are shown below with the structure number and condition on f_{ij} and a_1 for each structure [7]

Table 1 Various Structures generated by Proposed Configration in[7]

Structure	Condition on f_{ij} and a_1	Schematic configration
I	$a_1=f_{12}=f_{13}=1$ other $f_{ij}=0$	
II	$f_{11}=f_{12}=f_{13}=1$ $a_1=0$ other $f_{ij}=0$	
III	$f_{11}=f_{12}=f_{23}=1$ $a_1=0$ other $f_{ij}=0$	

IV	$a_1=f_{12}=f_{23}=1$ $f_{11}=0$ other $f_{ij}=0$	
V	$f_{11}=f_{12}=f_{33}=1$ $a_1=0$ other $f_{ij}=0$	
VI	$a_1=f_{12}=f_{33}=1$ $f_{11}=0$ other $f_{ij}=0$	
VII	$f_{11}=f_{22}=f_{13}=1$ $a_1=0$ other $f_{ij}=0$	

VIII	$a_1=f_{22}=f_{13}=1$ $f_{11}=0$ other $f_{ij}=0$	
IX	$f_{11}=f_{22}=f_{23}=1$ $a_1=0$ other $f_{ij}=0$	
X	$a_1=f_{22}=f_{23}=1$ $f_{11}=0$ other $f_{ij}=0$	
XI	$f_{11}=f_{22}=f_{33}=1$ $a_1=0$ other $f_{ij}=0$	
XII	$a_1=f_{22}=f_{23}=1$ $f_{11}=0$ other $f_{ij}=0$	

3.4 SIMULATION:

In this section , the port relationship of MO-CCCII are verified using PSPICE simulation . The simulation are carried out with MO-CCCII implemented in AMS .35µm CMOS technology with power supply of 2.5V supply and biasing current I_0 of 100 µA .The schematic internal circuit of basic block of MO-CCCII can be shown below in fig3.4 with two input terminal X and Y and four output terminals i.e two Z+ and two Z -.

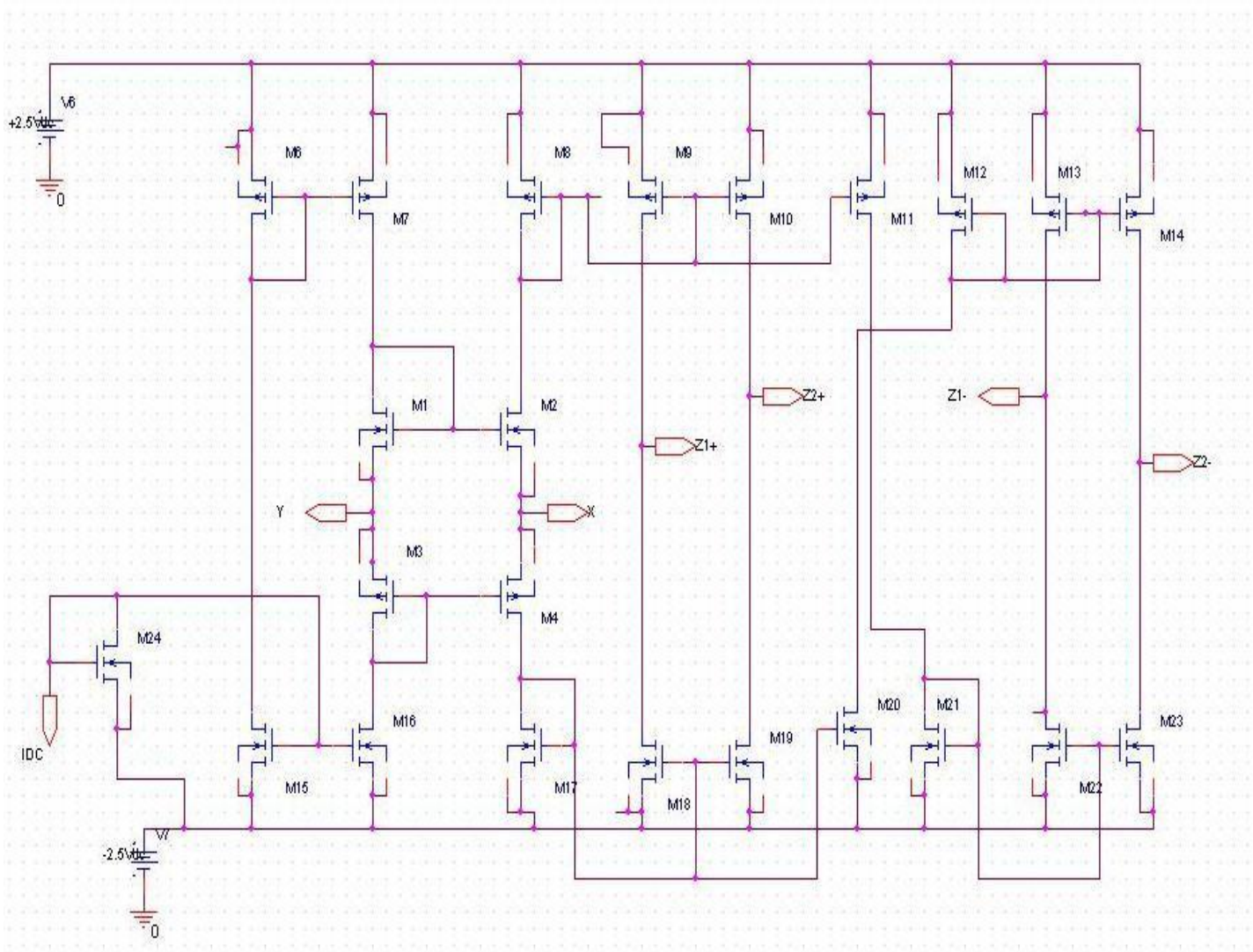


Fig3.4 SCHEMATIC INTERNAL STRUCTURE OF MO-CCCII

In the above shown internal circuit I_{DC} represent the terminal for the biasing current I_0 . The circuit is used to verify the three defining equations for the MO-CCCII which are

$$I_Y = 0 , \; I_{Z-} = - I_X , I_{Z+} = I_X$$

So now the above circuitry is taken into basic block form of MO-CCCII with six terminals i.e two input and four output as

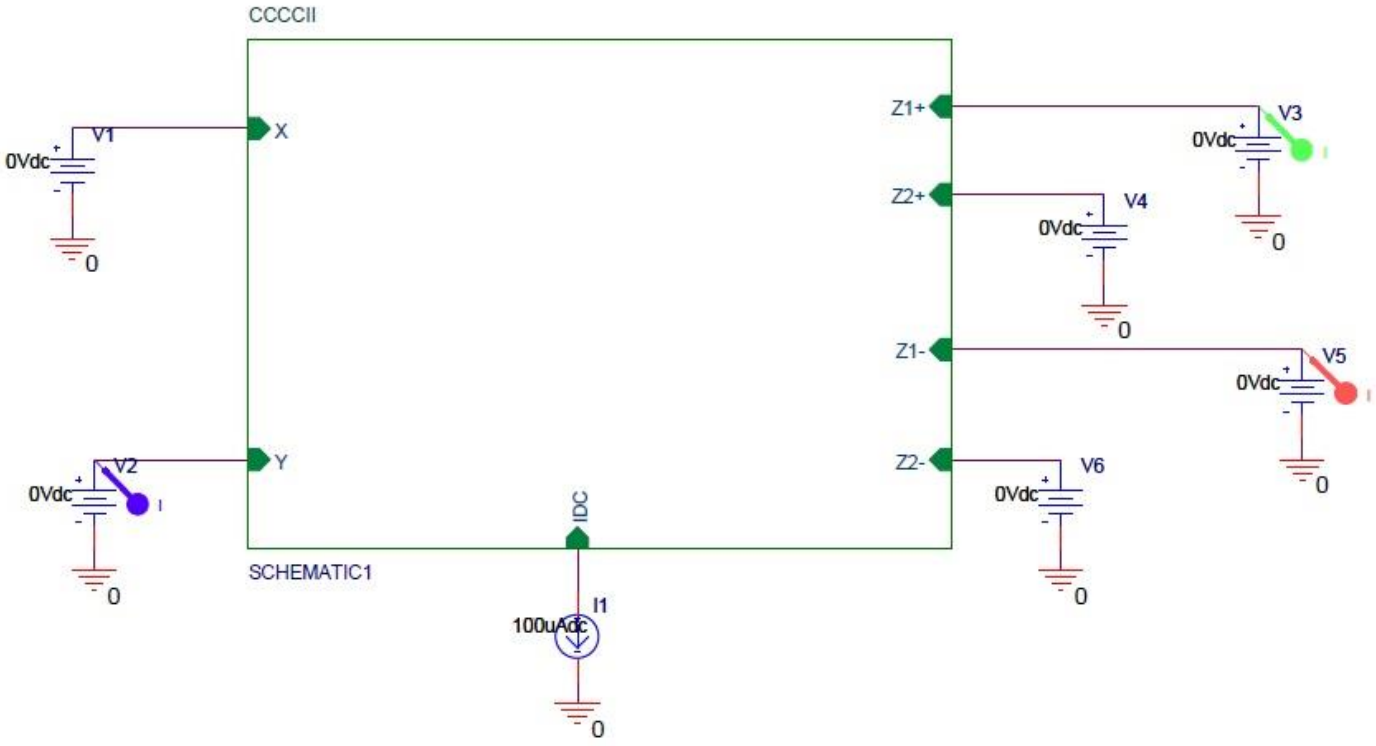


Fig3.5 Schematic block diagram of MO-CCCII

Now in the above block diagram markers have been placed at three terminal i.e one at terminal Y to verify $I_Y = 0$ and two other at output terminal Z+ and Z- , to verify that they will have equal value of currents but will have opposite polarity . The biasing current is taken as 100 μA .

The results obtained using PSPICE schematic can be shown as

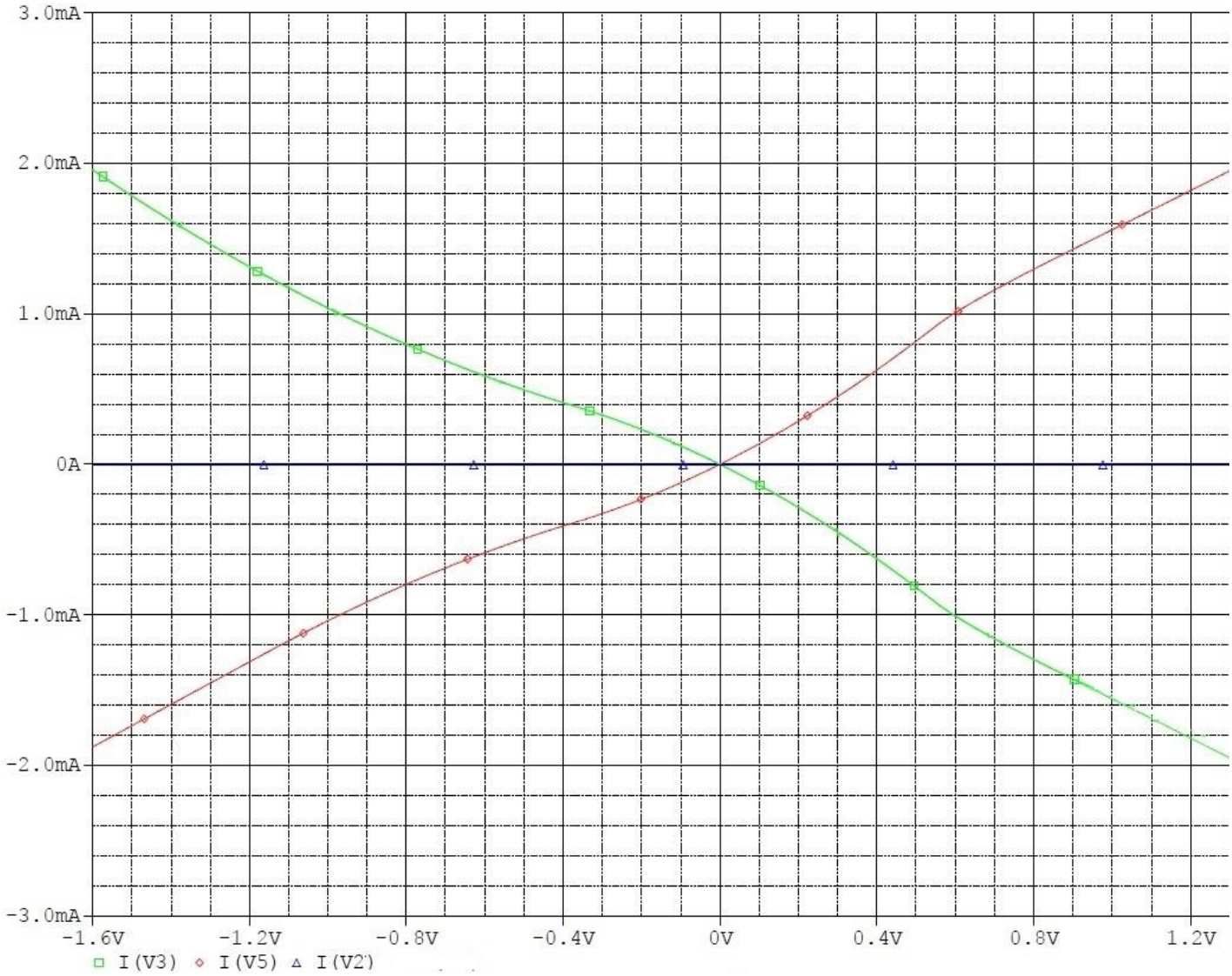


Fig3.6 Simulated port relationship $I_Y = 0$, $I_{Z-} = -I_X$, $I_{Z+} = I_X$

The above figure shows the graph of relationship between different terminals shown by the markers and defining equations has been verified , after that , biasing current is varied and effect of I_0 is taken on the graph which is shown in fig 3.7 as

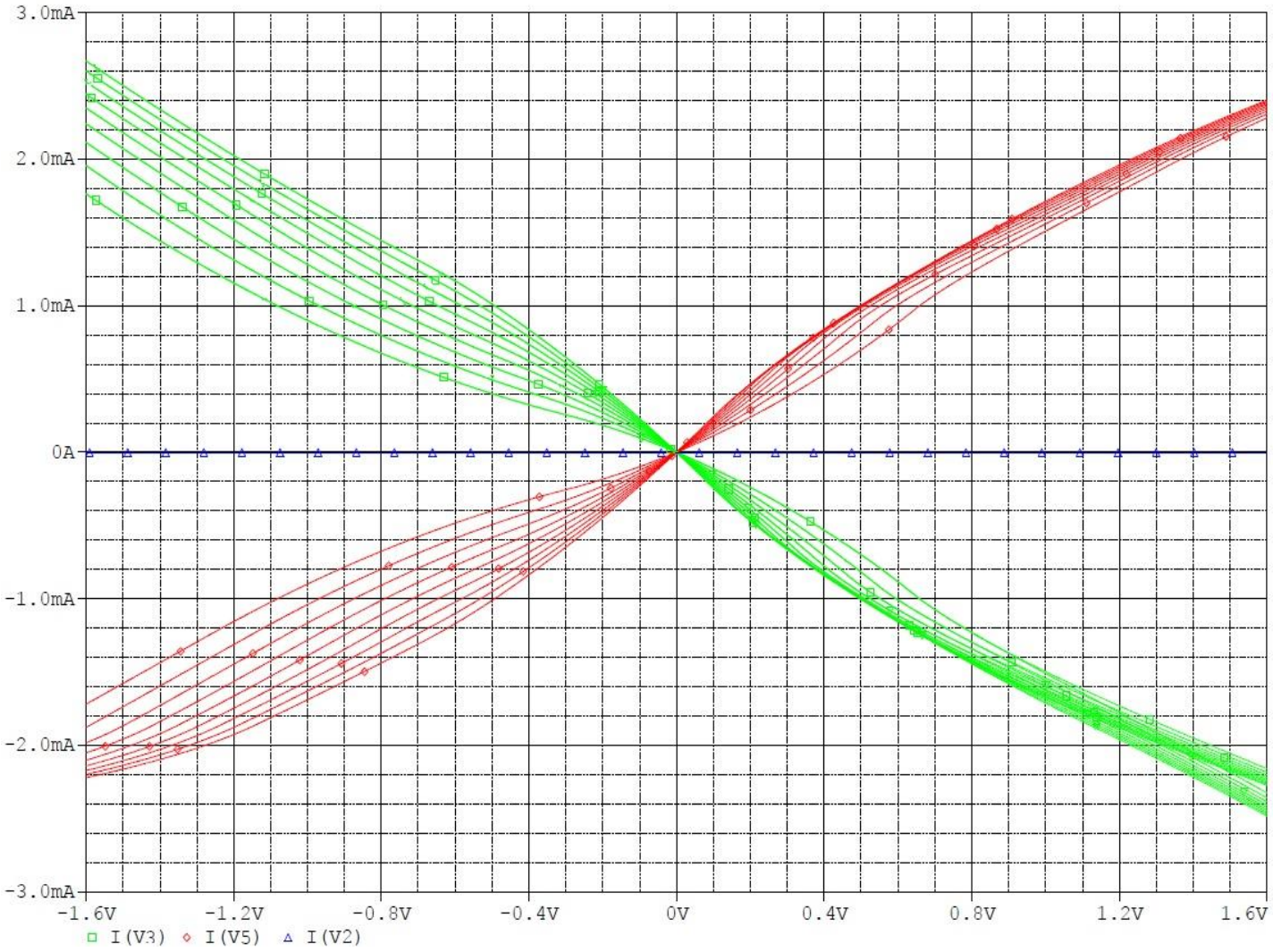


Fig3.7 Simulated port relationship with varying biasing current (I_0)

By above graph it can be concluded that effect of biasing current is more at initial voltages and as the voltages increases the effect become less.

3.4.1 Transfer function of current mode filter (I/I) :

In the equation (1) , the ratio of output current(I_{OUT}) to the input current (i_{in}) is given which is derived in [7] as

$$\frac{I_{OUT}}{i_{in}} = -\frac{N(s)}{D(s)}$$

Where

$$N(s) = k_{12}[(f_{33} - a_3 - b_3\, sC_3R_{x3})\,(f_{22} - a_2 - b_2 sC_2R_{x3}) + f_{23}k_{21}] + k_{11}k_{22}(f_{33} - a_3 - b_3\, sC_3R_{x3}) + k_{12}k_{21}(k_{31} + k_{32})$$

$$D(s) = (f_{11} - a_1)[(f_{33} - a_3 - b_3\, sC_3R_{x3})\,(f_{22} - a_2 - b_2 sC_2R_{x3}) + f_{23}\, k_{21}]$$

$$+ f_{12}\, k_{11}(f_{33} - a_3 - b_3\, sC_3R_{x3}) + f_{13}\, k_{11}k_{21}$$

The above equation is verified through simulation .For verification one of the 12 structures is to be considered and among the structure one of the four topologies is to be considered. In this section STRUCTURE I and topology A is taken into consideration . The defining equation for structure 1 is

$$a_1 = f_{12} = f_{13} = 1$$

other $f_{ij} = 0$

So the above expression get reduced to

$$\frac{I_{OUT}}{i_{in}} = \frac{k_{12}(a_3 + b_3\, sC_3R_{x3})(a_2 + b_2 sC_2R_{x3}) - k_{11}k_{22}(a_3 + b_3\, sC_3R_{x3}) + k_{12}k_{21}(k_{31} + k_{32})}{(a_3 + b_3\, sC_3R_{x3})(a_2 + b_2 sC_2R_{x3}) + k_{11}(a_3 + b_3\, sC_3R_{x3}) - k_{11}k_{21}}$$

After selecting the structure 1 , its topology A is considered . For topology A the value of a_2 = a_3 = 0 and b_2 = b_3 = -1 . The above expression get further reduced to

$$\frac{I_{OUT}}{i_{in}} = \frac{k_{12}(s^2C^2R_{x3}R_{x2})+k_{11}k_{22}(sCR_{x3})+k_{12}k_{21}(k_{31}+k_{32})}{(a_3+b_3\,sC_3R_{x3})(a_2+b_2sC_2R_{x3})+k_{11}(a_3+b_3\,sC_3R_{x3})-k_{11}k_{21}}$$

From the above expression , almost all types of filters can be realized by changing the values of coefficient k . Considering k_{11} = -1 and k_{21} = 1 , the schematic block diagram of above defined structure is

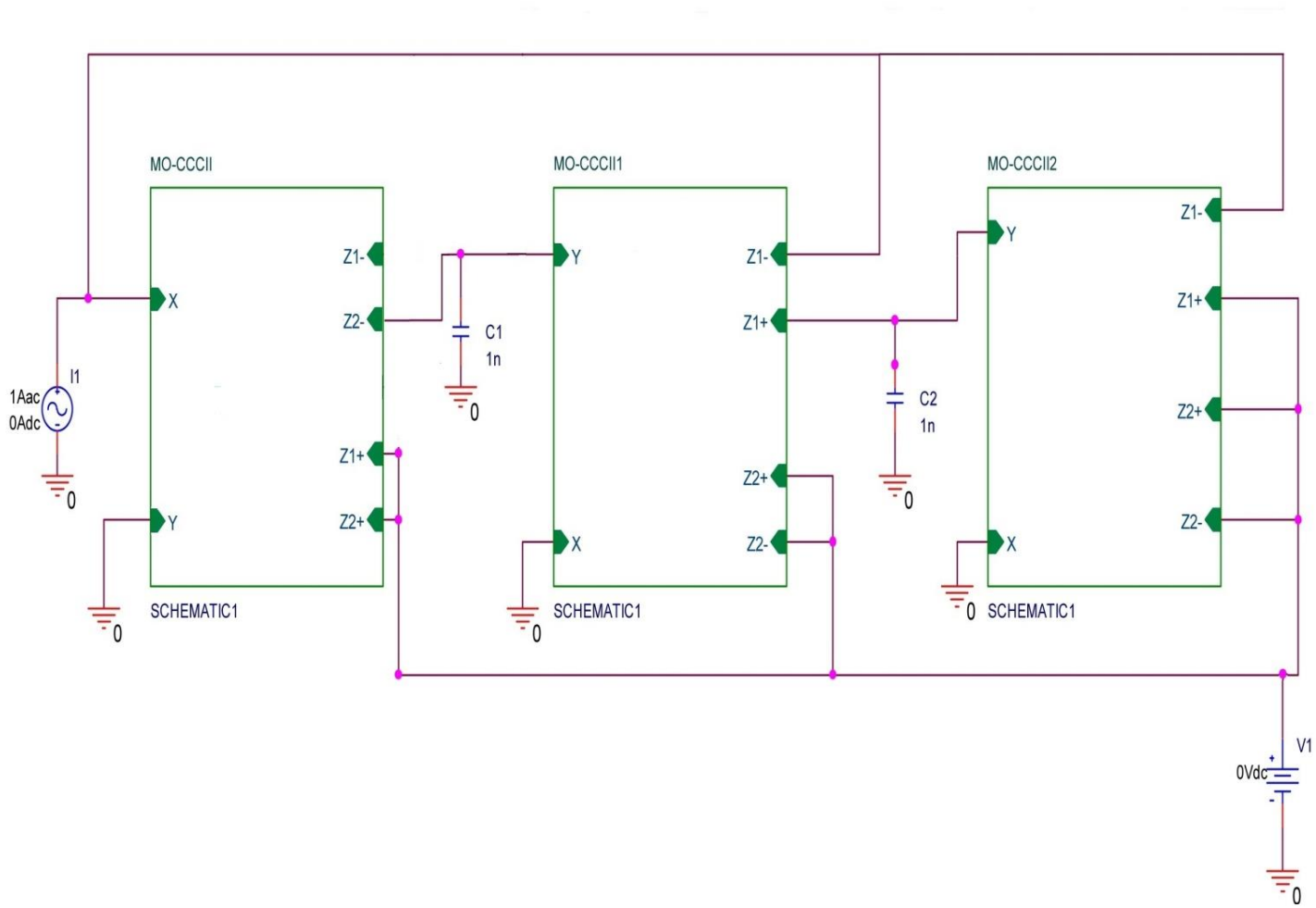


Fig 3.8 Schematic block diagram of structure I and topology A

Different filters can be generated using fig 3.8 depending on the value of different coefficient k . As the value of coefficient k changes the above schematic structure changes and at node V1 , the value output current (I_{OUT}) is considered .So taking different filters by modifying the values of coefficient k as

3.4.1.1 Low pass realization : For low pass realization value of k considered as $k_{12} = k_{22} = k_{32} = 0$ $k_{31} = -1$[7] . The schematic block diagram and simulation results accordingly are as follows

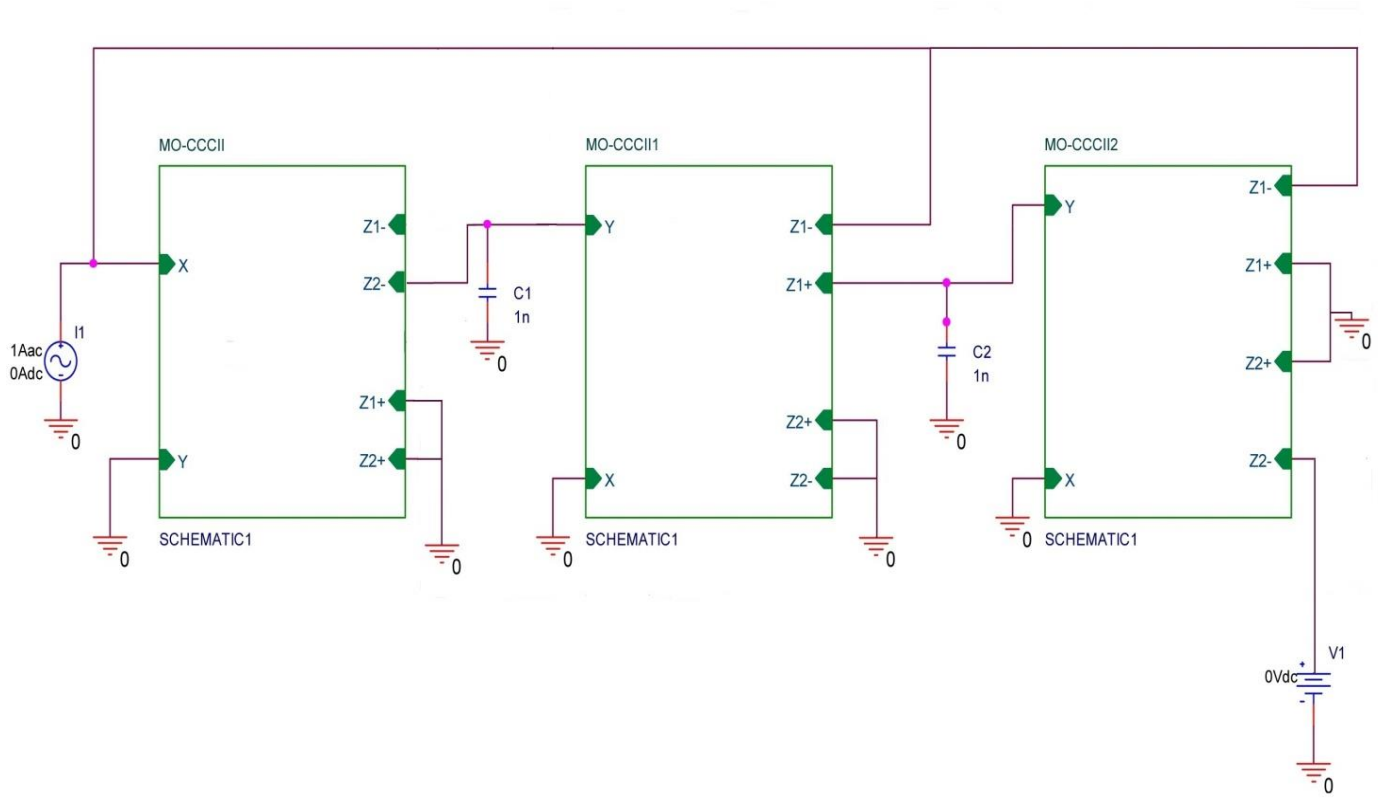


Fig 3.9 Schematic block diagram of structure I and topology A for low pass filter

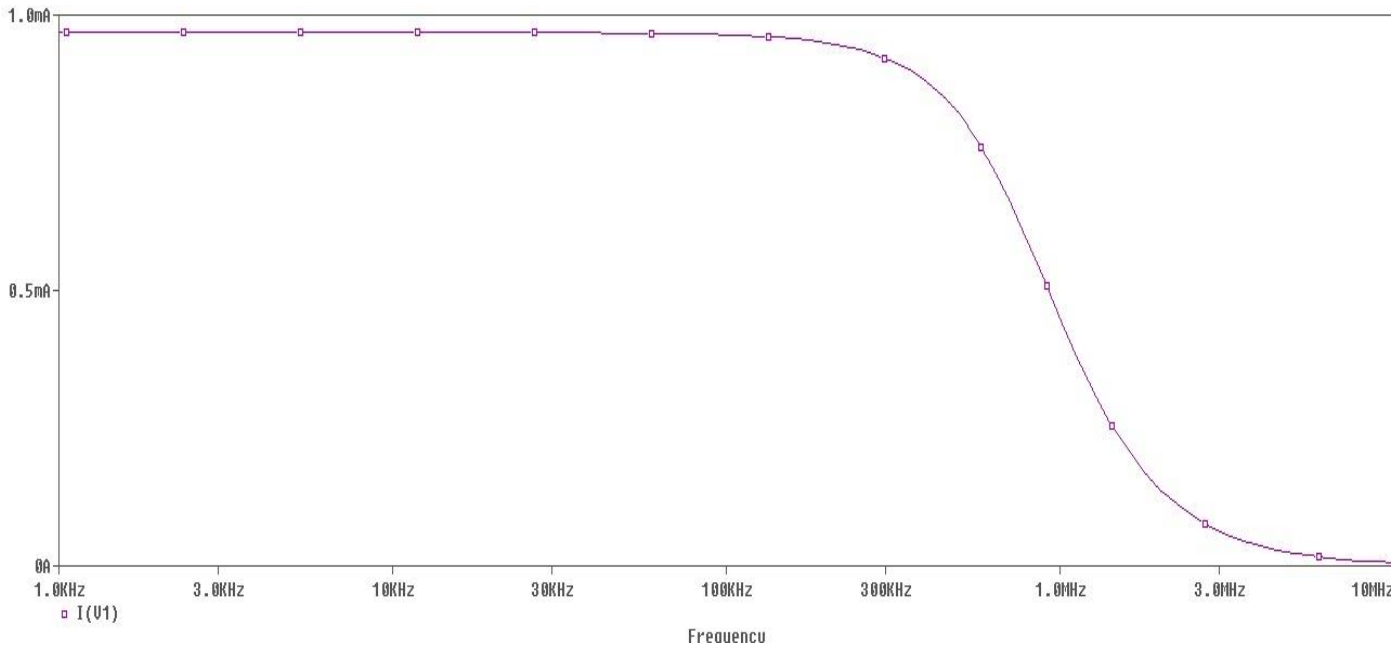


Fig 3.10 Graph of simulated structure I showing the low pass filter

3.4.1.2 Band pass realization : For low pass realization value of k considered as $k_{12} = k_{32} = k_{31} = 0$, $k_{22}=1$[7]. The schematic block diagram and simulation results accordingly are as follows

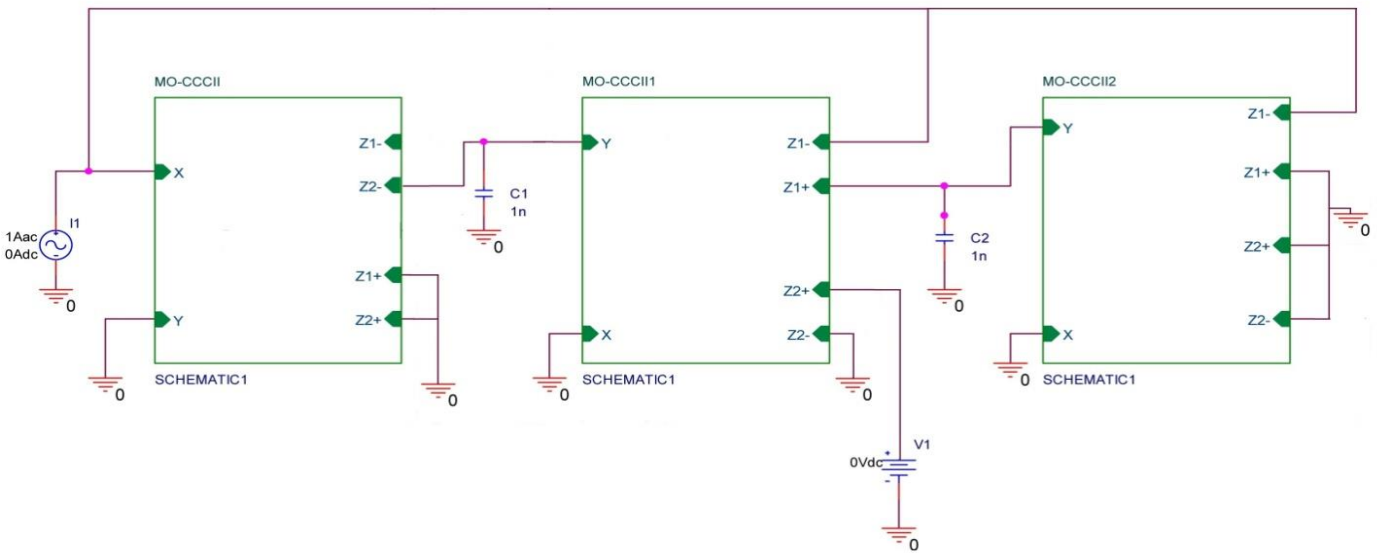


Fig 3.11 Schematic block diagram of structure I and topology A for band pass filter

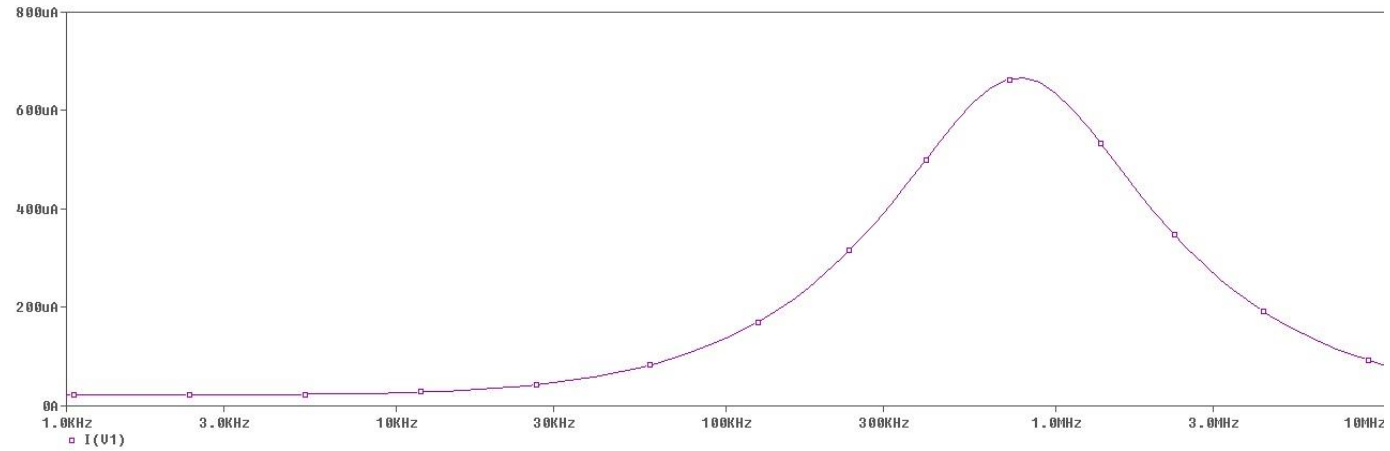


Fig 3.12 Graph of simulated structure I showing the band pass filter

3.4.1.3 High pass realization : For low pass realization value of k considered as $k_{12} = 1$ $k_{32} = k_{31} = 0$, $k_{22}=0$ [7]. The schematic block diagram and simulation results accordingly are as follows

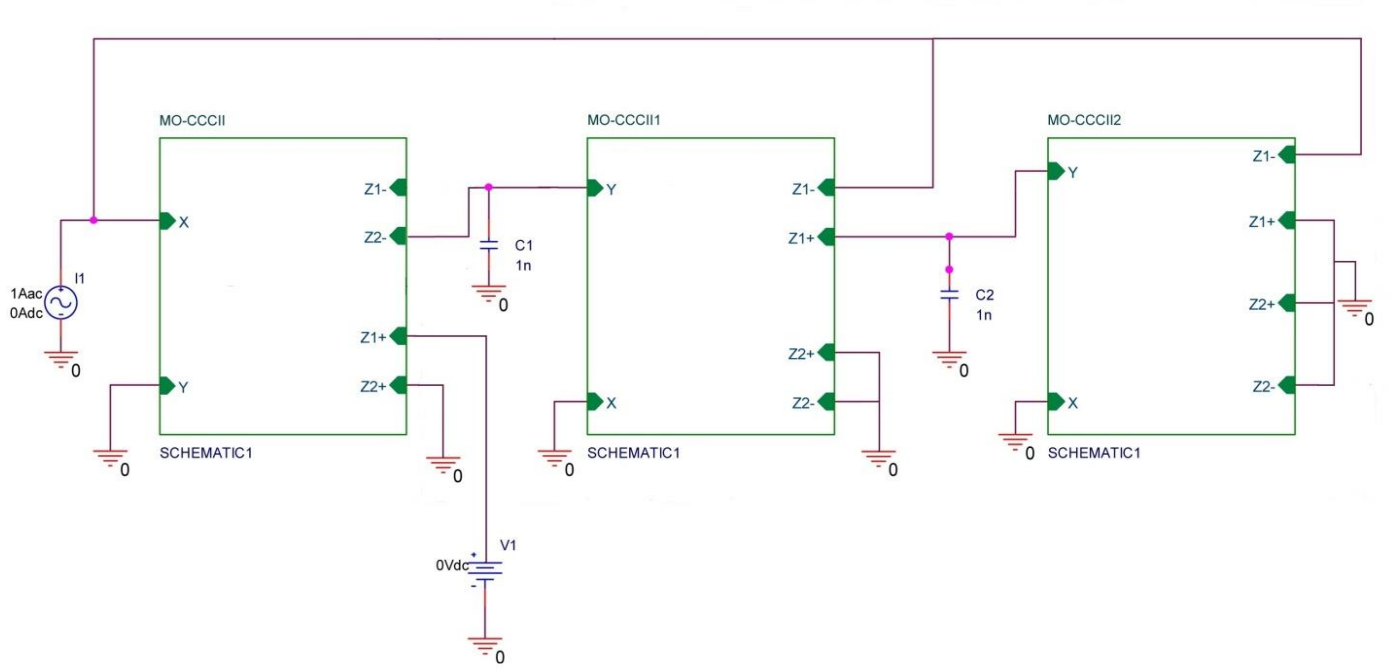


Fig 3.13 Schematic block diagram of structure I and topology A for high pass filter

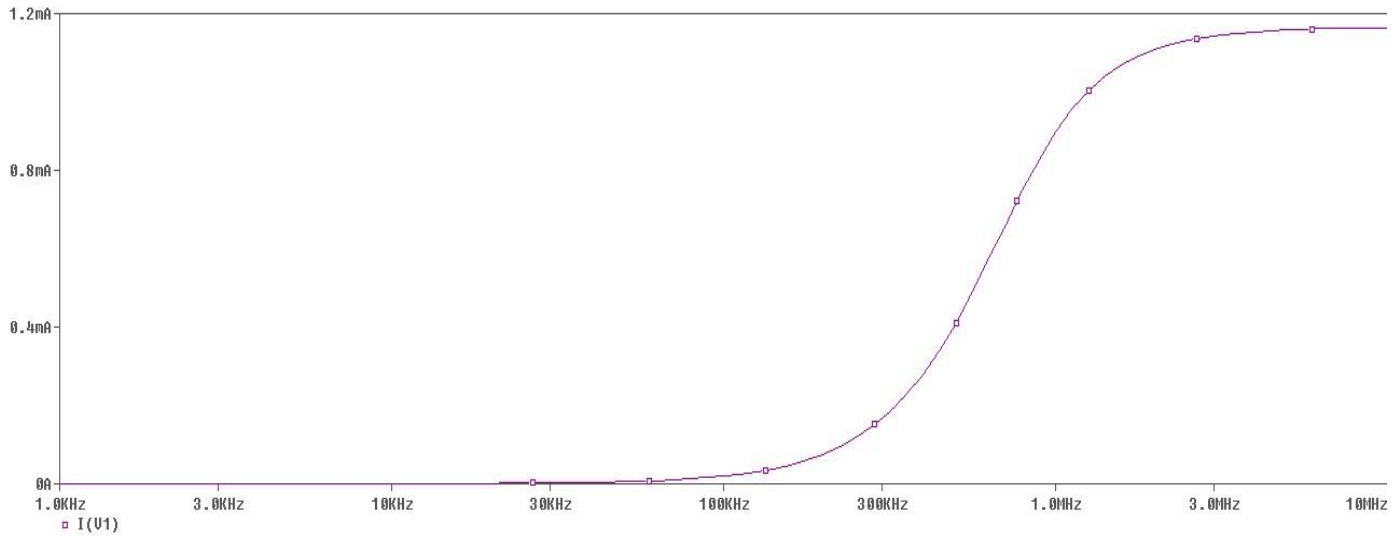


Fig 3.14 Graph of simulated structure I showing the high pass filter

3.4.1.4 Notch realization : For low pass realization value of k considered as $k_{12} = 1$ $k_{32} = k_{22}=0$,$k_{31} = -1$[7]. The schematic block diagram and simulation results accordingly are as follows

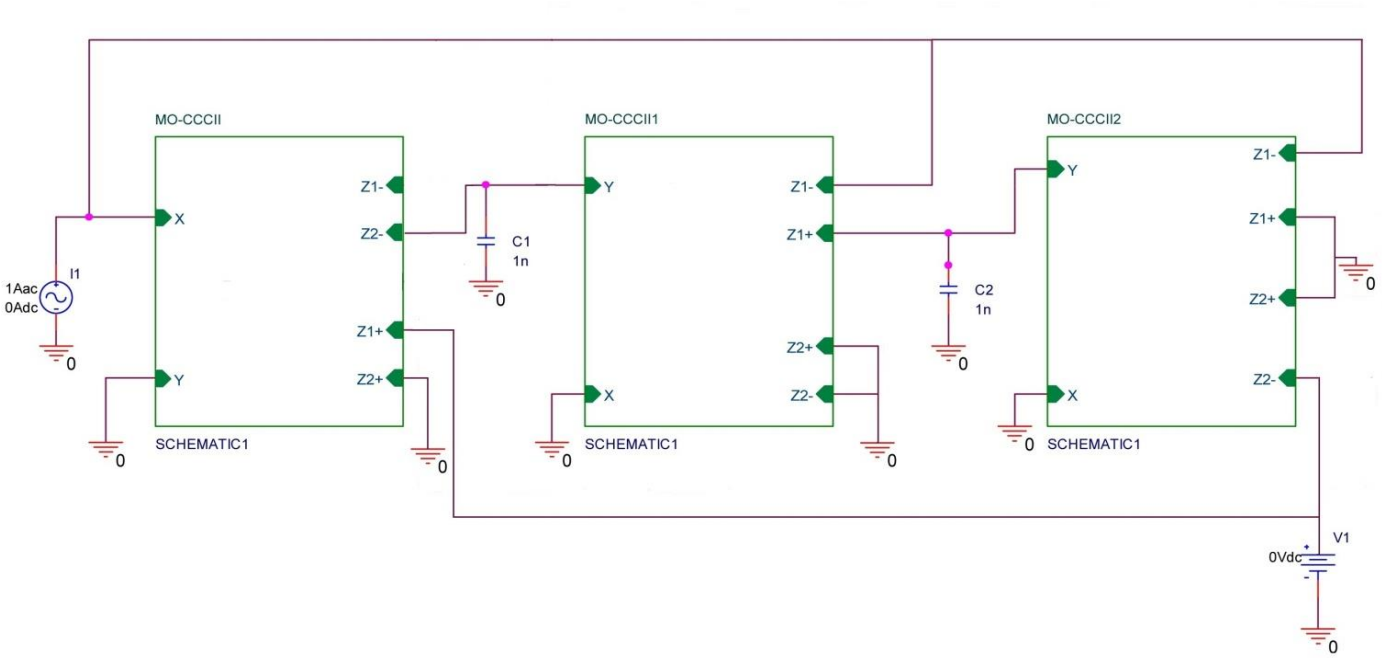


Fig 3.15 Schematic block diagram of structure I and topology A for notch filter

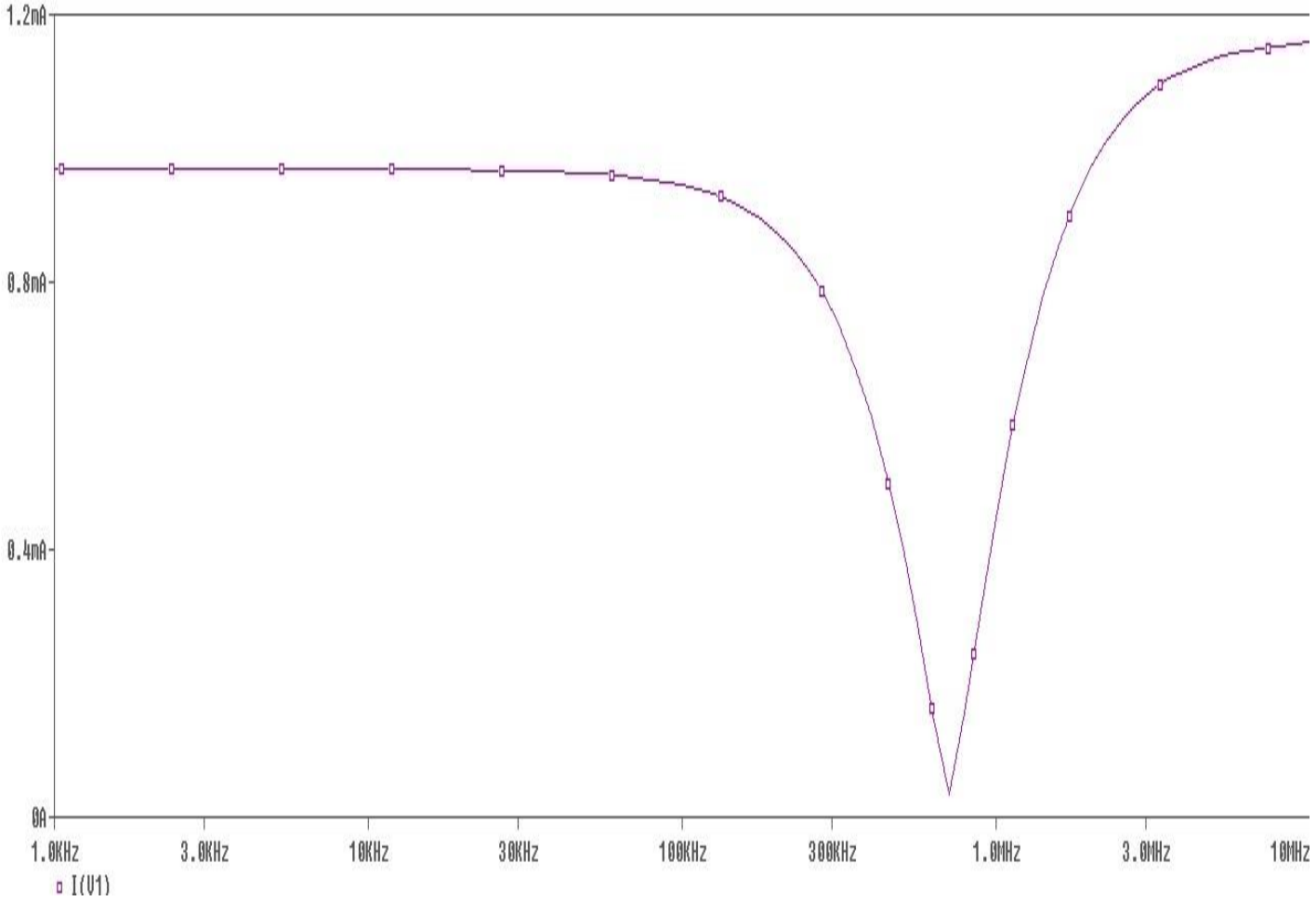


Fig 3.16 Graph of simulated structure I showing the notch filter

The above schematic block diagram and graph results are verified using PSPICE

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CHAPTER 4

Transresistance mode filter

This chapter examines the basic structure of multiple loop feedback transresistance mode filter employing three MO CCCII and two ground capacitors and its different coefficients.For transresistance mode of operation , the general expression between the different node voltage and the input current has been derived and the filter synthesis results are verified by simulating one such structure using PSPICE simulation .

4.1 THEORY :

The generalized multiple loop feedback MO-CCCII based filter model with all capacitors grounded[1] is shown in fig 4.1. Three blocks of MO-CCCII have been used with each block having the port relationship as shown below.

$$V_X = V_Y + i_X|R_{Xi}(I_{0i})|$$

$$i_Y = 0 , \; i_{Z-} = - i_X , \; i_{k_{i1}Z} = k_{i1} i_X , \; i_{k_{i2}Z} = k_{i2} i_X$$

where k_{i1} and $k_{i2} = \pm 1$ and $i = 1, 2, 3$. $R_{Xi} = {}^{V_T}/_{2I_{0i}}$ is bias current dependence resistance , V_T is thermal voltage , I_{0i} is bias current of CCCII [3].

To get MO-CCCII , simply current mirrors are inserted at the output of CCCII.

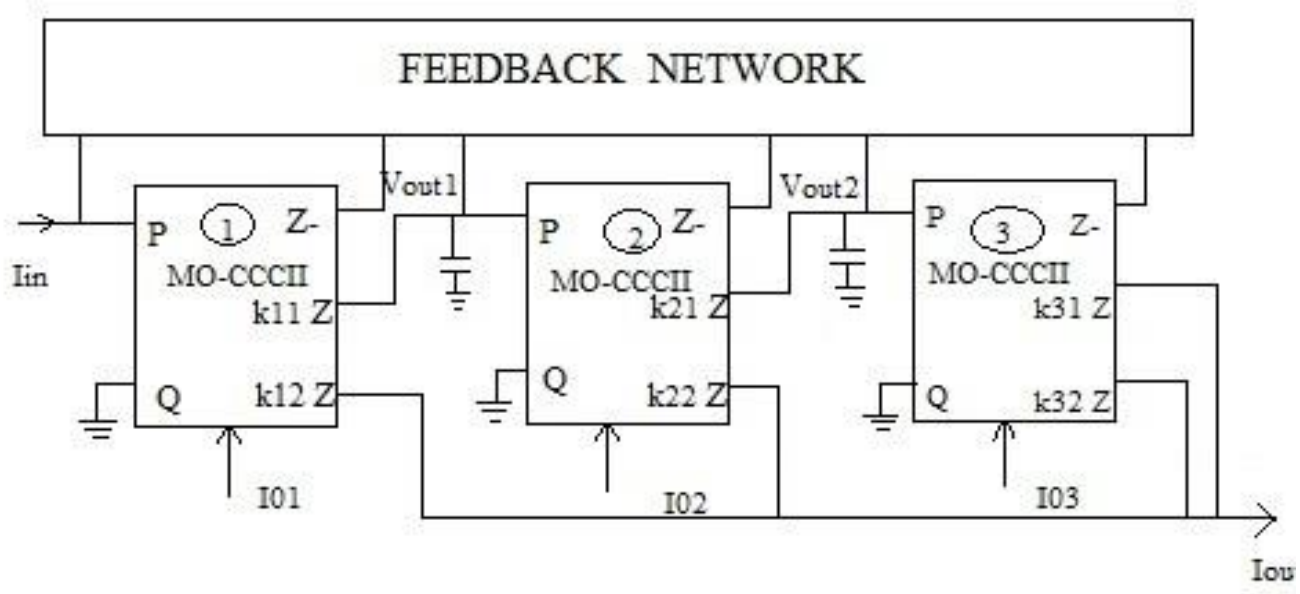

Fig4.1 Multiple loop feedback transresistance mode filter structure[1]

where notation P and Q is used instead of X and Y [1]and the direction of current flowing through the feedback or feed forward depends upon the values of k_{i0}, k_{i1} and k_{i2}.Current flowing into or out of CCCII depends upon filtering function[1].

4.2 General expression representing relation between i_{in} and node voltage V_{OUT1} :

As shown in the fig4.1 there is feedback network which is connected to one output terminal of multiple output system and other output are feed forwarded such that the shown fig 4.1 can be divided into two parts . One is feedback network and other is feed forward network .The basic feed back network can be shown by the equation as

$$I_{fi}=\sum_{j=1}^{3} f_{ij}\, I_{Xj} \qquad i = 1 , 2 , 3 \qquad (1)$$

Where f_{ij} is the current feedback coefficient from output of j^{th} MO-CCCII to the input of i^{th} MO-CCCII .The value of f_{ij} can have zero or unity depending upon whether there is open circuited or direct feedback connection between i^{th} and j^{th} MOCCCII . Now if the value of f_{ij} is zero that means no feedback and if f_{ij} is unity that means feedback[1] . So

representing in the current form such that I_{fi} is the current at the input of the i^{th} MO-CCCII and I_{xj} is the output current from j^{th} MO-CCCII. The above equation (1) can be also represented as

$$I_f = F\, I_x \qquad (2)$$

where $I_f=[i_{f1}\, i_{f2} i_{f3}]^T$, the feedback current matrix , $I_x = [i_{x1}\, i_{x2} i_{x3}]^T$, the output current matrix and $F = [f_{ij}]_{3*3}$, the feedback coefficient matrix . The superscript T represents transpose[1] . It may be noted that $f_{21} = f_{31} = f_{32} = 0$, being non – feedback coefficients.

As there are three MO-CCCII so there will be three equation which represents the feed forward network which can be shown as [1]

$$i_i + i_{f1} = a_1\, i_{x1} \qquad (3)$$

$$k_{11}\, i_{x1} + sC_2 V_{P2} + a_2\, i_{x2} = i_{f2} \qquad (4)$$

$$k_{21} i_{x2} + sC_3 V_{P3} + a_3\, i_{x3} = i_{f3} \qquad (5)$$

where notation a_i represents whether the current is flowing into the input of MO-CCCII or not . So its value can be 0 or 1, zero if the input is Y terminal and 1 if the input terminal is X as defined in the block equation earlier that $i_y = 0$.Now notation Vpi represents the node voltages at the capacitor[1]. As explained earlier the equation

$$V_X = V_Y + i_X |R_{Xi}(I_{0i})|$$

But in the condition shown in the basic block diagram that from two input terminal , one is grounded such that in that condition the node voltage at the input which can be represented as $V_P i$ has the equation

$$V_{Pi} = b_i\, i_{xi} R_{xi} \qquad (6)$$

Where V_{P2} and V_{P3} is taken as V_{OUT1} and V_{OUT2} respectively

Where value of notation b_i can be either 1 or -1 depending on whether the input is connected to the X terminal or Y terminal which can be found out by the value of a_i.So if the value of $a_i = 1$ means input is connected to terminal X and $b_i = 1$ if $a_i = 0$ then input to the MO-CCCII is connected to Y terminal means $b_i = -1$ [1]. Now modifying the equation (4) and (5) according to the equation (6), they becomes

$$k_{11}\, i_{x1} + sC_2 V_{OUT1} + a_2 V_{OUT1}/b_2\, R_{x2} = i_{f2} \tag{7}$$

$$k_{21}\, V_{OUT1}/b_2\, R_{X2} + sC_3 b_3 i_{x3} R_{x3} + a_3\, i_{x3} = i_{f3} \tag{8}$$

Now representing the equation (3) , (7) and (8) in the matrix form as

$$\begin{bmatrix} i_{f1} \\ i_{f2} \\ i_{f3} \end{bmatrix} = \begin{bmatrix} a_1 & 0 & 0 \\ k_{11} & (sC_2 + {}^{a_2}/_{b_2 R_{x2}}) & 0 \\ 0 & {}^{k_{21}}/_{b_2 R_{x2}} & (a_3 + b_3\, sC_3 R_{x3}) \end{bmatrix} \begin{bmatrix} i_{x1} \\ V_{OUT1} \\ i_{x3} \end{bmatrix} - \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} i_{in} \tag{9}$$

Subtraction of equation (9) from (2) gives

$$-\begin{bmatrix} f_{11} - a_1 & f_{12} & f_{13} \\ -k_{11} & f_{22} - (sC_2 + {}^{a_2}/_{b_2 R_{x2}}) & f_{23} \\ 0 & -{}^{k_{21}}/_{b_2 R_{x2}} & f_{33} - (a_3 + b_3\, sC_3 R_{x3}) \end{bmatrix} \begin{bmatrix} i_{x1} \\ V_{OUT1} \\ i_{x3} \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} i_{in}$$

$$\begin{bmatrix} i_{x1} \\ V_{OUT1} \\ i_{x3} \end{bmatrix} = -\begin{bmatrix} f_{11} - a_1 & f_{12} & f_{13} \\ -k_{11} & f_{22} - sC_2 - {}^{a_2}/_{b_2 R_{x2}} & f_{23} \\ 0 & -{}^{k_{21}}/_{b_2 R_{x2}} & f_{33} - a_3 - b_3\, sC_3 R_{x3} \end{bmatrix}^{-1} \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} i_{in}$$

Since $f_{21} = f_{31} = f_{32} = 0$

$$\begin{bmatrix} i_{x1} \\ V_{OUT1} \\ i_{x3} \end{bmatrix} = - D^{-1}(s) .I.i_{in}$$

$$\begin{bmatrix} i_{x1} \\ V_{OUT1} \\ i_{x3} \end{bmatrix} = -\frac{1}{|D(s)|}\begin{bmatrix} [f_{22} - sC_2 - {a_2}/{b_2 R_{x2}}][f_{33} - a_3 - b_3\, sC_3 R_{x3}] + \frac{f_{23}k_{21}}{b_2 R_{x2}} \\ k_{11}[f_{33} - (a_3 + b_3\, sC_3 R_{x3})] \\ k_{11}\, {k_{21}}/{b_2 R_{x2}} \end{bmatrix} i_{in}$$

So that final equation for the node voltage V_{OUT1} and i_{in}

$$\frac{V_{OUT1}}{i_{in}} = \frac{-k_{11}[f_{33} - (a_3 + b_3\, sC_3 R_{x3})]}{|D(s)|}$$

Where $|D(s)| = (f_{11} - a_1)[[f_{22} - sC_2 - {a_2}/{b_2 R_{x2}}][f_{33} - a_3 - b_3\, sC_3 R_{x3}] + \frac{f_{23}k_{21}}{b_2 R_{x2}}]$

$+ f_{12}[\, k_{11}[f_{33} - (a_3 + b_3\, sC_3 R_{x3})] + f_{13}k_{11}\, {k_{21}}/{b_2 R_{x2}}$

4.3 Relation between different terminal currents and input current :

The general expression between node voltage 2 (V_{OUT1}) and the input current has been derived such that if the value of node voltage is taken into consideration and values are put in the three feed forward equation , values of different node current with respect to input current can also be calculated as

$$\frac{i_{x1}}{i_{in}} = \frac{-[f_{22}-sC_2-{}^{a_2}/_{b_2R_{x2}}][f_{33}-a_3-b_3\,sC_3R_{x3}]+\frac{f_{23}k_{21}}{b_2R_{x2}}}{|D\,(s)|}$$

$$\frac{i_{x2}}{i_{in}} = \frac{-k_{11}[f_{33}-(a_3+b_3\,sC_3R_{x3})]}{b_2R_{x2}|D\,(s)|}$$

$$\frac{i_{x3}}{i_{in}} = \frac{-k_{11}k_{21}}{b_2R_{x2}|D\,(s)|}$$

Where $|D\,(s)|$represents the determinant of the matrix D(s) . The k_{12} , k_{22} , k_{31} and k_{32} can take values 1 , 0 , -1 indicating current flowing into , no current flow in the output and current flowing out of MO-CCCII respectively .

4.4 General expression representing relation between i_{in} and node voltage V_{OUT2} :

In this section generalized expression of ratio of node voltage 3rd (V_{OUT1}) to the input current i_{in} is derived . The feedforward equation (3) remains the same and equation (4) and (5) are modified .So node voltage at node 2 i.e V_{OUT1} is written as $b_2\,i_2\,R_{X2}$ and node voltage at node 3 is written as it is i.e V_{OUT2} . So they are modified as

$$k_{11}\,i_{x1} + sC_2b_2i_{x2}R_{x2} + a_2\,i_{x2} = i_{f2}$$

$$k_{21}i_{x2} + sC_3V_{OUT2} + \frac{a_3V_{OUT2}}{b_3R_{X3}} = i_{f3}$$

Now writing them into matrix form same as above

$$\begin{bmatrix} i_{f1} \\ i_{f2} \\ i_{f3} \end{bmatrix} = \begin{bmatrix} a_1 & 0 & 0 \\ k_{11} & (a_2 + sC_2b_2R_{x2}) & 0 \\ 0 & k_{21} & (sC_3 + \frac{a_3}{b_3R_{x3}}) \end{bmatrix} \begin{bmatrix} i_{x1} \\ i_{x2} \\ V_{OUT2} \end{bmatrix} - \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} i_{in}$$

repeating the above followed procedure

$$\begin{bmatrix} i_{x1} \\ i_{x2} \\ V_{OUT2} \end{bmatrix} = -\begin{bmatrix} f_{11} - a_1 & f_{12} & f_{13} \\ -k_{11} & f_{22} - a_2 - b_2sC_2R_{x2} & f_{23} \\ 0 & -k_{21} & f_{33} - sC_3 - \frac{a_3}{b_3R_{x3}} \end{bmatrix}^{-1} \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} i_{in}$$

$$\begin{bmatrix} i_{x1} \\ i_{x2} \\ V_{OUT2} \end{bmatrix} = -\frac{1}{|D_1(s)|} \begin{bmatrix} [f_{22} - a_2 - b_2sC_2R_{x2}][f_{33} - sC_3 - \frac{a_3}{b_3R_{x3}}] + k_{21}f_{23} \\ k_{11}[f_{33} - \left(sC_3 + \frac{a_3}{b_3R_{x3}}\right)] \\ k_{11}k_{21} \end{bmatrix} i_{in}$$

So finally the relation comes out to be

$$\frac{V_{OUT2}}{i_{in}} = \frac{-k_{11}k_{21}}{|D_1(s)|}$$

Where $|D_1(s)| = (f_{11} - a_1)[f_{22} - a_2 - b_2sC_2R_{x2}][f_{33} - sC_3 - \frac{a_3}{b_3R_{x3}}] + k_{21}f_{23}]$

$+ f_{12}[k_{11}[f_{33} - \left(sC_3 + \frac{a_3}{b_3R_{x3}}\right)]] + f_{13}k_{11}k_{21}$

4.5 Coefficients and their characteristic :

There are various coefficients that are used in the above expressions i.e feedback coefficients (f_{ij}) or a_i or b_i whose values decide the type of structure and further , type of filter that can be designed . But these coefficients have certain characteristic and relationship with other coefficients so that care should be taken to decide their values .

4.5.1 Feedback coefficients (f_{ij}) : These coefficients are represented by equation(2) . In the notation f_{ij} , i represents the input of the corresponding MO-CCCII and j represents the output of corresponding MO-CCCII, such that f_{ij} as whole represents the feedback from output of j^{th} MO-CCCII to the input of i^{th} MO-CCCII. As discussed earlier , i and j value can be 1 ,2 or 3 as three blocks are used and f_{ij} value can be either 1 or 0 depending on whether feedback is present or not , that's why , three components of F matrix i.e $f_{21} = f_{31} = f_{32}$ have zero values , such that , the matrix F can be seen as upper triangular matrix .To maintain unity feedback , the feedback matrix should have one and only one non-zero (unity) element in each column .There is one to one correspondence between feedback matrix F and circuit configuration and different F lead to different circuit structures , such that there is interconnection between component of F matrix and coefficient a_i i.e either $f_{11} = 1$ or $a_1 = 1$.Hence there are 2*3! Different combinations ,thus , 12 different filter structure are possible with three blocks[7].

4.5.2 Coefficient a_i : This coefficient represents whether the current is flowing into i^{th} MO-CCCII input terminal or not. It can take values 1 or 0 depending upon the input terminal of the respective MO-CCCII . If the input is going to X terminal then $a_i=1$ and if Y terminal than $a_i=0$. There are three blocks , first one is for the input and the last two blocks there is feed forward from previous block such that it can be into X terminal or Y terminal which decides the value of a_2 and a_3 ,so, there can be four set possible with each structure , so that , the total number of structure is increased to 48.

4.5.3 Coefficient b_i : This coefficient is defined for the node voltages and its value depends on the value of a_i .As defined earlier , expression for node voltage as $V_{Pi} = b_i i_{xi} R_{xi}$ where b_i can either be 1 or -1 depending on the value of a_i .If a_i =1 then $b_i = 1$ and if $a_i = 0$ then $b_i = -1$.

4.5.4 Coefficients k_{im} : These coefficient represents whether current is flowing into the block or outward the block or no current flows , at the output terminals of each block .In the notation k_{im} , i stands for the i^{th} MO-CCCII block where i = 1,2,3 and m stands for them m^{th} output terminal of the corresponding block where m = 0 , 1 ,2 . Its value can be 1 (for inward flow) , 0 (no current flow) ,-1(for outward flow).Till now there are 48 structures but depending on the values of k_{im} more topologies can be formed.

4.6 FILTER SYNTHESIS :

As the general expression between i_{in} and V_{OUT1} and between i_{in} and V_{OUT2} is derived so now expression are verified in various structure by putting values of feedback coefficients f_{ij} and values of coefficients k is selected , such that , some valid filter expression can be derived[1] . After selecting the particular structure ,values of feedback coefficients and a_1 and b_1 can be generated easily by merely observing the structure and each structure further will have four topologies depending on the combinations of values of a_2 and a_3 [1].

Now for consideration let take structure III whose block diagram is shown below in fig 4.2

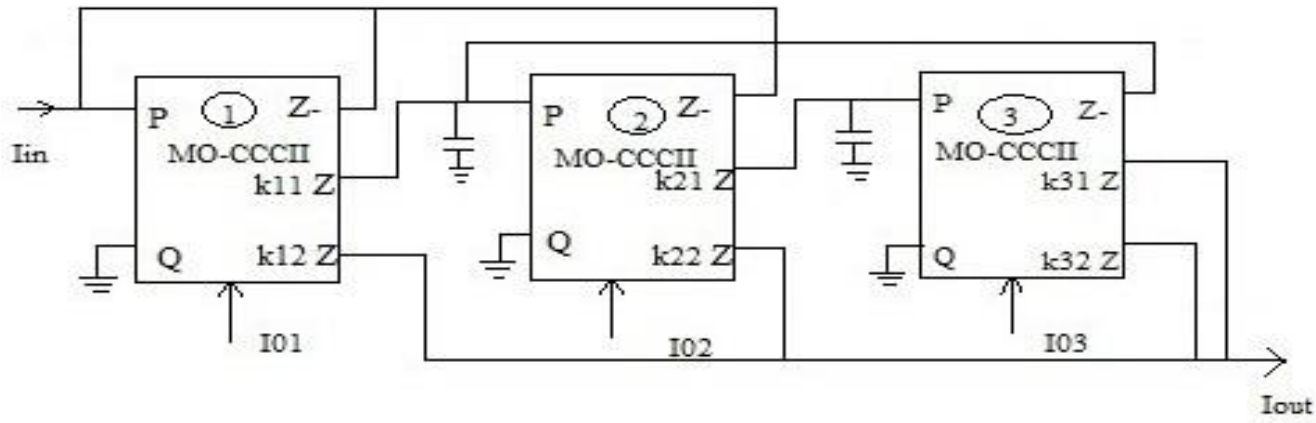

Fig 4 .2 **Block diagram of structure III**

So according to the structure values of different coefficients are

, $f_{11} = f_{12} = f_{23} = 1$, $a_1 = 0$

Other $f_{ij} = 0$

As derived the general expression for relation between I_{IN} and V_{OUT1} is

$$\frac{V_{OUT1}}{i_{in}} = \frac{-k_{11}[f_{33}-(a_3+b_3\, sC_3R_{x3})]}{|D(s)|}$$

Where $|D(s)| = (f_{11} - a_1)[[f_{22} - sC_2 - {}^{a_2}/_{b_2R_{x2}}][f_{33} - a_3 - b_3\, sC_3R_{x3}] + \frac{f_{23}k_{21}}{b_2R_{x2}}]$

$+ f_{12}[\, k_{11}[f_{33} - (a_3 + b_3\, sC_3R_{x3})] + f_{13}k_{11}\, {}^{k_{21}}/_{b_2R_{x2}}$

So after putting the above coefficients the expression reduced to

$$\frac{V_{OUT1}}{i_{in}} = \frac{-k_{11} b_2 R_{x2}(a_3 + b_3 sC_3 R_{x3})]}{[b_2 sC_2 R_{x2} + a_2][a_3 + b_3 sC_3 R_{x3}] - k_{11}(a_3 b_2 R_{x2} + b_3 b_2 sC_3 R_{x2} R_{x3}) + k_{21}}$$

So from the above expression it can be inferred that value of coefficient is either 1 or -1 such that the only type of filter that is possible is band pass filter whatever the value of coefficient k is chosen .

TOPOLOGY –A : In this topology , P terminal of both 2nd and 3rd MO-CCCII block is taken as Y and Q as X terminal i.e. $a_2 = 0$, $a_3 = 0$, $b_2 = -1$, $b_3 = -1$ and considering the value $k_{11} = -1$ and $k_{21} = +1$, band pass filter can be realized.

TOPOLOGY – B : In this topology , P terminal of 2nd MO-CCCII block is taken as X and P terminal of 3rd MO-CCCII block as Y terminal i.e $a_2 = 1$, $a_3 = 0$, $b_2 = 1$, $b_3 = -1$ and considering $k_{11} = -1$ and $k_{21} = -1$, band pass filter can be realized.

TOPOLOGY – C : In this topology , P terminal of 2nd MO-CCCII block is taken as Y and Q terminal of 3rd MO-CCCII block as X terminal i.e $a_2 = 0$, $a_3 = 1$, $b_2 = -1$, $b_3 = 1$ and considering this, no valid filter expression can be realized.

TOPOLOGY – D : In this topology , P terminal of both 2nd and 3rd MO-CCCII block is taken as X and Q as Y terminal i.e $a_2 = 1$, $a_3 = 1$, $b_2 = 1$, $b_3 = 1$ and considering this , no valid filter can be realized.

Now if the general expression of V_{OUT2} and i_{in} can be observed , then it can be realized that only low pass filter can be realized as

$$\frac{V_{OUT2}}{i_{in}} = \frac{-k_{11} k_{21}}{|D_1(s)|}$$

Where $D_1(s) = (f_{11} - a_1)[[f_{22} - sC_2b_2R_{x2} - a_2][f_{33} - \frac{a_3}{b_3R_{X3}} - sC_3] + k_{21}f_{23}]+ f_{12}[k_{11}[f_{33} - \frac{a_3}{b_3R_{X3}} - sC_3] + f_{13}k_{11}k_{21}$

4.7 FILTER CHARACTERISTIC AND EFFECT OF NON IDEALITIES

The transfer characteristic is defined by ω_0 (cut off frequency) and Q- factor such that if transfer function of structure III is taken and in that structure topology A is considered where $a_2 = a_3 = 0$, $b_2 = b_3 = -1$ then the transfer function get reduced to [1]

$$\frac{V_{OUT1}}{i_{in}} = \frac{sCR_{x2}R_{x3}}{s^2C^2R_{x2}R_{x3}+sCR_{x3}+1} \qquad (\text{ taking } C_2 = C_3 = C)$$

So that transfer function[1] is characterized by

$$\omega_0 = \left(\frac{1}{R_{x2}\,R_{x3}\,C^2}\right)^{1/2}, \quad \frac{\omega_0}{Q_0} = \frac{1}{R_{x2}\,C}, \quad Q_0 = \left(\frac{R_{x2}}{R_{x3}}\right)^{1/2}$$

But the above case is considered in ideal situations but if non idealities are considered the above results will be altered as in case of non idealities , port relations of CCCII are modified to

$$V_X = V_Y\beta + i_X|R_{Xi}(I_{0i})|$$

$$i_Y = 0\,,\; i_Z = \alpha\, i_X$$

where α and β are respectively current and voltage gains which are all equal to unity in the ideal case. In practice, they can be expressed as α =l- ε_i , $\beta = 1 - \varepsilon_V$ where $|\varepsilon_i| << 1$ and $|\varepsilon_v| << 1$. ε_i denotes the current tracking error and ε_v denotes voltage tracking error[2].

Considering the non – idealities outlined above , the denominator polynomial of above transfer function $D_1(s) = s^2C^2R_{x2}R_{x3} + sCR_{x3} + 1$ modifies to

$$s^2C^2R_{x2}R_{x3} + s\alpha_1\alpha_2\beta_2CR_{x3} + \alpha_1\alpha_2\alpha_3\beta_2\beta_3$$

Now the transfer fuctions are characterized by [1]

$$\omega_0\,|_n = \left(\frac{\alpha_1\alpha_2\alpha_3\beta_2\beta_3}{R_{x2}\,R_{x3}\,C^2}\right)^{1/2},\ \left.\frac{\omega_0}{Q_0}\right|_n = \frac{\alpha_1\alpha_2\beta_2}{R_{x2}\,C},\ Q_0\,|_n = \left(\frac{\alpha_3\beta_3R_{x2}}{\alpha_1\alpha_2\beta_2R_{x3}}\right)^{1/2}$$

ω_0 and Q_0 have to be checked for their sensitivities with respect to all the factor defined above i.e $\alpha_1, \alpha_2, \alpha_3, \beta_2, \beta_3, R_{x2}, R_{x3}, C$. Sensitivity of any term with respect to its factor can be denoted by S_B^A means sensitivity of term A with repect to its factor B .

Formula for calculating it numerically given by

$$S_B^A = \frac{B}{A}\frac{dA}{dB}$$

So checking the sensitivities of ω_0 with respect to their factors as[1]

$$S_{R_{x2}}^{\omega_0} = S_{R_{X3}}^{\omega_0} = S_{C_2}^{\omega_0} = S_{C_3}^{\omega_0} = -1/2\ ,\qquad S_{R_{X1}}^{\omega_0} = 0$$

$$S_{\alpha_1}^{\omega_0} = S_{\alpha_2}^{\omega_0} = S_{\alpha_3}^{\omega_0} = S_{\beta_2}^{\omega_0} = S_{\beta_3}^{\omega_0} = 1/2\ ,\quad S_{\beta_1}^{\omega_0} = 0$$

Now checking sensitivity of Q_0 with respect to their factors as[1]

$$-S_{\alpha_1}^{Q_0} = -S_{\alpha_2}^{Q_0} = S_{\alpha_3}^{Q_0} = -S_{\beta_2}^{Q_0} = S_{\beta_3}^{Q_0} = 1/2\,,\qquad S_{R_{x1}}^{Q_0} = S_{\beta_1}^{Q_0} = 0$$

$$S_{R_{X2}}^{Q_0} = 1/2 = S_{\beta_3}^{Q_0}\ ,\ S_{R_{X3}}^{Q_0} = -1/2$$

From the above observation it can be concluded that all the active and passive sensitivities are low and within 1 in magnitude , such that circuit can be considered as insensitive . The equation for pole frequency indicates that ω_0 can be adjusted by varying the bias current I_{03} without disturbing $\frac{\omega_0}{Q_0}$ .The ω_0 and Q_0 are orthogonally adjustable if R_{x2} and R_{x3} are simultaneously adjusted by common control bias current $I_{01} = I_{02} = I_{01}$.

4.8 SIMULATION :

In this section the above derived generalized expression is checked by putting the values of feedback coefficient for the structure and then putting values of coefficient which are topology dependent i.e coefficient a_i and b_i. After selecting one of the 12 structure and one of the topology in the given structure , reduced expression for transresistance is calculated and if any valid filter expression is derived , then it is verified through PSPICE simulation.

4.8.1 Transresistance 1 :Ratio of node voltage V_{OUT1} to the input current i_{in}

In the above case , structure III is taken into consideration for the node 2nd where voltage is $V_{OUT1}(V2(C_1))$, as mentioned earlier the reduced expression for transresistance after putting value of feedback coefficient($f_{11}=f_{12}=f_{23}=1$, $a_1=0$ other $f_{ij}=0$) becomes

$$\frac{V_{OUT1}}{i_{in}} = \frac{k_{11}b_2 R_{x2}(a_3+b_3 sC_3R_{x3})]}{[b_2sC_2R_{x2}+a_2][a_3+b_3sC_3R_{x3}]-k_{11}(a_3b_2 R_{x2}+b_3b_2sC_3R_{x2}R_{x3})+k_{21}}$$

By observing the above expression it can be easily realized that only valid filter expression for above case is band pass filter . In the given structure , consider topology B (where $a_2 = 1$, $a_3 = 0$ and $b_2 =1$, $b_3 = -1$), so expression further reduced to

$$\frac{V_{OUT1}}{i_{in}} = \frac{k_{11}\, sCR_{x3}R_{x2}}{s^2C^2R_{x3}R_{x2}+sCR_{x3}(k_{11}R_{x2}+1)+k_{21}} \qquad (\text{taking } C_2=C_3=C)$$

So from the above calculation , it can be observed clearly that it represents the band pass filter if values of k_{21} is taken as -1 and value of k_{11} is taken as -1.

Simulation results for MO-CCCII are obtained at 2.5V supply , 100 µA biasing current I_0 and 0.35 µm technology . The schematic block diagram for above is given in the fig 4.3 .

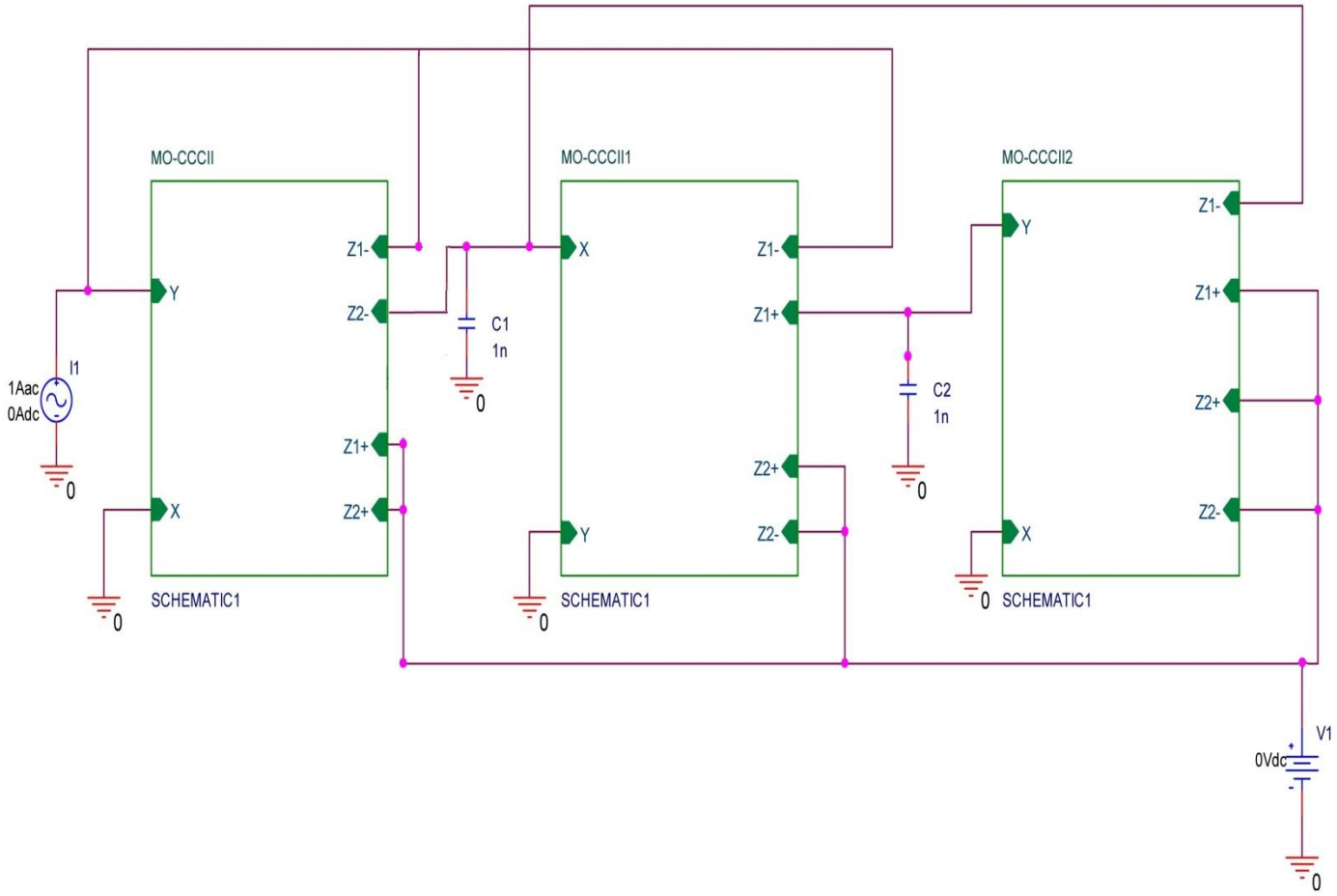

Fig 4.3 Schematic block diagram of structure III topology B

The voltage at node 2^{ND} is shown by V(N12) , as it is voltage at capacitor C_1 and the input current in form of independent current shown at terminal Y is shown by I_1.

Resultant band pass filter is realized from the above structure and the output is given as in the fig 4.4 showing graph as

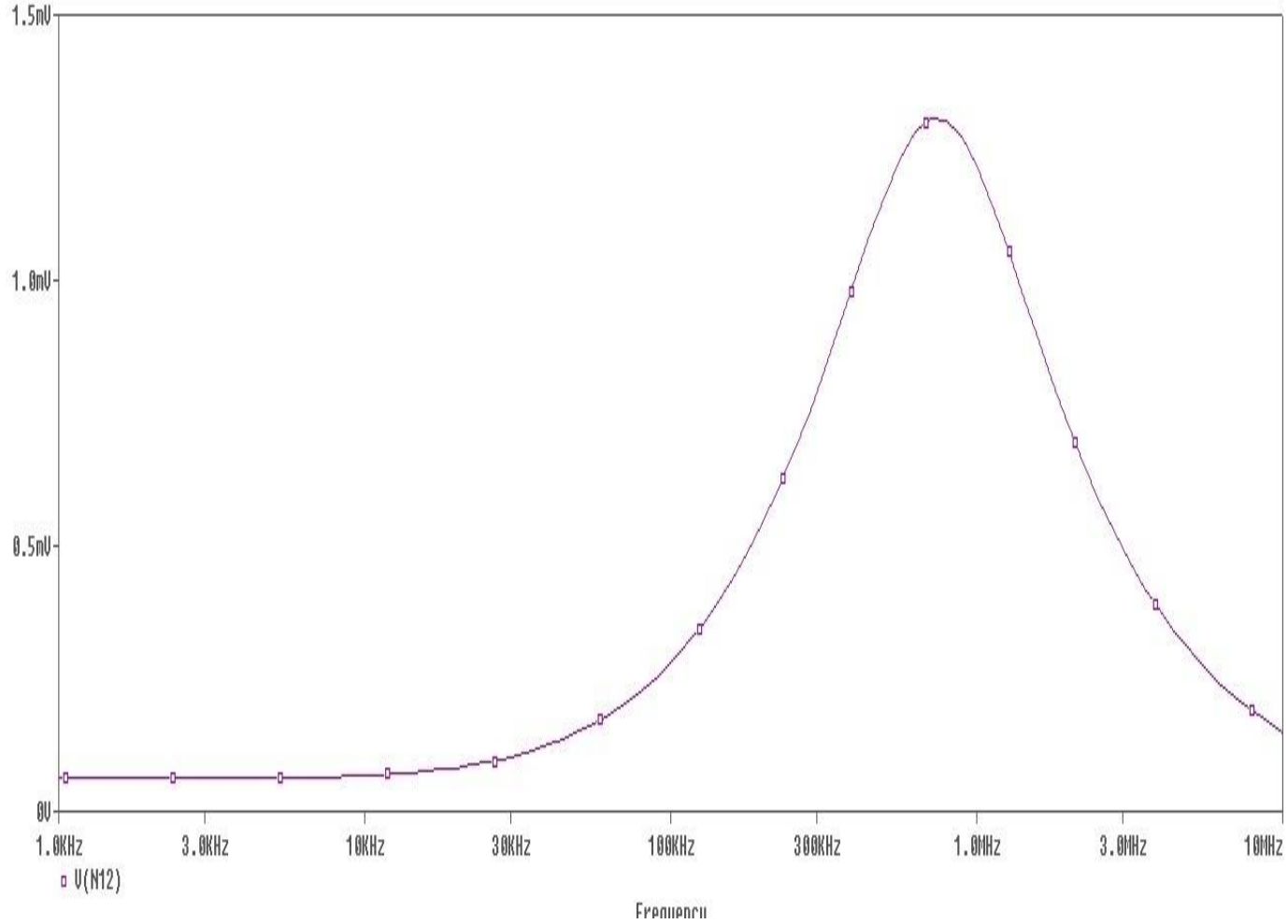

Fig 4.4 Graph of simulated structure III showing the band pass filter

So the above graph shows the transresistance relationship representing the band pass filter where voltage at node 2 (voltage at capacitor C_1) and input current at terminal Y of 1st MO-CCCII is considered . In the next section voltage at node 3 is taken and rest of the process remain the same .

4.8.2 Transresistance 2 : Ratio of node voltage V_{OUT2} to the input current i_{in}

In this case , again structure III is taken into consideration for the node 3rd where voltage is $V_{OUT2}(V3(C_2))$. The generalized expression for the transresistance of circuit with respect to the node voltage V_{OUT2} is

$$\frac{V_{OUT2}}{i_{in}} = \frac{-k_{11}k_{21}}{|D_1(s)|}$$

Where $D_1(s) = (f_{11} - a_1)[[f_{22} - sC_2b_2R_{x2} - a_2][f_{33} - \frac{a_3}{b_3R_{X3}} - sC_3] + k_{21}f_{23}]+ f_{12}[k_{11}[f_{33} - \frac{a_3}{b_3R_{X3}} - sC_3] + f_{13}k_{11}k_{21}$

If the above expression is observed , it can be inferred that only low pass filter can be realized .After putting value of feedback coefficient($f_{11}=f_{12}=f_{23}=1$, $a_1=0$ other $f_{ij}=0$) , the expression get reduced to

$$\frac{V_{OUT2}}{i_{in}} = \frac{-k_{11}k_{21}b_3R_{X3}}{[-sC_2b_2R_{x2}-a_2][-a_3-sC_3b_3R_{X3}]+k_{21}b_3R_{X3}]+k_{11}[-a_3-sC_3b_3R_{X3}]}$$

In the above expression of structure III , if the topology A is considered where coefficient

$a_2 = a_3 = 0$ and $b_2 = b_3 = -1$ and taking $k_{11}=+1$ and $k_{21} = -1$ then the above expression get reduced to

$$\frac{V_{OUT2}}{i_{in}} = \frac{1}{|s^2C^2R_{x2}+sC+1|}$$

Simulation results for MO-CCCII are obtained at 2.5V supply , 100 μA biasing current I_0 and 0.35 μm technology . Resultant low pass filter is realized from the above structure and the output is given as in the fig 4.5 showing graph as

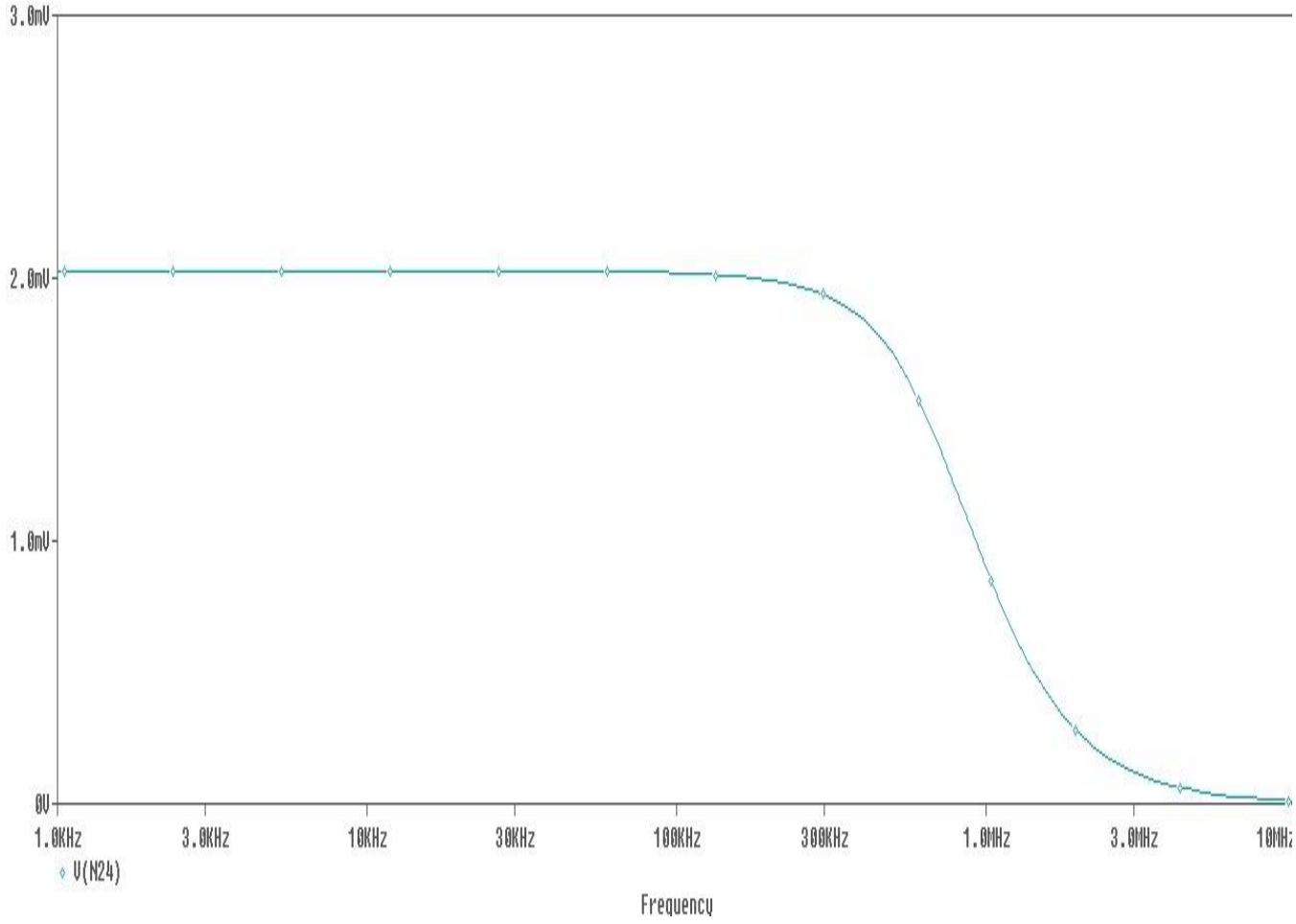

Fig 4.5 Graph of simulated structure III showing the low pass filter

So the above graph shows the transresistance relationship representing the low pass filter where voltage at node 3 (voltage at capacitor C_2) and input current at terminal Y of 1st MO-CCCII is considered .

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CHAPTER 5

Transadmittance mode filters

There are many applications in electronic circuits where voltage and current mode must be interconnected ,which is problematic situation . So to overcome these difficulties , voltage to current conveyor interface circuits(V-I) are required. During the V-I interfacing , signal processing can also be performed simultaneously which increases the total effectivity of electronic circuits[2].So keeping in mind the above advantages , in this chapter ,the generalized expression for output current to the applied input voltage (transadmittance) is derived . The filter synthesis results are verified by simulating one such structure using PSPICE simulation

5.1 General expression between I_{out} and V_{in2} :

It may be noted that , Q terminal of each block is grounded and the input is applied in the form of current source to the input terminal of 1st MO-CCCII. Now in the modified circuit , the input current source at input terminal is removed and input is applied in the form of voltage source to the earlier grounded terminal (Q terminal) of 2nd MO-CCCII .The general expression representing the relation between the output current with V_{in2} is calculated and different filter fuction have been derived by changing the various coefficients. The block diagram of transadmittance mode filter (TAM) is shown in the fig 5.1 on next page .

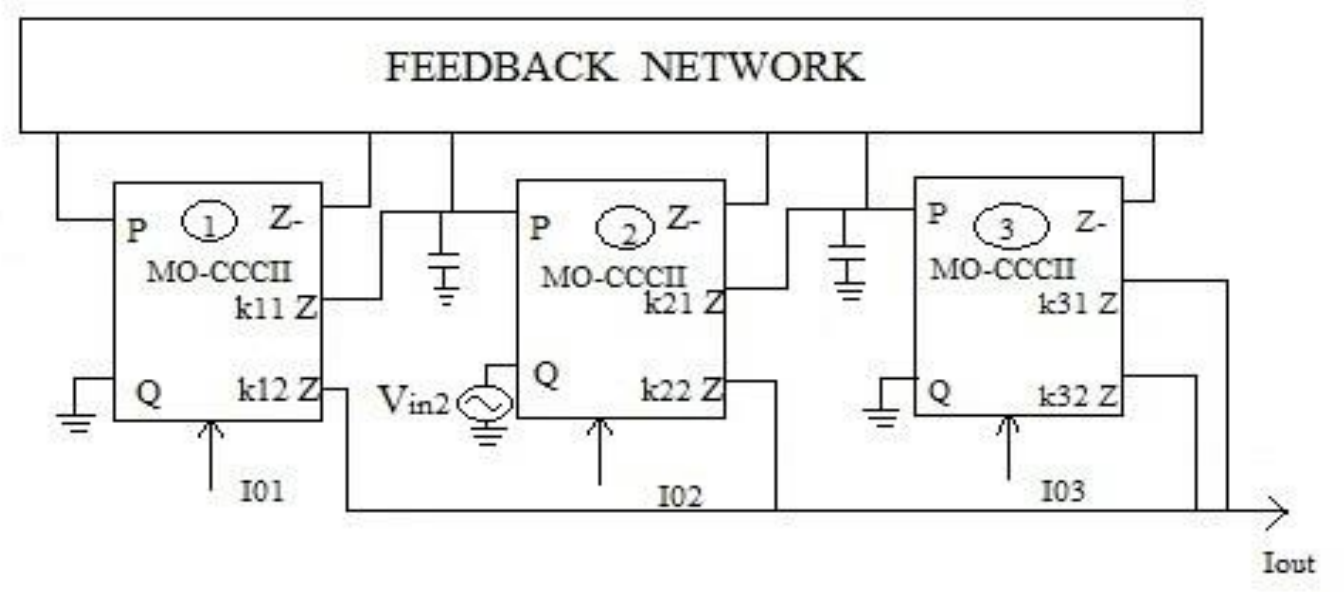

Fig 5.1 Multiple loop feedback transadmittance mode filter structure I

The general feed forward equation[2] are modified according to the above fig5.1 as

$$a_1 i_{x1} = i_{f1} \quad (1)$$

$$k_{11} i_{x1} + sC_2 V_{P2} + a_2 i_{x2} = i_{f2} \quad (2)$$

$$k_{21} i_{x2} + sC_3 V_{P3} + a_3 i_{x3} = i_{f3} \quad (3)$$

where $V_{P2} = V_{in2} + b_2 i_{x2} R_{x2}$ as per the general equation at any terminal given by

$V_X = V_Y + i_X |R_{Xi}(I_{0i})|$ and V_{p3} is given by $b_3 i_{x3} R_{x3}$, so modifying the equation (2) and (3) as

$$k_{11} i_{x1} + (sC_2 b_2 R_{x2} + a_2) i_{x2} + sC_2 V_{in2} = i_{f2}$$

$$k_{21} i_{x2} + (sC_3 R_{x3} + a3) i_{x3} = i_{f3}$$

so representing them in the matrix form

$$\begin{bmatrix} i_{f1} \\ i_{f2} \\ i_{f3} \end{bmatrix} = \begin{bmatrix} a_1 & 0 & 0 \\ k_{11} & (sC_2b_2R_{x2} + a_2) & 0 \\ 0 & k_{21} & (a_3 + b_3\, sC_3R_{x3}) \end{bmatrix} \begin{bmatrix} i_{x1} \\ i_{x2} \\ i_{x3} \end{bmatrix} + \begin{bmatrix} 0 \\ 1 \\ 0 \end{bmatrix} sC_2V_{in2} \quad (4)$$

$$I_F = F\, I_X \quad (5)$$

Subtracting equation (4) from (5)

$$\begin{bmatrix} f_{11} - a_1 & f_{12} & f_{13} \\ -k_{11} & f_{22} - a_2 - b_2sC_2R_{x3} & f_{23} \\ 0 & -k_{21} & f_{33} - a_3 - b_3\, sC_3R_{x3} \end{bmatrix} \begin{bmatrix} i_{x1} \\ i_{x2} \\ i_{x3} \end{bmatrix} = \begin{bmatrix} 0 \\ 1 \\ 0 \end{bmatrix} sC_2V_{in2}$$

$$\begin{bmatrix} i_{x1} \\ i_{x2} \\ i_{x3} \end{bmatrix} = [M(s)]^{-1} \begin{bmatrix} 0 \\ 1 \\ 0 \end{bmatrix} sC_2V_{in2}$$

$$\begin{bmatrix} i_{x1} \\ i_{x2} \\ i_{x3} \end{bmatrix} = \frac{1}{|M(s)|} \begin{bmatrix} -(f_{12}(f_{33} - a_3 - b_3\, sC_3R_{x3}) + f_{13}k_{21}) \\ (f_{11} - a_1)(f_{33} - a_3 - b_3\, sC_3R_{x3}) \\ k_{21}(f_{11} - a_1) \end{bmatrix} sC_2V_{in2}$$

So the various current equation with V_{in2} is given as

$$\frac{i_{x1}}{V_{in2}} = \frac{-sC_2(f_{12}(f_{33}-a_3-b_3\,sC_3R_{x3})+f_{13}k_{21}]}{|M(s)|} \quad \text{(a)}$$

$$\frac{i_{x2}}{V_{in2}} = \frac{sC_2(f_{11}-a_1)(f_{33}-a_3-b_3\,sC_3R_{x3})}{|M(s)|} \quad \text{(b)}$$

$$\frac{i_{x3}}{V_{in2}} = \frac{sC_2k_{21}(f_{11}-a_1)}{|M(s)|} \quad \text{(c)}$$

As we know from the block diagram

$I_{out} = k_{12}\, i_{x1} + k_{22}\, i_{x2} + (\, k_{31} + k_{32})i_{x3}$

$$\frac{I_{out}}{V_{in2}} = \frac{N(s)}{|M(s)|}$$

Where

$N(s) = sC_2[-k_{12}(f_{12}(f_{33} - a_3 - b_3\, sC_3R_{x3}) + f_{13}k_{21}) + k_{22}(f_{11} - a_1)(f_{33} - a_3 - b_3\, sC_3R_{x3}) + (k_{31} + k_{32})(k_{21}(f_{11} - a_1)]$

And $|M(s)| = (f_{11} - a_1)[(f_{33} - a_3 - b_3\, sC_3R_{x3})\,(f_{22} - a_2 - b_2sC_2R_{x2}) + f_{23}\, k_{21}]$

$+\ f_{12}\ k_{11}(f_{33} - a_3 - b_3\, sC_3R_{x3})\ +\ f_{13}\, k_{11}k_{21}$

5.2 General expression between I_{out} and V_{in3} :

Similar procedure have been followed for the input voltage source applied at the grounded terminal of 3rd MO-CCCII named as V_{in3} but there is small change in the matrix equation (3)

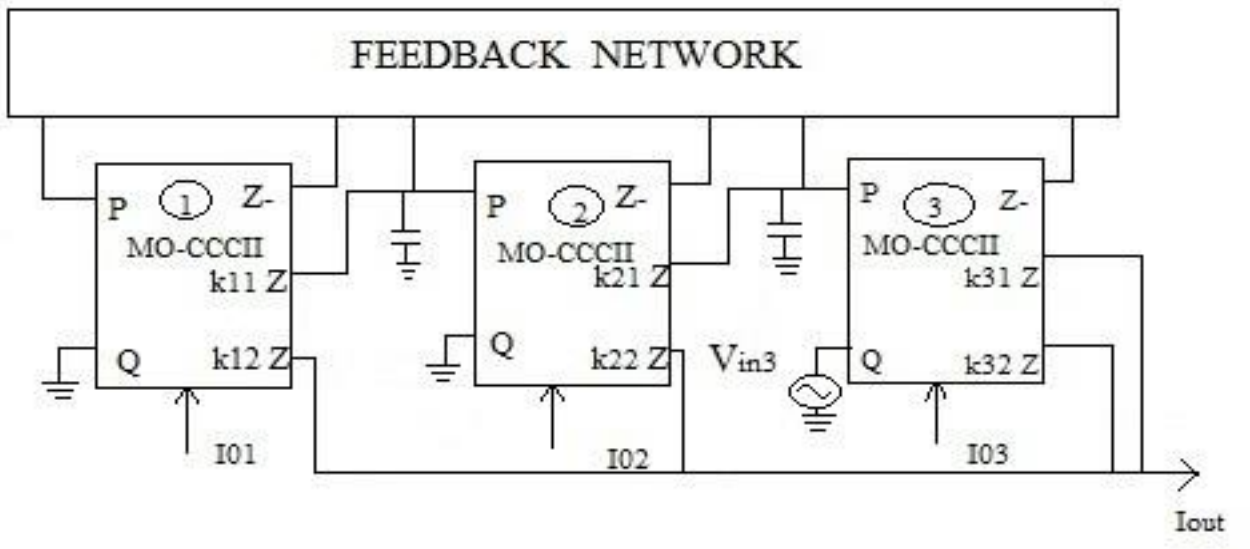

Fig 5.2 Multiple loop feedback transadmittance mode filter structure II

Rewriting the equation(3) as

$$k_{21}i_{x2} + (b_3sC_3R_{x3} + a_3)i_{x3} + sC_3V_{in3} = i_{f3}$$

Rewriting the matrix

$$\begin{bmatrix} i_{f1} \\ i_{f2} \\ i_{f3} \end{bmatrix} = \begin{bmatrix} a_1 & 0 & 0 \\ k_{11} & (sC_2b_2R_{x2} + a_2) & 0 \\ 0 & k_{21} & (a_3 + b_3\, sC_3R_{x3}) \end{bmatrix} \begin{bmatrix} i_{x1} \\ i_{x2} \\ i_{x3} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 1 \end{bmatrix} sC_3V_{in3}$$

After the subtraction of above matrix from equation (4) and taking inverse as done earlier the final matrix becomes

$$\begin{bmatrix} i_{x1} \\ i_{x2} \\ i_{x3} \end{bmatrix} = \frac{1}{|M(s)|}\begin{bmatrix} f_{12}f_{23} - f_{13}(f_{22} - a_2 - b_2sC_2R_{x2}) \\ -[(f_{11} - a_1)f_{23} + k_{11}f_{13}] \\ (f_{11} - a_1)(f_{22} - a_2 - b_2sC_2R_{x2}) + k_{11}f_{12} \end{bmatrix} sC_3V_{in3}$$

$$\frac{i_{x1}}{V_{in3}} = \frac{sC_3[f_{12}f_{23} - f_{13}(f_{22} - a_2 - b_2sC_2R_{x2})]}{|M(s)|} \quad (d)$$

$$\frac{i_{x2}}{V_{in3}} = \frac{-sC_3[(f_{11} - a_1)f_{23} + k_{11}f_{13}]}{|M(s)|} \quad (e)$$

$$\frac{i_{x3}}{V_{in3}} = \frac{sC_3[(f_{11} - a_1)(f_{22} - a_2 - b_2sC_2R_{x2}) + k_{11}f_{12}]}{|M(s)|} \quad (f)$$

Now putting the above three equation in the equation given below

$I_{out} = k_{12}\, i_{x1} + k_{22}\, i_{x2} + (k_{31} + k_{32})i_{x3}$

The final expression becomes

$$\frac{I_{out}}{V_{in3}} = \frac{H(s)}{|M(s)|}$$

Where

$$H(s) = sC_3\{k_{12}[f_{12}f_{23} - f_{13}(f_{22} - a_2 - b_2sC_2R_{x2})] - k_{22}[(f_{11} - a_1)f_{23} + k_{11}f_{13}]$$
$$+ (k_{31} + k_{32})[(f_{11} - a_1)(f_{22} - a_2 - b_2sC_2R_{x2}) + k_{11}f_{12}]\}$$

5.3 FILTER SYNTHESIS

As the general expression for relation between I_{OUT} andV_{in2} and between I_{OUT} and V_{IN3} has been derived , the next step follows is to check the derived expression among the twelve structures proposed in[1] , by putting the various values of feedback coefficients f_{ij} which are different for different structures as the values depends on the feedback connection between three blocks . After selecting the particular structure ,values of feedback coefficients and a_1 and b_1 can be generated easily by merely observing the structure and each structure further will have four parts depending on the combinations of values of a_2 and a_3.

The structure discussed below is structure IV which is as shown in fig 5.3

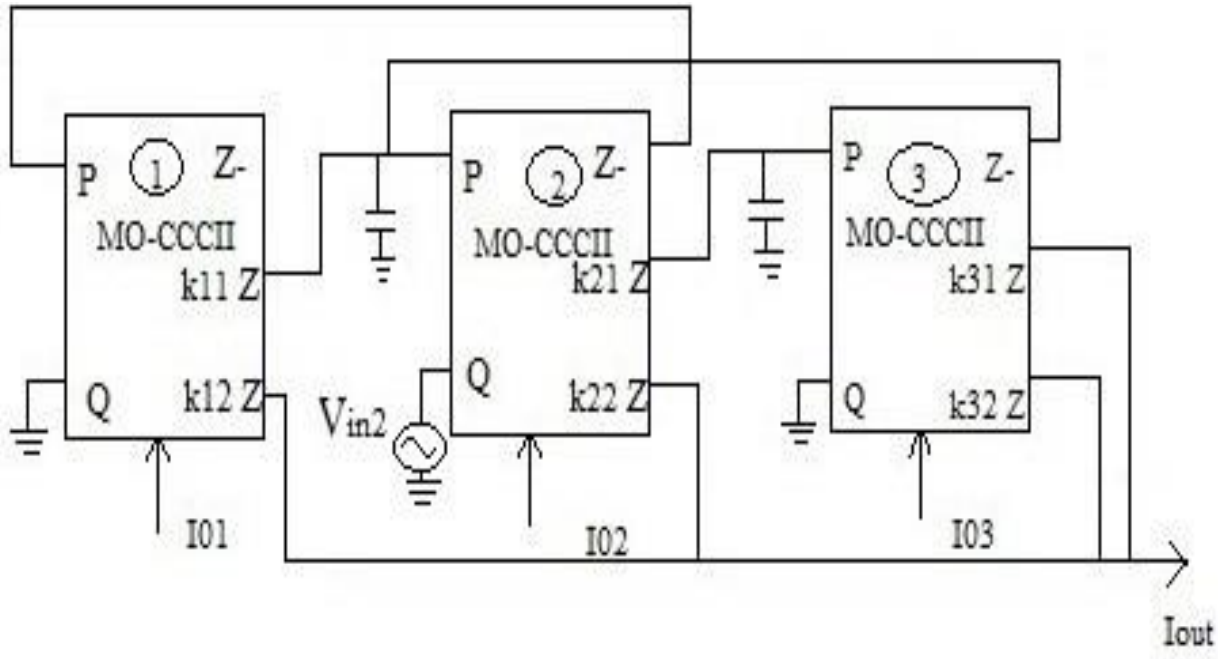

Fig 5.3 Block diagram of structure IV with input voltage V_{in2}

So according to the structure values of different coefficients are

$$a_1 = f_{12} = f_{23} = 1 \text{ , } f_{11} = 0$$

$$\text{Other } f_{ij} = 0$$

As derived the general expression for relation between I_{OUT} and V_{IN2} is

$$\frac{I_{out}}{V_{in2}} = \frac{N(s)}{|M(s)|}$$

Where

$$N(s) = sC_2[-k_{12}(f_{12}(f_{33} - a_3 - b_3\, sC_3R_{x3}) + f_{13}k_{21}) + k_{22}(f_{11} - a_1)(f_{33} - a_3 - b_3\, sC_3R_{x3}) + k_{21}\,(k_{31} + k_{32})((f_{11} - a_1)]$$

$$\text{And } |M(s)| = (f_{11} - a_1)[(f_{33} - a_3 - b_3\, sC_3R_{x3})\,(f_{22} - a_2 - b_2 sC_2R_{x3}) + f_{23}\,k_{21}]$$

$$+\ f_{12}\ k_{11}(f_{33} - a_3 - b_3\, sC_3R_{x3})\ +\ f_{13}\,k_{11}k_{21}$$

So after putting the values of above defined coefficients ,the transadmittance reduces to

$$\frac{I_{out}}{V_{in2}} = \frac{-sC_2\,[\,(a_3+b_3\, sC_3R_{x3}\,)(k_{12}+K_{22})-(k_{31}+k_{32})k_{21}]}{(a_3+b_3\, sC_3R_{x3}\,)\,(a_2+b_2\, sC_2R_{x2}\,) +\ k_{21} - k_{11}(a_3+b_3\, sC_3R_{x3}\,)}$$

Now variable coefficients are a_2 , a_3 , b_2 , b_3 and values of k coefficients , which when provided with different set of values gives different types of filter , so now depending upon combination of a_2 and a_3 , four topologies are possible which are explained below.

TOPOLOGY –A : In this topology , P terminal of both 2nd and 3rd MO-CCCII block is taken as Y and Q as X terminal i.e $a_2 = 0$, $a_3 = 0$, $b_2 = -1$, $b_3 = -1$ and considering $k_{11} = k_{21} = 1$,there are two types of filter possible . High pass realization : $k_{22} = 1$, $k_{12} = 0$ $k_{32}=1$,$k_{31} = -1$. Bandpass realization :$k_{22} = 1$, $k_{12}= -1$, $k_{31} =1$,$k_{32}=0$.

TOPOLOGY – B : In this topology , P terminal of 2nd MO-CCCII block is taken as X and P terminal of 3rd MO-CCCII block as Y terminal i.e $a_2 = 1$, $a_3 = 0$, $b_2 = 1$, $b_3 = -1$ and

considering $k_{11} = k_{21} = -1$, we get two types of filter . High pass realization : $k_{22} = 0$, $k_{12}=-1$ $k_{32} = k_{31} = 0$. Band pass realization : $k_{31} = k_{32} = 1, k_{12} = k_{22} = 0$.

TOPOLOGY – C : In this topology , P terminal of 2^{nd} MO-CCCII block is taken as Y and P terminal of 3^{rd} MO-CCCII block as X terminal i.e $a_2 = 0$, $a_3 = 1$, $b_2 = -1$, $b_3 = 1$ and considering $k_{11} = 1$, $k_{21} = -1$. High pass realization : $k_{22} = 0$, $k_{12} = 1$, $k_{32} = 0$, $k_{31} = -1$. Band pass realization : $k_{22} = 0 = k_{12}$, $k_{32} = 0$, $k_{31} = 1$.

TOPOLOGY – D : In this topology , P terminal of both 2^{nd} and 3^{rd} MO-CCCII block is taken as X and Q as Y terminal i.e $a_2 = 1$, $a_3 = 1$, $b_2 = 1$, $b_3 = 1$ and considering $k_{11} = -1$, $k_{21} = 1$ there are two types of filter possible . High pass realization : $k_{22} = 0, k_{12} = 1$, $k_{31} = 1$, $k_{32} = 0$. Bandpass realization : $k_{22} = 0 = k_{12}$, $k_{31} = 1, k_{32} = 0$.

In the similar way , relation between I_{OUT} and V_{IN3} can also be checked by using various coefficients . Now structure VII has been considered for the same whose block diagram is given below in fig 5.4

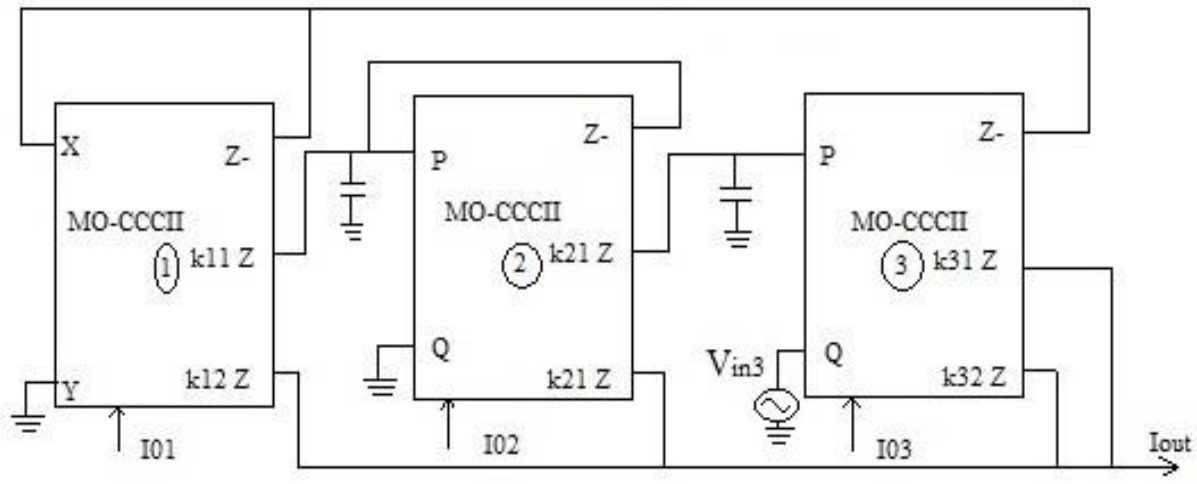

Fig 5.4 Block diagram of structure VII with applied input V_{in3}

So according to the structure values of different coefficients are

, $$f_{11} = f_{22} = f_{13} = 1 , a_1 = 0$$

Other $f_{ij} = 0$

The general expression derived between I_{OUT} and V_{IN3} is

$$\frac{I_{out}}{V_{in3}} = \frac{H(s)}{|M(s)|}$$

Where

$$H(s) = sC_3\{k_{12}[f_{12}f_{23} - f_{13}(f_{22} - a_2 - b_2sC_2R_{x2})] - k_{22}[(f_{11} - a_1)f_{23} + k_{11}f_{13}] + (k_{31} + k_{32})[(f_{11} - a_1)(f_{22} - a_2 - b_2sC_2R_{x2}) + k_{11}f_{12}]\}$$

Putting feedback coefficients values the reduced expression for transadmittance becomes

$$\frac{I_{out}}{V_{in3}} = \frac{-sC_3\{(k_{12}-(k_{31}+k_{32}))(1-a_2-b_2sC_2R_{x2})+k_{22}k_{11}\}}{(-a_3-b_3\,sC_3R_{x3})(1-a_2-b_2sC_2R_{x3})+K_{11}K_{21}}$$

Now variable coefficients are a_2 , a_3 , b_2 , b_3 and values of k coefficients , which when provided with different set of values gives different types of filter , so now depending upon combination of a_2 and a_3 , four topologies are possible which are explained below.

TOPOLOGY –A : In this topology , P terminal of both 2nd and 3rd MO-CCCII block is taken as Y and Q as X terminal i.e $a_2 = 0$, $a_3 = 0$, $b_2 = -1$, $b_3 = -1$ and considering $k_{11} = k_{21} = 1$,there are two types of filter possible . High pass realization : $k_{22} = 1$,$k_{12} = -1$, $k_{31} = 1k_{32} = -1$. Bandpass realization : $k_{22} = -1$, $k_{31} = 1$,$k_{32} = 0$,$k_{12} = 1$.

TOPOLOGY – B : In this topology , P terminal of 2nd MO-CCCII block is taken as X and P terminal of 3rd MO-CCCII block as Y terminal i.e $a_2 = 1$, $a_3 = 0$, $b_2 = 1$, $b_3 = -1$ and considering $k_{11} = 1$, $k_{21} = -1$, we get two types of filter . High pass realization : $k_{22} = 0$, $k_{32} = 0$, $k_{31} = 0$,$k_{12} = 1$. Band pass realization : $k_{22} = 1$, $k_{31} = 0 = k_{12}$, $k_{32} = 0$.

TOPOLOGY – C : In this topology , P terminal of 2nd MO-CCCII block is taken as Y and P terminal of 3rd MO-CCCII block as X terminal i.e$a_2 = 0$, $a_3 = 1$, $b_2 = -1$, $b_3 = 1$ and considering $k_{11} = -1$,$k_{21} = +1$. High pass realization : $k_{22} = 1$,$k_{12} = -1$, $k_{32} = 0$, $k_{31} = 0$. Band pass realization : $k_{22} = -1$, $k_{32} = 0$, $k_{31} = 0$,$k_{12} = 0$.

TOPOLOGY – D : In this topology , P terminal of both 2nd and 3rd MO-CCCII block is taken as X and Q as Y terminal i.e$a_2 = 1$, $a_3 = 1$, $b_2 = 1$, $b_3 = 1$ and considering $k_{11} = -1$, $k_{21} = -1$ there are two types of filter possible . High pass realization : $k_{22} = 0$, $k_{31} = k_{32} = 0$,$k_{12} = 1$. Bandpass realization : $k_{22} = -1$, $k_{31} = 1$, $k_{32} = 0$,$k_{12} = 1$.

5.4 SIMULATION :

In this section , above derived results for the transadmittance are verified . There are two structure which were taken for consideration . Structure IV is taken for consideration when input voltage is applied at the 2nd MO-CCCII block and structure VII is taken into consideration when input voltage is applied at 3rd MO-CCCII . So two transadmittance expressions are considered for different structure . The values of feedback coefficient are put into the expression and the reduced transadmittance expression is considered for one of the four topologies by putting the value of coefficients a_2 , a_3, b_2 and b_3 . The values of k coefficients are selected so as to get valid filter expression for the same.

5.4.1 Transadmittance 1 : Ratio of I_{out} to the applied voltage V_{in2} :

The structure which is considered for the transadmittance expression here is structure IV . In this transadmittance expression, input voltage is applied at the 2nd MO-CCCII of structure IV and ratio of output current I_{out} to the input voltage V_{in2} is derived . Now as discussed earlier the reduced expression for structure IV after putting the feedback coefficients ($a_1 = f_{12} = f_{23} = 1$,

$f_{11} = 0$ other $f_{ij}=0$) is

$$\frac{I_{out}}{V_{in2}} = \frac{-sC_2\,[\,(a_3+b_3\,sC_3R_{x3}\,)(k_{12}+K_{22})-(k_{31}+k_{32})k_{21}]}{(a_3+b_3\,sC_3R_{x3}\,)\,(a_2+b_2\,sC_2R_{x2}\,)+\,k_{21}-k_{11}(a_3+b_3\,sC_3R_{x3}\,)}$$

After selecting the structure IV , now one of its four technologies is considered , in this case topology A is considered where values of coefficients are $a_2 = 0$, $a_3 = 0$, $b_2 = -1$, $b_3 = -1$.

So final expression becomes

$$\frac{I_{out}}{V_{in2}} = \frac{sC\,[\,(sCR_{x3})(k_{12}+K_{22})+(k_{31}+k_{32})k_{21}]}{s^2C^2R_{x3}R_{x2} + k_{11}\,sC_3R_{x3} + k_{21}}$$

So it can be observed that from the above reduced expression , two valid filter expression can be achieved , one is high pass filter and other is band pass filter depending on the value of coefficient k . So for high pass filter realization , values of different coefficients of k are taken as $k_{11} = k_{21} = 1$, $k_{22} = 1$, $k_{12} = 0$ $k_{31} = 1$ $k_{32} = -1$ and for bandpass realization value of coefficients k are $k_{11} = k_{21} = 1$, $k_{22} = 1$, $k_{12} = -1$, $k_{31} = 1$,$k_{32} = 0$.

5.4.1.1 High pass realization : The structure IV topology A with different values of coefficient k are taken into consideration using ORCAD Pspice schematic .Value of coefficient k are taken as $k_{11} = k_{21} = 1$, $k_{22} = 1$, $k_{31} = -1$ $k_{32}=1$,$k_{12} = 0$ and accordingly block diagram is constructed . The schematic block diagram for above is given in the fig 5.5 as

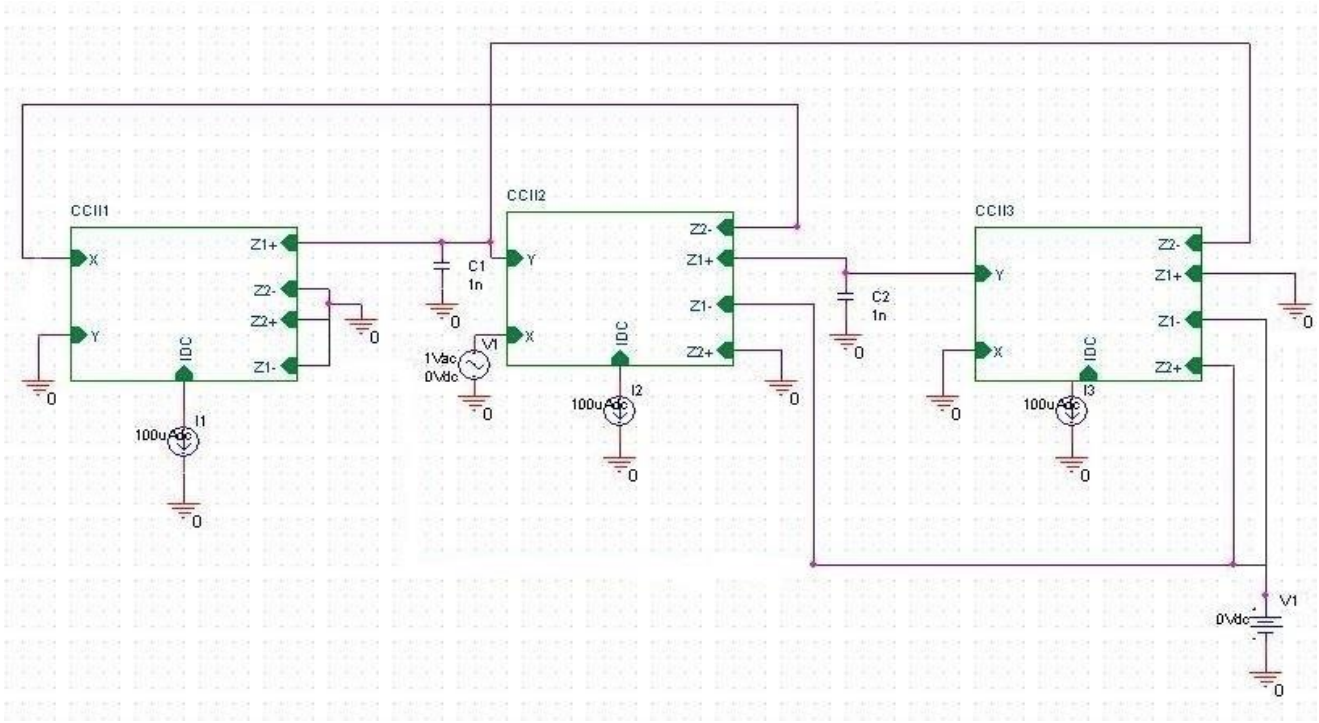

Fig 5.5 Schematic block diagram of structure IV topology A for high pass filter

Simulation results for MO-CCCII are obtained at 2.5V supply , 100 μA biasing current I_0 and 0.35 μm technology . Resultant high pass filter is realized from the above structure and the output is given as in the fig 5.6 showing graph as

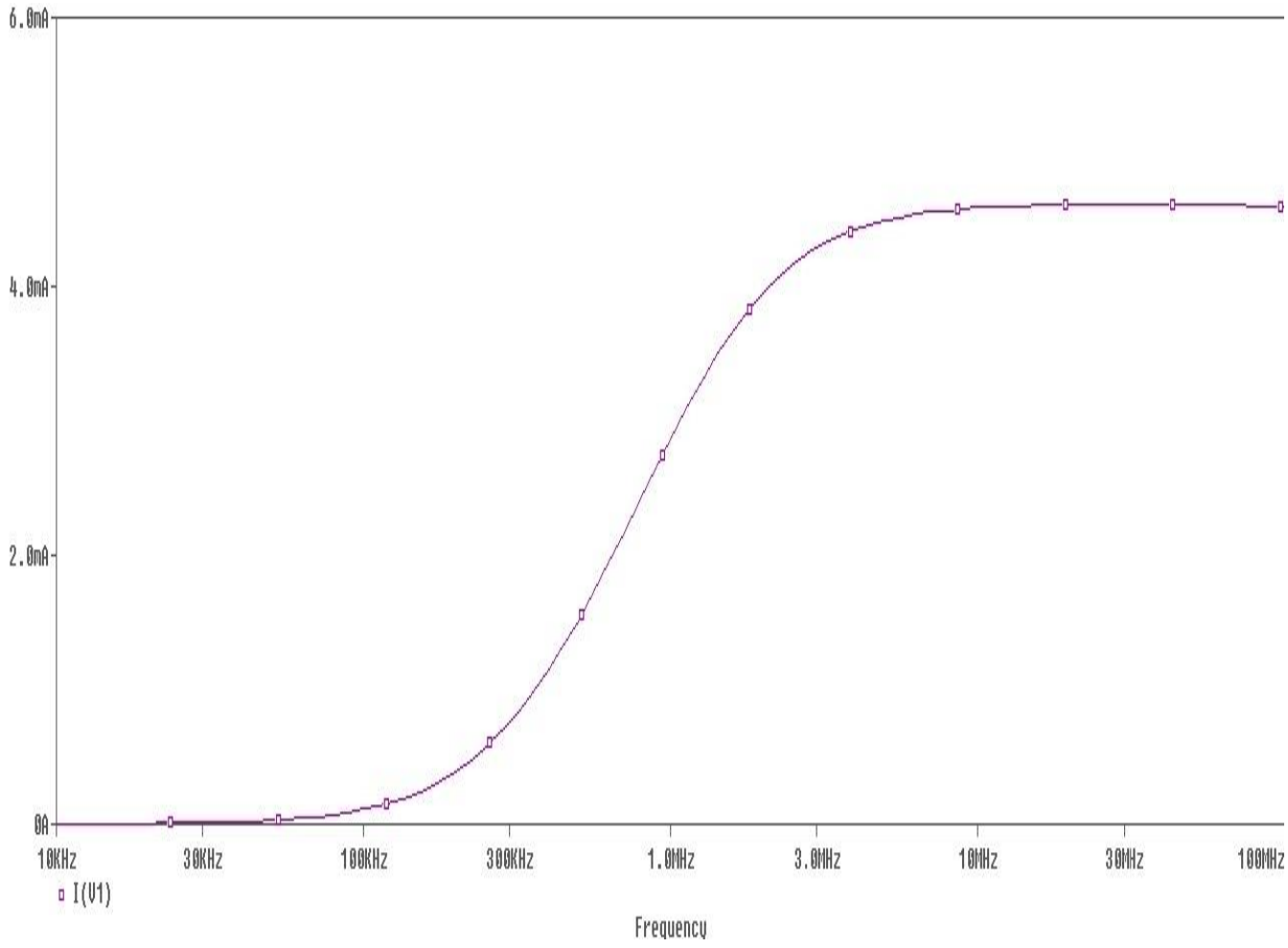

Fig 5.6 Graph of simulated structure IV showing high pass filter

5.4.1.2 Band pass realization : For band pass realization , the above block diagram remain the same except the few changes that need to be done due to changed values of coefficient k in this case . The coefficient k values are different than the previous case such that output terminals of three MO-CCCII have to be connected to the Iout terminal in different way as compared to the previous one . So the modified block diagram as shown in fig 5.7 as

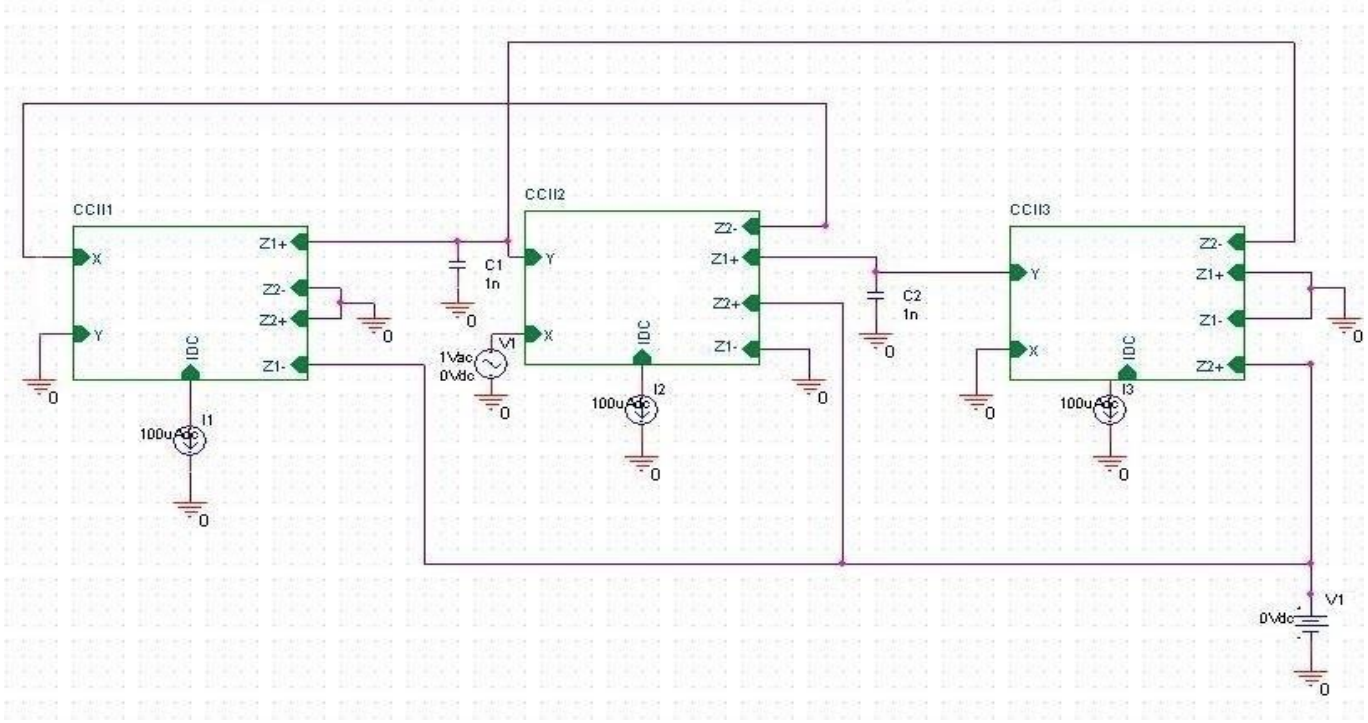

Fig 5.7 Schematic block diagram of structure IV topology A for band pass filter

For bandpass realization value of coefficients k are $k_{11} = k_{21} = 1$, $k_{22} = 1$, $k_{12} = -1$, $k_{31} = 1$,$k_{32} = 0$ and accordingly output of each MO-CCCII are connected to the I_{out} terminal represented by V1 in the above schematic diagram.

Simulation results for MO-CCCII are obtained at 2.5V supply , 100 μA biasing current I_0 and 0.35 μm technology . Resultant band pass filter is realized from the above structure and the output is given as in the fig 5.8 showing graph as

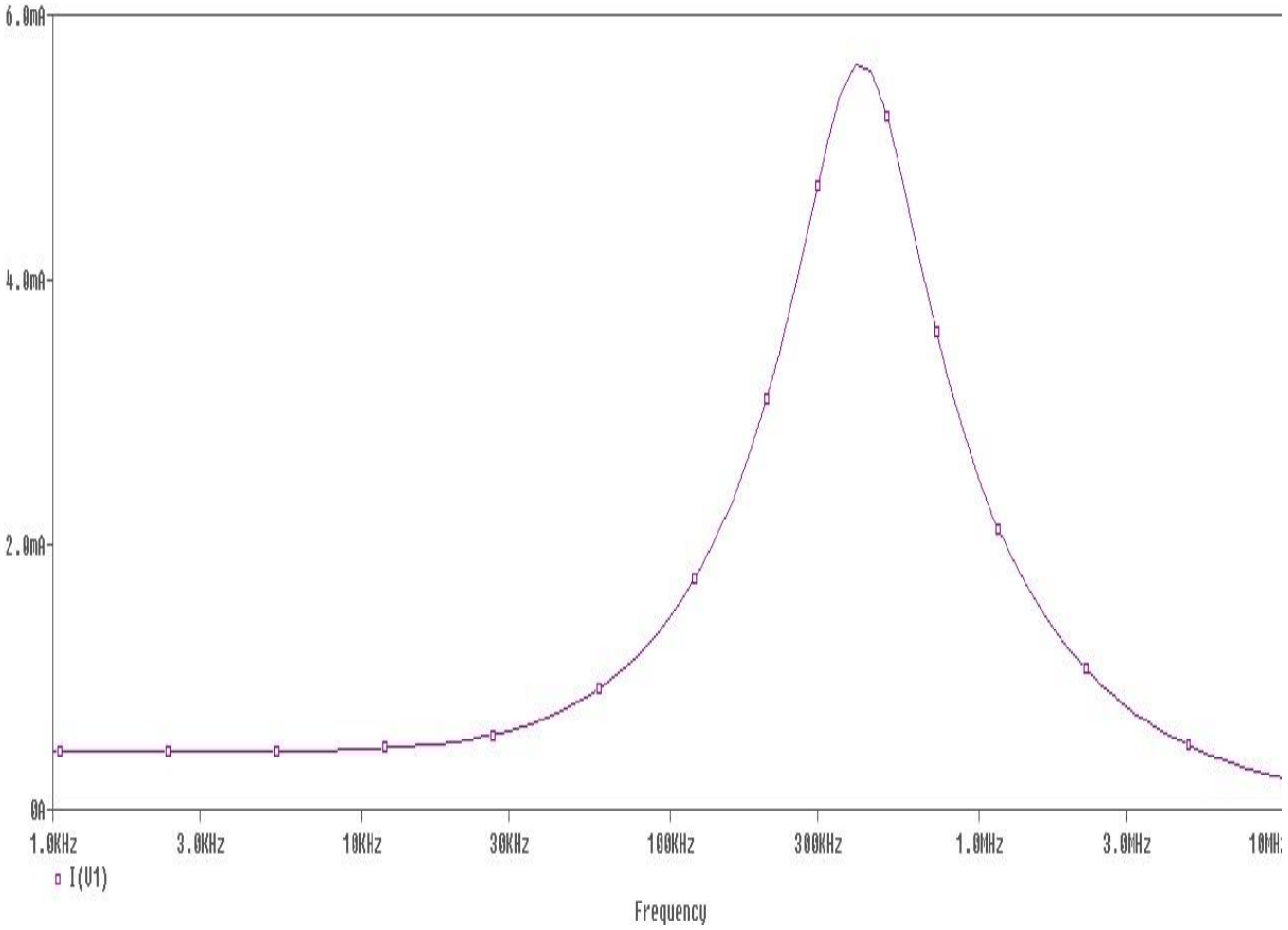

Fig 5.8 Graph of simulated structure IV showing the band pass filter

In the above graph , the output current (I_{OUT}) which is represented by I(V1) in the block diagram is shown in fig 5.8 .The ratio of same terminal are taken for the realization of band pass filter with same structure and same topology but only difference is the different connections

due to difference in values of k coefficients . Coefficients k decide the connection of output terminal of each MO-CCCII.

5.4.2 Transadmittance 2 : Ratio of I_{out} to the applied voltage V_{in3} :

In the previous section , transadmittance is considered when input voltage is applied at the 2nd MO-CCCII but in this section transadmittance expression is considered when the input voltage is applied at the 3rd MO-CCCII . The structure which is taken into consideration is structure VII . Now as discussed earlier the reduced expression for structure VII after putting the feedback coefficients ($f_{11} = f_{22} = f_{13} = 1$, $a_1 = 0$ other $f_{ij}=0$) is

$$\frac{I_{out}}{V_{in3}} = \frac{-sC_3\{(k_{12}-(k_{31}+k_{32}))(1-a_2-b_2sC_2R_{x2})+k_{22}k_{11}\}}{(-a_3-b_3\,sC_3R_{x3})(1-a_2-b_2sC_2R_{x2})+K_{11}K_{21}}$$

After selecting the structure VII , now one of its four technologies is considered , in this case topology A is considered where values of coefficients are $a_2 = 0$, $a_3 = 0$, $b_2 = -1$, $b_3 = -1$ .So the final reduced expression becomes

$$\frac{I_{out}}{V_{in3}} = \frac{-sC_3\{(k_{12}-(k_{31}+k_{32}))(1+sC_2R_{x2})+k_{22}k_{11}\}}{s^2C^2R_{x3}R_{x2}+sCR_{x3}+K_{11}K_{21}}$$

So it can be observed that from the above reduced expression , two valid filter expression can be achieved , one is high pass filter and other is band pass filter depending on the value of coefficient k .

5.4.2.1 High pass realization : The structure VII topology A with different values of coefficient k are taken into consideration using ORCAD Pspice schematic .Value of coefficient k are taken as $k_{11} = k_{21} = 1$, $k_{22} = 1$,$k_{12} = -1$, $k_{31} = 1k_{32} = -1$ and accordingly block diagram is constructed . The schematic block diagram for above is given in the fig 5.9 as

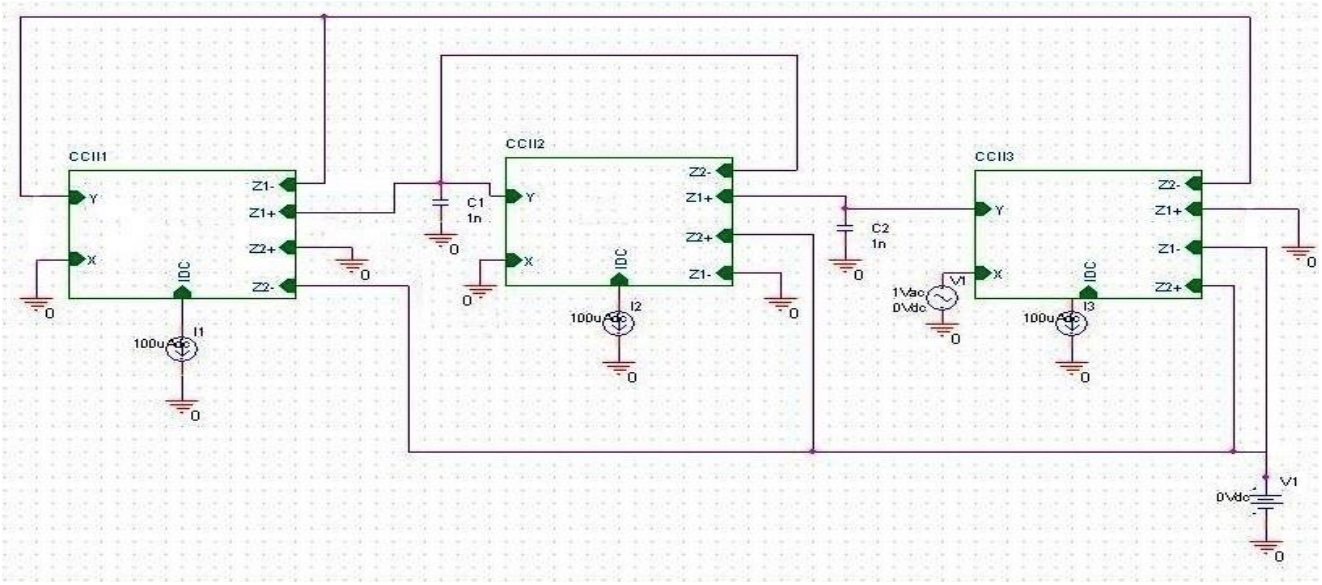

Fig 5.9 Schematic block diagram of structure VII topology A for high pass filter

The above block diagram is constructed according to the feedback and other coefficients. Simulation results for MO-CCCII are obtained at 2.5V supply , 100 μA biasing current I_0 and 0.35 μm technology . Resultant high pass filter is realized from the above structure and the output is given as in the fig 5.10showing graph as

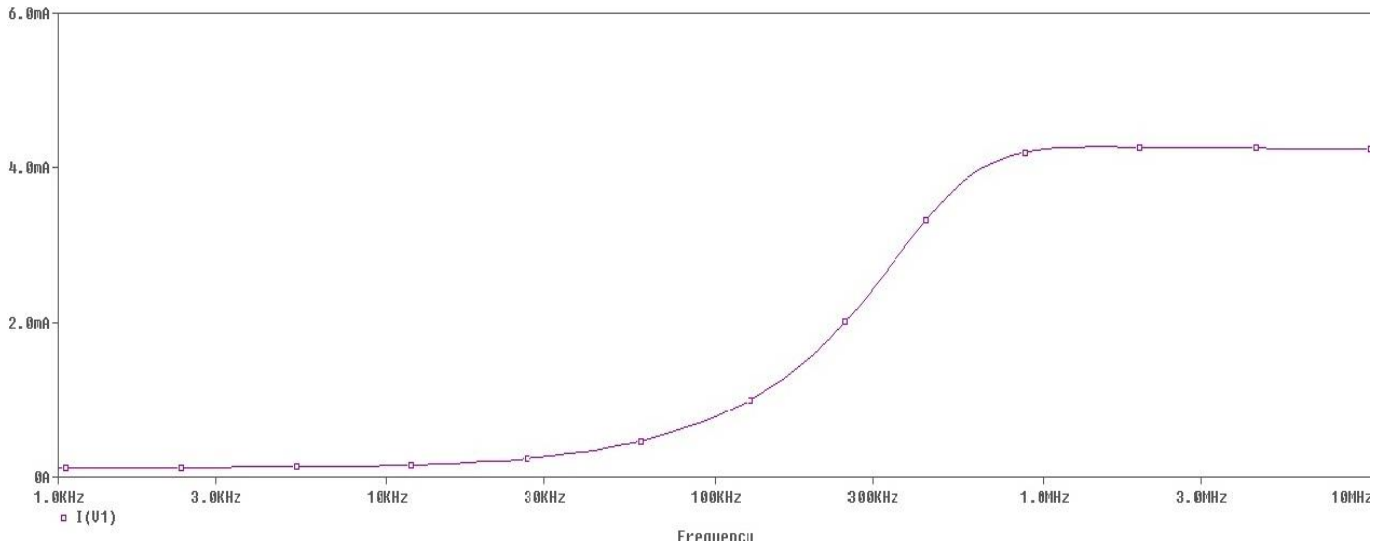

Fig 5.10 Graph of simulated structure VII showing the high pass filter

5.4.2.2 Band pass realization : For band pass realization ,the values of coefficients need to be changed. The coefficient k values are $k_{11} = k_{21} = 1$, $k_{22} = -1$, $k_{31} = 0, k_{32} = 1, k_{12} = 1$. So the modified block diagram as shown in fig 5.11 as

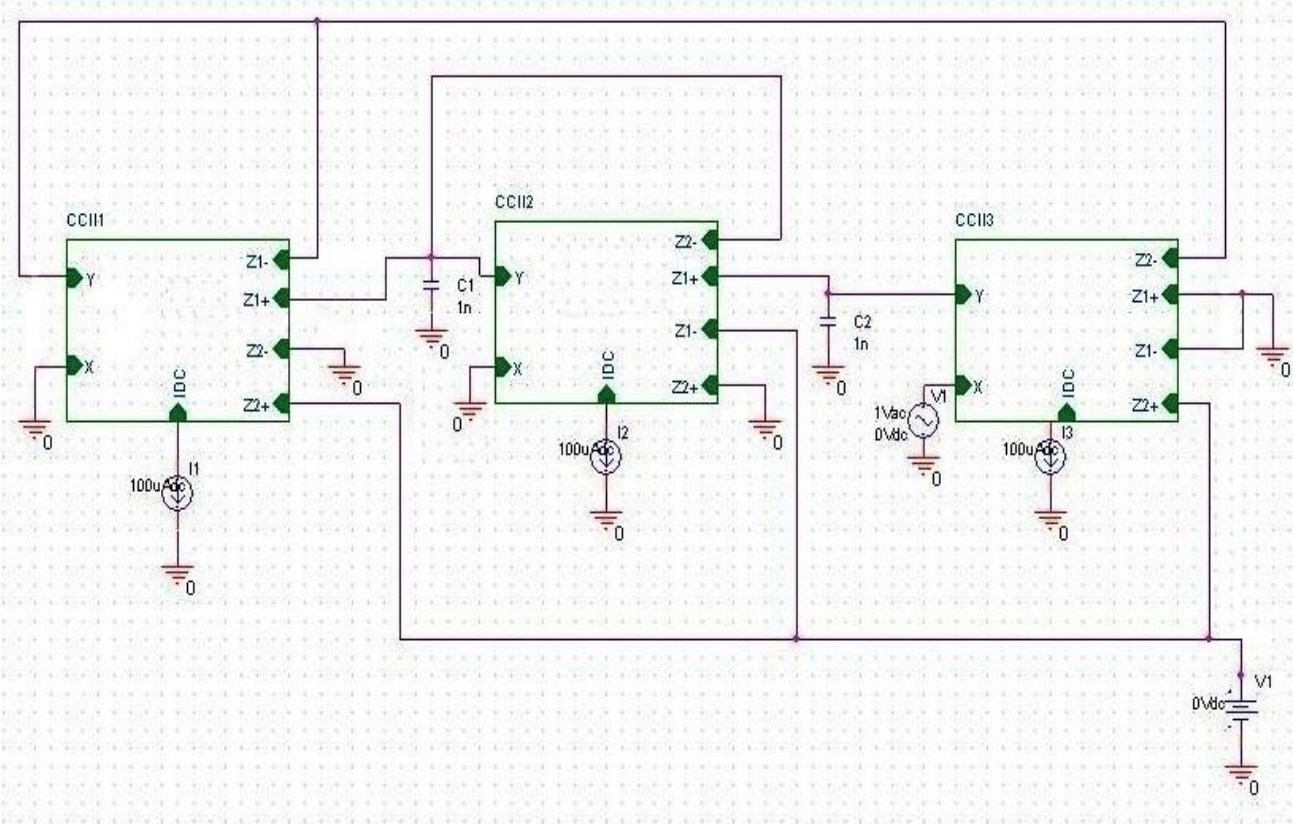

Fig 5.11 Schematic block diagram of structure VII topology A for band pass filter

As it can be seen that connection of output terminal of each MO-CCCII is changed according to the value of coefficient k , rest circuit remains the same with output and input terminals as used earlier .

Resultant band pass filter is realized from the above structure and the output is given as in the fig 5.12 showing graph as

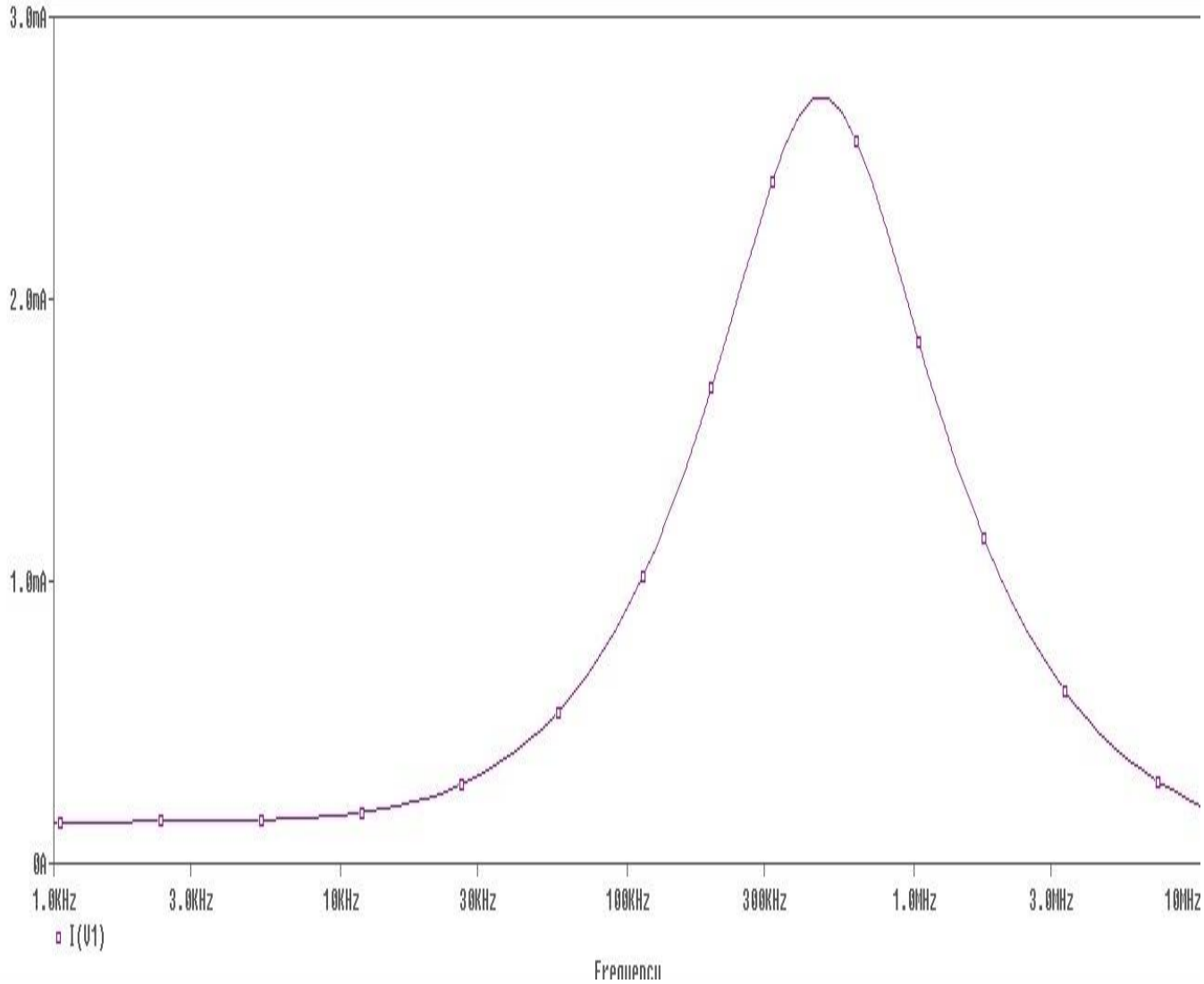

Fig 5.12 Graph of simulated structure VII showing the band pass filter

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CHAPTER 6

Voltage gain realization

In this chapter generalized expression of transfer function is calculated in the form of V/V ratio .The input voltage is applied at the grounded input terminal of 2nd MO-CCCII and the ratio of voltage at node 2nd to the applied input voltage is realized . Furthermore , generalized expression of ratio of voltage at node 3 to the input voltage applied at grounded input terminal of 2nd MO-CCCII is also calculated . In the same way , above step are repeated by applying input voltage at grounded terminal of 3rd MO-CCCII and realization of transfer fuction at node 2nd and node 3rd is realized .

6.1 General expression representing relation between input voltage V_{in2} and different node voltages :

For the realization of transfer fuction , input voltage is applied at the grounded input terminal of 2nd MO-CCCII block , as done in the previous chapter (chapter 5) and its transfer fuction in the form of V/V is calculated at the node 2nd and 3rd . So initially voltage node 2nd is considered , the block diagram considered is same as in the previous chapter as shown in fig 6.1

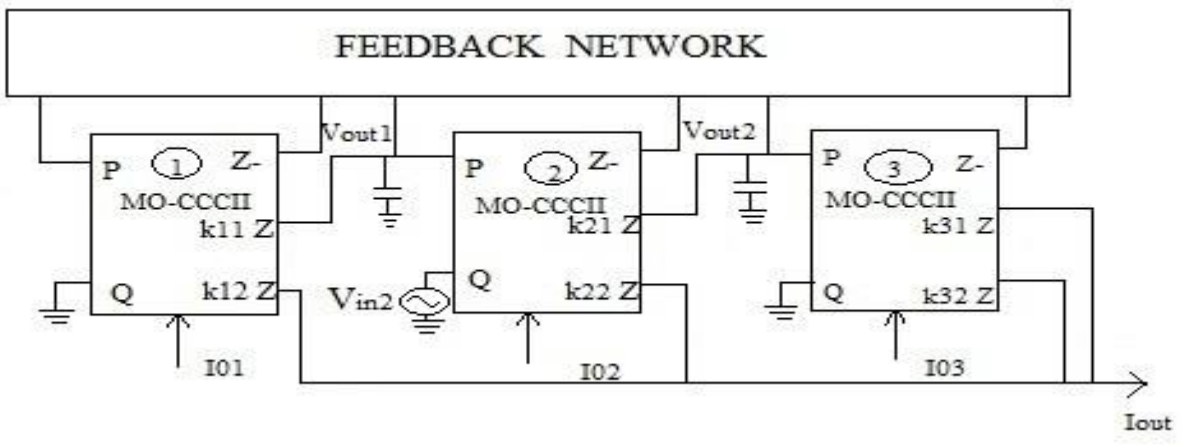

Fig 6.1 Multiple loop feedback voltage mode filter structure I

The general voltage equation[1] for the MO-CCCII is

$$V_X = V_Y + i_X|R_{Xi}(I_{0i})| \quad (1)$$

Where V_X and V_Y are the voltages at the input terminal of X and Y of the MO-CCCII block .If one of the input terminal is grounded then the voltage equation[1] reduced to

$$V_{pi} = b_i i_{xi} R_{xi} \quad (2)$$

Where value of notation b_i can be either 1 or -1 depending on whether the input is connected to the X terminal or Y terminal which can be found out by the value of a_i.So if the value of $a_i = 1$ means input is connected to terminal X and $b_i = 1$ if $a_i = 0$ then input to the MO-CCCII is connected to Y terminal means $b_i = -1$ [1] .

So as the generalized expression is to be derived , the input node cant be considered X or Y randomly . The representation for X and Y is given by P and Q which can be any terminal . Finally from above equation (1) and (2) , the voltage equation for the input node P of 2^{nd} MO-CCCII is given by[1]

$$V_{P2} = V_{in2} + b_2 i_{X2} R_{X2} \quad (3)$$

In the previous chapter (chapter 5) , generalized expression has been derived for the ratio of current at various input terminal to the applied input voltages at grounded input terminal of 2^{nd} MO-CCCII which is represented by equation (a) ,(b) and (c) in the last chapter given by

$$\frac{i_{x1}}{V_{in2}} = \frac{-sC_2(f_{12}(f_{33}-a_3-b_3\, sC_3R_{x3})+f_{13}k_{21}]}{|M(s)|} \quad (a)$$

$$\frac{i_{x2}}{V_{in2}} = \frac{sC_2(f_{11}-a_1)(f_{33}-a_3-b_3\, sC_3R_{x3})}{|M(s)|} \quad (b)$$

$$\frac{i_{x3}}{V_{in2}} = \frac{sC_2k_{21}(f_{11}-a_1)}{|M(s)|} \quad (c)$$

Considering node voltages V_{OUT1} and V_{OUT2} as V_{OUT1} and V_{OUT2} respectively .

Where

$$|M(s)| = (f_{11} - a_1)[(f_{33} - a_3 - b_3\, sC_3R_{x3})\,(f_{22} - a_2 - b_2 sC_2R_{x2}) + f_{23}\, k_{21}]$$

$$+\ f_{12}\ k_{11}(f_{33} - a_3 - b_3\, sC_3R_{x3})\ +\ f_{13}\, k_{11}k_{21}$$

So by putting the value of i_{X2} from the equation (b) in the voltage equation (3) , the resultant equation is

$$V_{OUT1} = V_{in2} + b_2\, R_{X2}\, \frac{sC_2(f_{11}-a_1)(f_{33}-a_3-b_3\, sC_3R_{x3})}{|M(s)|}\ V_{in2}$$

$$V_{OUT1} = V_{in2}\ \left(\frac{M(s)+b_2 sC_2R_{X2}(f_{11}-a_1)(f_{33}-a_3-b_3\, sC_3R_{x3})}{|M(s)|}\right)$$

$$\frac{V_{OUT1}}{V_{in2}} = \frac{M(s)+b_2 sC_2R_{X2}(f_{11}-a_1)(f_{33}-a_3-b_3\, sC_3R_{x3})}{|M(s)|} \qquad (3a)$$

Similarly the ratio of node voltage 3rd to the input voltage V_{in2} is calculated . The Q terminal of 3rd MO-CCCII is grounded so the voltage at node 3rd will satisfy the equation(2) as

$$V_{P3} = b_3\, i_{x3}R_{x3}$$

So modifying the above equation according to the node 3 voltage equation

$$V_{OUT2} = b_3\, i_{x3}R_{x3} \qquad (4)$$

Putting the equation (c) in the voltage equation (4) , the result derived is

$$V_{OUT2} = \frac{b_3 sC_2R_{x3}k_{21}(f_{11}-a_1)}{|M(s)|}\, V_{in2}$$

$$\frac{V_{OUT2}}{V_{in2}} = \frac{b_3 sC_2R_{x3}k_{21}(f_{11}-a_1)}{|M(s)|} \qquad (3b)$$

6.2 General expression representing relation between V_{in3} and different node voltages :

In this part , the input voltage is applied at the grounded input terminal of 3rd MO-CCCII block and generalized expression for the transfer function (V/V) is derived for the node voltages 2nd and 3rd . the block diagram shown for the same is in fig 6.2 as

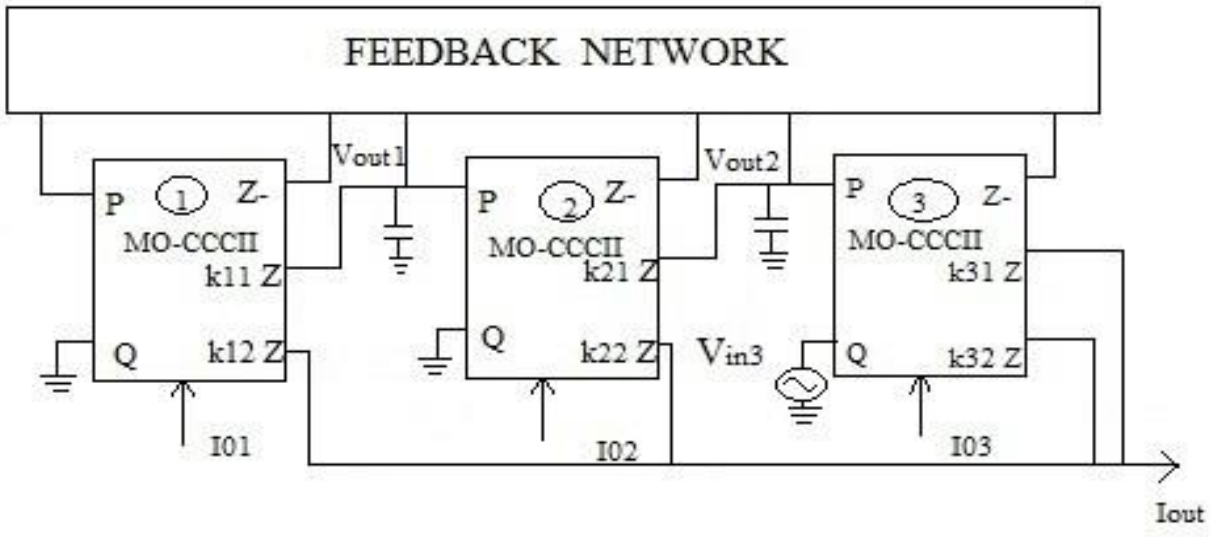

Fig 6.2 Multiple loop feedback voltage mode filter structure II

Now in the above block diagram , it is shown clearly that the input terminal Q of 2nd MO-CCCII block is grounded , so the node voltage 2nd will satisfy the equation (2)

$$V_{pi} = b_i i_{xi} R_{xi}$$

Modifying according to the node equation for 2nd node as [1]

$$V_{OUT1} = b_2 i_{x2} R_{x2} \qquad (5)$$

In the previous chapter , the generalized expression for the ratio of different input currents to the applied input voltage at grounded terminal 3rd MO-CCCII block is derived . The equation were represented by (d),(e) and (f) as

$$\frac{i_{x1}}{V_{in3}} = \frac{sC_3[f_{12}f_{23} - f_{13}(f_{22} - a_2 - b_2 sC_2 R_{x2})]}{|M(s)|} \quad (d)$$

$$\frac{i_{x2}}{V_{in3}} = \frac{-sC_3[(f_{11} - a_1)f_{23} + k_{11}f_{13}]}{|M(s)|} \quad (e)$$

$$\frac{i_{x3}}{V_{in3}} = \frac{sC_3[(f_{11} - a_1)(f_{22} - a_2 - b_2 sC_2 R_{x2}) + k_{11}f_{12}]}{|M(s)|} \quad (f)$$

Putting the equation (e) in the equation (5) , the result derived as

$$V_{OUT1} = \frac{-b_2 sC_3 R_{X3}[(f_{11} - a_1)f_{23} + k_{11}f_{13}]}{|M(s)|} V_{in3}$$

$$\frac{V_{OUT1}}{V_{in3}} = \frac{-b_2 sC_3 R_{X3}[(f_{11} - a_1)f_{23} + k_{11}f_{13}]}{|M(s)|} \quad (6a)$$

Where

$$|M(s)| = (f_{11} - a_1)[(f_{33} - a_3 - b_3 sC_3 R_{x3})(f_{22} - a_2 - b_2 sC_2 R_{x2}) + f_{23} k_{21}]$$

$$+ f_{12} k_{11}(f_{33} - a_3 - b_3 sC_3 R_{x3}) + f_{13} k_{11} k_{21}$$

For the node voltage 3 to be taken into consideration , it should be noted that the input terminal Q of 3rd MO-CCCII block is applied with input voltage V_{in3} , so the node voltage will satisfy the equation (1) as

$$V_{OUT2} = V_{in3} + b_3 i_{X3} R_{X3} \quad (7)$$

Putting the value of equation (f) in the equation (7)

$$V_{OUT2} = V_{in3} + \frac{b_3 s C_3 R_{X3}[(f_{11}-a_1)(f_{22}- a_2-b_2 s C_2 R_{x2})+ k_{11} f_{12}]}{|M(s)|} V_{in3}$$

$$V_{OUT2} = [1 + \frac{b_3 s C_3 R_{X3}[(f_{11}-a_1)(f_{22}- a_2-b_2 s C_2 R_{x2})+ k_{11} f_{12}]}{|M(s)|}]V_{in3}$$

$$\frac{V_{OUT2}}{V_{in2}} = \frac{M(s)+b_3 s C_3 R_{X3}[(f_{11}-a_1)(f_{22}- a_2-b_2 s C_2 R_{x2})+ k_{11} f_{12}]}{|M(s)|} \quad (6b)$$

The equation(3a) , (3b) , (6a) and (6b) represents the generalized expression of the transfer fuction at node 2 and 3 with repect to the input applied at 2nd and 3rd MO-CCCII. The derived expression are checked in the one of 12 structure and result are observed whether they satisfy any valid filter expression or not .

6.3 FILTER SYNTHESIS :

As the general expression between V_{in2} and V_{OUT1} and between V_{in2} and V_{OUT2} is derived so now they are tested in various structure by putting values of feedback coefficients f_{ij} and values of coefficients k is selected , such that , some meaningful expression can be derived . After selecting the particular structure ,values of feedback coefficients and a_1 and b_1 can be calculated easily by merely observing the structure and each structure further will have four topologies depending on the combinations of values of a_2 and a_3 .

Now for consideration let take structure VIII whose block diagram is shown below in fig 6.3

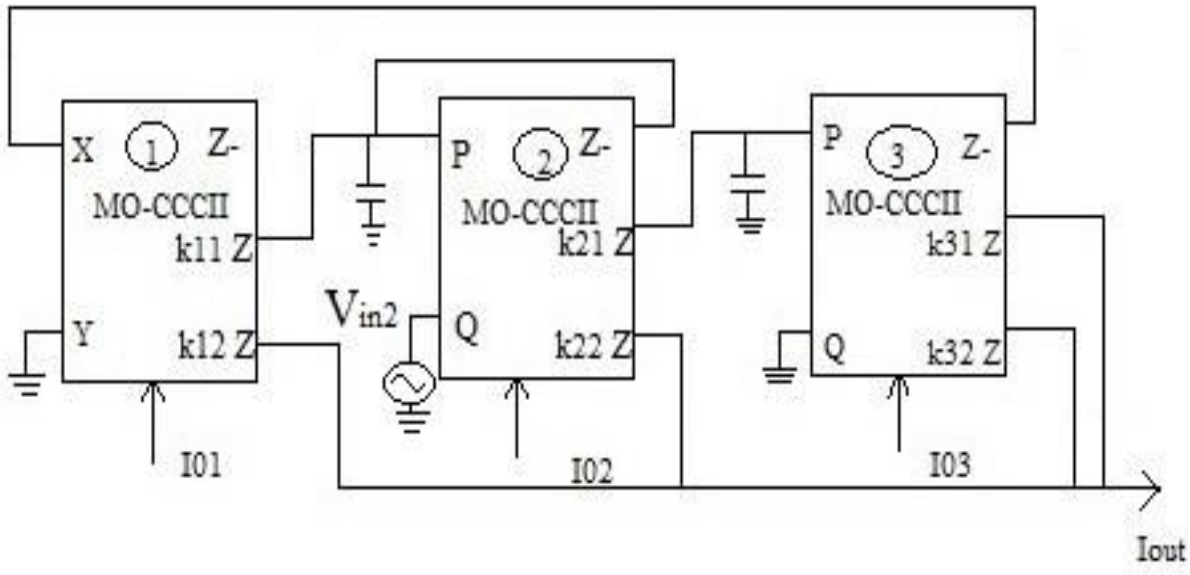

Fig 6.3 Block diagram of structure VIII with input voltage V_{in2}

The values of the coefficient for the above structure VIII is

$$a_1=f_{22}=f_{13}=1$$

$$f_{11}=0 \text{ other } f_{ij}=0$$

After taking the above coefficient into consideration , equation (3a) and (3b) get reduced to

$$\frac{V_{OUT1}}{V_{in2}} = \frac{(a_3+b_3\,sC_3R_{X3})(1-a_2-b_2sC_2R_{x2}) + k_{11}k_{21}+b_2sC_2R_{X2}(a_3+b_3\,sC_3R_{x3})}{(a_3+b_3\,sC_3R_{x3})\,(1-a_2-b_2sC_2R_{x2}) + k_{11}k_{21}}$$

$$\frac{V_{OUT2}}{V_{in2}} = \frac{-b_3sC_2R_{x3}k_{21}}{(a_3+b_3\,sC_3R_{x3})\,(1-a_2-b_2sC_2R_{x2}) + k_{11}k_{21}}$$

It can be observed that the equation (3b) will always be band pass filter whatever may be the topology, the derived expression is independent of the values of a_i and b_i . Now the above reduced expression is checked for different topology as

TOPOLOGY –A : In this topology , P terminal of both 2nd and 3rd MO-CCCII block is taken as Y and Q as X terminal i.e $a_2 = 0$, $a_3 = 0$, $b_2 = -1$, $b_3 = -1$ and considering $k_{11} = 1$ $k_{21} = -1$,the above reduced expression becomes

$$\frac{V_{OUT1}}{V_{in2}} = \frac{sCR_{X3} + 1}{s^2C^2R_{X2}R_{X3} + sCR_{X3} + 1} \qquad (\text{taking } C_2 = C_3 = C) \qquad (7.a)$$

$$\frac{V_{OUT2}}{V_{in2}} = \frac{sCR_{X3}}{s^2C^2R_{X2}R_{X3} + sCR_{X3} + 1} \qquad (7.b)$$

From the above result , it can be seen that equation 7.a provides no valid filter expression but equation 7.b provides expression for band pass filter . Considering topology B .

TOPOLOGY – B : In this topology , P terminal of 2nd MO-CCCII block is taken as X and P terminal of 3rd MO-CCCII block as Y terminal i.e $a_2 = 1$, $a_3 = 0$, $b_2 = 1$, $b_3 = -1$ and considering $k_{11} = k_{21} = 1$. The reduced equation becomes

$$\frac{V_{OUT1}}{V_{in2}} = \frac{1}{s^2C^2R_{X2}R_{X3} + 1} \qquad (\text{taking } C_2 = C_3 = C) \qquad (7.c)$$

$$\frac{V_{OUT2}}{V_{in2}} = \frac{sCR_{X3}}{s^2C^2R_{X2}R_{X3} + 1} \qquad (7.d)$$

No valid expression is observed from the above two equations.

TOPOLOGY – C : In this topology , P terminal of 2nd MO-CCCII block is taken as Y and Q terminal of 3rd MO-CCCII block as X terminal i.e $a_2 = 0$, $a_3 = 1$, $b_2 = -1$, $b_3 = 1$ and considering $k_{11} = 1$,$k_{21} = 1$.The reduced expression becomes

$$\frac{V_{OUT1}}{V_{in2}} = \frac{sCR_{X2} + 2}{s^2C^2R_{X2}R_{X3} + sC(R_{X3} + R_{X2}) + 2} \qquad (7.e)$$

$$\frac{V_{OUT2}}{V_{in2}} = \frac{sCR_{X3}}{s^2C^2R_{X2}R_{X3} + sC(R_{X3} + R_{X2}) + 2} \qquad (7.f)$$

Equation (7.f) gives filter expression for band pass.

TOPOLOGY – D : In this topology , P terminal of both 2nd and 3rd MO-CCCII block is taken as X and Q as Y terminal i.e $a_2 = 1$, $a_3 = 1$, $b_2 = 1$, $b_3 = 1$ and considering $k_{11} = -1$, $k_{21} = 1$ .Thr reduced expression becomes

$$\frac{V_{OUT1}}{V_{in2}} = \frac{1}{s^2C^2R_{X2}R_{X3} + sCR_{X2} + 1} \qquad (\text{taking } C_2 = C_3 = C) \qquad (7.g)$$

$$\frac{V_{OUT2}}{V_{in2}} = \frac{sCR_{X3}}{s^2C^2R_{X2}R_{X3} + sCR_{X3} + 1} \qquad (7.h)$$

From the above two equation , both gives valid filter expression , equation (7.g) gives expression for low pass filter and expression (7.h) provides expression for band pass filter.

After taking V_{in2} into consideration , now let takes V_{in3} into account for the same structure by grounding the Q terminal of 2nd MO-CCCII block and applying the input voltage V_{in3} to the Q terminal of the 3rd MO-CCCII . The block diagram can be shown as in fig 6.4 .

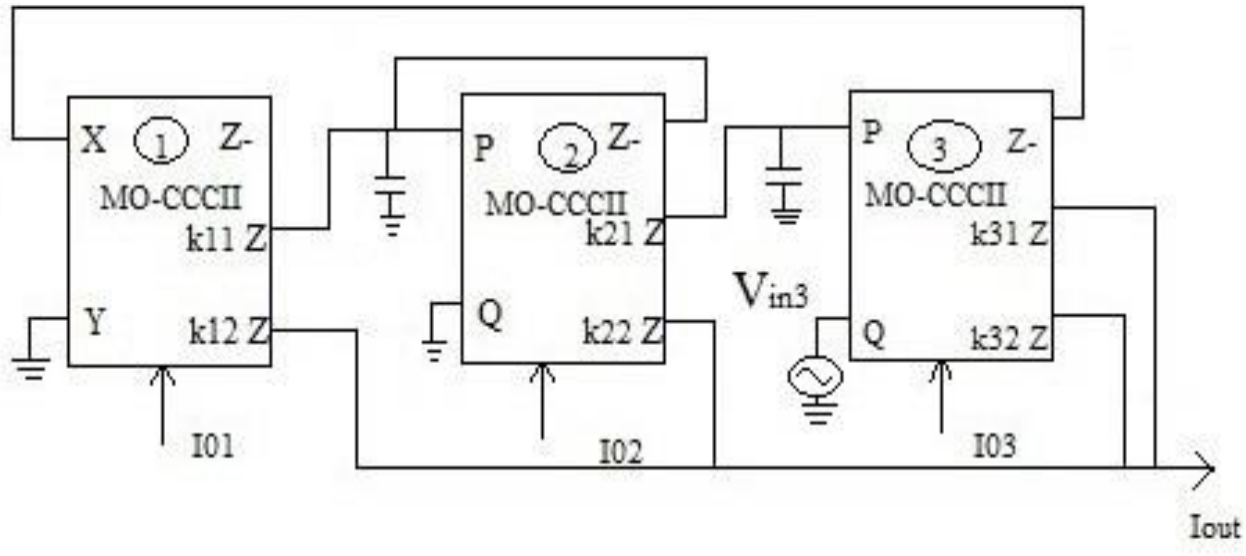

Fig 6.4 Block diagram of structure VIII with applied input V_{in3}

After taking coefficient into consideration ,equation (6a) and (6b) get reduced to

$$\frac{V_{OUT1}}{V_{in3}} = \frac{-b_2 sC_3 R_{X3} k_{11}}{|(a_3+b_3\, sC_3 R_{x3})(1-a_2-b_2 sC_2 R_{x2}) + k_{11}k_{21}|}$$

$$\frac{V_{OUT2}}{V_{in3}} = \frac{(a_3+b_3\, sC_3 R_{x3})(1-a_2-b_2 sC_2 R_{x2}) + k_{11}k_{21} - b_3 sC_3 R_{X3}(1- a_2-b_2 sC_2 R_{x2})}{|(a_3+b_3\, sC_3 R_{x3})(1-a_2-b_2 sC_2 R_{x2}) + k_{11}k_{21}|}$$

Considering the above two expression for the different topologies as

TOPOLOGY –A : In this topology , P terminal of both 2nd and 3rd MO-CCCII block is taken as Y and Q as X terminal i.e $a_2 = 0$, $a_3 = 0$, $b_2 = -1$, $b_3 = -1$ and considering $k_{11} = -1$ $k_{21} = 1$,the above reduced expression becomes

$$\frac{V_{OUT1}}{V_{in3}} = \frac{sCR_{X3}}{s^2C^2R_{X2}R_{X3}+sCR_{X3} + 1} \quad (\text{taking } C_2=C_3=C) \qquad (8.a)$$

$$\frac{V_{OUT2}}{V_{in3}} = \frac{1}{s^2C^2R_{X2}R_{X3}+sCR_{X3} + 1} \qquad (8.b)$$

The above both equations represents the valid filter expression , equation (8.a) is expression for band pass filter and expression (8.b) represents the low pass filter .

TOPOLOGY – B : In this topology , P terminal of 2nd MO-CCCII block is taken as X and P terminal of 3rd MO-CCCII block as Y terminal i.e $a_2 = 1$, $a_3 = 0$, $b_2 = 1$, $b_3 = -1$ and considering $k_{11} = k_{21} = -1$. The reduced equation becomes

$$\frac{V_{OUT1}}{V_{in3}} = \frac{sCR_{X3}}{s^2C^2R_{X2}R_{X3} + 1} \qquad (\text{taking } C_2 = C_3 = C) \qquad (8.c)$$

$$\frac{V_{OUT2}}{V_{in3}} = \frac{1}{s^2C^2R_{X2}R_{X3} + 1} \qquad (8.d)$$

TOPOLOGY – C : In this topology , P terminal of 2nd MO-CCCII block is taken as Y and Q terminal of 3rd MO-CCCII block as X terminal i.e $a_2 = 0$, $a_3 = 1$, $b_2 = -1$, $b_3 = 1$ and considering $k_{11} = k_{21} = 1$.The reduced expression becomes

$$\frac{V_{OUT1}}{V_{in3}} = \frac{sCR_{X3}}{s^2C^2R_{X2}R_{X3} + sC(R_{X3} + R_{X2}) + 2} \qquad (8.e)$$

$$\frac{V_{OUT2}}{V_{in3}} = \frac{sCR_{X3} + 2}{s^2C^2R_{X2}R_{X3} + sC(R_{X3} + R_{X2}) + 2} \qquad (8.f)$$

Equation (8.e) represents the band pass filter and equation (8.f) represents no valid expression

TOPOLOGY – D : In this topology , P terminal of both 2nd and 3rd MO-CCCII block is taken as X and Q as Y terminal i.e $a_2 = 1$, $a_3 = 1$, $b_2 = 1$, $b_3 = 1$ and considering $k_{11} = 1$, $k_{21} = -1$ .The reduced expression becomes

$$\frac{V_{OUT1}}{V_{in3}} = \frac{sCR_{X3}}{s^2C^2R_{X2}R_{X3} + sCR_{X2} + 1} \qquad (8.g)$$

$$\frac{V_{OUT2}}{V_{in3}} = \frac{sCR_{X3} + 1}{s^2C^2R_{X2}R_{X3} + sCR_{X2} + 1} \qquad (8.h)$$

The conclusion of above all the reduced expression is that the valid filter expression for both the node is achieved in two cases

1. For the transfer fuction(V/V) , when the voltage is applied at Q terminal of 2nd MO-CCCII block , the valid filter expression is derived for structure VIII and topology D where equation (7.g) represents low pass filter and (7.h) represents band pass filter.
2. For the transfer fuction (V/V) , when the input voltage is applied at the Q terminal of 3rd MO-CCCII block , the valid filter expression is derived for structure VIII and topology A where the equation (8.a) represents the band pass filter and (8.b) represents the low pass filter .

The above results are verified by simulation using PSPICE.

6.4 SIMULATION :

In this section , the derived results are verified using simulation results . The structure considered here is structure VIII .The block schematic diagram is considered twice , one with input voltage applied at the 2nd MO-CCCII block of structure VIII and topology D and other schematic block considered is input voltage applied at the 3rd MO-CCCII block of structure VIII and topology A By derivation , it was analyzed that two types of filter can be realized in transfer function, one is band pass filter and other is low pass filter .Simulation results for MO-CCCII are obtained at 2.5V supply , 100 μA biasing current I_0 and 0.35 μm technology .

The schematic block diagram of proposed circuit of structure VIII topology D with input voltage applied at the Q terminal of 2nd MO-CCCII is given below

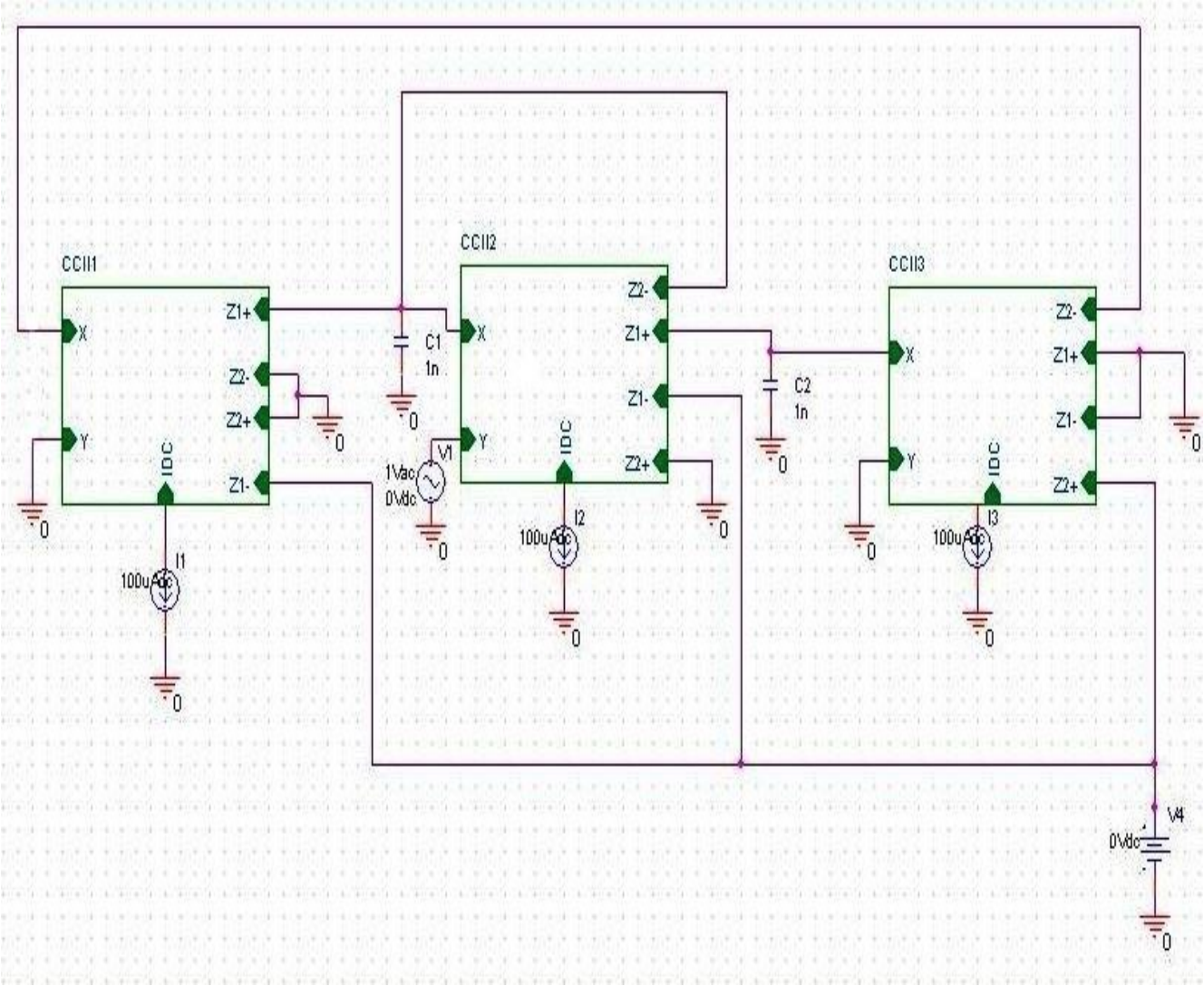

Fig 6.5 Schematic block diagram of structure VIII topology D with applied input voltage V_{in2}

So from the above structure two filters are possible , band pass and low pass filter . When the voltage ratio of node voltage 2^{nd} to the applied input voltage at 2^{nd} MO-CCCII block is considered , low pass filter is realized as shown in the graph shown in fig 6.6 .

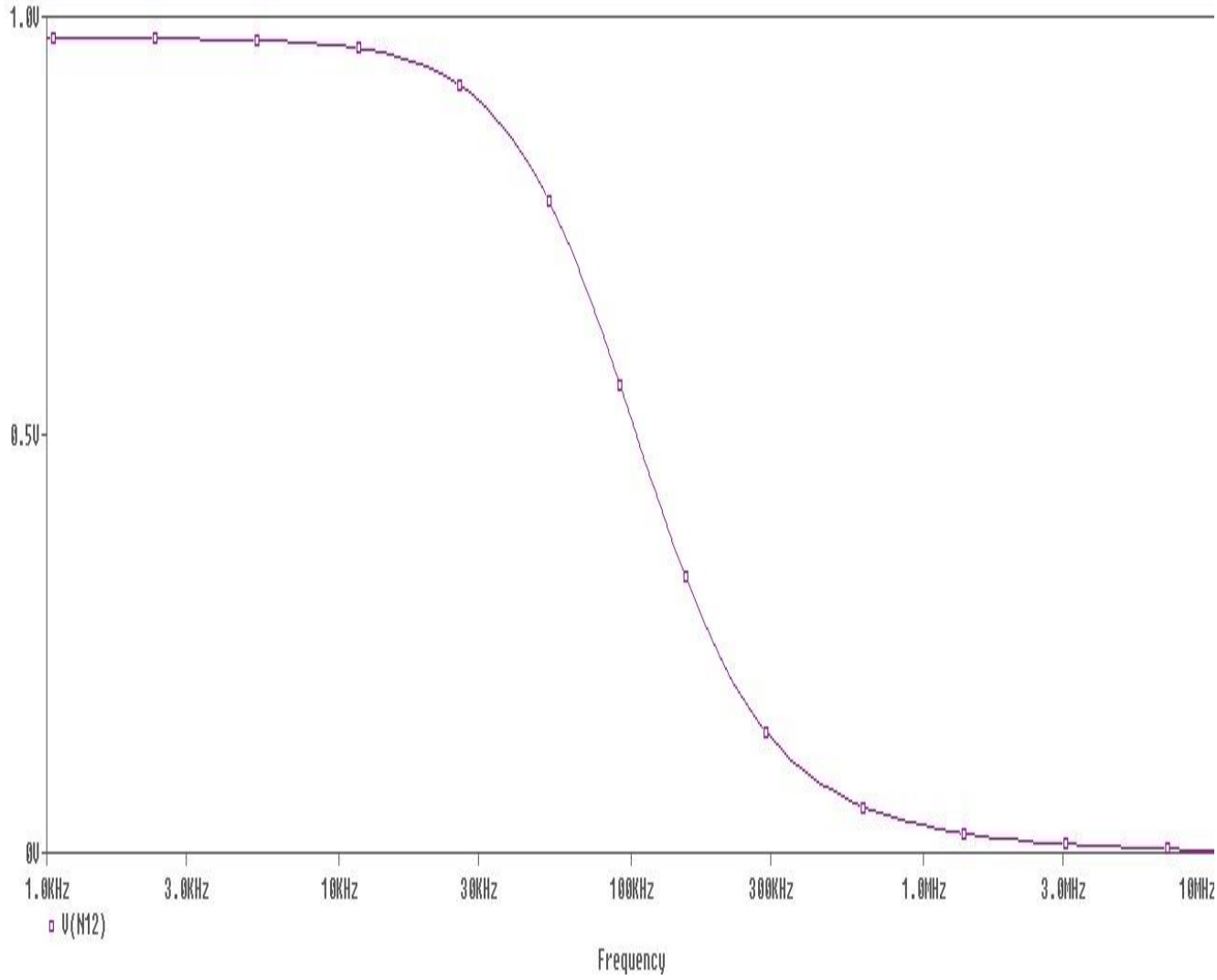

Fig 6.6 Graph of simulated structure VIII showing the low pass filter

The output node voltage at 2^{nd} node is represented by V(N12) .

When the voltage ratio of node voltage 3rd to the applied input voltage at 2nd MO-CCCII block is considered , band pass filter is realized as shown in the graph shown in fig 6.7 as

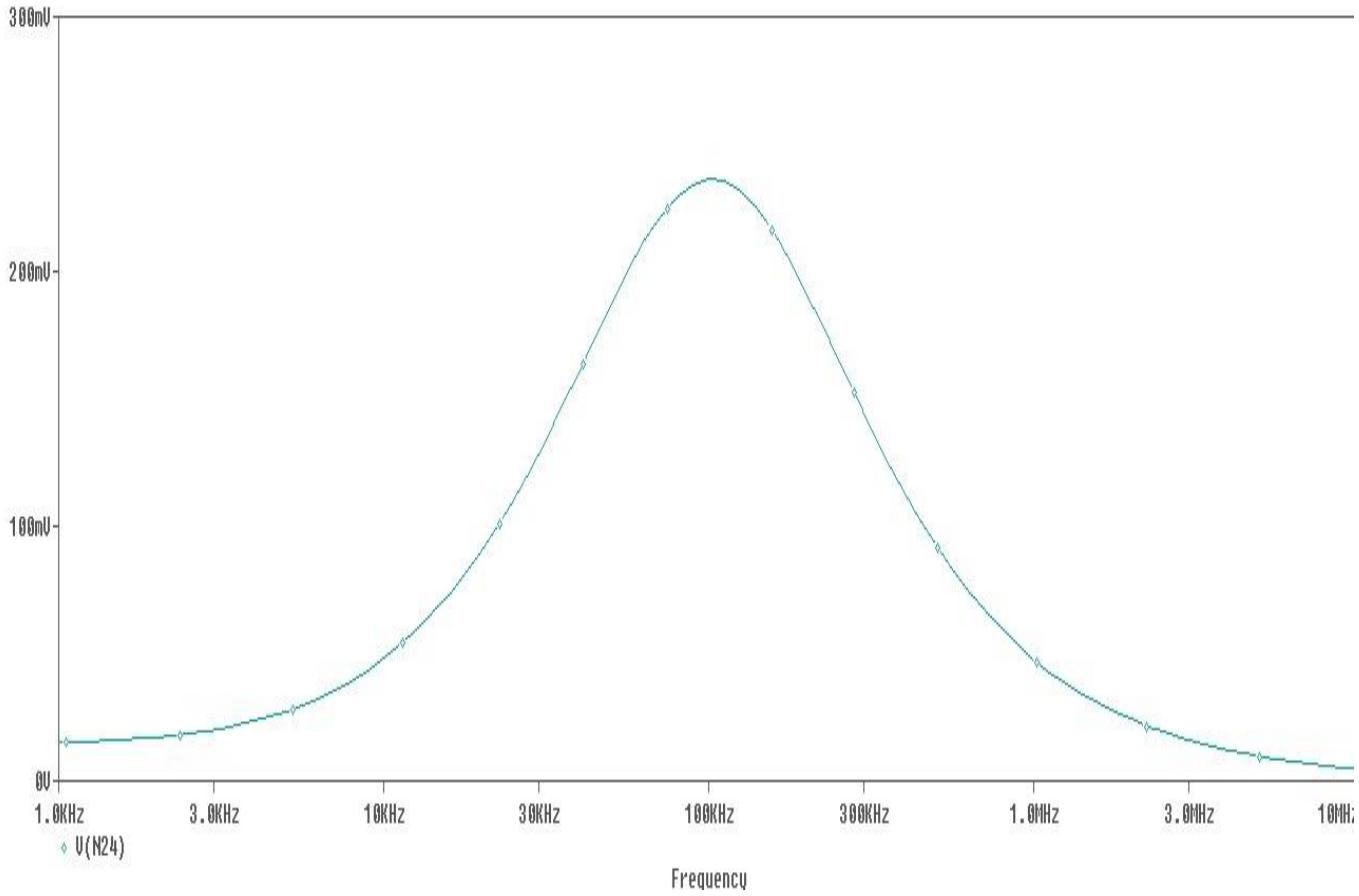

Fig 6.7 Graph of simulated structure VIII showing the band pass filter

The output node voltage at 3rd node (V_{OUT2}) is represented by V(N24) .

The schematic block diagram of proposed structure VIII topology A with applied input voltage at Q terminal of 3rd MO-CCCII block is given below as

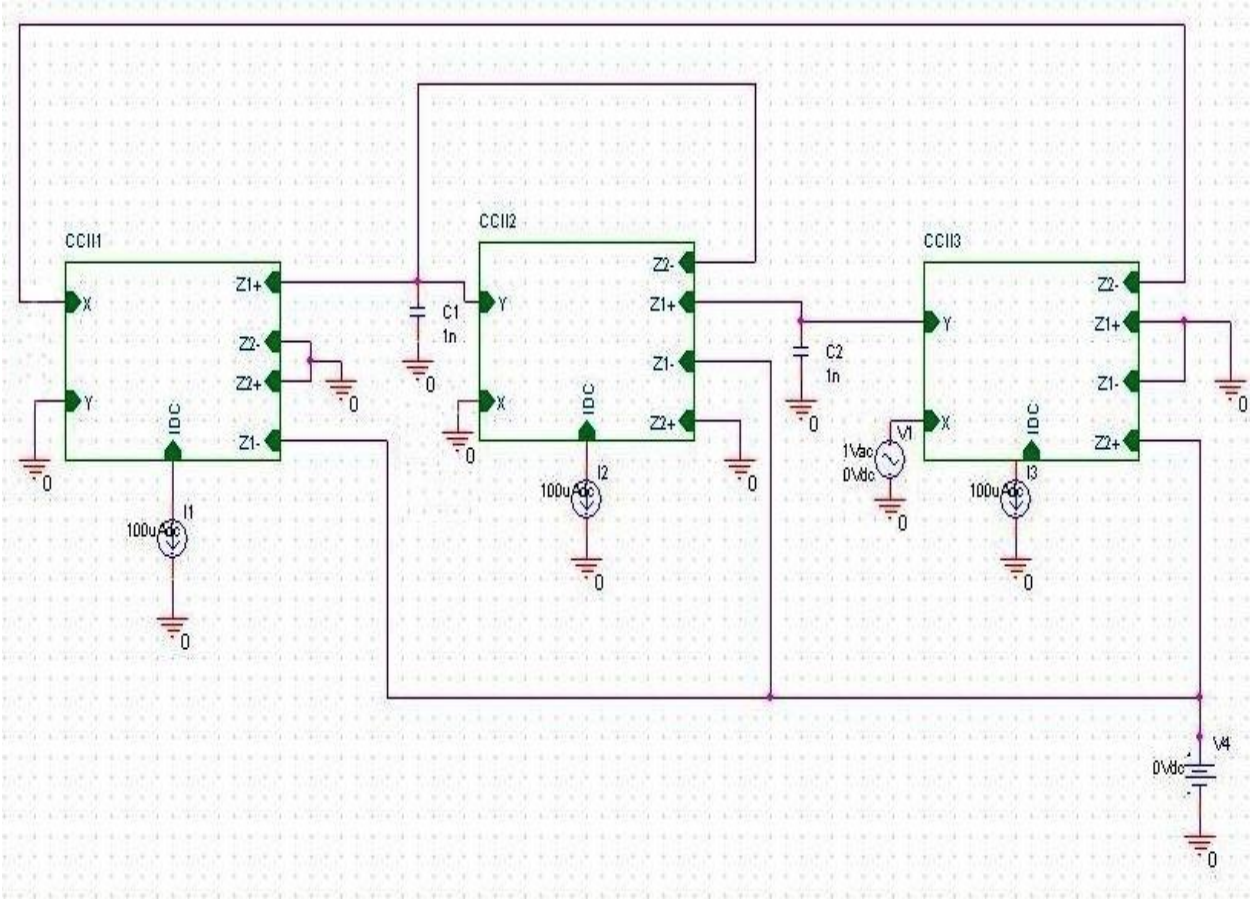

Fig 6.8 Schematic block diagram of structure VIII and topology A with applied input voltage V_{in3}

So from the above structure two filters are possible , band pass and low pass filter . When the voltage ratio of node voltage 2nd to the applied input voltage at 3nd MO-CCCII block is considered , band pass filter is realized as shown in the graph shown in fig 6.9 as

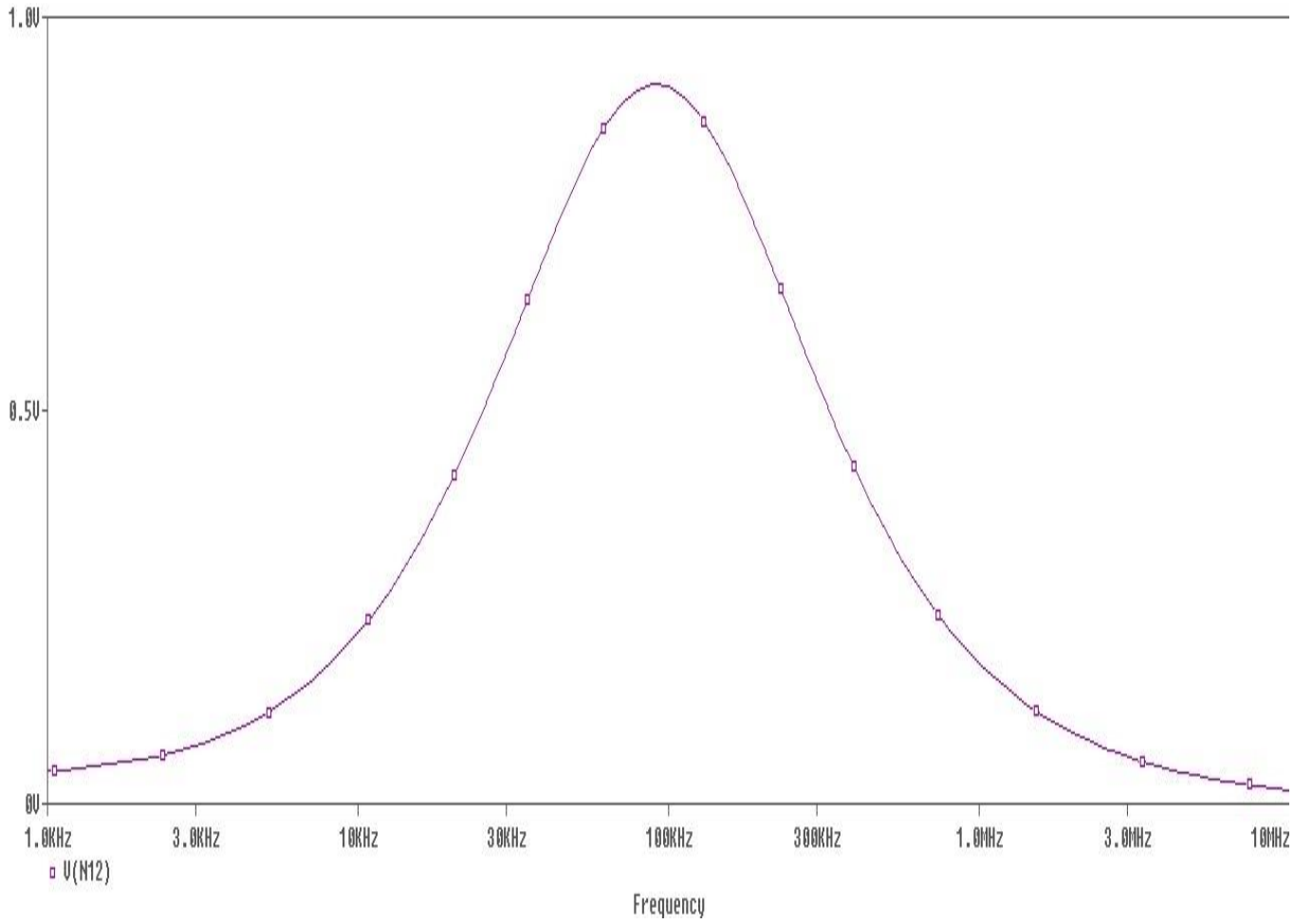

Fig 6.9 Graph of simulated structure VIII showing the band pass filter

When the voltage ratio of node voltage 3rd to the applied input voltage at 3nd MO-CCCII block is considered , low pass filter is realized as shown in the graph shown in fig 6.10 as

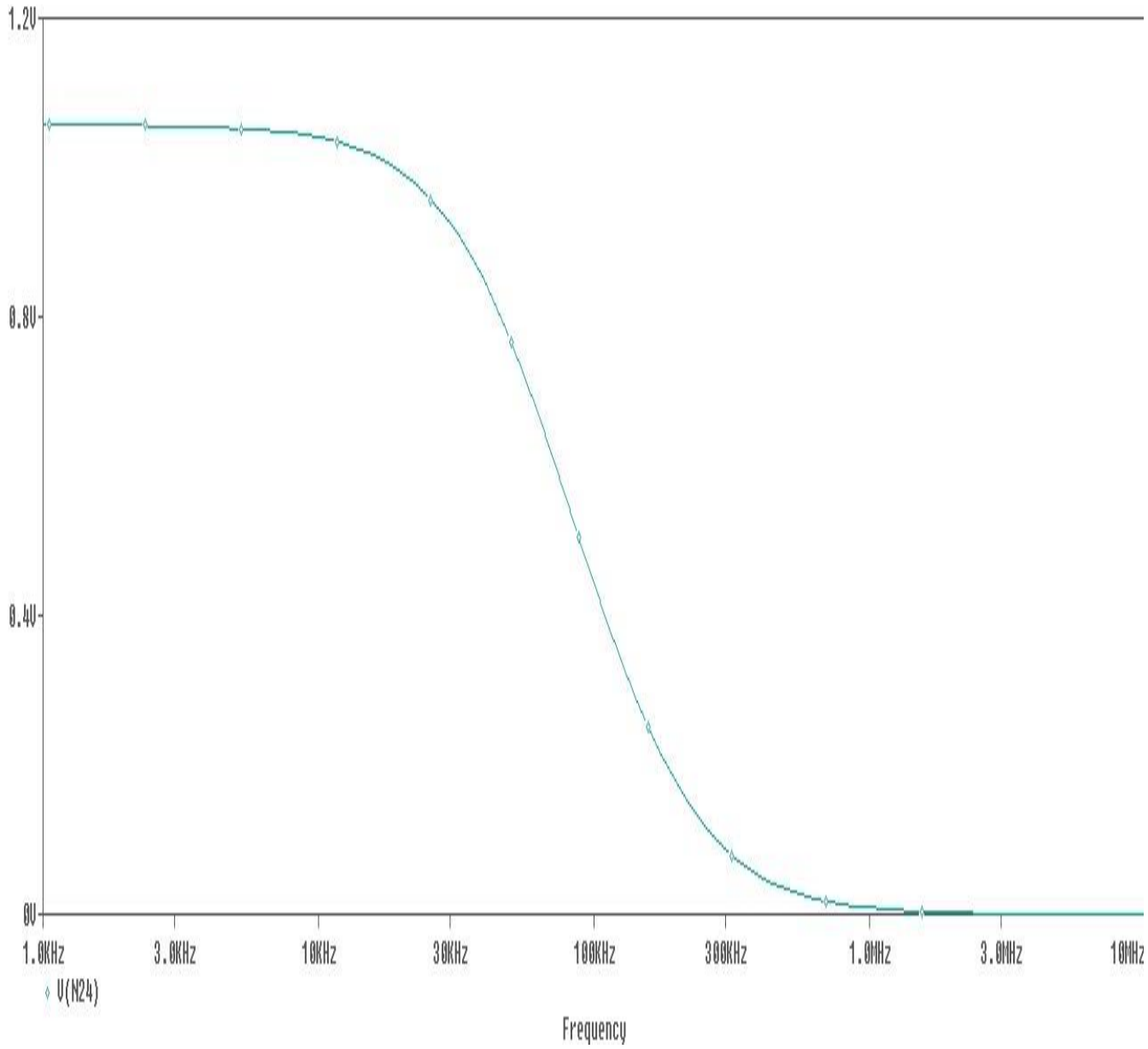

Fig 6.10 Graph of simulated structure VIII showing the low pass filter

REFERENCES

[1] Pandey, N., Paul, A. and Jain, S. B : Systematic generation and design of multiple loop feedback current controlled conveyor – grounded capacitor filter. *Journal of Active & Passive Electronic Devices; october 2012, Vol. 7 Issue 4, OUT171.*

CHAPTER 7

CONCLUSION

In this report universal filters are realized by taking current controlled conveyor as basic active block .The multi output current controlled conveyor (MO-CCCII) is used in the multiple loop feedback structure and universal filter are analysed in transresistance mode , transadmittance mode and voltage mode . This report is the extension of the multiple loop feedback current mode filter structure which is described in chapter 3 .The structure defining equations are verified and effect of biasing current on the equations are analysed using PSPICE simulation results are included in the chapter . The basic structure considered employs three MO-CCCII block and two capacitors is used for realization of filter in transresistance mode is explained in the chapter 4 and generalized expression of transresitance is derived for all the 12 defined structures and expression is verified on some structures and results are checked using PSPISCE simulation and it is observed that the results are in close agreement with theoretical propositions. The effect of non ideal behaviour of MO-CCCII has also been included in the proposed theory.In the chapter 5 , same structure is analysed for the realization of filters in transadmittance mode and generalized expression for transdmittance is derived and applied on structures and results are verified using PSPICE simulation and it is observed that the simulation results are in closed proximity to the theoretical derived results . Last chapter describes the defined structure (explained in chapter 3) in the voltage mode and generalized expression of transfer function in the form of V/V ratio is derived . The derived expression is applied on structures and valid filter expression are realized and results are checked using PSPICE simulation .The results came out to be very satisfactory according to the derived theoretical results . All the simulation have been carried out with MO-CCCII implemented in AMS .35 um CMOS technology with power supply of ± 2.5 V .

Appendix

Simulations have been performed using SPICE at 0.35um technology and the model files provided by MOSIS (AGILENT) used have the following parameters

.model NMOS

NMOS(Level=7 TOX=7.9E-9 NSUB=1E17 GAMMA=0.5827871 PHI=0.7 VTO=0.5445549 DELTA=0 U0=436.256147

+ETA=0 THETA=0.1749684 Kp=2.055786E-4 VMAX=8.309444E4 KAPPA=0.2574081 RSH=0.0559398 NFS=1E12 TPG=1 XJ=3E-7 LD=3.162278E-11

+WD=7.046724E-8 CGDO=2.82E-10 CGSO=2.8E-10 CGBO=1E-10 CJ=1E-3 PB=0.9758533 MJ=0.3448504 CJSW=3.777852E-10 MJSW=0.3508721)

.model PMOS

PMOS(Level=7 TOX=7.9E-9 NSUB=1E17 GAMMA=0.4083894 PHI=0.7 VTO=-0.7140674 DELTA=0 U0=212.2319801

+ETA=9.999762E-4 THETA=0.2020774 KP=6.733755E-5 VMAX=1.181551E5 KAPPA=1.5 RSH=30.0712458 NFS=1E12 TPG=-1 XJ=2E-7 LD=5.000001E-13

+WD=1.249872E-7 CGDO=3.09E-10 CGSO=3.09E-10 CGBO=1E-10 CJ=1.419508E-3 PB=0.8152753 MJ=0.5 CJSW=4.813504E-10 MJSW=0.5)