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Realization of Timer Circuit Using OTRA and Its Application

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CERTIFICATE

This is to certify that the dissertation titled "**Realization of Timer Circuit using OTRA and its Application**" is a bonafide record of work done by **Dheeraj Singh Rajput, Roll No. 2K12/VLS/04** at **Delhi Technological University** for partial fulfilment of the requirements for the degree of Master of Technology in VLSI and Embedded System Design. This project was carried out under my supervision and has not been submitted elsewhere, either in part or full, for the award of any other degree or diploma to the best of my knowledge and belief.

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ABSTRACT

The main objectives of this project are to study and design a simple, portable, and low cost timer and the limitations of the commercially available 555 Timer has been overcome. The presented topology uses two operational transresistance amplifier (OTRA). The proposed circuits are insensitive to parasitic capacitances and resistances due to internally grounded input terminals of OTRA. Low output impedance of the configuration enables the circuits to be cascaded without additional buffers.

The OTRA is suitable for analog VLSI applications since it does not suffer from constant gain bandwidth product. Hence, it can exhibit wide bandwidth at high gain values.
The operational transresistance amplifier (OTRA) is an amplifier which provides an output voltage with inputs as two differential currents. Thus, it is a current controlled voltage source. The transresistance required is very high so as to realize open loop circuits such as comparator and closed loop circuits such as filters.

With the help this timer circuit similar application can be design as with the 555 timer circuit overcoming the drawback. Under this project by using this timer circuit three applications Astable multivibrator, monostable multivibrator and pulse width modulator circuits have been implemented. The performance of the proposed Timer IC circuits is verified through PSPICE simulation using 0.5 μm CMOS process parameters provided by MOSIS (AGILENT).
Keywords: OTRA, Timer circuit, Astable multivibrator, monostable multivibrator and pulse width modulator.

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CHAPTER-1

INTRODUCTION

1.1 INTRODUCTION

The voltage and current at specified points in the circuits of analog chips vary continuously in time. In contrast, digital chips only use and create voltages or currents at discrete levels, with no intermediate values. In addition to Transistors, analog chips often have a larger number of passive elements (Inductor/Capacitors/Resistors) than digital chips typically do. Inductors tend to be avoided because of their large size. It was one of those fortunate discoveries that a transistor and capacitor together can do the work of an inductor. When this trick is used in a CFL, you get an electronic ballast.

Analog chips may also contain digital logic elements to replace some analog functions, or to allow the chip to communicate with a microprocessor. For this reason and since logic is commonly implemented using CMOS technology, these chips use BiCMOS processes by companies such as Free scale, Texas Instruments, STMicroelectronics and others. This is known as mixed signal processing and allows a designer to incorporate more functions in the chip. Some of the benefits include load protection, reduced pats count and higher reliability [1].

Pure analog chips in information processing have been mostly replaced with digital chips. Analog chips are still required for wideband signals on account of sampling rate requirements, high power applications and at the transducer interfaces. Research and industry in the field continues to grow and prosper. Some examples of long-lived and well-known analog chips are the 741 Operational Amplifiers, and the 555 timer.

Power supply chips are also considered to be analog chips. Their main purpose is to produce a well-regulated output voltage supply for other chips in the system. Since all electronic systems require electrical power, power supply ICs PMICs are important elements of those systems.

The Timers IC is one of the most important elements used in the process analog industry. Generally operational amplifiers are usedto design classical analog Timers. However the operational amplifiers, being voltagemode circuit, have their own limitation of constant gain

bandwidth product and low slewrate. Current mode building blocks such as Current Conveyor, OTA, CDBA, CDTA,OTRA etc. have larger bandwidth, dynamic range, and also greater linearity than theirvoltage-mode counterparts, op-amps [6].These active blocks therefore would be a bettersubstitute of OPAMP for designing the analog controllers.Operational Transresistance Amplifier (OTRA) is a high gain current input, voltage output amplifier [5]. OTRA being a current mode building block inherits the advantagesof current mode processing as well as it is free from parasitic input capacitances andresistances as its input terminals are virtually grounded and hence, non-ideality problemis less in circuits implemented using OTRA. In literature, OTRA based Timer IC has not been reported so far.

In low power analog applications, the effect of noise is prominent. To reduce the effect of noise on the circuits, designers of analogue ICs usually build their circuitry as differential rather than single-ended structure.

THE 555 TIMER is a universally accepted device for thegeneration of clock waveforms, single pulses, or pulse widthor frequency modulation.The data sheets furnished by the various manufacturers ofthis device provide a schematic and a logic diagram of itsconfiguration, along with a set of formulas for selecting thevalues of the external components needed for fixed monostableor astable operation. It is also suggested that the application ofan external voltage signal at pin 5 modulates the generatedpulse width or frequency.After a brief description of the internal configuration, thepaper analyzes the performance of the Timer and derivesexpressions for the design of fixed monostable and astablecircuits. After further analysis, practical nomograms for the design of modulated monostable and astable circuits are presented.

1.2 MOTIVATIOIN

Analog Integrated Circuit Design using CMOS non linear circuit become increasingly important with growing opportunities. Coupled with the various technological improvements such as the continuously shrinking feature size of the devices on IC's and the most attractive reduction of power supply voltages and power dissipation. This has led to creation of alternate analog design techniques.

The whole history of integrated circuits has followed a trend of descending supply voltage. The demand for circuits that can operate at very low power supply voltages (i.e., between 1 and 2 V)

is very high, Most important are the battery-operated systems [1]. In particular, they are of crucial Importance for Instrumentation, Automatic Control, Function Generators, Frequency Synthesizers and Communication.

The information processed by lumped electric networks can be represented by either the nodal voltages or branch currents of the networks. The former are referred to as voltage-mode circuits whereas the latter are known as current-mode circuits. Together, they provide a complete characterization of the behavior of the networks [2].

Historically analog design was viewed as a voltage dominated form of signal processing. This is apparent from the fact that current signals were transferred into voltage domain before any analogue signal processing could be done. But due to the advances in the process technology a shift is made to current mode of signal processing. Analog IC design is receiving a tremendous boost from the development and application of current mode processing which has an inherent performance feature of wider bandwidth [2].

Timer IC is the CMOS version of the industryStandard 555 series general purpose timers. Less than 1 mw Typical Power Dissipation at5V Supply. 1.5V Supply Operating Voltage Ensured. Reduced Supply Current Spikes during Output as a one-shot, the time delay is precisely controlled Transitions. Extremely Low Reset, Trigger, and Threshold Currents. Excellent Temperature Stability.

This theses deals with the design of a timer circuit for a very low power supply voltage in a standard CMOS process.

The OTRA is suitable for analog VLSI applications since it does not suffer from constant gain bandwidth product. Hence, it can exhibit wide bandwidth at high gain values.

In this theses with the help this timer circuit along with OTRA monostable multivibrator, astable multivibrator and pulse width modulator is proposed. The schematics of the proposed along with a set of formulas for selecting the values of the external components needed for fixed monostable, astable multivibrator and pulse width modulator are provided.

1.3 CURRENT MODE ANDVOLTAGE SIGNAL PROCESSING

Analog signal processing will remain irreplaceable for the implementation of interface circuitry between digital processing and the external world. It also competes with digital signal processing with respect to speed and silicon area, which makes it more economic in many cases. Current-mode analog signal processing [3][4] has recently gained prominence because of its capability to minimize voltage swings, resulting in increased signal handling capability even at reduced supply voltages. This makes it suitable to be employed in mixed analog-digital IC's operating at supply voltages of 3.3v, which is likely to become the future CMOS industrial standard.

With the evolution of submicron technologies such as 0.18 micron and 0.13 micron, the supply voltages have been reduced to 1.5Volts and lower. This makes it difficult to design a voltage mode CMOS circuits with high linearity and wide dynamic range. Recently, current mode circuits have become a viable alternative for future applications because of their inherent advantages over voltage mode circuits [5].

The main advantage of using current mode technique is because the non-linear characteristics exhibited by most field effect transistors. A small change in the input or controlling voltage results in a much larger change in the output current. Thus for a fixed supply voltage, the dynamic range of a current mode circuit is much larger than that of a voltage mode circuit. If a supply voltage is lowered, one can still get the required signals represented by the current.

A second advantage of current mode circuits is that they are much faster as compared to voltage mode circuits. The parasitic capacitances present in the analog circuits must be charged and discharged with the changing voltage levels. In a current mode circuit, a change in current level is not necessarily accompanied by a change in the voltage level. Hence, the parasitic capacitances will not affect the operating speed of the circuit by a significant amount.

Other advantages of using current mode circuits are that they do not require specially processed capacitors or resistors; they are more compatible with digital CMOS technology making integration of mixed signal circuits more feasible. Due to all the advantages of current mode analogue signal processing there has been an emergence of new analogue building blocks ranging from the current conveyor, OTA, OTRA and current feedback op-amps through to sampled data current circuits such as dynamic current mirrors and analogue neural networks.

Organization of thesis:

The theses are organized as follows:

CHAPTER-2: It describes the various blocks used in analog design. The circuit diagrams and equations of blocks are described.

CHAPTER-3: In this chapter Literature Survey of OTRA and timer circuit has been described.

CHAPTER-4: It describes the basics of OTRA, and differential OTRA. It further describes their internal circuit structures. Terminal characteristics of these circuits have been verified through PSPICE simulations**.**

CHAPTER-5: This chapter deals with the Timer Circuit Using Operational Amplifier and its applications as astable, monostable and pulse width modulator.

CHAPTER-6: This chapter describes the Proposed Timer Circuit Using OTRA and its applications as astable, monostable and pulse width modulator and the simulation results of the circuits proposed in this dissertation. Workability of the proposed circuits are verified through PSPICE simulations using 0.5μm AGILENT CMOS process parameter.

REFERENCE

[1].http://www.fairchildsemi.com/an/AN/AN-88.

[2].CMOS Current-Mode Circuits for Data Communications - Fei Yuan

[3]. A.F. Arbel, "A Unified Approach to the Design of Nuclear Instrumentation used in Low and High Energy Physics", D.Sc. Thesis, Technion-Israel Institute of Technology, 1966.

[4]. Analogue IC Design: The Current-Mode Approach. Edited by C. Toumazou et al., Peter Peregrinus Ltd., London, 1990.

[5]. Toumazou C, Lidjey FJ, Haigh D. Analog IC design: the current-mode approach. Peter Peregrinus, UK: Exeter; 1990.

[6]. Chen, J. J., Tsao H. W., Chen, C. C. Operational transresistance amplifier UsingCMOS Technology.Electronics Letters. 1992, vol. 28, no. 22, p. 2087–2088

CHAPTER-2

BLOCKS USED IN ANALOG DESIGN

2.1 TRANSIMPEDANCE AMPLIFIER

Transimpedance amplifier [1] consists of an inverting amplifier accepting the input signal in form of a current from a high impedance signal source, such as a photodiode or a semiconductor based detector for radiation particles, and converts it into an output voltage. The Transimpedance at DC and low frequencies is $\frac{v_o}{i} = R_f$. However, the high impedance signal source inevitably has a stray capacitance C_i , which deprives the amplifier from the feedback at high frequencies. Therefore the amplifier's feedback loop must be stabilized by a suitably chosen phase margin compensation capacitance C_f . Owed to the presence of these capacitances, and because of the amplifier's own limitations, the system response at high frequencies will be reduced accordingly.

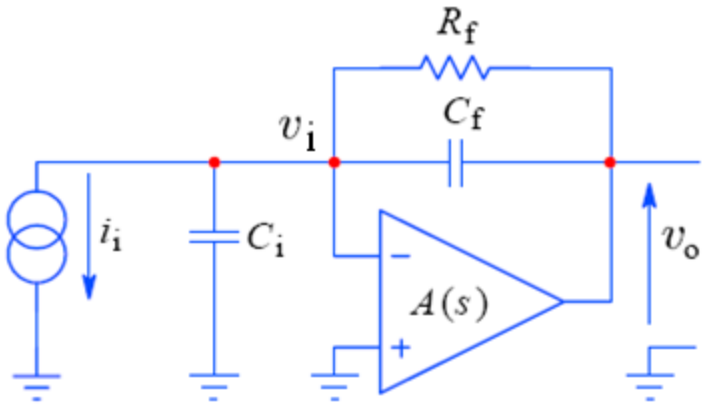


Figure 2.1Generalized Transimpedance system schematic diagram

The amplifier's inverting open loop voltage gain is modeled as:

$$\frac{v_o}{v_i} = -A(s) = -Ao\frac{-So}{S-So} = -Ao\frac{\omega o}{S+\omega o} \qquad (2.1)$$

where: S is the complex frequency variable;

A_O is the amplifier's open loop DC gain;

S_O is the amplifier's real dominant pole, so that:

$\omega o = 2\pi f_O$, f_o is the open loop cutoff frequency

2.2 OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

The operational transconductance amplifier (OTA) is an amplifier whose differential input voltage produces an output current [2]. Thus, it is a voltage controlled current source (VCCS). There is usually an additional input for a current to control the amplifier's transconductance. The OTA is similar to a standard operational amplifier in that it has a high impedance differential input stage and that it may be used with negative feedback.

The OTA is not as useful by itself in the vast majority of standard op-amp functions as the ordinary op-amp because its output is a current. One of its principal uses is in implementing electronically controlled applications such as variable frequency oscillators and filters and variable gain amplifier stages which are more difficult to implement with standard op-amps. In the ideal OTA, the output current is a linear function of the differential input voltage, and is given by:

(2.2a)

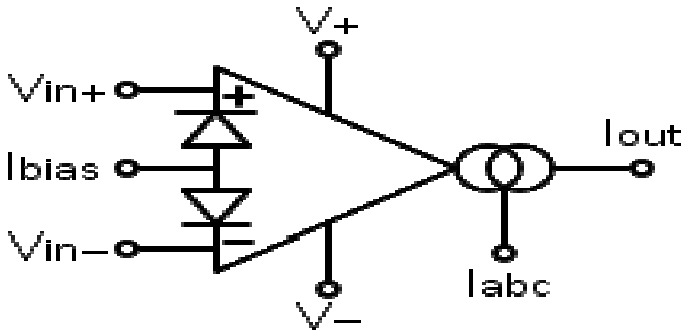


Figure 2.2 OTA Model

The amplifier's output voltage is the product of its output current and its load resistance:

(2.2b)

The voltage gain is then the output voltage divided by the differential input voltage:

(2.2c)

The transconductance of the amplifier is usually controlled by an input current, denoted I_{abc} . The amplifier's transconductance is directly proportional to this current. This is the feature that makes it useful for electronic control of amplifier gain, etc.

As an ideal OTA is usually considered to have the following properties and they are considered to hold for all input voltages:

- Infinite input impedance
- Infinite output impedance (i.e., $R_{out} = \infty$).
- $G_m$is variable and $G_m = \frac{I_{abc}}{2V_T}$, we cannot make $G_m$infinite.

2.3 CURRENT FEEDBACK OPERATIONAL AMPLIFIER

The current feedback operational amplifier (CFOA) is a type of electronic amplifier whose inverting input is sensitive to current, rather than to voltage as in a conventional voltage-feedback operational amplifier (VFA). The CFA was invented by David Nelson at Collinear Corporation, and first sold in 1982 as a hybrid amplifier, the CLC103. The first integrated circuits CFAs were introduced in 1987 by both Collinear and Elantec (designer Bill Gross). They are usually produced with the same pin arrangements as VFAs, allowing the two types to be interchanged without rewiring when the circuit design allows. In simple configurations, such as linear amplifiers, a CFA can be used in place of a VFA with no circuit modifications, but in other cases, such as integrators, a different circuit design is required. The circuit symbol of CFOA is as shown in fig.2.3. Its port relations can be characterized by the following matrix form:

$$\begin{bmatrix} I_y \\ V_x \\ I_z \\ V_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \\ I_o \end{bmatrix}$$

Therefore, this active element can be characterized with the following equations:

$$i_y=0,\ v_x = v_y,\ i_{z=i_x},\ v_o = v_z \qquad (2.3)$$

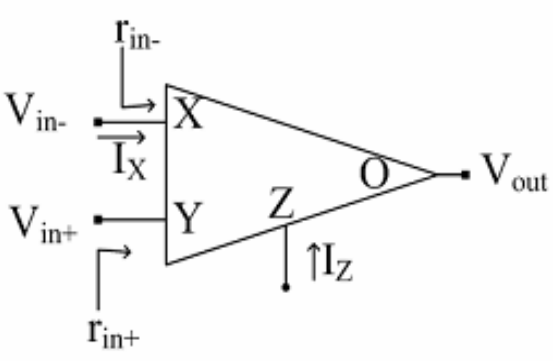


Fig.2.3 Circuit Symbol of CFOA

Current-Feedback Operational Amplifiers (CFOAs) are employed as an alternative to conventional voltage opamps because of their inherent advantages:

- The CFOA closed-loop bandwidth is independent of its close-loop gain, provided that the feedback resistance is kept constant
- The CFOA input and output stages work both in class AB and give high slew-rate values AD844A is CFOA chip which is commercially available in the market.

2.4 OPAMP

An operational amplifier, which is often called an op-amp, is a DC-coupled high-gain electronic voltage amplifier with a differential input and, usually, a single-ended output. Ideally the op-amp amplifies only the difference in voltage applied between its two inputs (V_+ andV_-), which is called the differential input voltage. The output voltage of the op-amp is given by the equation,

$$V_{out} = (V_+ - V_-).G_{open-loop} \quad (2.4)$$

Where V_+ is the voltage at the non-inverting terminal and V_- is the voltage at the inverting terminal and G open-loop is the open-loop gain of the amplifier.

The ideal operation is difficult to achieve and the non-ideal conditions often raise limitations like finite impedances and drift, their primary limitation being not especially fast. The typical performance degrades rapidly for frequencies greater than 1MHz, although some models are designed especially for higher frequencies. High input impedance at the input terminals (ideally infinite) and low output impedance at the output terminal(s) (ideally zero) are important typical characteristics. The other important fact about op-amps is that their open-loop gain is huge. This

is the gain that would be measured from a configuration in which there is no feedback loop from output back to input. A typical open-loop voltage gain is ~ 10^4 -10^5 .

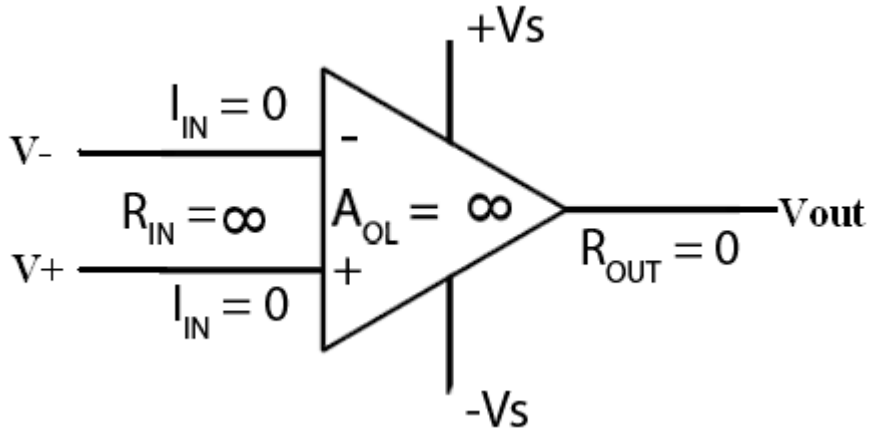


Figure 2.4 Ideal internal circuit of Op-amp

An ideal op-amp is usually considered to have the following properties, and they are considered to hold for all input voltages:

- Infinite open-loop gain.
- Infinite voltage range available at the output (V_{out}) (in practice the voltages available from the output are limited by the supply voltages Vs_+ andVs_-)
- Infinite bandwidth
- Infinite input impedance
- Zero input current
- Zero input offset voltage
- Infinite slew rate
- Zero output impedance
- Infinite Common-mode rejection ratio (CMRR)
- Infinite Power supply rejection ratio for both power supply rails.

2.5 CURRENT CONVEYOR

The current conveyor (CC) is the basic building block of a number of applications both in the current and voltage and the mixed modes. The principle of the current conveyor of the first generation was published in 1968 by K. C. Smith and A. S. Sedra [3]. Two years later, today's widely used second-generation CCII was described in [4], and in 1995 the third-generation CCIII [5]. However, initially, during that time, the current conveyor did not find many applications because its advantages compared to the classical operational amplifier were not widely appreciated. An IC Current Conveyor, namely PA630, was introduced by Wadsworth in 1989 and about the same time, the now well known CFOA AD844 was recognized to be internally a CCII+ followed by a voltage follower [6]. Today, the current conveyor is considered a universal analog building block with wide spread applications in the current mode, voltage mode, and mixed mode signal processing. Several generations of current conveyors have been defined over the years. Undoubtedly, the second generation conveyor (CCII) is the more well known of the device. The terminal relations of a CCII can be characterized by

$$\begin{bmatrix} V_x \\ I_y \\ I_z \end{bmatrix} = \begin{bmatrix} \beta & 0 & 0 \\ 0 & 0 & 0 \\ 0 & \pm\alpha & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix}$$

where $\alpha = 1 - \epsilon_i$ and $\beta = 1 - \epsilon_v$,$| \epsilon_i | << 1$ and $| \epsilon_v | << 1$ (2.5)

represent the current and voltage tracking errors, respectively, where the subscripts x, y, and z refer to the terminals labeled X, Y and Z in fig1 The CCII is defined in both a positive and a negative version where the +sign in the matrix is used for the CCII+ type conveyor and the –sign is used for the CCII- type conveyor. Its features find most applications in the current mode, when its voltage input y is grounded and the current, flowing into the low-impedance input x, is copied by a simple current mirror into the z output.

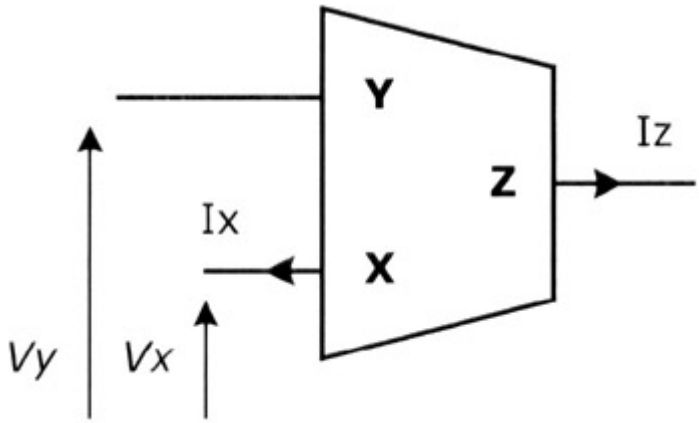


Fig 2.5 Block diagram of CCII

2.6 OPERATIONAL TRANSRESISTANCE AMPLIFIER

As signal processing extends to higher frequencies, traditional design methods based on voltage op-amps are no longer adequate. It is well known that a traditional operational amplifier has bandwidth which is dependent on the closed-loop voltage gain. The attempt to overcome this problem has led to a renewed interest in circuits which operate in current mode.

The OTRA is a current mode device that uses current mirrors and common source amplifier to give a current difference signal as input which in turn produce an appropriate voltage signal as output. The OTRA is a three terminal analog building block. Both the input and output terminals are characterized by low impedance. The circuit symbol of the OTRA is illustrated in Fig.2.6. The port relations of an OTRA can be characterized by the following matrix form [7].

$$\begin{bmatrix} v_p \\ v_n \\ v_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{bmatrix} \begin{bmatrix} i_p \\ i_n \\ i_z \end{bmatrix}$$

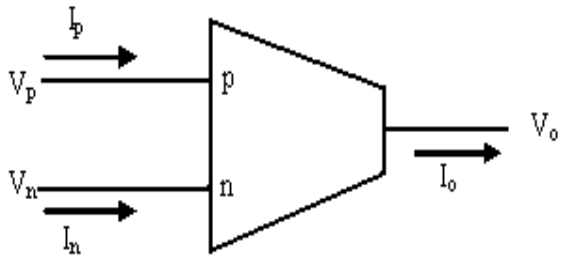


Fig 2.6 Circuit symbol of OTRA

It eliminates response limitations incurred by capacitive time constants leading to circuits that are insensitive to the stray capacitances at the input terminals. For ideal OTRA, the Transresistance gain, R_m, approaches infinity and external negative feedback must be used which forces the input currents to be equal [8]. Thus the OTRA must be used in a negative feedback configuration. Practically the Transresistance gain is finite and its effect should be considered.

The important advantages offered by OTRA are:

- Since the OTRA has one output terminal with low impedance and two input terminals that are virtually grounded, most effects of parasitic capacitances disappear and the remainder can be compensated without adding any extra components.
- Using current feedback techniques, OTRAs have a bandwidth almost independent of the closed loop-voltage gain.
- Due to the input terminals being virtually grounded, they are cascadable.

2.7 CURRENT DIFFERENCING TRANS-CONDUCTANCE AMPLIFIER

Current differencing transconductance amplifier (CDTA) is a new active circuit element. The CDTA is free from parasitic input capacitances and it can operate in a wide frequency range due to current mode operation. Some voltage and current mode applications using this element have already been reported in literature, particularly from the area of frequency filtering: general higher-order filters, biquad circuits, all-pass sections, gyrators, simulation of grounded and floating inductances and LCR ladder structures. Other studies propose CDTA-based high-frequency oscillators. Nonlinear CDTA applications are also expected, particularly precise rectifiers, current-mode Schmitt triggers for measuring purposes and signal generation, current-mode multipliers, etc.

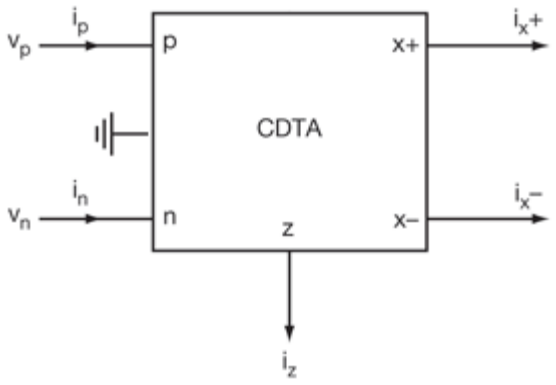


Figure 2.7 Block diagram of CDTA

The CDTA element with its schematic symbol in Fig 2.7 has a pair of low-impedance current inputs p, n and an auxiliary terminal z, whose outgoing current is the difference of input currents. Here, output terminal currents are equal in magnitude, but flow in opposite directions, and the product of transconductance (g_m) and the voltage at the z terminal gives their magnitudes. Therefore, this active element can be characterized with the following equations:

1. $V_P = V_N = 0$, (2.6a)
2. $I_Z = I_P - I_N$ (2.6b)
3. $I_{X+} = g_m V_Z$ (2.6c)
4. $I_{X-} = -g_m V_Z$. (2.6d)

Where $V_{Z-} = I_Z Z_Z$ and Z_Z is the external impedance connected to z terminal of the CDTA. CDTA can be thought as a combination of a current differencing unit followed by a dual-output operational transconductance amplifier, DO-OTA. Ideally, the OTA is assumed as an ideal voltage-controlled current source and can be described by$I_X = g_m(V_+ - V_-)$, where I_X is output current, V_+ and V_- denote non-inverting and inverting input voltage of the OTA, respectively. Note that g_m is a function of the bias current. When this element is used in CDTA, one of its

input terminals is grounded (e.g., V_- = 0V). With dual output availability, $I_{X+} = -I_{X-}$ condition is assumed.

2.8 CURRENT DIFERENCING BUFFERED AMPLIFIER

CDBA, current differencing buffered amplifier, is a multi-terminal active component with two inputs and two outputs [9]. Its block diagram can be seen from figure 2.8. It is derived from current feedback amplifier (CFA).

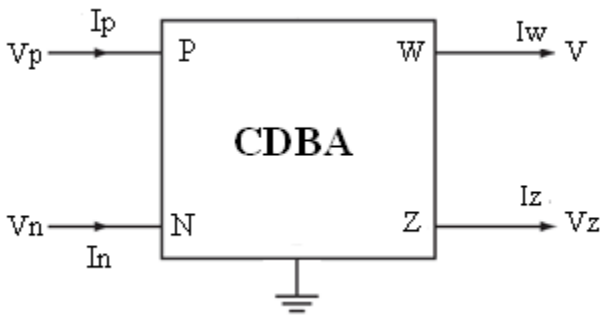


Figure 2.8 Block Diagram for CDBA

The characteristic equation of this element can be given as:

1. $V_P = V_N = 0$ (2.7a)
2. $I_Z = I_P - I_N$ (2.7b)
3. $V_W = V_Z$ (2.7c)

Here, current through z-terminal follows the difference of the currents through p-terminal and n-terminal. Input terminals p and n are internally grounded. The difference of the input currents are converted into the output voltageV_W, therefore CDBA element can be considered as a special type of current feedback amplifier with differential current input and grounded y input.

The CDBA is simplifying the implementation, free from parasitic capacitances, able to operate in the frequency range of more than hundreds of MHz (even GHz), and suitable for current mode operation while, it also provides a voltage output. Several voltage and current mode continuous-

time filters, oscillators, analog multipliers, inductance simulators and a PID controller have been developed using this active element.

The CDBA offers several advantageous features viz., high slew rate, improved bandwidth, and accurate port tracking characteristics when configured with a pair of matched current feedback amplifier (AD-844-CFA) devices which leads to extremely low active circuit sensitivity.

REFERENCES

[1] B.Razavi, Design of Analog CMOS Integrated circuits: McGraw-Hill, 2001.

[2] A 0.8-V 0.25-mW Current-Mirror OTA With 160-MHz GBW in 0.18μm CMOS – TsungHsien Lin, IEEE feb 2007.

[3] SMITH, K.C., SEDRA, A. The current conveyor: a new circuit building block. *IEEE Proc.* CAS, 1968, vol. 56, no. 3, p. 1368-1369.

[4] SEDRA, A.S., SMITH, K.C. A second generation current conveyor and its application. *IEEE Trans*., 1970, CT-17, p. 132-134.

[5] FABRE, A. Third generation current conveyor: A new helpful active element. *Electron. Lett.*, 1995, vol. 31, no. 5, p. 338–339.

[6] WADSWORTH, D.C. Accurate current conveyor topology and monolithic implementation. *Proc. IEE G*, 1990, vol. 137, no. 2, p. 88-94.

[7] J.J. Chen, H.W. Tsao, and C. Chen, "Operational transresistance amplifier using CMOS technology." *Electronics Letters*, vol. 28, no. 22, pp. 2087–2088, 1992.

[8] K.N. Salama and A.M. Soliman, "CMOS operational transresitance amplifier for analog signal processing applications." *Microelectronics Journal*, vol. 30, pp. 235–245, 1999.

[9] Microelectronics Journal 30 (1999) 157–160 'A new versatile building block: current differencing buffered amplifier suitable for analog signal-processing filters'

[10] Hassan Mostafa, Ahmed M. Soliman, A modified CMOS realization of the operational transresistance amplifier (OTRA) ."Frequenz, 60, pp. 70–76, 2006.

[11] U.Cam,C.Cakir and OguzhanCicekoglu,"Novel transimpedance type first order all-pass filter using single OTRA." *AE U—International Journal of Electronics and Communications*, vol. 58, pp. 296–298, 2004.

CHAPTER-3

LITERATURE SURVEY

OTRA is the basic building block of a number of applications both in current and voltageand mixed modes. The first CMOS circuit of OTRA was introduced in 1992 by J. J.Chen, H. W. Tsao & C. C. Chen [1]. Reference [2] 1995 shows that the input terminals of OTRA being virtually grounded, the circuits designed using OTRA were insensitive to stray capacitances [2]. In 1999 Salama and Ahmed M. Soliman introduced a simple CMOS realization of OTRA based on cascaded connection of modified differential current conveyor (MDCC) and a common source amplifier [3]. In [4] they proposed a new circuit based on same cascaded connection of modified differential current conveyor (MDCC) and a common source amplifier as in [3] but with improved performance and less number of transistors. The Circuit proposed in [5] is based on same input stage of OTRA proposed in [6] and a differential gain stage is used instead of the single common source amplifier and a compensation circuit is used to compensate difference between the two drain voltages of input transistors. The circuit proposed in [7] is another modification of circuit presented in [6] where differential gain stage is used instead of the single common source amplifier. Several other CMOS realizations of OTRA are also available in literature [8-10]. Circuit presented in [8] consists of a differential current controlled current source (DCCCS) followed by a voltage buffer whereas circuit reported in [9] is made of R_m cell, feedback network and output driver. A low voltage regulated cascade current mirror with a low voltage regulated cascode load forms core of the circuit proposed in [10]. OTRA is commercially available from several manufacturers under thename current differencing or Norton amplifier, [11-13]. Various applications of OTRA also exist in literature. Filters using OTRA are proposed in [2-3, 12-17] and oscillators & multi vibrators are presented in [14-19] whereas Schmitttrigger is presented in [20].

The 555 timer IC was first introduced around 1971 by the Signetics Corporation as the SE555/NE555 and was called "The IC Time Machine" and was also the very first and only commercial timer IC available. It provided circuit designers with a relatively cheap, stable, and user-friendly integrated circuit for both monostable and astable applications. Since this device was first made commercially available, a myriad of novel and unique circuits have been

developed and presented in several trade, professional, and hobby publications. The past ten years some manufacturers stopped making these timers because of competition or other reasons. Circuits presented in [21] are based on Op-Amps and have their own limitation of finite gain bandwidth.However, no such OTRA based Timers IC have been reported in literature so far.

Extensive literature survey shows that a lot of work has been done on analog signal processing using the voltage as a signal variable. Non-linear circuits using CMOS voltage mode circuit such as squarer, multiplier, log multiplier has been implemented enjoying the advantages of low power dissipation, voltage swing and applications in telecommunication, multimedia, signal processing etc. But with the increasing demand for high speed circuits operating in high frequency region, and the finite gain-bandwidth product associated with operational amplifiers, a different approach is required to be used. CMOS technology, using the current-mode circuits can achieve a considerable improvement in speed, accuracy and bandwidth, overcoming the finite gain–bandwidth product associated with operational amplifiers. Literature survey reveals the emergence of current-mode technology as an alternate approach. A variety of papers have been reported on OTRA during last one and a half decade. Current-mode techniques using the OTRA as active element has became a choice of modern analog design. This thesis includes CMOS realization of OTRA and a number of signal processing and generation applications such as voltage and current mode squarer, CMOS multiplier, frequency multiplier and frequency mixer realization

3.1 OTRA REALIZATION

3.1.1 CMOS Realization

The realization of OTRA with CMOS has increased input current range and also linearised the OTRA. Some of the attractive properties of OTRA are their fast speed in comparison with conventional op-amps. CMOS-OTRA is used in many of application instead of commercial operational amplifiers due to its features such as low power consumption, requirement of very low supply voltage and better result at high frequency. It reduces the zero cross-over distortion as compared to conventional op-amp. With the realization of CMOS-OTRA which is Transresistance amplifiers by which the above features arises results in improvement in multiplier, squarer or in any other circuit characteristics. The commercial realizations of

operational Transresistance amplifier under the name of current differencing amplifier or Norton amplifier are not widely used as they do not provide internal ground at the input port and they allow the input current to flow in one direction only. The former disadvantage limited the functionality of the OTRA whereas the latter forced to use external dc bias current leading to complex and unattractive designs. In recent years, several high-performance CMOS OTRA realizations have been presented and. This leads to growing interest for the design of OTRA-based analog signal processing circuits.

3.1.2 CFOA Realization

OTRA can also be realized using two AD844AN, a commercially available CFOA integrated chip.

3.2 OTRA APPLICATIONS

3.2.1 Multiplier

An analog multiplier is a device which takes two analog signals and produces an output which is product of these two signals [22]. The analog multiplier is a very important building block of analog signal processing system. It has many applications in automatic gain controlling, phase locked loop, modulation, detection, frequency translation, square rooting of signals, neural networks and fuzzy integrated systems[I].The power consumption is a key parameter in the design of high performance mixed signal integrated circuit. Linearity and accuracy parameters are very important in the analog multiplier design.

The multiplier performs the product of two continuous signals x and y, yielding an output $Z = K.x.y$, where K is a constant with suitable dimension. The linearity, speed, supply voltage and power dissipation are the main goals of the design. The input signal of the analog multiplier circuit can be voltage or current. Thus, it may operate both as a voltage mode or current mode device. Extensive literature review reveals that a large number of analog multiplier configurations have been presented. A dual mode four quadrant multiplier is an important configuration of the analog multiplier which has been extensively worked upon [23-25].Each of

these configurations has its own advantages and limitations which have been a case of improvement in the succeeding work.

3.2.2 Squarer

With decrease in dimensions of transistor, nonlinear CMOS analog circuits are gaining more attention [26-28].One of the most useful non-linear block is the squarer [29, 30], since it is the basic circuit for the implementation of various non-linear functions. Some useful applications of squarer circuit are in instrumentation, communication, and control systems.

A squarer circuit produces an output signal proportional to the square of applied input signals.One of the simplest architecture of a squarer circuit is made up of the mixed signal circuit. Literature review shows that in addition to the mixed signal circuit, many more architectures of squarer circuits are available. However, the basic principle of all these architectures is that their output is proportional to the square of applied input signals. Let V_i be differential input signal to a squarer circuit and Vo be output of the squarer circuit. Then,

$$V_o = kV_i^2$$

Where k is a constant.

A common feature of all the architectures of the squarer circuit is the use of MOS transistor in saturation mode [31]. Here, the advantage of the input-output characteristic of MOS transistors in the saturation region is utilized. Some of the squarer design has a special quality of operating in both voltage and current mode, one mode at a time. It has two inputs one is current and other is voltage. In voltage mode it provides square of voltage input and in current mode it provides output of current input. Some of the parameters degrading the performance of the squarer circuits are second order effects such as mobility reduction, transistor mismatch, body effect, and channel length modulation [31]. Although, the channel length modulation effect can be improved by using long-channel devices, other effects are the significant areas of research in the field of squarer circuit design.

3.2.3 Relaxation Oscillator

Square and Triangular waveform generators have wide applications in instrumentation, communication, and signal processing. Conventionally, a square/triangular waveform generator can be realized by using two opamps [32]. Apart from these opamp-based configurations, several new voltage-mode square/triangular waveform generators can be found in the literature [33,34]. Among them, one compact current- controllable generator is designed using two operational transconductance amplifiers (OTAs) [33]. The main drawback is that the oscillation frequency and the amplitude of the square wave are dependent, which leads to restricted applications of this circuit. In order to solve this problem, a third OTA is included to independently control the oscillation frequency and the amplitude of the square wave in [34].

Recently, an alternative approach called current-mode technology has attracted considerable attention for analog circuit designers due to its high performance and versatility [35]. Until now, there are many current-mode analog building blocks developed and the related applications have been reported [36].

Past studies have mentioned that the current mode circuits feature the advantages of a higher bandwidth, a better linearity, a larger dynamic range and the noninterference between the gain and the bandwidth [33]. Based on the above considerations, a single operational transresistance amplifier (OTRA) is used in this thesis to design square wave generator. The function of an OTRA is first introduced in chapter 4. The circuits requiring only a small number of passive components are discussed and analyzed.

3.2.4 Frequency mixer

Advancements in wireless technology have largely been driven by the desire for lower cost, low power dissipation, low voltage headroom consumption and low nonlinearity solutions in building high performance RF circuits in silicon, particularly CMOS. However the quest for higher data rate, network capacity, transmit range and multi standard radio solution has driven the CMOS process in high operating frequency band, further exploiting the transit frequency, f_T of the transistor and paving room in the realization of bulky on-chip passive devices, thus eliminating the need for costly discrete components integration.

The circuits for the front-end radio frequency (RF) signal processing[37] are typically implemented in silicon Bipolar, bipolar-complementary metal oxide semiconductor (BiCMOS), or in gallium arsenide (GaAs); whereas, these technologies offer better analog circuit performance in comparison to lossy silicon substrate which makes the design of high quality factor reactive components difficult.

The design architecture of the analog RF signal processing circuits in a standard CMOS technology has a growing concern of performance since a number of current mode circuits using CMOS are implemented. OTRA is an active current mode block having advantage of higher bandwidth, better linearity, and enhanced dynamic range.

Reference

[1]. Analogue IC Design: The Current-Mode Approach. Edited by C. Toumazou et al., Peter Peregrinus Ltd., London, 1990

[2]. Chen J. J., Tsao H. W., Liu S. and Chui W., Parasitic-capacitance-insensitive current-mode filters using operational transresistance amplifiers, IEE Proc. Circuits Devices and Systems 1995, vol. 142, no. 3, p. 186–192

[3]. Salama K. N., Soliman A. M., CMOS operational transresistance amplifier for analog signal processing. Microelectron J. 1999, vol. 30, issue 3, p. 235–45.

[4]. Toumazou C, Lidjey FJ, Haigh D. Analog IC design: the current-mode approach. Peter Peregrinus, UK: Exeter; 1990.

[5]. Kafrawy A. K. And Soliman A. M., "New CMOS Operational Transresistance Amplifier", International Conference on Microelectronics, 2008, p. 31-34.

[6]. Mostafa H. and Soliman A.M., A modified CMOS realization of the operationaltransresistance amplifier Frequenz, 2006, vol. 60, p. 70-76

[7]. Kafrawy A. K. and Soliman A. M., A modified CMOS differential operational transresistance amplifier (OTRA), Int. J. Electron. Commun. 2009, (AEU) vol. 63, p. 1067-1071.

[8]. Toker A., Özo˘guz S., Cicekoglu O. And Acar C., Current-mode allpass filters using Current differencing buffered amplifier and new high-Q bandpass filter Configuration, IEEE Tran. Circuits Syst. II, Analog Digital Signal Process. Sep. 2000, vol. 47, no. 9, p. 949–954.

[9]. Riewruja V., Parnklang J. And Julprapa A., Current Tunable Cmos Operational Transresistance Amplifier, ISIE 2001, vol. 2, p. 1328–1338.

[10]. Ravindran A., Salva A., Younus Md. I. And Ismail M., A 0.8V CMOS filter based On a novel low voltage OTRA, IEEE 2002, vol. III p. 368-371

[11]. Brodie J., A notch filter employing current differencing operational amplifier, International Journal of Electronics, 1976, vol. 41, no. 5, p. 501–508.

[12]. National Semiconductor Corp., Designing with a New Super Fast Dual Norton Amplifier, Linear Applications Data Book, 1981.

[13]. National Semiconductor Corp., The LM3900: A New Current Differencing ^ Quad of the Input Amplifiers, Linear Applications Data Book, 1986.

[14]. Pandey R. and Bothra M., Multiphase Sinusoidal Oscillators Using Operational Trans-Resistance Amplifier, IEEE Symposium on Industrial Electronics and Applications, 2009, p. 371-376.

[15]. Cam U., A Novel Single-Resistance-Controlled Sinusoidal Oscillator Employing Single Operational Transresistance Amplifier, Analog Integrated Circuits and Signal Processing, 2002, vol. 32, p. 183–186.

[16]. Salama K. N. and Soliman A. M., Novel oscillators using the Operational Transresistance Amplifiers, Microelectronics Journal, 2000, vol. 31, p. 39-47.

[17]. Lo Y. K. and Chien H. C., Single OTRA-based current-mode monostable multivibrator with two triggering modes and a reduced recovery time, IET Circuits Devices Syst., 2007, vol. 1, no. 3, p. 257–261.

[18]. Lo Y. K. and Chien H. C., Current-Mode Monostable Multivibrators Using OTRAs, IEEE Transactions On Circuits And Systems, Nov. 2006, vol. 53, no. 11, p. 1274-1278.

[19]. Hou C.L., Chien H.C. and Lo Y.K., Square wave generators employing OTRAs, IEEE Proc.-Circuits Devices Syst., Dec. 2005, vol. 152, no. 6, p. 718-722.

[20]. Lo Y. K., Chien H. C. and Chiu H. J., Current-input OTRA Schmitt trigger with dual hysteresis modes, Int. J. Circ. Theor. Appl., 2009.

[21]. http://www.fairchildsemi.com/an/AN/AN-88.

[22]. Ali Naderi, AbdollahKhoei, KhayrollahHadidi, HadiGhasemzadeh, " A new high speed and low power four quadrant CMOS analog multiplier in current mode" Int JComm2008.

[23]MontreeKumngern, KobchaiDejhan. "Versatile DualMode Class-AB Four-Quadrant Analog Multiplier" Int J Signal Process 2005;2(ISSN):1304-4494.

[24]Koichi Tanno, Okihiko Ishizuka, Zheng Tang, "Fourquadrant CMOS current-mode multiplier independent of device parameters". IEEE Trans Circuits Syst II 2000;47.

[25]. MirkoGravati, Maurizio Valle, Giuseppe Ferri, Nicola Guerrini, Linder Reyes, "A novel current-mode very low power analog CMOS four quadrant multiplier"

[26]. **S.** Liu, Y. Hwang, "CMOS Four-Quadrant Using Bias Feedback Techniques," *IEEE Jour. of Solid-state Circ.,* Vol. 29, No. 6, pp. 750-752, June 1994.

[27]. J. Schoeman, T. Joubert, "Four Quadrant Analogue CMOS Multiplier Using Capacitively Coupled Dual-Gate Transistors," *Electronics Letters,* Vol. 32, No. 3, pp. 209-210, Febr. 1996.

[28]. S. Liu, C. Chang, *Y.* Hwang, "New CMOS Four-Quadrant Multiplier and Squarer Circuits," *Analog Integrated Circuits and Signal Processing,* Vol. 9, pp. 257-263, 1996.

[29]. K. Kimura, "A Bipolar Four-Quadrant Analog Quarter-Square Multiplier Consisting of Unbalanced Emitter-Coupled Pairs and Expansions of Its Input Ranges," *IEEE Jour. of Solid-state Circ.,* Vol. 29, No. 1, pp. 46-55, Jan. 1994.

[30]. I. Filanovsky, H. Baltes, "Simple CMOS Analog Square-Rooting and Squaring Circuits," *IEEE Trans.* ***on*** *Circuits and Systems -part I,* Vol. 39, No. 4, pp. 312-315, April 1992.

[31]. IttipongChaisayun ,SomkiatPiangprantong, KobchaiDejhan, “Versatile analog squarer and multiplier free from body effect” 21 July 2011, Springer Science+Business Media, LLC 2011.

[32]. A. S. Sedra and K. C. Smith*, Microelectronic Circuits*, 4th ed. New York: Oxford University Press, 2004.

[33]. CA3080 Data Sheet Intersil, Milpitas, CA, Aug. 2004.

[34]. W. S. Chung, H. Kim, H. W. Cha, and H. J. Kim, “Triangular/squarewave generator with independently controllable frequency and amplitude,”*IEEE Trans. Instrum. Meas.*, vol. 54, no. 2, pp. 105–109, Feb.2005.

[35]. C. Toumazou, F. J. Lidegy, and D. Haigh, *Analog IC Design: The Current-Mode Approach*. Exeter, U.K.: Peter Peregrinus, 1990.

[36]. K. Kim, H. W. Cha, and W. S. Chung, "OTA-*R* Schmitt trigger with independently controllable threshold and output voltage levels," *Electron. Lett.*, vol. 33, pp. 1103–1105, Jun. 1997.

[37]. J. Crols, M. Steyaert, "A 1.5 *GHz* Highly Linear CMOS Downconversion Mixer," *IEEE Jour.* of *Solid-state Circ.,* Vol. 30, NO. 7, pp. 736-742, July 1995.

CHAPTER-4

OPERATIONAL TRANSRESISTANCE AMPLIFIER (OTRA)

4.1Operational Transresistance Amplifier (OTRA)

As signal processing extends to higher frequencies, traditional design methods based on voltage op-amps are no longer adequate. It is well known that a traditional operational amplifier has bandwidth which is dependent on the closed-loop voltage gain. The attempt to overcome this problem has led to a renewed interest in circuits which operate in current mode.

The OTRA is a current mode device that uses current mirrors and common source amplifier to give a current difference signal as input which in turn produce an appropriate voltage signal as output. The OTRA is a three terminal analog building block. Both the input and output terminals are characterized by low impedance. The circuit symbol of the OTRA is illustrated in Fig.4.1. The port relations of an OTRA can be characterized by the following matrix form [1].

$$\begin{bmatrix} v_p \\ v_n \\ v_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{bmatrix} \begin{bmatrix} i_p \\ i_n \\ i_z \end{bmatrix} \tag{4.1}$$

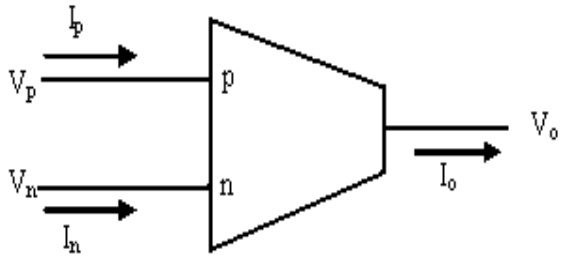


Fig 4.1 Circuit symbol of OTRA [1]

It eliminates response limitations incurred by capacitive time constants leading to circuits that are insensitive to the stray capacitances at the input terminals. For ideal OTRA, the Transresistance gain, R_m, approaches infinity and external negative feedback must be used which forces the input currents to be equal [2]. Thus the OTRA must be used in a negative feedback configuration. Practically the Transresistance gain is finite and its effect should be considered.

The important advantages offered by OTRA are:

- Since the OTRA has one output terminal with low impedance and two input terminals that are virtually grounded, most effects of parasitic capacitances disappear and the remainder can be compensated without adding any extra components.
- Using current feedback techniques, OTRAs have a bandwidth almost independent of the closed loop-voltage gain.
- Due to the input terminals being virtually grounded, they are cascadable.

The small signal ac equivalent of the OTRA is shown in the Fig. 4.2[3]:

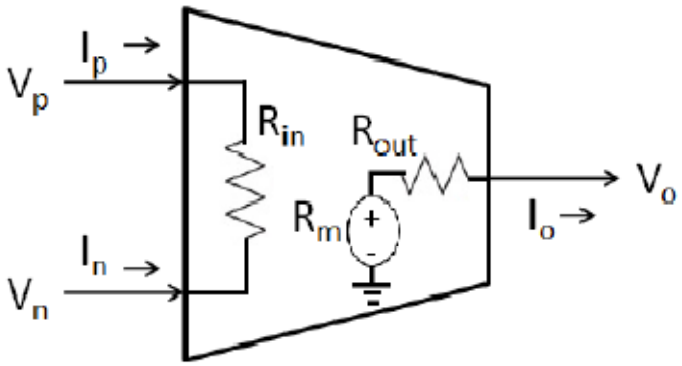


Fig. 4.2 The small signal ac equivalent of the OTRA [3]

4.2 Differential OTRA

Differential signal processing has higher dynamic range and power supply rejection compared to single-ended counterparts. These parameters are especially relevant in low power circuits. Other inherent advantages of differential circuits include immunity from common-mode noise signals and lower harmonic distortion. Differential OTRA is a four terminal device characterized by the matrix equation

$$\begin{bmatrix} V_p \\ V_n \\ V_{o+} \\ V_{o-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ R_m & -R_m & 0 & 0 \\ -R_m & R_m & 0 & 0 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ I_{o+} \\ I_{o-} \end{bmatrix} \quad (4.2)$$

Fig. 4.3 and 4.4 show the symbol and small signal ac equivalent of differential OTRA respectively [4].

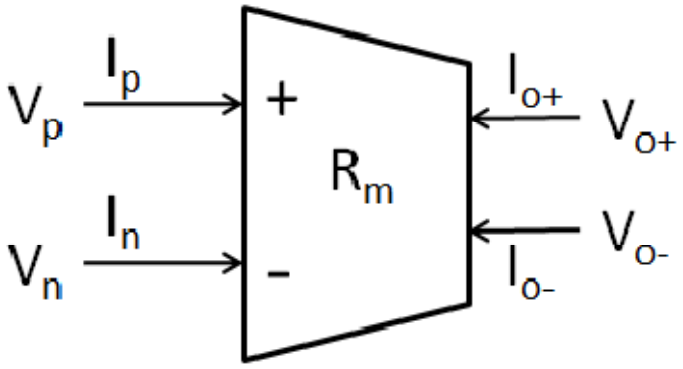


Fig.4.3 Symbol of Differential OTRA [4]

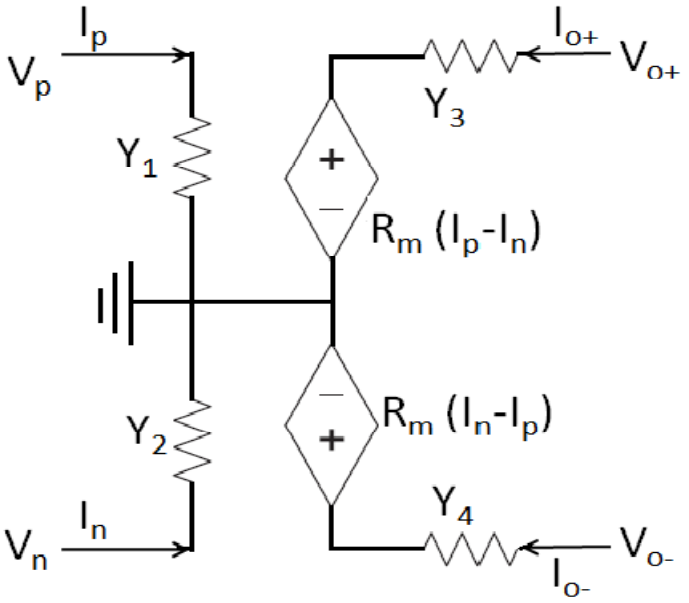


Fig. 4.4 Small Signal AC Equivalent of Differential OTRA [4].

4.3 Non-Ideal Analysis:

The output of the timer circuit may deviate due to non ideality of OTRA in practice. Ideally the Transresistance gain R_m is assumed to approach infinity. However, practically R_m is a frequency dependent finite value.The frequency limitations associated with OTRA should be considered. Considering a single pole model for the trans-resistance gain, R_m[5] can be expressed as

$$R_m(s) = \left(\frac{R_0}{1+\frac{s}{\omega_0}}\right) \tag{4.3}$$

where R_0 is dc transresistance gain. For high frequency applications the transresistance gain R_m (s) reduces to

$$R_m(s) = \left(\frac{1}{sC_p}\right) \tag{4.4}$$

Where $C_p = \frac{1}{R_0\omega_0}$

Where, Ro is DC open loop transresistance gain and ω_o is transresistance cut off frequency.

4.4.1 OTRA CMOS Realization

CMOS realization of the low power wide band OTRA as presented in [6] is shown in circuit 4.5. It is based on the cascaded connection of the modified differential current conveyor (MDCC) and a common source amplifier.

Assuming that each of the groups of the transistors (M1-M3), (M5 and M6), (M8-M11) and (M12 and M13) are matched and assuming that all the transistors operate in the saturation region, the circuit operation can be explained as follows.

The current mirrors formed by (M8-M11) forces equal currents (I_B) in the transistors M1, M2 and M3. This operation drives the gate to source voltages M1, M2 and M3 to equal and, consequently, forces the equal terminals to be virtually grounded.

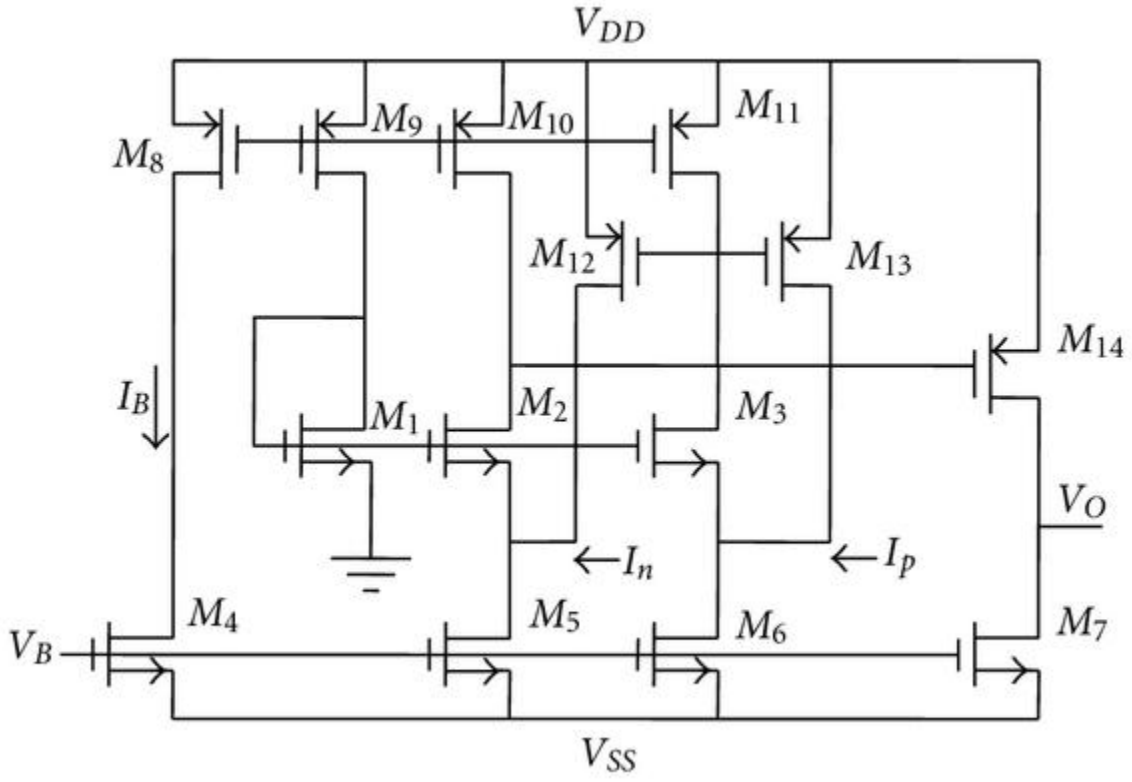


Fig.4.5 CMOS Realization of OTRA[6]

The current mirrors formed by the transistor pair (M10 and M11) and (M12 and M13) provide the current differencing operation, whereas the common source amplifier (M14) achieves high gain. The modified OTRA has smaller number of current mirrors than the OTRA introduced in [7] which reduces the transistor mirror mismatch effect and also increases the frequency capabilities. Moreover, this OTRA uses smaller number of transistors which reduces the power dissipation.

4.4.2 Simulation Results of OTRA

For simulation CMOS implementation of OTRA proposed in [8] is used. The SPICE simulation is performed using 0.5µm, Level 3, CMOS process parameters provided by MOSIS (AGILENT).Supply voltages VDD = -VSS = 1.5V are used. Aspect ratios used for different MOS transistors of OTRA are given in Table 1[8].

Table 1: Aspect ratio of the transistors in OTRA circuit.

Transistor	W (μm)/L (μm)
M_1–M_3	100/2.5
M_4	10/2.5
M_5, M_6	30/2.5
M_7	10/2.5
M_8–M_{11}	50/2.5
M_{12}, M_{13}	10/2.5
M_{14}	50/0.5

MOS transistor biasing voltage Biasing voltage V_B = -0.5V.The PSpice schematic of the OTRA is shown in fig.4.6. The simulated DC response is shown in fig.4.7.

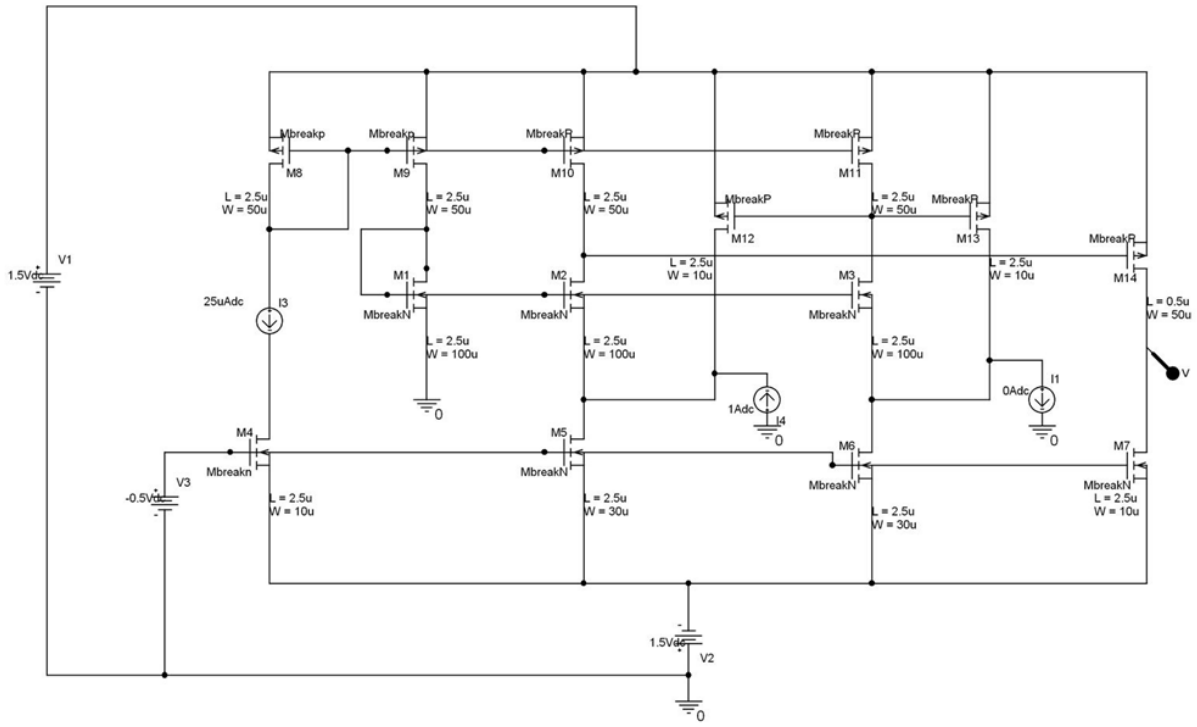


Fig.4.6 pSpice Schematic of CMOS realization of OTRA.

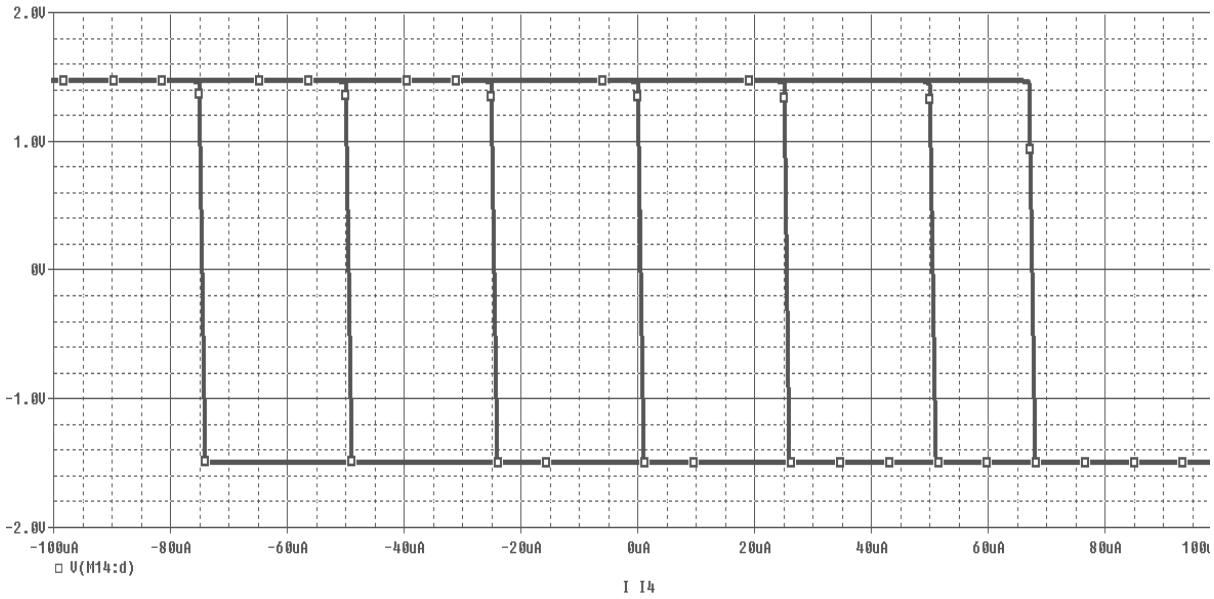


Fig.4.7 DC analysis of the realized OTRA

Frequency response and phase response OTRA is shown in fig.4.8 and fig.4.9.Maximum value of Rm is 135.014dB and $\omega_0$is 14.46 kHz.

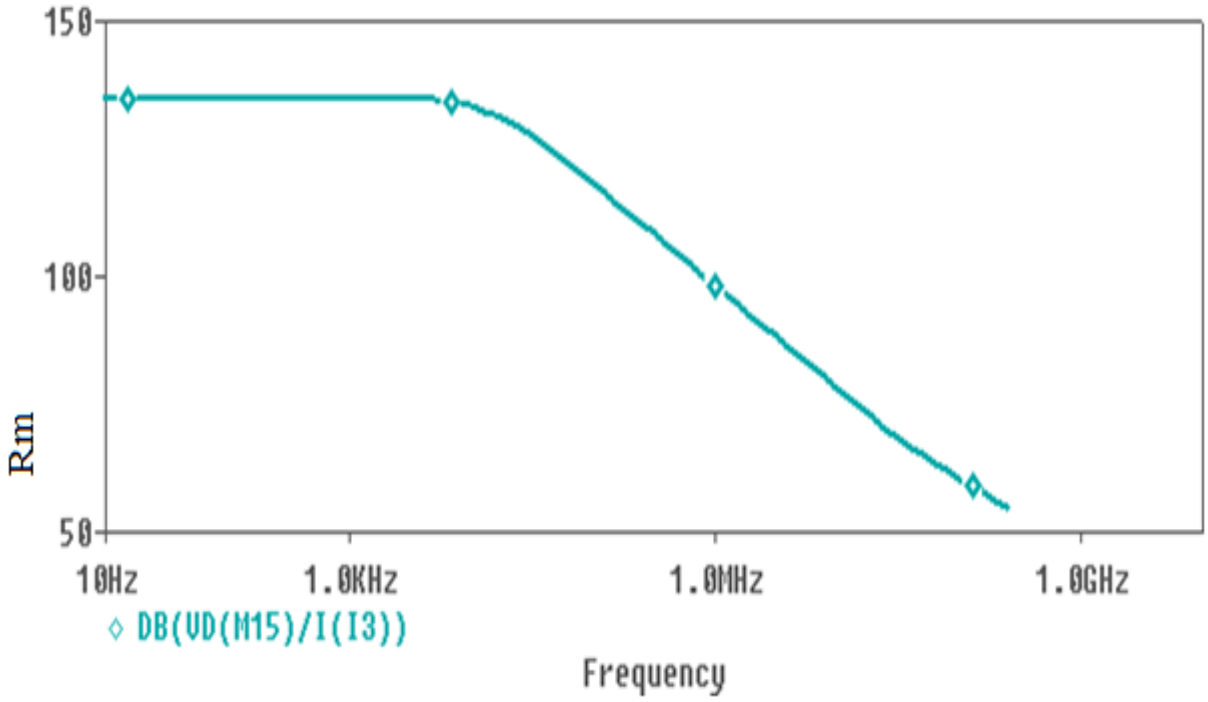


Fig.4.8 Frequency response OTRA

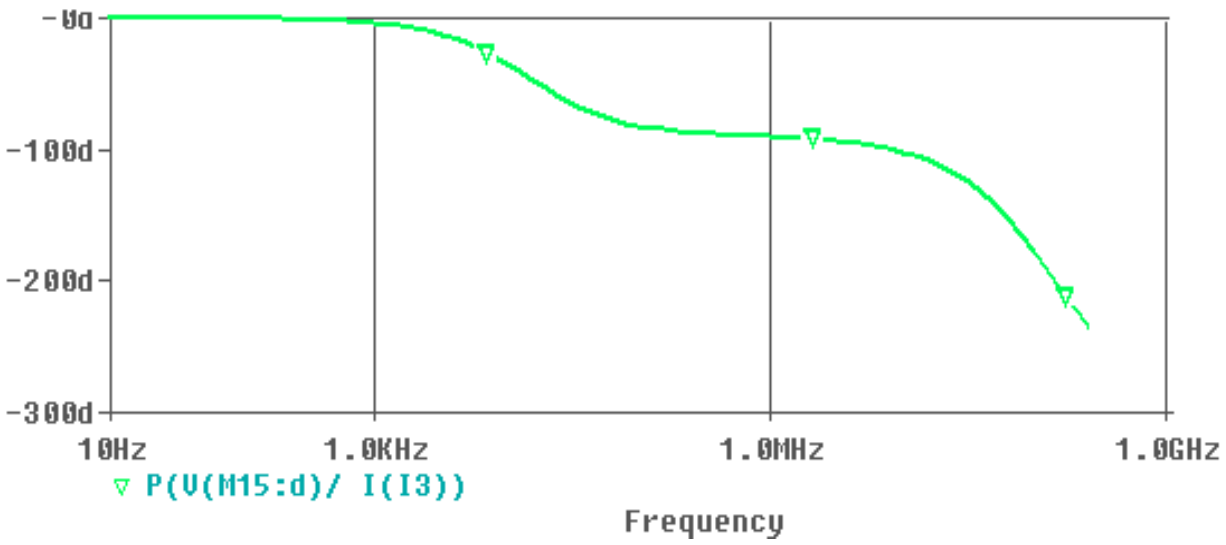


Fig.4.9 Phase response of OTRA

4.5 OTRA CFOA REALIZATION

The AD844 [9] is a high speed monolithic operational amplifier fabricated using Analog Devices' junction isolated complementary bipolar (CB) process. It combines high bandwidth and very fast large signal response with excellent dc performance. Although optimized for use in current to voltage applications and as an inverting mode amplifier, it is also suitable for use in many non- inverting applications. The AD844 can be used in place of traditional op amps, but its current feedback architecture results in much better ac performance, high linearity and an exceptionally clean pulse response.

This type of op amp provides a closed-loop bandwidth which is determined primarily by the feedback resistor and is almost independent of the closed-loop gain. The AD844 is free from the slew rate limitations inherent in traditional op amps and other current-feedback op amps.
The OTRA was realized using AD844 CFOA IC [9] as shown in Fig.[10]

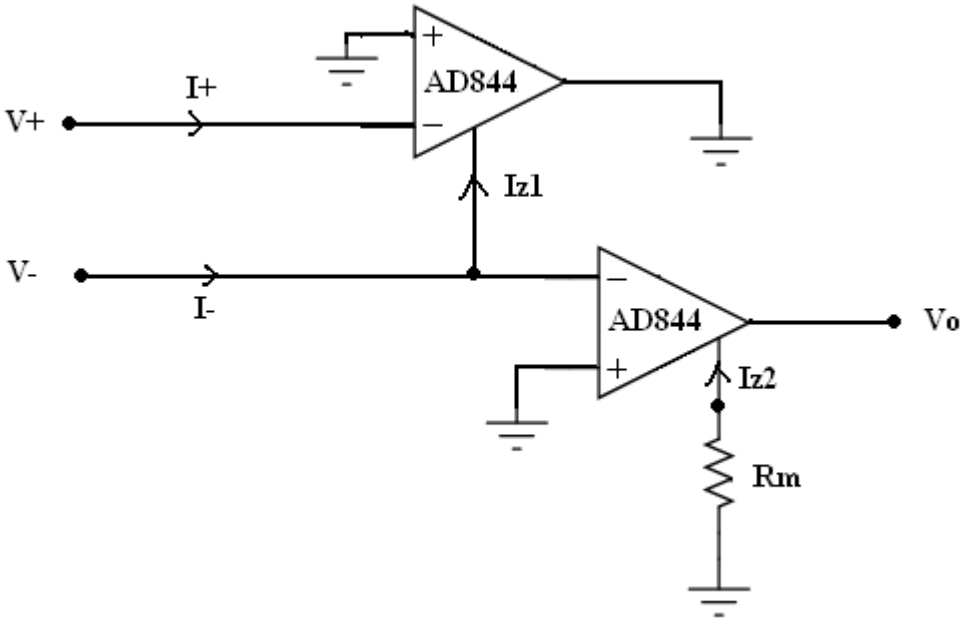


Fig.4.10 CFOA Realization of OTRA [10]

In order to simulate the virtual ground for the two input terminals of the OTRA, the non-inverting terminals of the AD844ANs have been grounded. TheAD844AN differs from the conventional operational amplifier in that the voltage on the non inverting signal input is transferred to the inverting input. Thus an inherent virtual short exists between these two terminals without any external negative feedback path. Owing to this characteristic, the following relations can be obtained.

$$V_{+} = V_{1-} = V_{1+} = 0 \;\&\; V_{-} = V_{2-} = V_{2+} = 0 \qquad (4.5)$$

Another feature of the AD844AN is that the current into the inverting terminal is equal to the current into the slewing node T_Z& the output voltage is the same as the voltage appearing at this pin.

$$I_{T1} = I_{1-} = I_{1+} \qquad (4.5)$$

$$V_{o1} = V_{T1} = V_{2-} = 0 \qquad (4.6)$$

$$I_{T2} = I_{2-} = I_{-} - I_{T1} = I_{-} - I_{+} \qquad (4.7)$$

$$V_o = V_{o2} = V_{T2} = -R_m * I_{T2} = R_m * (I_+ - I_-) \quad (4.8)$$

Thus wiring two CFOAs in this manner shown in figure 4.10, the terminal equations of OTRA can be realized. Fig 4.11 is the schematic of OTRA realized using CFOAs and fig 4.12 shows the DC response.

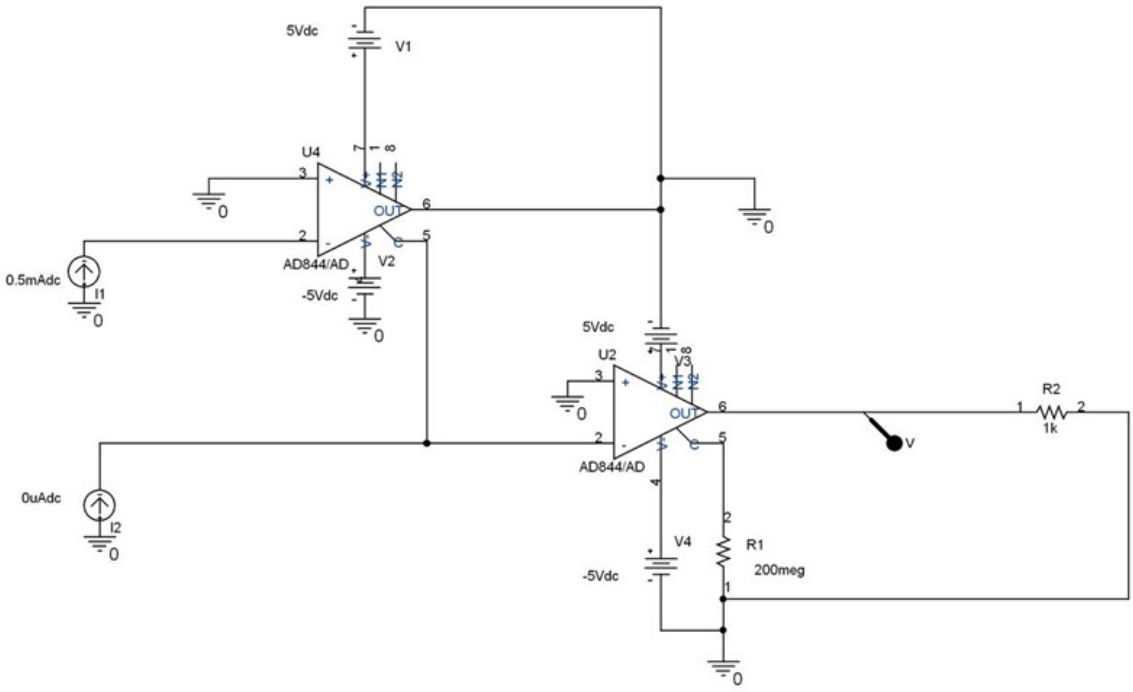


Fig.4.11 Pspice Schematic of CMOS realization of OTRA

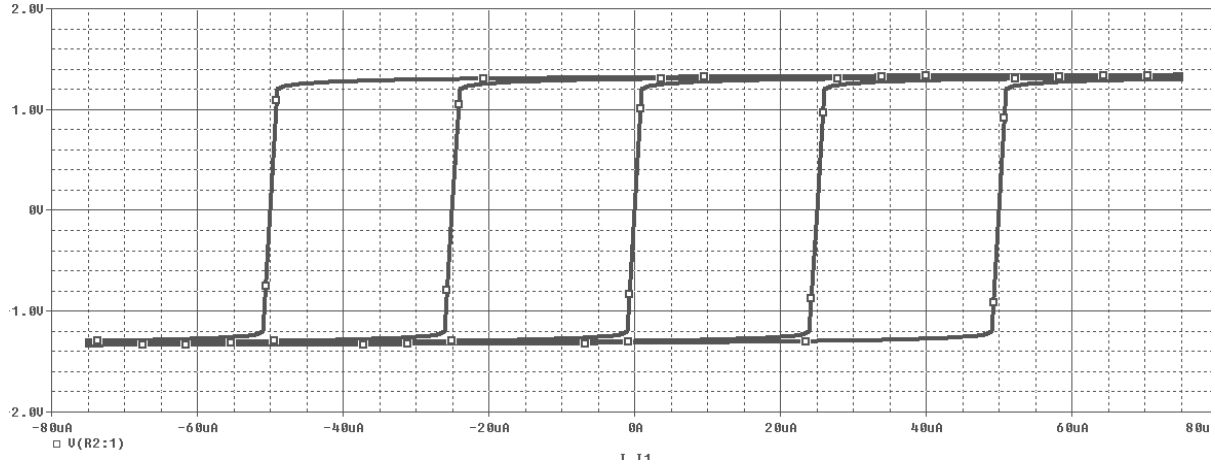


Fig.4.12 DC analysis of the realized OTRA

REFERENCES

[12] Chen J. J., Tsao H. W., Liu S. and Chui W., Parasitic-capacitance-insensitive current-mode filters using operational transresistance amplifiers, IEE Proc. Circuits Devices and Systems 1995, vol. 142, no. 3, p. 186–192.

[13] Salama K. N., Soliman A. M., CMOS operational transresistance amplifier for analog signal processing. Microelectron J. 1999, vol. 30, issue 3, p. 235–45.

[14] C. Toumazou, F. J. Lidegy, and D. Haigh, *Analog IC Design: The Current-Mode Approach*. Exeter, U.K.: Peter Peregrinus, 1990.

[15] Sánchez-López C., Fernández F.V. and Tlelo-Cuautle E., Generalized admittance matrix models of OTRAs and COAs. Microelectronics Journal, August 2010, vol. 41, issue 8, p. 502-505.

[16] Salama K. N., Soliman A. M., CMOS operational transresistance amplifier for analog signal processing. Microelectron J. 1999, vol. 30, issue 3, p. 235–45.

[17] Microelectronics Journal 30 (1999) 157–160 'A new versatile building block: current differencing buffered amplifier suitable for analog signal-processing filters.

[18] J.J. Chen, H.W. Tsao, and C. Chen, "Operational transresistance amplifier using CMOS technology." *Electronics Letters*, vol. 28, no. 22, pp. 2087–2088, 1992.

[19] H. Mostafa and A. M. Soliman, "A modified CMOS realizationof the operational transresistance amplifier (OTRA),"*Frequenz*, vol. 60, no. 3-4, pp. 70–76, 2006.

[20] AD844 Datasheet, Analog Devices Inc.

[21] Y. K. Lo, H. C. Chien "Switch controllable OTRA based square/triangular waveform generator," IEEE Transactions on Circuits and Systems II: Express Briefs, Vol. 54, No. 12, Dec 2007.

CHAPTER-5

5.1 Timer Circuit Using Operational Amplifier:

The IC was designed in 1971 by Hans Camenzind under contract to Signetics, which was later acquired by Philips (now NXP).Depending on the manufacturer, the standard 555 package includes 25 transistors, 2 diodes and 15 resistors on a silicon chip installed in an 8-pin mini dual-in-line package (DIP-8)[1][3]. Variants available include the 556 (a 14-pin DIP combining two 555s on one chip), and the two 558 & 559s (both a 16-pin DIP combining four slightly modified 555s with DIS & THR connected internally, and TR is falling edge sensitive instead of level sensitive).

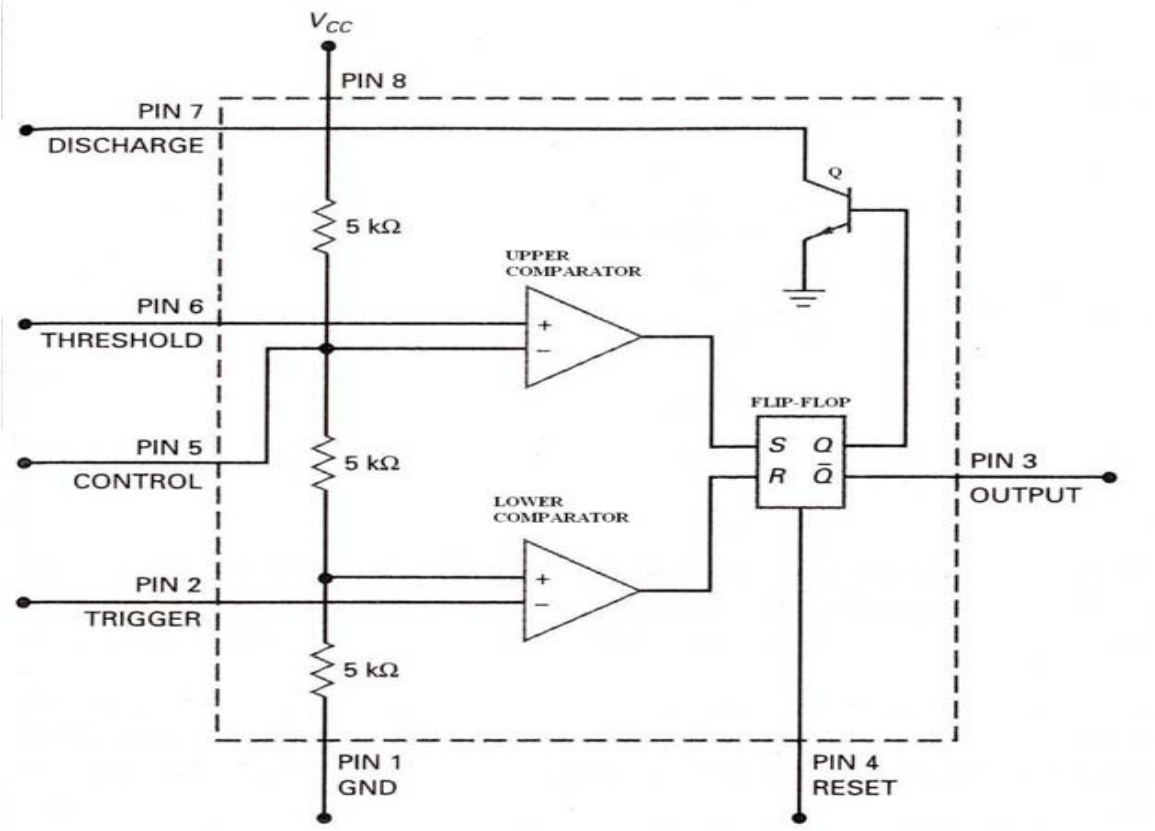


Fig. 5.1 Internal diagram of 555 timer

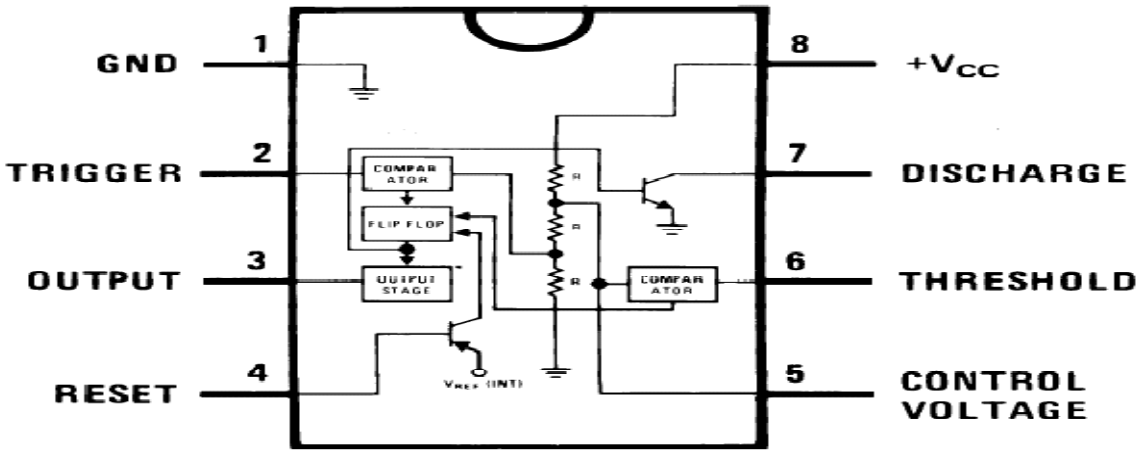


Fig.5.2 Pin diagram of 555 timer

The connection of the pins for a DIP package is as follows:

Pin	Name	Purpose
1	GND	Ground reference voltage, low level (0 V)
2	TRIG	The OUT pin goes high and a timing interval starts when this input falls below 1/2 of CTRL voltage (which is typically 1/3 of V_{CC}, when CTRL is open).
3	OUT	This output is driven to approximately 1.7V below $+V_{CC}$ or GND.
4	RESET	A timing interval may be reset by driving this input to GND, but the timing does not begin again until RESET rises above approximately 0.7 volts. Overrides TRIG which overrides THR.
5	CTRL	Provides "control" access to the internal voltage divider (by default, $2/3V_{CC}$).
6	THR	The timing (OUT high) interval ends when the voltage at THR is greater than that at CTRL ($2/3\ V_{CC}$ if CTRL is open).

7	DIS	Open collector output which may discharge a capacitor between intervals. In phase with output.
8	V_{CC}	Positive supply voltage, which is usually between 3 and 15 V depending on the variation.

5.1.1 OPERATION

The functional block diagram shows that the device consists of two comparators, three resistors and a flip-flop. A comparator is an OPAMP that compares an input voltage and indicates whether an input is higher or lower than a reference voltage by swinging into saturation in both the direction. The operation of the 555 timer revolves around the three resistors that form a voltage divider across the power supply to develop the reference voltage, and the two comparators connected to this voltage divider. The IC is quiescent so long as the trigger input (pin 2) remains at $+V_{CC}$ and the threshold input (pin 6) is at ground. Assume the reset input (pin 4) is also at $+V_{CC}$ and therefore inactive, and that the control voltage input (pin 5) is unconnected.

The three resistors in the voltage divider all have the same value (5K in the bipolarversion of this IC and hence the name 555), so the trigger and threshold comparator reference voltages are 1/3 and 2/3 of the supply voltage, respectively. The control voltage input at pin 5 can directly affect this relationship, although most of the time this pin is unused. The internal flip-flop changes state when the trigger input at pin 2 is pulled down below $+V_{CC}/3$. When this occurs, the output (pin 3) changes state to $+V_{CC}$ and thedischarge transistor (pin 7) is turned off. The trigger input can now return to $+V_{CC}$; it will not affect the state of the IC.However, if the threshold input (pin 6) is now raised above $+(2/3)V_{CC}$, the output willreturn to ground and the discharge transistor will be turned on again. When the threshold input returns to ground, the IC will remain in this state, which was the original state whenwe started this analysis. The easiest way to allow the threshold voltage (pin 6) togradually rise to $+(2/3)V_{CC}$ is to connect it externally to a capacitor being allowed tocharge through a resistor. In this way we can adjust the R and C values for almost anytime interval we might want.

5.2 IC555 Timer as Multivibrator

The 555 can operate in either mono/bi-stable or astable mode, depending on the connections to and the arrangement of the external components. Thus, it can either produce a single pulse when triggered, or it can produce a continuous pulse train as longas it remains powered.

5.2.1 Astable multivibrator

These circuits are not stable in any state and switch outputs after predetermined timeperiods. The result of this is that the output is a continuous square/rectangular wave with the properties depending on values of external resistors and capacitors. Thus, while designing these circuits following parameters need to be determined:

1. Frequency (or the time period) of the wave.
2. The duty cycle of the wave.

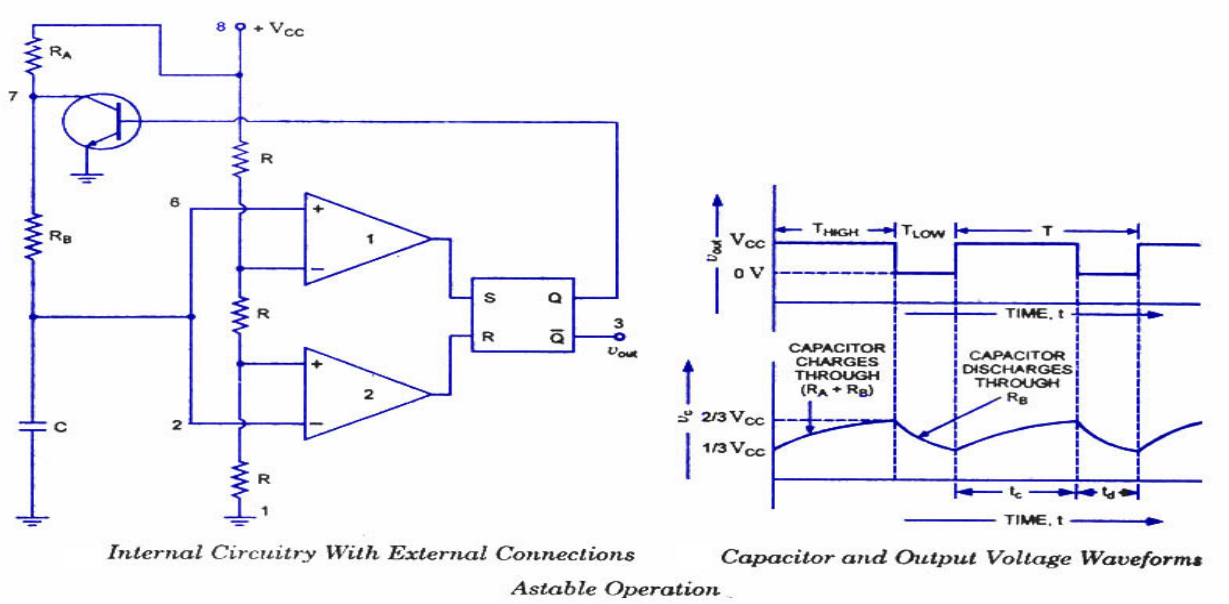
The key external component of the astable timer is the capacitor. An astablemultivibrator can be designed as shown in the circuit diagram (with typical componentvalues) using IC 555, for a duty cycle of more than 50%. The corresponding voltageacross the capacitor and voltage at output is also shown. The astable function is achievedby charging/discharging a capacitor through resistors connected, respectively, either toV_{CC} or GND. Switching between the charging and discharging modes is handled by resistor divider R1-R3, two Comparators, and an RS Flip-Flop in IC 555. The upper or lower comparator simply generates a positive pulse if V_C goes above 2/3 V_{CC} or below1/3 V_{CC}. And these positive pulses either SET or RESET the Q output.
The time for charging C from 1/3 to 2/3 Vcc, i.e, **ON Time = 0.693 (R_A + R_B). C**
The time for discharging C from 2/3 to 1/3 Vcc, i.e. **OFF Time = 0.693 R_B. C**
To get the total oscillation period, just add the two:

$$\mathbf{Tosc = 0.693\cdot(R_A+R_B)\cdot C + 0.693\cdot(R_B)\cdot C = 0.693 \cdot (R_A + 2\cdot R_B) \cdot C}$$

Thus,

$$\mathbf{fosc = 1/ Tosc = 1.44/(R_A + 2\cdot R_B).C}$$

$$\mathbf{Duty\ cycle = R_A+R_B/ R_A + 2\cdot R_B}$$



Internal Circuitry With External Connections *Capacitor and Output Voltage Waveforms*

Astable Operation

Fig.5.3 Astable multivibrator

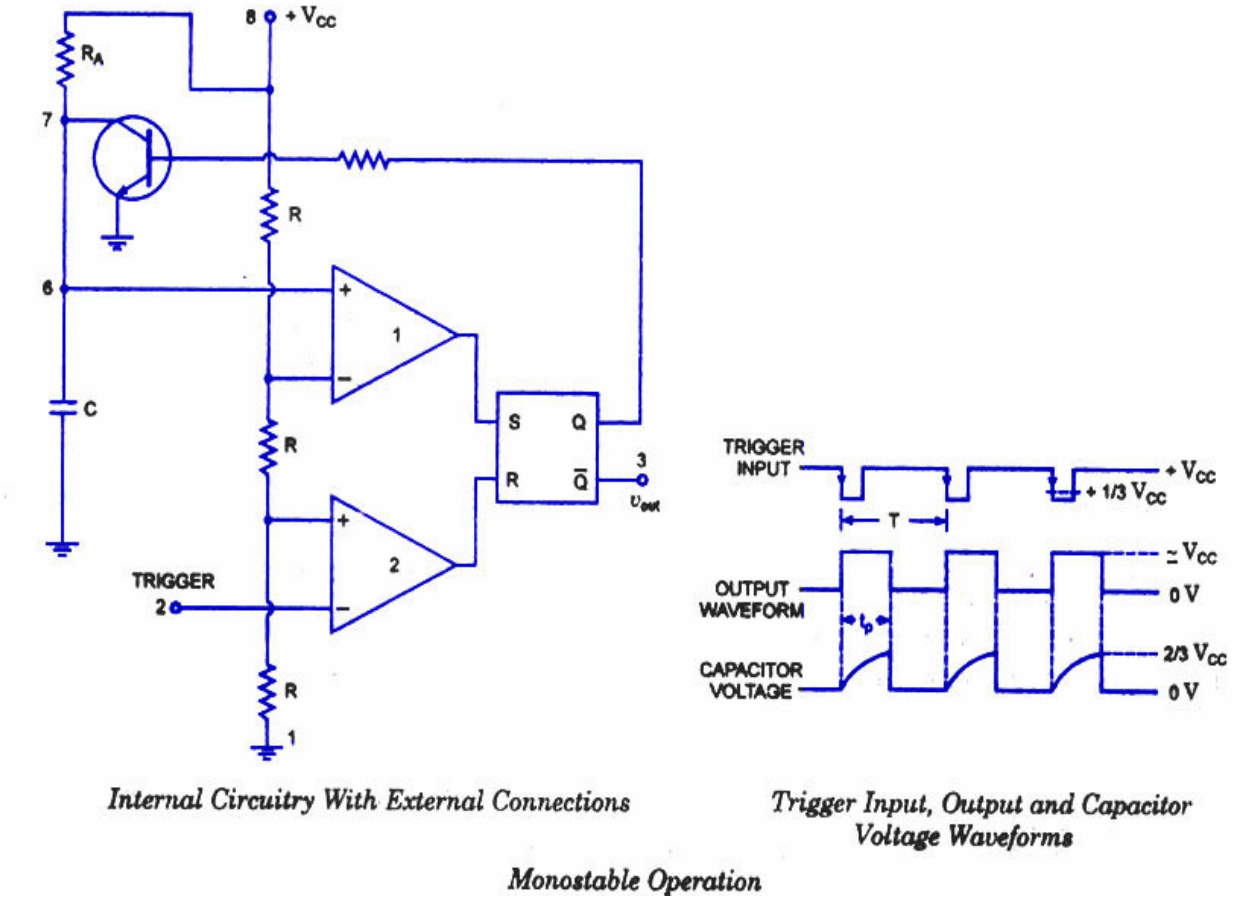
5.2.2 Monostable multivibrator

Monostable multivibrator often called a one shot multivibrator is a pulse generating circuit in which the duration of this pulse is determined by the RC network connected externally to the 555 timer. In a stable or standby state, the output of the circuit is approximately zero or a logic-low level. When external trigger pulse is applied (See circuit diagram) output is forced to go high (V_{CC}). The time for which output remains high is determined by the external RC network connected to the timer. At the end of the timing interval, the output automatically reverts back to its logic-low stable state. The output stays low until trigger pulse is again applied. Then the cycle repeats. The monostable circuit has only one stable state (output low) hence the name monostable. Initially when the circuit is in the stable state i.e, when the output is low, transistor Q in IC 555 is ON and the capacitor C is shorted out to ground. Upon the application of a negative trigger pulse to pin 2, transistor Q is turned OFF, which releases the short circuit across the external capacitor C and drives the output high. The capacitor C now starts charging up towards VCC through R. When the voltage across the capacitor equals $2/3V_{CC}$, the upper comparator's (see schematics of IC 555) output switches from low to high, which in turn drives the output to its low state via the output of the flip-flop. At the same time the output of the flip-flop turns transistor Q ON and hence the capacitor C rapidly discharges through the transistor. The output of the monostable remains low until a trigger pulse is again applied. Then the cycle

repeats. The pulse width of the trigger input must be smaller than the expected pulse width of the output waveform. Also the trigger pulse must be a negative going input signal with amplitude larger than 1/3 V_{CC} .The pulse width can be calculated as :

T= 1.1 R.C.

Once triggered, the circuit's output will remain in the high state until the set time, T,elapses. The output will not change its state even if an input trigger is applied again during this time interval. The circuit can be reset during the timing cycle by applying negative pulse to the reset terminal. The output will remain in the low state until a trigger is again applied. The circuit is designed as shown in the circuit diagram, the left part ofwhich shows how to generate negative a trigger pulse from a square wave signal.



Internal Circuitry With External Connections

Trigger Input, Output and Capacitor Voltage Waveforms

Monostable Operation

Fig.5.4 Monostable multivibrator

5.2.3 Pulse width modulator

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the outputpulse width can be modulated by a signal applied to the Control Voltage Terminal. Figure 12 shows the circuit, and in Figure 13 are waveform[2].

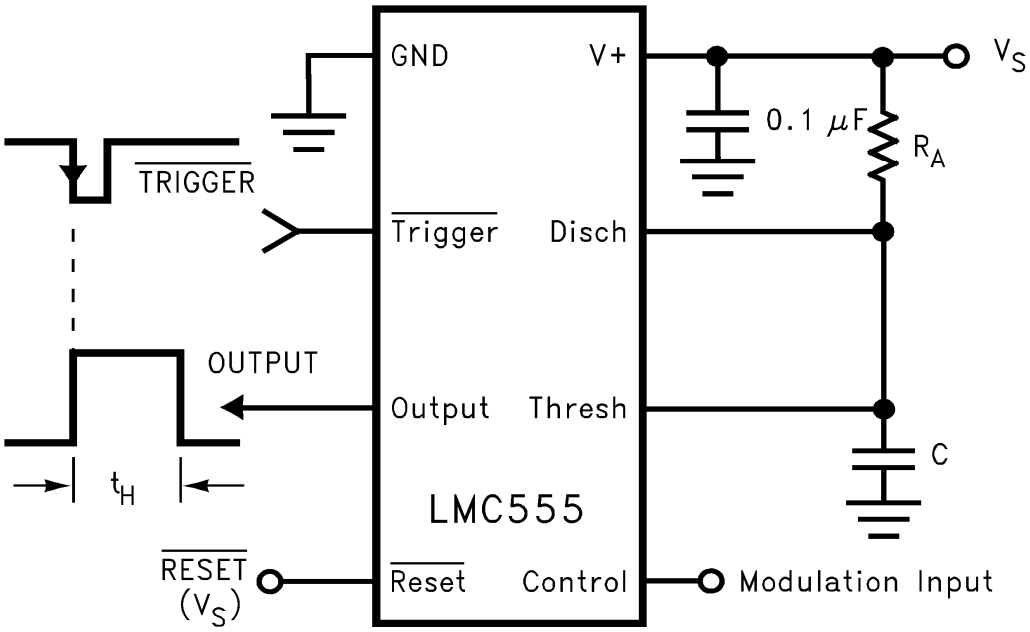


Fig.5.5 Pulse Width Modulator

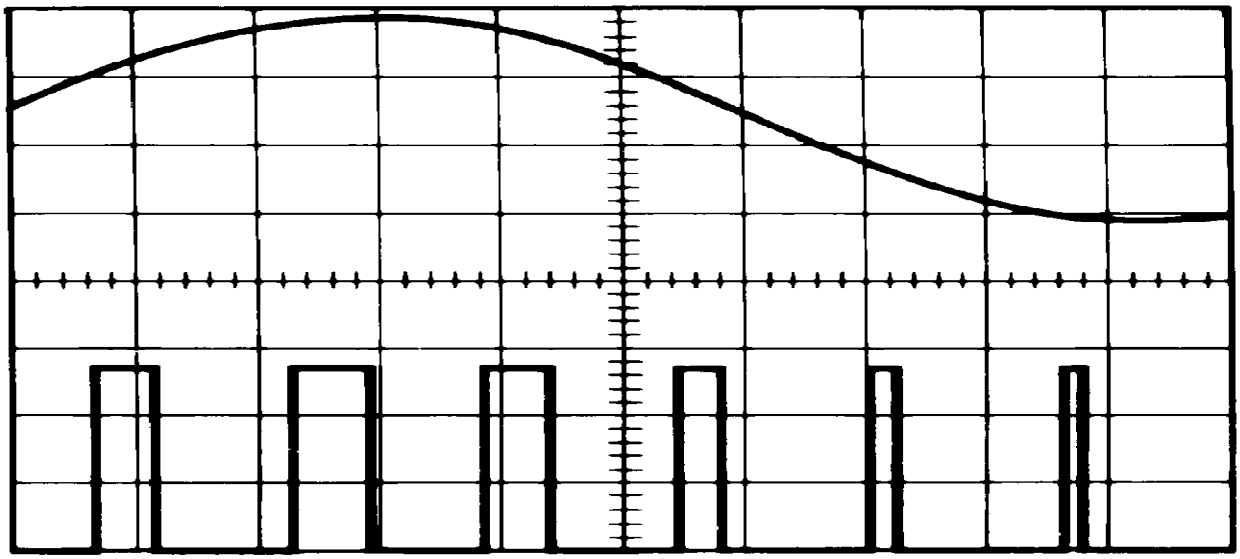


Fig.5.6 Pulse Width Modulator Waveform

REFERENCE

[1]. Franco Sergio, Design with opamp and analog integrated circuits, McGraw-Hill International, 1988.

[2]. 'Design and Analysis Nomo grams for Pulse-Width and Frequency Modulation Using the 555 Timer'by George K. Kostopoulos 0163-6812/84/0600-0004$1.00© 1984 IEEE.

[3]. Gayakwad , R.A., opamp and Linear Integrated cicuit Technology, Practice-Hall India Ltd. New Delhi,1987.

[4]. http://www.electronics.dit.ie/staff/mtully/555%20folder/555%20timer.htm.

CHAPTER-6

REALIZATION OF Timer Circuit Using OTRA

6.1 Proposed Timer Circuit Using OTRA

6.1.1 Circuit description

The Circuit diagram of Proposed Timer circuit using OTRA shown in fig.6.1. It consists of two comparators named as comp_1 and comp_2, an S-R flip-flop using Nand gates [2], a capacitor named C1, a NMOS named M1 and several resistors. Nand gate is implemented using CMOS [1].

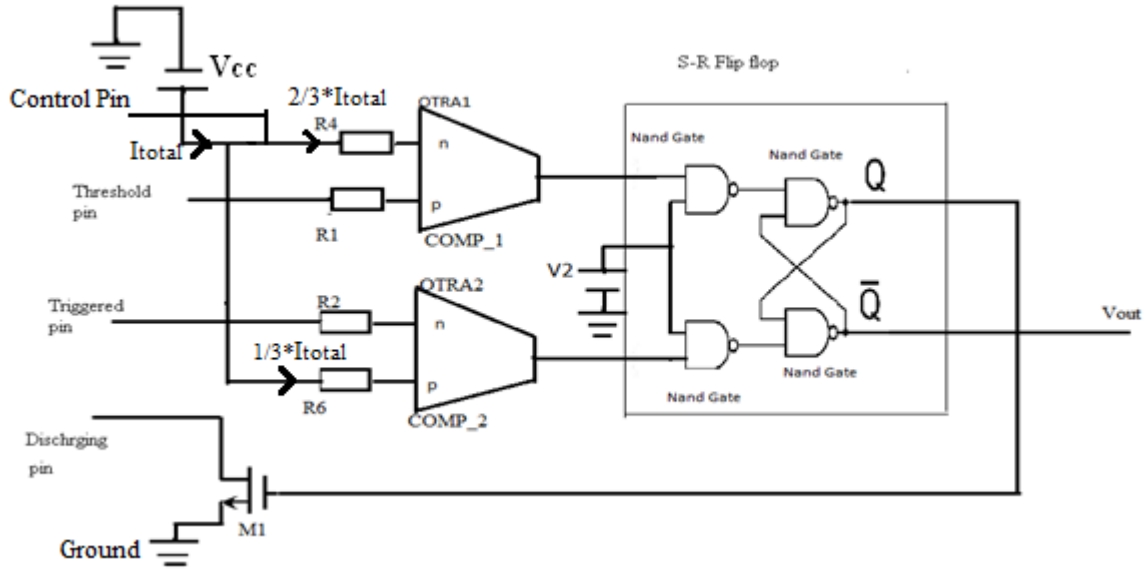


Fig.6.1 Proposed Timer circuit using OTRA

The supply voltage for the circuit is 1.5V. The output voltage can take on two states: a "high" state (~ 0.5V below the supply voltage) and a "low" state (~ 0.1V). The ground pin will be tied to the common ground point used for the rest of your circuit. The Trigger, Threshold and Discharge will require a closer inspection of the innards of the circuit to understand how they will be merged with the external circuitry.

The connection of the pin in the timer circuit is as follows:

GROUND PIN- Ground reference voltage, low level (0 V)

TRIGGER-The OUT pin goes high and a timing interval starts when this input falls below 1/2 of CTRL current (which is typically 1/3 of I_{total}, when CTRL is open).

OUT-Output is taken.

CONTROL PIN- Provides "control" access to the internal current divider (by default, 2/3 I_{total}).

THRESHOLD PIN-The timing (OUT high) interval ends when the current at THR is greater than that at CTRL (2/3 I_{total} if CTRL is open).

DISCHARGE PIN-Open collector output which may discharge a capacitor between intervals.

Vcc- Positive supply voltage, which is 1.5V.

I_{total}= Total current come in to the two comparator.

A comparator in general, is a circuit that compares voltage/current at its two input terminals and indicates whether an input is higher or lower than a reference voltage/current. But, here the comparator is made using OTRA which compares the input current at its two terminals, named $I_P$and I_n and provides output voltage which is either negative or positive. Output of OTRA is further connected to input of a cascaded inverter whose function is to change negative and positive voltages into two levels VCC (1) and zero (0) respectively. The operation of the this circuit revolves around the two resistors(R4,R6) that form a current divider across the power supply to develop the reference current, and the two comparators connected to this current divider. The two resistors in the current divider have the value such the current through I_n(n-terminal) of comp_1 and I_P(p-terminal) of comp_2 are 1/3 and 2/3 of the current through supply voltage to the two comparator, respectively. I_{total} is current through power supply to the two comparator. In this chapter with the help this timer circuit along with OTRA monostable multivibrator, astable multivibrator and pulse width modulator is proposed.

6.2 Proposed Astable Multivibrator Using Timer Circuit

Astable multivibrator using Timer circuit is shown in figure 6.2.Pspice schematic of astable multivibrator is shown in fig.6.3.

6.2.1 Operation

Assumption: Previous state of S-R flip flop is 1.

Initially, the current through I_P of comp_1 is 0A (since capacitor C1 is at 0V) and through I_n(n-terminal) of comp_1 is 2/3*I_{total} (due to current divider circuit) and hence its output is 0V

whereas, the current through I_n of comp_2 is 0A (since capacitor C1 is at 0V) and through I_P of comp_2 is $1/3*I_{total}$ (due to current divider circuit) and hence its output is V_{CC}. Hence, S-R Flip flop inputs are 0-1 respectively. So, its output is Q=0. Now, NMOS M1 is off since its gate terminal is connected to S-R Flip flop output terminal Q, which is at 0V.

Because of M_1 is off ,so capacitor starts charging by supply through resistors R3 and R5.As C1 charged to a value such that current through I_n of comp_2 get equals and then greater than I_P i.e. $1/3*I_{total}$, comp_2 output changes to 0V. Whereas, current through $I_P$of comp_1 is still less than I_n (2/3*Itotal) and hence its output remains at 0V. Now, flip flop inputs are S=0, R=0, hence its output is at previous state i.e. =0. M_1 is in off state and hence C_1 remains charging.

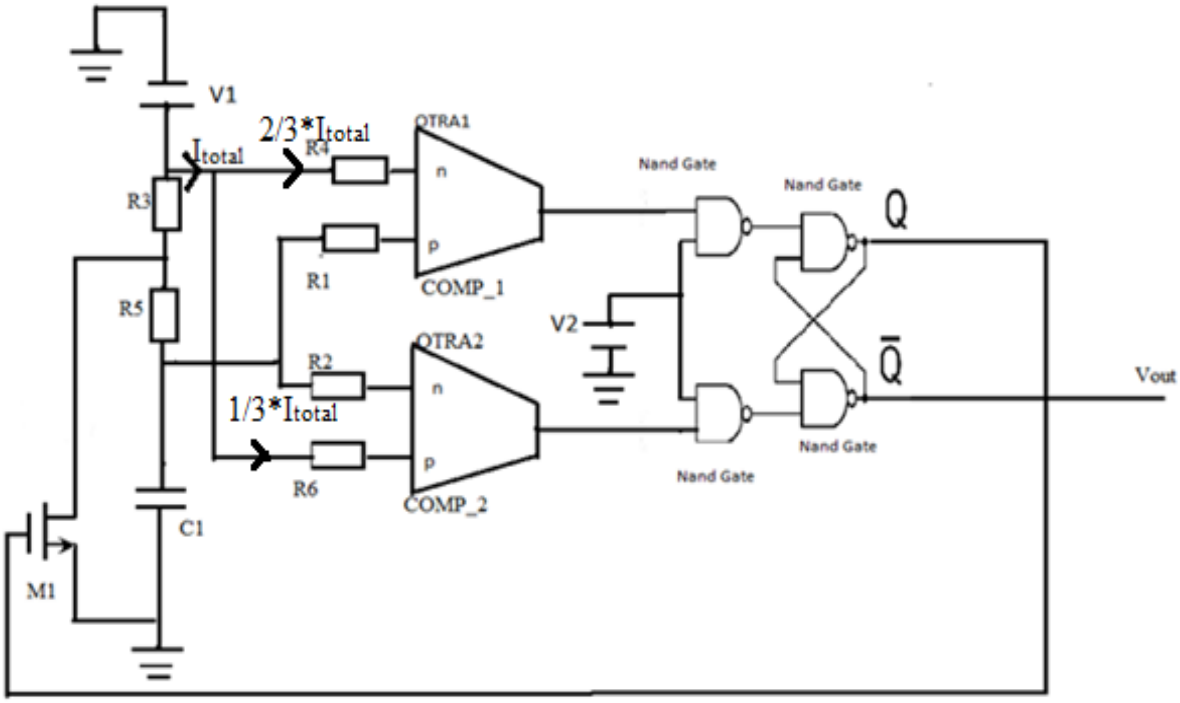


Fig.6.2 The proposed Astable multivibrator using timer circuit

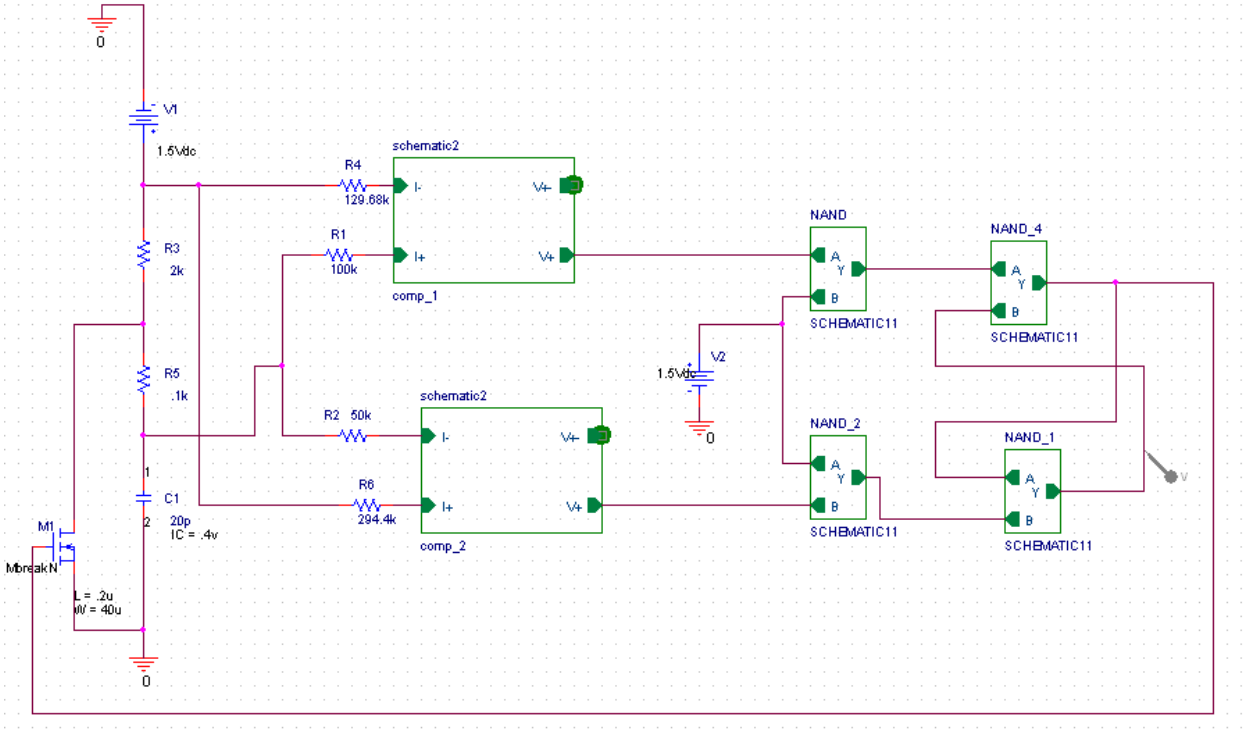


Fig.6.3 PSpice schematic of astable multivibrator.

As C_1 is charged to a voltage such that current through I_P of comp_1 gets equal and then greater than I_n (2/3*Itotal), its output changes to Vcc. Whereas, comp_2 output remains at 0V.Now, flip flop inputs are S=1, R=0, hence its output is at state Q=1. Now M_1 is in ON state and hence C_1 starts discharging via resistor R_5 and M_1 towards 0V.

As C1 discharged to a voltage level such that current through I_P of comp_1 gets equal and then lesser than I_n (2/3*Itotal), output of comp_1 changes to 0V. Whereas, output of comp_2 remains at 0V.Now, flip flop inputs are S=0, R=0, hence its output is at previous state i.e. Q=1. M_1 is in ON state and hence C_1 is still discharging via resistor R_5 and M_1 towards 0V.

As C_1 further discharged to a voltage level such that current through I_n of comp_2 gets equal and then lesser than I_P (1/3*Itotal), output of comp_2 changes to Vcc. Whereas, output of comp_1 remains at 0V.Now, flip flop inputs are S=0, R=1, hence its output is at state Q=0. Hence, M_1 gets OFF and C1 stops discharging via M_1 path. But C_1 starts charging through power supply and cycle repeats again and again. Output waveform of of astable multivibrator is shown in fig.5.10

So, current through I_P of comp_1 varies between 1/3*Itotal and 2/3*Itotal generating an astable current waveform.

The time for charging C_1 is $T_{on} = (R_3+R_5)*C_1$

The time for discharging C is $T_{off} = (R_3+Rmos)*C_1$

To get the total oscillation period, just add the two:

$$\mathbf{Tosc =}\ T_{on}+T_{off}$$

$$Tosc = (R_3+R_5)*C_1+(R_3+Rmos)*C_1$$

$$\text{Duty cycle} = \frac{Ton}{Ton+Toff}$$

Where, Rmos = MOSFET Resistance

6.3 Proposed Monostable multivibrator using Timer circuit

Proposed Monostablemultivibrator using Timer circuit is shown in figure 6.4.PSpice schematic of monostable multivibrator is shown in fig.6.5.

In this a pulse generator having two levels, for providing current trigger pulse is applied at the n-terminal of comp_2. The pulse generator has two levels I_1, a higher current value and I_2, a lower current value (lower than $1/3*I_{total}$), is shown in fig.5.11 (a).

6.3.1 Operation

Assumption: Previous state of S-R flip flop is 1.

Initially, the current through I_P (p-terminal) of comp_1 is 0A (since capacitor C_1 is at 0V) and through I_n(n-terminal) of comp_1 is $2/3*I_{total}$ (due to current divider circuit) and hence its output is 0V whereas, the current through I_n of comp_2 is at level I_1 (since pulse generator is at level I_1) and through I_P of comp_2 is $1/3*I_{total}$(due to current divider circuit) because I_1 is greater than $1/3*I_{total}$ and hence its output is 0V and S-R Flip-flop inputs are S= 0, R=0 respectively. So, its output is previous state i.e. Q=1. Now, M_1 is ON since its gate terminal is at high level (and hence capacitor C_1 is at 0V).

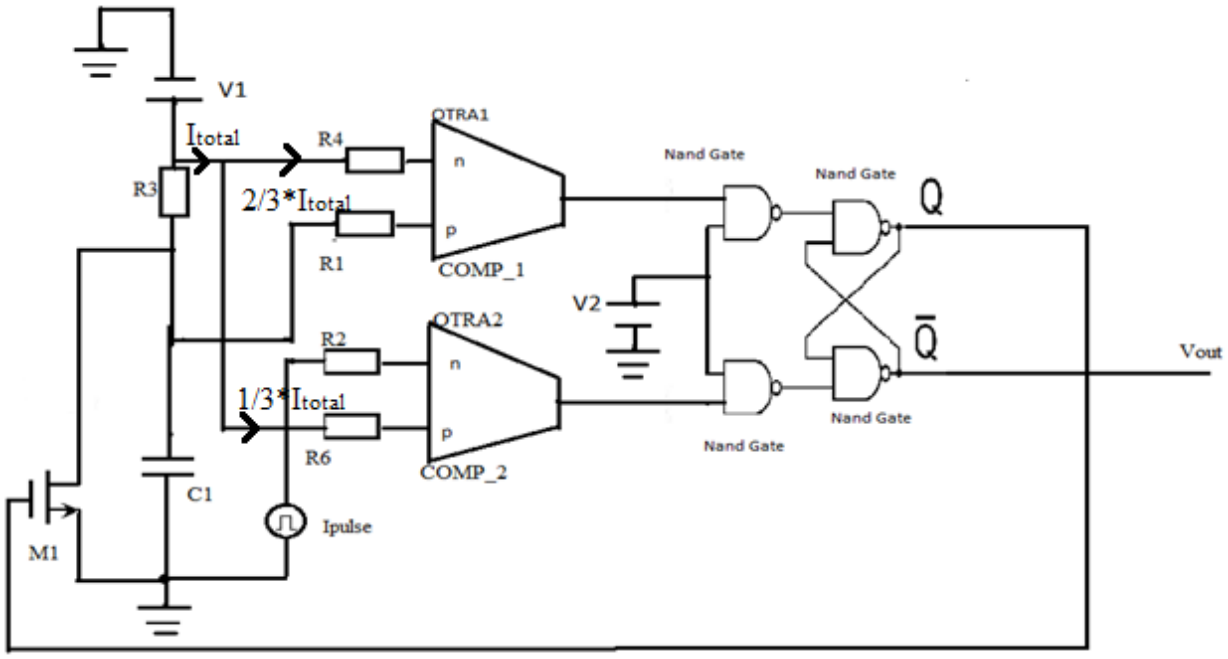


Fig.6.4 Proposed monostable multivibrator using Timer Circuit.

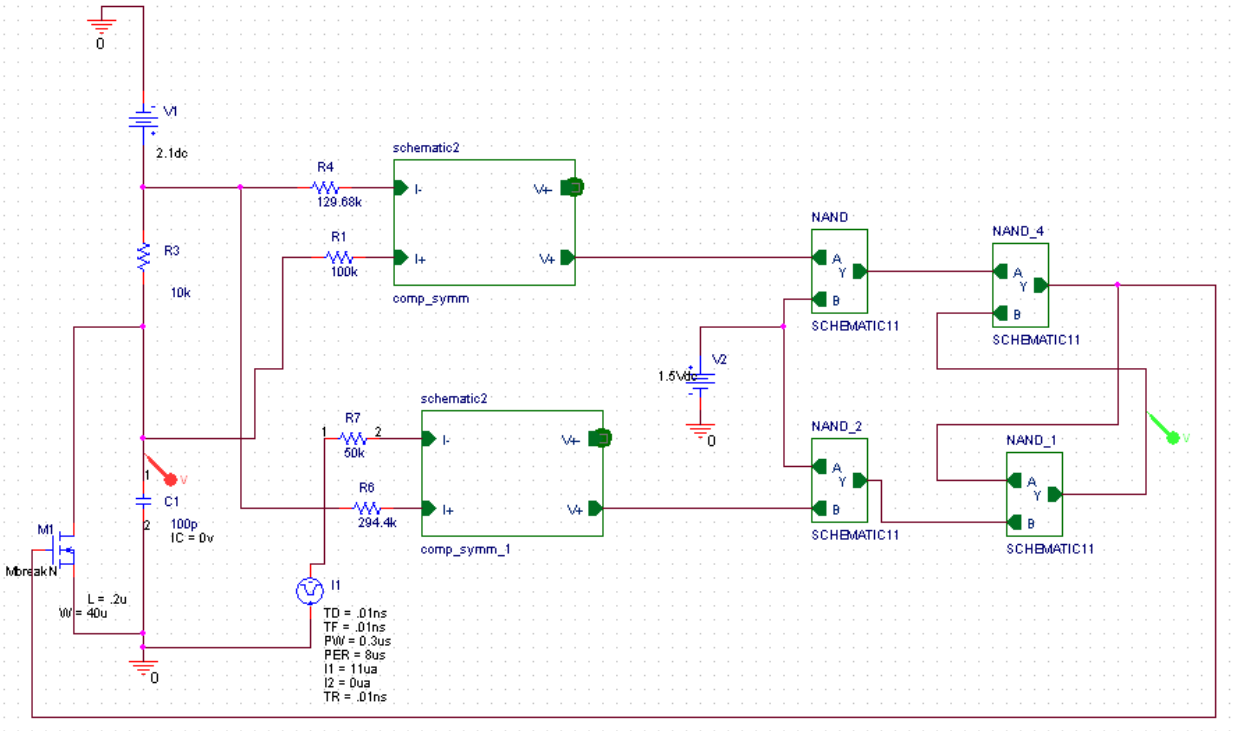


Fig.6.5 Pspice schematic of monostable multivibrator

As pulse generator (at I_n input of comp_2) triggers negative edge i.e., a current value less than $1/3*I_{total}$(current value at I_P of comp_2), output of comp_2 shift to Vcc, whereas output of

comp_1 remains unchanged at 0V. Hence, S-R flip flop inputs are now S=0, R=1, hence its output switches to new state i.e. Q=0. Now, M_1 gets in off state and hence C_1 starts charging via R_3.

Now C_1 keeps on charging towards Vcc. And during that time, in comp_2 I_n input again changes to higher level i.e., I_1 and I_P is fixed at 1/3*Itotal. Hence, its output switches back to 0V. Flip flop inputs are S=0, R=0, hence its output is at previous state i.e. Q =0. M_1 is in OFF state and hence C_1 keeps on charging via R_3 towards Vcc.

But as C_1 is charged to a voltage such that current through I_P of comp_1 gets equal and then greater than I_n (2/3*Itotal), its output changes to Vcc. whereas, output of comp_2 remains at 0V.Now, flip flop inputs are S=1, R=0, hence its output switches to new state i.e. Q=1. Now M_1 is in ON state and hence C_1 starts discharging via M_1.The output waveform of monostable multivibrator is shown in fig.6.11

This operation repeats again and again as trigger pulse is applied periodically.

6.4 Proposed Pulse Width Modulator Using Timer Circuit

Proposed Monostablemultivibrator using Timer circuit is shown in figure 6.6.Pspice schematic of monostable multivibrator is shown in fig.6.7.

A sinusoidal current signal applied at I_n input of comp_1,is shown in fig.5.12.Amplitude of this current sinusoidal current signal is low as compared to total current came into the current I_{total}(seen in fig.) . Let's assume these two values as I_1 and I_2 where I_1 is current value when sinusoidal signal has positive amplitude and I_2 is current value when sinusoidal signal has negative amplitude.

I_{total} is the total current come in to the comparator through power supply

6.4.1 Operation

Initially, the current through I_P of comp_1 is 0A (since capacitor C_1 is at 0V) and through I_n(n-terminal) of comp_1 is sum of 2/3*I_{total} and sinusoidal current signal and hence its output is 0V whereas, the current through I_n of comp_2 is 0A (since capacitor C_1 is at 0V) and through I_P of comp_2 is 1/3*Itotal (due to current divider circuit) and hence its output is Vcc. Hence, S-R Flip

flop inputs are S=0, R=1 respectively. So, its output is Q=0. Now, M_1 is off since its gate terminal is at 0V. Capacitor C_1 starts charging towards Vcc via R_3 and R_5.

As C_1 charged to a value such that current through I_n of comp_2 get equals and greater than I_P i.e. 1/3*Itotal, comp_2 output changes to 0V. Whereas, current through I_P of comp_1 is still less than sum of $2/3*I_{total}$ and sinusoidal current signal and hence its output remains at 0. Now, flip flop inputs are S=0, R=0, hence its output is at previous state i.e. Q=0. M1 is in off state and hence C1 remains charging.

As C_1 further charged to a voltage such that current through I_P of comp_1 gets equal and then greater than sum of $2/3*I_{total}$ and sinusoidal current signal, its output changes to 1. Whereas, comp_2 output remains at 0V.Now, flip flop inputs are S=1, R=0, hence its output is at state Q=1. Now M_1 is in ON state and hence C_1 starts discharging via M_1 towards 0V.

As C1 discharged to a voltage level such that current through I_P of comp_1 gets equal and then lesser than I_n (2/3*Itotal), output of comp_1 changes to 0V. Whereas, output of comp_2 remains at 0V.Now, flip flop inputs are S=0, R=0, hence its output is at previous state i.e. Q=1. M_1 is in ON state and hence C_1 is still discharging via M_1 towards 0V.

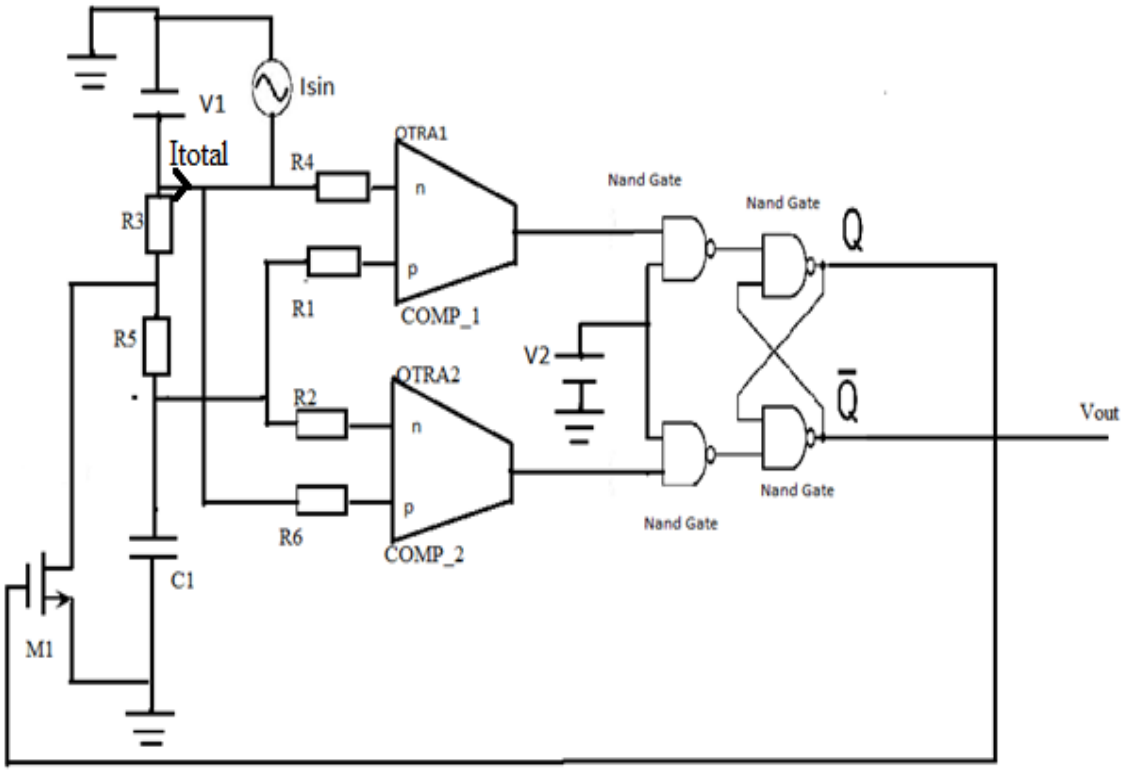


Fig. 6.6 Proposed Pulse Width Modulator Using Timer circuit.

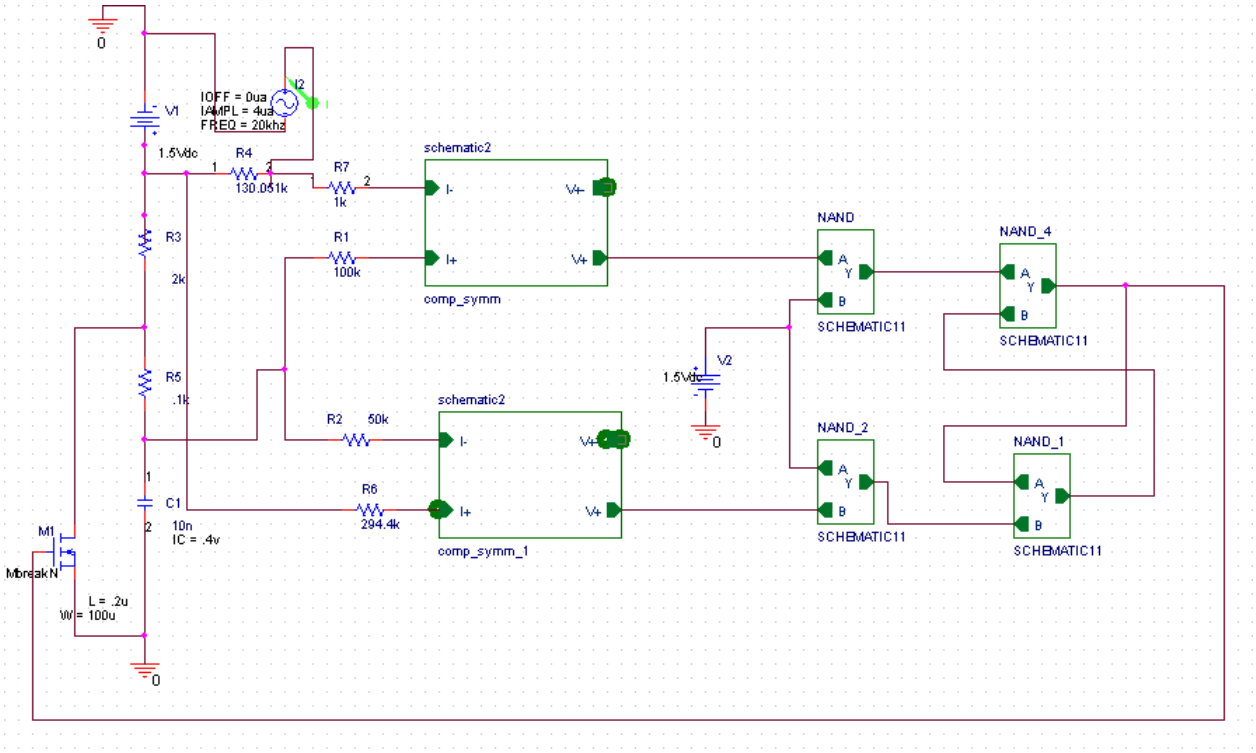


fig.6.7 Pspice schematic of Pulse width modulator

As C_1 further discharged to a voltage level such that current through I_n of comp_2 gets equal and then lesser than I_P (1/3*Itotal), output of comp_2 changes to Vcc. Whereas, output of comp_1 remains at 0V.Now, flip flop inputs are S=0, R=1, hence its output is at state Q=0. Hence, M_1 gets OFF and C_1 stops discharging via M_1 path.

Now ,current level at I_n of comp_1 is shifted to sum of $2/3*I_{total}$ and sinusoidal current signal and hence same cycle repeats but charging time and voltage up to which the capacitor charges is different(lesser than values for values when sinusoidal current was I_1). This operation repeats again and again as trigger pulse is applied periodically. Output waveform of pulse with modulator is shown in fig.6.13 and 6.14.

6.5 Application of Timer circuit

- Precision timing
- Pulse generation
- Sequential timing

- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Missing pulse detector

6.6 SIMULATION AND EXPERIMENTAL RESULTS

The performance of the proposed Timer circuits is verified through SPICE simulation using 0.5 μm CMOS process parameters provided by MOSIS (AGILENT). CMOS implementation of the OTRA [3] shown in Figure 2 is used for timer circuit realization and supply voltages $V_{DD} = -V_{SS}$ = 1.5V are used. Aspect ratio for MOS transistor M_1used in the timer circuit is W/L=.2μm /100μm.

Table:2 Component values used in Astable, Monostable multivibratorand Pulse width modulator

Component Name	Component values		
	Astable multivibrator	Monostable multivibrator	Pulse width modulator
R_1	100KΩ	100KΩ	100KΩ
R_2	50 KΩ	50 KΩ	50 KΩ
R_3	2 KΩ	2 KΩ	2 KΩ
R_4	129.68 KΩ	129.68 KΩ	129.68 KΩ
R_5	.1 KΩ	-------	.1 KΩ
R_6	294.4 KΩ	294.4 KΩ	294.4 KΩ
R_7	----------	----------	1 KΩ
C_1	20pF	100pF	100pF

6.6.1 Simulation Results of Astable Multivibrator Circuit

The astable multivibrator is designed for frequency 5.029MHZ.There is no input pulse for astable multivibrator. Capacitor charging and discharging in astable multivibrator is shown in fig., taking initial value of capacitor is 0.4V. The capacitor voltage varies between 1.12V and 0.226V. The waveform of capacitor voltage V_{C1} and output voltage V_{out} with time as shown in fig.6.8, fig6.9, fig.6.10. The duty cycle corresponds to this components is 47.45%.

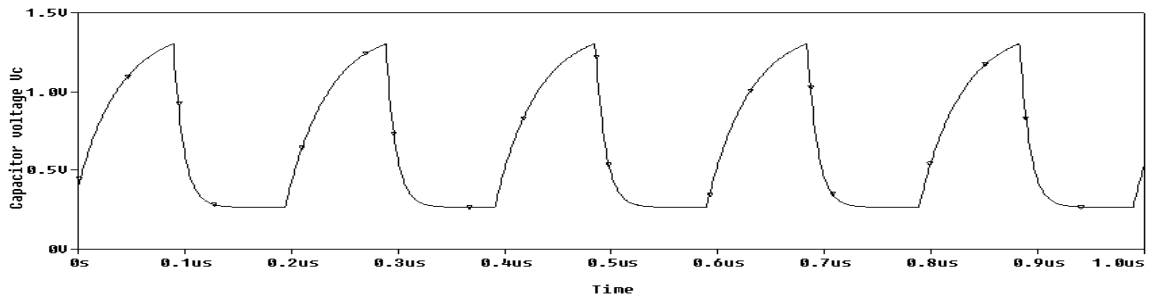


Fig.6.8 charging and discharging waveform of capacitor voltage

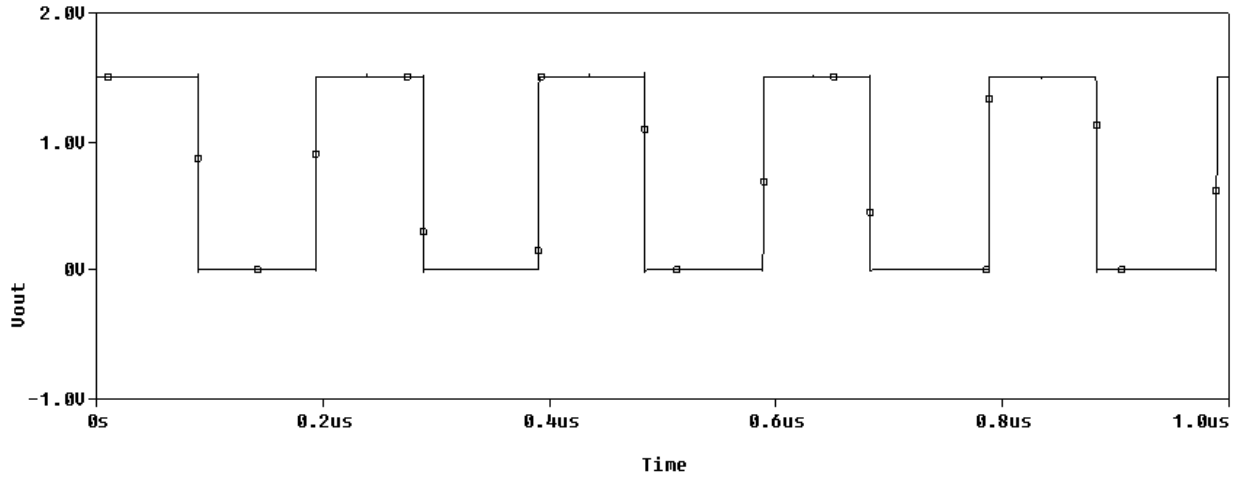


Fig.6.9 Output Voltage Waveform of Proposed Astable multivibrator

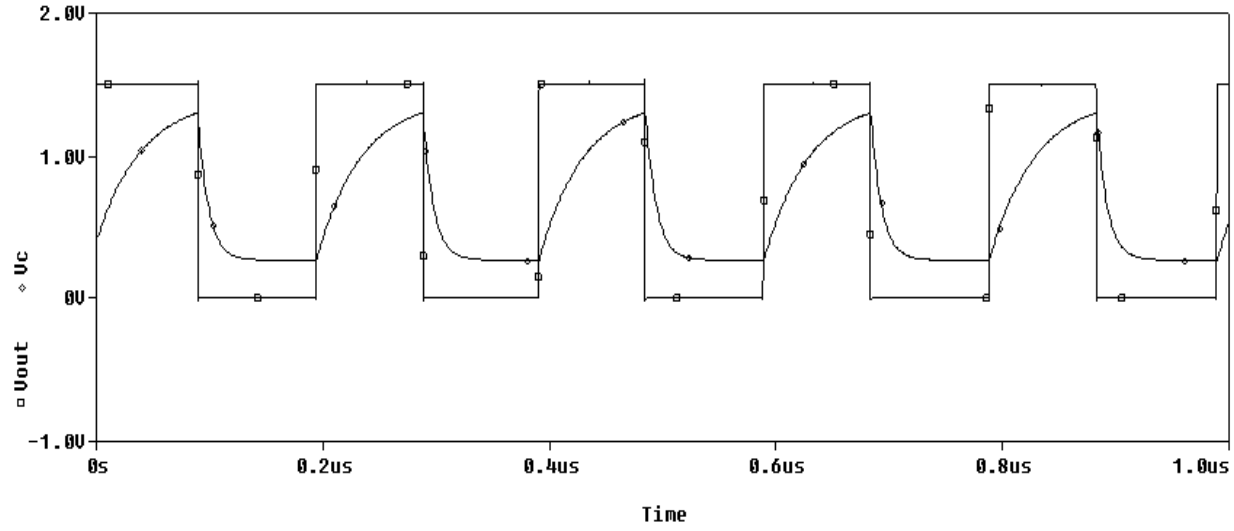


Fig.6.10 Waveform of capacitor voltage and output voltage with time.

6.6.2 Simulation Results of monostable Multivibrator Circuit

For monostable operation of this circuit, a negative current pulse is applied at the negative terminal of OTRA-2 .The current pulse is shown in the figure 5.11(a). The amplitude of current are I_1=11uA and I_2=0uA.Capacitor charging, output voltage variation with the current pulse input is shown in the figure 6.11(b), 6.11(c).

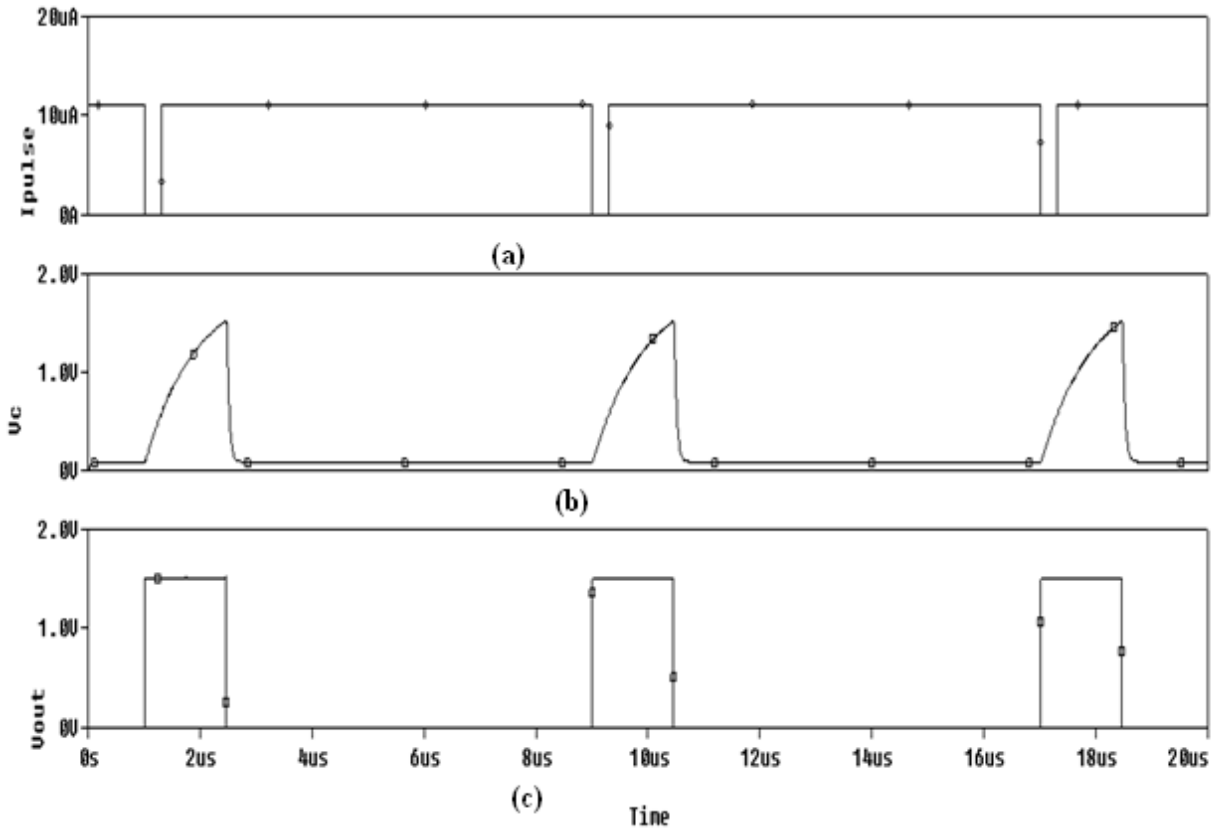


Figure.6.11 (a) current pulse input (b) Capacitor voltage variation (c) output voltage variation.

6.6.3 Simulation Results of Pulse width modulator Circuit

There is another application of Timer circuit as a Pulse width modulator. In this circuit a sinusoidal current signal of frequency of 20Khz is applied at I_n input of comp_1,shown in fig5.12.Figure 5.13 shows the pwm output waveform Vout when applied sinusoidal signal frequency is 10Khz. Figure 5.14 shows the pwm output waveform Vout when applied sinusoidal signal frequency is 20KHz.

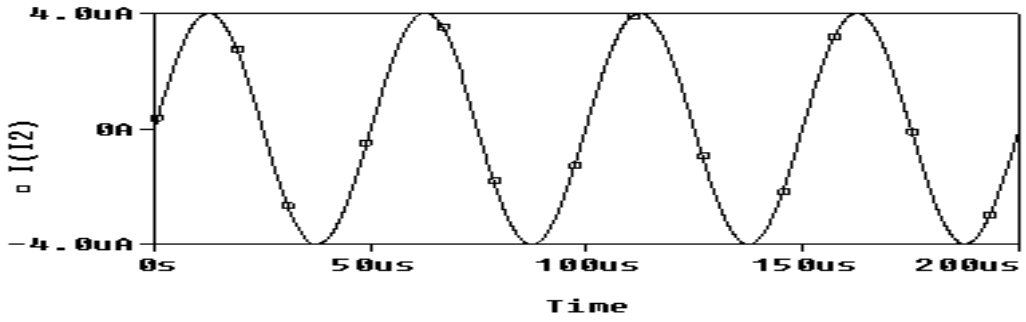


Fig.6.12 sinusoidal current signal

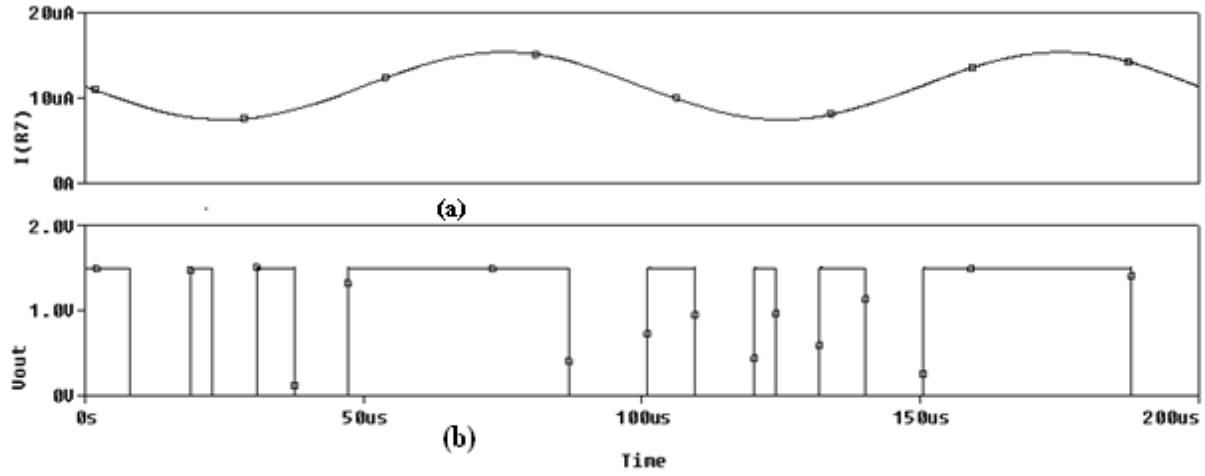


Fig.6.13 (a) when applied sinusoidal signal frequency is 10 KHz. (b)PWM output waveform

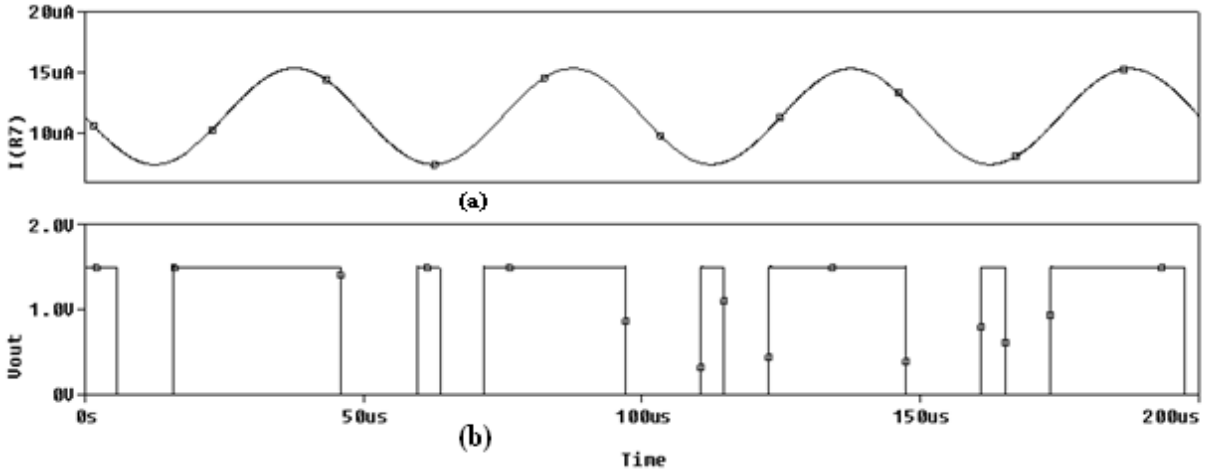


Fig.6.14 (a) when applied sinusoidal signal frequency is 20 KHz. (b) PWM output waveform

6.7 Electrical characteristics of Timer Circuit

Table: 4Electrical characteristics

PARAMETERS	**RATING**
Supply Voltage Vcc	1.5V
Power Dissipation at Temperature 27◦C	2.1mWatt
Maximum Operating Frequency	7MHz
Trigger Current	9uA<I<16uA
Rise Time of Output	.73nsec

Fall Time of Output	.343nsec
Comparator input current(maximum)	16uA
Ambient Operating Temperature	0 to 70°C

REFERENCE

[1]. M.GEETHA PRIYA ,AND K. BHASKERAN"A novel low paper 3 transistor based universal gate vlsi application "Journal of Scientific and industrial Research Vol.72, April-2013,pp.217-221

[2]. Journal Of Engineering Sciences & Research Technolog " Design Analysis And Circuit Enhancements Of Sr-Flip Flops"By Prof. Olawale J. Omotosho, Engr. Samson O. Ogunlere2,Issn: 2277, Impact Factor: 1.852, September-2013.

[3] H. Mostafa and A. M. Soliman, "A modified CMOS realizationof the operational transresistance amplifier (OTRA),"*Frequenz*, vol. 60, no. 3-4, pp. 70–76, 2006.

CONCLUSION AND FURTHER SCOPE

There are literally thousands of different ways that the 555 can be used in electronic circuits. In almost every case, however, the basic circuit is either a one-shot or an astable. The application usually requires a specific pulse time duration, operation frequency, and duty-cycle. Additional components may have to be connected to the 555 to interface the device to external circuits or devices.

While the commercially available 555 Timers have limitations in terms of speed and parameter tolerance, the concept itself is very flexible. With the availability of high-speed voltage comparators and gates, the configuration of the 555 Timer can be easily constructed, resulting in performance in the MHz range.

The OTRA is gaining increasing attention as a basic building block in analog circuit design. It is a building block having advantages of operating from low voltage supplies and overcomes the finite gain bandwidth product associated with traditional op-amp. The motive behind the design of OTRA is to provide amplification of high frequency signals with the ease of using standard operational amplifier.

In this thesis efforts are made to study the scope of OTRA as an active building block in analog circuits. Various CMOS realization of OTRA present in the literature are studied and these circuits are used to realize various signal processing and generating circuits having applications in communication. All the circuits were simulated using PSpice program and 0.5um process parameters. Simulation results show that the various characteristics are in good agreement with the theory. Slight variations in the results arise due to the non ideal behavior of the OTRA used. Further, a number of analog circuits can be designed using OTRA**.**

Operational amplifiers and some commercial IC's are commonly used to construct detectors and multivibrators. But these voltage mode circuits have some disadvantages like complex internal circuitries and use of more passive components.

APPENDIX

CMOS parameters model files

Model file for NMOS transistor

```
.MODEL  Nbreak  NMOS
+ LEVEL=3
+ UO=460.5
+ TOX=1E-8
+ TPG=1
+ VTO=.62
+ JS=1.8E-6
+ XJ=.15E-6
+ RS=417
+ RSH=2.73
+ LD=4E-8
+ ETA=0
+ VMAX=130E3
+ NSUB=1.71E17
+ PB=.761
+ PHI=.905
+ THETA=.129
+ GAMMA=.69
+ KAPPA=0.1
+ AF=1
+ WD=1.1E-7
+ CJ=76.4E-5
+ MJ=.357
+ CJSW=5.68E-10
+ MJSW=.302
+ CGSO=1.38E-10
+ CGDO=1.38E-10
+ CGBO=3.45E-10
+ KF=3.07E-28
+ DELTA=0.42
+ NFS=1.2E11
+ W=90U
+ L=4U
```

Model file for PMOS transistor

```
.MODEL Pbreak PMOS
+ LEVEL=3
+ UO=100
+ TOX=1E-8
+ TPG=1
+ VTO=-.58
+ JS=.38E-6
+ XJ=.1E-6
+ RS=886
+ RSH=1.81
+ LD=3E-8
+ ETA=0
+ VMAX=113E3
+ NSUB=2.08E17
+ PB=.911
+ PHI=.905
+ THETA=.12
+ GAMMA=.76
+ KAPPA=2
+ AF=1
+ WD=1.4E-7
+ CJ=85E-5
+ MJ=.429
+ CJSW=4.67E-10
+ MJSW=.631
+ CGSO=1.38E-10
+ CGDO=1.38E-10
+ CGBO=3.45E-10
+ KF=1.08E-29
+ DELTA=0.81
+ NFS=.52E11
+ W=200U
+ L=4U
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