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on

Design of Ultra Low Voltage Low Noise Analog Front End for Bio-Potential Signals

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by

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CERTIFICATE

This is to certify that the dissertation titled "**Design of Ultra Low Voltage Low Noise Analog Front End for Bio-Potential Signals**" is a bonafide record of work done by **Maheep Dwivedi, Roll No. 2K12/VLS/11** at **Delhi Technological University** for partial fulfilment of the requirements for the degree of Master of Technology in VLSI and Embedded System Design. This project was carried out under my supervision and has not been submitted elsewhere, either in part or full, for the award of any other degree or diploma to the best of my knowledge and belief.

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ABSTRACT

The information extracted from the bio-potential signals such as ECG, EEG, ECoG, ERG and ENG is extensively used for health care and medical treatment purposes. The use of bio-potential acquisition systems is not only limited to the hospitals but also extended to the homes for ubiquitous health care. Therefor the demand of portable bio-signal measurement system is increasing. The key constituent to this kind of systems is the analog front-end (AFE). The analog readout front-end extracts the bio-signals directly from human body through electrodes and defines the extracted signal quality.

The most critical block in an bio-potential acquisition system is the AFE as it is connected directly to the human body and the output this should be ready to feed the subsequent stages that are ADCs and DSPs. This block must operate under low power consumption with minimal added noise to ensure the better signal quality with enhanced battery life, when incorporated in portable bio-signal acquisition systems.

In this dissertation a novel multi-function Analog Front-End is proposed. This analog readout front end is oriented to be employed in flexible and portable bio-potential signal acquisition systems. The essential contribution of this work is the new Forward Body Biased Current Mode Amplifier (FBBCMA) based on convention forward body biased technique for low-voltage operation. The proposed FBBCMA achieves very low noise performance because of inherent properties of current mode topology. Forward body biasing of MOS devices further reduces the flicker noise that is a critical concern in circuits operating at low frequencies. Low power consumption and other advantages are achieved by the aid of the forward body biasing and current mode topology.

A complete analog readout front end is implemented and simulated using the standard TSMC 180nm parameters and P-Spice as simulator. This AFE consist of a pre amplifier followed by a band pass filter to enhance in band signals and reject the signals that are laying out of the band of interest. Tuneable bandwidth of AFE enables it to serve as the first stage in variety of bio-signal acquisition systems. The simulation results show that the designed circuits meet the basic requirements of the low power consumption under low noise operation for long time portable bio-potential recorders.

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INTRODUCTION

1.1 Motivation

The design methodologies of medical devices have evolved a lot with the expansion of integrated circuit over the last 40 years. Evolution of circuit technologies has facilitated the development of medical devices and the burgeoning need of health-care equipment has created a large demand for the new technology medical devices. In ubiquitous healthcare, acquisition and processing of bio-potential signals play a vital role. Bio-potential signals are commonly recorded in clinical centres for medical diagnosis and even at home for healthcare purpose. The most critical building block of such bio-signal acquisition systems is the analog front-end. This chapter introduces the challenges which occur while designing analog readout front-ends of bio-signals and the electrical characteristics of bio-potential signals with their associated acquisition system design.

Among the three categories of medical devices, implantable, in-vitro and external, designing of implantable devices is the most challenging task. The requirement of these devices to have low noise under low power consumption makes the design task cumbersome. Implantable medical devices include stimulatory devices, like pacemakers, implantable cardioverter defibrillators, neuro-stimulators and cochlea implants and measurement or control devices such as drug infusion, implanted diagnostic sensors and the very rapidly growing implanted diabetes monitor. Other than this, at medical and health-centres bio-potential signal acquisitions systems plays a critical role in diagnosis of various ailments.

While the bio-potential signals are being recorded from humans, the analog readout front-end circuits has to encounter various problems. These problems are because of extremely weak characteristics of bio-potential signals and the complex recording environments for different kinds of applications. In design perspective, despite the performance afforded by modern IC technology, electronic systems associated with implanted medical applications present formidable low power and low noise design challenges.

1.2 Multi-Functional Bio-potential Analog Front-ends:

Nowadays, doctors can extract more and more information from bio-potential signals of human body for healthcare and diagnosis purposes. Electrocardiogram (ECG), Electroretinogram (ERG), Electroencephalogram (EEG), Electrocorticogram (ECoG) and neural signals are of utmost concern. The acquisition process of bio-signals signals is normally safe and efficient for patients, and doctors can examine the conditions prevailing inside the human body and perform possible treatments. Moreover , the growing demand for home healthcare applications makes Multi-functional bio-potential signal acquisition systems even more advantageous. These not only help in improving the quality of life but also extend applications to sports, entertainment and comfort monitoring [1].

In this dissertation a multi-functional analog readout front-end is proposed that measures cardiac, visual and all sort of neural signals. This single analog front-end can be tuned to measure ECG, EEG, ECoG, ERG and neural signals with low power consumption. Low power consumption makes it extremely useful for portable applications and in addition to this, these low power consumption circuits add very little noise which in turn maintains the signal quality. It is a Current-mode AFE (Analog Front End), the detailed discussion of advantages of current-mode circuits over voltage-mode circuits is presented in subsequent part of this chapter. The simulation results show that the proposed low power low noise current-mode AFE meets the basic requirements of the long-time portable bio-potential acquisition system and is ready for connecting to next stages like ADC and DSP.

1.3 Bio-potential Signals:

Bio-potential signals are electrical potentials between the membrane of certain cells of nervous, muscular and tissues. Generally, these cells exhibit resting potential when they are at rest and action potential when stimulated.

The mechanism of resting potential is , when there is a change in the concentrations of ions between the two sides of the membrane of cells. The diffusion of K^+ from inner to outer membrane of the cell makes the concentration of free negative ions higher. This

increase in concentration of free negative ions causes the inner membrane to be more negative than the outer membrane. Thus the free negative ions attract K^+ to prevent the diffusion and finally the cell reaches a steady state. The equilibrium is reached with a polarization voltage in the range from -20 mV to -100 mV and this value is usually between -70 mV to -90 mV.

When the cells are at resting potential, only K^+ can diffuse freely through the membrane. After the stimulation of the cells once , the mobility of K^+ and Na^+ (also some Ca^{+2}) change. Diffusion of Na^+ ions into the cell makes it depolarized. When the depolarization of Na^+ reaches the threshold value, the action potential is produced. At this moment, the mobility of K^+ is enhanced on the depolarized membrane and that of Na^+ reduces to resting state, and the potential eventually restores to resting potential level. To make the cell polarized, the conductivity of K^+ is temporary increased and thereafter the cell restores to its resting state smoothly. This cycle of cellar potential is called action potential.

Bio-potential signals such as ECG, EEG, ECoG, ERG and neural signals are generated primarily due to combination of action potentials of different cells. The amplitude levels of bio-potential signals are very small practically and these are located at very low frequency band. They are prone to be affected by noise and common mode interference of human body, when extracted from surface placed electrodes. This may lead to false information about the physiology of the patient.

1.3.1 Electrocardiogram:

ECG (also known as EKG, abbreviated from the German word), is a surface measurement of the electrical potential caused by electrical activity in cardiac tissue [2]. The contraction and dilation of the heart that leads the heart's pumping action causes a current flow, in the form of ions. The ECG has become a routine part of any complete medical evaluation because these signals help to diagnose many diseases. ECG is being used as a diagnostic test since its discovery. Many types of damages of heart tissues can be detected with an ECG because an ECG is a measure of the electricity that is conducted through the heart muscle (known as the myocardium). The ECG waveform allows one to

infer information about electrical activity associated with different aspects of a heart-beat and is therefore of particular value for assessing an individual's cardiac rhythm and heart health.

A normal cardiac rhythm is originated in the sino-atrial node (S-A node)so it is referred to as a "sinus" rhythm. When this sinus rhythm gets disrupted, the phenomenon that causes death , it is known as arrhythmia. "Pacemaker" cells present in S-A node triggers each heartbeat. These cells generate action potentials at the rate of 60 - 100 beats per minute (while at rest). Action potentials propagate throughout the myocardium in a predefined way and depolarize the tissues by contraction. After the departure of action potential from S-A node, The two upper chambers of heart depolarized by them, these two upper chambers of the heart are known as the atria. After this, these stimuli move to the atrio-ventricular node (A-V node). The A-V node sits between the atria and the ventricles (the two lower chambers of the heart). It performs action of a backup pacemaker at a lower rate of 40 - 60 beats per minute. Another function of A-V node is to delay the electrical impulses up to about 120ms. By slowing down these pulses A-V node gives the atria enough time to pump their blood into the ventricles before ventricles' contraction. After the action potentials leave the A-V node, they propagate to the area known as the "His" bundle. Now the ventricles are depolarized by conductive fibres known as Purkinje fibres, depolarization starts from the left ventricle and swings to the right. After the depolarization and contraction of ventricles, the cycle starts over with another impulse from the S-A node [3].

The Electrocardiogram is a representation of the electrical activity of an ensemble of cells in the myocardium. It is a vector measurement electrical potential across the surface of the body. A typical ECG waveform (as shown on the right side of Figure 1.1) is composed of three primary features: the P wave, the QRS complex, and the T wave. Each wave has its own significance in medical diagnosis as all of them correspond to the electrical activity in specific parts of the heart.

P wave: it comes first and represents the depolarization of the atria. It causes the contraction in the atria. As described earlier the delay produced by A-V node is present in the wave as the the delay between the P wave and the QRS complex, also known as the

PR interval. This interval gives the atria time to contract before depolarizing the ventricles.

The QRS complex: This represents the combined effect of re-polarization of the atria and depolarization of ventricles. The R spike represents the contraction of ventricles. QRS complex is usually the strongest wave in an ECG.

T wave: The last wave is the ECG is known as T and it represents the re-polarization of the ventricles. And ***U wave*** (if present) is generally considered as the result of after potential in the ventricular muscles. Taking a differential measurement of the electrical potential on the body surface at different locations generates different ECG vectors. In practice ECG signals has amplitude of order of few µ Volts and lies between 300 mHz to 150 Hz

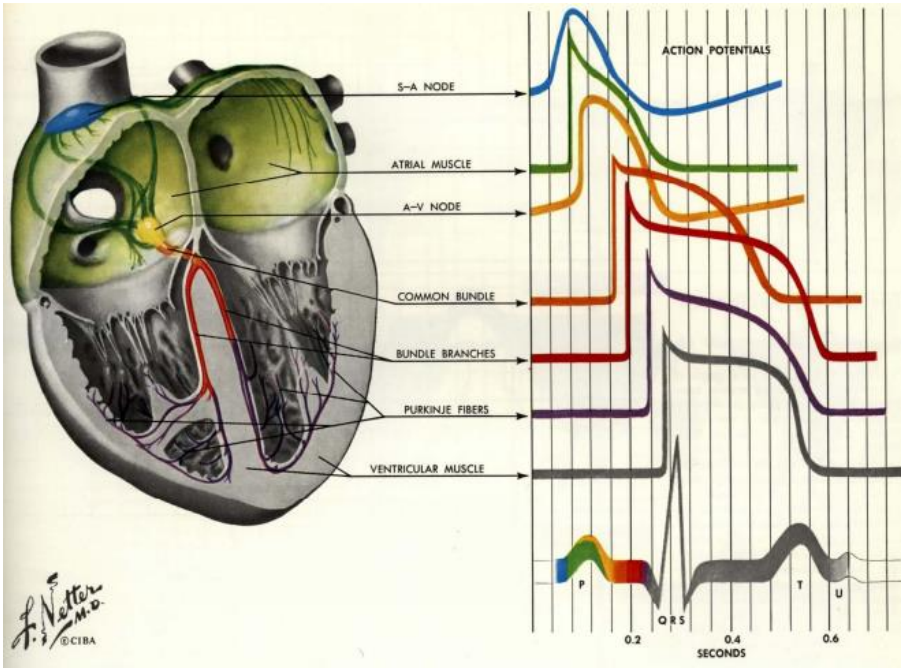

Figure 1.1: An ECG waveform is composed of action potentials originating in different areas of the heart. The ECG waveform recorded at the skin is the superposition of these different action potentials. [3]

Ideal Amplitude and duration of all components of the ECG signals are as follows [2]:

Amplitude:	P wave	0.25mV
	R wave	1.60mV
	Q wave	25% of Rwave
	T wave	0.1mV 0.5mV
Duration:	P-R interval	0.12 to 0.20 sec
	Q-T interval	0.35 to 0.44 sec
	S-T segment	0.05 to 0.15 sec
	P wave interval	0.11 sec
	QRS interval	0.09 sec

1.3.2 Electroencephalogram and Electrocorticogram:

The electroencephalography is a measurement of potential fluctuations of brain. It is firstly reported by a German psychiatrist Hanse Berger [3]. The EEG can help diagnose conditions such as epilepsy, brain tumours, brain injury, cerebral-palsy, stroke, liver kidney disease or brain death and helps to find many other physical problems [4].

Conventionally, there are three types of electrodes that are used to measure the electrical activity of brain- scalp, cortical and depth electrodes. When the electrodes are placed at exposed surface that is cortex of the brain, such recording is known as ***Electrocorticogram (ECoG.)*** . Another semi invasive method is to use insulated needles, in such case recording is referred to as a depth recording. In this kind of recording the insertion of appropriate size needle (electrode) causes little damage to brain tissue [3]. The EEG is typically 100 µV in amplitude with a frequency response of 0.5 to 80 Hz [4]

In ***Electrocorticogram (ECoG.)*** a specific set of neurons (also known as motor) is selected and potential fluctuations are measured through these motors. An example of such case is measurement of the evoked potential, after measurement of evoked potential the wish of patient can be interpreted. This kind of measurement is used in brain computing interface (BCI). The study and description of BCI and calculations of ECoG are beyond the scope of this work.

Signals	Bandwidth	Amplitude
Electrocortecography (Ecog)	0.5-200 Hz	< 100 µV
Electroencephalography (EEG)	< 100 Hz	10-20 µV
Neural	1Hz-5KHz	<500µV

Recording system: There is a slandered system for measurement of EEG recommended by the International Federation committee Society of Electroencephalography and Clinical Neurophysiology (IFSECN) that is known as a 10-20 system. The "10" and "20" refer to the fact that the actual distances between adjacent electrodes are either 10% or 20% of the total front-back or right-left distance of the skull. Another system is 20-21 system in same reference.

The American Society of Clinical Neurophysiology recommends the use of at least 21 electrodes for better resolutions. The electrodes with an even number are placed on the right and electrodes with a odd number are placed on the left side of the head. The letters specify an anatomical area; e.g. “F” means frontal, the electrodes between the ears are specified by “Cz”. The electrodes T3 and T4 of this system are referenced as a T7 and T8 in extended systems; and the electrodes T5 and T6 are referred as a P7 and P8 in the new nomenclature. See figure 3.2. The EEG helps physicians to study and analyse electrical activity in the brain [3].

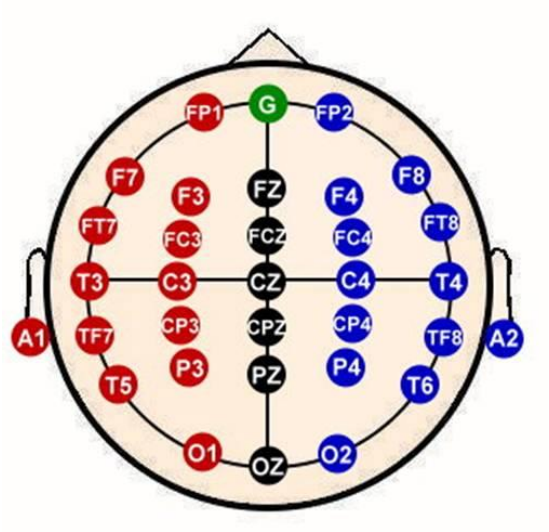

Figure 1.3: EEG electrode 10-20 system.

EEG signals features: The EEG signals are potential fluctuations with low frequencies recorded by scalp electrodes. The only required information about patient is his or her age and status, before starting the EEG. The status of the patient means the general clinical status of conscience in which the patient is. The analysis of EEG signal is pretty complex due the immense amount of information that is received by each electrode. The sorting criterion for different waves is their main frequency component and in some cases their shapes. There are six main groups that are defined as follows [5]:

Beta(β) activity: Beta activity is associated with signals having main frequency components between 13Hz and 30 Hz, and amplitudes between 5 µV*pp* to 20 µV*pp*. Figure 3.3 shows the β activity. β activity is associated with the reasoning, attention and focusing. It can reach 40Hz during the intense mental activity [5].

Alpha(α) activity: α activity is associated with signals having main frequency components from 8Hz to 13Hz, and amplitudes between 30 to 50µV*pp*. The Alpha waves are associated with mental relaxation and poor interest in something [5].

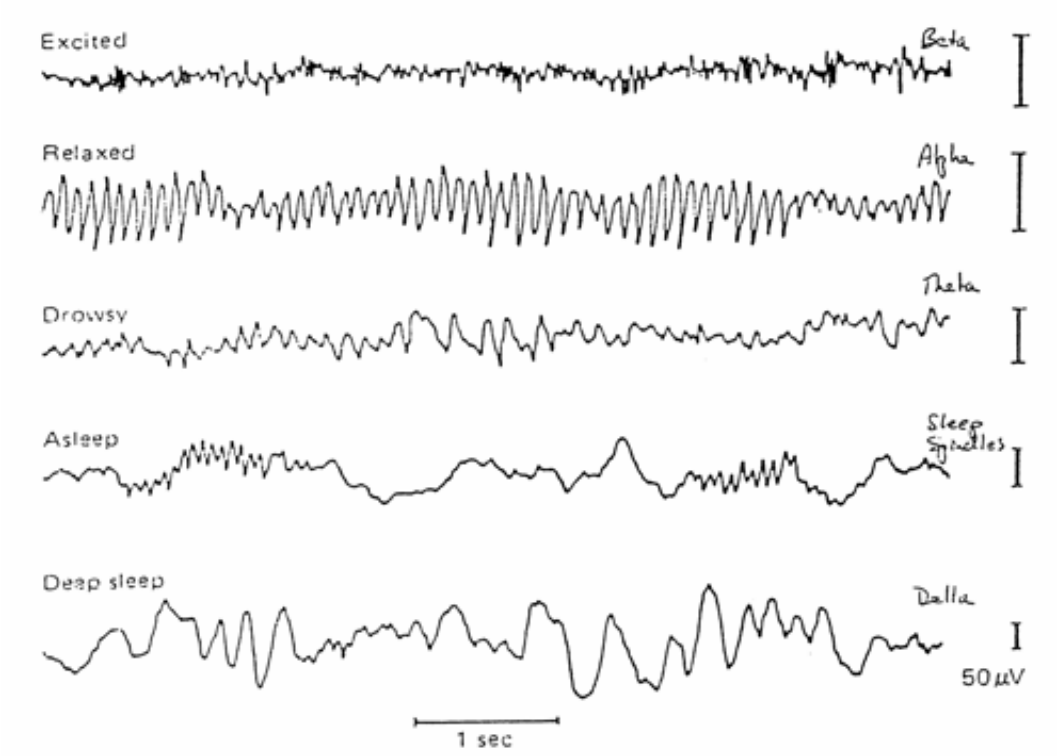

Figure1.3: Various EEG traces [4].

Mu(μ) activity: Mu(μ) activity can be defined as a spontaneous signal having frequency response around 8 to 10Hz and is the central rhythm of the Alpha activity. It can be measured in the motor cortex.

Delta(δ) activity: The Delta activity produces signals that have frequencies between 0.5Hz and 4Hz, with variable amplitude. The Delta signals are associated to the dream activity and if they are found in an awake patient, then it indicates malfunctioning of the brain.

Gamma(γ) activity: This activity is associated with the frequencies range of 35Hz to 100 Hz. This activity is related to cognitive tasks such as attention, learning and memorization.

Theta(θ) activity: Signals generated due to θ activities have frequencies from 6 to 7Hz, with the amplitude of more than 20 μV*pp*. The theta activity is reinforced by mental stress, like frustration in the frontal area of the brain. The Theta activity is also associated to the inspiration and depth meditation whose dominant frequency is 7Hz [5].

1.3.3 Electroretinogram:

ERG is the recording of electrical potentials evoked by a flash of light and picked up at the cornea of the eye using contact lens electrode [6]. It is a measure of the electrical response of the eye's light-sensitive cells, called rods and cones. These cells are part of the retina (the back part of the eye). The electroretinogram (ERG) is an electrophysiological tool used to measure electrical activity originating in the outer part of retina in response to a light stimulus. Deficiencies occurring at different levels of the retina can be detected by ERG. ERG signal is composed of a sequence of components originated in various retinal layers and provides valuable physiological information about the photoreceptor behaviour in the human eye. Understanding the explicit features (onset, time delay, amplitude, line shape) of the ERG components and their relationship characterizes the principal aim of past and present research in the field of ocular electrophysiology.

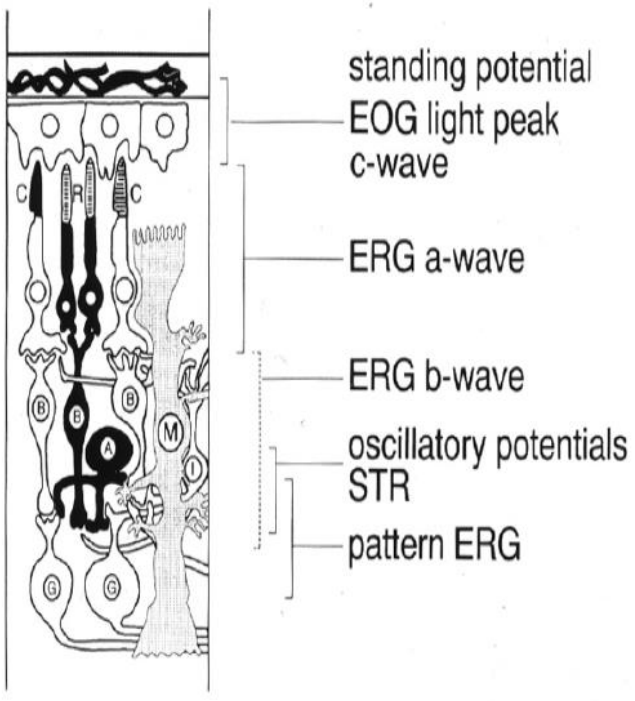

Figure 1.4: Simplified scheme of the human retina with the approximate sites of generation of electrophysiological signals [6].

Furthermore, the shape of the ERG wave indicates the likely retinal cell type responsible for the deficit. It consists of various components (wavelets) which generates in different layers of the retina reflecting light evoked potentials caused by different cells shown in Figure: 1.4. in the figure 1.4 A- amacrine cells; B- bipolar cells; C- cone photoreceptors; G- ganglion cells, I- interplexiforme cells, M- Müller (glial) cells; R- rod photoreceptors. The amplitude of an ERG signal is of the order of few µVolts that lies between the frequency range of 0.3 to 300Hz (in special case upper range may change)

The five different kind of ERG recording as per standards is depicted in figure 1.5.

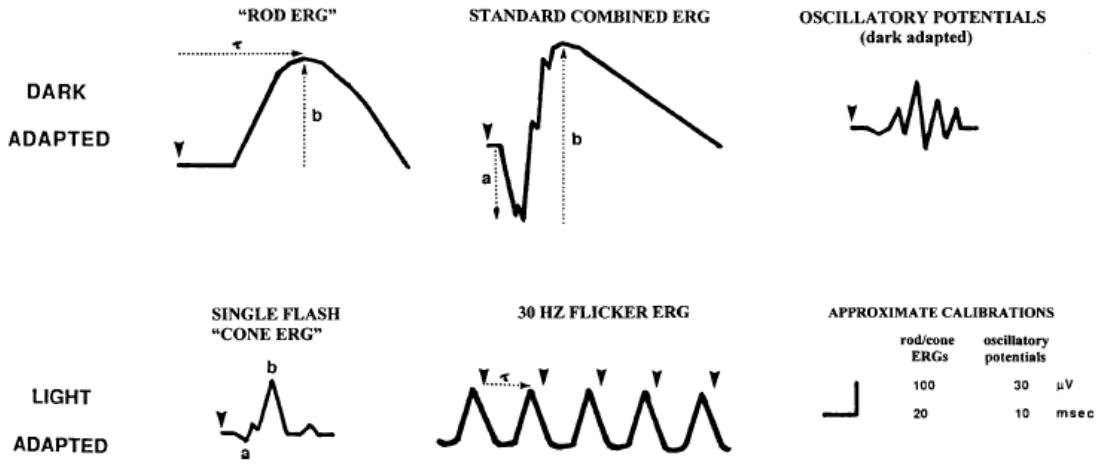

Figure 1.5: Diagram of the five basic ERGs defined by the Standard. These waveforms are exemplary only, and are not intended to indicate minimum, maximum or even average values. Large arrowheads indicate the stimulus flash. Dotted arrows exemplify how to measure time-to-peak (t, implicit time), as-wave amplitude and b-wave amplitude [7].

The ***early receptor potential (ERP)*** shown in figure 1.6 is a rapid discharge recorded with a very high intensity flash in a well dark adapted eye using high–frequency amplifiers. The ***a–wave*** is a negative potential produced extra-cellularly along the radial path from the cell body of the photoreceptors that hyperpolize in response to light, and it is an important component of the clinical ERG as a measure of photoreceptor activity. The a–

wave is made up of two components i.e., a1 and a2, generating from the cones and rods respectively.

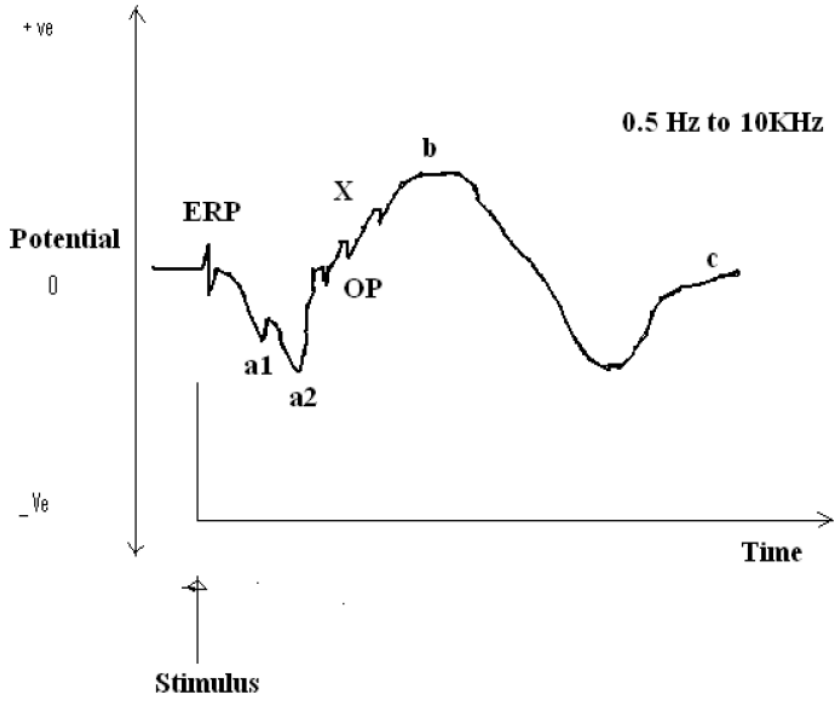

Figure 1.6: The Elecroretinogram (ERG) Signal [6]

The ***b–wave*** is the most readily recordable component of the clinical ERG. It reflects the postsynaptic summed neuronal activity of the inner nuclear layer and is thus an important measure. ***B–wave*** composed of two components, b1 and b2, representing the cone–mediated and rod–mediated responses like a-wave.

On the rising phase of the b-wave a rapid oscillation is evoked by a bright flash known as the ***oscillatory potential (OP)***. The last oscillation, that is relatively well defined can be measured and is called the ***x–wave*** or b1. The amacrine cells, the inner plexiform layer and optic nerve fibres have all been suggested as possible generators of the oscillatory potential. The ***c–wave*** is a small, slow, positive deflection after the b–wave. Although it actually started slowly from the beginning of light stimulation but it appears after b-wave only. Briefly the integrity of the pigment epithelium and photoreceptors is an essential factor for the generation of the c–wave.

1.4 Objective and Scope of the Project

The objective of this thesis is to a multi-function analog readout front end using P-spice Simulator. The parameter used in this work is TSMS standard 180nm level 7 parameter. The low-power and low noise analog front end is designed that produces a signal that is ready to use as an input to the ADC. The low power consumption makes it useful for portable applications while small amount of added noise ensures the signal quality.

This is a read out front end with tunable frequency, which ensures the utility of this AFE in variety of bio-signal recording systems. Multifunctioning along with low power consumption and low noise operation are key features of this analog readout front end.

1.5 Organization of Dissertation

The thesis outline is as follows:

Chapter 2: This chapter provides the well needed theoretical background for designing a low-voltage analog circuit. A comparison between the current mode and voltage mode topologies is illustrated.

Chapter 3: This chapter provides an insight to the forward body biased operation of the MOS devices. Along with the threshold voltage analysis, dependence of threshold voltage on forward body voltage is discussed.

Chapter 4: In this chapter detailed description of the proposed forward body biased current mode active block is presented. Large portion of the chapter deals with the design of forward body bias op-amp, last section describes the current mode amplifier architecture and working of the same, including the simulated results.

Chapter 5: This chapter gives an elaborated analysis of noise introduced by the active block in previous chapter. The noise added by the proposed active block is modeled and simulated in this chapter.

Chapter 6: This chapter provides the complete design of low-power low-noise analog read out front end for cardiac, visual and all kind of neural signals and simulation results for the same.

Chapter 7: This chapter deals with the conclusion from the interpreted results and explores the future work for this work.

CHAPTER 2

THEORETICAL BACKGROUND

With the continuously expanding market for portable devices such as wireless communication devices, portable computers, consumer electronics and implantable medical devices, low power is becoming increasingly important in integrated circuits. The low power design enables to increase operation time and/or utilize a smaller size and lighter-weight battery.

The analog power supply must be at least the sum of the magnitudes of the n-channel and p-channel thresholds [8]. The threshold voltages of future CMOS technologies may not decrease much below the existing values of available nowadays. Low voltage circuits in the future will be incompatible with the standard CMOS technology. Consequently, low-voltage circuit design methodologies are required to make compatible future CMOS technologies with low-voltage requirements. Figure 2.1 shows the trends of the threshold voltage from the 1µm to the 22nm CMOS process.

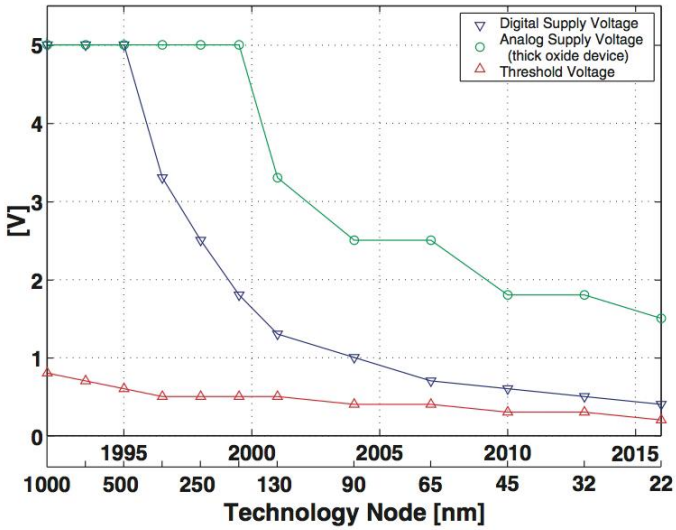

Figure 2.1: Supply voltage and threshold voltage of different technologies [9].

In this Part, several design methodologies of low power complementary metal-oxide-semiconductor (CMOS) analog integrated circuit design are investigated.

Node	Nm	250	180	130	90	65	⇓
L_{GATE}	Nm	180	130	92	63	43	
t_{OX} (inv.)	Nm	6.2	4.45	3.12	2.2	1.8	⇓
Peak g_m	µS/µm	335	500	720	1060	1400	⇑
g_{ds}**	µS/µm	22	40	65	100	230	⇑⇑
g_m/g_{ds}	-	15.2	12.5	11.1	10.6	6.1	⇓
V_{DD}	V	2.5	1.8	1.5	1.2	1	⇓⇓
V_{TH}	V	0.44	0.43	0.34	0.36	0.24	⇓
f_T	GHz	35	53	94	140	210*	⇑⇑

Table 2.1 MOS device parameter trendz.

The low-voltage/low-power design can utilize a smaller size or a lighter-weight battery and increase operation time between battery recharging cycle. Among several available device technologies such as bipolar junction transistor (BJT), gallium arsenide (GaAs), complementary metal-oxide-semiconductor (CMOS), bipolar-CMOS (BiCMOS) [10-12], the CMOS technology is the dominant technology in the development of low power portable devices for wide-ranging applications. For more than 20 years, numerous low power CMOS design techniques have been investigated that includes basic circuit design modifications as well as new fabrication techniques. First one inhabits architecture changes for implementing desired functions using low threshold voltage devices, power down strategies, optimization of transistor size, supply voltage scaling, along with other possible techniques [13-15]. While new fabrication technologies comprises carbon neon technology field effect transistor (CNTFET) and FINNFET. In the following section, literature review and historic development of low-power analog CMOS design techniques are presented.

Low-power design drew attention in the early 1990s with expansion in portable consumer electronic market. A critical overview abut change in power dissipation of CMOS circuits changed since 1980 has been described by Kuroda and Sakurai [16]. There is a constant increase in the power dissipation of commercial CMOS chips because of increased clock frequency. For example, power dissipation of a 5 V DSP chip was 0.1 W in 1982, and

increased to 10 W in 1991. Power dissipation peaked in 1990-1991. After 1991, power dissipation of CMOS chips have reduced because of increasing demand of large number of portable systems.

Some of the standard low power techniques as discussed below.

2.1 Sub-Threshold MOS

In the MOS devices gate to source voltage must be greater than a certain value known as threshold voltage (V_T) to turn on the device. When the VGS in the MOS transistor is less than the threshold voltage (V_T), the device operates in sub threshold region or weak inversion. In the sub threshold region the ID depends exponentially on drain to source voltage unlike regular case where curve has quadratic behavior.

Some assumptions are considered in order to develop the model for sub-threshold operation. Channel length modulation effects are negligible. Generation currents in the drain, channel, and source depletion regions are almost negligible. Source and drain currents of MOSFET are equal, density of fast surface states and fluctuations of surface potentials are all negligible. Then the Barron's derivation [8] can easily be extended for case of nonzero source-to-substrate voltage. For an N-channel transistor:

$$I_D = S\mu U_T^2 \sqrt{[\tfrac{1}{2} q \varepsilon_s n_i]}\, e^{-3\phi/2U_T} \frac{e^{\psi_S/U_T}}{\sqrt{\psi_S - U_T}} (e^{-V_S/U_T} - e^{-V_D/U_T}) \quad (2.1)$$

where S is the geometrical shape factor of the transistor (W/L), μ is the mobility of carriers in the channel, ψ_S is the surface potential, U_T is the thermal voltage (kT/q), ε_s is the permittivity of the Silicon, V_S the source-to-substrate voltage, ϕ is the bulk Fermi potential, V_D the drain-to-substrate voltage, V_G is the gate-to-substrate voltage and I_D is the drain current.

Equation 2.1 is valid for:

$$4U_T + \emptyset + V_S < \psi_S < 2\emptyset + V_S \quad (2.2)$$

On the other hand, the depletion capacitance C_d can be expressed as:

$$C_d = \sqrt{\frac{\frac{1}{2}q\epsilon_s n_i}{\psi_S - U_T}}\, e^{\emptyset/U_T} \tag{2.3}$$

Inserting (2.3) into (2.1), yields:

$$I_D = S\mu U_T^2 C_d\, e^{-2\emptyset/3U_T}\, e^{\psi_S/U_T}(e^{V_S/U_T} - e^{V_D/U_T}) \tag{2.4}$$

Because of very slow variation of C_d with ψ_S, I_D shows an exponential behaviour on ψ_S/U_T .

The relation between surface potential and gate voltage is given by:

$$\frac{\partial \psi_S}{\partial V_G} = \frac{C_{ox}}{C_{ox}+C_S} = 1 - \frac{C_G}{C_{ox}} \tag{2.5}$$

Where C_G is the gate-capacitance per unit area. According to (3.5), ψ_S is linearly depending on V_G in the range:

$$4U_T + \emptyset + V_S < \psi_S < 2\emptyset + V_S - 2U_T. \tag{2.6}$$

Then inside this range I_D take the form of:

$$I_{DS} = I_{DO}\frac{W}{L} e^{V_G/nU_T}(e^{-V_S/U_T} - e^{-V_D/U_T}). \tag{2.7}$$

Where I_{DO} is the characteristic current, n is the slope factor, The above equation is also applicable for p-MOSFETs by just changing the signs of all the potential that areV_G, V_S and V_D.

By definition, the gate trans-conductance can be found from equation (2.8):

$$g_{md} = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{1}{nU_T} I_{Ds} \tag{2.8}$$

The small signal source conductance can be found from equation 3.17 as:

$$g_{ds} = \frac{\partial I_{DS}}{\partial V_{Ds}} = \frac{1}{U_T} I_{DO}\frac{W}{L} e^{V_G/nU_T}(e^{-V_S/U_T} - e^{-V_D/U_T}) \tag{2.9}$$

When V_{DS} is less than $3U_T$ the device shows a poor linear behaviour. On the other hand when VDS>>$3U_T$ the conductance is almost constant [17].

2.2 The Composite Transistor

This is another technique for low power design which is based on the regulated-cascode current sink/source and is also known as the self-cascode technique and as the super-transistor [18]. It consists of a cascode configuration and a series feedback loop that upsurges the small signal output resistance without maximizing the voltage drop across the output of the current sink/source.

The composite transistor technique is depicted in the figure 3.1. The transistor T1 is input device that converts the input voltage V1 into drain current Io. The drain current of T1 flows through the drain to the source of the T2. V_{DS} of the transistor T1 is kept stable to reduce channel-length modulation; this is performed by a feedback that consists of an amplifier (transistor T3 and T1) and T2 is nothing but a follower [18].

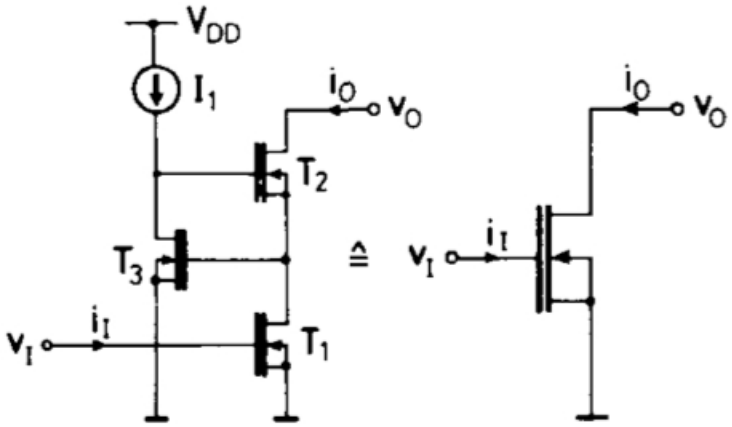

Figure 2.2: Composite transistor. [18]

2.3 The Lateral BJT

This technique overcomes the threshold limitation. When the voltage in the gate is negative enough (approximately $-V_G > 0.6V$) the dependence of the I_D on V_G vanishes, I_D depends only on V_S, staying exponential up to much higher values of current, with a slope n equals to U_T . Figure 2.3 depicts the cross-section of a NMOS transistor and the current flow in bipolar operation.

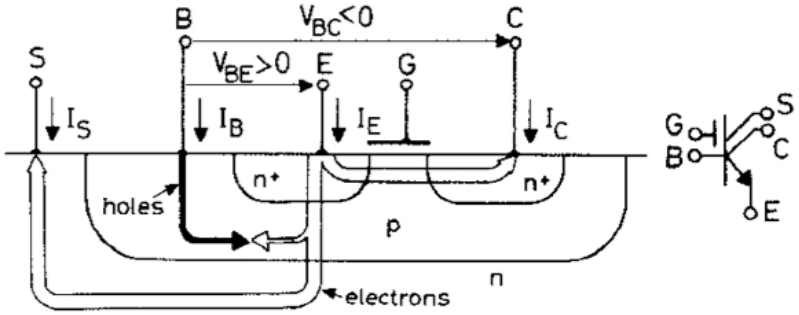

Figure 2.3: Cross-section of a NMOS transistor implemented in a p-well technology and its symbol. [19].

The lateral BJT n-p-n is combined with the vertical n-p-n. Emitter current I_E is parted into a base current I_B, a lateral collector current I_C, and a substrate collector current I_S. To improve device performance the emitter area is minimized along with the lateral base width, and by having the emitter surrounded by the collector, the ratio I_C=I_S is incremented. The presence of the gate that pushes the flow of diffusion carriers away from the surface might even improve the device with respect to normal lateral bipolar [19].

This solution has supplementary advantage of much less 1/f noise because current flow in the bulk of the material. Moreover, another advantage of the lateral BJT is its low value of V_{CE} which is also important in low voltage analog circuits. The only disadvantage the lateral BJT is that it requires turn on voltages of 0.6V to 0.7V so it does not provide that much advantage over the MOSFET.

2.4 Forward-Biased Bulk-Source

While operating the MOSFET at low voltage the only limitation is threshold voltage. This technique is based in reducing the threshold voltage by forward biasing on the bulk-source junction. Threshold voltage of a MOS transistor is given by [20]:

$$V_t = V_{t0} + \gamma\left[\sqrt{2\phi - V_{SB}} - \sqrt{2\phi}\,\right]. \qquad (2.10)$$

Where V_{t0} is the threshold voltage for zero substrate bias (VBS = 0V), is the bulk threshold parameter, and ϕ is the strong inversion surface potential of the MOSFET.

Figure 3.4 depicted the cross-section of a CMOS device using this technique which also includes the parasitic vertical BJTs. This technique is further discussed in next section

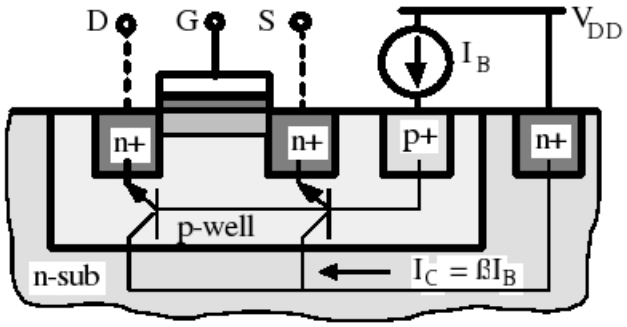

Figure 2.4: Cross-section of forward bias NMOS transistor (Taken from [20]).

2.5 Bulk-Driven MOSFETs

The bulk-driven MOSFET concept was proposed by A. Guzinski, et. al in 1987, as active components in an OTA differential input stage. The bulk driven differential pairs results in improved linearity and smaller trance-conductance. In 1998 a 1V op-amp was designed by P. E. Allen et al using the depletion characteristics of the bulk-driven MOSFET in order to achieve the low voltage requirements.[21]

Bulk-driven is the most significant solution to the threshold limitation in the MOS transistors. A CMOS cross section diagram illustrating this technique is shown in the figure 2.5.

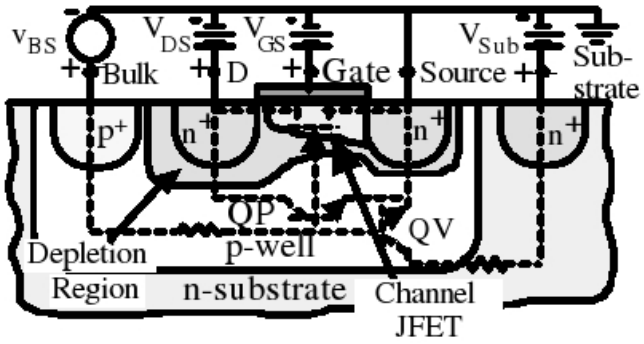

Figure 2.5: Cross-section of bulk-driven MOSFET [21].

Generally, the bulk terminal of the MOSFET is tied to the source when using MOSFET as part of an amplifier and the signal is fed in the gate. In bulk-driven MOSFET, the gate

is tied to a bias voltage that is sufficient to turn it on while the signal is fed into the bulk terminal of the MOSFET.

The current flowing in the channel is modulated by the reverse bias voltage that is applied on the bulk-channel junction. Resultantly a junction field-effect transistor is formed with the bulk as the signal input. Consequently, the bulk driven configuration has a high-input impedance depletion device that requires no DC bulk-source voltage for current flow [21].

2.6 Limitations of circuits in strong-inversion working with low-voltage power supply

All the described low voltage techniques show good performance working in strong inversion region. Among all The techniques composite transistor has, the better performance again short channel modulation, while having low V_{DS}(composite), being a good candidate for low-voltage applications. However, to keep the feedback transistors in saturation larger V_{DS}(sat) is required. The lateral BJT could be a powerful device that reduces the amount of 1/f noise, while having high gain but, using higher gate voltages to turn it on is inevitable. The forward biased bulk is the dominant technique to reduce the threshold voltage (V_T) of the transistor allowing lower $V_{DS(sat)}$. Unfortunately, the V_{BS} activate a parasitic transistor producing undesired currents. The last technique discussed is the bulk-driven technique uses the MOSFET's bulk as input terminal avowing in some degree the threshold limitation. Though, to keep the transistors ON, the values of the V_{GS} must be at least the V_{TH} of the transistor.

All the presented techniques excluding the composite transistor, could work in both strong inversion and sub-threshold region. However, operating at low power supply voltages in strong-inversion brings some important constraints. The primary limitation is the threshold voltage. In CMOS technology, minimum power supply requirement is given by: $V_{DD}+V_{SS}>V_{tN}+V_{tP}$ only in this condition the circuit works in strong inversion [20].

The other limitation is related to the decreased channel length of today and future submicron CMOS technologies. As discussed earlier the supply voltage is limited by the

threshold voltages of MOSFETs but the channel length keeps on decreasing so the resultant field across the channel mounts up. This phenomenon impacts in much larger channel length modulation effect. This results in poor signal gain because the small signal output resistance of the MOSFET has decreased [20].

The design of the low voltage analog circuits has become more challenging due to the lack of good analog models for deep submicron technologies and for low voltage operation. This limitation results in the use of longer channel lengths than necessary in order to have more reliable models. Subsequently, the full performance of submicron technologies is not utilized and more and more parasitic will be there [20].

Due to constant reduction in the device size such techniques are required that could operate supplies voltages as low as 0.5V. Therefore, most of the techniques presented here are not suitable to work in strong inversion region, as they require at least a supply voltage equal to the sum of the threshold voltages of the devices, in order to work properly. These limitations cause the obligation to work at sub-threshold region, allowing the reduction of the supply voltage.

In conclusion, circuits working in the sub-threshold region allow us to operate on reduced power supply voltage, while some of the presented techniques possibly will be used to improve the performance of the circuits.

Figure 1.3: CMOS inverter under (a) body-source short and (b) forward-body bias conditions. The $V_{BS,N}$ is the forward body-bias across the n-MOSFET and $V_{SB,P}$ is the forward body-bias across the p-MOSFET.

2.7 Voltage mode versus Current mode: A critical comparison

In any electrical network the information processed by lumped elements can be represented by either the branch current or nodal voltages. The latter are referred to as voltage-mode circuits whereas the former are known as current-mode circuits. To characterize complete behavior of any network both of the quantities are essential. However, Voltage-mode circuits are explored way too much and received a broader attention as compared with their current mode counterparts. Despite the fact that the

concept of ideal current mode circuits, similar to that of ideal volt age-mode circuits, emerged approximately 40 years ago. This is reflected by countless texts on voltage mode circuits over a handful monographs on current-mode circuits. The reasons for such admiration and acceptance that voltage-mode circuits have been enjoying can be summarized as follows [22]:

(i) In any electrical network Measurement of the nodal voltage is far more convenient than the measurement of the branch current of the networks. Nodal voltage can simply be measured using voltmeters without modifying the topology and altering the operation of the networks. On the contrary, the measurement of the branch current often needs a change of the configuration of the networks or supplementary circuitry,

(ii) The inherent property of MOS devices having infinite input impedance makes these transistor an ideal choice for the realization of voltage-mode circuits, especially while designing cascade configurations, such as multi-stage amplifiers,

(iii) The circuit design techniques, such as cascode and regulated cascodes make it easy to obtain a high voltage gain of voltage-mode circuits.

(iv) In past low-voltage design was not of a critical concern because high voltage supply voltages are available,

(v) High supply voltage makes the switching noise switching noise issue of least concern,

(vi) Low speed requirements allow slow charging and discharging of nodal capacitors.

In past few years an aggressive reduction in the supply voltage of CMOS analog circuits has been observed, while there is only a moderate reduction in the device threshold voltage. The performance of the CMOS voltage-mode circuits has been greatly affected due to this diverse reduction, typically reflected by a decreased dynamic range, an enhanced propagation delay, and poor noise margins. The current mode circuits are advantageous over voltage mode circuits even after aggressive reduction of supply voltage. This is because the performance of current-mode circuits, however, is less severely affected as compared to voltage-mode circuits. The reason behind is the different

design methodologies are used in voltage and current mode circuits, the design emphasis of current-mode circuits is on branch currents rather than nodal voltages. The CMOS current-mode circuits are useful in dealing with the combined difficulties arising from the reduction of the supply voltage and the increase in the operation speed. The different design focuses of both the topologies are arising from the intrinsic characteristics of branch currents and nodal voltages, result in distinct design methodologies. The internal nodes of a current mode circuits have inherent characteristics like low impedance and low voltage swings, which make the supply voltage reduction possible without affecting the performance, unlike voltage mode circuits. To reduce the power consumption of a device the dc operating current should be low along with the supply voltage. The voltage noise is inversely proportional to dc operating current whereas the current noise is proportional to dc operating current, with this fact it is impossible to design low noise devices under low power consumption. While in current mode circuits both the low power and low noise performance can be obtained.

CHAPTER 3

FORWARD BODY-BIAS TECHNIQUE

Transistors are treated as three terminal devices traditionally. While designing circuits the source and bulk terminal are shorted. It implies that the MOSFET operates as a zero bulk-biased threshold device. On the other hand, MOSFET can be used as a four terminal device forward or reverse bias can be applied between the bulk-source junctions of a MOSFET. As per the relation given in previous section under the reverse body-bias, the MOSFET threshold voltage is increased. Under the forward body-bias, the MOSFET threshold voltage is decreased. The detailed analysis of threshold voltage is discussed further. Figure 3.1 (a) depicts a standard CMOS inverter with zero body bias transistors. Figure 3.1 (b) depicts a CMOS inverter where MOS is used as a four terminal device under forward body-bias conditions.

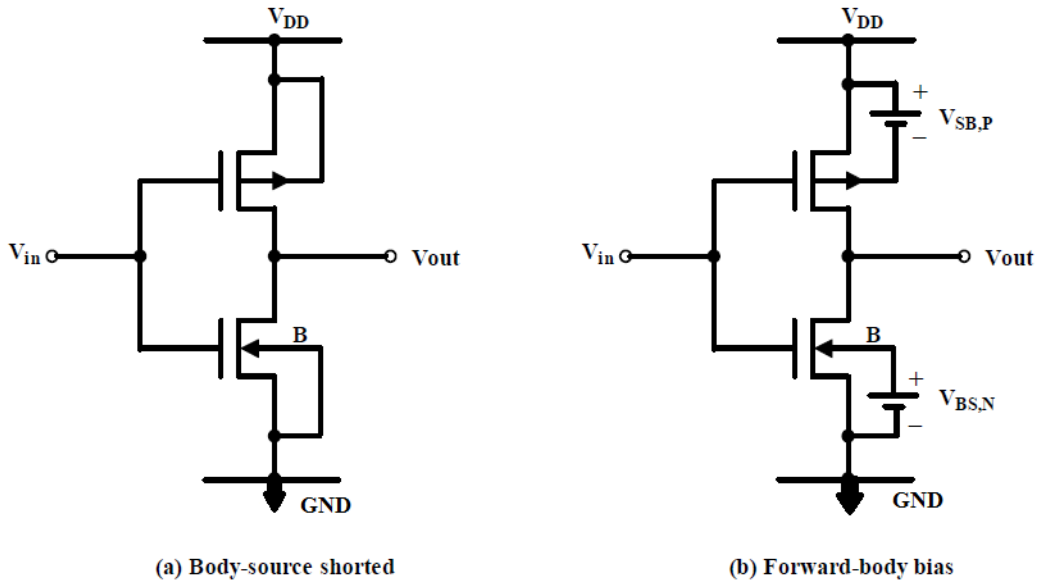

Figure 3.1: CMOS inverter under (a) body-source short and (b) forward-body bias conditions. The $V_{BS,N}$ is the forward body-bias across the n-MOSFET and $V_{SB,P}$ is the forward body-bias across the p-MOSFET.

In the design methodologies for ultra-low power, supply voltage scaling is a straight forward technique. Scaling down the supply voltage becomes more effective because of

the fact that the power consumption has square relation with the supply voltage. However, operating the circuit with low supply voltage, results in low voltage drop across the gate and the source of a MOS transistor. Subsequently, low threshold MOSFETs are desired for operation at the low supply voltage. With the utilization of circuit design techniques and device models low threshold transistors can be obtained in current CMOS technologies. Lengthen the device decreases the threshold voltage considerably while forward body bias is a circuit design techniques that lowers device threshold values. In this chapter, using both of the techniques initially a low power and low voltage operational amplifier is designed.

3.1 Threshold Voltage of the MOSFET

Threshold voltage modeling is elaborated in [10, 23]. The basic stages are presented in this section for completeness. Figure 3.2 depicts a long-channel enhancement mode n-MOSFET where bulk, source and drain terminals are connected to common reference termed as ground. A voltage, V_{GS} is applied to the gate and initially it is zero. As the gate voltage is increased to a positive magnitude from a zero value a depletion region is formed followed by weak inversion region close to the S_i-S_iO_2 interface. With further increment in gate voltage, a condition of strong inversion occurs where a p-type silicon is inverted to an n-type silicon. The certain value of the gate source voltage at which this condition occurs is called the threshold voltage, V_T.

There are three voltage components upon which threshold voltage, V_T of a MOSFET depends. These voltage components are the gate to bulk work function difference (ϕGC), $-Q_{OX}/C_{OX}$ because of fixed oxide charge present at the Si-SiO2 interface and in the oxide, and a gate voltage ($-2\,\phi_F - Q_B/C_{OX}$) to alter the surface potential and to offset the Q_B that is the induced depletion region charge ϕF is Fermi energy and C_{OX} is the gate oxide capacitance per unit area.

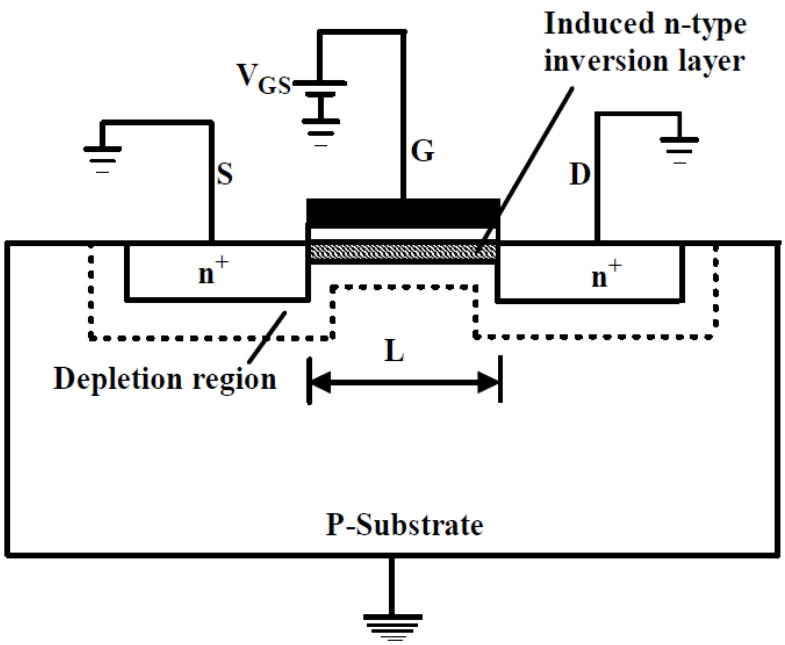

Figure 3.2: The cross-section of an n-MOS with positive gate voltage applied showing the depletion region and the inversion layer [10]. G is gate, D is drain and S is source.

Mathematically, V_T can be expressed as follows:

$$V_T = \phi_{GC} - \frac{Q_{ox}}{C_{ox}} + (-2\phi_F - \frac{Q_B}{C_{ox}}) \quad (3.1)$$

The first part $\emptyset_{GC} - \frac{Q_{ox}}{C_{ox}}$ represents required voltage to attain flat-band (FB) condition. The second part $(-2\phi_F - \frac{Q_B}{C_{ox}})$ represents voltage required to bend the bands in Si through a potential of $2\phi_F$.

The voltage that is required to attain the flat band condition is given by:

$$V_{FB} = \phi_{GC} - \frac{Q_{ox}}{C_{ox}} \quad (3.2)$$

For n-MOSFET Q_B is given by:

$$Q_B = qN_AX_d = \sqrt{qN_A\varepsilon_{si}|\phi_s - \phi_F|} \quad for\ |\phi_s - \phi_F| \geq 0 \quad (3.3)$$

In this equation N_A represents the substrate doping density; X_d is the thickness of the depletion region and ε_{si} represents the permittivity of silicon. The electrostatic surface potential of silicon with respect to Silicon substrate is ϕ_s. In strong inversion region when V_{SB}=0 (i.e. no body bias is applied) the depletion region charge Q_{BO} is given by

$$Q_B = \sqrt{-2qN_A\varepsilon_{si}|-2\phi_F|}. \quad (3.4)$$

While in the presence of body bias when $V_{SB} \neq 0$ the required surface potential to produce strong inversion region is modified to $|-2\phi_F| + V_{SB}$.

The depletion region charge in such condition will be:

$$Q_B = \sqrt{-2qN_A\varepsilon_{si}|-2\phi_F + V_{SB}|}. \quad (3.5)$$

For n-MOS the threshold voltage in this condition will be:

$$V_T = \phi_{GC} - 2\phi_F - \frac{Q_{BO}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} - \frac{Q_B - Q_{BO}}{C_{ox}}, \text{ or} \quad (3.6)$$

$$V_T = V_{TO} \pm \gamma(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}). \quad (3.7)$$

Where V_{TO} is the zero bias threshold voltage with bulk to source potential deference is zero. The γ parameter is known as body effect coefficient or body factor. .

Generally, $V_{SB} \leq 0$, results in $V_T \geq V_{TO}$ While with the substrate bias, $V_{SB} \geq 0$, V_T is less than V_{TO}. Thus, a MOSFET can be designed to operate at a reduced threshold voltage by forward biasing the bulk source junction.

The separate equations for the n-MOS and p-MOS are given bellow:

For n-MOSFET

$$V_{TN} = V_{TNO} + \gamma(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}). \quad (3.8)$$

Where the body factor is given by, $\gamma = \frac{1}{C_{ox}}\sqrt{2q\varepsilon_{si}N_A}$.

N_A is the doping density in p-substrate.

For the p-MOSFET

$$V_{TP} = V_{TPO} - \gamma(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}). \quad (3.9)$$

Where the body factor is given by, $\gamma = \frac{1}{C_{ox}}\sqrt{2q\varepsilon_{si}N_D}$.

N_D is the doping density in n-substrate.

3.2 Forward Body-Bias

With the upsurge in the use of battery-powered applications, design of low power circuit is enormously needed for portable devices like cellular phones, hand-held computers,

healthcare equipment and personal assistant devices. As discussed earlier power supply reduction is the straightforward technique to achieve low power consumption. Forward body-bias technique is very beneficial in the low voltage CMOS circuits design. In reference [24], a low voltage inverter is designed using this technique. Using forward body bias MOSFETs a 0.8 V CMOS amplifier is designed and reported in [25].

Now the question arises is there any limit on the forward body bias voltage that reduces the threshold voltage of MOS transistors? The amount of V_{SB}, is limited by the phenomenon of CMOS latchup. Since large V_{SB} may trigger CMOS latchup. In [26] it is reported that the latchup action will not be triggered for the value of $V_{SB} \leq 0.4$volts. A brief investigation on CMOS latchup is presented here. Figure 3.3 depicts the vertical cross section of an n-well CMOS with parasitic *npn* and *pnp* bipolar junction transistors (BJTs). The corresponding equivalent circuit including both of the parasitic *npn* and *pnp* BJTs is shown in Figure 3.4 where source-bulk junctions are forward-biased and V_{DD} is 0.8 V. Figure 3.5 depicts the latchup current versus the forward body-bias voltage. It is apparent from Fig. 3.4 that the latchup action does not take place for the $V_{SB} \leq 0.4$V [25].

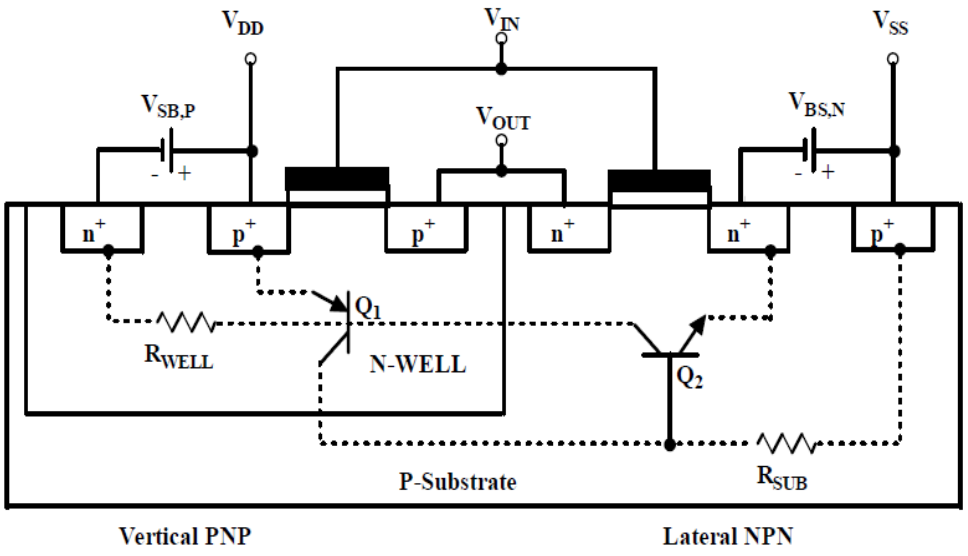

Figure 3.3: Vertical cross-section of an n-well CMOS showing parasitic bipolar junction transistors.[25]

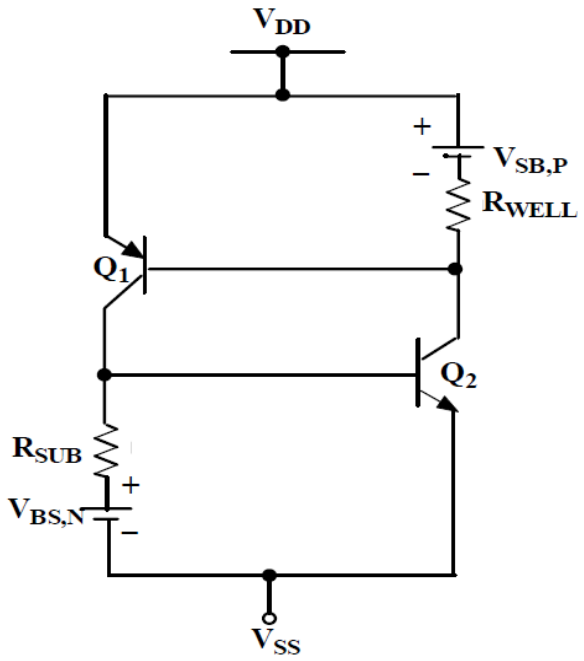

Figure 3.4: Extracted equivalent circuit of Figure 3.2.

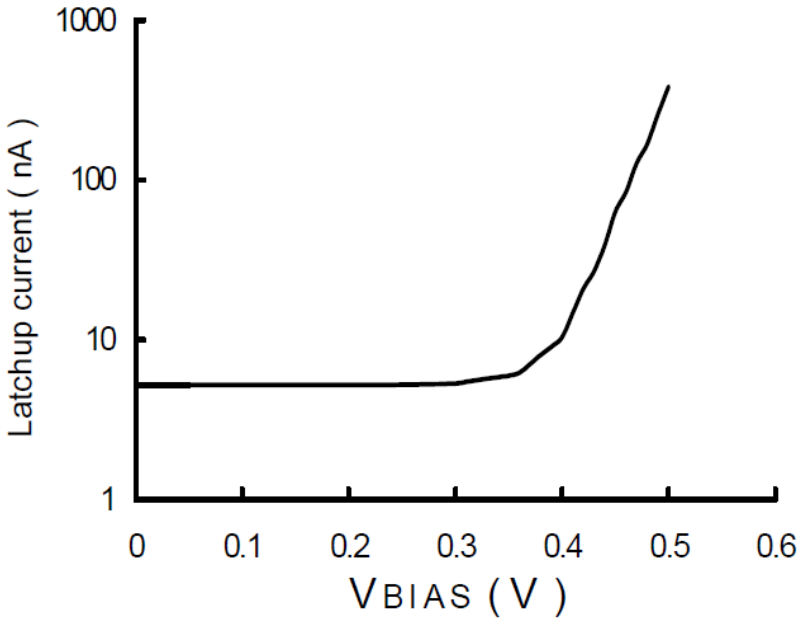

Figure 3.5: Latchup current under forward biased source-substrate condition for V_{DD}=0.8V [26].

Figure 3.6 depicts the current trough bulk-source junction in a typical n-MOS while varying forward body bias is applied. It is clear that the current in a forward biased bulk-source n+-p junction is negligible till the junction is biased below 0.4 V.

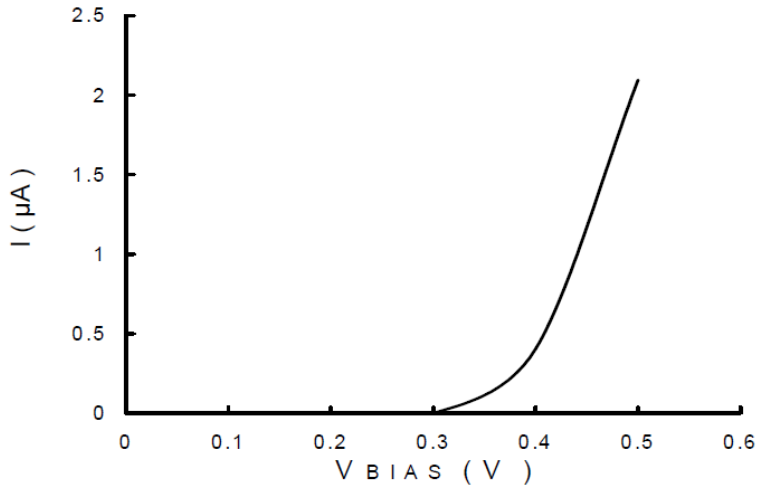

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Figure 3.6: Current through forward biased source-substrate junction in an n-MOSFET[25].

Figure 3.7 depicts how the threshold voltage is reduced for various values of bulk-source forward potential for a typical n- MOSFETs in a standard 180nm n-well CMOS process.

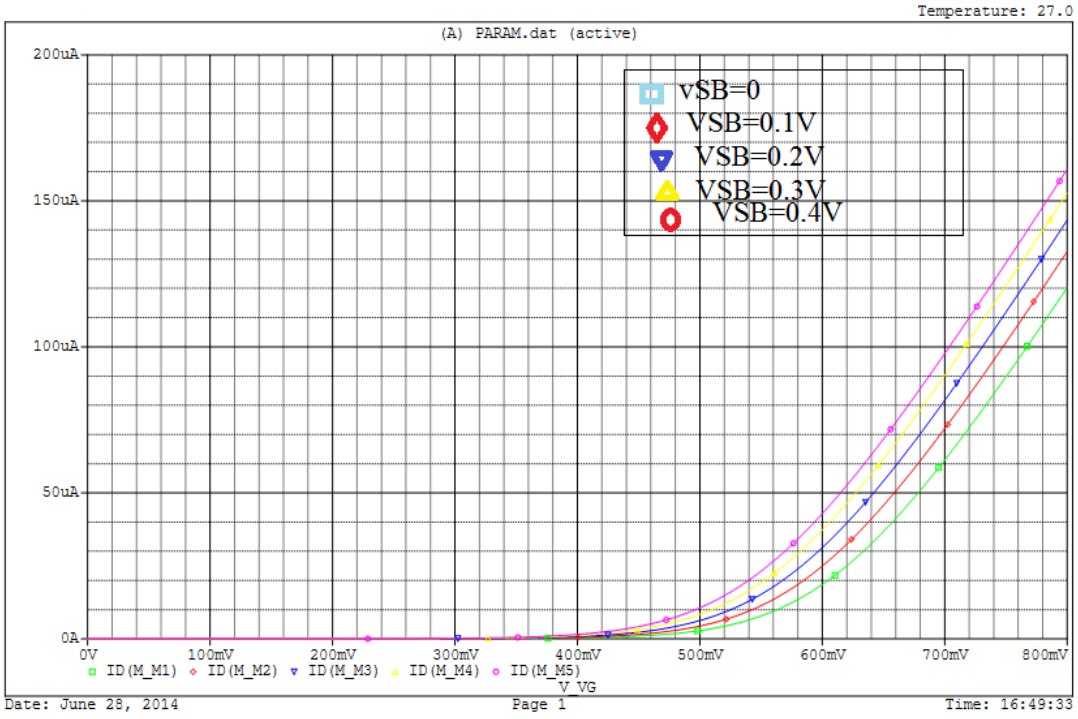

Figure 3.7: variation of drain current and threshold voltages w.r.t. bulk-source potential.

3.3 Noise of Forward Body-Bias MOSFETS

Noise is a major concern while designing analog circuits for low voltage applications. Basically there are three types of noise in MOS transistors, Flicker noise, thermal noise and shot noise are associated with devices. Flicker noise also known as the 1/f noise. This noise is caused by trapped charge in Si-SiO_2 interface that is due to fluctuation in processing parameters and dominates at lower frequencies in a MOSFET. It is expressed as follows: [27]

$$\frac{\overline{v_{flicker}^2}}{\Delta f} = \alpha \frac{I_D}{g_m^2 f}. \qquad (3.10)$$

Where $\frac{\overline{v_{flicker}^2}}{\Delta f}$ is spectral density of the flicker noise voltage. α is device specific constant. I_D, f and g_m are drain current, frequency of operation and trans-conductance of device respectively.

Other type of Noise is thermal noise that is caused by random motion of the electrons due to temperature variation in the channel of the MOSFET. It is given by [27]

$$\frac{\overline{v_{thermal}^2}}{\triangle f} = \frac{8}{3} kT \frac{1}{g_m}. \quad (3.11)$$

Where $\frac{\overline{v_{thermal}^2}}{\triangle f}$ is the spectral density of thermal noise voltage that is related to the V_{GS} of the MOSFET that is being operated in the saturation region. $k, T \; and \; g_m$ are the Boltzman's constant, absolute temperature and transconductance.

Shot noise is produced due to the transport phenomenon of charge carriers across the p-n junction. As each device has different energy and velocity transport is a random phenomenon. The shot noise is given by the following relation [27]:

$$\frac{\overline{\iota_{shot}^2}}{\triangle f} = 2qI_{DC}. \quad (3.12)$$

Where $\frac{\overline{\iota_{shot}^2}}{\triangle f}$ is the shot noise spectral density that is proportional to DC current I_{DC} in a p-n junction.

Noise analysis of proposed active devise is will be discussed is subsequent section of this report.

CHAPTER 4

DESIGN OF FORWARD BODY-BIASED CURRENT-MODE AMPLIFIER

Amplifiers are the basic and widely used building block in analog and mixed- signal system design. In some of the previous works reported on low-voltage analog design wherein, bulk driven and current driven have been used [21, 28, 29]. In the previous one, the input is directly fed to the bulk and not the gate of the MOSFET. In the current driven topology, the source-bulk junction is forward biased by a bias current through another MOSFET connected to the bulk. A 0.8 V low power CMOS amplifier design using forward body-biased MOSFETs is reported in [25]. Several current mode amplifiers are also reported in [30], [31] that uses either pseudo resistors or other means to have low frequency path that increase power dissipation along with increased noise.

In this chapter a systematic approach to design a forward body-biased current-mode amplifier is presented. Starting with the design of a low voltage forward body bias current mirror, we are led to a FBB op-amp design and then it will be transformed to a current mode amplifier (reported in [32]).

4.1 A Two-Stage CMOS Amplifier Topology

Figure 4.1 depicts the circuit diagram of a two-stage CMOS operational-amplifier. The first stage consists of a p-MOS input differential pair, M_1-M_2 with an n-channel current mirror active load, M_3-M_4. Transistors, M_5 and M_6 provide the bias current to M_7 that biases the complete first stage. The second stage consists of an n-channel common source amplifier that level shifts the output voltage to enhance the gain. M_9 is the n-MOS with a p-channel current-source load, M_8. Second stage is also biased by the current provided through M_5 and M_6 Transistors, and C_C is compensation (pole splitting) capacitor.

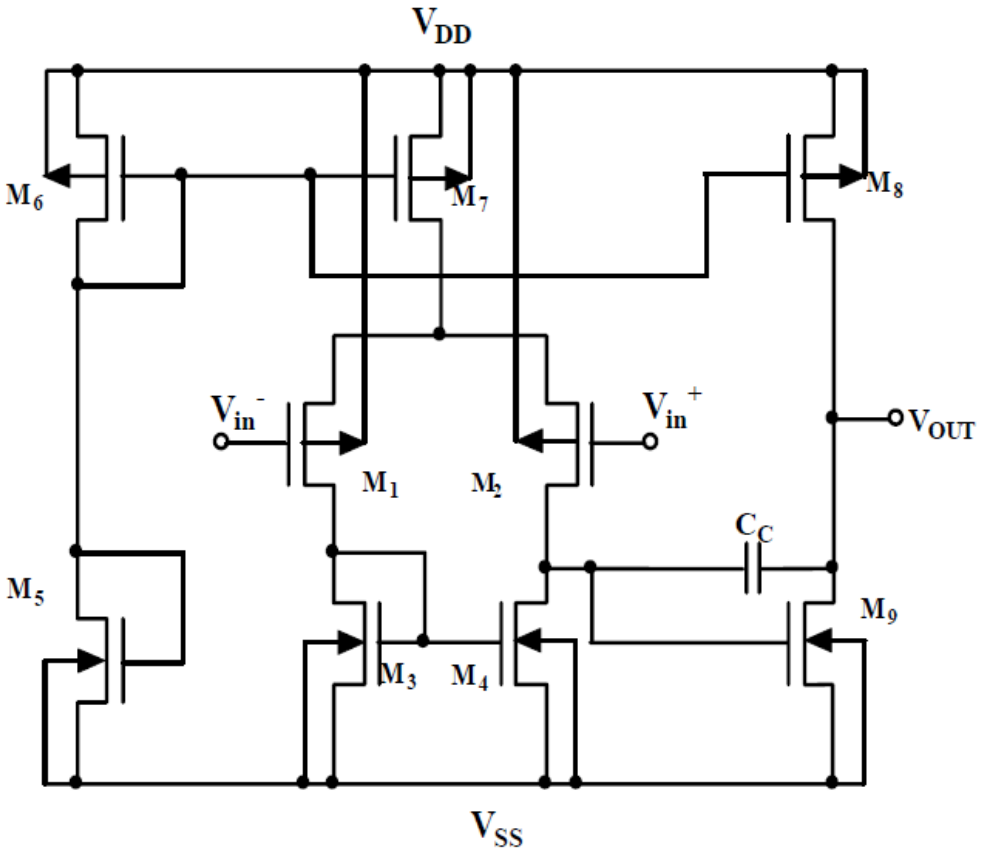

Figure 4.1: A two-stage CMOS operational amplifier.

4.2 Low Voltage Current Mirror Design

Current mirrors are vital building blocks in design of analog integrated circuits. Current mirrors are used as an active load to enhance gain in op-amp as well as the serve as biasing circuits to also provide bias currents. Figure 4.2 depicts the basic CMOS current mirror circuit.

For the p-MOS current mirror, we can write:

$$\frac{I_{OUT}}{I_{IN}} = \frac{(W_2/L_2)}{(W_1/L_1)} \qquad (4.1)$$

Where W_x and L_x is the channel width and length of transistor x respectively. In Fig. 4.2, to turn on the n-MOS transistor M_1 it needs an input voltage greater than the threshold voltage, V_{TN}. The current mirror circuit of Fig. 4.2 is modified to a level shift current mirror as shown in Fig. 4.3, where the bias voltage V_{DS1} can be obtained through following circuit design equations:

$$V_{DS1} = V_{GS1} - V_{SG3} \qquad (4.2)$$

The Eq. (4.2) defines that the bias voltage (V_{DS1}) to transistor M_1 is changed by the gate-source voltage of transistor M_3 i.e.$V_{SG3.}$ In this circuit, M_3 is operated in the sub-threshold region ($V_{SG3} < |V_{T,P}|$).

Figure 4.4 depicts a new level-shift current mirror design which combines the advantages of the level shift circuit for low voltage operation with the reduction in the threshold voltage of a forward body-biased MOSFET. It also includes output impedance enhanced architecture [33], which increases the output impedance of the current mirror, thereby enhancing the gain of the amplifier. This low voltage current mirror circuit of Fig. 4.4 operates as follows. $I_{D1} = I_{D2,}$ since $V_{GS1} = V_{GS2}$ where I_{Dx} is drain current of transistor x. The transistor M_9 provides the bias current to the input transistor M_1.

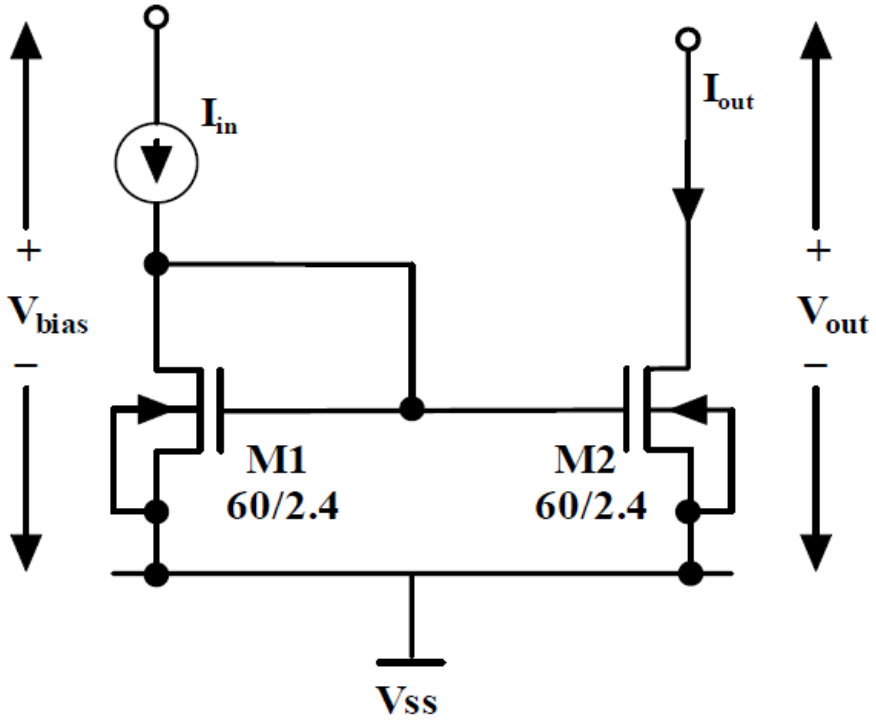

Figure 4.2: An n-MOS current mirror circuit in CMOS. The fraction indicate W/L ratio of the corresponding transistors.

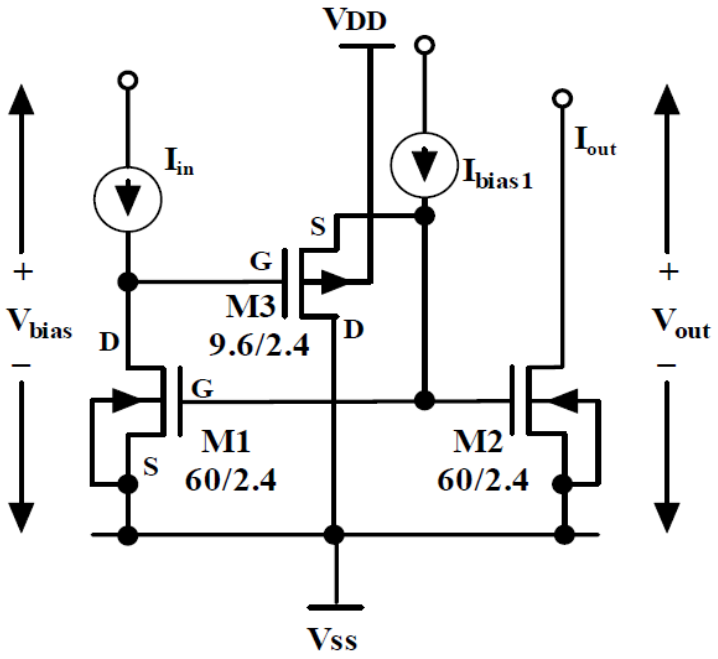

Figure 4.3: A CMOS level shift current mirror CMOS circuit. The fraction indicate W/L ratio of the corresponding transistors. [25]

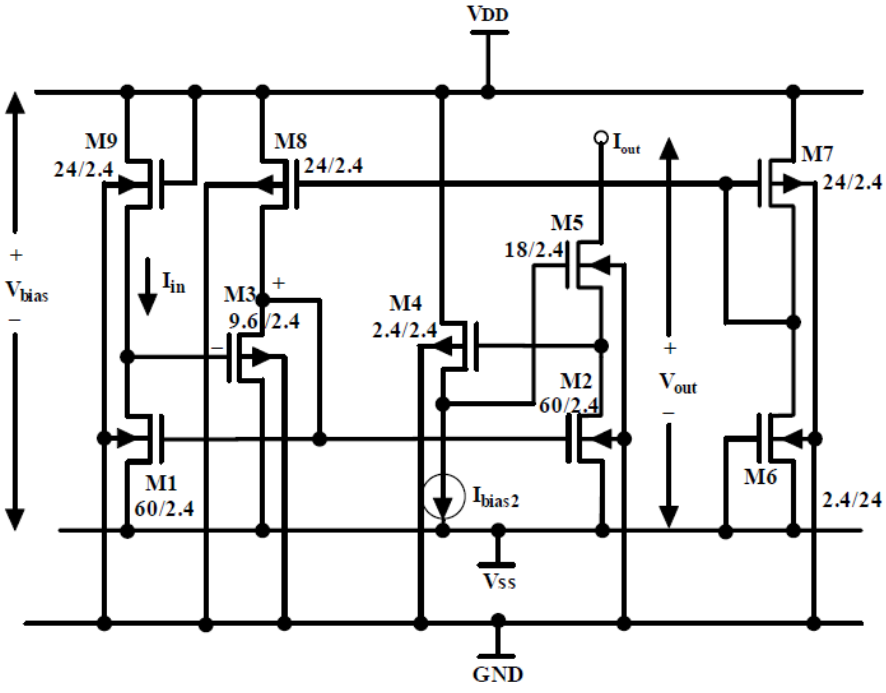

Figure 4.4: A new level shift current mirror CMOS circuit. The fraction indicate W/L ratio of the corresponding transistors. [34]

The transistor M_3 is a level shift transistor which provides a voltage shift, V_{SG3}. It sets

V_{DS1} equal to $|V_{GS1} - V_{SG3}|$ as described in Eq. 4.2. Thus, V_{DS1} is reduced from amount of V_{GS1} of the circuit of Fig. 4.3 it should be noted M_3 is operated in sub-threshold region i.e $V_{SG3} < |V_{TP}|$. The level shift transistor, M_3 is biased by the combination of transistors, M_6, M_7 and M_8**.** In the output branch the transistor M_5 which is being operated in common base configuration forms a cascode configuration with the common source transistor M_2, which enhances the output impedance of the current source. The transistor M_4 provides bias voltage to transistor M_5.

4.3 Low Voltage Operational Amplifier Design

Figure 4.5 depicts the circuit diagram of a two-stage CMOS operational amplifier for operation at 0.8 V to ground supply. The operation and circuit diagram of low voltage op-amp are described here. The input bias current generating stage provides bias current for both the stages of amplifier. In the input bias current generating block, M_{11} is biased through current provided by the transistor, M_{11}. M_{14} is the level shift transistor that is biased by the transistor, M_{17} through M_{15}-M_{16} current mirror.

In the first stage block, M_{12} is the corresponding transistor that mirrors the input current coming from the biasing stage. M_1 and M_2 are active loads for the differential input pair transistors, M_3 and M_4 the first stage. M_5 is the level shift transistor for M_1. M_5 biases itself through the combination of M_6, M_7 and M_8.

In the second stage block, M_9 is the corresponding transistor to mirror the input current. M_{10} is the input transistor of the common source second stage that further increases gain.. M_{20} is the cascode transistor to increase the output impedance of the second stage. M_{19} generates bias voltage for M_{20}. M_{18} generates bias current for M_{19}. C_C is for splitting poles of the two stage amplifier and improves its phase margin. All the n-MOSFETs and p-MOSFETs are forward body biased i.e. the bulk terminals of all the p-MOS transistors are tied to ground and of n-MOSFETS to bias voltage of 0.4V. So that both of n- and p-MOSFETs in the amplifier are forward body-biased at 0.4 V.

Table 4.1 summarizes the aspect ratio of all the transistors used in the circuit diagram,

depicted in figure: 4.5.

Trans	**W/L (µm/µm)**	**Trans**	**W/L (µm/µm)**	**Tran**	**W/L (µm/µm)**
M1	90/9	M2	90/9	M3	120/4.5
M4	120/4.5	M5	7.2/4.5	M6	36/4.5
M7	72/4.5	M8	4.5/4.5	M9	144/4.5
M10	36/9	M11	45/4.5	M12	45/4.5
M13	18/4.5	M14	14.4/4.5	M15	13.5/4.5
M16	13.5/4.5	M17	9/4.5	M18	9/4.5
M19	9/4.5	M20	90/4.5	C_C	10 Pf

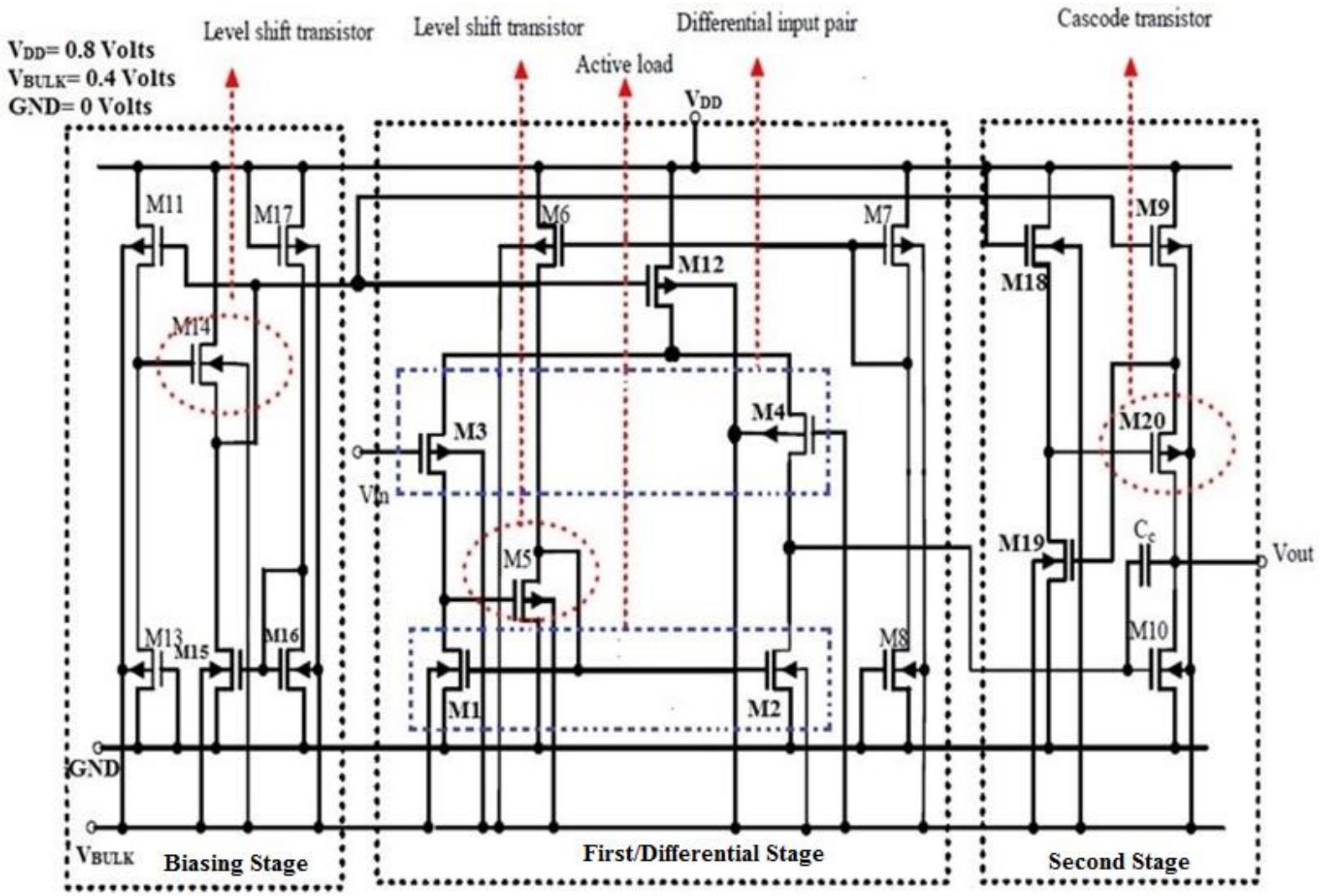

Figure 4.5: Circuit diagram of low voltage forward body bias CMOS Operationa Amplifier.

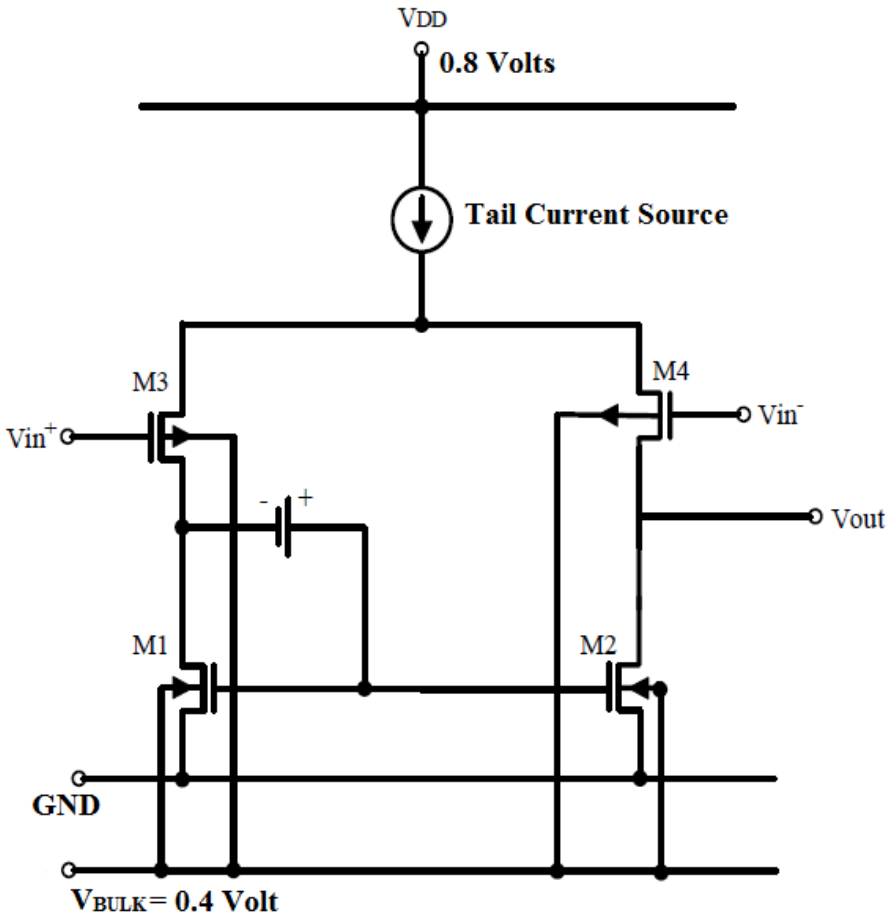

Figure 4.6: Simplified first stage circuit of amplifier circuit shown in Fig. 4.5.

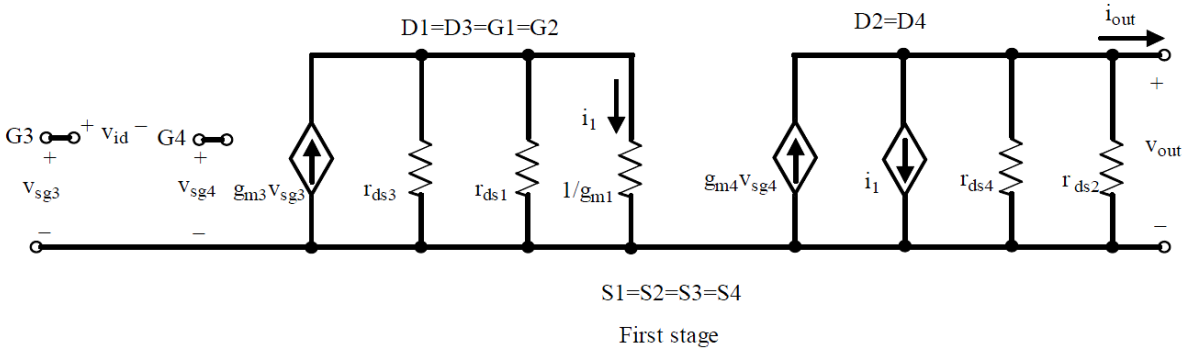

Figure 4.7: Small signal equivalent circuit for the simplified first stage circuit of Fig. 4.6. v_{id} is differential input voltage, i_1 is current through M_1 which is mirrored to M_2. D_X is the drain of transistors and S_X is the source of transistors.

The small signal gain of low voltage op-amp is given by

$$a_v = a_{v1}a_{v2}. \quad (4.3)$$

where a_{v1} and a_{v2} are the gain of the first and second stages, respectively. Figure 4.6 depicts the simplified differential stage of the amplifier circuit whereas Figure 4.7 depicts the small signal equivalent model of the simplified first stage circuits for gain calculation.

Assuming the differential amplifier circuit as an unloaded amplifier, in Fig. 4.7 the output current can be written as:

$$i_{out} = g_{m4}v_{sg4} - i_1 = g_{m4}v_{sg4} - g_{m3}v_{sg3}\frac{g_{m1}r_P}{1+g_{m1}r_P}. \quad (4.4)$$

Where g_X is the transconductance of the transistor M_X, r_p r_{ds3}// r_{ds1}.

For $g_{m1}r_P \gg 1$ equation (4.4) simplifies to

$$i_{out} \approx g_{m4}v_{sg4} - g_{m3}v_{sg3} = g_{m3}v_{id}. \quad (4.5)$$

Where $g_{m3} = g_{m4}$ and $v_{sg4} - v_{sg3} = v_{id}$.

The output voltage will be given by

$$v_{out} = i_{out}r_{out} = v_{id}g_{m3}(r_{ds2}//r_{ds4}). \quad (4.6)$$

Thus the gain of differential stage is given by

$$a_{v1} = g_{m3}(r_{ds4}//r_{ds2}). \quad (4.7)$$

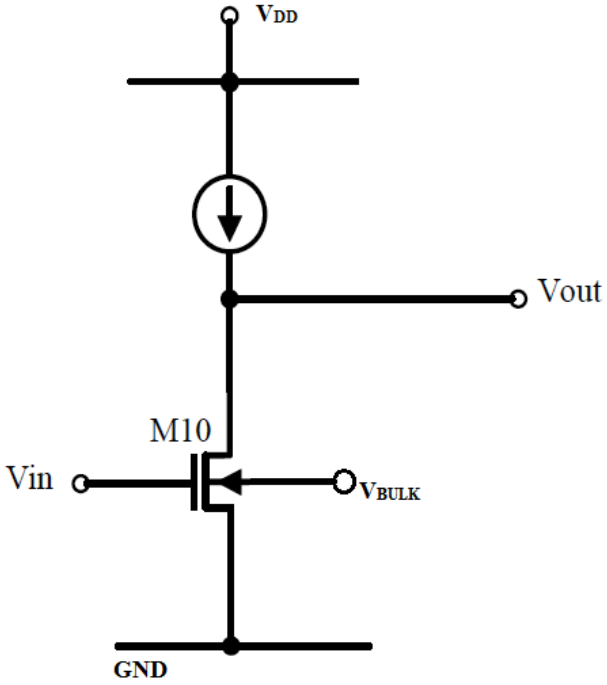

Figure 4.8: Simplified circuit for the second stage of the amplifier circuit shown in Fig.4.5.

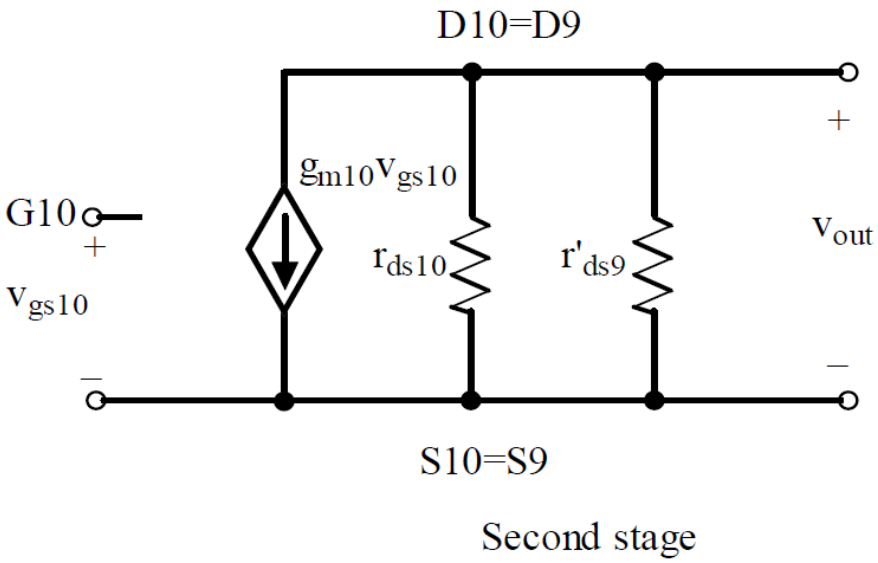

Figure 4.9: Small signal equivalent circuit of the second stage of the amplifier shown in Fig.4.8. D_X is the drain of transistors and S_X is the source of transistors.

Figure 4.8 shows the simplified version of second stage of proposed tow stage low voltage amplifier. Corresponding small signal model is described in the Fig. 4.9. From figure 4.9, we can write

$$g_{m10}v_{gs10} + \frac{v_{out}}{r_{ds10}} + \frac{v_{out}}{r'_{ds9}} = 0. \quad (4.8)$$

Where r'_{ds9} is the equivalent cascade resistance and is given by

$$r'_{ds9} = g_{m23}r_{ds20}r_{ds9}. \quad (4.9)$$

The second stage gain could be given by

$$a_{v2} = \frac{v_{out}}{v_{gs10}} = -g_{m10}(r_{ds10}//r'_{ds9}). \quad (4.10)$$

Putting Eq.(4.9) in Eq. (4.10), we obtain

$$a_{v2} = -g_{m10}\{r_{ds10}//(g_{m23}r_{ds9}r_{ds20})\}. \quad (4.11)$$

4.3.1 Simulated Results:

Frequency response of the proposed forward body biased CMOS op-amp is shown in the figure 4.10. The Bode plot of the proposed amplifier, simulated using P-spice depicts that the open loop gain of the amplifier is 64 dB with a phase margin of 52^0. Figure 4.11 depicts the transient response of the amplifier. This forward body biased op-amp consumes only 55µW of power. That is less than the power consumption of amplifiers reported in [25, 21, 28]. The unity gain frequency of the CMOS op-amp is 10MHz and the 3-dB bandwidth is around 300 KHz these results are apparent from the bode plot depicted in figure 4.10. The other characteristics are summarized in table 4.2. All the parameters are measured from the simulated circuit using P-SPICE for the standard TSMC 0.18µm CMOS Technology. Appendix C describes the several measurement techniques [8] and [35] used in extracting amplifier parameters. All the extracted parameters through spice simulator are compared with some of the low voltage amplifiers reported in [21, 25. & 28]. All of the comparisons are shown in the table 4.2

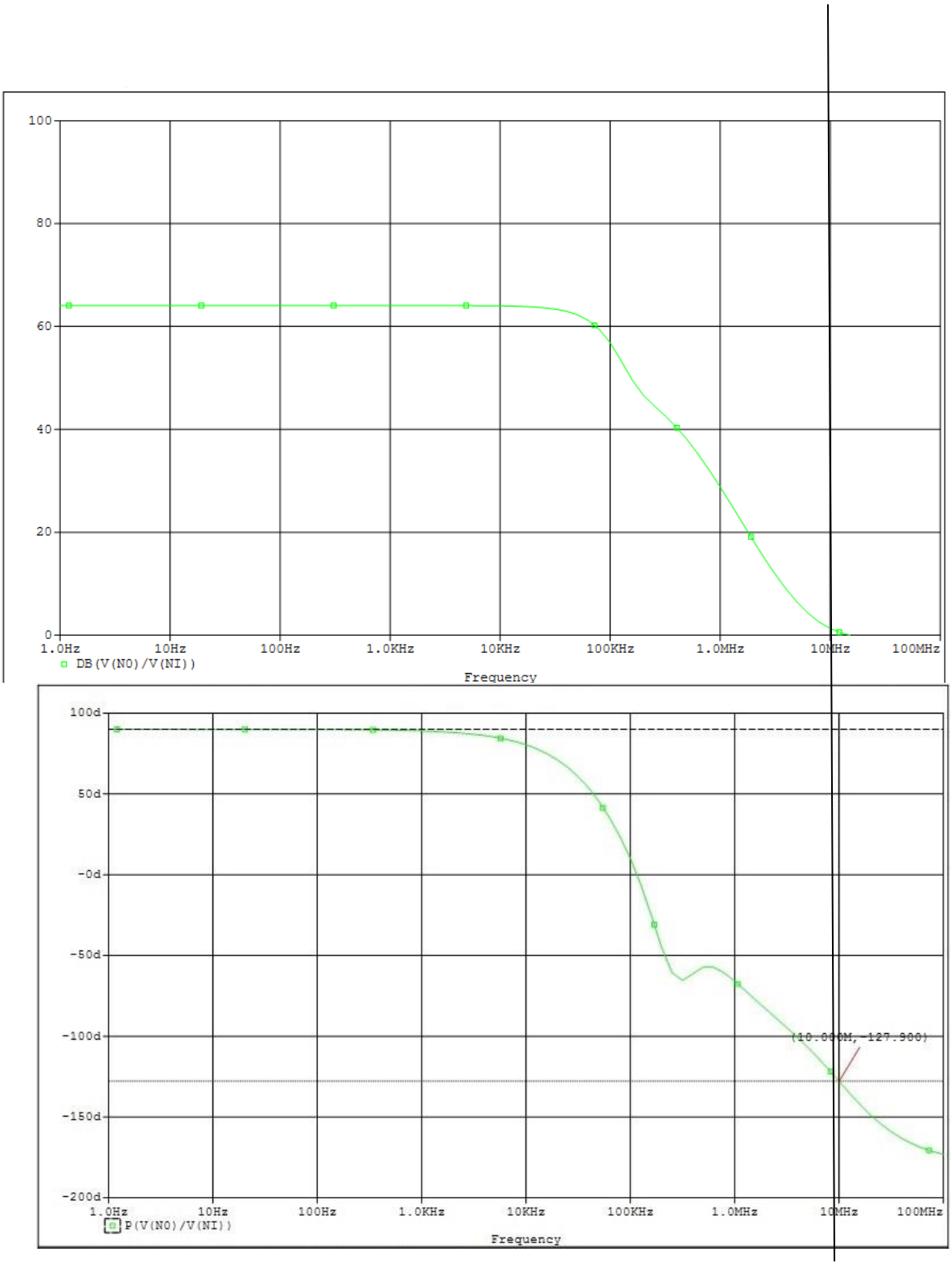

Figure 4.10: Simulated frequency response characteristics of the low power CMOS op-amp circuit. Phase margin is 52^0 (-28^0+180^0).

Parameters	**[21]**	**[28]**	**[25]**	**Current Design**
Supply Voltage	± 0.5 V	0.8 V	± 0.4 V	0.8 V
Open-loop gain	49 dB	46 dB	70 dB	64 dB
3-dB bandwidth	10 kHz	N/A	30 kHz	300 kHz
Phase margin	57^0	54^0	45^0	52^0
Input common mode range (ICMR)	490mV – 500mV	0V – 400 mV	-400 mV – 100 mV	0 V–350 mV
Output Voltage swing	-350 mV- 350 mV	150 mV – 650mV	-350 mV – 350 mV	120 mV – 690 mV
Power Dissipation	287 µW	N/A	60 µW	55 µW
Unity Gain bandwidth	1.3 MHz	0.8 MHz	1 MHz	10 MHz
Power Supply (PSRR)	61 dB @10 kHz	N/A	70 dB @10 kHz	85 dB @10 kHz
Slew rate (SR^+)	0.7 V/µS	0.4 V/µS	0.2 V/µS	0.49 V/µS
Slew rate (SR^-)	1.6 V/µS	-	0.5 V/µS	0.3 V/µS
Common Mode rejection Ratio (CMRR)	N/A	N/A	54 dB @10 kHz	60 dB @10 kHz

Table 4.2. Comparison with a few previous published works.

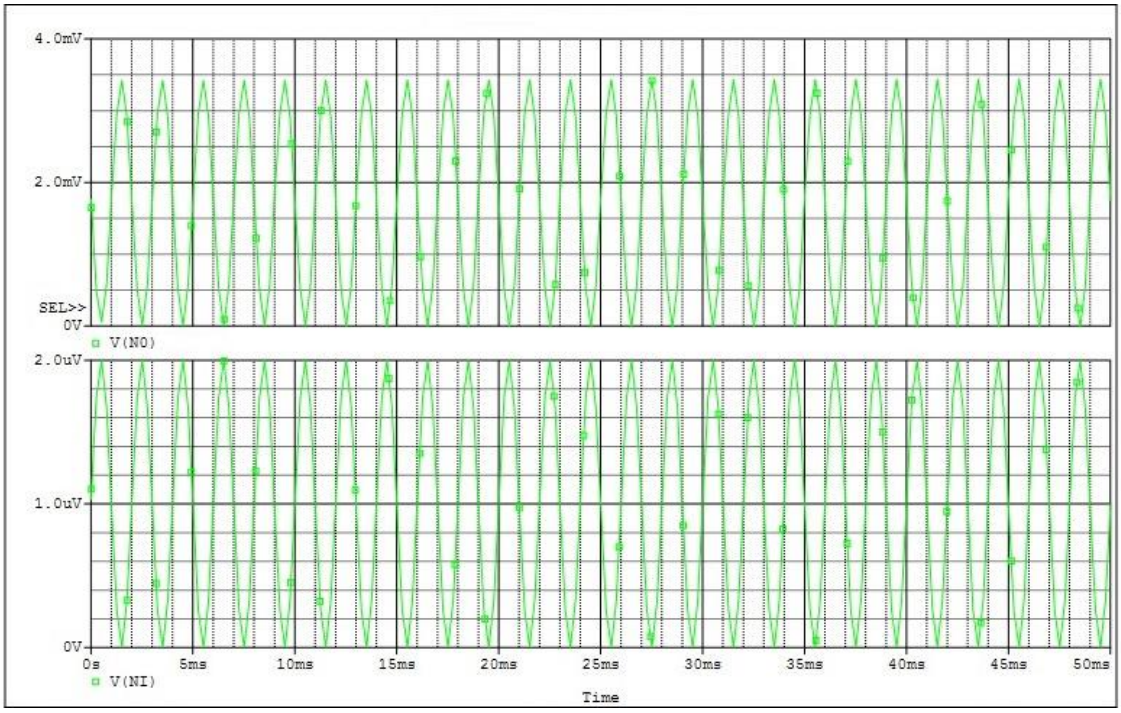

Figure 4.11: Transient Analysis of FBB CMOS op-amp.

4.4 Current Mode Amplifier Design Using FBB Op-Amp

The architecture of the proposed *Forward Body Biased Current Mode Amplifier (FBBCMA)* is shown in Fig. 4.12 which consists of a forward body biased op-amp with an active feedback loop. The current-mode amplifier designed to amplify the in-band current signals. The integrated active feedback loop is operated at a very low frequency, which bypass the dc offset current that is generated from the electrode-tissue interface.

Since the noise of the first stage is the dominate noise source, a current-mode preamplifier with low dc current is used as the first stage to suppress the noise contributed by this stage [32]. The operational amplifier that is incorporated as an active block is a two-stage topology as shown in figure 4.5. In the Structure of FBBCMA the dc voltages of the input node and the node outx are set to Vr =1/2V_{DD}(0.4V) via the negative feedback loop of FBB op-amp. The voltage of out′ is also set to Vr =1/2V_{DD}(0.4V) via the negative feedback loop in the next stage. As a result, the dc drain-source voltages of MN1, MN2, Mp1, and Mp2,are kept at 0 V.

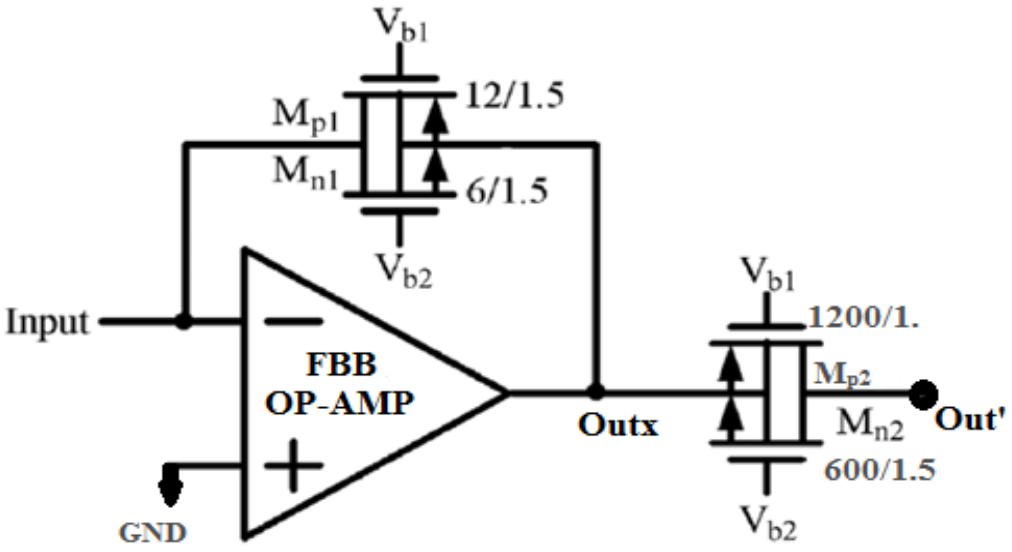

Figure 4.12: Structure of proposed current mode amplifier designed using forward body biased op-amp proposed in figure 4.5.

With Vb1=0.3V and Vb2=0.7V, all the feedback devices are being operated at a very low dc current in the linear sub-threshold region as resistors. Since the channel lengths of all devices are kept the same, the resistance ratio of Mp1 (MN1) to Mp2 (MN2) will be equal to the channel width ratio of Mp1 (MN1) to Mp2 (MN2) which is designed to be 100. With a small-signal input current flowing on Mp1 and Mn1, the small-signal voltage across M_{p1} and M_{n1} is the same as that of M_{p2} and M_{n2}. Thus the current flowing in M_{p2} and M_{n2} is 100 times of current flowing in M_{p1} and M_{n1} and a current gain of 100 can be obtained. The FBBCMA in Fig. 4.12 has low input impedance and distortion. The frequency response of the FBBCMA is shown in figure 4.13.

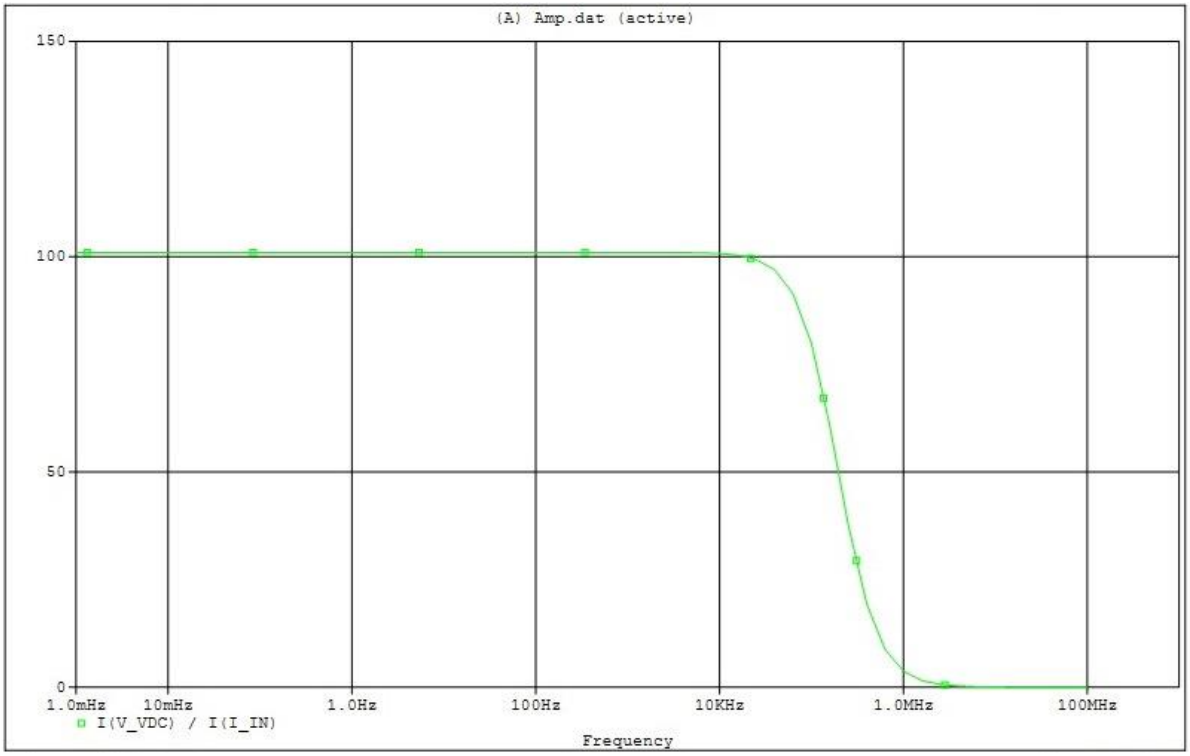

Figure 4.13: Frequency response of proposed FBBCMA with the gain of 100 A/A.

CHAPTER 5

NOISE ANALYSIS OF FBBCMA

Noise is a major concern while designing low power circuits. In designing amplifier for low voltage application the amplitude of noise can become comparable to the signal's amplitude. In Any bio-signal acquisition system the pre-amplifier is the first stage, this stage has the largest gain in complete analog readout front-end. This pre-amp stage is followed by the filters having smaller gains, comparatively. So the noise added by the pre-amplifier stage would be dominant and noise contribution of later stages (that are high pass and low pass filters) can be neglected. Keeping this fact in mind the noise analysis of first stage becomes critical.

In earlier part of this chapter the noise modeling of MOS transistors is presented. Thereafter noise analysis of forward body bias op-amp is described which is followed by the discussion of total noise added by the proposed Forward Body Bias Current Mode Amplifier.

5.1 Thermal noise

Random motion of charge carriers in a conductor causes low voltage fluctuations. These random fluctuations are known as thermal noise that can be measured across the conductor and they are independent of the current flowing into the component. Consequently, the thermal noise spectrum is proportional to the absolute temperature.

$$S_v(f) = 4kTR;\ f \geq 0 \qquad (5.1)$$

Where k is the Boltzman constant, R is the resistor value and T is the absolute temperature. Bellow 100 THz thermal noise can be assumed as white noise.

The thermal noise voltage is given by:

$$V^2_n = 4ktBR. \qquad (5.2)$$

Where B is bandwidth of interest.

5.2 Thermal noise in MOSFETs

The major share of thermal noise introduced by a MOS device is generated by its channel. When a long channel MOSFET is being operated in saturation, the noise can be modelled as a current source between drain and source terminals where its power spectral density (PSD) is:

$$\bar{I}_n^2 = 4kT\gamma g_m. \quad (5.3)$$

Figure 5.1 illustrates the MOSFET noise model for long channel transistors.

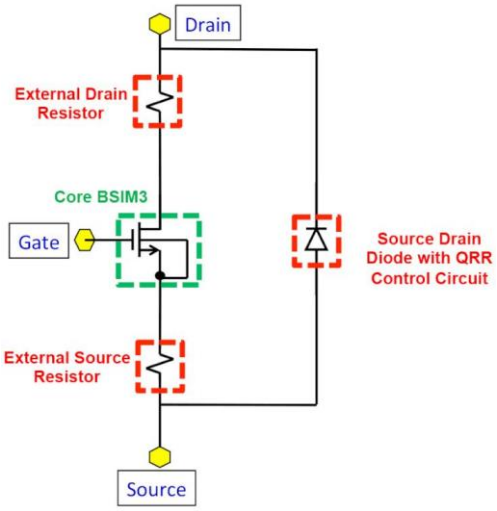

Figure 5.1: Thermal noise circuit model for a MOSFETs operating in saturation.

The γ coefficient for long channel transistors is equal to 2/3[8].

A MOSFET operating in the triode region also has thermal noise. All the terminals are mated of the materials that have a finite resistivity, therefore they induce noise. For a relatively wide transistor only gate resistance remains significant while the source and drain resistances are typically insignificant.

5.3 Shot noise

Shot noise is caused by the random crossing of charges across the potential barrier. So shot noise in diodes is given by:

$$\frac{\overline{i_{shot}^2}}{\Delta f} = 2qI_{DC}. \quad (5.4)$$

Here $\frac{\overline{i_{shot}^2}}{\Delta f}$ is the shot noise spectral density that is proportional to DC current I_{DC} in a p-n junction. As stated that it is caused by the crossing of charges across the potential barrier i.e. p-n junction in our case. The possibility of each carrier crossing the p-n junction is random in nature this results in a large number of random current pulses that composes DC current I_{DC}.

5.4 Flicker noise

The flicker noise is dominant at lower frequencies therefore also known as 1/f noise. When the charge carriers are either trapped or released randomly at the Si-SiO_2 interface and into the gate oxide, flicker noise is generated. MOSFETS are highly susceptible to flicker noise among all of the active semiconductor devices. It is because the current in the MOS devices, is a surface current, and there is a high probability of defects at interface during the manufacturing process.

A voltage source in series with the gate terminal models the flicker noise in MOSFETs and its equation it is given by:

$$\bar{V}_n^2 = \frac{K}{C_{ox}WL}\frac{\Delta f}{f}. \quad (5.5)$$

Where K is a constant of order of $10^{-25}V^2F$.

The power spectral density is inversely proportional to the frequency. The inverse dependency on W·L suggests that in order to diminish the noise in the device its area must be larger [35]. While designing the bio-medical application the effect of flicker noise dominates. The effect of 1/f noise is can be minimized by enlarging the devices. Large device size results in higher parasitic values but that will not affect our application as in our application the frequency of interest is rather low.

To quantify thermal noise with flicker noise, both PSD are plotted (figure 5.2). the corner frequency of flicker noise is the intersection between the thermal noise and flicker noise. In figure 5.2, f_c is computed by:

$$f_c = \frac{K}{C_{ox}WL} g_m \frac{3}{8kt}. \quad (5.6)$$

Generally f_c depends on both transistor size and bias current.

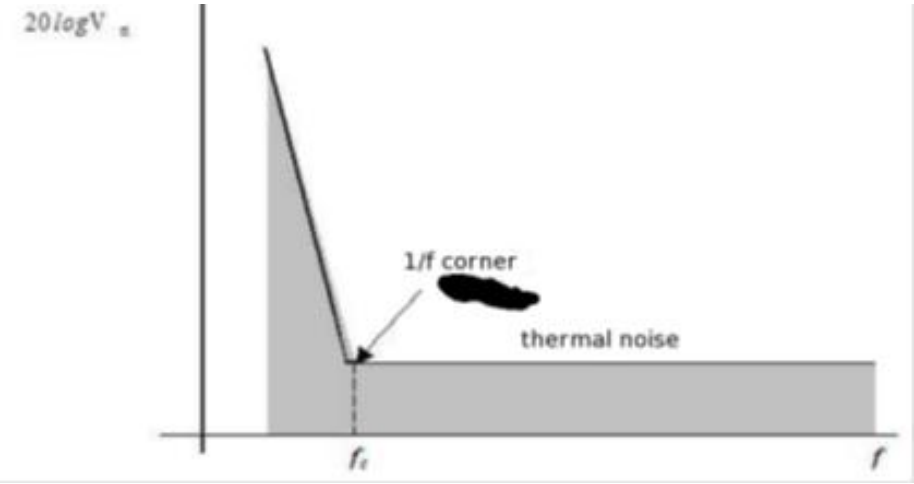

Figure 5.2: Flicker noise corner frequency.

Flicker noise has been reported in forward body biased MOSFETs [36]. In this chapter noise model is developed for a forward body biased MOSFETs and used in the detailed analysis of 0.8 V forward body biased op-amp that is reported in [37] and [38].

5.5 Noise in a Forward Body biased MOSFET

While operating the MOSFET under the zero body bias condition the shot noise can be neglected since number of carriers crossing the bulk-source reverse biased p-n junction is very small. Nevertheless, there will be significant increase in the magnitude of shot noise under the forward body-biased condition since the carriers across the junction increase exponentially. Consequently, it is clear that the forward body-bias should be limited to a certain level to avoid introducing significant noise especially when it becomes comparable to the input signal. Thus we can say that the amount of forward body voltage is also limited by the noise along with the latch-up current.

The shot noise current spectral density can be transformed to an equivalent noise voltage spectral density by multiplying Eq. (5.4) by the p-n junction impedance, $1/j\omega C_{SB}$. The angular frequency is ω and the source-bulk junction capacitance is C_{SB}. Experimental results demonstrate that the thermal noise of a MOSFET reduces with increasing forward bias between the source-bulk junction [37] & [38]. The forward-biased bulk results in a

reduced threshold voltage, which increases the trans-conductance, g_m that reduces the thermal noise. However, the shot noise in an n-MOSFET upsurges with increasing forward body-bias due to increase in conduction of the bulk-source p-n junction diode. Experimental results reported in [36] show that from noise analysis point of view also, a forward body-bias greater than 0.4 V is not recommended.

Figure 5.3 demonstrate the small signal noise model of forward body bias MOSFET. In figure 5.3 $\overline{\imath_d^2}$ is the drain current noise generator, $\overline{\imath_g^2}\ and\ \overline{\imath_s^2}$ are gate and substrate leakage current generators respectively, $g_{mb}V_{bs}$ is the current source due to source-bulk voltage V_{bs}, g_mV_{gs} is the current source due to gate-source voltage V_{gs}. r_d is the small signal output resistance, $C_{db}, C_{sb}, C_{gs}, C_{gd}$and C_{gb} are the capacitances of MOSFET.

While analyzing noise for a MOSFET, generally under the reverse body bias, the substrate leakage current noise generator $\overline{\imath_s^2}$ has a very small value so it is neglected. However for the forward body bias noise model $\overline{\imath_s^2}$ should be included. The leakage current has exponential dependence on the forward body bias voltage. The equivalent input referred noise is calculated by equating all the current sources to the output current [39]. We get

$$\frac{g_m}{j\omega c_{gs}} i_i = i_g \frac{g_m}{j\omega c_{gs}} + i_d + i_s \frac{g_{mb}}{j\omega c_{sb}}. \tag{5.7}$$

Where i_i, i_g, i_d, and i_s are the rms values of input, gate leakage, drain-source and substrate currents. $g_{mb}$is the transconductance due to forward biased bulk-source junction.

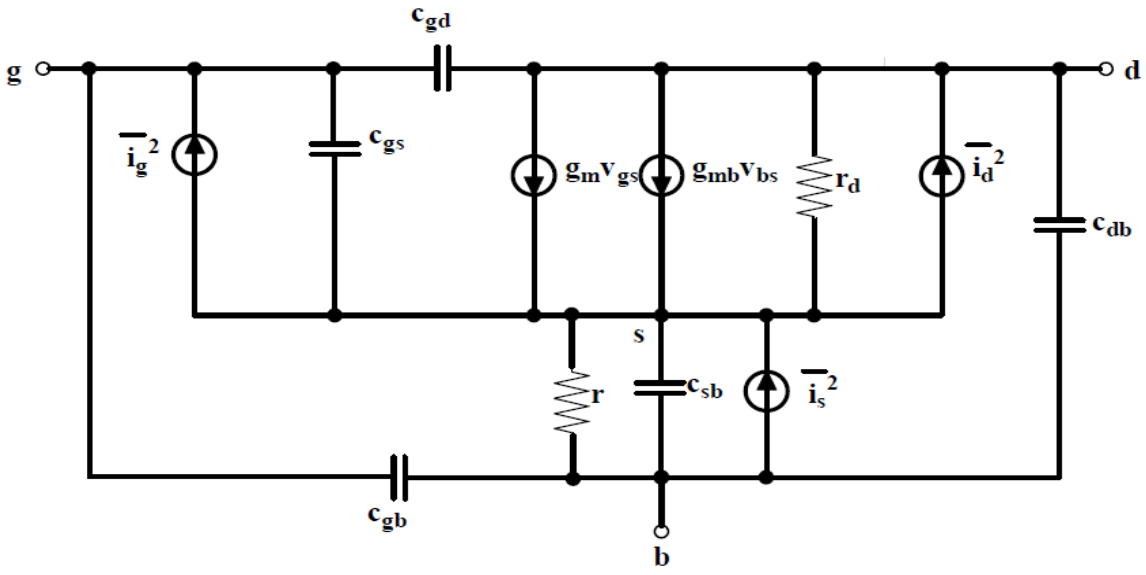

Figure 5.3: Small signal noise model of a forward body-biased n-MOSFET. Source, drain, gate and substrate are denoted by s, d, g and b, respectively.[36]

Equation (5.7) does not include the effect of all the parasitic capacitances since all the currents are independent, regardless of phase relationship we can write:

$$\overline{\imath_i^2} = \overline{\imath_g^2} + \overline{\imath_d^2}\frac{\omega^2 c_{gs}^2}{g_m^2} + \overline{\imath_s^2}\frac{c_{gs}^2}{c_{sb}^2}\frac{g_m^2}{g_{mb}^2}. \qquad (5.8)$$

Where PSDs can be defined as:

$\frac{i_d^2}{\Delta f} \approx \frac{8}{3} kT g_m$,

$\frac{i_g^2}{\Delta f} = 2qI_G$ and

$\frac{i_s^2}{\Delta f} = 2qI_S$. I_G is the gate current and I_S is the body leakage current.

The total noise current spectral density $\frac{i_d^2}{\Delta f}$ is the sum of both the components that are thermal noise density and flicker noise density. That is given by:

$$\frac{i_d^2}{\Delta f} = \frac{8}{3} kT g_m + \frac{KI_D^a}{f}. \qquad (5.9)$$

Where both K and 'a' are constants and the value of 'a' varies between 0.5 -2.

While designing low voltage circuits using forward body bias flicker noise reduces. It is reported that for a constant I_D flicker noise lowers at the rate of 9dB/V for forward body biased MOSFET, operated in strong inversion region [36]. Deen and Marinov [36] have also shown the quadratic behaviour of flicker noise with drain current. In the proposed op-amp the supply voltage is very low resultantly very less (Compared to typical 5 V regular op-amp only 20% drain current is flowing) drain current flows in each transistor. Flicker noise corner frequency is also pushed back in the forward biased CMOS op-amp. The thermal noise density part in the equation (5.8) is given by:

$$\frac{\overline{i_{i\ thermal}^2}}{\Delta f} = \frac{\overline{i_d^2}}{\Delta f}\frac{\omega^2 c_{gs}^2}{g_m^2} = \frac{8}{3}kT\frac{\omega^2 c_{gs}^2}{g_m}. \tag{5.10}$$

The shot noise part is given by:

$$\frac{\overline{i_{i\ shot}^2}}{\Delta f} = 2qI_G + \frac{c_{gs}^2}{\Delta f}\frac{g_{mb}^2}{g_m^2}. \tag{5.11}$$

After neglecting the gate current we can write the equation as [37]:

$$\frac{\overline{i_{i\ shot}^2}}{\Delta f} \approx 2qI_{S0}\left(e^{-V_{SB}q/kT} - 1\right)\frac{c_{gs}^2}{c_{sb0}^2/(1+V_{SB}/\psi_0)}\frac{\gamma^2}{4(2\phi_f+V_{SB})}. \tag{5.12}$$

Where $C_{SB} = \frac{c_{sb0}}{\sqrt{(1+V_{SB}/\psi_0)}}$ and $\frac{g_{mb}^2}{g_m^2} = \frac{\gamma^2}{4(2\phi_f+V_{SB})}$.

In this equation:

γ is the body coefficient parameter for the MOSFET, C_{sb0} is the bulk-source junction parasitic capacitor at zero body bias, ϕ_f is the surface potential also discussed in chapter 3, ψ_0 is build-in potential and I_{s0} is the reverse saturation current. The first term in the equation (5.12) the first term is caused by negligibly small gate current. After neglecting the first term $\overline{i_s^2}$ of equation (5.12) can be put as a gate-referred noise generator. It is quite clear from the equation (5.12) that the noise current density is a function of forward body bias voltage V_{SB} so it is kept 0.4 V , not more than that. This value of VSB not only avoids CMOS latchup [26] but also keep the total noise low [38].

5.6 Noise Analysis of Proposed Forward Body Biased Current Mode Amplifier

The forward body biased current mode amplifier is again shown in the figure 5.4. the input referred noise of this current mode amplifier is given by [40]:

$$\overline{I_n^2} = [\frac{kT}{3}\left(g_{m_{Mn1}} + g_{m_{Mp1}}\right) + (2\pi f)^2 C_{in}^2 \overline{V_{op}^2}]\Delta f. \quad (5.13)$$

Where k is the Boltzmann's constant, T is the absolute temperature, g_m is the transconductance of MOS devices, f is the signal frequency, C_{in} is the input capacitance of forward body bias low voltage op-amp, Δf is the bandwidth of the FBBCMA and Vop is the input referred voltage noise of op-amp.

The first term in (5.13) is because of MP1/MN1. This term is proportional to the transconductance of the MOS devices used. Low dc currents in the devices result in a low noise performance. Since these devices are being operated at low dc currents and their noise contribution to the equivalent input noise is divided by the closed loop gain of the current mode amplifier, the noise influence of is negligible.

In the second term of equation (5.13), Vop is total noise contribution by the forward body biased CMOS op-amp. The detailed noise analysis of the forward body biased op-amp is presented in this section the circuit diagram of the proposed op-amp is depicted one more time for simplicity in figure 5.5.

Using the noise model presented in [39] the noise of forward biased op-amp can be calculated. The equivalent noise model is depicted in figure 5.6 where $\overline{v_{eq1}^2}, \overline{v_{eq2}^2}, \overline{v_{eq3}^2}$ and $\overline{v_{eq4}^2}$ are input noise voltage generator for transistors M_1 to M_4 respectively. Differential input signal is applied to M_3 and M_4 that are differential input devices. Due to large current and voltage gains of differential stage, the noise associated with the following stages becomes insignificant as compare to the input referred noise of differential stage itself [39].

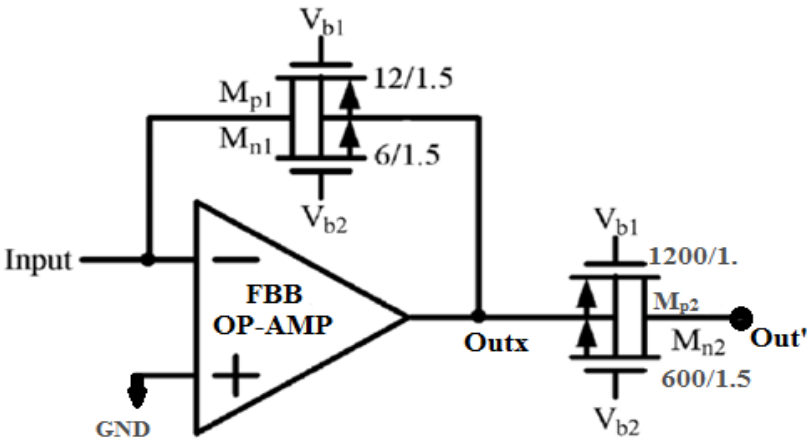

Figure 4.12: Structure of proposed current mode amplifier designed using forward body biased op-amp (same as fig. 4.12)

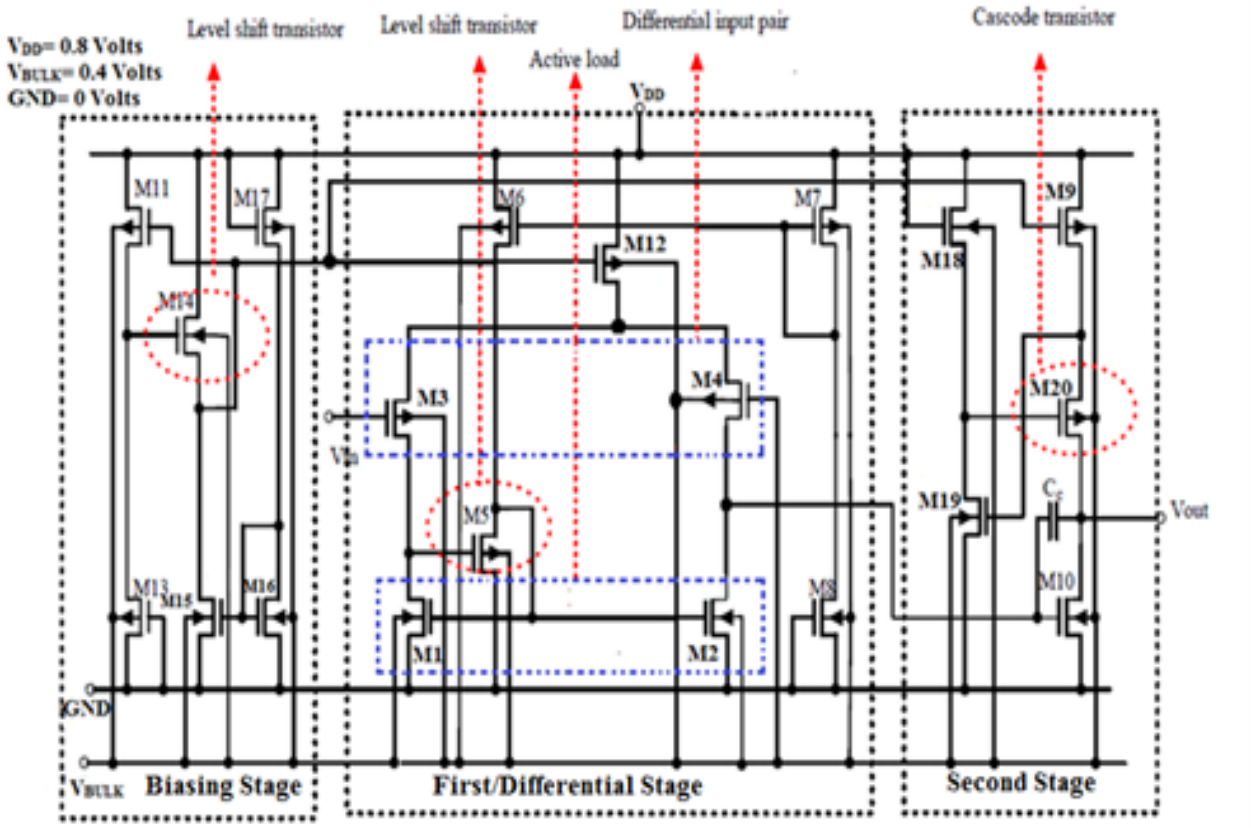

Figure 5.5: Circuit diagram of low voltage forward body bias CMOS Operationa Amplifier. Figure 5.5 is same as figure 4.5.

Assuming M_1 identical to M_2 and M_3 identical to M_4 the total equivalent input noise generator can be expressed as:

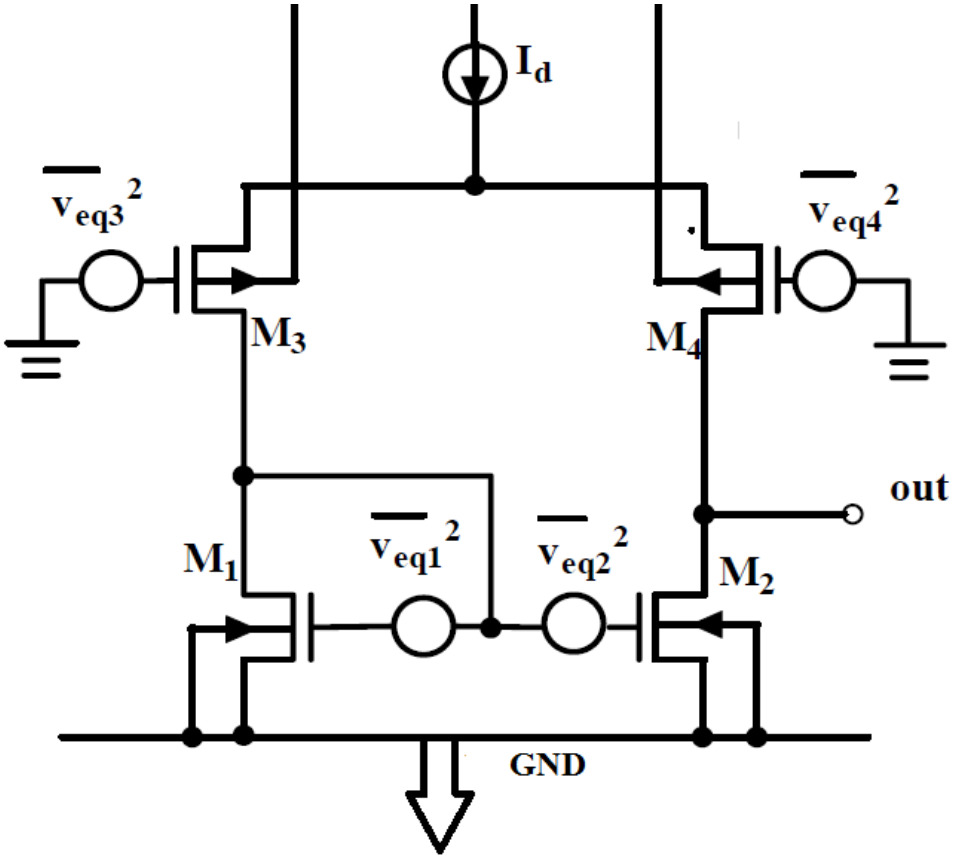

Figure 5.6: Noise model of a CMOS differential pair amplifier [39].

$$\overline{v_{eq\_total}^2} = \overline{v_{eq3}^2} + \overline{v_{eq4}^2} + \left(\frac{g_{m1}}{g_{m3}}\right)^2 \left(\overline{v_{eq1}^2} + \overline{v_{eq2}^2}\right). \tag{5.14}$$

Major noise contribution is caused by the differential stage of the op-amp.

Now the current noise generators described in equations (5.10) and (5.11) are converted into voltage noise generators, after doing so we obtain:

$$\frac{\overline{v_{i\ thermal}^2}}{\Delta f} = \frac{\overline{i_d^2}}{\Delta f}\frac{1}{g_m^2} = \frac{8}{3}kT\frac{1}{g_m}. \quad \text{and} \tag{5.15}$$

$$\frac{\overline{v_{i\ shot}^2}}{\Delta f} = \frac{\overline{i_s^2}}{\Delta f}|z^2|\frac{g_{mb}^2}{g_m^2} = 2qI_{S0}\left(e^{-V_{SB}q/kT} - 1\right)\left(r_{equ,s}//\frac{1}{\omega c_{sb}}\right)^2 \frac{\gamma^2}{4(2\phi_f + V_{SB})}. \tag{5.16}$$

As shown in the figure 5.6 the sources of the differential input pair (p-MOSFETs) are connected to the current source supplying current I_D, an equivalent output resistance will be present that is represented as $r_{equ,s}$ in equation (5.15). z is the equivalent load impedance. In the small signal equivalent of figure 5.6 $r_{equ,s}$ will appear in parallel with source-bulk capacitance C_{sb}, As discussed earlier the flicker noise will be negligible for this topology and $r_{equ,s}$ is infinite for an ideal current source. Using these assumptions substituting equation (5.15) and (5.16) in to equation (5.14) we yield:

$$\frac{\overline{v_{eq\_total}^2}}{\Delta f} =$$

$$\frac{16}{3}kT\frac{1}{g_{m3}} + 4qI_{S0}\left(e^{-V_{SB}q/kT} - 1\right)\left(r_{equ,s}//\frac{1}{\omega c_{sb}}\right)^2\frac{\gamma^2}{4(2\phi_f+V_{SB})} + \left(\frac{g_{m1}}{g_{m3}}\right)^2\left\{\frac{16}{3}kT\frac{1}{g_{m1}} + 4qI_{S0}\left(e^{-V_{SB}q/kT} - 1\right)\left(r_{equ,s}//\frac{1}{\omega c_{sb}}\right)^2\frac{\gamma^2}{4(2\phi_f+V_{SB})}\right\}. \quad (5.17)$$

By substituting equation (5.17) into equation (5.13) total noise of proposed forward biased current mode amplifier can be calculated. The output noise is plotted in figure 5.7, the simulated value of output noise is in close agreement with the calculated value from equation 5.17 which is $55\mu V/\sqrt{Hz}$. To obtain input referred noise the output noise voltage can be divided by the open loop gain of the op-amp, the obtained value of the input referred noise is 34.46 $nV/\sqrt{Hz}$ which is very good for bio-medical applications.

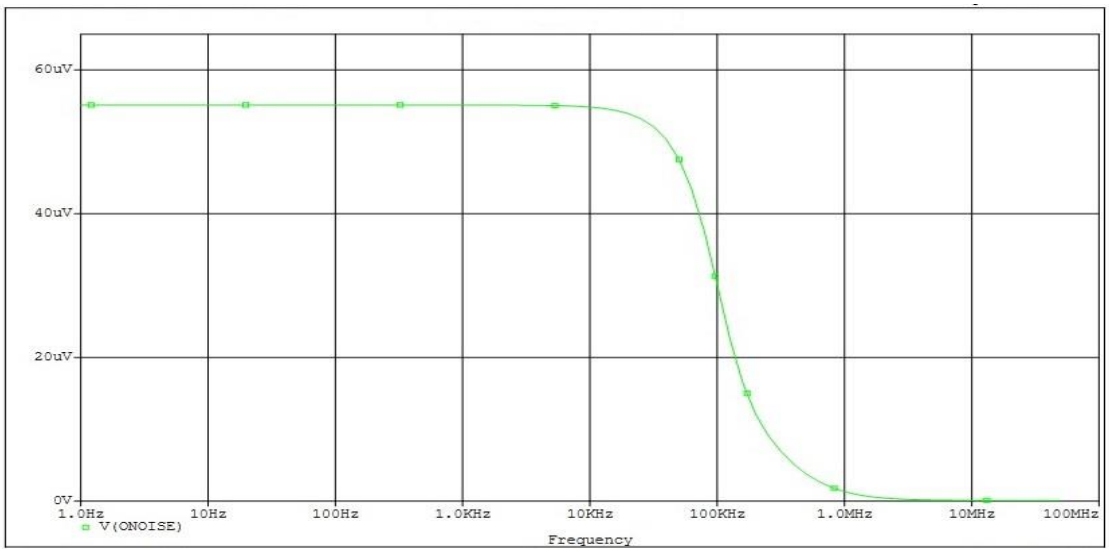

Figure 5.7: Output noise of forward body biased op-amp.

CHAPTER 6

AFE DESIGN USING FBBCMA

In this chapter a multi-functional analog readout frond end (AFE) is designed for bio-signal acquisition systems, using the forward body biased current mode amplifier (FBBCMA) proposed in section 4.4. This analog readout front-end is capable of processing cardiac signals (ECG), visual signals (ERG) and neural signals (EEG, ECoG and ENG). It has a tuneable response so it can provide current gain of 60 dB to in band signals and can reject signals that are interferers or lies out of the band of interest. This AFE provides a current gain of 1000 A/A. This analog front-end consumes very little power; the power consumption is only 150µW. The low power consumption enhances the battery life that is an essential criterion for the portable bio-signal recording systems. Very low input referred noise of value 34.46 $nV/\sqrt{Hz}$ added by this analog front-end ensures the batter signal quality. The output signal of this AFE is ready to be fed to the analog to digital converter and DSP respectively. This multi-functional analog readout front-end can be tuned for various bandwidths to provide a particular bio-signal as output. This single bio-signal readout could be employed in electrocardiograph/ electroencephalograph/ electrocorticograph/ electroretinograph or electroneurograph.

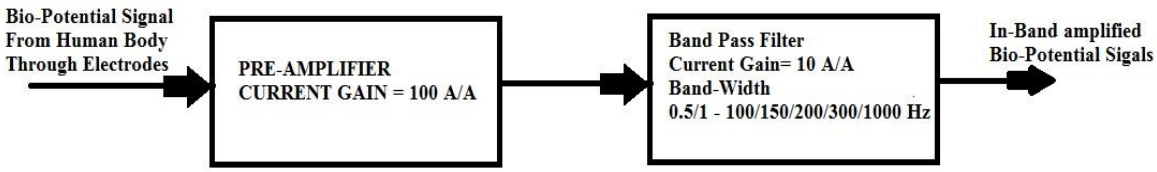

Figure 6.1: Block Diagram of current mode multi-function analog readout front-end.

The block diagram of analog front-end is shown in figure 6.1. The AFE has two blocks, a pre-amplifier block that is flowed by a band-pass filter having tunable cut-off frequencies. The block diagram consist of a current mode pre-amplifier block as a first stage that can amplify the bio-signal acquired from human body through electrodes with a current gain of 100. After that this amplified signal is fed to the current mode band-pass filter that rejects out of band signals and provides a gain of 10 A/A to different in-band signals. The block diagram showed in figure 6.1 shows the specification of each block

and the interconnections between the blocks. Figure 6.2 depicts the circuit diagram of each block shown in Figure 6.1. first block in figure 6.2 is circuit diagram of pre-amplifier that provides a current gain of 100 A/A the output of this is fed to a band-pass filter which provides tunable high and low cut-off frequencies with a current gain of 10 A/A. A forward body biased op-amp that is employed in each circuit being operated at 0.8V.

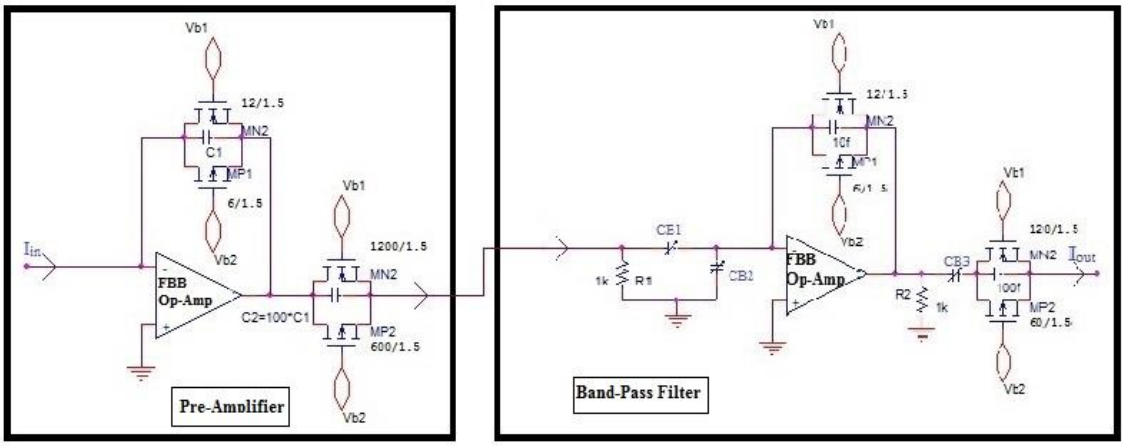

Figure 6.2: circuit diagram and interconnects of AFE shown in Fig. 6.1.

6.1 PRE-AMPLIFIER

This section deals with the design and functioning of the pre amplifier block. After that the simulation results are depicted. The pre amplifier design is the same as discussed in section 4.4. The pre amplifier shown in figure 6.3 is first stage of AFE it acquires the signal directly from human body through the electrodes. The architecture of the proposed pre amplifier consists of a forward body biased op-amp as active block. This pre-amplifier is a FBB op-amp with an active feedback loop. The current-mode pre-amplifier designed to amplify the in-band current signals. The integrated active feedback loop is operated at a very low frequency, which bypass the dc offset current that is generated from the electrode-tissue interface. Since the noise of the first stage is the dominate noise source, a current-mode preamplifier with low dc current is used as the first stage to suppress the noise contributed by this stage.

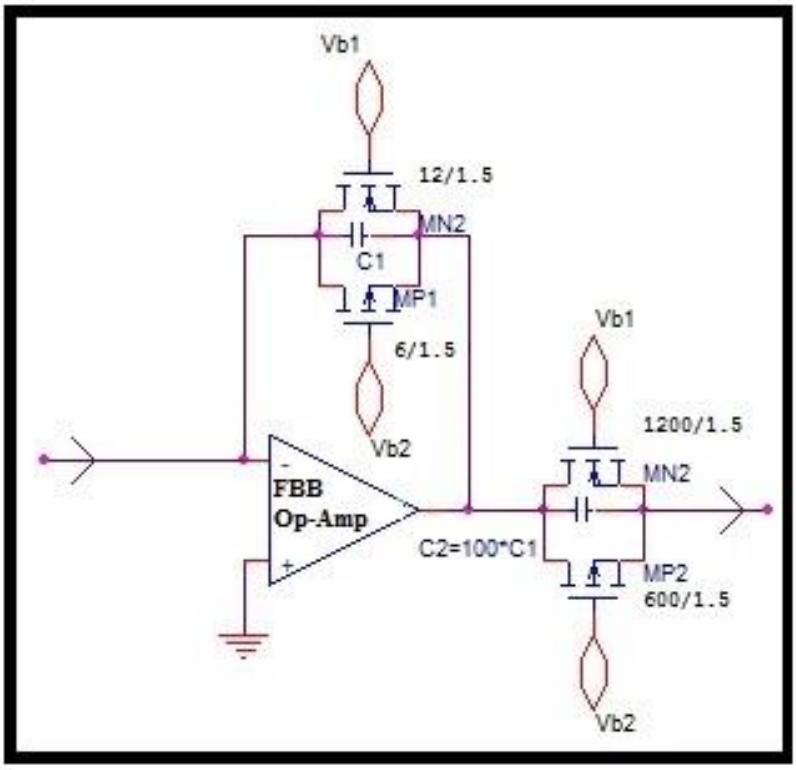

Figure 6.3: Circuit diagram of Pre-amplifier.

The operational amplifier that is incorporated as an active block is a two-stage topology. In the Structure of pre-amplifier the input and the output nodes of FBB Op-Amp are kept at same dc voltages via the negative feedback loop, consist of p-MOSFET and n-MOSFET. The dc voltage across the second stage MOSFETs is also set to zero via the negative feedback loop in the next stage. As a result, the dc drain-source voltages of all the MOS devices in feed-back are kept at 0 V. With Vb1=0.3V and Vb2=0.7V, all the feedback devices are being operated at a very low dc current in the linear sub-threshold region as resistors. Since the channel lengths of all devices are kept the same, the resistance ratio of Mp1 (MN1) to Mp2 (MN2) will be equal to the channel width ratio of Mp1 (MN1) to Mp2 (MN2) which is designed to be 100. With a small-signal input current flowing on Mp1 and Mn1, the small-signal voltage across M_{p1} and M_{n1} is the same as that of M_{p2} and M_{n2}. Thus the current flowing in M_{p2} and M_{n2} is 100 times of current flowing in M_{p1} and M_{n1} and a current gain of 100 can be obtained. The feed-back capacitances are to provide constant gain through-out the bandwidth. Current mode pre-

amplifier has low input impedance and low distortion. Frequency response of pre amplifier is shown in figure 6.4 same as in figure 4.13.

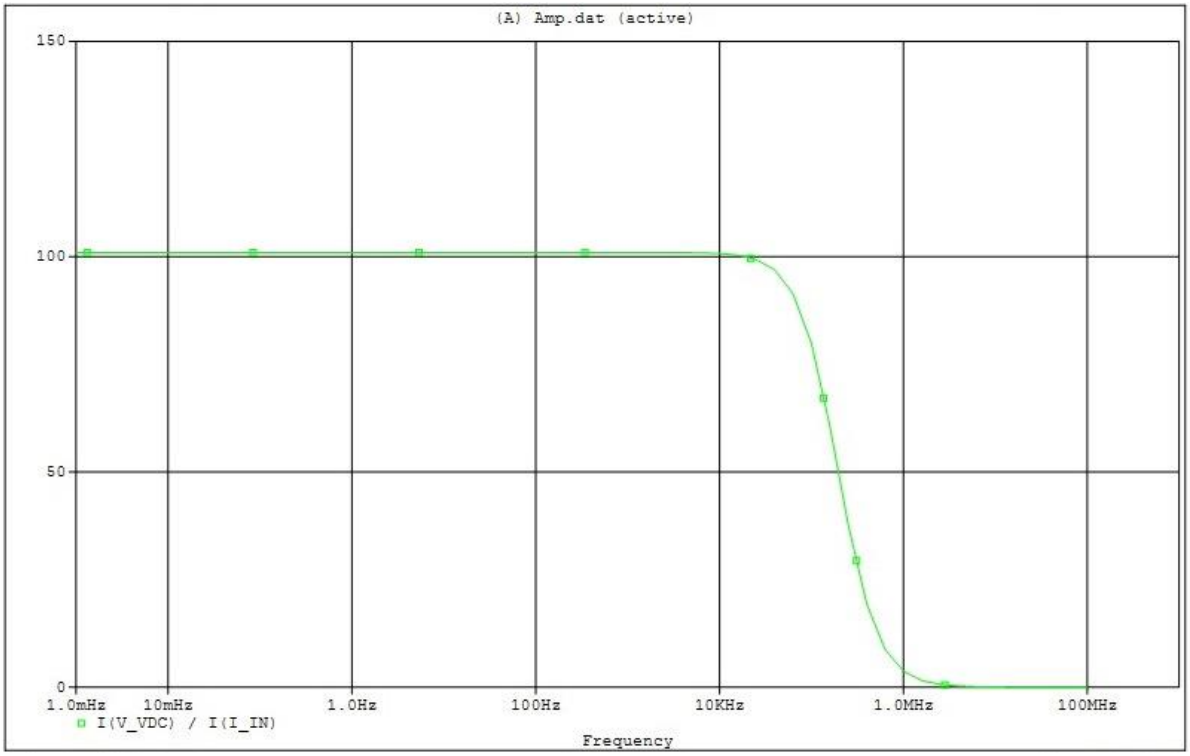

Figure 6.4: Frequency response of proposed FBBCMA with the gain of 100 A/A (same as Figure 4.13).

6.2 BAND-PASS FILTER

Figure 6.5 depicts the circuit diagram of the band-pass filter. The filter has input signal that is coming from the output node of the pre amplifier. The amplification mechanism of the band-pass filter is same as discussed earlier. The high-pass and low-pass cut-off frequencies of the band pass filter are tunable so that it can be defined for various bandwidths of different bio-signals. The tunable bandwidth makes it feasible to serve it as an AFE that could be incorporated in different bio-signal acquisition systems. The variable bandwidth is the key to this multi-functional system it enables us to provide the same gin for different band of frequencies of our interest in which various bio-signals lies. The high-pass and low pass cut-off frequencies can be given by flowing equations:

$$\left(f_{cut-off}\right)_{High-pass} = \left(\frac{C}{C+CB1}\right) Unity\ Gain\ Frequency. \quad (6.1)$$

$$\left(f_{cut-off}\right)_{Low-pass} = \left(\frac{C}{C+CB2}\right) Unity\ Gain\ Frequency. \quad (6.2)$$

Where C is feed-back capacitance connected in parallel to the Mn1 and Mn1 it should be 10 times smaller than the capacitance used in parallel to Mp2 and Mp1.

CB1=CB3 the variable capacitances CB1, CB2 and CB3 makes the response of this band-pass filter flexible.

Unity gain frequency is associated with the FBB Op-Amp employed in FBBCMA.

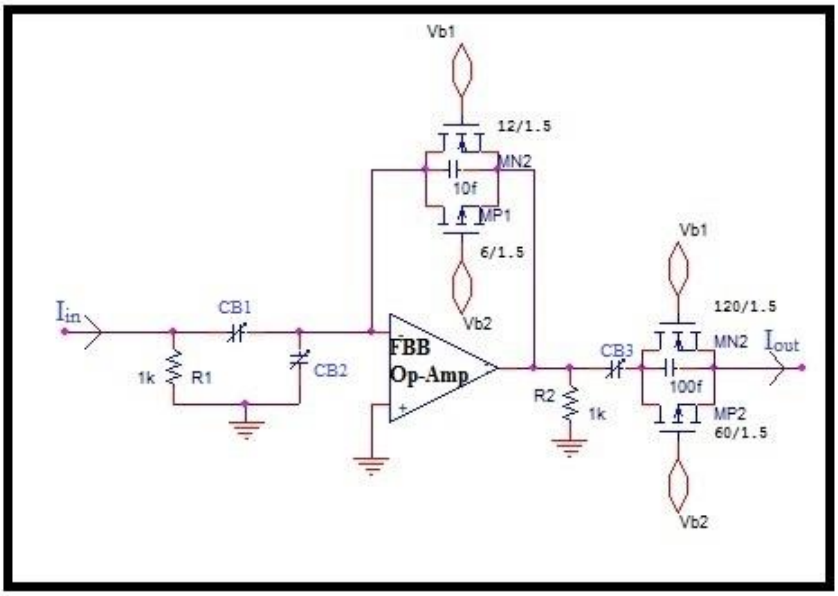

Figure 6.5: Circuit diagram of band-pass filter.

Frequency responses for various for various bio-signals are shown in figures 6.6 to figure 6.10.

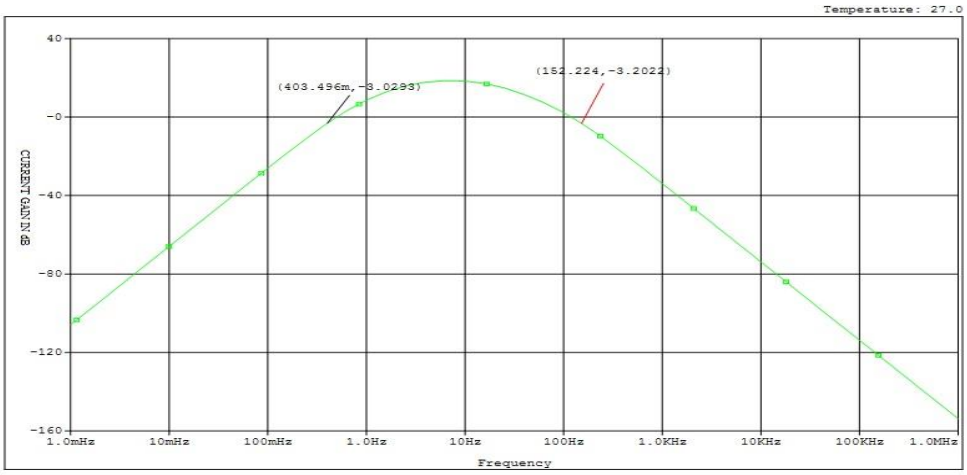

Figure 6.6: Band-pass response for ECG with cut-off frequencies.

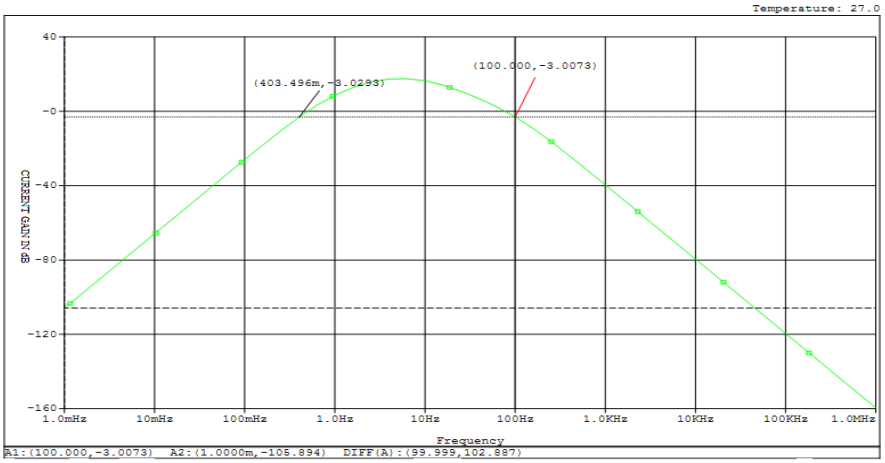

Figure 6.7: Band-pass response for EEG with cut-off frequencies.

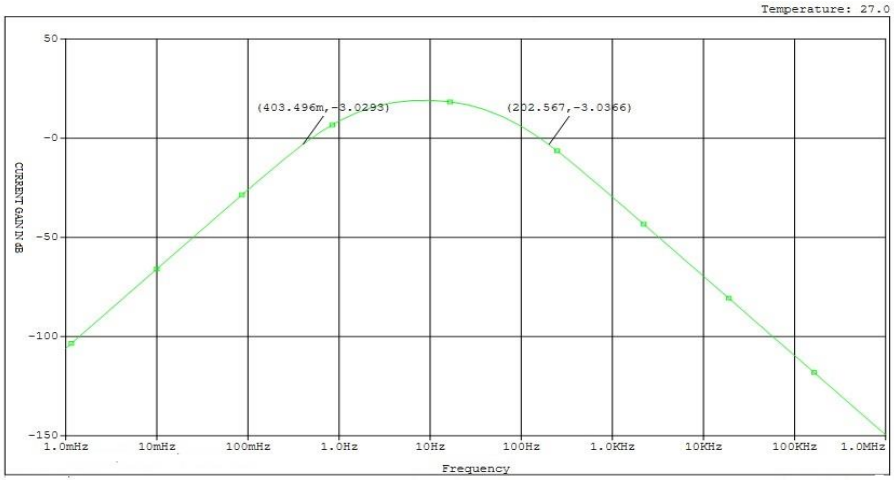

Figure 6.8: Band-pass response for ECoG with cut-off frequencies.

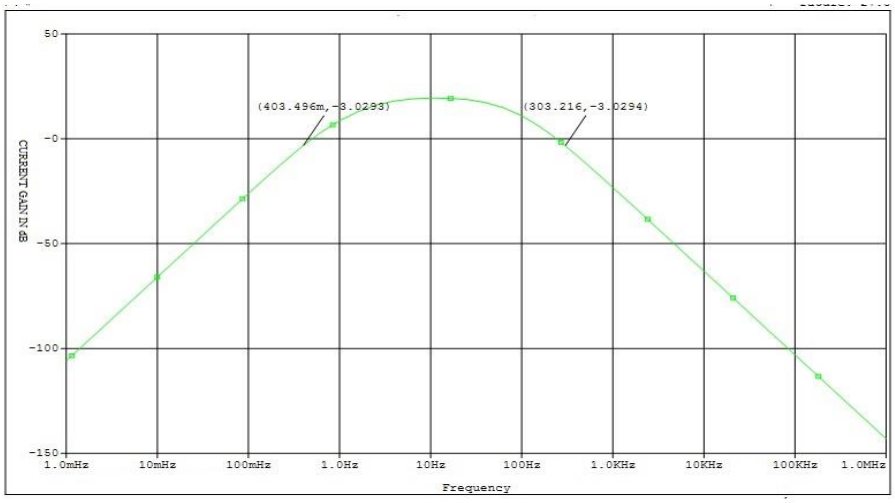

Figure 6.9: Band-pass response for ERG with cut-off frequencies.

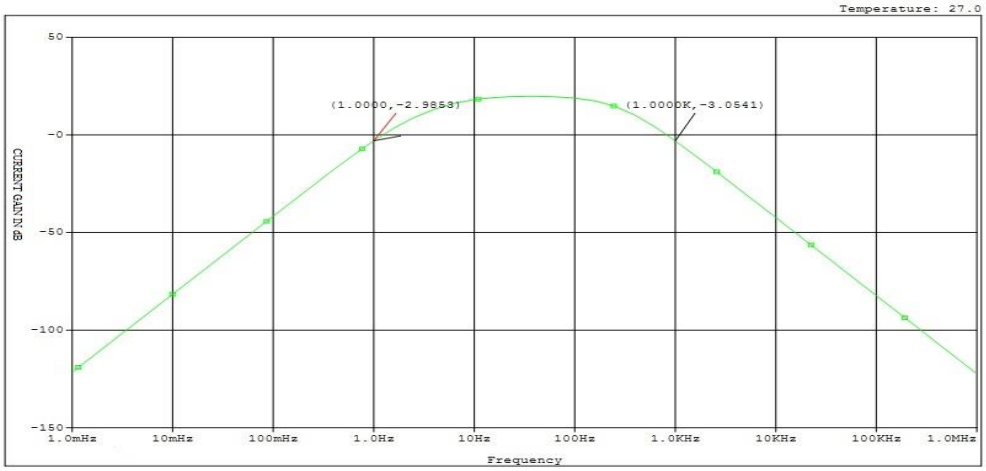

Figure 6.10: Band-pass response for ENG with cut-off frequencies.

6.3 Frequency Responses of AFE

Frequency responses of read out front end for different bio-potential signals are shown from figure 6.10 to 6.14. The power dissipated by the readout analog front end is 150 µW. the noise contribution by the pre-amplifier is the dominant due to the high gain provided by this stage. The input referred noise has a small value of 34.46 $nV/\sqrt{Hz}$.

Figure 6.11: Response for EEG Signal.

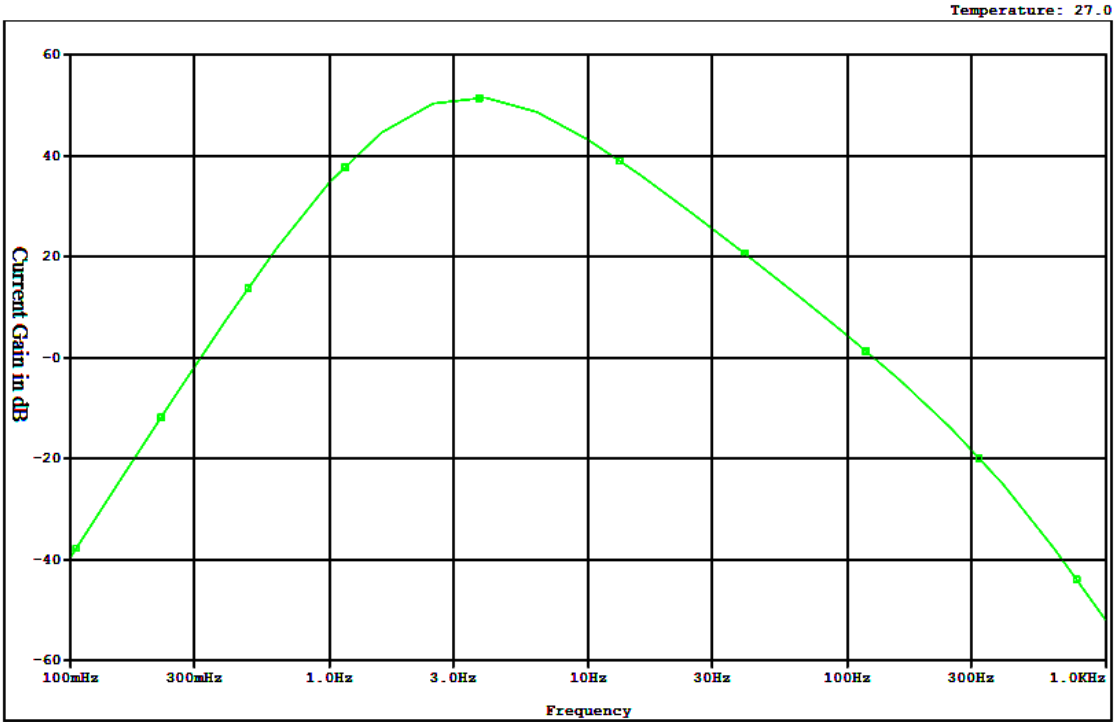

Figure 6.12: Response for ECG Signal.

Figure 6.13: Response for ECoG Signal.

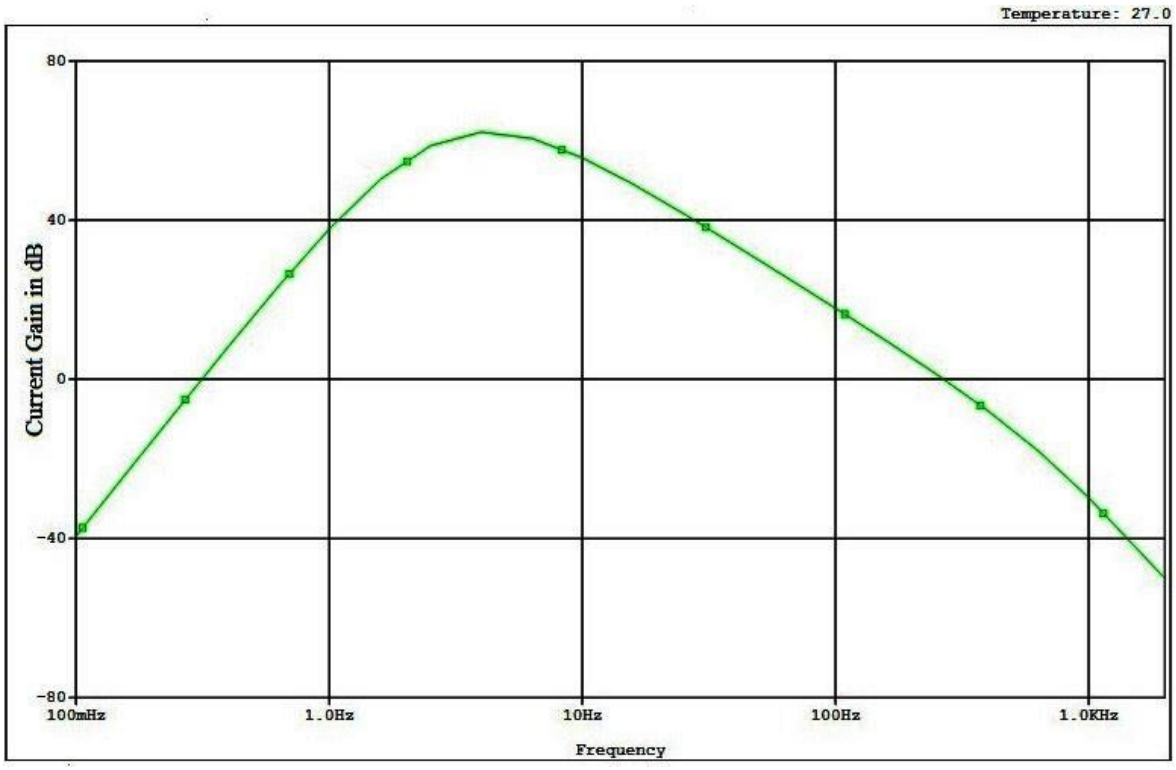

Figure 6.14: Response for ERG Signal.

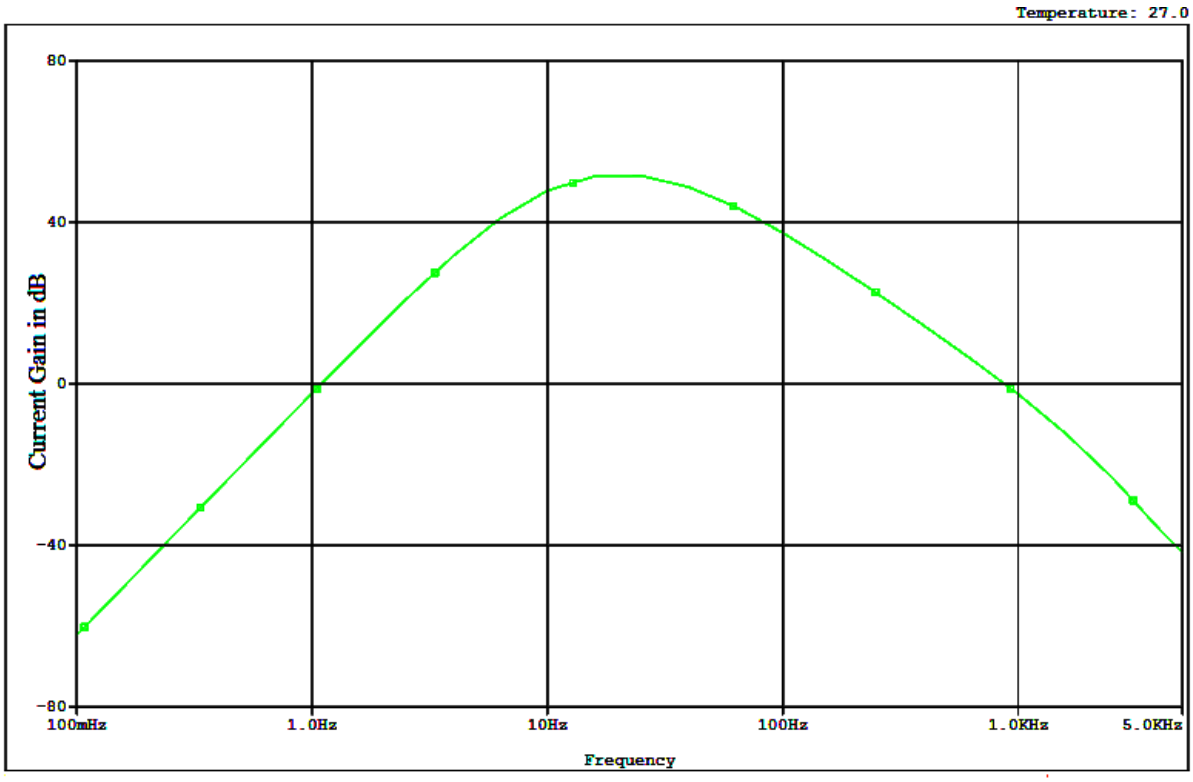

Figure 6.15: Response for ENG Signal.

CHAPTER 7

CONCLUSIONS AND FUTURE WORK

7.1 Conclusion

Electrocardiogram (ECG), electroencephalogram (EEG), Electrocorticogram (ECoG), Electroneurogram (ENG) and electroratinogram (ERG) are common bio-potential signals for practical clinic and health care applications. They are with very small amplitudes and locate in very low frequency signal band. In earlier days the patients were connected to the bulky devices to measure these signals at health centres.

Modern health care system which consists of signal readout front-end, diagnosis knowledge database, signal processor, wired/wireless communication transceiver and user terminal is of great demand. Low power light weight design is capable of extending the use of such a system from clinical centers to sports, entertainment and daily health care applications. The crucial and power consuming building block of the system is the analog readout front-end which is the key work of this dissertation.

Chapter 1 introduces the need and importance of the flexible analog readout front end along with the challenges that a designer has to face while designing the same. It also describes bio-potential signals and the corresponding recording methods and systems. In chapter the theoretical background is elaborated that is necessary for design. This chapter deals with the pros and cons of all the low voltage circuit design techniques that are being used in analog IC design. After that there is a critical comparison between the voltage mode and current mode circuits, this discussion led us to the final readout front end design that is a forward body biased current mode circuit, in which MOSFETs are employed as active devices.

Chapter 3 has an insight about the forward body biased MOSFET. This chapter has a detailed description of the device behaviour under a forward bias applied upon the source-bulk junction. Using this technique a low-voltage operational amplifier is designed in the chapter 4. In this chapter the low-power op-amp that is being operated at 0.8V power supply is characterize. The complete analysis of FBB op-amp and comparison with some other op-amp has been done in major portion of this chapter. The

last section of chapter 4 describes the current mode amplifier that incorporates the forward body bias op-amp. This block consumes small power of value 55 µW. being a current mode circuit it has low impedance and low distortion. Using this FBBCMA as an active block the complete analog readout front end is designed in this work.

Noise Is a matter of critical concern in the AFEs for bio-signals, chapter five deals with the noise analysis of the Forward Body Biased Current Mode amplifier (FBBCMA). The noise model for the FBB op-amp is studied and analysed and thereafter the noise of FBBCMA is modelled and simulated using P-Spice. As the first stage has the largest gain so noise introduced by subsequent stages is neglected. The value of input referred noise is about 34.5 $nV/\sqrt{Hz}$, that is low amount. As discussed earlier this would be the total input referred noise for the AFE.

In the last chapter the analog read out front end for all the above mentioned signal is designed using FBBCMA. In first section pre amplifier design is discussed which is having a current gain of 100 A/A. A tuneable band pas filter is the second stage of the AFE that has a current gain of 10 A/A. The adjustable frequency response of the band-pass filter enables us to use this AFE for acquisition of variety of bio-signals.

7.2 Future Work

The op-amp used in the used in the current mode amplifier (CMA) is expected to be further optimized and simplified for lower power dissipation. The use of large capacitances in the band-pass filters to achieve small cut-off frequencies making the circuit a bit bulkier. Moreover, these large capacitances are limiting the gain while cascading the circuit.

DC removing circuitry is required to be built for the circuit to operate in real situation, i.e. to reject the large electrode DC offset voltage. This could be done using active feed-back loops that will further increase the CMRR [40]. The circuit is also expected to be implemented on real silicon chip.

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APPENDIX A
MOSIS SPICE LEVEL 7 MODEL PARAMETERS FOR A STANDARD N-WELL CMOS TECHNOLOGY

The following SPICE level 3 MOS model parameters used in simulation have been obtained from the following website: www.mosis.org.

```
* PSPICE TSMC180nm.lib file  RWN  04/18/2010
* library  file for transistor parameters for TMSC 0.18 micron process
* uses BIM parameters added 01/15/98
* can configure and attach to Nbreak and Pbreak transistors in PSpice
****
******************  180nm TSMC parameters  **************
*T14B SPICE BSIM3 VERSION 3.1 PARAMETERS
* downloaded from MOSIS 04/18/10
*http://www.mosis.com/cgi-bin/cgiwrap/umosis/swp/params/
* tsmc-018/t92y_mm_non_epi_thk_mtl_params.txt
*SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8
* DATE: Jun  8/01
* LOT: T14B                WAF: 06
* Temperature_parameters=Default
*$
.MODEL TSMC180nmN NMOS (                                LEVEL   = 7
+VERSION = 3.1           TNOM    = 27            TOX     = 4.1E-9
+XJ      = 1E-7          NCH     = 2.3549E17     VTH0    = 0.354505
+K1      = 0.5733393     K2      = 3.177172E-3   K3      = 27.3563303
+K3B     = -10           W0      = 2.341477E-5   NLX     = 1.906617E-7
+DVT0W   = 0             DVT1W   = 0             DVT2W   = 0
+DVT0    = 1.6751718     DVT1    = 0.4282625     DVT2    = 0.036004
+U0      = 327.3736992   UA      = -4.52726E-11  UB      = 4.46532E-19
+UC      = -4.74051E-11  VSAT    = 8.785346E4    A0      = 1.6897405
+AGS     = 0.2908676     B0      = -8.224961E-9  B1      = -1E-7
+KETA    = 0.021238      A1      = 8.00349E-4    A2      = 1
+RDSW    = 105           PRWG    = 0.5           PRWB    = -0.2
+WR      = 1             WINT    = 0             LINT    = 1.351737E-8
*+XL     = -2E-8         XW      = -1E-8
+ DWG    = 1.610448E-9
+DWB     = -5.108595E-9  VOFF    = -0.0652968    NFACTOR = 2.4901845
+CIT     = 0             CDSC    = 2.4E-4        CDSCD   = 0
+CDSCB   = 0             ETA0    = 0.0231564     ETAB    = -0.058499
+DSUB    = 0.9467118     PCLM    = 0.8512348     PDIBLC1 = 0.0929526
+PDIBLC2 = 0.01          PDIBLCB = -0.1          DROUT   = 0.5224026
+PSCBE1  = 7.979323E10   PSCBE2  = 1.522921E-9   PVAG    = 0.01
+DELTA   = 0.01          RSH     = 6.8           MOBMOD  = 1
+PRT     = 0             UTE     = -1.5          KT1     = -0.11
+KT1L    = 0             KT2     = 0.022         UA1     = 4.31E-9
+UB1     = -7.61E-18     UC1     = -5.6E-11      AT      = 3.3E4
+WL      = 0             WLN     = 1             WW      = 0
+WWN     = 1             WWL     = 0             LL      = 0
```

```
+LLN    = 1          LW     = 0          LWN    = 1
+LWL    = 0          CAPMOD = 2          XPART  = 0.5
+CGDO   = 7.7E-10    CGSO   = 7.7E-10    CGBO   = 1E-12
+CJ     = 1.010083E-3  PB     = 0.7344298   MJ     = 0.3565066
+CJSW   = 2.441707E-10  PBSW   = 0.8005503   MJSW   = 0.1327842
+CJSWG  = 3.3E-10     PBSWG  = 0.8005503   MJSWG  = 0.1327842
+CF     = 0          PVTH0  = 1.307195E-3  PRDSW  = -5
+PK2    = -1.022757E-3  WKETA  = -4.466285E-4  LKETA  = -9.715157E-3
+PU0    = 12.2704847   PUA    = 4.421816E-11  PUB    = 0
+PVSAT  = 1.707461E3   PETA0  = 1E-4       PKETA  = 2.348777E-3   )
*
*$
.MODEL TSMC180nmP PMOS (                    LEVEL  = 7
+VERSION = 3.1        TNOM   = 27         TOX    = 4.1E-9
+XJ     = 1E-7       NCH    = 4.1589E17   VTH0   = -0.4120614
+K1     = 0.5590154   K2     = 0.0353896   K3     = 0
+K3B    = 7.3774572   W0     = 1E-6       NLX    = 1.103367E-7
+DVT0W  = 0          DVT1W  = 0          DVT2W  = 0
+DVT0   = 0.4301522   DVT1   = 0.2156888   DVT2   = 0.1
+U0     = 128.7704538  UA     = 1.908676E-9  UB     = 1.686179E-21
+UC     = -9.31329E-11  VSAT   = 1.658944E5  A0     = 1.6076505
+AGS    = 0.3740519   B0     = 1.711294E-6  B1     = 4.946873E-6
+KETA   = 0.0210951   A1     = 0.0244939   A2     = 1
+RDSW   = 127.0442882  PRWG   = 0.5        PRWB   = -0.5
+WR     = 1          WINT   = 5.428484E-10  LINT   = 2.468805E-8
*+XL    = -2E-8       XW     = -1E-8
+DWG    = -2.453074E-8
+DWB    = 6.408778E-9  VOFF   = -0.0974174  NFACTOR = 1.9740447
+CIT    = 0          CDSC   = 2.4E-4     CDSCD  = 0
+CDSCB  = 0          ETA0   = 0.1847491   ETAB   = -0.2531172
+DSUB   = 1.5        PCLM   = 4.8842961   PDIBLC1 = 0.0156227
+PDIBLC2 = 0.1       PDIBLCB = -1E-3      DROUT  = 0
+PSCBE1 = 1.733878E9  PSCBE2 = 5.002842E-10  PVAG   = 15
+DELTA  = 0.01       RSH    = 7.7        MOBMOD = 1
+PRT    = 0          UTE    = -1.5       KT1    = -0.11
+KT1L   = 0          KT2    = 0.022      UA1    = 4.31E-9
+UB1    = -7.61E-18   UC1    = -5.6E-11   AT     = 3.3E4
+WL     = 0          WLN    = 1          WW     = 0
+WWN    = 1          WWL    = 0          LL     = 0
+LLN    = 1          LW     = 0          LWN    = 1
+LWL    = 0          CAPMOD = 2          XPART  = 0.5
+CGDO   = 7.11E-10    CGSO   = 7.11E-10    CGBO   = 1E-12
+CJ     = 1.179334E-3  PB     = 0.8545261   MJ     = 0.4117753
+CJSW   = 2.215877E-10  PBSW   = 0.6162997   MJSW   = 0.2678074
+CJSWG  = 4.22E-10    PBSWG  = 0.6162997   MJSWG  = 0.2678074
+CF     = 0          PVTH0  = 2.283319E-3  PRDSW  = 5.6431992
+PK2    = 2.813503E-3  WKETA  = 2.438158E-3  LKETA  = -0.0116078
+PU0    = -2.2514581   PUA    = -7.62392E-11  PUB    = 4.502298E-24
+PVSAT  = -50        PETA0  = 1E-4       PKETA  = -1.047892E-4   )
*
.ENDS
```

APPENDIX B
MEASURMENT of AMPLIFIER PARAMETERS [35 & 8]

Figure B.1 shows a model of a non-ideal operational amplifier. C_{id} and R_{id} form the finite differential input impedance. The output resistance is modeled by R_{out}. The common mode input resistances are modeled by the resistor, R_{icm}. VOS is the input offset voltage. I_{B1} and I_{B2} are the input bias currents. The common mode rejection ratio (CMRR) is modeled by the voltage controlled voltage source. The op-amp noise is modeled by two noise sources, the voltage noise generator, $e_n^2$and the current noise generator, i_n^2. In the following sections, measurement techniques used in extraction of amplifies parameters are described.

B.1 COMMON MODE REJECTION RATIO (CMRR)

The CMRR is defined as follows:

$$CMRR = \frac{A_{DM}}{A_{CM}}. \qquad \text{(B.1)}$$

Where A_{DM} and A_{CM} are pure differential mode gain and common mode gains, respectively.

Figure B.2 shows the configuration for measuring the A_{CM}.

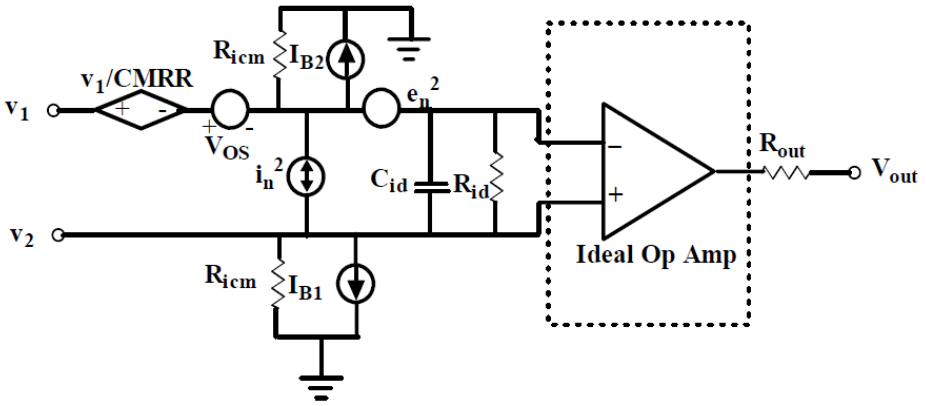

Figure B.1: Non ideal operational amplifier.

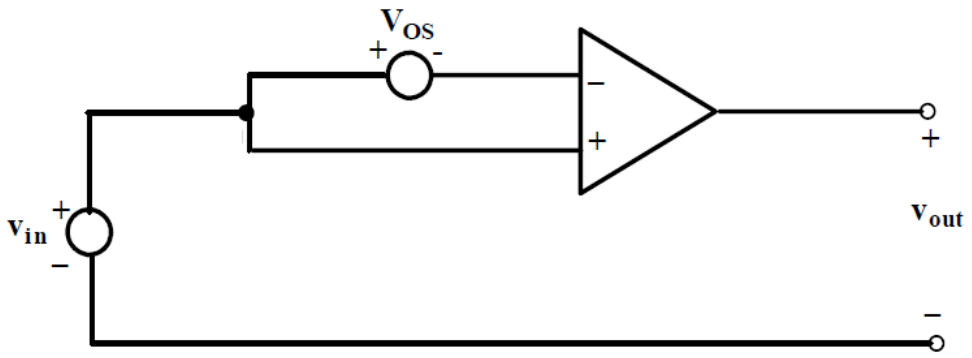

Figure B.2: Common mode gain A_{CM} measurement.

B.2 POWER SUPPLY REJECTION RATIO (PSRR)

The power supply rejection ratio (PSSR) is defined as the product of open loop gain of the amplifier and ratio of the change in power supply divided by the change in the output voltage which is caused by the change in the power supply voltage. A small signal is inserted in series with the power supply voltage to measure PSRR as shown in Fig. B.3.

PSSR can be calculated using the following equation:

$$PSRR = \frac{\Delta V_{DD}}{\Delta V_{out}} A_v. \qquad \text{(B.2)}$$

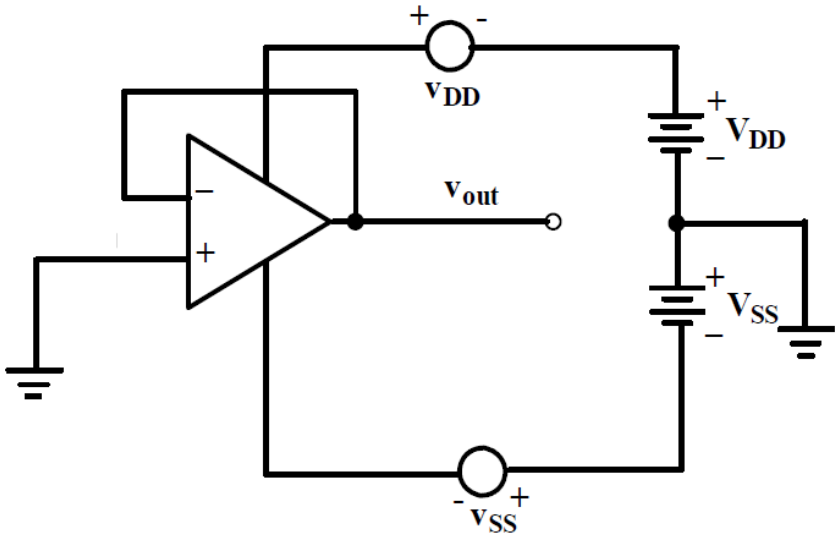

Figure B.3: PSRR measurement.

B.3 INPUT COMMON MODE RANGE (ICMR)

ICMR specifies the range of input common-mode voltage over which the differential amplifier continues to sense and amplify the difference signal with the same gain. Figure B.4 shows the ICMR measurement configuration where the amplifier is used in the unity-gain configuration. The ICMR is obtained from the linear past of the transfer curve, where the slope is unity, $V_{out}/V_{in}=1$.

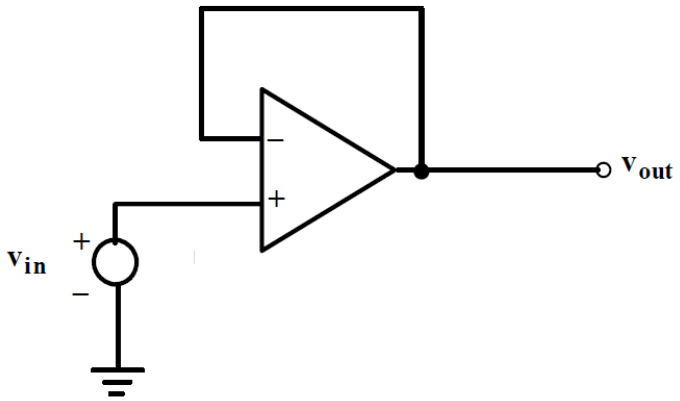

Figure B.4: ICMR measurement.

B.3 SLEW RATE (SR)

Slew rate is defined as the rate of change of the output voltage. It is related to current sourcing or sinking capability of the amplifier. A unity gain configuration is used to measure the slew rate. With a square wave form input whose step is sufficiently large (> 0.5 V) is applied, the output of amplifier will slew since amplifier needs enough current to charge and discharge the load capacitor. The slew rate is determined by the slope of the output wave form. The slope of the rising output is SR^{+}. The slope of the falling output is SR^{-}. Figure B.5 shows the configuration of amplifier for measuring SR.

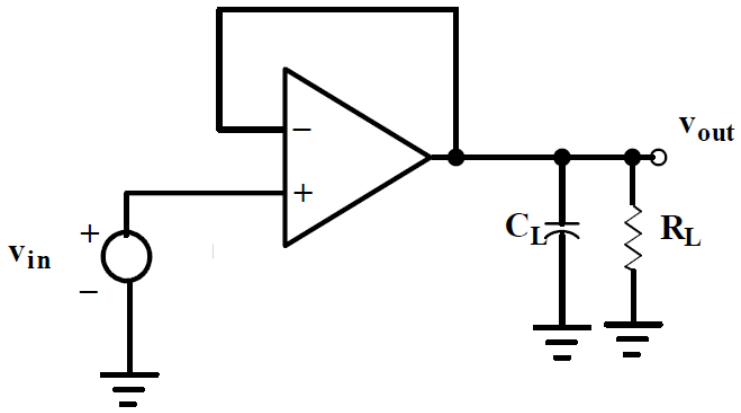

Figure B.5: Configuration of amplifier for measuring SR. R_L and C_L are included for the output loading during slew rate measurements.