CHAPTER 1

INTRODUCTON

The present dissertation deals with Wave Active Filters and their realization using Voltage Differencing Buffered Amplifier (VDBA). Today world is moving towards the Digital domain with a great pace. Nearly 85% work in the field of communication, electronic circuits and instrumentation is carried out with the help of Digital Signal Processing (DSP), but at the very basic level all signals available in nature are inherently analog which makes Analog Signal Processing (ASP) a bridge between the real world and so called digital world. In any digital system which is interfacing to an analog signal, the presence of ASP can't be avoided because of two reasons: first to remove aliasing before A/D conversion and second to match dynamic range of input signal to that of ADC [1]. Thus no matter how much advancements take place in the field of DSP and its application area, ASP will be needed. Indeed, the advancement in DSP also brings new challenges in the field of ASP as the requirements of advanced interfacing circuits are dealt by ASP only.

The choice of selection between ASP and DSP depends on our requirements. DSP provides higher accuracy, programmability, ease of storage and low cost implementation which makes it an obvious choice for signal processing but besides at the end points requirement, there are certain circumstances where ASP provides better results and is the only available solution. Signals having larger bandwidth need faster A/D converter as well as faster digital signal processor and to fulfill these requirements the required digital hardware (i.e. higher sampling rate switches) is not practically realizable [2]. These types of signals are better handled with ASP. There are certain limitations present in ASP as well. Though ASP is faster than DSP but it is less flexible and may need more expensive components.

In ASP, wide range of operations are performed such as filtering, amplification, signal generation, addition, comparison, multiplication, division, synchronous detection, interference minimization and noise reduction etc. This signal processing technique also deals with conversion of signals from one analog domain to another: voltage to current, current to voltage and ac to dc etc. These wide ranges of operations are possible due to availability of large amount of active

elements known as Active Building Blocks (ABBs). Starting from the basic transistor (both Bipolar as well as MOSFET), Operational Amplifier (Op-amp), Operational Tansconductance Amplifier (OTA), Current Feedback Operational Amplifier (CFOA), Current Conveyors and their numerous derivatives are basic active elements used in ASP. A very comprehensive catalogue of different active building blocks has been given in [3, 4]. As the present work deals with wave active filters it is worthwhile to review the fundamentals of active filters briefly.

1.1 FUNDAMENTALS OF FILTER

In ASP, Filtering is a very important and integrated process. Filter is a frequency selective circuit that reshapes the frequency spectrum of an input signal. In general, filter is a device that allows some quantity of interest while rejects others. In electrical engineering, usually the quantity of interest is either a voltage or current signal. Any voltage or current signal can be thought as being comprised of different frequency components. Thus an electronic filter passes the signal of certain frequencies or frequency range and prevents the passage of others [5]. The range of frequencies in which filter allows the signal to pass is known as "passband" while the range of frequencies in which signal is attenuated by the filter is known as a "stopband". There is another region between passband and stopband known as the "transition band" which signifies the transition from passband to stopband characteristics of a filter (Fig. 1-1).

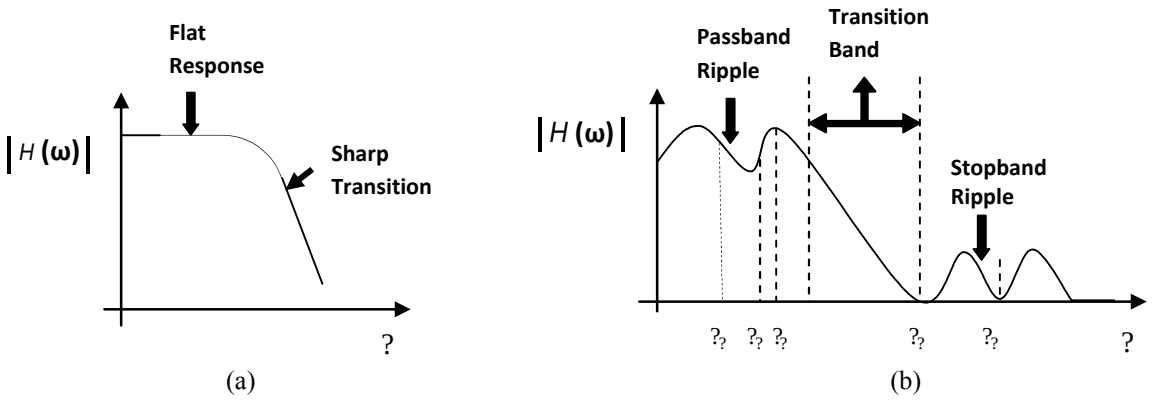


Fig. 1-1 (a) General and (b) practical filter characteristics

In passband a filter provides flat frequency response with no gain or sometimes some gain while in stopband it attenuates the signal. All the three regions specifying the characteristics of a filter is shown in Fig.1-1[6].

The presence of transition band shows that movement through passband to stopband is not abrupt. This band must be very narrow which also mean higher selectivity of a filter. The ripples in stopband are also very significant as in this band attenuation must be large enough to suppress the interferer to well below the signal level. In Fig. 1-1(b) the attenuation is degraded in between ?? and ?? because of the presence of the ripples in stopband.

The "flatness" in passband of a filter is classified as amount of "ripples" in its magnitude characteristics curve. The large amount of ripples degrades the frequency contents of the signal. In Fig.1-1(b), the signal frequencies between ?? and ?? are attenuated while those of ?? and ?? are amplified.

1.2 CLASSIFICATION OF FILTERS

The filters are classified on the basis of different criteria. The criteria may be the components used to implement the filter or their frequency characteristic.

1.2.1 Classification of filters on the basis of frequency characteristics

This classification is done on the basis of frequency band that a filter "passes" or "rejects". There are generally four types of filters [5]:

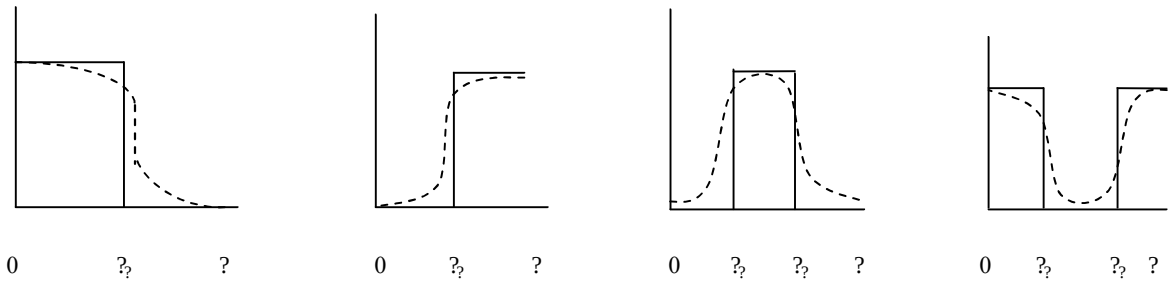
i) Low Pass Filter:- The filter which passes the low frequency components and rejects higher frequency components is known as low pass filter. The passband of low pass filter extends from ?= 0 to ? ? ?? where ?? is known as a cut off frequency (Fig. 1-2(a)).

ii) High Pass Filter:- It has the complementary frequency response that of low pass filter and its stopband extends from ?= 0 to ? ? ??. Its passband extends from ?? to infinity (Fig. 1-2(b)).

iii) Band Pass Filter:- This filter allows components that come only between a particular band from ?? to ?? while rejects all signals out of that band (Fig. 1-2(c)).

iv) Band Stop filter:- It has the reverse characteristics as that of band pass filter. It stops the components of a particular band from ?? to ?? and passes all other (Fig. 1-2(d)).

The frequency characteristics of all mentioned filters are shown in Fig.1-2. Besides these filters, there is one more filter known as "All pass filter" or delay equalizer which does not affect the magnitude response but alters the phase characteristics of a system.

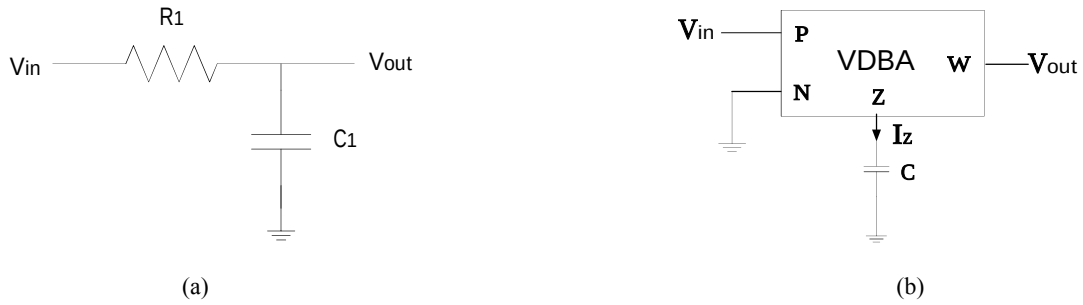


(a) Low Pass (b) High Pass (c) Band Pass (d) Band Stop

Fig. 1-2 Frequency characteristics of all basic filters. Solid lines: ideal characteristics; dashed lines: real characteristics

1.2.2 Classification of filters on the basis of components used in their implementation

This classification is concerned about the implementation of filters by "passive" and "active" components [5]. The filter realized by resistors, capacitors and inductors are known as "Passive filter" while those which use transistors, Op-amp, OTA or any other active device along with passive components is known as "Active filters". Active filters have inherent advantage of additional gain which is provided by the active devices. The implementation of low pass filter via only passive components is shown in Fig.1-3(a) while the same implementation is done with active topology in Fig. 1-3(b).



(a) (b)

Fig. 1-3 (a) Passive and (b) Active Realization of a low pass filter.

Passive filters do not use any amplifying devices which make them suitable for high frequency operation as there is no problem of finite gain bandwidth associated with every active device. Also there is no need to use any power supplies because of the absence of amplifying device. These filters are also applicable where large amount of current or voltage is needed at output unlike the active filters in which output voltage and current is limited by supply voltages and slew rate limitations. Along with so many advantages, passive filters have some major disadvantages. These include bulky size of inductor, absence of additional gain, problems associated with desired input and output impedances and highly time consuming tuning process.

Active filters find wider applications than passive filters, especially for low/medium range, because they are suitable for monolithic integration (as inductors are not used) which makes them compact in size and weight. It uses active devices which can provide any desirable gain unlike passive filters. Active filters can have desired input and output impedance levels. Different active devices provide flexibility in terms of input and output impedances as per the requirements of applications (either voltage mode or current mode or mixed mode signal processing). Though the operating range of frequency is limited by the gain bandwidth product of an active device, within that range active filters show more accuracy than passive filters. Noise problems associated with active devices can be minimized by using low noise amplifier (LNA).

1.2.3 Classification of filters on the basis of Structures

Filters can also be classified broadly in two categories on the basis of structure; variable structure filter and fixed structure filter. A short description on these filters is as follows:

A) Variable Structure Filter: Those filters in which interchanging of components (RC-CR Transformation) change the filter response (i.e. low pass to high pass and high pass to low pass etc.) come under the category of variable structure filters. The famous Sallen-Key filter [7] as shown in Fig. 1-4 is a variable structure filter.

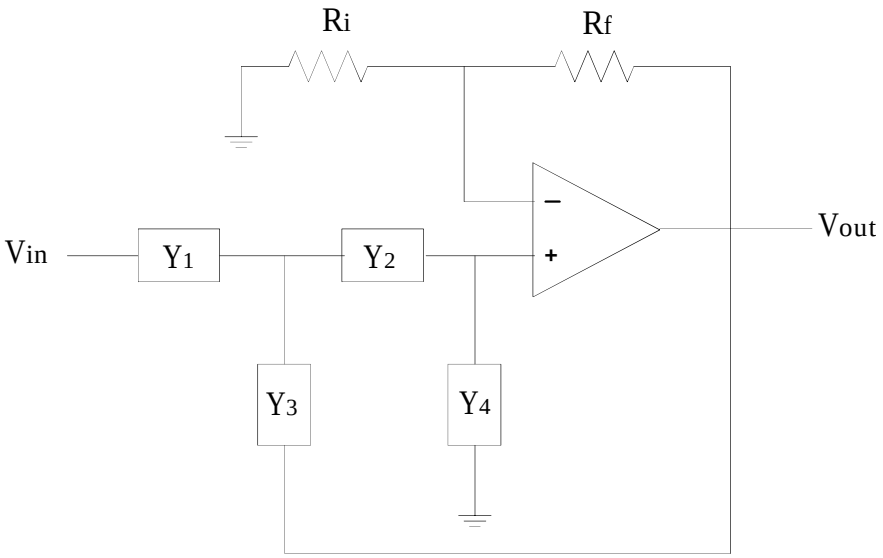


Fig. 1-4 General form of Second Order Sallen Key Filter [7]

A routine analysis of the circuit depicted in Fig. 1-4 shows that

$$\frac{?_{???}}{?_{??}} ? \frac{?_{?}?_{?}?_{?}}{?_{?}?_{?} ? ?_{?}??_{?} ? ?_{?} ? ?_{?}?? ?_{?}?_{?}?? \blacksquare ?_{?}?} \qquad ??.??$$

Where $?_{?} ? ? ? ?\frac{?_{?}}{?_{?}}?$??.??

Now if we put $?_{?} ? ?_{?} ? \frac{?}{?}$ and $?_{?} ? ?_{?} ? ??$ in Eq. (1.1) then we obtain

$$? ??? ? \frac{?_{?}}{?^{?}?^{?}?^{?} ? ????? \blacksquare ?_{?}?? ?}$$

$$? \frac{?_{?}?^{?}_{?}}{?^{?} ? ?\frac{?_{?}}{?}??? ?^{?}_{?}} \qquad ??.??$$

which is a standard second order low pass transfer function having following parameters:

i) Natural frequency $?_{?} ? \frac{?}{??}$ and ii) Quality Factor $? ? \frac{?}{???_{?}}$

Now if we interchange capacitors and resistors i.e. if we put $?_{?} ? ?_{?} ? ??$ and $?_{?} ? ?_{?} ? ? ? \frac{?}{?}$ in Eq. (1.1) then we obtain

$$? \; ??? \; ? \; \frac{?_{?}?^{?}}{?^{?} \; ? \; ?? \; ?_{?}?? \; ? \; ? \; ? \; ?_{?}^{?}} \qquad ??.??$$

Which is a standard second order high pass transfer function having natural frequency $?_{?} \; ? \; \frac{?}{??}$.

B) Fixed Structure Filters: Generally all universal filters (a single filter structure used to obtain all type of frequency response) come under the category of fixed structure filters. In these filters, components are not changed. On the basis of input and output ports these structure can be sub classified in following categories:

i) Single Input Multiple Output (SIMO) Structure: This kind of structure has a single input but outputs are taken at different parts of the circuit which shows different frequency characteristics. A well known state variable or KHN Biquad filter [8] as shown in Fig. 1-5 is an example of SIMO filter.

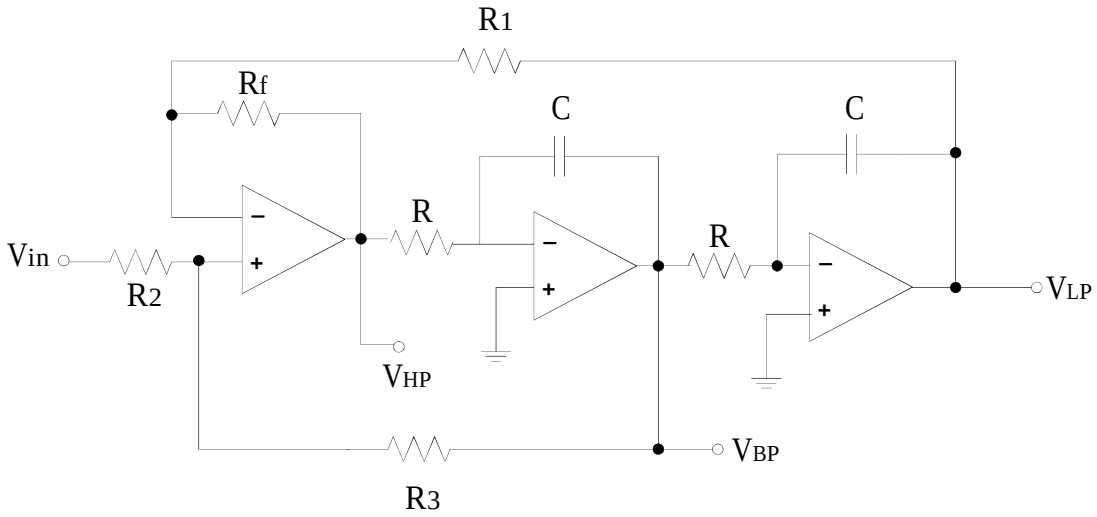


Fig. 1-5 Op-amp based KHN Biquad Filter (SIMO Structure) [8]

ii) Multiple Input Single Output (MISO) Structure: This kind of structure has multiple inputs but output is taken at a single node. A CFOA based universal filter [9] as shown in Fig. 1-6 is an example of MISO structure.

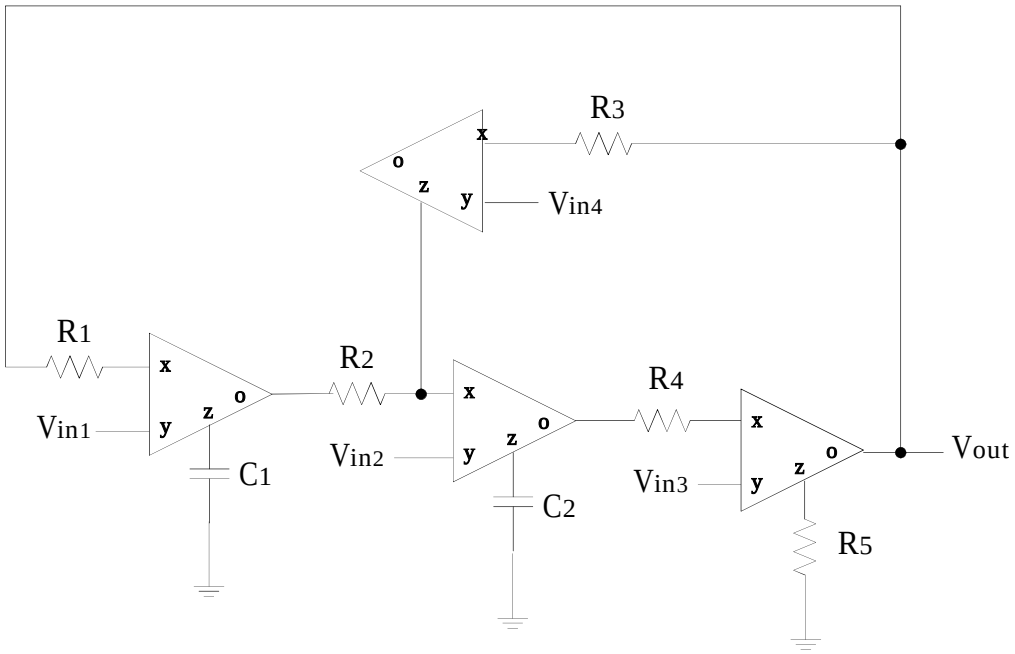


Fig. 1-6 CFOA based universal Filter (MISO Structure) [9]

iii) Multiple Input Multiple Output (MIMO) Structure: In this configuration, multiple inputs are applied and outputs are also taken at multiple nodes. MIMO structures show a distinct frequency characteristic for each input and output combination. A CDTA based universal filter [10] is shown in Fig. 1-7 which is an example of MIMO structure.

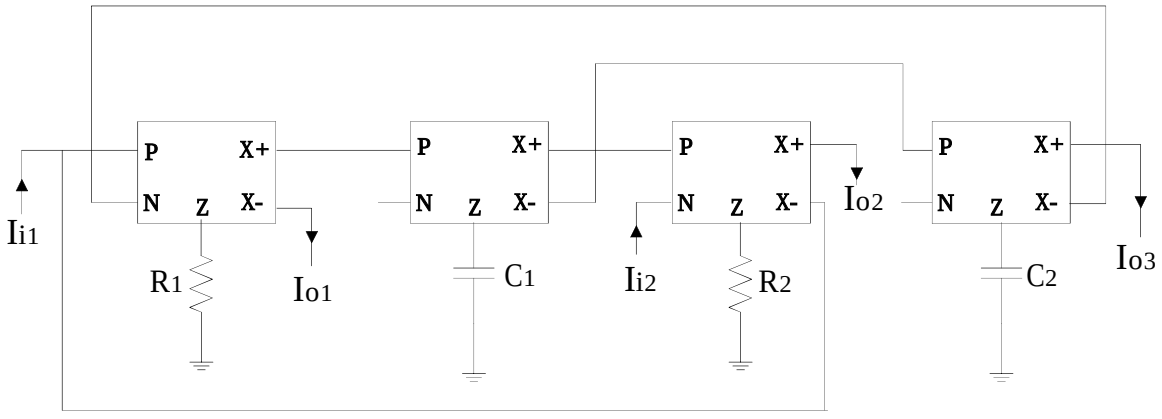


Fig. 1-7 CDTA based universal Filter (MIMO Structure) [10]

1.3 CHARACTERIZATION OF FILTERS

Filters can be classified on the basis of their orders i.e. first order, second order and higher order filters. These different order filters can be characterized as follows:

1.3.1 Specifications of First order Filters

A first order filter can be specified on the basis of two parameters; gain and cut off frequency. The standard first order transfer function is given as:

$$H(s) = \frac{a_1 s + a_0}{s + b_0} \qquad (1.5)$$

Where the values of a_1 and a_0 determine the filter response (i.e. low pas, high pass etc.) and b_0 represents the cut off frequency. The standard low pass filter transfer function can be obtained by setting $a_1 = 0$ in Eq. (1.5). Thus

$$H_{LP}(s) = \frac{a_0}{s + b_0} \qquad (1.6)$$

Similarly the high pass output can be obtained by putting $a_0 = 0$ in Eq. (1.5). Thus

$$H_{HP}(s) = \frac{a_1 s}{s + b_0} \qquad (1.7)$$

Hence any first order filter is characterized by its gain and cut off frequency.

1.3.2 Specifications of Second order Filters:

Second order filter are also known as Biquads. A standard second order filter transfer function can be written as

$$H(s) = \frac{a_2 s^2 + a_1 s + a_0}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \qquad (1.8)$$

Where the constants a_2, a_1 and a_0 determine the type of filter response and ω_0 and Q represents the natural frequency (pole frequency) and quality factor of the filters respectively. Thus second order filter can be specified with three parameters; gain, natural frequency and quality factor.

1.3.3 Specifications of Higher Order Filters:

In general, an n^{th} order transfer function is given as

$$H(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2} + \cdots + b_M z^{-M}}{1 + a_1 z^{-1} + a_2 z^{-2} + \cdots + a_N z^{-N}} \qquad (1.3)$$

where N is the order of filter. For a stable response the required condition is N≥ M. Higher order filters are those in which N > 2. The higher order filters can be specified in terms of following parameters:

i) Maximum variation allowed in passband transmission: δ_1

ii) Passband edge: ω_p

iii) Minimum attenuation required in stopband: δ_2

iv) Stopband edge: ω_s

All these parameters for low pass and band pass response is shown in Fig. 1-8 and 1-9 respectively.

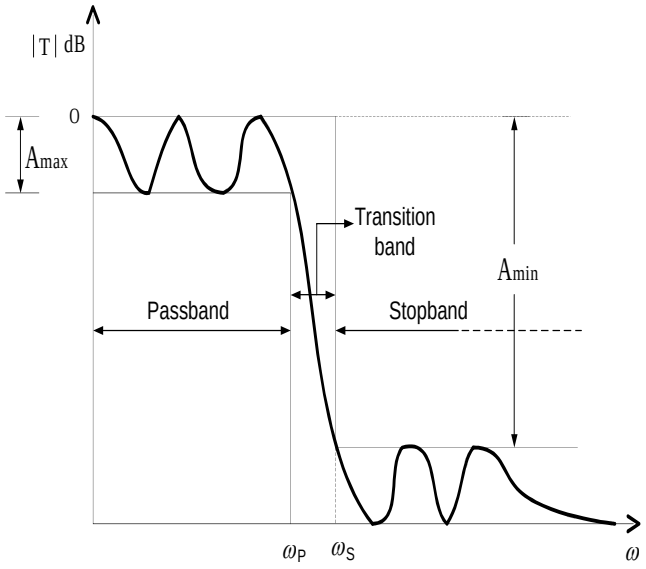


Fig. 1-8 Filter Specification for Low Pass Filter [8]

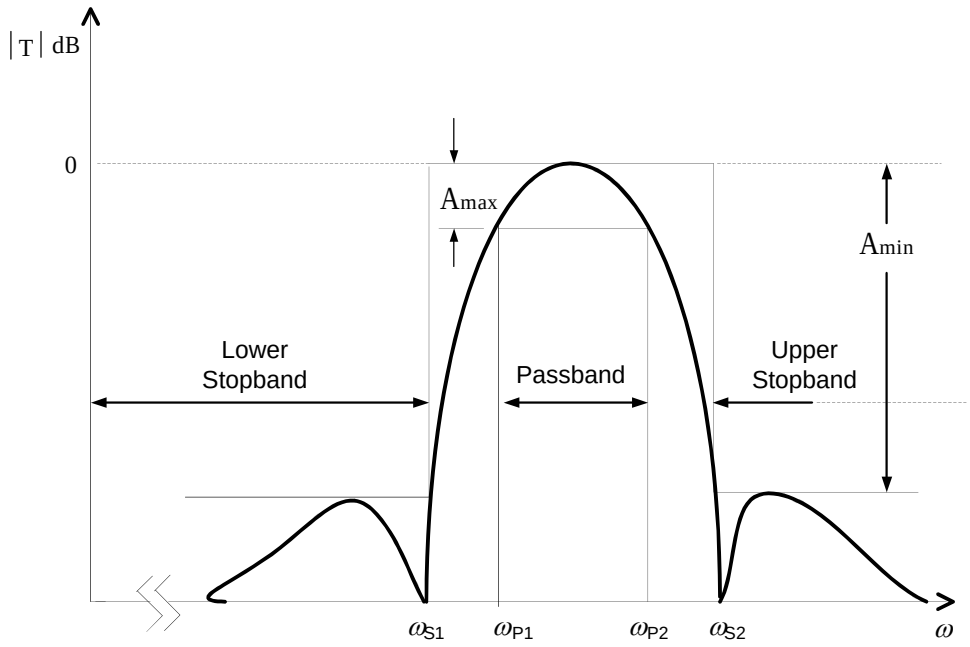


Fig. 1-9 Filter Specification for Band Pass Filter [8]

1.4 DESIGN ISSUES IN ACTIVE FILTER DESIGN

The first active *RC* filter was proposed around more than seventy years ago in which vacuum tubes were used as active elements. Since then, there have been great advancement in active filter design. A large amount of literature is available on the design of active filters [5, 7, 8]. Even today this design area is of great interest as an analog designer has to face several design issues while implementing active filters. These issues are sensitivity considerations, inductor simulation, frequency limitations of active device used, higher order filter implementations and noise effect etc.

Sensitivity of transfer properties with parameter variations is a major issue in active filter design [9]. The elements used in filter design are found highly sensitive to various parameters which degrade its performance. Several methods are introduced in open literature to reduce this problem such as use of multiple feedback and reactance ladder filter (while replacing inductor with its active counterpart) etc.

The trend in industry is to design active "inductorless" filters. Active filters are compatible with modern microelectronics system where considerations of size and weight make the use of

inductor prohibitive. In low frequency applications, active filters are implemented in fully integrated monolithic form which precludes the use of inductors.

Several active devices used for filter design have certain frequency limitations. The gain of active devices is not constant over all range of frequencies and it reduces as the frequency increases (after some order of MHz). This frequency dependence limits the range of operation, thus these filters are not designed for microwave frequency.

Higher order filters include filters having order more than two. Higher order filters can be designed simply by cascading second and/or first order filter but as cascading increases several issues like sensitivity, noise effect of each stage etc come into picture. To deal with these issues, deign of higher order filters are done on the basis of several approaches like multiple loop feedback approach [10], topological simulation, operational or leapfrog approach [5] and wave active approach [8].

Noise effect on filter performance plays an important role as dynamic range of active filter and effectiveness with which a signal can be recovered from a noisy background is solely dependent on the output noise of filter itself.

All the above issues must be considered in designing the active filters to obtain the desired results.

1.5 ORGANIZATION OF THE DISSERTATION

This dissertation is organized in 6 chapters.

Chapter-2 is about various methods for designing higher order filters. It covers the basic introduction of all three approaches- cascade approach, multiple loop feedback approach and LC ladder simulation approach used for designing higher order filters. Various ABBs used for designing active filters based on wave approach are discussed in Chapter-3. In Chapter-4 basic concept of wave active filter is presented and a wave active filter based on voltage differencing buffered amplifier (VDBA) is designed in chapter 5. The thesis is concluded in Chapter-6.

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CHAPTER 2

HIGHER ORDER FILTER REALIZATION

Higher order filters generally refer to the filters having order greater than two. In most cases the selectivity provided by second order filter is not sufficient. So higher order filters are designed to meet the stringent selectivity requirement in several places like instrumentation, communication system, and many other application areas [1], [2]. There are several methods available to design higher order filters as shown in Fig. 2-1.

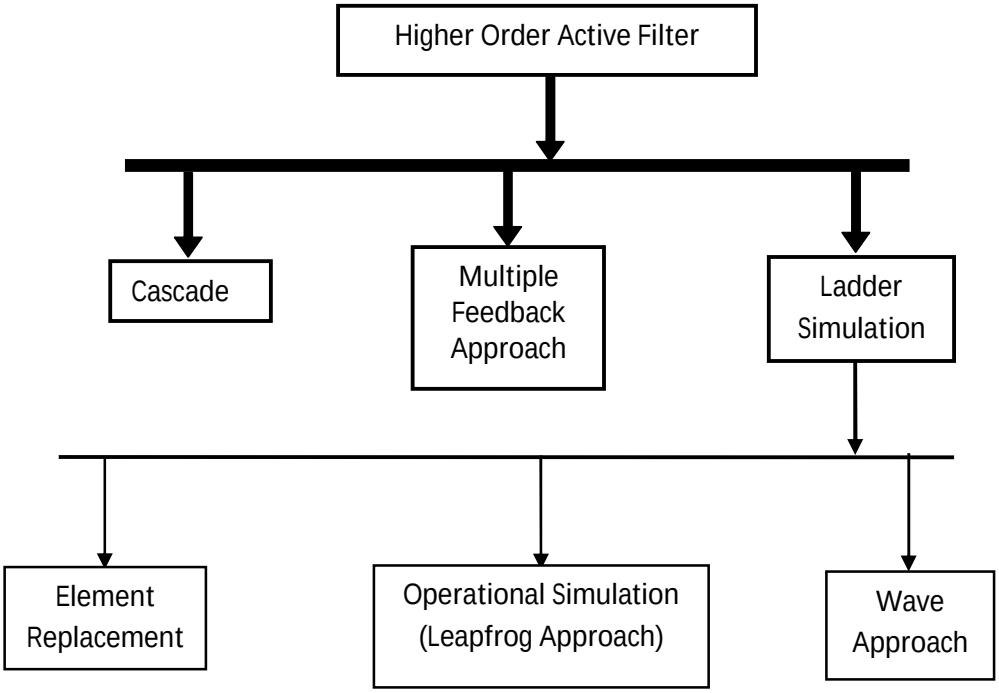


Fig. 2-1 Different approaches to design higher order active filters

In the following we present a brief introduction of all these techniques to design higher order active filter.

2.1 CASCADE DESIGN

In cascade design techniques, higher order filters are obtained simply by cascading second and first order (for odd order) filters. Higher order transfer function H(s) is factored in terms of second and/or first order transfer function. This is the simplest technique to realize higher order filters and used very frequently in industry. This approach offers several advantages [1] - [3]:

(a) It is easy to implement as all that is needed to design is connecting second and/or first order sub-section in cascade.

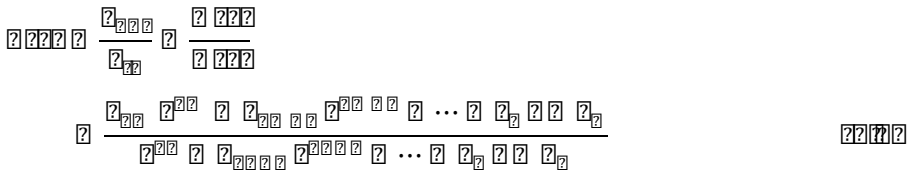
(b) It is simple, reliable and efficient in its use of devices as only one active device per pole pair is required.

(c) Cascaded filter is easy to tune as each biquad is responsible for only one pole pair and zero pair.

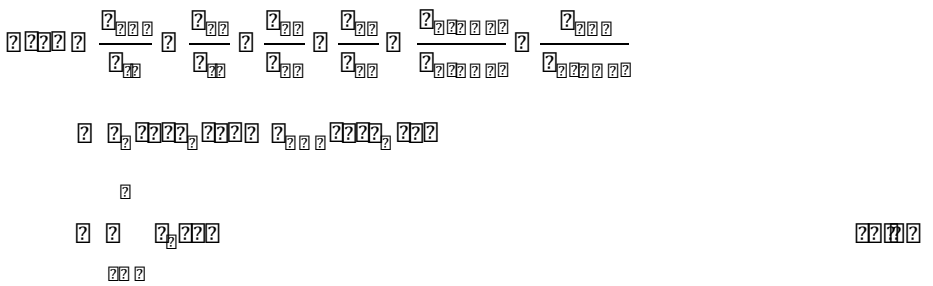
(d) Design methodology is general as any arbitrary transfer functions can be realized.

The major disadvantage of cascaded filter is low sensitivity to parameter variation when the order of filter exceeds to eight [1].

Now let us take a higher order transfer function as



Where degree of transfer function is assumed to be even so that all factored terms can take the standard biquad forms. Even if the degree is odd one of the cascaded sections will be first order section. Also the coefficient a_{0}=1 can be taken without loss of generality as it is always possible to divide *N(s)* and *D(S)* by a_{0} . Now the transfer function can be factored as



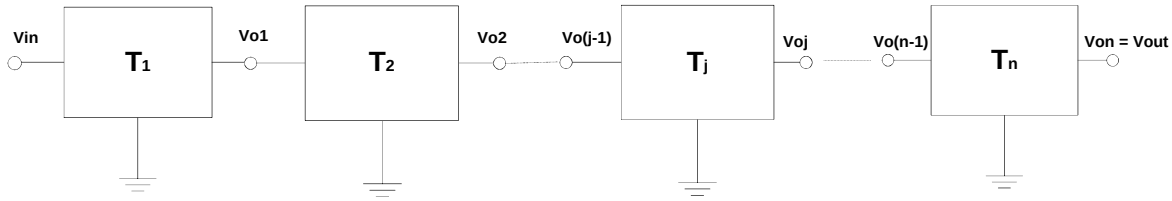


Fig. 2-2 Cascade connection of biquad sections to realize n^{th} order filter [1]

Eq. (2.2) can be represented in pictorial form as shown in Fig. 2-2. All the factored second order terms of the transfer function is connected in cascaded form. Now the remaining work is to realize each biquad section to obtain the complete higher order filter. As all terms of Eq. (2.2) have even degree of *N(s)* and *D(s)*, thus they can be factored as second order pole zero pair as following:

$$\frac{\prod_{i=1}^{n/2}(a_{2i}s^2+a_{1i}s+a_{0i})}{\prod_{i=1}^{n/2}(b_{2i}s^2+b_{1i}s+b_{0i})} \qquad (2.3)$$

The design process of Eq. (2.3) is straightforward and quite simple as ultimately the complete transfer function is now divided into standard biquad section. Yet there are some factors to be considered in cascaded design [1]-[3]:

(i) It must be determined which zero is assigned to which pole to form

(ii) The ordering of different section i.e. which section will come first and which will second and so on so forth is to be determined.

(iii) What will be the gain of each section?

Theoretically, answers to all the above questions are arbitrary as the total transfer function is a multiplication of all But in practical scenario all these questions must be dealt carefully as voltage available at the output of any active device (for example Op-amp) is limited by its slew rate besides DC biasing. Thus it is important to be concerned about the large voltage developed at any frequency at certain internal nodes of the circuit. If op-amps are over driven or

saturated they behaves like non-linear element and cause harmonic and intermodulation distortion which ultimately degrade filter performance.

The other reason that affects the answers of the above three mentioned factor is the electrical noise. Thus it must be ensured that signal at any node stay large enough to noise produced by random movements of electrons. Thus to optimize overall dynamic range (the difference between largest and smallest signal that a circuit can process without distortion) there are some rules of thumb [3]:

Rule (1) Place the zeros to that pair of poles which are closest to them.

Rule (2) All sections must be cascaded in the increasing value of Q.

Rule (3) Distribute the gains equally among the all sections.

2.2 MULTIPLE LOOP FEEDBACK (MLF) APPROACH

The major disadvantage of cascade design approach for higher order filter implementation is its low passband sensitivity to parameter variations, when order of the filter is more than eight [1]. Another approach used for the design of higher order filters is multiple loop feedback approach which shows lesser passband sensitivity compared to cascade approach. Similar to cascade approach, the higher order transfer function is decomposed into second order subsections in MLF approach but these subsections are interconnected via some sort of feedback topologies which introduce coupling between the subsections to reduce overall sensitivity [2]. This approach is also known as Coupled Biquad method.

The modular structure property of cascade approach is retained in MLF approach along with an excellent sensitivity performance. All biquad sections □□□of Eq. (2.3) are arranged in a certain feedback approach to realize overall higher order transfer function and on the basis of these arrangements there exist following 7 types of MLF topologies ([4] and references cited there):-

i) Follow the Leader Feedback (FLF): In this topology all biquad sections are connected in such a way that output of each section is fed back into a summer at the input of a filter. For the filter of order 6, the FLF topology is shown in Fig. where □ are second order biquad sections. The topology shown in Fig. 2-3(a) is for all poles transfer function. For arbitrary transmission zeros the output of each biquad can be fed forward into another summer placed at filters output.

ii) Primary Resonator Block (PRB): If quality factor Q_i of all biquad sections of FLF are made equal the resulting topology is known as Primary Resonator Block (PRB) which is shown in Fig. 2-3(b) for the filter of order 6.

iii) Shifted Companion Form (SCF): In this topology the first biquad section is different from rest of the sections which are identical as shown in Fig. 2-3(c).

iv) Leapfrog approach (LF): This topology is shown in Fig. 2-3(d). As every loop contains two sections; thus inverting and non-inverting section must be on alternate basis to keep overall gain negative thus system stable. All sections except first and last i.e. Q_1 and Q_n are lossless ($Q= \infty$) as it is derived from the classical resistively terminated LC ladder structure. This approach is similar to SFG representation for LC ladder so it will be discussed in more details in next section.

v) Modified Leapfrog approach (MLF): If in LF topology the internal biquad sections are made lossy instead of lossless then it is known as Modified leapfrog approach. This topology is shown in Fig. 2-3(e).

vi) Inverse Follow the leader Feedback Approach (IFLF): This topology is shown in Fig. 2-3(f) which is quite similar to FLF topology but it has last biquad section as inverting section. The dynamic range obtained for IFLF structure is found better than FLF.

vii) Minimum Sensitivity Feedback (MSF): This is the last topology of multiple loop feedback schemes which is shown in Fig. 2-3(g) for the filter of order 6.

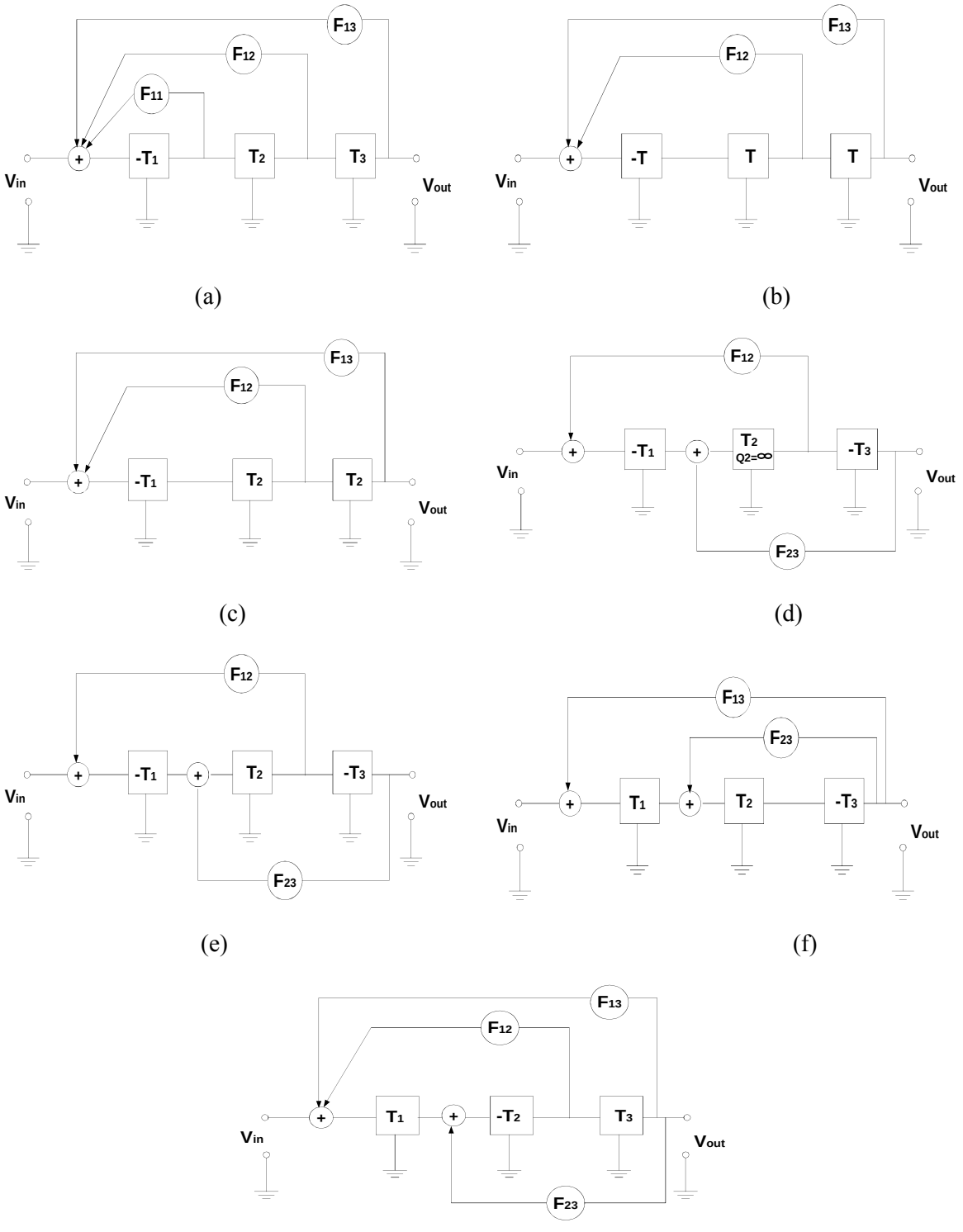


Fig. 2-3 Multiple Loop Feedback topologies with all pole band pass realization (a) FLF (b) PRB (c) SCF (d) LF (e) MLF (f) IFLF (g) MSF [4]

2.3 LADDER SIMULATION APPROACH [3]

It is well known fact that filters architecture of resistively terminated passive LC ladders show very low sensitivity to parameter variations. Also there is a large amount of information (like design tables) is available for the design of LC ladder. The major disadvantage of LC ladder realization is to realize inductor which is bulky and heavy except for higher frequency operations. Also inductors are hard to construct in monolithic form that is used in microelectronic circuits. Thus there is an approach which retains the two positive properties: low sensitivity and ample amount of design information, of LC ladder and replaces the inductor with its active counterpart. This LC simulation approach is broadly subdivided into three parts:

I) Element Replacement

II) Operational Simulation

III) Wave Active Filter approach.

The major disadvantage of this LC ladder technique is that a passive LC prototype exists before its active simulation can be done. Also the number of active components used for active realization is found larger than usual. As Wave Active filter approach is main part of this dissertation, it will be discussed in detail in chapter 4. For now, only first two approaches of LC Ladder simulation is described in the following section.

2.3.1 Element replacement

The primary focus of this technique is on replacing 'inductor" of a LC ladder with its active counterpart. Inductors are replaced with the active circuits whose input impedance resembles to be inductive. There are various ways to simulate an inductor; some of them are as follows:

i) General Impedance Converter (GIC): As the name suggest, GIC is used to realize various input impedance depending on the components chosen for its realization. An Op-amp based GIC is shown in Fig. 2-4.

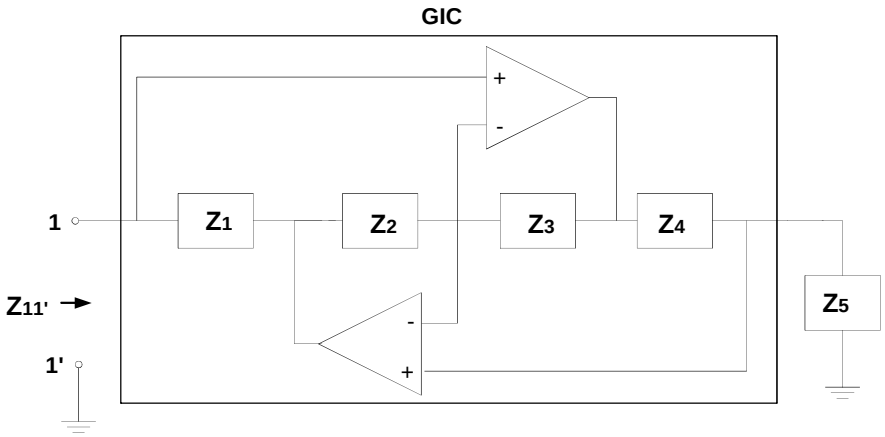


Fig. 2-4 General Impedance Converter (GIC) circuit

The regular analysis of the circuit shown in Fig. shows that the input impedance of GIC is

$$Z_{11'} = \frac{Z_1 Z_3 Z_5}{Z_2 Z_4} \qquad (2.1)$$

Now if $Z_1 = Z_2 = Z_3 = Z_4 = Z_5 = \frac{1}{sC}$ then ,

$$Z_{11'} = \frac{1}{sC} \qquad (2.2)$$

Thus the GIC circuit of Fig. realizes a grounded inductor. To obtain floating inductor two GIC of the Fig. 2-4 can be connected as shown in Fig. 2-5.

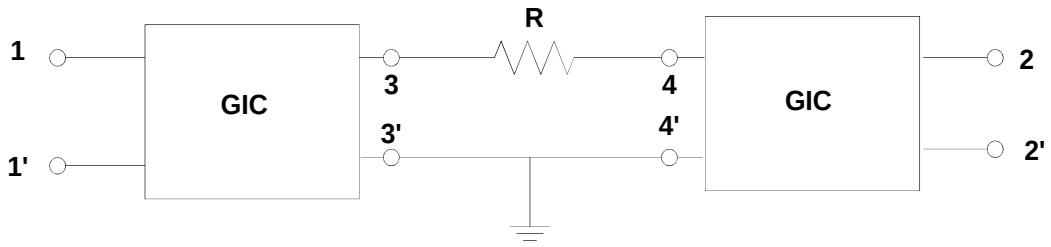


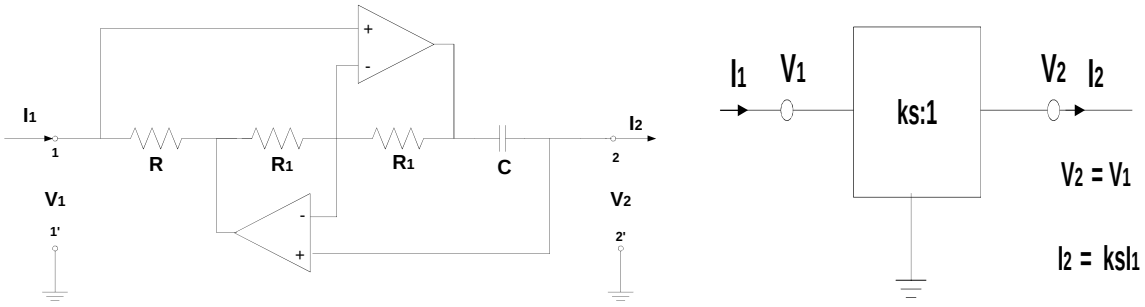
Fig. 2-5 Realization of floating inductor based on GIC

Now these grounded or floating inductors can be replaced with passive inductors in any LC ladder to realize higher order filters. Though this method of replacing passive inductor with GIC based active inductor is quite simple but it uses large number of active devices (two GIC for floating inductor which means four op-amps). Thus there are other methods as discussed below which overcome this problem by reducing the number of active blocks.

ii) Gorski-Popiel's Embedding Technique [2], [3]: The circuit based on GIC which is widely used for inductor simulation is shown in Fig. The regular analysis of the circuit shown in Fig. 2-6(a) shows that

$$\frac{V_1}{I_1} = sCR_1R \qquad (2.1)$$

Where CR_1R is a time constant which characterize a GIC.



(a) (b)

Fig. 2-6 (a) Circuit diagram for GIC (b) symbolic representation of GIC

The relation between currents and voltages of the GIC input and output ports are:

$$V_2 = V_1 \quad \text{and} \quad I_2 = -sCI_1 \qquad (2.2)$$

The symbolic representation of GIC showing its port characteristics can be presented as shown in Fig. 2-6(c).

If a resistance R is connected at the output of GIC circuit shown in Fig. 2-6(b) then it represents an inductor with $L = kCR$ as shown in Fig. 2-7.

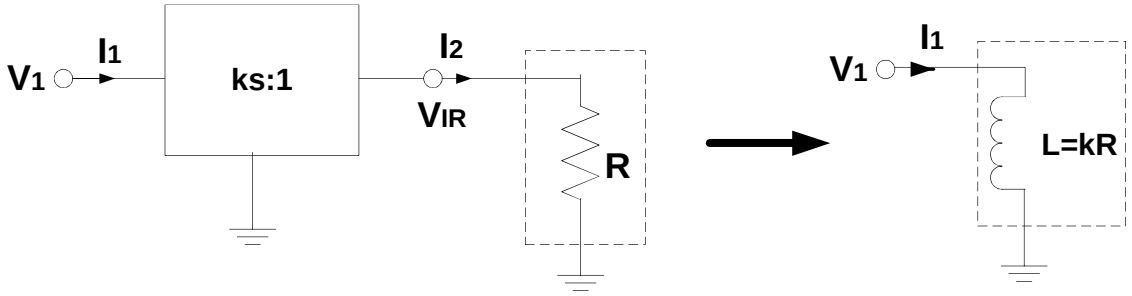


Fig. 2-7 Conversion of a Resistance into an Inductor

In this approach, first all inductor subnetworks are separated from a LC ladder and then it is replaced by resistive network followed by GIC. It can be shown that extending this approach, any subnetwork having (n+1) terminals consisting of inductors can be simulated by using only n GIC and resistive network topology. The above statement is clarified with the following example shown in Fig. 2-8.

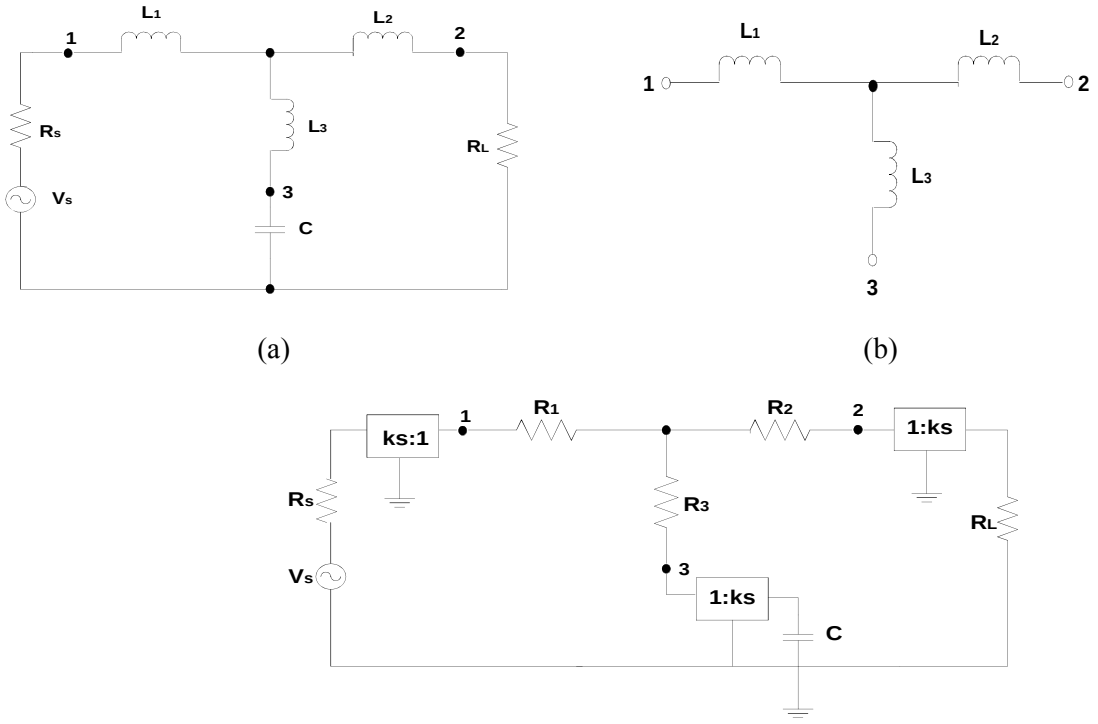


Fig. 2-8 (a) LC Ladder network (b) Subnetwok of inductors (c) simulated LC ladder

The LC ladder and inductor subnetwork is shown in Fig. 2-8 (a) and (b) respectively. It can be simulated with GIC followed by resistive network as shown in Fig.2-8(c). Here only three GICs are used instead of five (each floating inductance requires two GICs and one GIC for grounded L_3 if its position is exchanged with C to avoid its being floating).

iii) Bruton's FDNR Technique: This technique is based on the scaling of inductive impedance sL by $\frac{1}{s}$ by which a resistance with same value, R=L is obtained. Thus inductance can be eliminated from the ladder circuit. But to keep transfer function same, all elements are scaled by $\frac{1}{s}$ which

leads the transformation of resistance *R* into capacitance of value [illegible] and capacitance *C* is transformed into a new element whose impedance on $j\omega$ is as follows:

[illegible] (2.5)

This is a real, negative and frequency dependent quantity. Hence this transformed element is called Frequency Dependent Negative Resistance (FDNR) and represented by D. Bruton's transformation of all circuit elements are shown in Table 2-1.

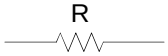
Element	Bruton transformed Elements
R 	C=1/R 
L 	R = L 
C 	D = C 

Table 2-1 Passive components obtained from the Bruton transformation

The realization of FDNR can be done by using GIC as shown in Fig. 2-9.

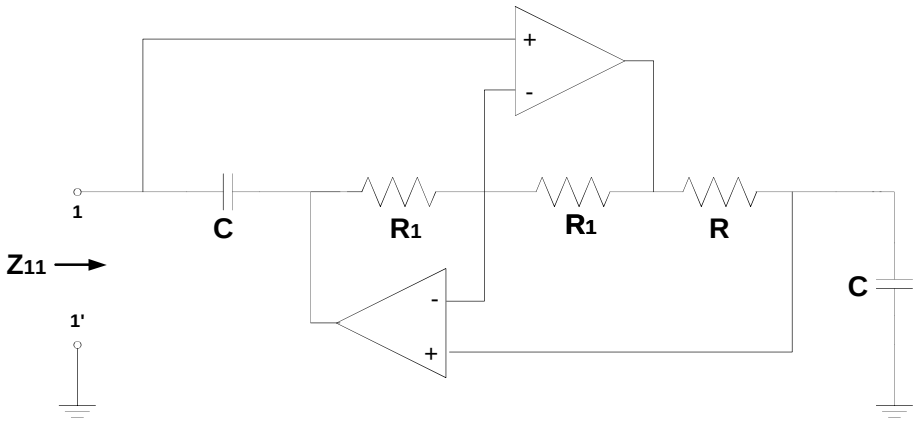


Fig.2-9 Circuit for Realization of FDNR with [illegible]

The routine analysis shows that the input impedance of the circuit of Fig. 2-9 is

$$Z_{in} = \frac{1}{sC_1} \rightarrow Z_{in}(s) = \frac{1}{sC_1}$$

Where $s = \sigma + j\omega$.

2.3.2 Operational Simulation

This is the second approach of simulating LC ladder circuits in which instead of simulating circuit elements, the operation of ladder is simulated. This approach can be explained by using following example. A ladder circuit is shown in Fig.2-10 in which voltage across the shunt branches and current through series branches are taken as state variables.

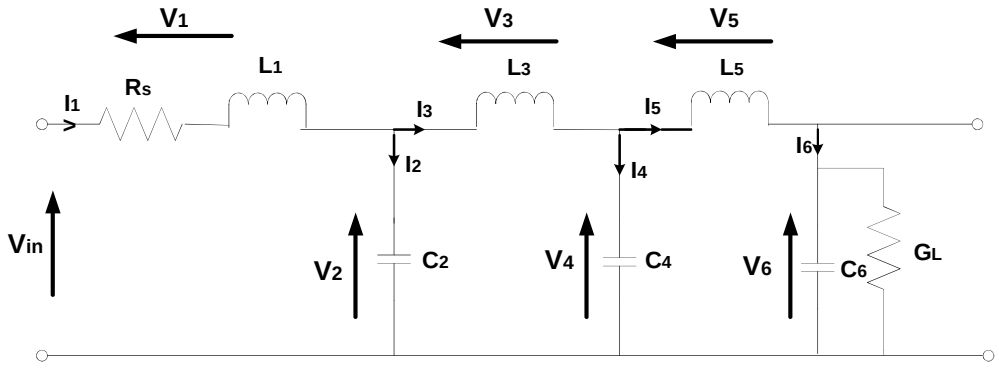


Fig. 2-10 A sixth order LC lowpass ladder

The ladder is expressed in terms of voltage and current relationship as follows:

$$I_1 = \frac{V_{in} - V_2}{R_s} \quad (2.10.1)$$

$$I_2 = \frac{V_2 - V_3}{sL_2} \quad (2.10.2)$$

$$I_3 = \frac{V_3 - V_4}{sL_3} \quad (2.10.3)$$

$$I_4 = \frac{V_4 - V_5}{sL_4} \quad (2.10.4)$$

$$I_5 = \frac{V_5 - V_6}{sL_5} \quad (2.10.5)$$

$$I_6 = V_6 G_L \quad (2.10.6)$$

Where $\alpha_1 = \frac{1}{Z_1 Z_2 + Z_1 Z_3 + Z_2 Z_3}$, $\alpha_2 = \frac{1}{Z_1 Z_2}$, $\alpha_3 = \frac{1}{Z_2 Z_3}$, $\alpha_4 = \frac{1}{Z_1 Z_3}$, $\alpha_5 = \frac{1}{Z_1 Z_2}$ and $\alpha_6 = \frac{1}{Z_1 Z_2 + Z_1 Z_3 + Z_2 Z_3}$ (2.11)

But as op-amp is used generally as an active block which is a voltage controlled voltage source so all current variables are multiplied by resistance *R* to obtain voltage variables as shown in following equations:

$$V_{1I} = Z_1 \overline{I_1} \rightarrow v_{1I} = Z_1 \overline{i_1} \quad (2.12.1)$$

$$V_2 = \frac{Z_2}{Z_1} V_{1I} \rightarrow v_2 = Z_2 \overline{i_1} \quad (2.12.2)$$

$$V_{3I} = Z_3 \overline{I_3} \rightarrow v_{3I} = Z_3 \overline{i_3} \quad (2.12.3)$$

$$V_4 = \frac{Z_4}{Z_3} V_{3I} \rightarrow v_4 = Z_4 \overline{i_3} \quad (2.12.4)$$

$$V_{5I} = Z_5 \overline{I_5} \rightarrow v_{5I} = Z_5 \overline{i_5} \quad (2.12.5)$$

$$V_6 = \frac{Z_6}{Z_5} V_{5I} \rightarrow v_6 = Z_6 \overline{i_5} \quad (2.12.6)$$

Where Z_{11} and Z_{12} are transfer functions which represents the ratio of two voltages. Also V_{1I} are represented as voltages of the form of v_{1I} where subscript 'I' is retained to remind that these quantities are transformed from currents in the circuits. To maintain the notation all other voltages are also represented in lower cases.

In op-amps, addition of two voltages is easier than subtraction. So the transfer functions of impedances Z_{11} are replaced by $\overline{Z_{11}}$. The same replacement can be done with Z_{12}. Now replacing Z_{12} by $\overline{Z_{12}}$ and keeping track of the minus signs, the Eqs. (2.12) can be modified as:

$$v_{11} = Z_{11} i_{11} + \overline{Z_1} i_{12} \quad (2.13.1)$$

$$\overline{Z_1} i_{11} + Z_{11} i_{12} + \overline{Z_{12}} i_{13} = \overline{Z_{12}} i_{14} \quad (2.13.2)$$

$$\overline{Z_{12}} i_{11} + Z_{11} i_{13} = \overline{Z_1} i_{14} \quad (2.13.3)$$

$$v_2 = \overline{Z_{11}} i_{11} - \overline{Z_{12}} i_{13} + Z_{12} i_{14} \quad (2.13.4)$$

$$v_{31} = Z_{31} i_{31} + \overline{Z_3} i_{32} \quad (2.13.5)$$

$$\overline{Z_3} i_{31} + Z_{31} i_{32} = \overline{Z_{31}} i_{32} \quad (2.13.6)$$

Now Eqs. (2.13) can be represented as in block diagram form as shown in Fig. 2-11 where all signals coming from current are placed in upper line. The block diagram of Fig. 2-11 can be redrawn as shown in Fig. 2-12 which again can be represented in the form of "Leapfrog" structure (Fig.2-13).

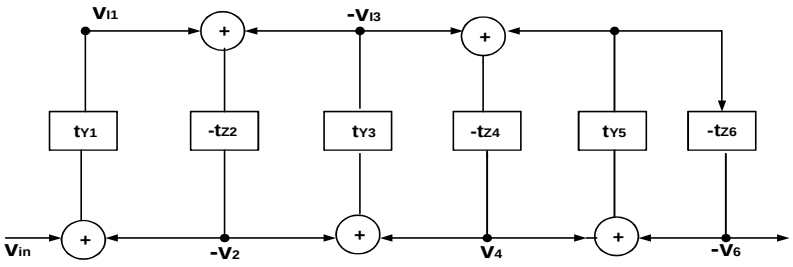


Fig. 2-11 Block diagram representation of Eq. (2.13)

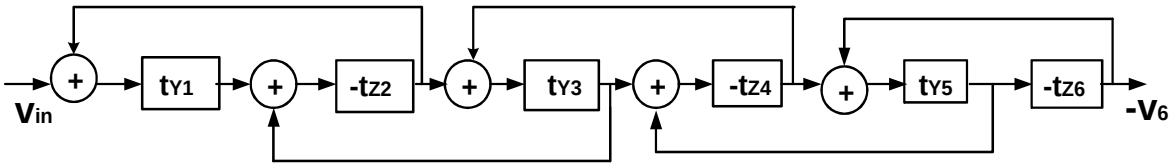


Fig.2-12 Block diagram redrawn from Fig. 2-11

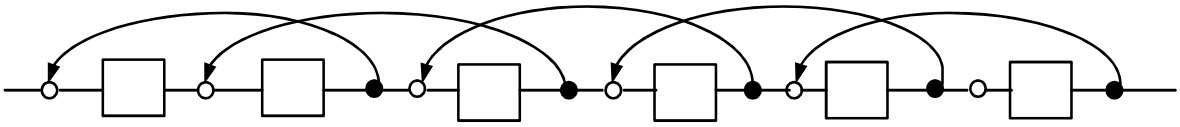
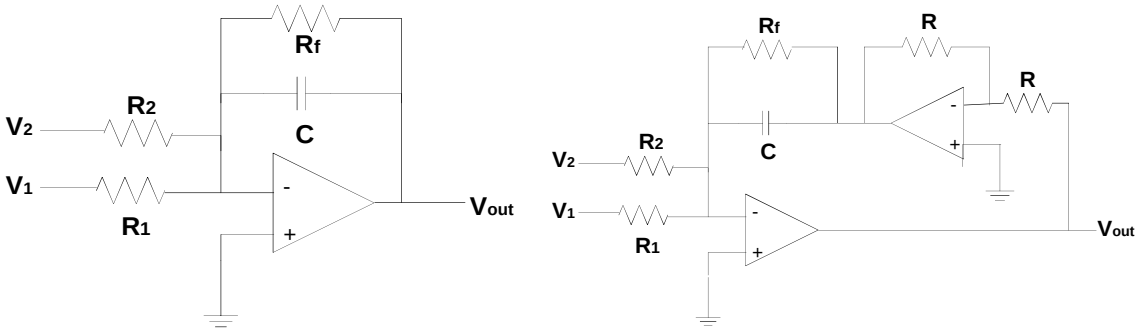


Fig.2-13 Leapfrog structure of ladder circuit

All the Eqs. of (2.13) represent the functional behavior of ladder circuit. To simulate these equations lossy and lossless integrators are required as $\frac{?}{??}$ and $\frac{?}{??}$ are lossy and rests are lossless integrators. Thus operational simulation of ladder circuit can be done by using inverting and non-inverting lossy/lossless integrators which integrates the sum of two voltages. Op-amp based inverting and non-inverting summing lossy integrators are shown in Fig. 2-14.



(a) (b)

Fig. 2-14 Summing lossy integrator (a) inverting configuration (b) non-inverting configuration

2.4 CONCLUSION

In this chapter the several methods of designing higher order filters such as cascade design, multiple loop feedback techniques and LC ladder simulation methods are discussed in brief. To achieve stringent requirement of sensitivity, LC ladder simulation technique is used as it shows the best result in terms of sensitivity performance among all the three methods. Two out of three techniques of LC ladder simulation i.e. element replacement and operational simulation methods are discussed in this chapter while the third technique i.e. wave approach will be discussed in details in chapter 4.

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4. LAKER, K.R., SHAUMANN, R., GHAUSI, M.S. Multiple-Loop Feedback Topologies for the Design of Low -Sensitivity Active Filters. IEEE Trans. On circuits and systems, vol. CAS-26, no.1, p. 1-21, 1979.

CHAPTER 3

ACTIVE BLOCKS USED FOR REALIZATION OF WAVE ACTIVE FILTER

As discussed in chapter 2, there is a method to realize doubly terminated LC ladder by active simulation known as Wave Active Filter which overcomes the shortcomings of other techniques; topological simulation and operational simulation. Conventional op-amps were used as an active blocks in realization of WAF [1]-[4]. A very large number of active building blocks have been introduced in literature for different applications in Analog Signal Processing. An excellent summary and classification of these blocks has been given in [5]. Many of those blocks have been used for realization of wave active filters. In this chapter we present a review of those blocks which have been used for realization of WAF.

3.1 OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

Operational Transconductance Amplifier (OTA) is a versatile block used in voltage mode as well as current mode applications. It is a differential amplifier whose output current is directly proportional to the difference of input voltages. Thus it acts as a Voltage Controlled Current Source (VCCS). The symbolic diagram of OTA is given in Fig. 3-1 [6]. The output current of OTA is given as:

$$i_{out} = g_m (v_{in1} - v_{in2}) \tag{3.1}$$

where g_m is a transconductance gain.

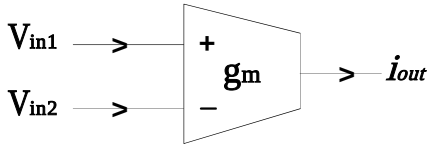

Fig. 3-1 Schematic symbol of Operational Transconductance Amplifier

Basic CMOS realization of OTA is given in Fig. 3-2. The output current for this case is

$$?_{???} ? \frac{?_?}{??_{??}??_?} ??_{??} \overline{?_{??}?}$$

$$? ?_? ??_{??} \overline{?_{??}?} \quad (3.2)$$

Where $?_? ? \frac{?_?}{??_?}$.

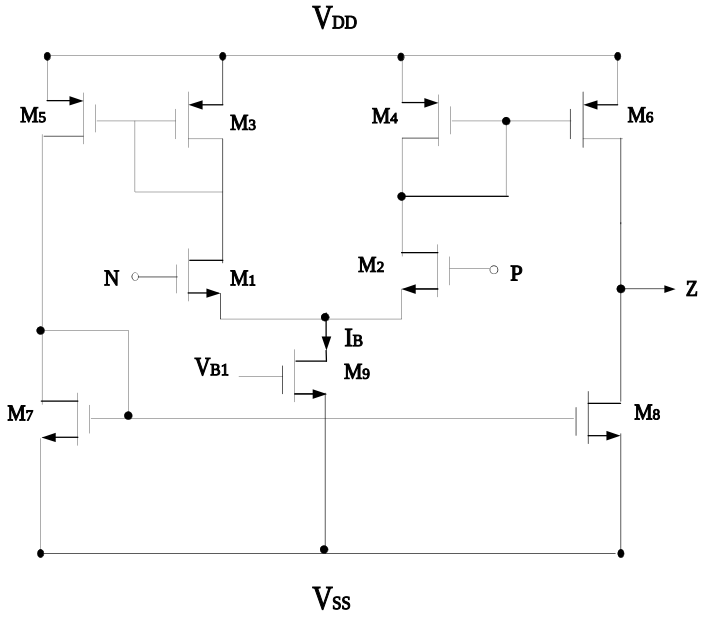

Fig. 3-2 CMOS Realization of OTA [30]

3.2 CURRENT FEEDBACK OPERATIONAL AMPLIFIER

CFOA is a novel active building block which offer wider signal bandwidth and higher linearity compared to conventional op-amps [7]-[10]. The functional block diagram of CFOA is shown in Fig. 3-3 and its terminal characteristics are defined as:

$$\begin{matrix} ?_? & ? & ? & ? & ? & ?_? \\ ?_? & ? & ? & ? & ? & ?_? \\ ?_? & ? & ? & ? & ? & ?_? \\ ?_? & ? & ? & ? & ? & ?_? \end{matrix} \quad (3.3)$$

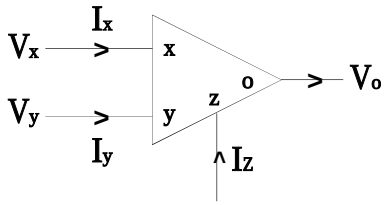

Fig. 3-3 Functional Block Diagram of CFOA

It is clear from the terminal characteristics of CFOA that it is comprised of a current conveyor of second generation along with a voltage buffer. It is also available in the form of IC AD-844.

3.3 DIFFERENTIAL VOLTAGE CURRENT CONVEYOR TRANSCONDUCTANCE AMPLIFIER

Differential Voltage Current Conveyor Transconductance Amplifier (DVCCTA) is a modified version of current conveyor in which input stage of a differential amplifier is followed by a transconductance cell.

The terminal characteristics of DVCCTA as shown in Fig. 3-4 are given as [11]-[13]:

$$\begin{bmatrix} ? \\ ? \\ ? \\ ? \\ ? \end{bmatrix} ? \begin{bmatrix} ? & ? & ? & ? & ? \\ ? & ? & ? & ? & ? \\ ? & ? & ? & ? & ? \\ ? & ? & ? & ? & ? \\ ? & ? & ? & ? & ? \end{bmatrix} \begin{bmatrix} ? \\ ? \\ ? \\ ? \\ ? \end{bmatrix} \tag{3.4}$$

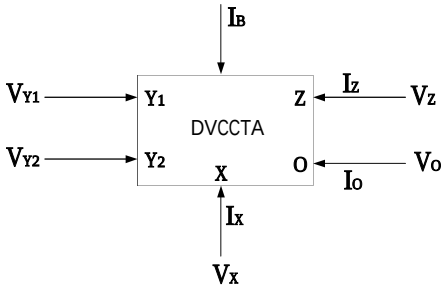

Fig.3-4 Schematic symbol of DVCCTA

The CMOS realization of DVCCTA is given in Fig. 3-5. The value of transconductance gain ?? from Z to O terminal is dependent on ?? by following relation:

$$?? \; ? \; ? \; ?? ?? ?? ?? ?? ?? ?? ?? ?? \qquad (3.5)$$

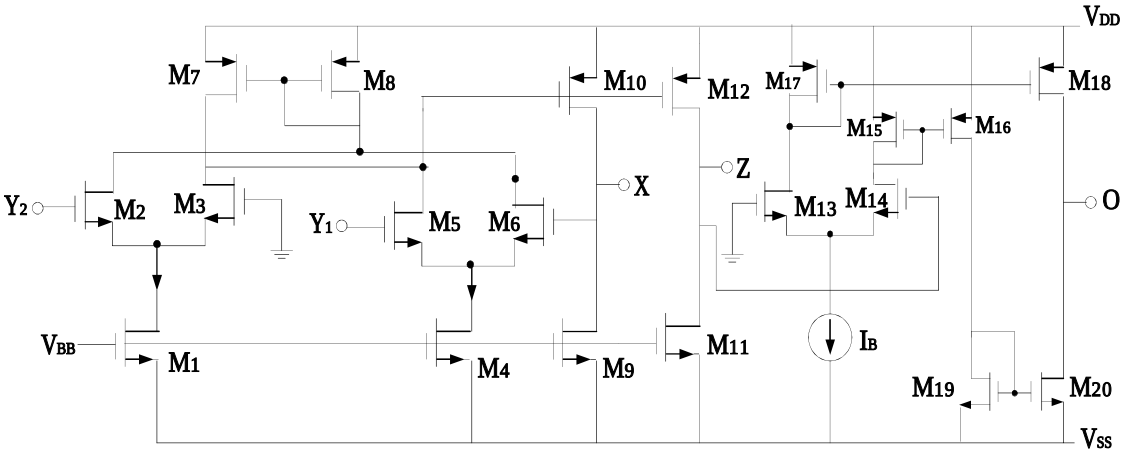

Fig. 3-5 CMOS Realization of DVCCTA [12]

3.4 DIFFERENTIAL VOLTAGE CURRENT CONTROLLED CONVEYOR TRANSCONDUCTANCE AMPLIFIER

Differential Voltage Current Controlled Conveyor Transconductance Amplifier (DVCCCTA) is based on DVCCTA. It comprised of differential amplifier, trans-linear loop and transconductance amplifier [14]-[15]. The symbolic representation of DVCCCTA is given in Fig. 3-6 and its port characteristics are represented by following matrix:

$$\begin{bmatrix} ?? \\ ?? \\ ?? \\ ?? \\ ?? \end{bmatrix} ? \begin{bmatrix} ? & ? & ? & ? & ? \\ ? & ? & ? & ? & ? \\ ? & ? & ?? & ? & ? \\ ? & ? & ? & ? & ? \\ ? & ? & ? & ?? & ? \end{bmatrix} \begin{bmatrix} ?? \\ ?? \\ ?? \\ ?? \\ ?? \end{bmatrix} \qquad (3.6)$$

where ?? is the intrinsic resistance at terminal X and ?? is the transconductance gain from Z to O terminal.

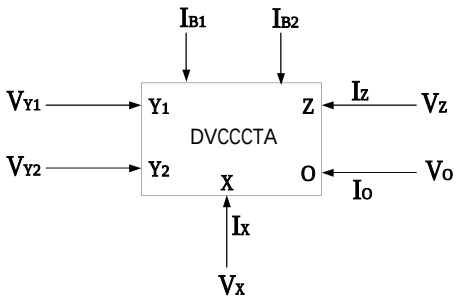

Fig. 3-6 Schematic symbol of DVCCCTA

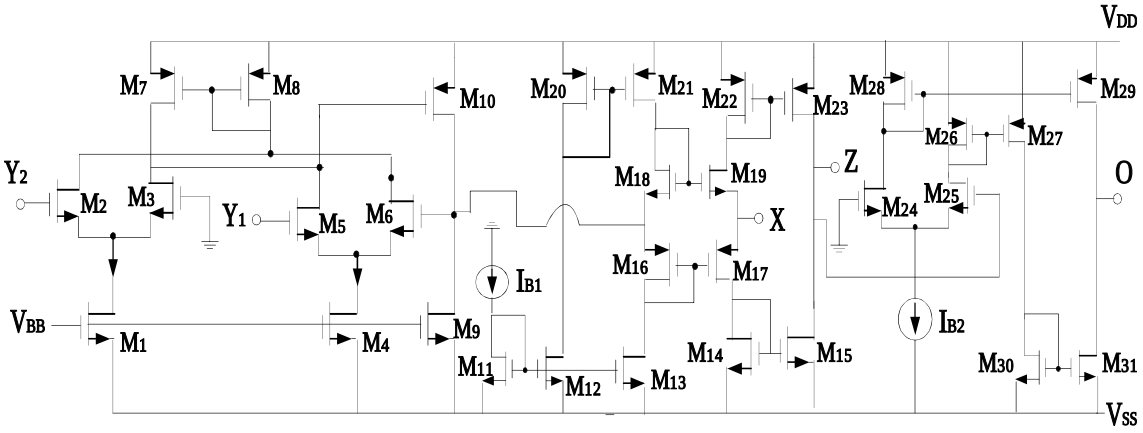

Fig. 3.7 CMOS Realization of DVCCCTA [15]

DVCCCTA can be implemented by using CMOS transistors as shown in Fig. 3-7. The values of ?? and ?? is dependent on bias currents ??? and ??? by following relations:

$$?_? \; ? \; ? \; ? \; ?_? \; ?_? \; ?^? \; ?_? ?_{???} ?_? \quad ? \quad ? \; ?_? \; ?_? \; ?^? \; ?_? ?_{???} ?_? \; ? \tag{3.7}$$

and

$$?_? \; ? \; ? \; ?_? \; ?_? \; ?^? \; ?_? ?_{???} ?_? \tag{3.8}$$

3.5 CURRENT CONTROLLED DIFFERENTIAL DIFFERENCE CURRENT CONVEYOR TRANSCONDUCTANCE AMPLIFIER

Current Controlled Differential Difference Current conveyor Transconductance Amplifier is new active building block which consists of current controlled differential difference current conveyor (CCDDCC) [16] as input block followed by a transconductance amplifier. It retains all the features of current controlled current conveyor transconductance amplifier (CCCCTA) [17] and differential voltage current controlled conveyor transconductance amplifier (DVCCCTA) [14] along with some special properties of differential difference current conveyor (DDCC) [18]-[20] such as easy implementation of differential and floating input circuits.

The symbolic representation and CMOS realization [21] of CCDDCCTA are depicted in Fig. 3-8 and Fig. 3-9.

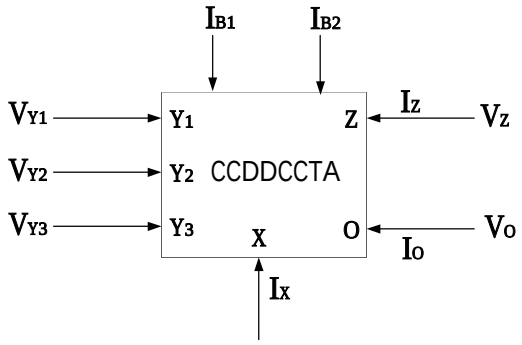

Fig. 3-8 Symbolic representation of CCDDCCTA

The ports of CCDDCCTA are characterized by following relation:

$$\begin{bmatrix} ? \\ ? \\ ? \\ ? \\ ? \\ ? \end{bmatrix} = \begin{bmatrix} ? & ? & ? & ? & ? & ? \\ ? & ? & ? & ? & ? & ? \\ ? & ? & ? & ? & ? & ? \\ ? & ? & ? & ? & ? & ? \\ ? & ? & ? & ? & ? & ? \\ ? & ? & ? & ? & ? & ? \end{bmatrix} \begin{bmatrix} ? \\ ? \\ ? \\ ? \\ ? \\ ? \end{bmatrix} \tag{3.9}$$

where (3.10)

and (3.11)

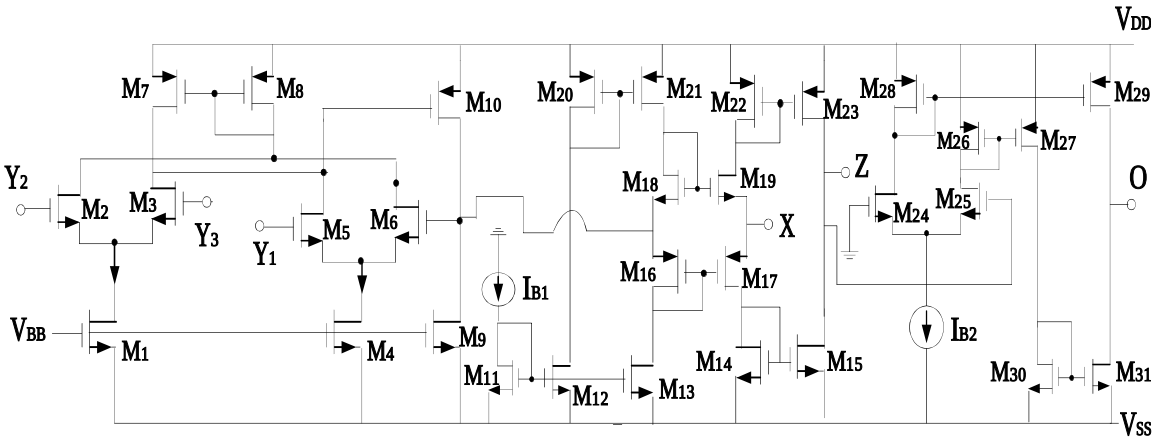

Fig. 3-9 CMOS Realization of CCDDCCTA [21]

3.6 OPERATIONAL TRANSRESISTANCE AMPLIFIER

Operational Transresistance Amplifier (OTRA) is a current mode active building block [22]-[24] which produces output voltage that is proportional to the difference of input currents. The schematic symbol of OTRA is given in Fig. 3-10 and it is characterized by following terminal relationship:

(3.12)

where is the trans-resistance gain.

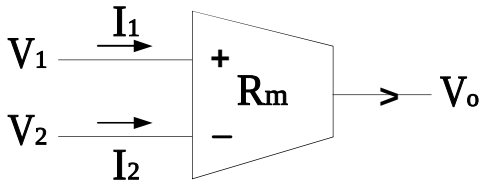

Fig. 3-10 Circuit Symbol of OTRA

The terminal characteristics show that it has low input and output impedance. In ideal case, ?? approaches to infinity and when negative feedback is used then ?? ? ??.

3.7 VOLTAGE DIFFERENCING TRANSCONDUCTANCE AMPLIFIER

Voltage Differencing Transconductance Amplifier (VDTA) is a recently introduced active building block which has OTA at its input and output stage [25]-[29]. It was proposed as a replacement of previously introduced current differencing transconductance amplifier (CDTA) [5]. Its symbolic representation and CMOS realization are given in Fig. 3-11 and 3-12.

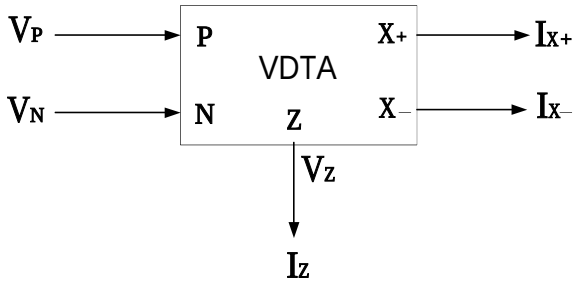

Fig. 3-11 Symbolic diagram of VDTA

The port relationship for VDTA can be represented as:

$$\begin{bmatrix} ?_? \\ ?_? \\ ?_? \end{bmatrix} = \begin{bmatrix} ?_? & ?_? & ?_? \\ ?_? & ?_? & ?_? \\ ?_? & ?_? & ?_? \end{bmatrix} \begin{bmatrix} ?_? \\ ?_? \\ ?_? \end{bmatrix} \tag{3.13}$$

where $$?_? = \frac{??_? ? ?_? ?}{?} \tag{3.14}$$

$$?_? = \frac{??_? ? ?_? ?}{?} + \frac{??_? ? ?_? ?}{?} \tag{3.15}$$

and $?_?$ represent the transconductance of $??$ transistor and is given by

$$?_? = \sqrt{?_? ?_? ?^? ?_? ?_? ?_?} \tag{3.16}$$

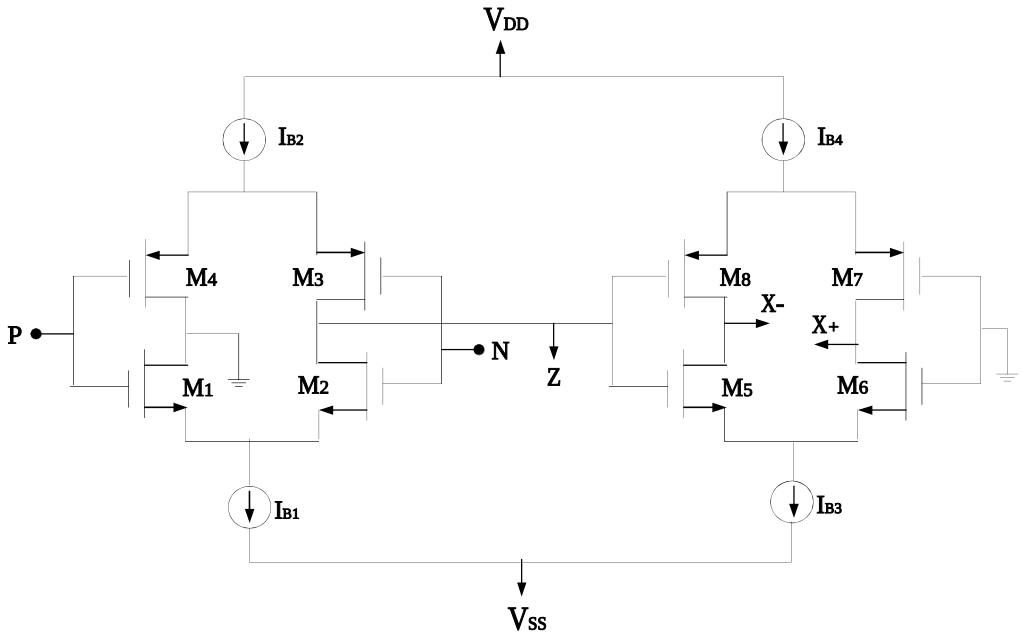

Fig. 3-12 CMOS Realization of VDTA [29]

3.8 CONCLUSION

This chapter is dedicated to several active devices that are used for realization of wave active filter so far. All of these active blocks are formed by some fundamental blocks such as differential pair, current mirrors, current conveyors and transconductance amplifier. A brief introduction of such active building blocks along with their symbolic representation and terminal characteristics are presented here.

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CHAPTER 4

WAVE ACTIVE FILTER

4.1 INTRODUCTION

To realize higher order filters, various methods are discussed in chapter 2. If sensitivities requirement are stringent then only resistively terminated LC ladder simulation techniques are used for higher order filter implementation as LC ladder has inherent lowest sensitivity to component tolerance. Apart from excellent sensitivity performance, the ample amounts of design information in the form of design tables for filter realization make this method an obvious choice for higher order filter realization [1].

The first two techniques i.e. “Element replacement” and “Operational simulation” for LC ladder simulation are discussed in chapter 2. Though these techniques show excellent sensitivity performance, these also have some disadvantages. If filters are realized by using operational simulation technique then signal flow graphs (SFGs) represent the voltage-current relationship of various passive components. These SFGs are implemented by using lossy and lossless integrators. Lossless integrators are difficult to design in physical form because of non ideal behavior of passive components used. Also this method employs floating capacitance which is not a favorable feature as per monolithic integration point of view. The other approach is element replacement in which inductors are replaced with gyrators. Although this approach shows good result in terms of sensitivity and noise performance, the realization of high quality gyrator for floating inductor is not an easy task [2]. This method also suffers from the inclusion of floating capacitors. Bruton’s FDNR method is another way of element replacement technique which is well suited for low pass filter design only.

In this chapter the last technique “Wave Active Filter approach” of LC ladder simulation is presented which overcomes the shortcomings of the two techniques described earlier.

4.2 WAVE ACTIVE FILTER APPROACH

Wave active filter design approach is an alternate way of simulating passive doubly terminated LC ladder circuit to obtain stringent sensitivity requirements. This technique is based on the splitting of complete ladder network in different individual series and shunt two port networks and then replacing each passive two port network with its active counterpart. This method makes use of scattering matrix to relate voltage and current quantities. In general scattering matrix is used for power quantity and it can also be extended here to represent terminal behavior but for simplicity voltage or current instead of power wave is used for active filter design [2].

A two port network is shown in Fig. 4-1 where A_1, A_2 are incedent waves and B_1, B_2 are reflected waves at port 1 and port 2 respectively. The normalized port resistances are represented as R_1, R_2 at port 1 and port 2 respectively. The terminal characteristics of this two port network are as follows [3], [4]:

$$V_1 = A_1 + B_1 \qquad I_1 = \frac{A_1 - B_1}{R_1} \tag{4.1}$$

$$V_2 = A_2 + B_2 \qquad I_2 = \frac{A_2 - B_2}{R_2} \tag{4.2}$$

where V_n and I_n are incident and reflected waves at port n respectively and R_n are the port normalization resistances.

Fig. 4-1 A two port network with incident and reflected waves

The transmission matrix for this two port network, considering the both currents are flowing into the network, is as follows:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \tag{4.3}$$

On combining eq. (4.1), (4.2) and (4.3), the following relationship is obtained between reflected and incident voltages of two port network:

(4.4)

where, (4.5.1)

(4.5.2)

(4.5.3)

(4.5.4)

(4.5.5)

(4.5.6)

Now let us take a ladder network as shown in Fig. 4-2 in which , ,…, are series branch impedances and , ,…, are shunt arm admittances. These elements are either inductors or capacitors or a combination of both.

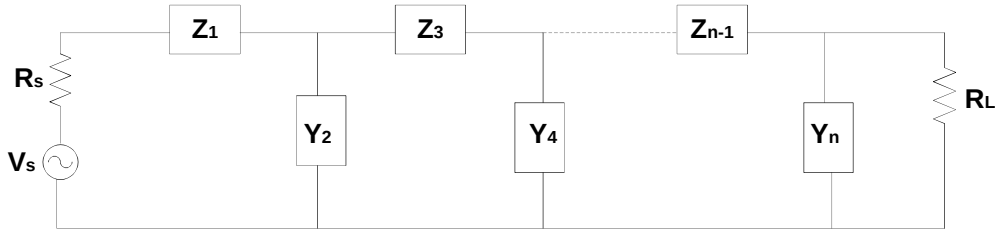
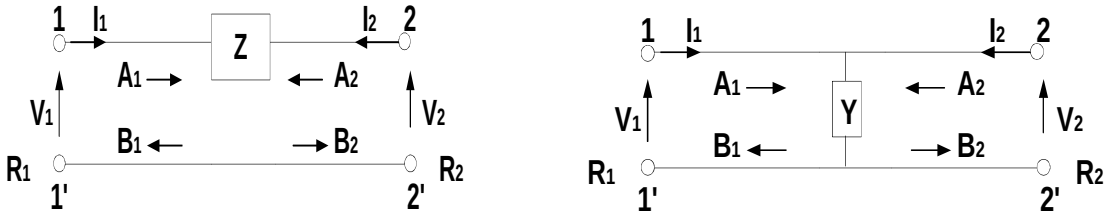


Fig.4-2 General form of LC Ladder circuit [2]

The ladder network can be split into smaller two port network containing either a series branch impedance or shunt branch admittance as shown in Fig. 4-3(a) and (b) respectively.



(a) (b)

Fig. 4-3 Two port Network (a) series arm impedance and (b) shunt arm admittance

The modified transmission matrices for series arm impedance and shunt arm admittance are given as:

(4.6)

(4.7)

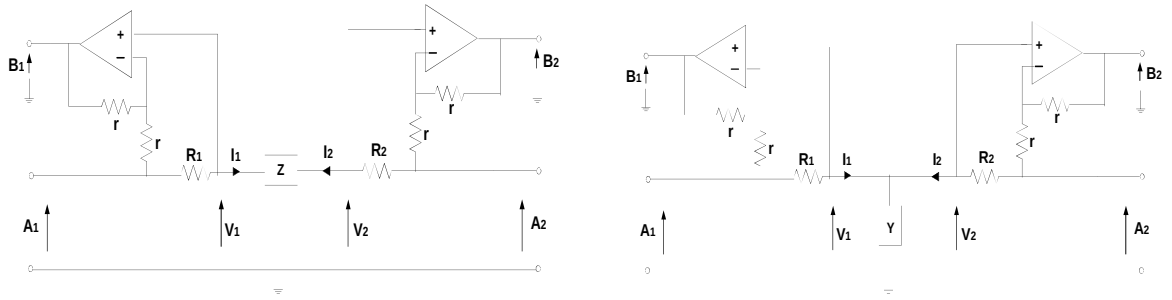
Substituting Eq. (4.6) into Eq.(4.5) or subsequently in Eq.(4.4) the scattering matrix for series arm impedance is obtained as follows:

(4.8)

Similar substitution for the subnetwork of Fig. 4-3(b) yields the relation between reflected and incident voltage waves as follows:

(4.9)

The active realizations (using Op-amps) of Eq. (4.8) and (4.9) are shown in Fig. 4-4(a) and (b) respectively [4].



(a) (b)

Fig. 4-4 Active realization of (a) Eq. (4.8) and (b) Eq. (4.9)

4.3 WAVE ACTIVE EQUIVALENTS (WAEs)

This section is dedicated to describe several wave equivalents for elementary two port network in the ladder circuit. This two port network may be an inductor or a capacitor or a tuned circuit.

4.3.1 Wave Equivalents for series arm impedance

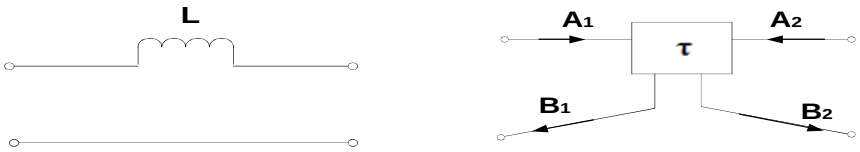
Let us consider that the series arm impedance for the subnetwork of Fig. 4-3(a) is inductor then according to Eq. (4.8) the scattering matrix will take the form as [3]:

(4.10)

Taking equal port normalization resistances i.e. , the Eq. (4.10) reduces as

or (4.11)

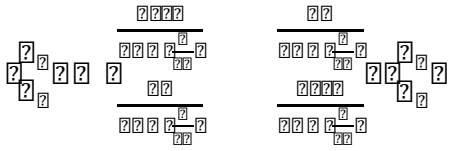
Where $\tau=L/2R$. The series inductor and its wave equivalent in symbolic form are shown in Fig. 4-5(a) and (b) respectively.

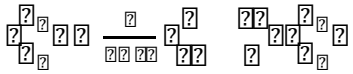


(a) (b)

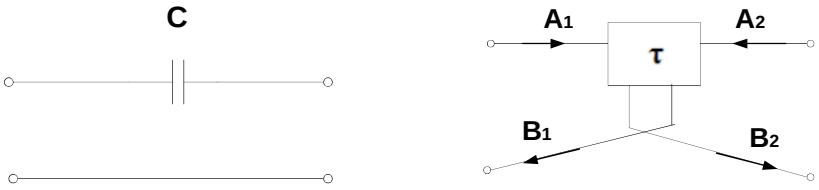
Fig. 4.5 (a) series arm inductor (b) wave equivalent

Now **τ** if the series arm impedance of the subnetwork of Fig. 4-3(b) is taken as capacitor [illegible] then Eq.(4.8) for equal port resistances take the form as



or  (4.12)

Where $\tau=2RC$. A little observation of Eq. (4.11) and (4.12) shows that only interchanging the rows of s-matrix for series branch inductance leads its conversion into series branch capacitance. Thus wave equivalent of series branch capacitance can be realized with wave equivalent of series inductor with swapped reflected waves. The symbolic representation of series branch capacitance is shown in Fig. 4-6.



(a) (b)

Fig. 4-6 (a) series arm capacitor (b) wave equivalent τ_2

Generalizing the above fact, if series branch impedance Z is replaced by its dual impedance Z' such that

$$Z' = \frac{1}{Z} \qquad (4.13)$$

then wave equivalent of Z' can be obtained by interchanging the reflected waves in wave equivalent of Z [2].

4.3.2 Wave Equivalents for shunt arm admittance

In Fig. 4-3(b), if the shunt element is a capacitor $Y = sC$ then scattering matrix of Eq. (4.9) for equal value of port normalization resistance will take form as

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} \frac{sC}{2+sC} & \frac{2}{2+sC} \\ \frac{2}{2+sC} & \frac{sC}{2+sC} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}$$

or

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} \frac{s\tau}{1+s\tau} & \frac{1}{1+s\tau} \\ \frac{1}{1+s\tau} & \frac{s\tau}{1+s\tau} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \qquad (4.14)$$

where $\tau = RC/2$.

Now, $$V_1 = \frac{s\tau}{1+s\tau} I_1 + \frac{1}{1+s\tau} I_2 \qquad (4.15.1)$$

$$V_2 = \frac{1}{1+s\tau} I_1 + \frac{s\tau}{1+s\tau} I_2 \qquad (4.15.2)$$

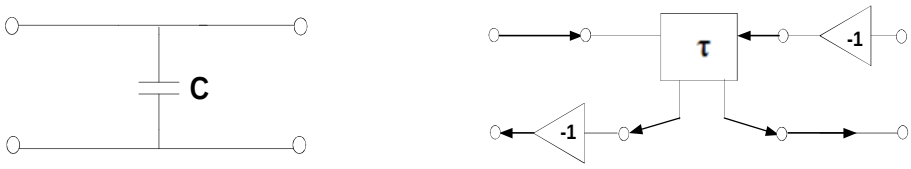
Rearranging Eq. (4.15), scattering matrix for shunt capacitor is obtained as

$$\begin{bmatrix} V_1 \\ -I_1 \end{bmatrix} = \begin{bmatrix} \frac{s\tau}{1+s\tau} & -\frac{1}{1+s\tau} \\ \frac{1}{1+s\tau} & \frac{s\tau}{1+s\tau} \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix}$$

or

$$\begin{bmatrix} -I_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} \frac{s\tau}{1+s\tau} & \frac{1}{1+s\tau} \\ -\frac{1}{1+s\tau} & \frac{s\tau}{1+s\tau} \end{bmatrix} \begin{bmatrix} V_1 \\ I_2 \end{bmatrix} \qquad (4.16)$$

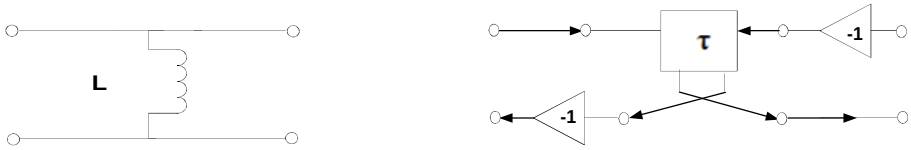
On comparing scattering matrix of Eq. (4.11) and (4.16), it is clear that both matrixes have the same form except one reflected wave V_1 and one incident wave I_1 are inverted in this case. Thus the symbolic diagram of shunt capacitor is same as series inductor with V_1 and I_1 is inverted as shown in Fig. 4-7.



(a) (b)

Fig. 4.7 (a) Shunt arm capacitor (b) wave equivalent

Following the similar approach, the wave flow diagram for shunt arm inductor is obtained whose symbolic representation is shown in Fig. 4-8.

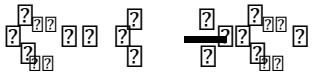


(a) (b)

Fig. 4-8(a) Shunt arm inductor (b) wave equivalent

4.3.3 Interconnection Rules [4]

After representing series and shunt elements in symbolic form, there is a necessity to explain the proper interconnection rules for adjacent wave equivalents to avoid errors raised from loading effects. Two adjacent passive networks N_a and N_b are shown in Fig. 4-9(a). As both networks are cascaded in ladder circuit, S_{22} is same as S_{22a} and S_{22} = S_{22a}. Thus,

 (4.17)

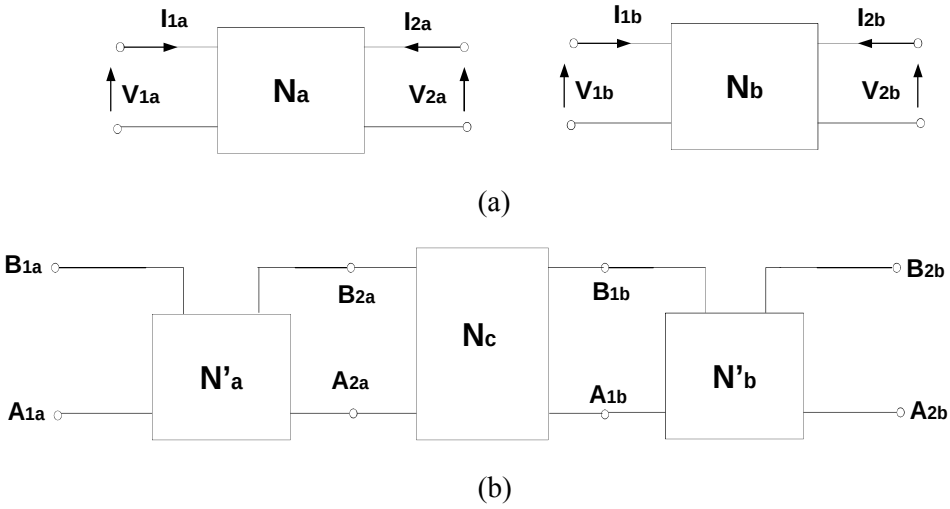


Fig. 4-9 (a) Two adjacent 2PN (b) their WAEs interconnected

It is obvious that adjacent ports of wave equivalent networks $\mathcal{N}'_a$ and $\mathcal{N}'_b$ can not be directly connected. A matching subnetwork $\mathcal{N}_c$ is assumed which properly interconnect the adjacent networks $\mathcal{N}'_a$ and $\mathcal{N}'_b$ as shown in Fig. 4-9(b). A non singular 2×2 matrix [P] can be described as:

$$\begin{bmatrix} B_{1a} \\ A_{1a} \end{bmatrix} = [P] \begin{bmatrix} B_{2b} \\ A_{2b} \end{bmatrix} \tag{4.18}$$

If port normalization resistances at port 1b and 2a are assumed to be equal then by using Eq. (4.1) and (4.2), it can be shown that:

$$B_{1a} = P_{11} B_{2b} + P_{12} A_{2b} \tag{4.19}$$

$$A_{1a} = P_{21} B_{2b} + P_{22} A_{2b} \tag{4.20}$$

Substituting B_{1a} A_{1a} from Eq. (4.17) into Eq. (4.19), we obtain that

$$\frac{V_{1a} - I_{1a} R_{1a}}{2\sqrt{R_{1a}}} = P_{11} \frac{V_{2b} + I_{2b} R_{2b}}{2\sqrt{R_{2b}}} + P_{12} \frac{V_{2b} - I_{2b} R_{2b}}{2\sqrt{R_{2b}}}$$

or

$$V_{1a} - I_{1a} R_{1a} = P_{11} \sqrt{\frac{R_{1a}}{R_{2b}}} (V_{2b} + I_{2b} R_{2b}) + P_{12} \sqrt{\frac{R_{1a}}{R_{2b}}} (V_{2b} - I_{2b} R_{2b}) \tag{4.21}$$

Now solving Eq.(4.20) for [illegible] and inserting its value in Eq. (4.21) provides:

[illegible]

or [illegible] (4.22)

On comparing Eq. (4.22) and (4.18), we get

[illegible] (4.23)

Hence, the matching network [illegible] has functionality such that [illegible] is connected to [illegible] and [illegible] is connected to [illegible] .This interconnection rule is schematically known as cross cascade connection which is shown in Fig. 4-10.

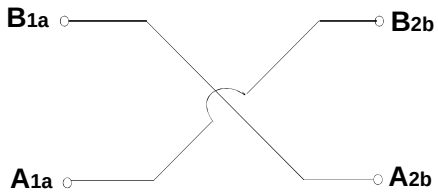


Fig. 4-10 cross cascade connection of two adjacent WAEs with equal normalization resistances

In general, the interconnection rule for multiple two port networks connected adjacently can be stated as " The wave equivalents of elementary two ports have to be connected such that the reflected waves of an elementary two port become the incident waves of the preceding and following ones and vice versa."[2]

4.3.4 Wave equivalents for Tuning Circuits

The tuned circuit can be comprised of series or parallel connection of inductor and capacitor connected as series arm impedance or shunt arm admittance. The wave equivalent of these tuned circuits can be drawn as shown in Fig. 4-11 (a) and (b) with the help of wave equivalents of individual wave flow diagram of elementary two port network and applying interconnection rule as stated in the previous section.

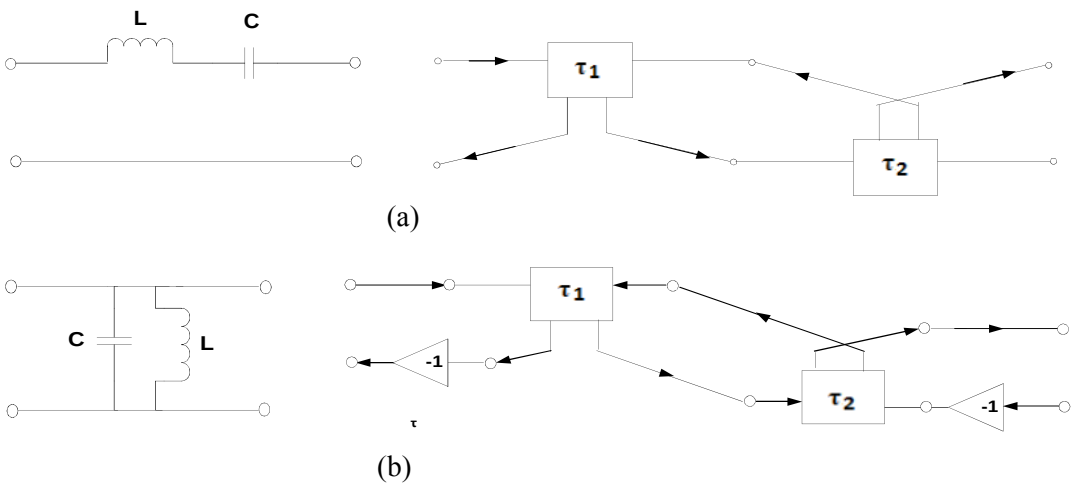


Fig. 4-11 Wave flow diagram for (a) series tuned series arm circuit (b) parallel tuned shunt arm circuit

For series tuned circuit connected in series arm the impedance is given as

$$Z = j\omega L + \frac{1}{j\omega C} = \frac{j\omega^2 LC - 1}{j\omega C} \tag{4.24}$$

Now if this Z is replaced by its dual impedance, then using Eq. (4.13) and (4.24)

$$Z' = \frac{j\omega^2 LC - 1}{j\omega C} = \frac{j\omega^2 LC - 1}{j\omega C\left(\frac{j\omega^2 LC - 1}{j\omega C}\right)} = \frac{1}{j\omega C} \tag{4.25}$$

Thus Eq. (4.25) represents the parallel tuned circuit connected in series arm comprised of inductor $L' = LC^2$ and capacitor $C' = \frac{1}{LC^2}$ whose wave equivalent is same as for series tuned series arm circuit (Fig. 4-11a) with interchanged reflected waves (Fig. 4-12) as discussed in section 4.3.1. Following the similar approach the wave equivalent of series tuned shunt arm circuit is shown in Fig. 4-13.

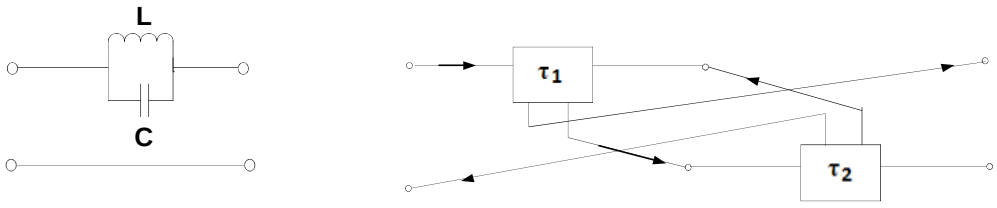


Fig. 4-12 Wave flow diagram for parallel tuned series arm circuit

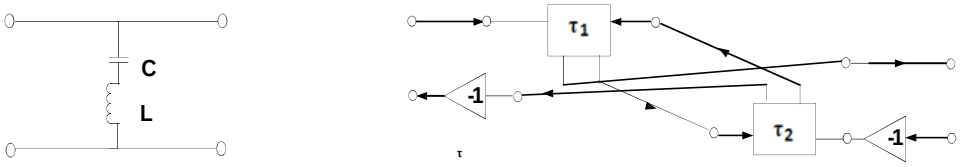


Fig. 4-13 Wave flow diagram for series tuned shunt arm circuit

Table (4-1) and (4-2) shows that all the wave flow diagrams for elementary two port networks connected in series and shunt arms respectively.

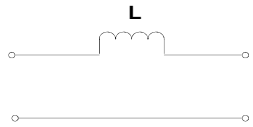
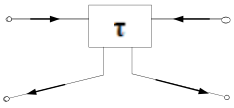
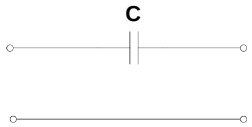
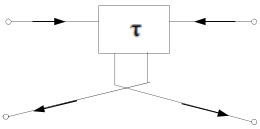
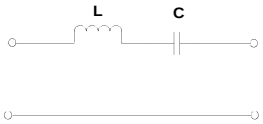
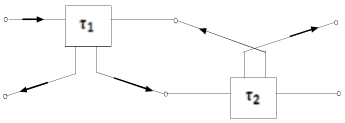
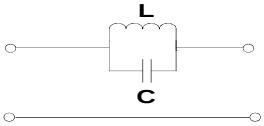
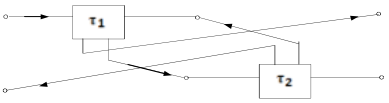
Elementary two port network	Wave Active Equivalent	Element values
		[illegible]
		[illegible]
		[illegible]
		[illegible]

Table 4-1 Wave Flow Diagrams for Series arm Impedances [2]

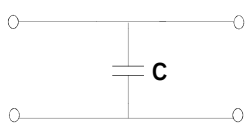
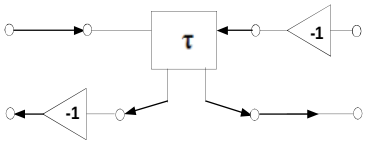
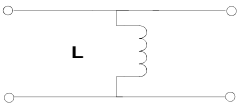
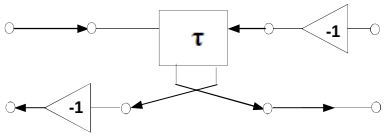
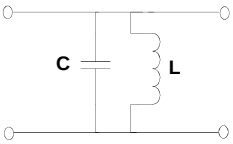
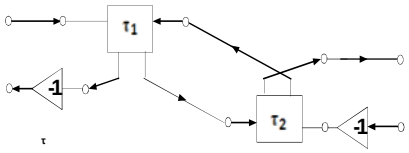
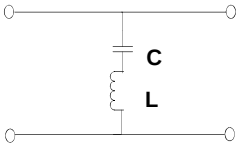
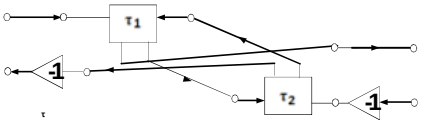
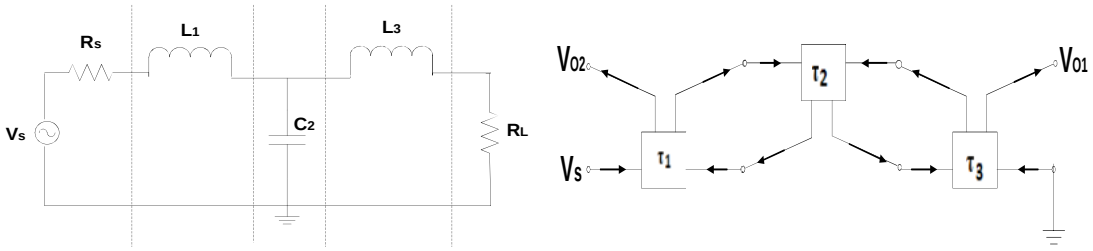
Elementary Two port Network	Wave Equivalent	Element Values
		$C = \frac{1}{2R}$
		$L = \frac{R}{2}$
		$C = \frac{C_1}{2R}$ $L = \frac{2RC_2}{2}$
		$C = \frac{C_1}{2R}$ $L = \frac{2RC_2}{2}$

Table 4-2. Wave Flow Diagrams for Shunt arm Admittances [2]

4.3.5 Wave Active Filter simulation example

To show the workability of wave active approach the third order LC ladder lowpass prototype with $R_s = R_L$ is shown in Fig. 4-14(a). First complete ladder network is divided into elementary two port networks as shown dotted lines and then these elementary networks are replaced by their wave equivalents as shown in Fig. 4-14(b).



(a) (b)

Fig. 4-14(a) 3rd order LC lowpass prototype (b) its wave equivalent

A close observation of Fig. 4-14(b) shows that there are two outputs V_{02} and V_{01} available in case of wave active filter. These two output transfer functions $\frac{V_{02}}{V_S}$ and $\frac{V_{01}}{V_S}$ are power complementary to each other when $R_S = R_L$. It can be seen that, for equal port normalization resistances $|T_{02}|^2 + |T_{01}|^2 = 1$, where T_{02} is one transfer function and T_{01} is its complement. In other words,

$$\left|\frac{V_{02}}{V_S}\right|^2 + \left|\frac{V_{01}}{V_S}\right|^2 = 1 \tag{4.26}$$

which means if $\frac{V_{02}}{V_S}$ is low pass function then $\frac{V_{01}}{V_S}$ will be high pass function and vice versa [4].

4.4 REALIZATION OF WAVE ACTIVE EQUIVALENTS

Wave active equivalents for an elementary two port network can be realized by using any active block. To see the realization process the S-matrix for series inductor from Eq. (4.11) is again presented here:

$$V_2 = \frac{2R}{2R+sL} V_1 + \frac{sL}{2R+sL} V_2 \tag{4.27.1}$$

$$V_2 = \frac{sL}{2R+sL} V_1 + \frac{2R}{2R+sL} V_2 \tag{4.27.2}$$

Rearranging Eq. (4.27) again, it can be written as:

$$V_2 = V_2 - \frac{sL}{2R+sL} V_2 - V_1 \tag{4.28.1}$$

$$V_2 = V_2 + \frac{sL}{2R+sL} V_2 - V_1 \tag{4.28.2}$$

The Eq. (4.28) clearly states that to realize a series inductor in its wave equivalent form only three components are required; a lossy subtracting integrator, a summer and a subtractor circuit [5]. These components can be implemented by using any active devices. WAEs for other elements can be obtained from WAE of series inductor by simply interchanging the terminals and/or signal inversion.

4.5 SALIENT FEATURES OF WAF [4, 5]

Wave active filter approach is an alternate way of simulating resistively terminated LC ladder circuit which offers some significant advantages over other approaches as follows:

a) Design methodology is simple as no mathematical representation of voltage and current quantities is required as in the case of leapfrog approach.

b) Modular filter structures are obtained as only wave equivalent for an elementary series inductor is needed and rest of the wave equivalents can be derived from it easily.

c) Only lossy integrators are required for the realization of wave equivalents unlike leapfrog approach where lossless integrators are used.

d) Only grounded capacitors are used in realization of wave equivalents unlike in leapfrog and element replacement approach.

e) Power complementary response is obtained for equal port resistances.

The major drawback of wave active approach is use of several active blocks to realize a capacitor. The large number of active building blocks causes more power consumption.

4.6 IMPLEMENTATION OF WAVE ACTIVE FILTER USING DIFFERENT ACTIVE DEVICES

As discussed in chapter 3, several active devices have been used for realization of wave active filters so far. In this section, some simulation results are presented which are obtained by realizing wave active filer using different active devices; CFOA and DVCCTA.

4.6.1 CFOA based Wave Active Filter [6]

Current feedback operational amplifier is a versatile ABB which was used for realizing wave active filter by Koukiou [6]. The basic wave equivalent of a series inductor using CFOA is depicted in Fig. 4-15.

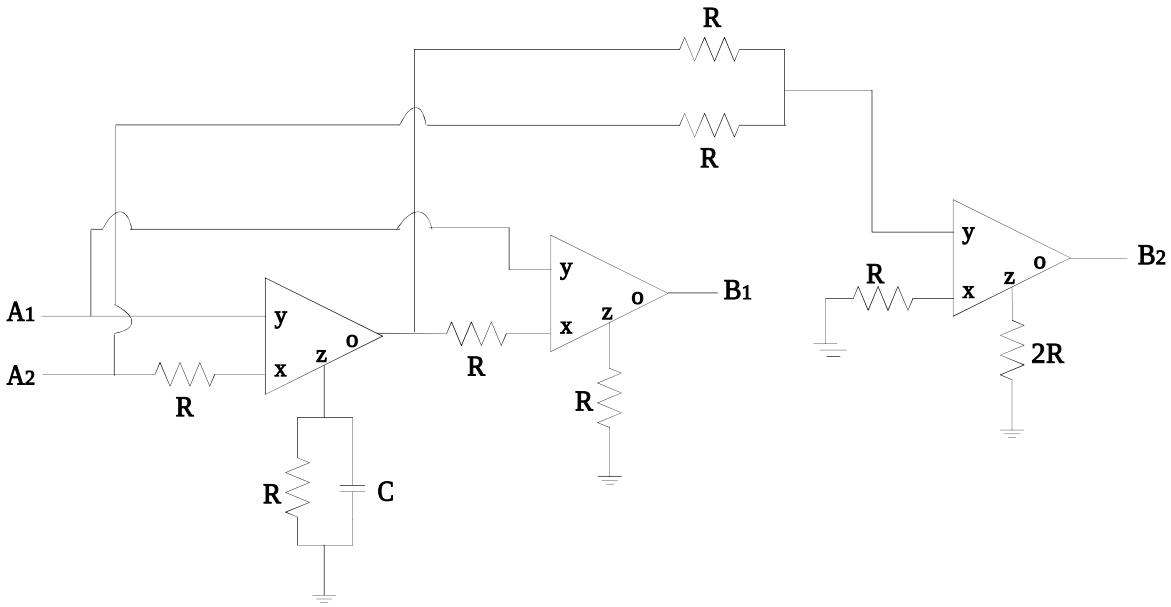


Fig. 4-15 Wave equivalent of series inductor based on CFOA [6]

The wave equivalents for other passive elements can be obtained with the wave equivalent of elementary series inductor by just swapping the outputs and/or using inverters as shown in Table 4-1 and 4-2.

A 3rd order low pass LC ladder prototype as shown in Fig. 4-14 (a) is simulated by wave active approach using CFOA as an active device. To design a chebyshev filter with 1dB ripple, the normalized components values are $R_1 = R_2 = 1\Omega$, $L_1 = L_3 = 1.5963$ and $C_2 = 1.0967$. For

designing filter with a cut off frequency of 100 KHz, the actual value of resistors and capacitors are 2.5 kΩ, 643 pF and 2.5kΩ, 320 pF for inductors and capacitors respectively. The power supply voltages are taken as ±5 V. The simulation results for low pass and its complementary high pass filter is shown in Fig. 4-16.

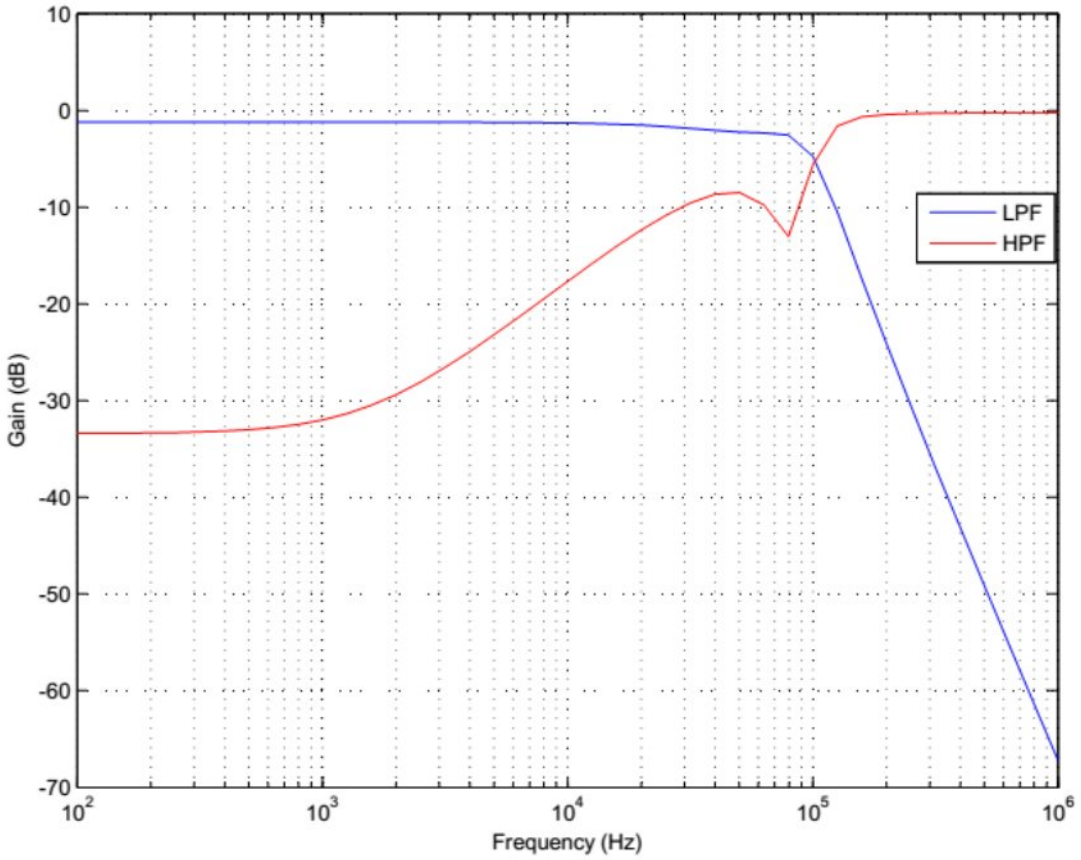


Fig. 4-16 Simulation Result for CFOA based Wave Active LPF and HPF

4.6.2 DVCCTA based Wave Active Filter [7]

Differential voltage current conveyor transconductance amplifier was used for realizing wave active filter by Panday [7]. The symbolic representation of DVCCTA is shown in Fig. 3-4 and its terminal characteristics are shown in Eq. (3.4). The wave equivalent for series arm inductor based on DVCCTA is shown in Fig. 4-17.

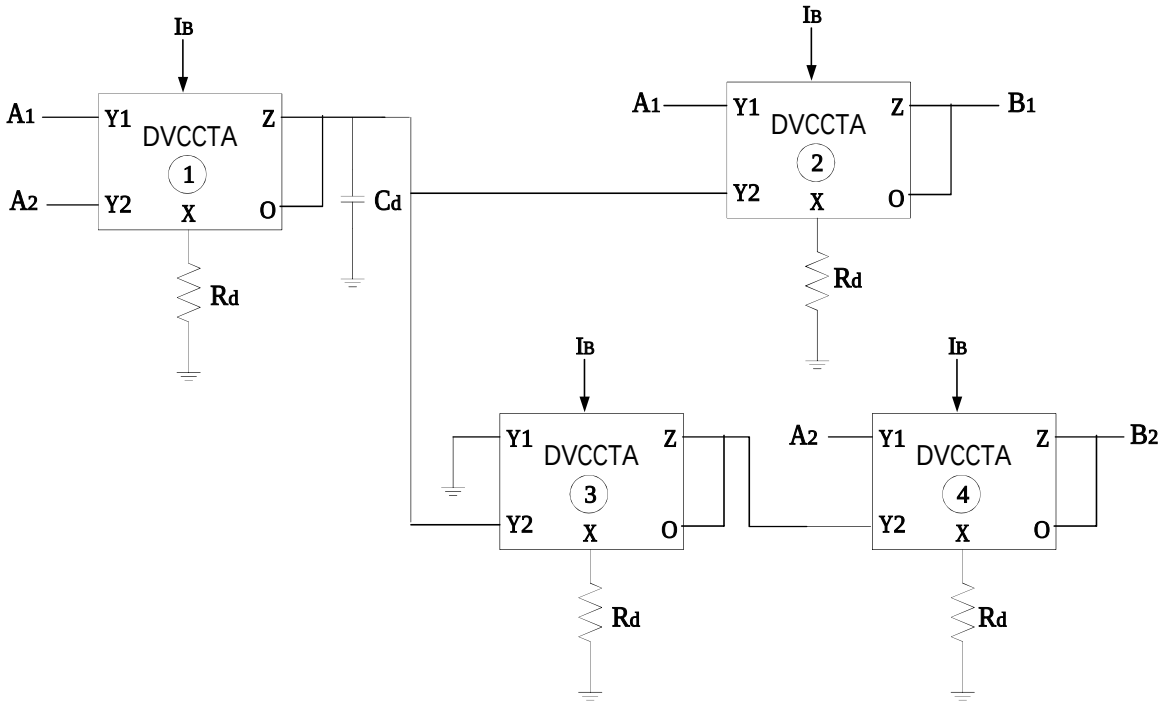


Fig. 4-17 Wave equivalent of series arm inductor by using DVCCTA [7]

A 4th order low pass Butterworth prototype LC ladder filter is simulated by using wave active approach with DVCCTA as an active block. The filter is designed for a cut off frequency of 200 kHz and bias current and voltages are taken as 200μA and ±1.25 V. The normalized components values are Rs = 1, L_1 = 0.7654, L_2 = 1.8485, C_1 = 1.8485, C_2 = 0.7654 and R_L = 1. The actual value of resistor for implementing the filter at desired frequency is R_d = 1447.5Ω and values of capacitors are 210.379 pF, 502.082 pF and 502.082 pF, 210.379 pF for wave equivalents of series inductors and shunt capacitors respectively. The filter structure is realized by using 0.25 μm TSMC technology parameters. The simulation results for low pass and high pass filters are shown in Fig. 4-18.

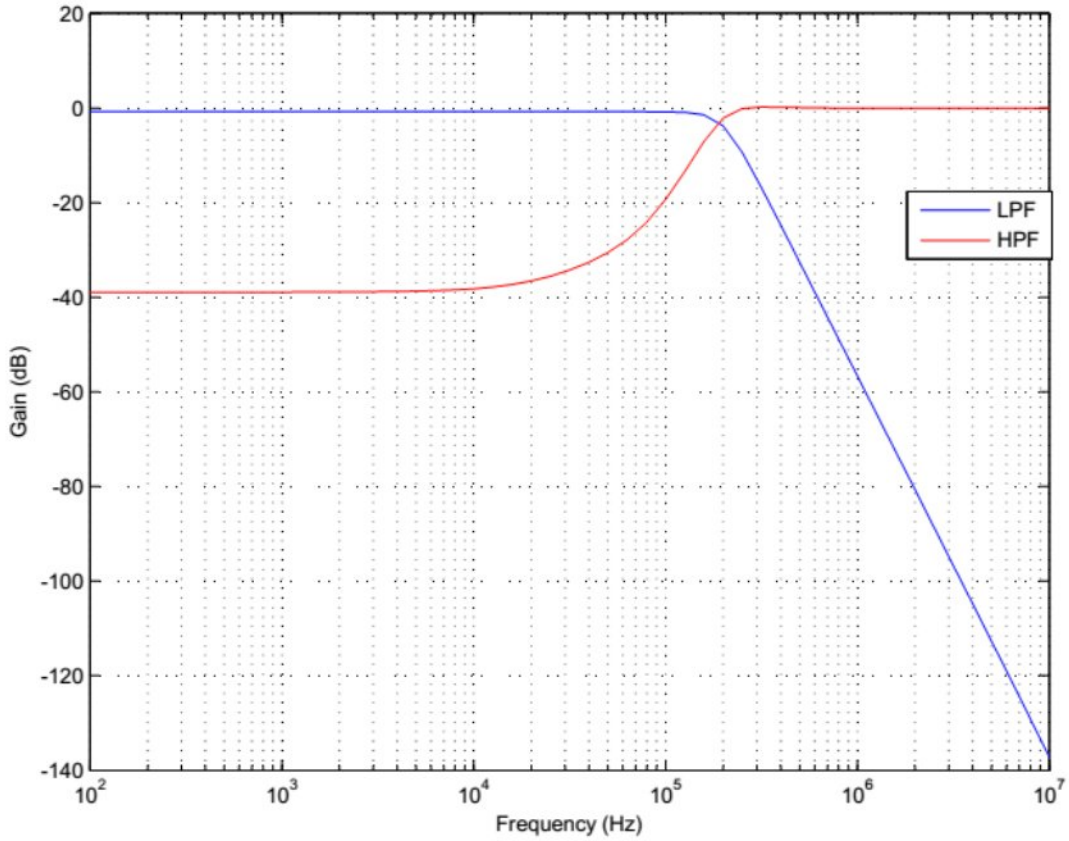


Fig. 4-18 Simulation Result for DVCCTA based Wave Active LPF and HPF

4.7 CONCLUSION

In this chapter, the detailed discussion on wave approach is presented. Wave approach is a part of LC ladder simulation technique which shows several advantages such as modular structure, presence of only lossy integrators and power complementary responses etc. over other techniques of LC ladder simulation. The design methodology of wave active filter is also very simple as wave equivalents of all passive elements can be obtained directly with the wave equivalent of elementary series inductor. Simulation results for wave active filter using CFOA and DVCCTA are also included.

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4. DELIYANNIS, T., SUN, Y., FIDLER, J.K. Continuous Time Active Filter Design. CRC Press, 1998.
5. SPANIDOU, A., PSYCHALINOS, C. Current Amplifier Based Wave Filters. Circuits Systems Signal Processing, vo. 24, no.3, p. 303-313, 2005.
6. KOUKIOU, G., PSYCHALINOS, C. Modular Filter Structures Using Current Feedback Operational Amplifiers. Radioengineering, vol.19, no. 4, p. 662-666, 2010.
7. PANDAY, N., KUMAR, P. Differential Voltage Current Conveyor Transconductance Amplifier based Wave Active Filter. Journal of Electron Devices, vol.10, p.429-432, 2011.

CHAPTER 5

VDBA BASED WAVE ACTIVE FILTER

5.1 INTRODUCTION

Several novel active building blocks were proposed by Biolek, Senani, Biolkova and Kolka [1] to add some significant features like enhanced universality, low parasite effects and electronic tunability etc. to the existing active devices and to make balance between speed and accuracy of electronic circuits. Voltage differencing buffered amplifier (VDBA) is one such active element. It is a voltage mode active device which was introduced as a dual of current differencing buffered amplifier (CDBA). The basic difference between VDBA and CDBA is that input and output variables are voltage in the former active block while current in the latter one [2]. In the present chapter we present a wave active filter using this building block.

5.2 VOLTAGE DIFFERENCING BUFFERED AMPLIFIER

VDBA is a combination of an operational transconductance amplifier (OTA) and voltage buffer. Having OTA at its input side and voltage buffer at output side, VDBA enjoys high input and low output impedance which makes it a favorable choice for voltage mode application. On the basis of input and output impedances it can be compared with conventional op-amps but VDBA is superior to op-amp as it also shows excellent features like wider bandwidth, less power consumption and higher slew rate of current mode active blocks. It's comparison with OTA is obvious as OTA is an integral part of it which facilitates it to electronic tunability of transconductance and avoidance of external resistors. The major difference between OTA and VDBA is that of output impedance which is low for former one and high for latter one [2].

Several modifications are done on the basic VDBA block to make it more versatile. As output portion of VDBA contain voltage buffer so the extended version can be derived by modifying inputs and outputs of the buffer. The device having inverted voltage at buffer output is known as voltage differencing inverted buffered amplifier (VDIBA) [3]. If voltage buffers use

differencing inputs, then the structure is known as voltage differencing differential input buffered amplifier (VD-DIBA) [4]-[7]. Similarly circuit element with differential output is known as voltage differencing differential output buffered amplifier (VD-DOBA) [1] or sometimes dual output-VDBA (DO-VDBA) [8]. To minimize the effect of digital noise and interference in mixed mode signal processing, analog circuits are designed with fully differential balanced architecture [9]. Thus a modification in VD-DOBA is known as fully balanced voltage differencing buffered amplifier (FB-VDBA) [10]-[12]. A further modification in existing VDBA structure leads to a new structure known as dual output controlled gain voltage differencing buffered voltage amplifier (DO-CG-VDBVA) [8].

5.2.1 Circuit Description of the VDBA

Voltage differencing buffered amplifier (VDBA) is shown in Fig. 5-1 in a symbolic form [2] where the difference of the voltage at input terminals (P and N) is transferred to Z terminal in the form of current with transconductance gain ?? and finally voltage at Z terminal is mirrored in to a low output impedance terminal 'W'.

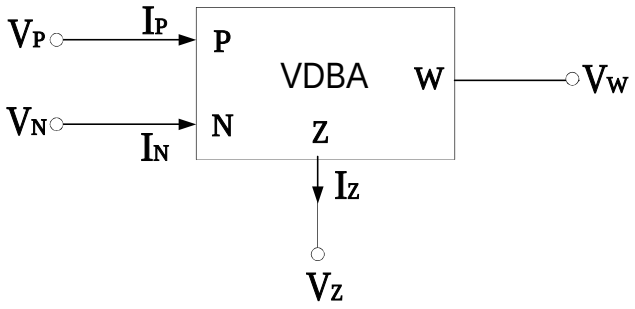


Fig. 5-1 Circuit symbol of VDBA

The terminal equations of VDBA are represented in matrix form as:

$$\begin{bmatrix} ?_? \\ ?_? \\ ?_? \\ ?_? \end{bmatrix} = \begin{bmatrix} ? & ? & ? & ? \\ ? & ? & ? & ? \\ ? & ? & ? & ? \\ ? & ? & ? & ? \end{bmatrix} \begin{bmatrix} ?_? \\ ?_? \\ ?_? \\ ?_? \end{bmatrix} \quad (5.1)$$

where ? is the voltage transfer ratio of ?? and ??. In general, ? ? ? ?? where ?? is the voltage tracking error having magnitude very less than unity. From Eq. (5.1) it is clear that ?? ? ?? ? ?

which implies that P and N are high input impedance terminals. As Z is a current output terminal which makes it high impedance terminal and finally W terminal is an output of voltage buffer having very low impedance.

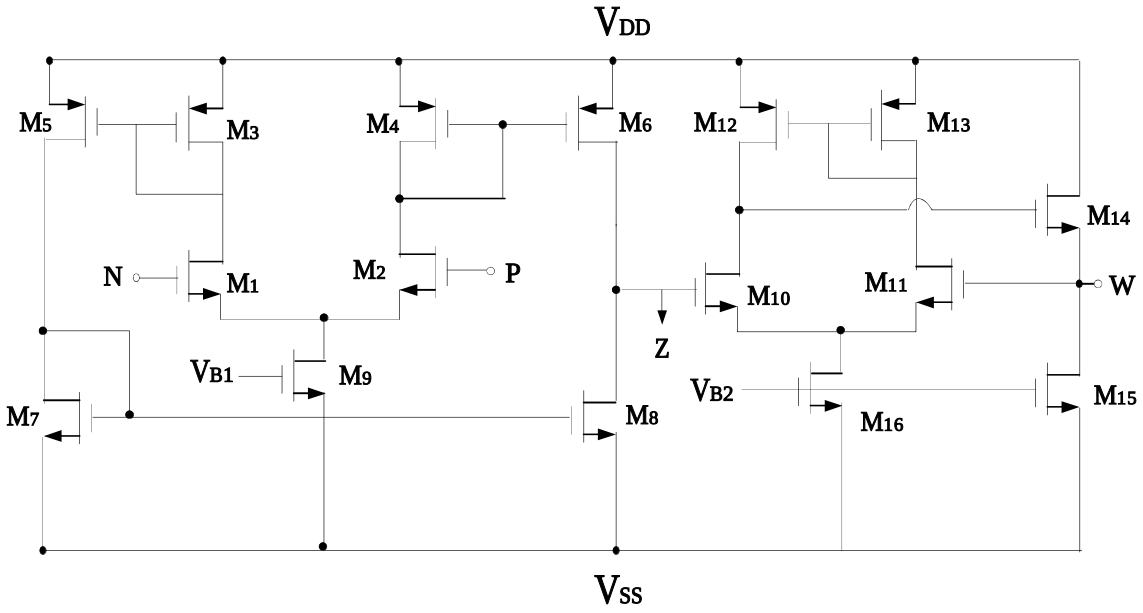


Fig. 5-2 CMOS Realization of VDBA [2]

The CMOS realization of VDBA is shown in Fig. 5-2 [2]. It is apparent from the circuit diagram that it consists of operational transconductance amplifier (OTA) block ($M_{\square}$ $\overline{\square_{\square}\square}$and the voltage buffer ($\square_{\square\square}$ $\overline{\square_{\square\square}\square}$block at output section. The transconductance gain is controlled by a biasing voltage or current of OTA section.

5.2.2 Characterization of the VDBA

To verify the theoretical behavior of VDBA, the circuit diagram of Fig. 5-2 is simulated in PSPICE with TSMC CMOS 0.35 μm technology. The supply voltages are □ 1.5V and biasing voltages are taken as $\square_{\square\square}$= -0.44V and $\square_{\square\square}$= -0.9V. The aspect ratios of different transistors of VDBA are listed in Table 5-1.

Transistors	W(μm)	L(μm)
□□-□□, □□□, □□□, □□□, □□□	7	0.35
□□[□□	21	0.7
□□[□□	7	0.7
□□	3.5	0.7
□□□ □□□	14	0.35

Table 5.1 Aspect Ratio for realization of VDBA [2]

Different parameters obtained through simulation results are as follows:

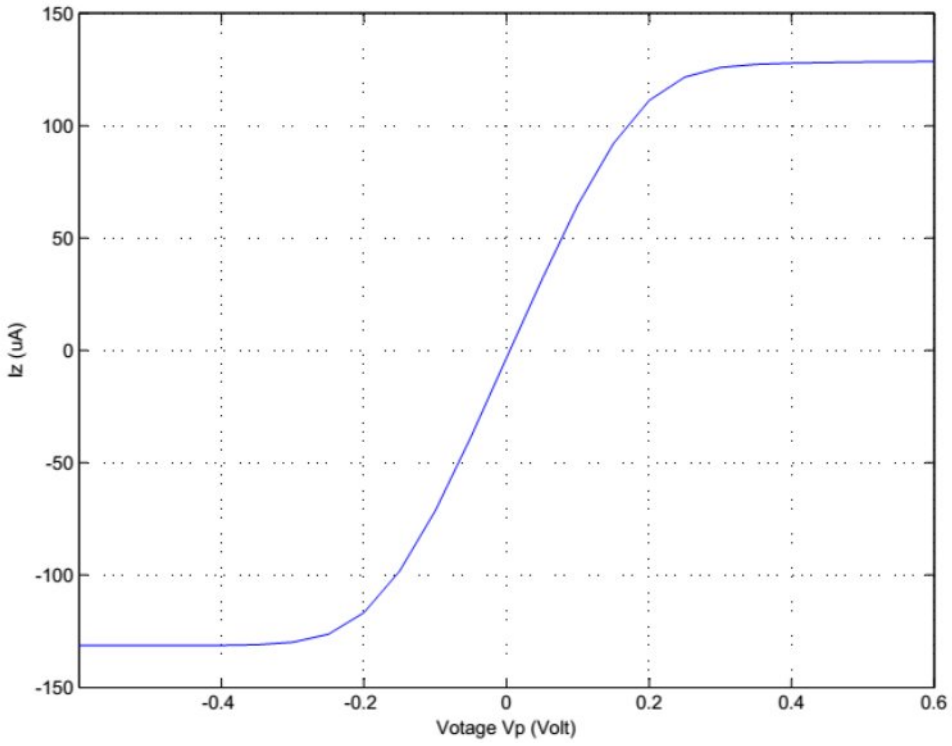
i) Transconductance □□ □ 714.5 uS

ii) Parasites at Z terminal: parallel connection of resistance □□□ □ 178.272kΩ and capacitor □□□ □ 0.0105pF.

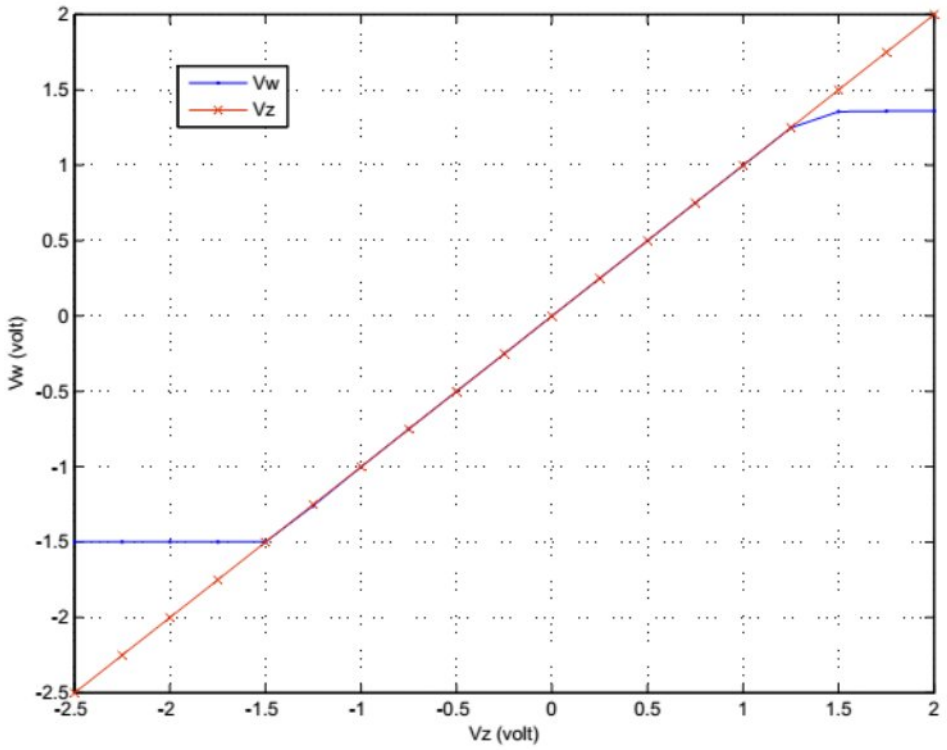
iii) Parasites at W terminal: A series resistance □□ □ □ 21Ω

iv) Power consumption: 0.636mW.

The DC and AC transfer characteristics of input and output sections of VDBA are shown in Fig 5-3 and 5-4 respectively. The graph between □□ □□ as shown in Fig. 5-3(a) is obtained by grounding the N terminal. This graph also tells that the linear range of operation for VDBA is from -163mV to 154mV. Similarly the DC characteristics □□ □□ plot as shown in Fig. 5-3(b) shows that the upper limit for □□ is 1.25V and lower bound is limited to negative supply voltage of VDBA.

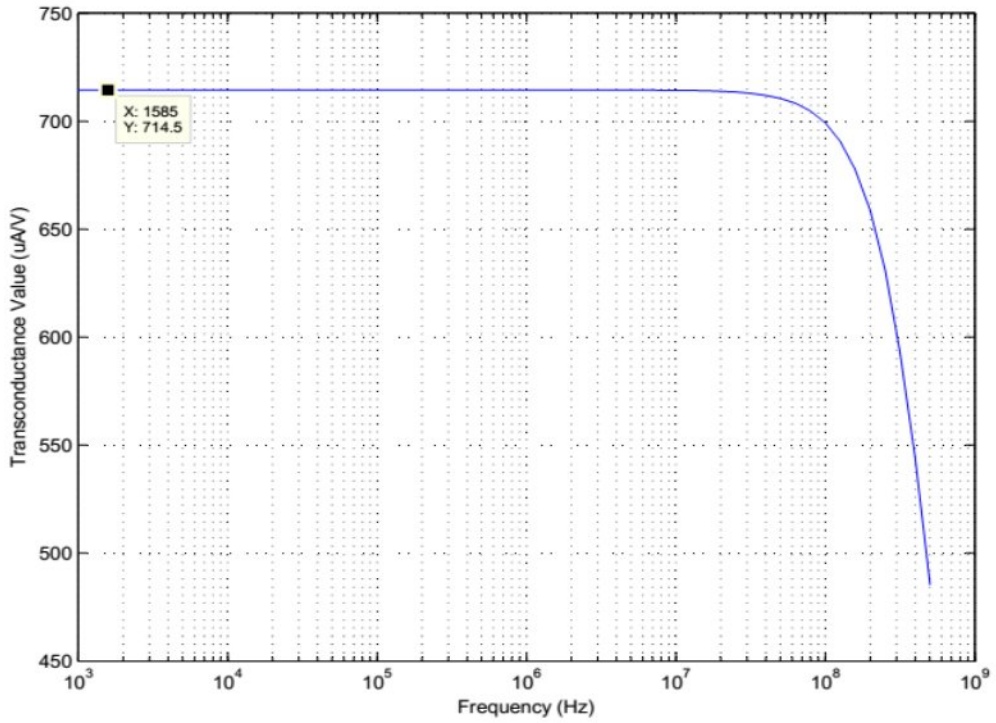


(a)

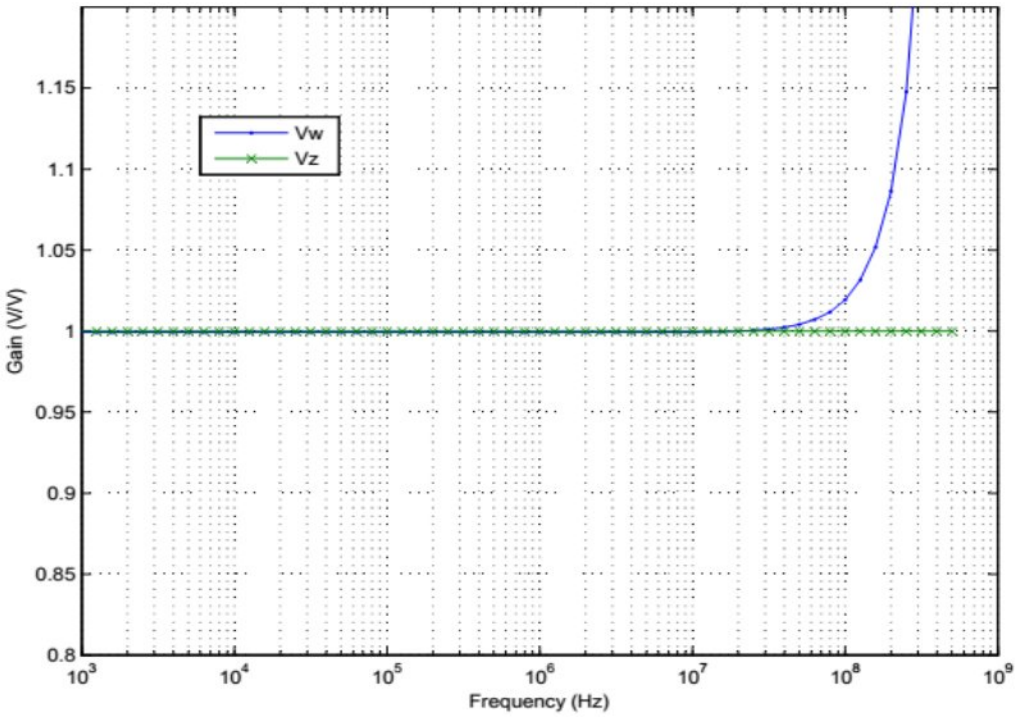


(b)

Fig. 5-3 DC Characteristics of VDBA (a) Input characteristics (b) Output characteristics



(a)



(b)

Fig. 5-4 AC characteristics of VDBA (a) Input Characteristics (b) Output characteristics

5.3 DO-VDBA

5.3.1 Circuit Description of the DO-VDBA

A modified version of VDBA with dual output (an additional inverted output) is known as DO-VDBA. The symbolic diagram of DO-VDBA is shown in Fig. 5-5.

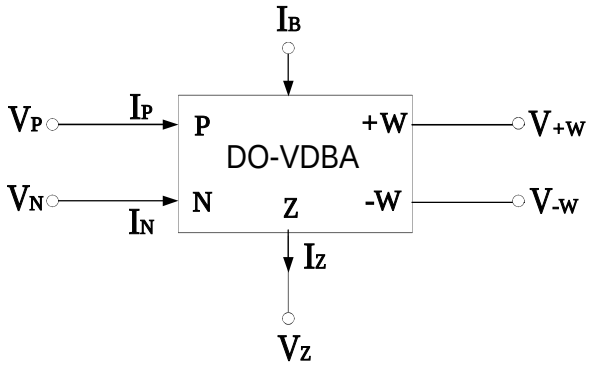


Fig. 5-5 Symbolic representation for DO-VDBA

The modified terminal characteristics of DO-VDBA are as follows:

$$\begin{bmatrix} ? \\ ? \\ ? \\ ? \\ ? \end{bmatrix} = \begin{bmatrix} ? & ? & ? & ? & ? \\ ? & ? & ? & ? & ? \\ ? & ? & ? & ? & ? \\ ? & ? & ? & ? & ? \\ ? & ? & ? & ? & ? \end{bmatrix} \begin{bmatrix} ? \\ ? \\ ? \\ ? \\ ? \end{bmatrix} \tag{5.2}$$

Thus in DO-VDBA two outputs with opposite signs and equal in magnitude are obtained. The CMOS realization of DO-VDBA is shown in Fig. 5-6 [8] in which ? ?-? ? form an OTA section. ? ?-? ? and ? ?-? ? are two voltage inverters.

5.3.2 Characterization of the DO-VDBA:

The circuit schematic shown in Fig. 5-6 is simulated in PSPICE using models of TSMC 0.18µm CMOS technology. The supply voltage is ± 1.2V and bias current is 50µA. The aspect ratios for different transistors of DO-VDBA are taken as shown in Table 5-2.

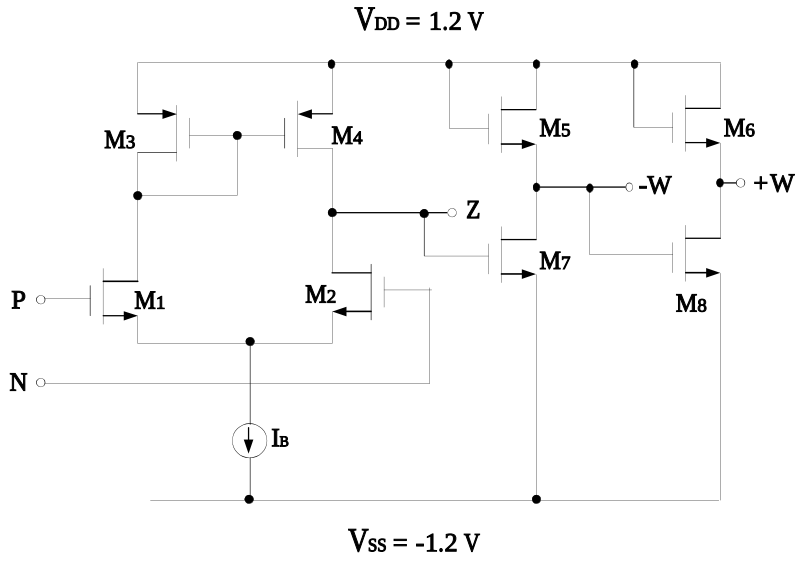


Fig. 5-6 CMOS Realization of DO-VDBA [8]

Transistors	W(µm)	L(µm)
M□,□ □	50	1
□ □[□ □	20	1
□ □ □ □	60	0.36

Table 5-2 Aspect Ratio for the realization of DO-VDBA [8]

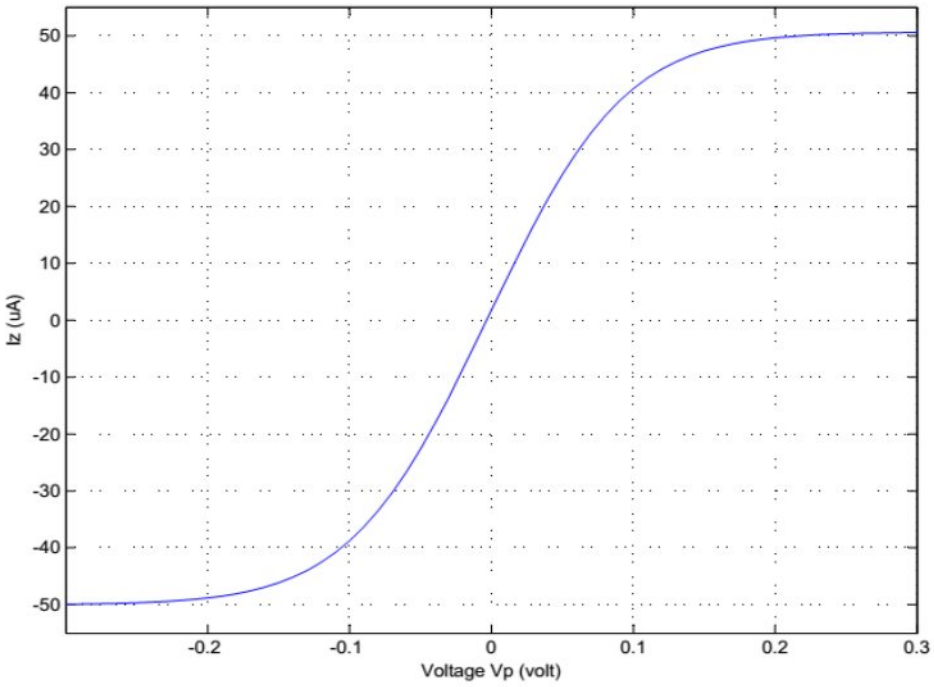
Different parameters of DO-VDBA, obtained through simulation results are as follows:

i) Transconductance □□ □ 518.4uS

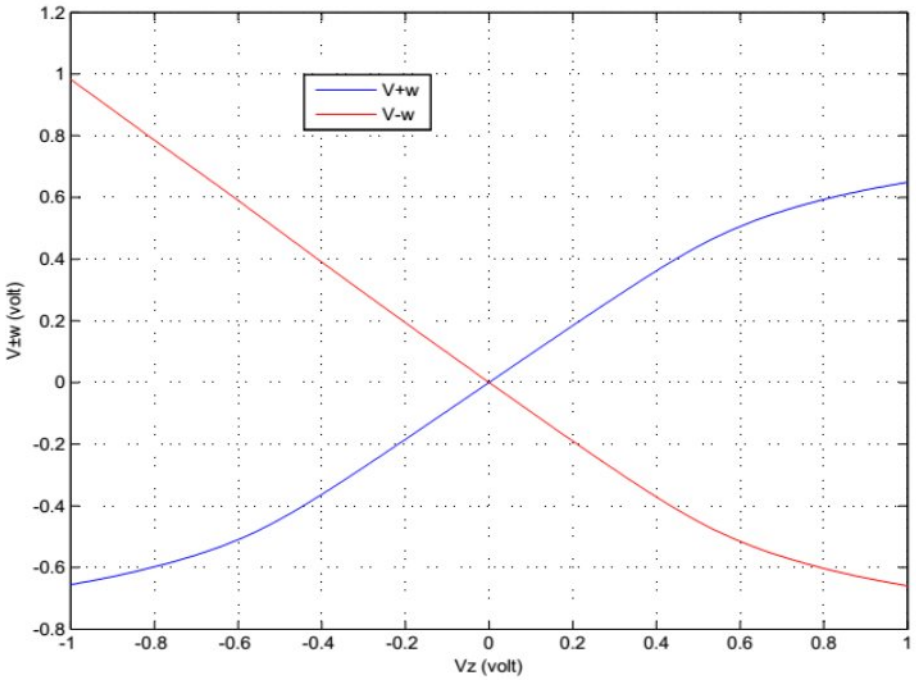
ii) Parasites at Z terminal: parallel connection of resistance □□□ □ 170kΩ and capacitor □□□ □ 0.35uF

iii) Parasites at ±W terminals: A series resistance □□ □ □ 53Ω

The DC and AC characteristics of input and output section of DO-VDBA are shown in Fig. 5-7 and 5-8. The voltage transfer ratio from terminal z to +w (□□□/□□□is 0.926 and from z to –w (□□□/□□□ is 0.962 as shown in Fig, 5.7 (a) and (b).

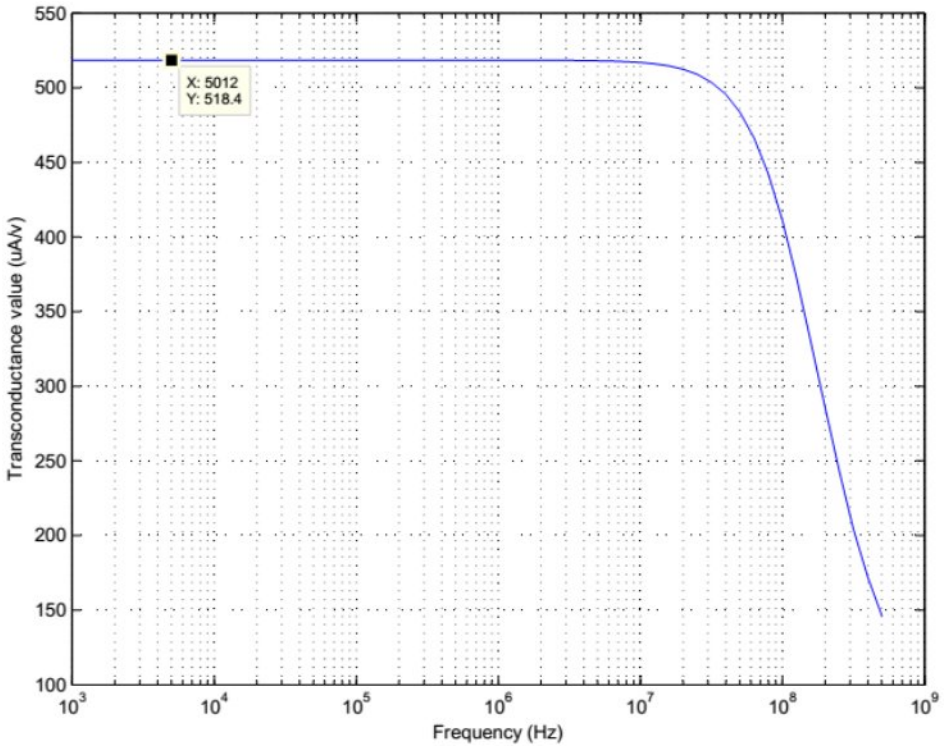


(a)

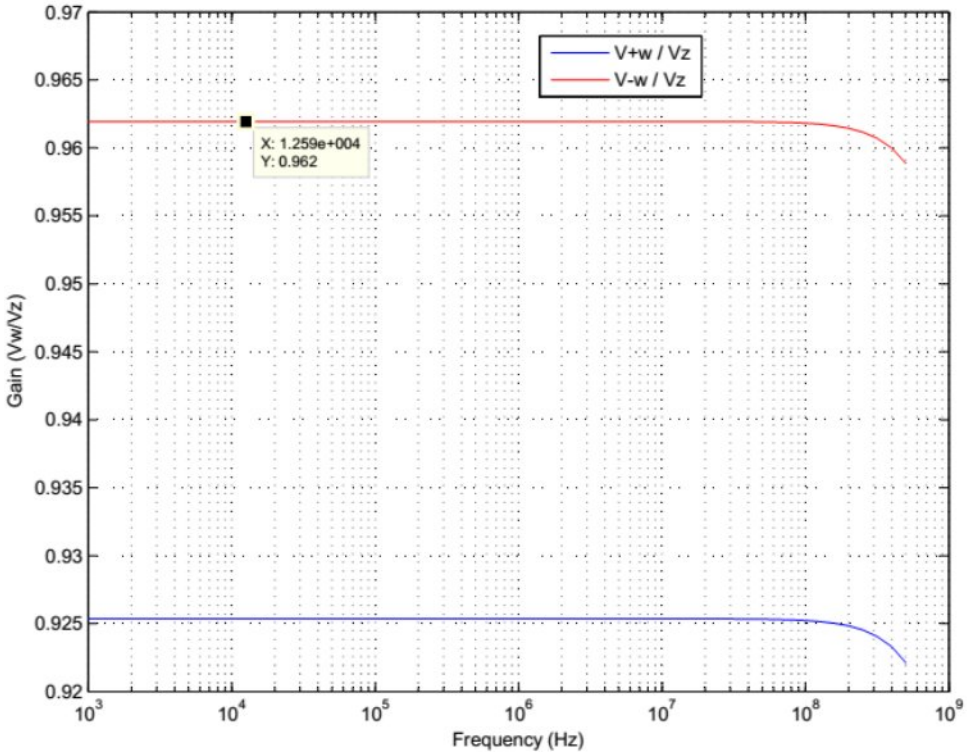


(b)

Fig. 5-7 DC Characteristics of DO-VDBA (a) Input Characteristics (b) Output Characteristics



(a)



(b)

Fig. 5-8 AC Characteristics of DO-VDBA (a) Input Characteristics (b) Output Characteristics

5.4 REALIZATION OF WAVE ACTIVE FILTER USING VDBA

Resistively terminated LC ladder filters show very low sensitivity to parameter variations. But because of difficulty involved in implementation of passive inductor, there are several methods to obtain simulated active inductor. Wave Active approach is a one such method discussed in chapter 4. In this section a voltage mode wave active filter is realized by using novel active block VDBA.

5.4.1 Wave Equivalent for series arm inductor:

VDBA is an attractive novel active device for voltage mode applications because of its high input and low output resistance. To design wave active filter, the design equations for elementary series inductor 'L'as presented in Eq. (4.28) are repeated here for convenience:

$$\square_{\square} \; \square \; \square_{\square} \; \overline{\frac{\square}{\square\square\square}} \square\square_{\square} \; \overline{\square_{\square}\square} \tag{5.3.1}$$

$$\square_{\square} \; \square \; \square_{\square} \; \square \; \frac{\square}{\square\square\square} \square\square_{\square} \; \overline{\square_{\square}\square} \tag{5.3.2}$$

where $\square \; \square \; \frac{\square}{\square\square}$ and R is port normalization resistance.

It is apparent from these equations that to realize wave equivalent of series inductor only three components are needed:

i) Summer circuit

ii) Subtractor circuit

iii) Lossy subtracting integrator

5.4.1.1 Summer circuit based on VDBA

A summer circuit is used for adding two voltages. VDBA based summer circuit is shown in Fig. 5.9. Here two DO-VDBAs are used. The regular analysis of first DO-VDBA block is as follows:

$$\square_{\square\square} \; \square \; \square_{\square \; \square}\square\square \; \overline{\square_{\square}\square\square} \; \overline{\square_{\square \; \square}\square_{\square}}$$

□□ □ □□□□ □ □□ □□□□

For □□ □□□ □ □, □□□ □ □□

or □□ □□□ □ □□□ □ □□

similarly, following the same approach it can be shown that

□□□□ □ □□ □ □□ (5.4)

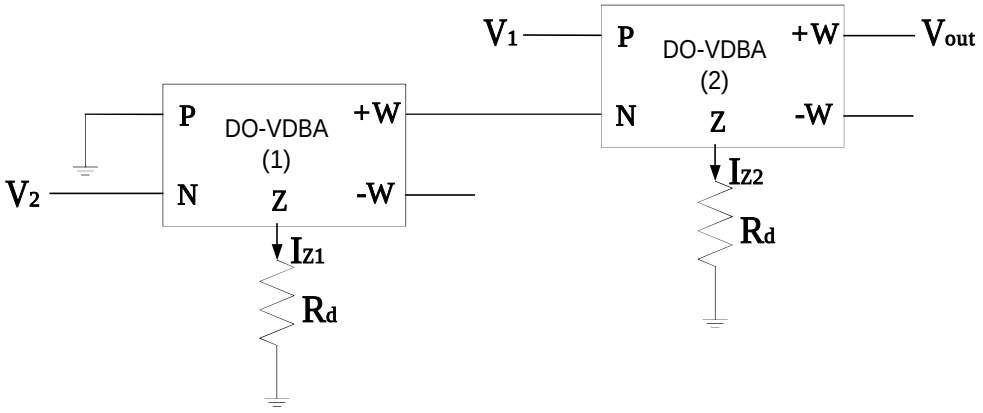


Fig. 5-9 Summer circuit using DO-VDBA

The simulation result for the summer circuit is shown in Fig. 5.10.

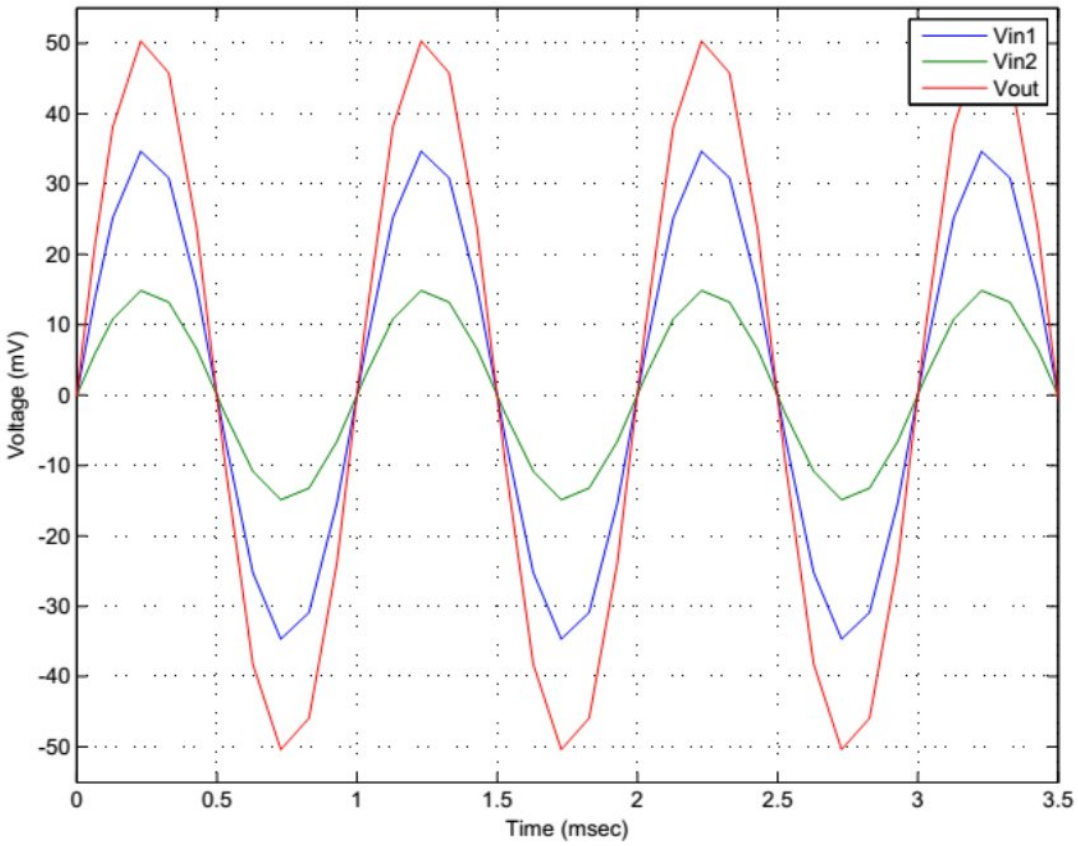


Fig. 5-10 Simulation Result of DO-VDBA based Summer circuit

5.4.1.2 Subtractor circuit based on VDBA

A subtractor circuit based on DO-VDBA is shown in Fig. 5.11. Here two subtracting output is obtained at +w and –w terminal which are equal in magnitude but opposite in sign. The output equations of subtractor circuit are as follows:

$$?_{??} \; ? \; ??_{?} \; \overline{?_{?}} \; ? \tag{5.5.1}$$

$$?_{??} \; ? \; \overline{??_{?}} \; \overline{?_{?}} \; ? \tag{5.5.2}$$

With $?_{?} \; ?_{?} \; ? \; ?$.

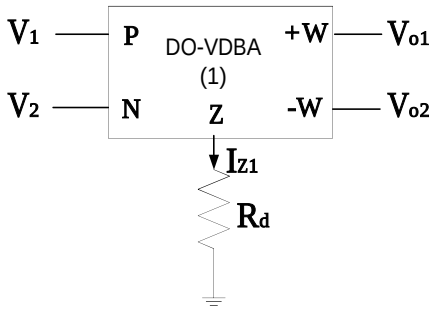


Fig. 5-11 Subtractor circuit using DO-VDBA

The inverter circuit can be obtained from the subtractor circuit with grounding the input 'p' terminal. The simulation results for subtractor and inverter circuit are shown in Fig. 5-12 and 5-13 respectively.

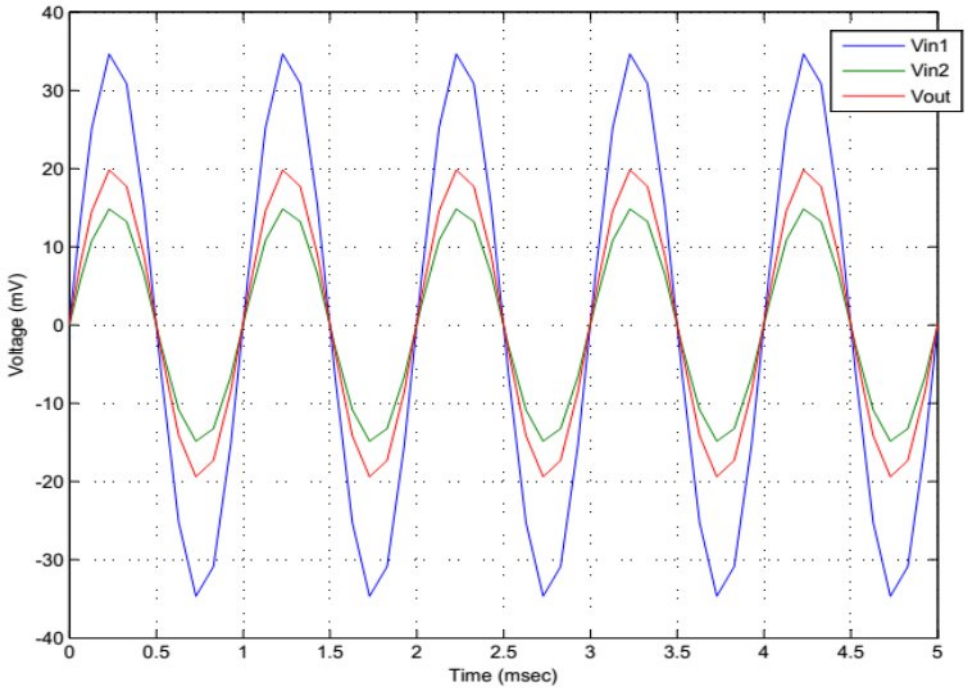


Fig. 5-12 Simulation Result of DO-VDBA based subtractor

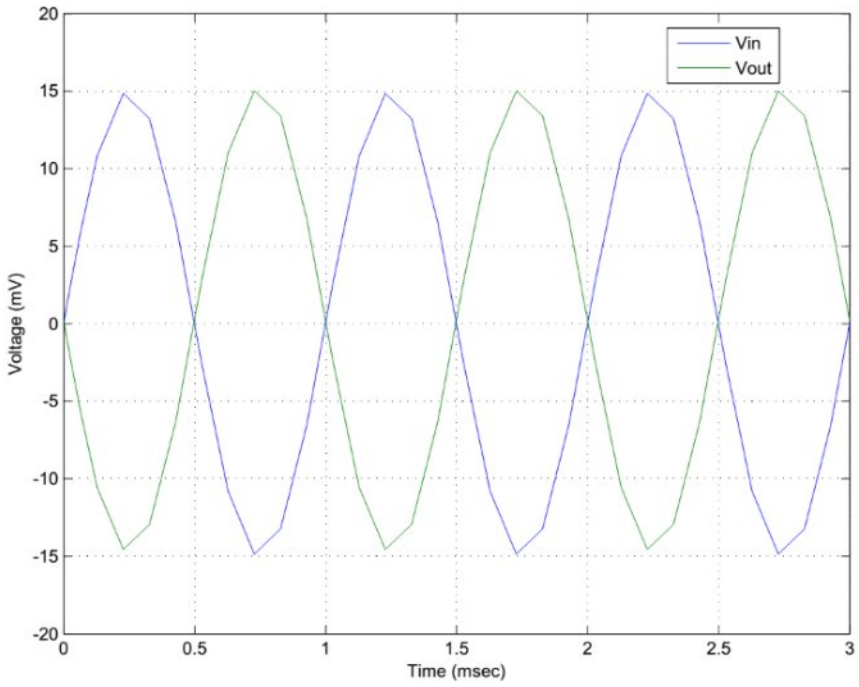


Fig. 5-13 Simulation Result of DO-VDBA based Inverter circuit

5.4.1.3 Lossy subtracting Integrator circuit by using VDBA

VDBA based lossy subtracting integrator is depicted in Fig. 5-14. It contains only one active block of DO-VDBA. The routine analysis of the circuit shows that:

$$?_{???} ? \frac{?}{?? ??} ??_{?} \quad \overline{?_{?}} ? \tag{5.6}$$

Where $\tau = ?_{?} ?_{?}$ and $?_{?} ?_{?} ? ?$.

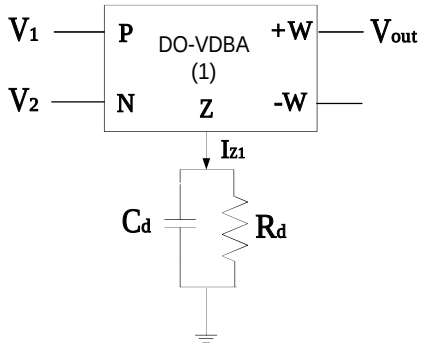
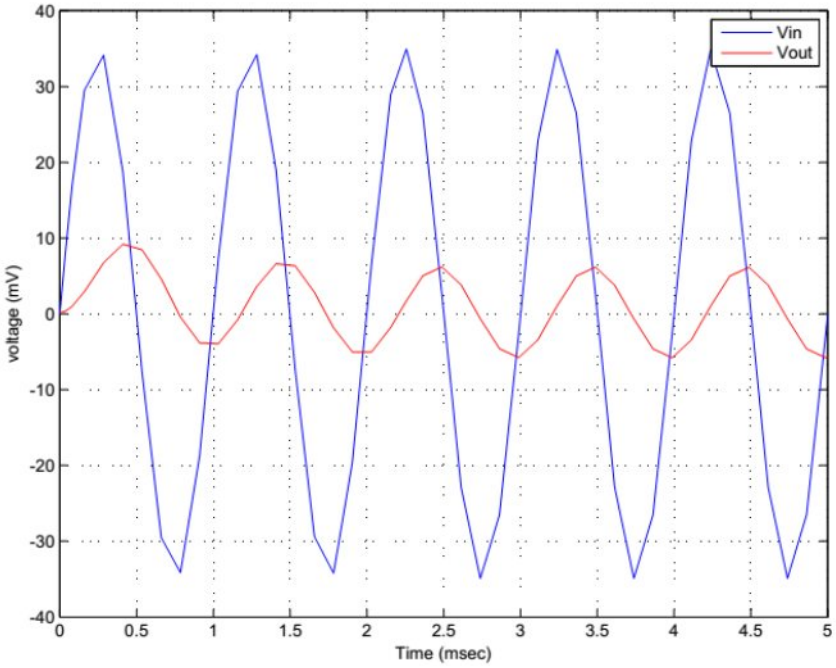
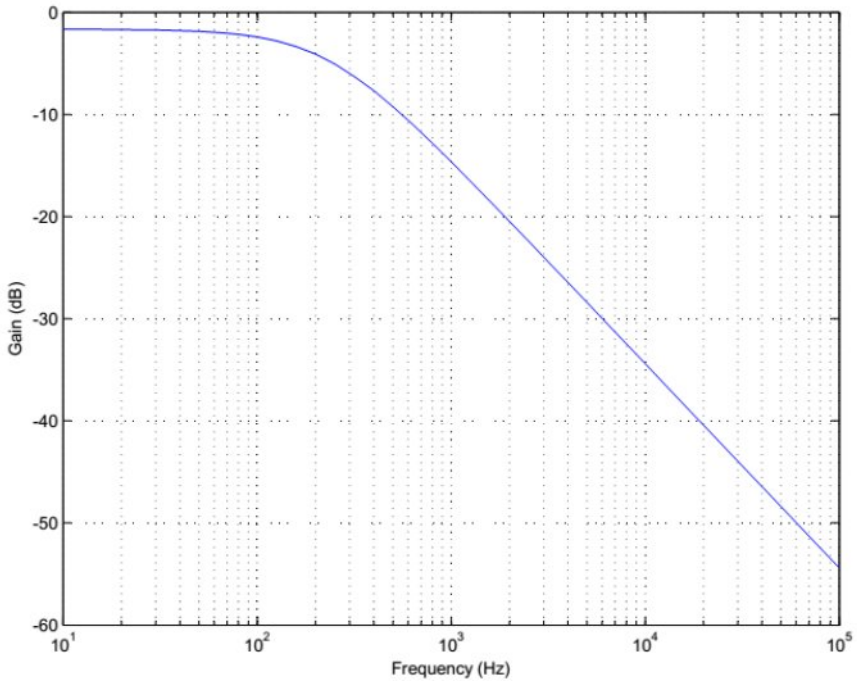


Fig. 5-14 Lossy integrator based on DO-VDBA

The frequency and transient response for lossy integrator is shown in Fig. 5-15 in which the second input $?_?$ is made grounded.



(a)



(b)

Fig. 5-15 Simulation Result of Lossy integrator (a) AC response (b) Transient Response

Now the wave equivalent of the series arm inductor can be obtained by combining all the above blocks: lossy integrator, summer and subtractor, as shown in Fig. 5-20, whose terminal characteristics are defined by Eq. 5.3. In Fig. 5-16, three DO-VDBA, three resistances and one grounded capacitor are used. The first block provides subtracting lossy integrating output with two opposite signs at output terminal w+ and w- respectively. The second block performs subtraction operation with $?_?$ and output available at w+ terminal of block (1) and produce desired output $?_?$. Similarly the third block produces output $?_?$ which completes the realization of series inductor.

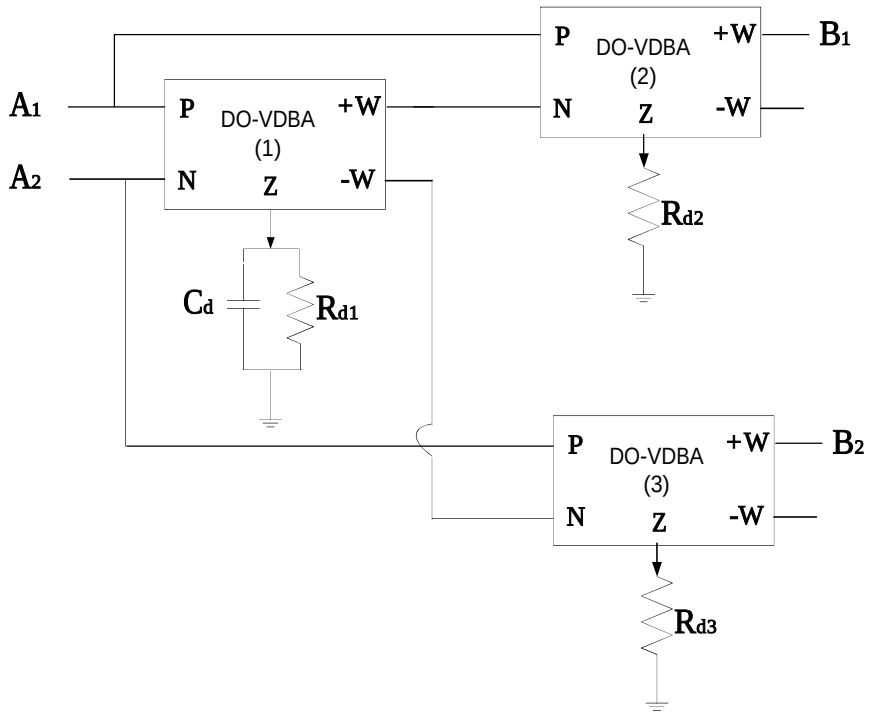


Fig. 5-16 Realization of Wave Equivalent for Series Inductor Using DO-VDBA

The required value of capacitor $?_?$ for the design of wave equivalent of series inductor 'L' can be obtained by equating the values of τ from Eq. (5.3) and (5.6) as

$$?_?\,?_?\;?\;\frac{?}{??}$$

where R is port normalization resistance. Taking $?\;?_?$, the value of $?_?$ will be

$$?_?\;?\;\frac{?}{??_?^?} \qquad (5.7)$$

5.4.2 Wave Equivalent for Shunt arm Capacitor

As it is clear from the Table 4-2 that wave equivalent for shunt arm capacitor is same as wave equivalent of series arm inductor except an inverted input and output terminal. In general WAE for shunt capacitor can be realized with WAE of series inductor with combining two additional inverters but as DO-VDBA is used here as an active device, only one extra inverter for the input is needed and other inverted output can be obtained from –w terminal of block (2) as shown in Fig. 5.17.

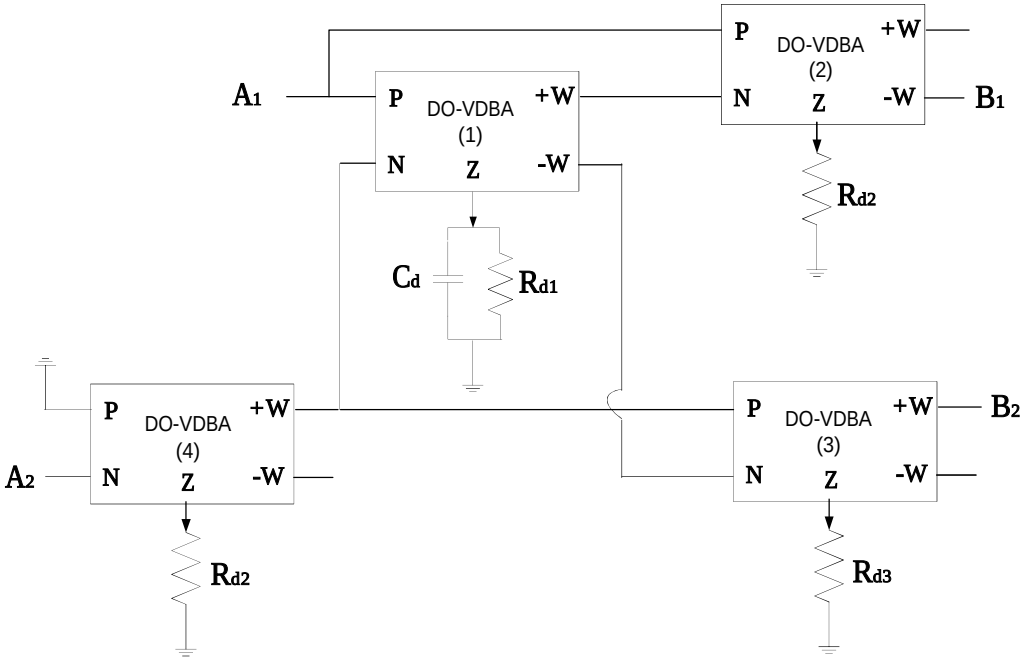


Fig. 5.17 Realization of wave equivalent for shunt capacitor using DO-VDBA

The terminal characteristics for the wave equivalent of shunt arm capacitor 'C' can be presented as Eq. (4.16) which is repeated here for convenience:

$$\overline{B_2} = \frac{}{} \frac{}{} + \frac{}{} \overline{}\ (5.8.1)$$

$$= \frac{}{} \frac{}{} + \frac{}{} \overline{}\ (5.8.2)$$

where = .

Again design value of C_2 can be obtained by equating the value of C in Eq. (5.6) and (5.8) and taking $C = C_2$. The required value of C_2 for wave equivalent of shunt arm capacitor is

$$C_2 = \frac{C}{2} \tag{5.9}$$

5.4.3 Realization of 4th order Wave Active Filters

To make clear the concept of wave active filter, a fourth order low pass prototype of LC ladder as shown in Fig. 5-18 is simulated with wave equivalents. The series inductors and parallel capacitors are replaced by their wave equivalents as given in Table 4-1 and 4-2. The complete schematic wave flow diagram is shown in fig. 5-19. To obtain a Butterworth low pass response the normalized component values are Rs = 1, L_1 = 0.7654, L_2 = 1.8485, C_1 = 1.8485, C_2 = 0.7654 and R_L = 1.

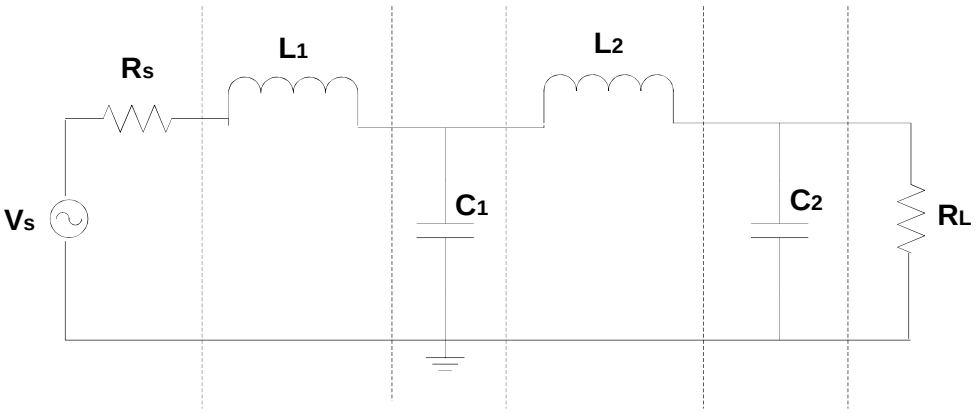


Fig. 5-18 4th order LC ladder low pass prototype

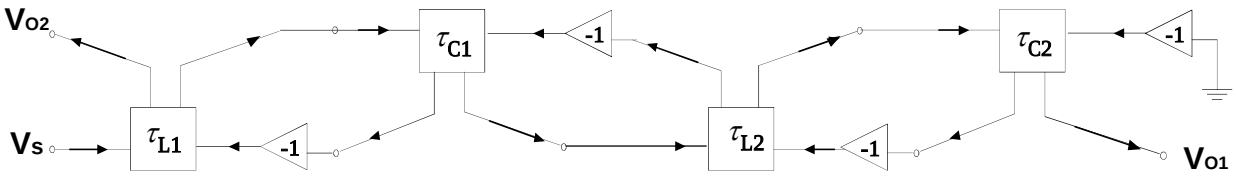


Fig. 5-19 Wave equivalent of low pass prototype

The fourth order low pass filter is designed for the cut off frequency f_0 = 1.59 MHz. DO-VDBA based wave equivalents for series inductor and shunt capacitor are replaced in the schematic diagram of Fig. 5-19. The required value of the capacitance of series arm inductors (L_1 and L_2) are 18.4pF and 44.378pF and for shunt arm capacitors (C_1 and C_2) are 44.362pF and 18.369 pF

respectively. The port resistances are taken as 2.085 kΩ. The frequency and transient response for low pass filter are shown in Fig 5-20 and Fig. 5-21 respectively.

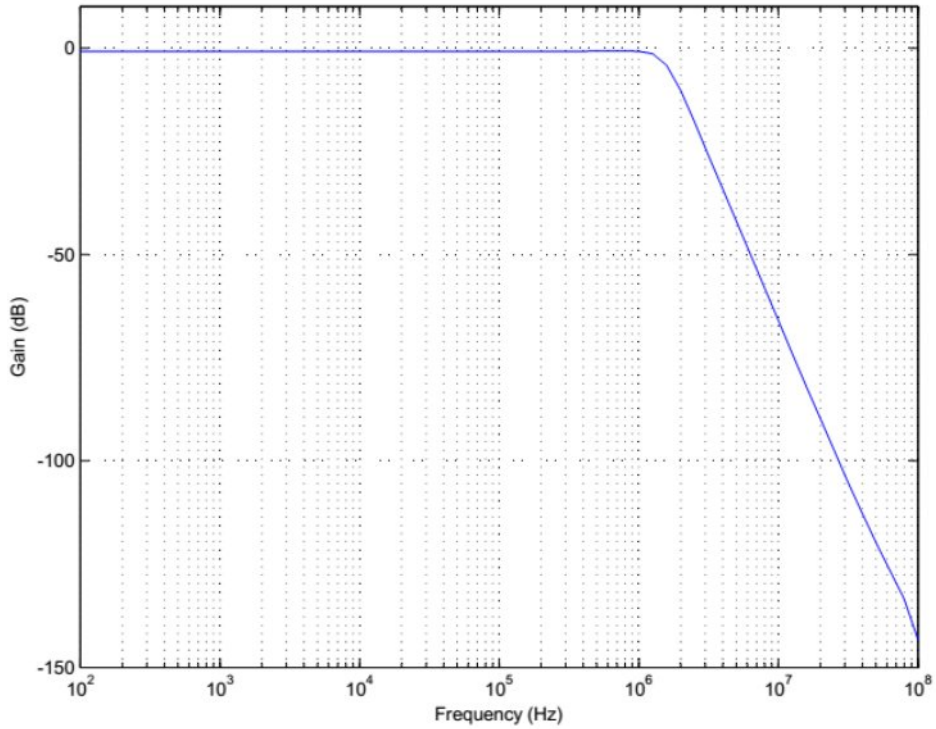


Fig. 5-20 Frequency response of Low Pass Filter

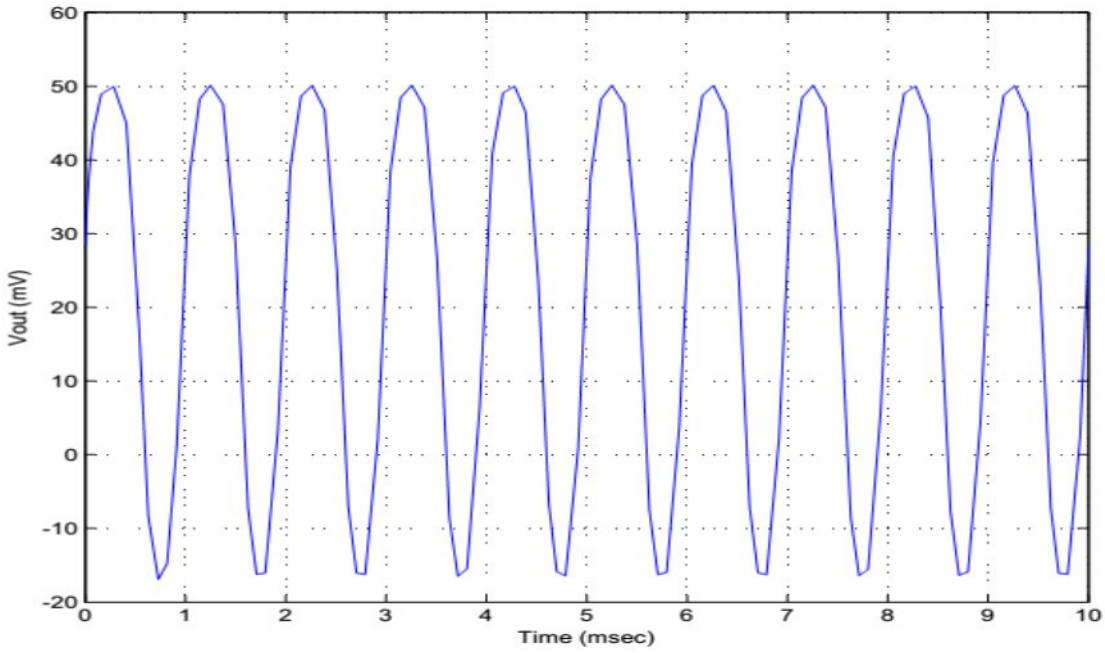


Fig. 5-21 Transient response of Low Pass Filter

As stated before, for equal port normalization resistance wave active approach provide complementary outputs. Thus frequency and transient response of high pass filter are presented in Fig. 5-22 and Fig. 5-23 respectively.

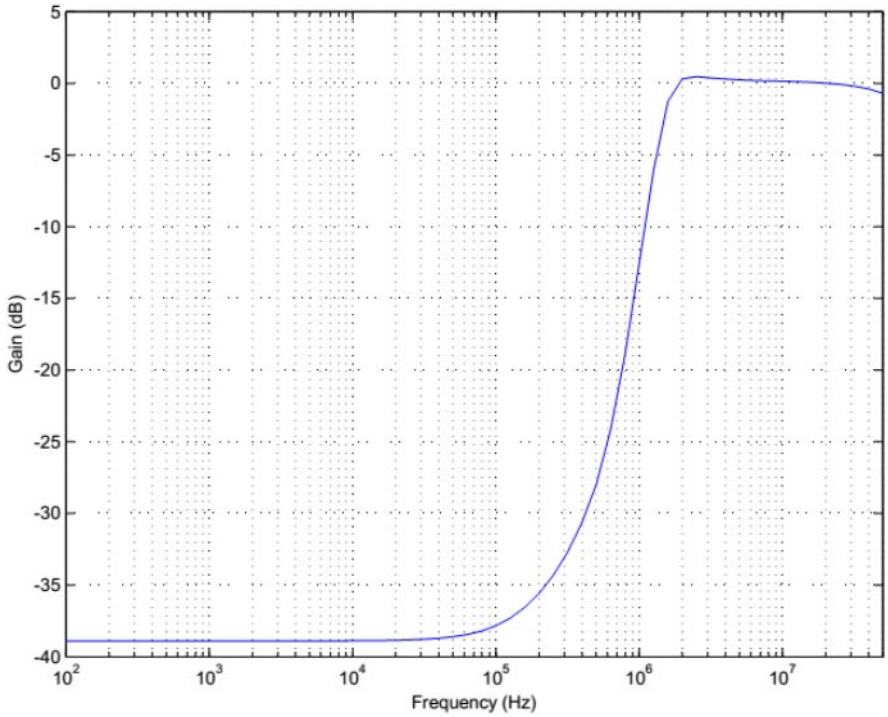


Fig. 5-22 Frequency Response of High Pass Filter

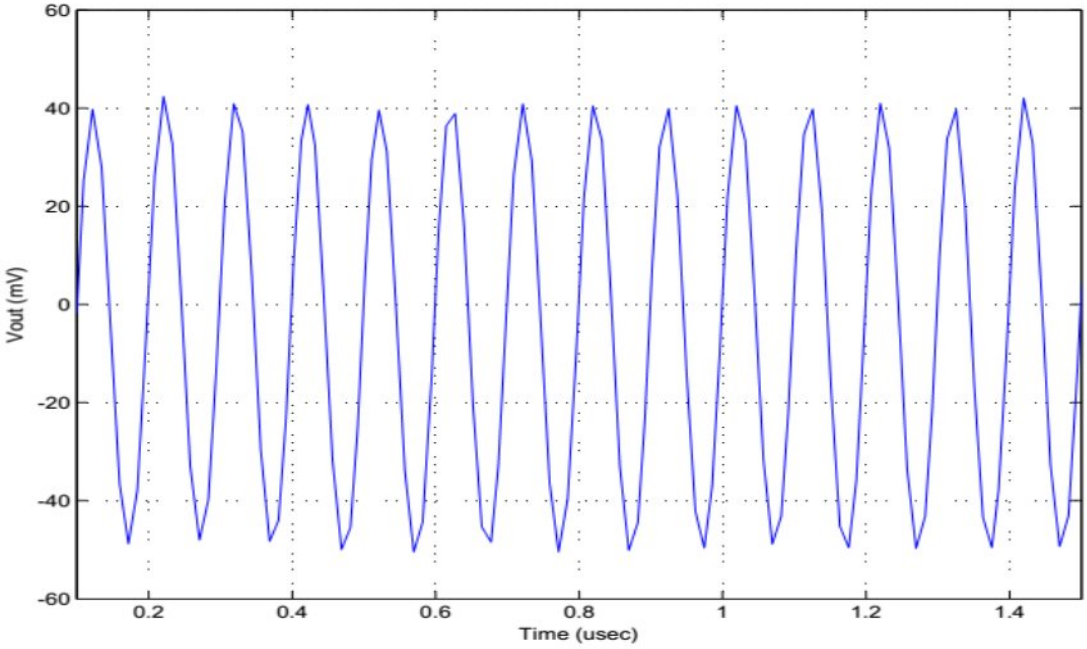


Fig. 5-23 Transient Response of High Pass Filter

5.5 CONCLUSION

This chapter includes the major work of the dissertation. First a newly presented active block voltage differencing buffered amplifier (VDBA) along with its terminal characteristics is discussed. Then its CMOS realization of VDBA and its DC and AC input-output characteristics are shown. After that, its modified version Dual Output Voltage Differencing Buffered Amplifier (DO-VDBA) along with its CMOS realization and input –output characteristics is discussed. Several fundamental applications such as adder, subtractor, inverter and integrator by using DO-VDBA are presented and finally wave equivalent of series arm inductor is designed. The wave equivalent of other elementary block such as shunt capacitor is also presented. A 4^{th} order low pass LC ladder filter for a cut off frequency of 1.59 MHz is simulated by using wave approach based on DO-VDBA. The simulation results show that cut off frequency of low pass and high pass filters are 1.53MHz and 1.50 MHz respectively which is a clear agreement with theoretically obtained results.

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CHAPTER 6

CONCLUSION AND FUTURE SCOPE

In the present work, higher order analog filters are designed using wave active approach. Voltage differencing buffered amplifier as an active block is used to realize filter structures.

In chapter 1 an introduction of filters are discussed. Several classification based on different attributes are discussed. Different characteristics of filters along with major design issues related to active filter design are presented.

In Chapter 2 several method of designing higher order filters are discussed. These methods can be classified broadly in three categories cascade design, multiple loop feedback method and LC ladder simulation techniques. Cascade design approach offers some desired features such as modularity, simply realizable structure and good tuning properties but the performance of filters designed via this technique degrades when the order of filter is exceeded to eight. Another technique for higher order filter realization is multiple loop feedback approach which shows better results as per sensitivity point of view than cascade design approach. The last method of realizing higher order filter is to simulate LC ladder structure. This method is used to achieve stringent requirements of sensitivity. The LC ladder simulation method is further divided into three parts: element replacement method, operational simulation and wave approach. The first two methods out of three to simulate LC ladder are discussed in brief.

In chapter 3, a brief introduction of some of the active devices that are used to implement wave active filter so far, is presented. These devices include OTA, CFOA, DVCCTA, DVCCCTA, CCDDCCTA, OTRA and VDTA. All of these devices are briefly discussed along with their symbolic representation and terminal characteristics.

Chapter 4 is dedicated to a detailed discussion of wave active approach of designing higher order filter. Wave approach is a type of LC ladder simulation technique. In this technique, passive elements of LC ladder i.e. series/ shunt inductors and shunt/series capacitors are first divided into several basic two port networks (i.e. series inductor or shunt capacitor) and then each two port network is replaced with their wave equivalents. As this method is based on LC ladder simulation,

it retains the property of very low sensitivity to parameter variations. Along with this, wave active filter shows some attractive features like modular structures, use of only lossy integrators, simple design methodology and power complementary responses etc. Several wave active filters using different active building blocks are available in open literature, out of them two wave active filter structures based on two different active devices i.e. current feedback operational amplifier (CFOA) and differential voltage current conveyor transconductance amplifier (DVCCTA) are also presented. Simulation results obtained via PSPICE for both wave active filters based on CFOA and DVCCTA are also shown.

In Chapter 5 a recently proposed ABB named as voltage differencing buffered amplifier (VDBA) is discussed. The CMOS realization of VDBA along with its terminal characteristics is presented. The two different versions of VDBA: dual output voltage differencing buffered amplifier (DO-VDBA) and fully balanced voltage differencing buffered amplifier (FB-VDBA) along with their CMOS realizations and terminal characteristics are also presented. Then a new VDBA based wave active filter is proposed. A 4^{th} order Butterworth low pass filter is designed for cut off frequency of 1MHz. The simulation work is done on PSPICE which shows a clear agreement with the desired theoretical results.

Scope for future work:

Wave active filters offer certain advantages over other methods for designing higher order filters. In the present work VDBAs have been used to design a WAF. We have selected a very simple and generic structure of VDBA. The wave equivalents are derived on this structure. Some of the directions in which the work presented in this dissertation can be extended are listed below:

1. Optimization of the filter structure in terms of active and passive components.

2. Employment of only grounded passive elements.

3. A resistorless structure can be obtained.

4. Realization of other type of filter responses such as Band pass and Band stop.

APPENDICES

APPENDIX I

PSPICE model file used for Process and electrical parameters CMOS 0.35 um from TSMC Technology

.MODEL nmos_transistor NMOS (LEVEL=7 MOBMOD=1.000e+00 CAPMOD=2.000e+00 NLEV=0 NOIMOD=1.000e+00

+K1=6.044e-01 K2=2.945e-03

+K3=-1.72e+00 K3B=6.325e-01 NCH=2.310e+17 VTH0=4.655e-01 VOFF=-5.72e-02 DVT0=2.227e+01 DVT1=1.051e+00 DVT2=3.393e-03

+KETA=-6.21e-04 PSCBE1=2.756e+08 PSCBE2=9.645e-06 DVT0W=0.000e+00 DVT1W=0.000e+00 DVT2W=0.000e+00 UA=1.000e-12 UB=1.723e-18

+UC=5.756e-11 U0=4.035e+02 DSUB=5.000e-01 ETA0=3.085e-02 ETAB=-3.95e-02 NFACTOR=1.119e-01 EM=4.100e+07 PCLM=6.831e-01

+PDIBLC1=1.076e-01 PDIBLC2=1.453e-03 DROUT=5.000e-01 A0=2.208e+00 A1=0.000e+00 A2=1.000e+00 PVAG=0.000e+00 VSAT=1.178e+05

+AGS=2.490e-01 B0=-1.76e-08 B1=0.000e+00 DELTA=1.000e-02 PDIBLCB=2.583e-01 W0=1.184e-07 DLC=4.000e-09 DWB=0.000e+00 DWG=0.000e+00

+LL=0.000e+00 LW=0.000e+00 LWL=0.000e+00 LLN=1.000e+00 LWN=1.000e+00 WL=0.000e+00 WW=0.000e+00 WWL=0.000e+00 WLN=1.000e+00

+WWN=1.000e+00 AT=3.300e+04 UTE=-1.80e+00 KT1=-3.30e-01 KT2=2.200e-02 KT1L=0.000e+00 UA1=0.000e+00 UB1=0.000e+00 UC1=0.000e+00

+PRT=0.000e+00 CGDO=1.120e-10 CGSO=1.120e-10 CGBO=1.100e-10 CGDL=1.350e-10 CGSL=1.350e-10

+CKAPPA=6.000e-01 CF=0.000e+00 ELM=5.000e+00 XPART=1.000e+00 CLC=1.000e-15 CLE=6.000e-01 RDSW=6.043e+02

+CDSC=0.000e+00 CDSCB=0.000e+00

+CDSCD=8.448e-05 PRWB=0.000e+00 PRWG=0.000e+00 CIT=1.000e-03 TOX=7.700e-09 NGATE=0.000e+00 NLX=1.918e-07 ALPHA0=0.000e+00

+BETA0=3.000e+01 AF=1.400e+00 KF=2.810e-27 EF=1.000e+00 NOIA=1.000e+20 NOIB=5.000e+04 NOIC=-1.40e-12 LINT=-1.67e-08

+WINT=2.676e-08 XJ=3.000e-07 RSH=8.200e+01 JS=2.000e-05 CJ=9.300e-04 CJSW=2.800e-10 CBD=0.000e+00 CBS=0.000e+00 IS=0.000e+00

+MJ=3.100e-01 N=1.000e+00 MJSW=1.900e-01 PB=6.900e-01 TT=0.000e+00 PBSW=6.900e-01)

.MODEL pmos_transistor PMOS (LEVEL=7 MOBMOD=1.000e+00 CAPMOD=2.000e+00 NLEV=0 NOIMOD=1.000e+00 K1=5.675e-01 K2=-4.39e-02

+K3=4.540e+00 K3B=-8.52e-01 NCH=1.032e+17 VTH0=-6.17e-01 VOFF=-1.13e-01 DVT0=1.482e+00 DVT1=3.884e-01 DVT2=-1.15e-02

+KETA=-2.56e-02 PSCBE1=1.000e+09 PSCBE2=1.000e-08 DVT0W=0.000e+00 DVT1W=0.000e+00 DVT2W=0.000e+00 UA=2.120e-10 UB=8.290e-19

+UC=-5.28e-11 U0=1.296e+02 DSUB=5.000e-01 ETA0=2.293e-01 ETAB=-3.92e-03 NFACTOR=8.237e-01 EM=4.100e+07 PCLM=2.979e+00

+PDIBLC1=3.310e-02 PDIBLC2=1.000e-09 DROUT=5.000e-01 A0=1.423e+00 A1=0.000e+00 A2=1.000e+00 PVAG=0.000e+00 VSAT=2.000e+05

+AGS=3.482e-01 B0=2.719e-07 B1=0.000e+00 DELTA=1.000e-02 PDIBLCB=-1.78e-02 W0=4.894e-08 DLC=4.000e-09 DWB=0.000e+00 DWG=0.000e+00

+LL=0.000e+00 LW=0.000e+00 LWL=0.000e+00 LLN=1.000e+00 LWN=1.000e+00 WL=0.000e+00 WW=0.000e+00 WWL=0.000e+00 WLN=1.000e+00

+WWN=1.000e+00 AT=3.300e+04 UTE=-1.35e+00 KT1=-5.70e-01 KT2=2.200e-02 KT1L=0.000e+00 UA1=0.000e+00 UB1=0.000e+00 UC1=0.000e+00

+PRT=0.000e+00 CGDO=7.420e-11 CGSO=7.420e-11 CGBO=1.100e-10 CGDL=1.290e-10 CGSL=1.290e-10

+CKAPPA=6.000e-01 CF=0.000e+00 ELM=5.000e+00 XPART=1.000e+00 CLC=1.000e-15 CLE=6.000e-01 RDSW=1.853e+03

+CDSC=6.994e-04 CDSCB=2.943e-04 CDSCD=1.970e-04 PRWB=0.000e+00 PRWG=0.000e+00 CIT=1.173e-04 TOX=7.700e-09

+NGATE=0.000e+00 NLX=1.770e-07 ALPHA0=0.000e+00 BETA0=3.000e+01 AF=1.290e+00 KF=1.090e-27 EF=1.000e+00 NOIA=1.000e+20

+NOIB=5.000e+04 NOIC=-1.40e-12 LINT=-8.14e-08 WINT=3.845e-08 XJ=3.000e-07 RSH=1.560e+02 JS=2.000e-05

+CJ=1.420e-03 CJSW=3.800e-10 CBD=0.000e+00 CBS=0.000e+00 IS=0.000e+00

+MJ=5.500e-01 N=1.000e+00 MJSW=3.900e-01 PB=1.020e+00 TT=0.000e+00 PBSW=1.020e+00)

APPENDIX II

PSPICE model file used for Process and electrical parameters CMOS 0.18 um from TSMC Technology

.MODEL nmos_transistor NMOS(LEVEL = 3

+ TOX = 5.7E-9 NSUB = 1E17 GAMMA = 0.4317311

+ PHI = 0.7 VTO = 0.4238252 DELTA = 0

+ UO = 425.6466519 ETA = 0 THETA = 0.1754054

+ KP = 2.501048E-4 VMAX = 8.287851E4 KAPPA = 0.1686779

+ RSH = 4.062439E-3 NFS = 1E12 TPG = 1

+ XJ = 3E-7 LD = 3.162278E-11 WD = 1.232881E-8

+ CGDO = 6.2E-10 CGSO = 6.2E-10 CGBO = 1E-10

+ CJ = 1.81211E-3 PB = 0.5 MJ = 0.3282553

+ CJSW = 5.341337E-10 MJSW = 0.5)

.MODEL pmos_transistor PMOS(LEVEL = 3

+ TOX = 5.7E-9 NSUB = 1E17 GAMMA = 0.6348369

+ PHI = 0.7 VTO = -0.5536085 DELTA = 0

+ UO = 250 ETA = 0 THETA = 0.1573195

+ KP = 5.194153E-5 VMAX = 2.295325E5 KAPPA = 0.7448494

+ RSH = 30.0776952 NFS = 1E12 TPG = -1

+ XJ = 2E-7 LD = 9.968346E-13 WD = 5.475113E-9

+ CGDO = 6.66E-10 CGSO = 6.66E-10 CGBO = 1E-10

+ CJ = 1.893569E-3 PB = 0.9906013 MJ = 0.4664287

+ CJSW = 3.625544E-10 MJSW = 0.5)