CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

The present work deals with voltage differencing current conveyor and its application in signal processing. There had been several major developments in the area of analog circuits and signal processing which have taken place during the past four decades. There is a bulk of material available about the various active blocks developed post Current Conveyors. In this dissertation an attempt has been made to highlight some of basic circuits and voltage differencing current conveyor (VDCC) based applications in analog signal processing.

Introduction of Current Conveyor was necessary because of limitations posed by the traditional Operational amplifier which is a highly versatile element [1]. With op-amps many circuits, both linear and non-linear, can be realized successfully. Extensive research had been carried out from mid-sixties to mid-eighties on the design of various linear and non-linear analogue circuits using integrated circuit (IC) op-amps. Since op-amp based circuits employ RC elements, their monolithic IC implementation was difficult because precise tuning of the time constant RC was difficult to implement. Moreover their limited performance due to less bandwidth, slew rate etc. forced the analog designers to look for other active blocks [2]. Switched capacitor circuits was one solution where the resistor was replaced by a periodically switched capacitor but it again posed problems like aliasing and clock feed through [3].

In eighties Operational Transconductance Amplifiers (OTA) was introduced. The OTA-C circuits employ only transconductors and capacitors to build various functional circuits and thus, do not require any resistors; moreover, their internal structure is also resistor-less, thus adding to its advantage list. In OTA circuits the

transconductance can be controlled electronically through an external DC bias voltage / current making its gain variable (programmable).

The developments in digital circuit design particularly, CMOS digital circuits, have had a profound influence on the developments in analogue circuits particularly in those cases where both digital and analogue parts are to be integrated on the same chip using the same technology (CMOS). Even though the digital systems have many advantages over the analog type the latter can't still be avoided as the natural world is analog. The various developments in the field of integrated circuit (IC) technology, again, posed various challenges to analog designers to match the analog system with their fast growing digital counterparts. It is such requirements which have resulted in continued research on efficient analog circuit designs especially current-mode (CM) techniques and circuits for evolution of elegant and efficient solutions to many contemporary problems in mixed-mode circuit design problems. The current mode approach to signal processing is often considered to have one or more of the following advantages: higher frequency range of operation, lower power consumption, higher slew rates, improved linearity and better accuracy. Before describing the developments in analog signal processing and circuit designs we will first analyze some of the basics of signal processing.

1.2 ANALOG AND DIGITAL SIGNAL PROCESSING

The signal processing operations involved in many applications like communication systems, control systems, instrumentation and biomedical signal processing etc. can be implemented in two different ways

(1) Analog or continuous time method and

(2) Digital or discrete time method.

The analog approach to signal processing was dominant for many years and it uses analog circuit elements such as resistors, capacitors, transistors, diodes etc. With the advent of digital computer and later microprocessor, the digital signal processing has become dominant now a days. The analog signal processing is based on natural ability of the analog system to solve differential equations that describe a physical system. The solutions are obtained in real time. In contrast digital signal processing relies on numerical calculations. The method may or may not give results in real time. The digital approach has two main advantages over analog approach

(1) Flexibility: Same hardware can be used to do various kind of signal processing operation, while in the core of analog signal processing one has to design a system for each kind of operation.

(2) Repeatability: The same signal processing operation can be repeated again and again giving same results, while in analog systems there may be parameter variation due to change in temperature or supply voltage. Added to these, digital signal processing has many advantages added to its list like, better noise immunity than analog signals. They are compact and much cheaper than their analog counterpart. Digital signals can be encrypted so that only the intended receiver can decode it. It Enables transmission of signals over a long distance and it enables multi-directional transmission simultaneously [5].

Taking these advantages into account, the designers are forced to look for digital solutions rather than analog in VLSI systems. Even then, analog circuits are fundamentally necessary in many of today's complex, high performance systems. This is caused by the reality that naturally occurring signals are analog. Practically all signals in the physical world are continuous in both amplitude and time, and hence always analog techniques will be required for conditioning of such signals before they can be processed by digital signal processing circuits. Therefore analog circuits act as a bridge between the real world and digital systems. Another important reason for the existence of analog signal processing is the bandwidth, which can be some order of magnitudes higher, if the signal is processed in analog circuits than in digital.

1.3 CURRENT MODE AND VOLTAGE MODE SIGNAL PROCESSING

Any signal processing done in electric or electronic circuits is performed by means of more or less organized movement of charge, where voltages and currents are usually the variables and time, resistances, capacitances and inductances are parameters of the circuit defining the properties of the signal processing. The main reason for using only voltages and currents in analog signal processing is that active devices, which are exploited in analog electronics, operate mostly with resistances (conductance), as parameters for controlling the signal processing. The signal is then processed by miscellaneous voltage-current and current-voltage conversions, amplification, weighted addition and multiplication, etc. [4]. Historically voltage has been used as the main variable for signal processing, probably because the thinking in

terms of voltages is easier and simpler for the designers, than the thinking in terms of currents. However, during the years the analog electronics became practically only voltage processing and most of the building blocks used in analog electronics (like op-amps) are typical voltage processing circuits.

In order to increase the speed of circuits for analog signal processing and to decrease the supply voltages of integrated circuits, designers devote their attention to the so-called current mode. Here the individual circuit elements should interact by means of currents and not with voltages.

The difference between voltage and current processing circuits is that a single output terminal of a current processing block is able to supply only a single input terminal**,** since the inputs of current processing blocks can't be arranged into a serial connection. Therefore, if more input terminals are required to be supplied by the same input signal, it is necessary to design current processing building blocks with multiple outputs giving the same output signal while in voltage processing circuits a single voltage-output terminal can supply more voltage-input terminals connected in parallel.

1.4 OUTLINE OF THE WORK PRESENTED IN THE DESERTATION

In this dissertation, chapter 1 covers the basic concepts of analog signal processing. The current and voltage mode processing is also discussed. In the second chapter, basic circuits which are used to derive the active building blocks are described in detail. Current conveyors and its derivatives with symbolic notation and characteristics are also covered in the second chapter.

Third chapter covers the basic description of VDCC and general functions of analog signal processing. Grounded and floating inductors are also verified by filter design application using PSPICE simulation.

In the fourth chapter, the proposed multifunction biquad filter using VDCC which verifies the workability of VDCC in analog signal processing.

REFERENCES

1. Smith, K.C. and Sedra, A. S., “The current conveyor: a new circuit building block. IEEE Proc. CAS, 1968, vol. 56, no. 3, p. 1368-1369.
2. Kuntman, H. A. “New Advances and Possibilities in Active Circuit Design” 10th International Conference on Development and Application Systems, Suceava, Romania, May 27-29, 2010
3. Schaumann, R. and Valkenberg, M. E. “Design of Analog Filters”, Oxford University Press, 2004.
4. Biolek D., Senani R., Biolkova V. and Kolka Z., “Active Elements for Analog Signal Processing: Classification, Review and New Proposals”, Radioengineering, Vol. 17, N0. 4, Dec. 2008.
5. Igor M., “New Circuit Principles for Integrated Circuits”, Part 2: Special Function Blocks for Analog Current Signal Processing, PhD Thesis, Brno University of Technology, 2010.

CHAPTER 2

CONSTITUTIVE CIRCUITS USED IN MODERN BIPOLAR/CMOS ACTIVE BUILDING BLOCKS

Hundreds of Bipolar/CMOS active building blocks have been proposed in the domain of analog signal processing by different research groups around the world during the past three-four decades. A very comprehensive summary of these blocks has been given in [1] and the references cited therein. After reviewing the circuit implementation of these blocks, it has been observed that these blocks utilize one or more of the following constitutive blocks

(i) Differential amplifier

(ii) Current mirrors

(iii) Active loads

(iv) Voltage buffers (translinear)

(v) Operational transconductance amplifier

In this chapter, we present these constitutive blocks and their important features.

2.1 DIFFERENTIAL PAIR

The differential pair or amplifier configuration is widely used active block in analog signal processing. In the case of operational amplifier, the input stage is a differential amplifier. With evolution of integrated circuits, differential amplifier has become widely popular in both bipolar and MOS technologies [2] because of its excellent properties of common mode signal rejection and high gain as compared to its single ended counterpart. The performance of the differential pair depends on the matching between the two sides of the circuit's parameters of the both side's

transistors. So the circuits are much less sensitive to interference and noise than single ended circuits. Differential circuits enable to bias the amplifier and to couple amplifier stages without using bypass and coupling capacitors such as those utilized in the design of discrete- circuit amplifier [2]. In IC fabrication, large capacitors are difficult to fabricate economically. A basic MOS based differential pair is shown in Fig.2.1. It consists of two matched transistors, M_1 and M_2 whose sources are connected together and biased by a constant current source ***I***. Here, current source is ideal and that it has infinite output impedance. There are two modes of operations as follows:

2.1.1 Operation in Common -Mode

In the common-mode operation, the two gate terminals are joined together and connected to the voltage V_{CM}, called the common mode voltage. In Fig.2.1 $v_{D1} = v_{D2} = V_{DD} - R_D I/2$, since both transistors are matched. By symmetry, it can be observed that the current *I* will divide equally between the two MOS transistors [2]. Thus

$$i_{D1} = i_{D2} = I/2 \qquad (2.1)$$

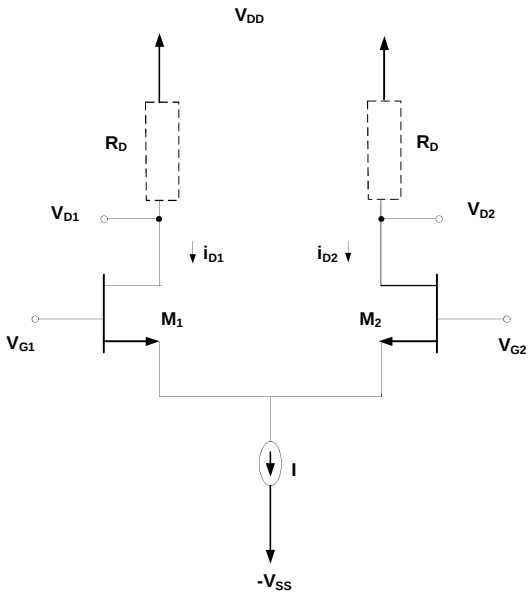


Fig.2.1 The basic MOS differential pair configuration [2]

Neglecting the channel-length modulation, the relation between gate-to-source voltage v_{GS} and a drain current is as follows:

$$\frac{\partial}{\partial} \quad \frac{\partial}{\partial}' \quad \frac{\partial}{\partial} \qquad \overline{\qquad} \qquad (2.2)$$

The voltage at each drain node will be

$$\qquad \quad \qquad \quad \overline{\frac{\partial}{\partial}} \qquad (2.3)$$

Thus the differential output voltage between the two drains will be ideally zero. In Fig. 2.1 R_D is generally realized with the help of active loads / current sources etc.

2.1.2 Operation for Differential Input

For differential input, the gate terminal V_{G2} may be set to zero and may be applied a signal V_{G1} at the gate terminal of the MOS transistor in Fig.2.1. The characteristic of differential pair is depicted in Fig. 2.2. The differential input voltage is as

$$\qquad \quad \overline{\qquad} \qquad (2.4)$$

If V_{id} is positive, V_{GS1} will be greater than V_{GS2} and hence and will be greater than. So the difference output voltage will be positive. On the other hand, If V_{GS1} is lower than V_{GS2}, i_{D1} will be smaller than i_{D2} and correspondingly V_{D1} will be greater than V_{D2}.

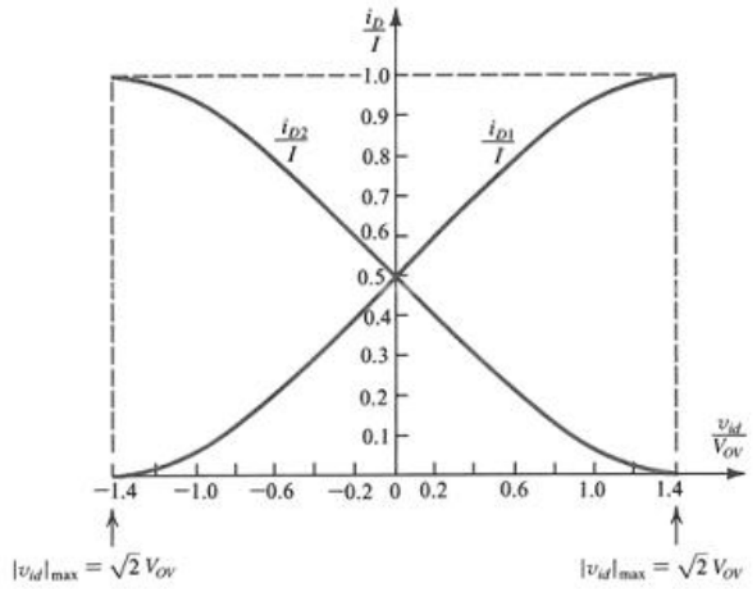


Fig. 2.2 Characteristic of CMOS based differential amplifier

2.2 CURRENT MIRROR

In IC technology, current sources play an important role to design the IC amplifier. The current sources are designed using current mirror circuits which are also widely used to derive several active building blocks are discussed in [1]. The basic BJT based npn current mirror is shown in Fig.2.3 where $R_o = r_{o2}$(output resistance of Q2). For the analysis of this circuit, we assume that both the transistors are identical and neglect the Early effect. The input current of the circuit is labeled as I_{REF} and output current I_o . The input-output current relation is given as

$$I_o = \frac{I_{REF}}{1 + \frac{2}{\beta}} \qquad (2.5)$$

from the above Eq. (2.5), I_o and I_{REF} become equal only when $\beta \to \infty$.

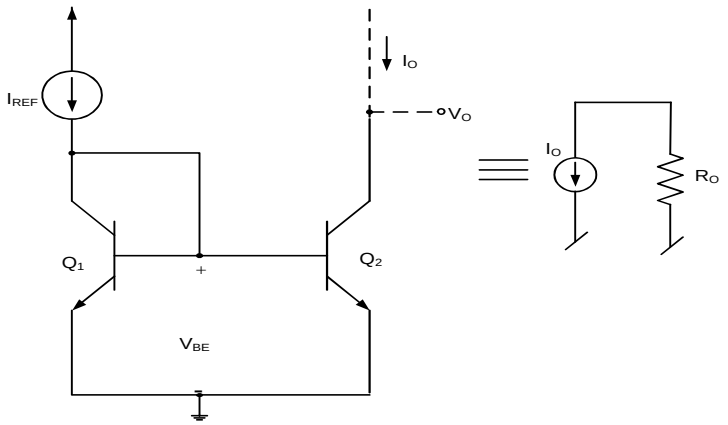


Fig.2.3 The basic BJT current mirror [2]

There are two performance parameters to determine the performance of the current mirror circuits, are listed as

- Accuracy of the current transfer ratio of the mirror circuit
- Output resistance of the current source

2.2.1 Base Current Compensated Current Mirror

The main problem in basic current mirror circuit shown in Fig.2.3 is that base current is finite. The base current error can be minimize by adding current gain to the reference transistor Q_1, the base current compensated current mirror configuration is shown in Fig.2.4. The base current of Q_3 is equal to the difference of I_{ref} and I_{C1}. In base current compensated current mirror R_0 is same as basic current mirror which is r_{o2}(output resistance of transistor Q2).

For the large value of beta, the base current term can be neglected. So the output current is defined as

$$I_2 \approx I_{ref} \frac{R_1}{R_2 + R_1} \qquad (2.6)$$

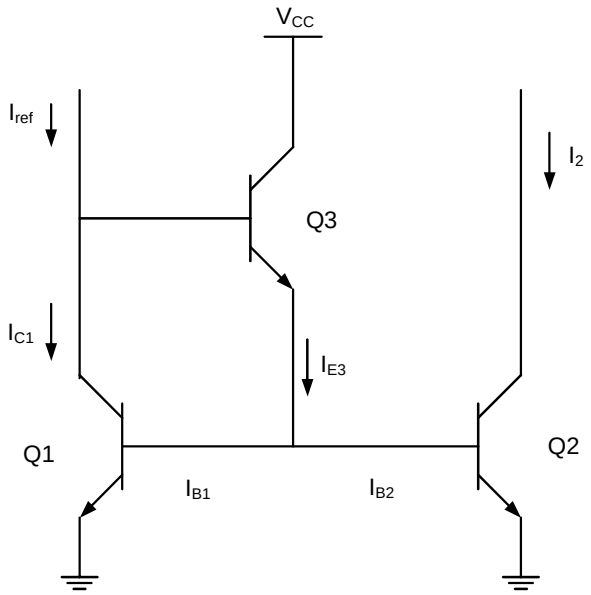


Fig.2.4 Base current compensated current mirror [2]

2.2.2 Cascode Current Source

The another cause of error in current sources is due to the finite output resistance of the current source transistors, which results a variation in output current with voltage in basic current mirror. The cascode current source is shown in Fig.2.5. In this cicuit, output resistance ($\approx r_{o2}/2$) has more value than the basic current mirror shown in Fig.2.3. This circuit consists two basic current mirror circuits which are configured using Q3 , Q4 transistors and Q1 , Q2 respectively, both current mirror

circuits are connected in series. In this configuration Q2 and Q4 form a common-base, common-emitter cascode pair.

The input and output current relation is derived as

$$I_o \approx I_{REF} \frac{\beta}{\beta + 2} \tag{2.7}$$

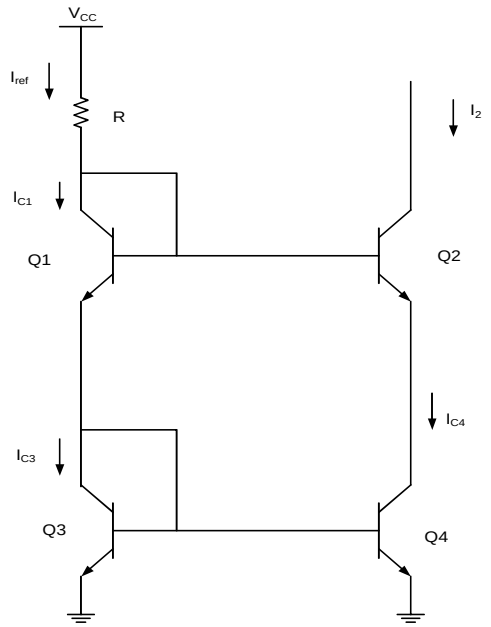


Fig.2.5 Cascode current source using BJTs [2]

2.2.3 The Wilson Current Mirror

A Wilson current mirror is shown in Fig.2.6. In analysis, the early effect is neglected and assumes the transistors to have identical parameters. The input-output currents relations are defined as

$$\frac{I_o}{I_{REF}} \approx \frac{\beta}{\beta + \frac{2}{\beta}} \tag{2.8}$$

If β becomes much higher than the input current (I_{REF}) will be equal to output current (I_o). The advantage of Wilson current mirror over the basic current mirror is that it has high output resistance ($\approx \beta r_o/2$). This is because of two positive feedback effects.

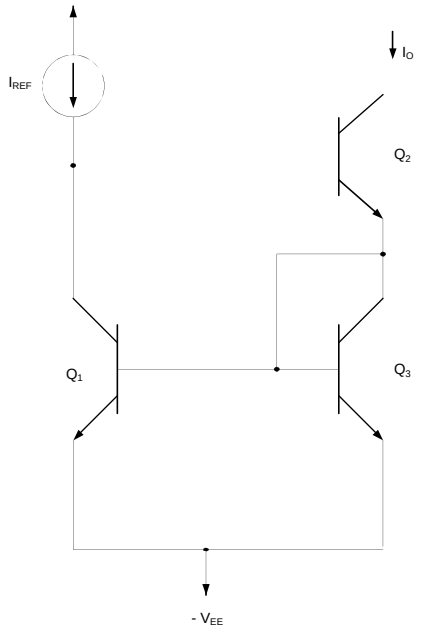


Fig.2.6 Wilson current mirror [2]

2.2.4 Generation of Complementary Current Outputs Using Cross Coupled Current Mirrors

In analog signal processing, various active building blocks are designed using cross coupled current mirror which is shown in Fig. 2.7. The beauty of this configuration is

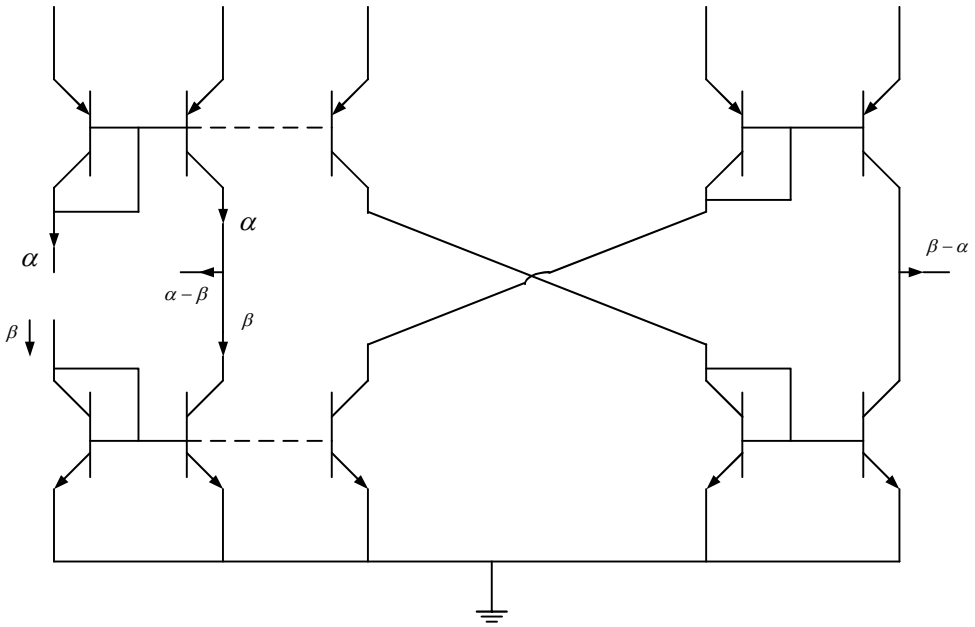


Fig. 2.7 Complementary current output using cross coupled current mirror

that it gives complementary currents outputs. In second generation current conveyors, it is used to provide two current outputs which have opposite polarity to each other. In VDCC, this configuration is used to generate currents as Iz+ and Iz- [1].

2.3 ACTIVE LOADS

In IC technology, resistor can be simulated using CMOS and other active blocks such as OTA to reduce the chip area and circuit efficiency. Such type of active loads also provides the electronic tunability which is the other advantage. A single ended differential amplifier is shown in Fig 2.8 with active load (PMOS current mirror).

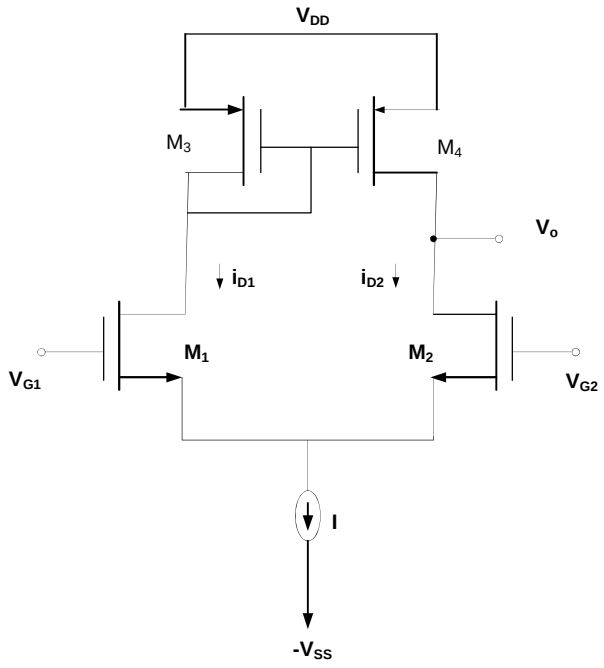
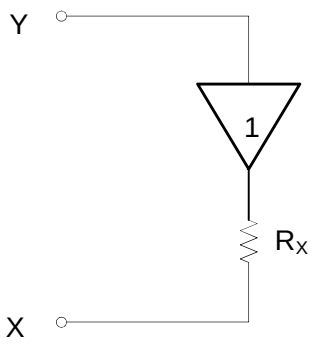


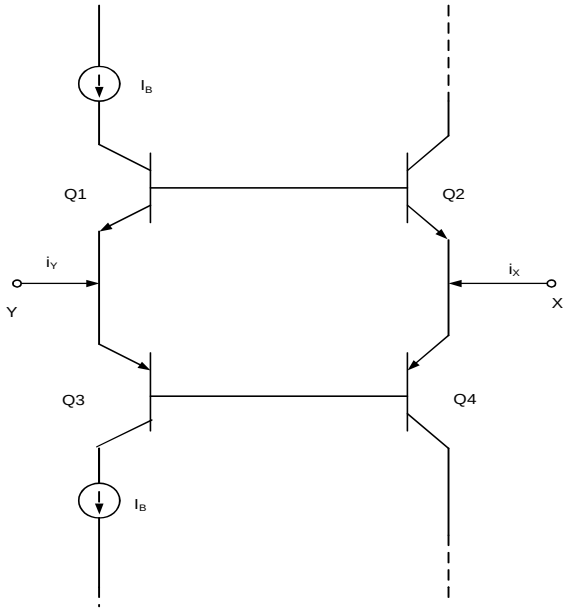
Fig. 2.8 Single ended differential amplifier using active load

2.4 VOLTAGE BUFFERS (TRANSLINEAR)

A voltage buffer is a very useful constitutive block with the following schematic diagram. The input and output impedances of an ideal voltage buffer is infinite and zero respectively. An emitter follower has been used as a voltage buffer in many active building blocks. An interesting configuration of a voltage buffer which works on the translinear circuit principle [29] is given below in Fig. 2.9. The value of Rx for this buffer is given by $I_B/2V_T$.



(a)



(b)

Fig.2.9 Translinear buffer (a) Equivalent diagram

(b) Realization using BJTs

2.5 OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

Operational transconductance amplifiers (OTA) are extensions of the basic differential amplifiers which are actively loaded [7,8]. Though the transconductance amplifiers are also available as off-the-shelf components (LM 3080, LM 13600), these amplifiers can be found as constitutive blocks in many of the recently proposed active building blocks such as Voltage Differencing Buffered Amplifier [27], Current

Differencing Transconductance Amplifier [28] etc. In the following we summarize the operational transconductance amplifiers and its features.

OTA is a differential VCCS (Voltage Controlled Current Source) in which output current is controlled by input voltage source and it is characterized by transconductance (g_m). The output current of the OTA is given by the following equation [9]

$$I_{out} = g_m (V_1 - V_2) \quad (2.9)$$

where V_1 and V_2 are voltages as non-inverting and inverting input terminal of OTA. The symbol of OTA is shown in Fig. 2.10

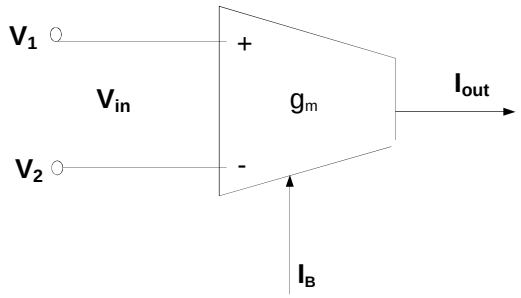


Fig. 2.10 Symbol of OTA

The trans-conductance is taken such as below

$$g_m = \sqrt{\mu_n C_{ox} \frac{W}{L} I_B} \quad (2.10)$$

where μ_n, C_{ox}, W/L and I_B are the electron mobility of NMOS, gate oxide capacitance per unit area, transistor aspect ratio and bias current of the OTA, respectively. In above equation, it can observe that the transconductance g_m is adjustable by a supplied bias current (I_B).

2.5.1.1 Ideal Characteristics

Characteristics of ideal OTA can be summarized as below [3, 4]:

Input impedance (Z_{in})= ∞, Output Impedance (Z_0) = ∞, Bandwidth = ∞ .

2.5.1.2 Schematic Circuit Diagram

The complete schematic of OTA using MOS transistors is shown in Fig.2.11. This circuit is formed by a differential input pair M_1, M_2, an actively loaded current mirror M_3, M_4 and constant current source derived from M_5. The output current for this case is

$$I_{out} = \frac{g_m}{2\pi C_L}(V_{in1} - V_{in2}) \qquad (2.11)$$

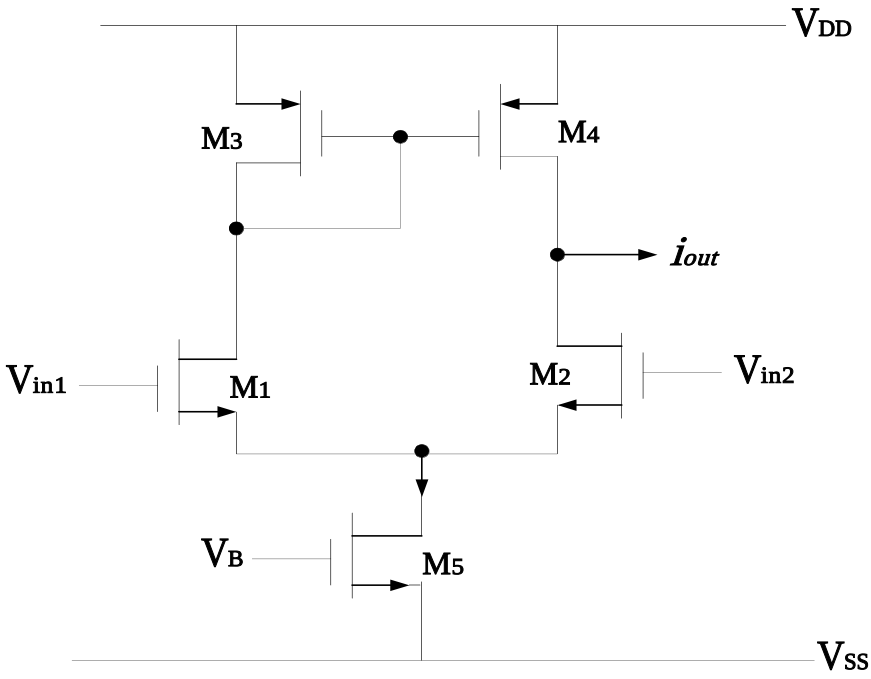


Fig.2 .11 CMOS realization of operational transconductance amplifier

2.6 CURRENT CONVEYOR

In analog signal processing, current conveyor (CC) is a fundamental building block in current mode techniques. It is basically a three terminal device which can be used for basic analog signal processing functions by using proper circuitry [12]. In many manners current conveyor simplifies circuit design in the same way as the conventional operational amplifier. The current conveyor extends an alternative manner of abstracting complex circuit functions, thus adding in the introduction of new and useful implementation. In addition, CC is a general active building block which can

replace classical operational amplifier in voltage mode applications or gives us chance to transform these applications to current-mode. During the last two decades many derivatives of the basic current conveyor have also appeared in literature. In the following we presented the basic current conveyor and some of its important derivatives.

The principle of the current conveyor of first generation was published by Smith and Sedra in 1968 [10]. After that many authors have implemented current conveyors for different applications. Unfortunately, current conveyors are not available in the form of IC. Many developers can't use this active blocks in their developed application of analog signal processing (ASP) and systems due this. If the scenario will change, the designers will be more familiar with the current conveyor and its usability in ASP. Now some op-amps having wideband and high speed, based on current conveyors are available in the form of integrated circuits such as OPA660, AD840, AD844.

Types of current conveyors are discussed as follows:

2.6.1 First Generation Current Conveyor (CCI)

The principle of the current conveyor of first generation was published by Smith and Sedra in 1968. The current conveyors is a grounded three port network represented by black box, is shown in Fig. 2.12. Its CMOS realization is shown in Fig. 2.13. In CC, if input terminal 'y' is connected to a potential 'v' then same voltage is appeared at other input terminal 'x'. In a dual manner, if a current 'I' is forced through terminal 'x' an equal current will flow through input 'y'. The same current is also conveyed through output terminal 'z' at high impedance level which can be used as current source. Its input-output relationship is given in matrix form as

$$\begin{bmatrix} ? \\ ? \\ ? \end{bmatrix} = \begin{bmatrix} ? & ? & ? \\ ? & ? & ? \\ ? & ? & ? \end{bmatrix} \begin{bmatrix} ? \\ ? \\ ? \end{bmatrix} \qquad (2.12)$$

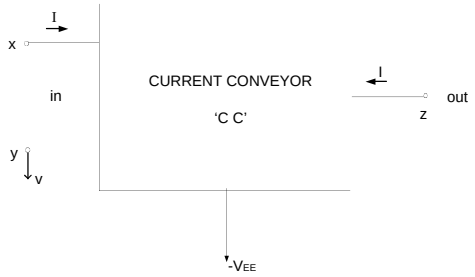


Fig. 2.12 Black box of basic current conveyor

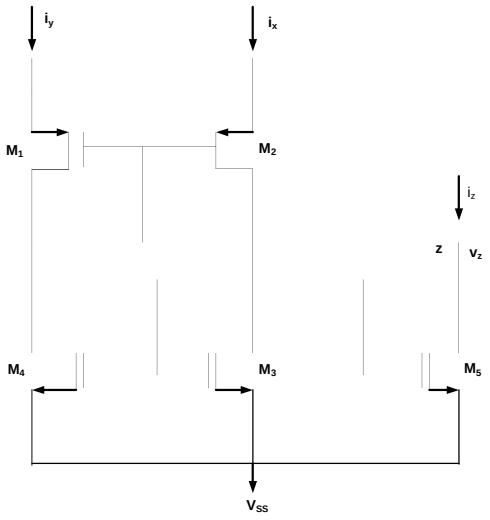


Fig.2.13 CMOS implementation of CCI [12]

2.6.2 Second Generation Current Conveyor (CCII)

The next generation current conveyor (CC) was evolved in 1970 [11]. The second generation current conveyor (CCII) has different and more versatile terminal characteristics. The symbol of CCII is shown in Fig. 2.14. The CCII is further classified as based on direction of output current at z terminal termed as CCII+ and CCII-. For CCII+ output current has positive sign and CCII- has negative direction. In CCII , applied input potential at terminal y is appeared on terminal x as same value and input terminal y has high input impedance .The input current ?? will be conveyed through output terminal z which is used as high impedance as a current source. The terminal equations can be described as follows

?? ? ? ? ??
??? ? ? ?? ?? ? ?? ?? ? ? (2.13)
?? ? ? ? ??

The CCII is introduced as a convenient active block that provides an easy approach to design the general linear analog systems.

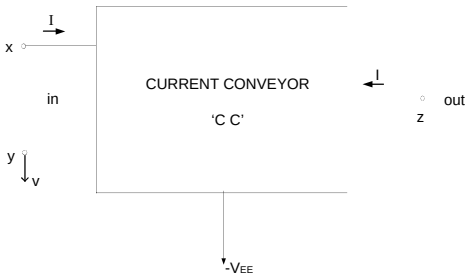
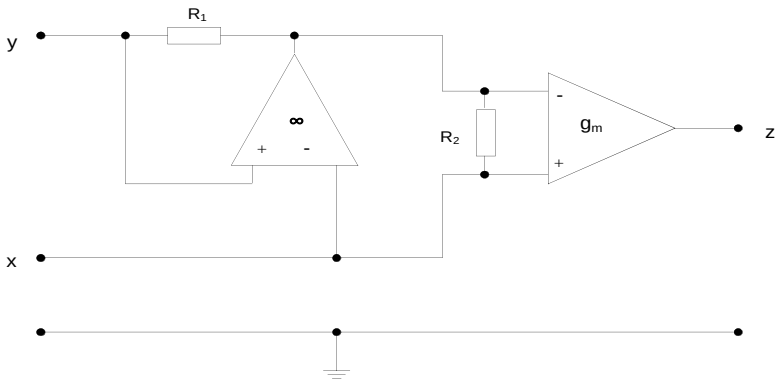


Fig. 2.14 Symbol for CCII

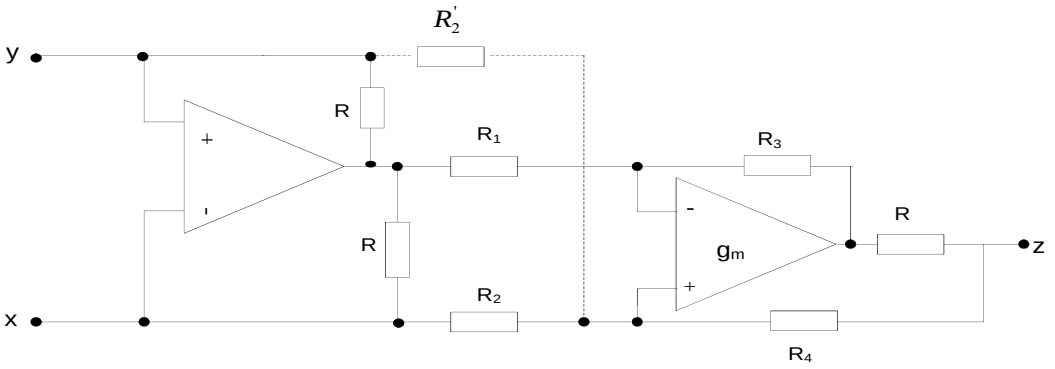
2.6.2.1 Circuit Implementation of CCII

After the bipolar implementation of CCII proposed by Sedra and Smith [11], some interesting implementations of CCII using off-the shelf available ICs have been proposed in literature [15-17]. The notable among them were those proposed by Senani [16] and Huertas [17]. These implementations are given in Fig. 2.15.

The CCII is shown in Fig. 2.15(a). If ?? is deleted and ?? ? ? ??, then the circuit can be used as CCII+. For CCII-, input terminals are interchanged keeping other previous conditions for CCII+ [16]. The simplified circuit is shown in Fig. 2.15(b), exhibits unsymmetrical nature because the equivalent resistors at x and y terminals are not identical. This circuit can be more balanced by connecting ?? and selected as ?? ? ??? ? ???.



(a)



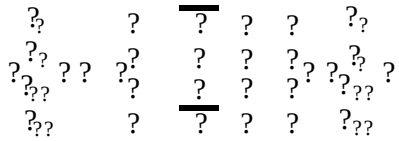
(b)

Fig. 2.15 (a) Implementation of CCII+ and CCII- [16]

(b) Simplified circuit for current conveyor [17]

2.6.3 Third Generation Current Conveyors

The third generation current conveyor (CCIII) has been introduced by Fabre [13]. CCIII can be used as current controlled current source with unity gain. It can be used to design filters, inductance simulation and filters because of the terminal properties. It has good dynamic swing and high output resistance which enables cascadability. The main advantages for using CCIII are low gain error (high accuracy), high linearity and wide frequency response. The symbol of CCIII is shown in Fig. 2.16, and CMOS realization of CCIII is shown in Fig. 2.17 and its terminal equations are defined in the matrix form as below



(2.14)

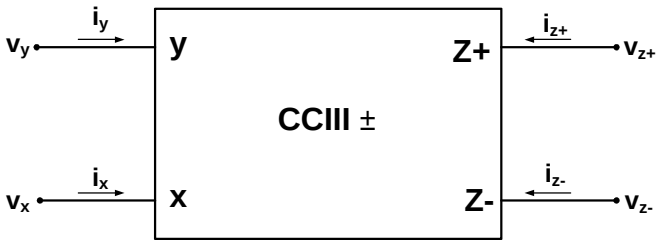


Fig. 2.16 Symbol of the CCIII [14]

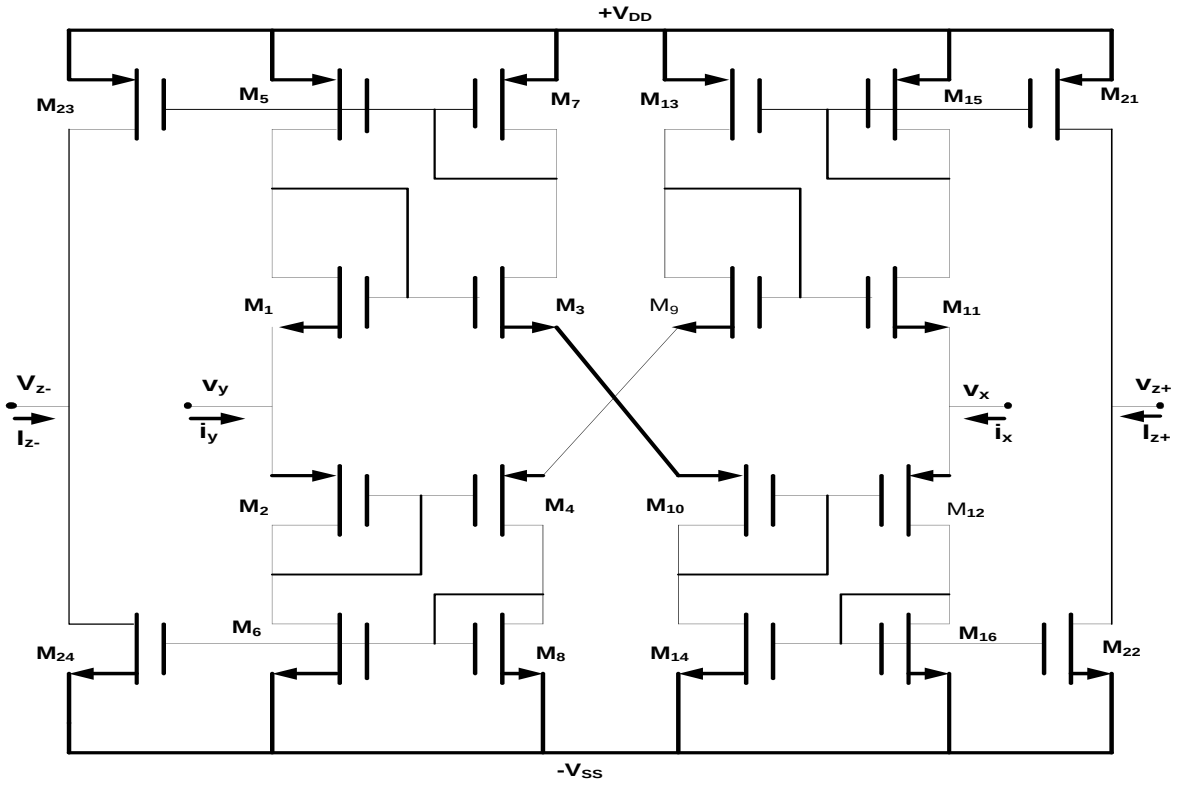


Fig. 2.17 CMOS realization of third generation current conveyor (CCIII) [14]

2.7 DERIVATIVES OF CURRENT CONVEYORS

The versatility of CCs has further been enhanced by modifying its basic structure or by adding some more functionality so as to make the CC more useful in realization of various analog signal processing circuits in both voltage as well as current mode. In the following we present some of these derivatives of current conveyors [18-26].

2.7.1 Fully Differential Current Conveyors (FDCCII)

The FDCCII is the extended version of CCII, was proposed in 2000 [18]. It has the all characteristics of the differential pair as well as current conveyors. It's an eight terminal active building block which symbolic diagram is shown in Fig. 2.18. The Y_1 and Y_2 terminals show high impedance while X_+ and X_- terminals are low impedance terminals.

The terminal equations are characterized as below

(2.15)

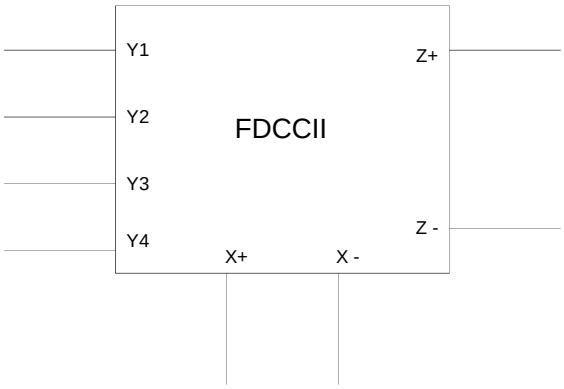


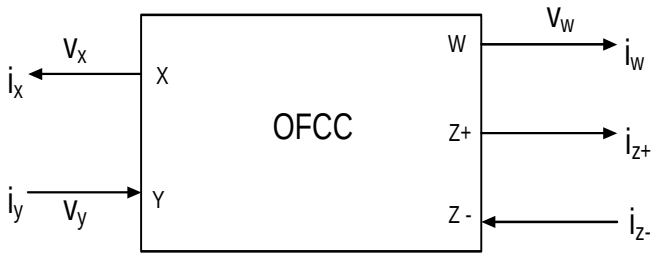
Fig. 2.18 Symbolic notation of FDCCII [18]

The CMOS realization of FDCCII and its various applications in the area of analog signal processing was discussed in [18]. This active building block is used for mixed mode applications where fully differential signals can be processed.

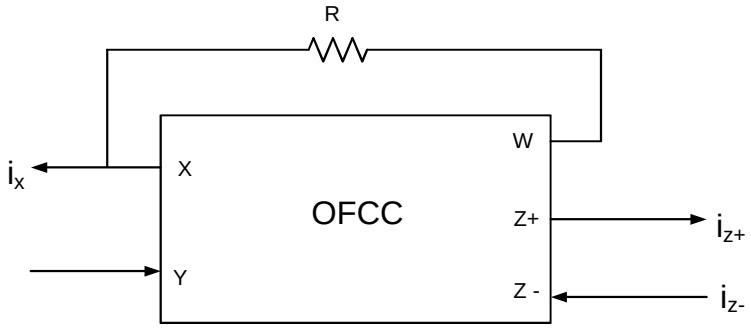
2.7.2 Operational Floating Current Conveyor (OFCC)

Operational floating current conveyor is a five terminal active building block, is shown in Fig. 2.19(a). OFCC contains the features of current conveyor (CC), current feedback operational amplifier (CFOA) and operational floating conveyor (OFC) [19]. It comprised the X, Y as input terminal and W, Z+ and Z- output terminals. The X terminal is used as current input terminal with low input impedance while terminal Y shows high input impedance as input voltage terminal. The output terminals Z+ and Z- give opposite polarity currents as output, show high output impedance terminals. Its terminal characteristics are defined in the form of matrix as below

(2.16)



(a)



(b)

Fig. 2.19 (a) Operational floating current conveyor

(b) The OFCC configured as CCII- and CCII+ [19]

The OFCC can be configured as second generation current conveyor (CCII) is shown in Fig. 2.19(b). The applied input voltage V_y appears at terminal X while current i_x is conveyed to the nodes Z+ and Z- with opposite polarity. So it can be used to configure both mode of CCII as CCII- and CCII+.

2.7.3 Current Controlled Conveyor (CCCII)

The CCCII was implemented using BJT in 1996 [20]. It is the derivative of second generation current conveyor (CCII) but it shows the electronic tunability which is the advantage over CCII. The symbolic representation of CCCII is shown in Fig. 2.20 In basic CCII, inbuilt electronic tunability is absent while CCCII shows this property, the parasitic resistance at X terminal can be controlled by varying the bias current is defined as

?? ? ?? ?? (2.17)

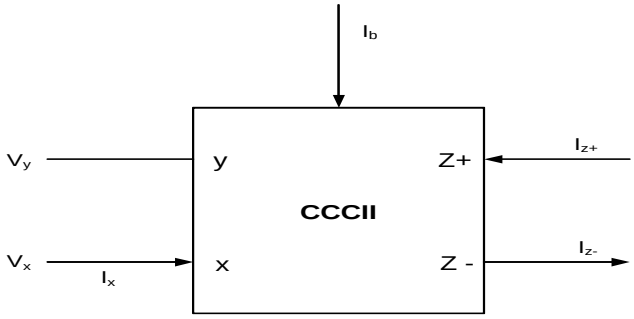


Fig. 2.20 Symbol of CCCII

The relationship between the voltage and current variables at input and output ports X, Y and Z of the CCCII can be expressed by the following matrix

$$\begin{bmatrix} I_y \\ V_x \\ I_{z+} \\ I_{z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & -1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_{z+} \\ V_{z-} \end{bmatrix} \tag{2.18}$$

CCCII are extensively used in analog signal processing such as current mode filters, oscillators, amplifiers, radio frequency oscillators and low noise amplifiers, ASK/FSK modulators. Several CMOS implementations of CCCII was also discussed in [21], each different configurations have different advantages over classical CCII.

2.7.4 Current Controlled Fully Balanced Current Conveyor (CFBCCII)

The circuit symbol of the CFBCCII is shown in Fig. 2.21, where bias current I_B is used to provide electronic tunability. The input terminals exhibit high input impedance at the Y terminals, two pairs of differential input terminals are configured by Y_1, Y_2, Y_3 and Y_4. X- and X+ terminals are used as voltage tracking terminals and current of X terminal is conveyed to Z port [22].

It's ideal port characteristics can be expressed as

$$I_{y1} = I_{y2} = I_{y3} = I_{y4} = 0 \tag{2.19 a}$$

$$V_{y1} - V_{y2} = V_{x+} - V_{x-} \quad V_{y3} - V_{y4} = V_{x+} - V_{x-} \tag{2.19 b}$$

$$I_{x+} - I_{x-} = I_{z+} - I_{z-} \tag{2.19 c}$$

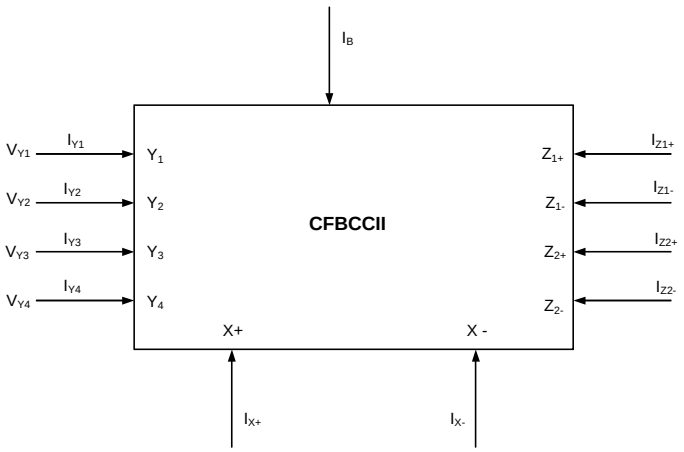


Fig. 2.21 Symbol of CFBCCII [22]

where $R_X=f(I_B)$ is current controlled resistance which can be tuned by varying bias current I_B. CFBCCII consists two main properties which makes it more versatile active building blocks in analog signal processing applications, are differential architecture and current controllability[24].

2.7.5 Universal Current Conveyor (UCC)

Universal current conveyor (UCC) is a versatile building block that is able to replace any type of existing current conveyors [23]. UCC is an eight-port active building block where three inputs terminals (differential Y1, Y2 and summing Y3) show high input impedance whereas X terminal shows low-impedance. The symbolic notation of UCC is depicted in Fig. 2.22 where currents on node Z1 and Z2 have their complementary currents also.

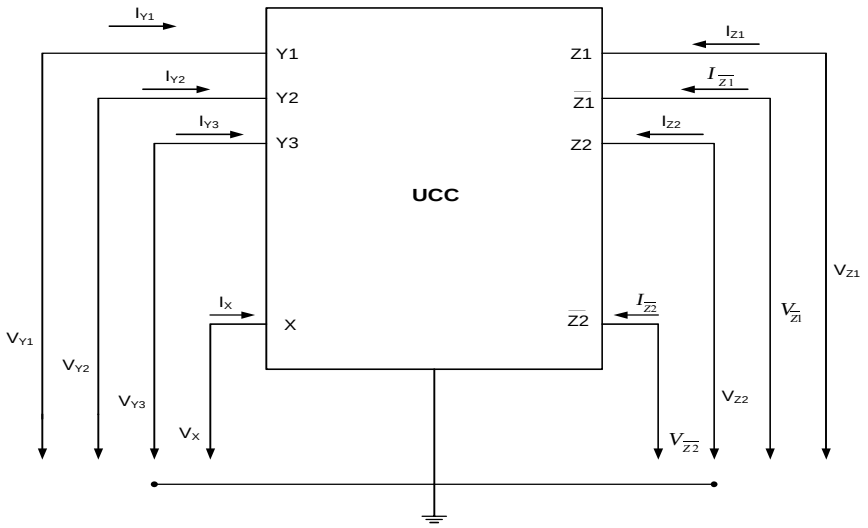


Fig. 2.22 Symbol of UCC [23]

The matrix description of terminal characteristics of UCC is given as

$$\begin{bmatrix} ? \\ ? \\ ? \\ ? \\ ? \\ ? \\ ? \\ ? \end{bmatrix} = \begin{bmatrix} ? & ? & ? & ? & ? & ? & ? & ? \\ ? & ? & ? & ? & ? & ? & ? & ? \\ ? & ? & ? & ? & ? & ? & ? & ? \\ ? & \overline{?} & ? & ? & ? & ? & ? & ? \\ ? & ? & ? & ? & ? & ? & ? & ? \\ ? & ? & ? & \overline{?} & ? & ? & ? & ? \\ ? & ? & ? & \overline{?} & ? & ? & ? & ? \\ ? & ? & ? & ? & ? & ? & ? & ? \end{bmatrix} \begin{bmatrix} ? \\ ? \\ ? \\ ? \\ ? \\ ? \\ ? \\ ? \end{bmatrix} \quad (2.20)$$

Several CC derivatives can be realized using UCC with appropriate connections. The procedure to realize CC derivatives was described in [23].

2.7.6 Dual-X Current Conveyor (DXCCII)

The DXCCII is an active building block which is the combination of basic second generation current conveyor (CCII) and inverting current conveyor (ICCII). The circuit symbol of DXCCII is shown in Fig. 2.23 which has two X terminals, namely non-inverting terminal (X_P) and inverting terminal (X_N).

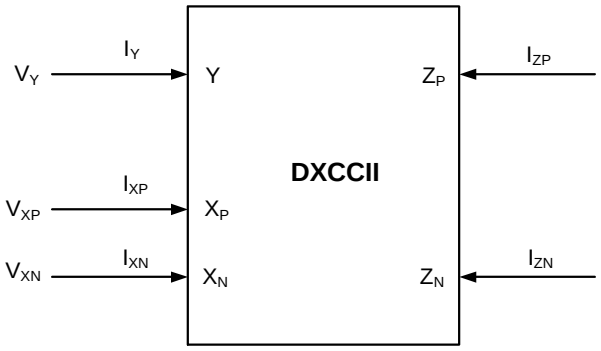


Fig. 2.23 Symbol of DXCCII [26]

The terminal characteristic equations are given as below matrix

$$\begin{bmatrix} ? \\ ? \\ ? \\ ? \\ ? \end{bmatrix} = \begin{bmatrix} ? & ? & ? \\ \overline{?} & ? & ? \\ ? & ? & ? \\ ? & ? & ? \\ ? & ? & ? \end{bmatrix} \begin{matrix} ? \\ ? \\ ? \\ ? \\ ? \end{matrix} \quad (2.21)$$

The practical realization of DXCCII was realized using only AD844 and rest with AD844 and op-amps [25]. This realization was used to design quadrature oscillator.

2.8 CONCLUSION

This chapter covers all the basic components which are used to design the almost several active building blocks, are as differential pair, active loads, current mirror, translinear buffer, current conveyor and OTA. Current conveyor is the mostly used active block to derive others. Types of current conveyors are mainly CCI, CCII and CCIII. Some derivatives of current conveyor are discussed such as FDCCII, OFCC, CCCII, CFBCCII, UCC and DXCCII. These active blocks are used to various analog signal processing applications as filters, oscillator, amplifier etc.

REFERENCES

[1] Biolek D., Senani R., Biolkova V., Kolka Z., “Active Elements for Analog Signal Processing: Classification, Review, and New Proposals”, Radioengineering, Vol. 17, No. 4, pp. 15 – 32, 2008.

[2] Adel S. Sedra, Kenneth C. Smith, “Microelectronic Circuits Theory and Application”, Oxford University Press, 5th edition, 2011.

[3] R L. Geiger and E. Sanchez-Sinencio, "Active Filter Design Using Operational Transconductance Amplifiers: A Tutorial", IEEE Circuits Device Mag., vol. I, pp.20-32, 1985.

[4] Intersil Semiconductors, “Application of the CA3080 High performance operational Transconductance Amplifiers” Application Note, AN6668.1, Nov.1996.

[5] T. Tsukutani, M. Higashimura, N. Takahashi, Y Sumi and Y. Fukui,"Novel Voltage-Mode Biquad Without External Passive Elements", International Journal of Electronics, vol.88, pp.13-22, 2001.

[6] W. Surakampontom, V. Riewruja, K. Kumwachara, C. Surawatpunya and K.Anuntahirunrat, "Temperature- Insensitive Voltage-to-Current Converter and Its Applications", IEEE Trans. Instrum. Meas., Vol.48, pp.1270-1277, 1999.

[7] J. Sila-Martinez and E. Sanchez-Sinencio, "Analogue OTA Multiplier Without Input Voltage Swing Restrictions and Temperature-Compensated”, Electron. Letts. Vol.22, pp.599-600, 1986.

[8] K. Kaewdang, C. Fongsamut and W.Surakampontorn, “A Wide Band Current Mode OTA-Based Analog Multiplier-Divider”, IEEE. 0-7803-7761, 2003

[9] H. S. Malvar, “Electronically Controlled Active Filters With Operational Transconductance Amplifiers”, IEEE Trans. Circuits Systs., Vol. CAS-29, pp. 333-336, May 1982

[10] Sedra A., Smith K.C, “The Current Conveyor: A New Circuit Building Block. Proc. IEEE, Vol.56, pp. 1368-1369, Aug. 1968

[11] Sedra A.S., Smith K.C., “A Second Generation Current Conveyor and Its Application”, IEEE Trans., CT-17, pp. 132-134, 1970.

[12] Sedra A., Roberts G., "The Current Conveyor: History, Progress and New Results", IEE Proceeding Part G ,137, pp. 78-87,1990.

[13] Fabre A., "Third Generation Current Conveyor: A New Helpful Active Element", Electronics Letters, 3 I, pp.338-359, 1995.

[14] S. Minaei, M. Yildiz, H. Kuntman, S. Tiirkoz, " High Performance CMOS Realization of The Third Generation Current Conveyor (CCIII) ", 45th Midwest Symposium, Pages 307-10, Vol.1, 2002.

[15] Bakhtiar M.S. and Aronhime P., "A Current Conveyor Realization Using Operational Amplifiers", Int. J. Electron., 45, pp. 283-288, 1978.

[16] Senani, R., "Novel Circuit Implementation of Current Conveyors Using Op-amp. and OTA." Electronic Letters., Vol. 16, pp. 2-3, 1980.

[17] Huertas, J. L., "Circuit Implementation of Current Conveyor", Electronics Letters., Vol. 16, pp. 225-226 , 1980.

[18] El-Adway, A. M. Soliman and H. O. Elwan, "A Novel Fully Differential Current Conveyor and Its Application For Analog VLSI," IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, Vol. 47, No. 4, pp. 306-313, 2000.

[19] Y. H. Ghallab, M. Abo El-Ela and M. Elsaid, "Operational Floating Current Conveyor: Characteristics, Modeling and Experimental Results", Proc. ICM, Kuwait, pp. 59–62, 1999.

[20] Alain Fabre, Omar Saaid and Christophe Boucheron, "High Frequency Applications Based on A new Current Controlled Conveyor", IEEE Transactions On Circuits and Systems-I: Fundamental Theory And Applications, Vol. 43, No. 2, February 1996.

[21] Wang Chunhua, She Zhixing, Liu Haiguang, " New CMOS Current-Controlled Second Generation Current Conveyors", IEEE, 978-1-4244-1708-7/08, 2008 .

[22] Wang Chunhua and Zhang Qiujing, "Current Controlled Fully Balanced Current Conveyor", Circuits and Systems, IEEE Asia Pacific Conference, pp. 1062-65, 2008.

[23] BEČVÁŘ D., VRBA K., ZEMAN V., MUSIL V., "Novel Universal Active Block: A Universal Current Conveyor", IEEE Int. Symp. on Circuit and Systems, Geneva (Switzerland), vol. 3, p. 471-473, 2000.

[24] Hussain A. Alzaher, Hassan Elwan, and Mohammed Ismail, “A CMOS Fully Balanced Second-Generation Current Conveyor”, IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, Vol. 50, No. 6, June 2003.

[25] Zeki A., Toker A., “The Dual-X Current Conveyor (DXCCII): A New Active Device for Tunable Continuous-Time Filters”, International Journal of Electronics, Vol. 89, No. 12, p. 913-923, 2002.

[26] Sudhanshu Maheshwari and Mohd. Samar Ansari, “Catalog of Realizations for DXCCII using Commercially Available ICs and Applications” Radioengineering, Vol. 21, No. 1, April 2012.

[27] Kacar F., Yesil A., Noori A., “New CMOS Realization of Voltage Differencing Buffered Amplifier and Its Biquad Filter Applications”, Radioengineering, Vol. 21, No. 1, p. 333-339, 2012.

[28] Biolek D., “CDTA-Building Block for Current-Mode Analog Signal Processing”, Proc. ECCTD, Cracow, Poland, Vol. III, pp.397-400, 2003.

[29] Gilbert B., “ Translinear Circuits: A Proposed Classification”, Electron. Lett., 1975

CHAPTER 3

VOLTAGE DIFFERENCING CURRENT CONVEYOR AND ITS GENERAL APPLICATIONS

3.1 INTRODUCTION

In the present chapter we discuss in detail an active building block namely Voltage Differencing Current Conveyor (VDCC) and its application in signal processing. This block was first proposed by Biolek, Senani, Biolkova and Kolka [1]. Very few circuit applications of this building block have appeared in literature. A CMOS implementation of VDCC has been proposed by Kacar, Yesil, Minaei and Kuntman and the workability of grounded inductor simulator was also verified [2]. After few months later, VDCC based floating inductor simulator was proposed and checked the usability of the circuit by Prasad and Ahmad [3].

In the following we discuss the CMOS implementation of VDCC given in [2]. The complete characterization of VDCC using 0.18um CMOS technology has been presented in PSPICE. The following application have also been presented

(i) Amplification of current signals

(ii) Addition of current signals

(iii) Subtraction of current signals

(iv) Differentiation of current signals

(v) Integration of current signals

(vi) Inductance simulation

PSPICE simulations have been carried out to verify the workability of all these circuits.

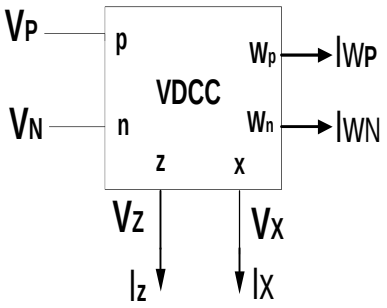
3.2 VOLTAGE DIFFERENCING CURRENT CONVEYOR

3.2.1 Circuit Description

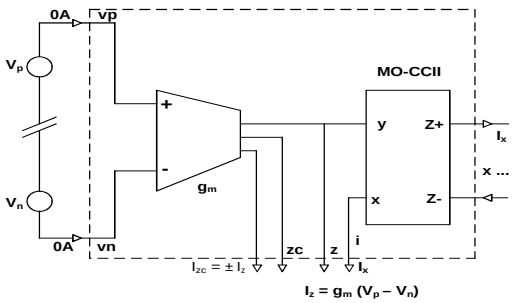
The block diagram of VDCC, is shown in Fig. 3.1(a), and its terminal characteristic is define by the following matrix

$$\begin{bmatrix} ? \\ ? \\ ? \\ ? \\ ? \\ ? \end{bmatrix} = \begin{bmatrix} ? & ? & ? & ? \\ ? & ? & ? & ? \\ ? & ? & ? & ? \\ ? & ? & ? & ? \\ ? & ? & ? & ? \\ ? & ? & ? & ? \end{bmatrix} \begin{bmatrix} ? \\ ? \\ ? \\ ? \end{bmatrix} \qquad (3.1)$$

where P and N are the input terminals and rest of the terminals Z, X, W_P and W_N are output terminals. Only X terminal exhibits low impedance and other terminals show



(a)



(b)

Fig 3.1 (a) The symbol of the VDCC [2]

(b) The behaviour model of VDCC [1]

high impedance. VDCC is an active block which is the combination of OTA and MOCCII [1-2]. The CMOS realization of VDCC is shown in Fig. 3.2 and its behavior model is shown in Fig. 3.1(b).

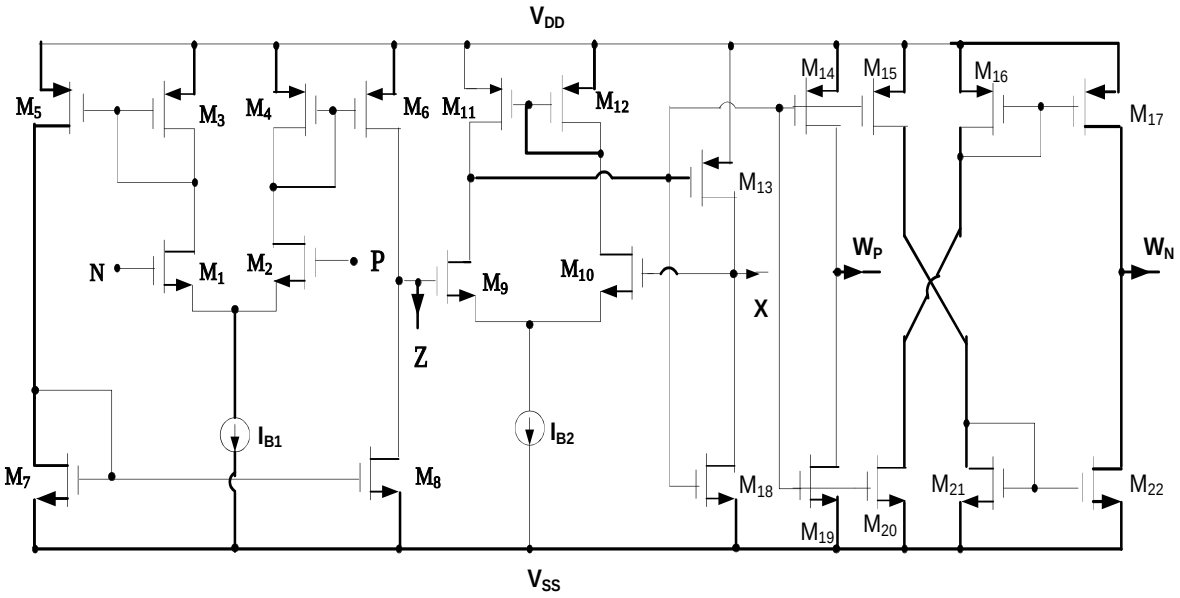


Fig. 3.2 CMOS realization of VDCC [2]

3.2.2 Simulation Results

The CMOS schematic diagram is shown in Fig. 3.2, was simulated in PSPICE using TMSC CMOS 0.18 μm process model parameters [2]. The aspect ratios of the transistors are given in Table 1. The supply voltages, are chosen as $V_{DD} = -V_{SS} = 0.9$ V, $I_{B1} = 50$ μA and $I_{B2} = 100$ μA. The following analysis has been carried out

(i) DC sweep (to obtain the linear voltage for various current and voltage transfers),

(ii) AC sweep (to obtain the bandwidth of the device).

The following terminating impedances were used in characterization of the VDCC as Rz = 9 k□, Rx = 100 □, Rwp = 100 □, Rwn = 100 □. The input signal for AC sweep was taken as 3 mV with frequency 10 MHz.

Transistors	W/L (μm)
$M_1 – M_4$	3.6/1.8
$M_5 – M_6$	7.2/1.8
$M_7 – M_8$	2.4/1.8
$M_9 – M_{10}$	3.06/0.72

$M_{11} - M_{12}$	9/0.72
$M_{13} - M_{17}$	14.4/0.72
$M_{18} - M_{22}$	0.72/0.72

Table: 1 Transistors aspect ratios for the VDCC of Fig. 3.2

Different parameters are obtained by PSPICE simulation of VDCC are listed as

Trans conductance g_m = 277 µA/V

Power consumption = 0.90 mW

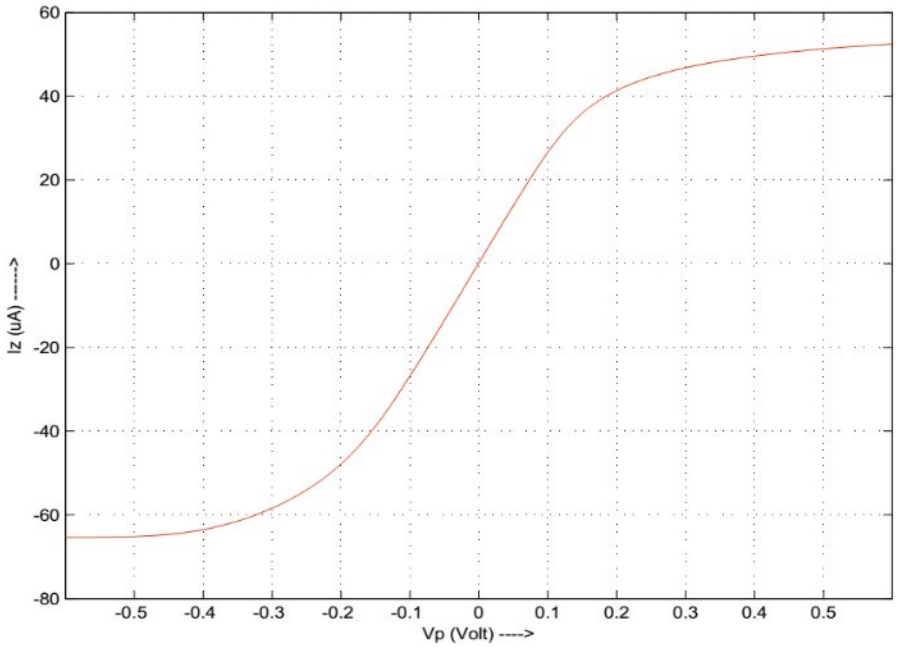


Fig. 3.3 Input DC characteristic of VDCC

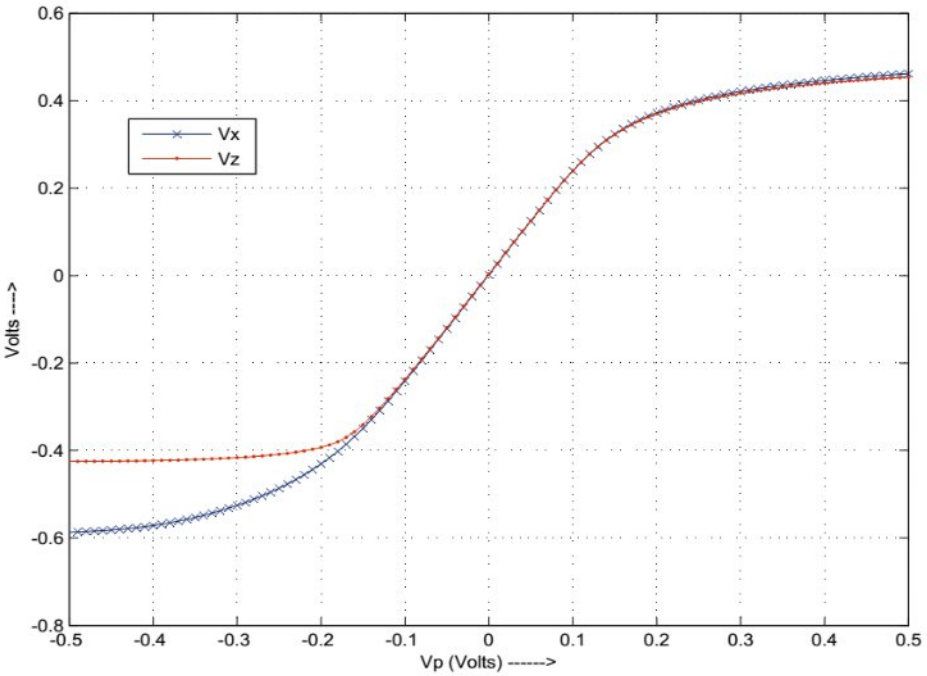


Fig. 3.4 DC characteristic of Vz and Vx terminal of VDCC

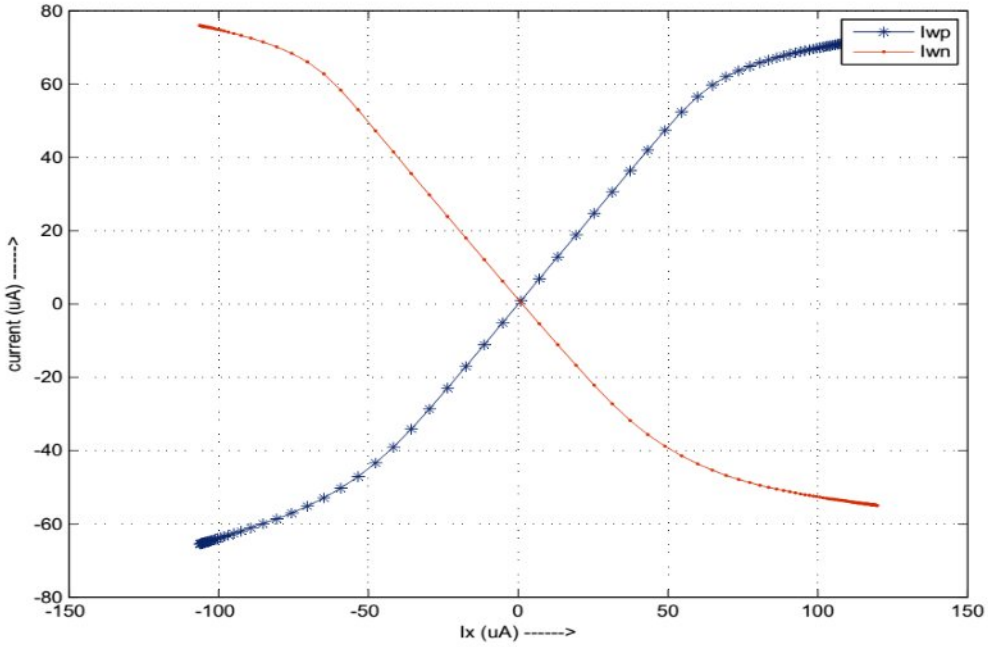


Fig. 3.5 Output DC characteristic of VDCC

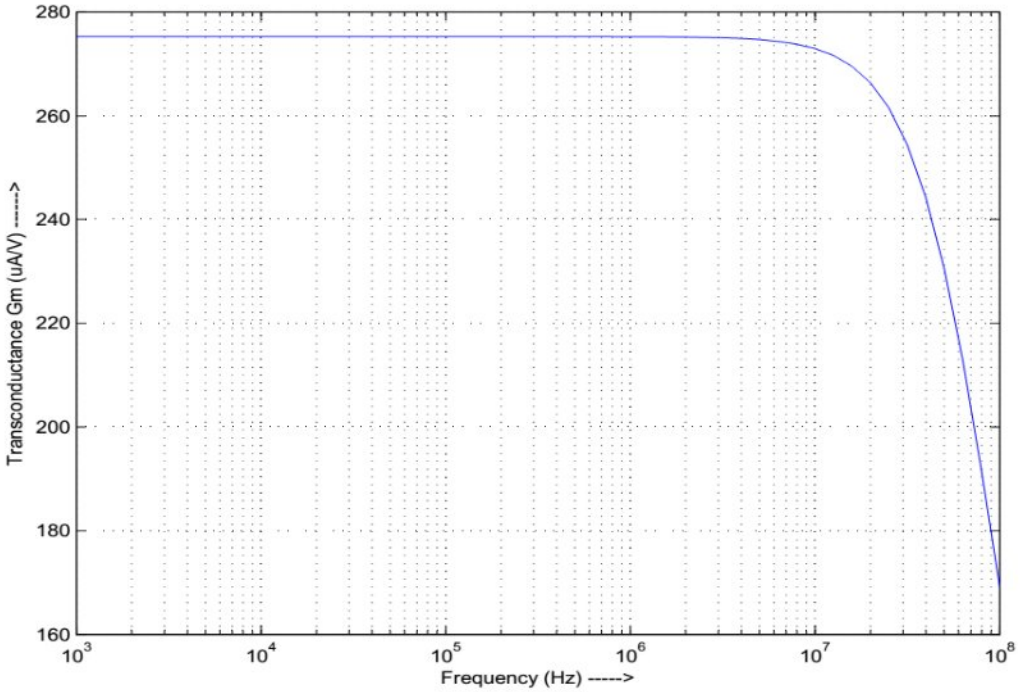


Fig. 3.6 Input AC characteristic of VDCC

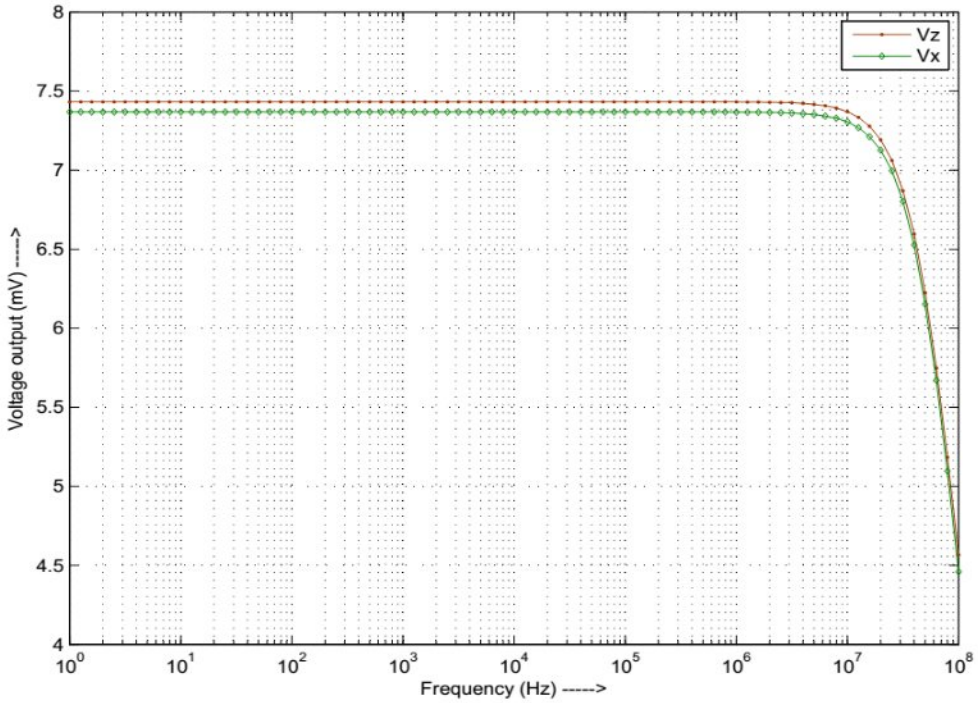


Fig. 3.7 AC characteristic of Vz and Vx terminal of VDCC

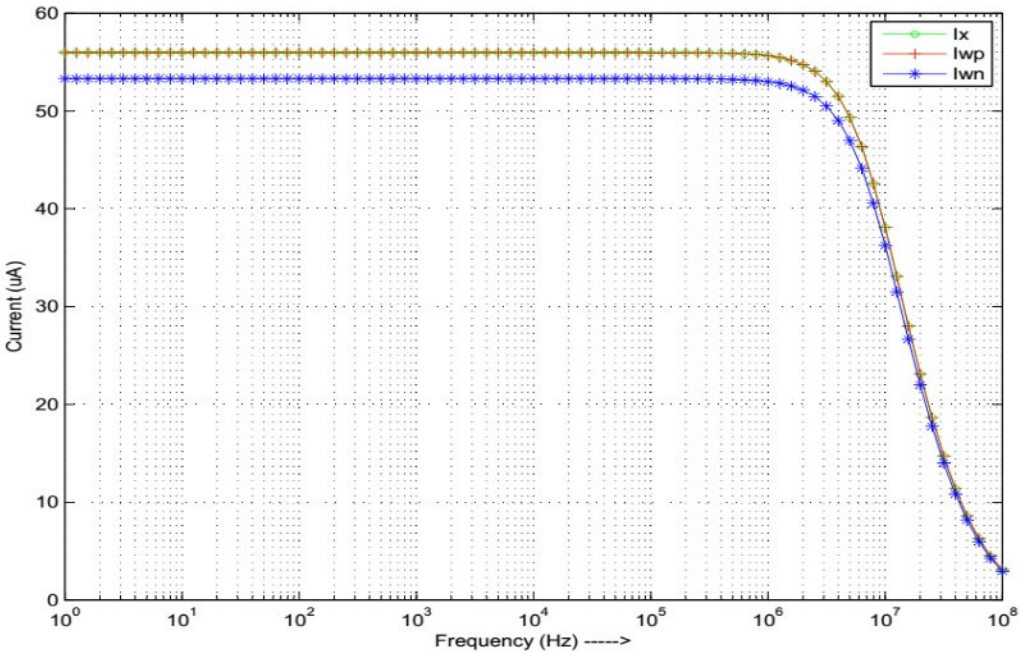


Fig. 3.8 Output AC characteristics of VDCC

3.3 APPLICATION OF VDCC IN CURRENT MODE SIGNAL PROCESSING

3.3.1 Amplifier

An amplifier which gives the output that is scaled version of an input current signal. Broadly amplifiers can be classified on the basis of their circuit configuration and methods of operation. In real world, sensors like piezo-electric, thermocouple etc. have small output signal. So by using amplifier their outputs can be amplified to drive the further circuitry such as lamp. Gain is basically ratio of the output divided by the input. Gain is unit less quantity as it's a ratio. In electronics, three types of amplifier gain can be measured such as Voltage Gain (Av), Current Gain (Ai) and Power Gain (Ap) [5]. Further amplifier can be classified on the basis of polarity of input and output. In inverting amplifier, output signal has opposite sign to the input signal. In the other hand, non-inverting amplifier gives output signal same as input signal polarity. VDCC based amplifier is shown in Fig. 3.9 which gives current gain. In this circuitry, if Wp is used as a output terminal then it is called as non-inverting amplifier. In contrast, if Wn is used as the output then its characteristic shows as inverting amplifier. By using single VDCC, it can be designed for the both inverting and non-inverting amplifier but this case is not found in the Op-amp. In the case of Op-amp, separately circuit is designed

for both types of amplifier. So, the beauty of VDCC based amplifier is that only choosing the output terminal which gives the opposite polarity, inverting and non-inverting. VDCC based amplifier has also some advantages over Op-amp based amplifier such as large bandwidth, less power supply, less power consumption and high slew rate etc. [2]. A simplified amplifier circuit of Fig. 3.9 is shown in Fig. 3.10. In this, OTA is used as a resistor which gives the less use of passive elements and also provides electronic tunability. The current gain for the Fig. 3.9 is described as follows

for non-inverting amplifier

(3.2)

and inverting amplifier

(3.3)

The current gain for the Fig. 3.10 is defined as follows

For non-inverting amplifier

(3.4)

Inverting amplifier

(3.5)

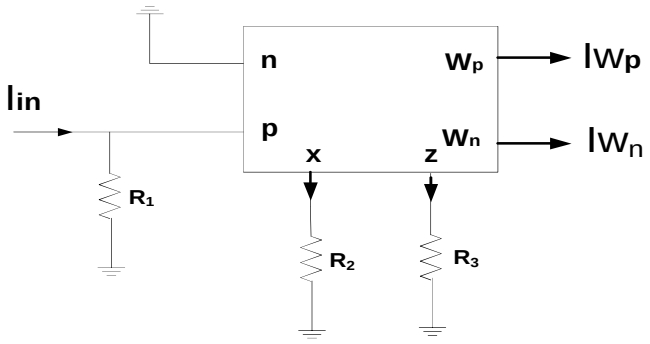


Fig. 3.9 VDCC based amplifier

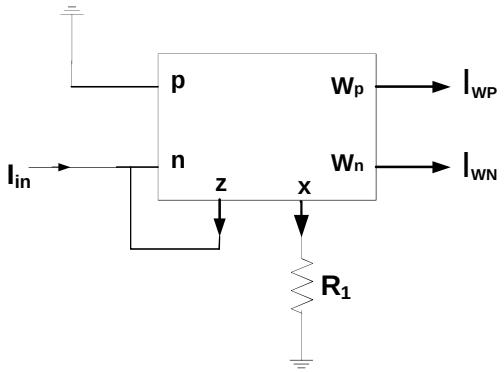


Fig. 3.10 Simplified amplifier using VDCC

3.3.1.1 Simulation Results

The amplifier is shown in Fig. 3.10 was simulated in PSPICE. The supply voltages, were selected as V_{DD} = - V_{SS} = 0.9V and bias currents I_{B1} = 34uA and I_{B2} = 50uA. The grounded resistor's value was selected as R_1 = 1 k⍰. The time and frequency responses of the Fig. 3.10 are shown in Fig. 3.11 and Fig. 3.12 respectively.

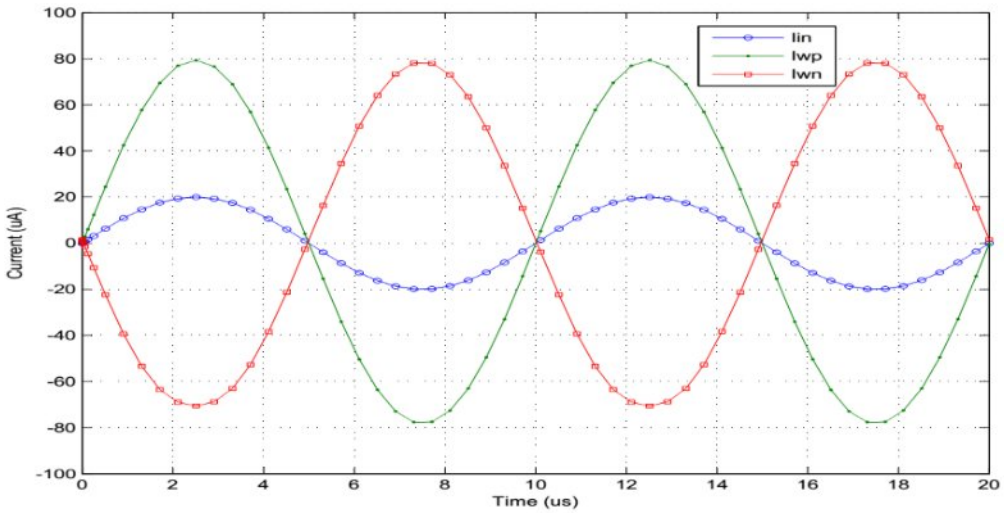
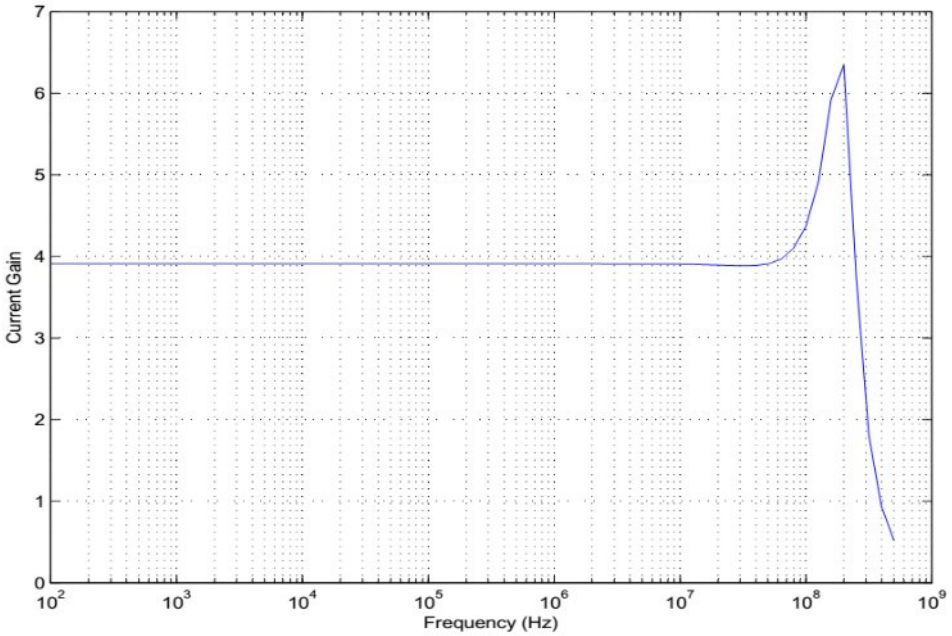


Fig. 3.11 Time response of amplifier circuit shown in Fig. 3.10



(b)

Fig. 3.12 Frequency response of the amplifier shown in Fig. 3.10

3.3.2 Addition

VDCC used to derive various analog functions. Addition can be realized using voltage or current mode technique. Here current addition can be done by using single VDCC block and grounded passive components as three grounded resistors [2, 5]. The circuit diagram of current adder is shown in Fig. 3.13. The transfer function of the circuit is as follows

$$I_{WP} = -I_{WN} = \frac{I_1 I_2 I_3}{I_4} \quad (3.6)$$

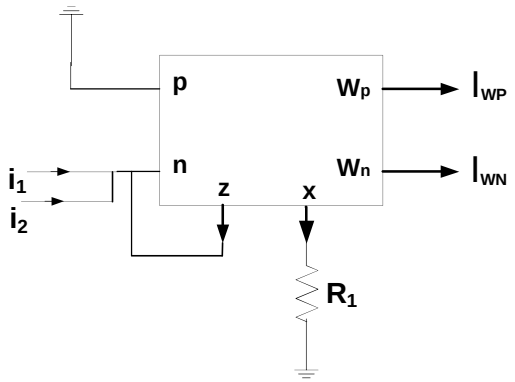


Fig. 3.13 VDCC based current mode summer

In VDCC, OTA can be used as a resistor. So the simplified circuit of the Fig. 3.13 is shown in Fig. 3.14, which is designed only using single grounded resistor.

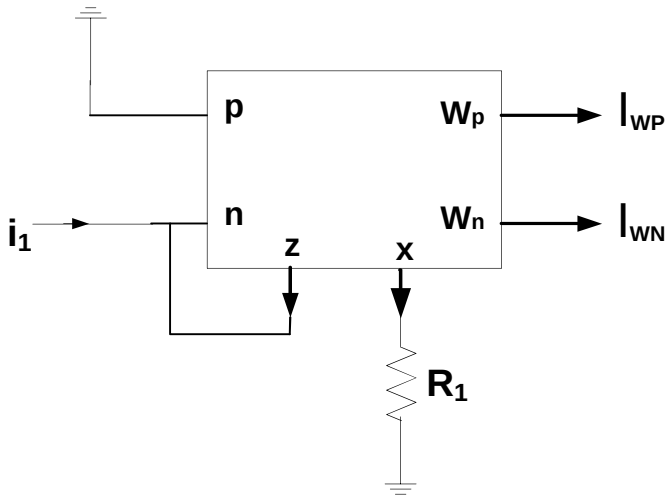


Fig. 3.14 Simplified Summer circuit of Fig. 3.13

The transfer circuit for the Fig. 3.14 is described as

$$\square_{\square\square} = -\square_{\square\square} = \frac{\square}{\square_{\square}\square_{\square}} \quad \square\square_{\square} \square \square_{\square} \tag{3.7}$$

3.3.1.1 Simulation Results

The summer circuit is shown in Fig. 3.14 was simulated in PSPICE. The passive element is selected as $\square_{\square} \square$ $\square\square\square\square\square$. The supply voltages, are selected as

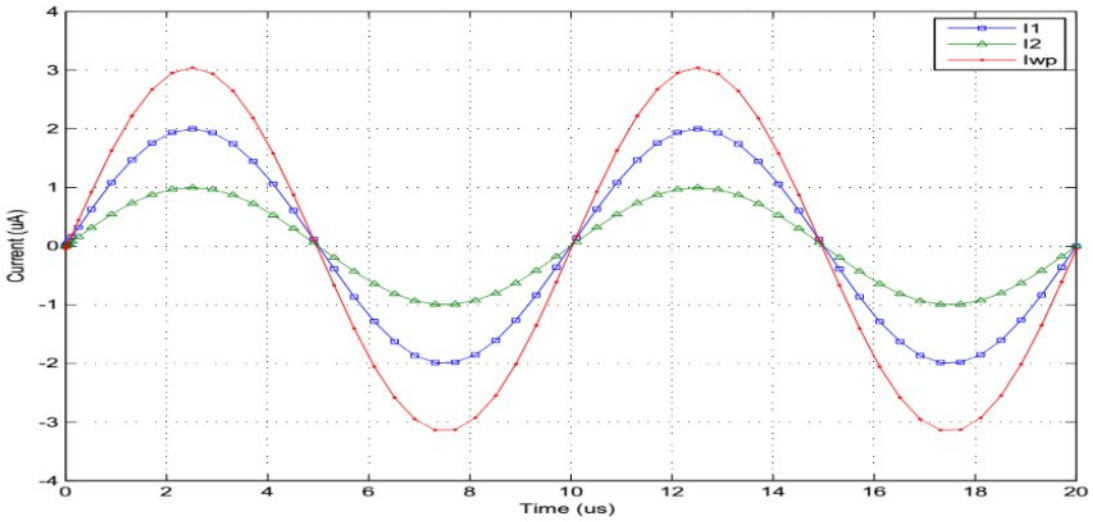


Fig. 3.15 Simulation result of Fig. 3.14

and constant bias currents , . The transient response of summer circuit is shown in Fig. 3.15 where I_1 and I_2 are the input current signals and Iwp as output current.

3.3.3 Subtraction

Signal subtraction is a special case of addition where the signal to be subtracted undergo a sign inversion before addition. A typical subtractor circuit using VDCC is shown in Fig. 3.16. In this figure, all the passive elements are grounded which cover less area rather floating elements in IC fabrication [2], [5]. The transfer function is described by Eq. 3.8. Subtractor is used for many ASP applications. A typical application is used to design summer/subtractor circuit is shown in Fig. 3.17. This circuit is used to add and subtract simultaneously using only single VDCC and four grounded resistors. Summer/Subtractor circuit is used to designed simulated inductor in wave active filter theory. Its input-output relation is defined by Eq. 3.9

(3.8)

(3.9)

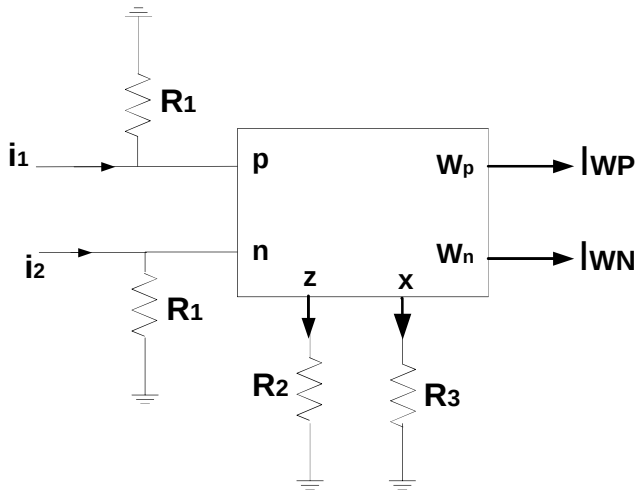


Fig. 3.16 VDCC based Subtractor circuit

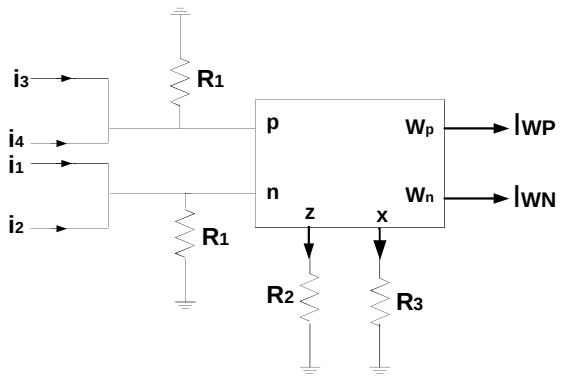


Fig. 3.17 Summer/ Subtractor based on VDCC

3.3.2.1 Simulation Results

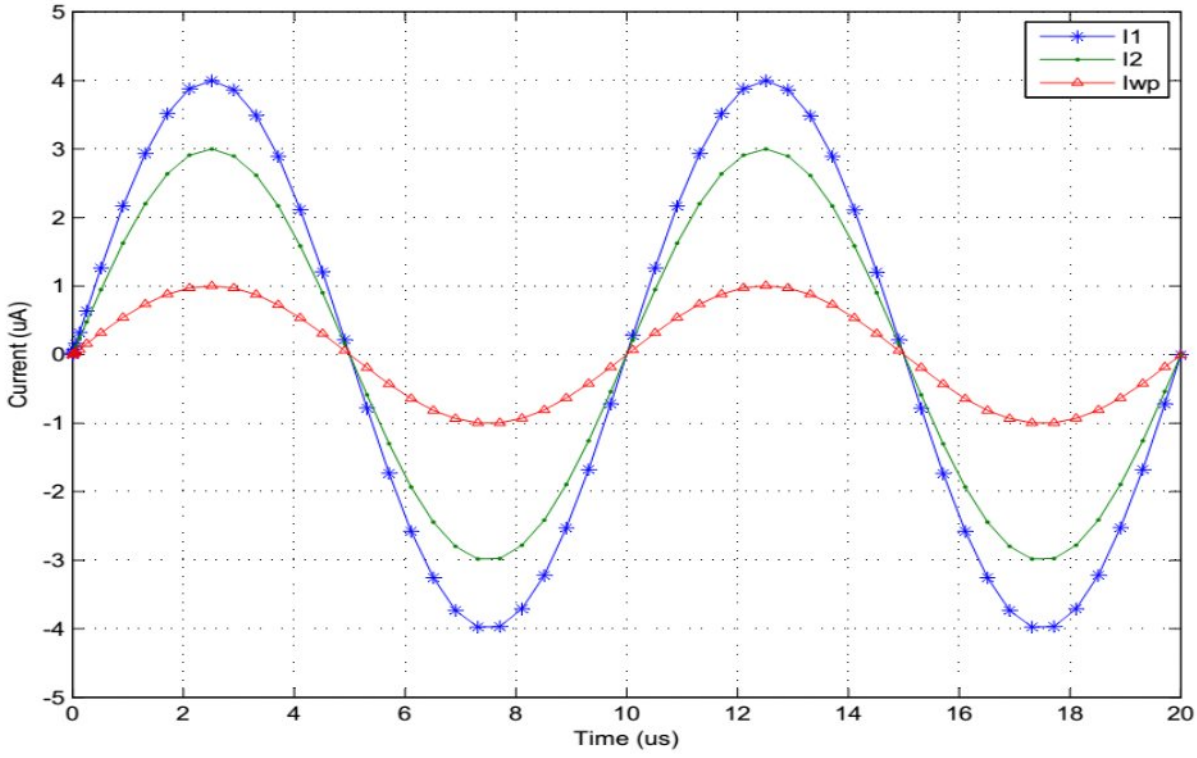


Fig. 3.18 Time response of subtractor circuit of Fig. 3.16

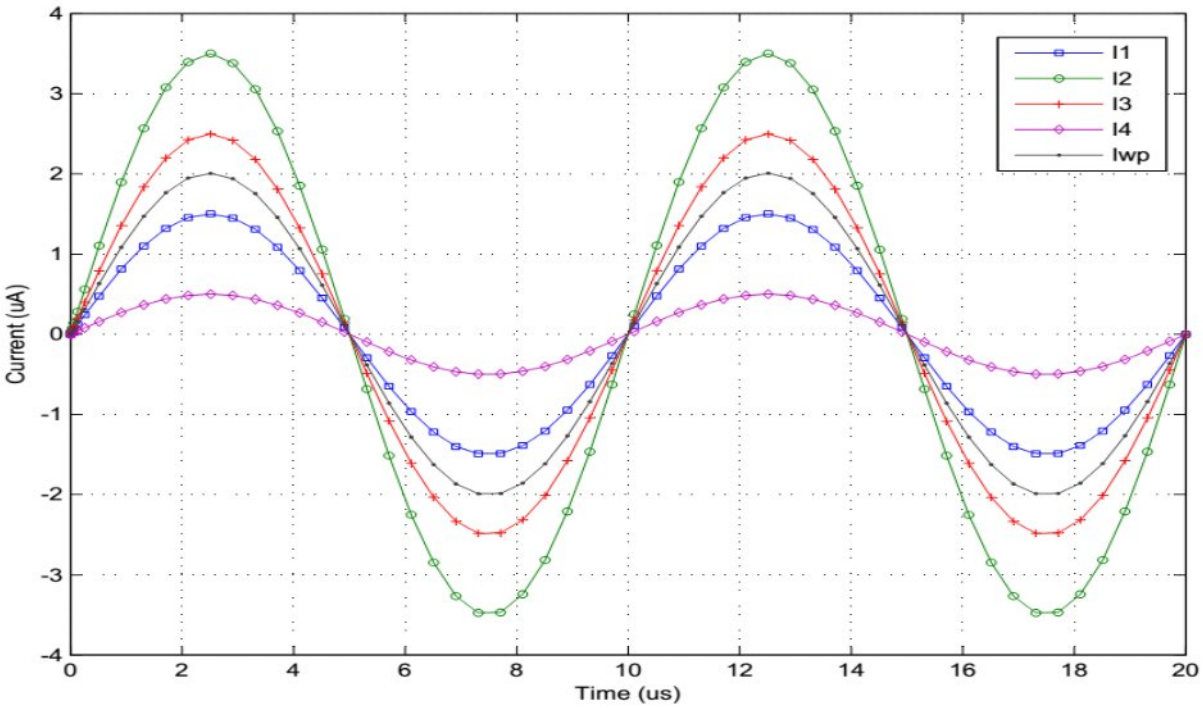


Fig. 3.19 Time response of the Fig. 3.17

The subtractor circuit is shown in Fig. 3.16 was simulated in PSPICE. The passive elements are selected as [illegible], [illegible], [illegible]. The supply voltages, are selected as [illegible] and constant bias currents [illegible], [illegible]. The transient response of subtractor circuit is shown in Fig. 3.18.

Above discussed passive parameters are used also in Fig. 3.17 and its time response of this circuit is shown in Fig. 3.19 where I_1, I_2, I_3 and I_4 are the input signal and Iwp as output current signal.

3.3.4 Differentiation

Differentiation is a linear operation in analog signal processing that gives the derivative of the signal processed. Differentiation can be used as peak detector: the derivative of a signal gives a zero crossing whenever the analog signal attains a peak value. If a signal is filtered and then passed through the differentiator, this method is more robust then detecting the peak amplitude because added noise could give erratic outcomes [5]. A current mode VDCC [2] based differentiator is shown in Fig. 3.20. In which one grounded capacitor and two grounded resistors are used to realize this circuit. The input-output relation can be characterized as

$$\frac{\partial I_{out}}{\partial V_{in}} = g_{m1}g_{m2}g_{m3}R_1R_2 \quad (3.10)$$

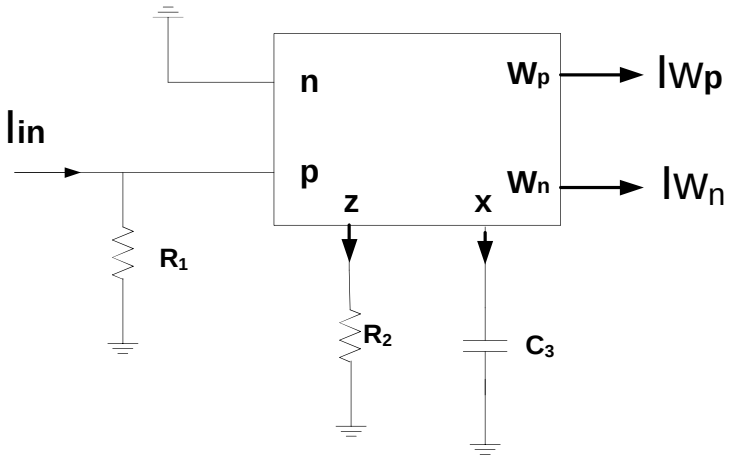


Fig. 3.20 Circuit diagram of differentiator using VDCC

3.3.3.1 Simulation Results

The integrator is shown in Fig. 3.20 was simulated using PSPICE. The supply voltages, were selected as $V_{DD} = -V_{SS} = 0.9V$ and bias currents $I_{B1} = 34.5$ uA and $I_{B2} = 100$uA. The passive elements were selected as $R_1 = 500\Omega$, $R_2 = 1k\Omega$ and $C_3 = 13pF$. The time response of the Fig. 3.20 is shown in Fig. 3.21

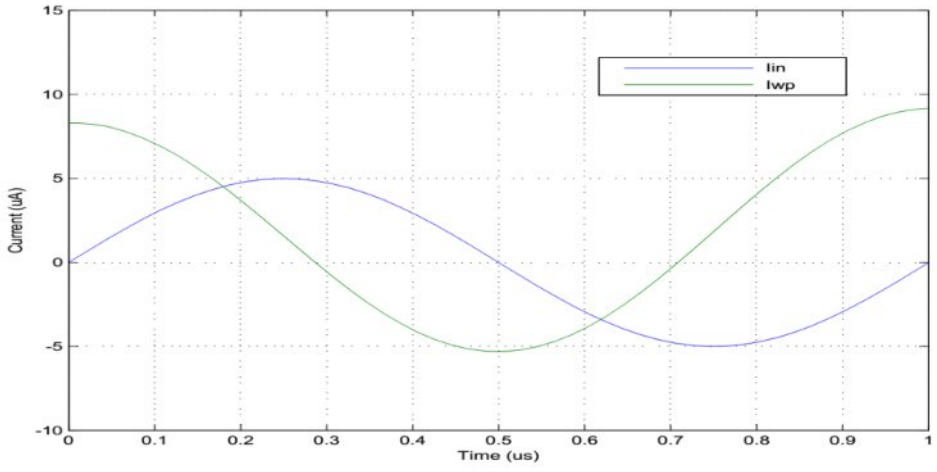


Fig. 3.21 Time response of differentiator circuit shown in Fig. 3.20

3.3.5 Integration

Integration is a basic linear function in analog signal processing. Mathematically, the integral give the area under the waveform or analog signal. In frequency domain, integration is defined by a transfer characteristic whose slope decreases by 20 dB/decade. VDCC based Integrator circuit is shown in Fig. 3.22 and its transfer function is defined as

$$\frac{V_{out}}{I_{in}} = \frac{1}{sC_2R_3R_1} \tag{3.11}$$

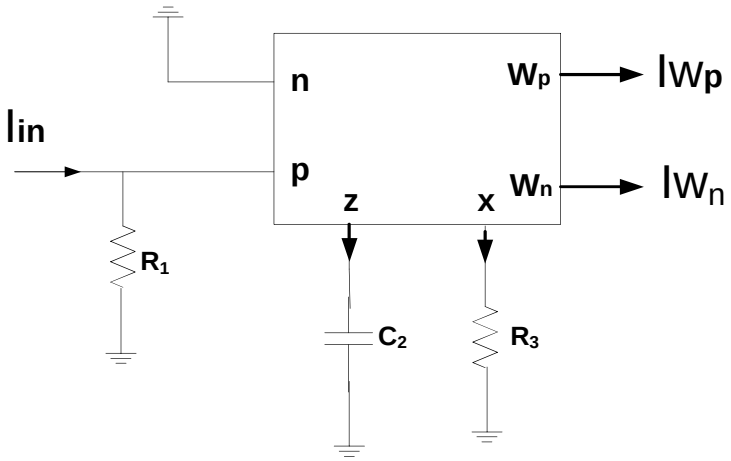


Fig. 3.22 VDCC based ideal integrator

3.3.4.1 Simulation Results

The integrator is shown in Fig. 3.22 was simulated using PSPICE. The supply voltages, were selected as V_{DD} = - V_{SS} = 0.9V and bias currents I_{B1} = 34.2 uA and I_{B2} = 100uA. The passive elements were selected as R_1 = 500Ω, R_3 = 1kΩ and C_2= 13pF. The time response of the Fig. 3.22 is shown in Fig. 3.23.

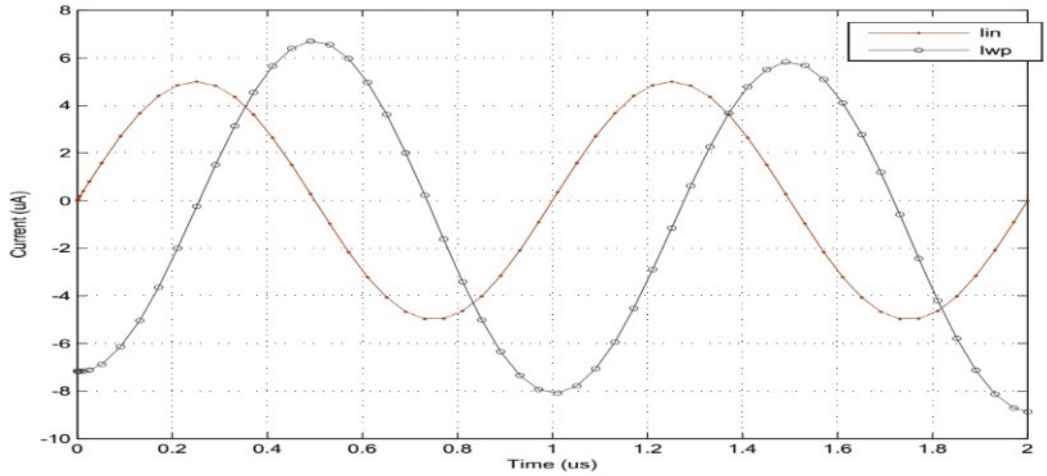
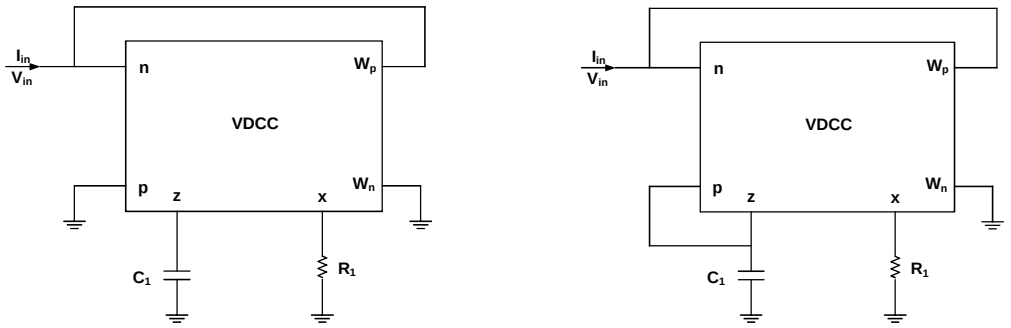


Fig 3.23 Time response of integrator circuit is shown in Fig. 3.22

3.4 VDCC BASED GROUNDED INDUCTANCE SIMULATION

VDCC based grounded inductance simulator circuit was proposed by Kacar, Yesil, Minaei and Kuntman [2]. The circuits for realization of grounded inductance are shown in Fig. 3.24. The entire configurations are designed with single VDCC, one grounded resistor and one grounded capacitor. By circuit analysis of these simulated inductor configuration, the input impedance, equivalent inductance and equivalent resistance as give in Table 3.1. Negative simulated inductor is used for many applications like designing of oscillators, active filters, impedance matching and analog phase shifter.



(a) (d)

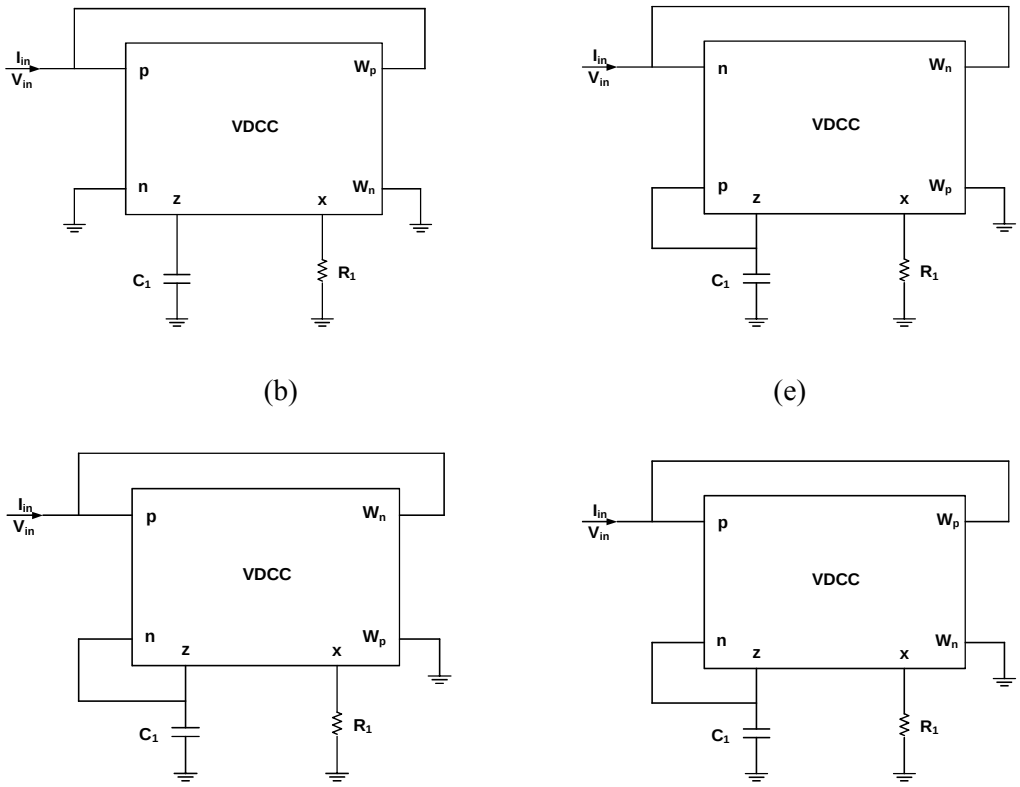


Fig. 3.24 Inductance simulators realized using VDCC [2]

Circuit	Z_{eq} input impedance	L_{eq} equivalent inductance	R_{eq} equivalent resistance	Type
Fig. 3.19a	$\frac{sC_1R_1}{}$	$\frac{C_1R_1}{}$	-	Pure L
Fig. 3.19b	$-\frac{sC_1R_1}{}$	$-\frac{C_1R_1}{}$	-	Pure – L
Fig. 3.19c	$\frac{sC_1R_1}{} + R_1$	$\frac{C_1R_1}{}$	R_1	+ L series with +R
Fig. 3.19d	$\frac{sC_1R_1}{} - R_1$	$\frac{C_1R_1}{}$	$-R_1$	+ L series with -R
Fig. 3.19e	$-\frac{sC_1R_1}{} + R_1$	$-\frac{C_1R_1}{}$	R_1	- L series with +R
Fig. 3.19f	$-\frac{sC_1R_1}{} - R_1$	$-\frac{C_1R_1}{}$	$-R_1$	- L series with –R

Table 3.1 The actively realizable inductance forms [2]

3.4.1 Parasitic Effect in VDCC

The simulated pure inductance of Fig. 3.24a is chosen for consideration of the parasitic impedances on VDCC and its equivalent circuit is shown in Fig. 3.20a and b respectively. As shown in Fig. 3.25a [illegible], [illegible], [illegible], [illegible] and [illegible] are the parasitic elements at different terminals of the VDCC [2], [6-13]. After consideration these effects, the impedance of simulated inductance is described as [1, 2]

[illegible] (3.12)

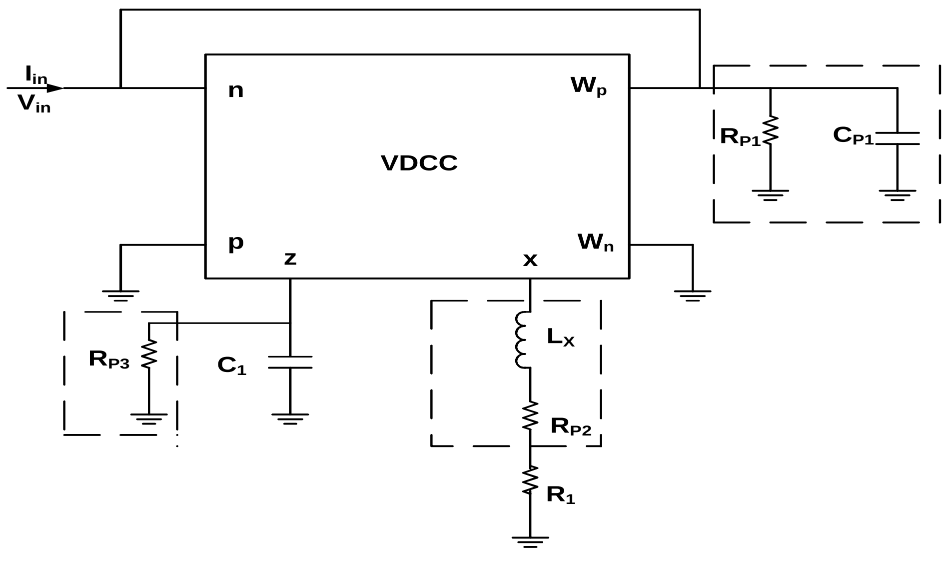
Circuit elements of Fig. 3.25b can be described from Eq. 3.12 as

[illegible] (3.13a)

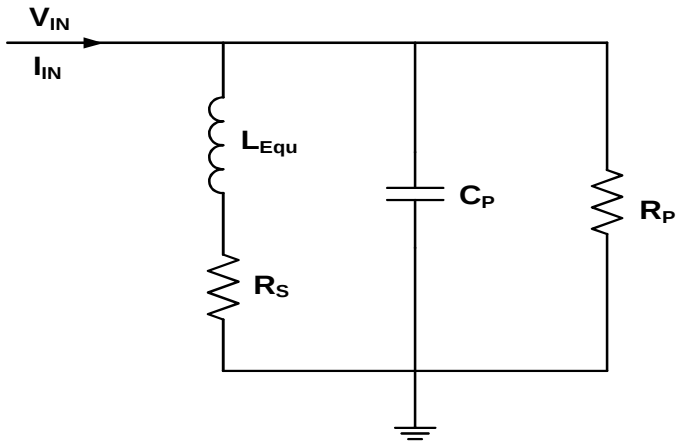
[illegible] (3.13b)

[illegible] (3.13c)

[illegible] (3.13d)



(a)



(b)

Fig. 3.25 (a) Inductance simulator with the parasitic impedances of VDCC

(b) Its equivalent passive realization [2]

If the circuit is used at high frequency then L_{eq} can be negative which may cause of the instability. To overcome this problem, L_{eq} should be greater than zero ($L_{eq} > 0$) as

$$\frac{R_{p1}R_{p2}R_{p3}}{R_{p4}} > \omega^2 L_{eq} C_{p1} \tag{3.14}$$

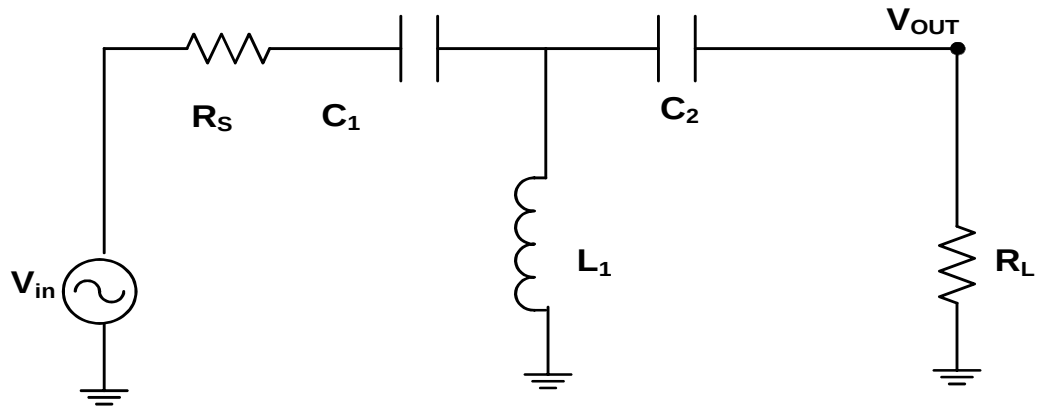
where f is the frequency of operation. Maximum frequency of operation can be derived from Eq. (3.14) to prevent stability problem can be defined as [2]

$$f_{max} = \frac{1}{2\pi}\sqrt{\frac{R_{p1}R_{p2}R_{p3}}{L_{eq}C_{p1}R_{p4}}} \tag{3.15}$$

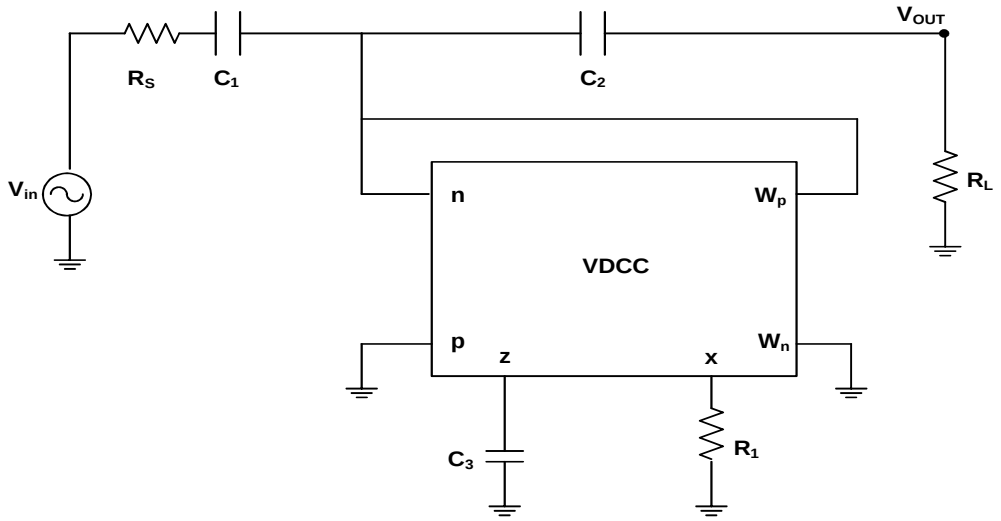
Thus, f_{max} can be increased by decreasing the parasitic inductance L_{eq}.

3.4.2 Application Example of New Grounded Inductance

Passive prototype of the third order butterworth high-pass filter is shown in Fig. 3.26a. In this circuit, grounded inductance is used which can be replaced by the simulated inductance. The VDCC based simulated grounded inductance is used in Fig. 3,26b to design a HPF where for pure inductance is taken from Fig. 3.24a.



(a)



(b)

Fig. 3.26 3rd order high pass Butterworth filter (a) Passive realization

(b) Realization with VDCC based inductance simulator [2]

3.4.3 Simulation Results

The simulated inductance (Fig. 3.24a) was used to design a 3rd order high-pass filter and verified the performance of simulated grounded inductance. The supply voltages, were selected as $\square_{\square\square} \square \overline{\square_{\square\square}} \square \square\square\square$ and constant bias currents are $\square_{\square\square} \square \square\square\square\square$ ($\square_{\square} \square \square\square\square\square\square\square\square$, $\square_{\square\square} \square \square\square\square\square$. The passive elements are selected as $\square_{\square} \square \square_{\square} \square \square\square\square\Omega$, $\square_{\square} \square \square_{\square} \square \square\square\square\square\square\square$, $\square_{\square} \square \square\square\Omega$ and $\square_{\square} \square \square\square\square\square$, which results in $\square_{\square\square} \square \square\square\square\square\square$. The frequency response of 3rd order HPF is shown in Fig. 3.27.

To find out the input range of the 3rd order HPF a sinusoidal signal of [illegible] with different amplitudes of input are applied. The THD of the output signal versus amplitude of input is shown in Fig. 3.28. By PSPICE simulation, the power dissipation of the filter was calculated as 0.845 mW which is acceptable to design an IC implementation.

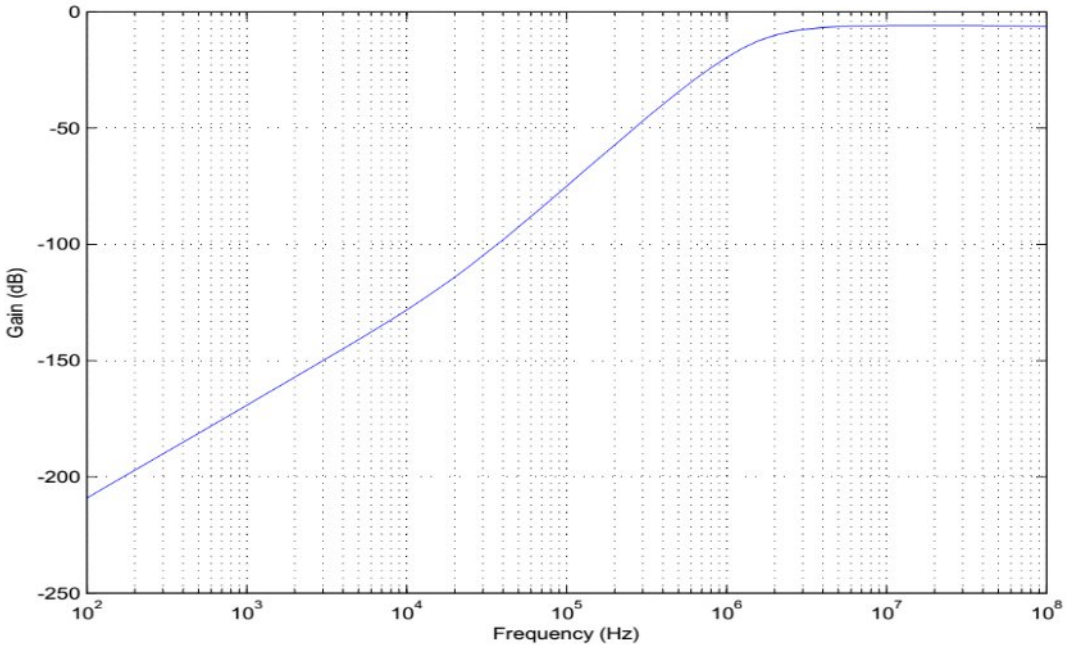


Fig. 3.27 Frequency response of 3rd order Butterworth high-pass filter

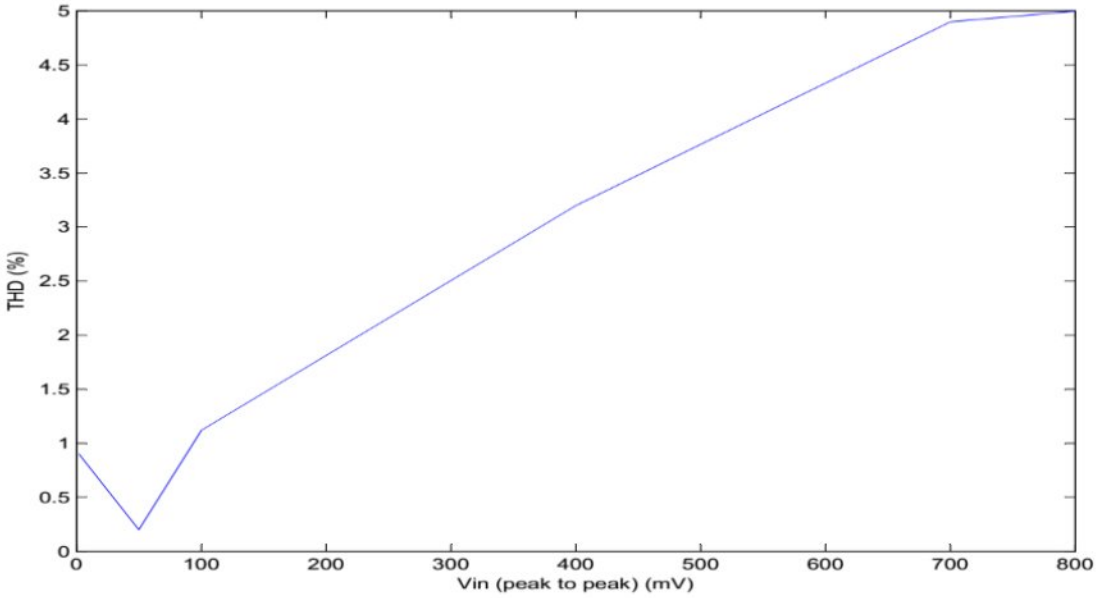


Fig. 3.28 Total harmonic distortion of high pass filter

3.5 ELECTRONICALLY CONTROLLABLE SYNTHETIC FLOATHING INDUCTANCE USING VDCC

The floating inductance simulator was proposed by Prasad and Ahmad [3]. The block diagram of VDCC based floating inductance simulator is shown in Fig. 3.29. This floating inductance (FI) is realized only using single VDCC active building block, one grounded resistor and one grounded capacitor (as desired for IC implementation). The circuit analysis of Fig. 3.29 is defined as

(3.16)

The equivalent inductance value is given as

(3.17)

where is defined as transconductance gain which can be controlled by bias current [2]. So FI is called electronically-controlled FI.

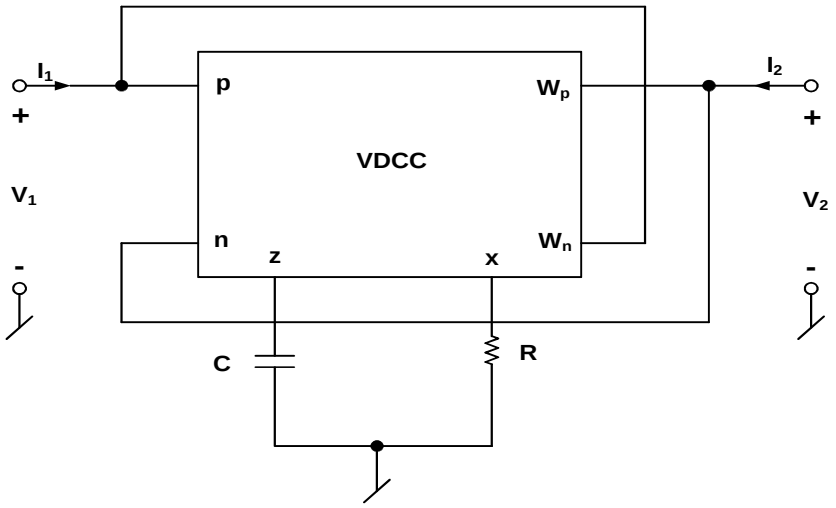


Fig. 3.29 VDCC based Floating Inductance [3]

3.5.1 Application Example of Floating Inductance Circuit

Floating inductor is used in many applications such as designing of ladder circuits, filters and oscillators etc. The filter application of FI circuit is demonstrated to implement band pass filter (BPF). The transfer function for the band pass filter is defined as [2, 3]

$$\frac{V_0}{V_{in}} = \frac{\frac{g_{m1}g_{m2}}{C_1C_2}}{s^2 + s\left(\frac{g_{m2}}{C_2}\right)\left(\frac{1}{R_2}\right) + \frac{g_{m1}g_{m2}}{C_1C_2}} \qquad (3.18)$$

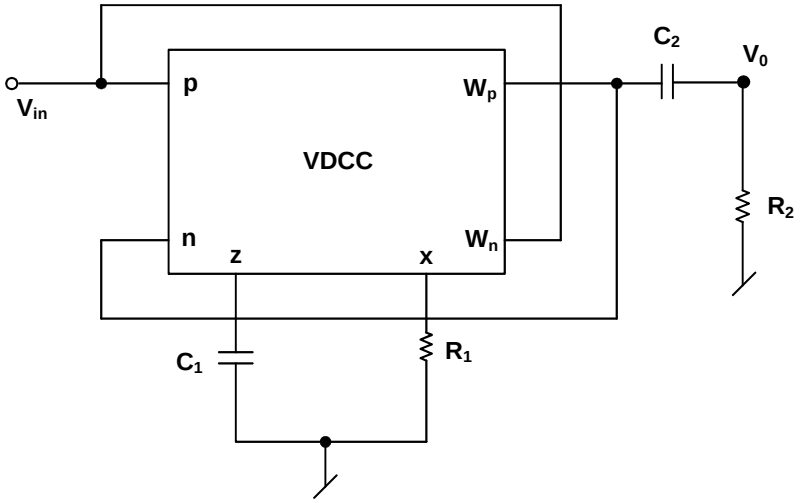


Fig. 3.30 Band pass filter implemented using FI circuit of Fig. 3.29

3.5.2 Simulation Results

The VDCC based simulated floating inductance (FI) (Fig. 3.24) is used to design a band-pass filter and verified the performance of floating inductance. The supply voltages, are selected as $V_{DD} = |V_{SS}| = 2.5V$ and constant bias currents are $I_{B1} = 100\mu A$ ($I_1 = 100\mu A$, $I_{B2} = 50\mu A$. The passive elements are selected as $C_1 = 100pF$, $C_2 = 50pF$, $R_1 = 1k\Omega$ and $R_2 = 2k\Omega$. The frequency response and time response are shown in Fig. 3.31 and Fig. 3.32 respectively. The simulated center frequency (f_0) was found 1.99MHz. The other filter parameters were calculated using PSPICE simulation as below

Total harmonic distortion at input frequency 2MHz = 2.91%

Total power dissipation = 0.845 mW

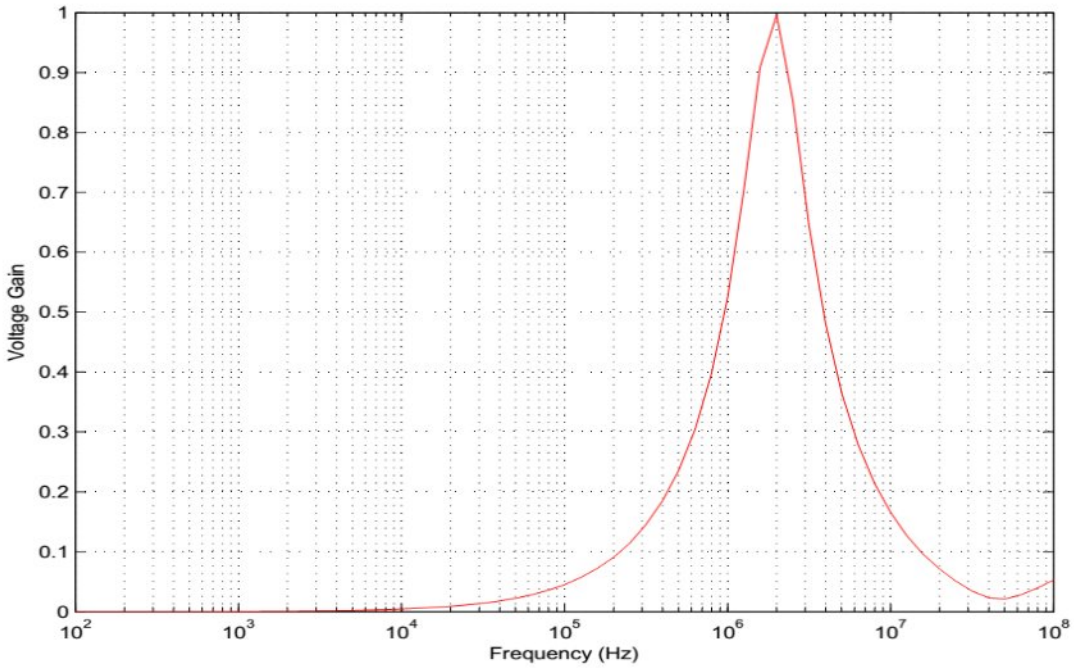


Fig. 3.31 Frequency response of band-pass filter

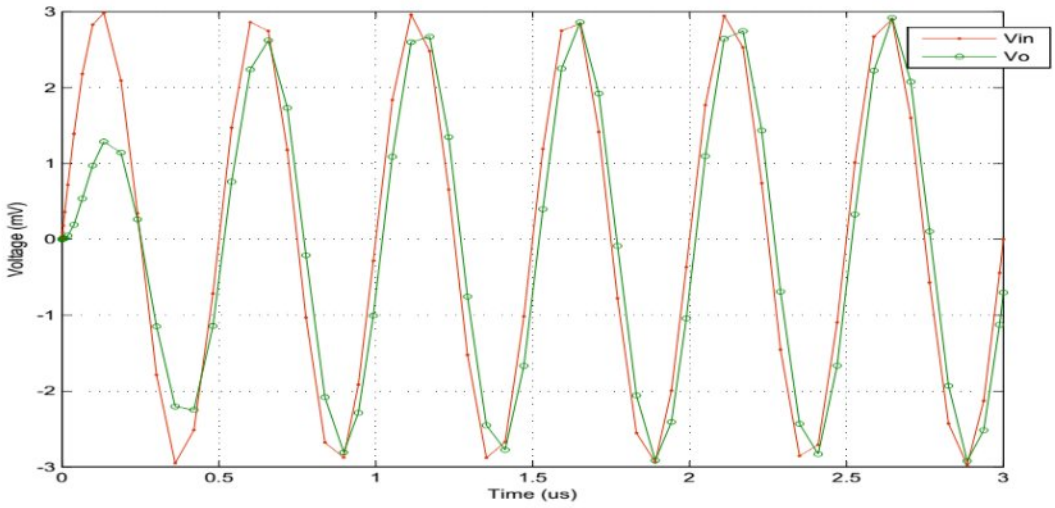


Fig. 3.32 Transient response of band-pass filter

3.6 CONCLUSION

In this chapter, a novel active building block namely the VDCC is discussed in detail. Its DC and AC characteristics of input-output were verified using PSPICE simulation. The basic signal processing applications such as adder, subtractor, differentiator, integrator and amplifier were designed using VDCC and simulated in PSPICE. In the section 3.4, grounded inductance simulation was described and applied to design a high-pass filter. In yet another application, floating inductance was designed

and simulated in PSPICE. The floating inductance was verified using PSPICE simulation of the band pass filter (BPF) with specified central frequency.

REFERENCES

[1] Biolek D., Senani R., Biolkova V., Kolka Z., "Active Elements for Analog Signal Processing: Classification, Review and New Proposals", Radioengineering, Vol. 17, No. 4, p. 15 – 32, 2008.

[2] Fırat Kacar, Abdullah Yesil, Shahram Minaei and Hakan Kuntman, "Positive/Negative Lossy/Lossless Grounded Inductance Simulators Employing Single VDCC and Only Two Passive Elements", International Journal of Electronics and Communications (AEÜ), pp.73– 78, 2014.

[3] Dinesh Prasad, Javed Ahmad, "New Electronically-Controllable Lossless Synthetic Floating Inductance Circuit Using Single VDCC ", Circuits and Systems, pages 13-17, 2014.

[4] Minaei S, Yuce E. " Novel Voltage-Mode All-Pass Filter Based on Using DVCCs" Circ. Syst. Sig. Process., 391–402, 2010.

[5] Ramon P. Areny, John G. Webster, "Analog Signal Processing", Wiley India Pvt. Ltd., 2012

[6] Senani R., "Three Op-Amp Floating Immittance Simulators: A Retrospection", IEEE Trans Circ Syst II, 36(11):1463–5, 1989.

[7] Cicekoglu O., "New Current Conveyor Based Active-Gyrator Implementation", Microelectron J, 29(8):525–8, 1998.

[8] Kacar F, Kuntman H., "CFOA-Based Lossless and Lossy Inductance Simulators", Radioengineering, 20(3), 2011.

[9] Ibrahim MA, Minaei S, Yuce E, Herencsar N, Koton J., "Lossless Grounded Inductance Simulation Using Only One Modified Dual Output DDCC", 34th International Conference on Telecommunications and Signal Processing (TSP), p. 261–4, 2011.

[10] Prasad D, Bhaskar DR, Singh AK, "New Grounded and Floating Simulated Inductance Circuits Using Current Differencing Transconductance Amplifiers", Radioengineering, 19(1):194–8, 2010.

[11] Keskin AU, Erhan H., "CDBA-Based Synthetic Floating Inductance Circuits With Electronic Tuning Properties", ETRI J, 27(2):239–42, 2005.

[12] Koomgaew C, Petchmaneelumka W, Riewruja V, “OTA-Based Floating Inductance Simulator”, ICROS-SICE International Joint Conference, Japan: Fukuoka International Congress Center, p. 857–60, 2009.

[13] Myderrizi I, Minaei S, Yüce E, “DXCCII-Based Grounded Inductance Simulators and Filter Applications”, Microelectron J ;42(9):1074–81, 2011.

CHAPTER 4

A NOVEL MULTI FUNCTION CURRENT MODE BIQUAD USING VDCC

4.1 INTRODUCTION

In the previous chapter some of the applications of VDCC in current mode signal processing have been discussed. The VDCC appears to be a very versatile active building block similar to other derivatives of current conveyors which were presented in chapter-II. A VDCC combines the features of a current conveyor and an operational transconductance amplifier. In the present chapter we have proposed a novel application of VDCC in the realization of a single input single output current mode multifunction filter with the following features.

(i) tunability of central frequency

(ii) tunability of bandwidth

Before we present the circuit of the multifunction filter it is worthwhile to have a review of multifunction/universal filters.

Realisation of filters, particularly biquad filters has been a very prominent application of any active building block. Out of different filter configurations implemented from these blocks universal / multifunction filter realisations are preferred as they provide more than one filter function from the same structure. Apart from their usual application as standard second-order building blocks for higher order filters, multifunction active biquad filters (e.g. those realising lowpass (LP), bandpass (BP) and highpass (HP) simultaneously from three different output terminals) find

applications in phase locked loop FM stereo demodulators, touch tone telephone systems and crossover networks used in three-way high fidelity loud speakers.

Multifunction filters can either be of fixed topology type in which the number and nature of the active and passive elements remain fixed and usually at least three out of the five generic filtering functions namely HP, LP, BP, band elimination (BE) and allpass (AP) are simultaneously available in current-mode/ voltage-mode or both, or of variable topology type in which the nature and number of elements vary for different output responses. A multifunction biquad is said to be 'Universal' if it is capable of realising all the five standard filter functions.

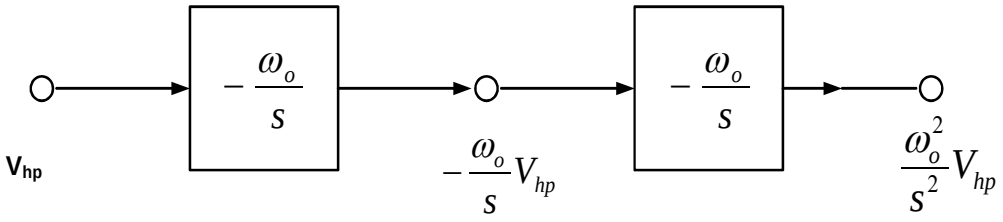
Yet another classification can be made on the basis of the number of inputs and number of outputs present in a particular realisation. In single-input single-output (SISO) universal biquads there is one input and only one output response is available at a time. This type of filter belongs to the variable topology class. In multiple-input single-output (MISO) type universal filters, multiple inputs are required and a single output response is available at a time. This type of filter will also be classified under variable topology. In single-input multiple-outputs (SIMO) type universal filters only one input is required and different output responses are simultaneously available at different nodes of the circuit. Lastly, under multiple-inputs multiple-output (MIMO) class, more than one input is applied and a particular output response is obtained by judicious choice of inputs or combinations thereof.

The proposed multifunction filter is based on the two integrator loop topology first proposed by Kerwin Hulseman and Newcomb and in the following we give a brief introduction of the two integrator in a loop topology before we present the proposed multifunction filter.

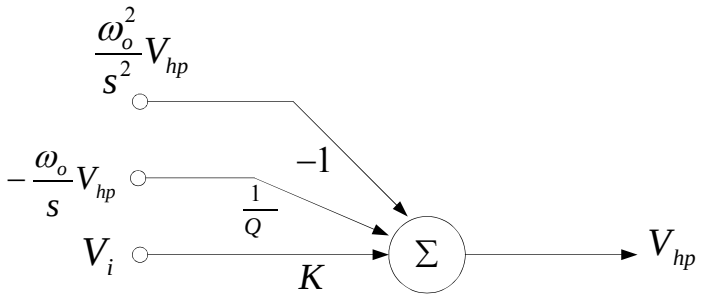
4.1.1 Kerwin-Huelsman-Newcomb (KHN) Biquad Filter

The kerwin-Huelsman-Newcomb (KHN) biquad filter is also known as state-variable filter which is used for multifunction filtering structures [4-9]. This structure is realized using two integrators in the feedback loops. The most important feature of this structure is to provide second order low-pass filter (LPF), high-pass filter (HPF) and band-pass filter (BPF) simultaneously. KHN-biquad filter is normally used because it provides some advantages like low component spread, low active and passive

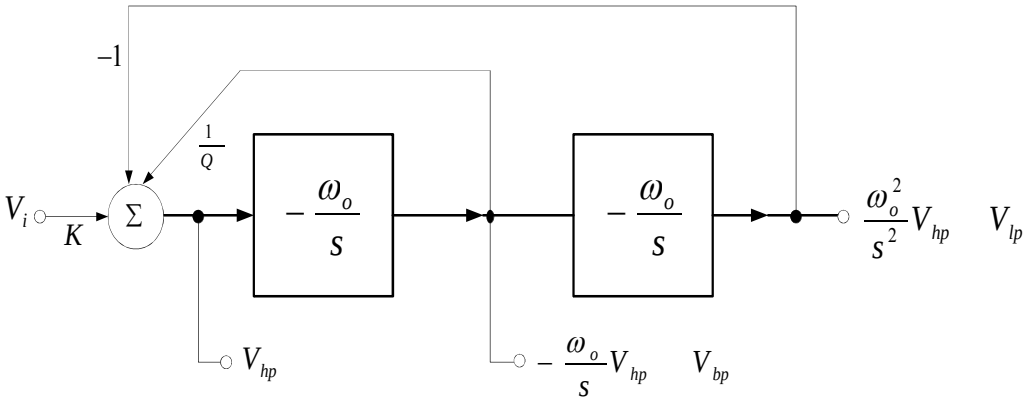
sensitivities and sufficient stable response. In literature, different active blocks are used to design KHN biquad filter. Some of them operate in current mode and others in voltage mode. Current mode circuits have some advantages over voltage mode such as linearity, less power consumption, wider bandwidth, larger dynamic range and simplicity in the circuit realization. The block diagram of KHN-biquad filter is shown in Fig. 4.1.



(a)



(b)



(c)

Fig 4.1 Block diagram of KHN biquad filter using two integrators in feedback loop

Consider a second order high-pass filter (HPF) as

$$\frac{V_{out}}{V_{in}} = \frac{s^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \tag{4.1}$$

where K is the gain at high frequency. To rearrange the Eq. 4.1, the expression as follows

$$V_{out} = \frac{1}{s}\left(\frac{\omega_0}{Q}V_{out}\right) + \frac{1}{s^2}\left(\omega_0^2 V_{out}\right) \tag{4.2}$$

The output signal V_{out} can be obtained by summing three signals which is shown in Fig. 4.1b from which two input signals can be generated which is shown by Fig. 4.1a where two integrators are used. The V_{out} signal can derived from Eq. 4.2 which is found as follows

$$V_{out} = V_{out}\left(\frac{1}{s}\right)\left(\frac{\omega_0}{Q}\right)V_{out} + \left(\frac{1}{s^2}\right)\omega_0^2 V_{out} \tag{4.3}$$

The transfer function of BPF which can be defined as

$$\frac{V_{out}}{V_{in}} = \left(\frac{1}{s}\right)\frac{\frac{\omega_0}{Q}s}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \tag{4.4}$$

Similarly, the transfer function of low pass filter (LPF) is derived as

$$\frac{V_{out}}{V_{in}} = \left(\frac{1}{s}\right)\left(\frac{1}{s}\right)\frac{\omega_0^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \tag{4.5}$$

The two integrator-loop biquad filter realizes three basic second order filter functions HP, BP and LP simultaneously. This circuit is most popular and it is commonly known as *universal active filter* (the kerwin-Huelsman-Newcomb biquad).

4.1.2 Tow–Thomas Biquad Filter

The block diagram of Tow-Thomas (TT) biquad filter is shown in Fig. 4.2. In TT based filters, two outputs can be taken simultaneously such as band-pass filter and low pass filter responses. Two negative integrator loops are used in which one is lossy integrator and other one is ideal integrator. The integrators can be realized by active building blocks [2]. One active building block is used to realize difference circuit. So a TT biquad filter can be implemented by using three active building blocks. In literature, TT biquad filter was implemented using Op-amp, OTRA, CCII and DVCC [3]. For

high quality factor (Q) and high center frequency the Tow-Thomas filter may be no longer right choice to implement a high Q based band pass filter.

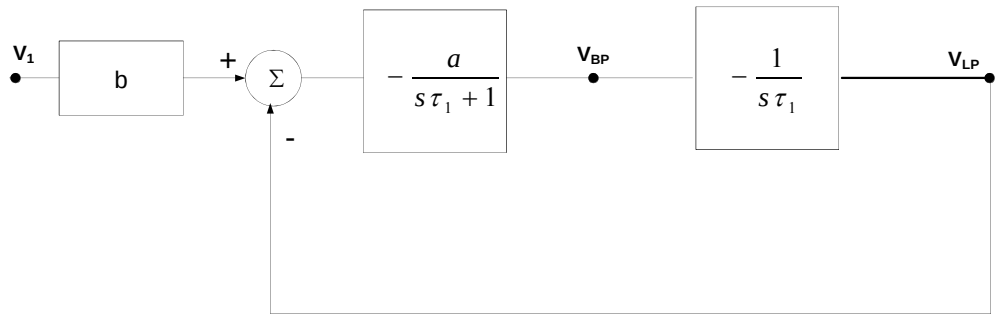


Fig. 4.2 Equivalent block diagram of the Tow-Thomas Filter [3]

4.2 THE PROPOSED VDCC BASED CURRENT MODE MULTI FUNCTION BIQUAD FILTER

The block diagram of proposed current mode multifunction biquad filter is shown in Fig. 4.3 which contains two lossless integrators ($\frac{?}{??_?}$ and $\frac{?}{??_?}$), one summer and proportional gain blocks (1 and K). The proposed VDCC based current mode multifunction biquad filter is shown in Fig. 4.4. In this, most important thing is that all the passive elements are used as grounded element. So it is easy to fabricate in the form of IC [9].

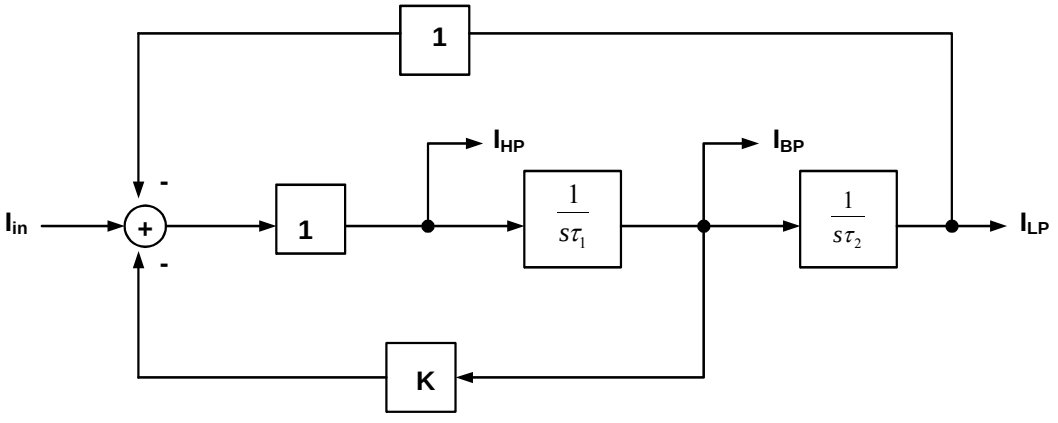


Fig. 4.3 Signal processing block diagram for realizing current mode KHN biquad filter

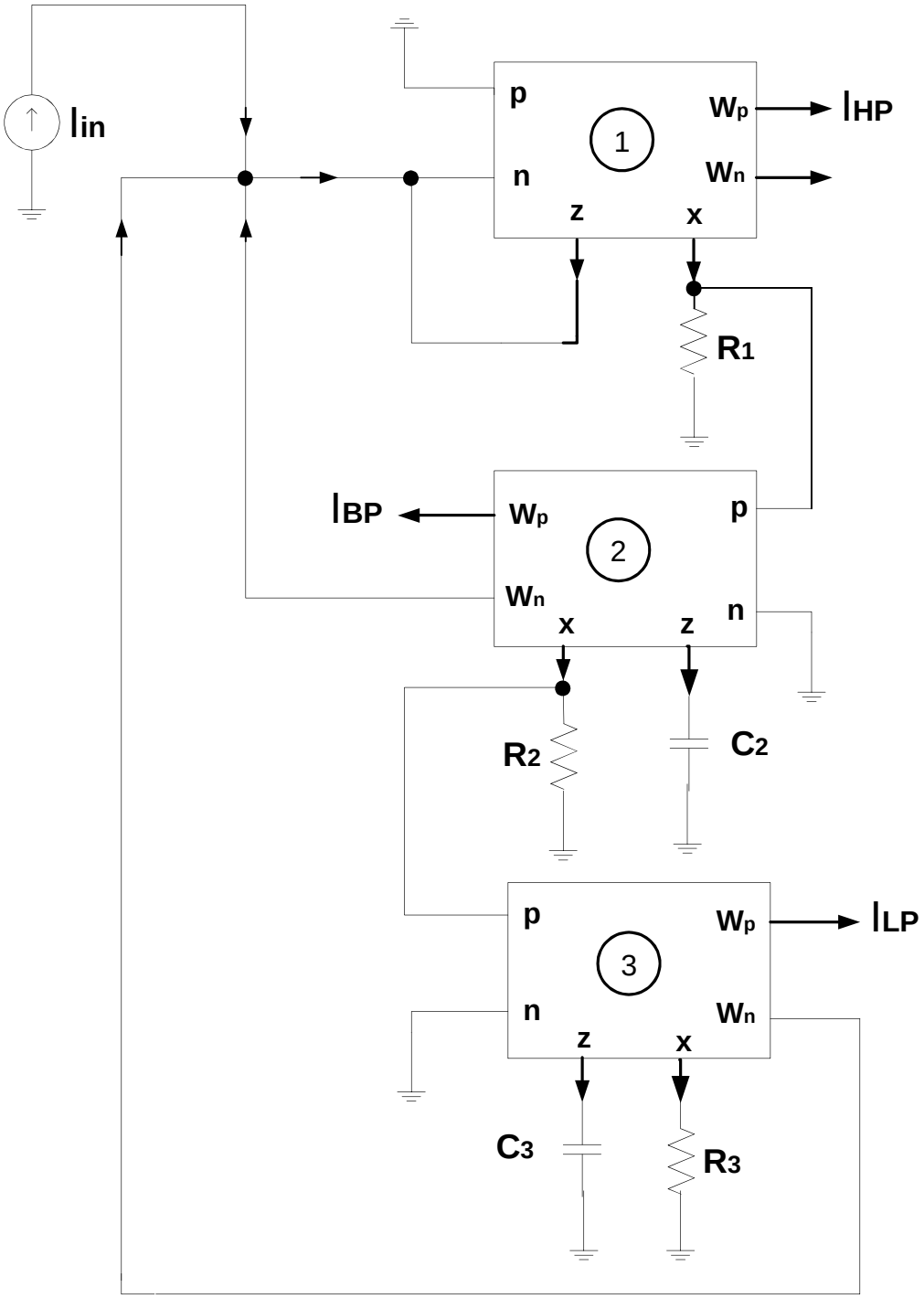


Fig. 4.4 Proposed current mode multifunction biquad filter using VDCC

By analysis the circuit shown in Fig. 4.4, the HP filter expression is given as

$$\text{(4.6)}$$

$$\frac{V_{out}}{V_{in}} = \frac{\frac{s}{C_1 R_1}}{D(s)} \quad (4.7)$$

Similarly, BPF and LPF transfer functions are defined as follows

$$\frac{V_{BP}}{V_{in}} = \frac{\frac{s}{C_1 R_1}}{D(s)} \quad (4.8)$$

and $$\frac{V_{LP}}{V_{in}} = \frac{\frac{1}{C_1 C_2 R_3 R_4}}{D(s)} \quad (4.9)$$

where D(s) is the characteristic equation and its expression is derived as

$$D(s) = s^2 + s\left(\frac{1}{C_1 R_1} + \frac{1}{C_2 R_3}\right) + \frac{1}{C_1 C_2 R_3 R_4} \quad (4.10)$$

The important parameters of the filters are pole frequency (ω_o) and bandwidth (BW) which can be expressed as

$$\omega_o = \sqrt{\frac{1}{C_1 C_2 R_3 R_4}} \quad ; \quad BW = \frac{1}{C_2 R_3} \quad (4.11)$$

It can be remarked that pole frequency can be adjusted by varying the R_4 without affecting the bandwidth (BW). Bandwidth can be controlled by R_3. So ω_o and BW can be tuned independently.

4.2.1 Circuit Sensitivities

The sensitivities of the proposed circuit can be described as

$$S^{\omega_o}_{C_1} = S^{\omega_o}_{C_2} = S^{\omega_o}_{R_3} = S^{\omega_o}_{R_4} = -\frac{1}{2}; \; S^{BW}_{C_2} = S^{BW}_{R_3} = -1; \; S^{BW}_{C_1} = S^{BW}_{R_4} = 0 \quad (4.12)$$

Therefore, all the active and passive sensitivities are equal or less than unity in magnitude.

4.2.2 Simulation Results

To prove the theoretical validity of the proposed filter (Fig.4.4), the filter was simulated with PSPICE program. The passive elements are selected as $R_1 = 1k\Omega$, $R_2 = 1k\Omega$, $R_3 = 1k\Omega$, $R_4 = 1k\Omega$ and $R_5 = 1k\Omega$. The supply voltages, are selected as $V_{DD} = -V_{SS} = 2.5V$, $V_{BB} = 1V$ and $V_{CC} = 1V$. The LPF, HPF and BPF frequency responses and time responses of Fig. 4.4 is shown in Fig. 4.5 and Fig. 4.6 respectively. The simulated center frequency of BPF was measured as 5.4 MHz. In the case of band-pass filter (BPF), center frequency and bandwidth (BW) can be varied which are shown in Fig. 4.7 and Fig. 4.8 respectively. The Monte Carlo simulation is

shown on Fig. 4.9 while input signal was taken as sinusoidal 20 uA (1 MHz) and the tolerance band in R_2 and R_3 was selected as 5%. The other important simulation results are discussed as below

Total power dissipation = 2.01 mW

Total harmonic distortion at input signal 20 uA (1 MHz) = 0.71 %

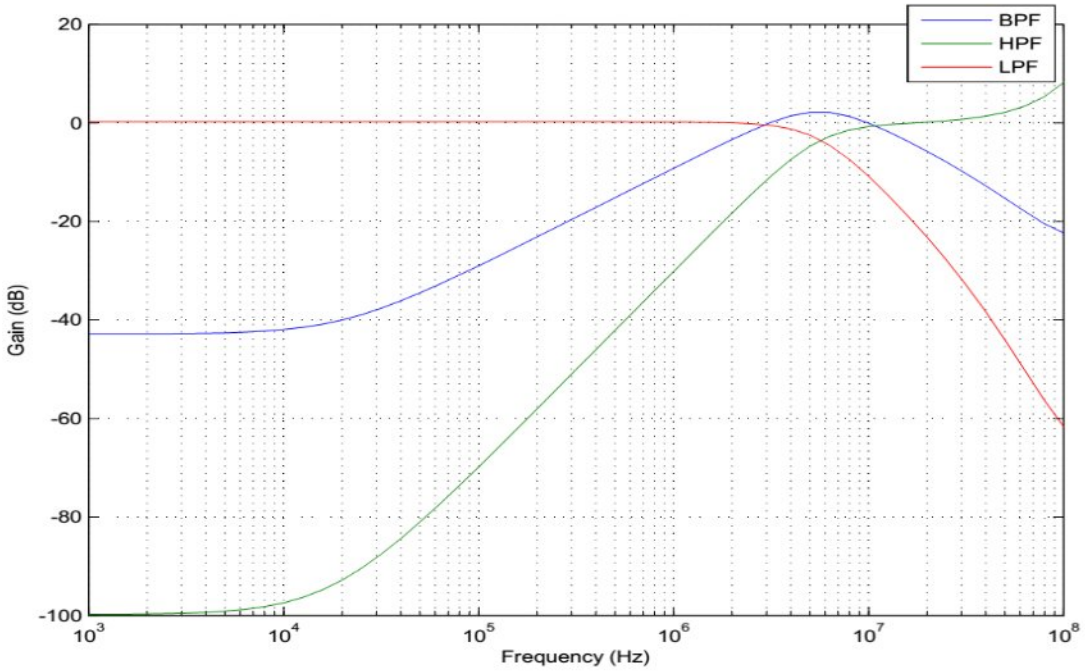


Fig. 4.5 Frequency Response of proposed multifunction biquad filter

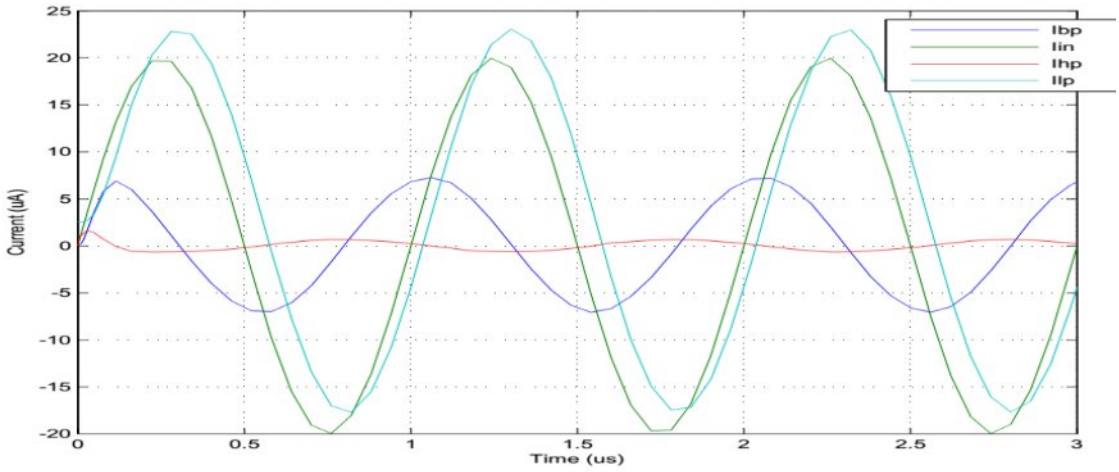


Fig. 4.6 Time response of LPF, HPF, BPF and input current signal (at 1 MHz)

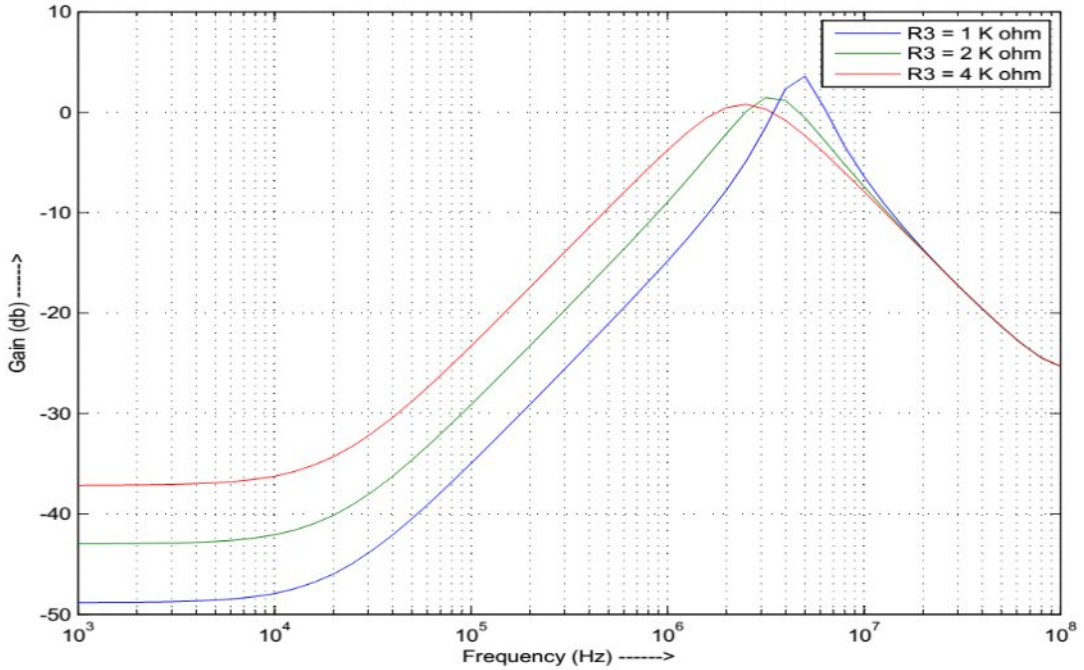


Fig. 4.7 Frequency response of BPF when is varied

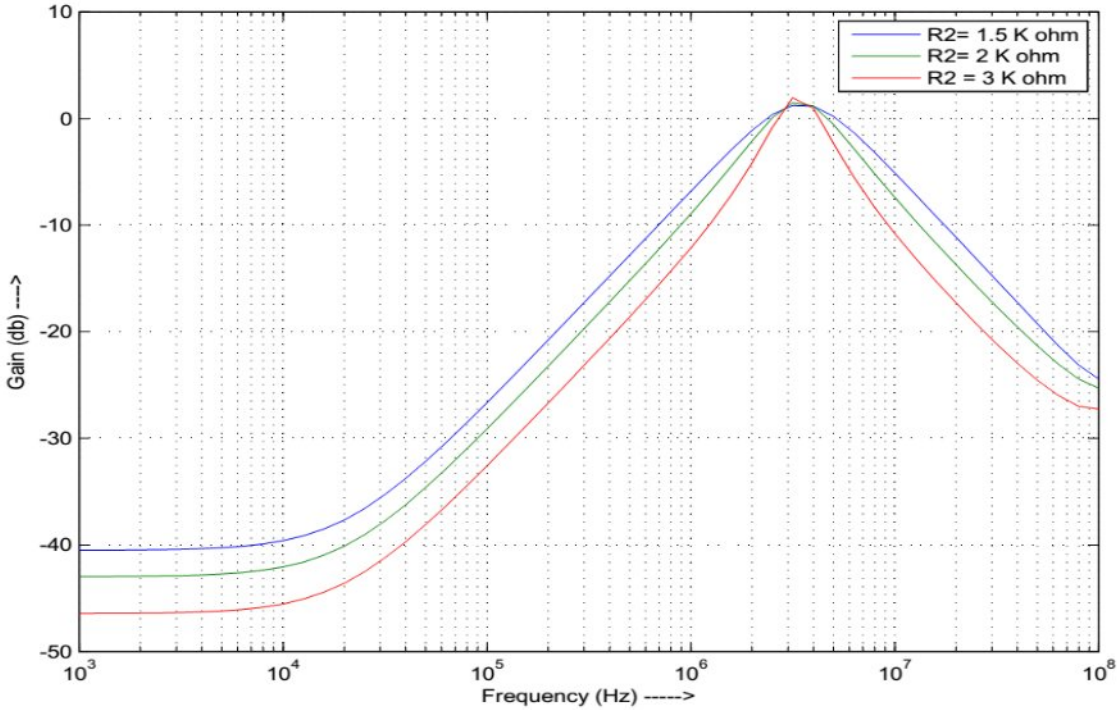


Fig. 4.8 Frequency response of BPF when BW is varied

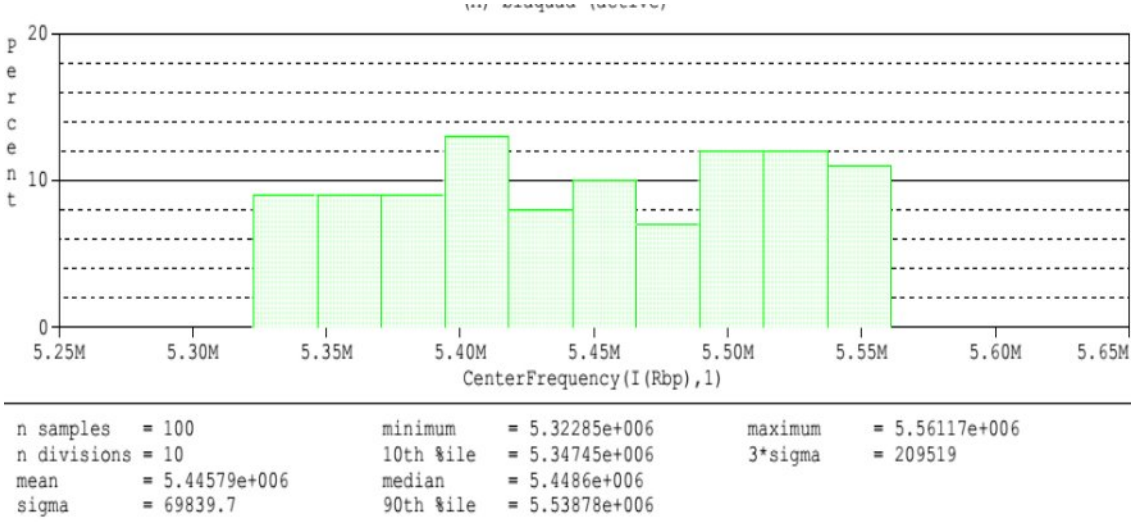


Fig. 4.9 Monte Carlo simulation of BPF

4.3 CONCLUSION

This chapter covers the basic theory of biquad filters and its types are such as Tow-Thomas and KHN-biquad. The VDCC based multifunction current mode biquad filter was proposed and simulated which verified the usability of VDCC in the analog signal processing among the novel active building blocks. Three type of current mode HPF, LPF and BPF outputs can be drawn using this proposed circuit. Using PSPICE simulation, the results of tunability of central frequency and bandwidth of band-pass filter (BFP) were noticed that they are independently to each other. Lastly, Monte-Carlo analysis was done for sensitivity analysis.

REFERENCES

[1] Schaumann, Van Valkenburg, “Design of Analog Filters”, Oxford University Press, 2004.

[2] Fırat Kacar, Abdullah Yesil, Shahram Minaei and Hakan Kuntman, “Positive/Negative Lossy/Lossless Grounded Inductance Simulators Employing Single VDCC and Only Two Passive Elements”, International Journal of Electronics and Communications (AEÜ), pp.73– 78, 2014.

[3] Ahmed M. Soliman, “ History and Progress of The TOW-THOMAS Biquad Filter Part II: OTRA, CCII and DVCC Realizations ”, Journal of Circuits, Systems, and Computers, Vol. 17, No. 5, 797–826, 2008.

[4] Bhopendra Singh, Abdhesh Kumar Singh, Raj Senani, “New Universal Current-Mode Biquad Using Only Three ZC-CFTAs”, Radioengineering, Vol. 21, No.1, 2012.

[5] Jetsdaporn Satansup, Worapong Tangsrirat, “Realization of Current-Mode KHN-Equivalent Biquad Filter Using ZC-CFTAs and Grounded Capacitors”, Indian Journal of Pure & Applied Physics, Vol. 49, pp. 841-866, 2011.

[6] Danupat Duangmalai, Aekkarat Noppakarn, Winai Jaikla,“Electronically Tunable Low-Component-Count Current-Mode Biquadratic Filter Using CFTAs”, International Conference on Information and Electronics Engineering, Vol.6, 2011.

[7] Muhammed A. Ibrahim, Shahram Minaei, Hakan Kuntman, “A 22.5 MHz Current-Mode KHN-Biquad Using Differential Voltage Current Conveyor and Grounded Passive Elements”, Int. J. Electron. Commun. (AEÜ), pp. 311 – 318, 2005.

[8] R. Senani, V.K.Singh, “ KHN-Equivalent Biquad Using Current Conveyors”, Electron Letters, Vol. 31, pp. 626-8, 1995.

[9] Shahram Minae, Muhamined A. Ibrahim and Hakan Kuntman, “A New Current-Mode KHN-Biquad Using Differential Voltage Current Conveyor Suitable for IF Stages”, IEEE, Vol.1,249-52, July 2003.

CHAPTER 5

CONCLUSION AND FUTURE SCOPE

CONCLUSION

Chapter 2 covers all the basic components namely differential pair, current mirror, active loads, translinear buffer and current conveyor which are used to design several active building blocks, are as. Current conveyor is the commonly used active block to derive others. Types of current conveyors are mainly CCI, CCII and CCIII. Some derivatives of current conveyor are discussed such as FDCCII, OFCC, CCCII, CFBCCII, UCC and DXCCII. In this chapter OTA has also been described. These active blocks are used to realize various analog signal processing applications such as filters, oscillator, amplifier etc.

In the chapter 3, a novel active building block namely the VDCC is discussed in detail. Its DC and AC characteristics of input-output were verified using PSPICE simulation. The basic signal processing applications such as adder, subtractor, differentiator, integrator and amplifier were designed using VDCC and simulated in PSPICE. The application of grounded inductance simulation was described and applied to design a high-pass filter. In yet another application, floating inductance was designed and simulated in PSPICE. The floating inductance was used to implement a band pass filter (BPF) with specified central frequency.

In chapter 4 a brief introduction of multifunction biquad filter design using the two-integrator in a loop methodology has been presented. Finally a novel single input multiple output type current mode multifunction filter using the voltage differencing current conveyor has been presented. The filter has high pass, band pass and low pass outputs in current mode. The filter employs two grounded capacitors. All the outputs are at high impedance nodes. The pole frequency and bandwidth of filter are

independently tunable. These filters have been simulated in PSPICE using 0.18 um CMOS technology. Sensitivity analysis using Monte-Carlo simulations have been presented.

SCOPE FOR FUTURE WORK

In the present work the application of VDCC for biquad filter application has been presented VDCC is a very versatile block as it combines the features of both OTA as well as CC. It can be used for realization of oscillators with different properties. There is scope for improvement in the basic structure of VDCC as well. Similarly filter circuits with electronically tunable parameters can also be realized with VDCC.

Thus there is enough scope for extension of the work presented in this dissertation.

APPENDICES

APPENDIX I

PSpice model file used for Process and electrical parameters CMOS 0.18 um from MOSIS Technology

```
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+VERSION = 3.1          TNOM    = 27          TOX     = 4.1E-9
+XJ     = 1E-7          NCH     = 2.3549E17   VTH0    = 0.354505
+K1     = 0.5733393     K2      = 3.177172E-3 K3      = 27.3563303
+K3B    = -10           W0      = 2.341477E-5 NLX     = 1.906617E-7
+DVT0W  = 0             DVT1W   = 0           DVT2W   = 0
+DVT0   = 1.6751718     DVT1    = 0.4282625   DVT2    = 0.036004
+U0     = 327.3736992   UA      = -4.52726E-11 UB     = 4.46532E-19
+UC     = -4.74051E-11  VSAT    = 8.785346E4  A0      = 1.6897405
+AGS    = 0.2908676     B0      = -8.224961E-9 B1     = -1E-7
+KETA   = 0.021238      A1      = 8.00349E-4  A2      = 1
+RDSW   = 105           PRWG    = 0.5         PRWB    = -0.2
+WR     = 1             WINT    = 0           LINT    = 1.351737E-8
*+XL    = -2E-8         XW      = -1E-8
+ DWG    = 1.610448E-9
+DWB    = -5.108595E-9  VOFF    = -0.0652968  NFACTOR = 2.4901845
+CIT    = 0             CDSC    = 2.4E-4      CDSCD   = 0
+CDSCB  = 0             ETA0    = 0.0231564   ETAB    = -0.058499
+DSUB   = 0.9467118     PCLM    = 0.8512348   PDIBLC1 = 0.0929526
+PDIBLC2 = 0.01         PDIBLCB = -0.1        DROUT   = 0.5224026
+PSCBE1  = 7.979323E10  PSCBE2  = 1.522921E-9 PVAG    = 0.01
+DELTA  = 0.01          RSH     = 6.8         MOBMOD  = 1
+PRT    = 0             UTE     = -1.5        KT1     = -0.11
+KT1L   = 0             KT2     = 0.022       UA1     = 4.31E-9
+UB1    = -7.61E-18     UC1     = -5.6E-11    AT      = 3.3E4
```

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+WWN    = 1           WWL     = 0           LL      = 0
+LLN    = 1           LW      = 0           LWN     = 1
+LWL    = 0           CAPMOD  = 2           XPART   = 0.5
+CGDO   = 7.7E-10     CGSO    = 7.7E-10     CGBO    = 1E-12
+CJ     = 1.010083E-3 PB      = 0.7344298   MJ      = 0.3565066
+CJSW   = 2.441707E-10 PBSW    = 0.8005503   MJSW    = 0.1327842
+CJSWG  = 3.3E-10     PBSWG   = 0.8005503   MJSWG   = 0.1327842
+CF     = 0           PVTH0   = 1.307195E-3 PRDSW   = -5
+PK2    = -1.022757E-3 WKETA  = -4.466285E-4 LKETA  = -9.715157E-3
+PU0    = 12.2704847  PUA     = 4.421816E-11 PUB    = 0
+PVSAT  = 1.707461E3  PETA0   = 1E-4        PKETA   = 2.348777E-3  )
*

.MODEL pmos_transistor PMOS ( LEVEL   = 7
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+XJ     = 1E-7        NCH     = 4.1589E17   VTH0    = -0.4120614
+K1     = 0.5590154   K2      = 0.0353896   K3      = 0
+K3B    = 7.3774572   W0      = 1E-6        NLX     = 1.103367E-7
+DVT0W  = 0           DVT1W   = 0           DVT2W   = 0
+DVT0   = 0.4301522   DVT1    = 0.2156888   DVT2    = 0.1
+U0     = 128.7704538 UA      = 1.908676E-9 UB      = 1.686179E-21
+UC     = -9.31329E-11 VSAT   = 1.658944E5  A0      = 1.6076505
+AGS    = 0.3740519   B0      = 1.711294E-6 B1      = 4.946873E-6
+KETA   = 0.0210951   A1      = 0.0244939   A2      = 1
+RDSW   = 127.0442882 PRWG    = 0.5         PRWB    = -0.5
+WR     = 1           WINT    = 5.428484E-10 LINT   = 2.468805E-8
*+XL    = -2E-8       XW      = -1E-8
+DWG    = -2.453074E-8
+DWB    = 6.408778E-9 VOFF    = -0.0974174  NFACTOR = 1.9740447
+CIT    = 0           CDSC    = 2.4E-4      CDSCD   = 0
+CDSCB  = 0           ETA0    = 0.1847491   ETAB    = -0.2531172
+DSUB   = 1.5         PCLM    = 4.8842961   PDIBLC1 = 0.0156227
+PDIBLC2 = 0.1        PDIBLCB = -1E-3       DROUT   = 0
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+PRT = 0 UTE = -1.5 KT1 = -0.11

+KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9

+UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4

+WL = 0 WLN = 1 WW = 0

+WWN = 1 WWL = 0 LL = 0

+LLN = 1 LW = 0 LWN = 1

+LWL = 0 CAPMOD = 2 XPART = 0.5

+CGDO = 7.11E-10 CGSO = 7.11E-10 CGBO = 1E-12

+CJ = 1.179334E-3 PB = 0.8545261 MJ = 0.4117753

+CJSW = 2.215877E-10 PBSW = 0.6162997 MJSW = 0.2678074

+CJSWG = 4.22E-10 PBSWG = 0.6162997 MJSWG = 0.2678074

+CF = 0 PVTH0 = 2.283319E-3 PRDSW = 5.6431992

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