INVESTIGATION OF DIFFERENT INTELLIGENT CONTROL ALGORITHM FOR D-STATCOM

DISSERTATION

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CERTIFICATE

I, **Anuj Varshney**, Roll No. 2K13/PSY/03 student of **M. Tech. (Power System)**, hereby declare that the dissertation titled **"Investigation of Different Intelligent control Algorithm for D-STATCOM"** under the supervision of **Dr. Rachana Garg,** Associate Professor, Department of Electrical Engineering, Delhi Technological University in partial fulfilment of the requirement for the award of the degree of Master of Technology has not been submitted elsewhere for the award of any Degree.

Place: Delhi **Anuj Varshney**

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ABSTRACT

The presence of harmonics in power supply network poses a severe power quality problem that results in huge power losses in distribution system, causes interference in the parallel running communication lines and, sometimes, operational failures of electronic equipment. DSTATCOM are employed to feed the required reactive power demand, suppress the current harmonics, minimize the unbalancing in the line currents and reduce the total harmonic distortion (THD) in the load. The voltage source converter (VSC) is the core of a DSTATCOM. The hysteresis current control is an indirect method of controlling the VSC. In this work, Synchronous Reference Frame (SRF) theory with Proportional-Integral controller, Conductance based Fryze Algorithm, Fuzzy logic control technique, different topologies of fuzzy logic controller and Adaptive Neuro-Fuzzy Inference system technique has been implemented for the generation of reference current signals for the controller. This work investigates the effectiveness of the proposed model in mitigation of harmonics currents, feed reactive power demanded by the load and reduce unbalancing due to the different loads in each phase by modelling a 3-φ three-wire D-STATCOM. Simulation results indicate that the proposed D-STATCOM can restrain the unwanted component of current from reaching to source effectively.

All topologies are tested for different loads (non-linear load and unbalanced linear load). Performance comparison between the PI controller, PI-like FLC, PI gain scheduled FLC, Hybrid FLC-PI controller and ANFIS controller are made in terms of several performance criteria such as peak overshoot, settling time (t_s) and rise time of the DC link voltage. Under all these topologies, THD of the grid side current is well within the IEEE standards and UPF at grid side is maintained.

Table of Contents

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATION

DC	Direct Current
AC	Alternating Current
VSC	Voltage Source Converter
PWM	Pulse Width Modulation
HCC	Hysteresis Current Controller
IGBT	Insulated Gate Bipolar Transistor
W	Watts
VAr	Reactive Volt Ampere
THD	Total Harmonic Distortions
PCC	Point of Common Coupling
PID	Proportional-Integral-Derivative
PLL	Phase Locked Loop
RMS	Root Mean Square
DVR	Dynamic Voltage Regulator
SVC	Static VAR Compensator
FC-TCR	Fixed Capacitor Thyristor Controlled Reactor
SSSC	Static Synchronous Series Compensator
TCSC	Thyristor Controlled Series Compensator
D-STATCOM	Distribution Static Compensator
ANFIS	Adaptive Neuro fuzzy Inference System
FLC	Fuzzy Logic Controller
SRFT	Synchronous Reference Frame Theory
CSC	Current Source Converter

CHAPTER 1
INTRODUCTION

1.1 Introduction

In present days, the increase in digital economy implies a distributed use of electronic equipment in each and every sectors (i.e. industrial, commercial and domestic). In literature various studies shows the data of the consumption share of electricity by the information and communication technology, and it has been concluded that nonresidential sector consumes 30-40% of annual electricity consumption. This shows greater demand of power and demand for high level of reliable quality power. The estimation suggests that the 30% power demand is from sensitive load equipment and continuously increasing day by day [1].

Now a days, number of factors decides the reliability of power supply, like non-linear loads, large switching loads and accidents can disrupt the electric power grid. The digital manufacturing assembly, information systems and our home appliances requires high grade of power [2]. The high power quality demand for electronic devices is due to the requirement of the semiconductor components which are highly sensitive to short power interruptions, low voltage direct current, require large amount of reactive power, sensitive to voltage surges/sags, current harmonics, and other waveform distortions [3].

Power system engineers and researchers are mostly concentrating on the idea of providing reliable, uninterrupted and high grade of power to the consumer. To achieve this, use of electronic equipment as a controller of power flow has been increased. Literature review in this area suggests different solutions for the problems related to high grade power and the idea of controlling different custom power devices using various evolutionary algorithms. Custom power devices include various FACTs devices like D-STATCOM, DVR, and UPQC etc [4].

This chapter highlights the power quality scenario in India, facts and figure related to different energy sources, installed capacity and contribution from renewable sources are provided. Problems due to distributed generation and problems due to different loads have been highlighted in this chapter. Various remedies to mitigate the power quality problems and how to increase the reliability and efficiency of the grid is explained in coming sections of this chapter.

1.2 Power Scenario in India

In India, the electricity sector has an installed capacity of 271.722 GW at the end of March 2015 [5]. Renewable power plants share 28% of total installed capacity and non-renewable energy plants shares the remaining 72%. India became the world's third largest manufacturer of electricity in 2013. During the year 2014-15, agriculture sector has recorded highest consumption of electricity. The per capita consumption suggests the standard of the society of the country and also its development. Despite the cheaper electricity tariff in India, the electricity per capita consumption in India is lower compared to many countries [6].

The demand of electricity in India is far more than can be met with the amount of installation at present. And as of alternative to the conventional energy sources, demand of renewable energy sources and different technologies to handle present load and to integrate new plants to the existing system has been increasing day by day. The integration of renewable energy based distribution generation will help in reduction of greenhouse gases and also help in meeting the demand of the country with cheaper form of electricity. But with the integration of the new technology to old power system, various technical problems arise in the area of power quality (i.e. voltage stability, harmonics, reliability, protection, and control) [7].

1.3 Power Quality

Power quality decides the wellness of electric energy to consumer loads. Synchronization of the voltage frequency and phase permits electrical systems to operate in their planned way without huge loss of performance. The term is utilized to depict electric power that drives an electrical burden and the load's capacity to work properly. Without the best possible power, an electrical load (or burden) may breakdown, fail to operate or not work at all. There are numerous causes in which electric power can be of low quality and numerous more reasons for such low quality power.

Now a days, integration of hundreds of generating plants and load center have made the power system circuit more complicated. The basic structure of typical power system is shown in Fig. 1.1. It shows a generating source, transmission line, sub transmission system and a distribution system [8, 9].

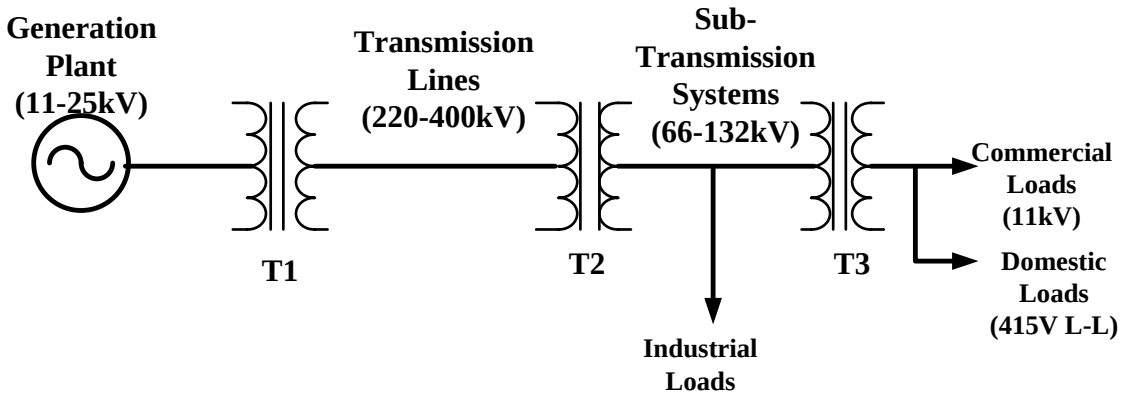


Fig. 1.1 Single line Diagram of a typical Power System

It can be seen from the Fig 1.1 that in between the generation and load point, various stages are there in power system. The correct operation of all the component is critical for reliable power system. There are many issues involved here such as the maintenance of power apparatus and system, the stability of the system, the operation of power distribution system, faults etc.

Few years back, consumers were mostly concerned about continuity of supply. Even though the generation is reliable, but distribution is not always so. Due to the exposure to the nature, the transmission systems also faces the problems (i.e. lightning, temperature etc.) [10]. But now a days, consumers wants continuity, with high grade of power. As there are various sensitive loads like hospital appliances, industries, air traffic control etc. connected to the same grid, and these all required uninterrupted clean power supply. Thus, in this changed scenario, where consumer is looking for high grade of power, 'Power Quality' term attains great significance. Literature suggests that power quality problems are distribution side problems but impact of transmission line problems is also significant on supply of high grade of power. Most of the transmission related problems arise due to the forces of nature or due to interconnection of grid, but individual consumer is mostly responsible for the distribution related problems [11].

1.4 Impact of Power Quality Problems on Consumer

Technically, the supply from utility should be pure sine wave of fundamental frequency (50/60 Hz) and the rated peak magnitude of the voltage wave. Unfortunately, the AC supply we receive from utility does not meet these specifications. Various problems associated to power quality, their characterization, methods and possible causes are listed [12] in Table 1.1.

Table 1.1 Power Quality problems and their causes

Broad categories	Specific categories	Methods of characterization	Typical causes
Transients	Impulsive	Peak magnitude, rise time and duration	Lightning strike, transformer energization and capacitor switching
	Oscillatory	Peak magnitude and frequency components	Line or capacitor or load switching
Short duration voltage variation	Sag	Magnitude and duration	Ferro resonant transformers, L-G faults
	Swell	Magnitude and duration	Ferro resonant X-mers, L-G faults
Long duration voltage variation	Under-voltage	Magnitude and duration	Switching on loads, capacitor de-energization
	Over-voltage	Magnitude and duration	Switching off loads, capacitor energization
Waveform distortion	Harmonic	THD, Harmonic spectrum	Adjustable speed drives and other nonlinear loads
	Notching	THD, Harmonic spectrum	Power electronic converters
	DC offset	Volts, Amps	Geo-magnetic disturbance, half wave rectification
Voltage flicker		Frequency of occurrence	Arc furnaces, arc lamps

The lack of quality power affects the customers in many ways. Impulsive transients do not travel too far but it can start an oscillatory transients which can cause transient overvoltage and damage the power line insulators. These are curbed using surge arresters.

Short duration voltage sags can cause loss of production in an automated industry by mal-operating or tripping a motor, computer systems or data processing systems can crash. Voltage swell can put stress on home appliances and computer systems, consequently shortening their lives.

The effect of long duration voltage variations is more than short duration voltage variations. Voltage unbalance can cause temperature rise in machines and can even cause a large machine to trip. Voltage waveform is distorted by Harmonics, notching and DC offset. Unnecessary losses is caused due to unwanted current harmonics flowing through distribution network. Also it can affect the operation of traffic control or any other lifesaving appliance in a hospital badly.

A periodic transient that rides on the supply voltage is called "Notch". It can damage shunt capacitor due to high rate of rise of voltage at the notches. It is therefore required to provide high grade of power to the consumer [13].

1.5 Power Quality Standards

Various standards for power quality have been proposed by Geneva based IEC (international electro-technical commission) and IEEE (Institute of electrical and electronic engineers).

In these standards, mainly IEEE-519 [14] is the mostly followed in various research and literature regarding power quality and its improvement, and to decide the limits for disturbances to the distribution system that affects other equipment and communication.

All type of power converters used in industries and commercial power systems produce harmonics and reactive power demand. Non-linear loads used in industry are made of static power converters, adjustable speed drives, UPS, arc discharge devices, and rotating machines. These devices are used in various conversions like ac to ac, dc to variable dc, dc to ac and vice-versa.

The sinusoidal nature of current waveform is altered by non-linear loads and therefore the ac voltage drop in the line, causing the flow of harmonic currents in ac power system, which produces interference with the communication lines and other neighboring equipment. The shunt capacitors used for improvement of the power factor, will start

resonating at some harmonic frequency with the nonlinear load, and this will cause high level of current distortion and harmonic voltage at PCC.

The harmonic distortion limits (recommended by IEEE-519 standards) establishes the maximum current distortion from a consumer.

TDD: Total Demand Distortion **(**TDD) gives the harmonic current distortion in percentage of maximum demand load current. And is an important index in defining the power quality. Table 1.2 lists all limits which should be used for designing a system for the worst case (conditions lasting longer than an hour). For shorter periods, during startups or unusual conditions, the limits may exceeded by 50%.

Table 1.2 Current distortion limits for General Distribution Systems

A / **B**						
I_{sc}/I_L	**<11**	**11<h<17**	**17<h<23**	**23<h<35**	**35<h**	**TDD**
<20	4.0	2.0	1.5	0.6	0.3	5.0
20<50	7.0	3.5	2.5	1.0	0.5	8.0

Where,

A = Maximum harmonic current distortion in % of I_L

B = Individual harmonic order (odd harmonics)

I_{sc} = maximum short circuit current at PCC,

I_L = maximum demand load current (fundamental frequency component) at PCC.

Even order harmonics are limited to $1/4^{th}$ of the odd harmonic limits listed in the table above. Distortions in currents due to DC offset, e.g. half wave converters, are not allowed The percentage of harmonic current injection from a consumer depends upon the load demand and the size of the system it is connected. As the size of the consumer demand decreases with respect to the size of the system, the percentage of harmonic current injection will rise. This protects the other users and the utility, which aims to maintain a certain quality of voltage to its customer.

1.6 Custom Power Devices

The application of power electronic converter at power distribution level for the benefit of consumer and utility is categorized under custom power devices [15]. Family of custom power devices can be broadly classified into:

- Shunt device (e.g. DSTATCOM, SVC and FC-TCR etc.)
- Series devices (e.g. Dynamic Voltage Regulator (DVR), SSSC, TCSC etc.)

- Hybrid devices (e.g. Unified Power Quality Conditioner (UPQC), Interline power flow controller (IPFC) etc.)

1.6.1 SHUNT DEVICES

Shunt devices are used to increase the limit for transmittable power and the voltage profile along the compensated line by controlling reactive power of the system. Various shunt devices have been suggested in literature (e.g. D-STATCOM, SVC, FC-TCR etc.). Shunt connected switched reactors are used to minimize overvoltage at load end during light load conditions and switched capacitors are used to maintain line voltage during heavy load conditions.

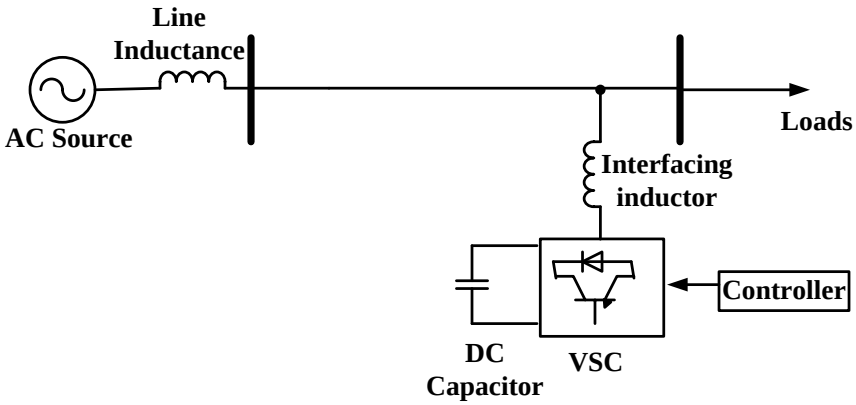


Fig 1.2 Single Line Diagram of DSTATCOM

The ideal single line diagram showing the connection of a D-STATCOM to an AC bus is shown in Fig 1.2. The use of D-STATCOM here is to maintain the PCC voltage magnitude constant irrespective of loads reactive power demand. Advancements in power electronics has produced fast switching devices using which a shunt connected device can be used to eliminate harmonics and at the same time can feed the required amount of reactive power to the system.

1.6.2 SERIES DEVICES

These devices are connected in the series with the line. It is used for compensation of supply voltage by regulating if there are problems on the supply side of the distribution system e.g. DVR, SSSC and TCSC etc. Desired voltage of required amplitude, phase and frequency is injected by DVR between grid and load. It is a very powerful device, which has the ability to mitigate the voltage swells and sags at the PCC. The difference between DVR and D-STATCOM is in the way they are connected to the system. DVR employs a transformer in series with the ac system.

Some functions of DVR are,

- Reactive Power Compensation
- Voltage Regulation
- Compensation for Voltage sags and Swells
- Unbalance Voltage Compensation (for 3-phase systems)

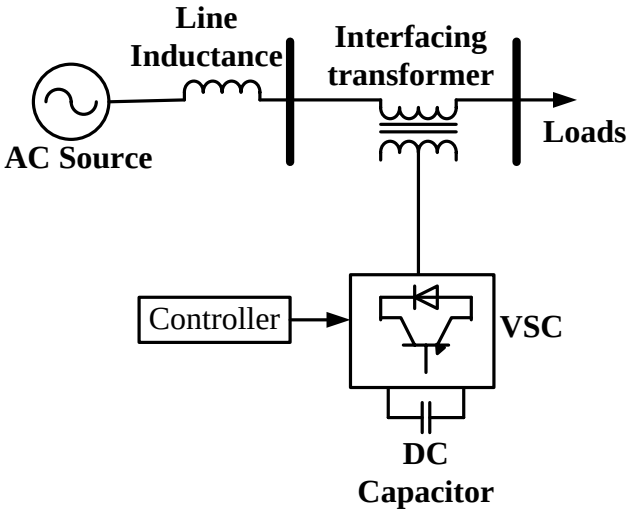


Fig 1.3 Single Line diagram of DVR connection to AC Line

1.6.3 HYBRID DEVICES

These type of devices are the combination of both series and shunt devices connected back to back. UPQC is a hybrid compensator having the capability to inject shunt currents and series voltage to the system. It consists of both series and shunt converters connected to the same DC link. It is a very powerful device which can mitigate both disturbances of current and voltage which may affect many sensitive loads. The basic structure of the UPQC is shown in Figure 1.4.

The UPQC has been used for real time control and dynamic compensation of AC transmission systems, providing multifunctional flexibility required to solve many of the problems faced by the power delivery industry. It can simultaneously or selectively control the flow of real and reactive power in the line.

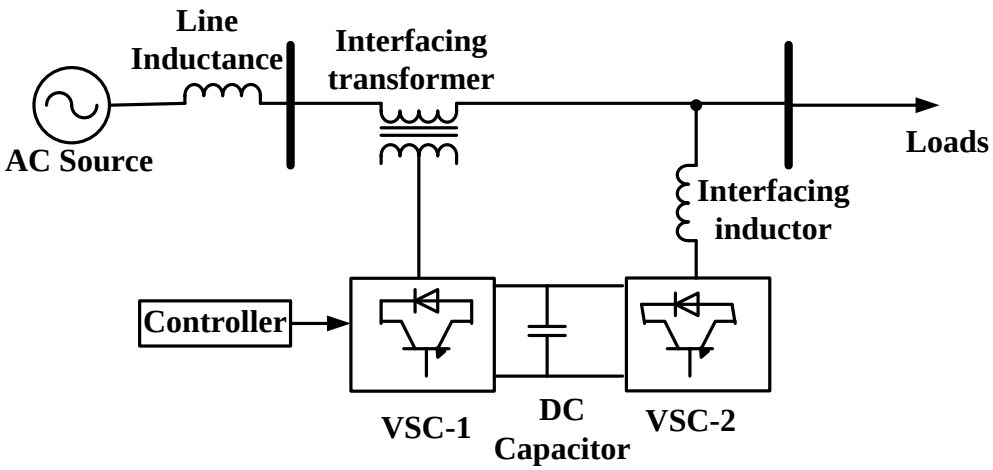


Fig 1.4 Single line diagram of Hybrid Compensator

In the present work, modelling and simulation of D-STATCOM is done with different types of intelligent controllers and various loads to analyze and compare the response of the D-STATCOM.

CHAPTER 2

LITERATURE REVIEW

2.1 GENERAL

In this chapter, many research papers and work related to D-STATCOM are reviewed. The review work is done for the areas given below,

- D-STATCOM Configuration
- SRFT and Fryze Algorithm
- FLC and different Topologies of PI-FLC
- ANFIS algorithm and control scheme

2.2 LITERATURE SURVEY

Arindam Ghosh and Gerard Ledwich [4] have characterized the various problems related to the distribution system and their effect on generation, transmission and neighboring loads. Also the remedies to diminish these effects using DSTATCOM and controlling of DSTATCOM using SRF theory have been explained.

A. Van Zyl et.al. [16] have shown power quality manager (PQM), a hybrid device comprising passive and active shunt filters. This topology has reduced the required rating of static VAR compensator, while reducing the harmonics and improving voltage regulation.

I. Wasiak et.al. [17] have shown the problems due to distributed energy resources and used DSTATCOM to compensate the various problems related to radial distribution system. DSTATCOM is controlled in both current controlled and voltage controlled mode to mitigate current and voltage related problems respectively.

Bhim singh et.al. [18] have simulated a stand-alone alternator feeding a three phase three wire distribution network. The DSTATCOM with three leg VSC is used to mitigate the power quality related problems and hysteresis rule base gating signals are produced to control the output of the DSTATCOM.

D. Nair et.al. [19] have explained the advantages of mitigating the power quality problems and used synchronous detection algorithm to control DSTATCOM for reactive power compensation and harmonic elimination.

P. Jayapraksh et.al. [20] have proposed H-Bridge topology for VSC instead of conventional four leg converter for three phase four wire distribution network, decreasing

the number of switches, while compensating the reactive power, elimination of harmonics, balancing load and neutral current compensation at point of common coupling (PCC).

G.O. Suvire et.al. [21] have shown the wind energy generation and its advantages and disadvantages on grid. The inclusion of renewable source generates number of power quality problems so DSTACOM is used to minimize those effects.

C. Kumar et.al. [22] have proposed the state space model of DSTATCOM with dead beat predictive controller for fast load voltage regulation during voltage disturbance. This proposed scheme is effective in eliminating the harmonics and power factor correction.

D.P. Kothari et.al. [23] have proposed a T-connected transformer and three leg VSC based DSTATCOM for power quality improvement. Here two single phase transformers are connected in T-configuration for interfacing three phase four wire distribution system with three leg VSC.

T.R. Somayajulu et.al. [24] have proposed a three leg VSC based DSTATCOM integrated with a zig-zag transformer for compensation of reactive power and elimination of harmonics at PCC.

J. Ramesh et.al. [25] have shown the effect of load variation on grid and mitigated those effects using DSTATCOM. The controlling of DSTATCOM is done using instantaneous symmetrical component theory, DC link voltage is maintained at set point value using conventional controller (PI).

G. Sahu and K. Mahapatra [26] have shown comparison of different reference current generation schemes viz. instantaneous p-q theory, synchronous reference frame theory (SRF), Modified SRF Theory, instantaneous symmetrical component theory and Average unit power factor theory to control DSTATCOM for different loads.

R. Sharma et.al. [27] have shown the control algorithm for DSTATCOM based on Synchronous Reference Frame Theory (SRFT), used to extract the reference source currents for load balancing, power factor correction and harmonic elimination at PCC.

R. Niwas and B. Singh [28] have proposed a distribution system with source of isolated diesel engine driven induction generator and mitigated the problems related to power quality using DSTATCOM, interfaced with a T-connected Transformer to the three phase four wire distribution system.

S. Bhowmick et.al. [29] have shown the modelling and control of DSTATCOM and battery energy storage system (BESS). DSTACOM is used to compensate for wide variety of loads.

B. Singh et.al. [30] have shown DSTACOM built with three single phase inverters interfaced to three phase four wire distribution system using three single phase inverters. This topology has the advantages of the use of "of the shelf" H-Bridge VSCs and optimum voltage ratings of VSCs.

P. Kumar [31] has shown the compensation for linear and nonlinear loads connected to a distribution system. The reference currents are derived using SRFT for reactive power compensation, harmonic elimination and load balancing.

J. Solanki et.al. [32] have shown three different reference current generation theory viz. instantaneous reactive power theory, synchronous reference frame theory and Adaline based algorithm, used to control DSTATCOM for linear and nonlinear loads.

A. Banerji et.al. [33] have shown an autonomous grid along with a DSTATCOM and battery energy storage system for rural locations, while harnessing the renewable energy available at these locations. DSTATCOM is used to enhance the stability of the grid and maintaining the power quality to optimum.

Karuppanan P. and **K. K. Mahapatra** [34] have presented shunt active filter for improving the power quality such as harmonics compensation and reactive power compensation because of non-linear loads. A novel compensation control scheme, generalized Fryze currents minimization based on positive sequence voltage detector is implemented and it is able to compensate harmonics and reactive power.

C.N. Rowe, T.J. Summers, R.E. Betz and **D. Cornforth** [35] presented on control scheme to control power flow in a standalone micro-grid, which is Power frequency droop method. This paper compares the effect of instantaneous and Fryze power calculations on the operation of a three phase, two inverter micro-grid.

Mauricio Aredes and **Luis F. C. Monteiro** [36] described a novel control strategy i.e. the sinusoidal Fryze current control strategy based on minimization method equations, together with a robust synchronizing circuit (PLL circuit) for shunt active filters.

Alexandru Bitoleanu and **Mihaela Popescu** [37] presented paper on the Reference Current Methods Calculation and their Implementation for the shunt filters. Many control schemes have been described such as the Fryze's theory, the theory of Fryze-Buchholz-Depenbrock, the so-called generalized theory of instantaneous reactive and non-active powers, the Currents' Physical Components Theory (CPC) and the Conservative Power Theory (CPT).

H. Suryanarayana et.al. [38] have shown the variation in DC link voltage due to load variation and its effect on compensation. At the time of transient, Fuzzy logic controller is

used to supervise the proportional and integral gains of conventional control to maintain DC link voltage and for fast settling of the system.

M. Labeeb et.al. [39] have proposed ANN based fuzzy logic controller to compensate reactive power, eliminate harmonics and load balancing is accomplished using DSTACOM.

R. Prajapati et.al. [40] have proposed a fuzzy logic controller based on Takagi-Sugeno inference system to control DC link voltage of DSTATCOM for eliminate harmonics and control reactive power in three phase three wire distribution system.

Ji Liu et.al. [41] have shown fuzzy PI control of DSTATCOM to maintain the DC link voltage constant. DSTATCOM is shunt connected at PCC to improve power factor and eliminate harmonics from the current.

P.P. Shimmeer et.al. [42] have proposed a hybrid topology of DSTATCOM and zigzag transformer. Also an enhanced PLL (EPLL) is used to generate reference source current even under polluted utility voltage. DC link voltage is maintained using fuzzy logic controller.

P. Nijhawan et.al. [43] have shown the effect of induction furnace load on neighboring loads and on system. DSTATCOM is used to compensate the harmonics produced from induction furnace operation and reactive power requirement of the loads.

Jan Jantzen [44] has proposed tuning of fuzzy PID controllers. This paper has shown various fuzzy PID control techniques and their implementation for error minimization in various plant processes. Also gives idea about tuning of PID controller using Ziegler Nichols technique.

Z. W. Woo et.al. [45] have proposed a PID type fuzzy controller with self-tuning scaling factors. This has improved the transient state and steady state performance of PID type controller. The scaling factors for PID type Fuzzy controllers are tuned on line.

W.Z. Qiao et.al. [46] have shown a PID type Fuzzy controller with on line tuning of scaling factors, and also incorporating a parameter adaptive method to improve the performance of the controller at transient and steady state time of the process.

Yanan Zhao et.al. [47] have proposed the control of industrial weigh belt feeder using a Fuzzy PI controller. In this paper fuzzy PID controllers are categorized in two parts; one category consists typical fuzzy logic controllers, while second category consists the combination of both PID and fuzzy controllers, named as ‘Fuzzy PID controllers’.

Amit V. Sant et.al. [48] have proposed a hybrid Fuzzy-PI control scheme with different weights assigned to the outputs of the two controllers. The paper presents the idea of stiff fuzzy control at transient time and stiff PID control at steady state time of the process.

R.K. Mudi et.al. [49] have shown the self-tuning PI type Fuzzy logic controller. The proposed self-tuning controller is designed using a very simple rule base and the most natural and unbiased membership functions (MFs) i.e. symmetric triangles with equal base and 50% overlap with neighboring MFs.

K.A. Gopala Rao et.al. [50] have presented the comparison of the fuzzy PI controller with fuzzy PID and conventional PID controllers.

T.B. Kumar et.al. [51] have presented the pros and cons of wind energy generation on grid and different sensitive loads connected to it. The mitigation of these harmful effects have been done using STATCOM and STATCOM is controlled using artificial neuro fuzzy inference scheme (ANFIS).

S. Farid Torabi et.al. [52] have shown the effects of low frequency oscillations on the power system, and STATCOM is used as a dynamic regulator to eliminate these oscillations. STATCOM is controlled using two intelligent control schemes fuzzy logic controller and ANFIS controller.

D. Nazarpour et.al. [53] have studied the effects of sub synchronous resonance on generation and sensitive loads. These effects are eliminated using STATCOM, while controlling of STATCOM is done using Fuzzy logic controller and ANFIS controller, and results from these two controllers are compared.

In this chapter, a brief literature review related to the different topics of D-STATCOM configuration and its controllers have been presented.

CHAPTER 3

MODELLING AND DESIGN OF D-STATCOM

It is a shunt connected FACT device, having same configuration as of STATCOM (Static compensator). The STATCOM is a voltage source converter supplied by a DC capacitor. The converter consists of six IGBT switches with anti-parallel diodes which are switched on and off through a gate drive circuit. The D-STATCOM is used at PCC of the system to counterbalance the loads demand of unwanted component i.e. harmonic current components, reactive power demand, load balancing etc. Voltage regulation can also be achieved using D-STATCOM. In voltage control mode it can regulate the bus voltage constant and balanced against any kind of disturbance from supply side or load side. To counterbalance the unbalance or distortions in the load current or the supply voltage, DSTATCOM feeds equal and opposite unbalanced and harmonically distorted current or voltage to PCC.

There are two modes of operation of DSTATCOM:

- Load compensation in current control mode
- Voltage regulation in voltage control mode

In the load compensation mode, DSTATCOM is used to counteract the unwanted components due to the load current demand. To achieve this goal, current control mode is used to design the controller for DSTATCOM. This controller has to generate reference currents so that the DSTATCOM can compensate reactive current demand, harmonics and unbalancing due to load supply currents. DSTATCOM rating for the load compensation depends on reactive power, harmonic distortion and power requirement of the load to be compensated.

Voltage regulation mode of DSTATCOM uses voltage control mode. It means that controller has to generate reference voltages to compensate harmonics from voltage waveform and to feed reactive power to eliminate voltage sag and swell at PCC.

In the present work, D-STATCOM is used in load compensation mode.

3.1 Load compensation using D-STATCOM

The single line diagram of a distribution system compensated by an ideal shunt compensator (DSTATCOM) is shown in Fig. 3.1.

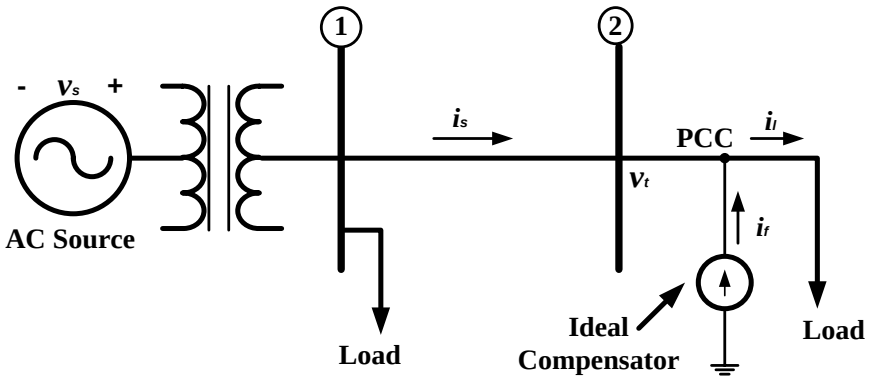


Fig. 3.1 Single line diagram of ideal load compensation

It can be seen from the Fig 3.1 that DSTATCOM is working in current control mode. And it is denoted by an ideal current source (i_f). It is assumed that load right to PCC is mixed i.e. reactive, non-linear and unbalanced. And in absence of the compensator the source current (i_s) will also be distorted and lagging in nature, consequently the bus-1 & 2 voltage will be distorted.

To make the source current fundamental and positive sequence only, the compensator has to feed the required amount of reactive, unbalance and harmonic compensating current to the PCC. This will cause the source current (i_s) to be in phase to the PCC voltage (v_t). Therefore, from utility side, it will look like a unity power factor load connected to PCC drawing harmonic free and balanced current from the grid.

The point at which the compensator is connected is called the utility-customer point of common coupling (PCC). The KCL at the PCC yields,

$$i_s + i_f = i_l \quad \Longleftrightarrow \quad i_s = i_l - i_f \qquad \ldots (3.1)$$

Where, i_l denotes the load current demand.

i_f is the current generated by the compensator to counteract the reactive component, harmonic component and unbalance of the load current at PCC.

Consider a three phase three wire distribution network with an ideal shunt compensator shown in Fig 3.2. The 3-φ source with grounded star point is connected to 3-φ load (nonlinear, unbalanced and reactive in nature). At the point of common coupling the ideal three phase shunt compensator is feeding to all the unwanted components of the load current.

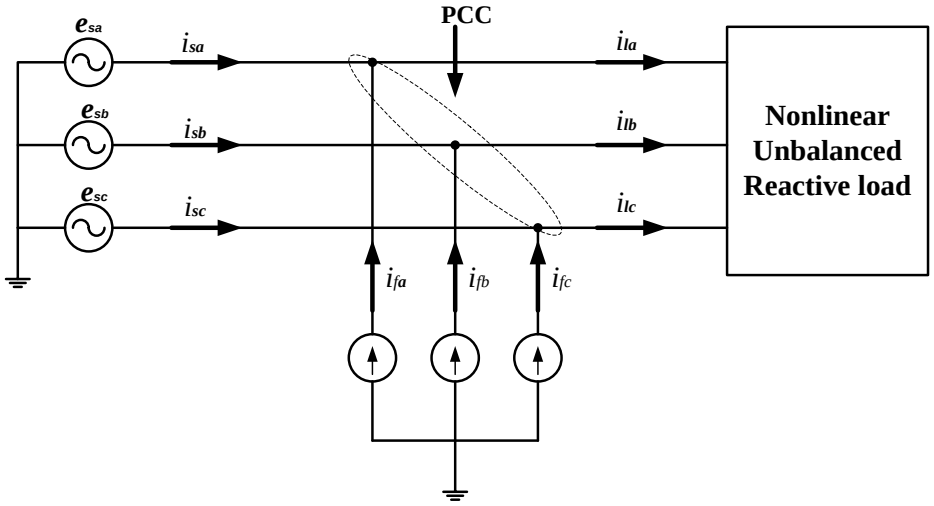


Fig 3.2 Schematic diagram of a 3-φ ideal shunt compensator connected to 3-φ three wire distribution system

.All the voltages and currents shown in the diagram are instantaneous quantities. Because the load currents may change frequently, and extracting the component to be compensated will be real time quantities. To extract the reference quantities various current segregation techniques have been suggested in literature such as synchronous reference frame theory (SRFT), instantaneous reactive power theory (IRPT), fryze current minimization algorithm etc.

The basic configuration of DSTATCOM consists of a voltage source converter and a DC capacitor at its DC terminals. Fig 3.3 (a) shows this configuration of DSTATCOM using VSC. The converter should have high switching frequency so that it can reproduce the compensating currents accurately. Normally,

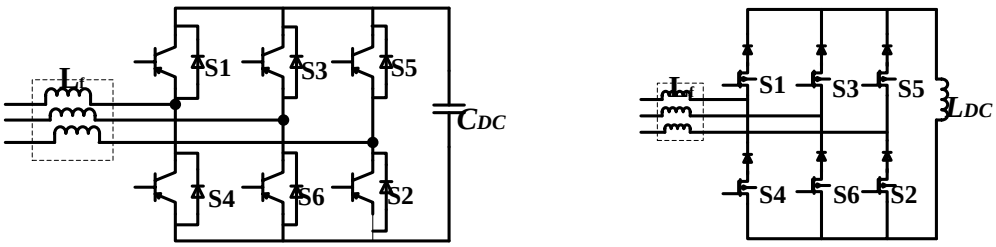
$$f_{PWM} > 10 * f_{hmax} \quad \ldots (3.2)$$

Where, f_{PWM} is the switching frequency of the converter,

f_{hmax} is the frequency of the highest order harmonic current to be compensated.

Another method of realizing shunt active filter is by using current source converter. In VSC the DC side source is a capacitor, while in case of current source converter it is an inductor. It is to be noticed here that no power supply element is used at DC side of the converter because the principal function of the DSTATCOM is to behave as a compensator i.e. ideally, the average energy exchange between the DSTATCOM and the power system should be equal to zero.

A voltage source converter having six IGBTs with antiparallel diodes connected to them is shown in Fig 3.3(a) and in Fig 3.3(b) a current source converter is shown



(a) Voltage Source Converter

(b) Current Source Converter

Fig 3.3 (a) Voltage source converter, (b) Current Source converter

The comparison of VSC and CSC is tabulated in Table 3.1

Table 3.1 Comparison of VSC and CSC

Voltage source converter	**Current source converter**
1. high efficiency	1. robust in nature
2. low initial cost	2. series connection of IGBT and diode (for reverse blocking)
3. smaller physical size	3. complicated device design and fabrication
4. due to anti-parallel diode no need for reverse voltage blocking in IGBTs	4. slightly worse device characteristics than conventional IGBTs

3.1.1 Operation modes of D-STATCOM

D-STATCOM can work in four modes,

A. Active power generator,

B. Active Power absorber,

C. Inductive mode or reactive power absorber,

D. Capacitive mode or reactive power generator.

Fig 3.4 shows the vector diagrams for all four modes of operation of D-STATCOM. It can be seen that the relation of voltage generated by the D-STATCOM and voltage at PCC will decide the mode of operation of D-STATCOM. The magnitude of the VSC terminal voltage will decide the flow of reactive power, and the angle between the VSC voltage and the PCC voltage will decide the flow of active power in either direction.

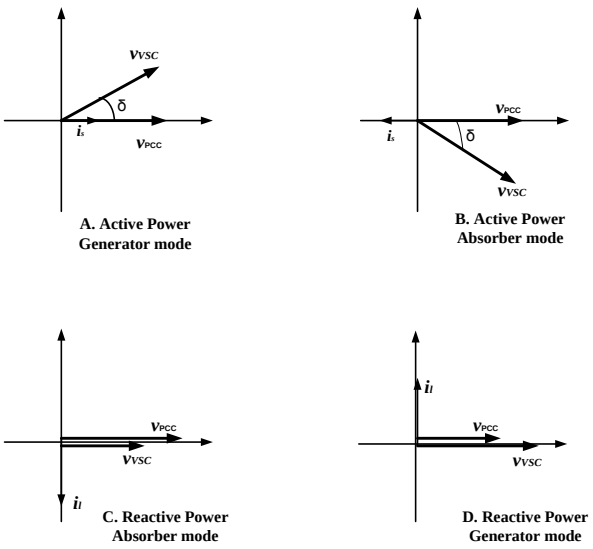


Fig 3.4 Different Modes of Operation of D-STATCOM

Where, v_{pcc} is the instantaneous voltage at the point of common coupling. v_{vsc} is the instantaneous voltage generated by the ideal D-STATCOM, i_l is the instantaneous line current from system to load.

3.2 Proposed System

A three phase AC distribution system of 415V (line to line), 50Hz frequency is taken as power circuit to be studied under this project. Unbalanced linear loads (Star connected) and non-linear loads are connected to the system. The D-STATCOM is connected to the system in shunt at the point of common coupling with an interfacing inductor (L_f). The proposed system diagram is shown in Fig 3.5. The D-STATCOM in this project is used to eliminate harmonics produced due to non-linear load connected to the system, reactive power demand of the loads and to minimize the unbalancing due to unbalanced nature of the loads. The control of D-STATCOM to compensate all unwanted component is done using SRF-theory with a conventional PI controller to maintain DC link voltage.

3.2.1 Design of D-STATCOM [54]

Three leg VSC is used to design D-STATCOM, voltage source converter is having six IGBTs with anti-parallel diodes connected in a bridge formation. The ratings of IGBTs used are 2500kV and 1500A [55]. The selection and calculation for DC bus voltage to be maintained across the VSC, DC capacitor rating to maintain this voltage across the VSC terminals, interfacing inductor rating, and design of ripple filter is done as follows,

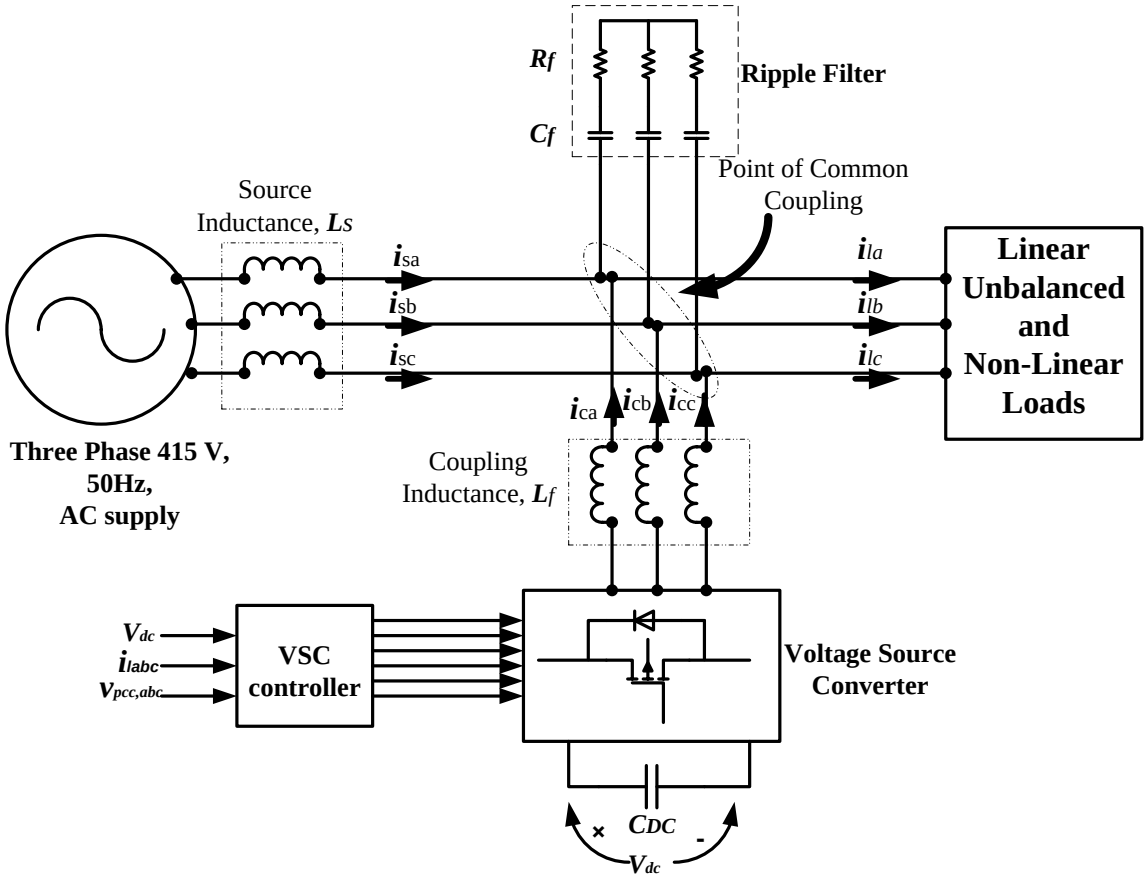


Fig 3.5 Schematic diagram for shunt connected DSTACOM to an AC Three phase three wire distribution system

i. DC Bus Voltage

The instantaneous energy fed to the D-STATCOM decides the DC terminal voltage magnitude. For a three leg VSC with a DC capacitor, the capacitor voltage is given by eqn. (3.3),

$$V_{dc} = 2\sqrt{2} * \frac{v_{ac}}{\sqrt{3}*m} \quad \ldots (3.3)$$

Where, m is the modulation index and taken as 1, and v_{ac} is AC terminal voltage of D-STATCOM and is equal to 415 V (RMS line to line). With these values the calculated value of V_{dc} is 677.61V. The selected magnitude of dc terminal voltage is 750V in this project.

The principle of generating instantaneous active power and reactive powers by D-STATCOM is shown in Fig 3.6 using phasor diagram,

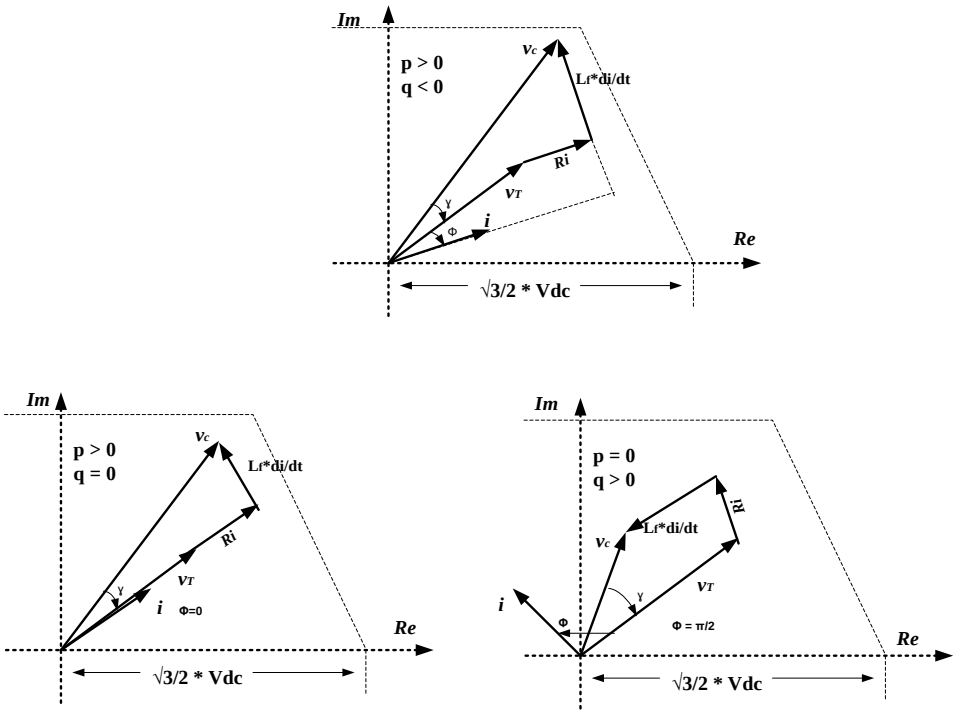


Fig 3.6 Principle of operation of D-STATCOM instantaneous active power and reactive power

It can be understood from the above figure that by generating a suitable AC voltage it is possible to produce arbitrary instantaneous vectors of both active and reactive power. The real component of currents is linked to the equivalent series resistance modelling losses on AC side. DSTATCOM can generate or absorb limited amount of active and reactive power. Circuit parameters and maximum ratings of VSC components are the reason behind this limitation. In Fig 3.6 a cautionary limit for AC voltage can be seen, it depends on VSC's DC side voltage (V_{dc}). The operating region of DSTATCOM is defined by the limits of filter inductance (L_f) and terminal voltage (v_T). To increase this limit the DC terminal voltage is chosen more than the calculated value. Also VSC is a boost type converter i.e. in order to guarantee the controllability of the Hysteresis current control, the DC side voltage should be kept more than the peak value of the AC bus voltage.

ii. DC Bus Capacitor Rating

The principle of energy conservation is given by eqn. (3.4),

$$\frac{1}{2}C_{dc}[(V_{dc})^2 - (V_{dc1})^2] = 3V_{ac}(\alpha I)t \quad \ldots (3.4)$$

Where V_{dc} is the reference DC voltage, v_{ac} is the phase voltage (240 V_{rms}), V_{dc1} is the minimum voltage level of DC bus, I is the phase current, α is the overloading factor, and t is time up to when the DC voltage is to be recovered.

Considering 5% voltage ripple in the DC bus and taking the values of the quantities as V_{dc1} =740V, V_{dc} =750V, V_{ac} =240V, I = 55.64A, t = 350μsec and α =1.2, the calculated value of C_{dc} is 2254 μF and is selected as 2500 μF.

In order to compensate for harmonic content of the current, the DC capacitor should be made large enough to behave as an energy storage element. So that it won't experience large voltage variations i.e. if DC voltage gets lower than the AC system's peak voltage, the VSC loses its inherent property of boost type converter and consequently loss of controllable compensation will not be achieved.

iii. Coupling Inductance (L_f)

The calculation of the coupling inductance (L_f) for VSC depends on the current ripple Δi, DC bus voltage (V_{dc} =750V) and switching frequency fs =10 kHz, and L_f is given by eqn. (3.5),

$$L_f = \frac{\sqrt{3} * m * V_{dc}}{12 * h * f_s * \Delta i} \quad \ldots (3.5)$$

Where, Δi =5% of 55.64(=I), h (=1.2) is overload factor and m (=1) is modulating index. The calculated value of L_f is 3.24 mH and L_f = 3.5 mH is taken in this investigation.

The interfacing inductor is equivalent representation of the leakage reactance offered due to the transformer connected in between the AC system and the DSTATCOM. The transformer is connected to decrease the rating of the DSTATCOM to be used and to decrease the switching ripples at PCC.

iv. Ripple Filter

The switching of the VSC causes noise in PCC voltages. To remove those noises from the voltage waveform, a first order high pass filter is tuned at half of the switching frequency and the connection of the filter at PCC can be seen in Fig 3.5. A combination of capacitor and resistance in series connected to each phase is selected as a ripple filter with common ground point. The ratings of filter capacitance and resistance are taken as 5μF and 6.2 Ω respectively. This combination offers high impedance(636.65 Ω) at fundamental frequency and low impendence (8.88 Ω) at half of the switching frequency (here 5kHz) which forbids the flow of fundamental components at fundamental frequency in the filter branch and permits the flow of high frequency noises through the filter branch at higher than fundamental frequency.

The switching pulses for the VSC are generated using SRFT, Fryze current minimization Algorithm, Fuzzy logic controllers and ANFIS based controller. These switching schemes are explained in coming sections of the thesis.

3.3 Synchronous Reference Frame Theory (SRFT)

In this thesis, the SRFT-based indirect control technique [56] is used to generate gate pulses for controlling of D-STATCOM. The block diagram representation of control technique based on SRF theory is shown in Fig 3.7. As grid is supposed to feed only active power to load at PCC, but due to loads reactive or unbalanced or nonlinear nature, unwanted components flow in the line like reactive power, harmonic currents etc. but with the D-STATCOM connected in line, these unwanted components can be fed at PCC directly using DC capacitor connected VSC in shunt. As control technique is indirect in nature so the currents from load end are sensed and using Park's transformation, the 3-φ load currents (i_{labc}) are converted to *d-q-0* frame [57].

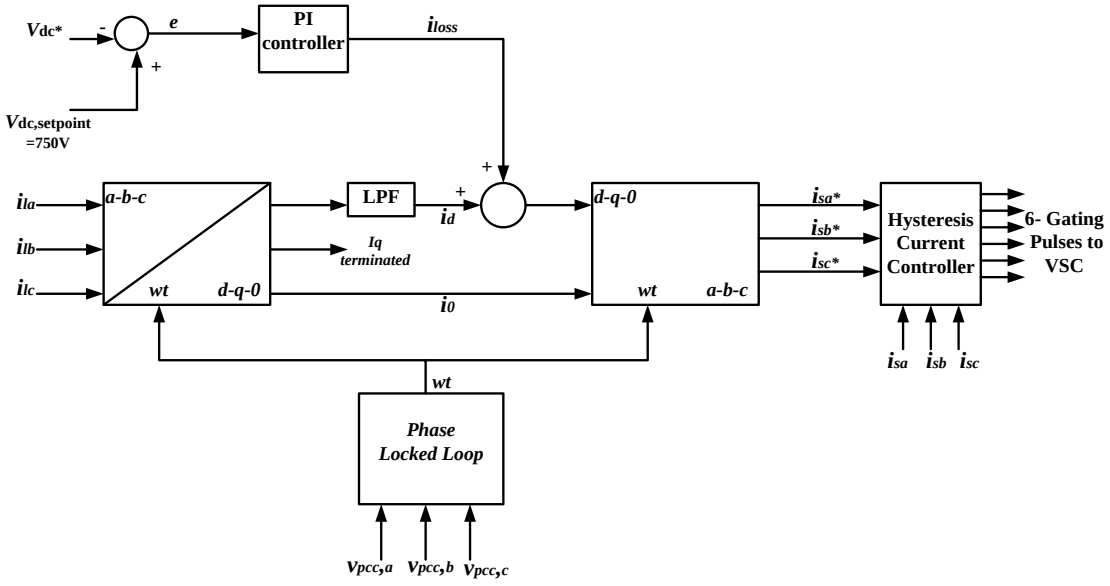


Fig 3.7 DSTATCOM Control Scheme Based on SRFT

Firstly, the current components in *α–β-0* co-ordinates are generated. '*a-b-c'* phasors can then be transformed into *α–β-0* coordinates using Clark's transformation as given by eqn. (3.6),

$$\begin{bmatrix} i_\alpha \\ i_\beta \\ i_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} i_{la} \\ i_{lb} \\ i_{lc} \end{bmatrix} \quad \ldots (3.6)$$

Then using ωt as the transformation angle, these currents can be transformed from *α–β-0* to *d–q-0* frame using eqn. (3.7) (Park's transformation),

$$\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \begin{bmatrix} \sin\omega t & -\cos\omega t & 0 \\ \cos\omega t & \sin\omega t & 0 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \\ i_0 \end{bmatrix} \quad \dots (3.7)$$

It can be seen that the load's active power requirement and the power required to maintain constant DC voltage at VSC's DC terminals is to be fulfilled by the grid and therefore these two are added. To maintain DC voltage constant, the error between reference signal and sensed DC voltage is fed into a PI controller [12], thus generating an output current (i_{loss}) equal to the loss in DC voltage and i_{loss} is given by eqn. (3.8),

$$i_{loss(n)} = i_{loss(n-1)} + k_p\left(V_{de(n)} - V_{de(n-1)}\right) + k_i * V_{de(n)} \quad \dots (3.8)$$

Where, $V_{de(n)}$ is error in DC terminal voltage signal and reference DC voltage of 750V at nth instant and given by eqn. (3.9),

$$V_{de(n)} = V_{dc}^{*} - V_{dc(n)} \quad \dots (3.9)$$

and the direct component (i_d) of current from *d-q-0* transformation is then selected and filtered using a 2nd order Butterworth filter to eliminate unwanted signals ($\tilde{\imath}$).

Therefore the total active power comprised in the grid current can be given by eqn. (3.10),

$$i_{active}^{*} = i_{dc} + i_{loss} \quad \dots (3.10)$$

To eliminate unbalancing due to the load current, the zero component is calculated from the *a-b-c* to *d-q-0* transformation and fed to the controller as shown in the block, as to eliminate the zero sequence components extra active power is needed, and this extra amount of power to be delivered from the grid.

A 3-φ PLL is used to synchronize these signals with the voltages at PCC. The angle ωt of park's transformation in eqn. (3.7 & 3.11) is the synchronous angular position determined by the PLL. The resultant currents in the *d-q-0* reference frame (i_d*=i_{active}*, i_q*=0, i_0*) are reverse transformed into reference source current (i_{sa}*, i_{sb}*, i_{sc}*) in *a-b-c* frame.

To obtain, three phase reference source current, is also a two-step process and is given by eqn. (3.11 & 3.12),

$$\begin{bmatrix} i_\alpha^{*} \\ i_\beta^{*} \\ i_0^{*} \end{bmatrix} = \begin{bmatrix} \sin\omega t & \cos\omega t & 0 \\ -\cos\omega t & \sin\omega t & 0 \\ 1 & 1 & 1 \end{bmatrix} * \begin{bmatrix} i_d^{*} \\ i_q^{*} \\ i_0^{*} \end{bmatrix} \quad \text{(Reverse Clark's transformation)} \dots (3.11)$$

$$\begin{bmatrix} i_{sa}^* \\ i_{sb}^* \\ i_{sc}^* \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 \\ \frac{-1}{2} & \frac{\sqrt{3}}{2} & 1 \\ \frac{-1}{2} & \frac{-\sqrt{3}}{2} & 1 \end{bmatrix} * \begin{bmatrix} i_{\alpha}^* \\ i_{\beta}^* \\ i_0^* \end{bmatrix} \quad \text{(Reverse Park's Transformation)} \quad \ldots (3.12)$$

These reference source currents, calculated from eqn. (3.12) are fed to hysteresis current controller (HCC) along with instantaneous source currents, thus generating switching signal for Voltage Source Converter (VSC).

3.3.1 Phase Locked Loop [58]

The schematic diagram of the Three-phase Phase locked loop is shown in Fig 3.8. This PLL is used in controlling the DSTATCOM. PLL generates ωt angle varying between 0 and 2π, and synchronized to zero crossing of the fundamental of phase A.

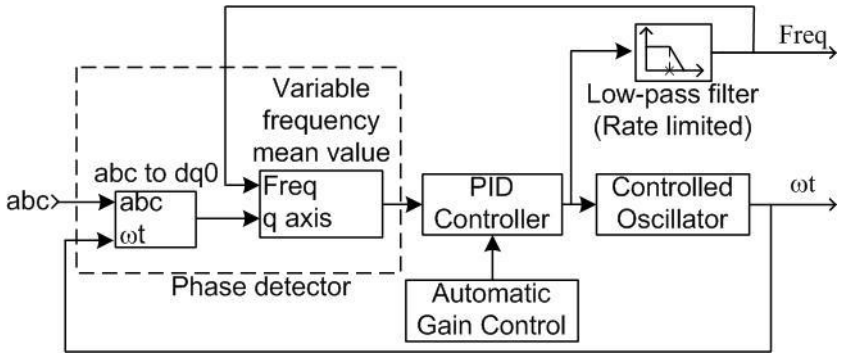


Fig 3.8 Schematic Diagram of 3-φ PLL

The 3-φ input signal to the PLL is transformed to the *d-q-0* rotating frame, the angular speed required for this conversion is provided by an internal oscillator. Then *q*-axis component of transformed signal, which is proportional to the phase difference between the *a-b-c* signal and the internal oscillator rotating frame, is filtered with a mean (variable frequency) block. The output of this block is fed to a PID controller having an optional automatic gain control (AGC), it keeps the phase differences to 0 by acting on a controlled oscillator. The PID output, corresponding to the angular velocity, is filtered and converted to frequency in Hz and output of the controlled oscillator is the angle (ωt) varying between 0 & 2π rad.

3.3.2 Hysteresis Current Controller

Gating pulses for a converter are generated using synchronized pulse width modulation (PWM) method or most famous and most used asynchronized hysteresis current control method [59]. Hysteresis current controller is used because of its simplicity in implementation and fast response with peak current limiting capability. But hysteresis current control scheme suffers with the disadvantage of wide variation in switching

frequency, which may be prohibitively high, and can cause higher losses of the converter switches due to increased number of switching per cycle.

The two level scheme is simplest in implementation, requiring the value of tracking error alone, which is the difference between the references (i_{sa}*, i_{sb}*, i_{sc}*) and the actual values (i_{sa}, i_{sb}, i_{sc}) of the grid side current.

In this method switching is done in an asynchronous way to ramp the actual current up and down so that it will follow the reference current. When the source current is exceeding the upper hysteresis limit, it turns on a negative voltage switching function and causes the source current to decrease. And if the current violates the lower hysteresis limit, then it turns on a positive voltage switching function to increase the source current. The hysteresis band limit used in this investigation is 0.2. The tracking of the actual current wave using a hysteresis current controller is shown in Fig 3.9

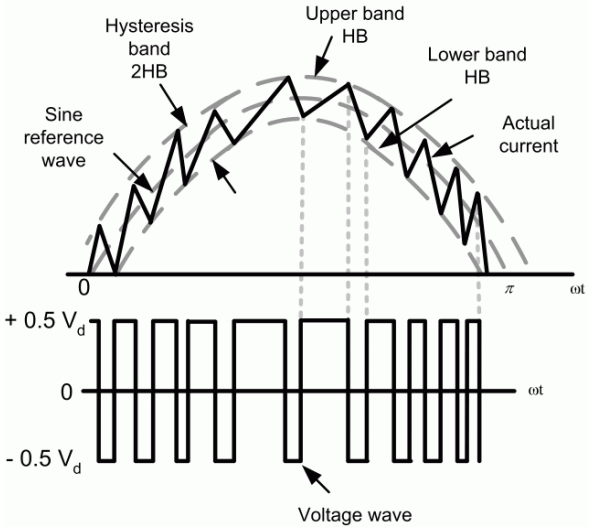


Fig 3.9 Hysteresis current control

The internal architecture of hysteresis current controller is shown in Fig 3.10. the six pulses are generated for six IGBT switches in VSC, as each phase is connected to two switches, the output pulses also contains one pulse for upper switch and one pulse for lower switch.

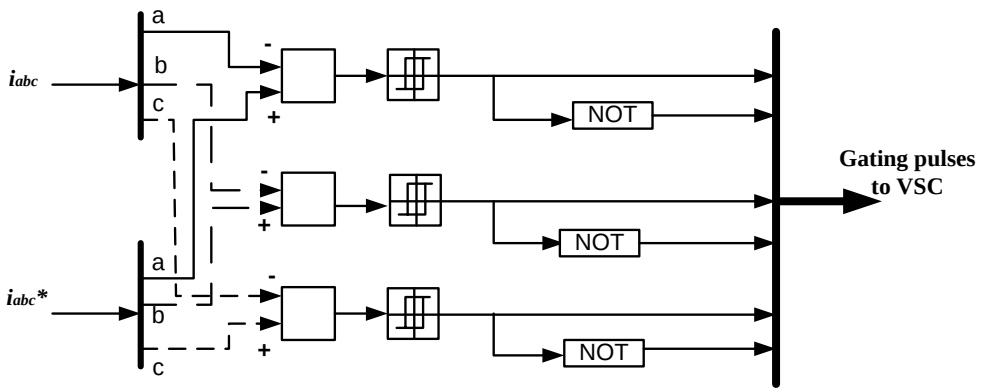


Fig 3.10 Schematic Diagram of Hysteresis Current Controller

3.4 Conductance based Fryze algorithm [35-37]

This theory is directly defined in a-b-c phases, i.e. use of instantaneous phase voltages and line currents. In this theory active component of the current and non-active component (reactive, harmonic and unbalance) of current are calculated. The instantaneous non-active current is the component of load current which does not contribute to the active power, although it enhances the current magnitude and losses in the system. The instantaneous non-active current can be find out using a minimization method. Let i_k is the load current (where k= a, b, c), it consist of an active current component i_{wk} and non-active component i_{qk} i.e,

$$i_k = i_{wk} + i_{qk} \quad \ldots (3.13)$$

The instantaneous non-active currents are given by eqn. (3.14),

$$\begin{bmatrix} i_{qa} \\ i_{qb} \\ i_{qc} \end{bmatrix} = \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} - \frac{(v_a * i_a + v_b * i_b + v_c * i_c)}{v_a^2 + v_b^2 + v_c^2} * \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad \ldots (3.14)$$

And instantaneous active current are given by eqn. (3.15),

$$\begin{bmatrix} i_{wa} \\ i_{wb} \\ i_{wc} \end{bmatrix} = \frac{(v_a * i_a + v_b * i_b + v_c * i_c)}{v_a^2 + v_b^2 + v_c^2} * \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad \ldots (3.15)$$

The active currents determined in equation (3.15) are affected by zero sequence components in the voltages and currents. The non-active components calculated above can be compensated using shunt compensator at the load end so that only active component has to be fed through the grid and this decreases the losses in the system.

The instantaneous active power is given by eqn. (3.16)

$$p_{3\emptyset} = (v_a * i_a + v_b * i_b + v_c * i_c) \quad \ldots (3.16)$$

The conductance calculated from the eqn. (3.15) is given by eqn. (3.17),

$$G_e = \frac{(v_a * i_a + v_b * i_b + v_c * i_c)}{v_a^2 + v_b^2 + v_c^2} \quad \ldots (3.17)$$

In case of distorted or unbalanced source voltages, the generalized Fryze currents minimization method is employed. The basic idea behind this method is to determine the minimized currents from the average value of the three phase instantaneous active power ($\overline{p_{3\emptyset}}$). In order to calculate average value for the equivalent conductivity ($i=G_e*v$), the instantaneous sum of squared phase voltages have also to be replaced by a sum of the squared RMS values of the voltages. This increases the complexity and also the time required to calculate RMS and average value increases. To avoid this, a low pass filter can be used to determine average admittance ($\overline{G_e}$), which is defined by eqn. (3.18),

$$\overline{G_e} = \frac{1}{T} * \int_0^T \left(\frac{v_a i_a + v_b i_b + v_c i_c}{v_a^2 + v_b^2 + v_c^2} \right) dt \quad \ldots (3.18)$$

This approach can be used to design controller for DSTATCOM. Fig 3.11 shows the schematic diagram to control DSTATCOM. The instantaneous equivalent conductance (G_e) is calculated using three phase instantaneous active power ($p_{3\varphi}$) and the sum of squared instantaneous phase voltage. The average conductance ($\overline{G_e}$) is obtained, passing equivalent conductance (G_e) through a low pass filter. In order to compensate for the switching losses in VSC a small amount of power is to be drawn from the supply otherwise the DC side capacitor will feed those losses and start discharging. To compensate, a PI controller is used to generate loss average conductance ($\overline{G_{loss}}$), which is added to the average conductance($\overline{G_e}$). Then the active reference currents are calculated as given by the eqn. (3.19)

$$\begin{bmatrix} \overline{i_{wa}} \\ \overline{i_{wb}} \\ \overline{i_{wc}} \end{bmatrix} = (\overline{G_e} + \overline{G_{loss}}) * \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad \ldots (3.19)$$

These reference currents are then fed to Hysteresis current controller with the instantaneous source currents to generate the gating pulses for voltage source converter.

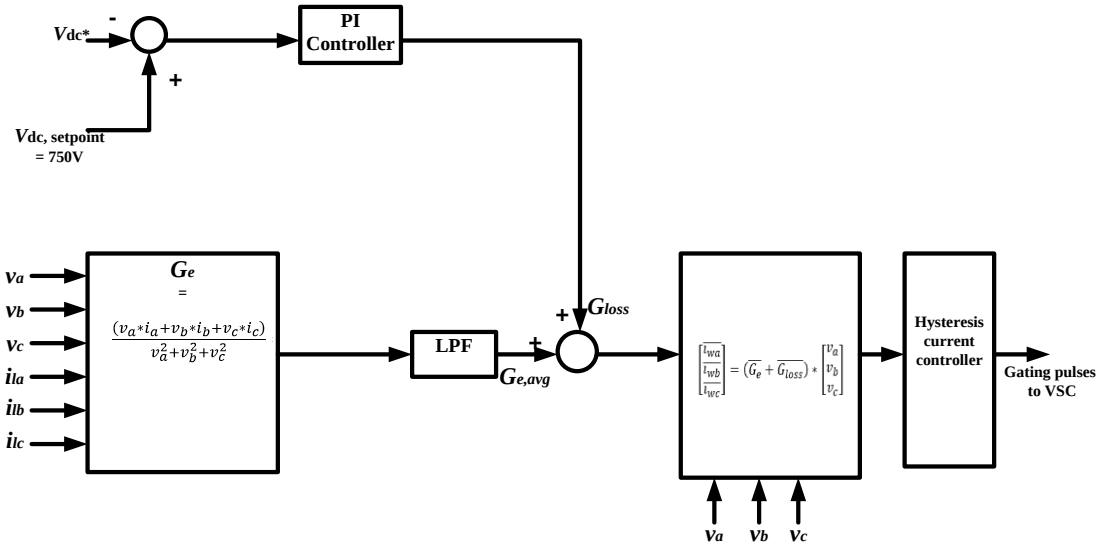


Fig 3.11 Control scheme for DSTATCOM using conductance based Fryze algorithm

In SRFT the real and imaginary part of the currents and voltages can be separated. Same goes with the Fryze algorithm, the active and non-active parts of the load currents can be separated from each other using this method. Although SRFT requires more calculation then Fryze algorithm. But SRFT is more efficient in dealing with the zero sequence components of the load currents and also different things like harmonics or reactive power component or zero sequence component of currents can be separated out and compensation of any of these can be carried out easily, which is not the case in Fryze algorithm.

In this chapter the working of ideal compensator, designing of D-STATCOM and generation of gating pulses using SRF theory and conductance based Fryze algorithm is explained. Also the components of proposed system are designed.

CHAPTER 4

DIFFERENT TOPOLOGIES OF FUZZY LOGIC CONTROLLERS FOR D-STATCOM

In conventional control of D-STATCOM, PID controller is used to maintain DC link voltage constant. But in the present work intelligent controllers such as Fuzzy logic controllers and its different topologies, ANFIS based controller, are designed to replace PID controller as these intelligent controller provide better transient response.

Fuzzy logic is a tool for transforming linguistically expressed knowledge into workable algorithm called a fuzzy logic model. Fig 4.1 shows the basic configuration of a fuzzy logic controller, which consists four principle components: a data control rule base, a decision making unit, an input fuzzification interface, and an output de-fuzzification interface. The rule base has a set of IF-THEN rules that expresses the knowledge that has been amassed about DSTATCOM controlling. It acts as a resource to the decision making logic, which makes successive decisions about which rules are most relevant to the current situation, and performs the actions suggested by these rules. The input fuzzifier takes the crisp numeric inputs and, as its name implies, fuzzify them as asked by the decision making logic. At the output, the de-fuzzification interface combines the results reached by the decision making logic and reverts them into crisp numeric values as required by control actions.

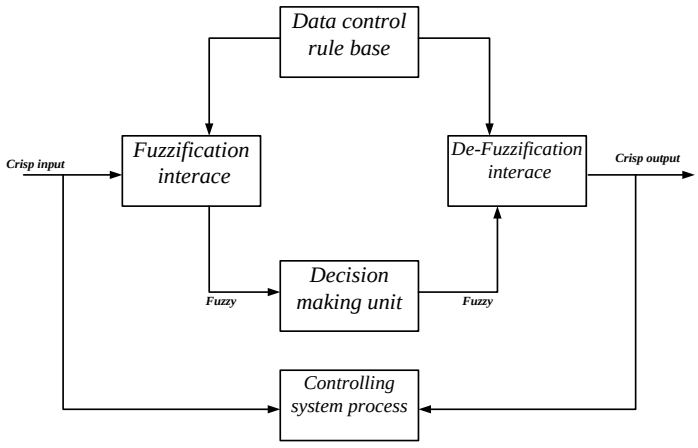


Fig 4.1 Simple fuzzy logic control system block diagram

For unknown or difficult system model and for their controller, Fuzzy logic controller has been found especially useful. It does not need an exact process model, and does not require any mathematical model. It is based on the simple linguistic rules obtained from the experience of the system operator. FLCs have been shown to be efficient with respect to

large uncertainties, disturbances, and transients in the process behavior. Under steady state conditions, Conventional PI controller has shown better performance then compared to FLC. The advantages of both fuzzy and PI controllers can be incorporated using FLC and PI controller in combination of series/parallel connection. Fuzzy-PI control has been widely studied and various types of Fuzzy-PI controllers has been proposed in literature. According to their construction, it can be classified into two major categories [60-62].

First category is PI-like Fuzzy controllers, consists of a typical FLC, a set of heuristic control rules are used to construct it. The input signal is constructed as a nonlinear function of the error (e) and change of error (Δe), where fuzzy reasoning is used for nonlinear function deduction. No proportional (k_p) and integral gains (k_i) are connected to the FLC. The control signal is directly derived from the knowledge base and fuzzy inference. This controller is called PI-like Fuzzy controller as its structure match up to the conventional PI controllers.

Second category is designed using the conventional PI controller in alignment with a FLC, and fuzzy output is used to tune the PI gains on line. To tune this Fuzzy-PI controller, it requires the ultimate gain (k_u) and the ultimate time period (T_u) of the system. Thus designing of this type of controllers requires more experimental experience with the system. In addition to these two category, there is this third category of Hybrid Fuzzy-PI controller in which under transient conditions, the output of the fuzzy logic controller is more than the PI controller output and under steady state conditions the output conditions switches to PI more and fuzzy less [63-65].

4.1 PI-like Fuzzy Logic Controller

In this section, the design of PI-like FLC to control the DSTATCOM operation is shown in the block diagram as shown in Fig 4.2. This PI-like FLC system has two normalized inputs, error and change of error, which are given by eqn. (4.1) & (4.2),

$$e = V_{dc,set} - V_{dc}^{*} \quad \ldots (4.1)$$

And, $$\Delta e = e(n) - e(n-1) \quad \ldots (4.2)$$

Where $V_{dc,set}$ and V_{dc}* are the applied set point input (750V) and DC terminal measured voltage across DSTATCOM. The output of the FLC is i_{loss} corresponds to differential energy (Δe_{dc}) needed for a self-supporting DC bus voltage for the DSTATCOM and to feed the losses in VSC power circuit [66]. The component i_{loss} is given by eqn. (4.3) and differential DC energy (Δe_{dc}) by eqn. (4.4),

$$i_{loss} = \frac{2}{3} * \frac{\Delta e_{dc}}{V_{sm} * T_x} \quad \ldots (4.3)$$

$$\Delta e_{dc} = e^*_{dc} - e_{dc} = \frac{1}{2} * C_{dc} * \left[\left(V_{dc,set}\right)^2 - (V^*_{dc})^2 \right] \quad \ldots (4.4)$$

And V_{sm} is the voltage magnitude of the system and T_x is the one sixth of the time constant of the supply voltage and given by eqn. (4.5),

$$T_x = \frac{1}{6} * T_s = \frac{1}{6} * \frac{1}{f_s} \quad \ldots (4.5)$$

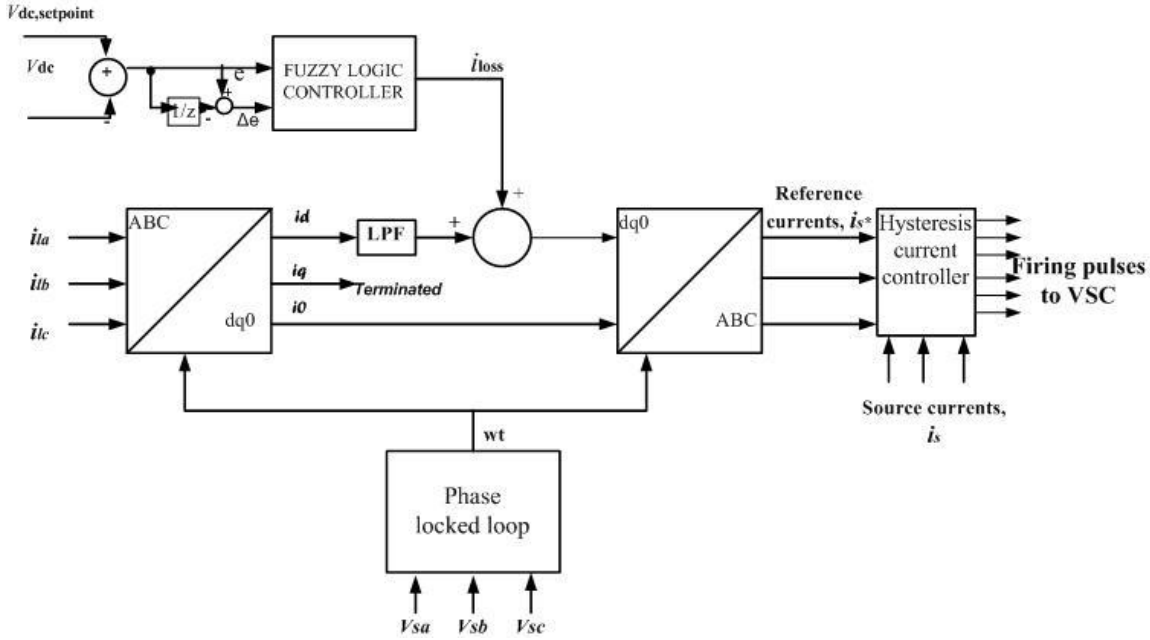


Fig 4.2 Schematic Diagram of Fuzzy Logic based control scheme for DSTATCOM

All MFs for the FLC inputs and the output are distributed in the range of [-1, 1], having a shape of symmetric triangles. These triangular membership functions overlap each other as shown in Fig 4.3. The MFs are denoted as NB, NM, NS, ZE, PS, PM and PB, which stands for Negative Big, Negative Medium, Negative Small, Zero, Positive Small, Positive Medium, Positive Big, respectively.

The two dimensional rule base, to compute $i_{loss,}$ the DC energy loss current component, is shown in Table. 4.1[67]. The control rules are based on the characteristics of the response as if the V_{dc} is moving far away from the set point, a large output current is required to pull it towards the set point, whereas a small output current is required when V_{dc} is close to the set point.

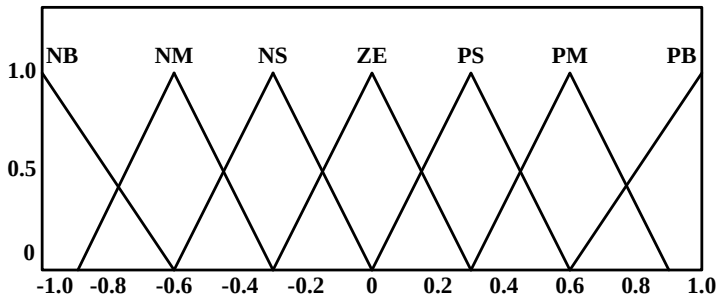


Fig 4.3 Membership functions of *e, ⊿e* and i_{loss}

Table. 4.1 FLCs rule base for computation of i_{loss}

⊿E / E	*nb*	*nm*	*ns*	*ze*	*PS*	*PM*	*PB*
NB	NB	NB	NM	NM	NS	NS	NS
NM	NM	NM	NS	NS	NS	ZE	ZE
NS	NM	NS	NS	NS	ZE	ZE	ZE
ZE	NS	NS	ZE	ZE	ZE	PS	PS
PS	ZE	ZE	PS	PS	PS	PM	PM
PM	ZE	ZE	PS	PS	PM	PM	PM
PB	PS	PS	PS	PM	PM	PB	PB

In the process of designing PI-like FLCs, once the membership functions (MFs) and rule bases are constructed, the scaling factors are tuned. Studies have been done to see the effect of scaling factors over closed loop system and their tuning procedure. The scaling factors required for normalization of inputs and de-normalization of output plays important role for controller stability and performance as in a conventional controller, as they are the source of possible instability, oscillations, and decayed damping effects [68]. The relationship between the scaling factors K_e, $K_{\Delta e}$ and K_{iloss} and the input output variables of the FLC are given by eqn. (4.6),

$$e_N = K_e * e \ ; \Delta e_N = \ K_{\Delta e} * \Delta e \ ; i_{loss,N} = K_{iloss} * \ i_{loss} \quad \ldots (4.6)$$

The expert knowledge of the system controller gives the idea to select suitable values of scaling factors, and also through trial and error these can be found out.

4.2 PI Gain Scheduling using FLC

PI-like FLC controller may result in steady state errors because the system does not have an inherent integrator to minimize this error. In this configuration both fuzzy logic controller and PI controller are used to incorporate the advantages of both the controllers into one system. In literature, some other controller configuration of fuzzy-PI controller

has also been used in which the tuning of gains (K_p & K_i) have been done using the FLC [69].

Here FLC is used to control the proportional gain (K_p) and integral gain (K_i) output based on the input error and change of error as shown in Fig 4.4. These output gains controls the PI-controller, which is tuned firstly based on Ziegler Nichols tuning method [70]. Here the initial values of the gain parameters are modified on line using fuzzy rules defined on *e and Δe*. The eqn. (4.7) shows the relationship of loss current required and the gains.

$$i_{loss} = u * \left[k_p + \frac{k_i * T_s}{z-1}\right] \quad \ldots (4.7)$$

For gain scheduling of PI controller, all MFs of the FLC are defined on the common normalized domain [-1, 1] and symmetric distribution of triangular MFs with 50% overlap is shown in Fig 4.5. The MFs are denoted as NB, NS, ZE, PS and PB which stands for negative big, negative small, zero, positive small and positive big respectively.

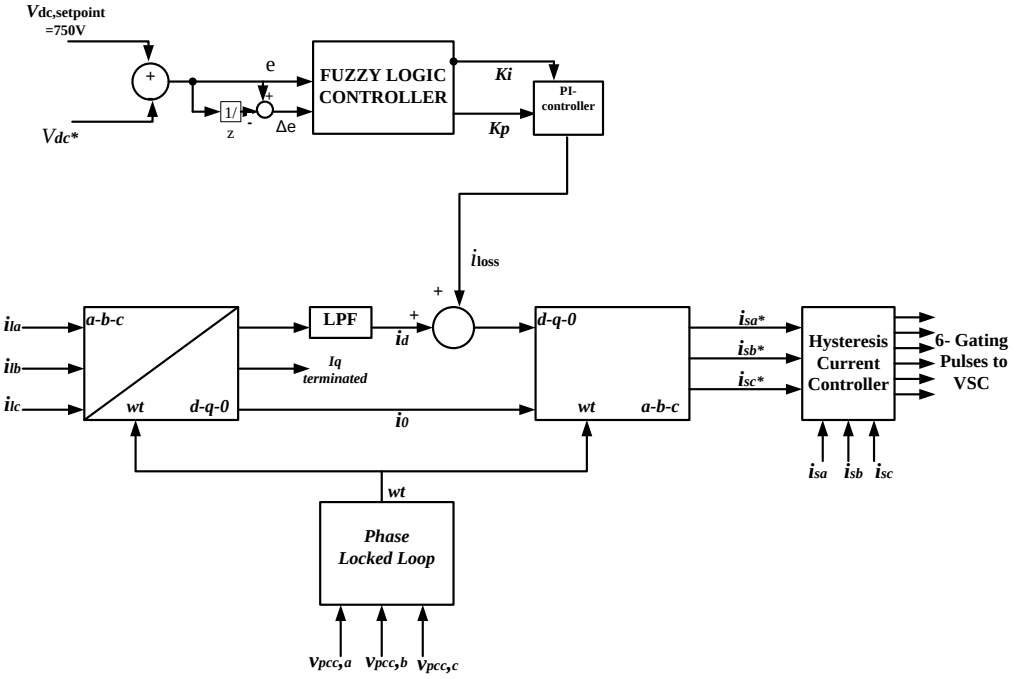


Fig 4.4 Schematic Diagram of PI gain Scheduled FLC

The control rules are based on the characteristics of the response as if the V_{dc} is deviating far away from the set point, a large output current is required to pull it towards the set point, whereas a small current is required when V_{dc} is near and moving towards the set point. The rule base is shown in Table. 4.2

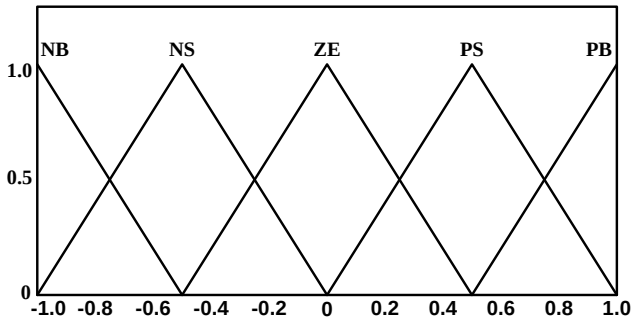


Fig 4.5 Membership function *e*, *Δe* and i_{loss}

Table. 4.2 FLCs rule base for computation of K_p and K_i

Δe / **e**	**NB**	**NS**	**ZE**	**PS**	**PB**
NB	NB	NB	NS	NS	ZE
NS	NB	NS	NS	ZE	PS
ZE	NS	NS	ZE	PS	PS
PS	NS	ZE	PS	PS	PB
PB	ZE	PS	PS	PB	PB

4.3 Hybrid Fuzzy-PI Controller

In this configuration a hybrid model of FLC and PI is developed in which the output of FLC and PI controller is added to produce the DC loss component of current (i_{loss}). The performance of Fuzzy logic controller, as compared to conventional PI controller is superior under transient conditions. The advantages of FLC and PI controller are obtained by implementing a Hybrid Fuzzy-PI controller for DC terminal voltage control. In literature Hybrid fuzzy-PI controller is used for the control of induction motor by activating the PI controller at the steady state conditions and FLC when transient and oscillations are detected [71]. The schematic block diagram of Hybrid Fuzzy-PI controller for DSTATCOM is shown in the Fig 4.6.

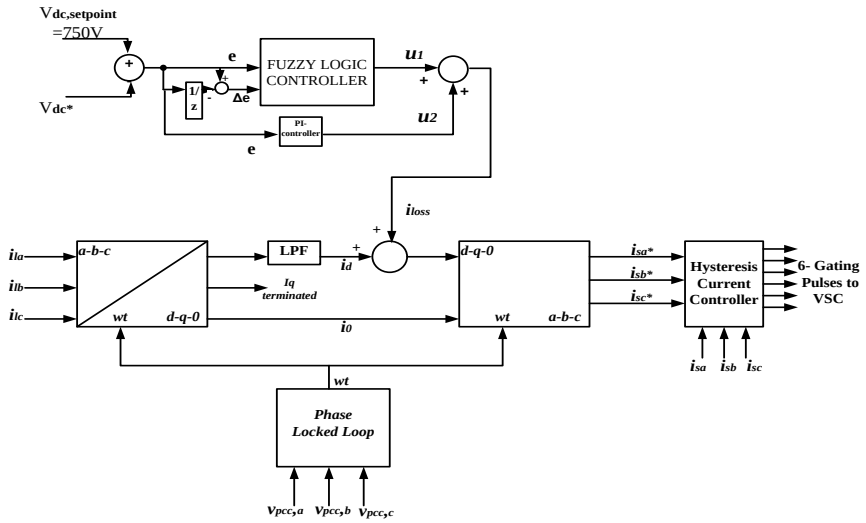


Fig 4.6 Schematic Diagram of Hybrid Fuzzy-PI controller

The error (e) and change (Δe) in error are the two inputs used to produce FLC output, while error only is fed to PI-controller to produce the output .both the outputs are added to produce the loss component of current (i_{loss}) to regulate the DC terminal voltage, this loss is added to the active component of current (i_d) calculated from the load current (i_l) which is transformed using the Park's Transformation.

The controlling rule base and the membership function design remains same as explained in section 4.1.

In this chapter the advantages of replacing PID controller with the Fuzzy logic controller has been shown. And different topologies of the FLC are explained with their rule-base and MFs architecture.

CHAPTER 5

ANFIS control scheme for DSTATCOM

In this chapter ANFIS (Adaptive neuro-fuzzy inference system) [72] a newly developed class of hybrid intelligent controller is presented. ANFIS uses fuzzy reasoning mechanism which is implemented using adaptive network framework. Human knowledge and input-output data pairs can be used to build input-output mapping using ANFIS tool.

By contrast, fuzzy IF-THEN rules can be employed using fuzzy reasoning, which models the human knowledge and reasoning processes. Takagi and Sugeno first modelled this fuzzy reasoning, this fuzzy identification technique has found many practical applications in control, forecasting and reasoning. But better understanding of fuzzy logic's basic aspect is needed to be done thoroughly. These aspects are,

1) To design a rule base and database of FIS, No standard methods exist.

2) Tuning of MFs needed to be improved so that the output error can be minimized and the performance index of the controller can be improved.

ANFIS tool can provide remedies to these problems as it can create the fuzzy IF-THEN rules with suitable MFs so that the satisfying input-output pairs can be generated. ANFIS is an artificial neural network that uses Takagi–Sugeno fuzzy inference system. Since ANFIS works with both principles i.e. neural networks and fuzzy logic, so it has advantage of both in a single model. ANFIS is regarded as a universal estimator as it has fuzzy logic inference mechanism to approximate nonlinear functions.

5.1 Architecture and Algorithm

To understand the working of ANFIS tool, a simple multilayer feedforward network is explained to show the use of neural network learning algorithms and fuzzy reasoning to map an input space to an output space.

An example of the five-layer hybrid neuro-fuzzy system is the *Adaptive-Network-based Fuzzy Inference System*. It was proposed by J.S Jang [23]. ANFIS represents a Sugeno type fuzzy system, where the fuzzy rules take the following form,

Rule 1: if x is A_1 and y is B_1 then $z_1 = p_1 * x + q_1 * y + r_1$

Rule 1: if x is A_2 and y is B_2 then $z_2 = p_2 * x + q_2 * y + r_2$

Where, x and y is the input linguistic variable in the antecedent part of the first rule. And A_1 & B_1 are the linguistic label attached with it in that rule. A_1 has its associated

membership function given by$\mu_{A_i}(x_i)$. z_1 is the consequent output of the 1st rule and p_1, q_1 and r_1 are the Sugeno parameters.

The structure of the ANFIS consists of a five-layer feedforward network. The nodes in each layer have the same functionality. ANFIS only supports Sugeno type systems, with the following constraints,

- First or zero order Sugeno-type systems.
- Single output, obtained using a weighted average de-fuzzification method (linear or constant output membership functions).
- The weight of each rule is unity.

Fig 5.1 illustrates the ANFIS five-layer architecture for a two input (*x* & *y*) and one output (*z*) first order Sugeno-fuzzy model with four rules.

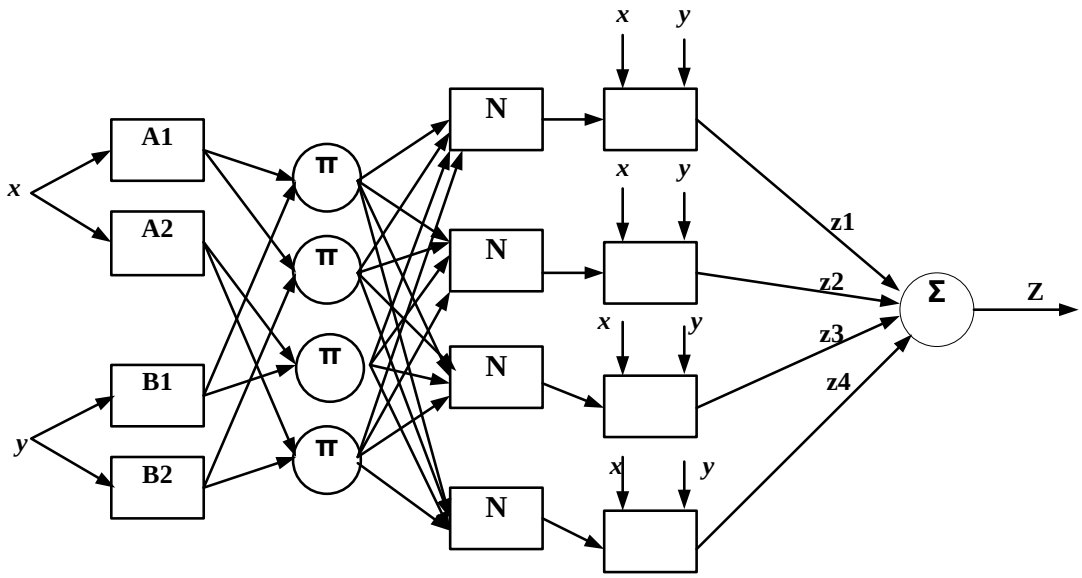


Fig 5.1 Five-layer ANFIS Feedforward Network

Layer 1: *input nodes*. Every node in this layer is characterized by its corresponding output function:

$O_{1,i} = \mu_{A_i}(x)$ For i = 1, 2

$O_{1,i} = \mu_{B_{i-2}}(y)$ For i = 3, 4 … (27)

Where *x* & *y* are the input to the nodes, and A_i & B_i is the linguistic label associated with this node function. Each node in this layer stores three parameters a_i, b_i, c_i to define a bell shaped membership function that represents the profile of the linguistic variables (*x* & *y*).

$$\mu_{A_i} = \frac{1}{1+\left|\frac{x-c_i}{a_i}\right|^{2b_i}} \quad ; \quad \mu_{B_{i-2}} = \frac{1}{1+\left|\frac{y-c_i}{a_i}\right|^{2b_i}} \qquad \ldots (28)$$

Layer 2: rule nodes. This layer stores the rules. Each rule is represented by one node. Each node is connected to those nodes in the previous layer that forms the antecedent of the rule. For a node *r*, the inputs are degrees of membership functions, which are multiplied through a T-norm operator $\otimes$ to determine the degree of fulfillment w_k of the rule.

$$O_{2,k} = w_k = \mu_{A_i}(x) \otimes \mu_{B_j}(y) \quad ; \qquad k = 1,\ldots, 4;\ i = 1, 2;\ j = 1, 2 \qquad \ldots (29)$$

Layer 3: average nodes. In this layer a unit computes the relative degree of fulfillment for every rule. Consequently, $\overline{w_i}$ is taken as the normalized firing strength

$$O_{3,i} = \overline{w_i} = \frac{w_i}{\sum_{k=1}^{4} w_k} \quad ; \qquad i = 1,\ldots, 4 \qquad \ldots (30)$$

Layer 4: consequent nodes. The nodes of this layer are connected to all input nodes and with exactly one node in layer three. Each node in this layer computes the output for the rule. In other words, it computes the consequent of the rule (*then* part):

$$O_{4,i} = \overline{w_i} f_i = \overline{w_i}(p_i x + q_i y + r_i) \quad ; \qquad i = 1,\ldots, 4 \qquad \ldots (31)$$

Where $\overline{w_i}$ is the output from the previous layer's i^{th} node. And $\{p_i, q_i, r_i\}$ are the parameter set.

Layer 5: output nodes. An output node computes the final output as the summation of all incoming signals from layer 4.

$$O_{5,1} = \sum_{i=1}^{4} \overline{w_i} f_i = \frac{\sum_{i=1}^{4} w_i f_i}{\sum_{i=1}^{4} w_i} \qquad \ldots (32)$$

And the de-fuzzification process converts each fuzzy result into a crisp output in this layer.

5.2 Construction of Neuro-Fuzzy System [73]

Usually to construct a neuro-fuzzy system we use a set of numerical set of data consisting of an input-output space. The construction of ANFIS involves two stages,

a. Structure learning phase (structure identification), It aims to determine the fuzzy rules structure.
b. Parameter learning phase, it used to tune and optimize the parameters of each fuzzy rules constructed in first phase.

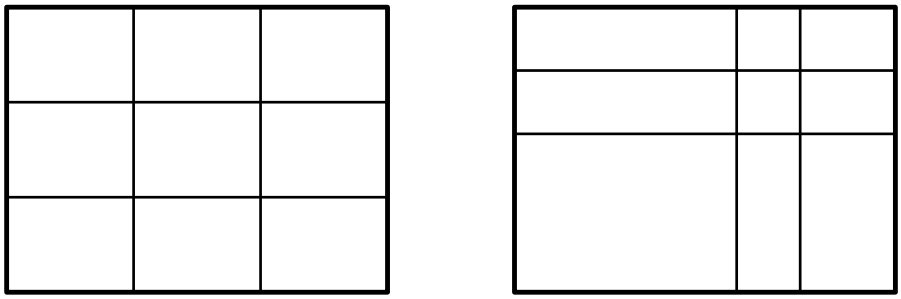
5.2.1 Structure Identification Phase

This is based on the partitioning of input output space. After the partitioning process, each partition represents one rule. In systems which uses crisp rules no overlap is seen in between their boundaries, while here in fuzzy system this overlap exists between boundaries.

There are several partitioning methods. Most common ones are given below,

5.2.1.1 Grid type Partitioning

In this, the multidimensional population of input-output data is divided into several partitions. And each partition corresponds to single fuzzy rule.



(a) **(b)**

Fig 5.2 (a) Fixed and (b) Adaptive Grid Partitioning

Fig 5.2 (a & b) shows the two types of grid partitioning methods, first is fixed and second is adaptive grid partitioning. In the first method, whole grid is partitioned into equal space, while in second fuzzy adaptation is applied i.e. there is no formal way in partitioning the space.

The advantage of grid partitioning method is that all the fuzzy rules can be generated using small number of linguistic variables but the serious disadvantage with this method is that the size of fuzzy rules generated by the grid partitioning method grows exponentially with the size of the space.

5.2.1.2 Clustering

The idea of clustering means to partition a collection of data points into distinct subset or clusters. The objects belonging to same clusters have same properties. In "hard" clustering each data point is assigned to a distinct cluster without any degree of membership of other clusters. However, in fuzzy cluster technique, each data point belong to a cluster with a specific degree determined by membership function value. Hence a data point can belong to any number of clusters with different membership function values.

Advantages of ANFIS tool:

- It possesses good capability of learning, constructing, expensing, and classifying.
- It has the advantage of allowing the extraction of fuzzy rules from numerical data or expert knowledge and adaptively constructs a rule base.
- It can tune the complicated conversion of human intelligence to fuzzy systems.

Drawback of the ANFIS:

- The time requested for training structure and determining parameters, which took much time.

5.3 Design of ANFIS for Proposed work

In this control scheme, where neural network optimization is used to generate rule base for fuzzy inference system. The controller is widely used as it incorporates the advantages of both NN and FIS. The MATLAB neuro-fuzzy toolbox is used to control the FLC. To train the neural network first input-output data pairs are collected and fed as an array to the toolbox. By using this data FIS file is generated using Grid partitioning method. This FIS file is then fed to the Fuzzy logic controller. The generated FIS file has two input and one output. The rule base is Sugeno based rule base, and the number of MFs used here are 5 for input and 5 for output, both having Gaussian bell shape. While both input MFs has same G_BELL shape and distribution and shown in Fig 5.3.

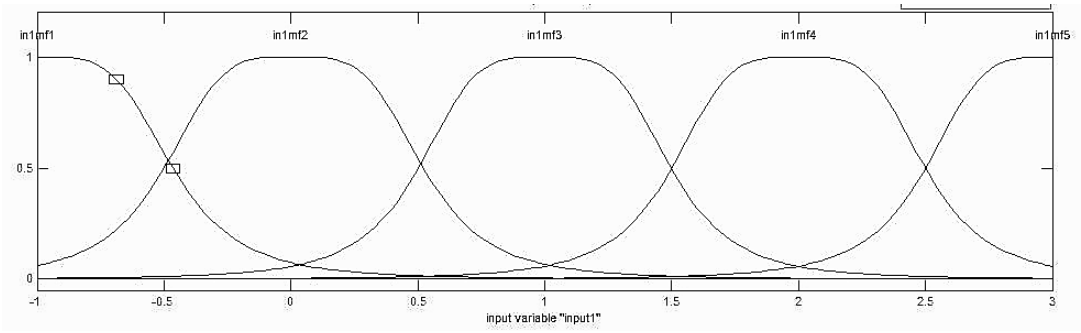


Fig 5.3 Membership Functions plot for Input variables of ANFIS controller

The rule base is tabulated in Table 5.1. The rule base is based on Sugeno method. The output is constant values and these are listed in the table below.

Table 5.1 Rule Base using ANFIS toolbox

e / **Δe**	**in1mf1**	**in1mf2**	**in1mf3**	**in1mf4**	**in1mf5**
in2mf1	-1.221	-1.022	-1.028	-0.8012	-0.1528
in2mf2	1.189	0.0297	1.319	-0.02458	0.01552
in2mf3	-3.515	0.641	0.9328	0.03428	0.006819
in2mf4	-0.4305	0.4893	0.06705	0.004406	0.02793
in2mf5	-0.07154	0.4702	0.03378	0.02392	0.4676

The rule base from the toolbox are shown in Fig 5.4.

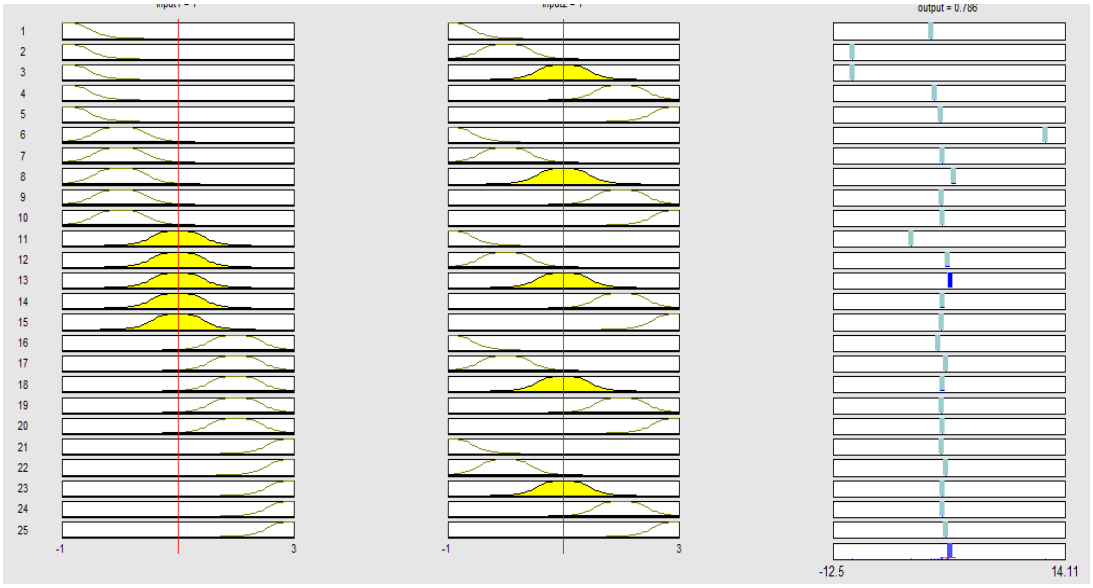


Fig 5.4 Rule Base view from the toolbox

In this chapter ANFIS algorithm is explained and a five layer architecture is shown to explain the working of ANFIS based feedforward network. The designing of membership functions and the rule base to control the DC link voltage is also explained.

Chapter 6

Results and Discussion

6.1 System configuration and Simulink model

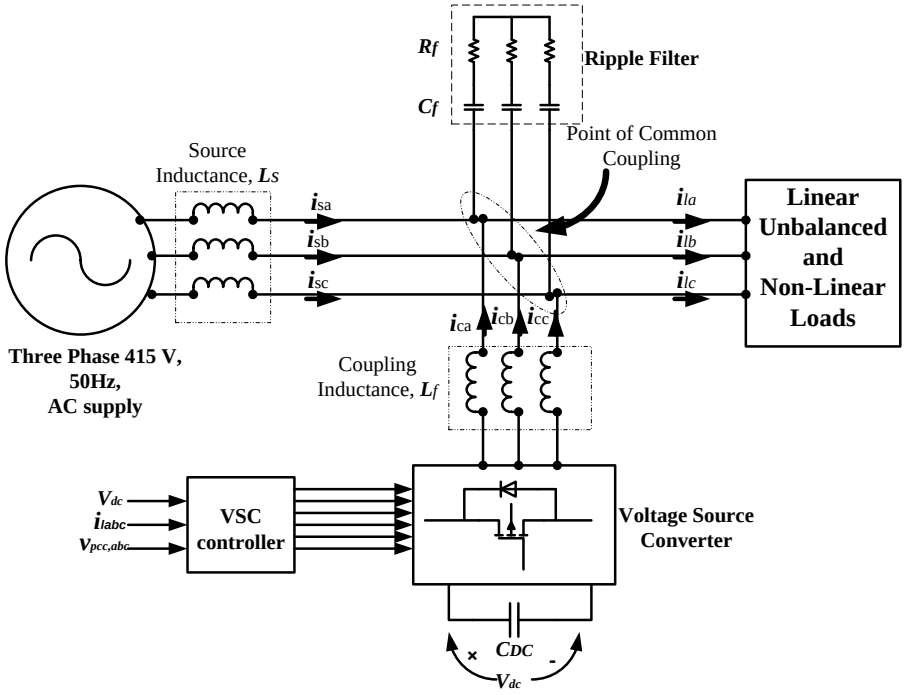


Fig 6.1 Schematic diagram for shunt connected DSTACOM to an AC Three phase three wire distribution system

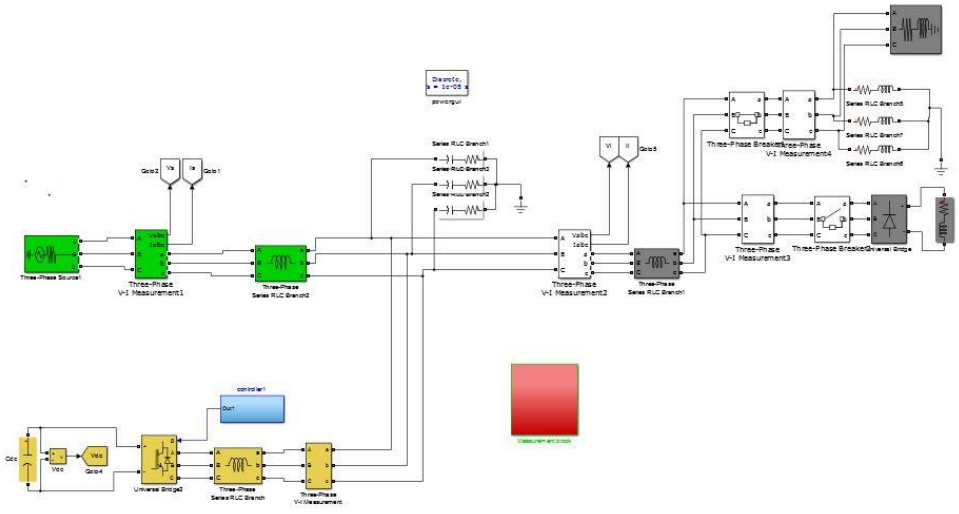


Fig 6.2 Simulink model of the system with shunt connected DSTATCOM

The system used for simulating the DSTATCOM and to show its performance against the linear+unbalanced and non-linear loads is shown in Fig 6.1. The Simulink model of the proposed system is shown in Fig 6.2. It can be seen that it has a three phase source generating three phase balanced voltage of magnitude 415 V, 50 Hz, depicting a balanced

grid or a distribution station. Two types of load (i.e. linear+unbalanced and non-linear) is used to check the performance of the system with and without the DSTATCOM. The ideal DSTATCOM configuration is used, using a universal bridge and DC capacitor to maintain constant voltage at the DC terminal of the bridge. Universal bridge has the configuration of three legged voltage source converter (VSC) i.e. six switches, each having one IGBT and an anti-parallel diode configuration. The loads are connected to the source through a short lossless line. The point of common coupling is at load side, as load compensation has been the concern in this thesis. The ripple filter is connected at PCC to eliminate the switching noise from the voltage at PCC.

To control the DSTATCOM different techniques are used to minimize the unwanted components of load current and stop them from reaching to grid (i.e. maintaining the source current sinusoidal and within IEEE 519 limits). The loads current demand without the compensator is shown in Fig 6.3.

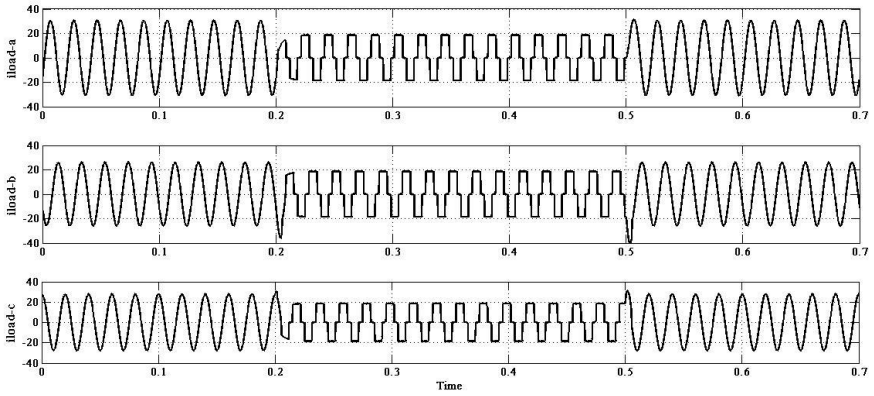


Fig 6.3 Load current waveform in each phase without D-STATCOM

For all the system configuration the linear unbalanced load is connected till 0.2 sec. from 0.2 to 0.5 sec only non-linear load is connected. At 0.5 sec again the initial linear unbalanced load is reconnected to the system.

The FFT analysis at different times for different line current is shown. The Fig 6.4 (a, b) is for linear+unbalanced and for non-linear loads in phase-*a* at time 0.1 sec and 0.3 sec.

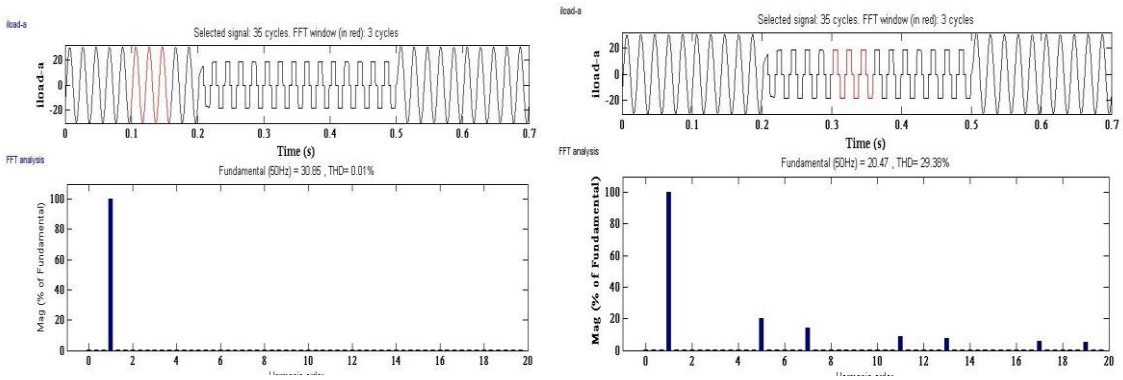


Fig 6.4 FFT analysis for phase-*a* line current with (a) linear+unbalanced load and (b) non-linear load

The magnitude of current flowing in line-*a* with linear+unbalanced load is 30.85A with negligible THD, and with non-linear load it is 20.47A with a THD of 29.38%.

Similarly, in line-*b* and line-*c* the FFT analysis is performed and the results are shown below.

The magnitude of line-*b* current, with linear+unbalanced load is 26.09 A with negligible THD, while with non-linear load it is 20.46A with 29.38% THD shown in Fig 6.5 (a & b) respectively.

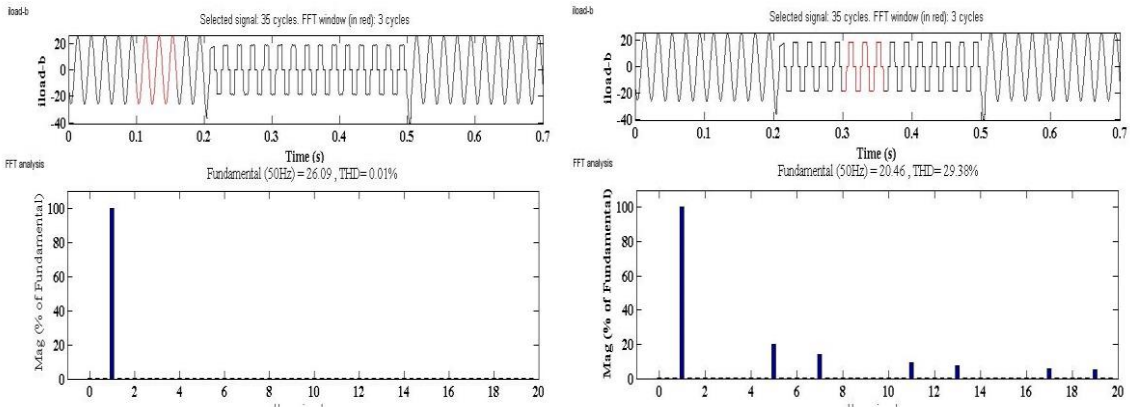


Fig 6.5 FFT analysis for phase-*b* line current with (a) linear+unbalanced load and (b) non-linear load

The magnitude of line-*c* current, with linear+unbalanced load is 27.9 A with negligible THD, while with non-linear load it is 20.47A with 29.38% THD is shown in Fig 6.6 (a & b) respectively.

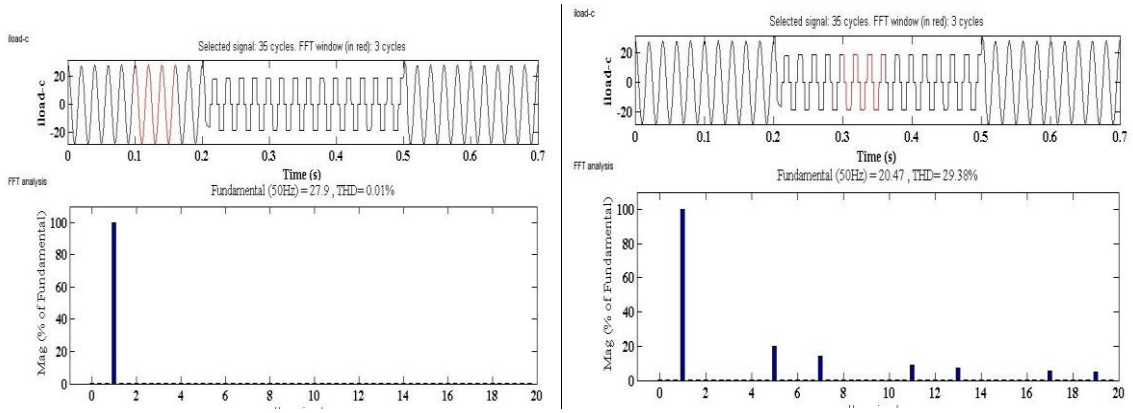


Fig 6.6 FFT analysis for phase-*c* line current with (a) linear+unbalanced load and (b) non-linear load

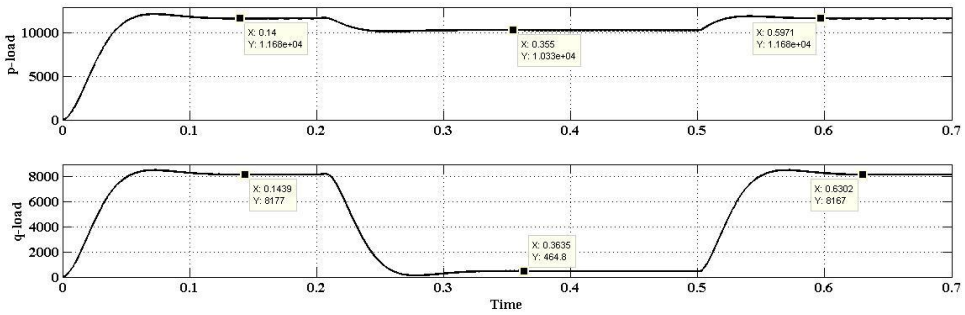


Fig 6.7 Instantaneous active and reactive power demand of loads

The instantaneous active and reactive power demand of the loads is shown in Fig 6.7. The magnitude of the instantaneous active power requirement of the linear+unbalanced load is $1.168*10^4$ W and reactive power requirement is 8139 VAr respectively. The instantaneous active and reactive power demand of non-linear load are $1.032*10^4$ W 438.4 VAr respectively.

The instantaneous active and reactive power supplied by the source through distribution center is shown in Fig 6.8. The different data cursors at the plot shows the active and reactive power feed to the load at different time instant. The mismatch between the required amount of power and delivered amount of power is due to the line impedances and the ripple filter losses.

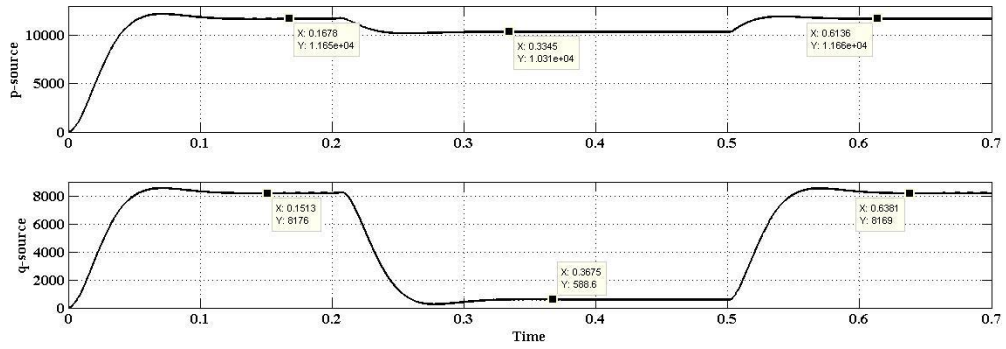


Fig 6.8 Instantaneous active and reactive power supply from source

To minimize the harmonic effect and reduce the reactive power requirement to zero, while maintaining balanced sinusoidal current at source side of the system (i.e. left to PCC), different controlling technique have been developed, some of the intelligent controlling technique and their results have been explained in coming sections of this chapter.

6.2 Synchronous Reference Frame Theory

This theory and its control technique is already explained in section 3.1. The Simulink model for the control technique is shown in Fig 6.9.

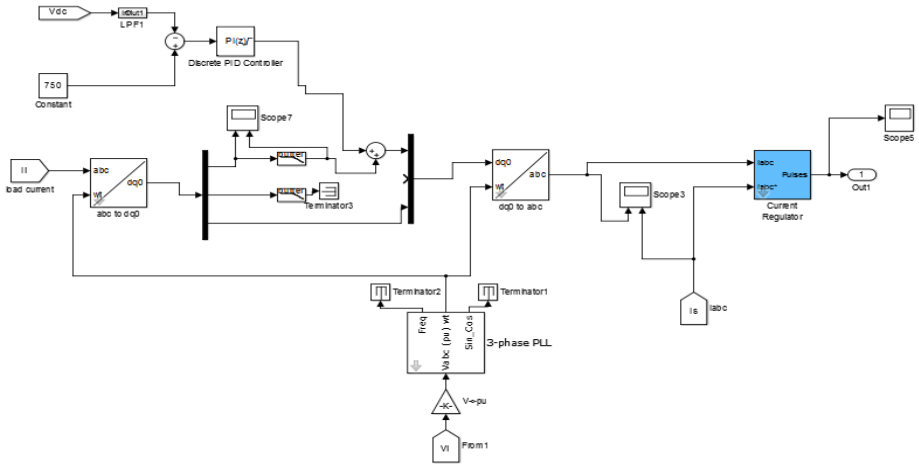


Fig 6.9 Simulink Control model based on SRFT

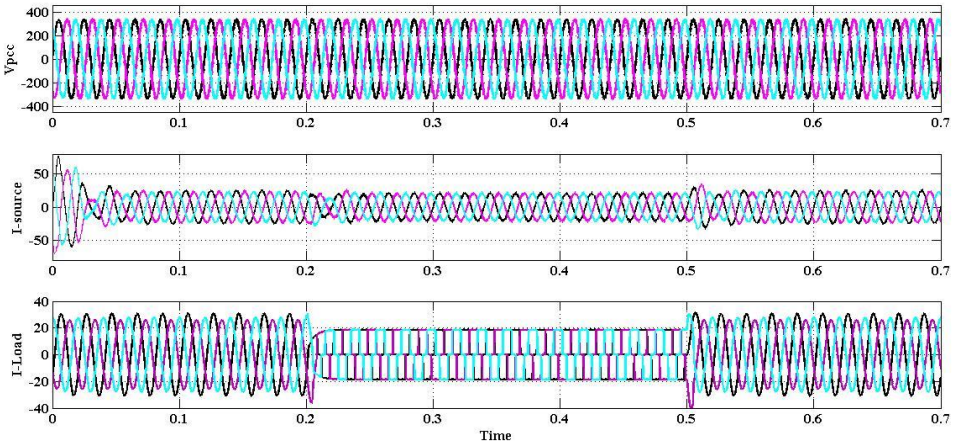


Fig 6.10 Three phase waveform of voltage at PCC (v_{pcc}), source current ($i_{s\text{-}abc}$) and load current ($i_{load\text{-}abc}$)

The controller shown is able to eliminate harmonics due to non-linear load, unbalancing and reactive power requirement of the linear+unbalanced load. The three phase waveforms of voltage, source current and load current is shown in Fig 6.10. The source current has

become sinusoidal irrespective of the distortions caused due to load current demand. Which means that all the unwanted current components are eliminated or stopped at the PCC by the DSTATCOM.

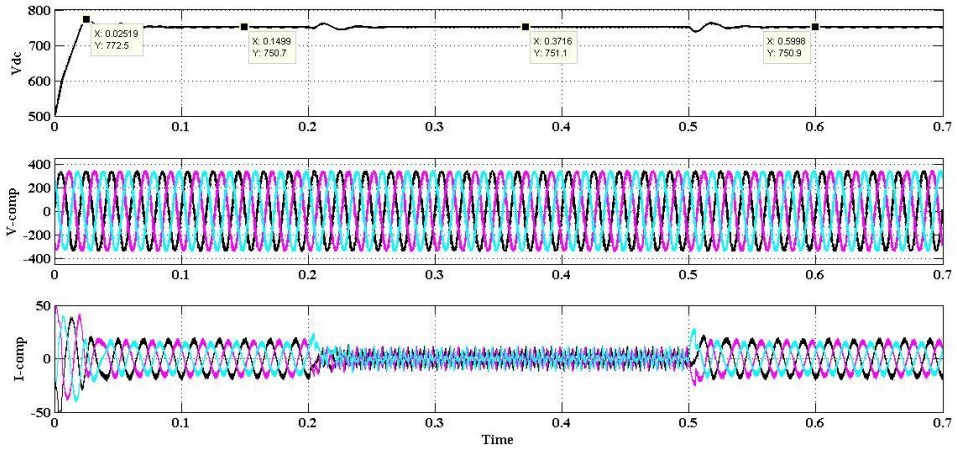


Fig 6.11 Waveforms of DC terminal voltage, AC voltage and current generated by the DSTATCOM

The Fig 6.10 shows the voltage at DC terminal and voltage and current at AC side of the inverter. The three phase waveform of the current generated from the DSTATCOM are shown separately in Fig 6.12.

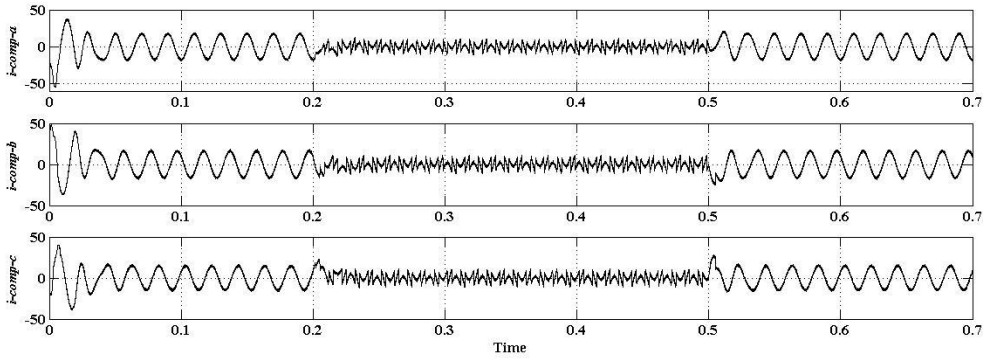


Fig 6.12 Three phase current waveform generated by the DSTATCOM

The FFT analysis of three source current waveform after the compensation is shown in Fig 6.13 (*a, b & c*). The FFT analysis of the currents shows that all the currents are having THD below 5%, which is the standard limit of IEEE-519 and the magnitude of the current flowing at source side of the PCC is also reduced.

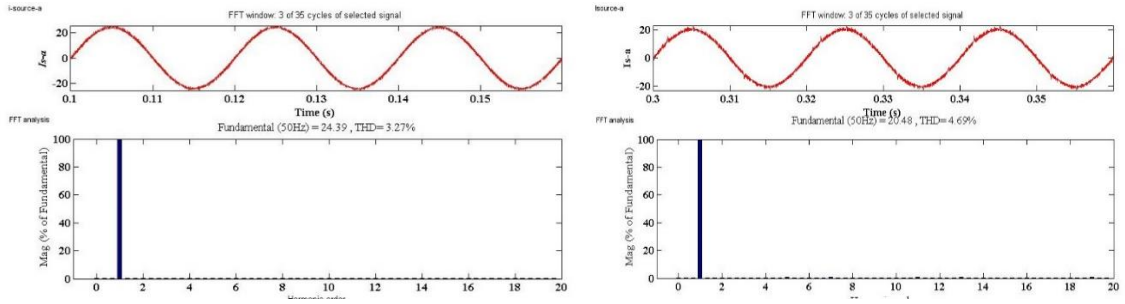


Fig 6.13 (a) Source current waveform of Phase-*a* at time 0.1 sec and 0.3 sec

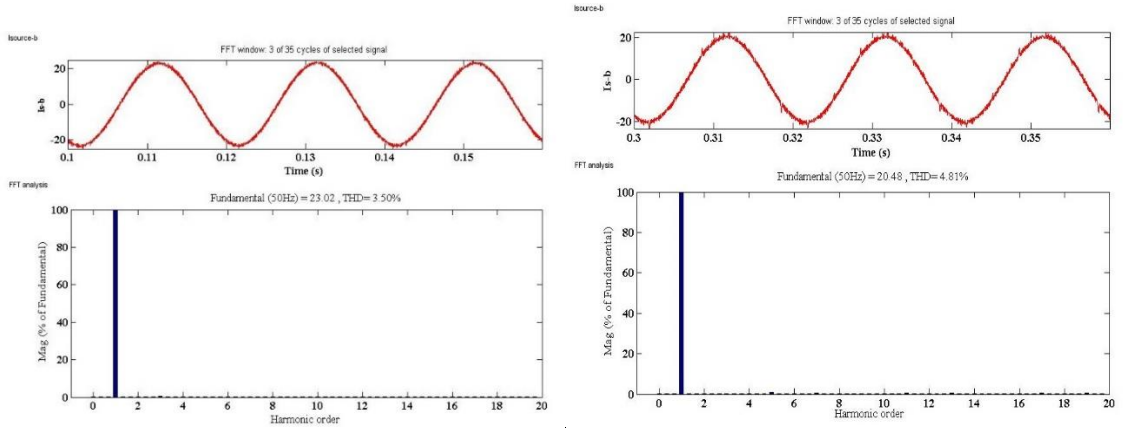


Fig 6.13 (b) Source current waveform of Phase-*b* at time 0.1 sec and 0.3 sec

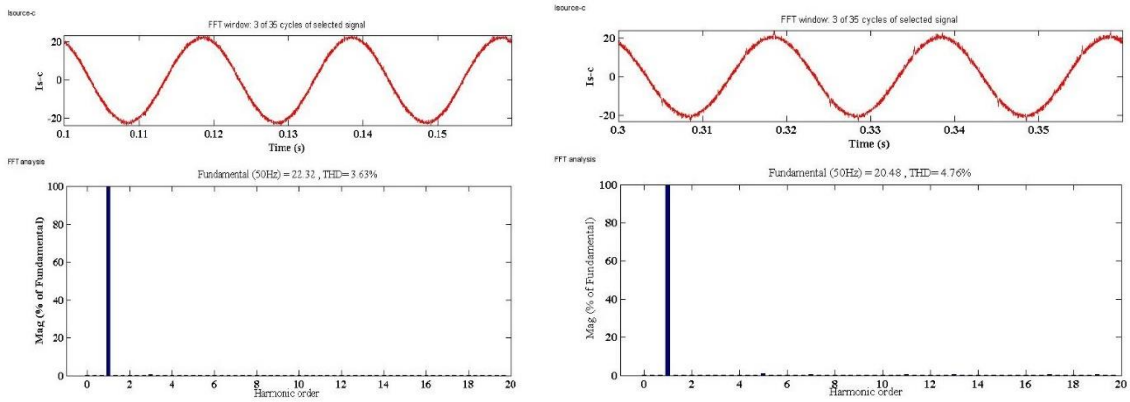


Fig 6.13 (c) Source current waveform of Phase-*c* at time 0.1 sec and 0.3 sec

Table. 6.1 List of Magnitude and THD % in three line currents after compensation

Type of Load / Phase	(Linear+unbalanced load) (At t=0.1 sec)	Non-linear load (at t=0.3 sec)
i_{sa}	Magnitude =24.39A THD = 3.29%	Magnitude = 20.48A THD = 4.69%
i_{sb}	Magnitude =23.02A THD =3.50%	Magnitude =20.48A THD = 4.81%
i_{sc}	Magnitude = 22.32A THD = 3.63%	Magnitude = 20.48A THD = 4.76%

The instantaneous active and reactive power from source and compensator and demand of the load are shown in Fig 6.14 (a, b & c). It can be seen from the Fig. that almost all reactive power demand of the load is fulfilled by the DSTATCOM, while the losses in the line and in VSC are fulfilled by the source.

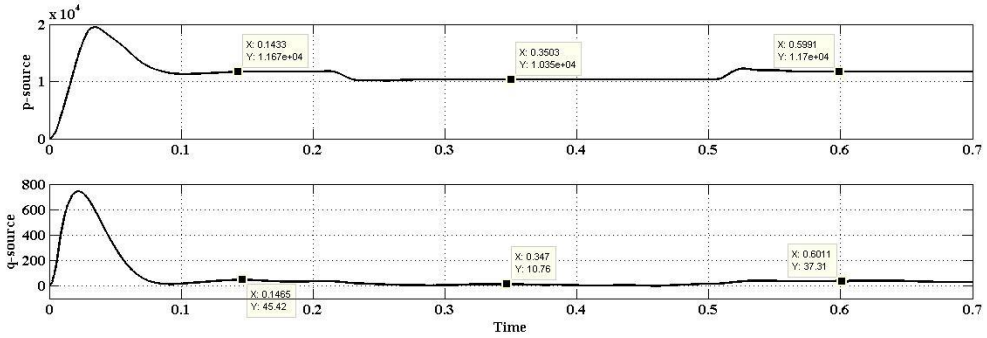


Fig 6.14 (a) Instantaneous active and reactive power delivered from source

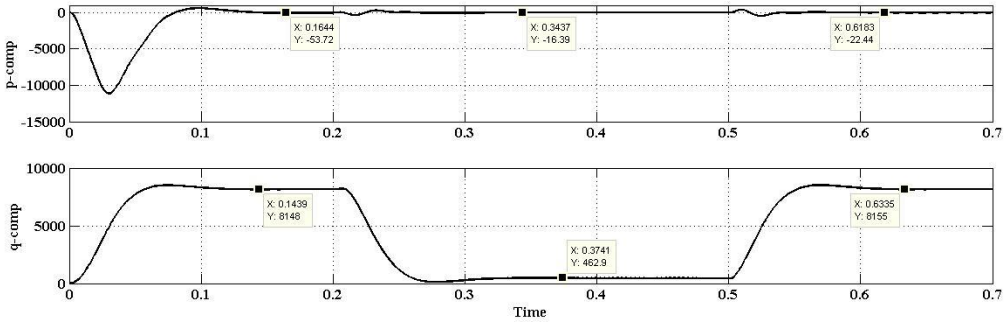


Fig 6.14 (b) Instantaneous active and reactive power delivered from DSTATCOM

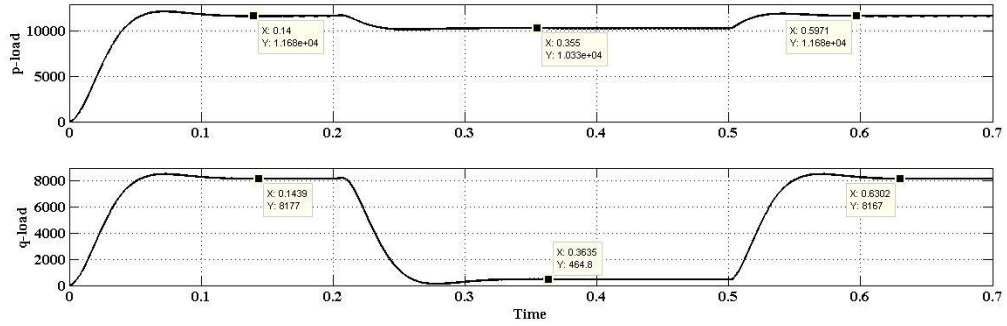


Fig 6.14 (c) Instantaneous active and reactive power demand of load

6.3 Conductance based Fryze algorithm

The Fryze algorithm and its controller is explained in section 3.2 of this thesis. The Simulink model of the controller is shown in Fig 6.15. The 3-φ waveforms of the voltages at PCC, currents from the source and current demand of the load are shown in Fig 6.16.

The source current waveforms are sinusoidal irrespective of the distorted load because of the DSTATCOM. The voltage at DC terminal, the voltage at compensator AC terminal and the current generated by the DSTATCOM is shown in Fig 6.17.

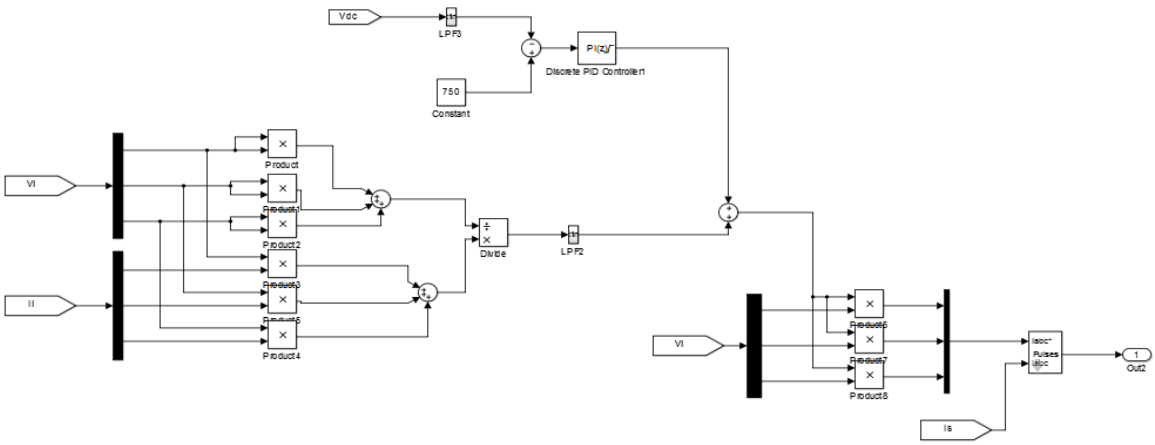


Fig 6.15 Simulink model of the Fryze algorithm based controller

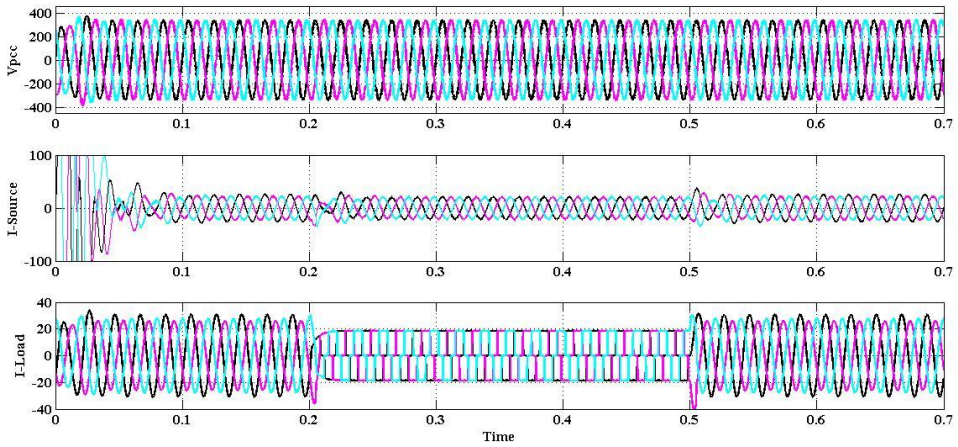


Fig 6.16 Voltage at PCC (V_{pcc}), source current (*I-source*) and load current (*I-load*)

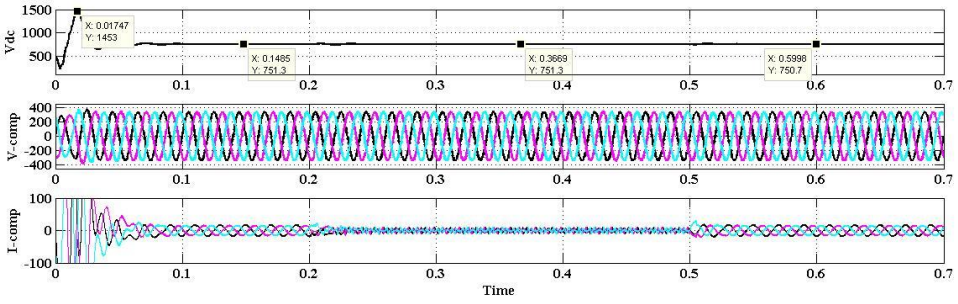


Fig 6.17 Voltage at DC terminal (V_{dc}), at AC terminal (V-comp) and current (I-comp) generated by the compensator respectively

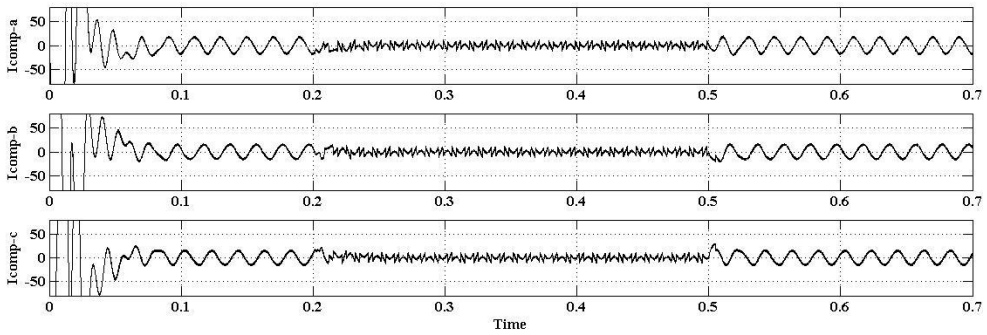


Fig 6.18 Three phase AC current generated from DSTATCOM

Three phase current generated from the DSTATCOM to compensate the load from DSTATCOM is shown in Fig 6.18. The current is too much distorted at the starting because of the DC voltage controller. As the requirement of active power at starting is high to maintain the DC terminal voltage at 750 *V*.

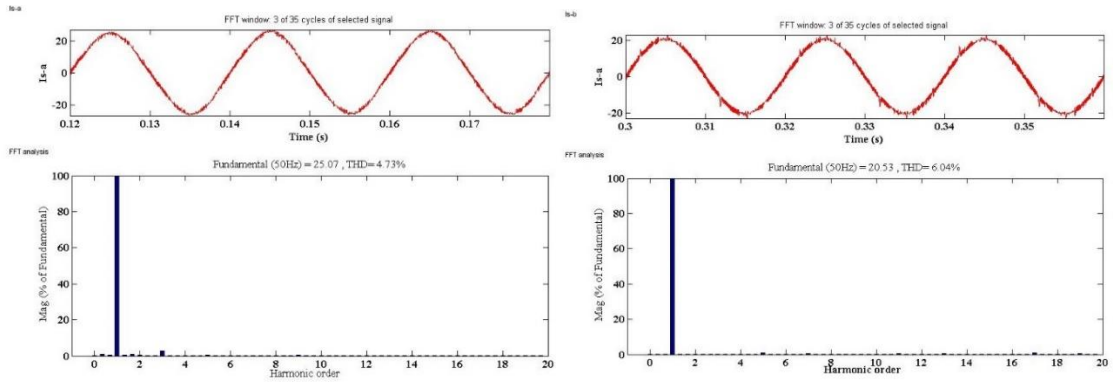


Fig 6.19 (a) THD of the line current of phase-*a* at time *t* = 0.1 sec and at *t* = 0.3 sec respectively

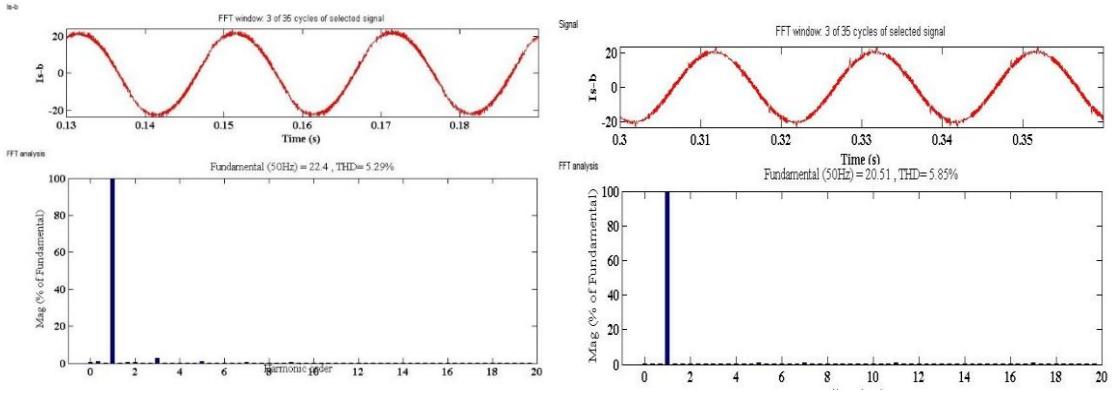


Fig 6.19 (b) THD of the line current of phase-*b* at time *t* = 0.1 sec and at *t* = 0.3 sec respectively

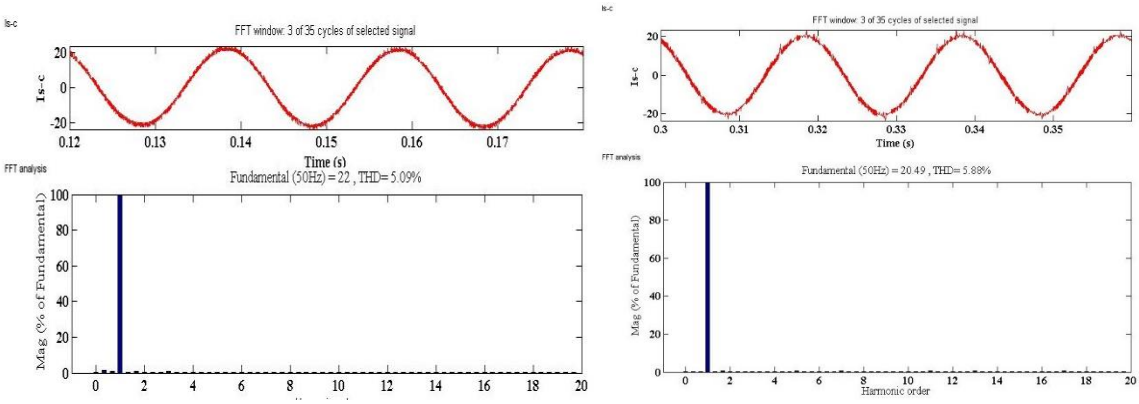


Fig 6.19 (c) THD of the line current of phase-*c* at time *t* = 0.1 sec and at *t* = 0.3 sec respectively

The FFT analysis of three source currents are shown in Fig 6.19 (a, b & c). The resulted waveform show the slightly higher THD in current waveform then the IEEE-519 standards. Also this technique is not able to minimize the unbalancing present in the load current.

The instantaneous active and reactive power fed from the source, from D-STATCOM and to load are shown in Fig 6.20 (a, b & c) respectively.

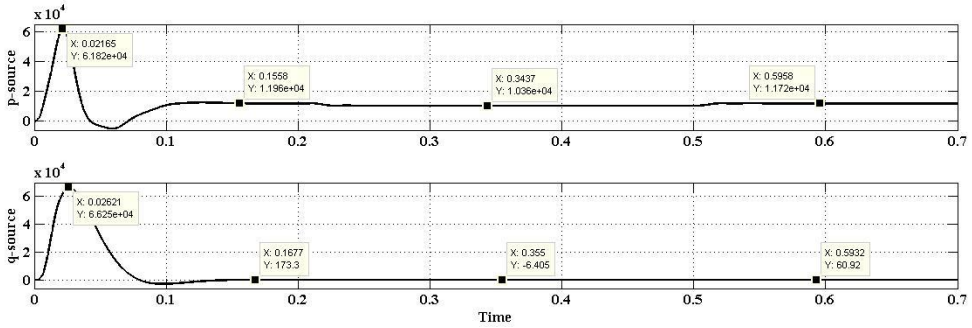


Fig 6.20 (a) Instantaneous active and Reactive power supplied from source

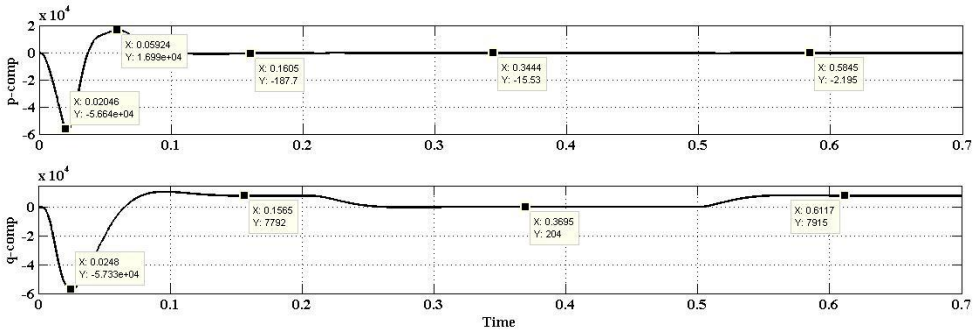


Fig 6.20 (b) Instantaneous active and Reactive power supplied from DSTATCOM

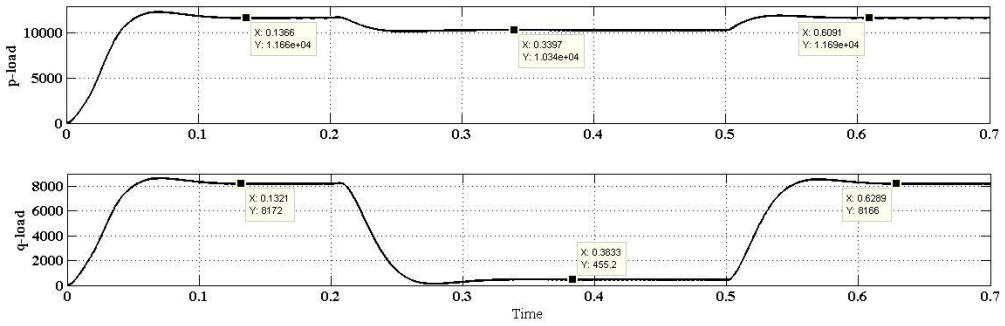


Fig 6.20 (c) Instantaneous active and Reactive power demand of load

From the graph of instantaneous active and reactive power of the compensator and the source it can be deduced that at the time of starting the requirement of active power and reactive power is quite high, but at the time of switching (i.e. transient) the DC voltage remains almost constant and this represent stable nature of this algorithm in case of the transients occur in the system. But all the reactive power and harmonic power requirement is met by the DSTATCOM, so the losses in the transmission and the apparent power send from the source will be reduced.

6.4 Different Topologies of FLC

6.4.1 PI-like FLC

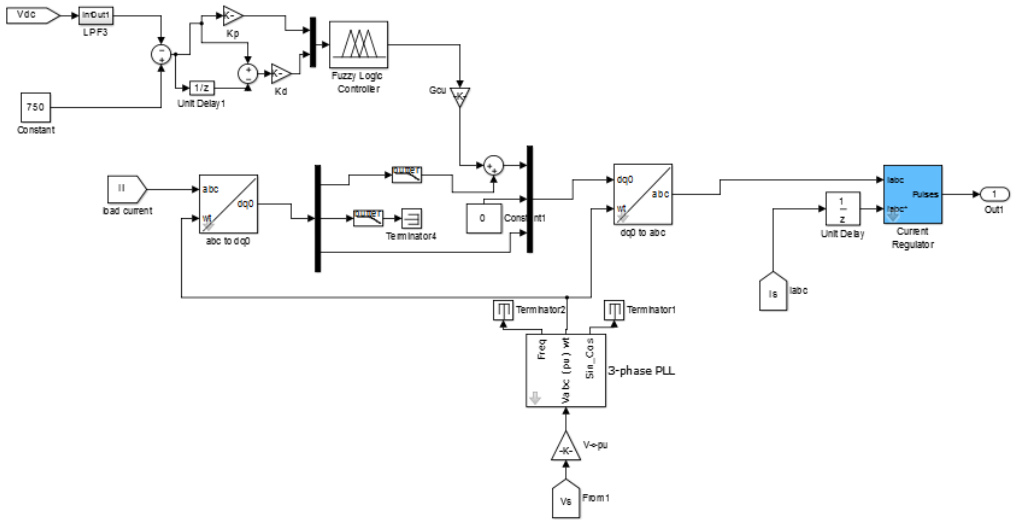


Fig 6.21 Simulink model of PI-like FLC controller for DSTATCOM

The controller designing and the working rules and membership functions are explained in section 4.1 of this thesis. Here we only look at the response of this controller on the system and on the load. The Simulink model for PI-like FLC is shown in Fig 6.21.

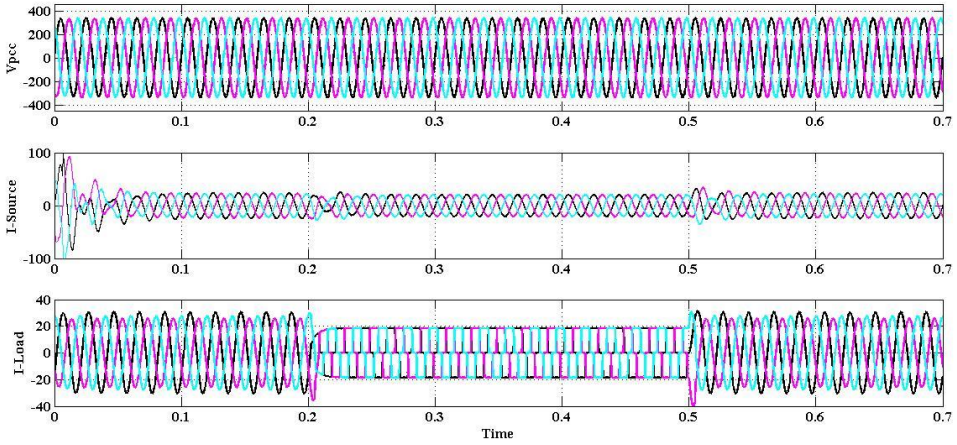


Fig 6.22 Three Phase Voltage at PCC (v_{pcc}), source side current (i_{source}) and Load side current (I_{load})

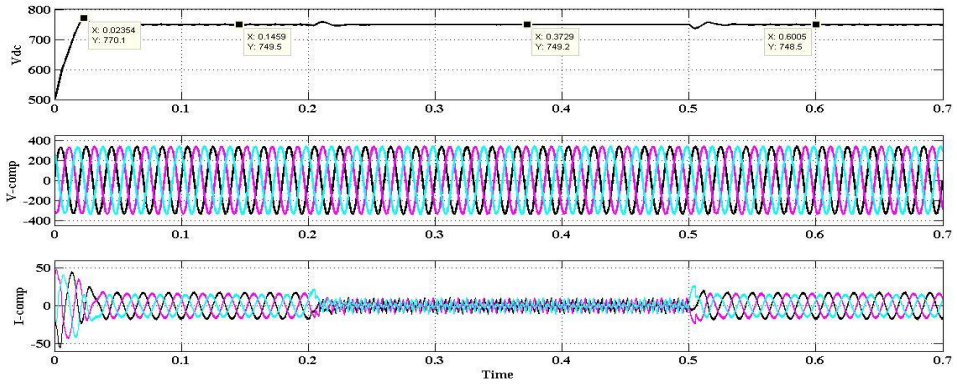


Fig 6.23 Voltage at DC terminal (V_{dc}), at AC terminal (V-comp) and current (I-comp) generated by the compensator respectively

The three phase waveforms of voltage at PCC, line current at source side and line current at load side is shown in Fig 6.22. The DC terminal voltage and the AC side voltage at the DSTATCOM terminals with the line current fed by the compensator are shown in Fig 6.23.

it can be seen from the fig that all the unwanted component of load current are removed and source side current is perfectly sinusoidal. The FFT analysis at three line current of source side are shown in Fig 6.24 (a, b & c).

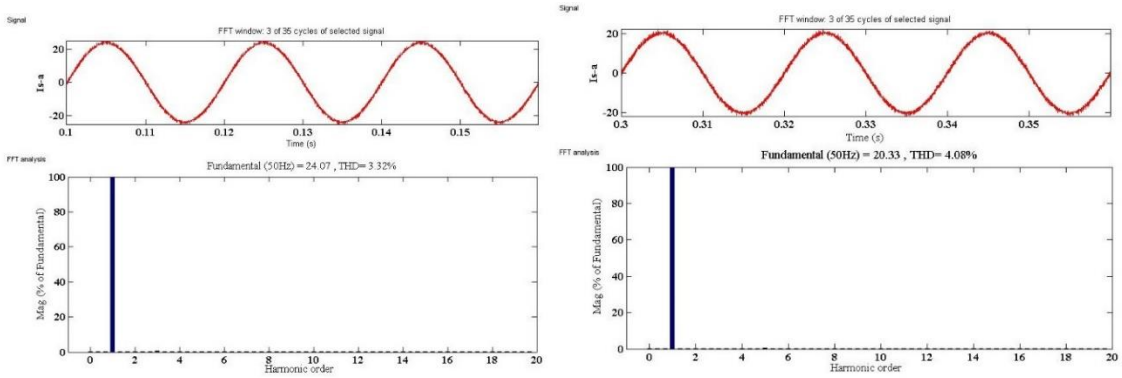


Fig 6.24 (a) THD of the line current of phase-*a* at time *t* = 0.1 sec and at *t* = 0.3 sec respectively

The three line currents have THD within IEEE-519 limits. And it can be seen that the unbalancing in all three currents is minimized at source side.

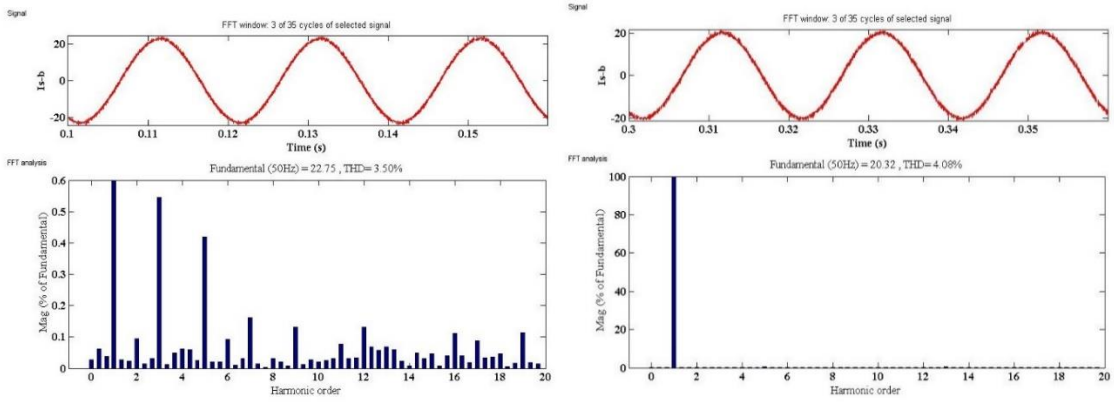


Fig 6.24 (b) THD of the line current of phase-*b* at time *t* = 0.1 sec and at *t* = 0.3 sec respectively

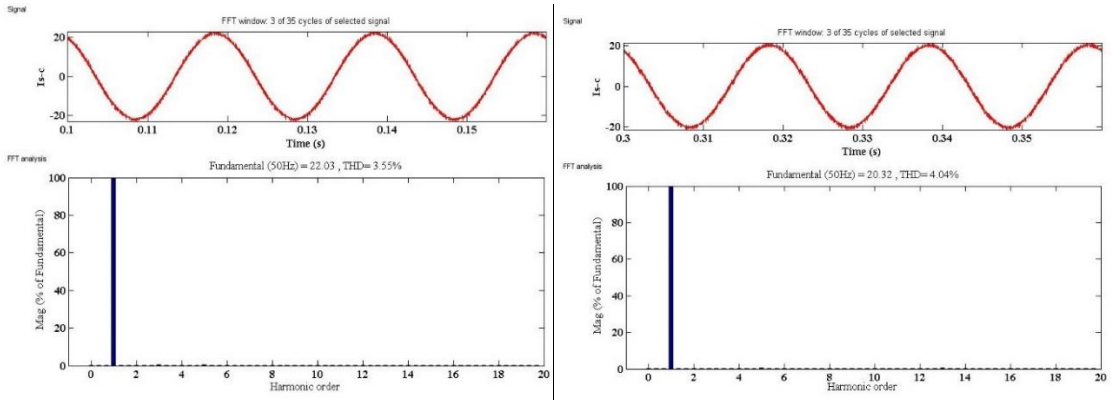


Fig 6.24 (c) THD of the line current of phase-*c* at time *t* = 0.1 sec and at *t* = 0.3 sec respectively

The instantaneous active and reactive powers from the source, from DSTATCOM and to the load are shown in Fig 6.25 (a, b & c).

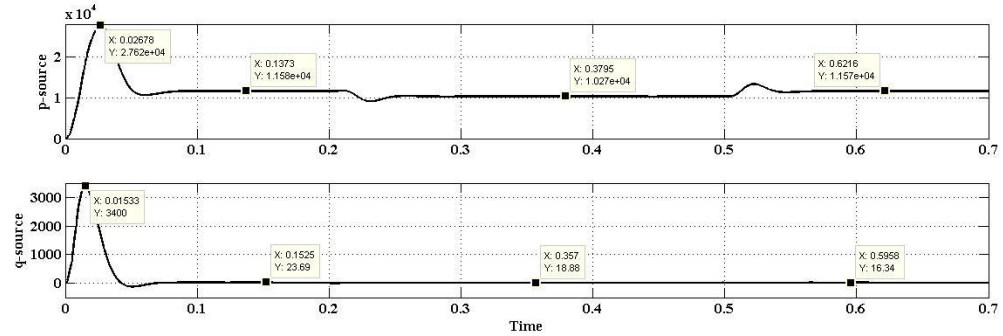


Fig 6.25 (a) Instantaneous active and reactive powers from source respectively

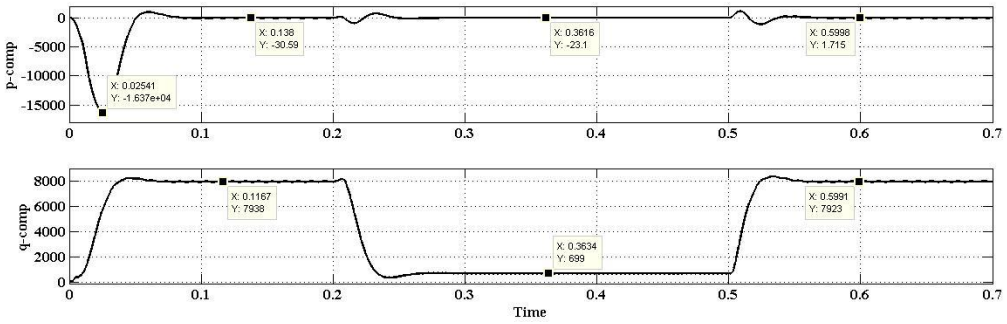


Fig 6.25 (b) Instantaneous active and reactive powers from DSTATCOM respectively

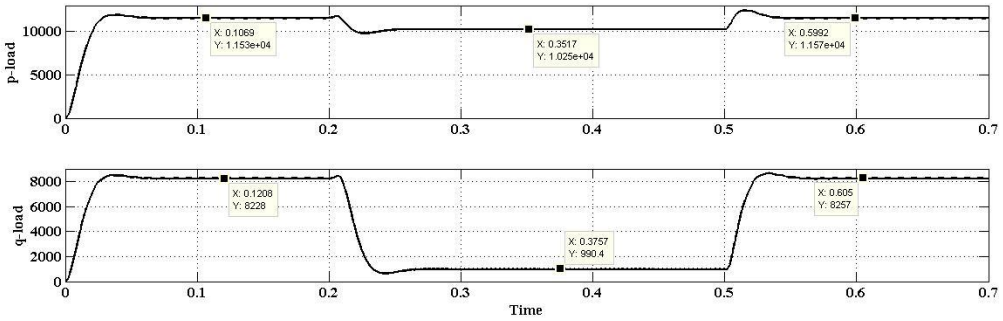


Fig 6.25 (c) Instantaneous active and reactive powers to load respectively

It can be seen from the above fig that all the active power requirement of the load with the losses into the system lines and in VSC is fed from the source, while the reactive power requirement and harmonic elimination is done by the DSTATCOM. This can be concluded as the apparent power required from the source is reduced so as the losses in the system.

6.4.2 PI Gain Scheduling using FLC

This is another topology used as an advancement to the fuzzy logic controllers. In this both the controllers i.e. FLC and PI controller, are used to incorporate the advantages of both controllers in one. FLC is used to on-line control the gains of the PI controller. The Simulink model of the controller is shown in Fig 6.26.

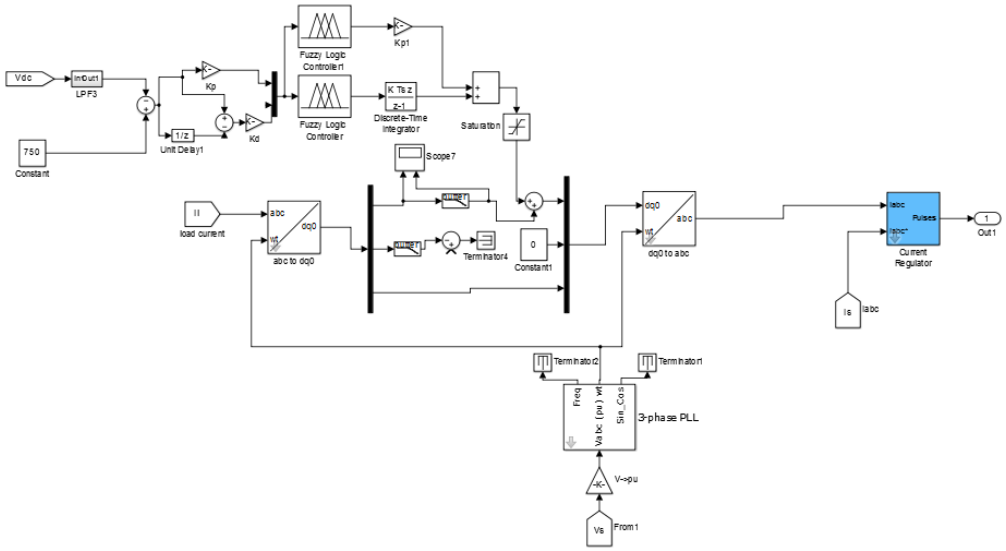


Fig 6.26 Simulink model for PI gain scheduled type FLC controller

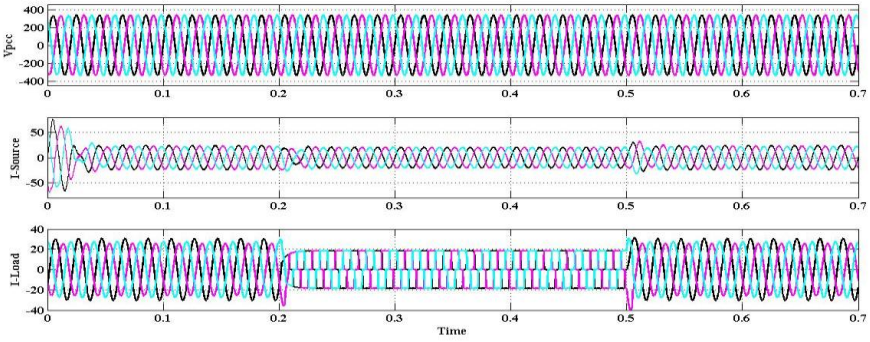


Fig 6.27 Three phase waveform of Voltage at PCC (V_{pcc}), Current at source side (I-source), current at load side (I-load) respectively

The three phase waveforms of PCC voltages, line currents from source and line currents at load side respectively are shown in Fig 6.27. The source side line currents are sinusoidal waveforms irrespective of the distorted load current. The DC terminal voltage, three phase AC terminal voltage and the DSTATCOM three phase line currents are shown in Fig 6.28.

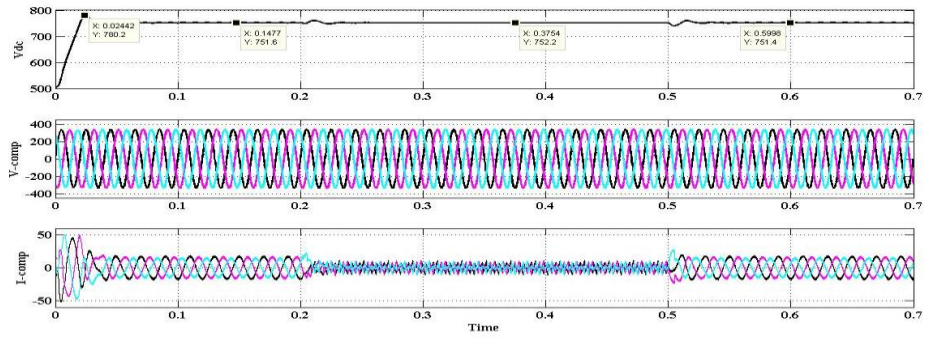


Fig 6.28 DC terminal voltage (V_{dc}), three phase AC terminal voltage (V_{comp}) and line currents (I_{comp}) from DSTATCOM respectively

The DC terminal voltage is maintained at 750V constant, even when switching of loads take place in the system. The THD analysis of the three line currents at source side is shown in Fig 6.29 (a, b & c). And the instantaneous active and reactive powers from source, from DSTATCOM and to load are shown in Fig 6.30 (a, b & c) respectively.

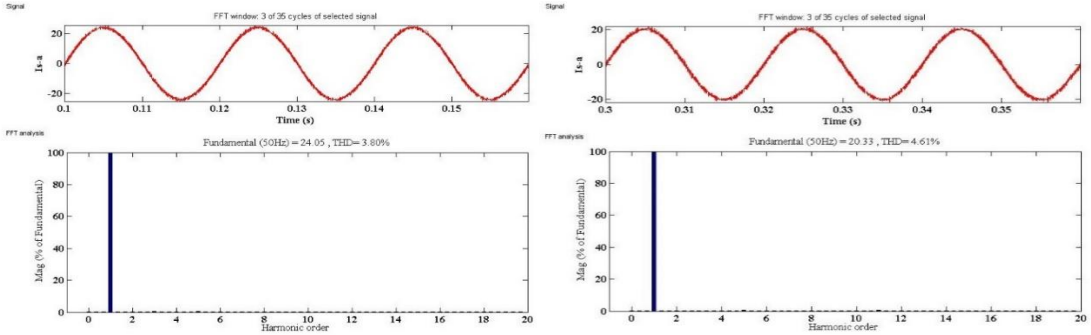


Fig 6.29 (a) THD of the line current of phase-*a* at time *t* = 0.1 sec and at *t* = 0.3 sec respectively

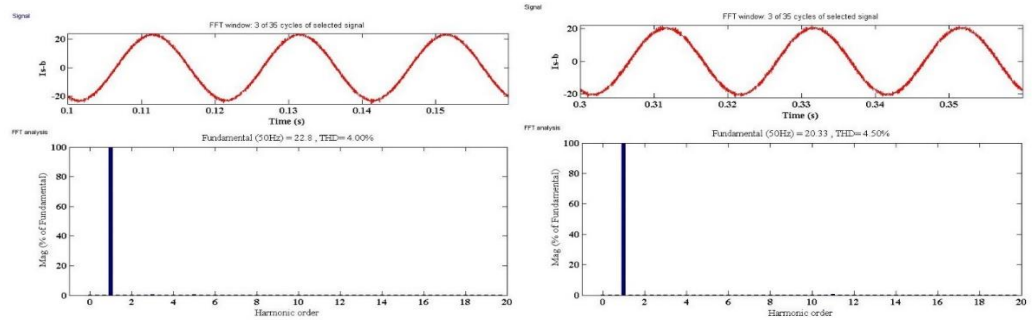


Fig 6.29 (b) THD of the line current of phase-*b* at time *t* = 0.1 sec and at *t* = 0.3 sec respectively

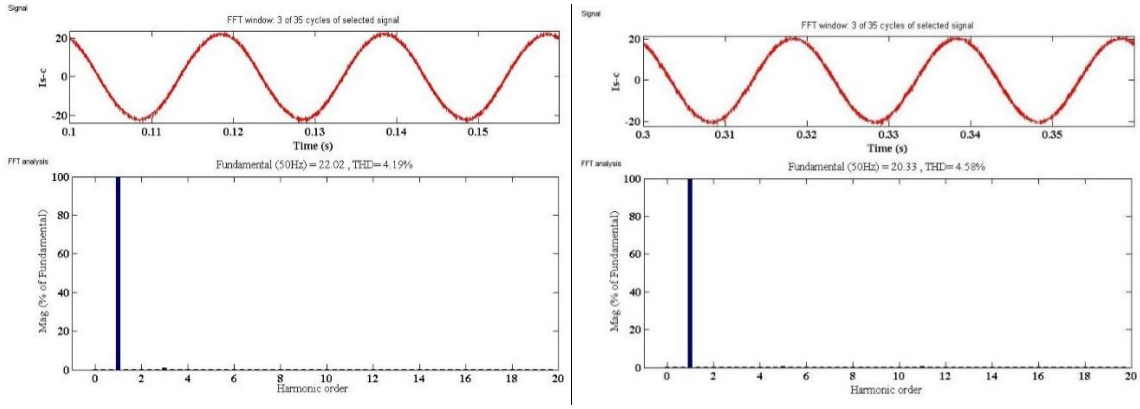


Fig 6.29 (c) THD of the line current of phase-*c* at time *t* = 0.1 sec and at *t* = 0.3 sec respectively

The THD analysis of the line current shows the harmonic content available in the line current, and it can be seen that it is well below the THD limit of 5% as per IEEE-519 standards. So the DSTATCOM is able to eliminate the harmonics and the reactive power

demand of the load is also fulfilled from the DSTATCOM which can be verified from the Fig 6.29 (b).

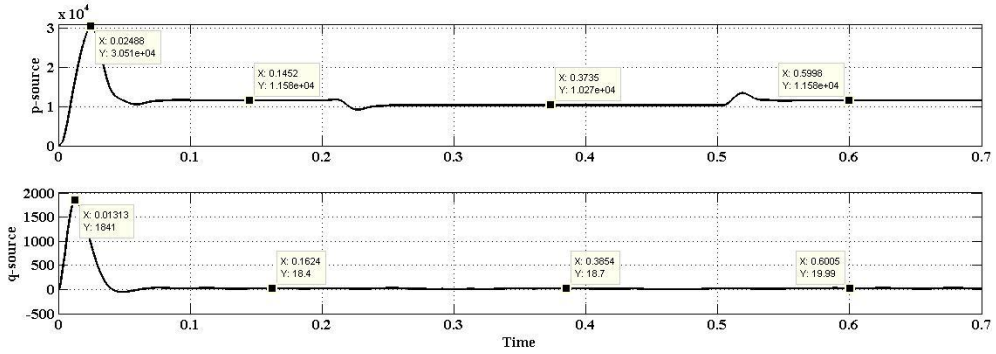


Fig 6.30 (a) Instantaneous active and reactive powers from source respectively

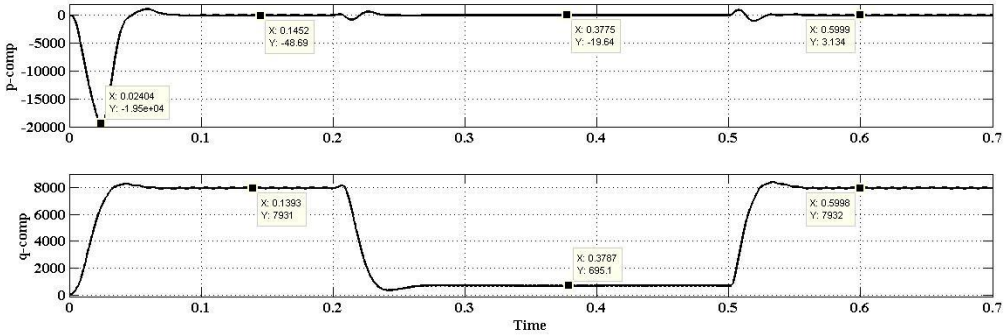


Fig 6.30 (b) Instantaneous active and reactive powers from DSTATCOM respectively

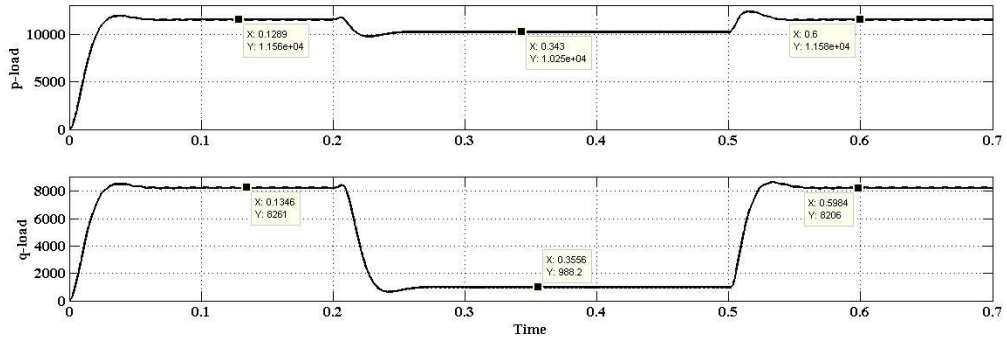


Fig 6.30 (c) Instantaneous active and reactive powers to the load respectively

6.4.3 Hybrid Fuzzy-PI controller

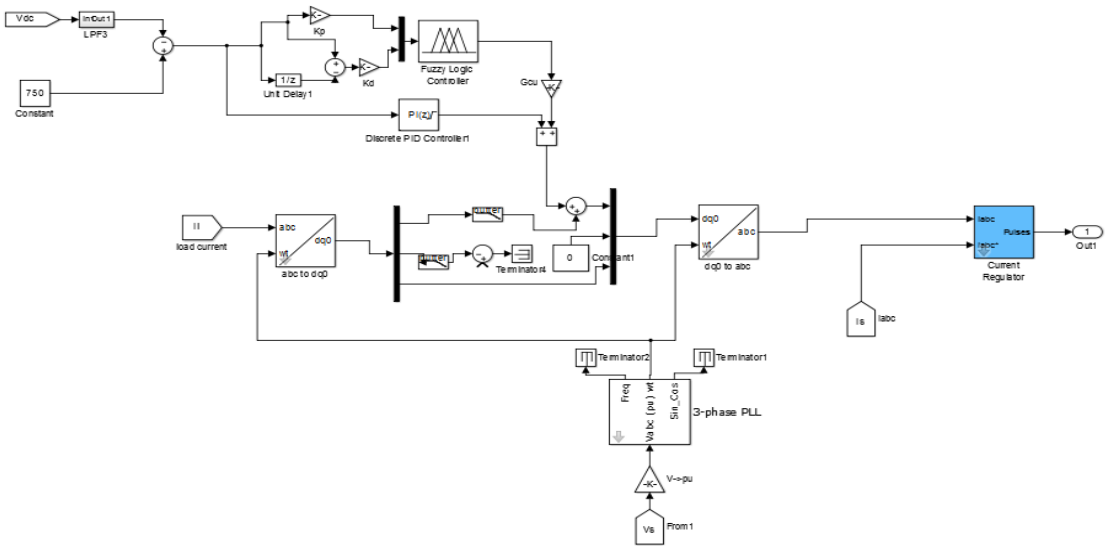


Fig 6.31 Simulink model of Hybrid fuzzy-PI controller for DSTATCOM

The hybrid Fuzzy-PI controller is already explained in section 4.3, also the working of the controller is explained there only. The Simulink model of the Hybrid fuzzy-PI controller is shown in Fig 6.31. The resulted three phase waveforms of voltage at PCC, line currents from the source and line currents to the load is shown in Fig 6.32.

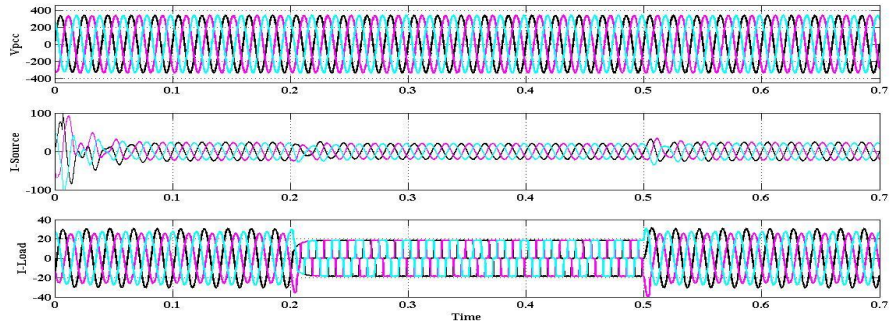


Fig 6.32 Three phase voltage at PCC (V_{pcc}), line current from source (I-source) and line current from load (I-Load) respectively

The three phase line currents can be seen to be sinusoidal irrespective of the distorted and lagging load current. The DC terminal voltage, AC terminal voltage and the compensating current generated by the DSTATCOM are shown in Fig 6.33 respectively.

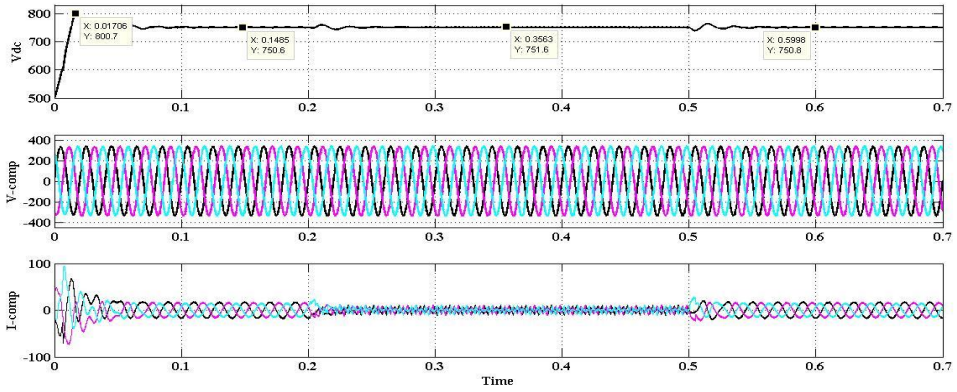


Fig 6.33 DC terminal voltage (V_{dc}), AC terminal voltage (V_{comp}) and compensating currents (I_{comp}) respectively

The FFT analysis of the source currents of each phase are shown in Fig 6.34 (a, b & c) respectively. The THD of the current is seen to be within IEEE-519 limits.

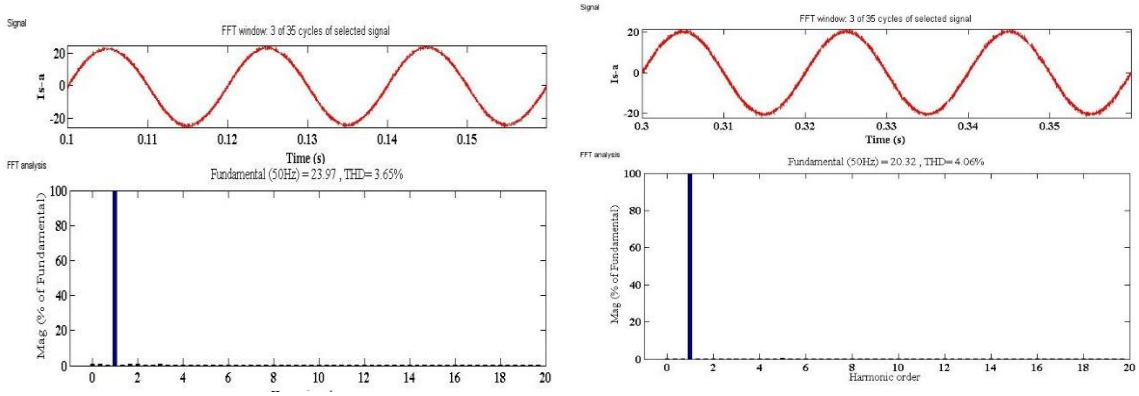


Fig 6.34 (a) THD of the line current of phase-*a* at time *t* = 0.1 sec and at *t* = 0.3 sec respectively

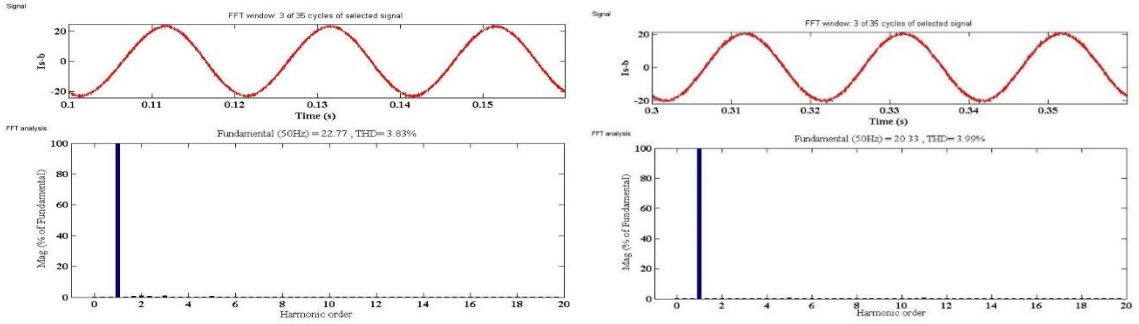


Fig 6.34 (b) THD of the line current of phase-*b* at time *t* = 0.1 sec and at *t* = 0.3 sec respectively

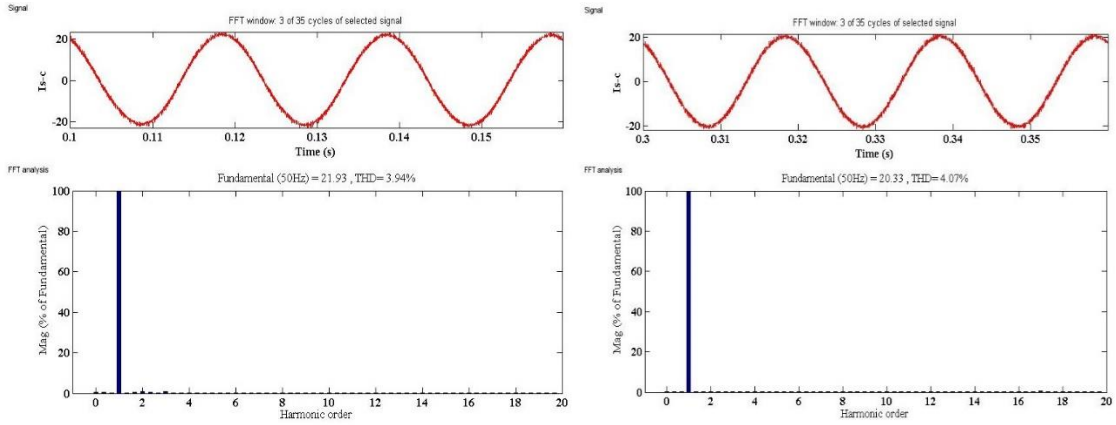


Fig 6.34 (c) THD of the line current of phase-*c* at time t = 0.1 sec and at t = 0.3 sec respectively

The instantaneous active and reactive power fed from source, from DSTATCOM and to load are shown in Fig 6.35 (a, b & c) respectively.

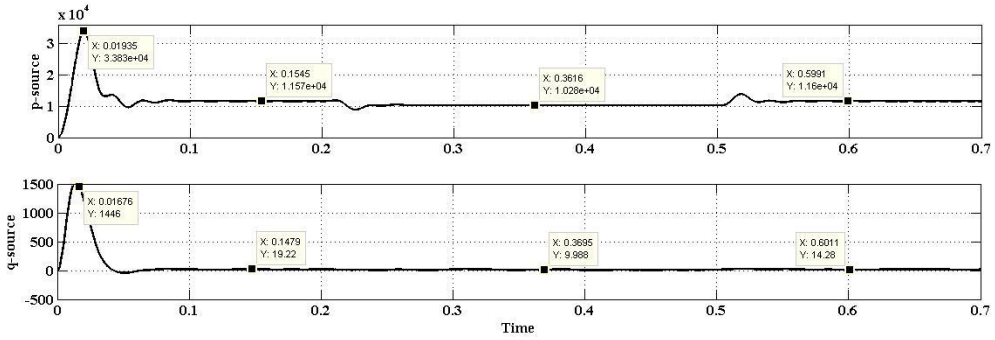


Fig 6.35 (a) Instantaneous active and reactive powers from source respectively

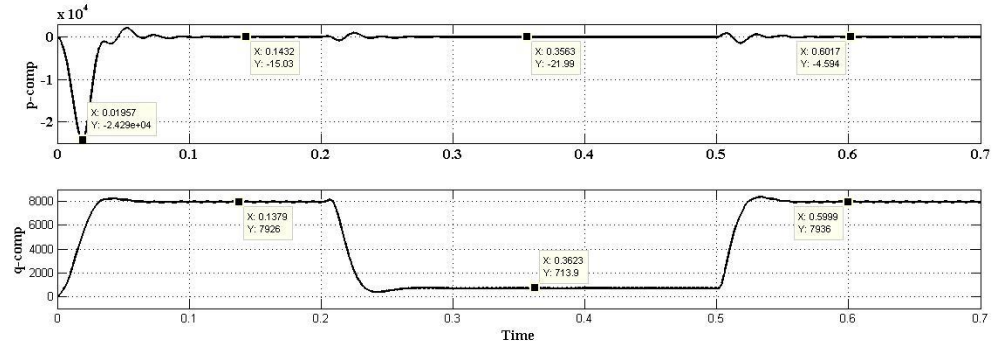


Fig 6.35 (b) Instantaneous active and reactive powers from DSTATCOM respectively

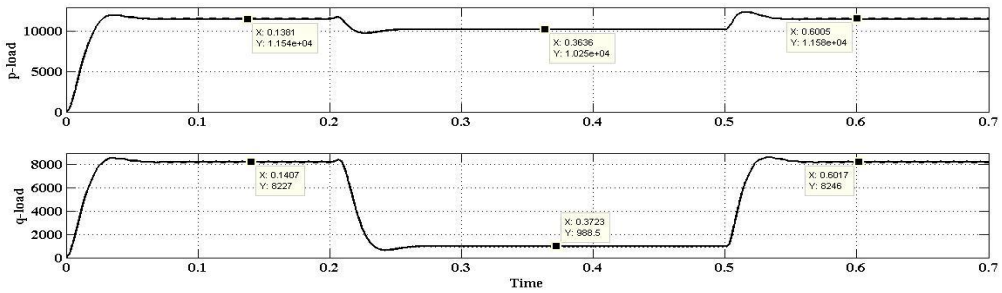


Fig 6.35 (c) Instantaneous active and reactive powers to load respectively

It can be deduced from the Fig 6.35 (a), that all the active power is send from the source with negligible amount of reactive power. So the apparent power send from the source is reduced, consequently reducing the losses in the system. The required reactive power by the load is fed from DSTATCOM, simultaneously the harmonic content of the load is reduced to the standard limits of 5%.

6.5 ANFIS based Control Scheme

The three phase voltage at PCC, line current from source and line current to load is shown in Fig 6.36 respectively.

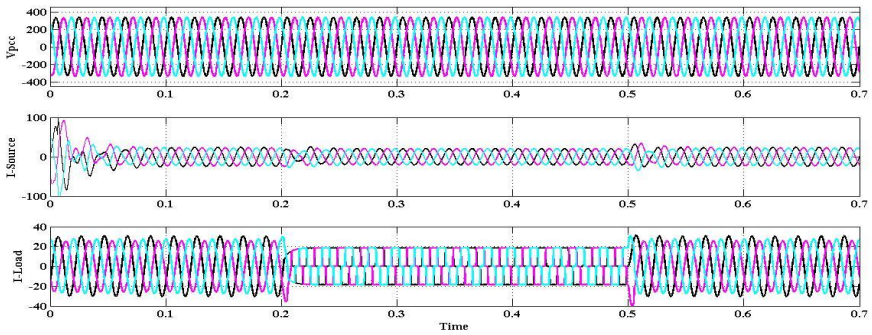


Fig 6.36 Three phase voltage at PCC (Vpcc), line currents from source (I-source) and line currents to load (I-load) respectively

The line currents are almost sinusoidal waveforms, while the load side current is highly reactive and having harmonic content above the IEEE-519 standard limit. The DC terminal voltage, AC terminal voltages and the compensating current generated from the DSTATCOM is shown in Fig 6.37.

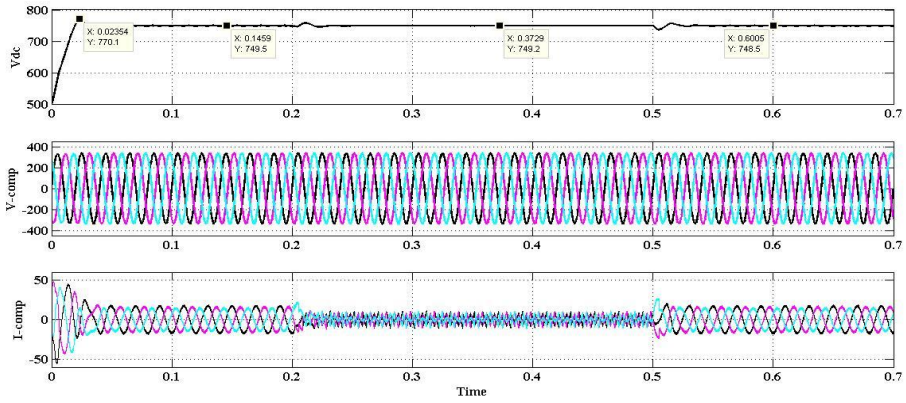


Fig 6.37 DC terminal voltage, three phase AC terminal voltage and Compensating current generated from DSTATCOM respectively

The FFT analysis of each phase source current is performed and the results are shown in Fig 6.38 (a, b & c) respectively. The FFT analysis result shows the THD content of the waveform and it can be seen that the THD content in line currents at source side is well below the IEEE standards.

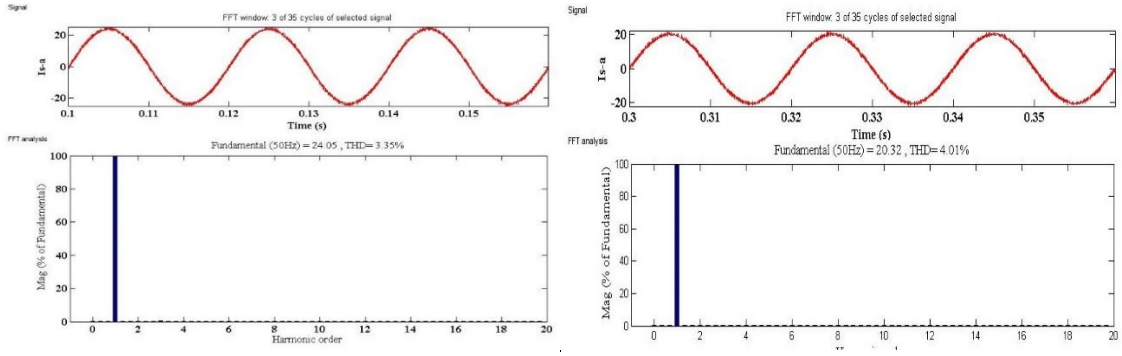


Fig 6.38 (a) THD of the line current of phase-*a* at time *t* = 0.1 sec and at *t* = 0.3 sec respectively

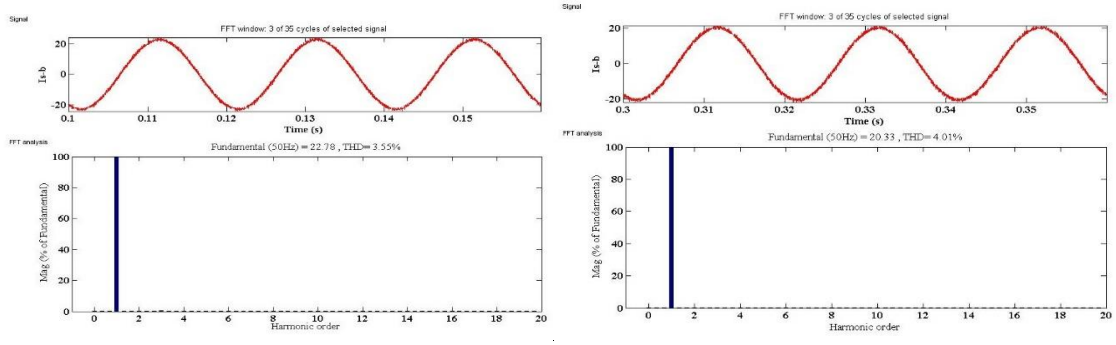


Fig 6.38 (b) THD of the line current of phase-*b* at time *t* = 0.1 sec and at *t* = 0.3 sec respectively

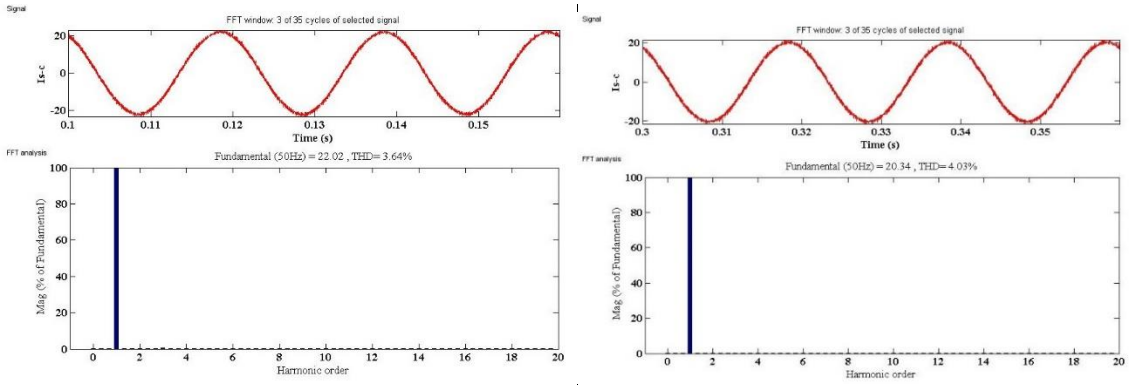


Fig 6.38 (c) THD of the line current of phase-*c* at time *t* = 0.1 sec and at *t* = 0.3 sec respectively

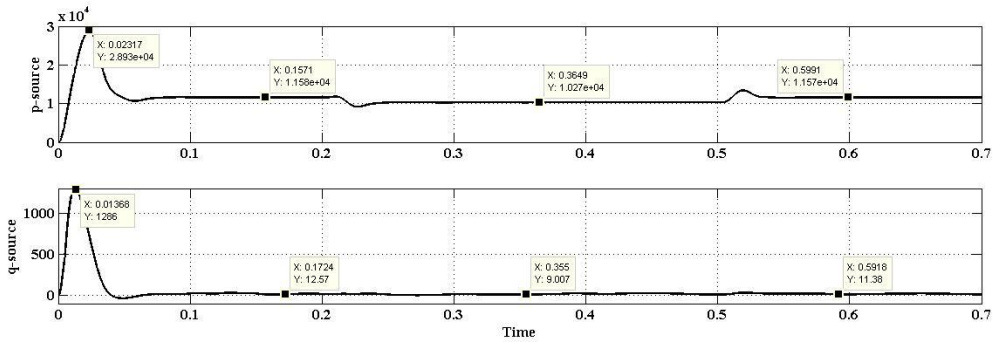


Fig 6.39 (a) Instantaneous active and reactive powers from source respectively

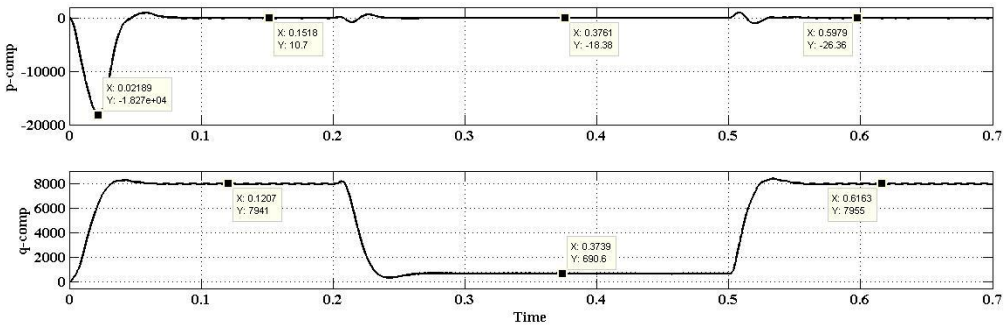


Fig 6.39 (b) Instantaneous active and reactive powers from D-STATCOM respectively

From instantaneous powers shown in Fig 6.39 (a, b & c) it can be seen that the power factor of the source side is improved to almost unity, while at load side it is equal to 0.8 lagging at time t = 0.1 sec and at time t = 0.3 sec (i.e. non-linear load connected to the system) the power factor of the load is 0.9 lagging. So the requirement at the time of non-linear load is only to minimize the harmonics.

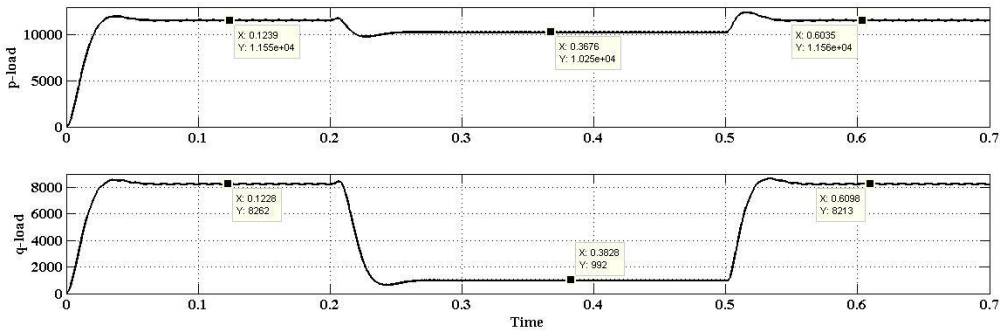


Fig 6.39 (c) Instantaneous active and reactive powers to load respectively

All different controller and their results have been shown in this chapter. Also it has been seen from the results that the D-STATCOM is able to minimize the harmonics from the source current waveform, while maintaining the sinusoidal nature of the PCC voltage and the power factor of the system at source is seen to be almost unity. The sinusoidal balanced currents and voltages are the key to a stable, and efficient system. Table 6.2 (a & b) is listing the magnitude of the source currents and total harmonic distortion percentage during different control schemes.

Table 6.2 (a) List of THD % and Magnitude of current in line currents during linear+unbalanced load

	SRF theory	**Fryze Algorithm**	**PI-like FLC**	**PI Gain Scheduled FLC**	**Hybrid Fuzzy-PI**	**ANFIS**
THD (%) and magnitude of current in phase-a	3.27%; 24.39A,	4.73%; 25.07A,	3.32%; 24.07A,	3.8%; 24.05A,	3.65%; 23.97A,	3.35%; 24.05A,
THD (%) and magnitude of current in phase-b	23.02A, 3.50%;	22.4A, 5.29%;	22.75A, 3.50%;	22.8A, 4.00%;	22.77A, 3.83%;	22.78A, 3.55%;
THD (%) and magnitude of current in phase-c	22.32A, 3.63%;	22A, 5.09%;	22.03A, 3.55%;	22.02A, 4.19%;	21.93A, 3.94%;	22.02A, 3.64%;

Table 6.2 (b) List of THD % and Magnitude of current in line currents during Non-linear load

	SRF theory	**Fryze Algorithm**	**PI-like FLC**	**PI Gain Scheduled FLC**	**Hybrid Fuzzy-PI**	**ANFIS**
THD (%) and magnitude of current in phase-a	20.48 A, 4.69%	20.53A, 6.04%	20.3A, 4.08%	20.33A, 4.61%	20.32A, 4.06%	20.32A, 4.01%
THD (%) and magnitude of current in phase-b	20.48A, 4.81%	20.51A, 5.85%	20.32A, 4.08%	20.33A, 4.50%	20.33A, 3.99%	20.33A, 4.01%
THD (%) and magnitude of current in phase-c	20.48A, 4.76%	20.49A, 5.88%	20.32A, 4.04%	20.33A, 4.58%	20.33A, 4.07%	20.34A, 4.03%

Table 6.3 (a) Instantaneous active and Reactive powers magnitude during linear+unbalanced load

	SRF theory	**Fryze Algorithm**	**PI-like FLC**	**PI Gain Scheduled FLC**	**Hybrid Fuzzy-PI**	**ANFIS**
Instantaneous Power (Active and reactive) load demand	11680W; 8177VAr	11660W; 8172VAr	11530W; 8228VAr	11560W; 8261VAr	11540W; 8227VAr	11550W; 8262VAr
Instantaneous Power (Active and reactive) Source side	11670W; 45.42VAr	11960W; 173.3VAr	11580W; 23.69VAr	11580W; 18.4VAr	11570W; 19.22VAr	11580W; 12.57VAr
Instantaneous Power (Active and reactive) at DSTATCOM	-53.72W; 8148VAr	-187.7W; 7792VAr	-30.51W; 7938VAr	-48.69W; 7931VAr	-15.03W; 7926VAr	-10.7W; 7941VAr

Table 6.3 (b) Instantaneous active and Reactive powers magnitude during Non-linear load

	SRF theory	**Fryze Algorithm**	**PI-like FLC**	**PI Gain Scheduled FLC**	**Hybrid Fuzzy-PI**	**ANFIS**
Instantaneous Power (Active and reactive) load demand	10330W; 464.8VAr	10340W; 455.2 VAr	10250W; 990.4 VAr	10250W; 988.2 VAr	10250W; 988.5 VAr	10250W; 992 VAr
Instantaneous Power (Active and reactive) Source side	10350 W; 10.76VAr	10360W; 6.405 VAr	10270W; 18.88 VAr	10270W; 18.7 VAr	10280W; 9.988VAr	10270W; 9.007VAr
Instantaneous Power (Active and reactive) at DSTATCOM	-16.39W; 462.9VAr	-15.53W; 204VAr	-23.1 W; 699VAr	-19.64W; 695.1VAr	21.99 W; 713.9VAr	-18.38W; 690.6VAr

Table 6.3 (a & b) is listing all the instantaneous powers (active and reactive) at various points of the system like load end, source end and at D-STATCOM.

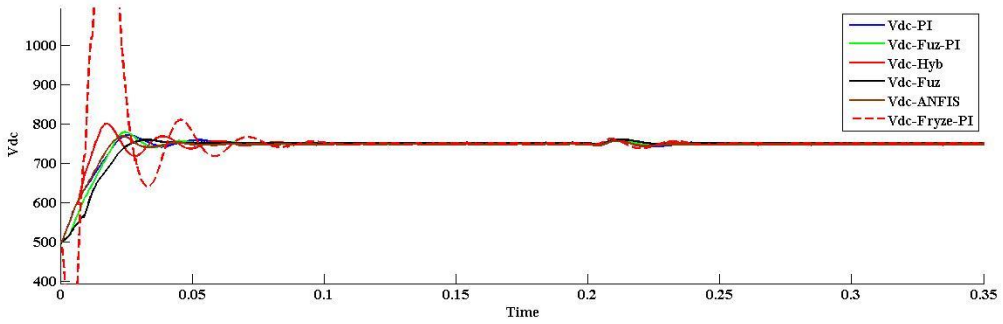


Fig 6.40 (a) DC terminal voltage waveform due to different control schemes

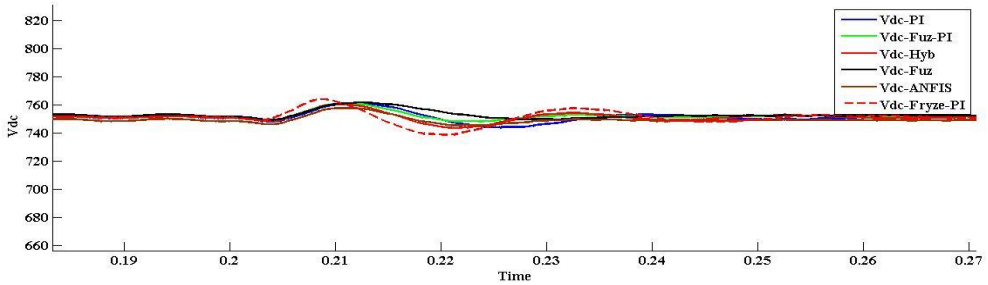


Fig 6.40 (b) DC terminal voltage at t = 0.2 sec (insertion of non-linear load)

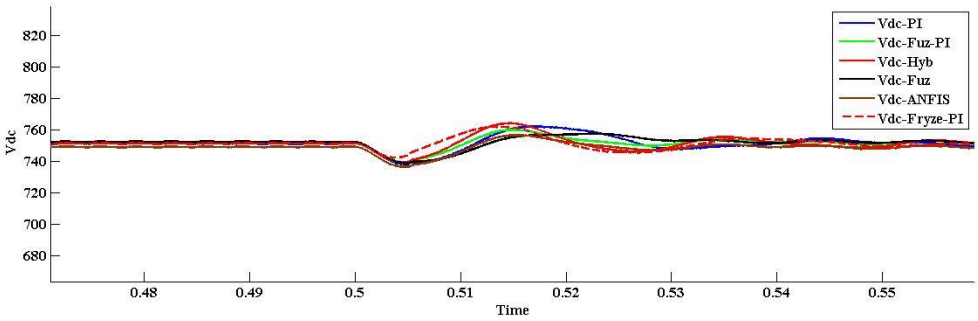


Fig 6.40 (c) DC terminal voltage at t = 0.5 sec (removal of non-linear load)

The DC terminal voltage, at the VSC, response due to different control schemes is compiled in single plot and different points (i.e. starting, insertion/removal of load) is shown in Fig 6.40 (a, b & c) respectively. The comparison of these results have been tabulated in Table 6.4 on various parameters like rise time, overshoot percentage, settling time and steady state error percentage.

Table 6.4 Comparison of DC terminal voltage response due to different controllers

	SRF-PI	Fryze-PI	PI-like FLC	PI gain Scheduling using FLC	Hybrid Fuzzy-PI	ANFIS Controller
Rise Time (sec)	0.0209	0.01	0.025	0.0209	0.014	0.019
Settling time (sec)	0.065	0.08	0.055	0.07	0.07	0.08
Overshoot % at (t = 0 sec)	3.04	93.78	1.6	4	6.667	2.667
Overshoot % at (t = 0.2)	1.533	1.933	1.6	1.6	1.467	1
Undershoot % at (t = 0.5 sec)	1.0667	1	1.4	1.4667	1.333	1.6266

CHAPTER 7

CONCLUSION AND FUTURE SCOPE

7.1 Conclusion

This work dealt with D-STATCOM, one of the FACTs devices to compensate for the loads requirement for reactive power and to eliminate harmonics at load end only. The working and controlling of the D-STATCOM is explained in this thesis. The results after compensation using D-STATCOM suggests that device is able to counter the harmonics generated from the load at load end, and it is able to maintain the sinusoidal nature of the source current with unity power factor operation The controlling of the D-STATCOM DC link voltage is done using PI controller, three different topologies of Fuzzy Logic controller and ANFIS algorithm based controller. The different control schemes have shown promising results for load compensation operation of D-STATCOM. The harmonic content of the source current in all the schemes is well below the standard limits of 5% mentioned in IEEE-519. The reactive power requirement and unbalancing in the load current is also been minimized at load end. Moreover, all the schemes work well under dynamics of load changes, and load unbalancing too.

7.2 Future Scope

1. There are many conventional control algorithms like IRPT, SRF etc. as well as many other adaptive filtering control algorithms cab be implemented. There are many adaptive filtering control algorithms such as normalized LMS sign algorithm, sign-sign LMS algorithm, variable step size LMS (VSLMS) algorithm, the leaky LMS algorithm, linearly constrained LMS algorithm, Kalman filtering algorithm, self-correcting adaptive filtering (SCAF), transform domain adaptive LMS filtering, recursive least-squares (RLS) algorithms, QR-RLS algorithms etc. can be implemented.

2. The proposed system is capable of harmonic compensation as well as reactive power compensation for the distribution system, but it is unable to transfer the active power to the distribution system, because there is no active power source at the DSTATCOM side. So one improvement can be in the system by making the system capable to transfer the active power in the distribution system by adding any real power source such as battery energy storage system (BESS) or renewable source (wind power system, solar power system etc.).

3. For maintaining the DC link voltage, the DC voltage regulator with PI-controller can be replaced by using controller based on artificial neural network (ANN), Particle swarm optimization (PSO) technique, Genetic Algorithm.

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APPENDIX

System specifications and circuit parameters

System voltage (V_{ac})	415 V (RMS L-L)	
System Frequency (f_s)	50 Hz	
Source Resistance (R_s)	0.1Ω	
Grid side Inductance (L_g)	0.09mH (Each Phase)	
Non Linear Load	3-φ diode bridge with 30Ω, 150mH on DC side	
Linear Load (Balanced)	10kVA, 0.8pf (lag)	
Linear Load (unbalanced)	Phase A	25Ω, 0.05H
	Phase B	44Ω, 0.08H
	Phase C	35Ω, 0.061H
Coupling inductor (L_c)	3.5mH (Each Phase)	
DC capacitor (C_{dc})	2500μF	
Ripple Filter	6.2Ω, 5μF	
Switching Frequency	10000 Hz	
k_p and k_i	0.9 and 75	
Hysteresis Band Limit (h)	0.2	

PUBLICATIONS

Published

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