IMPLEMENTATION OF ANALOG SIGNAL PROCESSING CIRCUITS USING INTEGRATED CIRCUIT OTA, LM13600

A

DISSERTATION
SUBMITTED IN PARTIAL FULFILLMENT OF THE
REQUIREMENTS
FOR THE AWARD OF THE DEGREE
OF

MASTER OF TECHNOLOGY
IN
CONTROL AND INSTRUMENTATION

Submitted by

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CANDIDATE'S DECLARATION

I, **Rahul Pal**, Roll No**. 2K13/C&I/11** student of M. Tech. (Control and Instrumentation), hereby declare that the dissertation/project titled **"IMPLEMENTATION OF ANALOG SIGNAL PROCESSING CIRCUITS USING INTEGRATED CIRCUIT OTA, LM13600"** under the supervision of **Dr. Pragati Kumar**, of Electrical Engineering Department, Delhi Technological University in partial fulfilment of the requirement for the award of the degree of Master of Technology has not been submitted elsewhere for the award of any Degree.

Place: Delhi
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This is to certify that the dissertation '**IMPLEMENTATION OF ANALOG SIGNAL PROCESSING CIRCUITS USING INTEGRATED CIRCUIT OTA, LM13600"** on Major Project-II being submitted by Rahul Pal (2K13/C&I/11) in partial fulfilment of the requirements for the degree of Master of Technology in control & instrumentation at D.T.U is an authentic record of the work carried out by him under my supervision and guidance.

Place: Delhi
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ACKNOWLEDGEMENT

I am thankful to the Almighty because without his blessing this work was not possible. It gives me a great pleasure to express my profound gratitude to my supervisor and project guide Dr. Pragati Kumar, Department of Electrical Engineering, Delhi Technological University (formerly Delhi College of Engineering), for his invaluable guidance, encouragement and patient reviews throughout the progress of this dissertation.

I would also like to express my heartfelt thanks to Dr. Madhusudan Singh, head of department and all faculty members of Department of Electrical Engineering, Delhi Technological University, for keeping the spirits high and clearing the vision to work on the project.

Finally, I am also thankful to my family and friends for their constant support and motivation during this work.

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ABSTRACT

Operational transconductance amplifiers, more popularly referred to as OTAs belong to a class of analog signal processing elements for which the output is a current rather than a voltage .OTAs have establish themselves as a very useful active building block because of certain features which are not present in the other signal processing blocks namely operational amplifiers. These features include availability of high output impedance terminals and variability of open loop gain. Operational transconductance amplifier can be used in a variety of applications such as voltage controlled amplifier (VCA), voltage controlled resistance (VCA), voltage controlled filters etc. In the present work many of these applications have been implemented using integrated circuit operational transconductance amplifier IC LM13600.This IC has two diodes linearized transconductance amplifier and two uncommitted Darlington transistors available on the chip which can be used as voltage buffers. These buffers can be used in conjunction with the OTA to realize other active building blocks also.

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List of symbols and abbreviations

Symbols	Description
I_c	Collector current
I_s	Reverse saturation current
V_e	Emitter voltage
V_b	Base voltage
V_{dd}	Source Supply Voltage
V_{be}	Base emitter voltage
I_e	Emitter current
V_T	Thermal Voltage
V_{bias}	Bias Voltage
I_{bias}	Bias Current
Q	Quality Factor
OTA	Operational transconductance amplifier
VCA	Voltage Controlled Amplifier
VCR	Voltage Controlled Resistor
VCGR	Voltage Controlled Grounded Resistor
VGFR	Voltage Controlled Floating Resistor
VCO	Voltage controlled Oscillator
VCF	Voltage Controlled Filter
BJT	Bipolar Junction Transistor
CMOS	Complementary Metal Oxide Semiconductor
FET	Field Effect Transistor
S&H	Sample and Hold circuit

Chapter 1

Introduction

1.1 Introduction

The present work deals with the application of integrated circuit operational transconductance amplifier IC LM13600. Operational transconductance amplifiers, more popularly referred to as OTAs belong to a class of analog signal processing elements for which the output is a current rather than a voltage .OTAs have establish themselves as a very useful active building block [1] because of certain features which are not present in the other signal processing blocks namely operational amplifiers. These features include availability of high output impedance terminals and variability of open loop gain.

Operational transconductance amplifier can be used in a variety of applications such as voltage controlled amplifier (VCA), voltage controlled resistance (VCA), voltage controlled filters etc. In the present work we have implemented many of these applications using integrated circuit operational transconductance amplifier IC LM13600.

Both bipolar as well as CMOS implementation of the OTAs [2] have been available in literature for quite some time but the popularity of this device has been mainly due to availability of this device in integrated circuit forms. It the following, we present the schematic and brief overview of the important features of classical OTA architecture.

1.2 An overview of OTA

Fig. 1.1 shows the symbol used to represent the operational transconductance amplifier. Since it is a transconductance amplifier, ideally it must offer infinite input impedance to any signal source which is connected to its input terminal and present infinite output at its output (which is current terminal). The ideal equivalent circuit thus can be represents as given in fig. 1.2

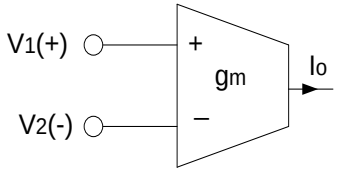

Fig 1.1: An OTA symbol

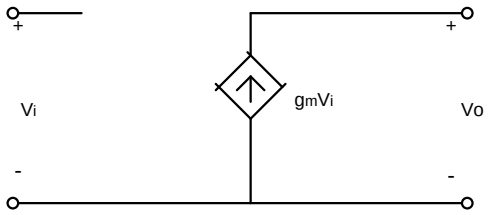

Fig 1.2 ideal equivalent circuit

The transconductance gain g_m unlike an OP-AMP is not a constant to be decided by the parameter of the transistor used in the architecture rather, it can be varied electronically by simply changing an external voltage current/ resistance. It is thus feature which has made the OTA very popular in applications like music synthesizer and voltage controlled filters, resisters and filters etc.

Characteristics of the ideal OTA:

a) Input impedance = ∞
b) Output impedance = ∞
c) Bandwidth = ∞
d) Transconductance is proportional to DC bias current

Real OTAs do not have all these architecture attributes. The equivalent circuit of a real OTA can be drawn as shown in fig. 1.3. An alternative symbol has also used to represent the OTA (mainly in industries). This symbol is given in fig.1.4

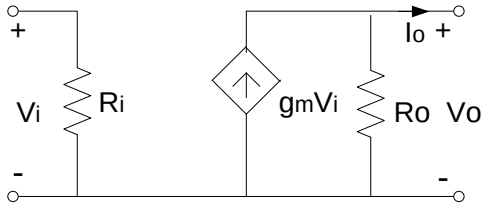

Fig. 1.3 equivalent circuit of real OTA

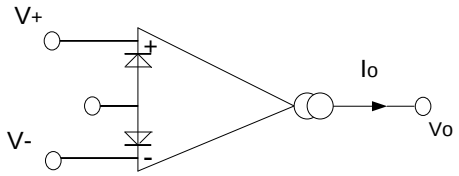

Fig. 1.4 An alternative symbol of OTA

1.3 Applications of OTA

There are many applications of Operational transconductance amplifiers (OTA) such as automatic gain control (AGC) amplifiers, active filters, and fast control loop amplifiers, control resistors, control filter, control oscillators, and control amplifiers for capacitive sensors and it can be also used for high-performance video applications. OTA has applications in electronics as well in electrical field. Some applications of OTA in electronics and electrical field, It can be seen in light emitting diode (LED) driver circuits for fiber optic transmissions, current-controlled oscillators, integrators for fast pulses, in power system analog emulation[3], and as a current mode gain boost amplifier[4]. Some Additional applications for operational transconductance amplifiers (OTA) include sample-and-hold circuits [5], timers, video and broadcast equipment multiplexers, high-speed data acquisition devices.

1.4 Outline of the work presented in dissertation

The work carried out in this dissertation has been organized as follows: chapter I consists of introduction of this dissertation and chapter II covers the review of architecture of the OTA, chapter III, we have presented the limitations of classical OTA and methods used to overcome these limitations this chapter also covers the experimental characterization of LM13600. In chapter IV, we have been covered implement voltage controlled amplifiers. Voltage controlled resistors, filters and oscillators have been covered in chapter V and VI. In chapter VII, we will discuss general application of LM13600. In the last chapter, the summary of the work carried out in this dissertation and scope for further work has been presented.

CHAPTER 2

Architecture of OTA

2.1 Introduction

In this chapter, we will present a generic OTA structure that is employed to make different types of OTA with bipolar, CMOS AND FET [2] [6] etc. For forming OTA, Differential pair is a basic element of OTA that will be discussed with transistor and MOSFET. Over a period of time, lot of improvisation has been done in OTA architecture. Some of them improvised OTA architecture will be presented in this chapter.

2.2 A generic OTA architecture

This generic OTA architecture is shown in fig. (2.1) here the collector / drain currents of the differential pair are subtracted using the current mirror networks A_1, A_2 and A_3 to give the output current:

$$I_O = I_{C2} - I_{C1} \tag{2.1}$$

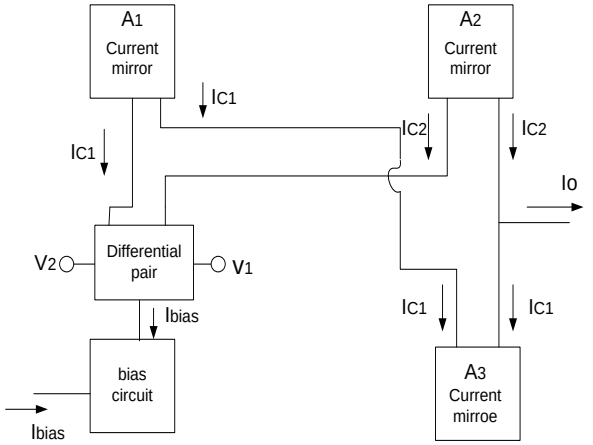

Fig.2.1 A basic OTA architecture

It is seen that from the above figure architecture that we need differential amplifier and current mirrors to realize an OTA into either bipolar or CMOS form. In the addition the bias architecture used for the differential pair is a transistor current source. In the following we will discuss the core of OTA i.e. the differential amplifier.

2.3 The differential pair

The bipolar and MOSFET differential pair will be discussed to achieve equation of output current and its depending parameters. Further we will see the difference between bipolar and CMOS differential output current.

2.3.1The bipolar differential pair

BJT Differential pair is the basic element of the Bipolar OTA. In the figure (2.2), assume the I_{EE} Biasing current is initially ideal and the effect of a finite output impedance of current source will be considered later. Assuming ideal transistors, currents are summed up at the common emitter node.

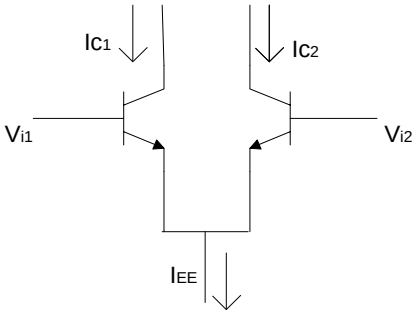

Fig 2.2: A Bipolar Differential Pair (with NPN transistors)

The current at common emitter node is represented by V_{EE}.

$$I_{EE} = I_{e1} + I_{e2} = \frac{I_{c1}}{\alpha_F} + \frac{I_{c2}}{\alpha_F} \tag{2.2}$$

Where, neglecting the early effect

$$I_{c1} = I_S e^{\frac{qV_{be1}}{kT}}, I_{c2} = I_S e^{\frac{qV_{be1}}{kT}} \tag{2.3}$$

Summing the voltages the base-emitter loop of the two transistors gives

$$-V_{i1+} + V_{be1} - V_{be2} + V_{i2} = 0 \tag{2.4}$$

$$V_{be1} - V_{be2} = V_{i1} - V_{i2} \equiv V_{id} \tag{2.5}$$

Where, V_{id} represents the difference of two inputs, the differential input voltage, the two collector currents are scaled,

$$\frac{I_{c1}}{I_{c2}} = e^{\frac{q(V_{be1} - V_{be2})}{kT}} = e^{\frac{qV_{id}}{kT}} \tag{2.6}$$

This combined with Eq. (2.2),

$$I_{c1} = \frac{\alpha_F I_{EE}}{1+e^{-\frac{qV_{id}}{kT}}}, I_{c2} = \frac{\alpha_F I_{EE}}{1+e^{\frac{qV_{id}}{kT}}} \tag{2.7}$$

The collector current is a function of differential input voltage and V_{id} is equal to $\frac{4kT}{q}$ that is approximately 100mv at room temperature. On transistor is off and second transistor is off essentially, then full bias current. The differential output current,

$$I_o = I_{c1} - I_{c2} \tag{2.8}$$

$$I_o = \alpha_F I_{EE}\left(\frac{1}{1+e^{-\frac{qV_{id}}{kT}}} - \frac{1}{1+e^{\frac{qV_{id}}{kT}}}\right) \tag{2.9}$$

It is to be manipulated to be expressed in the following form:

$$I_O = \alpha_F I_{EE} tanh\frac{qV_{id}}{kT} \tag{2.10}$$

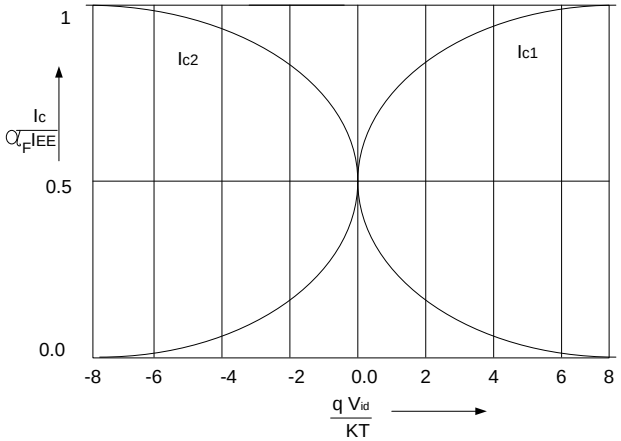

Fig.2.3 Collector current as a function of differential input voltage for the bipolar differential pair

The Slop of the $I_o - V_{id}$ represents the differential transconductance,

$$g_m = \frac{dI_o}{dV_{id}} = \frac{q\alpha_F I_{EE}}{2kT} sech^2\left(\frac{qV_{id}}{2kT}\right) \quad (2.11)$$

It is maximum at V_{id} near zero:

$$\frac{dI_o}{dV_{id}} = \frac{q\alpha_F I_{EE}}{2kT} = \frac{qI_c}{kT} = g_m \quad (2.12)$$

The maximum differential transconductance of the differential pair is equal to the transconductance of the transistor. Where I_c is collector current of either transistor.

2.3.2The MOS Differential Pair

An OTA could also be implemented in CMOS technology by replacing the current mirrors and the input differential pair with their MOS equivalents [2]. Assuming ideal current mirrors and current sources, the only difference is the switch to a MOS differential pair.

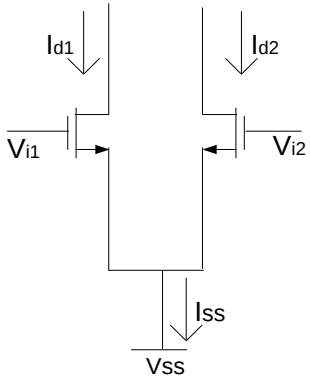

Fig 2.4: A MOS Differential Pair

In the MOSFET differential pair, summing the currents at the common source node,

$$I_{SS} = I_{S1} + I_{S2} = I_{d1} + I_{d2} \quad (2.13)$$

They are working in saturation region, assuming identical MOS and neglecting channel length modulation,

$$I_{d1} = \frac{\mu_n C'_{ox}}{2}\left(\frac{W}{L}\right)\left(V_{gs1} - V_{TH}\right)^2 \ , \ I_{d2} = \frac{\mu_n C'_{ox}}{2}\left(\frac{W}{L}\right)\left(V_{gs2} - V_{TH}\right)^2 \quad (2.14)$$

The voltage around the gate source loops,

$$V_{id} = V_{gs1} - V_{gs2} = V_{i1} - V_{i2} \quad (2.15)$$

Using equation (2.13)

$$V_{id} = \sqrt{\frac{I_{d1}}{\frac{\mu_n C'_{ox}}{2}\left(\frac{W}{L}\right)}} - \sqrt{\frac{I_{d2}}{\frac{\mu_n C'_{ox}}{2}\left(\frac{W}{L}\right)}} \tag{2.16}$$

Combining equation (2.13) and (2.14) and giving drain current as a function of differential input voltage,

$$I_{d1} = \frac{I_{SS}}{2} + \frac{\mu_{nC'_{ox}}}{4}\left(\frac{W}{L}\right) V_{id}\sqrt{\frac{4I_{SS}}{\mu_{nC'_{ox}}\left(\frac{W}{L}\right)} - V_{id}^2} \tag{2.17}$$

$$I_{d2} = \frac{I_{SS}}{2} - \frac{\mu_{nC'_{ox}}}{4}\left(\frac{W}{L}\right) V_{id}\sqrt{\frac{4I_{SS}}{\mu_{nC'_{ox}}\left(\frac{W}{L}\right)} - V_{id}^2} \tag{2.18}$$

Under the conditions when the differential voltage is too large only one of the transistors will be conducting and the maximum drain current that can flow through it is I_{SS} as one MOS is off and other is working with full bias current. Using equation (2.15), the range of V_{id} for which equation (2.17) and (2.18) is valid.

$$-\sqrt{\frac{I_{SS}}{\frac{\mu_n C'_{ox}}{2}\left(\frac{W}{L}\right)}} < V_{id} < \sqrt{\frac{I_{SS}}{\frac{\mu_n C'_{ox}}{2}\left(\frac{W}{L}\right)}} \tag{2.19}$$

The input range of the MOSFET differential pair depends on device geometry as well as bias current. Typically, the input range of MOSFET is form 1 to 3 V. taking the differential output current is,

$$I_0 = I_{d1} - I_{d2} \tag{2.20}$$

$$I_o = \frac{\mu_{nC'_{ox}}}{2}\left(\frac{W}{L}\right) V_{id}\sqrt{\frac{4I_{SS}}{\mu_{nC'_{ox}}\left(\frac{W}{L}\right)} - V_{id}^2} \tag{2.21}$$

The output current is as a function of the differential input voltage, the transconductance of the MOSFET pair is

$$g_m = \frac{dI_o}{dV_{id}} = \frac{\mu_{nC'_{ox}}}{2}\left(\frac{W}{L}\right)\sqrt{\frac{4I_{SS}}{\mu_{nC'_{ox}}\left(\frac{W}{L}\right)} - V_{id}^2}\left[1 - \frac{V_{id}^2}{\frac{4I_{SS}}{\mu_{nC'_{ox}}\left(\frac{W}{L}\right)} - V_{id}^2}\right] \tag{2.22}$$

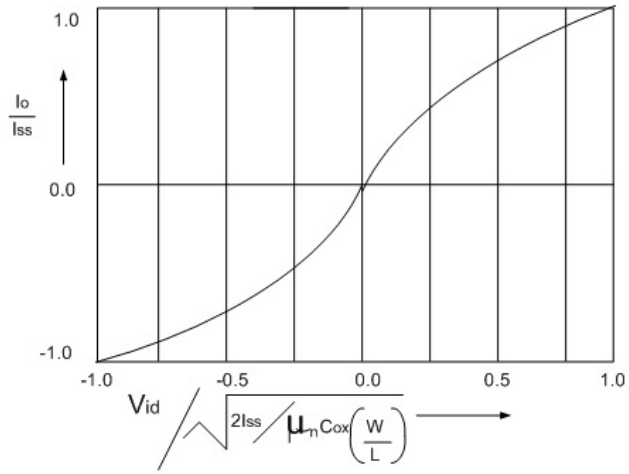

Fig. 2.5 Output current as a function of differential input voltage for a MOSFET differential pair.

It is maximum at V_{id} near zero:

$$g_m = \frac{dI_o}{dV_{id}} = \sqrt{\frac{I_{SS}}{\mu_n C'_{ox}\left(\frac{W}{L}\right)}} \tag{2.23}$$

The maximum differential transconductance of the MOSFET differential pair is equal to the quiescent transconductance of the transistor.

2.4 The complete OTA

Figure 2.6 shows the circuit diagram of a bipolar OTA [2] in which output current is proportional to the difference in input voltage. At the input stage is a differential pair with current source for loads. The output stages consist of a complementary pair of current source driven by input stage. The collector current in the differential pair transistor Q_2 provides the reference current for the PNP current source Q_7 and Q_8, whereas the collector current in the current source transistor Q_4provides the reference current for the NPN current source Q_9 and Q_{10} at the output.

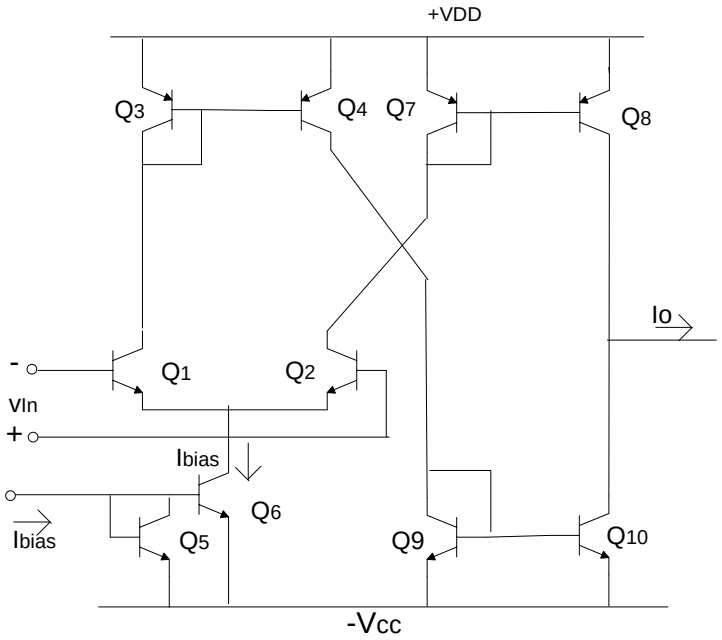

Fig. 2.6 A bipolar OTA architecture

2.5 The MOS OTA

This architecture is commonly used i.e. CMOS OTA [6]. Transconductance of this OTA (g_m) is a function of the amplifier bias current, for the case of OTAs using CMOS transistors in saturation. The transconductance g_m are proportional to $\sqrt{I_{abc}}$ for CMOS transistors operating in weak inversion. For the bipolar transistors, the transconductance g_m is directly proportional to I_{abc}. Ideally it is observed that it is OTA has infinite input and output resistance.

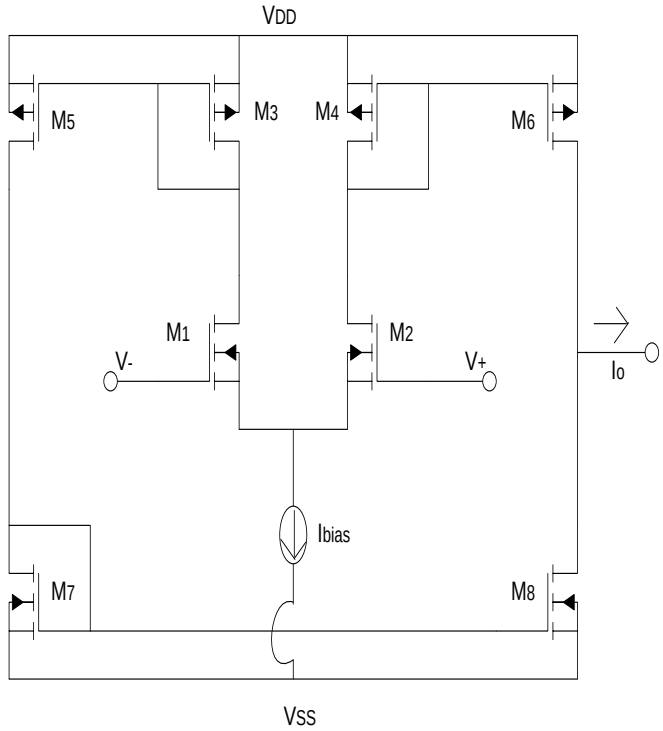

Fig. 2.7 A MOS OTA architecture

2.6 Recent development in OTA architecture

Over a period of time, lot of development has been done in OTA architecture. These improvisations are done to improve characteristics of OTA in terms of frequency, differential input range and temperature. Some of them advance OTA architectures are described below.

2.6.1 A fully differential digital programmable OTA

This fully differential digital programmable OTA [7] is ranging over three decades of dynamic range, which is intentionally designed for acoustic and sonar analog signal processing applications. This type of application requires design of operational transconductance amplifiers (OTAs) that can be configured over wide frequency range in multiple bands and achieve low power consumption and low harmonic distortion.

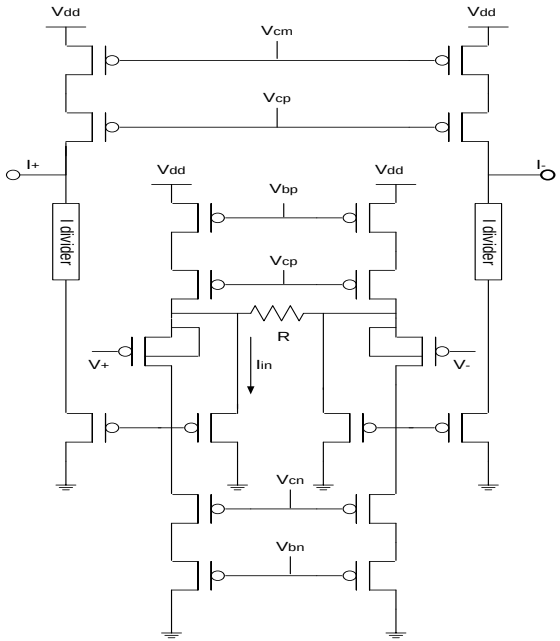

Fig 2.8(a): Fully differential digitally programmable OTA.

2.6.2 A low voltage wide-input range bulk-input CMOS OTA

This OTA architecture is using a novel bulk-input differential pair [8] without the use of a tail current source that still Good CMRR is achieved by using the gate terminal to control the total current in the differential pair, via the use of a dummy pair. This OTA also exhibits a wide differential input range and good g_m tune-ability.

The differential pair of this OTA is having a large linear input range due to its intrinsically low transconductance value, thus it is suitable to a wide range of current mode analog signal processing techniques, where a low input bias current can be tolerated as for example in filtering applications.

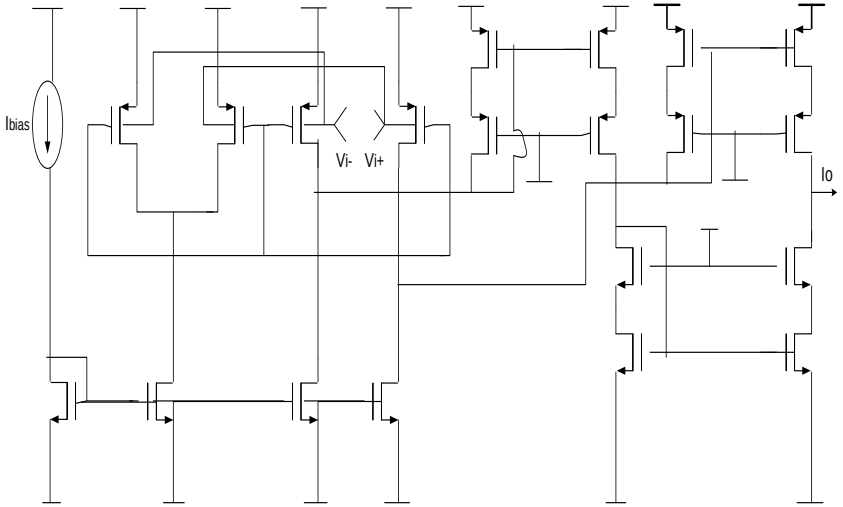

Fig 2.8(b): Complete bulk-input OTA.

2.6.3 A highly linear pseudo-differential transconductance

This is a pseudo differential, fully balanced fully [9], symmetric CMOS Operational Transconductance Amplifier (OTA). It is having inherent common mode detection which exhibits a very linear behaviour at frequency around 10.7MHz. Output is linearized through a proposed feedback circuit while keeping the output voltage controllable. This OTA structure (Linearized pseudo-differential fully symmetric OTA) is capable of extracting its input DC voltage information in a very linear manner.

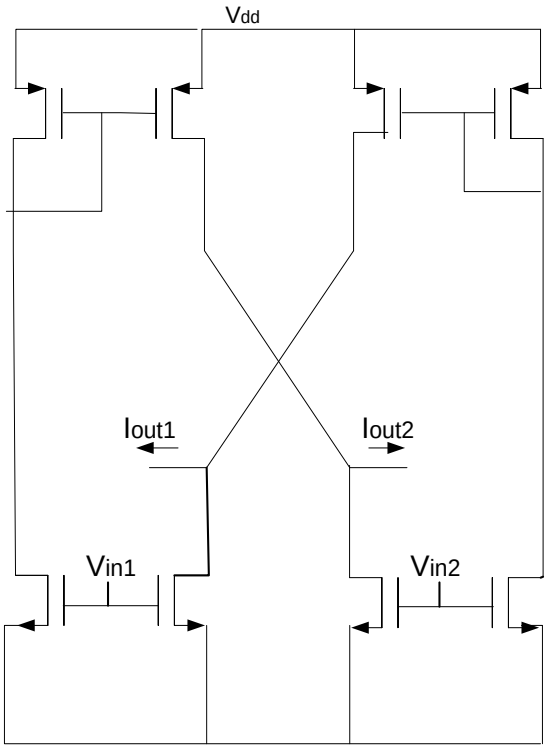

Fig 2.8(c): PD OTA with differential output current

2.6.4 A low voltage wide g_m adjustable range highly linear BiCMOS OTA

A low distortion low-voltage BiCMOS OTA wide g_m adjustment [10] range is shown in figure 2.8(d), it is having large input range and it has advantage of both linear and reciprocal linearg_m can be controlled. It is based on gain programmable current mirrors which are linear and continuously adjustable. This proposed circuit is overcome some of the practical limitations of other low voltage linear OTA structure and to provide increased versatility to the OTA as a building block for analog VLSI system.

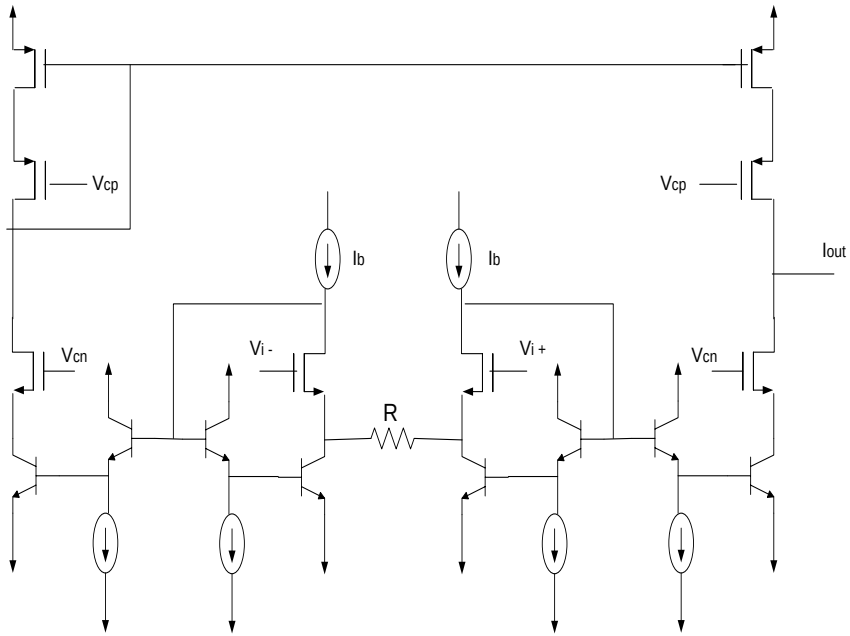

Fig 2.8(d): Wide g_m adjustable BiCMOS OTA

2.6.5 Folded cascode OTA

This folded cascade OTA [11] is shown in Figure 2.8(e). The folded cascode amplifier compromises between the two-stage amplifier and the telescopic cascode amplifier. It allows low supply voltage, but having a rather high output voltage swing and the input and output common mode levels is designed to be equal. Gain of this OTA is compared to the two-stage amplifier OTA and its speed is lower than for the telescopic cascode OTA that makes it a good compromise between these two amplifiers.

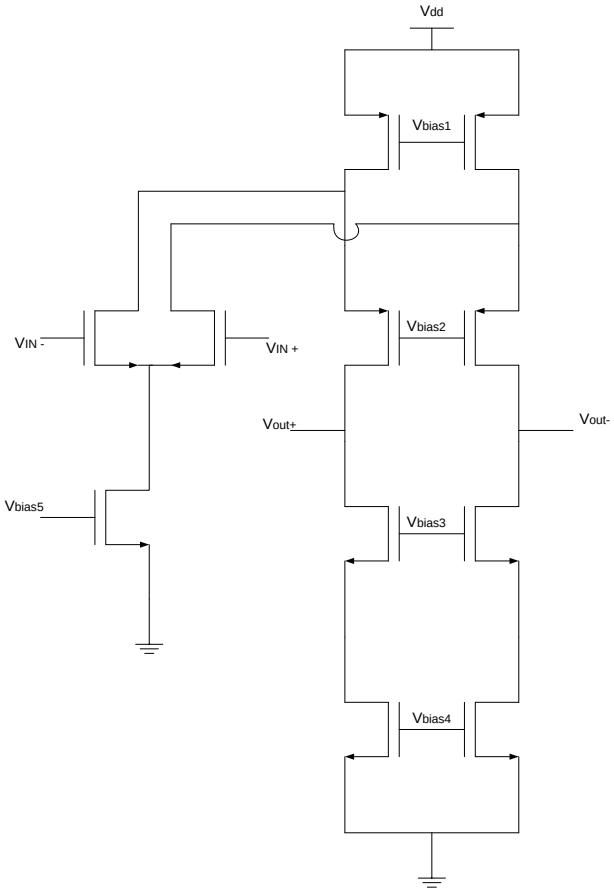

Fig.2.8 (e) Folded cascode amplifier

2.7 Conclusion

In this chapter we have presented the generic architecture of the OTA. We have also developed the defining equations of the transfer characteristics of differential amplifier (Both bipolar as well CMOS). A brief review of some of the recent development in the architecture of OTA has also been presented.

Chapter 3

Architecture and experimental characterization of LM13600

3.1 Introduction

In the last chapter a brief review of the general architecture of both bipolar as well as CMOS OTAs was presented. In the present chapter, one of the major limitations of the OTA architecture, namely its very small input range, will be discussed. We will also present the general methods [2] [12] used for increasing the linear range of a differential pair and how this method has been employed to increase the input linear range in LM13600. A complete experimental characterization of this IC OTA has been presented.

3.2 Limitation of the classical OTA

The transfer characteristics of the bipolar differential pair are given in equation (2.10) and fig. (2.3) are reproduced below:

$$I_O = \alpha_F I_{EE} tanh \frac{qV_{id}}{2kV_T} \tag{3.1}$$

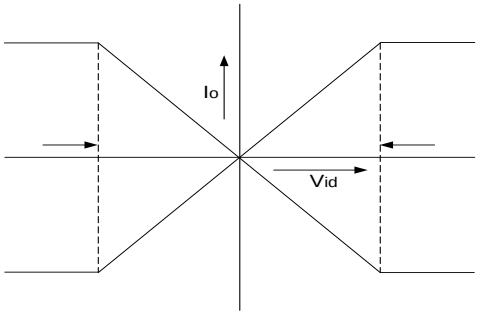

Fig.3.1 Transfer characteristic of bipolar OTA

From the above equation it is observed that for $V_{id} \ll \frac{2kT}{q}$ the $tanh$ non-linearity can be approximated by a simple linear term given by $\frac{V_{id}}{2V_T}$ thus $I_O = \alpha_F I_{EE} \frac{qV_{id}}{2kV_T}$. It is observed from the above figure that the input linear range is limited to:

$$-\frac{2kT}{q} < V_{id} < \frac{2kT}{q} \tag{3.2}$$

3.3 Methods of linearization

There are several methods used to linearize the bipolar differential OTA, some of them are described below. By using these methods, the input linear range can be extended up to certain limit and can be used for small signals. These methods are diode linearization and emitter degeneration.

3.3.1 Diode linearization

The origin of the non-linearity in the characteristic is the exponential relationship between the collector and the base emitter voltage of the input transistor. The non-linearity can be off-set if we pre-distort the input voltage by an inverse tanh non-linearity. This concept is utilized in analog multipliers also. Let us consider the relationship between the voltage and current of a conducting OTA given as:

$$I_D = I_S e^{\frac{V_D}{V_T}} \tag{3.3}$$

By simplifying,

$$V_D = V_T ln \frac{I_D}{I_S} \tag{3.4}$$

If the input voltage to the differential input stage of the OTA is applied through the diodes then the tanh non-linearity introduce by the differential pair will be cancelled out. In addition we will get rid of the temperature dependent term, let us quantitatively establish this effect.

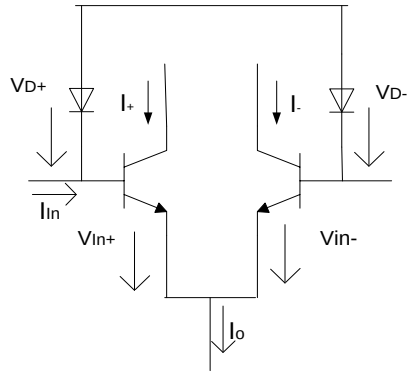

Fig 3.2: Principle of Input Diode Linearization

Now we are going to apply KVL in the base-emitter diodes of the differential pair.

$$V_{D+} + V_{In+} = V_{D-} + V_{in-} \tag{3.5}$$

Reordering it and expressing in terms of current,

$$V_T ln\ \frac{I_+}{I_{S+}} - V_T ln\ \frac{I_-}{I_{S-}} = V_T ln\ \frac{I_{D-}}{I_{D,S-}} - V_T ln\ \frac{I_{D+}}{I_{D,S+}} \tag{3.6}$$

When transistor are matched then saturation current are same and we get simplified form,

$$V_T ln\ \frac{I_+}{I_-} = V_T ln\ \frac{I_{D-}}{I_{D+}} \tag{3.7}$$

The current ratio must be equal to

$$\frac{I_+}{I_-} = \frac{I_{D-}}{I_{D+}} \tag{3.8}$$

And now,

$$I_D = I_{D-} + I_{D+} \tag{3.9}$$

$$I_{In} = I_{D-} - I_{D+} \tag{3.10}$$

Again assumes $\beta \gg 1$, then we can rewrite the equations,

$$I_+ = \frac{1}{2}(I_{O-} + I_{out}) \tag{3.11}$$

$$I_- = \frac{1}{2}(I_{O-} - I_{out}) \tag{3.12}$$

$$I_{D+} = \frac{1}{2}(I_D - I_{In}) \tag{3.13}$$

$$I_{D-} = \frac{1}{2}(I_D + I_{In}) \tag{3.14}$$

And further simplify and arrive at

$$I_{out} = \frac{I_O}{I_D}\ I_{In} \quad \text{Where, } |I_{In}| < I_D \tag{3.15}$$

Observing the last equation we get that we have achieved a current amplifier rather than a transconductance amplifier because the independent variable is a current instead of a voltage. The temperature dependence of the transconductance is compensated in the positive side. Of course we can use a resistor at each input to convert voltage into current

and it is restriction or condition here that the maximum input current should not exceed the diode bias current at the maximum input voltage. It is also observed that the maximum transconductance is achieved for dying out diode biasing. While it comes that transconductance can be made infinitely large, this is not the case when the input range is also zero at that point. We know that for dying out diode bias current the OTA returns to its non-linearized form.

When driven by voltage signals, resistors can be used to provide voltage to current conversion (the potential at the bases of the input transistors is almost constant). With equal input resistors the transconductance becomes

$$I_{out} = \frac{I_O}{R_{In} I_D}\ I_{In} \quad \text{Where, } |I_{In}| < R_{In} I_D \tag{3.16}$$

Now we observed that compensating for temperature is not easy and it is depending on how you generate the currents for the tail and diodes. It clips the signal by Overdriving a linearized OTA at the input terminal. If any changes occur in the input potential that are effected by changes in I_0 or I_D that produce common mode inputs and it can be suppressed at the output if the common mode input range is not exceeded.

3.3.2 Emitter degeneration

Linearization can also be done by placing resistor in emitter of differential pair, two forms of emitter degeneration are shown in fig.3.3 (a) and 3.3 (b).

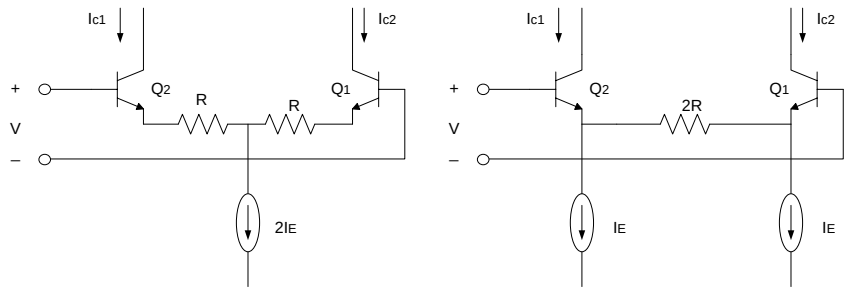

Fig.3.3 (a) and 3.3(b) two forms of linearization of emitter degeneration

Applying the KVL around the base emitter loop,

$$V = V_{be1} + RI_{c1} - RI_{c2} - V_{be2} \tag{3.17}$$

If $I_E R \gg \frac{kT}{q}$, then Base current is neglected so that base emitter voltage of both transistors are equal, then $I_{c1} - I_{c2} = \frac{V}{R}$ also $I_{c1} + I_{c2} = 2I_E$, recombining these two relations with eq.(3.15)

$$I_{c1} = \left(1 + \frac{V}{2I_E R}\right) I_E \ = (1 + x) I_E \tag{3.18}$$

$$I_{c2} = \left(1 - \frac{V}{2I_E R}\right) I_E \ = (1 - x) I_E \tag{3.19}$$

Where, $x = \frac{V}{2I_E R}$

The second form of emitter degeneration as shown in fig. 3.3(b) is giving the same result. However, input voltage range of this is about $2V_{be}$ but it lower than first form emitter degenerative.

3.4 Bipolar OTA with enhanced linear range

LM13600 is a bipolar OTA manufactured by National semiconductor. It is an OTA IC in which the diode linearization method discussed in 3.3.1 has been used to enhance the input linear range. The complete circuit diagram of the linearized OTA [2] is given below in fig (3.4).

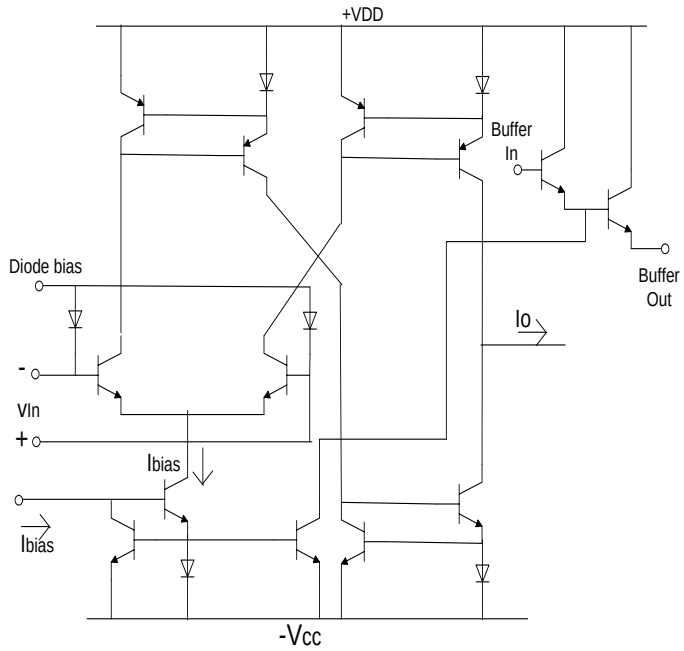

Fig.3.4 Circuit diagram of linearized OTA

LM13600 contains an on-chip Darlington pair which can be used as a voltage buffer. This feature makes the IC more useful as the loading effect of the output of the OTA is reduced to a very large extent because of the very high input impedance of the voltage buffer.

3.5 Characterization of LM13600

LM13600 is a Dual-in-line and small outline DIP IC package [12], in which two linearized OTAs are packaged. Its pin diagram and circuit symbol as given in data sheet of LM13600 are given below.

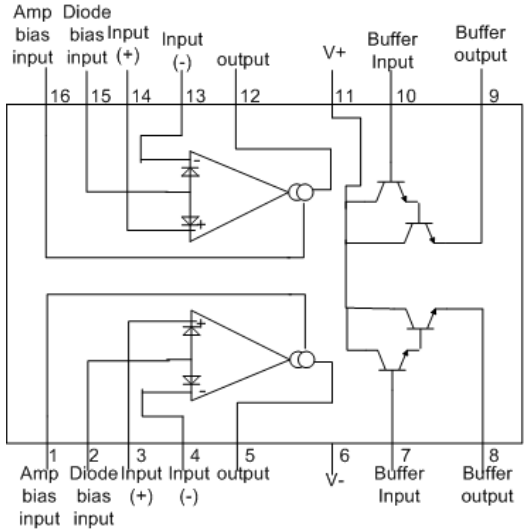

Fig.3.5 Pin diagram of LM13600 includes circuit symbol.

This type of diode linearization concept is used in many commercial transconductance amplifiers. In this amplifier, transconductance g_m is adjustable over six decades with bias current and range of bias current is 0.1uA to 1mA. It provides good linearity with this range. If we talk about open loop bandwidth i.e. 2 MHz and a unity gain compensated slew rate i.e. 50V/us. Darlington buffer is also included in LM13600 as an optional.

3.5.1 Determination of linear range of OTA (LM13600) without diode linearization

It is necessary to find out input linear range of any device. The operational transconductance amplifier has certain input limits. If the input is given beyond this range, distortion will occur. It is because of nonlinearity and then output will not be appropriate. It can be realized practically in OTA, how long transconductance of OTA can stay constant to certain differential input limits because transconductance is constant or fixed for fixed bias current. OTA shows linearity as long as transconductance of OTA is constant for certain input limits. There is linear relationship between input and output which is true for certain input range. A circuit is designed to find out input linear range as shown in figure (3.6).

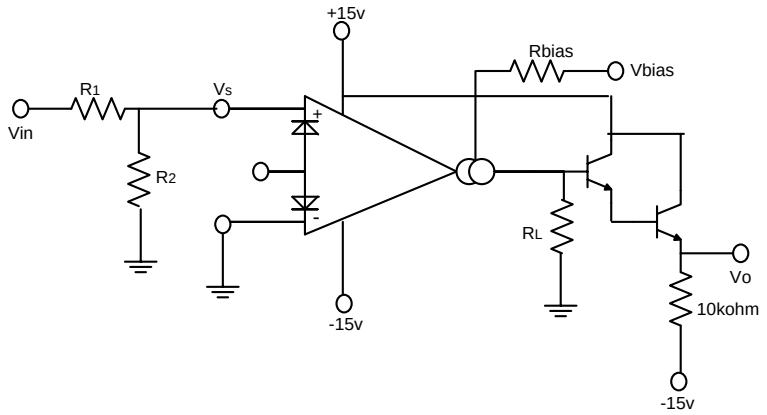

Fig 3.6: voltage control amplifier without diode linearization

This is a basically voltage control amplifier that is designed to find out linear range of OTA (LM13600). As we know that it is controlled by the bias current and the bias current is generated by applying bias voltage and placing bias resistance at amp bias node. The differential input voltage is $(V_+ - V_-)$, the inverting terminal is kept at ground and input is fed to non-inverting terminal through voltage divider circuit. The Voltage divider circuit is used to attenuate the signal to few millivolts because practically, the signal of few millivolts is not possible to feed to input. The output current will be consumed by the load so that the output voltage will appear across applied load and load can be varied, this output is fed to Darlington circuit, and the Darlington circuit is a

current amplifier that provides unity gain and working as voltage buffer. Output before and after Darlington circuit is same but output after Darlington circuit will have DC shift of V = -1.4 volt.

$$g_m = \frac{I_C}{2V_T} \quad (3.20)$$

$$I_C = \frac{V_{CC}+1.4-V_{bias}}{R_{bias}} \quad (3.21)$$

$$I_o = g_m(V_+ - V_-) \quad (3.22)$$

$$V_o = I_o R_L \quad (3.23)$$

3.5.1.1 Experimental and simulation results

It is found that the input range of OTA (LM13600) without linearization is 60 mV_{P-P} because there is linear relationship between V_s and I_o up to 60 mV_{P-P} and transconductance is also constant up to this differential input value. It is found that input linear range is 60 V_{P-P}. Transfer characteristic of OTA is plotted for these values which are shown in table.3.1 (output current corresponding input voltage for non-linearized OTA). Where, $R_{L=}$ 10kΩ, $R_{bias=}$ 20kΩ, $V_{bias=}$ − 3.6v, g_m=10ms.

Table.3.1 (output current corresponding input voltage for non-linearized OTA)

S.NO.	INPUT VOLTAGE(V_s)	OUTPUT CURRENT(I_0)
1.	0mV	0ma
2.	6.23mV	0.067ma
3.	8.43mV	.092ma
4.	10.3mV	.115ma
5.	12.3mV	.135ma
6.	13.7mV	.155ma
7.	15.6mV	.177ma
8.	17.64mV	.205ma
9.	19.60mV	.269ma
10.	23.33mV	.310ma
11.	25.490mV	.330ma
12.	31.56mV	.370ma
13.	35.49mV	.410ma
14.	39.21mV	.413ma
15.	49.mV	.503ma
16.	58.82mV	0.508ma
17.	68.82mV	0.510ma

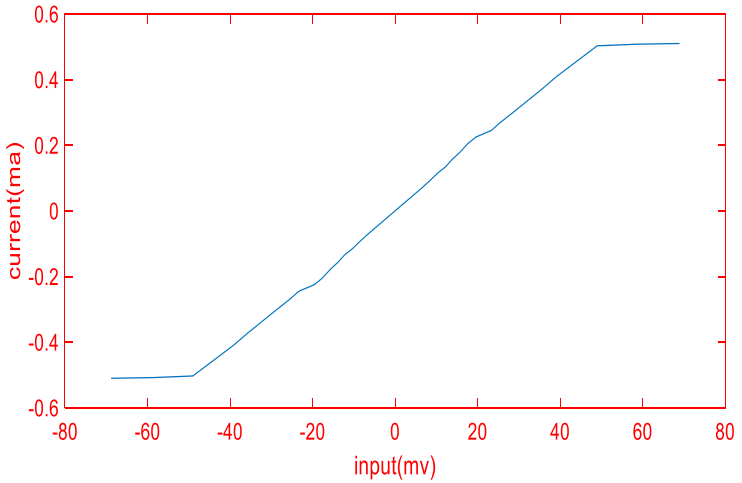

Fig 3.7(a): Transfer function of OTA (LM13600) without diode linearization (Experimental data)

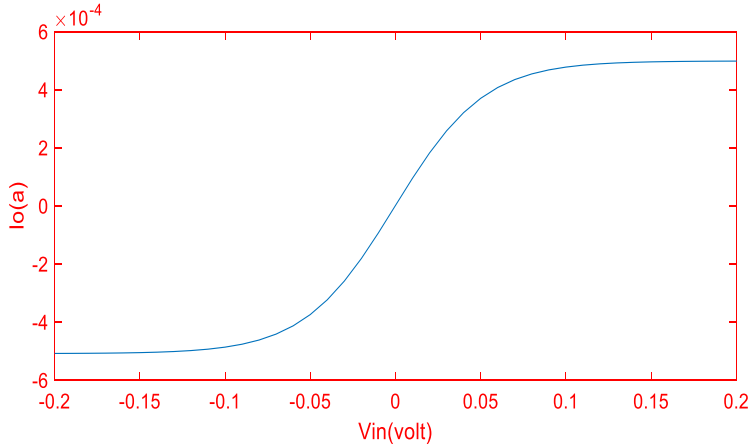

Fig 3.7(b): Transfer function of OTA (LM13600) without diode linearization (PSPICE)

3.5.2 Determination of linear range of OTA (LM13600) with diode linearization

The circuit below in fig (3.8) was used to determine the input linear range of the OTA when the linearizing diodes were used. We have used the same component values which were used in determining of the linear range without linearizing diodes. A value of R_D= 15kΩ was used. The following table gives the value of the input voltage and output current used to calculate the transconductance and the linear range.

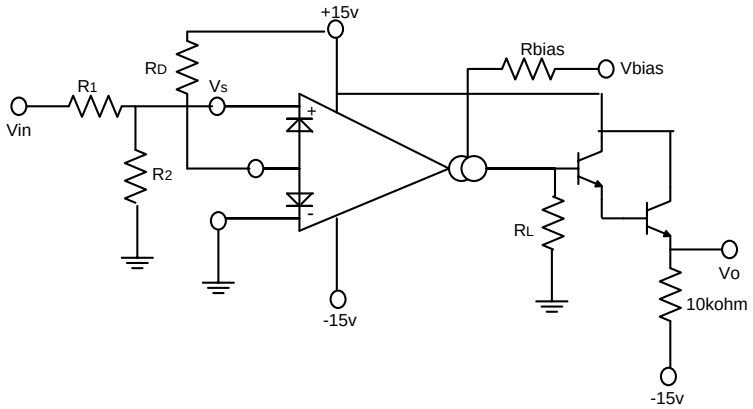

Fig 3.8: Voltage control amplifier with diode linearization

Fig (3.9) gives a plot of the output current as a function of the input voltage. The slope of this graph nearly constant between $V_i = \pm 500mv$.

3.5.2.1 Experimental and simulation results

It is found that the input range of OTA (LM13600) with linearization is 1 V_{P-P} because there is linear relationship between V_s and I_o up to 1 V_{P-P}. Transfer characteristic of OTA is plotted for these values which are shown in table.3.2 (output current corresponding input voltage for non-linearized OTA). Where, $R_{L=}$ 10kΩ, $R_{bias=}$ 20kΩ, $V_{bias=} - 3.6v$, g_m=10ms, $R_{D=}$ 15kΩ.

Table.3.2 (output current corresponding input voltage for linearized OTA)

S.NO.	INPUT VOLTAGE(V_s)	OUTPUT CURRENT(I_0)
1.	0mV	0ma
2.	45.20mV	.0420ma
3.	51.04mV	.0460ma
4.	56.04mV	.0480ma
5.	62.91mV	0.056ma
6.	89.58mV	0.072ma
7.	102.08mV	0.084ma
8.	112.5mV	0.090ma
9.	137.5mV	.111ma
10.	150mV	.121ma
11.	166.66mV	.135ma
12.	206.25mV	.161ma
13.	343.75mV	.245ma
14.	416.66mV	.293ma
15.	527mV	.362ma
16.	663mV	.483ma
17.	818mV	0.53ma
18.	1150mV	0.58ma

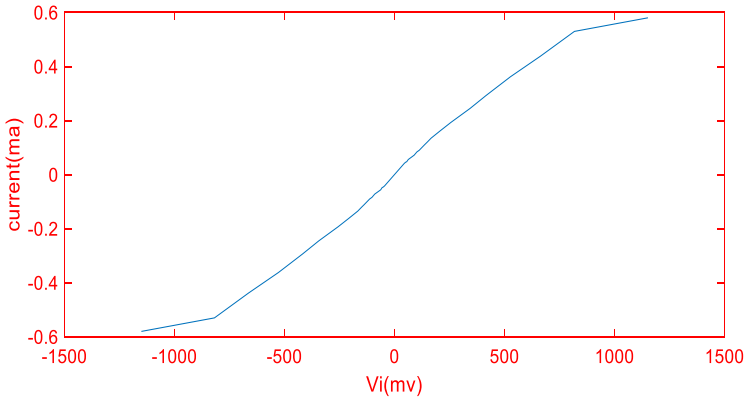

Fig 3.9(a): Transfer function of OTA (LM13600) with diode linearization (Experimental data)

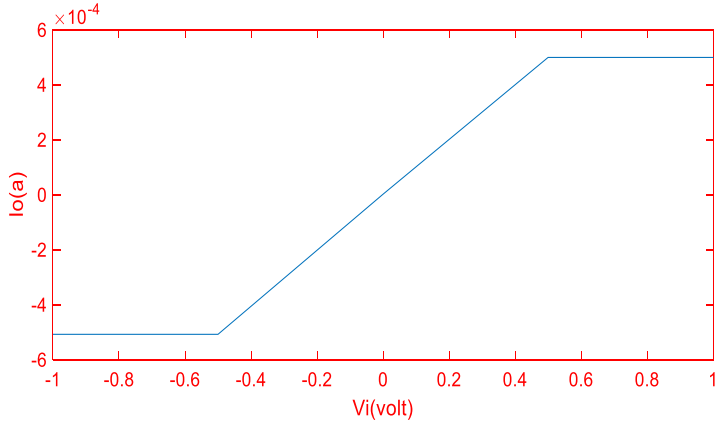

Fig 3.9(b): Transfer function of OTA (LM13600) with diode linearization (PSPICE)

3.5.3 Frequency response of transconductance OTA (LM13600)

Finally the circuit given in figure (3.6) is used to determine the frequency response of the OTA, IC LM13600 experimentally. The frequency response is expected to be 2 Mega Hertz.

3.5.3.1Experimental results

The circuit is designed for $R_{L=}$ 20kΩ, $R_{bias=}$ 30kΩ, $V_{bias=}$ − 5v so that transconductance is evaluated, g_m=5.73ms. The input signal is of 1 V_{p-p} for all frequencies and the input signal is applied through attenuator circuit, where $R_{1=}$ 20kΩ, $R_{2=}$ 1kΩ. From the experimental result, Frequency response of transconductance is shown in figure (3.10). This response of transconductance can be expressed as:

$$g_m = \frac{g_{mo}}{\left(1+j\frac{f}{f_o}\right)} \qquad (3.24)$$

Where, the 3-db frequency is f_o , f is the input signal frequency and g_{mo} is the transconductance of OTA. The 3-db frequency of g_m is approx. 1.7 MHz (Experimentally).

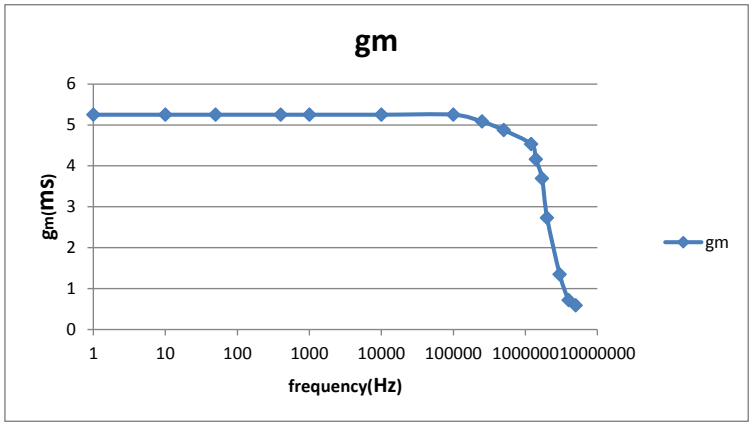

Fig 3.10: Frequency response of transconductance of OTA (LM13600)

3.6 Conclusion

In this chapter we discussed diode linearization methods, which are done to increase the input linear range of OTA that are more efficient than non-linearized OTA in terms of differential input voltage because linearized OTA is having wide input linear range. We did experiment to find out input linear range of linearized and non-linearized OTA. We have used these values for implementation of other applications of OTA in subsequent chapters. Finally the frequency response of IC LM13600 has also been determined the f_{3db} of the OTA was found to be 1.7MHz (Experimentally).

Chapter 4

Implementation of voltage controlled amplifiers

4.1 Introduction

In this chapter, we will discuss the voltage controlled amplifiers and some of applications of voltage control amplifier. Amplitude modulator and automatic gain control will be implemented through OTA and these applications will be implemented through the linearized OTA that minimize the SNR at output and gets more efficient result. We will also discuss operation of each application which is being implemented in this chapter.

4.2 Voltage control amplifier with diode linearization

The linearizing diodes can be used in a voltage – controlled amplifiers. To understand the input biasing, it is best to consider the R_D= 13kΩ resistor as a current source and use a Thevenin equivalent circuit as shown in figure. The potentiometer in figure (4.1) is used to minimize the offset error in output voltage.

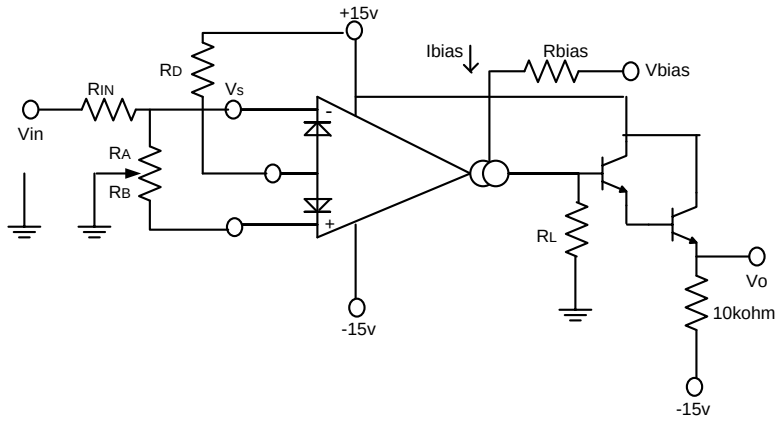

Fig 4.1: Voltage control amplifier

For optimum signal-to-noise performance, I_{ABC}should be large and larger amplitudes of input signal also improves the S/N ratio. The linearizing diodes help here by allowing larger input signals for the same output distortion. S/N may be optimized by adjusting

the magnitude of input signal via R_{IN} until the output distortion is below some desired level. The output voltage swing can then be set at any level by selecting R_L.

Although the noise contribution of the linearizing diode is negligible relative to the contribution of the amplifier's internal transistors, I_D should be as large as possible. This minimizes the dynamic junction resistance of the diodes (r_e) and maximizes their linearizing action against R_{IN}.

The input is fed at inverting terminal through voltage divider circuit and non-inverting terminal is grounded and biasing voltage is applied through bias resistance and output of linearized OTA is fed to voltage buffer realized by Darlington pair, Darlington is working as voltage buffer. Output voltage is taken at the output terminal of Darlington. Darlington is a pair of two transistors, emitter of one transistor is connected to base of second resistor so that minimum 1.4 volt is required to keep on the darlington, causing of this output voltage is having DC shift of 1.4 volt. As we know that voltage gain of Darlington is unity so that output is same as taken at output terminal of OTA except DC shift of 1.4 volt.

Amplifier gain is derived for these values, R_{IN}=30Ω, R_L=30kΩ, R_D=13kΩ.

$$\frac{V_O}{V_{IN}} = 940 * I_{bias} \tag{4.1}$$

$$I_{bias} = \frac{V_S - 1.4 + V_{bias}}{R_{bias}} \tag{4.2}$$

4.2.1 Experimental results

This circuit is designed for these valuesR_{bias}=20kΩ, V_{bias}= 0 Volt. Thereafter, Evaluating the bias current, $I_{bias} = 0.68\,mA$. Output voltage approximately $V_O = 3.44\,V_{p-p}$ for input signal of V_{IN} = $5\,V_{p-p}$. The voltage controlled amplifier's output result is shown in fig (4.2). In the figure 4.2(b), it shows the relation between V_0 and V_{bias}. This relation is achieved by simulating this circuit in PSPICE.

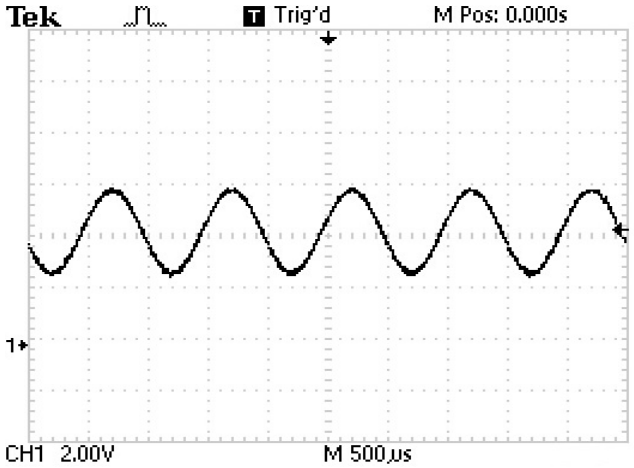

Fig 4.2(a): Voltage controlled amplifier's output

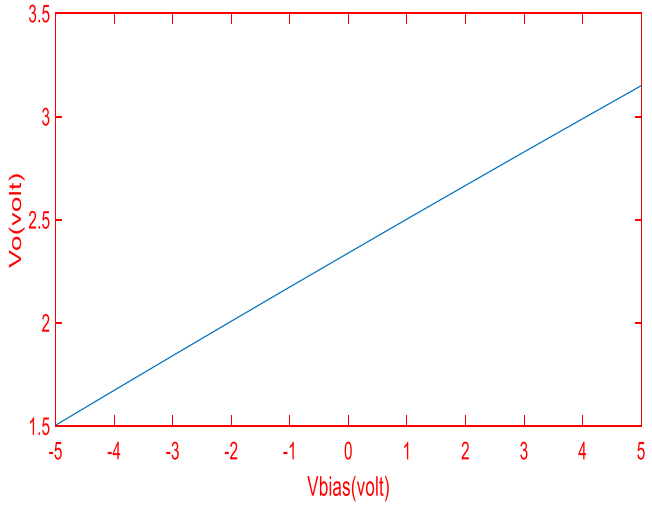

Fig 4.2(b): VCA's output with variation of amp bias voltage

4.3 Amplitude modulator

It is one of the amplitude modulation techniques [13] to generate radio signal. If any signal's amplitude is varied accordance to the carrier signal that is known as amplitude modulation. It consists of carrier signal and two side bands as shown in fig 4.4(b)

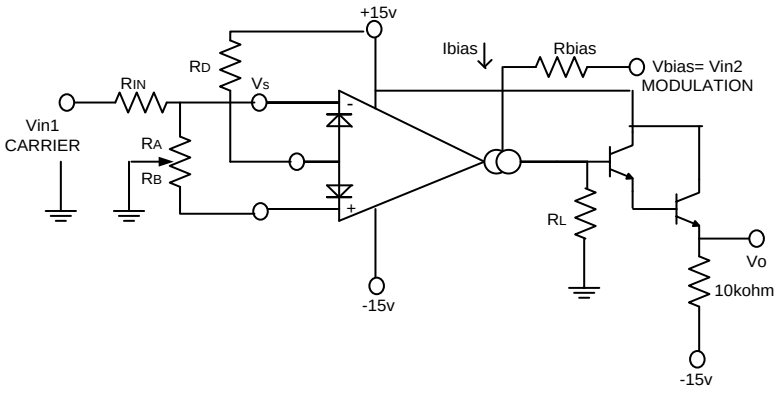

Fig 4.3: Amplitude modulator

Here amplitude modulated signal is produced using OTA (LM13600). Carrier signal is fed to input terminal of Linearized OTA and modulation signal is applied as bias voltage which provides bias current. Modulated output will appear at output terminal of buffer. Modulation signal's amplitude is being varied accordance to carrier signal that's why noise will be more as compare to frequency modulation so that to minimize the noise we are using diode resistance to improve the S/N power.

Modulation signal: $A_m sinw_m t$ (4.3)

Carrier signal: $A_c sinw_c t$ (4.4)

By using the equation (4.1),

$$\frac{V_O}{V_{in1}} = 940 * I_{bias}$$

$$\frac{V_O}{V_{in1}} = 940 * \left(\frac{V_{in2}+1.4}{R_{bias}}\right) \quad (4.5)$$

$$V_O = 940 * \left(\frac{V_{in2}+1.4}{R_{bias}}\right) * V_{in1} \quad (4.6)$$

$$V_O = a(1 + b\,V_{in1})c(t) \quad (4.7)$$

Where, $V_{in1} = c(t), V_{in2} = m(t)$

$$V_O = a[1 + bm(t)]\,c(t) \quad (4.8)$$

4.3.1 Experimental results

This modulator circuit is designed for carrier signal $c(t) = 5\sin(10 * 10^3 \pi f_c t)$, modulation signal $m(t) = 3sin(10^3 \pi f_m t)$. The modulated signal is shown in fig4.4 (b) and the result is verified by showing frequency spectrum as shown in fig4.4 (a) and. The lower and upper side band frequencies are $f_c - f_m = 4.5khz$, $f_c + f_m = 5.5khz$ and central frequency is $f_c = 5khz$. Where, R_{IN}= 30kΩ, R_D= 13kΩ, R_L = 30kΩ, V_{bias}=$m(t)$.

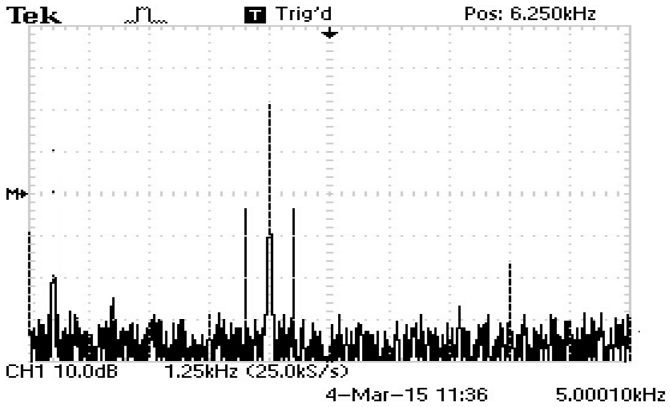

Fig 4.4(a): Frequency spectrum of amplitude modulator

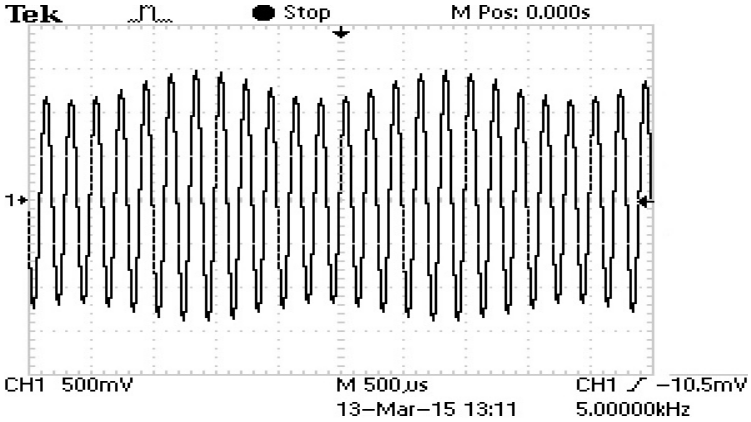

Fig 4.4(b): Modulated signal

4.4 Automatic gain control

Automatic gain control (AGC) [15] amplifier is a close loop system that can automatically adjust the gain to maintain a constant output signal level. There are feedback and feed forward type automatic gain control. Feed forward AGC is not mostly used because loop performance is sensitive to parameter variation due to faster change in input signal amplitude.

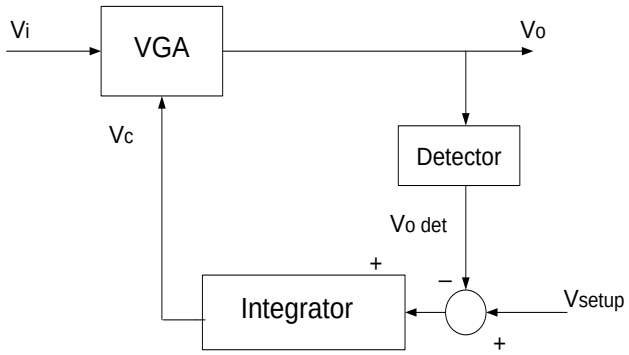

Fig 4.5: The block diagram of the feedback-type AGC

Voltage Gain amplifier is situated in forward path, it amplifies the input signal at specified gain determine by feedback loop. The forward path gain is monitored by an amplitude detector in feedback path and difference of detector output and reference set up voltage produces an error and thereafter it is integrated as DC like voltage to control the VGA gain. When input signal magnitude rises, initially output $V_o$will increase. At feedback path the detector detects this change in the very beginning, and correspondence a voltage change at output $V_{0\,det}$. The change at detector output will cause s difference compared with set up voltage. This difference is smoothed by integrator VGA to lower the gain of VGA that's how it compensates the increasing signal magnitude appeared at AGC output so that constant magnitude is maintained at AGC output

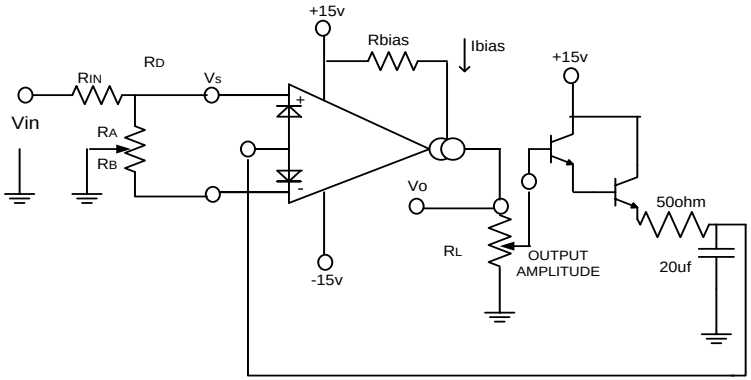

Fig 4.6: AGC amplifier

Figure (4.6) shows an AGC amplifier using this approach. V_o reaches high enough ($3V_{BE}$) to turn on the Darlington transistors and difference of output and reference set up voltage is fed to linearizing diodes and if I_D increases, then it will reduce the Amplifier gain to hold the constant output V_o. Difference of output and reference set up voltage is smoothed by $R\,C$ circuit and whenever input amplitude increases, then output will increase. The Difference of output and reference set up voltage will be positive and will rise to I_D and it will reduce the voltage gain and keep it at constant value as shown in figure (4.7).

4.4.1 Simulation results:

An automatic gain control is designed for following values, $R_A = 8.5k\Omega, R_B = 8.5k\Omega$, $R_{IN} = 250k\Omega$, $R_{bias} = 30k\Omega$, $R_L = 100k\Omega$. Output of AGC would be approx. 1.8 volt for unit step input signal as shown in figure (4.7).

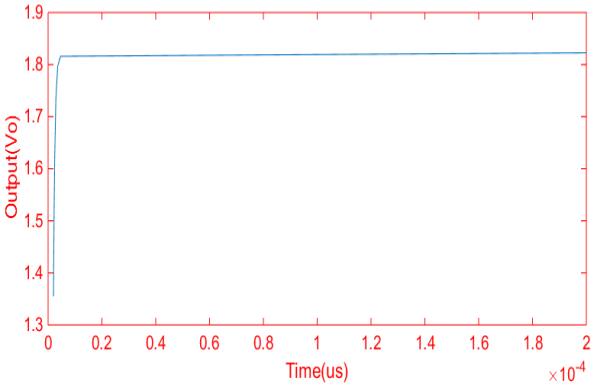

Fig 4.7: AGC Output (V_o)

4.5 Conclusion

In this chapter we have presented the experimental results of voltage controlled amplifier and amplitude circuits. In both these applications we have used the linearized OTA. We have also simulated a feedback type AGC.

Chapter 5

Implementation of Voltage controlled resistors and filters

5.1 Introduction

In this chapter we will present voltage controlled resisters and filters, which are implemented through OTA experimentally. In voltage controlled resistors, grounded and floating resistors will be realized. Chapter will also cover voltage controlled first order filters and second order filters [15]. We have implemented first order low pass filter, first order high pass filter experimentally. We have also implemented Biquad filters [16] based on two-integrators in loop architecture.

5.2 Single ended voltage controlled resistor

An operational transconductance amplifier can be used to implement a voltage controlled resistor as shown in figure (5.1).

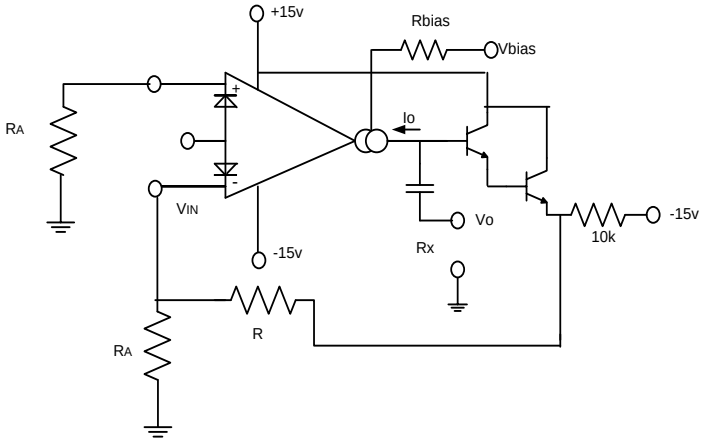

Fig 5.1: Voltage controlled resistor, single ended

As it can be observed in the circuit, buffer output is fed into inverting terminal through voltage divider; it is done to attenuate the signal to maintain V_{IN} within linear range of the LM13600. The signal is attenuated by $\frac{R_A}{R_A+R}$ and non- inverting terminal is at ground, so output current will be product of g_m and attenuated signal and g_m is controlled by

applied bias voltage. If it is observed that the ration of $\frac{V_o}{I_o}$ provides resistance which depends on bias current that's why R_X serves as a voltage controlled resistor and input is given between input terminal of buffer and ground so that it forms grounded or single ended resistor. The input capacitor is used to AC couple the signal to the realized resistors and value of the voltage controlled resistor is:

$$R_x = \frac{R_A+R}{g_m R_A} \tag{5.1}$$

5.2.1 Experimental results

This grounded resistor is designed for following values R_A= 220Ω, R= 100kΩ, R_{bias}= 20kΩ, DC input is applied with respect to ground and getting current of corresponding inputs, these values of voltage and current are shown in table.5.1. The simulated resistance value depends upon bias voltage, which is varied to achieve different values of resistances as shown in figure (5.2). The resistance value is shown in table 5.2. The one more thing is observed that the circuit gives almost correct value of resistance at high bias voltage than low bias voltage.

Table.5.1 (current corresponding input at fixed bias voltage)

S.NO.	Input voltage(volts)	$I_0(\mu A)$ at V_{bias}= 0V	$I_0(\mu A)$ at V_{bias}= -5V	$I_0(\mu A)$ at V_{bias}= -10V
1.	4	127.3	83	38.81
2.	4.5	138.9	93.1	42.50
3.	5	150.6	101.1	46.20
4.	5.5	162.4	109.2	49.83
5.	6	174.0	117.1	53.44
6.	6.5	186.0	125.1	57.2
7.	7	198.0	133.1	60.56
8.	7.5	210.2	141.0	64.06

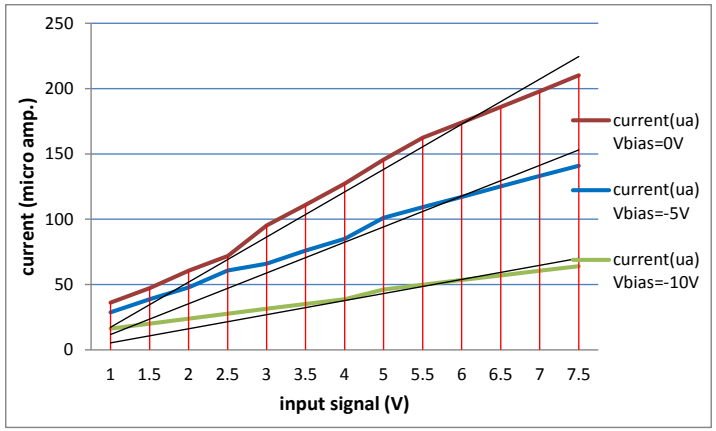

Fig 5.2: Resistors value for different values of V_{bias} or g_m

Table 5.2 theoretical and practical VCGR value for different V_{bias}

S/No.	Theoretical value	Practical value
1. V_{bias} = 0 V	34.83kΩ	42.21kΩ
2. V_{bias} =-5 V	55.08kΩ	60.34kΩ
3. V_{bias} = -10 V	131.60Ω	138.61kΩ

5.3 Floating voltage controlled resistor

Floating resistor is quite different from grounded resistor. In grounded resistor input signal is applied with respect to ground but in floating resistor input voltage is given with respect to another voltage that's why it is called floating resistor..

Input is applied between input terminals of the two buffers (output terminal of OTA). This input is fed to inverting terminals of OTA through buffer and the same input is fed to another OTA's non-inverting terminal, non-inverting terminal is directly shorted to another OTA's inverting terminal. Both OTA's inverting terminal connected through a resistance of R. Specifically, circuit is designed in a way to set same g_m of both OTAs that's why amp bias input of both OTA are shorted to provide same transconductance.

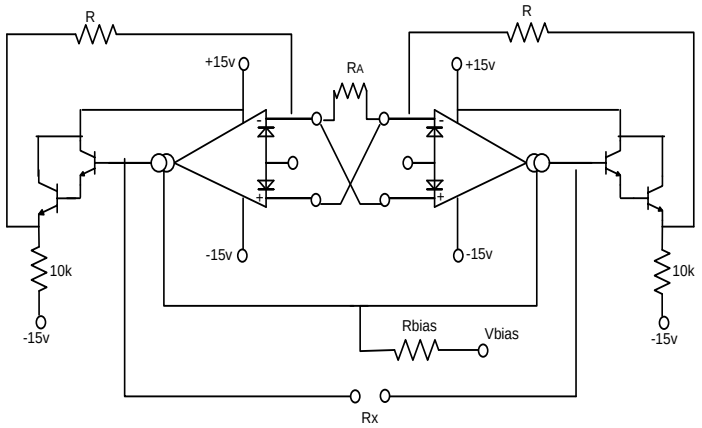

Fig 5.3: Floating Voltage controlled Resistor

If it is observed that the ration of V_o/I_o provides resistance which depends on bias current that's why R_X serves as a voltage controlled resistor and input is given between input terminals of both buffer as shown in figure(5.3) so that it forms floating resistor. The schematic diagram of a floating resistor is given in fig (5.3). A simple analysis to the circuit gives,

$$R_x = \frac{R_A+2R}{g_m R_A} \tag{5.2}$$

5.3.1 Experimental result

Fig (5.3) shows the experimental set for determining the value of floating VCR R_A= 1kΩ, R= 100kΩ R_{bias}= 20kΩ. DC input is applied between two inputs and getting current of corresponding inputs, these values of voltage and current are shown in table.5.3. This resistance value depends upon bias voltage, which is varied to achieve different values of resistances as shown in figure (5.4). The resistance value is shown in table 5.4. The one more thing is observed that the circuit gives almost correct value of resistance at high bias voltage than low bias voltage.

Table.5.3 (current corresponding input at fixed bias voltage)

S.NO.	Input voltage(volts)	$I_0(\mu A)$ at V_{bias}= -3V	$I_0(\mu A)$ at V_{bias}= -5V	$I_0(\mu A)$ at V_{bias}= 0V
1.	4	119.4	84.4	148.4
2.	4.5	132.3	92.8	169.2
3.	5	144.7	101.0	185.6
4.	5.5	156.8	109.0	201.7
5.	6	168.6	116.6	217.1
6.	6.5	179.9	124.1	232.3
7.	7	190.9	131.3	247.1
8.	7.5	201.6	138.2	261.3

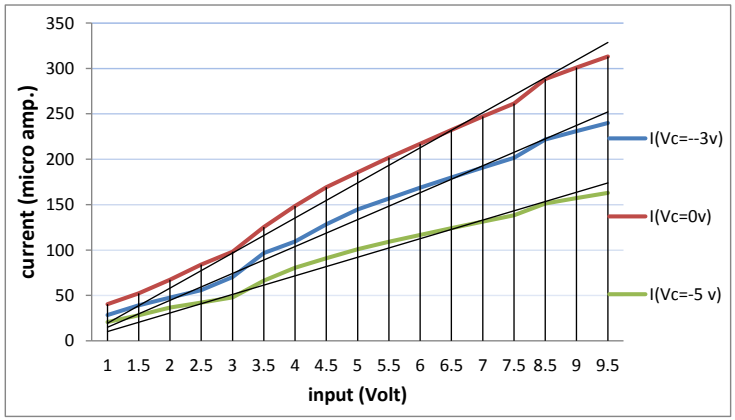

Fig 5.4: Resistors value for different values of V_{bias} or g_m

Table 5.4 theoretical and practical VCFR value for different V_{bias}

S/No.	Theoretical value	Practical value
1. V_{bais} = -3 V	39.63kΩ	42.57kΩ
2. V_{bais} =-5 V	48.85kΩ	65.05kΩ
3. V_{bias} = 0 V	30.89kΩ	31.00kΩ

5.4 Voltage controlled first order Low pass filter

OTA's are extremely useful for implementing voltage controlled filters, cause of its advantage. The cut off frequency can be changed without varying any passive component that is used in circuit. The cut-off frequency can be varied by changing only bias voltage or bias resistance that can be seen in describing equations, Cut-off frequency of low pass filters directly proportional to transconductance g_m.

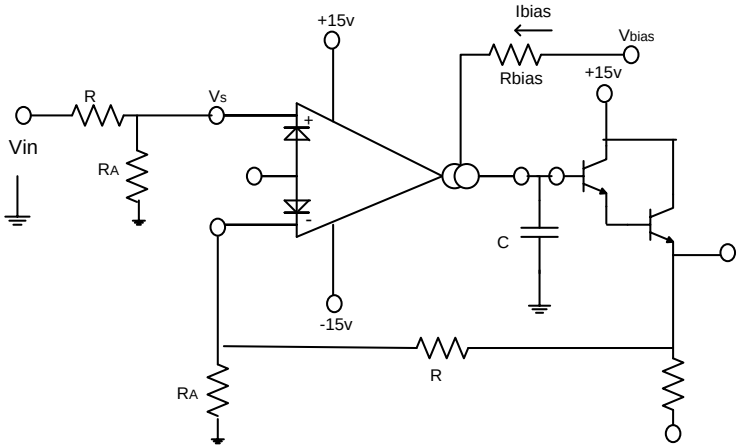

Fig 5.5: Circuit diagram of Low pass filter

For the single pole low pass filter shown above, input signal is given at non-inverting terminal through voltage divider and transconductance is controlled by applied bias voltage or bias resistance. A capacitor is used at output terminal of OTA that is employed between input terminal of Darlington and ground and Darlington pair is working as voltage buffer. Output of voltage buffer is given back to inverting terminal of OTA trough resistor.

Below the cut off frequency it is working as unity gain voltage buffer and above cut off frequency the circuit provides a signal RC roll-off of the input signal amplitude with a -3dB point defined by the equation.

The equation of first order low pass filter is,

$$\frac{V_o}{V_{in}} = \frac{1}{(1+sc/g_m k)} \tag{5.3}$$

Where, $k = \frac{R_A}{R_A+R}$

Cut off frequency of low pass filter,

$$f_o = \frac{R_A g_m}{(R_A+R)2\pi C} \tag{5.4}$$

5.4.1 Experimental results

The circuit given in figure (5.5) was used to implement a LPF with a cut off frequency of 81 kHz, Obtained values of passive components for designed the frequency are R_A= 220Ω, R= 100kΩ, C= 33Pf and V_{bais}= - 4 Volt. Fig5.6(a) shows the transient response, yellow one signal represents the input signal(6 V_{p-p} , frequency 4 KHz) and green one signal represents the output signal, Fig5.6(b)shows frequency response for this applied bias voltage(V_{bais}= - 4 Volt, $g_m = 9.23ms$), Cut off frequency for this bias voltage is approx. 80KHz(practical value) .

To experimentally verify the relationship given in equation (5.4) the cut off frequency of the circuit given in figure (5.5) was made to with different V_{bias}. The variation of the cut frequency with $g_m(V_{bias})$ is shown in figure 5.6(c)

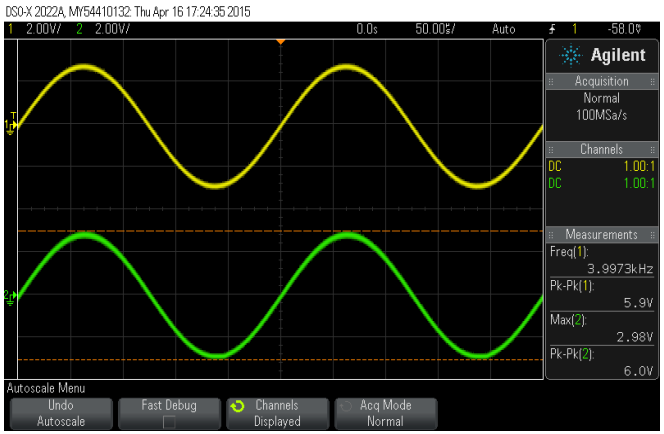

Fig 5.6(a): Transient response of filter LPF

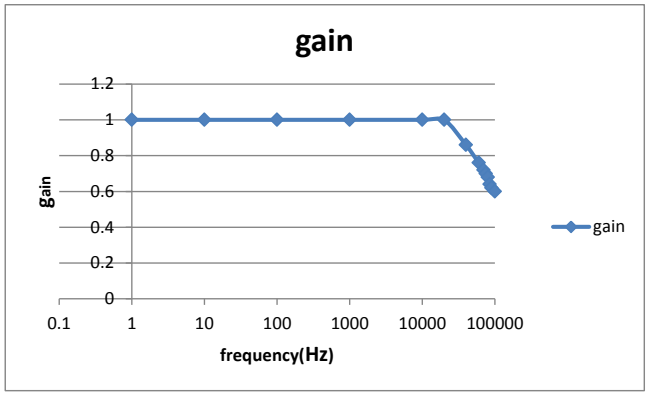

Fig 5.6(b): Frequency response of low pass filter

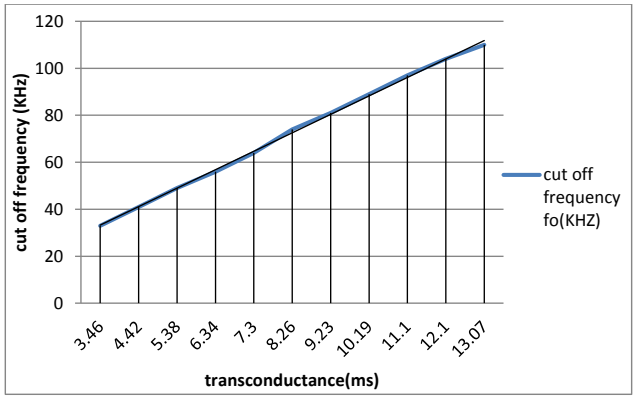

Fig 5.6(c): Variation of Cut-off frequency with g_m

5.5 Voltage controlled High pass filter

Fig (5.7) shows a voltage controlled single pole high pass filter, input signal is given through capacitor and transconductance is controlled by applied bias voltage or bias resistance. Output of voltage buffer is given back to inverting terminal of OTA through resistor, Above cut off frequency it is working as unity gain voltage buffer, below cut off frequency the circuit provides a signal RC roll-off of the input signal amplitude with a -3dB point defined by the equation given below.

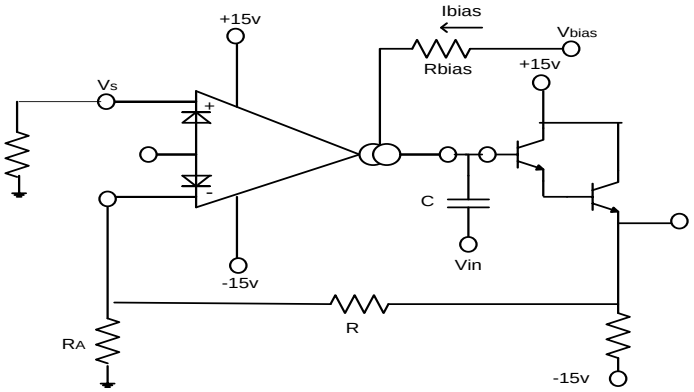

Fig 5.7: Circuit diagram High pass filter

The equation of first order high pass filter is,

$$\frac{V_o}{V_{in}} = \frac{Cs}{g_m k(1+sc/g_m k)} \tag{5.5}$$

Where, $k = \frac{R_A}{R_A+R}$

Cut off frequency of high pass filter,

$$f_o = \frac{R_A g_m}{(R_A+R)2\pi C} \tag{5.6}$$

5.5.1Experimental result

The circuit given in figure (5.5) was used to implement a HPF with a cut off frequency of 348 Hz, obtained values of passive components for designed frequency are R_A= 1kΩ, R= 100kΩ, C= 40nf and V_{bais}= - 4 volt. Fig5.8 (a) shows the transient response, yellow

one signal represents the input signal (3.30 V_{p-p}, frequencyo76 KHz) and green one signal represents the output signal. Fig5.8 (b) shows frequency response for this applied bias voltage (V_{bais}= - 4 Volt, g_m = 9.23ms).

To experimentally verify the relationship given in equation (5.6) the cut off frequency of the circuit given in figure (5.7) was made to with different V_{bias}. The variation of the cut frequency with $g_m(V_{bias})$ is shown in figure 5.8(c).

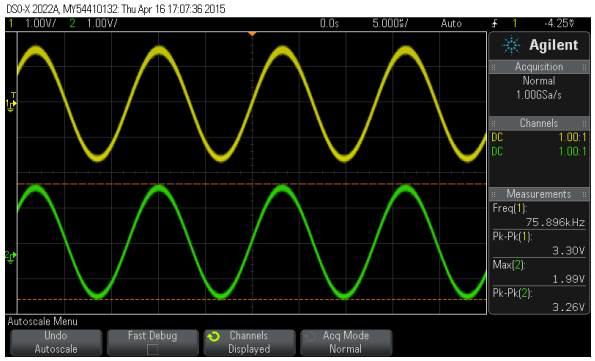

Fig 5.8(a): Transient response high pass filter of filter

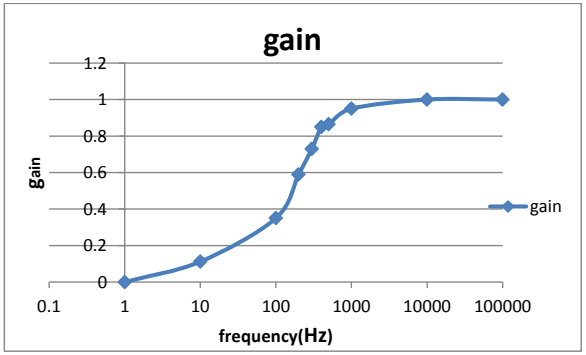

Fig 5.8(b): Frequency response of high pass filter

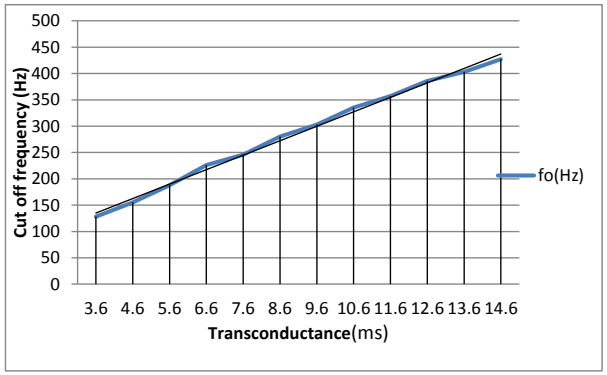

Fig 5.8(c): Variation of Cut-off frequency with g_m

5.6 Voltage controlled second order low pass filter

Figure (5.9) shows a two pole low pass filter, input signal is given at non-inverting terminal through voltage divider and transconductance is controlled by applied bias voltage or bias resistance. Below cut off frequency it is working as unity gain voltage buffer, above cut off frequency the circuit provides a signal RC roll-off of the input signal amplitude with a -3dB point defined by the equation below.

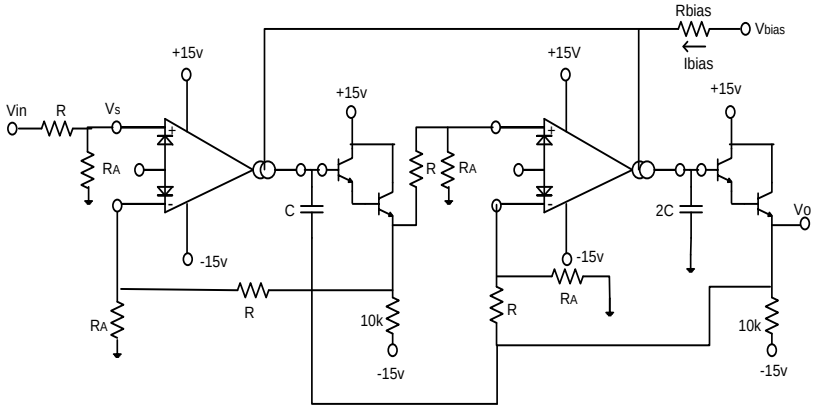

Fig 5.9: Circuit diagram second order low pass filter

The equation of second order low pass filter is,

$$\frac{V_o}{V_{in}} = \frac{g_m^2 k^2/2C^2}{(s^2+3g_m ks/2C+g_m^2 k^2/2C^2)} \qquad (5.7)$$

Where, $k = \frac{R_A}{R_A+R}$

Cut off frequency of low pass filter,

$$f_o = \frac{R_A g_m}{2\sqrt{2}(R_A+R)2\pi C} \qquad (5.8)$$

5.6.1 Experimental result

The circuit given in figure (5.5) was used to implement a LPF with a cut off frequency of 10 kHz, Obtained values of passive components for designed frequency are R_A= 220Ω, R= 100kΩ, C= 80Pf and V_{bais}= - 4 Volt, g_m=9.3ms). Fig 5.10(a) shows the transient response, yellow one signal represents the input (1 V_{p-p} , frequency 10 KHz) signal and green one shows the output signal. Experimentally cut off frequency for this bias voltage is approx. 13.9 KHz.

To experimentally verify the relationship given in equation (5.8) the cut off frequency of the circuit given in figure (5.9) was made to with different V_{bias}. The variation of the cut frequency with $g_m(V_{bias})$ is shown in figure 5.10(c).

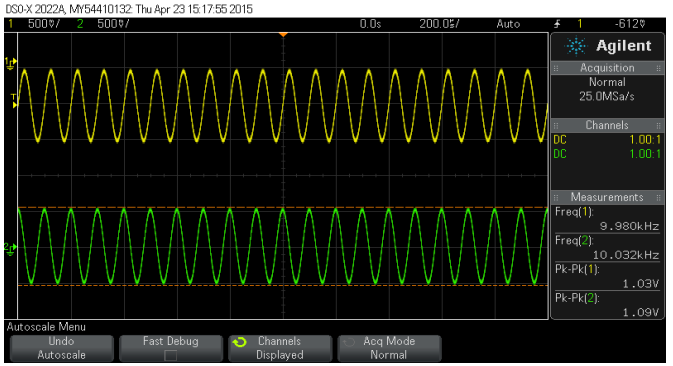

Fig 5.10(a): Transient response second order low pass filter of filter

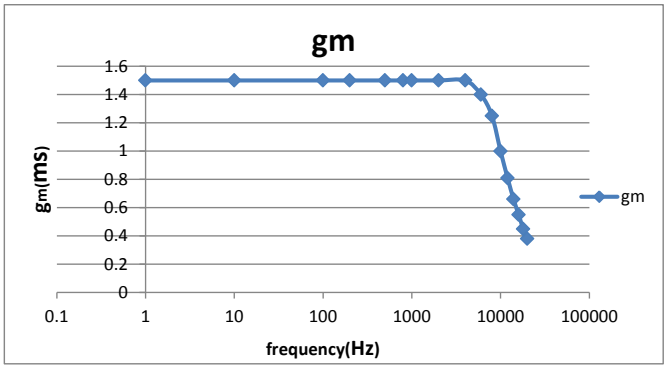

Fig 5.10(b): Frequency response of second order low pass filter

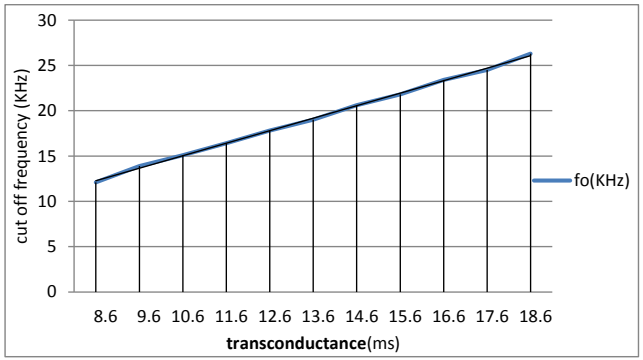

Fig 5.10(c): Variation of Cut-off frequency with g_m

5.7 KHN filter

KHN filter [16] [17] can provide simultaneously the three filtering transfer equations at different terminal, they are band pass filter (V_{01}), low pass filter(V_{02}) and high pass filter (V_{03}). The general architecture of a two-integrator is in a loop type active filter in which three outputs are available is given in figure (5.11). The following circuit have five OTAs, which is used to realize KHN filter and having transconductance g_{m1}, g_{m2}, g_{m3}, g_{m4}, g_{m5}. There are no externally connected resistors in circuit, only grounded capacitor is used. The most important features of KHN filter is that the pole frequency depends on the bias current and quality factor is adjusted independently by varying bias current of OTAs.

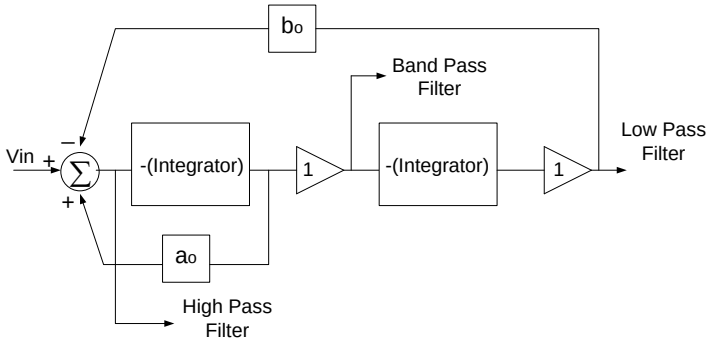

Fig.5.11 block diagram of KHN filter

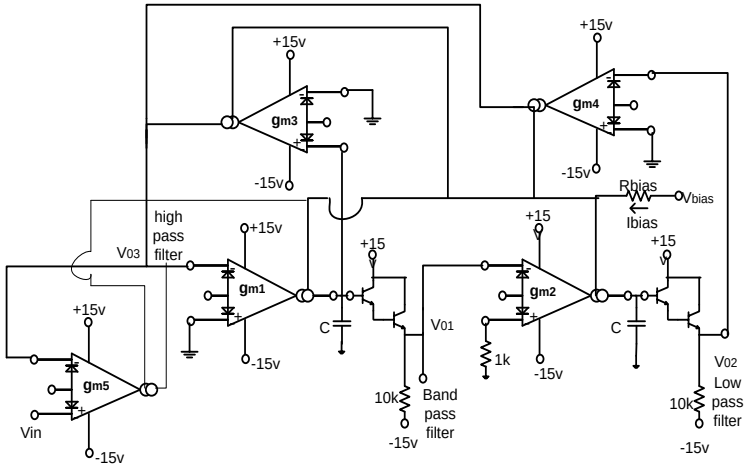

Fig 5.12: Circuit diagram of KHN filter

There are low pass filter, high pass filter and band pass filters, which are realized here and transfer function shows the type of filter which are given below.

Transfer functions of filters:

I. Band Pass filter :

$$\frac{V_{01}}{V_i} = \frac{-sg_{m1}/C_1}{s^2 + s\,{}^{g_{m1}g_{m3}}/_{C_1 g_{m5}} + {}^{g_{m1}g_{m2}g_{m4}}/_{C_1 C_2 g_{m5}}} \qquad (5.9)$$

II. Low Pass filter:

$$\frac{V_{02}}{V_i} = \frac{g_{m1}g_{m2}/C_1C_2}{s^2+s\,{}^{g_{m1}g_{m3}}/_{C_1g_{m5}}+{}^{g_{m1}g_{m2}g_{m4}}/_{C_1C_2g_{m5}}} \quad (5.10)$$

III. High Pass filter:

$$\frac{V_{03}}{V_i} = \frac{s^2}{s^2+s\,{}^{g_{m1}g_{m3}}/_{C_1g_{m5}}+{}^{g_{m1}g_{m2}g_{m4}}/_{C_1C_2g_{m5}}} \quad (5.11)$$

The pole frequency,

$$f_o = \sqrt{g_{m1}g_{m2}g_{m4}/C_1C_2g_{m5}} \quad (5.12)$$

Quality factor:

$$Q = \sqrt{\frac{C_1g_{m5}g_{m2}g_{m4}}{C_2g_{m1}g_{m3}^2}} \quad (5.13)$$

.

5.7.1 Simulation result:

This filter is designed for unity quality factor and pole frequency is $51kHz$ for which $g_{m1} = g_{m2} = g_{m3} = g_{m4} = g_{m5} = g_{m0} = 9.61ms$ and $C_1 = C_2 = C = 30nf$. Frequency response is shown in figure (5.13).

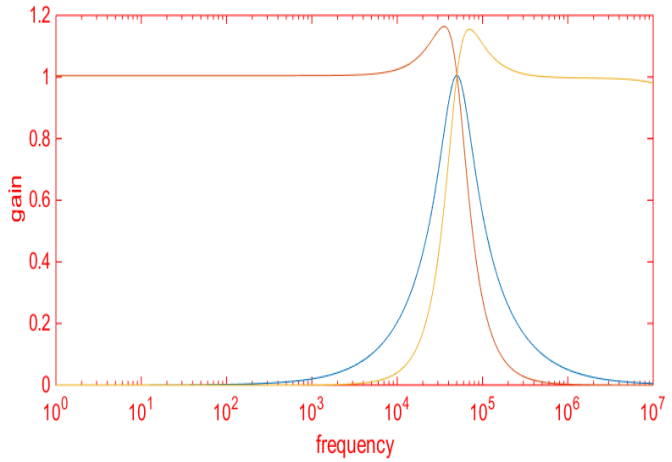

Fig 5.13: Frequency response of KHN filter

5.8 Voltage controlled state variable filter

The general architecture of a two integrated of a two integrated in a loop type active filter in which two outputs are available. This is a state variable filter. This is formed by two integrators, which are cascaded through buffer and output of integrators is used as negative feedback to feed back at input side as shown in figure (5.14). Output of first integrator is Band Pass filter and output second integrator is Low Pass filter. It is also implemented by Op-amp but we have implemented with OTA implemented through OTA so that output gain depends on bias current that's why it is also called voltage controlled state variable filter[19], due to excellent g_m tracking of the two amplifiers and the varied bias of the buffer darlington, these filters perform well over several decades of frequency.

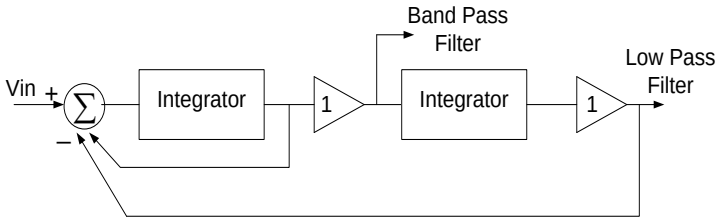

Fig 5.14: Block diagram of Tow-Thomas filter

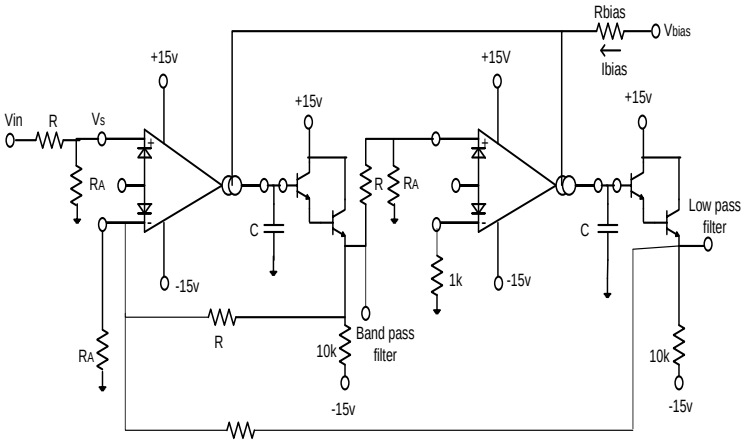

Fig 5.15: Circuit diagram of state variable filter filter

A simple analysis of the above circuit gives the following transfer function:

$$\frac{V_{BP}}{V_{in}} = \frac{(kg_m/C)s}{(s^2+skg_m/c+g_m^2k^2/C^2)} \quad (5.14)$$

$$\frac{V_{LP}}{V_{in}} = \frac{g_m^2k^2/C^2}{(s^2+skg_m/c+g_m^2k^2/C^2)} \quad (5.15)$$

Where, $k = \frac{R_A}{R_A+R}$

Cut off frequency of low pass filter,

$$f_o = \frac{R_A g_m}{(R_A+R)2\pi C} \quad (5.16)$$

5.8.1 Simulation results

This filter is designed for 63 kHz for which we Obtained values of passive components are R_A= 1kΩ, R= 20kΩ, C= 400pf and V_{bais}= - 5 Volt. This circuit is simulated in PSPICE and frequency response of state variable filter is shown in figure (5.16).

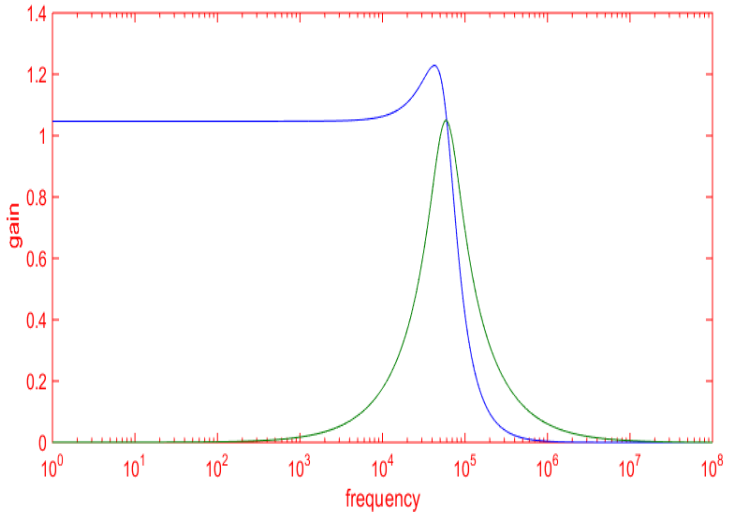

Fig 5.16: Frequency response of two pole second order LPF

5.9 Conclusion

In this chapter, we discussed voltage controlled resistors and voltage controlled filters. Both grounded as well as floating voltage controlled resistors have been realized experimentally we have also realized first and second order voltage controlled filters. This is a very close argument between the experimentally observed and simulated values of cut-off frequency for these filters.

Chapter 6

Implementation of voltage controlled relaxation and harmonic oscillators

6.1 Introduction

In this chapter, we will present voltage controlled oscillators [18]-[23], triangular/ square wave, ramp/pulse and sinusoidal VCO are realized through OTA and their oscillating frequency is varied by varying bias voltage of OTA. It is a very easy to change oscillating frequency in comparison of op-amp because in op-amp oscillating frequency can't be changed without varying the values of passive element but in OTA oscillating frequency can be changed without varying the values of passive element.

6.2 Triangular/square-wave VCO

Triangular and square wave [18]-[20] is generated simultaneously using IC LM13600. It is using both the halves of LM13600 and output of A_2 amplifier is fed to non-inverting terminal of OTAs as a positive feedback. It is voltage controlled oscillator, frequency of triangular and square wave depends on bias voltage (V_{bias}). Necessary condition for oscillator is that differential input voltage should not go beyond input linear range.

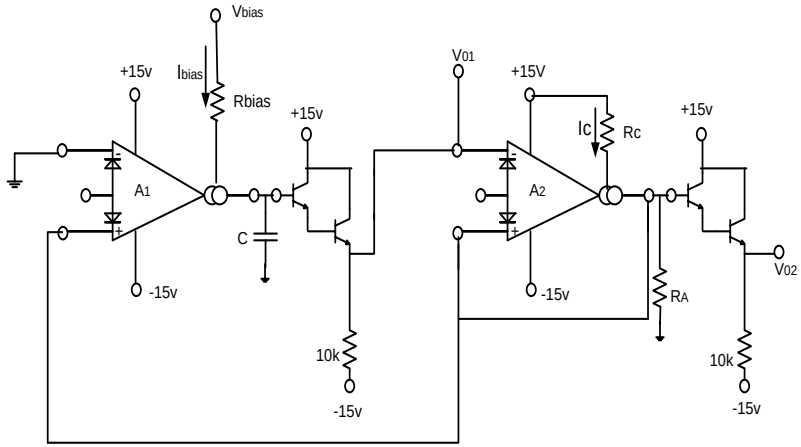

Fig 6.1: Circuit diagram of triangular/ square wave oscillator

To understand the operating theory, assume initially that capacitor is negatively charged, under this condition, positive voltage will develop across R_A and square wave will be switched high. This positive voltage will be fed to non-inverting terminal of both OTAs. This voltage makes amplifier A_1 generates positive current; this current will flow into capacitor. It will show positive going linear-ramp. This ramp signal is fed to inverting terminal of amplifier A_2 through buffer. Under this condition, this voltage equals that on the non-inverting terminal, at which point the output of amplifier A_2 will switch to negative and negative voltage will appear across R_A. This negative voltage will be fed to non-inverting terminal of both OTAs. This voltage makes amplifier A_1 generates negative current; this current causes capacitor C will discharge linearly. It will show negative going linear-ramp. This process repeats itself.

Oscillating frequency,

$$f_{OSC} = \frac{I_{bias}}{4CI_CR_A} \tag{6.1}$$

6.2.1 Simulation results

The Oscillator is designed for frequency of 442 KHz. For this component values are $R_{bias} = 30k\Omega$, $R_C = 51k\Omega$, $R_A = 5\Omega$, $C = 100pf$, $V_{bias} = 2.4V$. Frequency of triangular and square wave is calculated by equation (6.1). . This circuit is simulated in PSPICE and results are shown in figure6.2 (a) and figure6.2 (b).

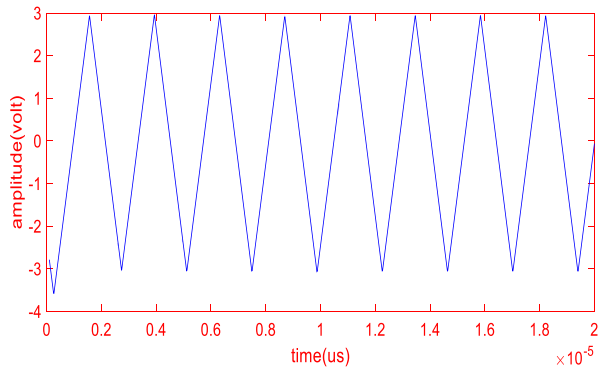

Fig 6.2(a): Triangular wave

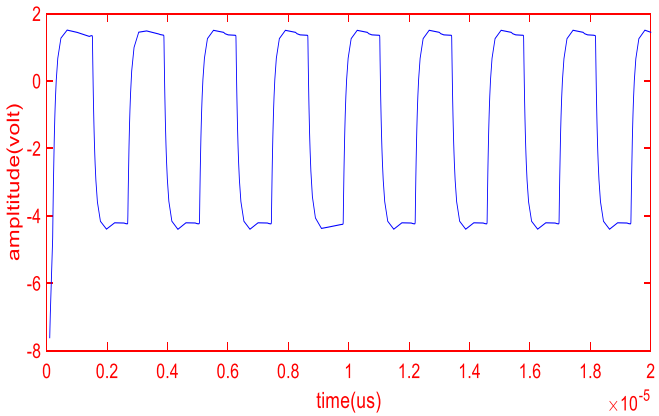

Fig 6.2(b): Square wave

6.3 Ramp/pulse VCO [20]

Figure 6.3 shows a voltage controlled Ramp and pulse generator. This circuit same as previous circuit but only difference is that charging current and discharging current are different. Charging current is relatively high than discharging current. Necessary condition for oscillator is that differential input voltage should not go beyond input linear range.

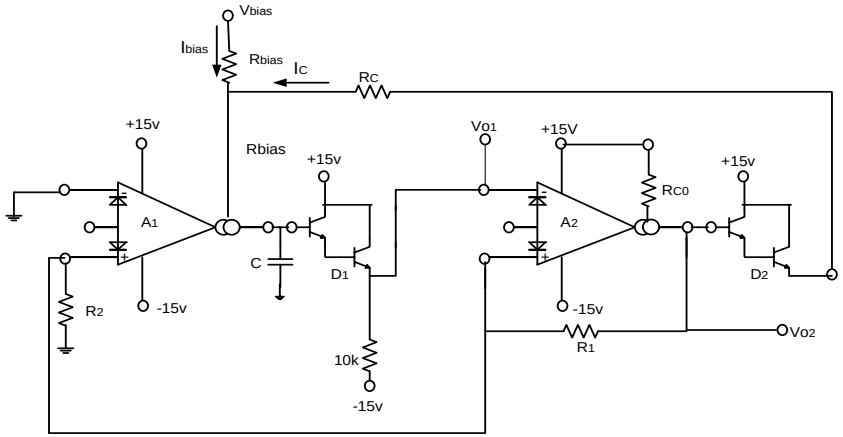

Fig 6.3: Circuit diagram of Ramp/ pulse VCO

To understand operating theory, assume initially V_{o2} is high enough to on the Darlington D_2 that adds current I_C to current I_{bias} to increase amplifier A_1's bias current and thus to increase the charging current. When V_{o2} is low, only current I_{bias} will flow as an amplifier A_1's bias current. It is a key of this circuit to generate pulse wave V_{02}. If charging current is high, then charging time will be low and pulse will be present at V_{o2}. The remaining operating theory is same as fig (46). Charging time is very low than discharging time, due to this pulse on time of is very low than off time. Ramp signal will appear at $V_{01}$and pulse wave will appear at V_{02}.

Peak voltage,

$$V_{PK} = \frac{(V^- - 0.8V)R_2}{R_1+R_2} \quad (6.2)$$

Pulse on time,

$$t_H \approx \frac{2V_{PK}C}{I_F} \quad (6.3)$$

Pulse off time,

$$t_L = \frac{2V_{PK}C}{I_C} \quad (6.4)$$

Oscillating frequency,

$$f_{OSC} \approx \frac{I_{bias}}{2V_{PK}C} \; for \; I_C < I_F \quad (6.5)$$

6.3.1 Simulation results

The oscillator is designed for frequency 142 KHz. For this, Obtained values of passive components for designed oscillator frequency are $R_{bias} = 510k\Omega$, $R_{C0} = 51k\Omega$, $R_1 = 100k\Omega, R_2 = 24k\Omega, R_C = 30k\Omega$, $C = 50pf$, $V_{bias} = 6.4V$, evaluating Peak voltage =2.748. Pulse on time = 311 ns, pulse off time= 7.046 us and Oscillating frequency of ramp and pulse wave is calculated by equation (6.5). This circuit is simulated in PSPICE and results are shown in figure6.4 (a) and figure6.4 (b).

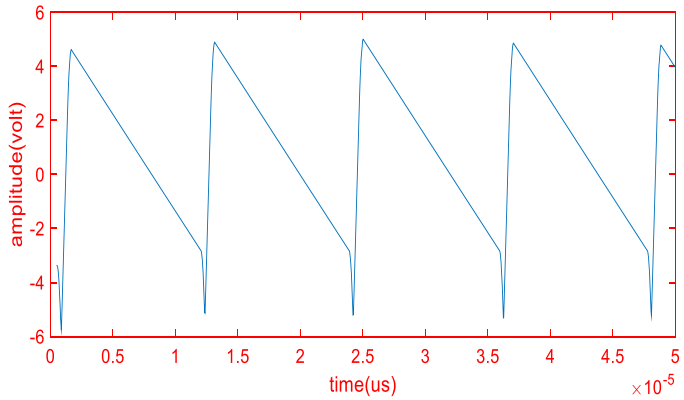

Fig 6.4(a): Ramp wave

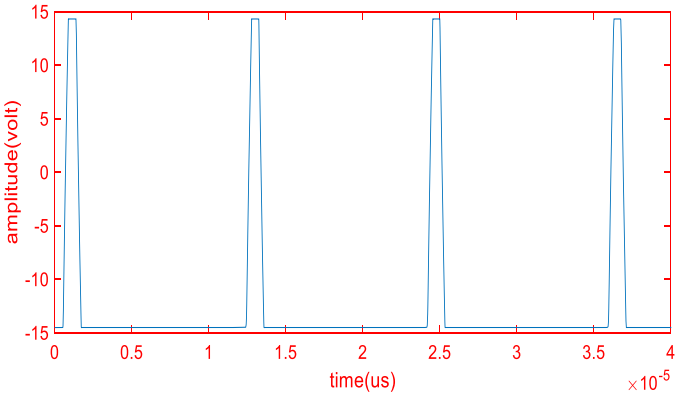

Fig 6.4(b): Pulse wave

6.4 Sinusoidal VCO

Voltage controlled sinusoidal [21]-[23] oscillator has its applications in power controllers, communication and signal processing. OTA is used as an active device for realization of odd phase oscillator. These oscillators provide same phase as well as same amplitude. This is also called multiphase sinusoidal oscillators.

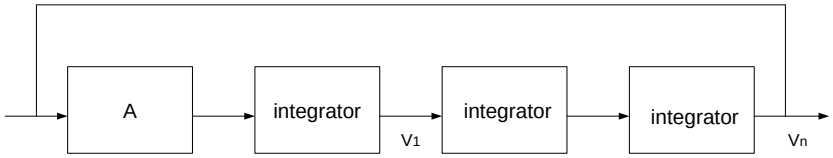

Fig 6.5: Block diagram of multiphase sinusoidal oscillator

In the figure (6.5), integrator blocks show identical inverting simple low pass section [23]. Voltage transfer function of each block is:

$$T(s) = -\frac{a}{s+b} \tag{6.6}$$

Where, the gain of low pass is a and the pole frequency is b, A is the gain of amplifier. The net loop gain of the n sections is:

$$\frac{V_0}{V_i} = A\left(-\frac{a}{s+b}\right)^n \tag{6.7}$$

The loop gain is unit then it sustains sinusoidal oscillations, i.e.

$$A\left(-\frac{a}{s+b}\right)^n = 1,\ s = jw \tag{6.8}$$

Here n =3, a = $\frac{g_m}{C}$ and b =$\frac{kg_m}{C}$,

$$A\left(-\frac{g_m}{kg_m+sc}\right)^3 = 1 \tag{6.9}$$

Finally oscillating frequency,

$$f = \frac{\sqrt{3}kg_m}{2\pi C} \tag{6.10}$$

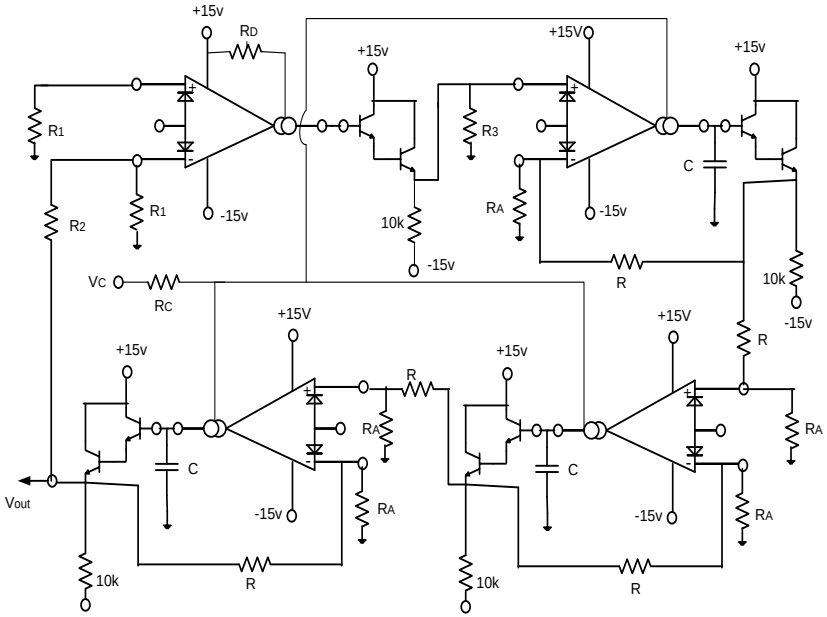

Fig 6.6: Circuit diagram sinusoidal oscillator

6.4.1 Simulation results

The oscillator is designed for frequency 6.09 KHz. For this, Obtained values of passive components for designed oscillator frequency are R_A= 220Ω, R = 100kΩ, R_1 = 620 Ω, R_2 = 10kΩ, R_3 = 30Ω, R_D = 30kΩ, V_C = 0V, C = 300pf as shown in figure (6.6), Oscillating frequency is calculated by using equation (6.10) as shown in figure 6.7(a) and frequency spectrum of sinusoidal oscillator is shown in figure6.7(b).

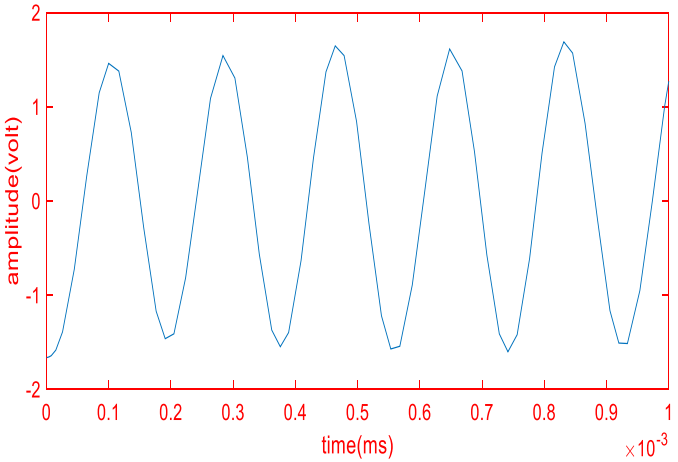

Fig 6.7(a): Sinusoidal wave

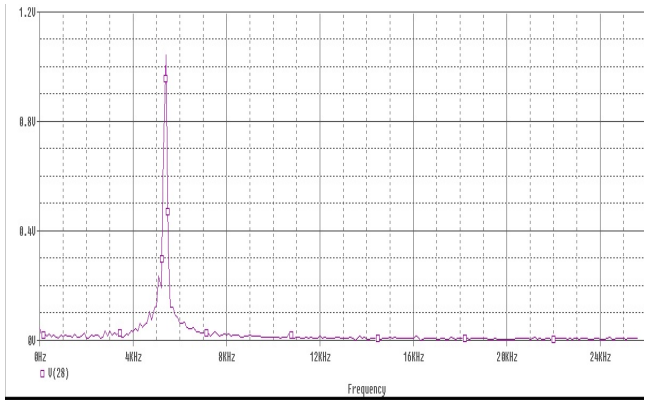

Fig 6.7(b): Frequency spectrum of sinusoidal oscillator

6.5 Conclusion

In this chapter, we have presented voltage controlled relaxation and the relaxation oscillators are based on the simple principle charging and discharging of a capacitor between two fixed with constant DC current. The harmonic oscillators is designed by cascading three lossy integrator and an amplifier in a positive feedback loop and applying bark hausen criteria for determining the condition of oscillation. PSPICE simulations have been presented to confirm, the workability of these circuits.

Chapter 7

General Applications of IC LM13600

7.1 Introduction

In this chapter we will present general applications of LM13600 which included Phase locked loop, Schmitt trigger, sample-hold circuit, log amplifier and logarithm current source. These applications are very useful in communication field that are realized through OTA. For log amplifier [25] and logarithm current [26] source we need external transistors but in the LM13600, it is already inbuilt in the IC. In all applications, it gives freedom to get instant change by varying bias voltage. Now we will discuss briefly in following section.

7.2 Phase locked loop

The main work of phase locked loop [24] is to maintain synchronization between input (reference) signal frequency f_i , and the corresponding output frequency f_o , using phase comparison technique. PLL is a feedback system that is containing a VCO, low pass filter and phase detector with its feedback loop. The phase locked loop is a control system allowing one oscillator to follow with another. It is likely to have phased offset between input and output phase or frequency, but when locked, the frequencies must be exactly tracked.

$$\varphi_{out}(t) = \varphi_{in}(t) + const. \tag{7.1}$$

$$\omega_{out}(t) = \omega_{in}(t) \tag{7.2}$$

The Phase locked loop output can be taken from either the output of the VCO or from V_{cont} (filtered (almost DC) VCO control voltage) depending on the application. The previous signal provides an output that tracks the any change in phase variation at the input. We are using voltage controlled oscillator as a local oscillator to produce a clock signal for a digital system. We can us phase or frequency as the input or output variables and Loop becomes locked when phase of input and output signal is same.

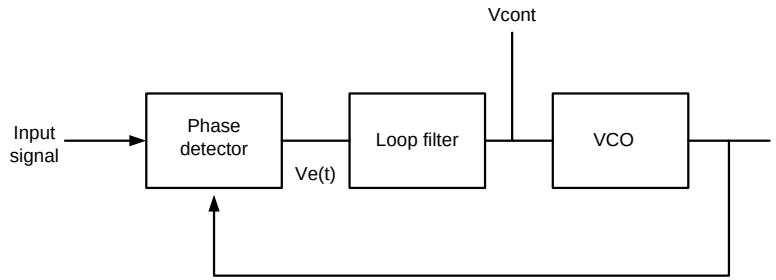

Fig 7.1: Block diagram of phase locked loop

Phase and frequency are interrelated by:

$$\omega(t) = \frac{d\varphi}{dt} \tag{7.3}$$

$$\varphi(t) = \varphi(0) + \int_0^t \omega(t')\ dt' \tag{7.4}$$

Phase detector compares the phase for each input with output signal and generates error signal.

$$V_e(t) = K_D(\varphi_{out}(t) - \varphi_{in}(t)) \tag{7.5}$$

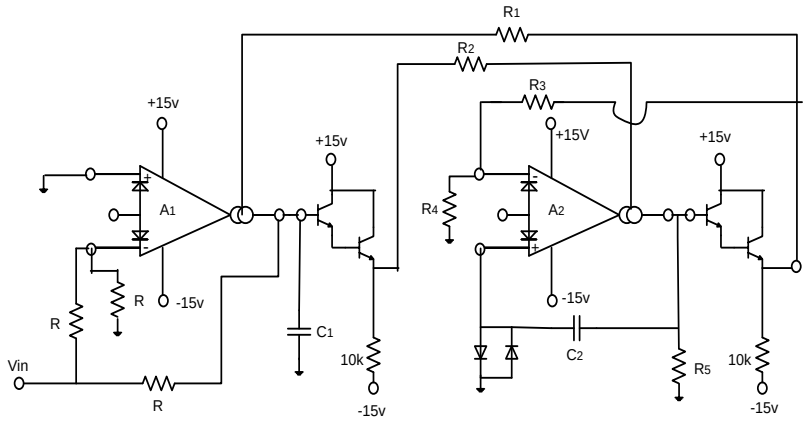

Fig 7.2: Circuit diagram of phase locked loop

The phase locked loop is designed using LM13600. A_2 is working as a VCO and it is controlled by voltage which is generated by loop filter and A_1 is consisting phase detector and loop filter. Loop filter is just a low pass filter and A_1 is controlled by output voltage, it compares input and output signal and generate phase error. VCO generates phase according to change in error and this voltage is fed back to A_1 which compares it with input and tries to minimize error. It is locked when input and output phase becomes same.

7.2.1 Simulation results

Phase locked loop is designed for these values R= 10kΩ, C_1 = 1uf, C_2 = .033uf, R_1 = $30kohm$, R_2 = 30kΩ, R_3 = 10kΩ, R_4 = 1.5kΩ, R_5 = 1kΩ. Input signal is 300 mv_{p-p} of 500 Hz frequency and output signal is also of 500 Hz frequency as shown in figure (7.3). Output signal will have DC phase shift of 2.8 V because of two Darlington pair.

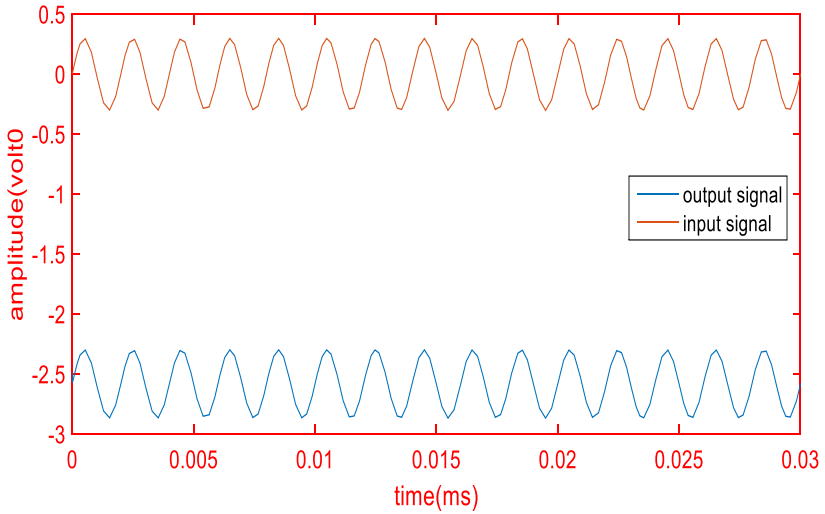

Fig 7.3: Input and Output signal of PLL

7.3 Schmitt Trigger

Schmitt trigger is a comparator circuit with hysteresis, implemented by applying positive feedback to the non-inverting input of a comparator or differential amplifier. It converts an analog signal to a digital signal. This is named a "trigger" because the output retains its value until the input changes sufficiently to trigger a change. When the input is higher than a certain chosen threshold value, the output is high. When the input is below a different (lower) chosen threshold value, the output is low, and when the input is between the two levels, the output retains its value.

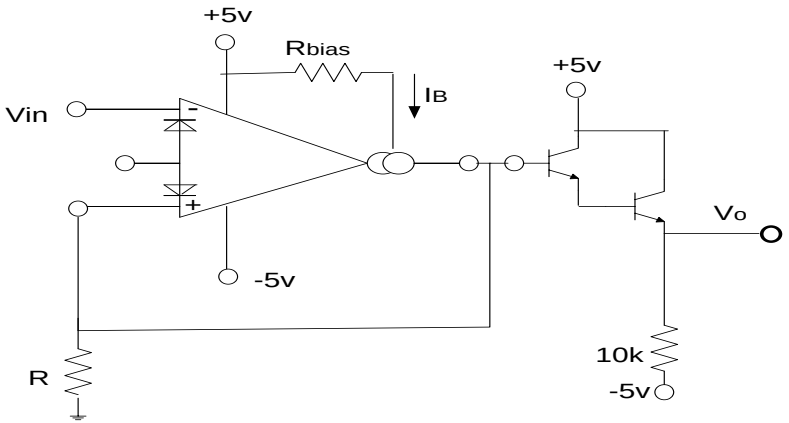

Fig 7.4: Circuit diagram of Schmitt Trigger

The lower and higher threshold value is:

$$V_{LT=}V_{UT} = \left|R\left(\frac{2V_{CC}-1.4}{R_{bias}}\right)\right| \qquad (7.6)$$

7.3.1 Simulation results

Schmitt trigger is designed for V_{LT}= -1V, V_{HT}= 1V and V_H= $|(V_{HT} - v_{LT})|$ = 2 V as shown in the figure (7.5) and output signal will have DC shift of 1.4 volt. Obtained values of passive component for this V_H= 2 V are R = 10kΩ, R_{bias}= 82kΩ, obviously amplitude input signal must be greater than amplitude of V_{HT} so that V_{In} of $6V_{p-p}$ and frequency of input signal is 100Hz.

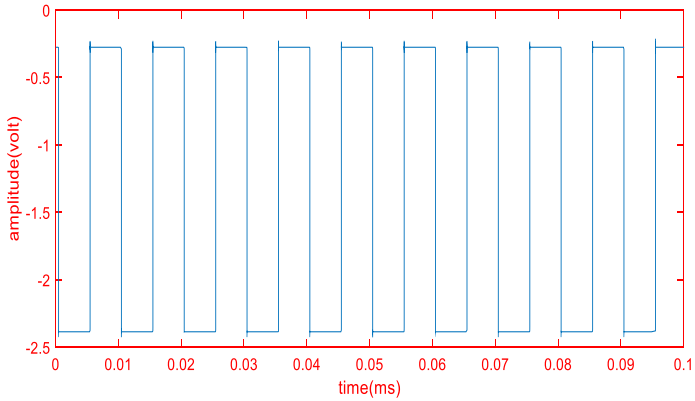

Fig 7.5: Output signal of Schmitt trigger

7.4 Log amplifier

A log amplifier [25] is an amplifier for which the output voltage V_{out} is k times the natural log of the input voltage V_{in}. This can be expressed as,

$$V_{out} = kln\frac{V_{in}}{V_{ref}} \tag{7.7}$$

Where, V_{ref} is the normalization constant in volts and K is the scale factor

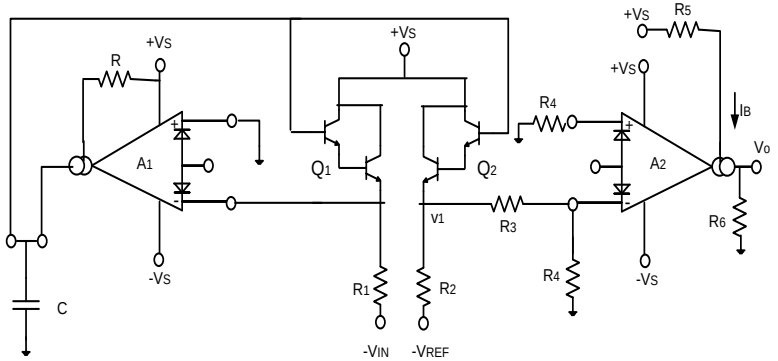

Fig 7.6: Circuit diagram of logarithm amplifier

The log amplifier responds to the ratio of currents through buffer transistors Q_1 and Q_2. Zero temperature dependence for V_{out} is ensured because the temperature coefficient of the A_2 transfer function is equal to the temperature coefficient of the logging transistor Q_1 and Q_2.

A_1 is just working as amplifier to provide enough voltage to keep on both darlington pair. Emitter of Q_2 is connected to inverting terminal through voltage divider and A_1's non-inverting terminal is grounded, inverting terminal is directly connected to emitter of Q_1 which gets negative voltage but it becomes positive after amplifying through A_1.

$$V_{out} = g_{m2}V_1\left(\frac{R_4}{R_3+R_4}\right)R_6 \tag{7.8}$$

$$V_{out} = V_1\left(\frac{2V_s-1.2}{2V_TR_5}\right)\left(\frac{R_4}{R_3+R_4}\right)R_6 \tag{7.9}$$

Where, we get V_1 after solving loop equations .i.e.

$$V_1 = ln\frac{(V_2+V_{IN})R_2}{(V_1+V_{REF})R_1} \tag{7.10}$$

$$V_1 \approx ln\frac{V_{IN}R_2}{V_{REF}R_1} \tag{7.11}$$

$$V_{out} = \frac{(2V_s-1.2)R_4R_6}{(R_3+R_4)R_5}\ln\frac{V_{IN}R_2}{V_{REF}R_1} \tag{7.12}$$

7.4.1 Simulation results

The Circuit is designed for Output voltage V_{OUT}= 5.83. For this, obtained following values are $V_s = 15v$, $R_4 = 13k\Omega$, $R_3 = 100k\Omega$, $R_5 = 100\Omega$, $R_6 = 120k\Omega$, $R_1 = 13K\Omega$, $R_2 = 13k\Omega$ and where $V_{IN} = 22v, V_{REF} = 5v$. Simulation result is as shown in figure (7.7).

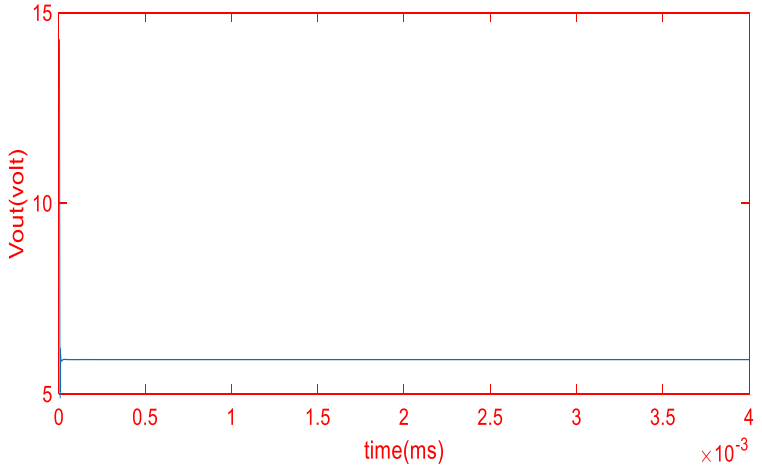

Fig 7.7: Output of logarithm amplifier

7.5 Logarithm current source [19]:

A voltage controlled logarithmic current source (VCCS log) [26] is often needed in an analog synthesizer. The VCCS controls the current I_{abc} through the OTA.

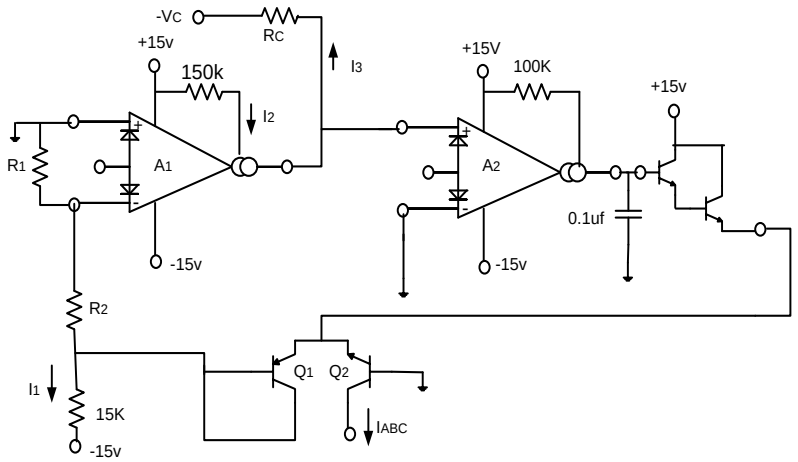

Fig 7.8: Circuit diagram of logarithm current source

This circuit provides a logarithm current out for a linear voltage in. Since the closed-loop configuration ensures that the input to A_2 is held equal to 0V, the output current of A_1 is equal to $I_3 = -\frac{V_C}{R_C}$. The differential voltage between Q_1 and Q_2 is attenuated by R_1 and R_2 network so that A_1 may be assumed to be operating within its linear range.

The input voltage to A_1 be:

$$V_{IN} = -\frac{2kTI_3}{qI_2} = \frac{2kTV_C}{QI_2R_C} \tag{7.13}$$

The voltage on the base of Q_1 is then,

$$V_B = \frac{(R_1+R_2)V_{IN}}{R_1} \tag{7.14}$$

The ratio of the Q_1 and Q_2 collector currents are defined by:

$$V_B = \frac{kT}{q}\ln\frac{I_{C2}}{I_{C1}} = \frac{kT}{q}\ln\frac{I_{ABC}}{I_1} \tag{7.15}$$

Combining and solving for I_{ABC}yields:

$$I_{ABC} = I_1\, exp\left[\frac{2(R_1+R_2)V_C}{R_1I_2R_C}\right] \tag{7.16}$$

7.5.1 Simulation results

This logarithm current source is designed for these values $R_1 = 1k\Omega, R_2 = 5k\Omega, V_C = -10v\ to\ 10v$. Circuit is simulated in PSPICE and the result verifies the equation (7.16). Current I_{ABC} is showing in the figure (7.9) corresponding V_C.

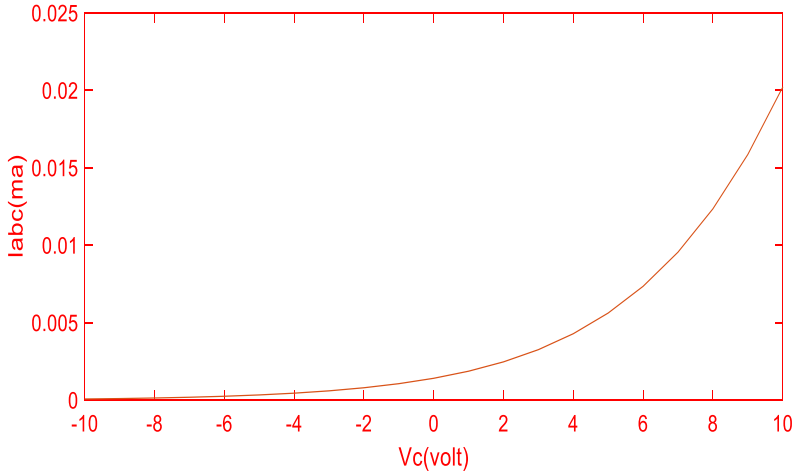

Fig 7.9: Output of logarithm current source

7.6 Conclusion

In this chapter we have presented some applications of OTA. The applications include Schmitt trigger, logarithm amplifier, and phase locked loop and logarithm current source. Since the LM13600 IC package includes two uncommitted Darlington transistors. The application does not require external transistor. PSPICE simulation results confirming the workability of these circuits have also been presented.

Chapter 8

Conclusion and future scope

8.1 Conclusion

In chapter I of the dissertation, we have given a general introduction of the operational transconductance amplifier and discussed its ideal characteristics amplifier and general application in analog signal processing. In chapter II of the dissertation, the general architecture of OTA and its limitations has been discussed. In chapter III of the dissertation, we have discussed the various methods of linearization of the bipolar OTA [2]. We have also carried out experimental characterization of the OTA IC LM13600 to find its input range (linear) and frequency response. In chapter IV of the dissertation, we have realized voltage controlled amplifiers, amplitude modulator, and automatic gain control. . In chapter V of the dissertation, both grounded as well as floating voltage controlled resistors have been realized experimentally we have also realized first and second order voltage controlled filters [15]. There is a very close argument between the experimentally observed and simulated values of cut-off frequency for these filters. In chapter VI of the dissertation, we have presented voltage controlled relaxation oscillators. These oscillators are based on the simple principle of charging and discharging of a capacitor between two fixed with constant DC current. The harmonic oscillator is designed by cascading three lossy integrators and an amplifier in a positive feedback loop and applying Barkhausen criteria for determining the condition of oscillation. PSPICE simulations have been presented to confirm, the workability of these circuits. In chapter VII of the dissertation, we have presented some general applications of OTA. The applications include Schmitt trigger, logarithm amplifier, and phase locked loop and logarithm current source. Since the LM13600 IC package [12] includes two uncommitted Darlington transistors. The application does not require external transistor. PSPICE simulation results confirming the workability of these circuits have also been presented.

8.2 Future scope

In this dissertation, we have implemented analog signal processing applications through IC OTA LM13600. Since this OTA IC has uncommitted voltage buffers on chip and two OTAs are available on the same chip many interesting Active building blocks suggested in may be synthesized with this IC. Notable among these is VDBA (Voltage Differencing Buffered Amplifier. The IC LM13600 can be used to realize most of these active building blocks in conjunction with current transistor arrays, current feedback operational amplifier and 741 type of ICs.

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