DESIGN AND IMPLEMENTATION OF CURRENT MODE FILTERS USING LOG DOMAIN TECHNIQUES

A

DISSERTATION

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Submitted by

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CANDIDATE'S DECLARATION

I **Mohit Saxena** Roll No. **2K13/C&I/06** student of M.Tech (Control and Instrumentation), hereby declare that the dissertation/project titled **"Design and implementation of current mode filters using log domain techniques"** under the supervision of **Prof. Pragati Kumar** of Electrical Engineering Department, Delhi Technological University in partial fulfillment of the requirement for the award of the degree of Master of Technology has not been submitted elsewhere for the award of any degree .

Place: Delhi

Date: 28/07/15

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CERTIFICATE

This is to certify that the dissertation **"Design and implementation of current mode filters using log domain techniques"** on Major Project-2 being submitted by **Mohit Saxena (2K13/C&I/06)** in partial fulfillment of the requirements for the degree of **Master of Technology** in **Control and Instrumentation** at Delhi Technological University is an authentic record of the work carried out by him under my supervision and guidance.

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

Place: Delhi

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MOHIT SAXENA

ABSTRACT

Due to the ongoing trends of lower power supply voltages and low power operation, the area of analog integrated filters is facing challenges. The maximal dynamic range achievable through conventional filter implementation techniques such as OA (Operational amplifier), MOSFET-C, transconductance-C etc. are restricted by the supply voltage. With log domain filters having signal swing of 100 mV, we can achieve 60-80 dB of dynamic range in circuits operating in the MHZ range using power supplies of 2.5V or less. These features make them an interesting choice in signal processing applications. Log-domain filters have emerged in recent years as a new and important class of Current-mode circuits The present works deals with the signal processing applications of the log domain circuits. After presenting an overview of the log domain filtering, translinear principle for log domain filters, Bernoulli cell and its implementation to higher order filters have been presented. In the later part, design of log domain filters based on operational simulation of LC ladders and state space synthesis have been presented. All the circuits presented in the dissertation have been simulated in PSPICE.

CONTENTS

LIST OF FIGURES

LIST OF SYMBOLS AND ABBREVIATIONS

Symbols	Descriptions
I_C	Collector Current
I_S	Reverse Saturation Current
V_T	Thermal Voltage
V_c	Collector Voltage
V_b	Base Voltage
V_{cc}	Source Supply Voltage
I_b	Base current
I_o	Bias Current
I_{damp}	Damping Current
V_{be}	Base Emitter Voltage
R_E	Emitter Resistance
w_o	Pole Frequency
Q	Quality Factor
BJT	Bipolar Junction Transistor
KCL	Kirchhoff ’s Current Law
KVL	Kirchhoff ’s Voltage Law
TLP	Translinear Principle
CW	Clockwise
CCW	Counter clockwise
ADC	Analog to Digital Convertor
OA	Operational Amplifier

Chapter 1
Introduction

1.1 Introduction

The present work deals with realization of current mode filters using log-domain techniques. Log domain filters exploit the non-linear relationship between the collector current and base-emitter voltage of bipolar transistors [1]. This relationship is an exponential relationship. In conventional RC-active filters, the active devices are used in their linear region of operations and the circuits are limited in their performance by temperature and dynamic range. The log domain filters do not suffer from both these problems as the temperature dependent terms in the design of the circuit cancel out. Similarly as the transistors non-linear characteristics is retained so there is theoretically no limitation on the amplitude of the input signals. Another noteworthy feature of the log domain circuits is the elimination of passive resistors thus making the circuits suitable for integration. As the parameters of the designed filters depends on the values of external DC currents these parameters can be varied by changing these DC bias currents thus making them electronically tunable.

In the following we present the evolution of the log-domain circuits followed by an introduction to log-domain filtering techniques. The outline of this chapter is as follows the first section will provide a description of the evolution of the log domain filter as it pertains to this work [2]. The next section will present an introduction to the concepts of log domain filtering, and will provide an overview of a log-domain filter structure and its implementation. The final section will discuss the organization of this thesis and provide an outline of its contents.

1.2 A historical background

The concept of the log-domain filter was originally proposed by Adams and introduced to the Audio Engineering Society in 1979 [3]. Adams had developed a method by which the resistor in an RC filter could be replaced with a diode, a nonlinear element. By controlling the bias Current of the diode, the cutoff frequency of the filter could be electronically tuned over several decades of frequency. Adams described the discovery as "a circuit composed of both linear and non-

linear elements, which when placed between a log converter and an anti-log converter, will cause the system to act as a linear filter".

The technique introduced by Adams did not receive significant attention until 1993, when Frey [1] proposed a formal procedure for synthesizing log-domain filter functions. The method developed by Frey introduced the state-space matrices as a means to explain the operation of the filter.

The Transistor level approach for Log-Domain Filtering was proposed by Emmanuel M. Drakakis, Alison J.Payne and Chris Toumazou in 1997[8]. The method introduced a continuous-time circuit element termed as Bernoulli cell which is composed of an npn BJT and an emitter connected grounded capacitor and is governed by the differential equation of the Bernoulli form. The Bernoulli cell can be utilized in both the analysis and synthesis of Log-Domain circuits.

Also, the more intuitive procedure for synthesizing log-domain filter functions was proposed by Perry and Roberts in 1995 [16]. The method introduced signal-flow graphs as a means to describe the operation of the filter, from which common filter design techniques, such as the operational simulation of LC ladders, could be applied. Such techniques can be used to simplify the filter design procedure, and can be applied to high-order systems.

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1.3 An overview of log domain filtering

A simple explanation of the principle of log domain filtering can be understood in terms of the diode - capacitor circuit described by Adams [3], as shown in Fig.1.1**.** If we assume that the current flowing through the diode can be expressed by a simple exponential function, the differential equation describing the operation of this circuit can be expressed as

$$e^{(V_I - V_0)} = C\frac{d}{dt}(V_0) \tag{1.1}$$

Where V_I is input voltage and V_0 is output voltage.

Which can be written as

$$e^{V_I} = C\frac{d}{dt}(e^{V_0}) \tag{1.2}$$

Or in integral form as

$$e^{V_0} = \frac{1}{c}\int(e^{V_I})dt \tag{1.3}$$

This circuit does not implement a linear integrator in terms of the input and output voltages V_I and V_0 [3]. However, if these variables were replaced by X_I and X_o, according to

$$V_I = \ln (X_I) , V_0 = \ln (X_0), \quad (1.4)$$

Which can be written as

$$X_0 = \frac{1}{C} \int (X_I) dt \quad (1.5)$$

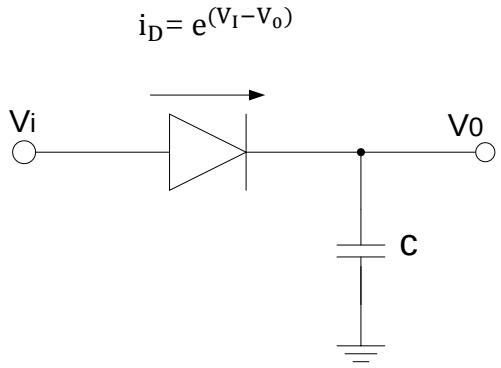

Fig.1.1 A Simple log domain integrator

Therefore, by logarithmically compressing the signal X_I according to equation (l.4) to obtain V_I at the circuit input and by exponentially expanding V_0 according to the inverse of equation (l.4) to obtain X_0 at the circuit output, a linear integration can be realized. Such a means of expansion and compression is readily available in the form of the voltage to current relationship of the diode equation. In this case, the desired input and output signals, X_I and X_0, are in fact currents, and the integration which is taking place is performed on logarithmically compressed signals named as "logarithmic domain".

A generic block diagram for a log domain filter is shown in Fig.1.2. This filter is composed of three distinct sections an input compression stage, a filter stage, and an output expansion stage. Voltage to current conversion and logarithmic compression are performed in the first stage, as shown by the progression of the V_{in}, I_{in} and $\vec{V_i}$ signals in the figure. The V/I conversion ratio is represented as shown in Fig.1.2, and the logarithmic compression is performed by means of a bipolar transistor. Filtering (in the logarithmic domain) is performed in the second stage. The symbol for

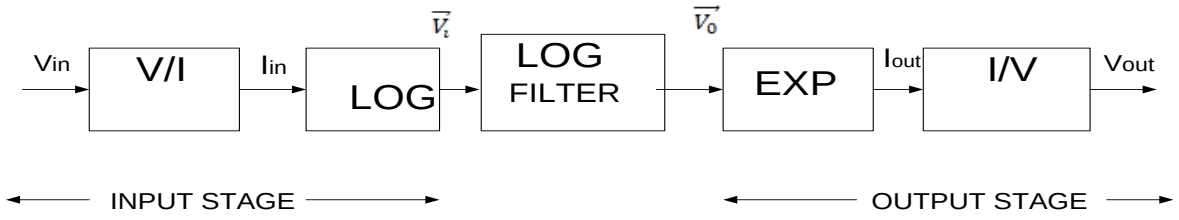

Fig.1.2 Block diagram of log domain filter

the log-domain integrator, the basic building block for the filter, is drawn in the Fig.1.2. Exponential expansion and I/V conversion are performed in the final stage, as shown in the progression of $\overrightarrow{V_0}$, I_{out} and V_{out} signals. Exponential expansion is once again performed by means of a bipolar transistor, and then the I/V conversion ratio is done.

1.4 Outline of the work presented in the dissertation

In this dissertation, chapter 1 covers the basic concepts of log domain filtering. The Basic log domain integrator and history of log domain is also discussed. Second chapter covers the basic description of Translinear circuits, design of log domain filters using translinear principle, and its general applications in analog signal processing. It also covers the basic concepts of Bernoulli cell and implementation of higher order filters have been verified by PSPICE simulation. In the third chapter, LC ladders and design of log domain filters based on simulation of LC ladders have been discussed. In fourth chapter, state space synthesis in linear circuits and corresponding log domain state space synthesis have been discussed. In the last and final chapter a summary of the work carried out has been presented alongwith some scope for future extension of the work.

Chapter 2

Log domain filters based on translinear circuits and the Bernoulli cell

2.1 Introduction

In the present chapter, we will discuss the translinear circuit principle [5] and the Bernoulli cell [7]. Both translinear circuit principle and the Bernoulli cell have been used extensively in design of log domain filters, so it is worthwhile to present a review of these two in details. After the review we have also simulated simple first order, second order and higher order filter structures using these concepts.

The term translinear was first used by B. Gilbert in 1975 [7] though he had introduced these concepts as early as 1969. By translinear circuits he meant those circuits where the linear model of the transistor was not used to arrive at the input-output relations between the current input and current output in a circuit consisting of BJT's in which the base emitter junctions consists of an even number of transistors. He had proved that in such circuits (i) The input-output current relationships were independent of temperature. (ii) The relationships were not limited by the amplitude of the inputs (in contrast to the circuits in which a linear model of the transistor is used to arrive at the input-output relationships).

The Bernoulli cell comprises an npn transistor and an emitter-connected grounded capacitor. Its dynamic behavior is determined by a differential equation of the Bernoulli form [8]. The identification of the Bernoulli cell leads to the design of a system of linear differential equations which describe the dynamics of the derived log-domain state-variables. This approach can be used for the analysis of log-domain circuits. The collector current of the transistor have a form of Bernoulli's general non-linear differential equation [8]. By changing the suitable variables, Bernoulli's equation can be converted to a linear form and hence the Bernoulli cell can be used as a basic element for the synthesis of linear circuits.

In this chapter, a log domain lossy integrator, first order low pass and high pass filter circuits based on translinear principle and also the application of Bernoulli cells like first order lossy integrator, second order filter containing zero and a third order and proposed fourth order butterworth low-pass filter circuits have been constructed. Frequency domain and time domain

responses have also been given to illustrate the performance of these circuits using PSPICE simulations.

2.2 Translinear circuit principle

2.2.1 The bipolar translinear principle

The translinear principle uses the linear relationship between the transconductance and collector current in a bipolar transistor which is given by

$$I_C \cong I_S\, e^{(V_{be}/V_T)} \tag{2.1}$$

or

$$V_{be} \cong V_T \ln(I_c/I_s) \tag{2.2}$$

The transconductance is defined as

$$\frac{\partial I_c}{\partial V_{be}} = \frac{I_s\ e^{(V_{be}/V_T)}}{V_T} = \frac{I_c}{V_T} \tag{2.3}$$

Where I_s is the saturation current of the device, and V_T is the device thermal voltage. The translinear principle applies to circuits in which a number of forward biased base-emitter (V_{be}) junctions are connected in a continuous loop. The transistors within the loop can be identified as clockwise (CW) or counter clockwise (CCW), depending on the direction of current flow through the junction. The transistors may be npn or pnp but the complete loop must satisfy the following condition [6]

(i) The number of CW npn V_{be} junctions is equal to the number of CCW npn V_{be} junctions.

(ii) The number of CW pnp V_{be} junctions is equal to the number of CCW pnp V_{be} junctions

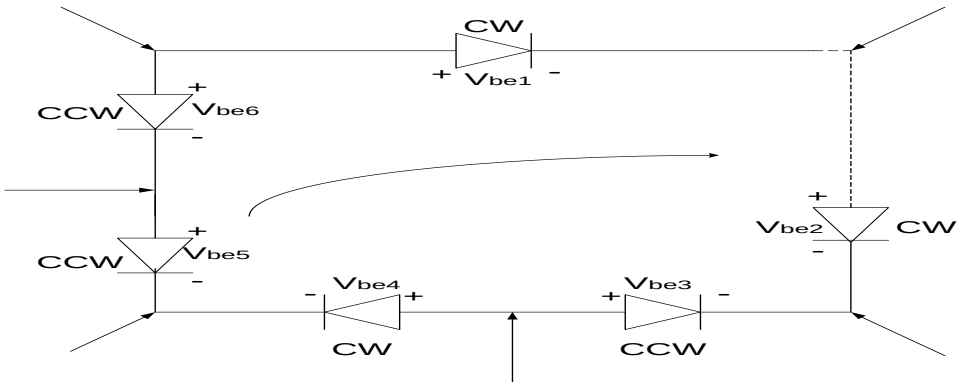

Fig.2.1 Loop diagram using diodes

By applying KVL in the circuit, we have

$$V_{be1} + V_{be2} + V_{be4} = V_{be3} + V_{be5} + V_{be6} \tag{2.4}$$

Using equation (2.2), the above relationship can be written as

$$V_T \ln\left(\frac{I_1}{I_S}\right) + V_T \ln\left(\frac{I_2}{I_S}\right) + V_T \ln\left(\frac{I_4}{I_S}\right) = V_T \ln\left(\frac{I_3}{I_S}\right) + V_T \ln\left(\frac{I_5}{I_S}\right) + V_T \ln\left(\frac{I_6}{I_S}\right) \tag{2.5}$$

or

$$V_T \ln\left[\frac{I_1}{I_S} . \frac{I_2}{I_S} . \frac{I_4}{I_S}\right] = V_T \ln\left[\frac{I_3}{I_S} . \frac{I_5}{I_S} . \frac{I_6}{I_S}\right] \tag{2.6}$$

or

$$I_1 . I_2 . I_4 = I_3 . I_5 . I_6 \tag{2.7}$$

Let us Consider a loop where there are j numbers of npn V_{be} junctions in each direction and k numbers of pnp V_{be} junctions in each direction. By generalizing the result of equation (2.4), we can write

$$\sum_{CW_j} V_{bej} + \sum_{CW_k} V_{bek} = \sum_{CCW_j} V_{bej} + \sum_{CCW_k} V_{bek} \tag{2.8}$$

$$\sum_{CW_j} V_t \ln(I_{cj}/I_{sn}) + \sum_{CW_k} V_t \ln(I_{ck}/I_{sp}) = \sum_{CCW_j} V_t \ln(I_{cj}/I_{sn}) + \sum_{CCW_k} V_t \ln(I_{ck}/I_{sp}) \tag{2.9}$$

where I_{cj} and I_{ck} represents the collector current associated with each of the V_{be} junctions within the loop. I_{sn} and I_{sp} represent the npn and pnp saturation currents respectively and can be expressed in terms of current densities ($I_{sn} = J_{sn}A$, $I_{sp} = J_{sp}A$), where J_{sn} and J_{sp} are process dependent.

$$\sum_{CW_j} \ln\left(\frac{I_{cj}}{J_{sn}A_j}\right) + \sum_{CW_k} ln(\frac{I_{ck}}{J_{sp}A_p}) = \sum_{CCW_j} \ln(\frac{I_{cj}}{J_{sn}A_j}) + \sum_{CCW_k} \ln(\frac{I_{ck}}{J_{sp}A_p}) \tag{2.10}$$

$$\prod_{CW_{j,k}} \frac{I_{cj}I_{ck}}{{J_{sn}}^j A_j {J_{sp}}^k A_k} = \prod_{CCW_{j,k}} \frac{I_{cj}I_{ck}}{{J_{sn}}^j A_j {J_{sp}}^k A_k} \tag{2.11}$$

or

$$\prod_{CW_{j,k}} \frac{I_{cj}I_{ck}}{A_j A_k} = \prod_{CCW_{j,k}} \frac{I_{cj}I_{ck}}{A_j A_k} \tag{2.12}$$

If (j + k = m), then

$$\prod_{CW_m} \frac{I_{cm}}{A_m} = \prod_{CCW_m} \frac{I_{cm}}{A_m} \tag{2.13}$$

Hence, we can say that the above equation represents bipolar translinear principle in which the product of clockwise junction current densities is equal to the product of the counterclockwise junction current densities.

2.2.2 Principles of log domain design

Translinear circuits are the fundamental structure of log-domain circuits. Fig.2.2 shows a translinear loop formed by the base-emitter junctions in bipolar transistors [6]. For the purpose of analysis, we consider all transistors to be ideal and perfectly matched having collector current given by

$$I_C \cong I_S \, e^{(V_{be}/V_T)} \tag{2.14}$$

or

$$V_{be} \cong V_T \ln(I_c/I_s) \tag{2.15}$$

where V_{be} is the base to emitter voltage, V_T is the thermal voltage (0.025V at room temperature) and I_s is the reverse saturation current.

Using the equation (2.13) (in which we have assumed equal emitter area for all the transistors), we get the following equation

$$I_1 \, . \, I_3 \, . \, I_5 = I_2 \, . \, I_4 \, . \, I_6 \tag{2.16}$$

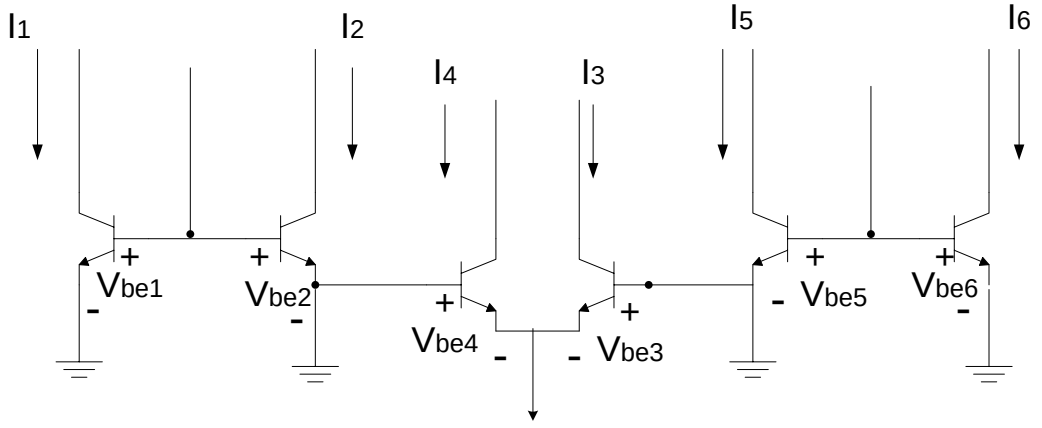

Fig.2.2 Translinear loop with CB and CE configurations

The translinear principle gives a simple rule for computing products of currents. For designing filter circuits we need to find some equation which involves time-derivative of output current in the following form

$$\dot{I_{out}} \propto I_{in} \tag{2.17}$$

By grounding the emitter (V_e = 0) and adding a capacitor C to the system yields an equation composed of current-mode variables [9]. Fig.2.3 shows such a system i.e. a basic building block of log-domain filters, in which a constant voltage V_{shift} is inserted between the capacitor node Z and the base without affecting the equation solution. Now the output current is given by

$$I_{out} = I_s \, e^{(V_{be}/V_T)} \tag{2.18}$$

$$I_{out} = I_s \, e^{(V_b - V_e/V_T)} \tag{2.19}$$

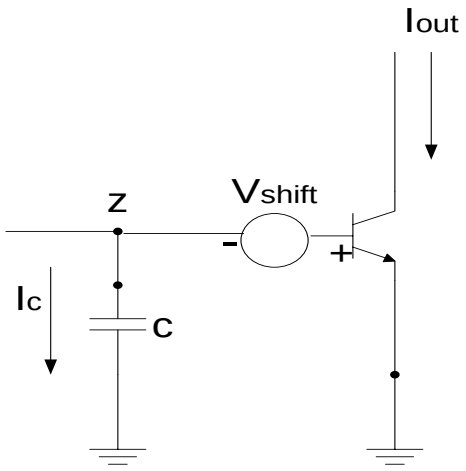

Fig.2.3 Filter pole formed using a transconductor.

On differentiating equation (2.19), we get

$$\dot{I_{out}} = \frac{1}{V_T} \, I_{out} \, \frac{d}{dt} (V_b - V_e) \tag{2.20}$$

Since I_c = C $\dot{V_{be}}$, we can write equation (2.20) as

$$\dot{I_{out}} = \frac{I_{out} I_c}{V_T \, C} \tag{2.21}$$

From this equation, we can find the derivative of a current by multiplying two currents together which can be done using a translinear loop circuit.

2.3 Synthesis of log domain blocks using translinear principle

In this section, we will discuss the applications based on translinear principle.

2.3.1 Log-domain lossy integrator

Fig.2.4 shows a log-domain lossy integrator based on the translinear principle [11]. Here we assume that each transistor has an ideal exponential characteristic. By applying KCL, the base-emitter voltage relations can be written as

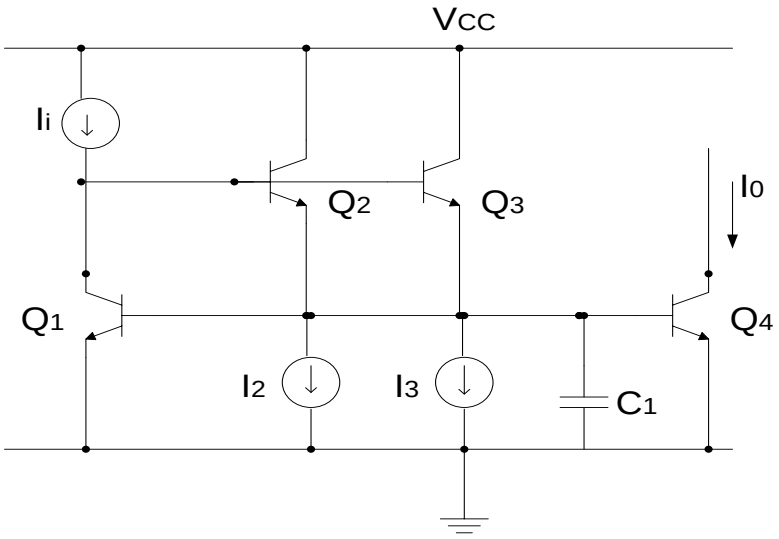

Fig.2.4 Log domain lossy integrator.

$$V_{be1} + V_{be2} - V_{be3} - V_{be4} = 0 \tag{2.22}$$

The collector current of the transistor is given by

$$I_C \cong I_S \; e^{(V_{be}/V_T)} \tag{2.23}$$

Now applying the translinear principle (TLP) to transistor Q1-Q4 as

$$I_{C1}I_{C2} = I_{C3}I_{C4} \tag{2.24}$$

If $I_{C1} = I_i$, $I_{C2} = I_2$, $I_{C4} = I_0$, then

$$I_iI_2 = I_{C3}I_0 \tag{2.25}$$

The collector current of Q3 can be expressed as

$$I_{C3} = I_3 + C_1\dot{V_{C1}} \tag{2.26}$$

The derivative of the voltage across the capacitor C_1 is given by

$$\dot{V_{C1}} = \frac{dV_{C1}}{dt} = \frac{V_T}{I_O}\frac{dI_{out}}{dt} = \frac{V_T\,\dot{I_O}}{I_O} \tag{2.27}$$

The derivative of the output current based on equation (2.23) is given by

$$\dot{I_O} = \frac{dI_O}{dt} = \frac{I_S}{V_T}\, e^{(V_{C1}/V_T)}\, \frac{dV_{C1}}{dt} = \frac{I_O \dot{V_{C1}}}{V_T} \tag{2.28}$$

Substituting equation (2.26), (2.27) and (2.28) into equation (2.24) & (2.25), we get

$$I_1 I_2 = \left(I_3 + \frac{C_1 \dot{I_O} V_T}{I_O}\right) I_O \tag{2.29}$$

Let us assume $I_2 = I_3 = I$, then equation (2.29) become

$$I_i = I_o + \frac{C_1 \dot{I_O} V_T}{I} \tag{2.30}$$

By taking the Laplace transform, the transfer function of the circuit of Fig.2.4 in s-domain can be written as

$$H(s) = \frac{I_O(s)}{I_i(s)} = \frac{1}{S\left(\frac{C_1 V_T}{I}\right) + 1} \tag{2.31}$$

From equation (2.31), we can say that H(s) corresponds to the transfer function of a lossy integrator and the pole frequency can be controlled by the bias current I.

2.3.2 Simulation results

The translinear lossy integrator simulated in PSPICE is shown in Fig.2.4. The bias currents are taken as $I_1 = I_2 = 50$ uA. The power supply voltage is taken as 2.5V and capacitance is taken as $C_1 = 50$ pF.

The transient and frequency responses of the Fig.2.4 are shown in Fig.2.5 (a) to Fig.2.5(c).

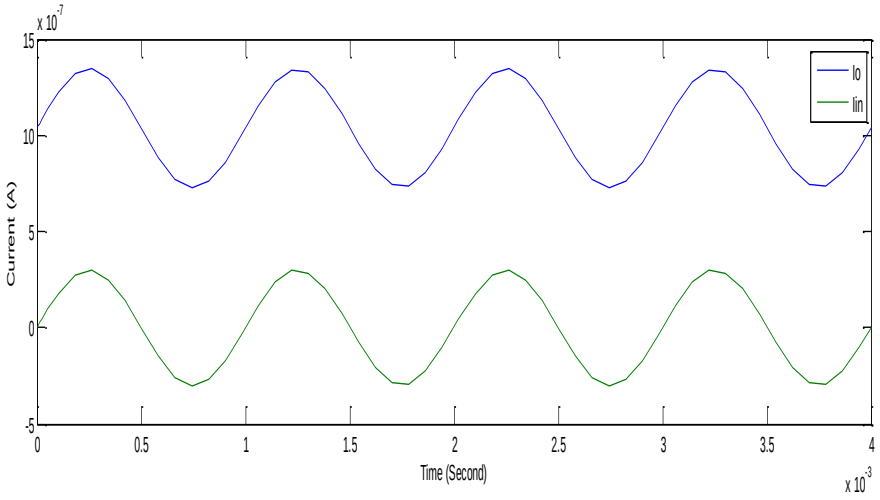

Fig.2.5 (a) Time response of lossy integrator.

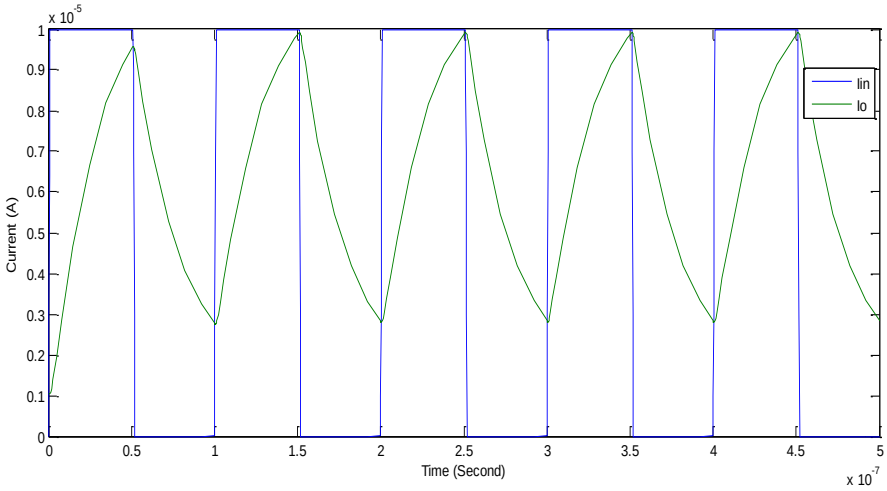

Fig.2.5 (b) Integrator output for frequency (f_{in}) = 1MHZ of lossy integrator.

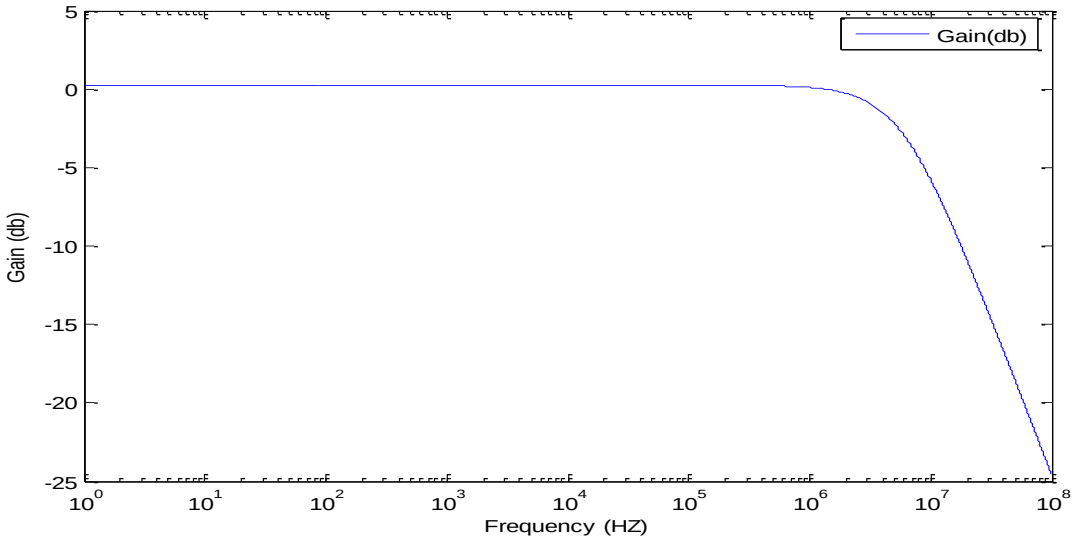

Fig.2.5 (c) Frequency response of lossy integrator.

By PSPICE simulation, we get pole frequency = 5.7 MHZ which is close to the theoretically pole frequency = 6.1 MHZ.

2.3.3 First-order log domain filter

The dynamic translinear circuit principle has been used to realize first order log domain filters [12] .The circuit given below in Fig.2.6 has been used to realize this filter.

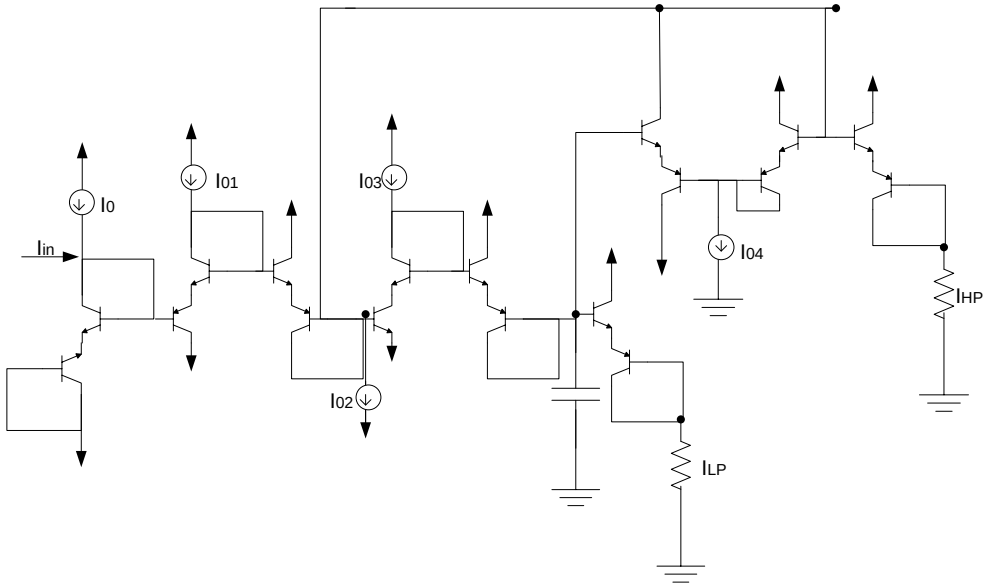

Fig. 2.6 Log domain high pass and low pass first order filter.

The current through the capacitor is given by

$$C\frac{dV_o}{dt} = I_O\, e^{\left[\frac{(V_{in}-V_o)}{2V_T}\right]} \tag{2.32}$$

From Fig.2.6 the current-mode transfer functions [9] is given by

$$T_{LP} = H\frac{w_o}{s+w_o} \tag{2.33}$$

$$T_{HP} = H\frac{s}{s+w_o} \tag{2.34}$$

The pole frequency (w_o) and gain (H) of the given filter in terms of bias current are given below

$$w_o = \frac{1}{2V_T C}\left(\frac{I_{03}I_{04}}{I_{02}}\right) \tag{2.35}$$

$$H_{HP} = \frac{I_{01}}{I_{02}} \tag{2.36}$$

$$H_{LP} = \frac{I_{01}}{I_{03}} \tag{2.37}$$

From equations (2.35) to (2.37), it is seen that the filter parameters are tunable through the respective biasing currents. The pole frequency (w_o) can be adjusted by I_{02}, I_{03} and I_{04} and also H_{LP} and H_{HP} can be tuned by I_{01}without disturbing w_o[12].

2.3.4 Simulation results

The first order high pass and low pass filter is simulated in PSPICE to check the workability. The circuit is designed for a pole frequency of 1.59 MHZ, Q =1 and H=1. The value of parameters are selected as C = 200 pF and I_{01}= I_{02}= I_{03}= I_{04}= 100 uA with V_{CC}= 3V. The current signal is taken across load resistor of 1 ohm. The time responses of low pass and high pass filter are shown in Fig.2.7 (a) and Fig.2.7 (b).

Fig.2.7 (c) and Fig.2.7 (d) shows the simulation results of low pass and high pass filter. The tuning characteristics for low pass and high pass filters are observed by varying respective bias currents. Fig.2.7 (e) and Fig.2.7 (f) shows the variation of gain and also Fig.2.7 (g) and Fig.2.7 (h) shows the variation of pole frequency. The pole frequency using PSPICE simulation for low pass and high pass filter comes out to be 1.78 MHZ and 1.23 MHZ respectively which is close to the theoretical pole frequency of 1.59 MHZ.

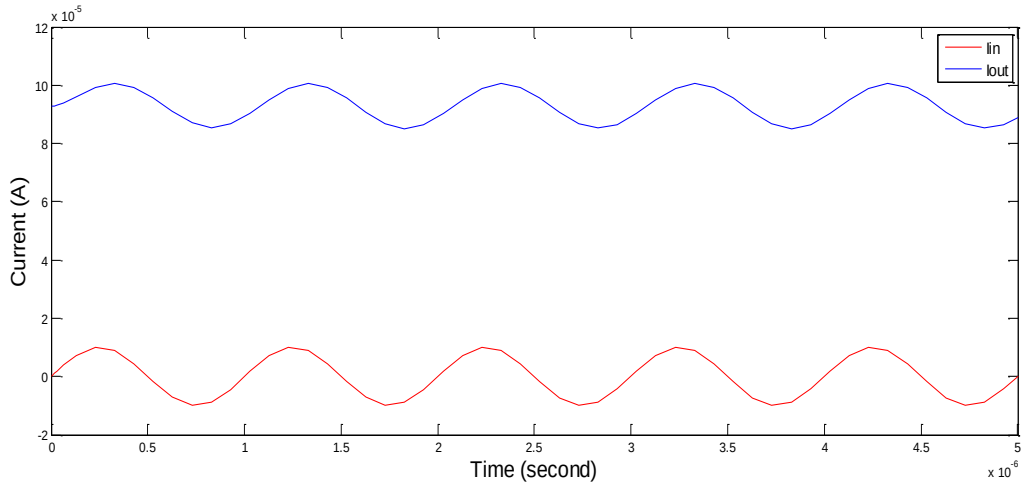

Fig.2.7 (a) Time response of low pass filter

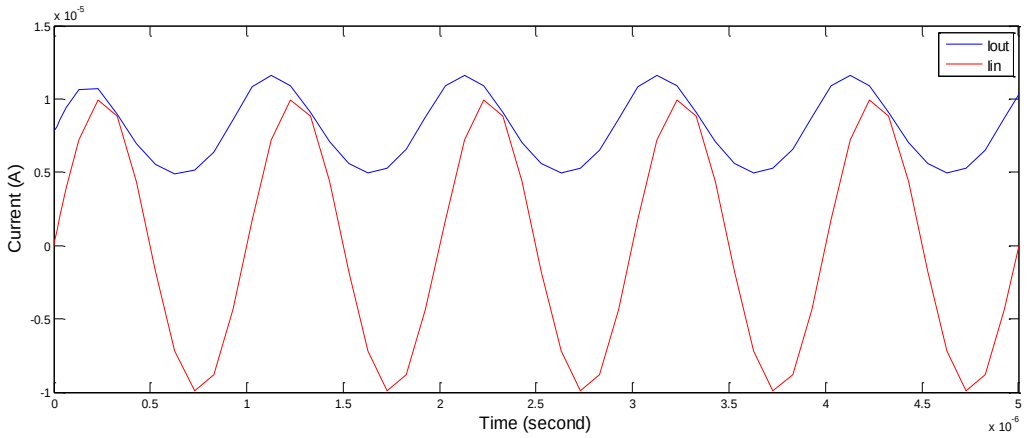

Fig.2.7 (b) Time response of high pass filter.

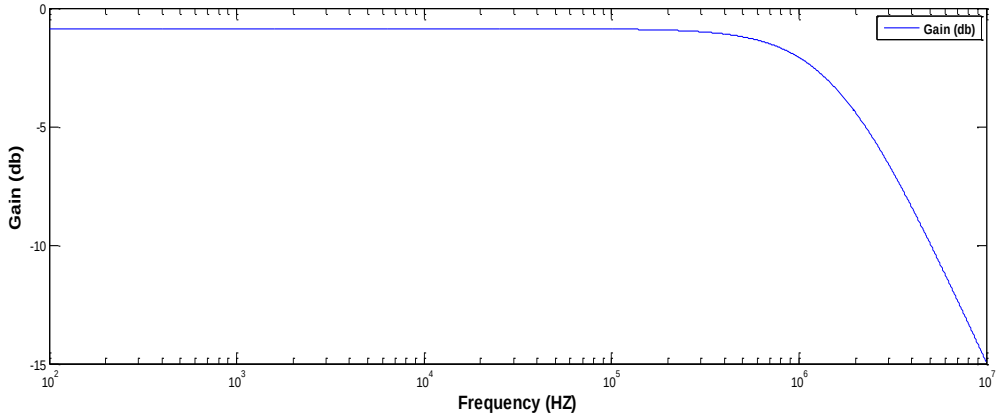

Fig.2.7 (c) Frequency response of low pass filter.

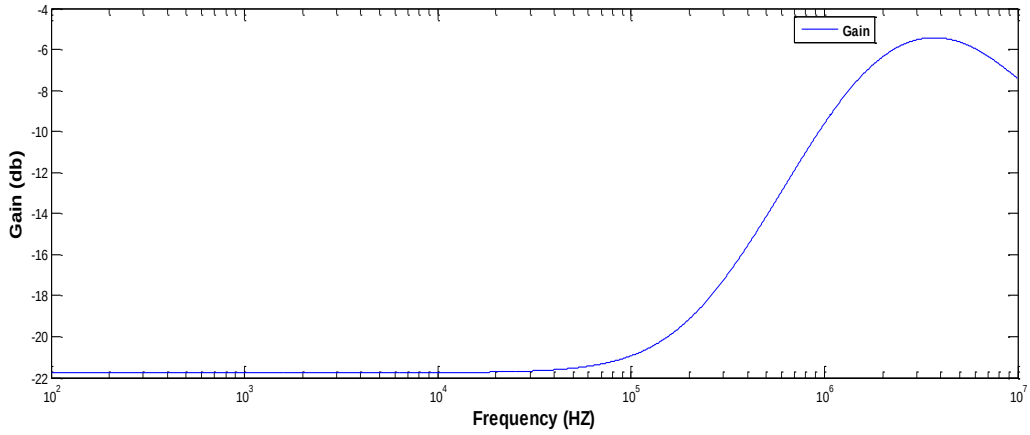

Fig.2.7 (d) Frequency response of high pass filter.

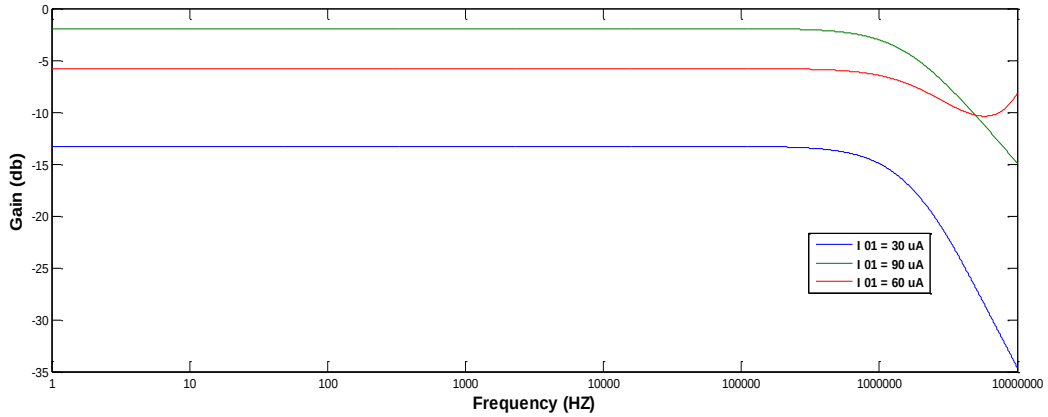

Fig.2.7 (e) Variation of gain for different values of I_{01} for low pass filter.

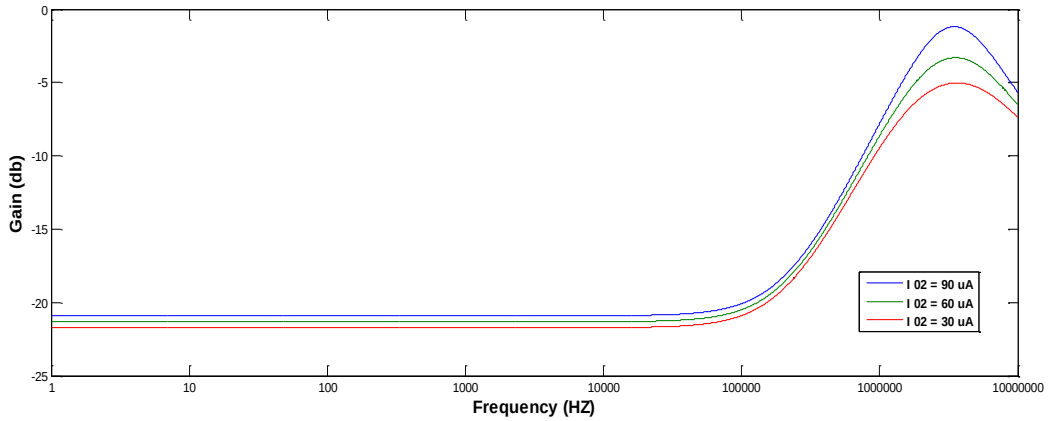

Fig.2.7 (f) Variation of gain for different values of I_{O2} for high pass filter.

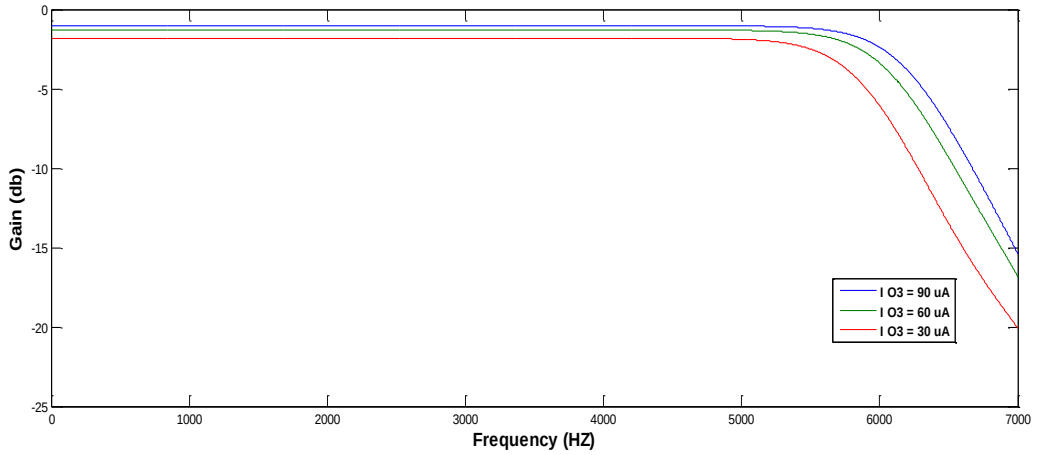

Fig.2.7 (g) Variation of pole frequency for different values of I_{O3} for low pass filter.

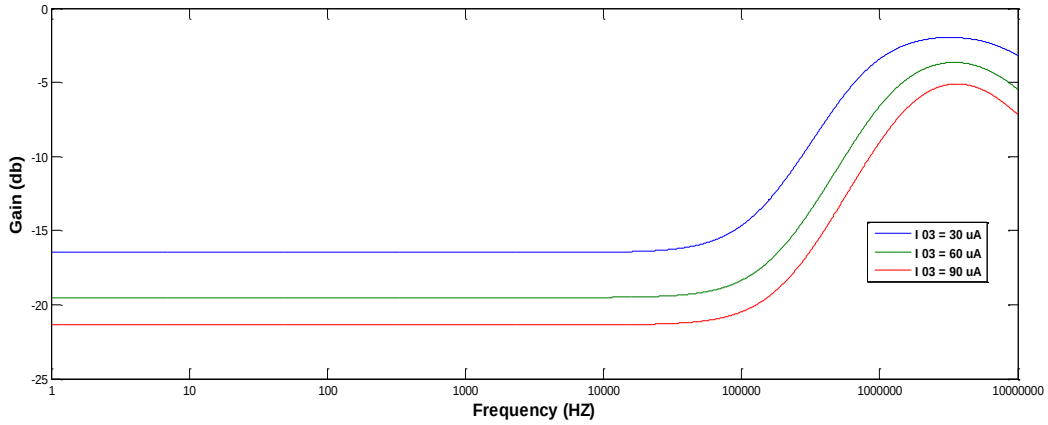

Fig.2.7 (h) Variation of pole frequency for different values of I_{O3} for high pass filter.

2.4 A Bernoulli cell

The Bernoulli cell is a nonlinear continuous–time circuit element. The Bernoulli cell comprises an npn transistor and an emitter-connected grounded capacitor and its dynamic behavior is determined by a differential equation. The collector current can be represented in form of Bernoulli's general non-linear differential equation. Bernoulli cell approach allows the transformation of a frequency domain transfer function into time domain transfer function which can be directly implemented by translinear (TL) loops [7]. By changing the suitable variables, Bernoulli's equation can be converted to a linear form and hence the Bernoulli cell can be used as a basic element for the synthesis of linear circuits.

The Bernoulli cell is formed by connecting a grounded capacitor of value C at the emitter of a forward-biased npn BJT as shown in Fig.2.8. The collector current I_C obeys the exponential law given below

$$I_C\,(t) = I_S\, e^{\,[(V_B(t) - V_C(t)/V_T]} \tag{2.38}$$

Where I_S is reverse saturation current, $V_B(t)$ is base voltage, $V_C(t)$ is capacitor voltage and V_T is thermal voltage, then

$$\frac{dV_C(t)}{dt} = \dot{V_C}(t) = i_c(t)/C = \ [I_C(t) - u(t)]/C \tag{2.39}$$

Differentiation of (2.38) yields the following nonlinear differential equation

$$\dot{I_C(t)} - \left(\frac{\dot{V_B(t)}}{V_T} + \frac{u(t)}{CV_T}\right) I_C(t) + \frac{(I_C(t))^2}{CV_T} = 0 \tag{2.40}$$

Equation (2.40) represents Bernoulli form and Fig.2.8 shows Bernoulli Cell. Equation (2.40) is nonlinear and can be linearized by a nonlinear substitution

$$I_C(t) = 1/P(t) \neq 0 \tag{2.41}$$

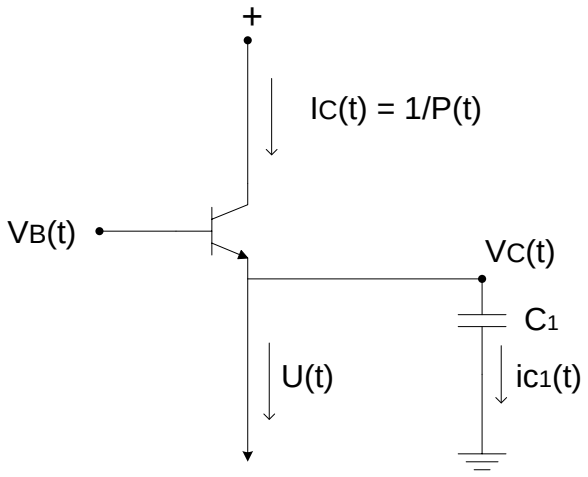

Fig.2.8 A Bernoulli cell

Equation (2.40) reduces to

$$\frac{dP(t)}{dt} + \left(\frac{\dot{V_B}(t)}{V_T} + \frac{u(t)}{CV_T}\right) \mathrm{P(t)} - \frac{1}{CV_T} = 0 \tag{2.42}$$

Equation (2.42) is a linear first order differential equation. Variables V_B (t) and u (t) are "free" parameters.

Let us considered a translinear loop of even number of 2m base emitter junctions (where emitter junction is forward biased).

$$\mathrm{CW} \prod_{j=1}^{m} I_j(t) = \mathrm{CCW} \prod_{j=1}^{m} \grave{I}_J(\mathrm{t}) \tag{2.43}$$

where $\mathrm{I_j(t)}$ represents the collector currents in clockwise (CW) direction and $\grave{\mathrm{I}}_\mathrm{J}(\mathrm{t})$ represents the collector currents in counter clockwise (CCW) direction [7]. If we assume $\mathrm{I_C(t)} = \mathrm{I_k(t)}$, then P(t) $= \frac{1}{I_C(t)} = \frac{1}{I_k(t)}$.

So, finally we can write

$$\mathrm{P(t)} = \frac{1}{I_C(t)} = \frac{1}{I_k(t)} = \frac{\mathrm{CW} \prod_{j=1}^{m,(j\neq k)} I_j(t)}{\mathrm{CCW} \prod_{j=1}^{m} \grave{I}_J(\mathrm{t})} \tag{2.44}$$

2.5 A Bernoulli cell in log domain structures

2.5.1 A single input-driven Bernoulli cell

A single input driven Bernoulli cell is shown in Fig.2.9. Input current I_{in} can be converted to a logarithmically compressed voltage V_B as

$$\dot{V_B} = V_T \frac{\dot{I_{in}(t)}}{I_{in}(t)} = V_T \frac{d}{dt} [\ln(I_{in}(t)] \tag{2.45}$$

By substituting equation (2.45) into (2.42) gives

$$CV_T \frac{d}{dt} \{\ln[P(t)\, I_{in}(t)]\} + u(t) = \frac{1}{P(t)} = I_C(t) \tag{2.46}$$

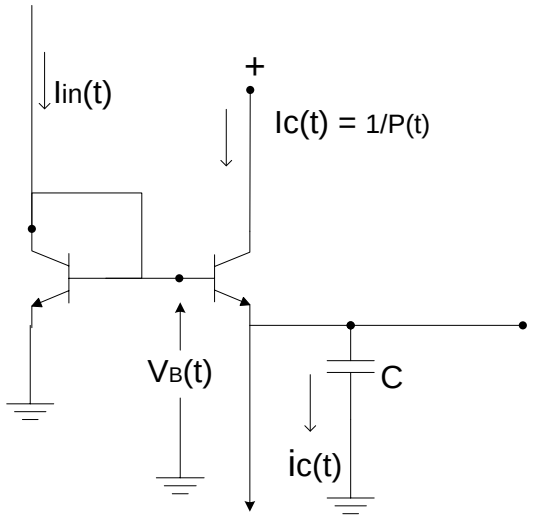

Fig.2.9 A single input driven Bernoulli cell

The capacitor current can be written as

$$i_C(t) = C\, V_T \frac{d}{dt} \{\ln[P(t)\, I_{in}(t)]\} \tag{2.47}$$

2.5.2 Interconnection of Bernoulli cell

In Fig.2.10 (a), two Bernoulli cells are connected by a voltage level shifter Q_{01}[8]. For the first cell, we can write

$$C_1 V_T \frac{d}{dt} \{\ln[P_1(t)\, I_{in}(t)]\} + u_1(t) = \frac{1}{P_1(t)} = I_{C1}(t) \tag{2.48}$$

The linearized expression for the second cell according to equation (2.42) is given by

$$\frac{dP_2(t)}{dt} + \left(\frac{\dot{V_{B2}(t)}}{V_T} + \frac{u_2(t)}{C_2 V_T}\right) P_2(t) - \frac{1}{C_2 V_T} = 0 \tag{2.49}$$

where $I_{C2}(t) = \frac{1}{P_2(t))}$, and C_2 is the capacitor value of the second Bernoulli Cell. From equation (2.47), we can write

$$\frac{dV_{C1}(t)}{dt} = V_T \frac{d}{dt} \{\ln[P_1\ (t)\ I_{in}(t)]\} \tag{2.50}$$

From equation (2.49), we can write

$$C_2 V_T \frac{d}{dt} \{\ln[P_2\ (t)\ P_1(t)\ I_{in}(t)]\} + u_2\ (t) = \frac{1}{P_2(t)} = I_{C2}(t) \tag{2.51}$$

Hence, generalizing the equation (2.51) for mth cell, we can write

$$C_m V_T \frac{d}{dt} \{\ln[P_m\ (t)\ P_{m-1}(t) \ldots\ldots P_1\ (t)\ I_{in}(t)]\} + u_m\ (t) = \frac{1}{P_m(t)} = I_{Cm}(t)$$

(2.52)

And capacitor currents of mth Bernoulli cell is given by

$$i_{C1}(t) = C_1 V_T \frac{d}{dt} \{\ln[P_1(t)\ I_{in}(t)]\}$$

$$i_{C2}(t) = C_2 V_T \frac{d}{dt} \{\ln[P_2(t) P_1(t)\ I_{in}(t)]\}$$

……

$$i_{Cm}(t) = C_m V_T \frac{d}{dt} \{\ln[P_m(t) \ldots . P_2(t) P_1(t)\ I_{in}(t)]\}$$

$$i_{Cm}(t) = C_m V_T \frac{d}{dt} \left\{\ln\left[\left[\prod_{j=1}^{m} P(t)\right] I_{in}(t)\right]\right\} \tag{2.53}$$

Now, by substituting the products of $P_k(t) \ldots . P_1(t) I_{in}(t)$, a new variable $w_k(t)$ is given by

$$w_k(t) = \left[\prod_{j=1}^{k} P_k(t)\right] I_{in}(t) = P_k(t) w_{k-1}(t) \tag{2.54}$$

From equation (2.53), we can write

$$i_{C1}(t) = C_1 V_T \frac{d}{dt} \{\ln[w_1(t)]\}$$

$$i_{C2}(t) = C_2 V_T \frac{d}{dt} \{\ln[w_2(t)]\}$$

…….

$$i_{Cm}(t) = C_m V_T \frac{d}{dt} \{\ln[w_m(t)]\} \tag{2.55}$$

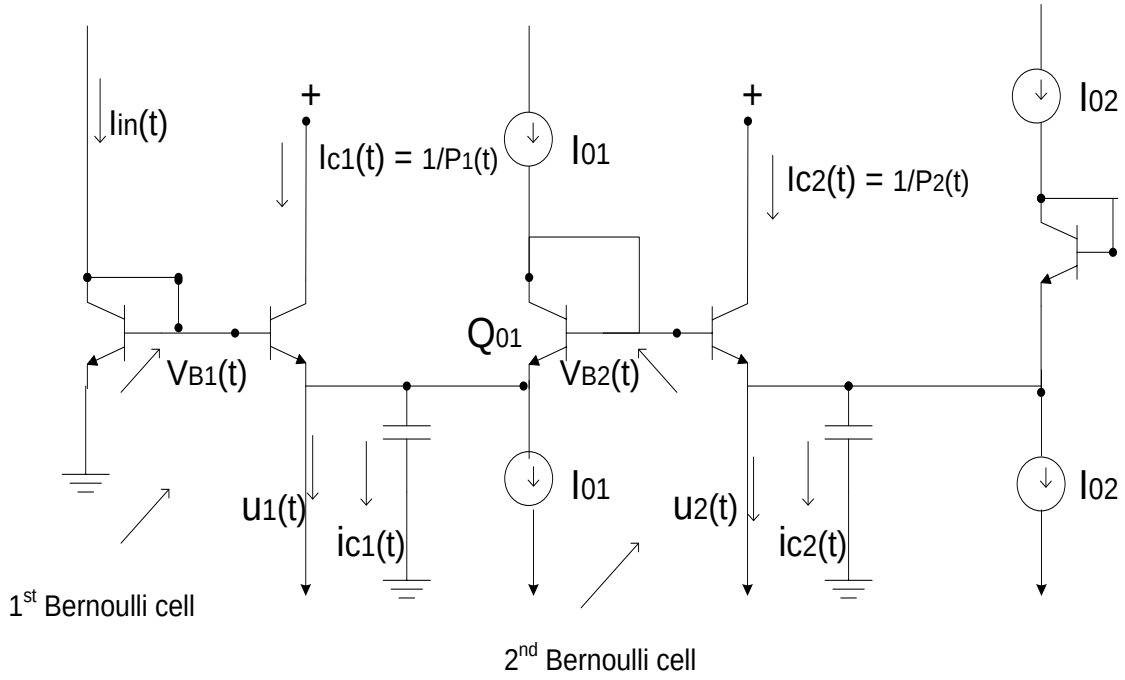

Fig.2.10 (a) Two interconnected Bernoulli cell

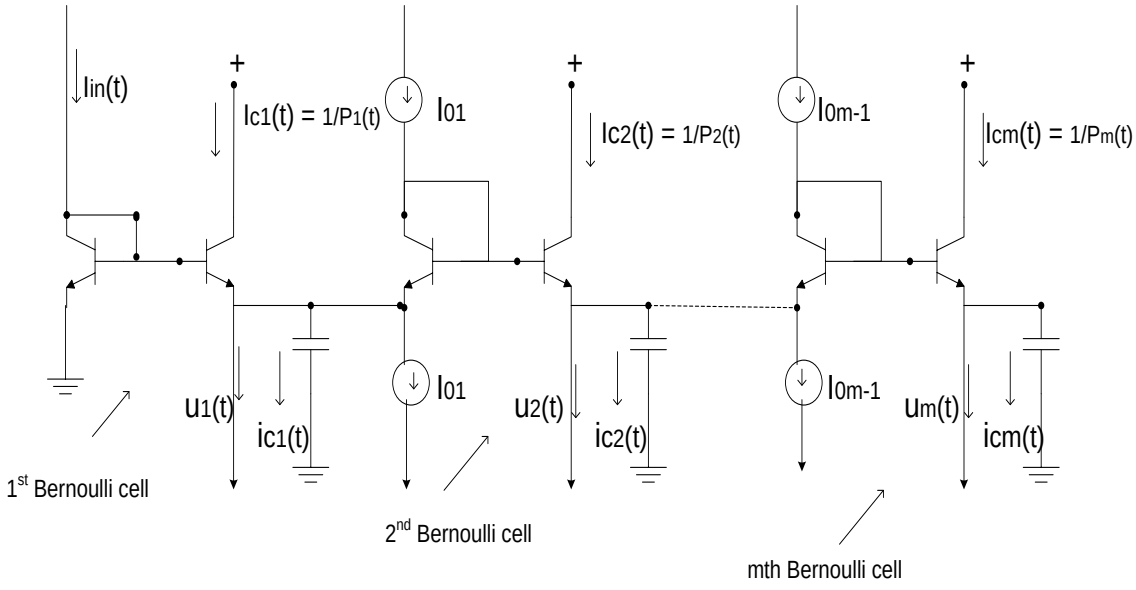

Fig.2.10 (b) Cascaded Bernoulli cell

The identification of the variable $w_k(t)$ used for the analysis of higher order filter is given by

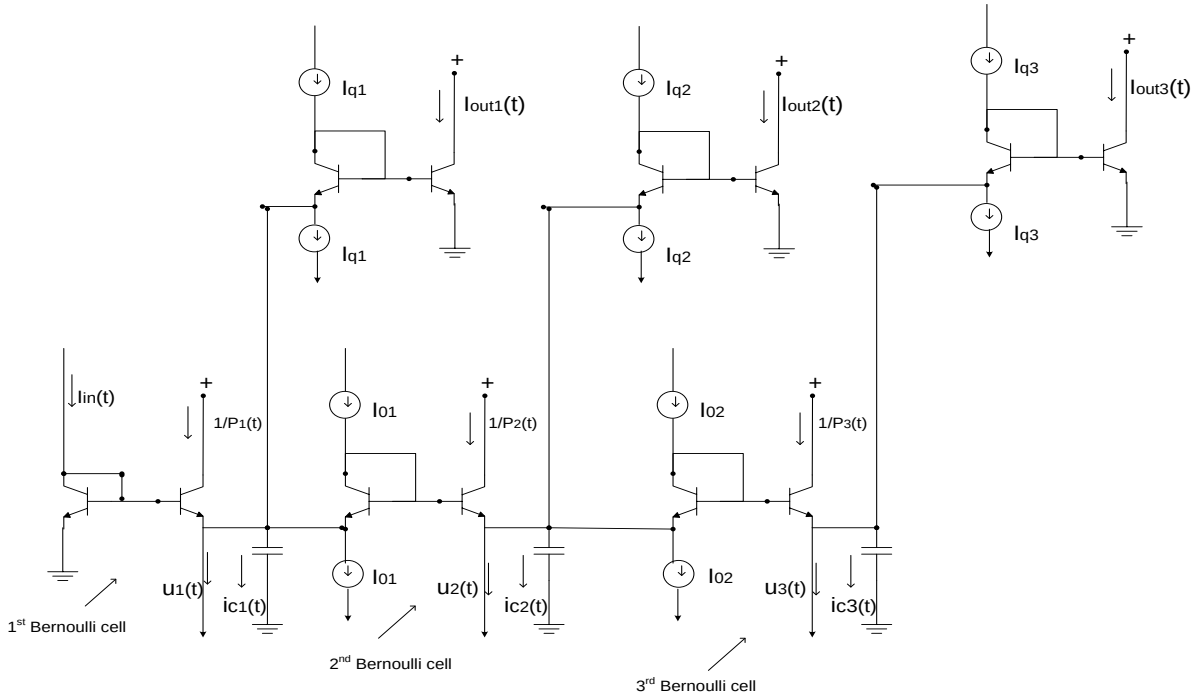

Fig.2.11 Identification of variable $w_k(t)$ for a cascade of Bernoulli cell

Finally by equation (2.55), we can write

$$w_1(t) = u_1\, e^{(V_{C1}(t)/V_T)}$$

$$w_2(t) = u_2\, e^{(V_{C2}(t)/V_T)}$$

……

$$w_m(t) = u_m\, e^{(V_{Cm}(t)/V_T)} \qquad (2.56)$$

where $u_1, u_2, \ldots u_m$ are constant in time quantities and $V_{C1}(t), V_{C2}(t), \ldots, V_{Cm}(t)$ are the capacitor node voltages. u_1 is dimensionless and the dimensions of u_m is $[amp]^{-(m-1)}$.

2.6 Applications of Bernoulli cell

In this section, we will discuss the application of Bernoulli cell in log domain filters.

2.6.1 Log domain lossy integrator

Let us assume that the desired lowpass frequency response is given by [13]

$$\frac{I_{out}(s)}{I_{in}(s)} = \frac{k}{s + w_0} \tag{2.57}$$

Lossy integrator is shown in Fig.2.12.

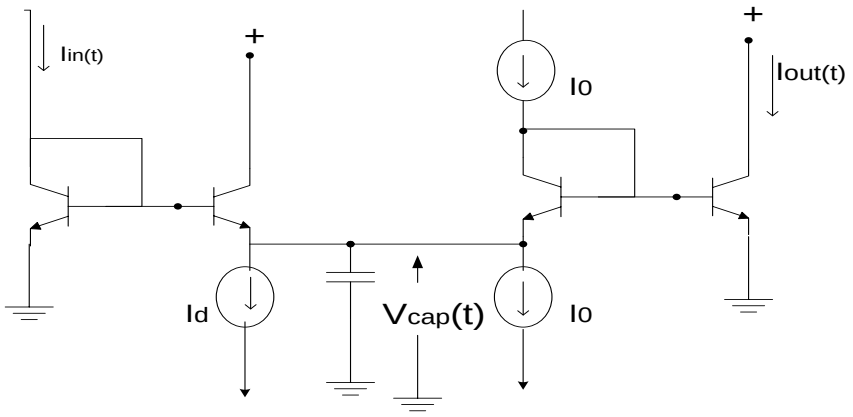

Fig.2.12 A log domain lossy integrator

In time domain, we can write

$$I_{out}(t) = I_S\, e^{\left[\frac{V_T\, ln(I_O/I_S) + V_{cap}}{V_T}\right]} = I_O\, e^{\left(\frac{V_{cap}}{V_T}\right)} \tag{2.58}$$

or $$I_d + \mathrm{C}\, \dot{V_{cap}} = I_S\, e^{\left[\frac{V_T\, ln(I_{in}/I_S) - V_{cap}}{V_T}\right]} = I_{in}\, e^{\left(\frac{-V_{cap}}{V_T}\right)} \tag{2.59}$$

From equation (2.58) and (2.59), we get

$$\frac{d}{dt}\left[e^{\left(\frac{V_{cap}}{V_T}\right)}\right] = e^{\left(\frac{V_{cap}}{V_T}\right)}\left(\frac{\dot{V_{cap}}}{V_T}\right) \tag{2.60}$$

So, we can write

$$I_d\, \frac{I_{out}}{I_0} + (\mathrm{C}\, V_T)\, \frac{\dot{I_{out}}}{I_0} = I_{in} \tag{2.61}$$

So, in Laplace form, we can write

$$\frac{I_{out}(s)}{I_{in}(s)} = \frac{(I_O/\mathrm{C}\, V_T)}{s + (I_d/\mathrm{C}\, V_T)} \tag{2.62}$$

2.6.2 Simulation results

To prove the theoretical validity, lossy integrator of Fig.2.12 is simulated with PSPICE program. The coefficients were solved for C = 40 pF , $I_d = I_0 = 100$ uA having cut off frequency of 14.8 MHZ which is close to the theoretical cut off frequency of 15.2 MHZ. The integrator response and frequency responses are shown in Fig.2.13 (a) to Fig.2.13 (c).

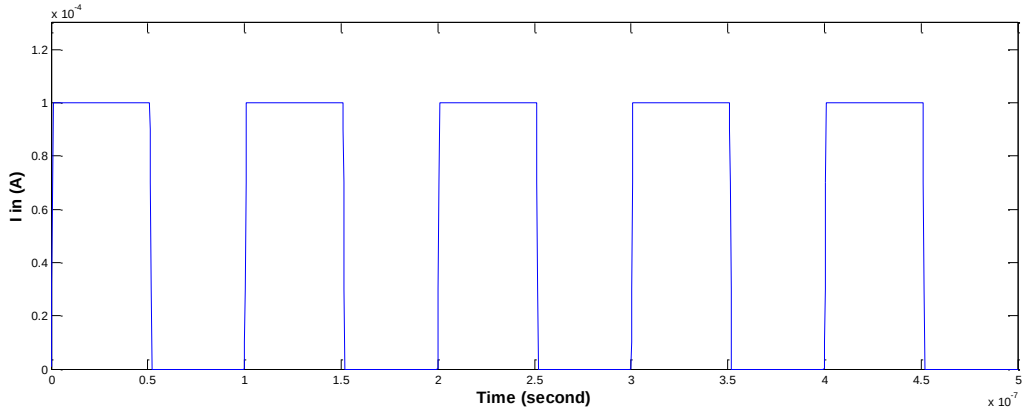

Fig.2.13 (a) Input frequency of 10 MHZ for lossy integrator.

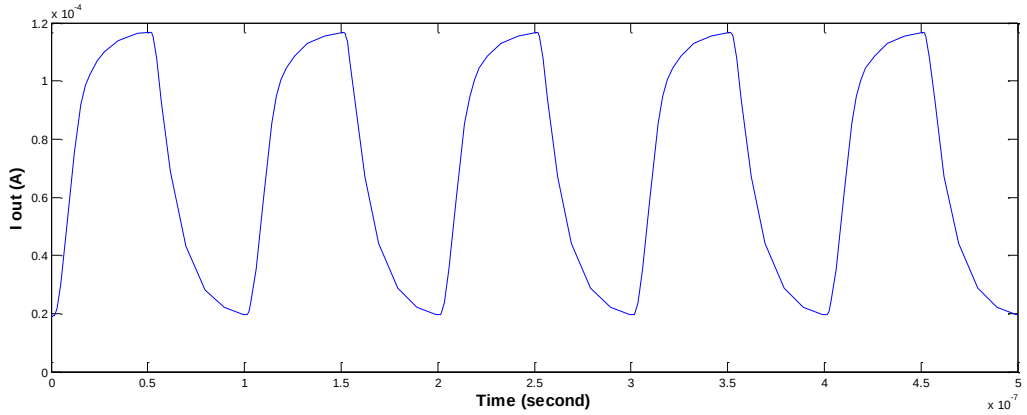

Fig.2.13 (b) Integrator response for lossy integrator.

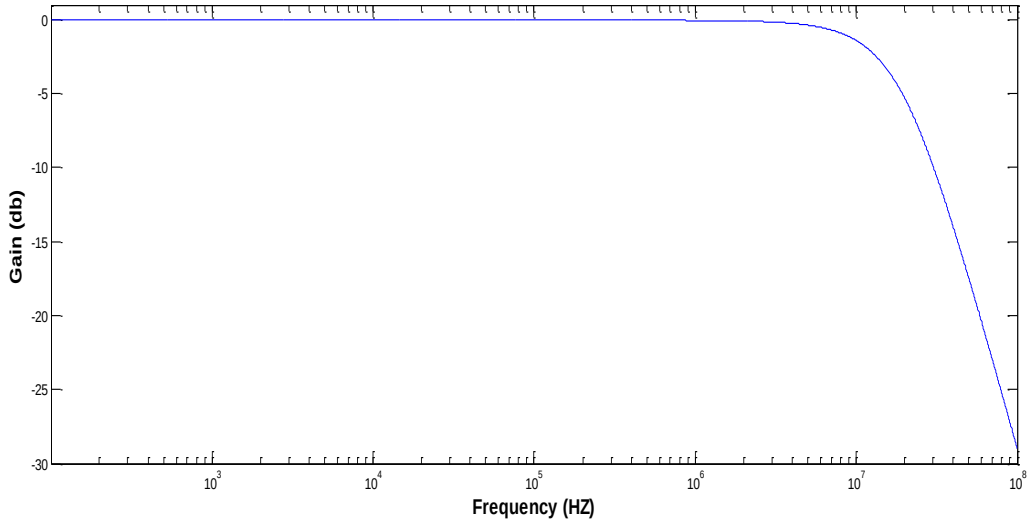

Fig.2.13 (c) Frequency response for lossy integrator

2.6.3 Second order filter containing zero

Let us assume that the desired Transfer function is given by [7]

$$\frac{I_{out}(s)}{I_{in}(s)} = \frac{ks + ak}{s^2 + as + b} \tag{2.63}$$

In time domain, we can write

$$\frac{I_{out}(t)}{I_{in}(t)} = \frac{k\frac{d}{dt}[\ln(I_{in})] + ak}{\frac{d}{dt}[\ln(\dot{I_{out}})]\left\{\frac{d}{dt}[\ln(I_{out})]\right\} + a\frac{d}{dt}[\ln(I_{out})] + b} \tag{2.64}$$

Here, after assuming $\frac{d}{dt}\left[\ln(\dot{I_{out}})\right] = \frac{i_{c2}}{CV_T}$ and $\frac{d}{dt}[\ln(I_{out})] = \frac{i_{c1}}{CV_T}$. The problem regarding wheather the term $\frac{d}{dt}[\ln(I_{in})]$ would be substituted for $\frac{i_{c2}}{CV_T}$ or $\frac{i_{c1}}{CV_T}$ is solved by assigning a subscript j at each s-term converting it to s_j.

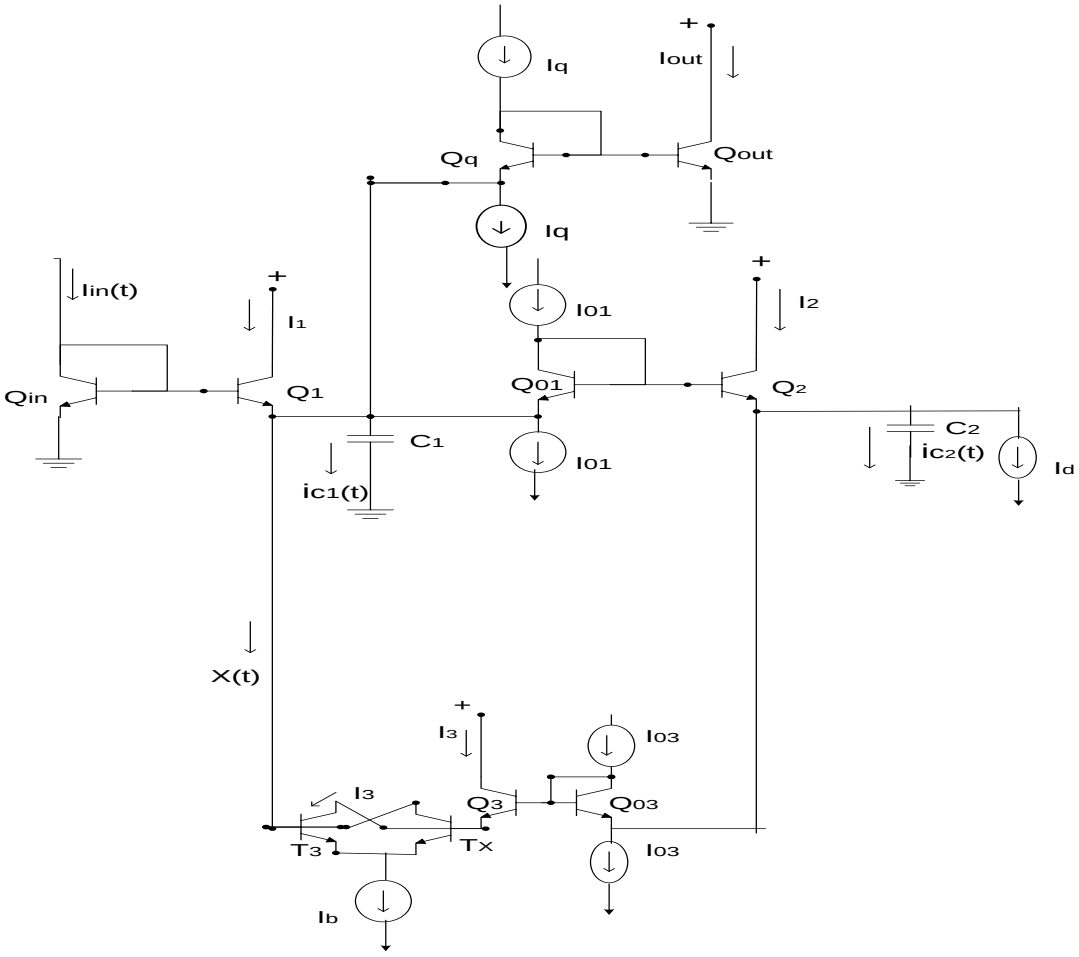

Fig.2.14 Second order filter circuit containing zero.

So, we can write

$$\frac{I_{out}(s)}{I_{in}(s)} = \frac{ks + ak}{s^2 + as + b} = \frac{k}{s + \frac{b}{S_2 + a}} = \frac{ks_2 + ak}{s_1\, s_2 + as_1 + b} \tag{2.65}$$

Thus the terms $\frac{d}{dt}[\ln(I_{in})]$ and $\frac{d}{dt}\left[\ln(\dot{I_{out}})\right]$ can be substituted for $\frac{i_{c2}}{CV_T}$ if $\frac{d}{dt}[\ln(I_{out})]$ is equal to $\frac{i_{c1}}{CV_T}$. So, the final time domain transfer function can be written as [10]

$$\frac{I_{out}(t)}{I_{in}(t)} = \frac{\grave{k}\,(\,i_{c2} + a\,CV_T\,)}{i_{c1}\,i_{c2} + i_{c1}(\,a\,CV_T) + b\,(CV_T)^2} = \frac{\grave{k}}{i_{c1} + \frac{b\,(CV_T)^2}{i_{c2} + (\,a\,CV_T)}} \tag{2.66}$$

Let us assume

$$\frac{b\,(CV_T)^2}{i_{c2}+(\,a\,CV_T)} = \text{x (t)} \tag{2.67}$$

So, time domain transfer function can be written as

$$\frac{I_{out}(t)}{I_{in}(t)} = \frac{\grave{k}}{i_{c1}+\text{x(t)}} = \frac{k\,(CV_T)}{i_{c1}+\text{x(t)}} \tag{2.68}$$

The second order circuit containing zero is shown in Fig.2.14.

Equation (2.67) corresponds to the translinear loop formed by Q_{01} T_3 T_X Q_3 Q_{03} Q_2 and equation (2.68) corresponds to the translinear loop formed by $Q_{in}Q_1$ Q_q Q_{out} .

2.6.4 Simulation results

To prove the theoretical validity, Second order filter containing zero in Fig.2.14 is simulated with PSPICE program. The coefficients were solved for C = 5 pF having loss of 40db in next decade. The time response is shown in Fig.2.15 (a) and Fig.2.15 (b).

The frequency response of Second order filter containing zero for

(a) $I_d = 5$ uA , $I_q = 4.33$ uA , $I_{01} = I_{03} = 5$uA having Pole frequency = 4 MHZ is shown in Fig.2.15 (c).

(b) $I_d = 4.33$ uA , $I_q = I_{01} = I_{03} = 5$ uA having Pole frequency = 4.4 MHZ is shown in Fig.2.15 (d).

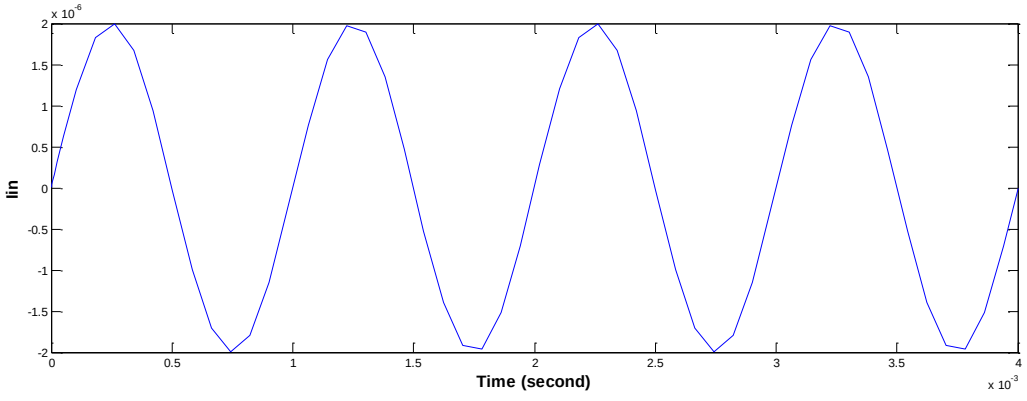

Fig.2.15 (a) Time response for input of second order filter.

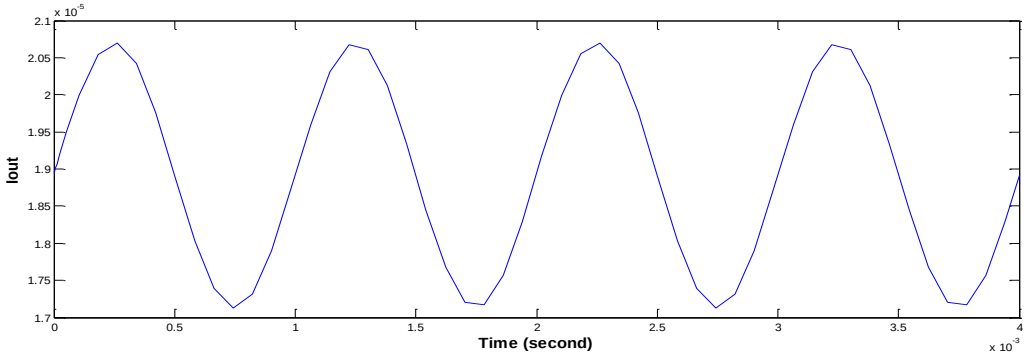

Fig.2.15 (b) Time response for output of second order filter.

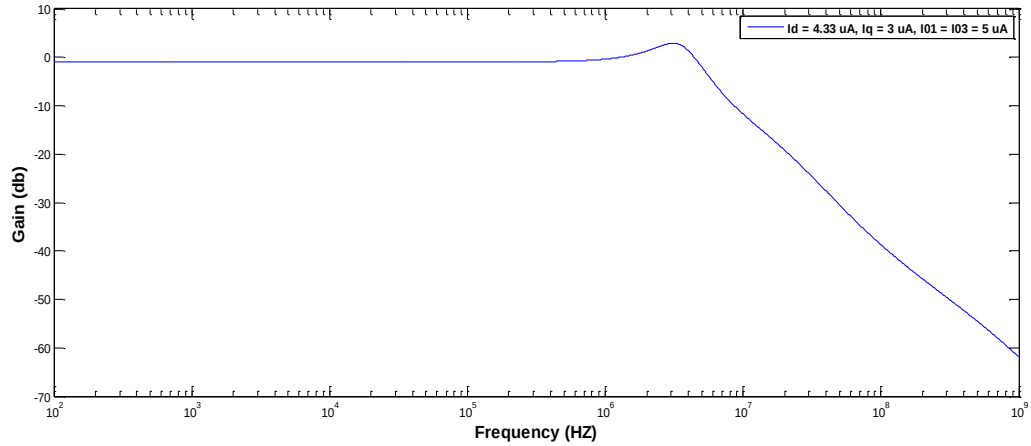

Fig.2.15 (c) Frequency response of second order filter for f_0 = 4 MHZ.

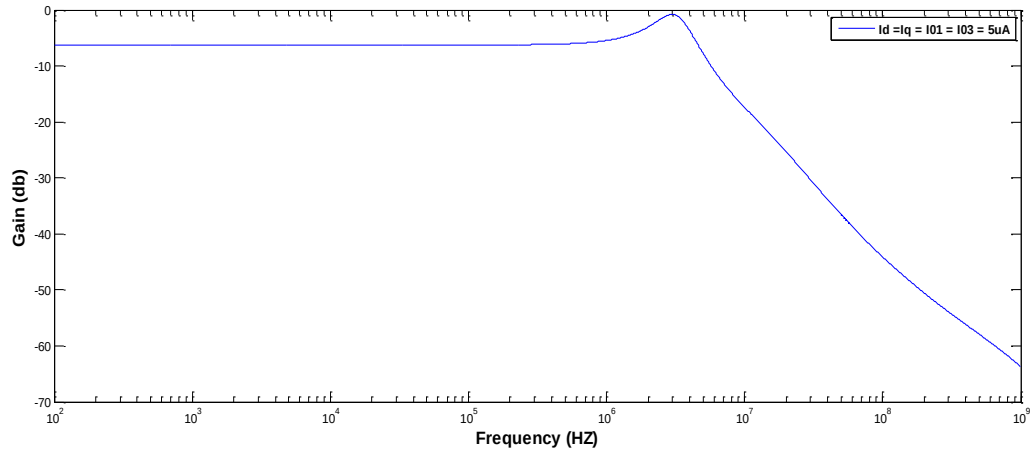

Fig.2.15 (d) Frequency response of second order filter for f_0 = 4.4 MHZ.

2.6.5 Third order low pass Butterworth filter

Let us assume that the desired lowpass frequency response is given by [7]

$$\frac{I_{out}(s)}{I_{in}(s)} = \frac{b_m}{s^3 + as^2 + bs + b_0} \tag{2.69}$$

In time domain, we can write

$$\frac{I_{out}(t)}{I_{in}(t)} = \frac{b_m}{b_0 + b\left\{\frac{d}{dt}[\ln(I_{out})]\right\} + a\left\{\frac{d}{dt}[\ln(I_{out})]\right\}\left\{\frac{d}{dt}[\ln(\dot{I_{out}})]\right\} + \left\{\frac{d}{dt}[\ln(I_{out})]\right\}\left\{\frac{d}{dt}[\ln(\dot{I_{out}})]\right\}\left\{\frac{d}{dt}[\ln(\ddot{I_{out}})]\right\}} \tag{2.70}$$

By expressing all term of form $\frac{d}{dt}[\ln(\,)]$ and using equation (2.55) and equation (2.69), we can write

$$\frac{I_{out}(t)}{I_{in}(t)} = \frac{b_m}{b_0 + b\frac{i_{c1}}{CV_T} + a\frac{i_{c1}\,i_{c2}}{(CV_T)^2} + \frac{i_{c1}\,i_{c2}\,i_{c3}}{(CV_T)^3}} \tag{2.71}$$

or in fraction form, we can write

$$\frac{I_{out}(t)}{I_{in}(t)} = \frac{\frac{\frac{b_m(CV_T)^3}{i_{c3}+(aCV_T)}}{i_{c2}+\frac{b(CV_T)^2}{i_{c3}+(aCV_T)}}}{i_{c1} + \frac{\frac{b_0(CV_T)^3}{i_{c3}+(aCV_T)}}{i_{c2}+\frac{b(CV_T)^2}{i_{c3}+(aCV_T)}}} \tag{2.72}$$

Let us assume

$$\frac{b(CV_T)^2}{i_{c3}+(aCV_T)} = x_3(t) \tag{2.73}$$

and

$$\frac{(b_0/b)(CV_T)x_3}{i_{c2}+x_3} = x_2(t) \tag{2.74}$$

Equation (2.72) can be written as

$$\frac{I_{out}(t)}{I_{in}(t)} = \frac{b_m}{b_0}\frac{x_2}{i_{c1}+x_2} \tag{2.75}$$

From equation (2.71), it is clear that dimensions of quantities $b_m(CV_T)^3$, $b_0(CV_T)^3$, $b(CV_T)^2$ and aCV_T are $[amp]^3$, $[amp]^3$, $[amp]^2$ and [amp] respectively .

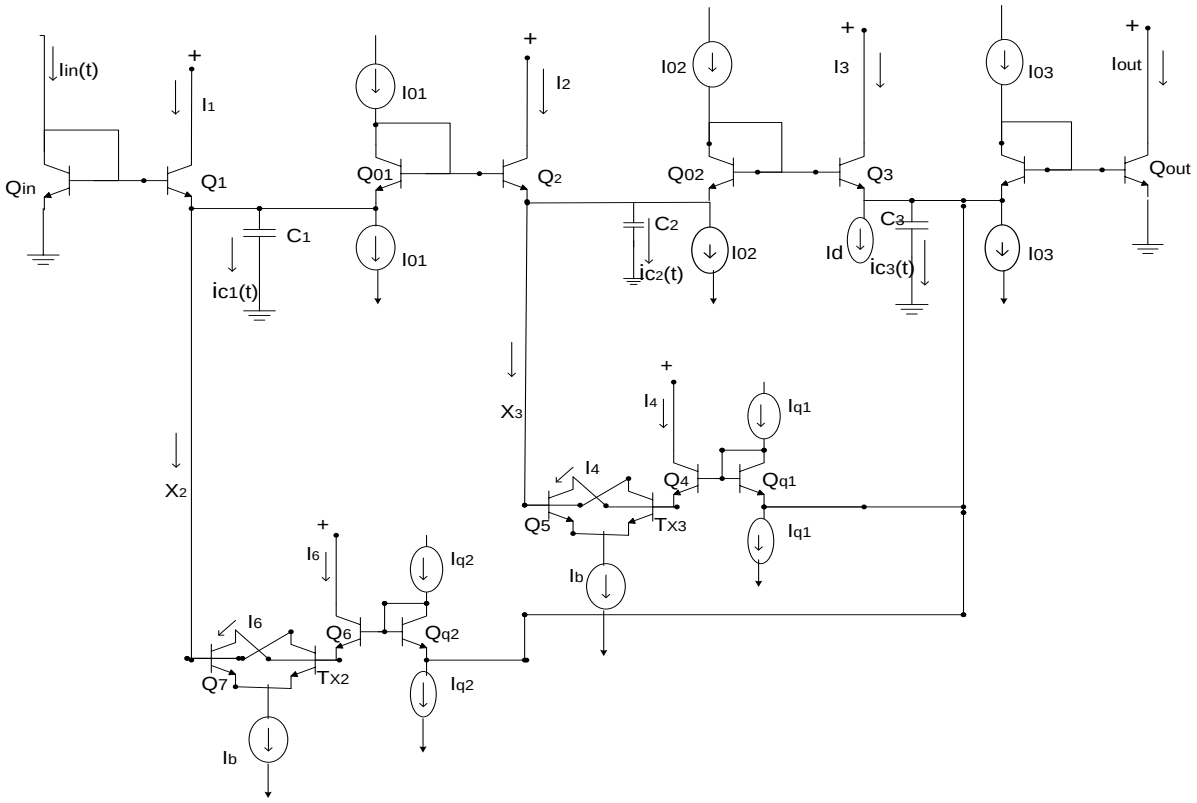

Fig.2.16 Third order Butterworth filter circuit.

Let we assume $u_1(t) = x_2(t)$, $u_2(t) = x_3(t)$, $u_3(t) = I_d = a\,CV_T$ and $I_{01}\ I_{02}\ I_{03} = b_m(CV_T)^3$.

The third order butterworth filter is shown in above Fig.2.16. Translinear loop formed by the equation (2.73) is $Q_{02}Q_5T_{X3}Q_4Q_{q1}Q_3$ when $I_{02}\ I_{q1} = b(CV_T)^2$, while equation (2.75) corresponds to loop formed by $Q_{in}Q_1Q_7T_{X2}Q_6Q_{q2}Q_{03}Q_{out}$ when $\frac{I_{03}}{I_{q2}} = \frac{b_m}{b_0}$.

2.6.6 Simulation Results

To prove the theoretical validity, Third order Butterworth filter in Fig.2.16 is simulated with PSPICE. The coefficients were solved for C = 40 pF having loss of 60 db in next decade. The values of the coefficients are $I_d = aCV_T = 10.9$ uA, $I_{02}I_{q1} = b(CV_T)^2 = 59.3\ (uA)^2$, $I_{01}I_{02}I_{03} = b_m(CV_T)^3 = 161.4(uA)^3$ and $\frac{I_{03}}{I_{q2}} = \frac{b_m}{b_0} = 1$. The time response is shown in Fig.2.17 (a) and Fig.2.17 (b).

The frequency response of third order Butterworth filter for

(a) $I_d = 10.9$ uA, $I_{01} = I_{03} = I_{q2} = 4.4$ uA , $I_{02} = I_{q1} = 7.7$ uA having Pole frequency = 627 KHZ is shown in Fig.2.17 (c) .

(b) $I_d = 10.9$ uA , $I_{03} = I_{q2} = 2.7$ uA , $I_{01} = I_{q1} = 5$ uA , $I_{02} = 11.9$ uA having Pole frequency = 687 KHZ is shown in Fig.2.17 (d) .

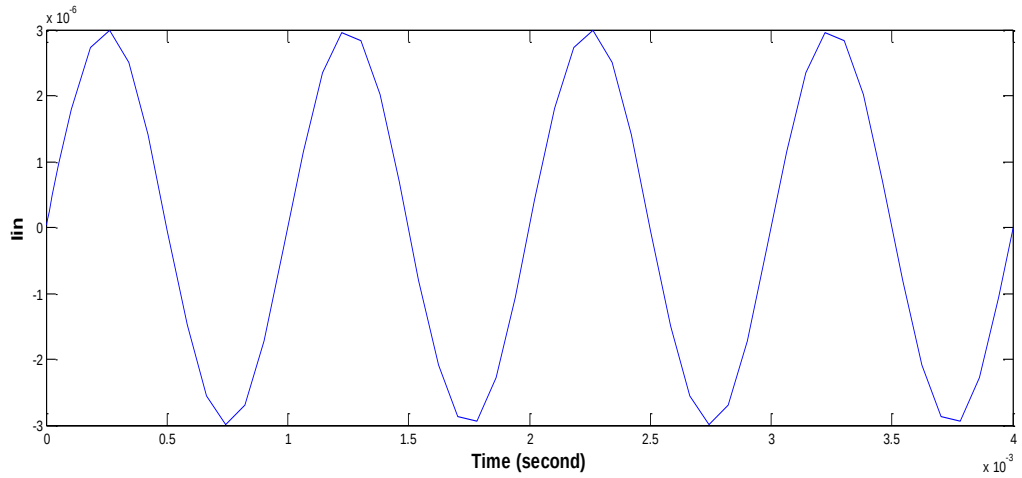

Fig.2.17 (a) Time response for input of third order Butterworth filter.

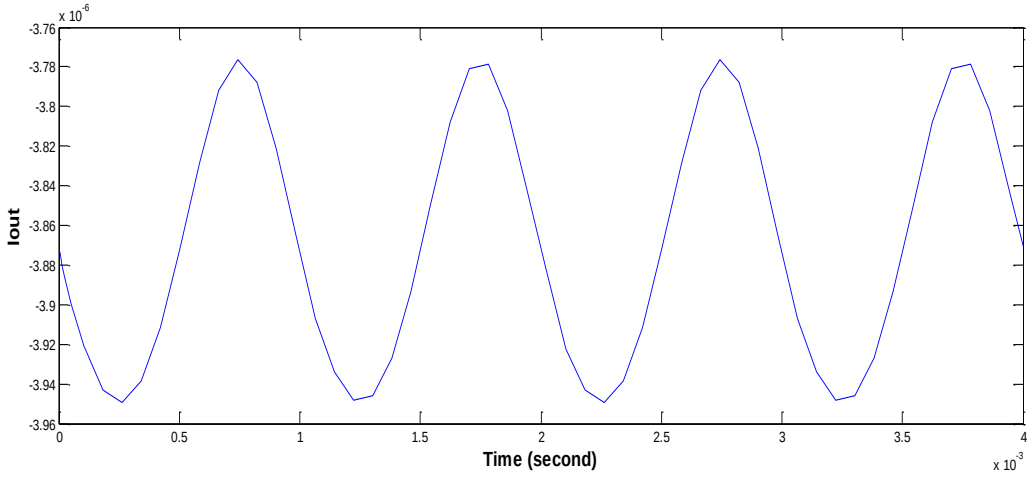

Fig.2.17 (b) Time response for output of third order Butterworth filter.

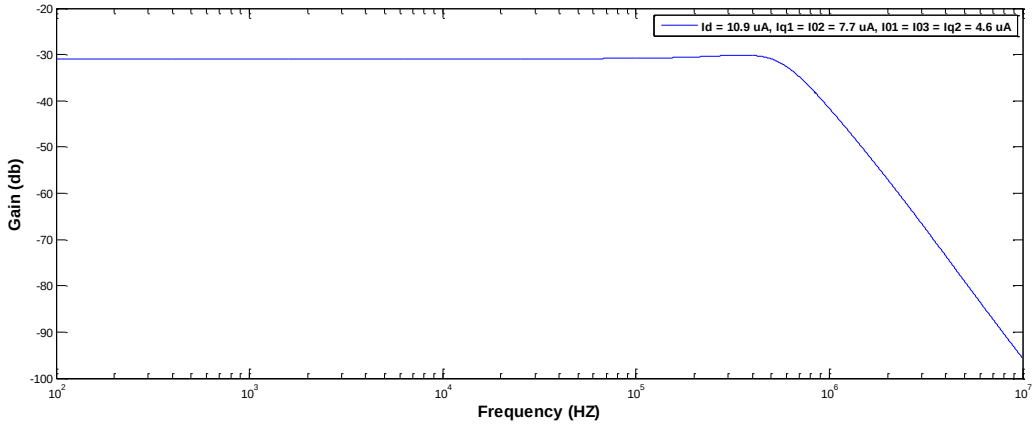

Fig.2.17 (c) Frequency response of third order Butterworth filter for f_0 = 627 KHZ.

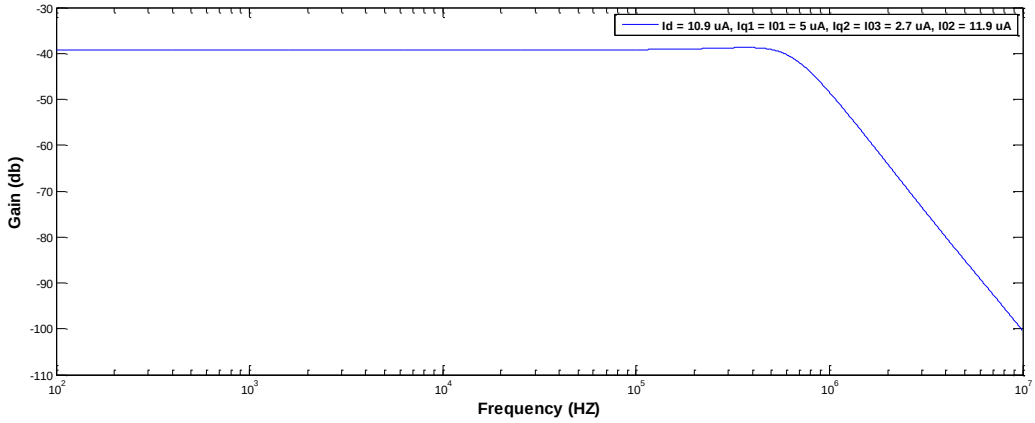

Fig.2.17 (d) Frequency response of third order Butterworth filter for f_0 = 687 KHZ.

2.6.7 Proposed fourth order low pass Butterworth filter

Let us assume that the desired lowpass frequency response is given by

$$\frac{I_{out}(s)}{I_{in}(s)} = \frac{c_m}{s^4 + as^3 + bs^2 + cs + c_0} \tag{2.76}$$

In time domain, we can write

$$\frac{I_{out}(t)}{I_{in}(t)} = \frac{c_m}{c_0 + c\left\{\frac{d}{dt}[\ln(I_{out})]\right\} + b\left\{\frac{d}{dt}[\ln(I_{out})]\right\}\left\{\frac{d}{dt}[\ln(\dot{I}_{out})]\right\} + a\left\{\frac{d}{dt}[\ln(I_{out})]\right\}\left\{\frac{d}{dt}[\ln(\dot{I}_{out})]\right\}\left\{\frac{d}{dt}[\ln(\ddot{I}_{out})]\right\} + \left\{\frac{d}{dt}[\ln(I_{out})]\right\}\left\{\frac{d}{dt}[\ln(\dot{I}_{out})]\right\}\left\{\frac{d}{dt}[\ln(\ddot{I}_{out})]\right\}\left\{\frac{d}{dt}[\ln(\dddot{I}_{out})]\right\}} \tag{2.77}$$

By expressing all term of form $\frac{d}{dt}[\ln(\ )]$, using equation (2.52) and equation (2.76), We can write

$$\frac{I_{out}(t)}{I_{in}(t)} = \frac{c_m}{c_0 + c\frac{i_{c1}}{CV_T} + b\frac{i_{c1}\,i_{c2}}{(CV_T)^2} + a\frac{i_{c1}\,i_{c2}\,i_{c3}}{(CV_T)^3} + \frac{i_{c1}\,i_{c2}\,i_{c3}\,i_{c4}}{(CV_T)^4}} \tag{2.78}$$

Let us assume

$$\frac{b(CV_T)^2}{i_{c4} + (aCV_T)} = x_4(t) \tag{2.79}$$

$$\frac{(c/b)(CV_T)x_4}{i_{c3} + x_4} = x_3(t) \tag{2.80}$$

and

$$\frac{(c_0/c)(CV_T)x_3}{i_{c3} + x_3} = x_2(t) \tag{2.81}$$

So, we can write

$$\frac{I_{out}(t)}{I_{in}(t)} = \frac{c_m}{c_0}\frac{x_2}{i_{c1} + x_2} \tag{2.82}$$

It is clear that dimensions of quantities $c_m(CV_T)^4$, $c_0(CV_T)^4$, $c(CV_T)^3$, $b(CV_T)^2$ and aCV_T are $[amp]^4$, $[amp]^4$, $[amp]^3$, $[amp]^2$ and [amp] respectively.

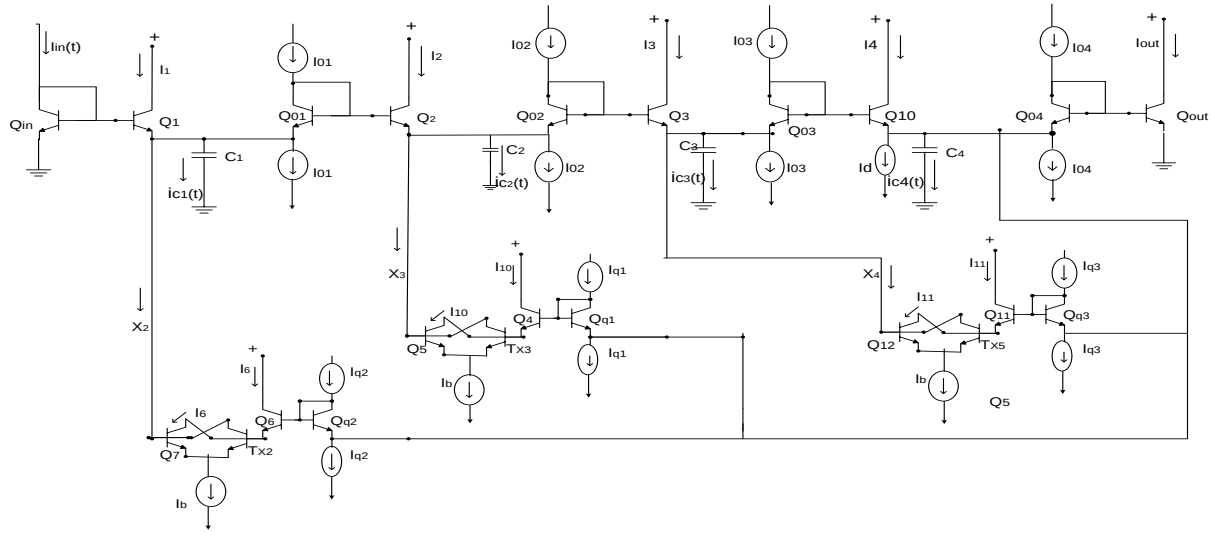

Fig.2.18 Proposed Fourth order Butterworth filter circuit.

Let us assume $u_1(t) = x_2(t)$, $u_2(t) = x_3(t)$, $u_3(t) = x_4(t)$, $u_3(t) = I_d = aCV_T$ and $I_{01}\ I_{02}\ I_{03}\ I_{04} = c_m(CV_T)^4$.

The fourth order butterworth filter is shown in above Fig2.18. Translinear loop formed by the equation (2.79) is $Q_{03}Q_{12}T_{X5}Q_{11}Q_{q3}Q_{10}$ when $I_{03}I_{q3}=b(CV_T)^2$, while equation (2.82) corresponds to loop formed by $Q_{in}Q_1\ Q_7T_{X2}\ Q_6Q_{q2}Q_4\ Q_{out}$ when $\frac{I_{04}}{I_{q2}} = \frac{c_m}{c_0}$.

2.6.8 Simulation results

To prove the theoretical validity, Fourth order Butterworth filter in Fig.2.18 is simulated with PSPICE program. The coefficients were solved for C = 40 pF having loss of 80 db in next decade. The values of the coefficients are $I_d = aCV_T = 10.9$ uA, $I_{03}\ I_{q1} = b(CV_T)^2 = 59.5\ (uA)^2$. The time response are shown in Fig.2.19 (a) and Fig.2.19 (b).

The frequency response of fourth order Butterworth filter for

(a) $I_d = 10.9$ uA, $I_{02} = I_{03} = 11.9$ uA, $I_{01} = I_{q1} = I_{q3} = 5$ uA, $I_{04} = I_{q2} = 2.7$ uA having Pole frequency = 890 KHZ is shown in Fig.2.19 (c).

(b) $I_d = 10.9$ uA, $I_{02} = I_{03} = 11.9$ uA, $I_{q1} = I_{q3} = 5$ uA, $I_{04} = I_{q2} = 2.7$ uA, $I_{01} = 15$ uA having Pole frequency = 970 KHZ is shown in Fig.2.19 (d).

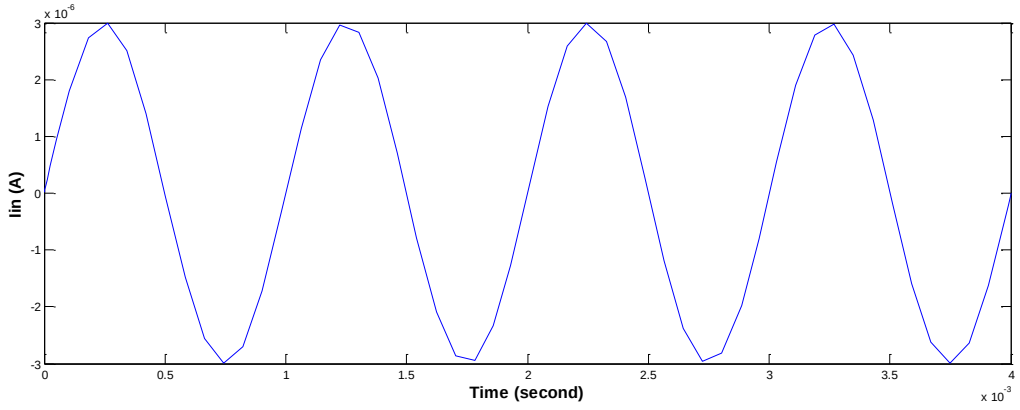

Fig.2.19 (a) Time response for input of fourth order Butterworth filter.

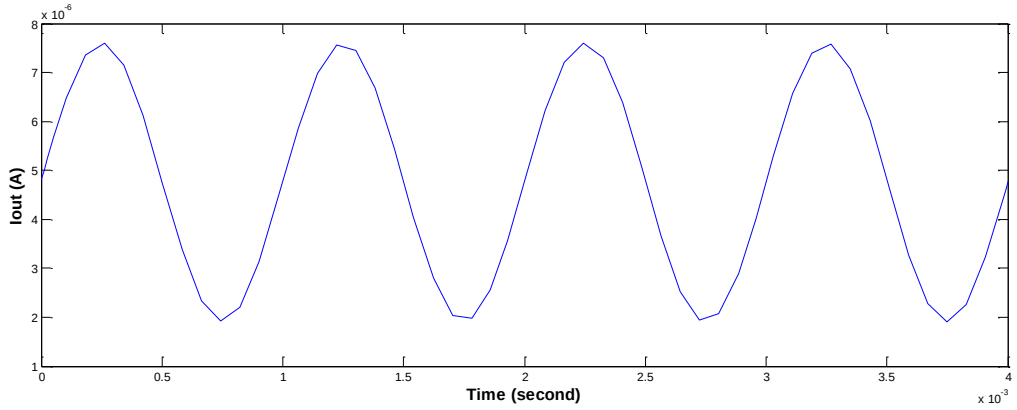

Fig.2.19 (b) Time response for output of fourth order Butterworth filter.

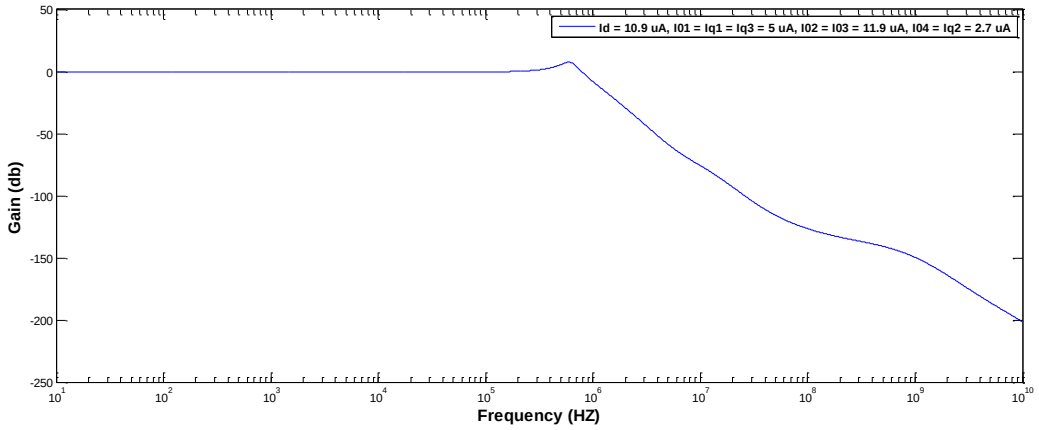

Fig.2.19 (c) Frequency response of fourth order Butterworth filter for f_0 = 890 KHZ.

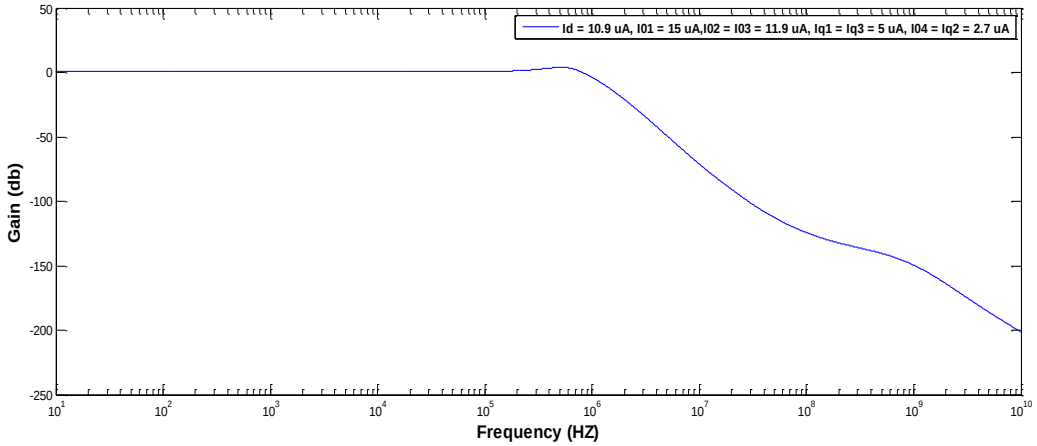

Fig.2.19 (d) Frequency response of fourth order butterworth filter for f_0 = 970 KHZ.

2.7 CONCLUSION

In this chapter, we have discussed how first order systems can be synthesized using translinear principle. Also the basic structure of Bernoulli cell and its implementation to higher order filters is discussed. The Bernoulli cell relate Translinear loops and log domain structures and proves its utility in expressing a suitable time varying form of the Translinear principle. The basic applications using translinear principle such as lossy integrator and a first order low pass and high pass log domain filter is presented. The designed filter is based on integrator loops, current sources and grounded capacitors. The gain and pole frequency are independently and electronically tunable through the variation of bias currents. Applications of Bernoulli cell like lossy integrator, second order filter containing zero, third order filters have been presented. We have designed a new fourth order low pass filter with butterworth characteristics using the Bernoulli cell. All the circuits have been tested with PSPICE simulations using the parameters of transistor AT & T CBIC-R Transistor.

Chapter 3

Design of log domain filters based on simulation of LC ladders

3.1 Introduction

Frequency shaping networks or filter is an electronic circuit that performs a frequency selection function passing the signals whose frequency spectrum lies within a specified range and stopping the signals whose frequency spectrum falls outside this range. In the previous chapters, we have discussed the log domain filters and their design by Bernoulli cell. Log domain filters can be designed by various methods. Operational simulation of LC ladder is one of these methods.

In this chapter, we will present a design of log domain filters which is based on the operational simulation of LC ladder networks [15]. The basic advantages of this method are the lowest component sensitivities over the passband and filter design at high frequency. Section 3.2 and Section 3.3 explains the basics of LC ladder filters and introduction of Log and Exp operator respectively. Section 3.4 explains the basic log domain building blocks and Section 3.5 demonstrates the design of two high-order log-domain filters i.e. third order elliptic filter and fifth order Chebyshev filter. Conclusions are drawn in Section 3.6.

3.2 Basic of LC ladder filters

3.2.1 LC ladders

LC ladders are the circuits where all components apart from source and load resistors are lossless i.e. they are capacitors and inductors that dissipate no energy [14]. LC ladders have an inherent advantage over active filters in terms of their low sensitivity to component tolerances. The basic third order LC ladder is shown in Fig.3.1 (a).

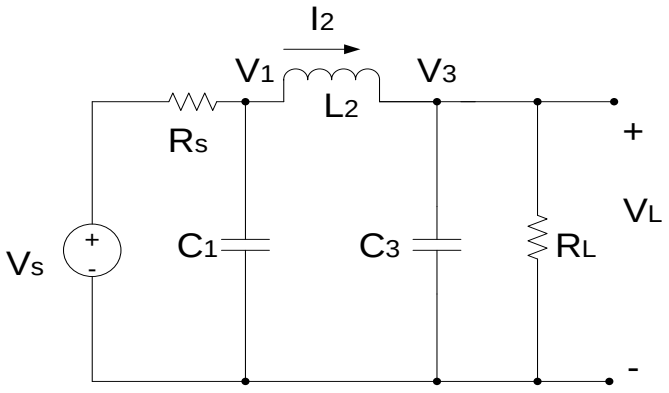

Fig.3.1 (a) A third order LC ladder

3.2.2 Signal flow graph representation of LC ladder

There are different methods for active simulations of these LC ladders namely (i) Inductor simulation using GIC's (ii) Replacement of inductor by FDNR elements (iii) Operational simulation of the LC ladder. It is this method which we have used for simulation of LC ladders. In the following, development of this method is explained briefly.

Using KCL at all capacitor nodes and KVL around each inductor branch in Fig.3.1 (a), we have following equations

$$L_2 \frac{d}{dt} I_2 = V_1 - V_3 \tag{3.1}$$

$$C_1 \frac{d}{dt} V_1 = \frac{V_S}{R_S} - \frac{V_1}{R_S} - I_2 \tag{3.2}$$

$$C_3 \frac{d}{dt} V_3 = I_2 - \frac{V_3}{R_L} \tag{3.3}$$

$$V_L = V_3 \tag{3.4}$$

Now, let us define a set of variables which will correspond to both voltages and currents.

$X_S \leftrightarrow V_S$, $X_1 \leftrightarrow V_1$, $X_2 \leftrightarrow I_2$, $X_3 \leftrightarrow V_3$, $X_L \leftrightarrow V_L$

The signal flow graph corresponding to equations (3.1) to (3.4) is shown in Fig.3.1 (b).

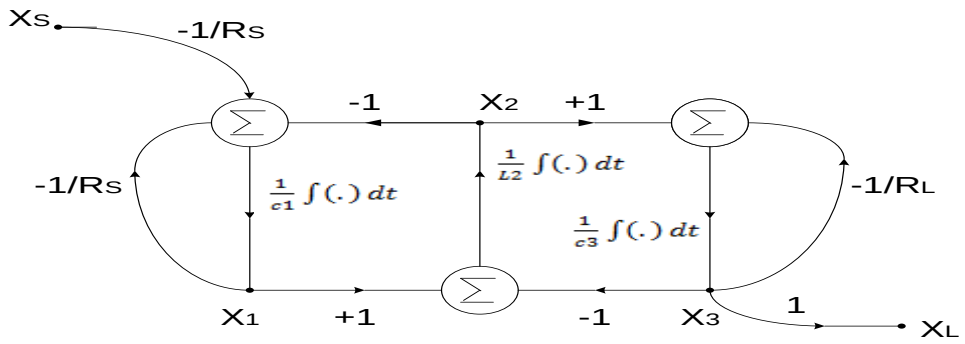

Fig.3.1 (b) Signal flow graph of Fig.3.1 (a)

3.2.3 Components needed in signal flow graph for LC ladder

(i) **Summer -** Summer is the basic building block and can be used for addition and subtraction of the node voltages and currents.

(ii) **Inverter -** Inverter can be used for changing the sign of the scaling factor.

(iii) **Nodes and branches -** Nodes represents the variables (i.e. voltage across capacitor and current in an inductor) and branch can be used for representing the transfer functions.

(iv) **Integrator -** In LC ladder, integrator can be used for applying KCL and KVL equations around inductor and capacitor respectively.

3.3 Introduction of Log and Exp operators

Log domain filters include two mathematical inverse operators i.e. Log and Exp [15]. Fig.3.2 shows a basic log domain cell in which we can write the equation which relates the voltage drop across the input-output terminals and the current I_B as

$$I_B = \mathrm{K}.\, I_0 \,.\, e^{(V_A - V_B)/2V_T} \tag{3.5}$$

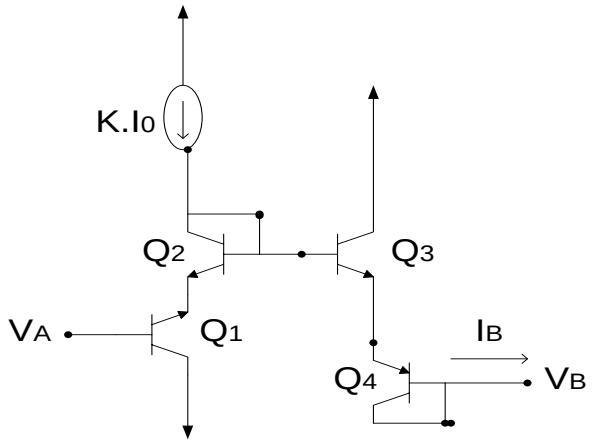

Fig.3.2 A basic log domain cell

We define the Exp function as

$$\text{Exp (x)} = I_0 \,.\, e^{X/2V_T} \tag{3.6}$$

It will be equal to equation (3.5), if K = 1 and V_B is tied to ground, so

$$I_B = I_0 \,.\, e^{V_A/2V_T} \tag{3.7}$$

Let we assume, the Log function is defined as inverse of the Exp function

$$\text{Log (Y)} = 2\, V_T \,.\, \ln\left(\frac{Y}{I_0}\right) \tag{3.8}$$

The block diagram of a linear system is shown in Fig.3.3 (a).

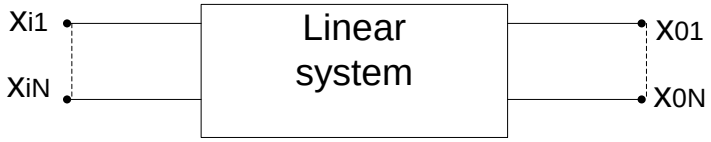

Fig.3.3 (a) Linear system

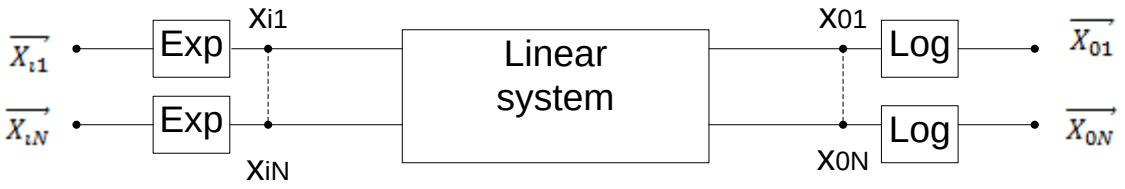

Fig.3.3 (b) Log domain structure of Fig.3.3 (a).

If in any system, Exp block appears at input and a Log block appears at output, then we have the system as shown in Fig.3.3(b).Variables marked with arrow (→) denotes the signals in log domain. It helps to easily track the signals in log domain.

One possible way to make the non-linear system to linear is to place Log blocks preceding each input and Exp blocks after each output as shown in Fig.3.4 (a) to Fig.3.4 (c).

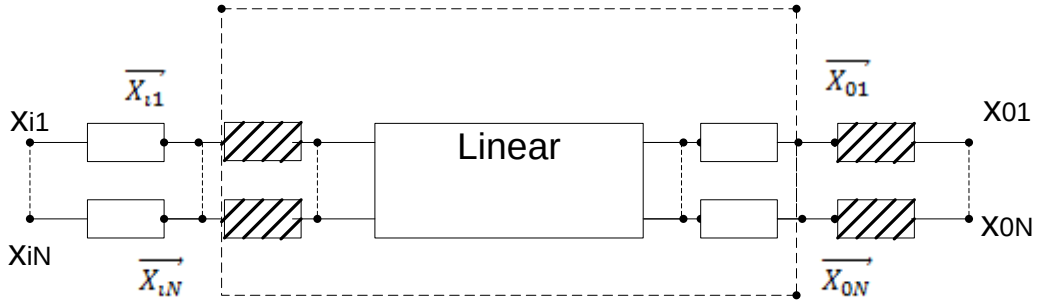

Fig.3.4 (a)

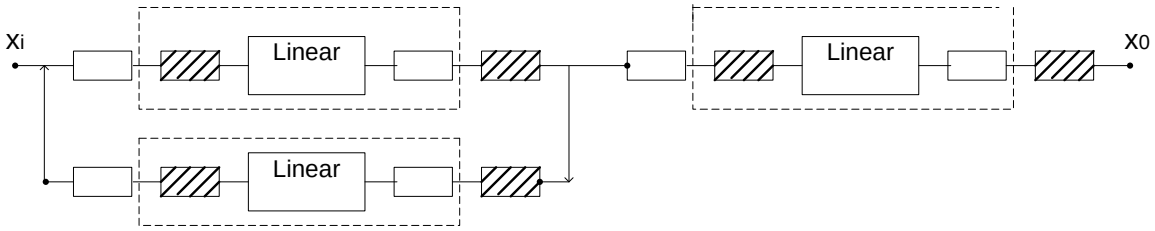

Fig.3.4 (b)

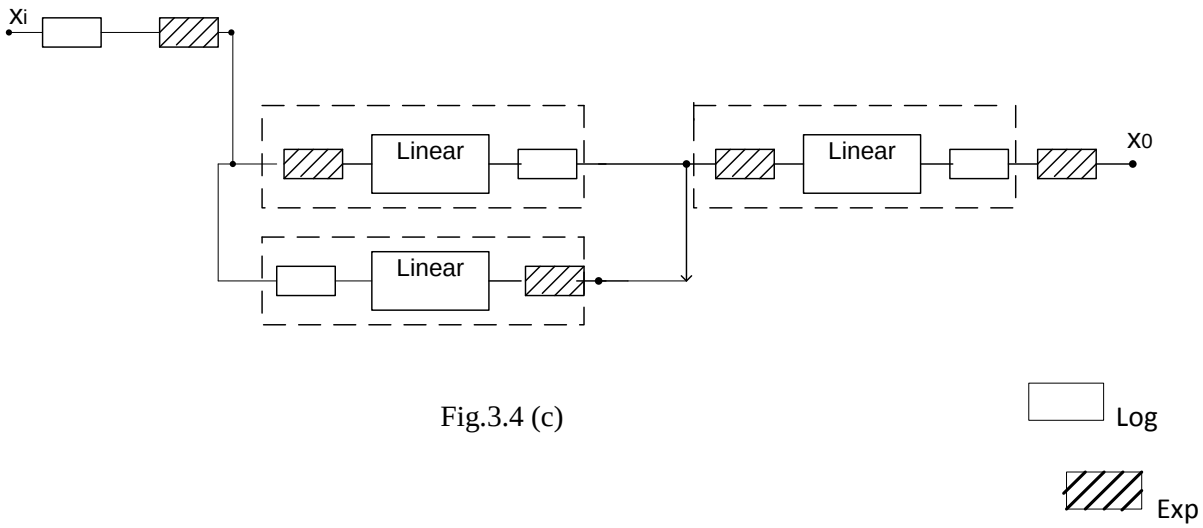

Fig.3.4 (c)

Fig.3.4 (a)-(c) Linearization of a log domain system.

3.4 Basic log domain building blocks

3.4.1 Multiple input non inverting integrator

The circuit of multiple input non inverting integrator can be drawn using basic log domain cell [15] and is shown in Fig.3.5 (a) and its signal flow graph representation is shown in Fig.3.5 (b). Analysis of non-inverting integrator is given below

Using basic log domain equation and by applying KCL, we can write

$$C.\frac{d}{dt}\vec{V}_0 = \vec{K}_{i1} \,.\, I_0 \,.\, e^{(\vec{V}_{i1} - \vec{V}_0)/2V_T} + \ldots\ldots\ldots + \vec{K}_{iN} \,.\, I_0 \,.\, e^{(\vec{V}_{iN} - \vec{V}_0)/2V_T} \tag{3.9}$$

Multiplying by $e^{\vec{V}_0/2V_T}$, we get

$$C.\, e^{\vec{V}_0/2V_T}.\frac{d}{dt}\vec{V}_0 = \vec{K}_{i1} \,.\, I_0 \,.\, e^{(\vec{V}_{i1}/2V_T} + \ldots\ldots\ldots + \vec{K}_{iN} \,.\, I_0 \,.\, e^{\vec{V}_{iN}/2V_T} \tag{3.10}$$

Finally, we can write

$$\frac{C.2V_T}{I_0}.\frac{d}{dt}\left[I_0.\, e^{\vec{V}_0/2V_T}\right] = \vec{K}_{i1} \,.\, I_0 \,.\, e^{\vec{V}_{i1}/2V_T} + \ldots\ldots\ldots + \vec{K}_{iN} \,.\, I_0 \,.\, e^{\vec{V}_{iN}/2V_T} \tag{3.11}$$

We assign new constant K_i as

$$K_i = \frac{\vec{K}_i \cdot I_0}{2V_T} \tag{3.12}$$

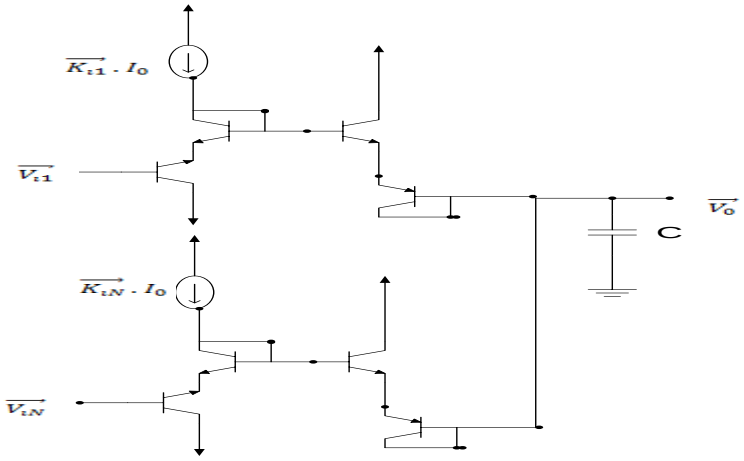

Fig.3.5(a) A multiple input non inverting integrator.

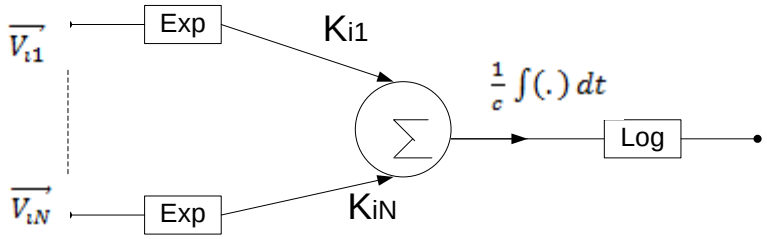

Fig.3.5 (b) Signal flow graph of multiple input non inverting integrator

So, we can write

$$c \cdot \frac{d}{dt}\left[I_0 . e^{\vec{V}_0/2V_T}\right] = K_{i1} \cdot I_0 \cdot e^{\vec{V}_{i1}/2V_T} + \ldots\ldots\ldots + K_{iN} \cdot I_0 \cdot e^{\vec{V}_{iN}/2V_T} \tag{3.13}$$

Using Exp operator, equation (3.13) becomes

$$c \cdot \frac{d}{dt}\left[\mathrm{Exp}(\vec{V}_0)\right] = K_{i1} \cdot \mathrm{Exp}(\vec{V}_{i1}) + \ldots\ldots\ldots + K_{iN} \cdot \mathrm{Exp}(\vec{V}_{iN}) \tag{3.14}$$

or $$\vec{V}_0 = \log\left\{\frac{1}{c} \cdot \int\left[K_{i1} . \mathrm{Exp}(\vec{V}_{i1}) + \ldots + K_{iN} . \mathrm{Exp}(\vec{V}_{iN})\right]dt\right\} \tag{3.15}$$

3.4.2 Damped integrator

The circuit of damped integrator can be obtained by giving the output back to its input as shown in Fig.3.6 (a) and the corresponding signal flow graph [15] is shown in Fig.3.6 (b) .

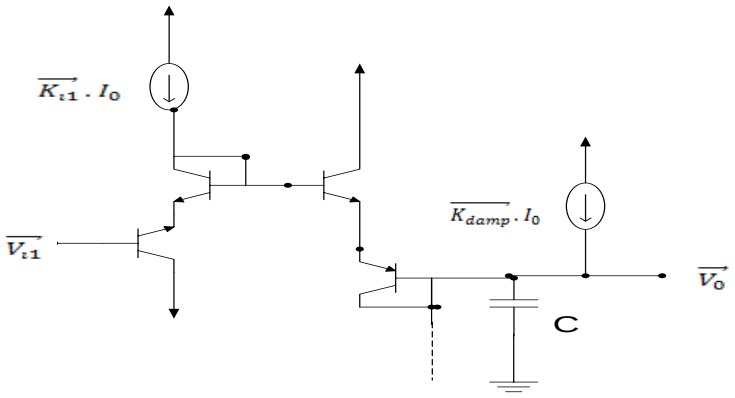

Fig.3.6 (a) Damping using a current source

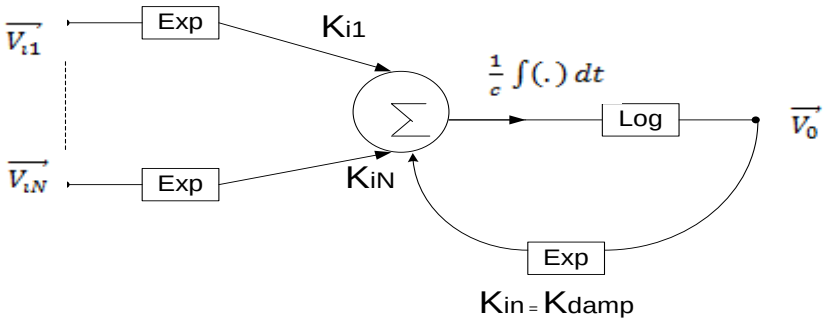

Fig.3.6 (b) Signal flow graph of damped integrator.

So, damping current can be expressed as

$$I_{damp} = \vec{K}_{damp} . I_0 . e^{(\vec{V}_0 - \vec{V}_0)/2V_T} \quad (3.16)$$

Which reduces to

$$I_{damp} = \vec{K}_{damp} . I_0 \quad (3.17)$$

3.4.3 Input and output stages

For linearization of a log domain system, a Log block should be placed at the input and Exp block at the output [15]. The corresponding circuit and the signal flow graph are shown in Fig.3.7 (a) and Fig.3.7 (b).

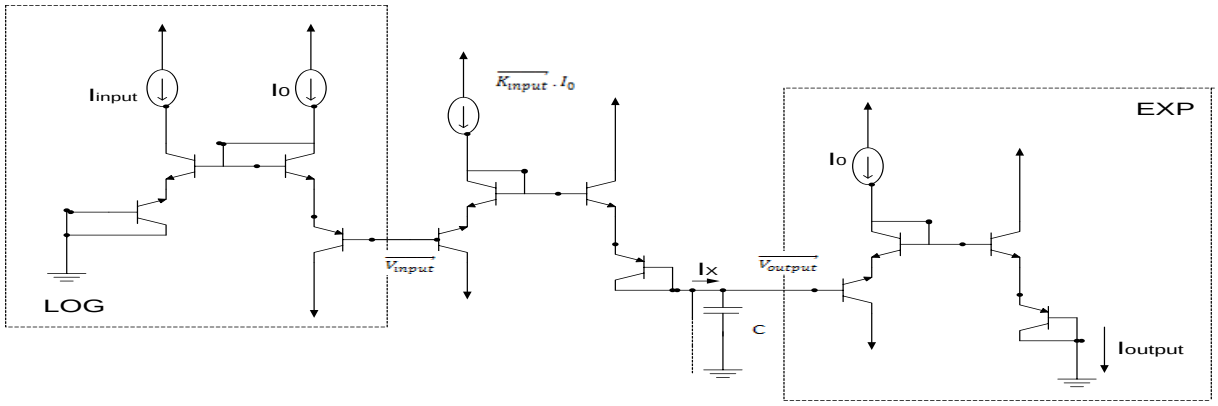

Fig.3.7 (a) Input and output stage of log domain system.

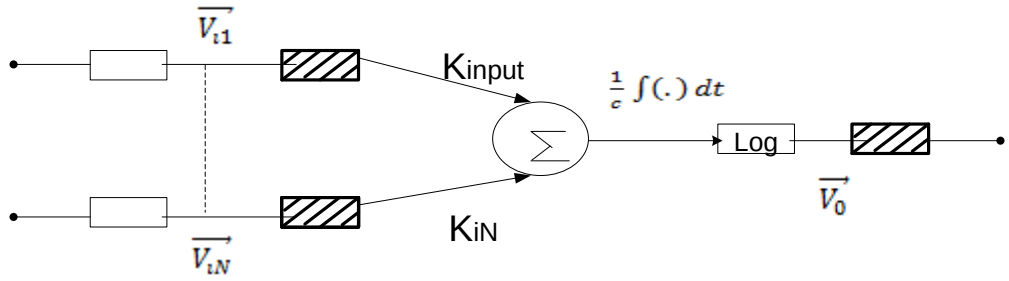

Fig.3.7 (b) Signal flow graph of Fig.3.7 (a).

3.5 Design of elliptic and chebyshev filters

Operational simulation of the LC ladder has been used to realize higher order filters. For design of log domain filters, the signal flow graph of the LC ladder is converted to the form which is compatible with signal flow graph of log domain structures [15]. In the following, we will explain two exemplary filters i.e. elliptic and chebyshev filters. The rules for converting a linear signal flow graph into a log domain signal flow graph is given below.

a) A Log block is placed after each integrator.
b) An Exp block is placed at input to each summer.

c) An Exp block is placed at output of the system.

d) A Log block is placed at input to the system.

The signal flow graph of a simple third order LC ladder and its log domain equivalent is shown in Fig.3.8 (a) and Fig.3.8 (b).

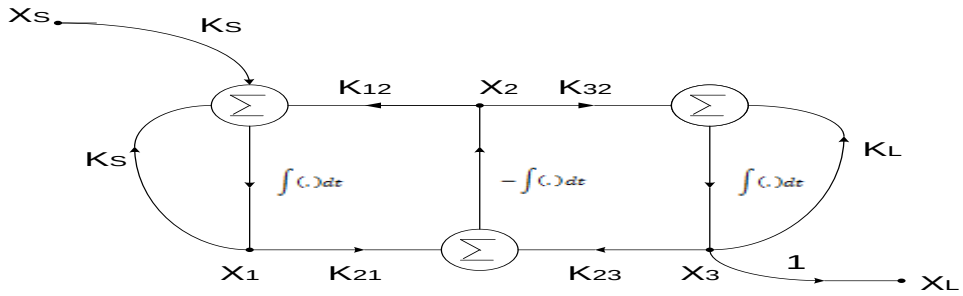

Fig.3.8 (a) Signal flow graph of a simple ladder

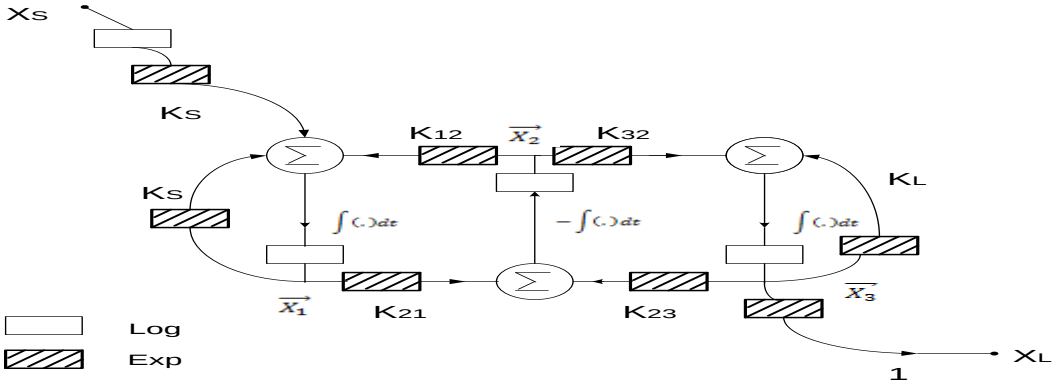

Fig.3.8 (b) Log domain equivalent of Fig.3.8 (a)

3.5.1 Design of third order elliptic filter

The LC ladder which represents the third order elliptic filter is shown in Fig.3.9 (a).

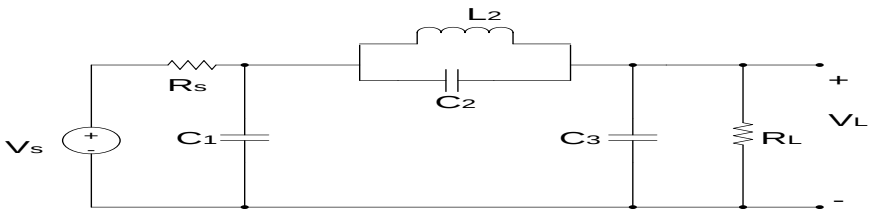

Fig.3.9 (a) LC ladder of third order elliptic filter .

The signal flow graph and third order elliptic filter circuit [15] are shown in Fig.3.9 (b) and Fig.3.9 (c).

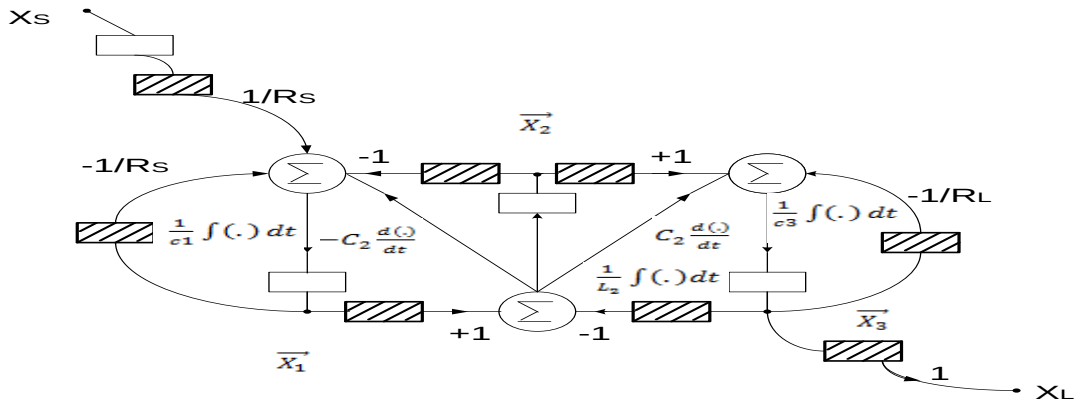

Fig.3.9 (b) Signal flow graph of third order elliptic filter.

Analysis of third order elliptic log domain filter is given below

Using basic log domain equation and by applying KCL, we can write

$$C_{C3}.\frac{d}{dt}\overrightarrow{V_3}=\overrightarrow{K_{23}}.I_0.\,e^{(\overrightarrow{V_2}-\ \overrightarrow{V_3})/2V_T}+\ldots\ldots\ldots+C_{C2}.\frac{d}{dt}(\overrightarrow{V_2}-\overrightarrow{V_3}) \tag{3.18}$$

Multiplying by $e^{\overrightarrow{V_3}/2V_T}$, we get

$$C_{C3}.\,e^{\overrightarrow{V_3}/2V_T}.\frac{d}{dt}\overrightarrow{V_3}=\overrightarrow{K_{23}}.I_0.e^{\overrightarrow{V_2}/2V_T}+\ldots\ldots\ldots+C_{C2}.\,e^{\overrightarrow{V_3}/2V_T}.\frac{d}{dt}\overrightarrow{V_1}-\,C_{C2}.\,e^{\overrightarrow{V_3}/2V_T}.\frac{d}{dt}\overrightarrow{V_3} \tag{3.19}$$

Let $e^{\overrightarrow{V_1}/2V_T}=e^{\overrightarrow{V_3}/2V_T}$ (3.20)

Finally, we can write

$$C_{C3}\,.\frac{d}{dt}\left[\mathrm{Exp}(\overrightarrow{V_3})\right]=K_{23}.\mathrm{Exp}(\overrightarrow{V_2})+\ldots+C_{C2}\,.\frac{d}{dt}\left[\mathrm{Exp}(\overrightarrow{V_1})\right]-C_{C2}\,.\frac{d}{dt}\left[\mathrm{Exp}(\overrightarrow{V_3})\right] \tag{3.21}$$

where

$$K_{23}=\frac{\overrightarrow{K_{23}}.I_0}{2V_T} \tag{3.22}$$

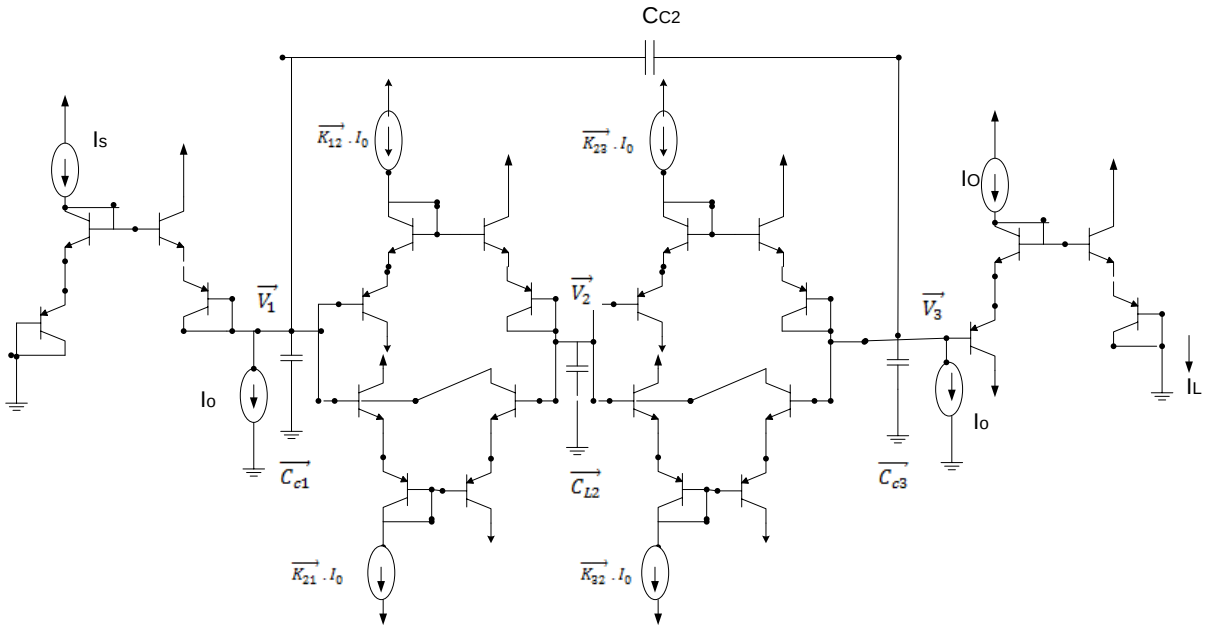

Fig.3.9 (c) Circuit diagram of third order elliptic filter.

So, equation (3.21) is given by

$$\overrightarrow{V_3} = \log\left\{\frac{1}{C_{C3}} . \int \left[K_{23}.\mathrm{Exp}(\overrightarrow{V_2}) \ + .. + C_{C2} . \frac{d}{dt}(\mathrm{Exp}(\overrightarrow{V_1}) - \mathrm{Exp}(\overrightarrow{V_3})\right] dt\right\} \quad (3.23)$$

3.5.2 Simulation results

To prove the theoretical validity of third order elliptic log domain filter of Fig.3.9 (c), the filter is simulated with PSPICE. The passive elements are selected as C_{C1} = 6.79560 nF, C_{L2} = 3.47308 nF, C_{C3} = 9.55216 nF. The supply voltages taken as $V_{CC+} = 5V$ and $V_{CC-} = -5V$. The cut off frequency selected is 40 KHZ for bias current (I_O) = 90 uA. The transient response, frequency response in full frequency range and passband is shown in Fig.3.9 (d) to Fig.3.9 (f).

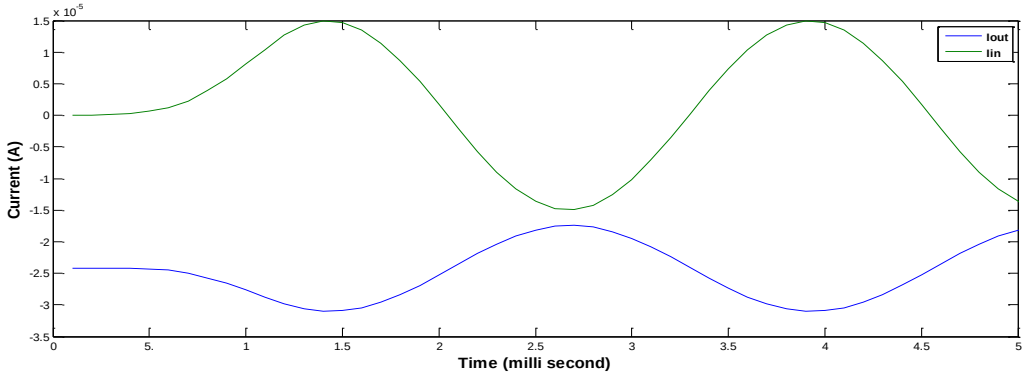

Fig.3.9 (d) Transient response of third order elliptic filter

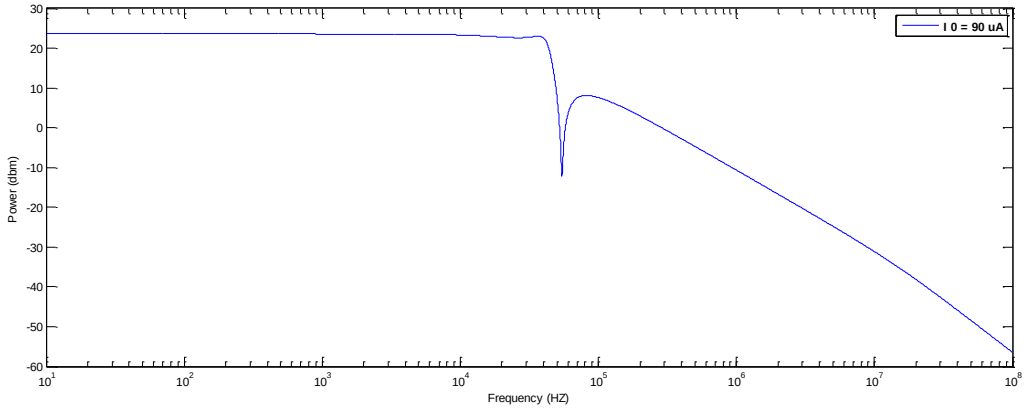

Fig.3.9 (e) Frequency response of third order elliptic filter for I_O = 90 uA

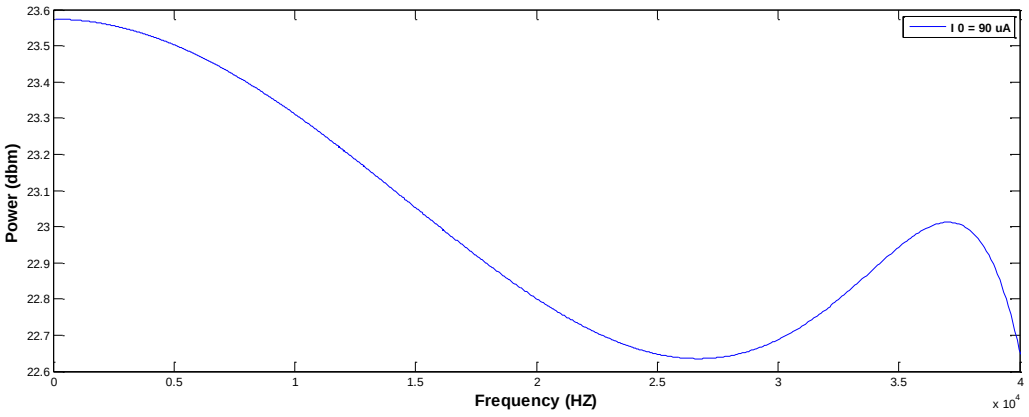

Fig.3.9 (f) Passband range of third order elliptic filter

The tunability of this filter is controlled by biasing current (I_O) having values 90 uA, 150 uA and 200 uA is shown in Fig.3.9 (g) and effect of emitter resistance (R_E) having values 0, 20, 40 is shown in Fig.3.9 (h).

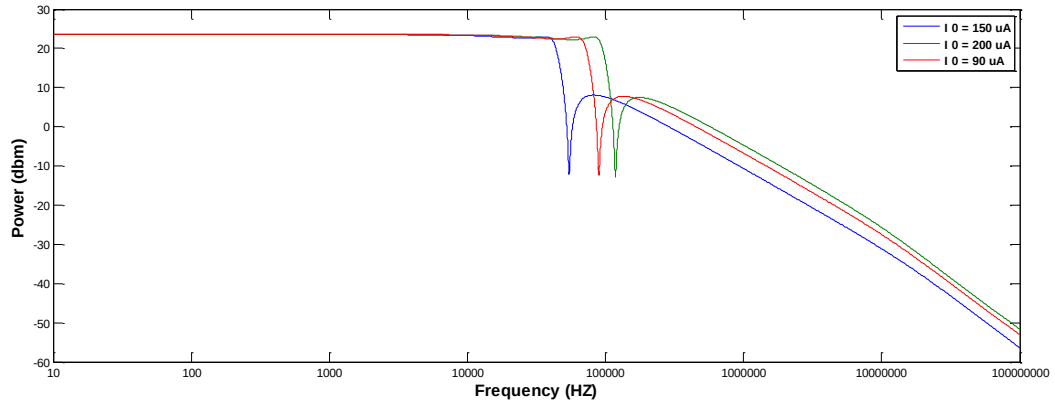

Fig.3.9 (g) Tunability of third order elliptic filter by I_O.

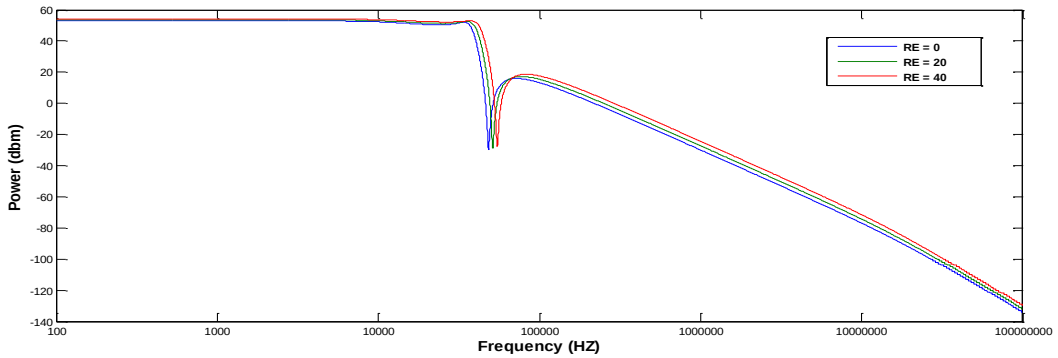

Fig.3.9 (h) Effect of different R_E on frequency response of third order elliptic filter

3.5.3 Design of fifth order chebyshev filter

The LC ladder which represents the fifth order [15] Chebyshev filter is shown in Fig.3.10 (a).

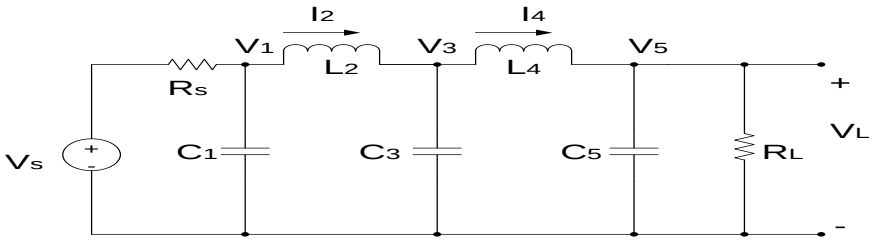

Fig.3.10 (a) LC ladder of fifth order chebyshev filter.

By applying KVL around each inductor branch and KCL at all capacitor nodes, we have following equations

$$L_2 \frac{d}{dt} I_2 = V_1 - V_3 \tag{3.24}$$

$$L_4 \frac{d}{dt} I_4 = V_3 - V_5 \tag{3.25}$$

$$C_1 \frac{d}{dt} V_1 = \frac{V_S}{R_S} - \frac{V_1}{R_S} - I_2 \tag{3.26}$$

$$C_3 \frac{d}{dt} V_3 = I_2 - I_4 \tag{3.27}$$

$$C_5 \frac{d}{dt} V_5 = I_4 - \frac{V_5}{R_L} \tag{3.28}$$

$$V_L = V_5 \tag{3.29}$$

Now, let us define a set of variables which will correspond to both voltages and currents.

$X_S \leftrightarrow V_S$, $X_1 \leftrightarrow V_1$, $X_2 \leftrightarrow I_2$, $X_3 \leftrightarrow V_3$, $X_4 \leftrightarrow I_4$, $X_5 \leftrightarrow V_5$, $X_L \leftrightarrow V_L$

The signal flow graph corresponds to LC ladder and fifth order Chebyshev filter circuit are shown in Fig.3.10 (b) and Fig.3.10 (c).

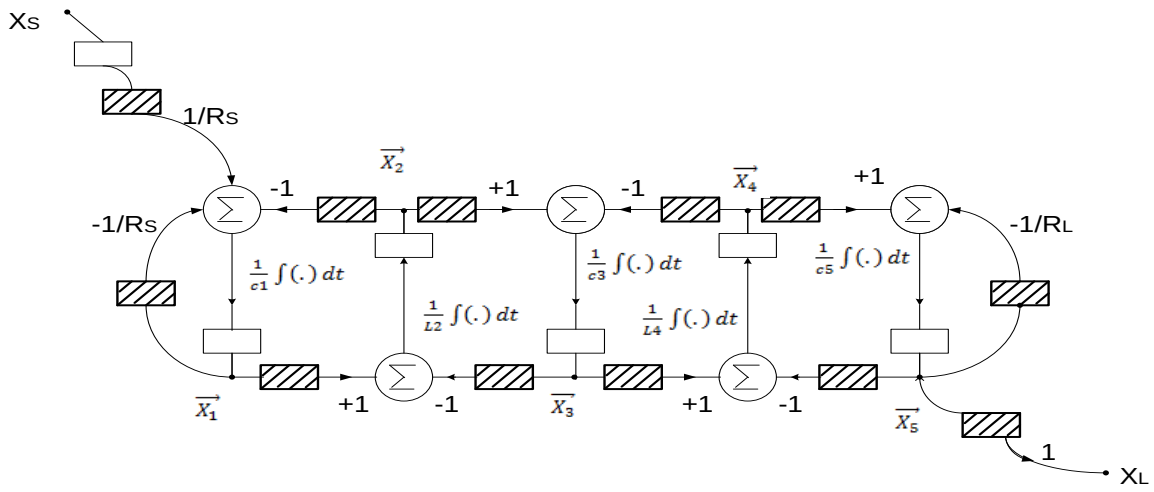

Fig.3.10 (b) Signal flow graph of fifth order Chebyshev filter.

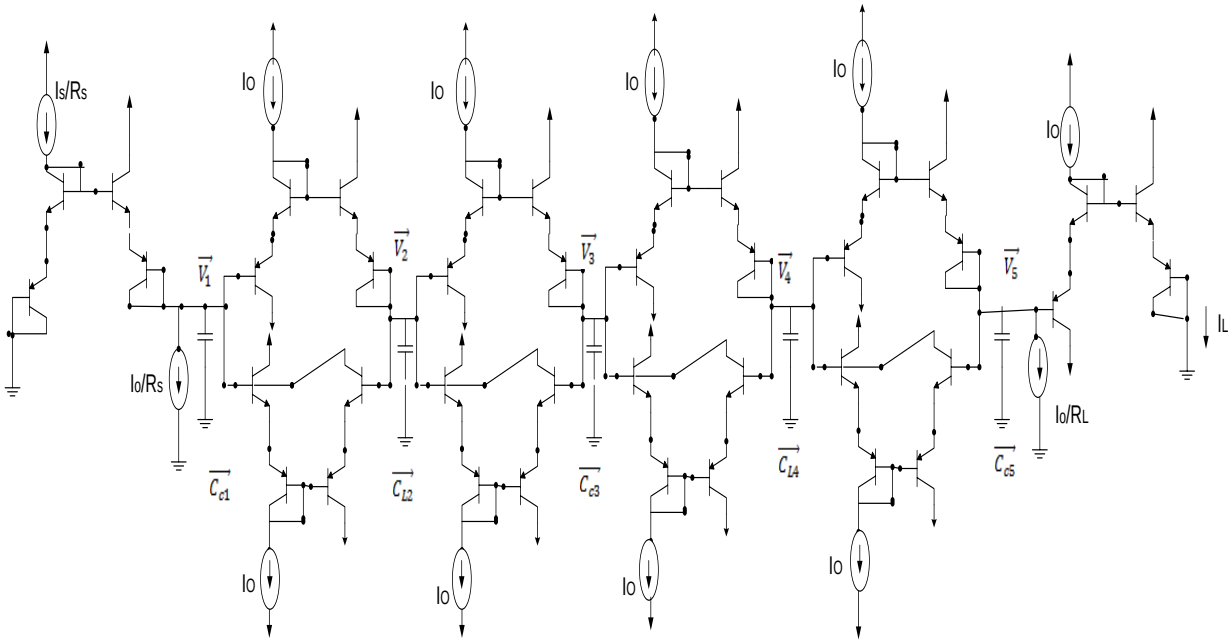

Fig.3.10 (c) Circuit diagram of fifth order chebyshev filter.

3.5.4 Simulation results

To prove the theoretical validity of fifth order chebyshev log domain filter of Fig. 3.10 (c), the filter is simulated with PSPICE. The passive elements are selected as R_S = 1 Ω, C_{C1} = 6.79560 nF, C_{L2} = 3.47308 nF, C_{C3} = 9.55216 nF , C_{L4} = 3.47308 nF , C_{C5} = 6.79560 nF , R_L = 1 Ω . The supply voltages are taken as $V_{CC+} = 5V$ and $V_{CC-} = -5V$ .The cut off frequency selected is 50 KHZ for bias current (I_O) = 220 uA. The transient response, frequency response in full frequency range and passband are shown in Fig.3.10 (d) to Fig.3.10 (f).

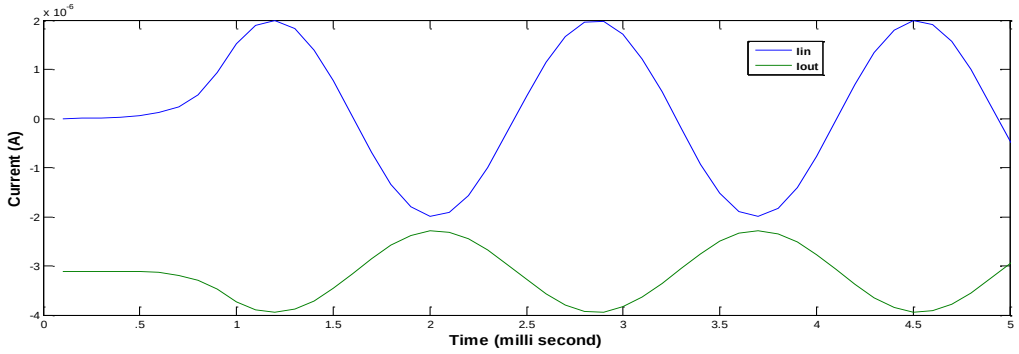

Fig.3.10 (d) Transient response of fifth order chebyshev filter

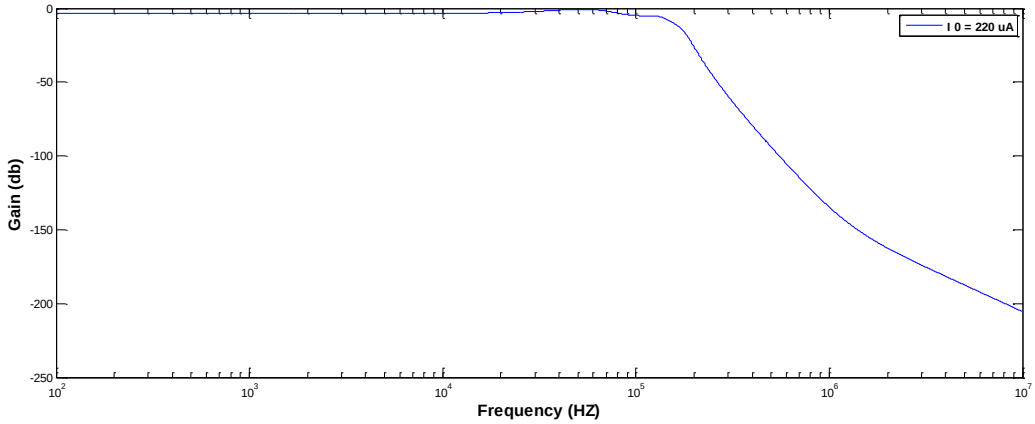

Fig.3.10 (e) Frequency response of fifth order chebyshev filter for I_O = 220 uA

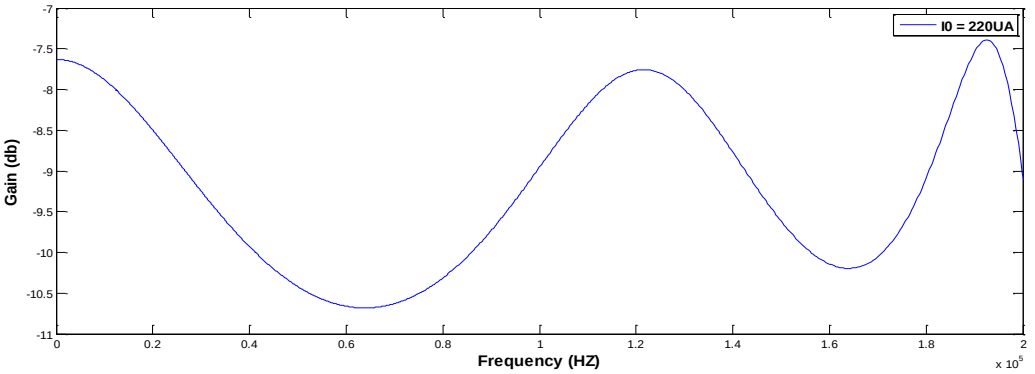

Fig.3.10 (f) Passband range of fifth order chebyshev filter

The tunability of this filter is controlled by biasing current (I_O) having values 140 uA, 180 uA and 220 uA is shown in Fig.3.9 (g) and effect of emitter resistance (R_E) having values 0, 20, 40 is shown in Fig.3.10 (h).

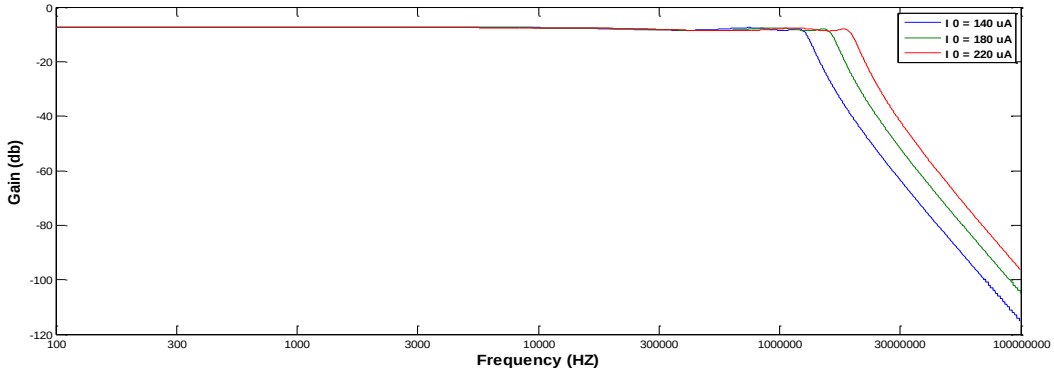

Fig.3.10 (g) Tunability of fifth order chebyshev filter by I_O .

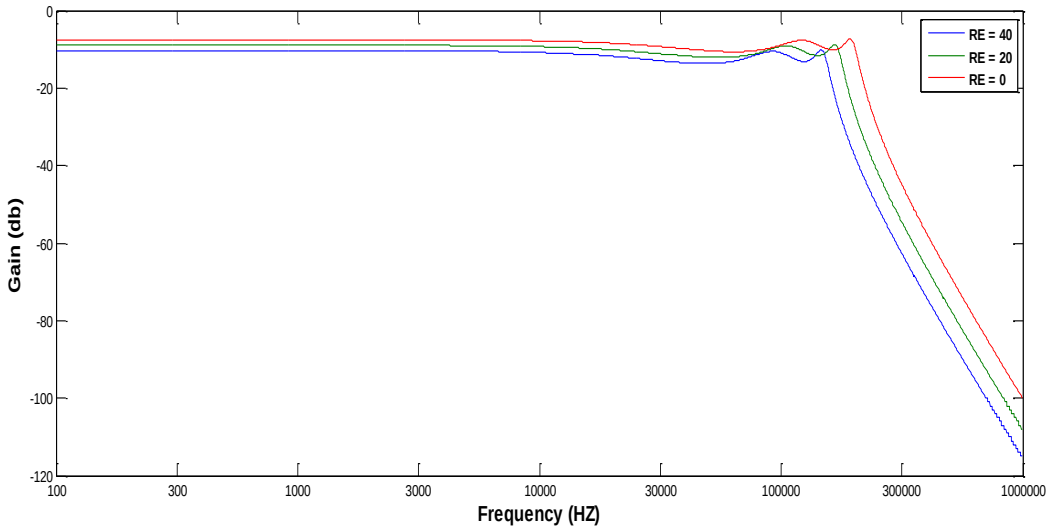

Fig.3.10 (h) Effect of different R_E on frequency response of fifth order chebyshev filter

3.6 Conclusion

This chapter covers the technique for the design of log domain filters which is based on simulation of LC ladder circuits having low component sensitivities over passband region. The design of third order elliptic filter and fifth order chebyshev filter are used to demonstrate the technique. The behaviour of this filters are verified through PSPICE. The time responses and frequency responses for these filters have been shown which are simulated using PSPICE.

Chapter 4

State space synthesis of log domain filter

4.1 Introduction

In the previous chapters, we have discussed the different topologies of log domain filters i.e. Translinear principle, Bernoulli cell and LC ladder. In this chapter, we will discuss the synthesis of log domain filters by state-space representation.

In 1993, Frey [16] presented a method for synthesis of log-domain filters using state-space realization. In state-space synthesis method, the bipolar junction transistor can be directly used to realize log-domain filters by mapping from state-space linear differential equations. In this chapter we will present a systematic transistor level approach suitable for the design of log domain filters. The method presented is based on set of linear differential equations termed as log domain state space which can be identified through Bernoulli differential equation.

4.2 State space synthesis

The state-space synthesis method is an approach for synthesis of log-domain filters. It provides a solution for realizing the filter function. A state-space model of a filter consists of set of first-order differential equations. There is a one-to-one correspondence between the mathematical model and the circuit realization. In addition, all the capacitors in a current-mode implementation of state-space filters have one terminal connected to ground which makes the filter more suitable for IC implementation. In 1993, a formal synthesis procedure, based on the state-space description of the desired filter function was introduced by Frey [17]. In the following, we summarize the same.

The filter contains three essential parts

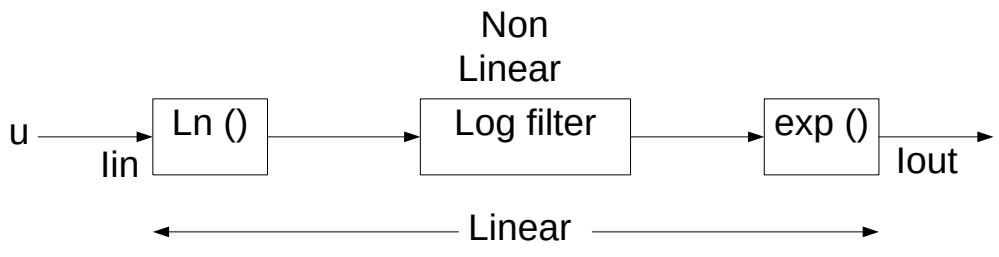

Fig.4.1 Log domain filter set up.

At the input, the input current is compressed into a logarithmic voltage. This voltage is filtered next by a log filter. After this, the output voltage is expanded exponentially into output current [17]. The rules for state space synthesis are given below

a) Obtain the appropriate state space description of the filter.
b) An exponential mapping function for both input and state variables is determined.
c) The set of equations are manipulated to find a set of nodal equations.
d) Finally, the circuit using transistors, grounded capacitors and current source is implemented using the state space description.

Let the state space description of the desired transfer function corresponding to a single input and single output system be given by

$$\dot{X} = AX + Bu \tag{4.1}$$

$$y = CX + Du \tag{4.2}$$

Where u is scalar input, y is scalar output and $X = (x_1, x_2, .., x_N)^T$ is state variable vector. Let us assume that non - linear mapping is imposed on state variables as follows

$$x_i = f(V_i) \text{ with } \dot{f}(V_i) \neq 0 \text{ for finite } V_i \tag{4.3}$$

By taking into consideration the above mapping and its derivatives and then substituting into equation (4.2), we get following equations

$$C_i \dot{V}_i = \sum_{j=1}^{N} C_i A_{ij} \frac{f(V_j)}{\dot{f}(V_i)} + C_i B_i \frac{f(V_0)}{\dot{f}(V_i)} \tag{4.4}$$

$$Y = \sum_{j=1}^{N} C_{0j} A_{ij} \frac{f(V_j)}{\dot{f}(V_{N+1})} + D_0 \frac{f(V_0)}{\dot{f}(V_{N+1})} \tag{4.5}$$

Where A_{ij} is the ij^{th} element of state matrix A and C_{0j}, D_0 are scaling constants, V_i and V_j denotes the i^{th} node voltage of the circuit.

LHS corresponds to the current in a grounded capacitor at node i and RHS corresponds to the output current.

4.3 Applications of state space synthesis in log domain filters

In the following, we will present the various types of filters synthesized using state space methodology.

4.3.1 A first order log domain low pass filter

A low pass filter is a frequency selective circuit that passes signals with a frequency lower than a certain cut off frequency and attenuates signals with frequencies higher than cut off frequency. The amount of attenuation for each frequency depends on the filter design [17]. In the following, we will present the design of a first order low pass current mode filter that is systematically derived using the state space method .Gain and cut off frequency of the filter can be tuned by changing the value of DC currents. The first order filter is shown below in Fig.4.2.

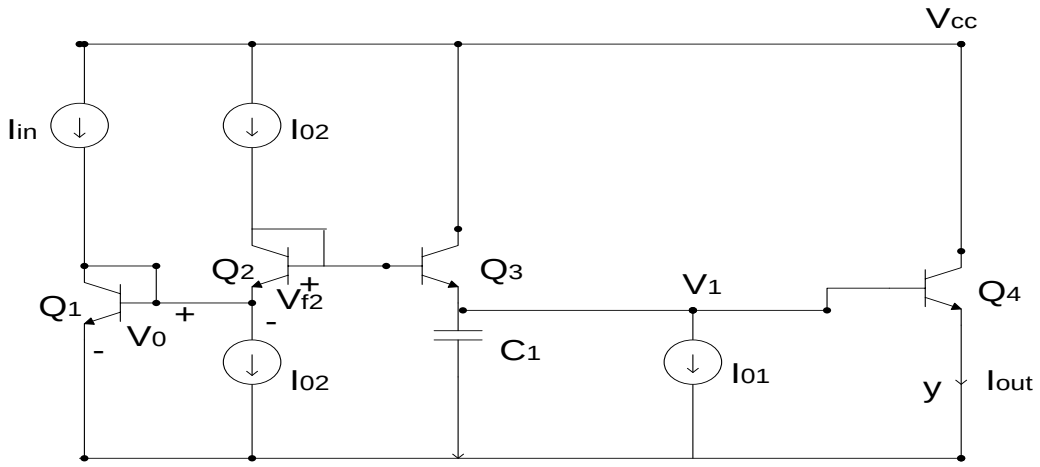

Fig.4.2 A first order log domain low pass filter.

A first order low pass filter transfer function can be written as

$$H(S) = \frac{Y(S)}{U(S)} = \frac{I_{out}(S)}{I_{in}(S)} = a_1 \frac{w_0}{s+w_0}, \qquad a_1 > 0 \tag{4.6}$$

Using state space mapping, we can write

$$\dot{y} = - w_0 \, y + a_1 \, w_0 \, u \tag{4.7}$$

Let state variable x be taken as $x = y$ (4.8)

so, equation (4.7) can be written as

$$\dot{x} = - w_0 \, x + a_1 \, w_0 \, u \tag{4.9}$$

The output equation is given by $y = x$ (4.10)

Equation (4.9) can be transformed into a set of nodal equations using exponential mappings on the input and state variables. The mappings applied are given below

$$x = I_S \, e^{V_1/V_T}, \; u = I_S \, e^{V_0/V_T} \tag{4.11}$$

Also, $$\dot{x} = I_S \, \frac{1}{V_T} \, \dot{V}_1 \, e^{V_1/V_T}, \; \dot{u} = I_S \, \frac{1}{V_T} \, \dot{V}_0 \, e^{V_0/V_T} \tag{4.12}$$

The above relationship can be applied to equation (4.9) and can be arranged to the following nodal equations

$$C \, \dot{V}_1 = - w_0 \, CV_T + a_1 \, w_0 \, CV_T \, e^{\frac{V_0 - V_1}{V_T}} \tag{4.13}$$

Let us assume

$$I_{01} = w_0 \, CV_T \, , \; I_{02} = a_1 \, w_0 \, CV_T \tag{4.14}$$

Where I_{01} and I_{02} are positive constants .So, equation (4.13) can be written as

$$C \, \dot{V}_1 = - I_{01} + I_{02} \, e^{\frac{V_0 - V_1}{V_T}} \tag{4.15}$$

If $I_{02} = I_S \, e^{\frac{V_{F2}}{V_T}}$, equation (4.15) can be written as

$$C \, \dot{V}_1 = - I_{01} + I_S \, e^{\frac{V_0 + V_{F2} - V_1}{V_T}} \tag{4.16}$$

The cut off frequency and gain of the filters are given below

$$w_0 = I_{01}/CV_T \tag{4.17}$$

$$a_1 = I_{02}/I_{01} \tag{4.18}$$

4.3.2 Simulation results

The first order low pass filter is simulated in PSPICE. The circuit parameters are selected as a_1 = 1, V_{CC} = 3V, I_{01} = I_{02} = 100 uA and C = 200 pF .The cut off frequency of filter is 3 MHZ. The transient, gain and phase response are shown in Fig.4.3 (a) to Fig.4.3 (d).

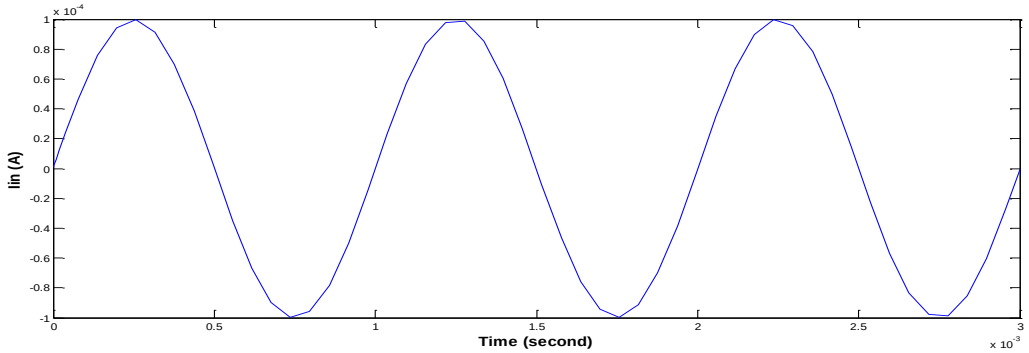

Fig.4.3 (a) Time response for input of low pass filter.

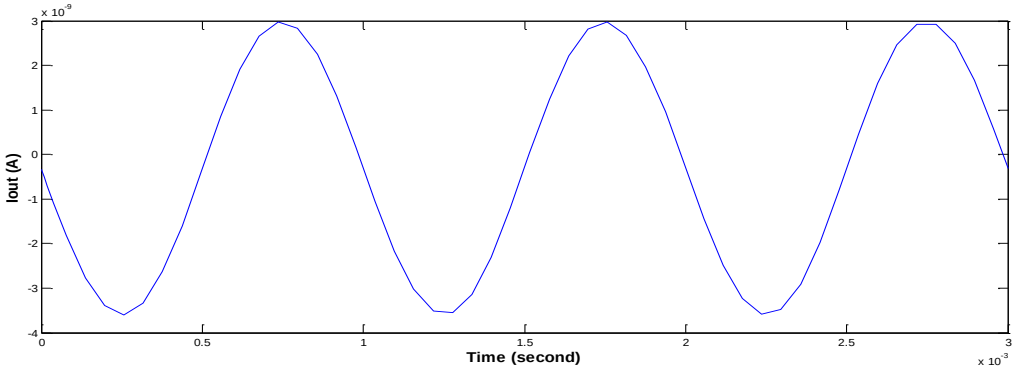

Fig.4.3 (b) Time response for output of low pass filter.

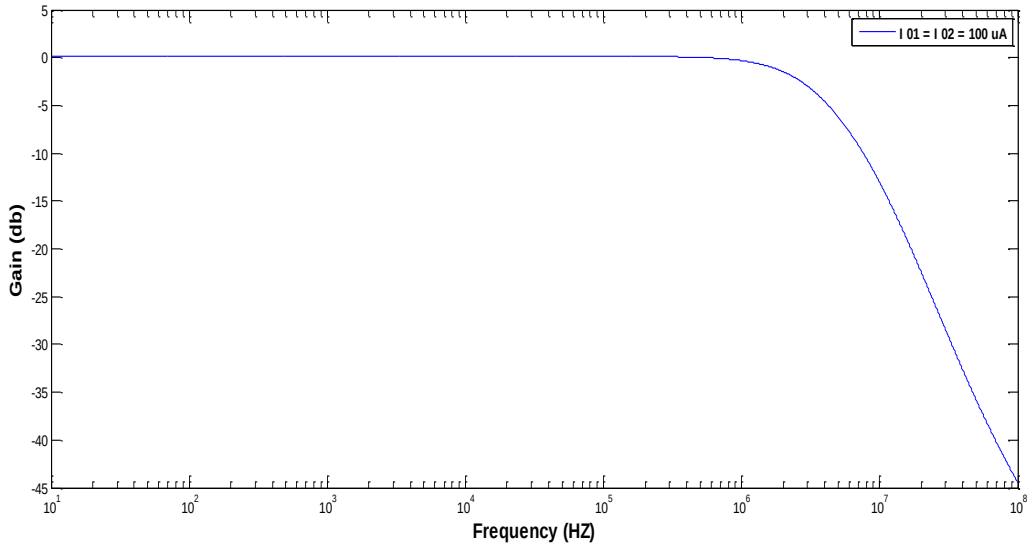

Fig.4.3 (c) Gain response of low pass filter.

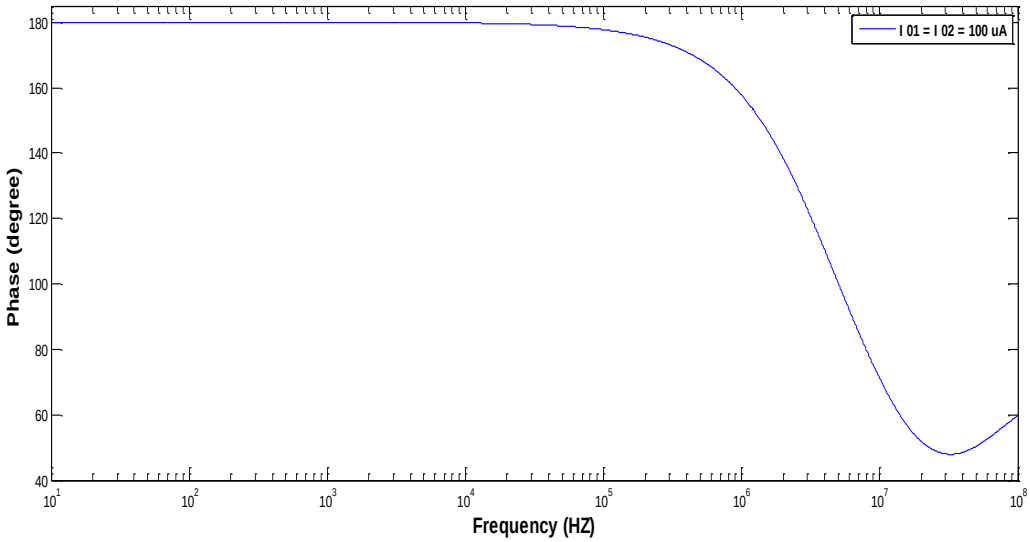

Fig.4.3 (d) Phase response of low pass filter.

4.3.3 A log domain lossless integrator

The circuit diagram of lossless integrator is shown in Fig.4.4 [8].

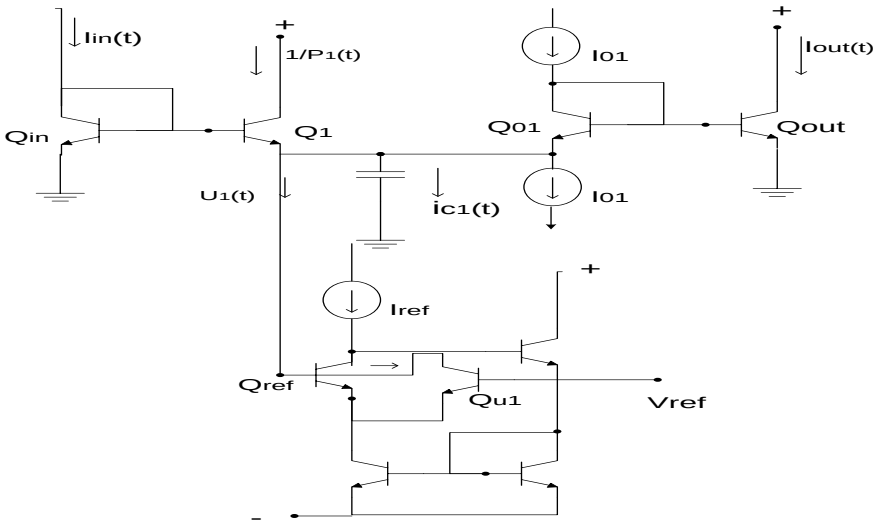

Fig.4.4 Circuit diagram of lossless integrator.

The transfer function of the integrator is expressed as

$$H(s) = \frac{K}{S} \tag{4.19}$$

The linear state space representation is given by

$$\dot{x_1}(t) = U(t) \tag{4.20}$$

and

$$y(t) = k\, x_1(t) \tag{4.21}$$

where $x_1(t)$ is state variable, U(t) is input and y(t) is output.

The log domain state space design equation can be expressed as

$$C_1 V_T \dot{w}_1 + u_1(t)\, w_1(t) = I_{in}(t) \tag{4.22}$$

and necessary design equations are

$$u_1(t)\, w_1(t) = n_1 \tag{4.23}$$

and

$$I_{out}(t) \propto w_1(t) \tag{4.24}$$

So, transfer function can be written as

$$I_{out}(s) = \frac{(I_{01}/C_1 V_T)}{s} I_{in}(s) \qquad (4.25)$$

Where $w_k(t) = \left[\prod_{j=1}^{k} T_k(t)\right] I_{in}(t) = P_k(t) w_{k-1}(t)$, $w_1(t) = u_1\, e\left[\frac{V_{C1}(t)}{V_T}\right]$ & $I_C(t) = 1/P(t) \neq 0$ and n_1 is a constant.

4.3.4 Simulation results

The log domain lossless integrator is simulated in PSPICE. The power supply voltages are taken as 1.5V, Biasing current (I_0) = 100 uA. The integration time constant (τ) = C_1/V_T depends both on capacitance and biasing current. The integrator response for the 100 KHZ input frequency for C = 20 pF and C= 40 pF are shown in Fig.4.5 (a) to Fig.4.5 (c).

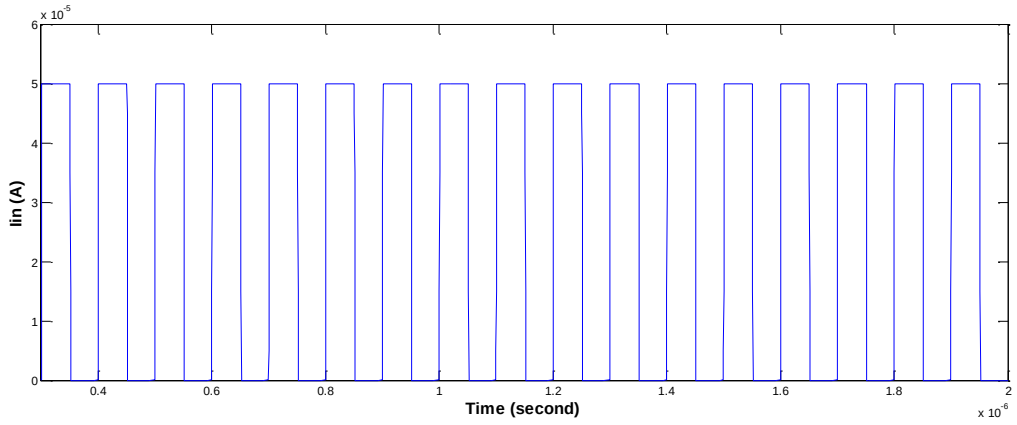

Fig.4.5 (a) Input frequency of 100KHZ for lossless integrator

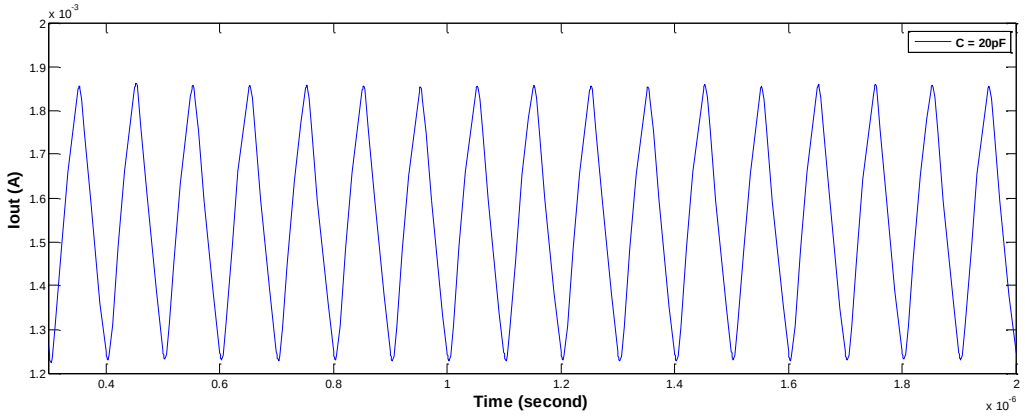

Fig.4.5 (b) Integrator response for C = 20 pF for lossless integrator

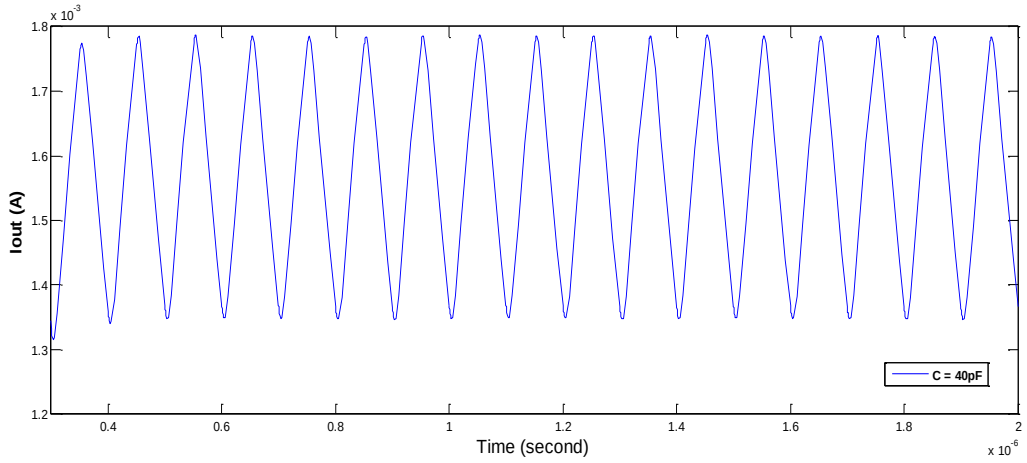

Fig.4.5 (c) Integrator response for C = 40 pF for lossless integrator

4.3.5 Log domain band pass filter

The general form of transfer function for band pass filter is given by

$$H\ (s) = \frac{K(\frac{w_0}{Q})s}{s^2+(\frac{w_0}{Q})s+\omega_0^2} \tag{4.26}$$

The circuit diagram of band pass filter is shown in Fig.4.6 [8].

The linear state space representation is given by

$$\dot{x_1}\ (t) + (\ \frac{w_0}{Q}\ )\ x_1\ (t) + w_0 x_2\ (t) = \ w_0 U(t) \tag{4.27}$$

$$\dot{x_2}\ (t) = w_0 x_1\ (t) \tag{4.28}$$

and

$$\text{y (t)} = (\ \frac{w_0}{Q}\ )\ x_1\ (t) \tag{4.29}$$

The log domain state space design equation can be expressed as

$$C_1\ V_T\ \dot{w_1}(t) + u_1\ (\text{t})\ w_1\ (t) = I_{in}\ (t) \tag{4.30}$$

$$C_2\ V_T\ \dot{w_2}(t) + u_2\ (\text{t})\ w_2\ (t) = w_1\ (t) \tag{4.31}$$

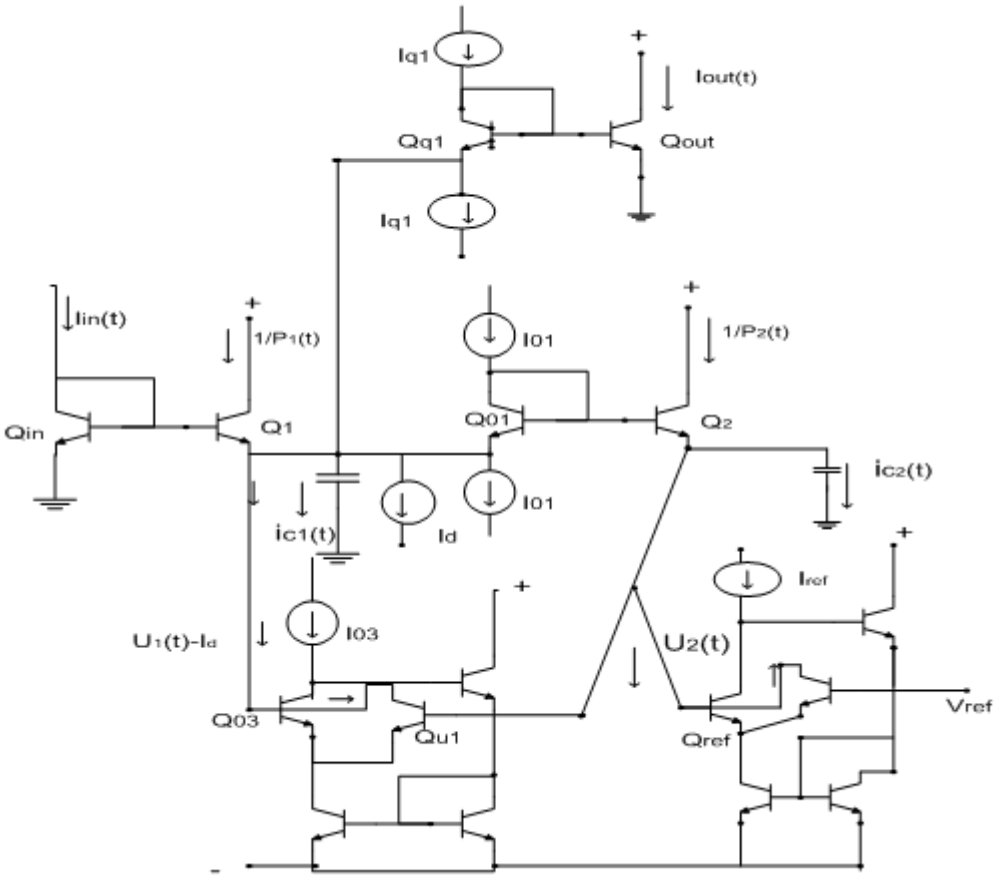

Fig.4.6 Circuit diagram of band pass filter.

And necessary design equations are

$$u_1(t)\, w_1(t) \alpha\ (w_1(t) + w_1(t)) \tag{4.32}$$

$$u_2(t)\, w_2(t) = n_2 \tag{4.33}$$

$$I_{out}(t) \alpha\, w_1(t) \tag{4.34}$$

Where $w_k(t) = \left[\prod_{j=1}^{k} T_k(t)\right] I_{in}(t) = P_k(t) w_{k-1}(t)$, $w_1(t) = u_1\, e\left[\frac{V_{C1}(t)}{V_T}\right]$ & $I_C(t) = 1/P(t) \neq 0$ and n_2 is a constant.

The transfer function is calculated as

$$I_{out}(s) = \frac{(I_{q1}/C_1 V_T)\, S}{s^2 + (I_d/C_1 V_T)s + (I_{01} I_{03} / C_1\ C_2 V_T^2)} I_{in}(s) \tag{4.35}$$

The cut off frequency (w_0) and quality factor (Q) are calculated as

$$w_0 = (\sqrt{I_{01}\, I_{03}} / \sqrt{C_1\, C_2}\, V_T) \tag{4.36}$$

$$Q = \left(\sqrt{\frac{C_1}{C_2}} \right) \left(\sqrt{I_{01}\, I_{03}} / I_d \right) \tag{4.37}$$

4.3.6 Simulation results

The log domain Band pass filter is simulated in PSPICE. The power supply voltages are taken as 1.5 V. The transient and frequency responses for different quality factor and cut off frequency are shown in Fig.4.7 (a) to Fig.4.7 (d).

The transient response is shown below in Fig.4.7 (a).

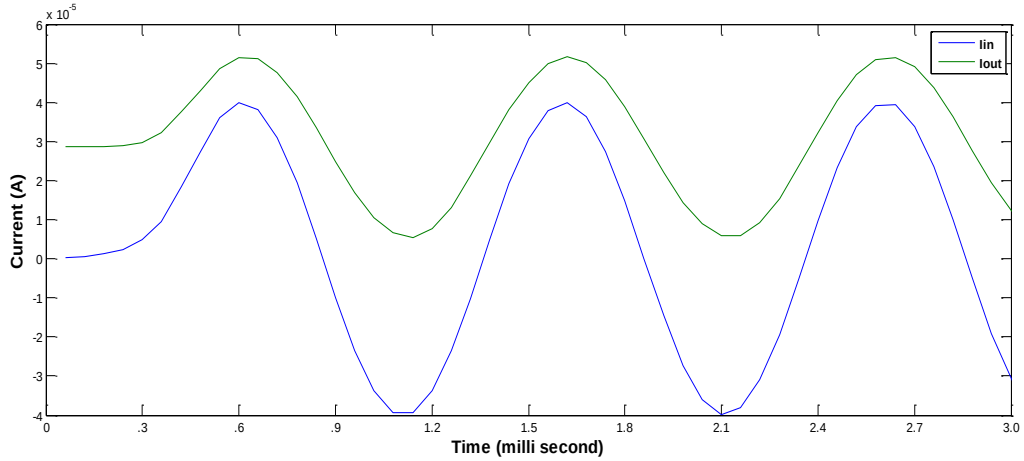

Fig.4.7 (a) Transient response of band pass filter.

The frequency response for

1) f_0 = 10 MHZ and Q = 1 having parameter values $I_D = I_{q1} = I_{ref} = I_{01} = I_{03}$= 50 uA, V_{ref} = -12 mV, $C_1 = C_2$ = 30 pF is shown in Fig.4.7 (b).
2) f_0 = 16 MHZ and Q = 1.6 having parameter values $I_D = I_{q1} = I_{ref} = I_{01}$ = 50 uA, I_{03}= 125 uA, V_{ref} = -39 mV, $C_1 = C_2$ = 30 pF is shown in Fig.4.7 (c).
3) f_0 = 20 MHZ and Q = 3.3 having parameter values I_D = 30 uA, $I_{01} = I_{03}$ = 100 uA, I_{ref} = 50 uA, V_{ref} = -20 mV, $C_1 = C_2$ = 30 pF is shown in Fig.4.7 (d).

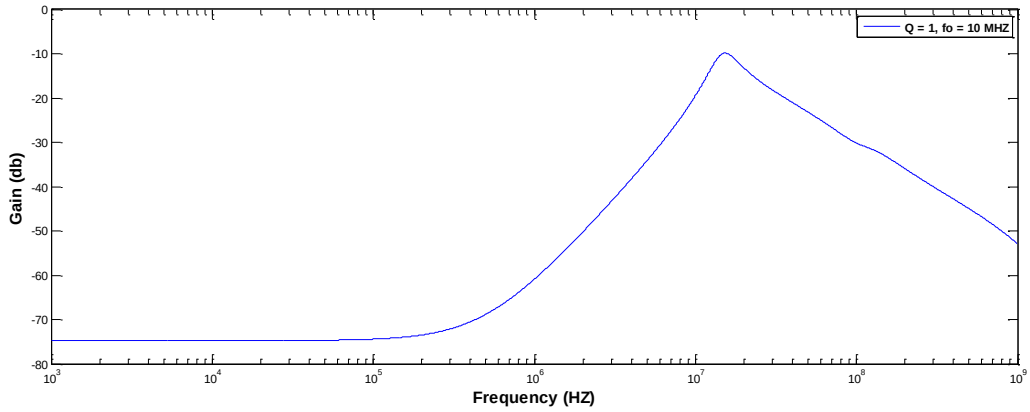

Fig.4.7 (b) Frequency response of f_0 = 10 MHZ and Q = 1 for band pass filter.

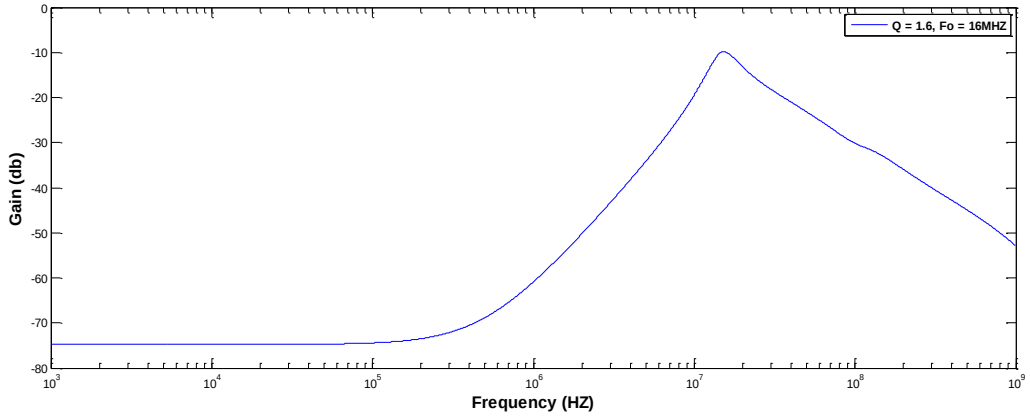

Fig.4.7 (c) Frequency response of f_0 = 16 MHZ and Q = 1.6 for band pass filter.

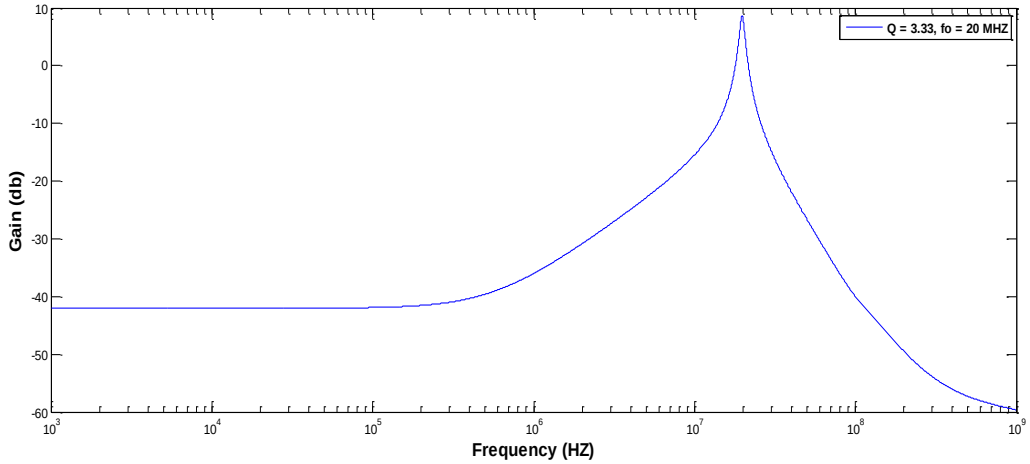

Fig.4.7 (d) Frequency response of f_0 = 20 MHZ and Q = 3.33 for band pass filter.

4.3.7 Proposed second order low pass filter

The general form of transfer function for low pass filter is given by

$$H\ (s) = \frac{K(\omega_0^2)}{s^2+(\frac{w_0}{Q})s+\omega_0^2} \tag{4.38}$$

The circuit diagram of low pass filter is shown in Fig.4.8 [8].

The linear state space representation is given by

$$\dot{x_1}\ (t) + w_0 x_2\ (t) = \ w_0 U(t) \tag{4.39}$$

$$\dot{x_2}\ (t) + \ (\frac{w_0}{Q})x_2\ (t)\ = w_0 x_1\ (t) \tag{4.40}$$

and

$$\text{y (t)} = \text{k}\ x_2\ (t) \tag{4.41}$$

The log domain state space design equation can be expressed as

$$C_1\ V_T\ \dot{w_1}(t) + u_1\ (\text{t})\ w_1\ (t) = I_{in}\ (t) \tag{4.42}$$

$$C_2\ V_T\ \dot{w_2}(t) + u_2\ (\text{t})\ w_2\ (t) = w_1\ (t) \tag{4.43}$$

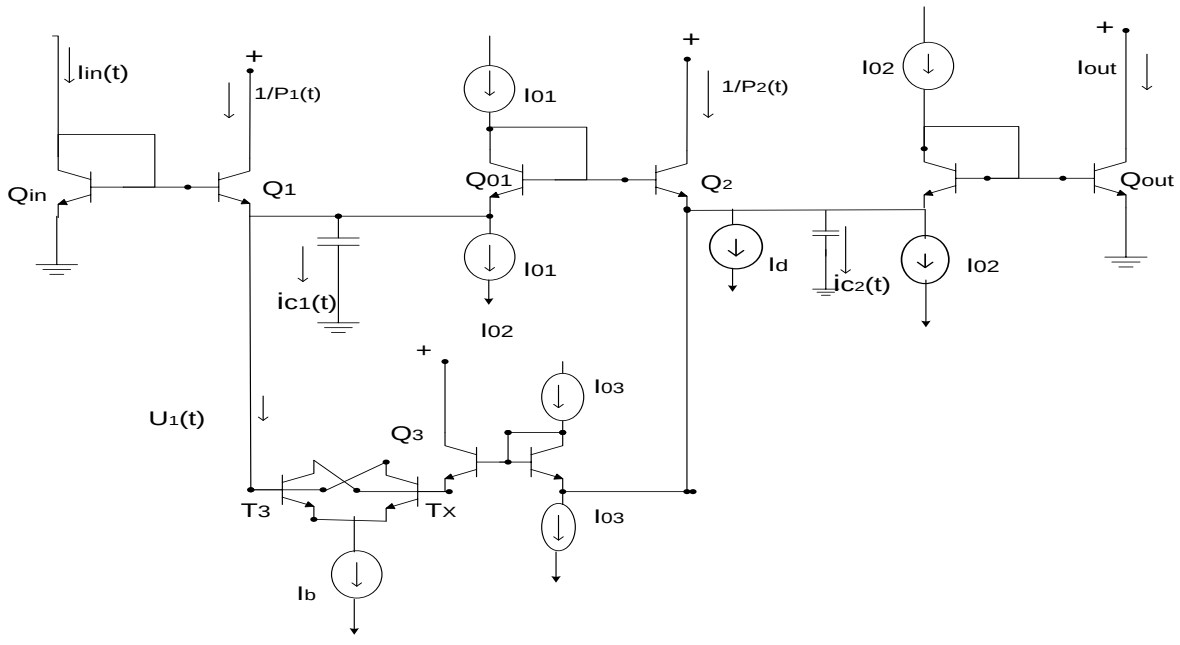

Fig.4.8 Circuit diagram of second order low pass filter

.

And necessary design equations are

$$u_1\,(t)\; w_1\,(t)\;\alpha\;\; w_2\,(t) \tag{4.44}$$

$$u_2\,(t)\; w_2\,(t)\;\alpha\; w_2\,(t) \tag{4.45}$$

$$I_{out}\,(t)\;\alpha\; w_2\,(t) \tag{4.46}$$

Where $w_k(t) = \left[\prod_{j=1}^{k} P_k(t)\right] I_{in}(t) = P_k(t) w_{k-1}(t)$, $w_1(t) = u_1\, e\left[\frac{V_{C1}(t)}{V_T}\right]$ & $I_C(t) = 1/P(t) \neq 0$

The transfer function can be written as

$$H\,(s) = \frac{(I_{01} I_{02}/C_1 C_2\, V_T^2)}{s^2 + (I_d/C_2 V_T)s + (I_{01} I_{03}/C_1 C_2\, V_T^2)} \tag{4.47}$$

.The cut off frequency (w_0) and quality factor (Q) are calculated as

$$w_0 = (\sqrt{I_{01}\, I_{03}}/\sqrt{C_1\, C_2}\, V_T\,) \tag{4.48}$$

$$Q = \left(\sqrt{\frac{C_2}{C_1}}\right)\left(\sqrt{I_{01}\, I_{03}}/I_d\right) \tag{4.49}$$

4.3.8 Simulation results

The log domain second order log domain low pass filter is simulated in PSPICE. The power supply voltages are taken as 1.5 V, $C_1 = C_2 = 30$ pF, $I_D = I_{01} = I_{02} = I_{03} = 50$ uA. The PSPICE simulated cut off frequency calculated is 5.57 MHZ which is close to the theoretical cut off frequency of 6 MHZ. The transient and frequency responses are shown in Fig.4.9 (a) to Fig. 4.9 (d).

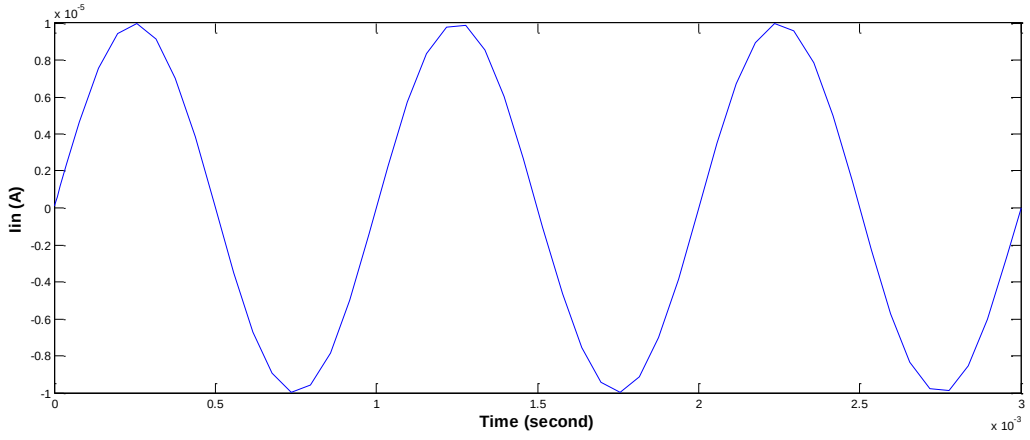

Fig.4.9 (a) Transient response for input of low pass filter.

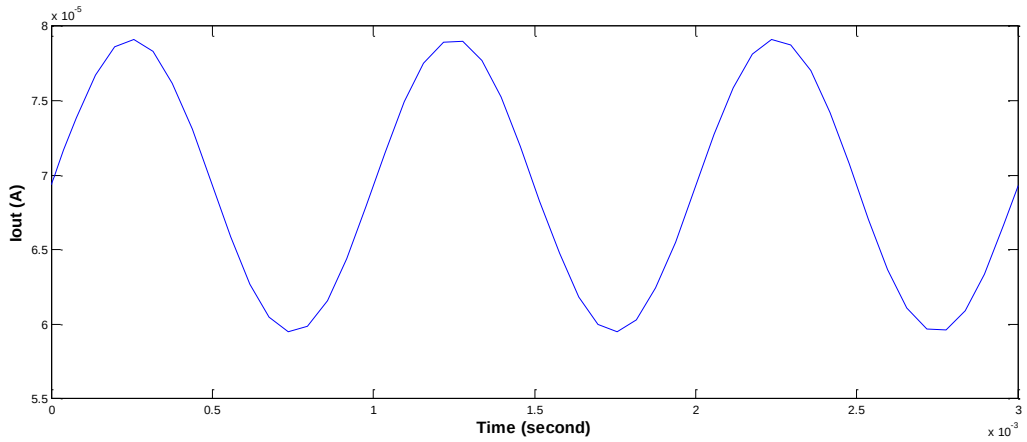

Fig.4.9 (b) Transient response for output of low pass filter.

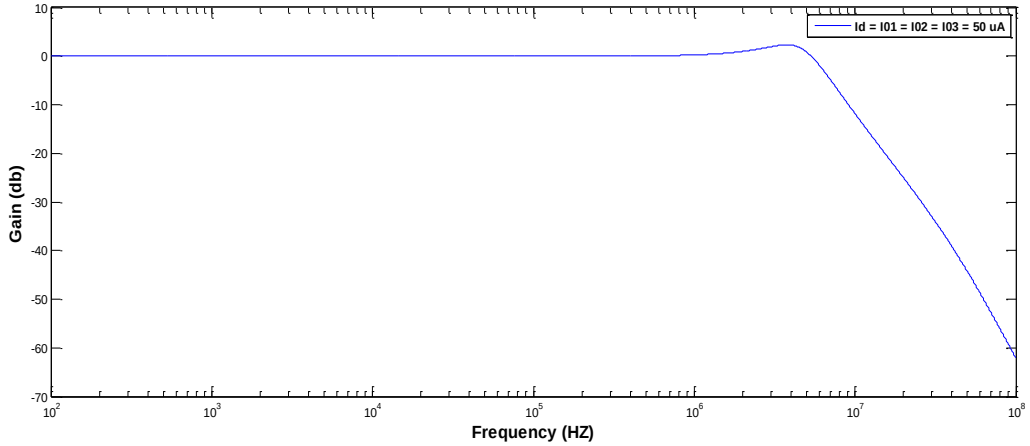

Fig.4.9 (c) Gain response of low pass filter.

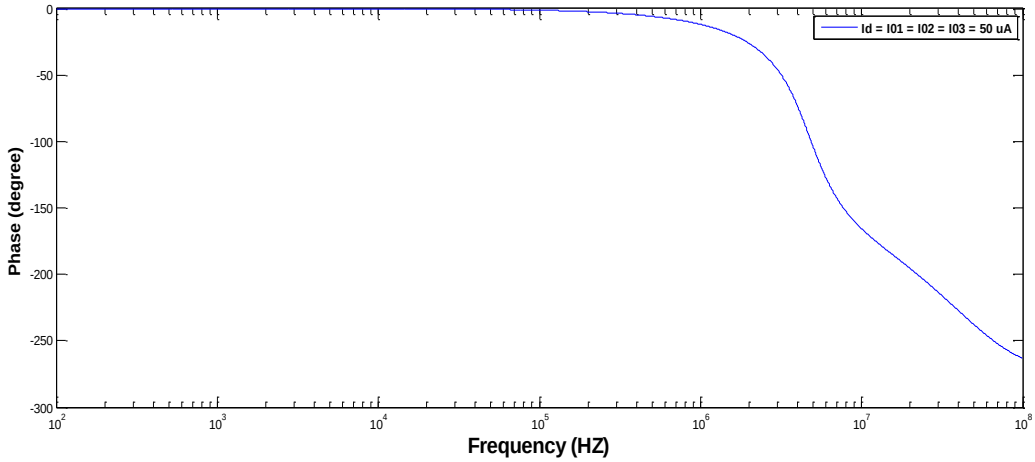

Fig.4.9 (d) Phase response of low pass filter.

4.4 Conclusion

This chapter covers the state space synthesis of log domain filters created through Bernoulli cell. In this chapter we have presented the state space method for design of log domain integrator, first and second order current mode filters. PSPICE Simulations are also provided to confirm the theoretical results. The time and frequency responses for these filters have been simulated using PSPICE.

Chapter 5

Conclusion and future scope

5.1 Conclusion

In chapter 2, The Translinear circuit and principles of log domain circuits based on translinear principle has been discussed in detail. The Bernoulli cell, basic principles of Bernoulli cell and interconnection of Bernoulli cell has been discussed for implementation of higher order filter circuits. Applications of translinear principle for design of log domain lossy integrator and first order current mode filter circuits have also presented and Bernoulli cell applications like first order lossy integrator, second order filter circuit containing zero and Third and proposed fourth order low pass butterworth filter have been designed which was simulated using PSPICE.

In chapter 3, LC ladders and design of log domain filters based on simulation of LC ladders have been discussed. Applications of LC ladder in log domain filters like design of chebyshev and elliptic filters have been designed which was simulated using PSPICE.

In chapter 4, State space syntheses of linear circuits and corresponding log domain state space realization have been discussed. Applications of state space approach in realization of log domain filters are also discussed. The pole frequency and bandwidth of log domain filters can be tuned independently. Design of first order log domain low pass filter, lossless integrator and band pass and lowpass biquad have been presented and was simulated using PSPICE.

5.2 Scope for future work

In this dissertation we have presented the various techniques used for designing transistor level current mode filters employing log-domain techniques and its applications in analog circuits. Log domain filters have advantage over other filters as it directly exploits the non-linear characteristics of the transistors to linearize the whole filter. Log domain filters have a simple structure and have capability to run at high frequencies and also having low power supply requirement. It can be used for realization of sinusoidal oscillators and nth order universal filter. There is scope for the improvement in the design topology of log domain filters. Thus there is enough scope for extension of the work presented in this dissertation.

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APPENDICES

Appendix-1

The PSPICE model file used for the AT & T CBIC-R Transistors.

*** NR200N–2X NPN Transistor**

.MODEL QN NPN (RB=524.6 IRB=0 RBM=25 RC=50 RE=1 IS=121E-18 EG=1.206 XTI=2 +XTB=1.538 BF=137.5 IKF=6.974E-3 NF=1 VAF=159.4 ISE=36E-16 NE=1.713 BR=0.7258 +IKR=2.198E-3 NR=1 VAR=10.7 ISC=0 NC=2 TF=0.425E-9 TR=0.425E-8 CJE=0.214E-12 +VJE=0.5 MJE=0.28 CJC=0.983E-13 VJC=0.5 MJC=0.3 XCJC=0.034 CJS=0.913E-12 VJS=0.64 +MJS=0.4 FC=0.5)

***NR200N–2X NPN Transistor**

.MODEL QN NPN (RB=262.5 IRB=0 RBM=12.5 RC=25 RE=0.5 IS=242E-18 EG=1.206 XTI=2 +XTB=1.538 BF=137.5 IKF=13.94E-3 NF=1.0 VAF=159.4 ISE=72E-16 NE=1.713 BR=0.7258 +IKR=4.396E-3 NR=1 VAR=10.73 ISC=0 NC=2 TF=0.425E-9 TR=0.425E-8 CJE=0.428E-12 +VJE=0.5 MJE=0.28 CJC=1.97E-13 VJC=0.5 MJC=0.3 XCJC=0.065 CJS=1.17E-12 VJS=0.64 +MJS=0.4 FC=0.5)

*** HSB2 NPN Transistor**

.MODEL C12TYP NPN (IS=7.40E-018 BF=1.00E+002 BR=1.00E+00 NF=1.00E+000 +NR=1.00E+000 TF=6.00E-012 TR=1.00E-008 XTF=1.00E+001 VTF=1.50E+000 ITF=2.30E-002 +PTF=3.75E+001 VAF=4.50E+001 VAR=3.00E+000 IKF=3.10E-002 IKR=3.80E-003 ISE=2.80E +016 NE=2.00E+000 ISC=1.50E-016 NC=1.50E+000 RE=5.26E+000 RB=5.58E+001 +IRB=0.00E+000 RBM=1.55E+001 RC=8.09E+001 CJE=3.21E-014 VJE=1.05E+000 MJE=1.60E-+001 CJC=2.37E-014 VJC=8.60E-001 MJC=3.40E-001 XCJC=2.30E-001 CJS=1.95E-014 +VJS=8.20E-001 MJS=3.20E-001 EG=1.17E+000 XTB=1.70E+000 XTI=3.00E+000 KF=0.00E+00 +AF=1.00E+000 FC=5.00E-001)

***PR200N–2X PNP Transistor**

.MODEL QP PNP (RB=163.5 IRB=0 RBM=12.27 RC=25 RE=1.5 IS=147E-18 EG=1.206 XTI=1.7
+XTB=1.866 BF=110 IKF=4.718E-3 NF=1.0 VAF=51.8 ISE=50.2E-16 NE=1.650 BR=0.4745
+IKR=12.96E-3 NR=1 VAR=9.96 ISC=0 NC=2 TF=0.610E-9 TR=0.610E-8 CJE=0.36E-12
+VJE=0.5 MJE=0.28 CJC=0.328E-12 VJC=0.8 MJC=0.4 XCJC=0.074 CJS=1.39E-12 VJS=0.55
+MJS=0.35 FC=0.5)

Appendix-2

Circuit file used in PSPICE Simulations.

(i) Log domain lossy integrator in Fig.2.4

```
Q1 1 2 0 0  QN
Q2 3 1 2 0  QN
Q3 3 1 4 0 QN
Q4 5 4 0 0 QN
C1 4 0 50PF
Vcc 3 0 DC 2.5V
VQOUT 5 0 DC 2.5V
Iin 3 1 AC 20UA
Iin1 0 1 DC 2UA
I2 2 0 DC 50UA
I3 4 0 DC 50UA

.MODEL QN NPN  (IS=7.40E-018 BF=1.00E+002
+BR=1.00E+00  NF=1.00E+000  NR=1.00E+000
+TF=6.00E-012  TR=1.00E-008 XTF=1.00E+001
+VTF=1.50E+00  ITF=2.30E-002 PTF=3.75E+001
+VAF=4.50E+001  VAR=3.00E+000  IKF=3.10E-
+002IKR=380E-003ISE=2.80E-016
+NE=2.00E+000  ISC=1.50E-016  NC=1.50E+000
+RE=5.26E+000  RB=5.58E+001 IRB=0.00E+000
+RBM=1.55E+001  RC=8.09E+001  CJE=3.21E-
+014VJE=1.05E+000MJE=1.60E-001 CJC=2.37E-
+014VJC=8.60E-001MJC=3.40E+001
+XCJC=2.30E-001  CJS=1.95E-014  VJS=8.20E-
+001MJS=3.20E-001EG=1.17E+000
+XTB=1.70E+000 XTI=3.00E+000 KF=0.00E+00
+AF=1.00E+000 FC=5.00E-001)
```

```
*Iin 3 1 SIN (0 .3UA 1KHZ)
.AC DEC 1000 1HZ 100MEGHZ
*Iin 0 1 DC 50UA PULSE(0 100UA 0 1NS 1NS
50NS 100NS)
Iin 3 1 AC 10UA PULSE(0 10UA 0 1NS 1NS
0.05US 0.1US)
*.PARAM VAL=20UA
*C1 4 0 {VAL}
*.STEP PARAM VAL 20PF 60PF 20PF
*.TRAN 0US 0.5US
.PROBE
.END
```

(ii) Log domain high pass and low pass first order filter in Fig.2.6

```
Q1 1 1 3 0 QN
Q3 6 6 8 0 QN
Q5 10 6 11 0 QN
Q7 13 13 15 0 QN
Q9 17 13 18 0 QN
Q11 12 19 20 0 QN
Q13 23 19 24 0 QN
Q15 26 12 27 0 QN
Q17 28 12 29 0 QN
Q2 4 4 3 0 QP
Q4 9 1 8 0 QP
Q6 12 12 11 0 QP
Q8 16 12 15 0 QP
Q10 19 19 18 0 QP
Q12 22 21 20 0 QP
Q14 25 25 24 0 QP
Q16 21 21 27 0 QP
Q18 30 30 29 0 QP

.MODEL QN NPN (RB=262.5 IRB=0 RBM=12.5
RC=25 RE=0.5 IS=242E-18 EG=1.206 XTI=2
+XTB=1.538 BF=137.5 IKF=13.94E-3 NF=1.0
+VAF=159.4 ISE=72E-16 NE=1.713 BR=0.7258
+IKR=4.396E-3 NR=1 VAR=10.73 ISC=0 NC=2
+TF=0.425E-9 TR=0.425E-8 CJE=0.428E-12
+VJE=0.5 MJE=0.28 CJC=1.97E-13 VJC=0.5
+MJC=0.3 XCJC=0.065 CJS=1.17E-12 VJS=0.64
+MJS=0.4 FC=0.5)

.MODEL QP PNP (RB=163.5 IRB=0 RBM=12.27
+RC=25 RE=1.5 IS=147E-18 EG=1.206 XTI=1.7
+XTB=1.866 BF=110 IKF=4.718E-3 NF=1.0
+VAF=51.8 ISE=50.2E-16 NE=1.650 BR=0.4745
+IKR=12.96E-3 NR=1 VAR=9.96 ISC=0 NC=2
+TF=0.610E-9 TR=0.610E-8 CJE=0.36E-12
+VJE=0.5 MJE=0.28 CJC=0.328E-12 VJC=0.8
+MJC=0.4 XCJC=0.074 CJS=1.39E-12 VJS=0.55
+MJS=0.35 FC=0.5)
```

```
IIN 0 1 AC 20uA
*IIN 0 1 SIN(0 50uA 1KHZ)
*.PARAM VAL=10UA
*I01 0 6 {VAL}
*.STEP PARAM VAL 10UA 30UA 5UA
*I02 12 0 {VAL}
*.STEP PARAM VAL 10UA 30UA 5UA
*PARAM VAL=10UA
*I03 0 13 {VAL}
*.STEP PARAM VAL 10UA 30UA 5UA
I0 0 1 DC 100UA
I01 0 6 DC 100UA
I02 12 0 DC 100UA
I03 0 13 DC 100UA
I04 21 0 DC 100UA
C 19 0 200PF
R1 25 0 1OHM
*R2 30 0 1OHM
VQ17 28 0 DC 3V
VQ15 26 0 DC 3V
VQ13 23 0 DC 3V
VQ5 10 0 DC 3V
VQ9 17 0 DC 3V
VQ12 22 0 DC 0V
VQ8 16 0 DC 0V
VQ2 4 0 DC 0V
VQ4 9 0 DC 0V
VQ18 30 0 DC 0V
.AC DEC 1000 100HZ 10MEGHZ
*.TRAN 1MS 2MS
.PROBE
.END
```

(iii) A Log domain lossy integrator in Fig.2.12

```
Q1 1 1 2 0 QN
Q2 3 1 4 0 QN
Q3 5 5 4 0 QN
Q4 6 5 7 0 QN

.MODEL QN NPN (RB=262.5 IRB=0 RBM=12.5
+RC=25 RE=0.5 IS=242E-18 EG=1.206 XTI=2
+XTB=1.538 BF=137.5 IKF=13.94E-3 NF=1.0
+VAF=159.4 ISE=72E-16 NE=1.713 BR=0.7258
+IKR=4.396E-3 NR=1 VAR=10.73 ISC=0 NC=2
+TF=0.425E-9 TR=0.425E-8 CJE=0.428E-12
+VJE=0.5 MJE=0.28 CJC=1.97E-13 VJC=0.5
+MJC=0.3 XCJC=0.065 CJS=1.17E-12 VJS=0.64
+MJS=0.4 FC=0.5)

C1 4 0 40PF
ID 4 0 DC 100UA
IO1 0 5 DC 100UA
IO2 4 0 DC 100UA
IIN 0 1 AC 30UA
IIN1 0 1 DC 20UA
```

```
VQ2 3 0 DC 1.5V
VQQ4 6 0 DC 1.5V
VQ1 2 0 DC 0V
VQ4 7 0 DC 0V
.AC DEC 1000 100HZ 100MEGHZ
*Iin 0 1 AC 50UA PULSE(0 100UA 0 1NS 1NS
50NS 100NS)
*.TRAN .4US .5US
.PROBE
.END
```

(iv) Second order filter containing zero in Fig.2.14

```
QIN 1 1 0 0 QN
Q1 2 1 3 0  QN
Q01 6 6 3 0  QN
Qq 4 4 3 0 QN
Q2 7 6 8 0 QN
Q03 9 9 8 0 QN
Q3 10 9 11 0 QN
QOUT 5 4 0 0 QN
QTX 3 11 12 0 QN
QT3 11 3 12 0 QN

.MODEL QN NPN (RB=524.6 IRB=0 RBM=25
+RC=50 RE=1 IS=121E-18 EG=1.206 XTI=2
+XTB=1.538 BF=137.5IKF=6.974E-3 NF=1
+VAF=159.4 ISE=36E-16 NE=1.713 BR=0.7258
+IKR=2.198E-3 NR=1 VAR=10.73 ISC=0 NC=2
+TF=0.425E-9 TR=0.425E-8 CJE=0.214E-12
+VJE=0.5 MJE=0.28 CJC=0.983E-13 VJC=0.5
+MJC=0.3 XCJC=0.034 CJS=0.913E-12 VJS=0.64
+MJS=0.4 FC=0.5)
```

```
IIN 0 1 AC 20UA
IIN1 0 1 DC 20UA
*IIN 0 1 SIN(0 2UA 1KHZ)
I01 0 6 DC 5UA
I02 3 0 DC 5UA
I03 0 9 DC 5UA
I04 8 0 DC 5UA
ID 8 0 DC 4.33UA
Iq1 0 4 DC 3UA
Iq2 3 0 DC 3UA
IB 12 0 DC 10UA
C1 3 0 5PF
C2 8 0 5PF
VQ1 2 0 DC 3V
VQ2 7 0 DC 3V
VQ3 10 0 DC 3V
VQOUT 5 0 DC 3V
.AC DEC 1000 100HZ 1000MEGHZ
*.TRAN 1MS 4MS
.PROBE
.END
```

(v) Third order Butterworth filter in Fig.2.16

```
QIN 2 2 3 0 QN
Q1 4 2 5 0  QN
Q01 7 7 5 0  QN
Q2 8 7 9 0 QN
Q02 11 11 9 0 QN
Q3 12 11 13 0 QN
Q03 15 15 13 0 QN
QOUT 16 15 50 0 QN
Q7 17 5 18 0 QN
QX2 5 17 18 0 QN
Q6 19 20 17 0 QN
Qq2 20 20 13 0 QN
Q5 22 9 23 0 QN
QX3 9 22 23 0 QN
Q4 24 25 22 0 QN
Qq1 25 25 13 0 QN

.MODEL QN NPN(RB=524.6 IRB=0 RBM=25
+RC=50 RE=1 IS=121E-18 EG=1.206 XTI=2
+XTB=1.538 BF=137.5IKF=6.974E-3 NF=1
+VAF=159.4 ISE=36E-16 NE=1.713 BR=0.7258
+IKR=2.198E-3 NR=1 VAR=10.73 ISC=0 NC=2
+TF=0.425E-9 TR=0.425E-8 CJE=0.214E-12
+VJE=0.5 MJE=0.28 CJC=0.983E-13 VJC=0.5
+MJC=0.3 XCJC=0.034 CJS=0.913E-12 VJS=0.64
+MJS=0.4 FC=0.5)

IIN 0 2 AC 20UA
IIN1 0 2 DC 20UA
*IIN 0 2 SIN(0 3UA 1KHZ)
I01 0 7 DC 4.6UA
I02 0 11 DC 7.7UA
I03 0 15 DC 4.6UA
I04 5 0 DC 4.6UA
I05 9 0 DC 7.7UA
I06 13 0 DC 4.6UA
ID 13 0 DC 10.9UA
Iq2 0 20 DC 4.6UA
Iq3 13 0 DC 4.6UA
Iq1 0 25 DC 7.7UA
Iq4 13 0 DC 7.7UA
IB1 18 0 DC 10UA
IB2 23 0 DC 10UA
C1 5 0 40PF
C2 9 0 40PF
C3 13 0 40PF
VQ1 4 0 DC 3V
VQ2 8 0 DC 3V
VQ3 12 0 DC 3V
VQ6 19 0 DC 3V
VQ4 24 0 DC 3V
VQIN 3 0 DC 0V
VQOUT 16 0 DC 0V
VQQOUT 50 0 DC 0V
.AC DEC 1000 100HZ 10MEGHZ
*.TRAN 1MS 4MS
.PROBE
.END
```

(vi) Proposed fourth order Butterworth filter in Fig.2.18

```
QIN 2 2 0 0 QN
Q1 4 2 5 0  QN
Q01 7 7 5 0  QN
Q2 8 7 9 0 QN
Q02 11 11 9 0 QN
Q3 12 11 13 0 QN
Q03 53 53 13 0 QN
Q10 52 53 51 0 QN
Q04 15 15 51 0 QN
QOUT 16 15 0 0 QN
Q7 17 5 18 0 QN
QX2 5 17 18 0 QN
Q6 19 20 17 0 QN
Qq2 20 20 51 0 QN
Q5 22 9 23 0 QN
QX3 9 22 23 0 QN
Q4 24 25 22 0 QN
Qq1 25 25 51 0 QN
Q12 56 13 57 0 QN
QX5 13 56 57 0 QN
Q11 55 54 56 0 QN
Qq3 54 54 51 0 QN

.MODEL QN NPN (RB=524.6 IRB=0 RBM=25
+RC=50 RE=1 IS=121E-18 EG=1.206 XTI=2
+XTB=1.538 BF=137.5 IKF=6.974E-3 NF=1
+VAF=159.4 ISE=36E-16 NE=1.713 BR=0.7258
+IKR=2.198E-3 NR=1 VAR=10.73 ISC=0 NC=2
+TF=0.425E-9 TR=0.425E-8 CJE=0.214E-12
+VJE=0.5 MJE=0.28 CJC=0.983E-13 VJC=0.5
+MJC=0.3 XCJC=0.034 CJS=0.913E-12 VJS=0.64
+MJS=0.4 FC=0.5)

IIN 0 2 AC 20UA
IIN1 0 2 DC 5UA
```

```
*IIN 0 2 SIN(0 3UA 1KHZ)
I01 0 7 DC 15UA
I02 0 11 DC 11.9UA
I03 0 53 DC 11.9UA
I04 0 15 DC 2.7UA
I05 5 0 DC 15UA
I06 9 0 DC 11.9UA
I07 13 0 DC 11.9UA
I08 51 0 DC 2.7UA
ID 51 0 DC 10.9UA
Iq2 0 20 DC 2.7UA
Iq3 51 0 DC 2.7UA
Iq1 0 25 DC 5UA
Iq4 51 0 DC 5UA
Iq5 0 54 DC 5UA
Iq6 51 0 DC 5UA
IB1 18 0 DC 10UA
IB2 23 0 DC 10UA
IB3 57 0 DC 10UA
C1 5 0 40PF
C2 9 0 40PF
C3 13 0 40PF
C4 51 0 40PF
VQ1 4 0 DC 3V
VQ2 8 0 DC 3V
VQ3 12 0 DC 3V
VQ10 52 0 DC 3V
VQ6 19 0 DC 3V
VQ4 24 0 DC 3V
VQ11 55 0 DC 3V
VQOUT 16 0 DC 1V
.AC DEC 1000 10HZ 10000MEGHZ
*.TRAN 1MS 4MS
.PROBE
.END
```

(vii) Third order elliptic filter in Fig.3.9 (c)

```
Q1 1 1 2 0 QN
Q2 4 1 5 0 QN
Q3 7 7 8 0 QN
Q4 10 7 11 0 QN
Q5 15 6 16 0 QN
Q6 6 12 13 0 QN
Q7 18 18 19 0 QN
Q8 21 18 22 0 QN
Q9 24 12 25 0 QN
Q10 12 23 27 0 QN
Q11 29 29 30 0 QN
Q12 32 29 33 0 QN
Q13 3 3 2 0 QP
Q14 6 6 5 0 QP
Q15 9 6 8 0 QP
Q16 12 12 11 0 QP
Q17 17 17 16 0 QP
Q18 14 17 13 0 QP
Q19 20 12 19 0 QP
Q20 23 23 22 0 QP
Q21 26 26 25 0 QP
Q22 28 26 27 0 QP
Q23 31 23 30 0 QP
Q24 34 34 33 0 QP

.MODEL QN NPN (RB=262.5 IRB=0 RBM=12.5
+RC=25 RE=0 IS=242E-18 EG=1.206 XTI=2
+XTB=1.538 BF=137.5 IKF=13.94E-3 NF=1.0
+VAF=159.4 ISE=72E-16 NE=1.713 BR=0.7258
+IKR=4.396E-3 NR=1 VAR=10.73 ISC=0 NC=2
+TF=0.425E-9 TR=0.425E-8 CJE=0.428E-12
+VJE=0.5 MJE=0.28 CJC=1.97E-13 VJC=0.5
+MJC=0.3 XCJC=0.065 CJS=1.17E-12 VJS=0.64
+MJS=0.4 FC=0.5)

.MODEL QP PNP (RB=163.5 IRB=0 RBM=12.27
+RC=25 RE=0 IS=147E-18 EG=1.206 XTI=1.7
+XTB=1.866 BF=110 IKF=4.718E-3 NF=1.0
+VAF=51.8 ISE=50.2E-16 NE=1.650 BR=0.4745
+IKR=12.96E-3 NR=1 VAR=9.96 ISC=0 NC=2
+TF=0.610E-9 TR=0.610E-8 CJE=0.36E-12
+VJE=0.5 MJE=0.28 CJC=0.328E-12 VJC=0.8
+MJC=0.4 XCJC=0.074 CJS=1.39E-12 VJS=0.55
+MJS=0.35 FC=0.5)
```

```
CC1 6 0 6.79560nF
CL2 12 0 3.47308nF
CC2 6 23 6.79560nF
CC3 23 0 9.55216nF
IO1 0 7 DC 90uA
IO2 0 18 DC 90uA
IO3 17 0 DC 90uA
IO4 26 0 DC 90uA
IO5 6 0 DC 90uA
IIN 0 1 AC 15uA
IIN1 0 1 DC 20UA
*IIN 0 1 SIN (0 15uA 1000HZ)
IO6 23 0 DC 90uA
IO7 0 29 DC 90uA
VQ2 4 0 DC 5V
VQ4 10 0 DC 5V
VQ8 21 0 DC 5V
VQ5 15 0 DC 5V
VQ9 24 0 DC 5V
VQ12 32 0 DC 5V
VQ15 9 0 DC -5V
VQ19 20 0 DC -5V
VQ18 14 0 DC -5V
VQ22 28 0 DC -5V
VQ23 31 0 DC -5V
VQ13 3 0 DC 0V
VQ24 34 0 DC 0V
.AC DEC 1000 1HZ 100KHZ
*.TRAN 0ms 2ms
.PROBE
.END
```

(viii) Fifth order chebyshev filter in Fig.3.10 (c)

```
Q1 1 1 2 0 QN
Q3 4 1 5 0 QN
Q5 9 9 7 0 QN
Q6 10 9 11 0 QN
Q9 51 6 52 0 QN
Q10 6 12 53 0 QN
Q13 15 15 16 0 QN
Q14 18 15 19 0 QN
Q17 54 12 55 0 QN
Q18 12 20 21 0 QN
Q21 24 24 25 0 QN
Q22 27 24 28 0 QN
Q25 30 20 31 0 QN
Q26 20 29 80 0 QN
Q29 34 34 35 0 QN
Q30 37 34 38 0 QN
Q33 40 29 41 0 QN
Q34 29 39 43 0 QN
Q37 45 45 46 0 QN
Q38 48 45 49 0 QN
Q2 3 3 2 0 QP
Q4 6 6 5 0 QP
Q7 8 6 7 0 QP
Q8 12 12 11 0 QP
Q11 13 13 52 0 QP
Q12 14 13 53 0 QP
Q15 17 12 16 0 QP
Q16 20 20 19 0 QP
Q19 23 23 55 0 QP
Q20 22 23 21 0 QP
Q23 26 20 25 0 QP
Q24 29 29 28 0 QP
Q27 32 32 31 0 QP
Q28 33 32 80 0 QP
Q31 36 29 35 0 QP
Q32 39 39 38 0 QP
Q35 42 42 41 0 QP
Q36 44 42 43 0 QP
Q39 47 39 46 0 QP
Q40 50 50 49 0 QP
.MODEL QN NPN (RB=262.5 IRB=0 RBM=12.5
+RC=25 RE=0.5 IS=242E-18 EG=1.206 XTI=2
+XTB=1.538 BF=137.5 IKF=13.94E-3 NF=1.0
+VAF=159.4 ISE=72E-16 NE=1.713 BR=0.7258
+IKR=4.396E-3 NR=1 VAR=10.73 ISC=0 NC=2
+TF=0.425E-9 TR=0.425E-8 CJE=0.428E-12
VJE=0.5 +MJE=0.28 CJC=1.97E-13 VJC=0.5
MJC=0.3 +XCJC=0.065 CJS=1.17E-12 VJS=0.64
MJS=0.4 +FC=0.5)
```

```
.MODEL QP PNP(RB=163.5 IRB=0 RBM=12.27
+RC=25 RE=1.5 IS=147E-18 EG=1.206 XTI=1.7
+XTB=1.866 BF=110 IKF=4.718E-3 NF=1.0
+VAF=51.8 ISE=50.2E-16 NE=1.650 BR=0.4745
+IKR=12.96E-3 NR=1 VAR=9.96 ISC=0 NC=2
+TF=0.610E-9 TR=0.610E-8 CJE=0.36E-12
+VJE=0.5 MJE=0.28 CJC=0.328E-12 VJC=0.8
+MJC=0.4 XCJC=0.074 CJS=1.39E-12 VJS=0.55
+MJS=0.35 FC=0.5)
CC1 6 0 6.79560nF
CL2 12 0 3.47308nF
CC3 20 0 9.55216nF
CL4 29 0 3.4708nF
CC5 39 0 6.79560nF
IO1 0 9 DC 220uA
IO2 0 15 DC 220uA
IO3 0 24 DC 220uA
IO4 0 34 DC 220uA
IO5 0 45 DC 220uA
IIN 0 1 AC 50uA
IIN1 0 1 DC 11UA
IO7 6 0 DC 220uA
IO8 13 0 DC 220uA
IO9 23 0 DC 220uA
I10 32 0 DC 220uA
I11 42 0 DC 220uA
I12 39 0 DC 220uA
VQ3 4 0 DC 5V
VQ6 10 0 DC 5V
VQ14 18 0 DC 5V
VQ22 27 0 DC 5V
VQ30 37 0 DC 5V
VQ38 48 0 DC 5V
VQ9 51 0 DC 5V
VQ17 54 0 DC 5V
VQ25 30 0 DC 5V
VQ33 40 0 DC 5V
VQ7 8 0 DC -5V
VQ15 17 0 DC -5V
VQ23 26 0 DC -5V
VQ31 36 0 DC -5V
VQ12 14 0 DC -5V
VQ20 22 0 DC -5V
VQ28 33 0 DC -5V
VQ36 44 0 DC -5V
VQ39 47 0 DC -5V
VQ2 3 0 DC 0V
VQ40 50 0 DC 0V
.AC DEC 1000 100HZ 1MEGHZ
.PROBE
.END
```

(ix) A first order log domain low pass filter in Fig.4.2

```
Q1 1 1 12 0 QN
Q2 3 3 1 0 QN
Q3 7 3 5 0 QN
Q4 7 5 12 0 QN

.MODEL QN NPN (RB=262.5 IRB=0 RBM=12.5
+RC=25 RE=0.5 IS=242E-18 EG=1.206 XTI=2
+XTB=1.538 BF=137.5 IKF=13.94E-3 NF=1.0
+VAF=159.4 ISE=72E-16 NE=1.713 BR=0.7258
+IKR=4.396E-3 NR=1 VAR=10.73 ISC=0 NC=2
+TF=0.425E-9 TR=0.425E-8 CJE=0.428E-12
+VJE=0.5 MJE=0.28 CJC=1.97E-13 VJC=0.5
+MJC=0.3 XCJC=0.065 CJS=1.17E-12 VJS=0.64
+MJS=0.4 FC=0.5)

IF1 5 0 DC 100UA
IF2 1 0 DC 100UA
IF3 7 3 DC 100UA
```

```
Iin 7 1 AC 50UA
IIN1 7 1 DC 10UA
*Iin 7 1 SIN (0 100UA 1KHZ)
C1 5 0 200PF
VCC 7 0 DC 3V
VNEG 12 0 DC 0V
*VQ3 4 0 DC 3V
*VQ4 6 0 DC 3V
.AC DEC 1000 10 100MEGHZ
*.TRAN 1MS 2MS
.PROBE
.END
```

(x) A log domain lossless integrator in Fig.4.4

```
Qin 1 1 0 0  QN
QA 3 1 4 0  QN
Qref 8 4 9 0 QN
QU1 4 13 9 0 QN
Q1 9 11 12 0 QN
Q2 11 11 12 0 QN
QB 10 8 11 0 QN
Q01 5 5 4 0 QN
Qout 6 5 0 0 QN
C1 4 0 20PF
VQA 3 0 DC 1.5V
VQOUT 6 0 DC 1.5V
VQB 10 0 DC 1.5V
VNEG 12 0 DC 0V
VREF 13 0 DC 0V
IREF 0 8 DC 50UA
I01 0 5 DC 50UA
I02 4 0 DC 50UA
.MODEL QN NPN(RB=262.5 IRB=0 RBM=12.5
+RC=25 RE=0.5 IS=242E-18 EG=1.206 XTI=2
+XTB=1.538 BF=137.5 IKF=13.94E-3 NF=1.0
+VAF=159.4 ISE=72E-16 NE=1.713 BR=0.7258
+IKR=4.396E-3 NR=1 VAR=10.73 ISC=0 NC=2
+TF=0.425E-9 TR=0.425E-8 CJE=0.428E-12
+VJE=0.5 MJE=0.28 CJC=1.97E-13 VJC=0.5
```

```
+MJC=0.3 XCJC=0.065 CJS=1.17E-12 VJS=0.64
+MJS=0.4 FC=0.5)
Iin 0 1 AC 400uA
iin1 0 1 DC 30UA
*Iin 0 1 SIN (0 50UA 1KHZ)
*Iin 0 1 AC 500UA PULSE(0 50UA 0 1NS 1NS
0.05US 0.1US)
*.PARAM VAL=20UA
*C1 4 0 {VAL}
*.STEP PARAM VAL 20PF 60PF 20PF
*.TRAN 1uS 10uS
.AC DEC 1000 1 100MEGHZ
.PROBE
.END
```

(xi) Log domain bandpass filter in Fig.4.6

```
Qq1 16 16 4 0  QN
Qout 17 16 0 0  QN
Qin 1 1 0 0 QN
Q1 3 1 4 0 QN
Q01 5 5 4 0 QN
Q2 6 5 7 0 QN
Q03 13 4 14 0 QN
QF 20 13 15 0 QN
Qref 8 7 9 0 QN
Qu2 7 100 9 0 QN
QA 12 8 10 0 QN
QU1 4 7 14 0 QN
QB 14 15 11 0 QN
QC 15 15 11 0 QN
QD 9 10 11 0 QN
QE 10 10 11 0 QN

.MODEL QN NPN(RB=262.5 IRB=0 RBM=12.5
+RC=25 RE=0.5 IS=242E-18 EG=1.206 XTI=2
+XTB=1.538 BF=137.5 IKF=13.94E-3 NF=1.0
+VAF=159.4 ISE=72E-16 NE=1.713 BR=0.7258
+IKR=4.396E-3 NR=1 VAR=10.73 ISC=0 NC=2
+TF=0.425E-9 TR=0.425E-8 CJE=0.428E-12
+VJE=0.5 MJE=0.28 CJC=1.97E-13 VJC=0.5
+MJC=0.3 XCJC=0.065 CJS=1.17E-12 VJS=0.64
+MJS=0.4 FC=0.5)
```

```
IIN 0 1 AC 20UA
IIN1 0 1 DC 50UA
*IIN 0 1 SIN (0 40UA 1MEGHZ)
Iq1 0 16 DC 50UA
Iq11 4 0 DC 50UA
I01 0 5 DC 35UA
I011 4 0 DC 35UA
ID 4 0 DC 50UA
I03 0 13 DC 50UA
IREF 0 8 DC 50UA
C1 4 0 30PF
C2 7 0 30PF
VQOUT 17 0 DC 1.5V
VQ1 3 0 DC 1.5V
VQ2 6 0 DC 1.5V
VQF 20 0 DC 1.5V
VQA 12 0 DC 1.5V
VREF 100 0 DC -12mV
VQNEG 11 0 DC -1.5V
.AC DEC 1000 100HZ 100GHZ
*.TRAN .1US 3US
.PROBE
.END
```

(xii) Proposed log domain lowpass filter in Fig.4.8

```
Qin 1 1 0 0  QN
Q1 2 1 3 0  QN
Q01 4 4 3 0 QN
Q2 5 4 6 0 QN
Q02 7 7 6 0 QN
Qout 8 7 0 0 QN
Q4 9 3 10 0 QN
Q5 3 9 10 0 QN
Q6 11 12 9 0 QN
Q7 12 12 6 0 QN

.MODEL QN NPN(RB=262.5 IRB=0 RBM=12.5
+RC=25 RE=0.5 IS=242E-18 EG=1.206 XTI=2
+XTB=1.538 BF=137.5 IKF=13.94E-3 NF=1.0
+VAF=159.4 ISE=72E-16 NE=1.713 BR=0.7258
+IKR=4.396E-3 NR=1 VAR=10.73 ISC=0 NC=2
+TF=0.425E-9 TR=0.425E-8 CJE=0.428E-12
+VJE=0.5 MJE=0.28 CJC=1.97E-13 VJC=0.5
+MJC=0.3 XCJC=0.065 CJS=1.17E-12 VJS=0.64
+MJS=0.4 FC=0.5)
```

```
C1 3 0 50PF
C2 6 0 50PF
I01 0 4 DC 50UA
I02 3 0 DC 50UA
ID2 6 0 DC 50UA
I03 0 7 DC 50UA
I04 6 0 DC 50UA
IB 10 0 DC 70UA
I05 0 12 DC 50UA
I06 6 0 DC 50UA
VQ1 2 0 DC 1.5V
VQ2 5 0 DC 1.5V
VQOUT 8 0 DC 1.5V
VQ6 11 0 DC 1.5V
IIN1 0 1 DC 30UA
IIN 0 1 AC 40UA
*IIN 0 1 SIN(0 10UA 1KHZ)
*.TRAN 1ms 3ms
.AC DEC 1000 100HZ 100MEGHZ
.PROBE
.END
```