A DISSERTATION

ON

IMPLEMENTATION OF VLSI CIRCUITS USING CURRENT CONVEYORS

Submitted in partial fulfillment of the requirement for the award of Degree of
MASTER OF TECHNOLOGY

in

VLSI Design and Embedded Systems

Submitted by

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This is to certify that the project entitled "**Implementation of VLSI circuits using Current Conveyors**" has been completed by **Antony CX** in partial fulfillment of the requirement of **Master in Technology** in **VLSI Design and Embedded Systems**. This is a record of his work carried out by him under my supervision and support. He has completed his work with utmost sincerity and diligence.

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ACKNOWLEDGEMENT

I express my deepest gratitude to my project guide **Asst. Prof. Alok Kumar Singh,** Department of Electronics and Communication Engineering, Delhi Technological University whose encouragement, guidance and support from the initial to the final level enabled me to develop an understanding of the subject. His suggestions and ways of summarizing the things made me to go for independent studying and trying my best to get the maximum for my project, this made my circle of knowledge very vast. I am highly thankful to him for guiding me in this project.

I also express my profound sense of gratitude to **Prof Prem R. Chadha (H.O.D. ECE),** for giving encouragement and opportunity to complete my project smoothly.

Finally, I take this opportunity to extend my deep appreciation to my friends especially **Mr. Robin Jain** and **Mr. Rahul Pal** for helping me cross the hurdles. I thank God for helping me at all times.

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ABSTRACT

Analog VLSI can deal with nearly all real world issues and has extended its range of circuits (amplifier, filters, communication circuits, current comparators etc) for new information processing applications in numerous fields like integrated sensors, image processing, speech recognition, hand writing recognition etc. This lead to an increased interest in the evolution process of active elements which are used for analog signal processing.

Current conveyors an excellent linear active element with high bandwidth, greater dynamic range and better high frequency response has evolved as a building block for higher efficiency blocks. Evolved in 1968 as the first generation current conveyor, the block gained huge reputation with the second generation in 1970 and the third generation in 1995.

Differential Difference Current Conveyor an active block which is similar to the DDA at the input side and CCII at the output and hence combining the qualities of Current Conveyor and Differential Difference Amplifier whose simple implementation makes it a universal building block has huge applications.

Project Guide

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF SYMBOLS

R_0	Output resistance
I_0	Output current
H_o	Gain at ωo
K	Voltage divider ratio
Q	Quality factor
H_o'	Modified H_o
Q’	Modified Q
W	Channel width
L	Channel length
A_o	Open loop gain
V_{SS}	Negative supply voltage
V_{DD}	Positive supply voltage
V_B	Bias Voltage
ωo	Natural frequency
I_{REF}	Reference Current
V_O	Output Voltage

ABBREVIATIONS

DDCC	Differential Difference Current Conveyor
DDA	Differential Difference Amplifier
OpAmp	Operational Amplifier
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
BJT	Bipolar Junction Transistor
NMOS	N-channel Metal Oxide Semiconductor
PMOS	P-channel Metal Oxide Semiconductor
VLSI	Very Large Scale Integration
SAB	Single Amplifier Biquad
HPF	High Pass Filter
LPF	Low Pass Filter
CMOS	Complementary Metal-Oxide Semiconductor
IC	Integrated Circuit
CCI	First Generation Current Conveyor
CCII	Second Generation Current Conveyor
CCIII	Third Generation Current Conveyor
DC	Direct Current

CHAPTER 1
INTRODUCTION

1.1 INTRODUCTION

Operational amplifiers have changed the face of linear analog electronics since its invention. Op-amps find usability in various fields such as of voltage references, analog multipliers, wave shaping circuits, oscillators and function generators. But it suffers from less gain bandwidth product and decreased slew rate at output. This causes hindrance in its usability at higher frequencies. Current conveyors [1] have bridged this gap in op-amps as there is no requirement of higher voltage gain and higher precision passive components so the designing can be done with transistors. Current conveyors provide higher voltage gain in a wide frequency range in small and large signal operation therefore they have a larger gain bandwidth product.

In tuning too current conveyors are preferred as op-amps have less output swing of voltage. Current conveyors are flexible and versatile and widely used in filters, oscillators and other analog circuits. Current conveyors have been functionally as good as op-amps but with advantages like better linearity, wide dynamic range, low power consumption it is preferred over op-amps.

Another versatile analog building block the differential difference current conveyors (DDCC) [2] is popular because of the advantages of 2^{nd} generation current conveyors [1] and the differential difference amplifier (DDA) [3] like large signal bandwidth, increased linearity, wide dynamic range, arithmetic operational ability and simple circuitry. They also have two high impedance terminals which make easy for cascading and higher order filters can be built. Some blocks also have multiple outputs for filters. Like highpass, bandpass, lowpass, notch and all-pass filters can be implemented [4]. However there are some drawbacks to this too

(i) Need to match passive components
(ii) More passive components used

Still on the whole DDCC works with the qualities of two active elements and gives a platform for many applications.

1.2 SIGNAL PROCESSING DOMAINS

According to Alan V. Oppenheim and Ronald W. Schafer, the principles of signal processing can be found in the classical numerical analysis techniques of the 17th century. Oppenheim and Schafer further state that the "digitalization" or digital refinement of these techniques can be found in the digital control systems of the 1940s and 1950s.

It is sometimes desirable to have circuits capable of selectively filtering one frequency or range of frequencies out of a mix of different frequencies in a circuit. A circuit designed to perform this frequency selection is called a filter circuit, or simply a filter. A common need for filter circuits is in high-performance stereo systems, where certain ranges of audio frequencies need to be amplified or suppressed for best sound quality and power efficiency. The equalizers used allow the amplitudes of several frequency ranges to be adjusted to suit the listener's taste and acoustic properties of the listening area. A tweeter (high-frequency speaker) is inefficient at reproducing low-frequency signals such as drum beats, so a crossover circuit is connected between the tweeter and the stereo's output terminals to block low-frequency signals, only passing high-frequency signals to the speaker's connection terminals. This gives better audio system efficiency and thus better performance. Both equalizers and crossover networks are examples of filters, designed to accomplish filtering of certain frequencies.

Digital signal processing is a rapidly developing field and it advanced as growth in IC technology granted compact and efficient implementation of its algorithms on silicon chips. Even though various forms of signal processing have shifted to digital domain, but still analog circuits are essentially required in plenty of complex and high performance modern systems. It is a known fact that naturally occurring signals are analog. Therefore, analog circuits form a bridge between the digital domain and the actual world. Analog VLSI can deal with nearly all real world issues and has extended its range for new information processing applications in numerous fields like integrated sensors, image processing, speech recognition, hand writing recognition etc. This lead to an increased interest in the evolution process of active elements which are used for analog signal processing.

Communication systems, control systems, instrumentation, measurement, bio-medical, etc. find signal processing applications. There are two different ways to implement signal processing, which are given as:

- Analog or continuous time method and
- Digital or discrete time method.

The analog signal processing was dominant for as long as the solutions were based on the fact that the real world is analog. It uses analog circuit constituents such as diodes, resistors, capacitors, transistors, etc. With the developments like growing influence of digital computer and microprocessor, the digital signal processing started edging its analog counterpart and has become dominant now a days. The analog signal processing is based on the natural ability of the system to solve differential equations that describe a physical system; the solutions thus obtained are in real time. On the other hand, digital signal processing relies on numeric calculations. The method may sometimes not give results in real time. The digital signal processing has some advantages over analog approach; two prominent among them are-

- Flexibility: Various kind of signal processing operation can be done using same hardware; while in the core of analog signal processing, a different hardware has to be designed for each kind of operation.
- Repeatability: A signal processing operation can be repeated again and again and we can get same results, while in analog systems if there is a parameter variation due to change in temperature or supply voltage, the results may change.

Apart from these, digital signal processing has many other advantages also like, better noise immunity than analog signals. They are compact and much cheaper than their analog counterpart. The digital systems also give the encryption facility so that the signals to be transmitted are encrypted and only the intended receiver can decode it. It enables transmission of signals over a long distance and it enables multi-directional transmission simultaneously.

As we see that digital systems and circuits have many advantages, so the designers try to look for digital solutions rather than analog for the problems of VLSI system design. All advantages apart, the analog circuits and systems are still fundamentally necessary in many complex and high performance systems. In reality, all signals in the physical world are continuous in both amplitude and time and hence for conditioning of such signals, before they can be processed by digital signal processing circuits, analog techniques will always be required. Another important reason for the existence of analog signal processing is the bandwidth, which can be some order of magnitudes higher, if the signal is processed in analog circuits than in digital.

1.3 ANALOG DOMAIN

The active filters use active components like amplifiers in their circuit along with other passive elements. Inclusion of active components, like amplifiers, improves the performance of a filter, while the requirement for inductors (inductors are typically expensive and bulky) is also avoided. An amplifier inhibits the load impedance of the succeeding stage from upsetting the characteristics of the filter. The active devices also bring in some limitations to the circuits like finite bandwidth, more power consumption, noise injection into the circuit, etc.

Another type of active filter is a biquadratic or biquad filter. This linear filter implements transfer function in the ratio of two quadratic equations. Biquad filters are active filters that are implemented using a single-amplifier biquad (SAB) or multiple amplifier topologies.

1.4 REPORT ORGANIZATION

CHAPTER 2: The literature review shows the history and configurations of current conveyors. It also details internal characteristics and application of different models. Differential Difference Amplifier (DDA) an important block which along with current conveyor constitute the Differential Difference Current Conveyor and hence combining the advantages of the two. The block diagram along with the circuit characteristics is described.

CHAPTER 3: It describes the DDCC the versatile block which has many applications and is the focus of this report. The internal structure is described. The block diagram and the block characteristics are also described.

CHAPTER 4: Implementation of full wave rectifier using DDCC. The DDCC has an advantage of zero cut-in voltage as against a diode used in rectifiers.

CHAPTER 5: Biquad filters are implemented using DDCC. LPF and HPF are implemented with various cut-off frequency but maintaining the same Q-factor. Filters with Q-magnification is also shown with its advantage over a current conveyor implementation.

CHAPTER 6: Two types of all-pass filters one with grounded resistor and the other with grounded capacitor is implemented

CHAPTER 7: Conclusion and future scope.

CHAPTER 2
LITERATURE REVIEW

Extensive literature survey shows that a lot of work has been done on analog signal processing using the voltage as a signal variable. Non-linear circuits using CMOS voltage mode circuit such as squarer, multiplier, log multiplier has been implemented enjoying the advantages of low power dissipation, voltage swing and applications in telecommunication, multimedia, signal processing etc. But with the increasing demand for high speed circuits operating in high frequency region, and the finite gain-bandwidth product associated with operational amplifiers, a different approach is required to be used. CMOS technology, using the current-mode circuits can achieve a considerable improvement in speed, accuracy and bandwidth, overcoming the finite gain–bandwidth product associated with operational amplifiers. Literature survey reveals the emergence of current-mode technology as an alternate approach.

2.1 CURRENT MIRROR

A current mirror is a circuit designed to copy a current through one active device by controlling the current in another active device of a circuit, keeping the output current constant regardless of loading. The current being 'copied' can be, and sometimes is, a varying signal current. Conceptually, an ideal current mirror is simply an ideal current amplifier. The current mirror is used to provide bias currents and active loads to circuits.

In the past two decades, due to the greater emphasis on current-mode circuits current sources are playing an important role to design the IC amplifier. The current mirrors are used to design current sources along with several other active building blocks as discussed in [5]. A basic BJT based NPN current mirror is shown in fig. 2.1 where $R_0 = r_{02}$ (output resistance of Q2). For the analysis, it is assumed that both the transistors in this circuit are identical and the Early effect is neglected. The input current of the circuit is I_{REF} and output current is I_0. the relation between input and output current is given as:

$$I_0 = \frac{I_{REF}}{1+{}^{2}/_{\beta}} \qquad (2.1)$$

From the equation above, I_0 and I_{REF} become equal only when $\beta \rightarrow \infty$.

Two performance parameters are there to determine the performance of the current mirror circuits, they are listed below:

- Accuracy of the current transfer ratio of the mirror circuit
- Output resistance of the current source

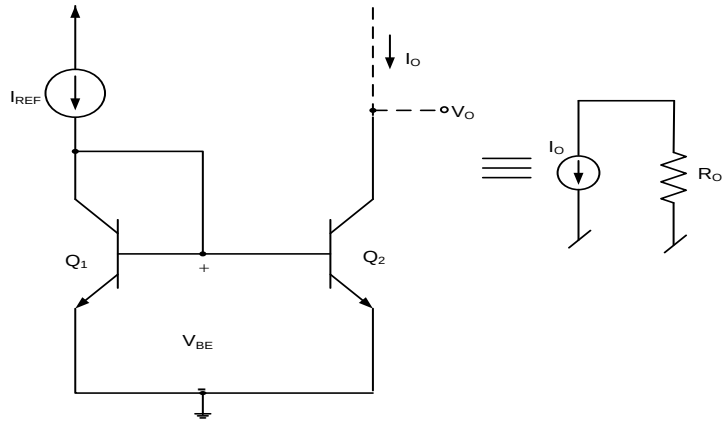

Fig. 2.1 The basic BJT current mirror [6]

2.1.1 BASE CURRENT COMPENSATED CURRENT MIRROR

The basic current mirror circuit shown in fig.2.1 faces some problems and the main problem is that the base current is finite. By adding current gain to the reference transistor Q_1, the base current error can be minimized. The base current compensated current mirror configuration is shown in fig.2.2. In this configuration, the base current of transistor Q_3 is equal to the difference of I_{ref} and I_{C1}. The R_0 of this configuration is same as in the basic current mirror which is r_{02} (output resistance of transistor Q_2).

For large values of beta, the base current term can be neglected. So the output current is defined as:

$$\frac{I_2}{I_{ref}} = \frac{1}{1+\frac{2}{(\beta^2+\beta)}} \approx \frac{1}{1+\frac{2}{\beta^2}} \qquad (2.2)$$

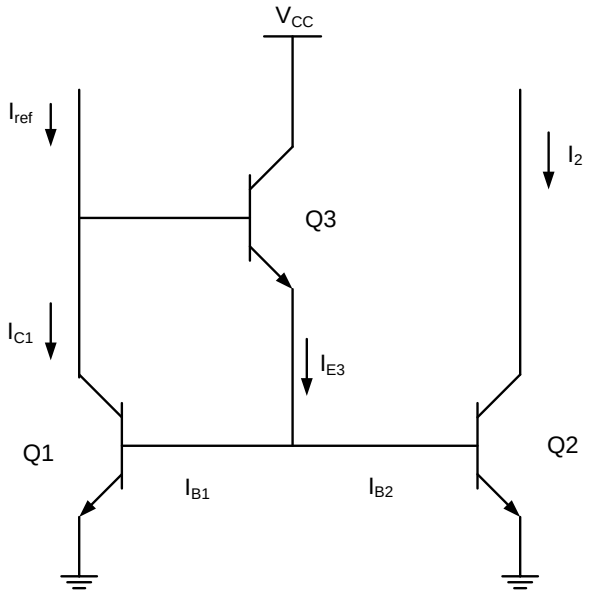

Fig.2.2 Base current compensated current mirror [6]

2.1.2 THE WILSON CURRENT MIRROR

The circuit of Wilson Current Mirror is shown in fig.2.3. In the analysis it is assumed that the transistors have identical parameters and the Early effect is neglected. The relation between input and output currents are defined as:

$$\frac{I_0}{I_{REF}} = \frac{1}{1+\frac{2}{\beta(\beta+2)}} \qquad (2.3)$$

If β becomes much high then the input current (I_{REF}) will be equal to output current (I_0). The advantage of Wilson Current Mirror over the basic current mirror is that it has high output resistance ($\approx \beta r_{02}/2$).

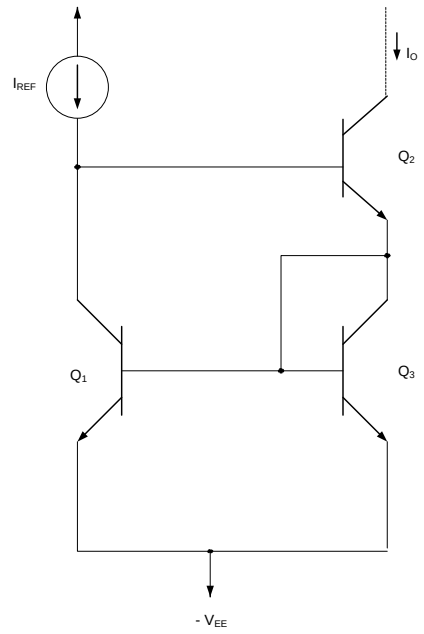

Fig.2.3 Wilson current mirror [6]

2.1.3 GENERATION OF COMPLEMENTARY CURRENT OUTPUTS USING CROSS COUPLED CURRENT MIRRORS

In analog circuit design, various active blocks are designed using cross coupled current mirror which is shown in fig. 2.4. The attractive feature of this configuration is that it gives

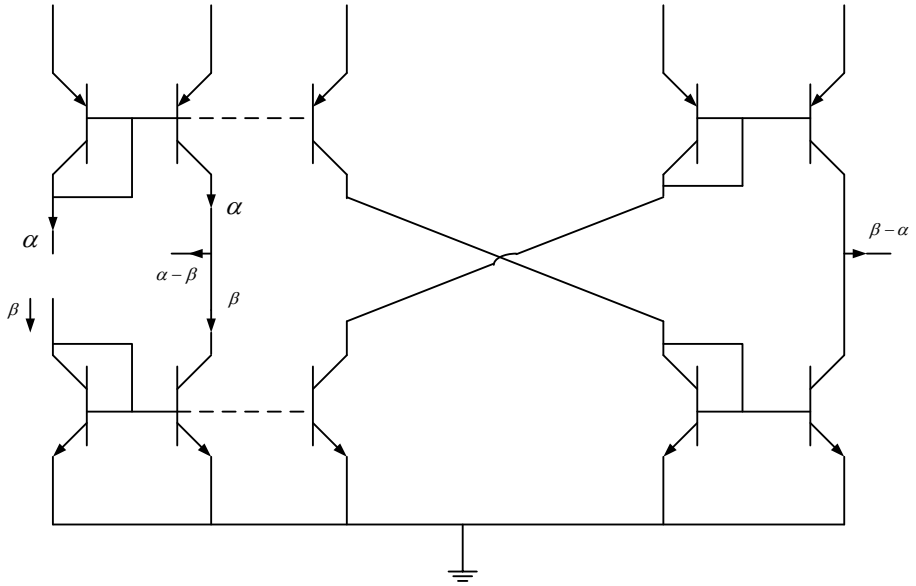

Fig. 2.4 Complementary current output using cross coupled current mirror

complementary outputs. This configuration is used in second generation current conveyors.

2.2 CURRENT CONVEYORS

This chapter details about the development of current conveyors, its types and structures then and now and modes of operation.

Current conveyors [1] are unity gain analog building block having high linearity, wide dynamic range and provide higher gain-bandwidth product. The current conveyors operate at low voltage supplies and consume less power. It has high input impedance, low output impedance and unity current gain (Iz/Ix=±1) as well as unity voltage gain (Vx/Vy=1). The working principle of Current Conveyors is very simple. The current conveyors can easily be implemented using voltage follower and current mirrors. The main features of these current conveyors are low voltage, less power, high slew rate and wide bandwidth for voltage transfer (Vy to Vx) and current transfer (Ix to Iz) which make them suitable for high frequency and low power applications.

2.3 CMOS CURRENT CONVEYORS

The current conveyors which can operate in both voltage and current modes are desired by many designers today because of its simple architecture and features that it possesses.

Current conveyor of the first generation was published in 1968 by K. C. Smith and A. S. Sedra [1]. In 1970 today's widely used second-generation current conveyor was described in [7], and in 1995 the third-generation current conveyor [8]. It has a simple architecture, larger bandwidth, operates at lower voltages and excellent for current mode operation.

Today current conveyors are used in variety of applications ranging from multifunction and universal filters [1,20,12], Variable current gain circuits [21], oscillators and immittance design to integrators and differentiators.

The three current conveyors namely the first generation, second generation and the third generation have similar structure but vary by their characteristics. Shown below is the block diagram of the current conveyor.

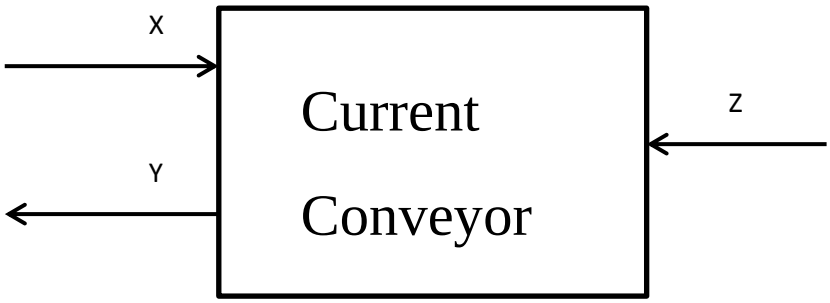

Fig. 2.5 Current Conveyor

- Port X works as a hybrid port functioning as input port for current signals and output port for voltage signals at the same time.
- Port Y is a voltage input port.
- Port Z is a current output port, which can either sink or source current equal to the current injected into port X.

When a voltage source is applied to port Y, then the same potential will appear on the port X. Now when a current is forced at port X the same current is also conveyed to output port Z, which is at a high impedance level.

In general the following actions are ensured for a current conveyor:-

- Voltage transfer at the X and Y ports
- Current transfer at the X and Z ports

For an ideal current conveyor the port X should have lowest impedance as it acts a voltage output and current input terminal. On the other hand port Z should have highest impedance as it acts as a current output port. The current from port X is copied to port Z by current mirror. While the voltage from port Y is copied to port X by a voltage follower. These should work with minimum offset for the close to ideal performance of the current conveyor.

2.3.1 FIRST GENERATION CURRENT CONVEYOR (CCI)

It was proposed by Sedra and Smith in 1968. Denoted by CCI± it consists of three terminals X,Y and Z. the polarity of the current flowing in port Z specifies whether it is the same as the current input at X or opposite to it. The block diagram of the CCI± is shown below.

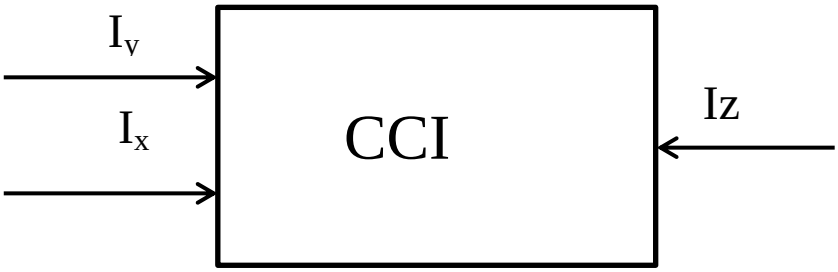

Fig. 2.6 First generation current conveyor

The following matrix gives the input output relation of the current conveyor first generation in the matrix form.

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix} \tag{2.4}$$

The current flowing in port Y is equal to the current flowing in port X i.e. it is copied and is independent of any voltage applied at port Y.

The voltage at port X is equal to the voltage at port Y and is independent of any current applied at port X.

The current at port Z is equal to the current at port X if current at Z flows in the same direction as that of X or else it is taken with opposite polarity.

The impedance level of different ports are given in the table below.

CCI PORTS	IMPEDANCE LEVEL
X	Low (ideally zero)
Y	Low (ideally zero)
Z	High (ideally infinite)

Table 2.1 Impedance level at ports of CCI

The application of CCI± becomes difficult because both the ports X and Y have zero input impedance in order to sink currents.

2.3.1.1 IMPLEMENTATION OF CCI+

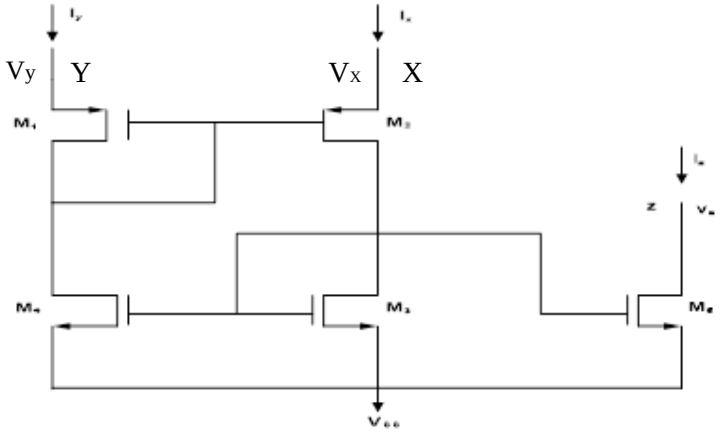

Fig 2.7 Implementation of CCI+ [25]

Here when a voltage is applied at Y the same appears at X and hence there is a voltage following action. Also when a current is applied at X the same current appears at Y and it also appears at Z, hence the current from X is mirrored at Y and Z.

2.3.1.2 APPLICATIONS OF CCI

The first generation current conveyor, CCI is a basic building block can be used for variety of applications. Some of the applications of CCI+ is given below:

- It is used as a current amplifier because of the low impedance at the input terminal.
- The voltage at the Y-terminal can set the DC-voltage level at the current input port X to a desired value and input voltage-to-current conversion is easier than in the case of a current-mirror.

2.3.2 SECOND GENERATION CURRENT CONVEYOR (CCII)

The second generation current conveyor (CCII) is one of the most versatile current-mode building block. For many applications, a high impedance input port is preferable in order to avoid loading effect. So, second generation current conveyor was developed to fulfil this requirement. It has one high and one low impedance input port rather than the two low impedance input ports of CCI. The terminal Y of the device is a high impedance port as no current flows through it. The block diagram of the CCII is shown below:-

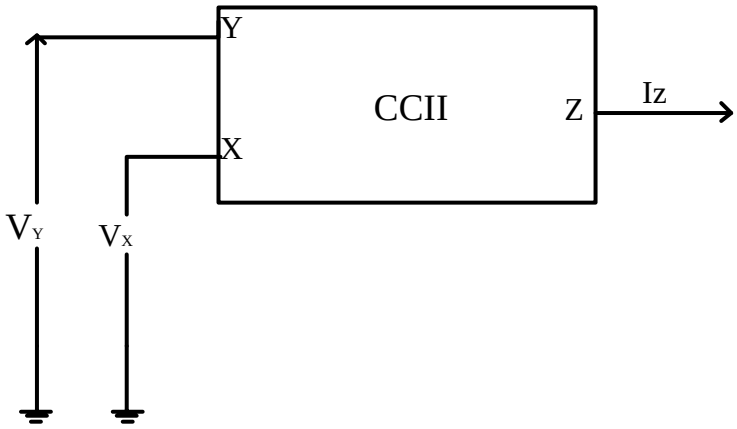

Fig 2.8 Second generation current conveyor

The following matrix relation gives the input output relation of the block:-

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \qquad (2.5)$$

Unlike the first generation current conveyor no current flows in terminal Y while only voltage can be inputted at Y. Terminal X is a voltage output and current input terminal and terminal Z is a current output terminal. Thus Z is a high impedance terminal.

The two types of second generation current conveyors are:-

(i) **Positive current conveyor: -** In this the current flowing out of the Z port will be in the same polarity as of the current inputted at the X port.

(ii) **Negative current conveyor: -** In this the current flowing out of the Z port will be in the opposite polarity to the current inputted to the X port.

The circuit diagram of CCII is shown below:-

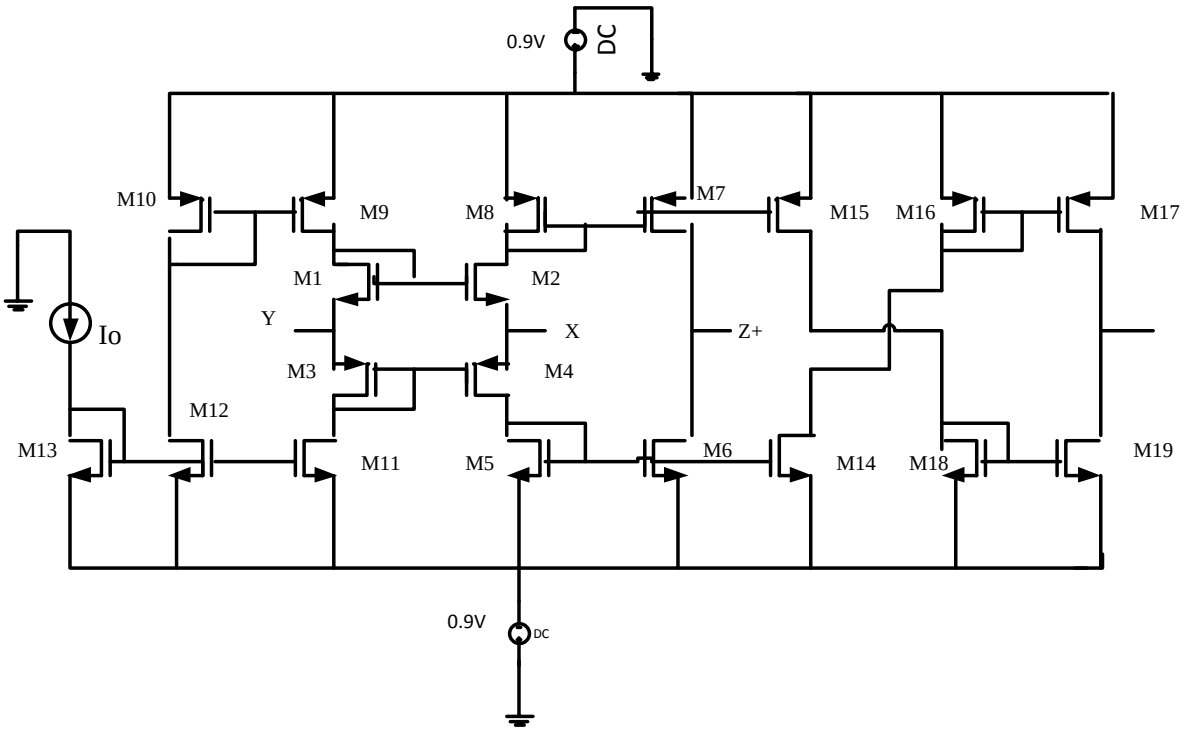

Fig 2.9 Second Generation Current Conveyor Circuit [26,27]

The impedance level of various ports are shown in the table below:-

CCII	Ports Impedance Level
X	Low (ideally zero)
Y	High (ideally infinite)
Z	High (ideally infinite)

Table 2.2 Impedance level at ports of CCII

2.3.2.1 APPLICATION OF CCII

Many active elements have been developed by second generation current conveyor and have found many applications

(i) Filters

(ii) Variable current gain

(iii) Current amplifier

(iv) Current follower

(v) Voltage follower

2.3.3 THIRD GENERATION CURRENT CONVEYOR (CCIII)

It is a unity gain current controlled current source device. High performance current mirrors are required in the CMOS structure realization of CCIII in order to provide the good dynamic swing and high output resistance which enables cascadability [8].

The main features of the CCIII are:

- Low gain errors (high accuracy)
- High linearity
- Wide frequency response

The CCIII is a 3 terminal device and the relation between them can be given by the following matrix relation.

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \qquad (2.6)$$

The properties of CCIII are the same as that of CCII with the only difference that the current in port Y will be opposite the polarity of the current applied at port X. This property enables the device to be used as integrated floating current sensing device.

The circuit diagram of the CCIII is shown below:-

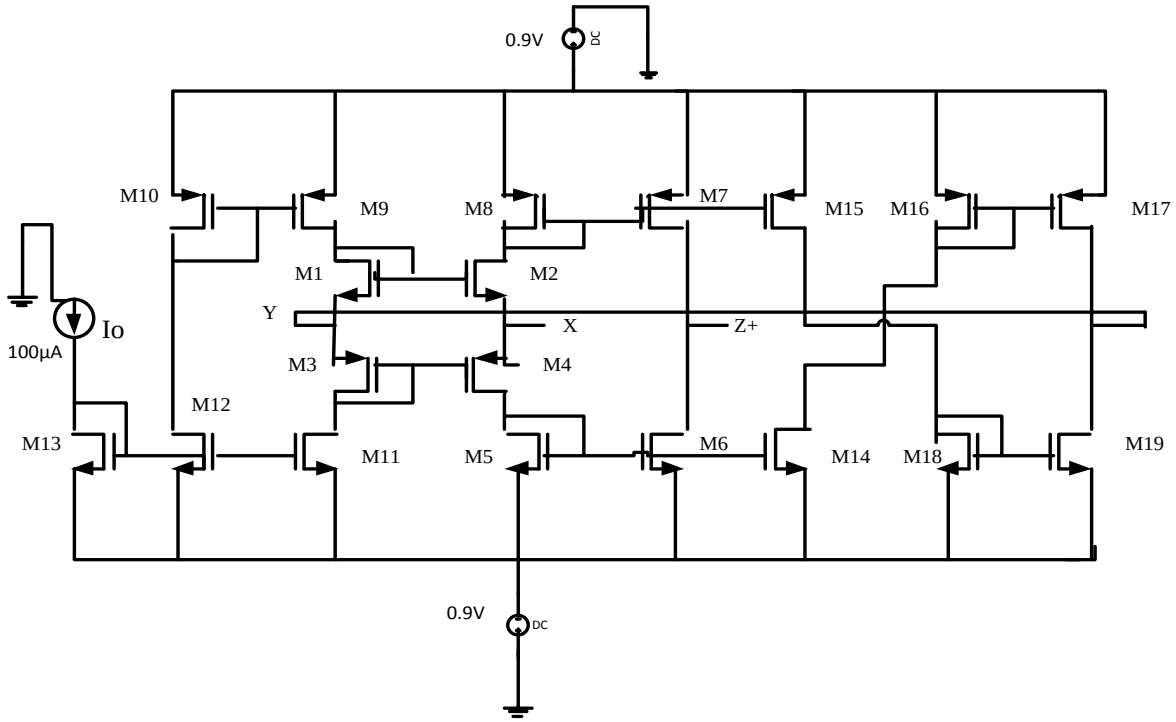

Fig 2.10 Third Generation Current Conveyor [8, 27]

2.4 DIFFERENTIAL DIFFERENCE AMPLIFIER

The op-amp with a negative feedback adjusts the difference in input to a negligible value. For ideal op-amp the gain is infinity and therefore the differential input will be zero.

The op-amp compares two single ended inputs while the Differential Difference Amplifier [3] compares two differential input voltage signals.

2.4.1 SYMBOL OF DDA

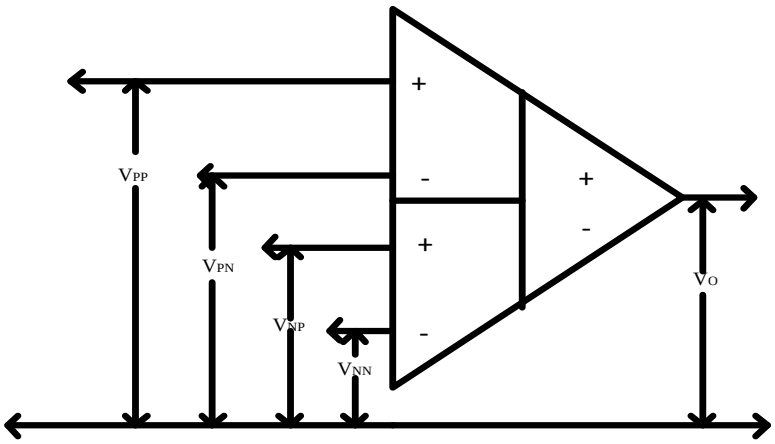

Fig 2.11 Block diagram of DDA [3]

Therefore with negative feedback the property of the DDA can be defined as:-

$$V_{PP}\text{-}V_{PN}=V_{NP}\text{-}V_{NN} \qquad (2.7)$$

But it is not possible to implement a DDA using three op-amps predominantly because of two reasons:-

- Op-amp cannot handle large differential voltage and therefore will be overdriven.
- Gains of first two op-amps should exactly match.

2.4.2 CHARACTERISTICS OF THE DDA

The following matrix shows the characteristics of the DDA

$$\begin{bmatrix} V_D \\ V_{CP} \\ V_{CN} \\ V_{CD} \end{bmatrix} = \begin{bmatrix} 1 & -1 & -1 & 1 \\ 1/2 & 1/2 & 0 & 0 \\ 0 & 0 & 1/2 & 1/2 \\ 1/2 & -1/2 & 1/2 & -1/2 \end{bmatrix} \begin{bmatrix} V_{PP} \\ V_{PN} \\ V_{NP} \\ V_{NN} \end{bmatrix} \qquad (2.8)$$

The circuit diagram of the DDA is shown below.

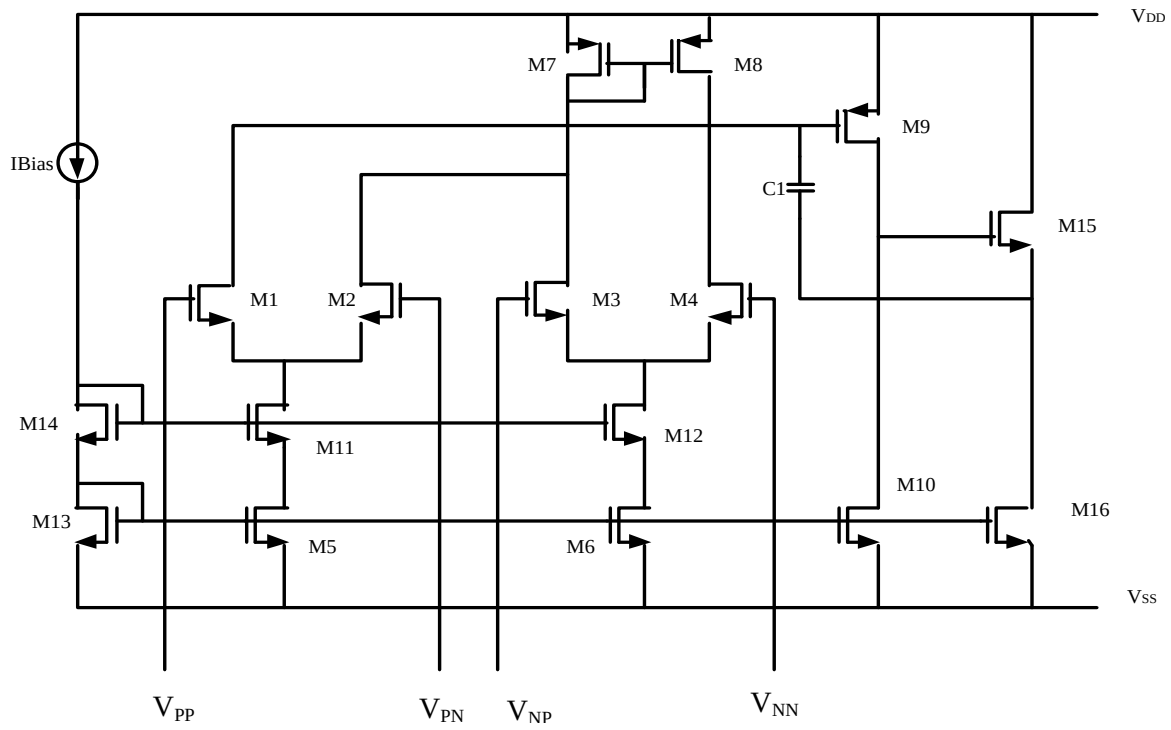

Fig 2.12 Circuit diagram of DDA [3]

CHAPTER 3
DIFFERENTIAL DIFFERENCE CURRENT CONVEYORS

3.1 INTRODUCTION

Wide frequency operation, high accuracy and wide range of applicability are always desired. Differential Difference Current Conveyor [2] combines the effectiveness of two active blocks namely the Current Conveyor [7] and Differential Difference Amplifier [3].

3.2 CIRCUIT DESCRIPTION

The block diagram of DDCC is shown below:-

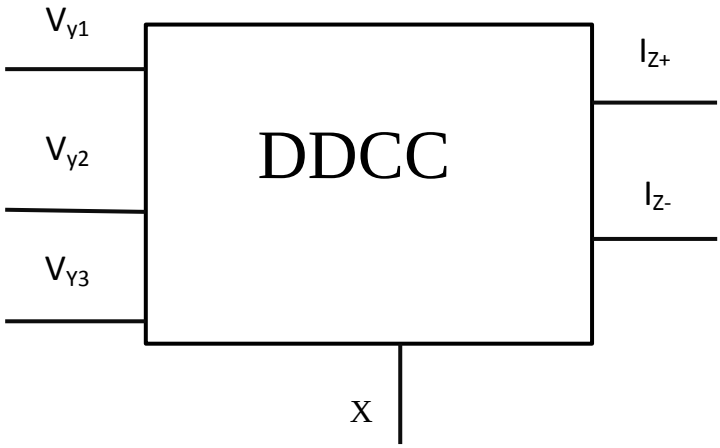

Fig 3.1 Block diagram of DDCC

The terminal characteristics are described by:-

$$V_x=V_{y1}-V_{y2}+V_{y3} \quad (3.1)$$

$$I_{z+} = I_x \text{ and } I_{z-} = -I_x \quad (3.2)$$

The transient proofs of which are given below respectively in fig 3.2 and fig 3.3

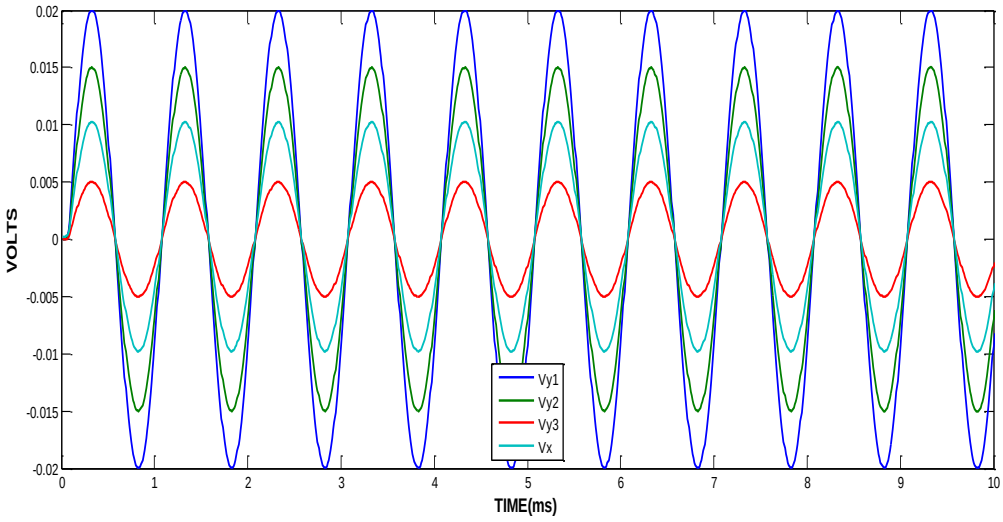

Fig 3.2 Voltage property

Where $V_x=V_{y1}-V_{y2}+V_{y3}$ (V_{y1}=20mV, V_{y2}=15mV, V_{y3}=5mV), all 1kHz

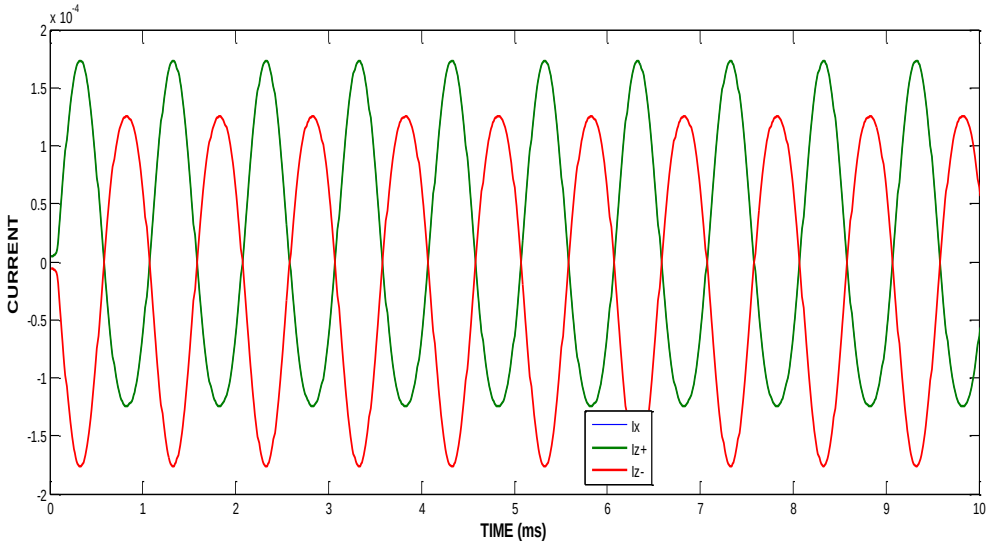

Fig 3.3 Current Property

Where $I_z=I_x$ (V_{y1}=5mV, V_{y2}=5mV, V_{y3}=5mV), all 1kHz

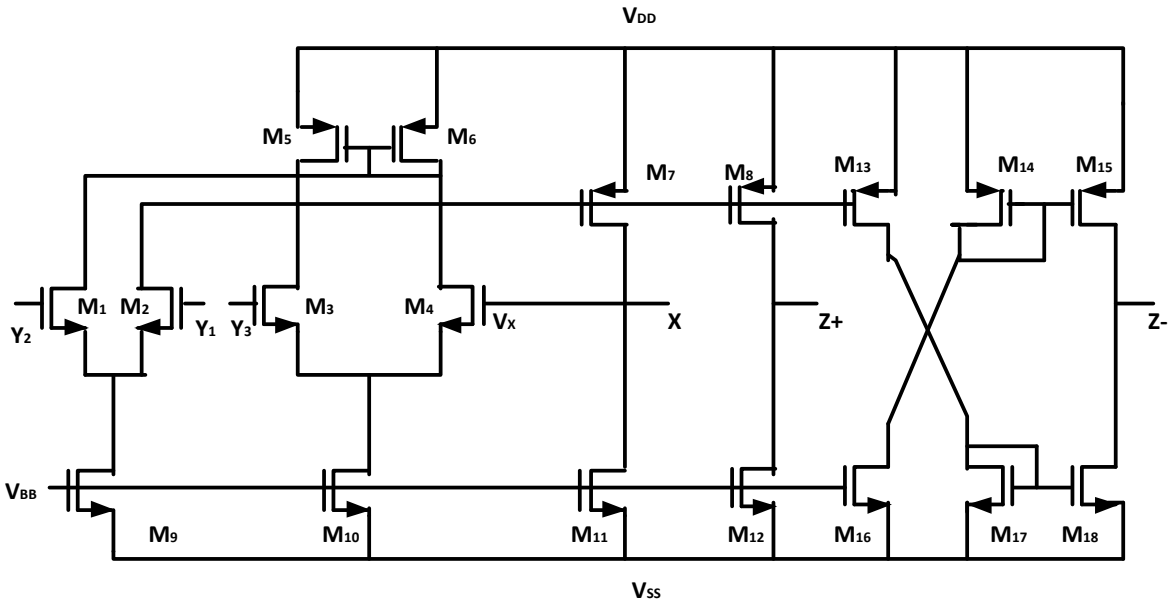

Fig 3.4 Circuit diagram of DDCC [2]

The trans-conductance elements with differential stages are transistors M1, M2 and M3, M4. The current mirror formed by transistors M5 and M6 converts the differential current to single ended current output M7

The output voltage equation is

$$V_X = A_o[(V_{Y1}-V_{Y2})- (V_X- V_{Y3})] \quad (3.3)$$

Where Ao is the open loop gain. A negative feedback from X to gate of M_4 is also provided. If the open loop gain A_o is made very much greater than unity then the voltage at X is modified as:-

$$V_x= \frac{Ao}{Ao+1}(V_{Y1}-V_{Y2}+ V_{Y3}) \approx (V_{Yl} - V_{Y2}+ V_{Y3}) \quad (3.4)$$

3.3 ADVANTAGE AND APPLICATION

Clubbed with the advantage of DDA and CC the DDCC has wide bandwidth, greater linearity, high slew rate, wide dynamic range, simple circuitry, low power consumption and arithmetic operation capability.

As DDCC combines the effectiveness of two active blocks it finds wide appreciation and is used for various purposes. Some of which are filters, squarer [2], rectifiers etc.

CHAPTER 4
DDCC AS A RECTIFIER

4.1 INTRODUCTION

All of the digital devices run on DC voltages and power supply finds wide applications. The rectifier circuitry conventionally constructed using diodes is made using DDCC having zero cut-in voltage [9]. For the positive half cycle of the input DDCC1 conducts and for the negative half cycle of the input DDCC2 conducts.

4.2 CIRCUIT DIAGRAM

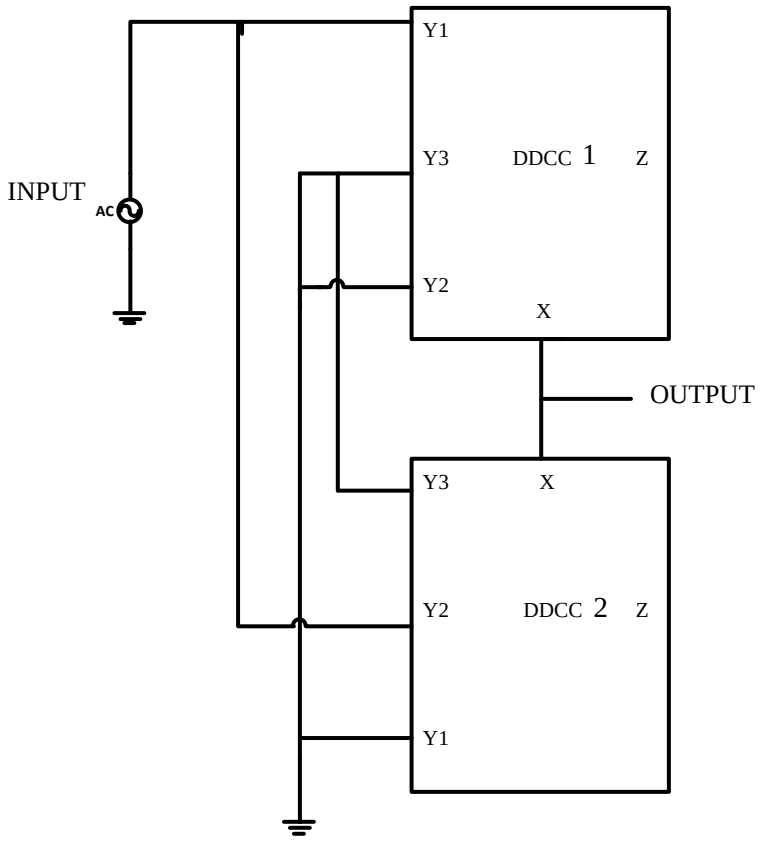

Fig 4.1 Block diagram of Full Wave Rectifier [9]

Here the output voltage equation $V_x=V_{y1}-V_{y2}+V_{y3}$ is used for the formation of pulsating DC output. Two DDCC circuits are used with their X terminal interconnected. The input is connected to the terminal Y1 of the first DDCC and to the terminal Y2 of the second DDCC. While inputs Y2 and Y3 of the first DDCC and Y1 and Y3 of the second DDCC are grounded.

During the positive half cycle the first DDCC conducts while the second DDCC is off and the output is as the input applied. During the negative half cycle the first DDCC is turned off and the second DDCC conducts and gives the output as the mod of the input.

$$V_{in} > 0,\ V_{out}=V_{in},\ \text{DDCC1 on and DDCC2 off} \quad (4.1)$$

$$V_{in} < 0,\ V_{out}=-V_{in},\ \text{DDCC1 off and DDCC2 on} \quad (4.2)$$

Therefore

$$V_{out}= |V_{in}| \quad (4.3)$$

4.3 SIMULATIONS

4.3.1 DC CHARACTERISTICS

The DC characteristics of the full wave rectifier part is shown below.

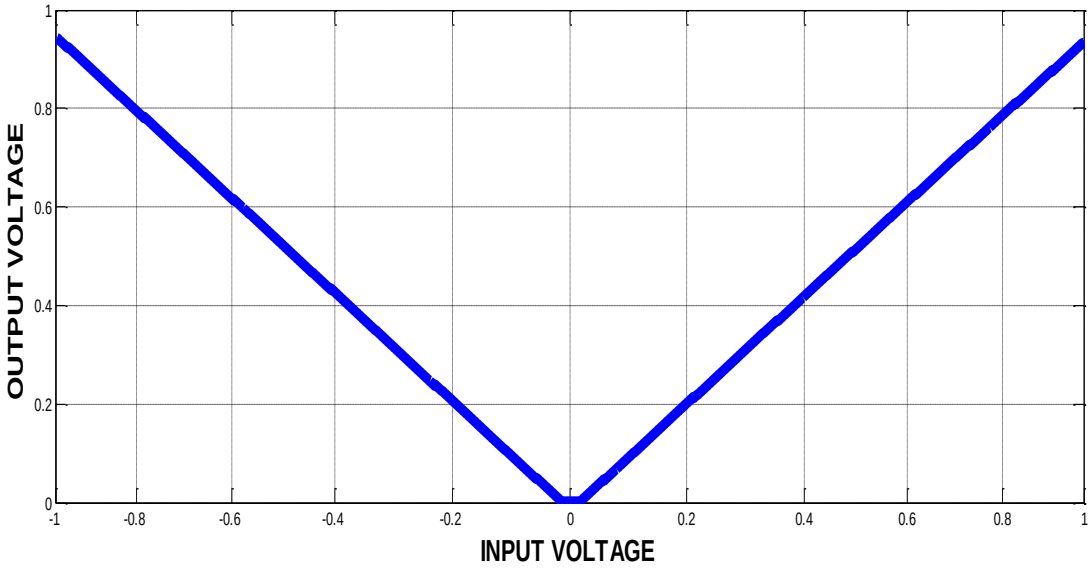

Fig 4.2 DC Characteristics of Full wave rectifier

A varying DC input from -1 to +1 volt was applied and the mod of the input was obtained as output.

4.3.2 FULL WAVE RECTIFIED OUTPUT

The full wave rectified output for various frequencies are shown below:-

(i) Input signal 1kHz at 250mV peak to peak

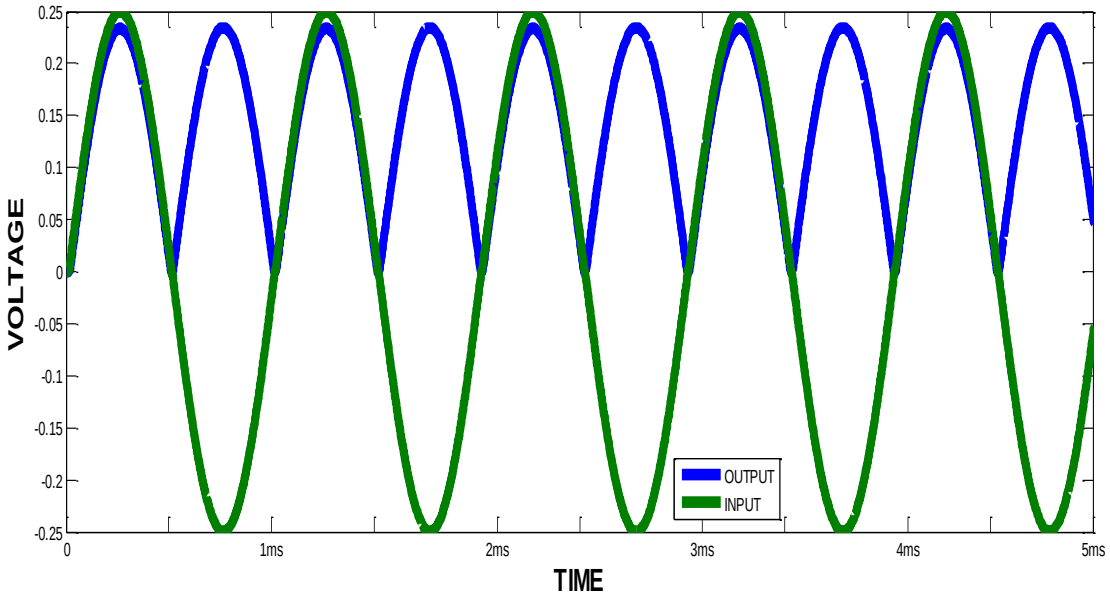

Fig 4.3 Full wave rectified output

(ii) Input signal 1Mhz, at 250mv peak to peak

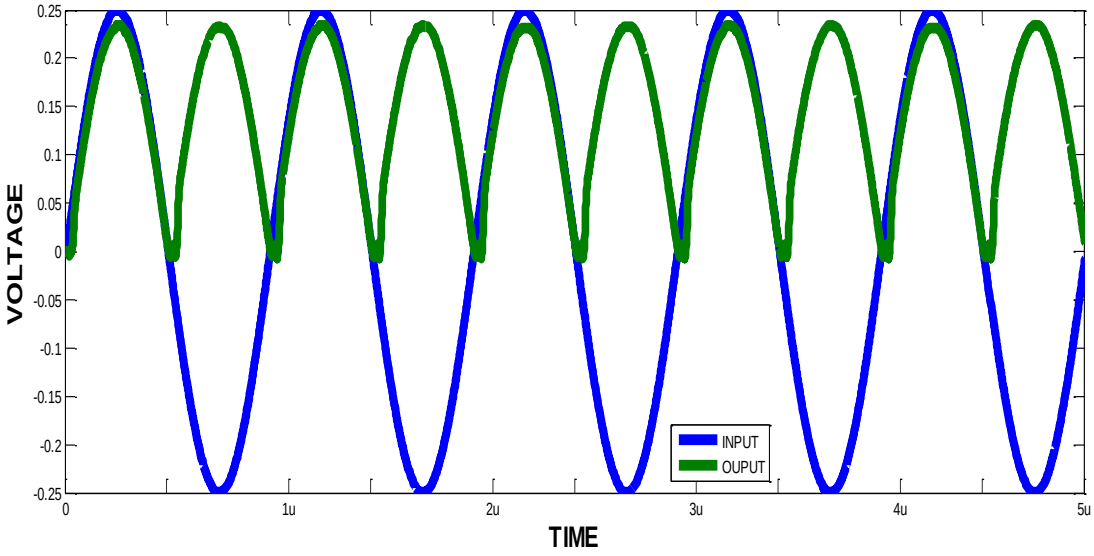

Fig 4.4 Full wave rectified output

Transistor	*W* (*μ*m)	*L* (*μ*m)
M1–M4	1.6	1
M5–M6	8	1
M7–M8	20	1
M9–M10	29	1
M11–M12	90	1
M13–M15	20	1
M16–M18	90	1

Table 4.1 Transistor aspect ratio

The device model parameters used is MIETEC 0.5μm CMOS process. The supply voltages selected are $V_{DD} = -V_{SS} = 2.5V$ and bias voltage is $V_B = -1.7V$.

CHAPTER 5
CONSTRUCTION OF BIQUAD FILTERS USING DDCC

5.1 INTRODUCTION

Biquad filters are of great importance because several such blocks can be connected in cascade without loss and implement higher order filters. Second generation current conveyors regarded as a versatile block has been used widely in various applications notably due to its high bandwidth and high slew rate. They however have the following disadvantages as till 2004:-

(i) Two or more current conveyors are used. [10,11, 22, 23]

(ii) They need many passive elements [10,12, 24]

Therefore the biquads formed here [13] use only one DDCC as the active element and minimum passive elements. The low pass and high pass filters formed so also can have different cut off frequencies but maintain the same Q-factor. Another circuitry which gives the band pass and low pass response has Q-magnification property.

5.2 LOW PASS FILTER USING DDCC

Shown below is the circuit diagram of the low pass filter designed using DDCC [13]. If Y_1 and Y_3 are resistors and Y_2 and Y_4 are capacitors the circuit operates as a low pass filter.

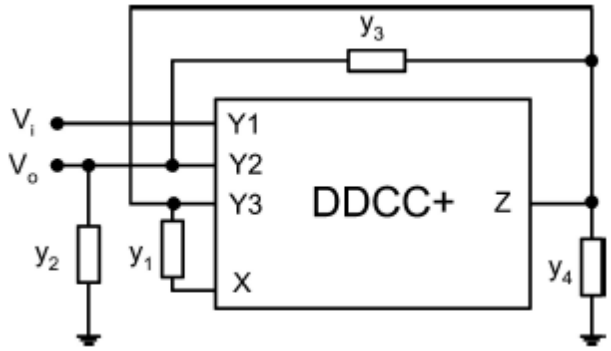

Fig 5.1 Block diagram of LPF using DDCC [13]

The transfer function obtained is:-

$$\frac{V_o}{V_i} = \frac{\frac{1}{R_1 R_3 C_2 C_4}}{s^2 + \frac{C_2 + C_4}{R_3 C_2 C_4} s + \frac{1}{R_1 R_3 C_2 C_4}} \qquad (5.1)$$

The natural frequency ω_o and quality factor Q can be expressed as:-

$$\omega_o = \sqrt{\frac{1}{R_1 R_3 C_2 C_4}} \qquad \text{and} \quad Q = \sqrt{\frac{R_3}{R_1}} \frac{\sqrt{C_2}\sqrt{C_4}}{(C_2 + C_4)} \qquad (5.2)$$

Therefore the natural frequency can be changed by varying R_3 and R_1 keeping the ratio constant; thus keeping Q same.

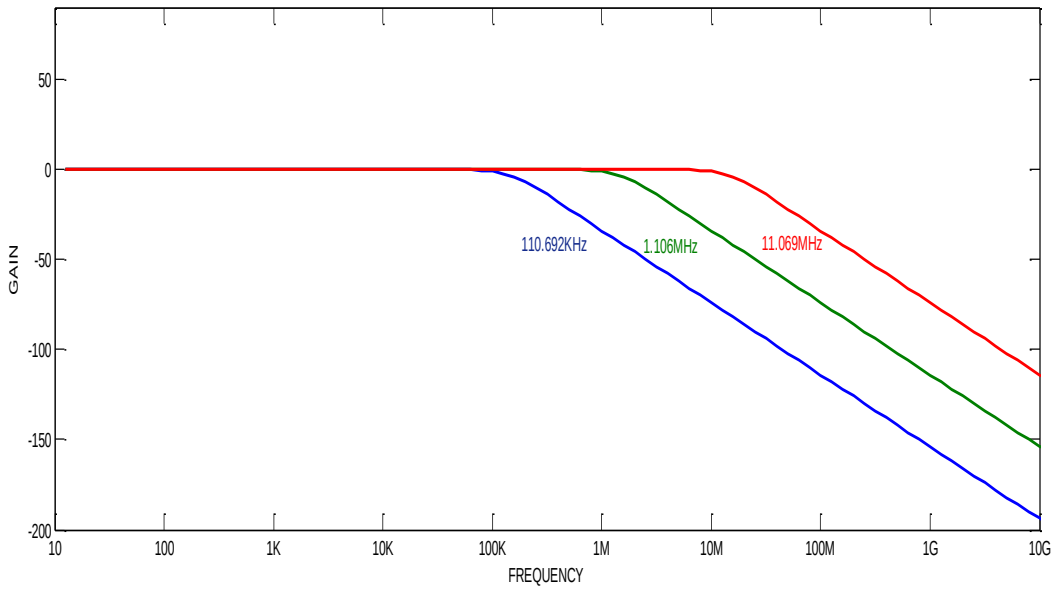

Fig 5.2 Frequency responses of LPF

The above graph shows various natural frequencies with the same Q. As the resistance increases the cut off frequency decreases as apparent from the equation of natural frequency.

R_1 and R_3	ω_o
10k	11.069MHz
100k	1.106MHz
1000k	110.692kHz

Table 5.1 The variation in natural frequency

5.2.1 TRANSIENT ANALYSIS

Input frequency=100 kHz

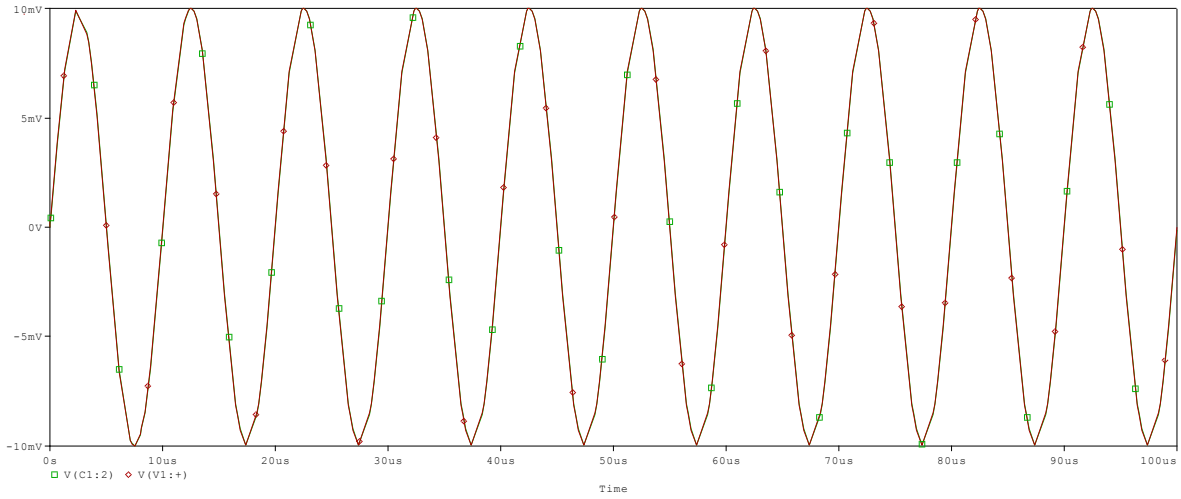

Fig 5.3 Low frequency response of LPF

Input frequency=20MHz

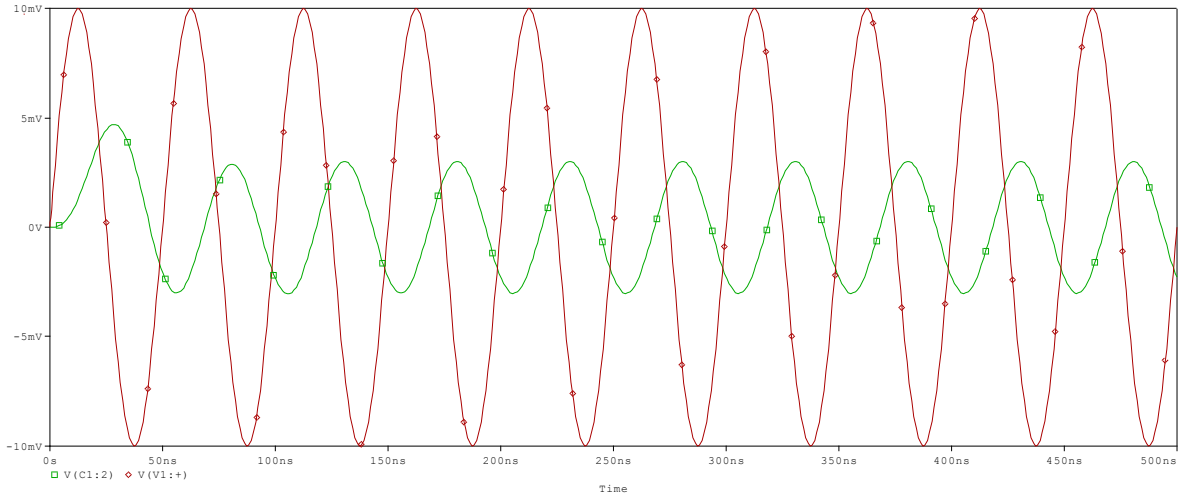

Fig 5.4 Frequency response just over the cut-off

5.3 HIGH PASS FILTER USING DDCC

Shown below is the circuit diagram of the high pass filter designed using DDCC [13]. If Y_1 and Y_3 are capacitors and Y_2 and Y_4 are resistors the circuit operates as a high pass filter.

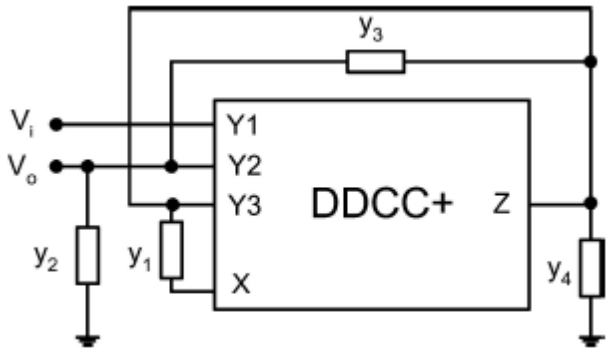

Fig 5.5 Block diagram of HPF using DDCC [13]

The transfer function is obtained as:-

$$\frac{V_o}{V_i} = \frac{s^2}{s^2+\frac{R_2+R_4}{2R_2R_4C_1}s+\frac{1}{R_2R_4C_1C_3}} \tag{5.3}$$

The natural frequency ω_o and quality factor Q can be expressed as:-

$$\omega_o = \sqrt{\frac{1}{R_2R_4C_1C_3}} \quad Q = \sqrt{\frac{C_1}{C_3}}\frac{\sqrt{R_2}\sqrt{R_4}}{(R_2+R_4)} \tag{5.4}$$

Therefore the natural frequency can be changed by varying C_3 and C_1 keeping the ratio constant; thus keeping Q same.

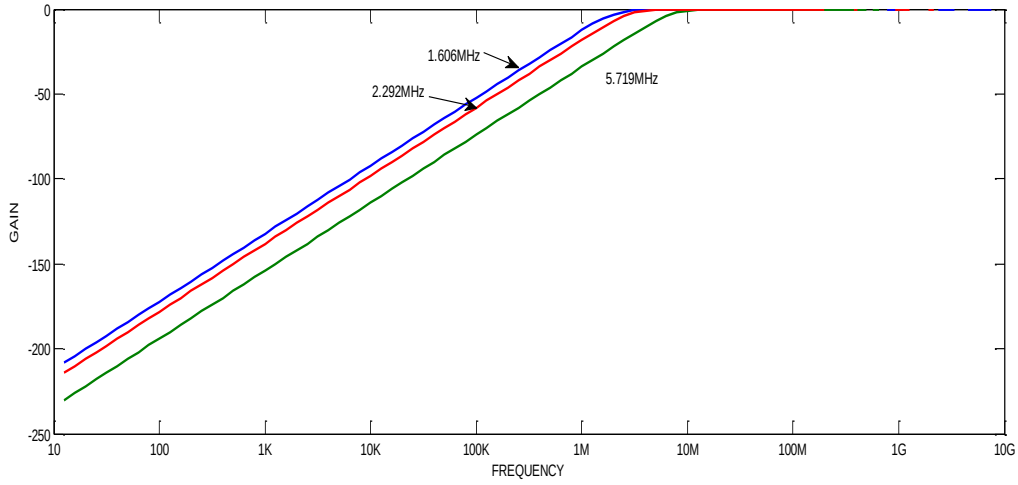

Fig 5.6 Frequency responses of HPF

The above graph shows various natural frequencies with the same Q. As the capacitance increases the cut off frequency decreases as apparent from the equation of natural frequency.

C_1 and C_3	ω_o
2p	5.719MHz
5p	2.292MHz
7p	1.606MHz

Table 5.2 The variation in natural frequency

5.3.1 TRANSIENT ANALYSIS

Input frequency=10MHz

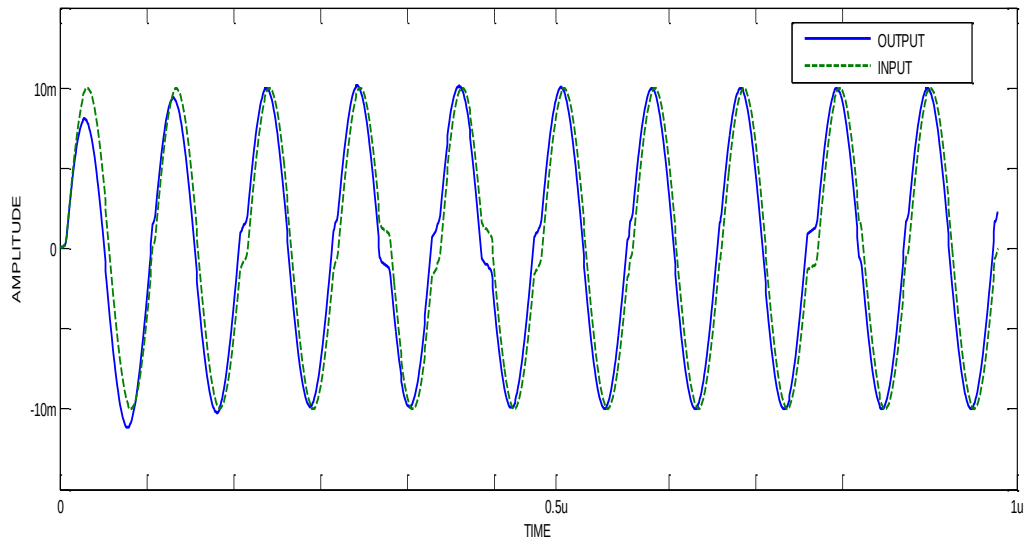

Fig 5.7 Pass band response of HPF

Input frequency=1MHz

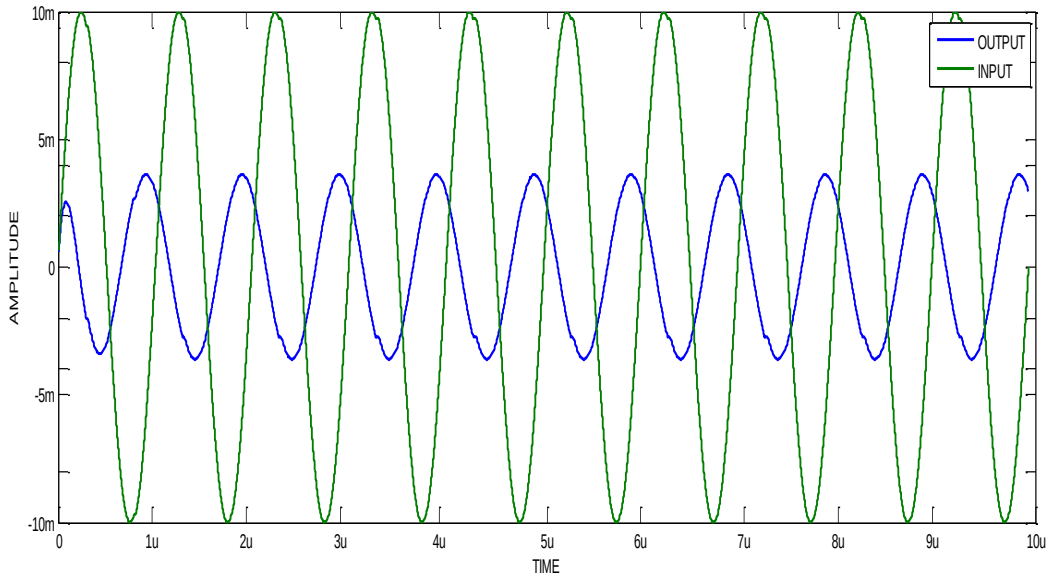

Fig 5.8 Frequency response just below cut-off

5.4 LOW PASS FILTER AND BAND PASS FILTER WITH Q-MAGNIFICATION

The circuit shown below shows low pass filter and band pass filter formed by a CCII- This is an improvement to the circuits proposed in [10,14] that employ one or two CCII with few passive elements that are able to implement low Q filters.

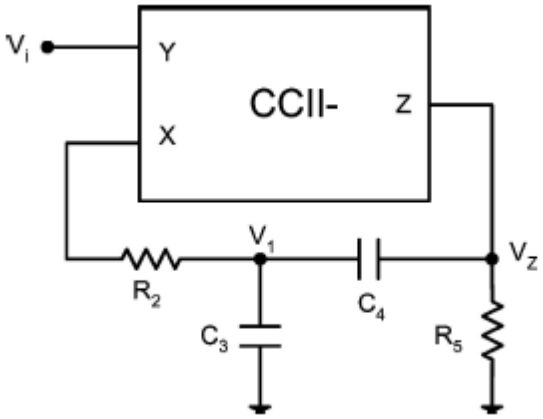

Fig 5.9 Block of LPF and BPF with CCII [14]

Where R_2=5k, R_5=10k, C_3=C_4=2pF

Transfer function

$$\frac{V_{bpf}}{V_i} = \frac{-H_o as}{bs^2+as+1} \qquad (5.5)$$

$$\frac{V_{lpf}}{V_i} = \frac{1}{bs^2+as+1} \quad (5.6)$$

Where $$H_o = \frac{C_3R_5}{R_2(C_3+C_4)} = 1 \quad (5.7)$$

And $a=R_2(C_3+C_4)$, and $b=R_2R_5C_3C_4$ (5.8)

with $$\omega_o = \sqrt{\frac{1}{C_3C_4R_2R_5}}$$ and $$Q = \frac{1}{C_3+C_4}\sqrt{\frac{C_3R_5C_4}{R_2}} \quad (5.9)$$

and ω_o = 11.25MHz, Q=0.707

If the CCII block of the circuit in Fig. 5.9 is replaced by DDCC and resistance R_5 replaced by a potentiometer then a factor K decides the Q-values.

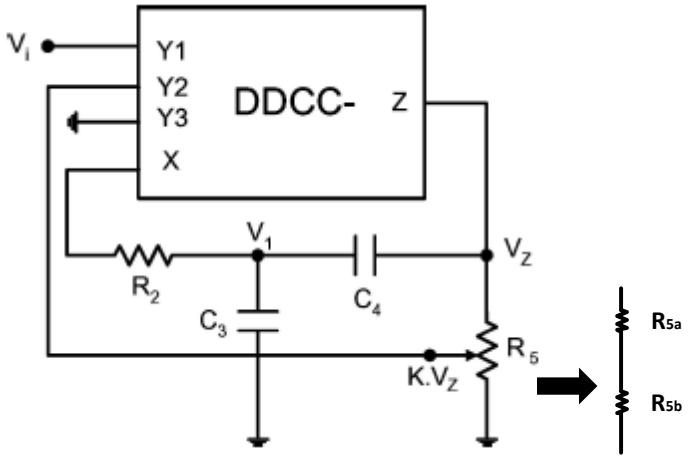

Fig 5.10 Block diagram of LPF and BPF using DDCC [13]

Where R_2=5k, R_5=10k, C_3=C_4=2pF

Transfer function

The circuit yields the following transfer functions:-

$$\frac{V_{bpf}}{V_i} = \frac{-H_o as}{bs^2+a(1-H_oK)s+1} \quad (5.10)$$

$$\frac{V_{lpf}}{V_i} = \frac{1}{bs^2+a(1-H_oK)s+1} \quad (5.11)$$

Where $0 < H_oK < 1$

The centre frequency remains the same for the circuit because R_5 is the same, while the quality factor changes.

$$Q' = \frac{Q}{1-H_oK} \quad (5.12)$$

The value of Q' will be greater than Q when the value of K is greater than 0 as H_o is equal to 1. The value of K varies from 0 to 1. Q' can be attained to a maximum of 10Q.

While the value of H_o will be:-

$$H_o' = \frac{H_o}{(1-H_oK)} \quad (5.13)$$

The frequency response of the low pass filter is shown below:-

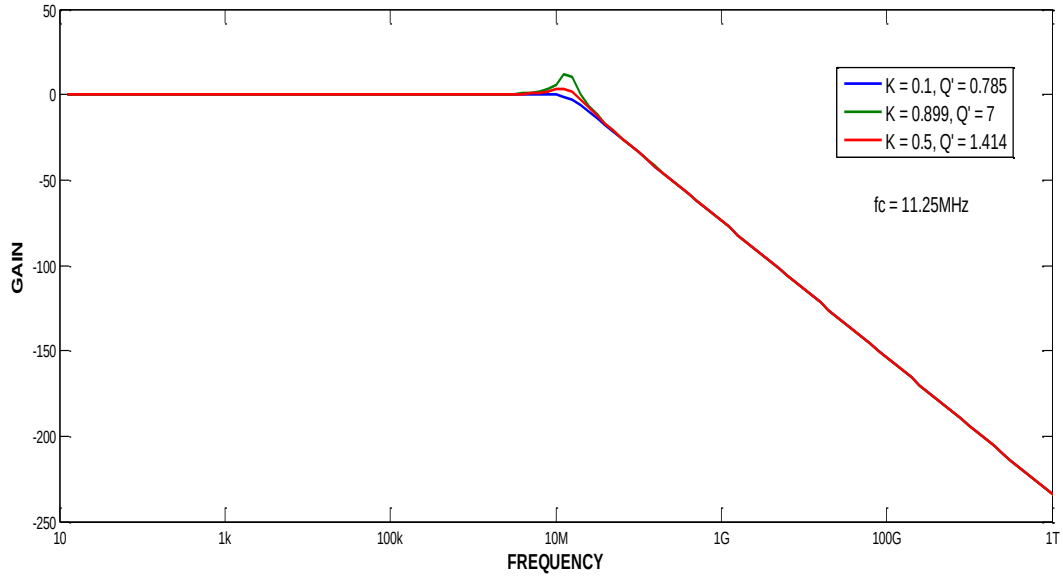

Fig 5.11 Frequency response of LPF with Q-magnification

The transient response of the low pass filter at the cut-off frequency (11.25MHz) with R_{5a}=1k and R_{5b}=9k is shown below:-

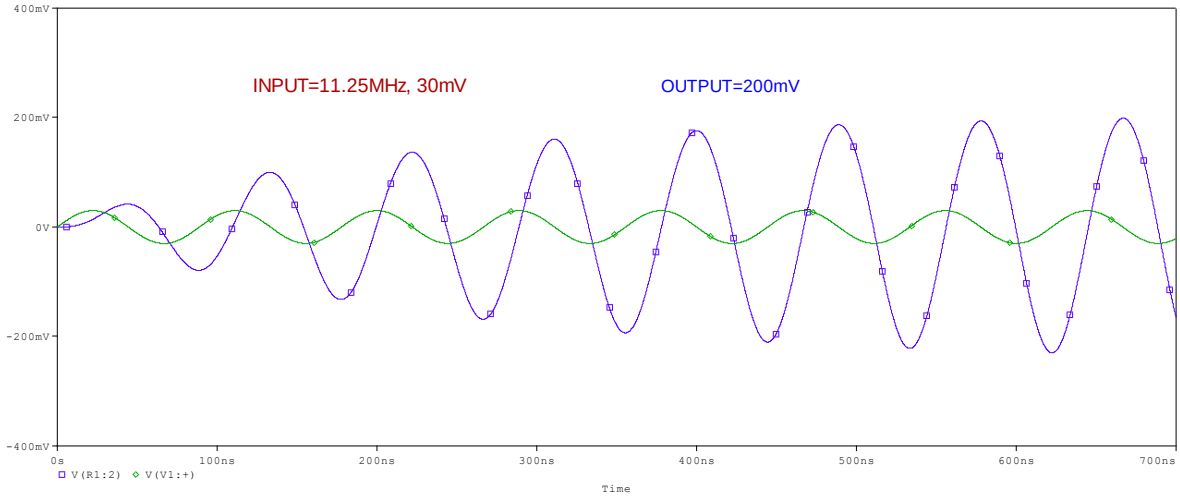

Fig 5.12 Transient analysis at cut-off for LPF

The transient response of the low pass filter at 15MHz with R_{5a}=9k and R_{5b}=1k is shown below:-

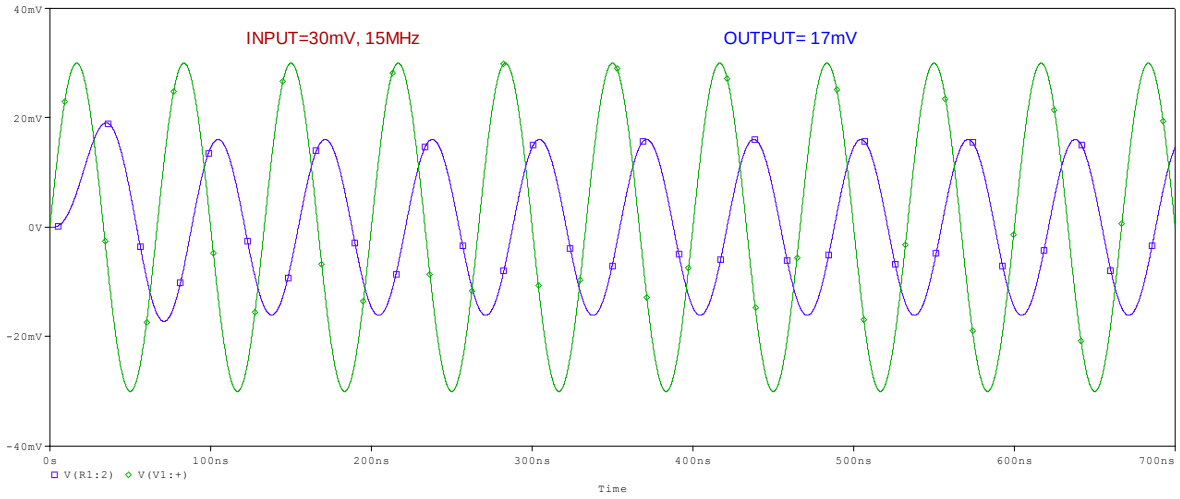

Fig 5.13 Frequency response just above the cut-off

The frequency response of the band pass filter is shown below:-

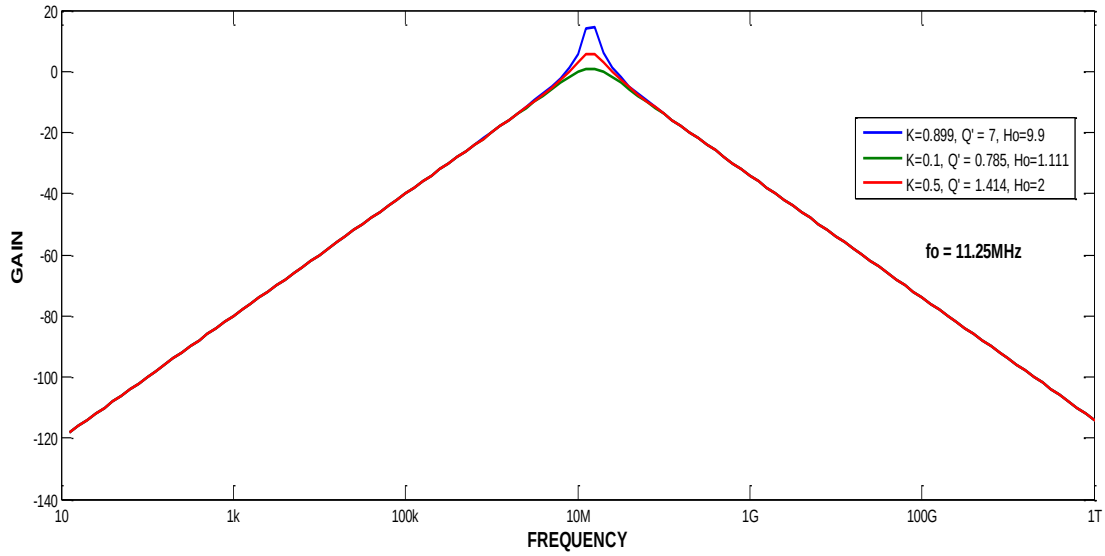

Fig 5.14 Frequency response of the band pass filter with Q-magnification

The transient response of the band pass filter at 11.25MHz with R_{5a}=1k and R_{5b}=9k is shown below:-

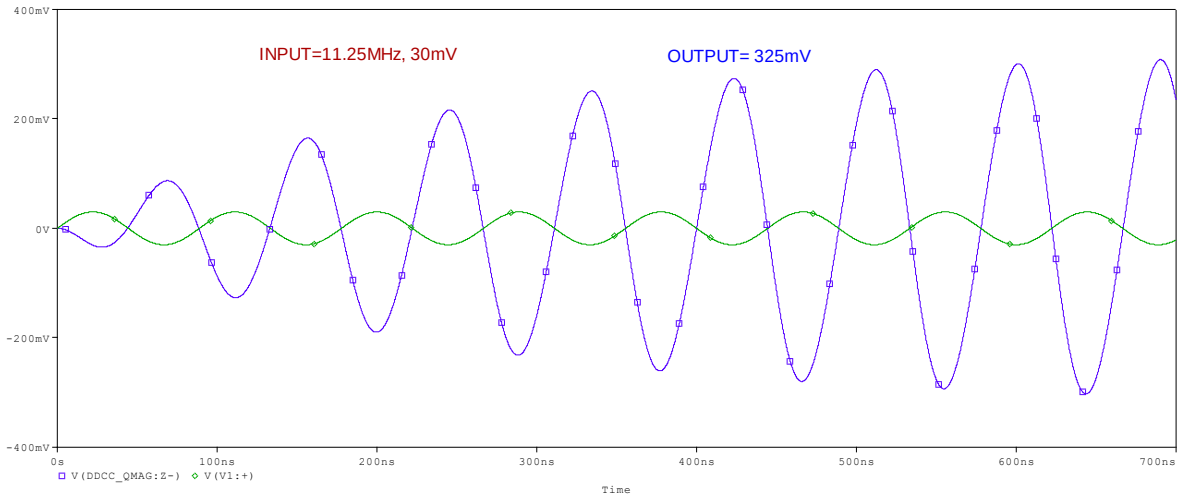

Fig 5.15 Transient response of the band pass filter at 11.25MHz

The phase shift of 180^{o} is apparent from the above graph.

The transient response of the band pass filter at 35MHz with R_{5a}=9k and R_{5b}=1k is shown below:-

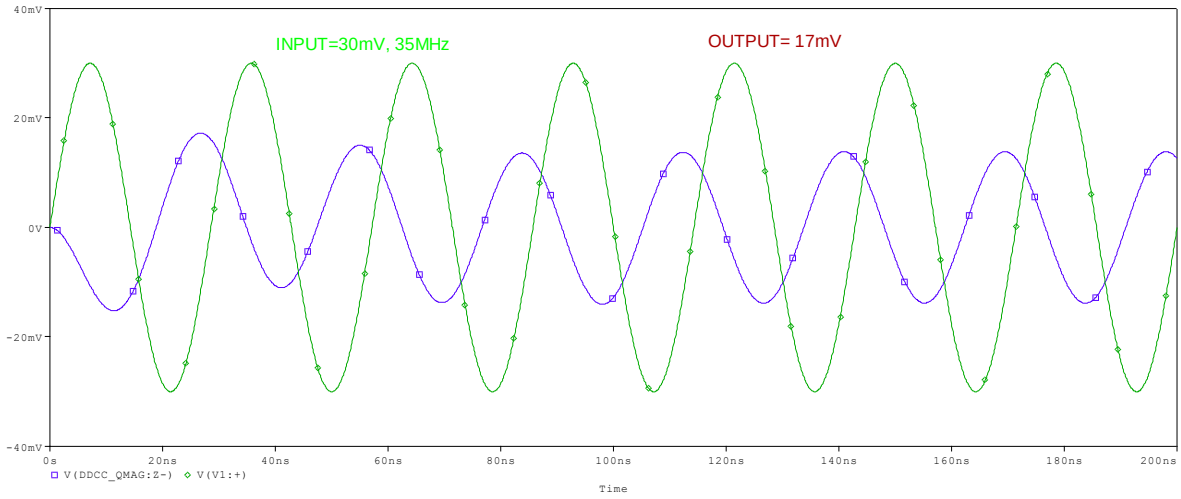

Fig 5.16 Transient response of the band pass filter at 35MHz

The following table shows the bifurcated values of R_5, corresponding values of K, Q' and H_o'

R_{5a} and R_{5b}	K	Q'	H_o'
1k and 9k	0.899	7	9.9
5k and 5k	0.5	1.414	2
9k and 1k	0.1	0.785	1.11

Table 5.3 Various values of R_5 as potentiometer

Faithful output was obtained for input signal to a maximum of $2V_{p-p}$. The aspect ratio of the transistors for DDCC is given in the table below. All the designed filters are Butterworth filters.

Transistor	*W* (*μ*m)	*L* (*μ*m)
M1–M4	1.6	1
M5–M6	8	1
M7–M8	20	1
M9–M10	29	1
M11–M12	90	1
M13–M15	20	1
M16–M18	90	1

Table 5.4 Transistor dimensions of the DDCC used

CHAPTER 6
IMPLEMENTATION OF ALL PASS FILTER USING DDCC

6.1 INTRODUCTION

First order all pass filters are widely used in communication and instrumentation field to provide phase delay equalization by providing phase shift from 0 to ∏ or ∏ to 0 keeping the amplitude unchanged [15-18]. Two circuits are shown, one with grounded resistor and the other with grounded capacitor both using single DDCC [19].

6.2 ALL PASS FILTER WITH GROUNDED RESISTOR

The circuit shown below is the first order all pass filter with grounded resistor and a floating capacitor. The circuit uses a single DDCC.

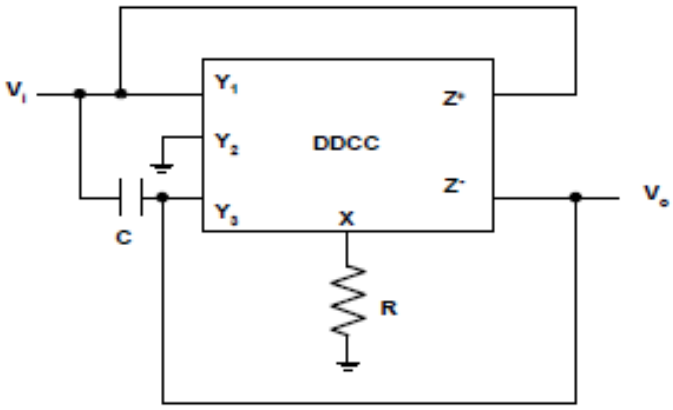

Fig 6.1 Block diagram of grounded resistor APF [19]

The transfer function for the above circuit is:-

$$\frac{V_o}{V_i} = \frac{sCR-1}{sCR+1} \qquad (6.1)$$

phase response for the circuit is:-

$$\phi(\omega) = 180^o - 2\tan^{-1}(\omega RC) \qquad (6.2)$$

6.2.1 FREQUENCY RESPONSE OF THE GROUNDED RESISTOR ALL PASS FILTER

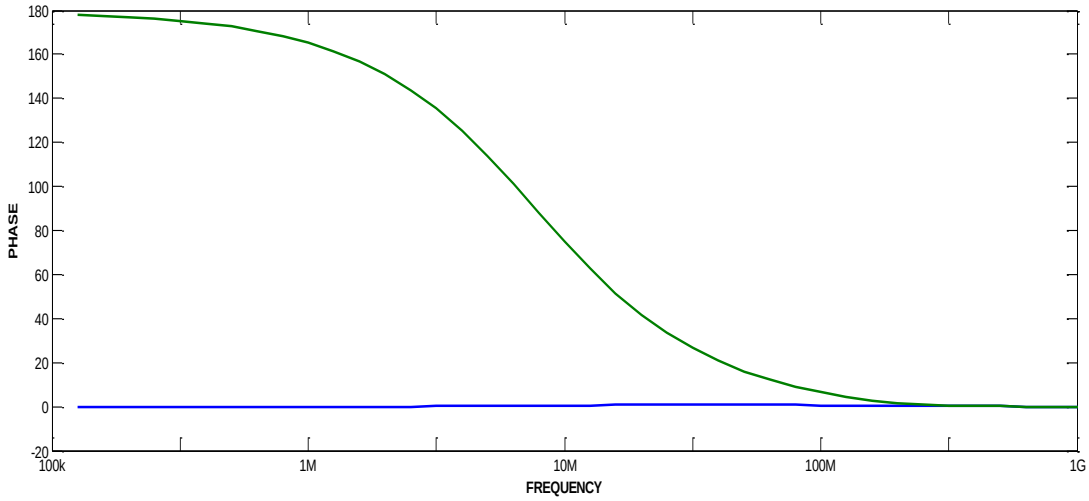

Fig 6.2 Grounded resistor APF frequency response using DDCC

The response shows a 0dB gain with a phase change from 180^o to 0^o and f_o=10MHz.

6.3 ALL PASS FILTER WITH GROUNDED CAPACITOR

The circuit shown below is the first order all pass filter with grounded capacitor and a floating resistor. The circuit uses a single DDCC.

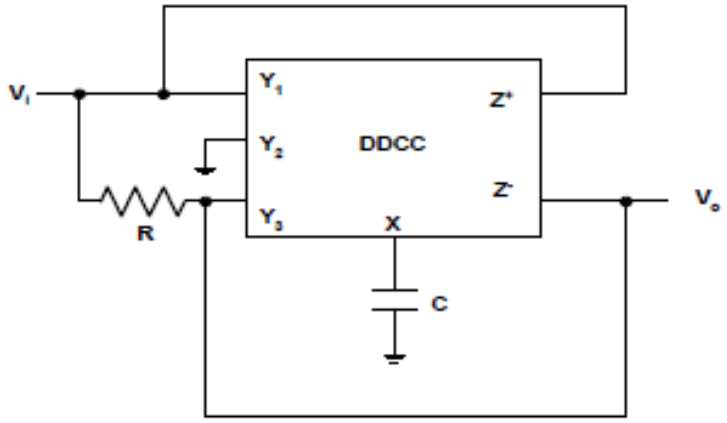

Fig 6.3 Block diagram of grounded capacitor APF [19]

The transfer function for the above circuit is:-

$$\frac{V_o}{V_i} = \frac{1-sCR}{1+sCR} \qquad (6.3)$$

The phase response for the circuit is:-

$$\phi(\omega) = -2\tan^{-1}(\omega RC) \qquad (6.4)$$

6.3.1 FREQUENCY RESPONSE OF THE GROUNDED CAPACITOR ALL PASS FILTER

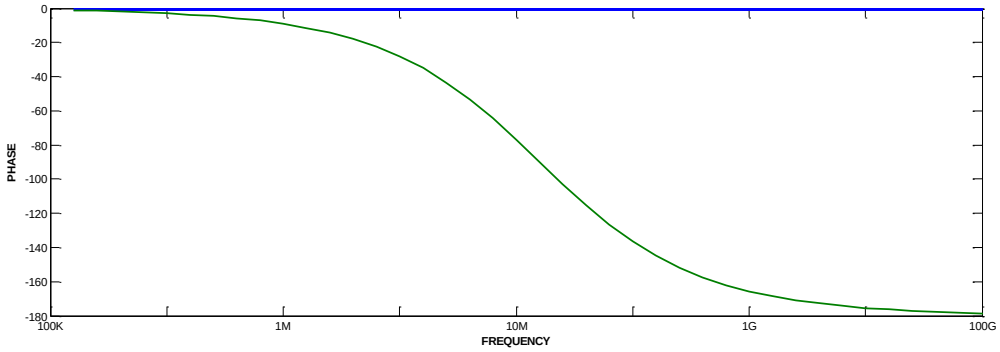

Fig 6.4 Grounded capacitor APF frequency response using DDCC

The response shows a 0dB gain with a phase change from 0^o to -180^o and f_o=10MHz.

The aspect ratio taken are W/L = 0.24/0.18 μm. The supply voltages were taken as V_{DD} = 2.5V and V_{SS} = -2.5V. The biasing voltage V_{BB} is taken as -1.892V. The capacitor value taken was 15.9pF and the resistor used is 1k Ω.

CHAPTER 7
CONCLUSION AND FUTURE SCOPE

7.1 CONCLUSION

Current conveyors an important building block in analog signal processing was described with its applications and variants. The three current conveyors namely the first, second and third generation were described with their unique properties and advantages in comparison with the others. To extend towards a more versatile block called differential difference current conveyor the differential difference amplifier was described. Clubbed with the advantage of DDA and CC the DDCC has wide bandwidth, greater linearity, high slew rate, wide dynamic range, simple circuitry, low power consumption and arithmetic operation capability.

A full wave rectifier was designed using DDCC's. With the advantage of 0 cut-in voltage the circuit is able to faithfully rectify signals as low as 100mV.

A low pass and high pass biquad filters were simulated using DDCC. In this the natural frequency could be altered without changing the Q by adjusting the passive components. By the use of a variable resistor the Q-magnification property was also brought about in low pass and band pass filters. The configurations enabled high input impedance therefore help in cascading.

First order all pass filters with grounded capacitors and grounded resistors respectively were simulated. DDCC was the active element used. The circuits provided high input impedance. All the circuits were simulated on PSPICE with device model parameters MIETEC 0.5µm CMOS process.

7.2 FUTURE SCOPE

Current conveyors are the emerging class of high performance analog circuits due to its versatile features. In the present scenario as the supply voltage and the threshold voltage of the device reduces the performance delivered is affected in the form of reduced noise margin,

bandwidth reduction, increased propagation delay and so on. However current conveyors capable of operating in current mode too helps to solve these problems.

Current conveyors which can be operated in voltage and current mode have wide applications such as oscillators, filters, analog to digital converter and various analog signal processing blocks. Current mode operation provides voltage independent high bandwidth. Here the emphasis is on current in various branches and voltage at nodes is not of a concern.

APPENDIX

MODEL PARAMETERS MIETEC 0.5µM CMOS PROCESS

PMOS

+ LEVEL=3 + UO=100 + TOX=1E-8 + TPG=1 + VTO=-.58 + JS=.38E-6 + XJ=.1E-6

+ RS=886 + RSH=1.81 + LD=3E-8 + ETA=0 + VMAX=113E3 + NSUB=2.08E17

+ PB=.911 + PHI=.905 + THETA=.12 + GAMMA=.76 + KAPPA=2 + AF=1 + WD=1.4E-7

+ CJ=85E-5 + MJ=.429 + CJSW=4.67E-10 + MJSW=.631 + CGSO=1.38E-10

+ CGDO=1.38E-10 + CGBO=3.45E-10 + KF=1.08E-29 + DELTA=0.81 + NFS=.52E11

+ W=200U + L=4U

NMOS

+ LEVEL=3 + UO=460.5 + TOX=1E-8 + TPG=1 + VTO=.62 + JS=1.8E-6 + XJ=.15E-6

+ RS=417 + RSH=2.73 + LD=4E-8 + ETA=0 + VMAX=130E3 + NSUB=1.71E17

+ PB=.761 + PHI=.905 + THETA=.129 + GAMMA=.69 + KAPPA=0.1 + AF=1

+ WD=1.1E-7+ CJ=76.4E-5 + MJ=.357 + CJSW=5.68E-10 + MJSW=.302 + CGSO=1.38E-10 + CGDO=1.38E-10 + CGBO=3.45E-10 + KF=3.07E-28 + DELTA=0.42 + NFS=1.2E11

+ W=90U + L=4U

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