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Performance Evaluation of CML based Serilalizer/Deserializer

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by

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CERTIFICATE

This is to certify that the dissertation titled **"Performance Evaluation of CML based Serilalizer/Deserializer"** is a bonafide record of work done by **Garima Bhatia, Roll No. 2K13/VLS/07** at **Delhi Technological University** for partial fulfilment of the requirements for the degree of Master of Technology in VLSI and Embedded System Design. This project was carried out under my supervision and has not been submitted anywhere else, either in part or full, for the award of any other degree or diploma to the best of my knowledge and belief.

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ABSTRACT

In communication systems, serializers and deserializers are the common and important building blocks. They are used in optical networks for purpose of telecommunication for long distance as well as for high speed connections over small distance comparable to the length of circuit board, to meet higher data bandwidth. Since CMOS based circuits have this huge disadvantage of larger power dissipation at higher frequencies, this has led to a shift in trend to current mode circuits as they have innate advantage of higher speed performance because of reduced voltage swing and much less power consumption at higher frequencies, as compared to CMOS based circuits.

This thesis provides novel Serializers and deserializers for which triple-tail MCML cell based D-latch with feedback resistors has been used as basic building block which is not only immune to various device mismatches caused by threshold voltage fluctuation and also operates at higher frequencies as compared to simple MCML based D-latch and triple-tail based MCML D–latch.

MCML D-latch uses two stacked transistors for logic implementation and puts a limit on minimum power supply that can be applied and hence have huge static power dissipation. This static power can be further reduced by decreasing the power supply, for which triple-tail MCML based D-latch, has come into picture, which uses one stack of transistors in PDN and hence can operate at low power supply as compared to traditional MCML D-latch. Despite of being shown that MCML circuits consumes less power as compared to CMOS at operation frequencies of very high in range, designers are showing reluctance to replace CMOS with MCML because its performance is greatly affected by the fluctuation of threshold voltages of the differential pair transistors of PDN network because of its differential nature.

For the basis of this thesis, first the study of basic MCML inverter, MCML based D-latch and triple-tail MCML based D-latch, their design parameters and static analysis have been

completed, also, how threshold voltage effects the circuit has been studied for both basic MCML circuit and triple-tail MCML based circuit, and the mathematical formulation of effect of threshold voltage among NMOS transistor has been studied and the mathematical formulation of effect of threshold voltage among PMOS transistor has been derived in this thesis.

To overcome the problem of threshold voltage fluctuation, effect of using feedback resistance between input and output of MCML based circuits, a method to reduce the effect of threshold-voltage fluctuation has been analyzed for MCML inverters, and a significant improvement in their frequency i.e. 91% hike in cut-off frequency MCML inverters have been witnessed, and in our thesis, this scheme has been used in MCML based D-latch and triple-tail MCML based D-latch, for faster i.e. 74.7% speed improvement at the expense of reduced gain and robust D-latches, which later used as basic building blocks of our serializers and deserializer which are faster, more robust and more power efficient. Thus, the three performance parameters, i.e. power, area and speed are compared for Serializers and Deserializers whose building blocks are MCML based D-latch and triple-tail MCML based D-latch ,and the latter is more efficient in all three performance parameters i.e. is more delay, power and area efficient.

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Chapter 1

Introduction

1.1 Thesis Motivation

This is the generation of portable mobile devices, and much recent advancement in VLSI technology has made possible the rapid growth in the area of hand-held electronic devices. PDAs, smart phones and portable laptops have all taken a substantial place in our daily life. Two main concerns while utilizing these devices are its speed and battery life. With the scaling down of the process technology, processing power demand is increasing also and hence, if architectural changes are not made now, the power consumption will increase over the time of future IC's[1]. The International Technology Road map for Semiconductors (ITRS) has stated in its 2005 report on Radio Frequency and Analog /Mixed-Signal Technologies for Wireless Communications that "As the integration density and the operation frequency increase, protection of noise sensitive analog circuits from noisy digital circuits will become increasingly difficult"[2]

New technologies and networks, including potent microprocessors, multimedia devices with vast bandwidth requirements are pushing the limits of system performances and data transfers in telecommunication area. The rapidly-increasing sizes of data in telecommunication networks have relighted interest in high-speed optical and electronics devices and systems. A digital logic style namely MOS Current Mode Logic (MCML) is a promising alternative to CMOS logic, in both reducing power consumption at high frequencies and providing high performance for mixed-signal applications [3-5]. In digital communication, because of high speed of MCML circuits, current-mode logic can be used in implementation of IC as a serializer(parallel to series converter converter) and deserializer(series to parallel converter) , which is key component in gigahertz optical fiber link systems because of growing demand for high-speed communications.

Also, static power can be further reduced by decreasing the power supply, but the traditional MCML D-latch have stacked transistor and puts a limit on minimum power supply that can be applied. And hence for power can be lowered by reducing the number of stacks, for which triple-tail MCML based has been introduced in [14].

Despite of being shown that MCML circuits consumes less power as compared to CMOS at operation frequencies of more than 300MHz[3], designers are showing unwillingness to replace CMOS with MCML because its performance is greatly affected by the fluctuation of threshold voltages of the differential pair transistors of PDN network because of its differential nature[5,10].

1.2 Thesis Objectives

The purpose of this work is to study the effect of threshold-voltage fluctuation in MCML circuits and triple-tail MCML D-latch. The method introduced in [10] to reduce the effect of threshold-voltage fluctuation has been studied and implemented on triple-tail based d-latch. Further, high speed serializer/ deserialzers are designed in this thesis using CMOS, traditional MCML and triple-tail MCML topology and comparative study has been done.

1.3 Thesis Organization

In next chapter a brief introduction of MCML and MCML based D-latch has been done. The discussion includes the general operation of the circuits, design parameters of both inverter and D-latch have been discussed. The requirements and problems associated with logic are also introduced in next chapter.

Chapter 3 discusses the triple-tail based D-latch. Its operation have been discussed Also, analysis of the circuit, and its technique to design the circuit with respect to its design parameters have also been studied in this chapter.

In chapter 4 how threshold voltage effects the circuit has been studied for both basic MCML circuit and triple-tail MCML based circuit, and the mathematical formulation of effect of threshold voltage among NMOS transistor has been studied and the mathematical formulation of effect of threshold voltage among PMOS transistor has been derived in this chapter of our thesis.

Also, a method to reduce the effect of threshold-voltage fluctuation introduced in [10] has been studied for MCML inverters and is also applied and varied using SPICE simulations for triple-tail based D-latch.

In chapter 5, an introduction has been done on how serializer and deserialzer are designed using d-latch. Then serializer/ deserialzers are designed in this chapter using CMOS, traditional MCML and triple-tail MCML topology and comparative study has been done.

Chapter 2

MCML Based D-Latch Design

2.1 Basics of MCML Operation

MOS Current-Mode Logic or MCML is a differential amplifier used in implementation of digital applications. Figure 2.1 shows a basic block of an MCML circuit. In Fig. 2.1, it can be observed that, by switching of current from one branch to another, the logic is comprehended, thus basically implements a voltage-controlled current switch.

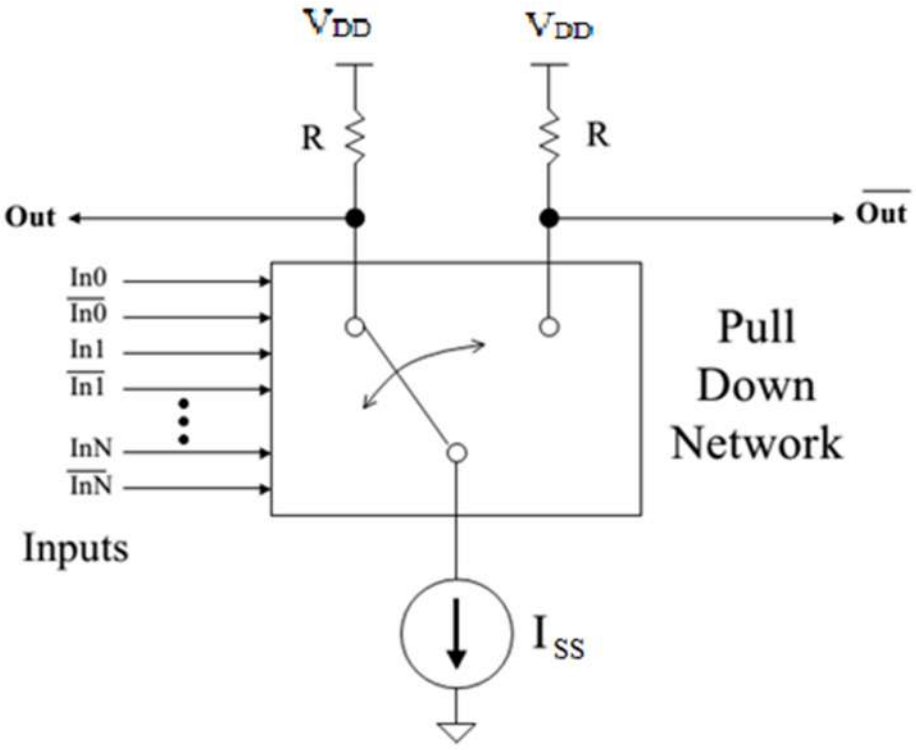


Fig. 2.1 Basic block of an MCML circuit.

The circuit is composed of a set of differential-pair transistors, which are organized to steer the bias current, I_{SS} in one branch and switching off the other in a certain way, to realize the logic, according to the differential-inputs applied to the circuit. The voltages at corresponding output terminals are V_{DD} and $V_{DD} - \Delta V$, where $\Delta V = I_{SS} \times R$. Since the supply current required by the gate is almost constant, which in turn leads to static power dissipation and also the low-switching noise feature of MCML. An active load such as a PMOS transistor operating in the linear region can replace the load resistance and an NMOS transistor working in saturation region can control the tail-current I_{SS}.

For best performance, all the bias current, I_{SS} needs to flow though ON branch only, and the load resistance should be small to reduce the RC delay. This ensures the one output node of the circuit is at voltage V_{DD}, while other one is at the voltage $V_{DD} - \Delta V$, where $\Delta V = I_{SS} \times R$, where I_{SS} is the value of current flowing through the current source and R is load resistance implemented by PMOS transistors M_3 and M_4. It is advantageous to have low voltage-swing because: (1) delay of the gate is reduced significantly and (2) results in reduction of cross-talk between the nearby signals. Also, another advantage of MCML is high immunity to common-mode noise because of its differential nature. Also the static current source in MCML provides a steady current irrespective of switching activity, thus MCML is a friendly alternative for mixed-signal applications as compared to CMOS.

MCML has some major drawbacks. Firstly, due to constant current source, large static power is dissipated. But compared with CMOS circuits, using Power/MHz as a measure for power dissipation, it can be seen from Fig. 2.3 that MCML consumes less power at higher frequencies and more at lower frequencies. Thus, MCML is preferred in applications operating at high frequencies only, in order to reduce the overhead dissipation of static power. Also, the maximum operation frequency of the MCML, is greatly affected by the fluctuation of threshold voltages (V_{TH}) of the differential pair transistors of the pull-down network[5] and this threshold voltage fluctuation increases as the gate length decreases, it turns out to be a serious problem for deep-submicron CMOS transistors. More details will be given in chapter 5, about how this threshold voltage fluctuation affects the working of MCML circuit and how it can be over-come this problem.

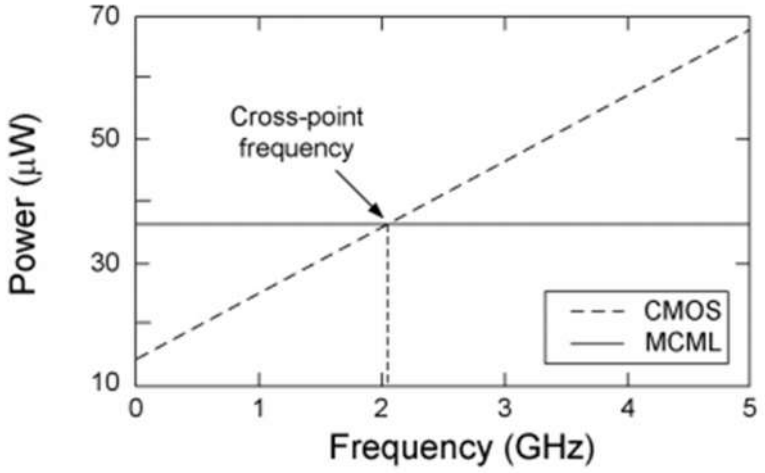


Fig. 2.2 Power vs. Frequency for MCML inverters[8]

2.2 MCML Design Parameters

Let us consider an MCML inverter shown in Fig. 2.3. Here load capacitance C_L represents the loading effect of the wiring capacitance and following gates connected at the output. The NMOS differential transistor pair $M_1 - M_2$, which is driven by the differential input signal $v_i = v_{i1} - v_{i2}$ and works in the saturation or the cut-off region and is biased by the constant current source I_{SS} , implemented by a NMOS transistor working in saturation region . When v_i is high, the bias current, I_{SS} flows through transistors M_1 and M_3, and the differential output voltage $v_o = v_{o1} - v_{o2}$ is at the low level and is equal to $v_o = -\Delta V$, where ΔV is the voltage drop across M_3 when its drain current is equal to I_{SS}. Similarly, if v_i is low, output voltage $v_o = \Delta V$, and hence the logic swing of the gate is equal to $2\Delta V$. To keep M_1 out of the linear region, $\Delta V = I_{SS} \times R$, where R is the resistance implemented by PMOS transistors M_3 and M_4 , must be kept lower than the threshold voltage of NMOS transistor, $V_{T,n}$[6].

In particular, assuming transistor operation in the saturation region, currents iD1 and iD2 of transistors $M_1 - M_2$ differential pair shown in Fig. 2.2 can be expressed as a function of the differential input voltage $v_i = v_{i1} - v_{i2}$as

$$i_{D1}(v_i) = \begin{cases} 0 & if\ v_i \le \sqrt{\frac{2I_{SS}}{\mu_n C_{ox}\frac{W_n}{L_n}}} \\ \frac{I_{SS}}{2} + \frac{v_i}{2}\sqrt{\mu_n C_{ox}\frac{W_n}{L_n} I_{SS} - \left(\mu_n C_{ox}\frac{W_n}{L_n}\frac{v_i}{2}\right)^2} & if\ |v_i| \le \sqrt{\frac{2I_{SS}}{\mu_n C_{ox}\frac{W_n}{L_n}}} \\ I_{SS} & if\ v_i \ge \sqrt{\frac{2I_{SS}}{\mu_n C_{ox}\frac{W_n}{L_n}}} \end{cases} \quad (2.1a)$$

$$i_{D1}(v_i) = I_{SS} - i_{D1}(v_i) \quad (2.1b)$$

Where W_n and L_n are the effective width and length of NMOS differential pair shown in Fig. 2.2, respectively and C_{ox} is the oxide capacitance per unit area, μ_n is the carrier mobility of NMOS transistor and I_{SS} is the bias current. For complete steering of bias current I_{SS} to the one of the transistors, the input differential voltage should be greater than $\sqrt{\frac{2I_{SS}}{\mu_n C_{ox}\frac{W_n}{L_n}}}$. This steered current is converted into differential output voltage through the PMOS transistors acting as active load $M_3 - M_4$.

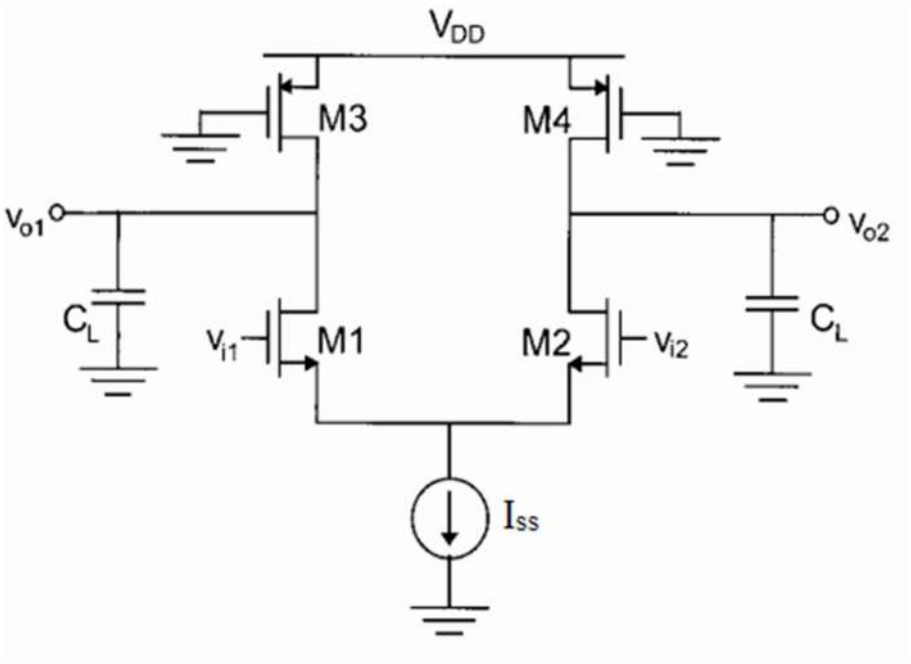


Fig. 2.3 MCML Inverter/Buffer[8]

The design parameters of a typical MCML circuit are the circuit delay t_d, voltage swing ΔV, voltage gain A_v, noise margin *NM* and total power dissipation P_D. And the design variables available to achieve the aforementioned parameters are the total bias current I_{SS}, transistor sizes of the differential pull-down network, load resistance and hence transistor sizes of PMOS transistors which implements the load resistances.[8]

(A) Voltage-Swing (ΔV):

As mentioned above, the voltage-swing of MCML circuits is expressed as,

$$V_{SWING} = 2\Delta V \quad (2.2a)$$

$$\Delta V = I_{SS} \times R \quad (2.2b)$$

It can be noted that, the circuit with same ΔV and C_L, would require a larger bias current I_{SS}, in order to have a shorter t_d. Thus ΔV is an important parameter that links

performance with power dissipation. Simulation results of transient analysis of MCML inverter has been shown in Fig. 2.4, for 400mV voltage swing and 80µA bias current. The voltage swing of the output came out to be 381mV with the error of 4.75%. Table 2.1 shows the voltage swing obtained for MCML inverter simulated for different bias currents and error between simulated and predicted values.

Table 2.1 Voltage swing of MCML inverter simulated for different bias currents

$I_{SS}(\mu A)$	Voltage Swing (in mV)	Error(in %)
20	380.25	4.9
50	378	5.5
80	381	4.75

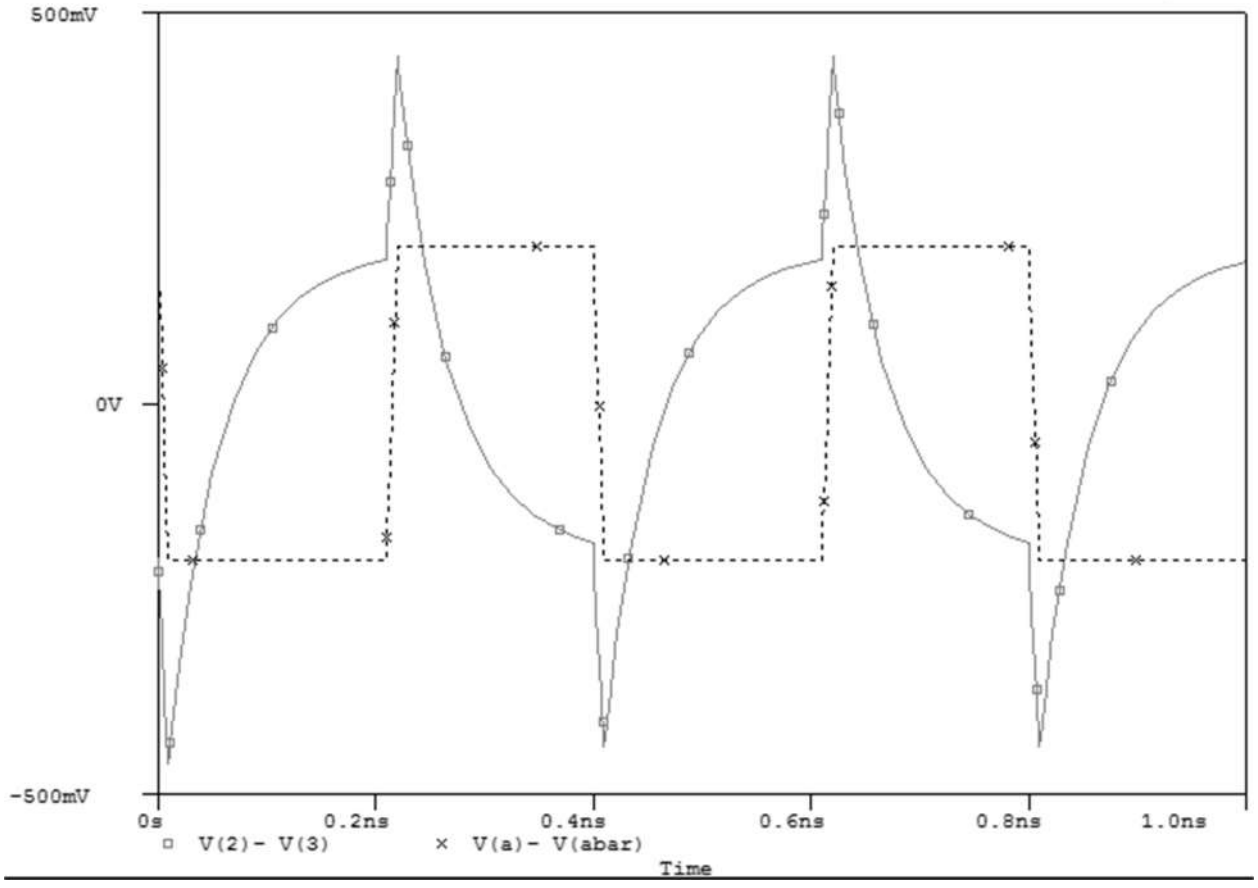


Fig. 2.4 Transient Analysis of MCML inverter

(B) *Voltage gain (A_v):*

DC Voltage gain is defined as the voltage gain at common-mode voltage. A_v is a key parameter in regulating the stability and circuit regeneration. For MCML inverter, A_v can be expressed as

$$A_v = g_{m,1}R = R\sqrt{2\mu_n C_{ox}\frac{W_n}{L_n}\frac{I_{SS}}{2}} = \Delta V\sqrt{\mu_n C_{ox}\frac{W_n}{L_n}\frac{1}{I_{SS}}} \quad (2.3)$$

where $g_{m,1}$ is the tranconductance on the NMOS transistor M_1 of MCML inverter shown in Fig. 2.3, $\mu_n$is the electron mobility, C_{ox} is the oxide capacitance and W_n and $L_n$are the effective width and length of M_1, respectively.

MCML inverter has been simulated for bias current value of 50μA and gain 4, AC analysis of which is shown in Fig. 2.5. It can be seen that there is a close relation between simulated and predicted voltage gain.

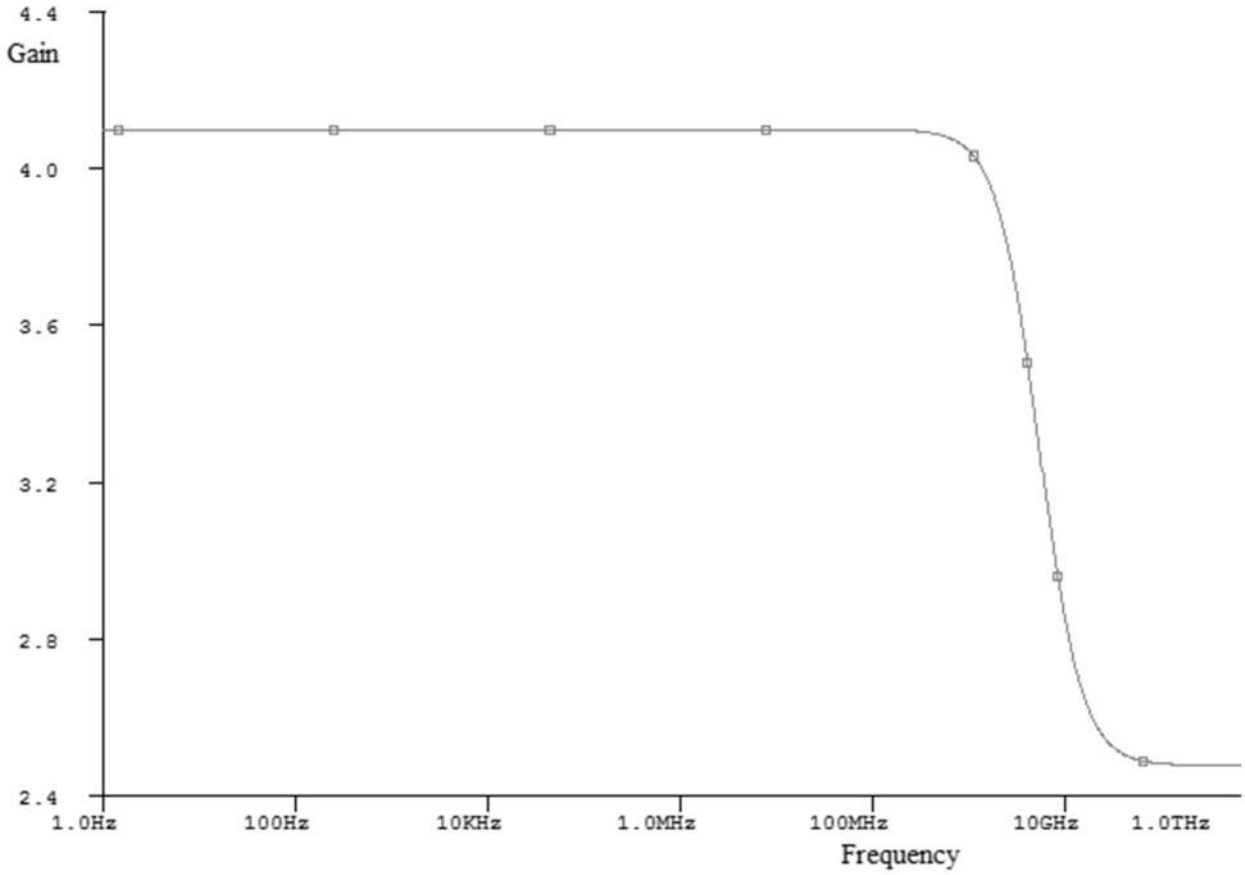


Fig. 2.5 AC Analysis of MCML inverter

(C) Total circuit delay (t_d):

A small signal model can used to approximate the behavior of MCML circuits, as they experience small voltage swing[9]. Equivalent small-signal model of MCML inverters is shown in Fig. 2.6. Here, $C_{db,1}$ and $C_{gd,1}$ are the drain-bulk capacitance and gate-drain overlap capacitance of the NMOS transistor of the pull-down network, respectively, and, $C_{db,2}$ and $C_{gd,2}$ are the drain-bulk capacitance and gate-drain overlap capacitance of the PMOS transistor, respectively. C_L is the load capacitance which includes the loading effect of wiring capacitance and fan-out capacitances of the gates connected to the output of the circuit.

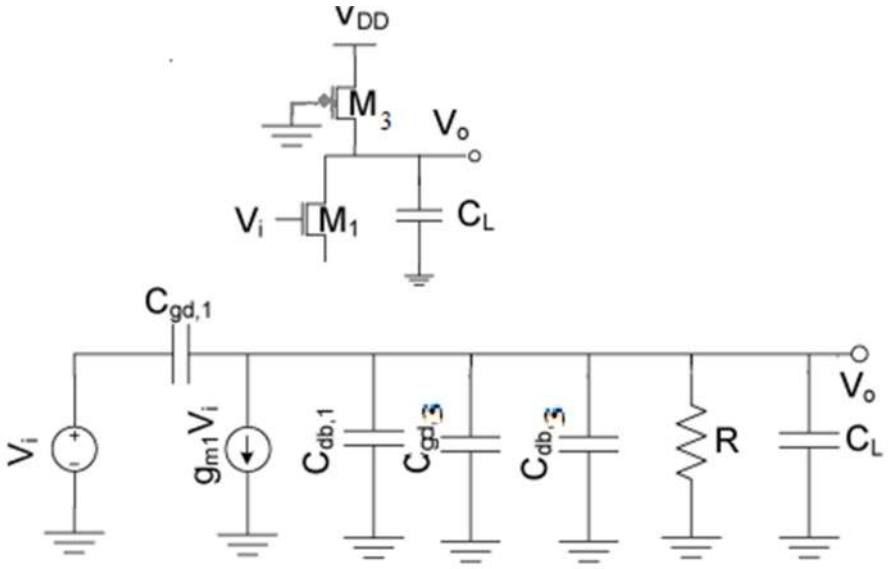


Fig. 2.6 Small-signal equivalent of MCML inverter

Using analysis of first-order circuits, delay of the inverter t_d can be approximated by

$$t_d = 0.69R(C_{gd,1} + C_{db,1} + C_{gd,3} + C_{db,3} + C_L) \quad (2.4)$$

In table 2.2, simulated delay for different bias current values for 400mV voltage swing and for voltage gain equals to 4 with 50fF load capacitance has been tabulated. It can be seen that with increment in the value of bias current, delay keeps on decreasing, because for same voltage swing, value of load resistance is required less and hence, from eq. 2.4, with increment in current bias value, delay of the circuit decreases.

Table 2.2 Delay between input and out for different bias current for MCML inverter

$I_{SS}(\mu A)$	Delay (t_d)
20	54.7ps
50	52.67ps
80	43.37ps

(D) *Power Dissipation* (P_D)*:*

Because of the use of constant current source, MCML circuits consume static power and compared to which dynamic power of the MCML circuits is ignorable [5]. P_D in MCML is given by

$$P_D = V_{DD} \times I_{SS} \tag{2.5}$$

Table 2.3 shows the simulated power dissipation of the MCML inverter for 1.4 supply voltage. As formulated, the power dissipation of the inverter has come out be their product. Thus, to minimize the dissipation, one has to reduce the power supply, such that all the transistors are in saturation for proper operation of the MCML based circuits.

Table 2.3 **Power Dissipation for different bias current for MCML inverter.**

$I_{SS}(\mu A)$	**Power Dissipation(Watts)**
20	2.80E-05
50	7 E-05
80	11.2 E-05

(E) *Noise Margin (NM):*

Because of reduced voltage swings, large noise margins can be achieved in MCML circuits. However, designers can accept small values of noise margins because of high noise immunity of MCML circuits which is result of differential nature of current-mode logic circuits. For MCML circuit, NM is given by [16]

$$NM = \Delta V \frac{\sqrt{4A_v^2 - 1 - \sqrt{8A_v^2 + 1}}}{A_v^2\sqrt{2}} \times \left(\frac{\sqrt{4A_v^2 - 1 + \sqrt{8A_v^2 + 1}}}{2\sqrt{2}} - 1 \right) \tag{2.6}$$

which lead to following expression

$$NM = \Delta V\left(1 - \frac{\sqrt{2}}{A_v}\sqrt{1 - \frac{1}{\sqrt{2}A_v}}\right) \cong \Delta V\left(1 - \frac{\sqrt{2}}{A_v}\right) \quad (2.7)$$

The voltage transfer characteristics of the MCML inverter has been shown in Fig. 2.7 simulated for 400mV voltage swing, 50µA bias current, 4 voltage gain and 130mV noise margin and the noise margin came out from simulation is 138.45 mV with the error of 6.5%.

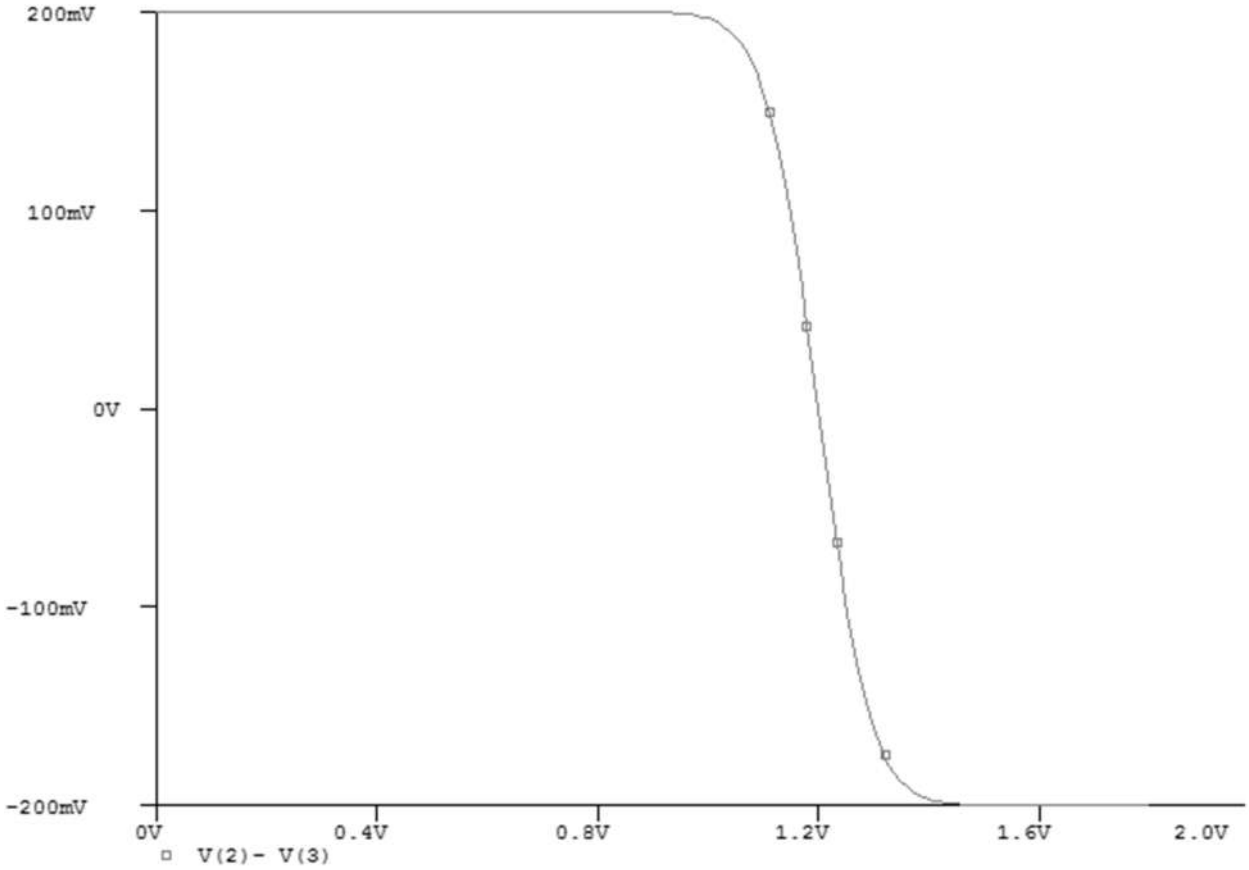


Fig. 2.7 Threshold Voltage characteristics of MCML inverter.

2.3 Design strategies of MCML based D-latch:

In literature, MCML gates have been explored in terms of delay modeling and noise margin. In this section, design strategies for MCML based D-latch has been studied. Since, MCML has superior power efficiency and speed at higher frequencies as compared to CMOS, hence they are more suitable for implementation of serializer/deserializer (also known by acronym SerDes), for which the fundamental gates that is used is D=latch, in the applications of digital broadband communications as the exhibit implementation of multiplexing/demultiplexing in the range of 10Gbps with much higher operating frequency and less power dissipation than static CMOS logic[10]. This strategy allows us to meet the speed constraint or aid us in optimizing the delay and power consumption by sizing the bias current transistor and aspect ratios of transistors of pull-down network and PMOS transistors which are used to implement resistors.

The circuit used to implement the MCML based D-latch has been shown in Fig. 2.8. In the circuit, according to the logic level of clock, new data carried by '$D - \overline{D}$' signal is conveyed at output or pervious output is restored. Indeed, static behavior of the circuit is not affected by other constant input.

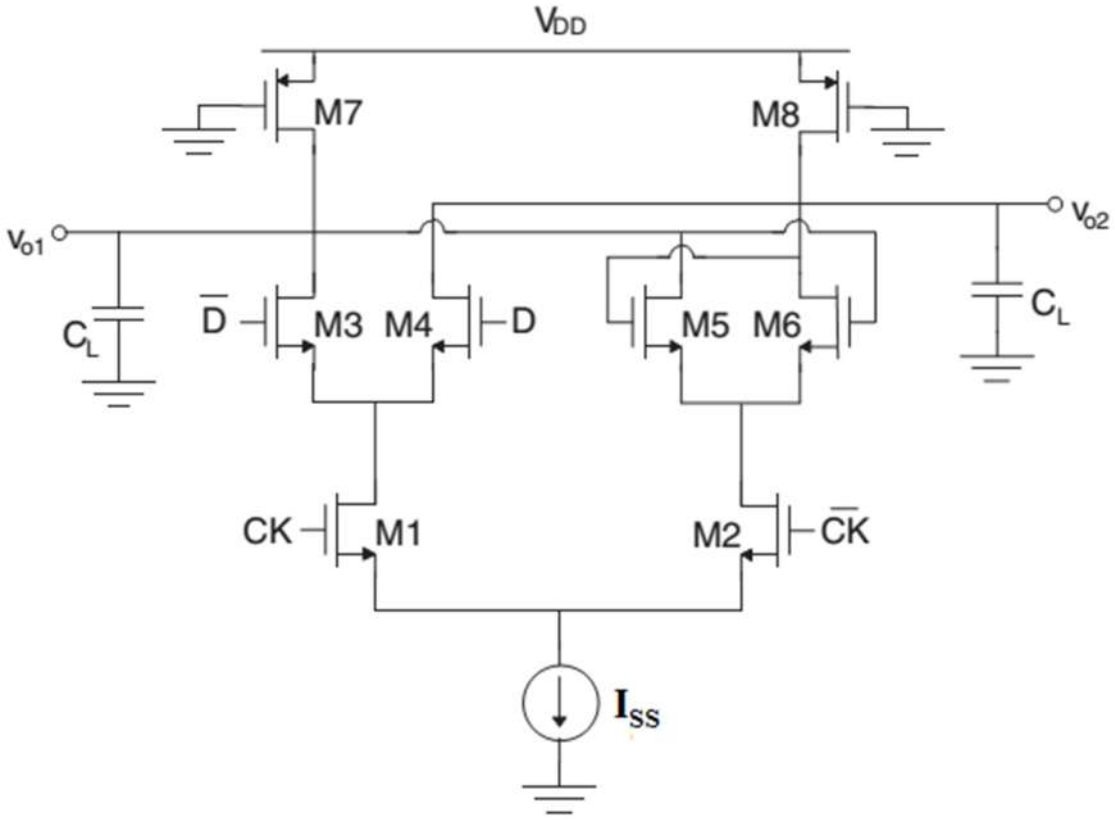


Fig. 2.8 MCML based D-latch

(a) *Voltage-swing:*

As mentioned for MCML invertor shown in Fig. 2.2, the voltage-swing for D-latch can be expressed as

$$V_{SWING} = 2I_{SS}R_P \tag{2.8a}$$

Here, R_P is the resistance implemented by PMOS transistors working in linear region and by using the BSIM3v3 model[11], the expression R_P can be computed as

$$R_P = \frac{R_{int}}{1-\frac{(R_{DSW}*10^{-6})/W_P}{R_{int}}} \tag{2.8b}$$

where R_{DSW} is the empirical model parameter and the parameter R_{int} is the intrinsic resistance of the PMOS transistor in the linear region and is given as

$$R_{int} = [\mu_{eff,p} C_{ox} \frac{W_P}{L_P} (V_{DD} - |V_{TP}|)]^{-1} \quad (2.9)$$

where C_{ox} is the oxide capacitance per unit area and the parameters $\mu_{eff,p}$ is effective hole mobility, V_{TP} is the threshold voltage, W_P and L_P the effective channel width and effective channel length of the load transistor. For 400mV voltage swing, 20μA bias current and 4 voltage gain, transient analysis of MCML based D-latch is shown in Fig. 2.9, where when clock is 1, data is transferred at output and when clock is 0, previous output is maintained as current output of the latch, with the total simulated voltage swing came out to be 383.27mV with error of 4.2% between the predicted and simulated results.

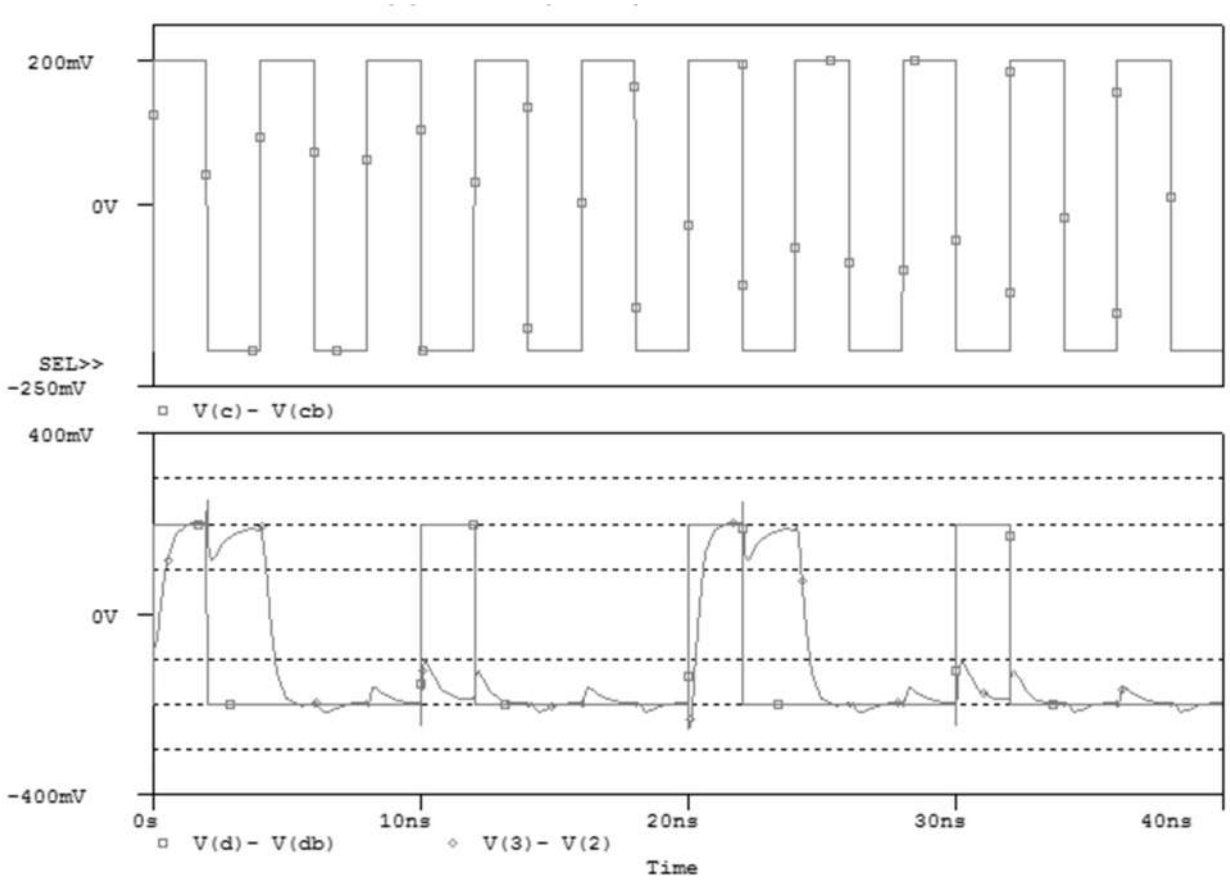


Fig. 2.9 Transient analysis of MCML based D-Latch

(b) DC Voltage gain (A_v):

As studied for MCML invertor shown in Fig. 2.2, when the logic threshold is zero i.e. at the common-mode input voltage, the small-signal voltage gain is resulted as

$$A_v = g_{m,n}R_P = R_P\sqrt{2\mu_n C_{ox}\frac{W_n}{L_n}\frac{I_{SS}}{2}} = \frac{V_{SWING}}{2}\sqrt{\mu_n C_{ox}\frac{W_n}{L_n}\frac{1}{I_{SS}}} \quad (2.10)$$

Where $g_{m,n}$ is the small-signal transconductance of NMOS transistors, W_n and L_n are the channel width and length of NMOS transistors shown in Fig.2.8 and μ_n is the effective mobility which is given as [11]

$$\mu_n = \frac{\mu_o}{1+(U_A+U_C V_{bseff})\left(\frac{V_{gst}+2V_{th}}{T_{ox}}\right)+U_b\left(\frac{V_{gst}+2V_{th}}{T_{ox}}\right)^2} \quad (2.11)$$

Where $V_{gst} = V_{gs} - V_{th}$.

MCML inverter has been simulated for 30μA bias current and gain 4, AC analysis of which is shown in Fig. 2.10. It can be seen that there is a close relation between simulated and predicted voltage gain

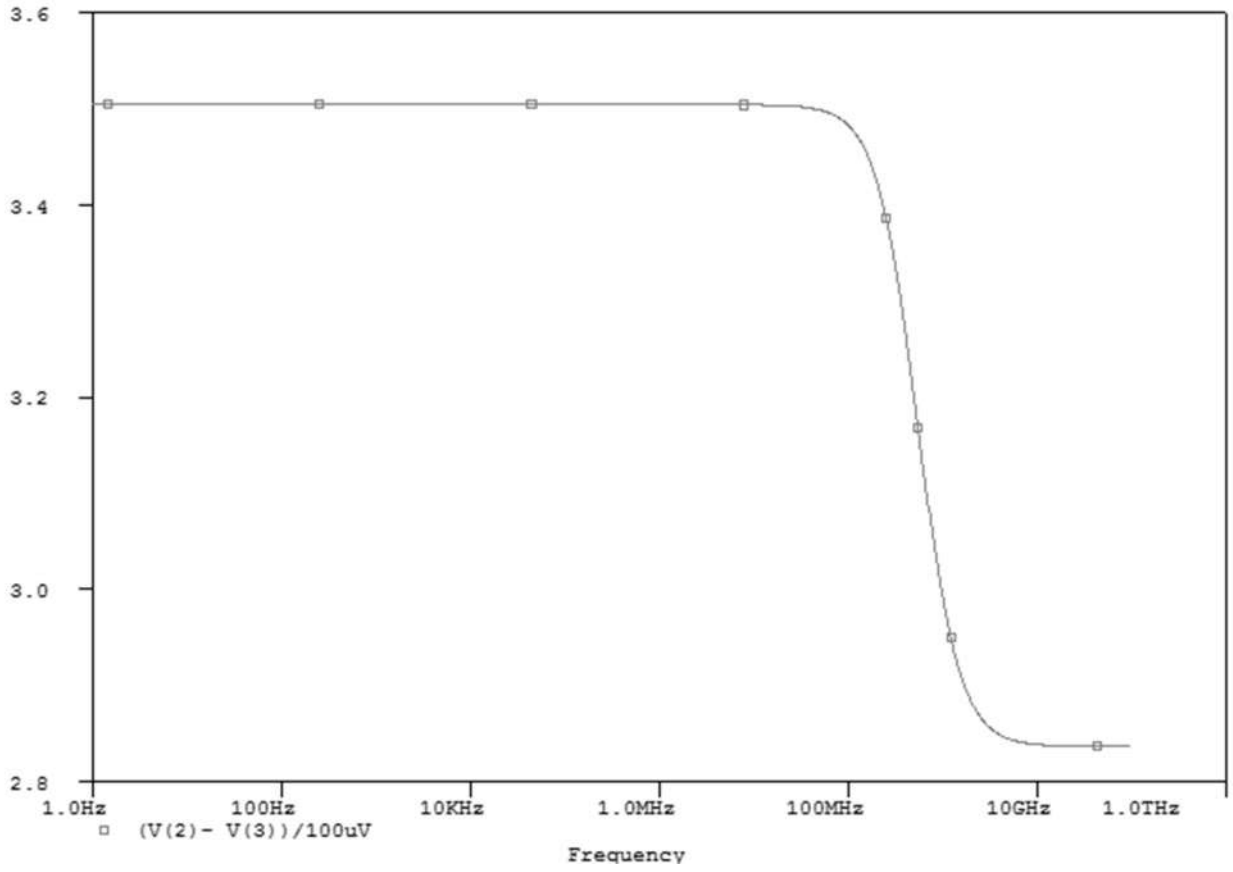


Fig. 2.10 AC analysis of MCML based D-latch

(c) *Noise-Margin:*

As studied for MCML invertor shown in Fig. 2.2, noise-margin can be expressed as[9]

$$\mathrm{NM} = \frac{\mathrm{V_{SWING}}}{2}\left(1 - \frac{\sqrt{2}}{\mathrm{A_v}}\sqrt{1 - \frac{1}{\sqrt{2}\mathrm{A_v}}}\right) \cong \frac{\mathrm{V_{SWING}}}{2}\left(1 - \frac{\sqrt{2}}{\mathrm{A_v}}\right) \tag{2.12}$$

(d) *Delay model of D-latch:*

As studied in [12], the worst case propagation delay is obtained by switching the clock signal applied to M_1 and M_2, transistors shown in Fig. 2.8, keeping all the other inputs constant. Thus, the delay can be realized by analyzing the half-circuit of the MCML D-latch shown in Fig. 2.8, is shown in Fig. 2.11

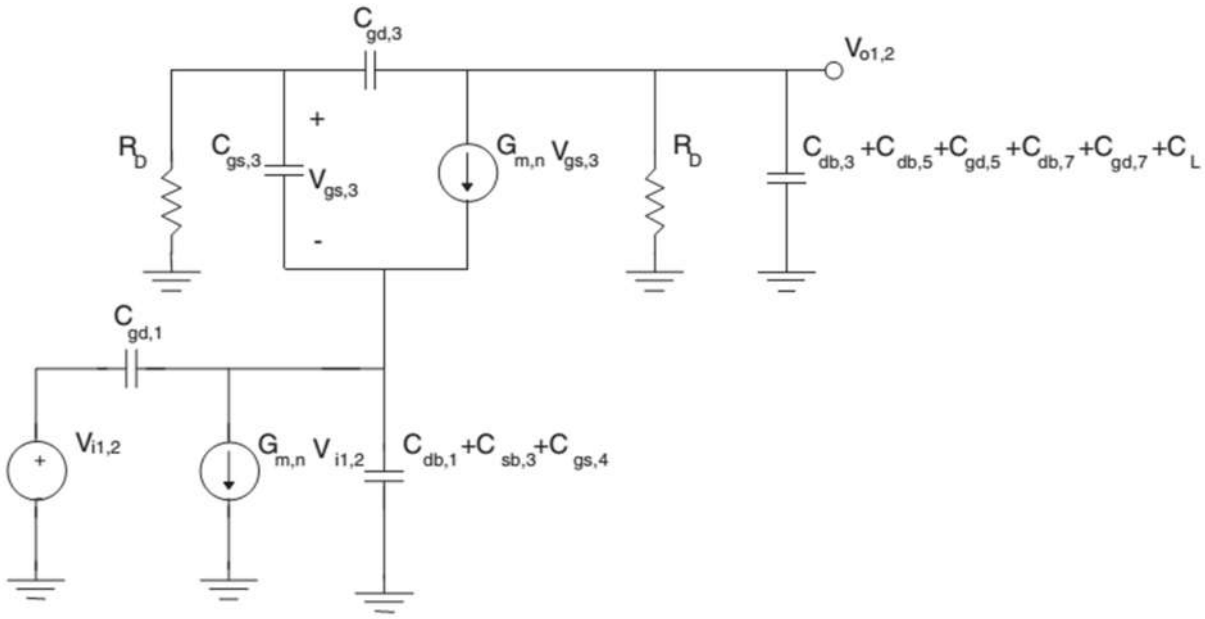


Fig. 2.11 Small-signal Half-circuit equivalent of MCML D-latch

Using dominant pole concept, delay is obtained as

$$t_{d,latch} = 0.69\left[R_P\left(2C_{gd,3} + C_{db,3} + C_{gd,5} + C_{db,5} + C_{gd,P} + C_{db,P} + C_L\right) + \frac{1}{G_{M,n}}\left(C_{gd,1} + C_{db,1} + C_{gs,3} + C_{sb,3} + C_{sb,4} + C_{gs,4}\right)\right] \quad (2.13)$$

Here it's worth noting that $G_{M,n}$ cannot be approximated by $g_{m,n}$ i.e. its small-signal assessment in saturation region. $G_{M,n}$ can be expressed as [12]

$$G_{M,n} = \sqrt{\frac{\mu_n C_{ox}}{2}\frac{W_{n3}}{L_{n3}} I_{SS}} = \frac{g_{m,n}}{2} \quad (2.14)$$

Hence, the delay can be expressed in terms of V_{SWING}, I_{SS} and A_v as

$$t_{d,latch} = 0.69\frac{V_{SWING}}{2I_{SS}}\left[3C_{gd,1} + 2C_{db,3} + C_{gd,P} + C_{db,P} + C_L + \frac{2}{A_v}\left(2C_{gd,1} + 3C_{db,1} + C_{gs,3}\right)\right] \quad (2.15)$$

where all NMOS transistors have an equal aspect ratio.

In table 2.4, simulated delay for different bias current values for 400mV voltage swing and for voltage gain equals to 4 with 50fF load capacitance has been tabulated. It can be seen that with increment in the value of bias current, delay keeps on decreasing, because for same voltage swing, value of load resistance is required less and hence, from eq. 2.15, with increment in current bias value, delay of the circuit decreases.

Table 2.4 Delay between input and out for different bias current for MCML based D-latch

$\mathbf{I_{SS}}(\boldsymbol{\mu A})$	**Delay** $(\mathbf{t_d})$
20	375.57ps
50	335.082ps
80	193.57ps

2.4 Effect of process variation in MCML based D-latch:

The impact of parameter variation on traditional MCML based D-Latch performance is studied at different design corners. The findings for various operating conditions are given in Table 2.5. It is found that the voltage swing, small-signal voltage gain, and noise margin for the traditional MCML based D-Latch, the voltage swing, small-signal voltage gain, and noise margin varies by a factor of 1.12, 1.02, and 1.06 respectively between the best and the worst cases. Here, TT, FF, FS, SF and SS represents the different process corners, and are typical NMOS typical PMOS, fast NMOS fast PMOS, fast NMOS slow PMOS, slow NMOS fast PMOS and slow NMOS slow PMOS.

Table 2.5 Effect of process variation on static parameters the traditional MCML based D-latch

Parameter	NMOS PMOS	T T	F F	S S	F S	S F
Simulation Conditions: $A_v = 4$, $V_{swing} = .4V$, $C_L = 50$ fF, $I_{SS} = 100\mu A$						
$\mathbf{V_{swing}(mV)}$		381	387	330	378	379
$\mathbf{A_v}$		2.1	2.12	2.12	2.1	2.1
NM(mV)		139.6	139.5	139.6	141.2	140.7
Simulation Conditions: $A_v = 4$, $V_{swing} = .4V$, $C_L = 50$ fF, $I_{SS} = 10\mu$						
$\mathbf{V_{swing}(mV)}$		384	381	342	380	377
$\mathbf{A_v}$		2.09	2.12	2.13	2.1	2.1
NM(mV)	Traditional	139.57	142.28	140.1	135.4	137.8

Table 2.6 Effect of process variation on the delay of the traditional MCML based D-latch

Parameter	NMOS PMOS	T T	F F	S S	F S	S F
Simulation Conditions: $A_v = 4$, $V_{swing} = .4V$, $C_L = 50$ fF, $I_{SS} = 100\ \mu A$						
$\mathbf{t_{PD}(ps)}$		142.3	113.4	172.5	127	138.6
Simulation Conditions: $A_v = 4$, $V_{swing} = .4V$, $C_L = 50$ fF, $I_{SS} = 10\mu A$						
$\mathbf{t_{PD}(ps)}$		385.57	372.46	403.24	392.16	396.7

2.5 Minimum Power Supply for MCML based D-Latch:

This MCML based D-latch consist of two series stacked NMOS devices as shown in Fig. 2.8. Therefore, the main disadvantages of this scheme are

- The delay is also quite large as it includes load capacitance of both of the stacked transistors.
- This would require high voltage supply V_{DD} to keep both the stacks and bias current transistor in saturation for proper working. And hence, power dissipation is quite high in two series stacked D-Latch. The minimum supply required for proper working of D-latch can be calculated as[13]

$$V_{DD\_min} = V_{DS,source_{LVT}} + V_{DS,1_{LVT}} + V_{GS,3} \tag{2.16}$$

Where $V_{DS,source_{LVT}}$, $V_{DS,1_{LVT}}$ and $V_{GS,3}$ represents drain-source saturation voltage of bias current transistor and M_1 and gate-source voltage of the corresponding transistor M_3 in Fig. 2.8, respectively. In general drain-source saturation voltage, $V_{DS_{LVT}}$ is expressed as

$$V_{DS_{LVT}} = V_{GS} - V_{th} \tag{2.17}$$

Where V_{th} represents the threshold voltage of the transistor. In the saturation region, V_{GS} can be expressed as

$$V_{GS} = \sqrt{\frac{I}{K}} + V_{th} \tag{2.18}$$

Where I is the current flowing through the transistor and K is the parameter in the process-transconductance and the aspect ratio of the device Thus, $V_{DS_{LVT}}$ can be written as

$$V_{DS_{LVT}} = \sqrt{\frac{I}{K}} \tag{2.19}$$

Taking $I_{SS} = I_1 = I_3$ for the conducting case and $K_1 = K_3 = K$, and hence, using eq. (2.17-2.19) eq. (2.16) can be written as

$$V_{DD\_min} = \sqrt{\frac{I_{SS}}{K_{source}}} + \sqrt{\frac{I_1}{K_1}} + \sqrt{\frac{I_3}{K_3}} + V_{th,3} \tag{2.20}$$

$$= \sqrt{I_{SS}}\left(\frac{1}{\sqrt{K_{source}}} + \frac{2}{\sqrt{K}}\right) + V_{th,3}$$

$$= \sqrt{K_{source}(V_{bias} - V_{th})^2}\left(\frac{1}{\sqrt{K_{source}}} + \frac{2}{\sqrt{K}}\right) + V_{th,3}$$

$$= (V_{bias} - V_{th,source})\left(1 + \frac{2\sqrt{K_{source}}}{\sqrt{K}}\right) + V_{th,3}$$

$$\approx 3V_{bias} - 3V_{th,source} + V_{th,3} \qquad (2.21)$$

Where $V_{th,source}$ and $V_{th,3}$, are the threshold voltages of bias current source transistor and M_3 respectively. Here, it can be seen from eq. (2.21), that if somehow we can reduce the stack of the transistor, we can decrease the minimum power supply and hence the power dissipation of the circuit. With this triple-tail MCML based D-latch comes into the scenario presented by K. Gupta et. al [14], which will be studied in next chapter.

Chapter 3

Triple-tail MCML based D-latch

The triple-tail MCML based D-Latch proposed in [14] with differential inputs D and CLK is shown in Fig. 3.1. It consists of two current sources of $I_{SS}/_2$ value biasing the two triple-tail assembled by transistors (M_{LV4},M_{LV4} , M_{LV7}) and (M_{LV5},M_{LV6} , M_{LV8}). Differential CLK input drives the transistors M_{LV7} and M_{LV8} and are connected between the supply terminal and the common source terminal of transistor pairs $M_{LV4} - M_{LV4}$ and $M_{LV5} - M_{LV6}$ respectively. The transistor M_{LV8} is switched on by a high differential CLK voltage, and thus the transistor pair $M_{LV5} - M_{LV6}$ is deactivated. At the same time, the transistor M_{LV7} turns off so that the output is generated by transistor pair $M_{LV4} - M_{LV4}$ according to the differential input D. Similarly, the transistor pair $M_{LV4} - M_{LV4}$ gets activated for low differential CLK voltage and restores the previous output and thus the latch, for low differential CLK, operates in hold stage. For proper operation, aspect ratios of transistors M_{LV7} and M_{LV8} is made larger (N times) than the other transistors [14].

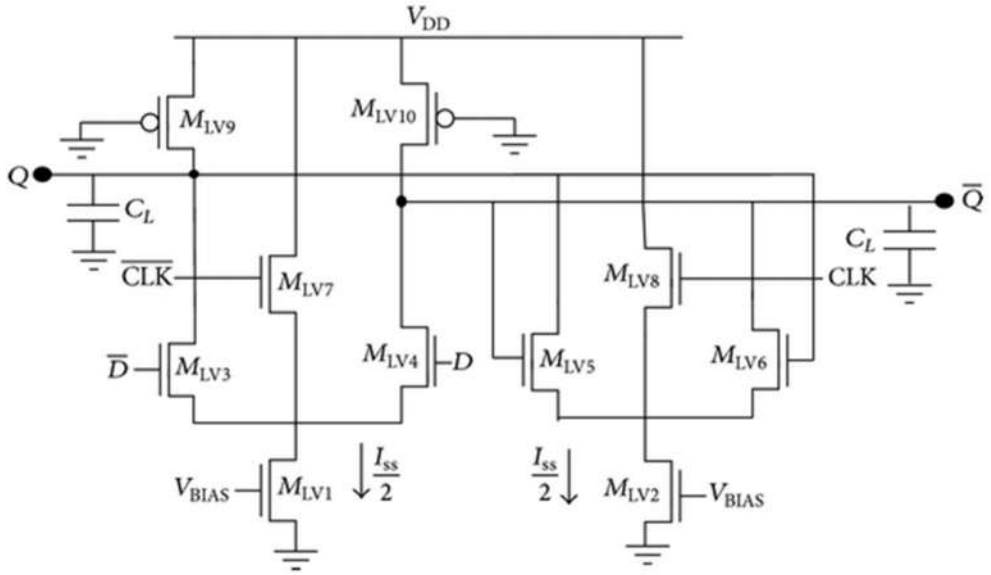


Fig. 3.1 Triple-tail MCML based D-Latch

The minimum supply voltage, $V_{DD\_MIN\_LV}$ for the triple-tail MCML based D-Latch is computed by the method outlined in [11] as

$$V_{DD\_MIN\_LV} = 2V_{BIAS} + V_{T1} - 2V_T \quad (3.1)$$

WhereV_{T1} is the threshold voltage of transistors$M_{LV4,4,5,6}$, V_T is the threshold voltage of M_{LV1} and V_{BIAS} is the biasing voltage of M_{LV1}. Here, we can see that the minimum supply voltage required for proper working of the latch is less than the supply voltage required (eq. 2.21). Hence, this scheme dissipates less power as compared to traditional MCML based D-Latch studied in chapter 2.

3.1 Analysis of the triple-tail MCML based D-latch:

As it can be observed that if all the transistors in triple tail in Fig. 3.1 have equal aspect ratios , then the transistors M_{LV7} and M_{LV8} will not be able to completely switch off the transistor pair $M_{LV4} - M_{LV4}$ and $M_{LV5} - M_{LV6}$. And hence for proper operation we have taken the aspect ratios of tail-transistors in Fig. 3.1 ($M_{LV7,8}$) larger than the aspect ratios of other transistors of pull-down network ($M_{LV4,4,5,6}$). The detailed analysis of impact of larger area of the tail transistors in Fig. 3.1, on the circuit operation, is studied in this section

.

3.1.1 Static Analysis:

The static model is derived by modeling the load transistorsM_{LV9}, M_{LV10} by an equivalent linear resistance, R_P [6]. The linear resistance, R_P is computed by using the standard BSIM3v3 model, as

$$R_P = \frac{R_{int}}{1-\frac{(R_{DSW}*10^{-6})/W_P}{R_{int}}} \tag{3.2}$$

where R_{DSW} is the empirical model parameter and the parameter R_{int} is the intrinsic resistance of the PMOS transistor in the linear region and is given as

$$R_{int} = [\mu_{eff,p} C_{ox} \frac{W_P}{L_P} (V_{DD} - |V_{TP}|)]^{-1} \tag{3.3}$$

where C_{ox} is the oxide capacitance per unit area and the parameters $\mu_{eff,p}$ is effective hole mobility, V_{TP} is the threshold voltage, W_P and L_P the effective channel width and effective channel length of the load transistor.

As it can be observed that if all the transistors in triple tail in Fig.3.1 have equal aspect ratios [14], then the transistors M_{LV7} and M_{LV8} will not be able to completely switch off the transistor pair $M_{LV4} - M_{LV4}$ and $M_{LV5} - M_{LV6}$. Hence, the aspect ratios of transistors M_{LV7} and M_{LV8} is kept larger than other transistors' aspect ratios by a factor of *N* the linear resistance,

R_P is computed. For, high differential input at D and low differential input at CLK, the transistors M_{LV4} and M_{LV7} have the same gate-source voltages, then for this input condition, currents flowing through M_{LV4} and M_{LV7} can be written as

$$i_{D,LV4} = \frac{\mu_{eff,n} C_{ox}}{2} \frac{W_N}{L_N} (V_{GS} - V_{T1})^2 \quad (3.4a)$$

$$i_{D,LV7} = \frac{\mu_{eff,n} C_{ox}*N}{2} \frac{W_N}{L_N} (V_{GS} - V_{T1})^2 \quad (3.4b)$$

Also, the sum of the drain currents of M_{LV4} and M_{LV7} will be constant i.e.

$$i_{D,LV4} + i_{D,LV7} = \frac{I_{SS}}{2} \quad (3.4c)$$

Solving the above equations for $i_{D,LV4}$ and $i_{D,LV7}$, we get the following results

$$i_{D,LV4} = \frac{I_{SS}}{2} \frac{1}{N+1} \quad (3.5a)$$

$$i_{D,LV7} = \frac{I_{SS}}{2} \frac{N}{N+1} \quad (3.5b)$$

The current $i_{D,LV4}$, i.e. the current through transistor M_{LV4}, can be increased by increasing its area , that is by increasing the factor N. The input condition high differential input at D and high differential input at CLK , produces minimum output voltage, represent as V_{OL1} as

$$V_{OL1} = V_Q - \overline{V_Q}$$

$$= R_P\left[(i_{D,4} + i_{D,6}) - (i_{D,3} + i_{D,5})\right] \quad (3.6)$$

$$= -\frac{R_P I_{SS}}{2}\left(1 + \frac{1}{N+1}\right) \quad (3.7)$$

For another input condition, when differential signals -clock signal CLK is low, D is high and previous state is low then

$$V_{OL2} = V_Q - \overline{V_Q}$$

$$= R_P\left[(i_{D,4} + i_{D,6}) - (i_{D,3} + i_{D,5})\right]$$

$$= -\frac{R_P I_{SS}}{2}\left(\frac{N}{N+1}\right) \quad (3.8)$$

Where $i_{D,3}$, $i_{D,4}$, $i_{D,5}$and $i_{D,6}$are the currents through transistors M_{LV3}, M_{LV4}, M_{LV5} and M_{LV6}, respectively. The Output in the form of differential voltage can be either V_{OH} or V_{OL}, depending for various input combination when applied to D-latch proposed in [14], which are enlisted in Table 3.1.

Table 3.1 Output in the form of differential voltage for various input combination when applied to triple-tail based MCML D-latch

Differential Inputs		**Present State**	**Current through the transistors**						**Differential output**
CLK	**D**	**Q**	$\mathbf{M_{LV3}}$	$\mathbf{M_{LV4}}$	$\mathbf{M_{LV5}}$	$\mathbf{M_{LV6}}$	$\mathbf{M_{LV7}}$	$\mathbf{M_{LV8}}$	$\mathbf{V_Q - \overline{V_Q}}$
L	L	L	I_3	0	I_1	0	I_2	0	V_{OL1}
L	L	H	I_3	0	0	I_1	I_2	0	V_{OH2}
L	H	L	0	I_3	I_1	0	I_2	0	V_{OL2}
L	H	H	0	I_3	0	I_1	I_2	0	V_{OH1}
H	L	L	I_1	0	I_3	0	0	I_2	V_{OL2}
H	L	H	I_1	0	0	I_3	0	I_2	V_{OL2}
H	H	L	0	I_1	I_3	0	0	I_2	V_{OH2}
H	H	H	0	I_1	0	I_3	0	I_2	V_{OH1}

Here $I_1 = \frac{I_{SS}}{2}$, $I_2 = \frac{I_{SS}}{2}\frac{N}{N+1}$ and $I_3 = \frac{I_{SS}}{2}\frac{1}{N+1}$.

(a) Voltage Swing:

Hence, from table 3.1 one voltage swing of the circuit, when input and output are same, can be expressed as

$$V_{SWING1} = V_{OH1} - V_{OL1} = R_P\left(1 + \frac{1}{N+1}\right) \quad (3.9a)$$

Where $V_{OH1}\ and\ V_{OL1}$, for same input and output, are the maximum and minimum output voltage respectively. For different input and output, other voltage swing of the circuit can be calculated as

$$V_{SWING2} = V_{OH2} - V_{OL2} = R_P\left(\frac{N}{N+1}\right) \quad (3.9b)$$

Where $V_{OH2}\ and\ V_{OL2}$, for same input and output, are the maximum and minimum output voltage respectively.

As it can be seen that $V_{SWING2} < V_{SWING1}$, considering the pessimism here, we can consider the swing of the latch as V_{SWING2} i.e.

$$V_{SWING} = R_P\left(\frac{N}{N+1}\right) \quad (3.9c)$$

Table 3.2 Voltage swing of triple-tail MCML based D-Latch

$I_{SS}(\mu A)$	Voltage Swing (in mV)	Error(in %)
20	380.25	4.93
50	390.12	2.47
80	387.24	3.15

For 400mV voltage swing, 50µA bias current, N=5, 400mC voltage swing and 4 voltage gain, transient analysis of triple-tail MCML based D-latch is shown in Fig. 3.2, where when clock is 1, data is transferred at output and when clock is 0, previous output is maintained as current output of the latch, with the total simulated voltage swing came out to be 390.124mV with error of 2.47% between the predicted and simulated results.

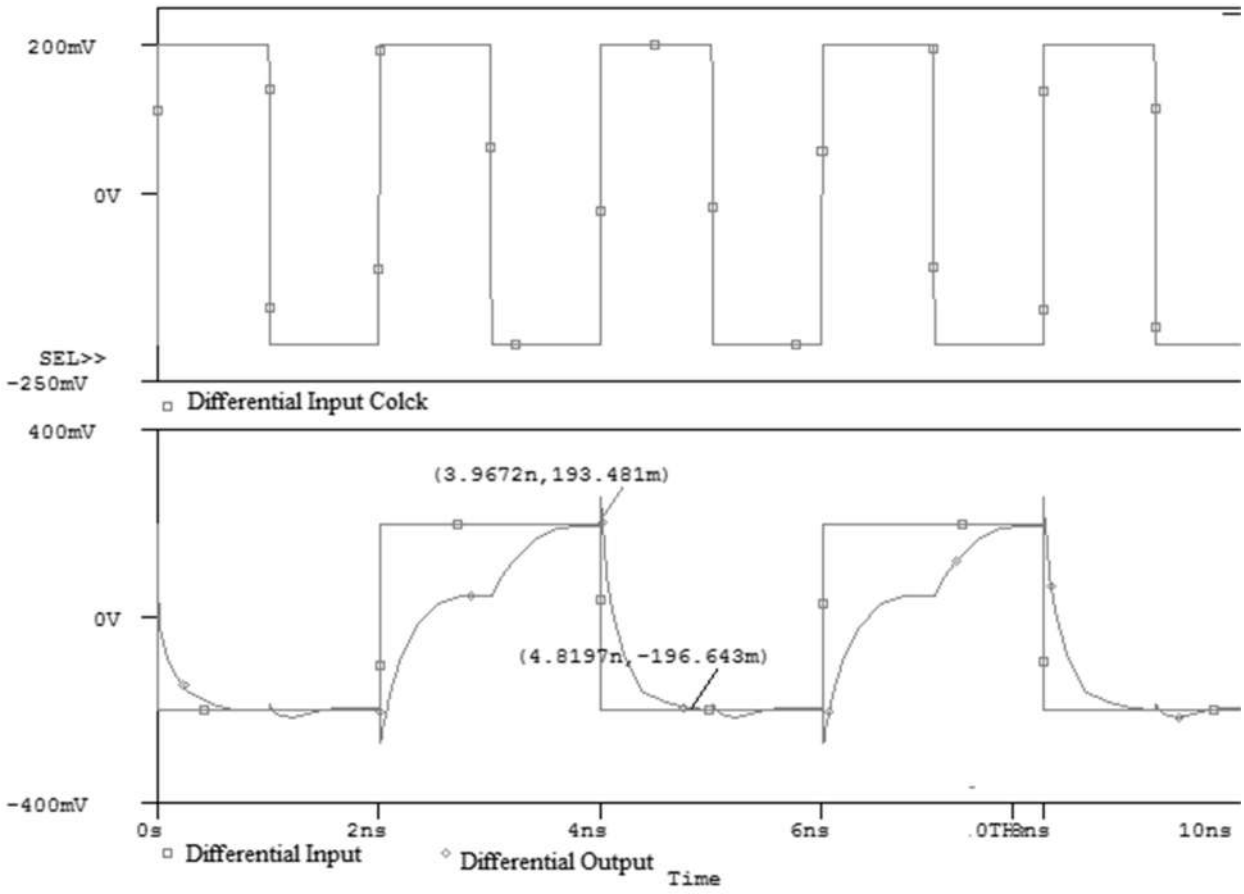


Fig. 3.2 Output and voltage swing of triple-tail MCML based D-latch

(b) *Voltage-Gain*:

The small-signal voltage gain (A_v) and noise margin (NM) for the triple-tail MCML D-latch are computed as

$$A_v = g_{m,n}R_P = \frac{N+1}{N}\frac{V_{SWING}}{2}\sqrt{2\mu_{eff,n}C_{OX}\frac{W_N}{L_N}.\frac{1}{I_{SS}}} \tag{3.10}$$

$$NM = \frac{V_{SWING}}{2}\left[1-\frac{\sqrt{2}}{A_v}\right] \tag{3.11}$$

Where $\mu_{eff,n}$,$g_{m,n}$,W_N and L_N are the effective electron mobility, the transconductance, the effective channel width and length of transistors$M_{LV4,4,5,6}$ respectively.

triple-tail MCML based D-latch has been simulated for 50µA bias current, N=5, 400mV voltage swing and gain 4, AC analysis of which is shown in Fig. 3.3. It can be seen that there is a close relation between simulated and predicted voltage gain .

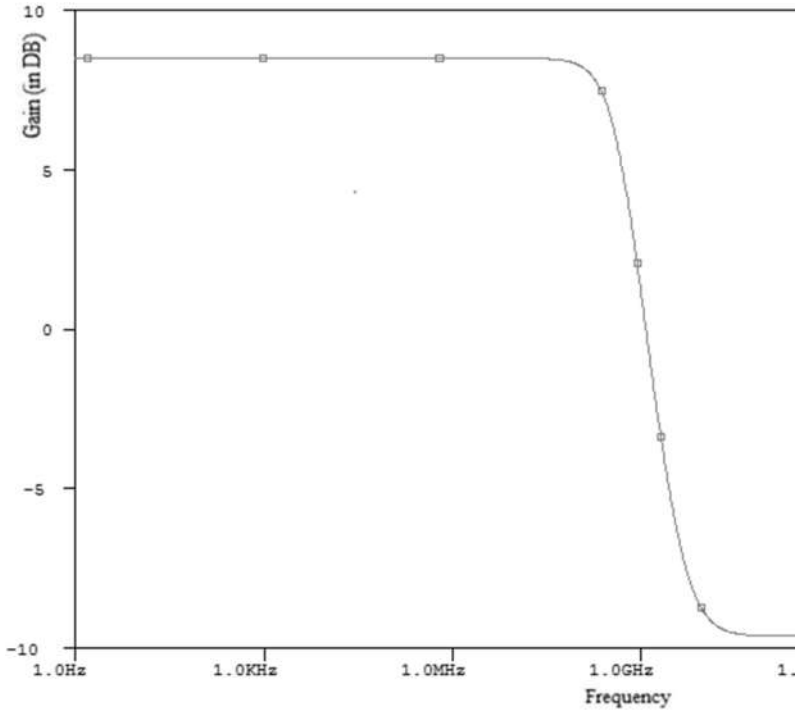


Fig. 3.3 AC analysis of triple-tail MCML D-Latch

3.1.2 Delay Model

In case of a low-to-high transition on CLK input that causes switching at the by activating (deactivating) the transistor pair $M_{LV4} - M_{LV4}$ ($M_{LV5} - M_{LV6}$), and hence, the circuit reduces to a simple MCML inverter. The equivalent linear half circuit is shown in Fig. 3.4 where C_{gdi} and C_{dbi} represents the gate–drain capacitance and the drain–bulk junction capacitance of the ith

transistor. For NMOS transistors operating in saturation region, C_{gd} is equal to the overlap capacitance $C_{gdo}W_n$ between the gate and the drain [6]. C_{input} is the input capacitance of the source-coupled pair ($M_{LV5} - M_{LV6}$) .For the PMOS transistor operating in linear region, C_{gd} is evaluated as the sum of the overlap capacitance and the intrinsic contribution associated with its channel charge [6].

The delay of the triple-tail based MCML D-latch can be expressed as

$$t_{PD} = 0.69\, R_P\, (C_{db3} + C_{gd3} + C_{gd9} + C_{db9} + C_{db5} + C_{gd5} + C_L + C_{input}) \qquad (3.12)$$

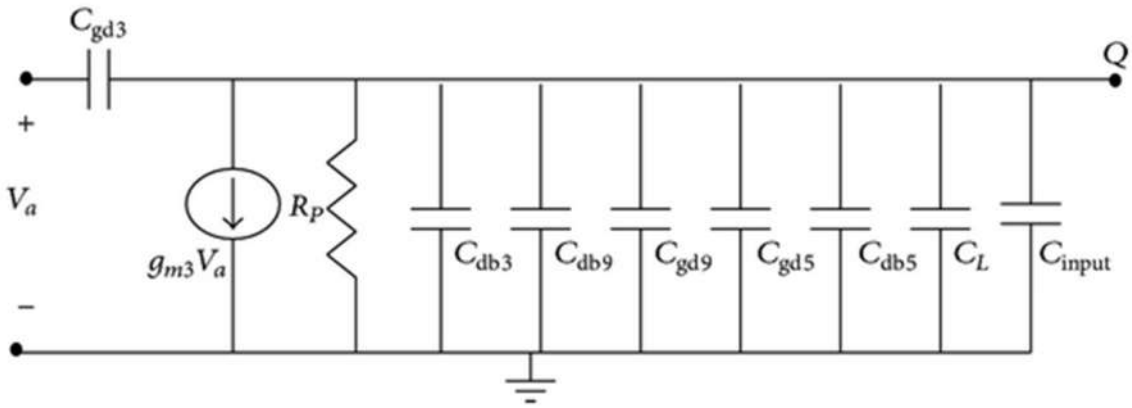


Fig. 3.4 Linear Half-circuit (with low value of differential input A)

where $C_{db3} = C_{db5}$, $C_{gd3} = C_{gd5}$ and, $R_P = \frac{N+1}{N}\frac{V_{SWING}}{I_{SS}}$, Eq.(3.12) can be rewritten as

$$t_{PD} = 0.69\, \frac{N+1}{N}\frac{V_{SWING}}{I_{SS}}\, (2C_{db3} + 2C_{gd3} + C_{gd9} + C_{db9} + C_L + +C_{input}) \qquad (3.13)$$

3.2 Design of triple-tail based MCML D-latch:

In this section, with the help of static model studied in previous section, sizing of load and differential pair transistors has been done first, and then the delay model is discussed in detail and expressed in terms of design parameters required for designing the gate i.e. bias current and voltage swing. This can be further used for trade-off between delay and power.

3.2.3 Design of the Differential pair and load transistors :

On the basis of static model, an approach is studied to size the transistors of the triple-tail based MCML D-latch gate in this section. For a specified value of NM, factor N and Av (≥1.4 for MCML [8]), calculation of the voltage swing of the triple-tail based MCML D-latch is done using Eq.(3.11) as

$$V_{SWING} = \frac{2NM}{1-\frac{\sqrt{2}}{A_V}} \tag{3.14}$$

It may be noted that V_{SWING} should be lower than the maximum value of $2V_{T1}$ so as to ensure that transistors $M_{LV4,4,5,6}$ operates in saturation region. The voltage swing obtained from Eq.(3.14) requires sizing of the load transistor with equivalent resistance R_P

$$R_P = \frac{N+1}{N}\frac{V_{SWING}}{I_{SS}} \tag{3.15}$$

To this end, first for the minimum sized PMOS, the equivalent resistance, R_{P_MIN}, is determined and then for the required voltage swing, the bias current I_{HIGH} is determined as

$$I_{HIGH} = \frac{V_{SWING}}{R_{P\_MIN}} \tag{3.16}$$

If the bias current is higher than I_{HIGH}, then R_P should be less than R_{P_MIN} and to achieve this L_P is set to its minimum value i.e. L_{MIN} and W_P which is calculated by solving Eq.(3.2) and (3.3) as

$$W_P = \frac{N}{N+1}\frac{I_{SS}}{V_{SWING}} * \frac{L_{MIN}}{\left[\mu_{eff,p}C_{ox}\frac{W_P}{L_P}(V_{DD}-|V_{TP}|)\right]1-\frac{(R_{DSW}X10^{-6})}{L_{MIN}}\left[\mu_{eff,p}C_{ox}\frac{W_P}{L_P}(V_{DD}-|V_{TP}|)\right]} \quad (3.17)$$

Similarly, if the bias current is lower than I_{HIGH}, then R_P should be greater than R_{P_MIN} and to achieve this W_P is set to its minimum value i.e. W_{MIN} and L_P which is calculated by solving Eqs. (3.2) and (3.3) as

$$L_P = \mu_{eff,p}C_{ox}W_{MIN}(V_{DD}-|V_{TP}|)\left(\frac{N+1}{N}\frac{V_{SWING}}{I_{SS}} - \frac{R_{DSW}*10^{-6}}{W_{MIN}}\right) \quad (3.18)$$

For the sizing of transistors $M_{LV4,4,5,6}$, the small-signal voltage gain A_v (Eq.(3.10)) has been used. The width, for minimum sized transistors, can be computed as

$$W_N = 2\left(\frac{A_v}{V_{SWING}}\right)^2\left(\frac{N}{N+1}\right)^2\frac{L_{MIN}I_{SS}}{\mu_{eff,n}C_{ox}} \quad (3.19)$$

In table 3.4, using above design methodology presented in [14], sizing of NMOS transistors and load transistors have been tabulated for different values of bias current.

Table 3.3 Sizing of transistors and load resistance for different bias current for triple-tail MCML based D-latch

$I_{SS}(\mu A)$	R_P (in KΩ)	W_n/L_n	$W_n/L_n * N$
20	24	11.11	55.55
50	9.6	27.78	138.9
80	6	44.45	222.25

Chapter 4

Threshold-Voltage Fluctuation and MCML Circuits

With the scaling of MOSFET device, for reliability and also to keep power dissipation in check, supply voltage is also scaled down. And because of this continuous scaling, the system is becoming more and more sensitive to device characteristics fluctuation. In deep-submicron (DSM) technologies, where the size of the MOSFET transistors shrink, because of variations related to process in the gate length, gate-oxide thickness and channel dopant's random placement, causes the fluctuation in the threshold voltage (V_{th}) of the MOSFET. This fluctuation can result in malfunction of the circuit operation because of transistor mismatching and reduced voltage-swing.

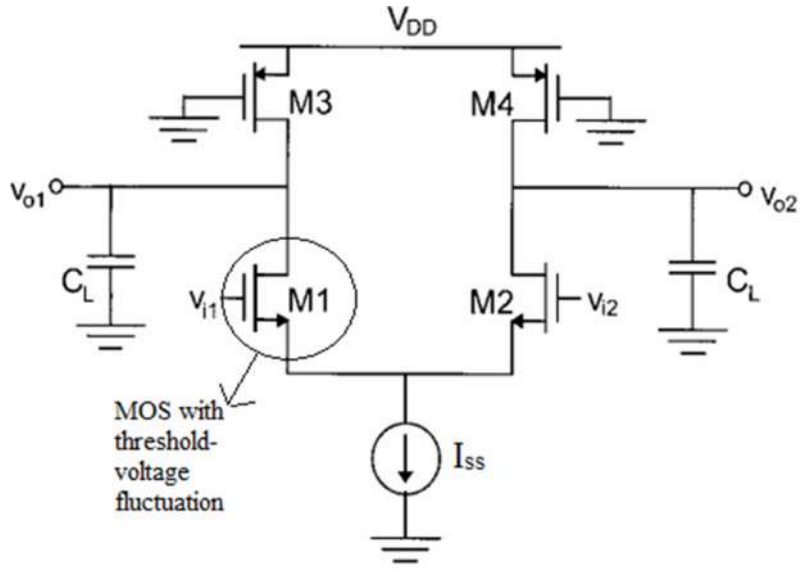
Among these sources of fluctuation, the random placement of channel dopants is chief as it cannot be reduced by simply improving the process technology. Also, its impact increases as the device shrinks which is inevitable and quite a necessity for today's portable devices. Hence, one possible solution to this problem can be completely removing the impurity in the channel. In this chapter, how threshold voltage fluctuation effects the MCML circuits have been studied and a simple solution presented in [10] has been studied and applied to triple-tail cell.

4.1 Effect of V_{th} Fluctuation among NMOS transistors in MCML inverter and MCML D-latch:

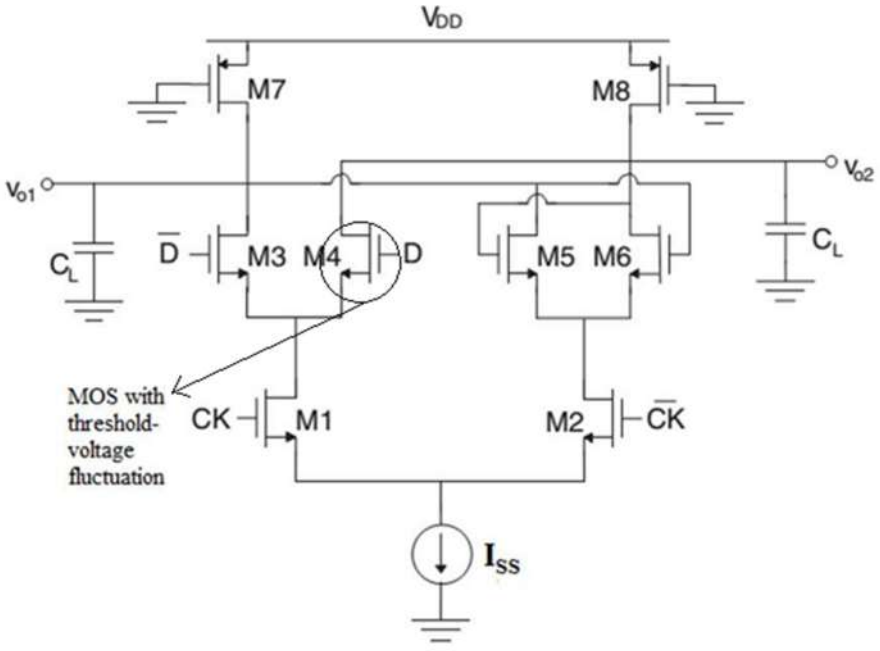
This has been studied in previous chapter that MOS Current Mode logic circuits are much faster than the static CMOS logic because of its small signal amplitude and smaller input capacitance and hence are capable of operating at much higher frequencies. But the voltage-threshold fluctuation reduces the maximum operating frequency. And as discussed, this problem of V_{th} fluctuation becomes more prominent with the decrease in device technology and hence becomes a major problem for deep-submicron (DSM) CMOS transistors.

This fluctuation is caused by fluctuation of the gate-length, gate oxide thickness, etc. V_{th} fluctuation is also caused by random placement of channel dopants, but its effect is not severe for the devices having large enough gate widths ($\geq 1\mu m$). As with the lowering of threshold-voltage, because of severe short channel effect, in deep-submicron region, because of fluctuation of gate length, V_{th} fluctuation becomes great.

If we consider an MCML inverter with threshold-voltage fluctuation, there can be two cases as shown in Fig. 4.1 and Fig. 4.4 that shows that device mismatching can occur in two forms i.e. mismatching in NMOS transistors or mismatching in PMOS transistors because of threshold-voltage fluctuation among the respective pair of transistors.



(a)



(b)

Fig. 4.1 Mismatching in NMOS transistors because of V_{th} Fluctuation (a) MCML inverter (b) MCML based D-latch

In this case because of threshold-voltage fluctuation, there is a difference between values of threshold voltages of NMOS differential pair transistors ($M_1 - M_2$) and therefore the output waveforms will be unbalanced. Fig. 4.2(a) and 4.2(b) shows output waveform with and without threshold voltage fluctuation. The effect of threshold voltage fluctuation is formulated with taking in consideration that the differential pair transistors operate in saturation region. Therefore, their drain currents can be written as [10]

$$I_D = \mu_n C_{ox} \frac{W}{L} \left(V_g - V_{th}\right)^2 \tag{4.1}$$

Where μ_n, C_{ox}, W and L are mobility, gate oxide capacitance, gate width and gate length of the transistor.

$$g_m = \frac{dI_D}{dV_g} = 2\mu_n C_{ox} \frac{W}{L} \left(V_g - V_{th}\right) \tag{4.2}$$

And change in drain current with respect to the change in threshold voltage can be expressed as

$$\frac{dI_D}{dV_{th}} = -2\mu_n C_{ox} \frac{W}{L} \left(V_g - V_{th}\right) = -g_m \tag{4.3}$$

And the DC gain of the MCML circuit i.e. G(0) is given by

$$\mathrm{G}(0) = g_m R_L \tag{4.4}$$

Here, R_L is the load resistance implemented by PMOS transistors (M_3 and M_4) and for small-signal analysis, input signal is assumed to be much smaller than V_g i.e. the gate voltage. If the threshold voltage fluctuation (ΔV_{th}) is also assumed to be much smaller than V_g, the the fluctuation in bias voltage can be formulated as

$$\Delta V_B = -\frac{dI_d}{dV_{th}} \Delta V_{th} R_L$$

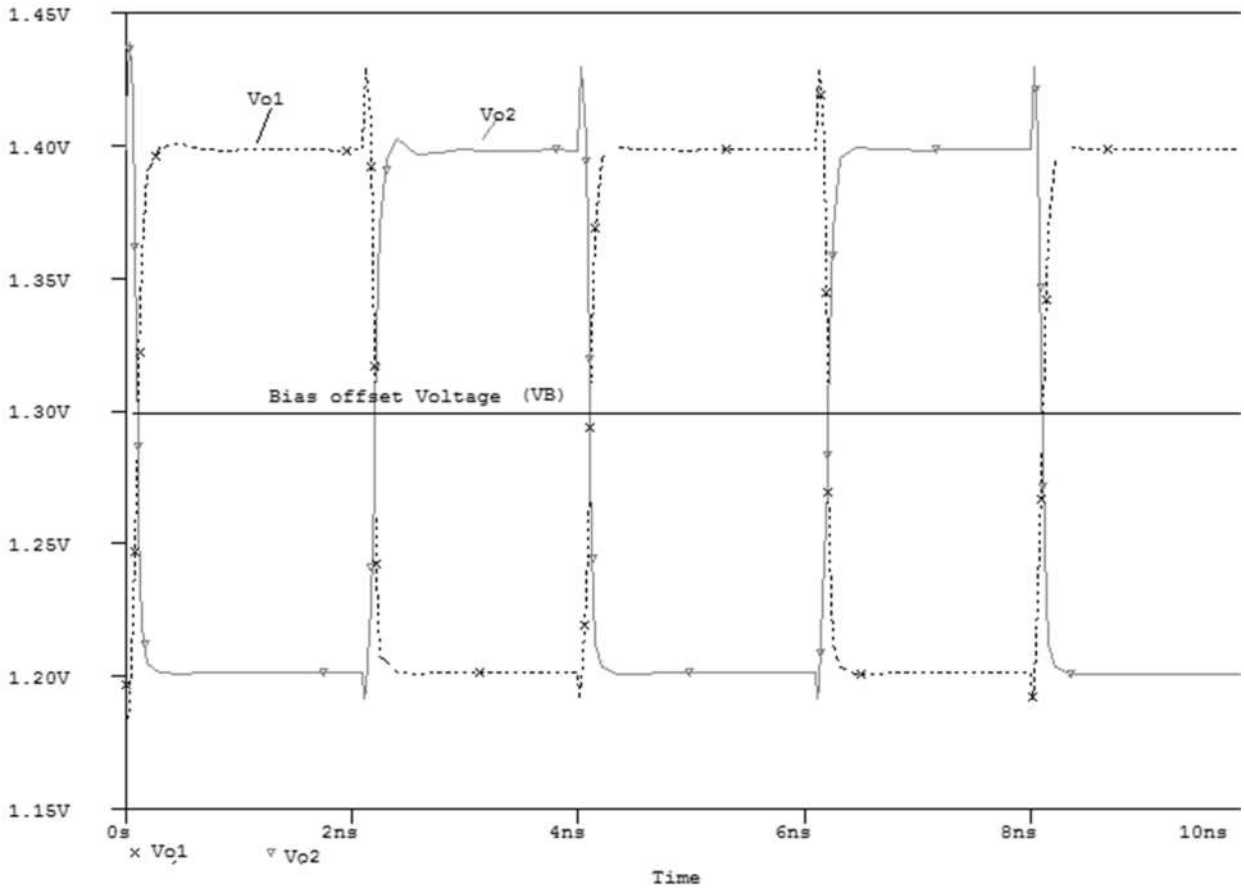
$$= g_m R_L \Delta V_{th} = G(0) \Delta V_{th} \tag{4.5}$$

As it can be seen from Fig. 4.2(b), that the minimum differential output voltage V_{MIN} decreases with increase in ΔV_B and hence will result in faulty operation of the circuit. So, a small DC gain is desirable for the circuit as from eq. (4.5), it can be seen that ΔV_B is directly proportional to DC gain of the circuit, to ensure there is much less fault because of threshold-voltage fluctuation in the circuit. Fig. 4.3 shows variations in ΔV_B with respect to the threshold-voltage fluctuation (ΔV_{th}). When there is no mismatching among transistors due to threshold voltage fluctuation, the output at both nodes have same bias-offset voltage as seen from Fig. 4.2a. But when there is mismatching among transistors due to threshold voltage fluctuation, the output at nodes have different bias-offset voltage as seen from Fig. 4.2b. Fig. 4.3 shows a close relationship between the calculated differences in bias-offset voltage and simulated bias-offset voltage for MCML inverter simulated for gain 4, 400mV voltage swing and 50μA bias current.

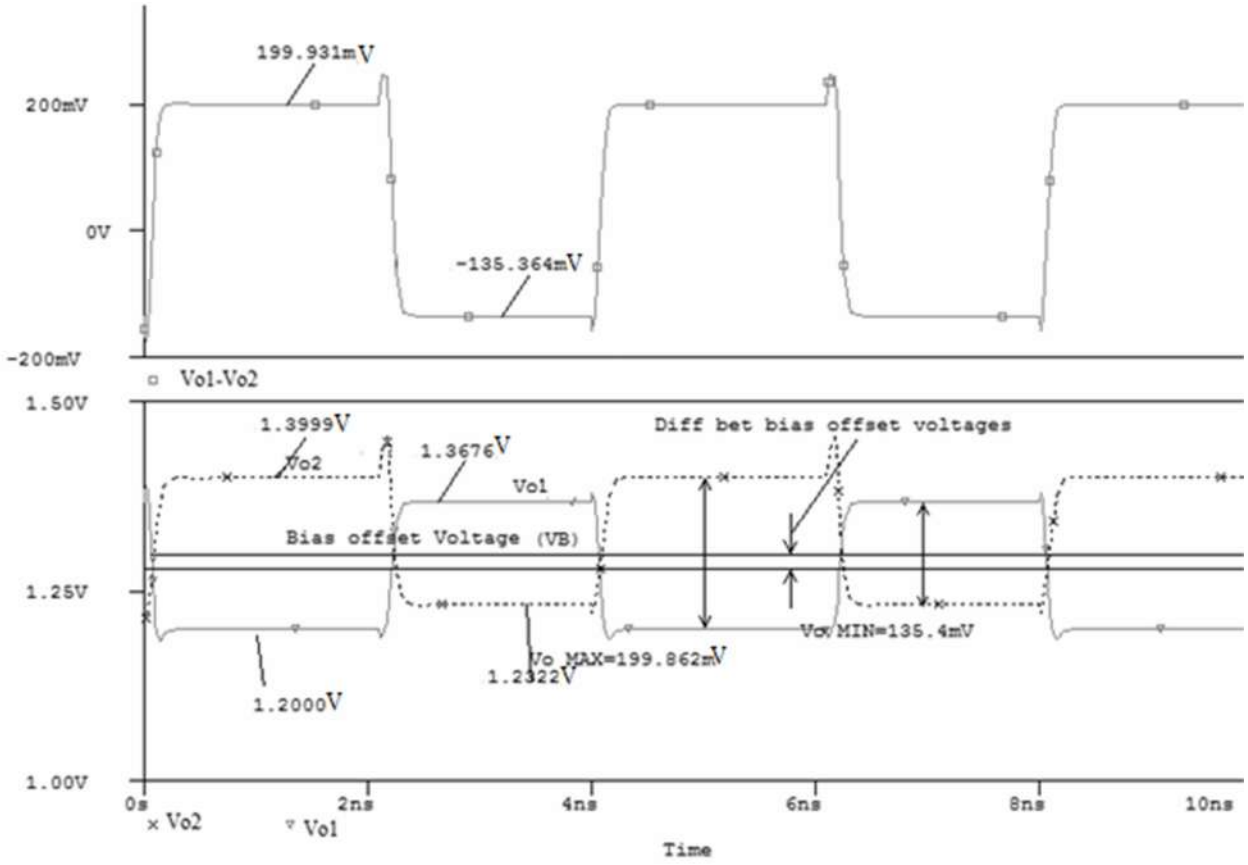
It may be noted that, because of device mismatch, there is difference in bias offset voltages of the output, and this also affected the required voltage swing of our circuit. When there is no mismatch, in Fig. 4.2a, the bias offset voltage of both outputs is as 1.3v, which is the common mode operating point of the circuit. But because of device mismatch among NMOS transistors, because of different threshold voltages, both have different driving capabilities and the have different bias offset voltages. One output has 1.3V, while the other output has bias offset voltage as 1.2834V, thus the difference between them come out to be .0165V, which is the amount of expense paid on swing because of threshold voltage fluctuation.

From Fig. 4.2 c, it can be observed that the swing of D-latch has also reduced because of threshold voltage fluctuation.

This can be observed from Fig. 4.3 that the more this fluctuation is, the more the operation of inverter gets affected, which basically results in less voltage swing than the expected value of 400mV.


1.45V
1.40V
1.35V
1.30V
1.25V
1.20V
1.15V
Vo1
Vo2
Bias offset Voltage (VB)
0s
2ns
4ns
6ns
8ns
10ns
× Vo1
▽ Vo2
Time

(a)


199.931mV
200mV
0V
-135.364mV
-200mV
Vo1-Vo2
1.50V
1.3999V
Vo2
1.3676V
Vo1
Diff bet bias offset voltages
Bias offset Voltage (VB)
1.25V
Vo MIN=135.4mV
Vo MAX=199.862mV
1.2322V
1.2000V
1.00V
0s
2ns
4ns
6ns
8ns
10ns
× Vo2
▽ Vo1
Time

(b)

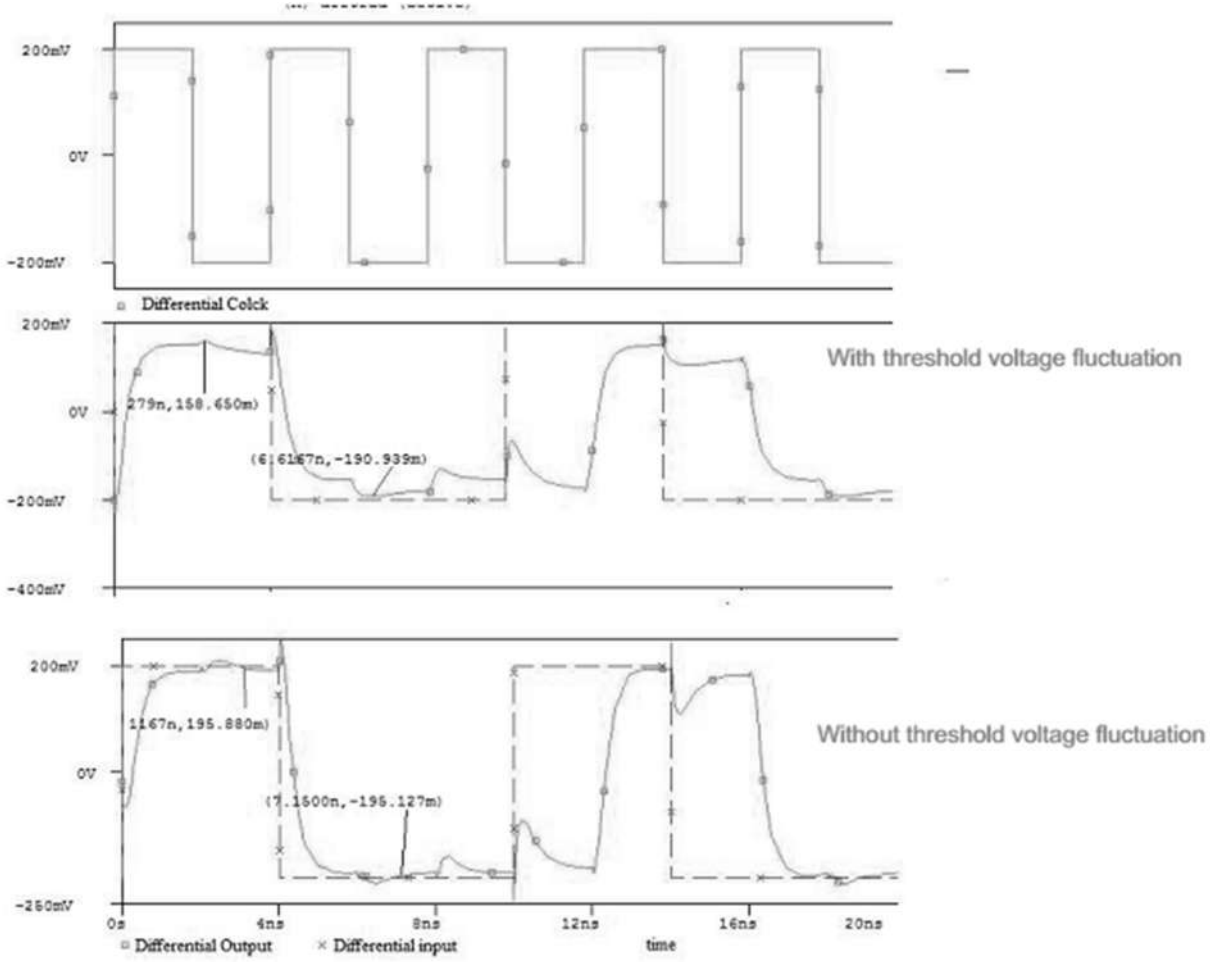


Fig. 4.2 MCML Inverter output waveforms (a) without threshold voltage fluctuation (b) with threshold voltage fluctuation among NMOS transistors. MCML based D-latch output waveforms (c) with and without threshold voltage fluctuation.

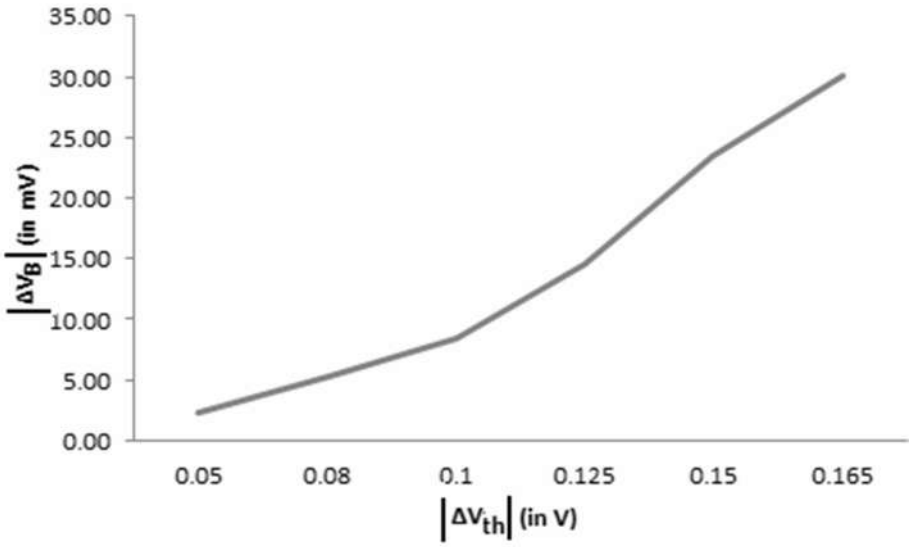


Fig. 4.3 Variations in ΔV_B with respect to the threshold-voltage fluctuation (ΔV_{th}).

4.2 Effect of V_{th} Fluctuation among PMOS transistors in MCML inverter and MCML D-latch:

Another case of threshold-voltage fluctuation is shown in Fig. 4.4 where there is mismatching among PMOS transistors and Fig. 4.5 shows the corresponding output waveform with threshold voltage fluctuation. Here, we already studied in previous chapter, that the linear resistance, R_P is computed [6] by using the standard BSIM3v3 model, as

$$R_P = \frac{R_{int}}{1-\frac{(R_{DSW}*10^{-6})/W_P}{R_{int}}} \tag{4.6}$$

where R_{DSW} is the empirical model parameter and the parameter R_{int} is the intrinsic resistance of the PMOS transistor in the linear region and is given as

$$R_{int} = [\mu_{eff,p} C_{ox} \frac{W_P}{L_P} (V_{DD} - |V_{TP}|)]^{-1} \quad (4.7)$$

where C_{ox} is the oxide capacitance per unit area and the parameters $\mu_{eff,p}$ is effective hole mobility, V_{TP} is the threshold voltage, W_P and L_P the effective channel width and effective channel length of the load transistor.

To study the effect of threshold-voltage fluctuation among PMOS transistors in MML inverters, We can proceed as shown in [10] and can derive it's effect. Hence, differentiating R_{int} with respect to threshold-voltage V_{TP}, we obtain

$$\frac{dR_{int}}{dV_{TP}} = \frac{d[\mu_{eff,p} C_{ox} \frac{W_P}{L_P} (V_{DD} - |V_{TP}|)]^{-1}}{dV_{TP}} \quad (4.8)$$

$$= \frac{1}{\mu_{eff,p} C_{ox} \frac{W_P}{L_P} (V_{DD} - |V_{TP}|)^2} \quad (4.9)$$

$$= \frac{R_{int}}{(V_{DD} - |V_{TP}|)} \quad (4.10)$$

Now, differentiating R_P with respect to threshold-voltage, it is computed as

$$\frac{dR_P}{dV_{TP}} = \frac{dR_P}{dR_{int}} \cdot \frac{dR_{int}}{dV_{TP}} \quad (4.11)$$

$$= \frac{\left(R_{int} - {(R_{DSW} * 10^{-6})}/{W_P}\right) * 2R_{int} - {R_{int}}^2}{\left(R_{int} - {(R_{DSW} * 10^{-6})}/{W_P}\right)^2} \cdot \frac{dR_{int}}{dV_{TP}}$$

Using eq. (4.10) and solving further, $\frac{dR_P}{dV_{TP}}$ is obtained as

$$\frac{d\mathrm{R_P}}{\mathrm{dV_{TP}}} = \frac{\left(R_{int} - {}^{2\left(R_{DSW}*10^{-6}\right)}/_{\mathrm{W_P}}\right)R_{int}}{\left(R_{int} - {}^{\left(R_{DSW}*10^{-6}\right)}/_{\mathrm{W_P}}\right)^2 (\mathrm{V_{DD}} - |\mathrm{V_{TP}}|)} \tag{4.12}$$

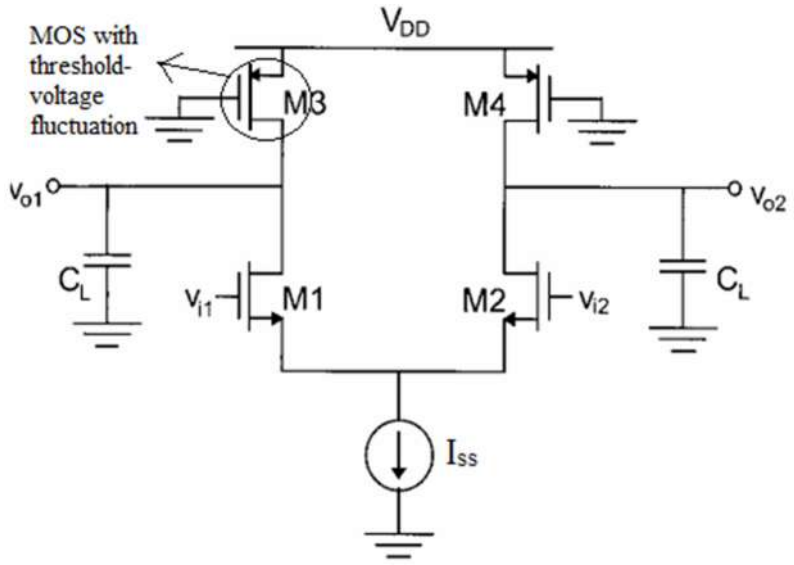
Here, all the symbols have their usual meaning. The bias offset voltage ΔV_B obtained for this case, can be formulated as

$$\Delta V_{B,p} = I_{SS}\Delta R_P$$

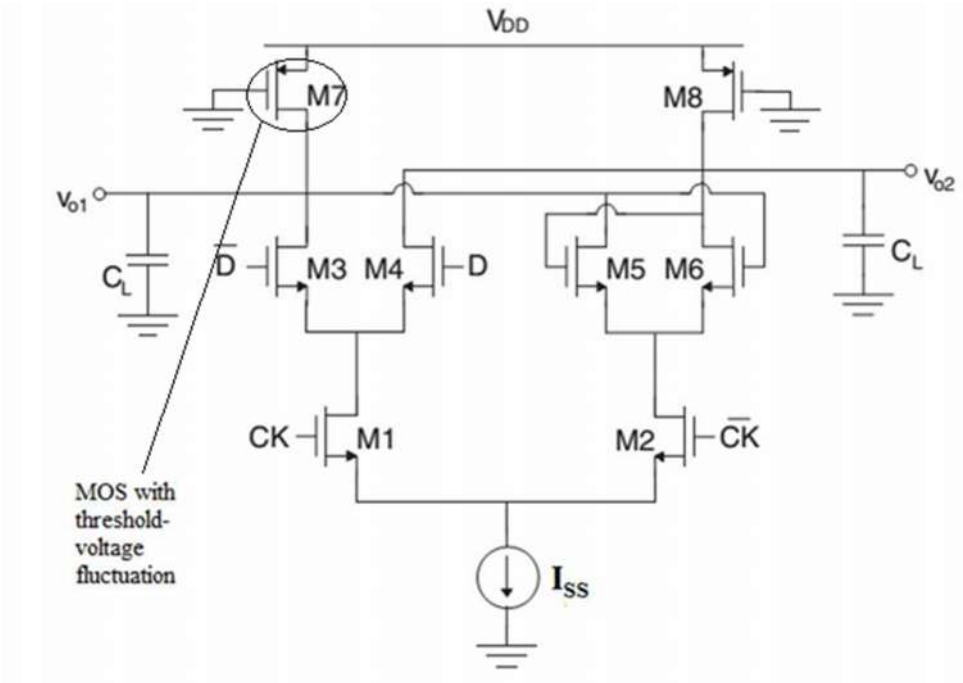
$$= I_{SS}\frac{d\mathrm{R_P}}{\mathrm{dV_{TP}}} \cdot \Delta V_{TP} \tag{4.13}$$

Using eq. (4.12), bias offset voltage ΔV_B is obtained as

$$\Delta V_{B,p} = I_{SS}\frac{\left(R_{int} - {}^{2\left(R_{DSW}*10^{-6}\right)}/_{\mathrm{W_P}}\right)R_{int}}{\left(R_{int} - {}^{\left(R_{DSW}*10^{-6}\right)}/_{\mathrm{W_P}}\right)^2 (\mathrm{V_{DD}} - |\mathrm{V_{TP}}|)} \cdot \Delta V_{TP} \tag{4.14}$$



(a)



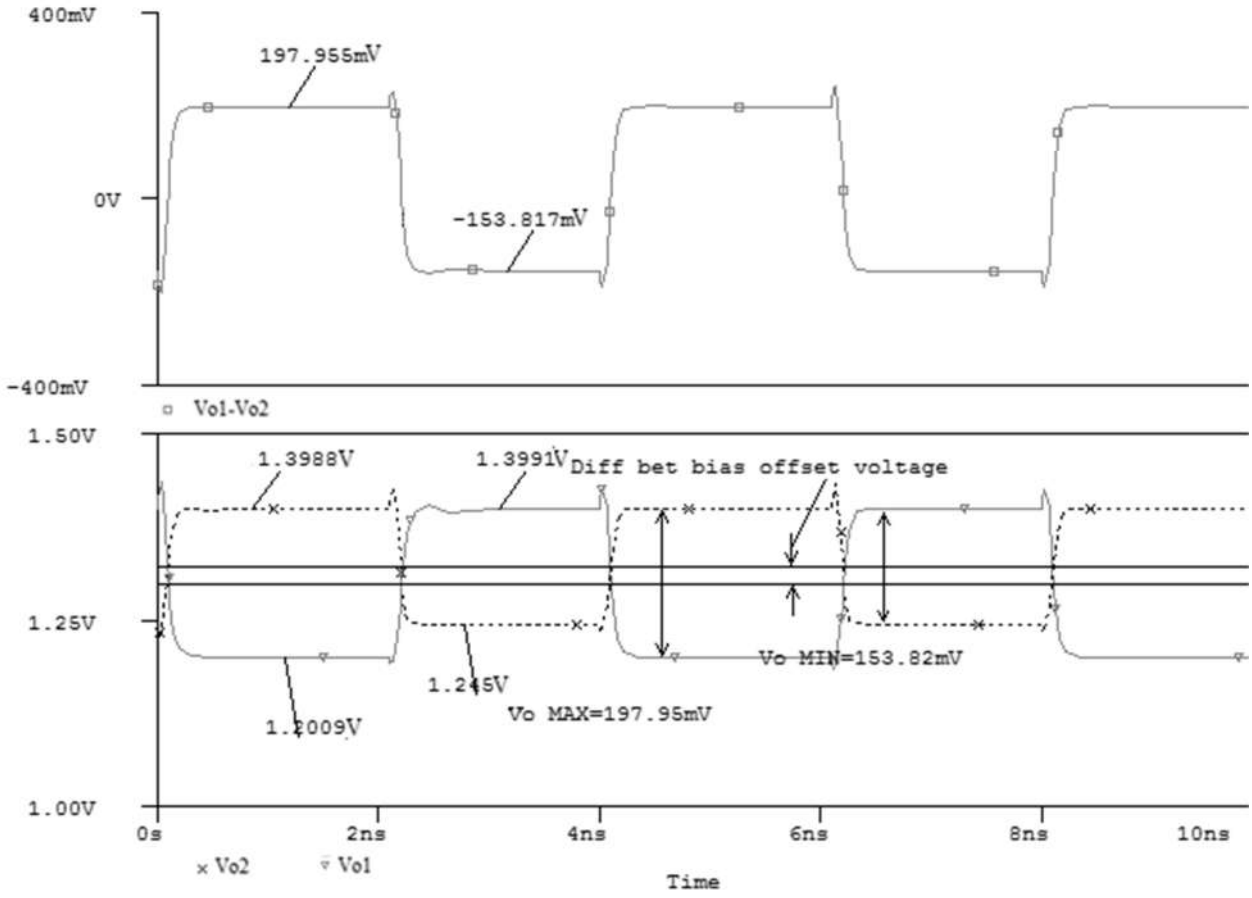
(b)

Fig. 4.4 Device mismatching because of threshold-voltage fluctuation in PMOS transistor in (a) MCML inverter (b) MCML based D-latch

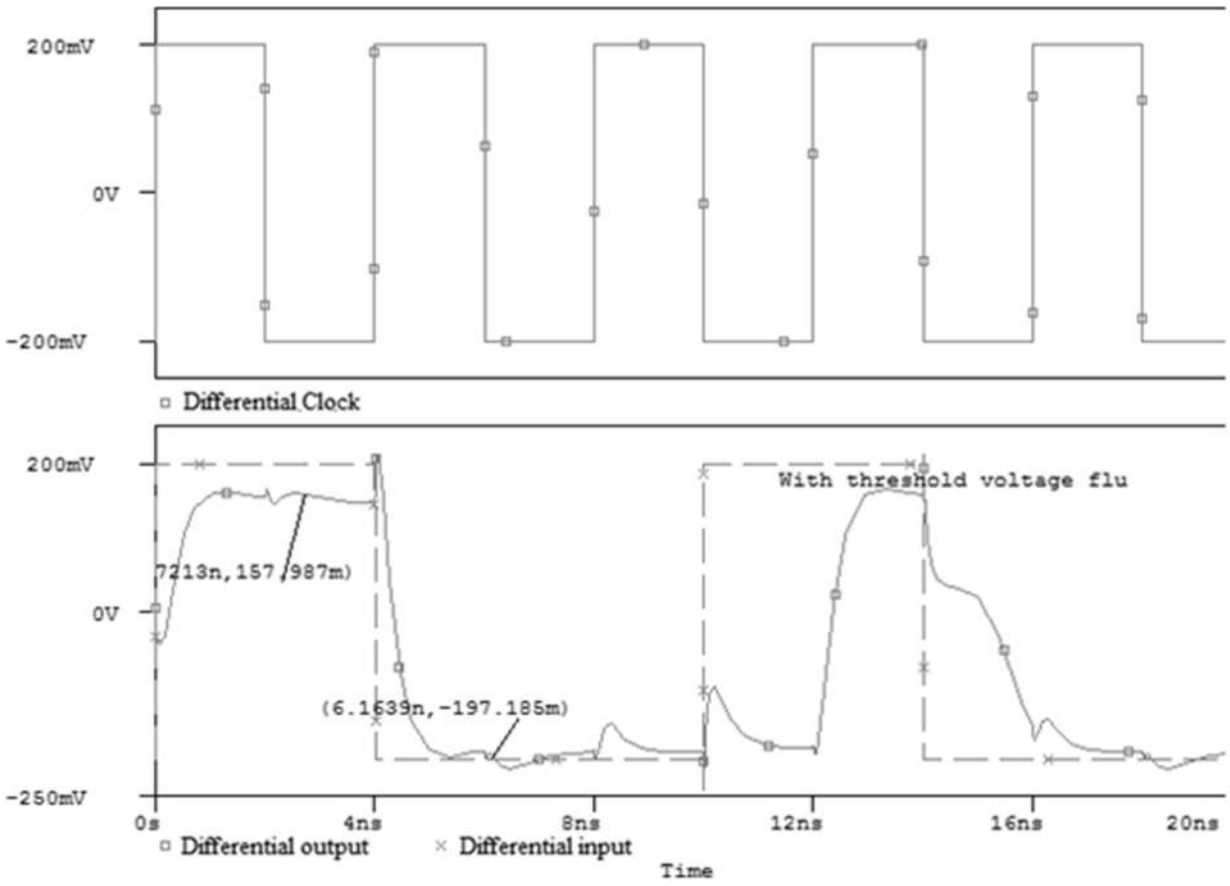
When there is mismatching among transistors due to threshold voltage fluctuation, the output at nodes have different bias-offset voltage as seen from Fig. 4.5 for MCML inverter simulated for gain 4, 400mV voltage swing and 50μA bias current.

It may be noted that, because of device mismatch, there is difference in bias offset voltages of the output, and this also affected the required voltage swing of our circuit. When there is no mismatch, in Fig. 4.2, the bias offset voltage of both outputs is as 1.3v, which is the common mode operating point of the circuit. But because of device mismatch among PMOS transistors, as shown in output in Fig. 4.5, because of different threshold voltages, both have different linear resistances and thus have different bias offset voltages. One output has 1.3V, while the other output has bias offset voltage as 1.3225V, thus the difference between them come out to be .0225V.

This can be observed from Fig. 4.6 that the more this fluctuation is, the more the operation of inverter gets affected, which basically results in less voltage swing than the expected value of 400mV.


400mV
197.955mV
0V
-153.817mV
-400mV
Vo1-Vo2
1.50V
1.3988V
1.3991V
Diff bet bias offset voltage
1.25V
Vo MIN=153.82mV
1.245V
Vo MAX=197.95mV
1.2009V
1.00V
0s
2ns
4ns
6ns
8ns
10ns
Vo2
Vo1
Time

(a)



(b)

Fig. 4.5 Output waveform with threshold voltage fluctuation among PMOS transistors in (a) MCML inverter (b) MCML based D-latch

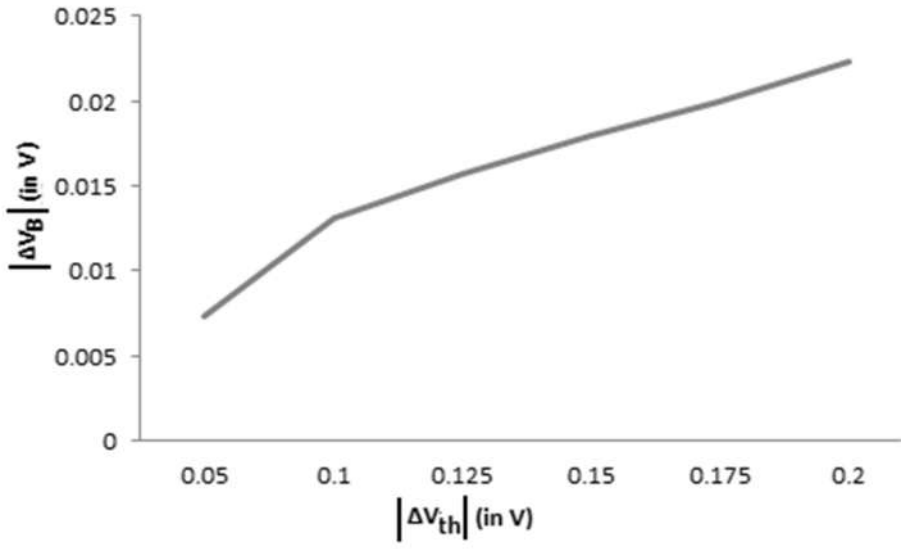


Fig. 4.6 Variations in ΔV_B with respect to the threshold-voltage fluctuation **(ΔV_{th}).**

4.3 Different cases of threshold voltage fluctuation:

As studied in previous section there can be four cases of threshold voltage fluctuation that can be present in the circuit.

- **Case 1:** This is the case when device mismatch among NMOS differential pair transistors due to threshold voltage fluctuation in NMOS transistor in the MCML inverter as shown in Fig. 4.4(a)

- **Case 2:** This is the case when device mismatch among PMOS active load transistors due to threshold voltage fluctuation in PMOS transistor in the MCML inverter as shown in Fig. 4.4(a)

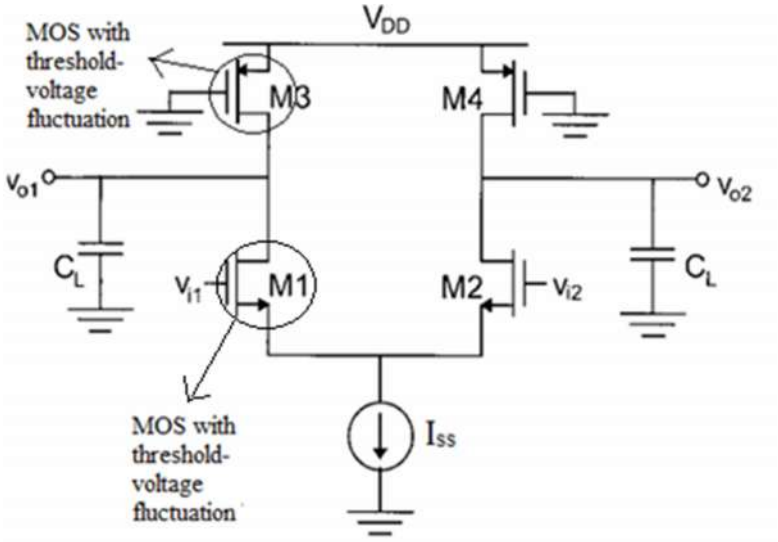
- **Case 3: :** This is the when device mismatch among both NMOS and PMOS transistors due to threshold voltage fluctuation in NMOS and PMOS transistor both occurs at the same branch of the MCML inverter as shown in Fig. 4.7(a)

- **Case 4: :** This is the when device mismatch among both NMOS and PMOS transistors due to threshold voltage fluctuation in NMOS and PMOS transistor occurs at the different branch of the MCML inverter as shown in Fig. 4.7(b)

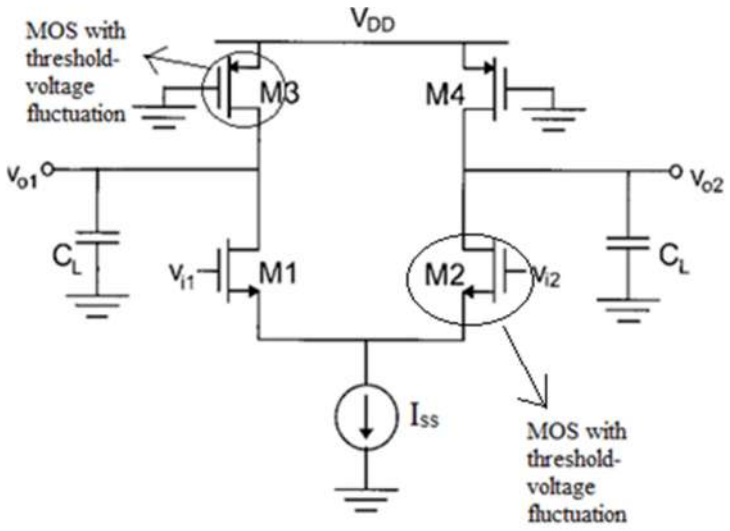
In case 3 and case 4, the effective change in bias voltage can be computed as sum of change in bias offset voltage due to individual transistors from eq. 4.5 and 4.14. From output, it may be noted that, when device mismatch is in same branch, NMOS mismatch is causing ΔV_B to increase and PMOS mismatch is causing ΔV_B to decrease and thus effective change is difference of both. While case when device mismatch is in different branches, both NMOS and PMOS mismatch causing ΔV_B to increase and thus effective change is the sum of both results. We can say that, there is no fix direction of the effective change in bias voltage depending on the four cases, and hence, generalization cannot be made according to the cases on the direction of effective change in bias voltage

Table 4.1 Voltage swing and bias offset voltage change for all the cases.

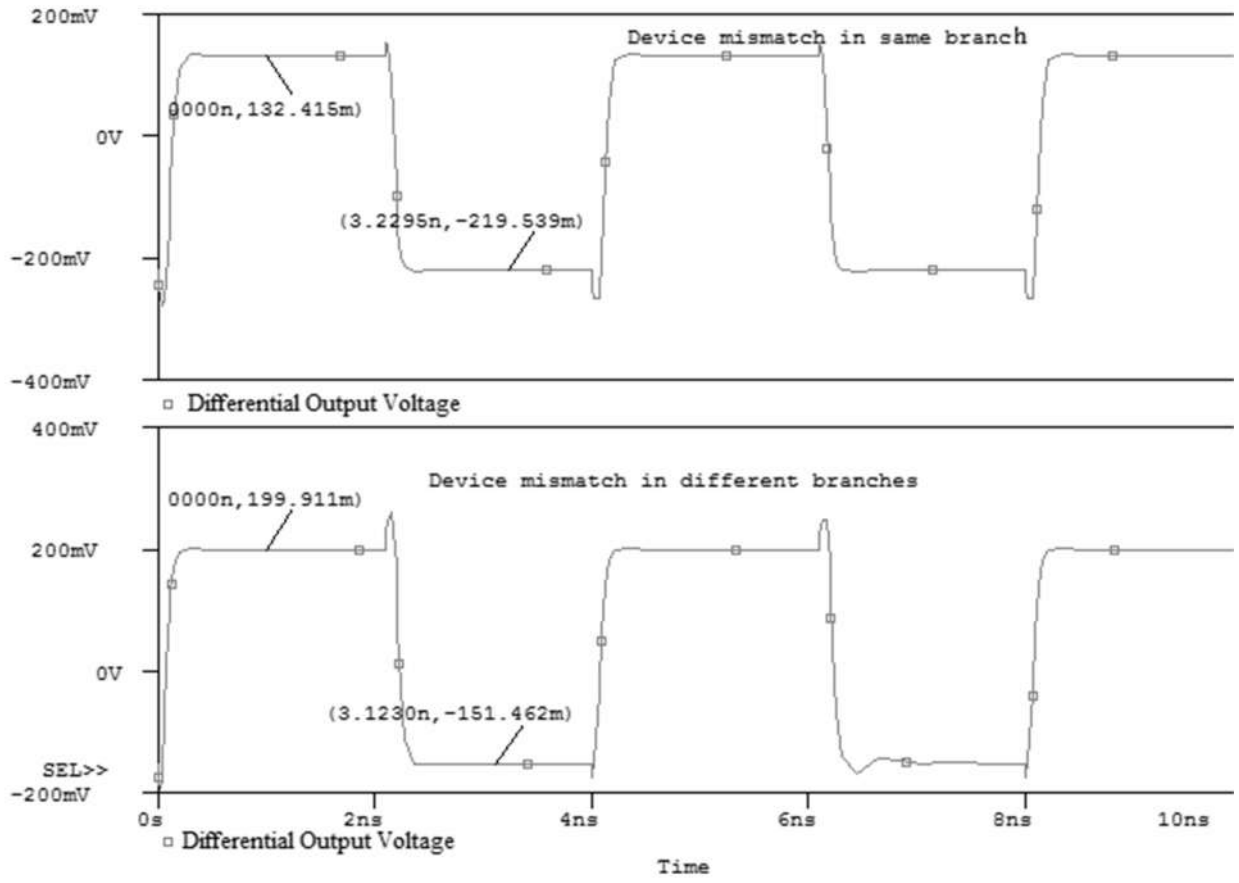
Cases	ΔV_B	V_{swing}
Case 1	0.0161V	.3353V
Case 2	0.0236V	.3528V
Case 3	0.024V	.352V
Case 4	.0248V	.3504V


MOS with threshold-voltage fluctuation
V_{DD}
M3
M4
v_{o1}
v_{o2}
C_L
v_{i1}
M1
M2
v_{i2}
C_L
MOS with threshold-voltage fluctuation
I_{ss}

(a)


MOS with threshold-voltage fluctuation
V_{DD}
M3
M4
v_{o1}
v_{o2}
C_L
v_{i1}
M1
M2
v_{i2}
C_L
I_{ss}
MOS with threshold-voltage fluctuation

(b)



(c)

Fig. 4.7 Device mismatch among NMOS and PMOS transistors (a) in same branch of MCML inverter (b) in different branches of MCML inverter (c) output waveform of both cases 3 and 4

4.4 Effect of threshold fluctuation in triple-tail MCML based D-Latch

The triple-tail MCML based D-latch has been studied in the previous chapter. In this section, the effect of threshold-voltage fluctuation has been studied on triple-tail based MCML D-Latch.

As we know that, the operation differential CLK signal is to switch on or off the tail transistor, which further aids in evaluating whether the D-latch will work in transparent or hold state. Thus, we can say that in triple-tail based circuits (D-latch/XOR/MUX), after switching of the tail

transistor, it behaves as MCML inverter only. Hence, we can deduce that the effect of threshold-voltage fluctuation over triple-tail based MCML D-latch will be same as that of that the effect of threshold-voltage fluctuation on the MCML inverter studied and derived in previous section, mathematically.

Hence, the effect of threshold-voltage fluctuation among NMOS transistors for triple-tail MCML based D-latch can be formulated as

$$\Delta V_B = -\frac{dI_d}{dV_{th}}\Delta V_{th} R_L$$

$$= g_m R_L \Delta V_{th} = G(0)\Delta V_{th} \tag{4.15}$$

And the effect of threshold-voltage fluctuation among PMOS transistors triple-tail MCML based D-latch can be formulated as

$$\Delta V_{B,p} = I_{SS}\Delta R_P$$

$$= I_{SS}\frac{d\mathrm{R_P}}{\mathrm{dV_{TP}}} \cdot \Delta V_{TP} \tag{4.16}$$

Using eq. (4.12), bias offset voltage ΔV_B is obtained as

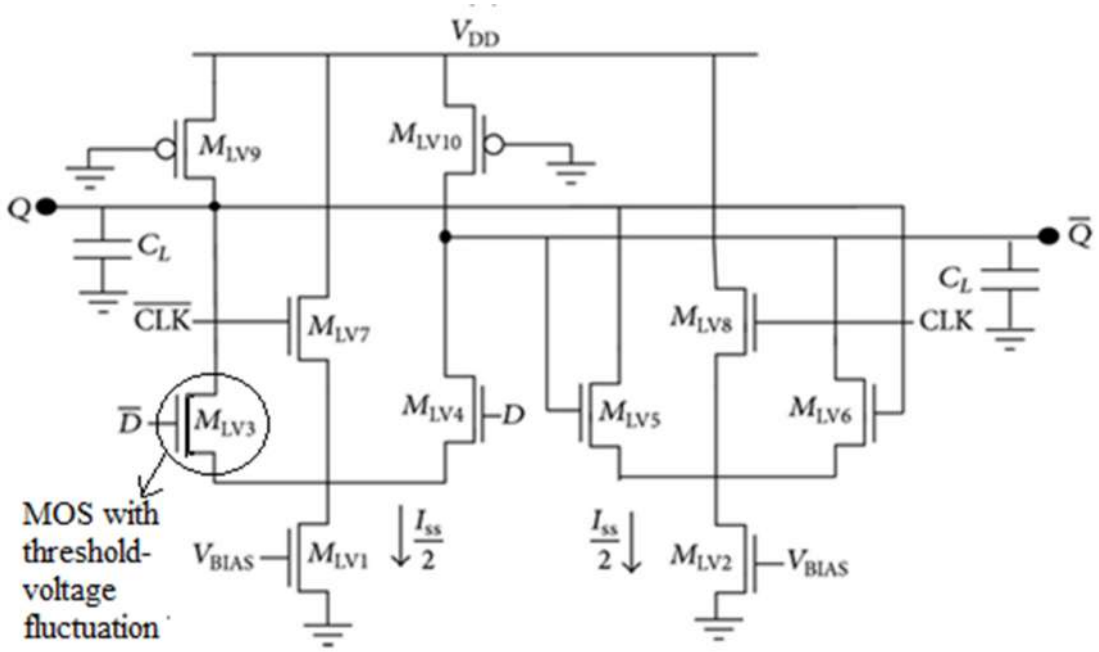
$$\Delta V_{B,p} = I_{SS}\frac{\left(R_{int} - {}^{2(R_{DSW}*10^{-6})}/_{\mathrm{W_P}}\right)R_{int}}{\left(R_{int} - {}^{(R_{DSW}*10^{-6})}/_{\mathrm{W_P}}\right)^2 (\mathrm{V_{DD}} - |\mathrm{V_{TP}}|)} \cdot \Delta V_{TP} \tag{4.17}$$

In Fig. 4.8, triple-tail MCML based D-latch with threshold voltage fluctuations and output waveforms of triple-tail MCML based D-latch without threshold voltage fluctuations, output waveforms of triple-tail MCML based D-latch with threshold-voltage fluctuations among NMOS transistor and output waveforms of triple-tail MCML based D-latch with threshold-voltage fluctuations among PMOS transistor has been shown. From Fig. 4.8d, it is evident that because of mismatching among transistors due to threshold voltage fluctuation, along with bias-offset

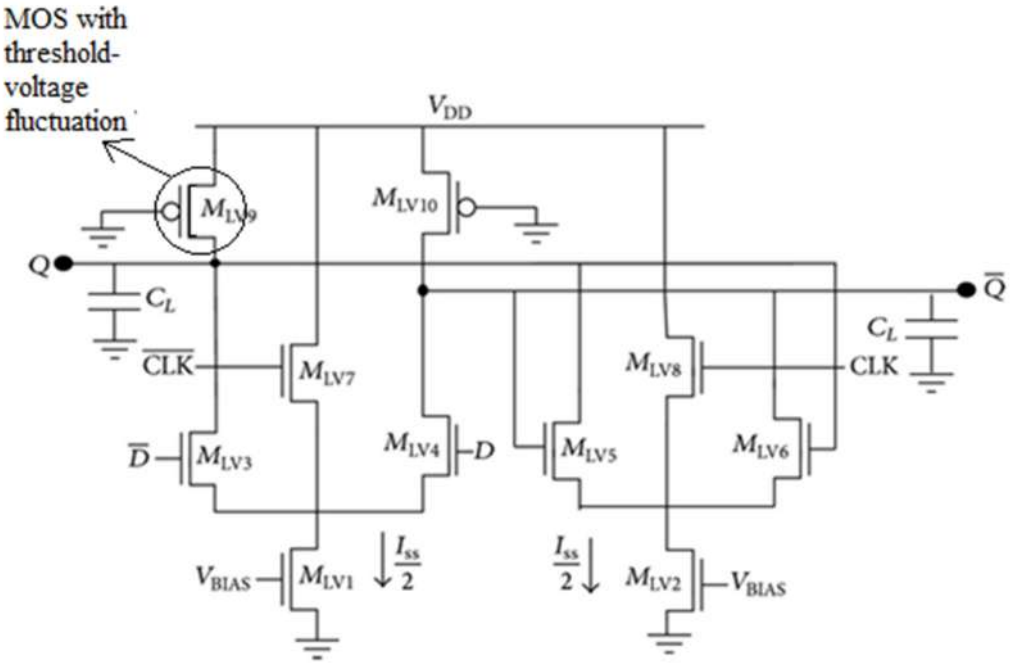
voltage, there is a huge impact on voltage swing also, as the current driving capability of MOS has been affected because of this mismatch.

Because of device mismatch among NMOS transistors of the triple-tail MCML based d-latch, the required voltage swing of our circuit is affected. When there is no mismatch, in Fig. 4.8c, the voltage swing of the D-latch came out to be 396.44mV. But because of device mismatch among NMOS transistors, because of different threshold voltages, both have different driving capabilities and the swing has reduced to 324.88mV.

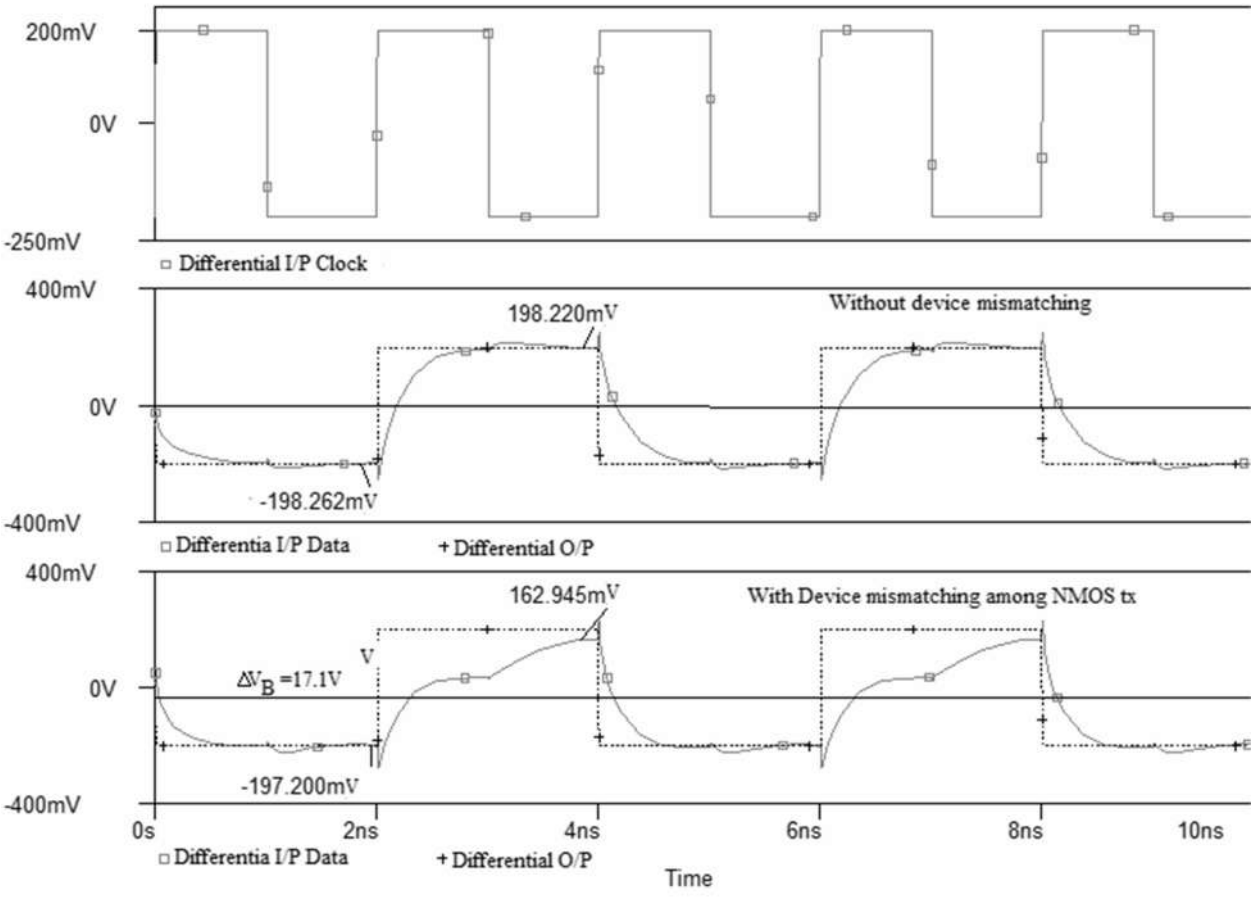
The same reduction in swing can be observed from Fig. 4.8d, that the device mismatch among PMOS transistors due to threshold voltage fluctuation, also affects the swing of the D-latch.



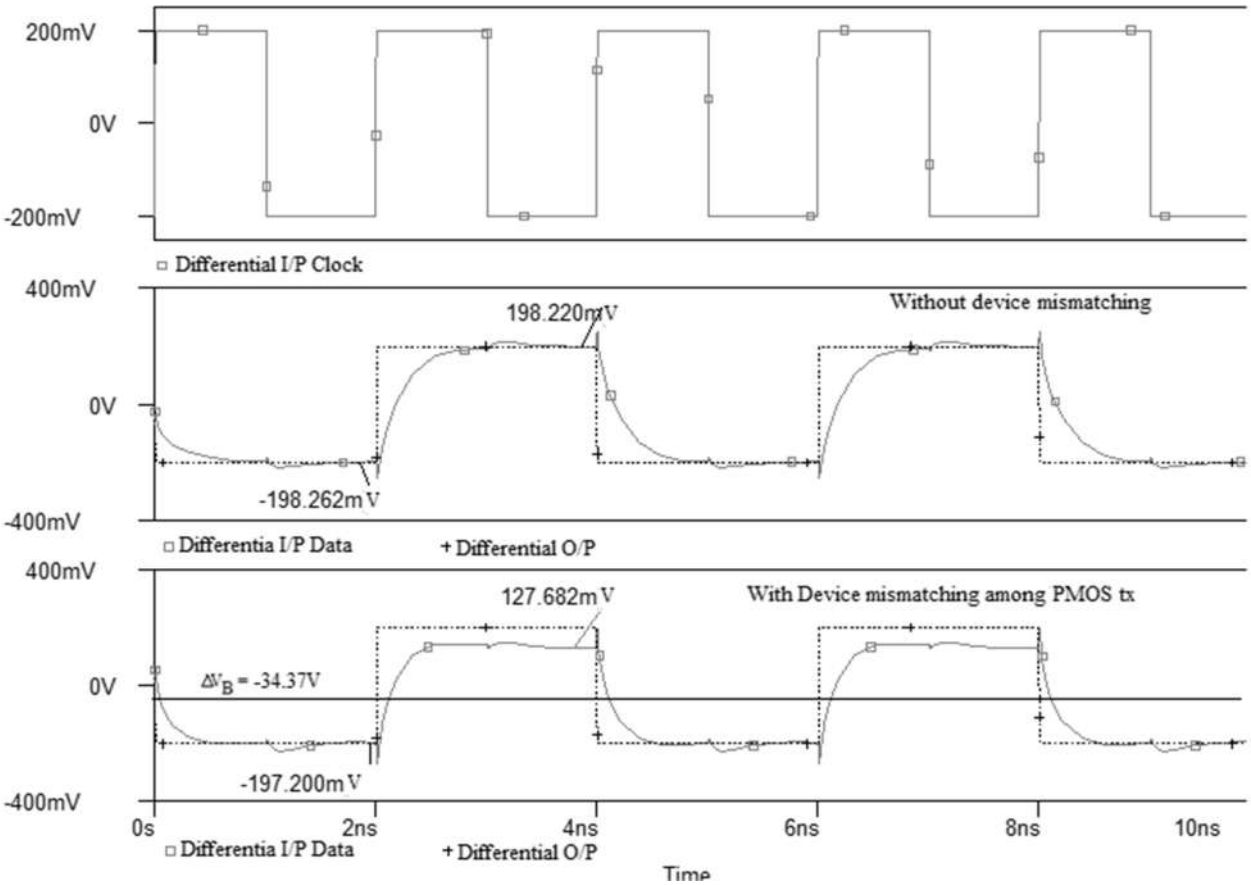
(a)


MOS with threshold-voltage fluctuation
V_{DD}
M_{LV9}
M_{LV10}
Q
$\overline{Q}$
C_L
C_L
$\overline{CLK}$
M_{LV7}
M_{LV8}
CLK
$\overline{D}$
M_{LV3}
M_{LV4}
D
M_{LV5}
M_{LV6}
V_{BIAS}
M_{LV1}
$\frac{I_{ss}}{2}$
$\frac{I_{ss}}{2}$
M_{LV2}
V_{BIAS}

(b)


200mV
0V
-250mV
Differential I/P Clock
400mV
198.220mV
Without device mismatching
0V
-198.262mV
-400mV
Differentia I/P Data
+ Differential O/P
400mV
162.945mV
With Device mismatching among NMOS tx
V
ΔV_B =17.1V
0V
-197.200mV
-400mV
0s
2ns
4ns
6ns
8ns
10ns
Differentia I/P Data
+ Differential O/P
Time

(c)



(d)

Fig. 4.8 Triple-tail MCML based D-latch with threshold-voltage fluctuation (a) among NMOS transistors (b) among PMOS transistors and Output waveforms of triple-tail MCML based D-latch (c) with threshold-voltage fluct fluctuations (among NMOS transistor) (d) with threshold-voltage fluctuations (among PMOS transistor)

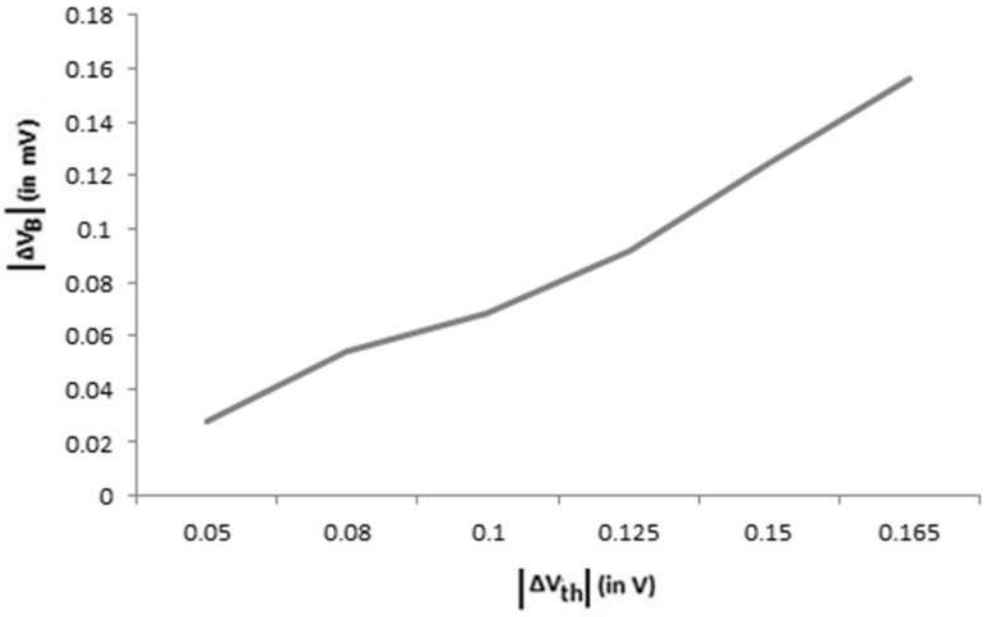


Fig. 4.9 Variations in ΔV_B with respect to the threshold-voltage fluctuation (ΔV_{th}) in triple-tail MCML based D-latch**.**

Fig. 4.9 shows the effect of threshold voltage fluctuation on difference in bias voltage of the two output terminals. It can be seen that the working of D-latch is greatly affected because of threshold voltage fluctuation. To overcome this, a method feedback resistors between input and output of the MCML logic has been suggested in [10], which will introduced and further analyzed in triple-tail MCML based D-latches, in the next section.

4.5 Feedback MCML Circuit

In the previous section, the effect of threshold voltage is studied for conventional MCML and triple-tails based circuits. If the bias offset voltage ΔV_B becomes large because of this high of threshold voltage fluctuation, then it can cause the malfunctioning of the circuit.

To reduce the effect of threshold-voltage fluctuation, a feedback has been used in MCML circuit in [10]. Feedback MCML circuit has been shown in the Fig. 4.10, where a purely resistive PMOS transistors M_{F1} and M_{F2} biased in linear region, are added as feedback transistors and have been connected between input and output.

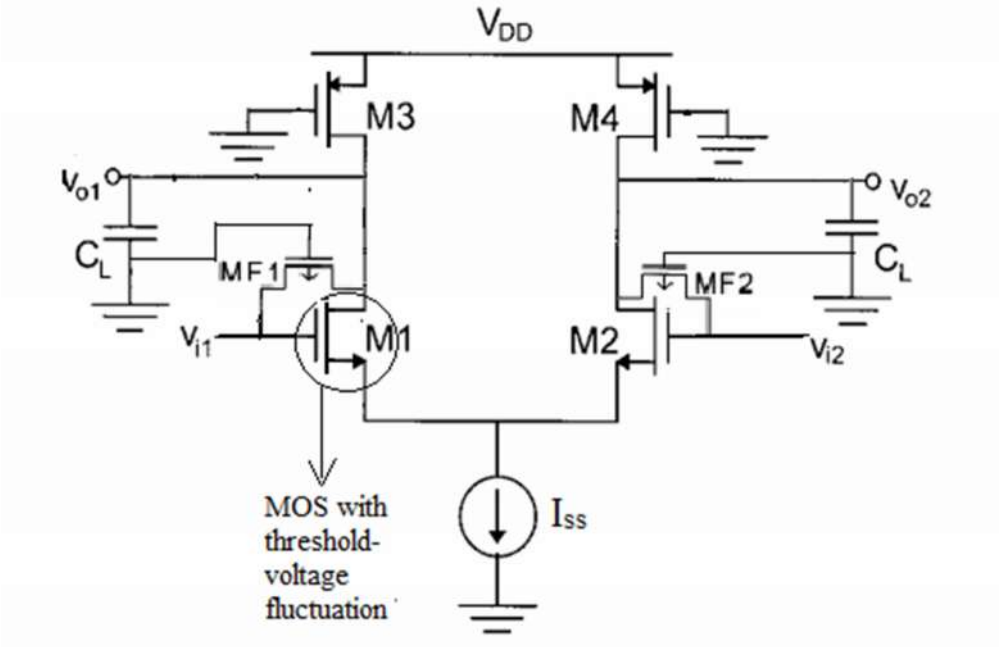


Fig. 4.10 Feedback MCML circuit

The effect of these PMOS feedback transistors on threshold voltage fluctuation is studied in this section. In MCML circuits, as they are nothing but simply source-coupled pair circuit, its differential –mode voltage gain $G_c(f)$ at a frequency f is given by

$$G_c(f) = \frac{G_c(0)}{1-j\left(2\pi f/p\right)} \tag{4.18}$$

Where the DC gain of the circuit is represented by $G_c(0)$ and p is the pole of MCML inverter, which is a function of load capacitance and load resistance implemented by the PMOS transistors, M_3 and M_4. [15].

The impact of feedback transistors on the gain of conventional MCML, assuming PMOS are purely resistive, is given by

$$G_F(f) = \frac{G_c(f)}{1+F_B G_c(f)}$$

$$= \frac{G_c(0)}{1+F_B G_c(0)} \frac{1}{1-j\left({}^{2\pi f}/_{p}\right){}^{1}/_{T+1}} \tag{4.19}$$

Where, F_B is a feedback function and represents the feedback gain of the feedback transistors (M_3 and M_4) [14]. If we define loop gain $T = F_B G_c(0)$, then $G_F(f)$ can be computed as

$$|G_F(f)| = \frac{1}{T+1} \frac{G_c(0)}{\sqrt{1+\left({}^{2\pi f}/_{p(T+1)}\right)^2}} \tag{4.20}$$

It can be seen that, when T=0, eq. (4.20) produces the gain of conventional MCML inverters and for non-zero positive loop gain, i.e. T > 0, (4.20) produces the gain of feedback MCML inverters. Fig. 4.12 shows simulation result of frequency response of traditional MCML and with feedback MCML inverters using 0.18µm Technology**.**

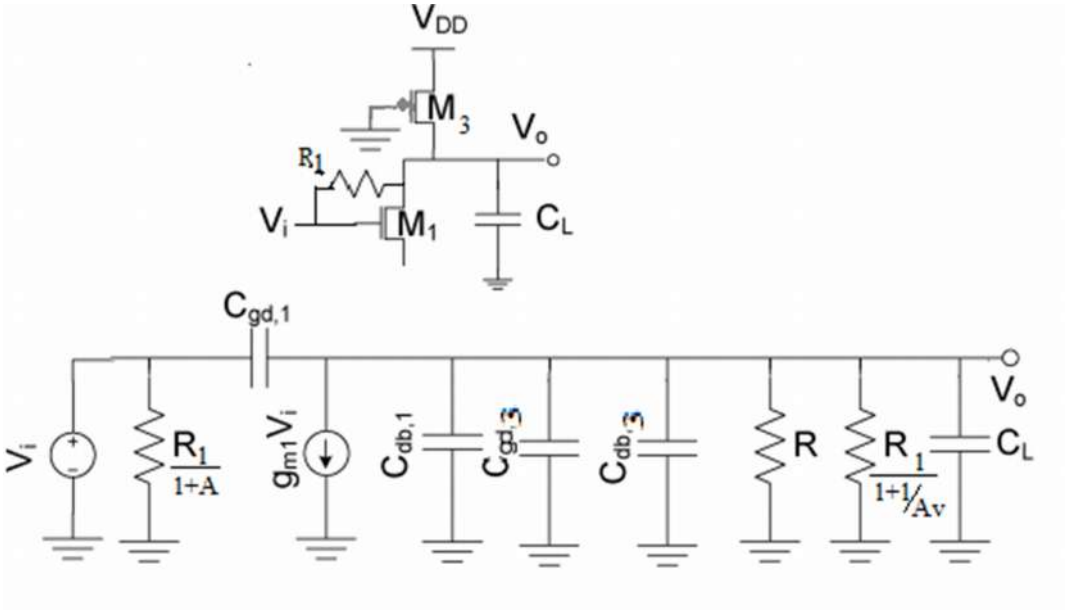
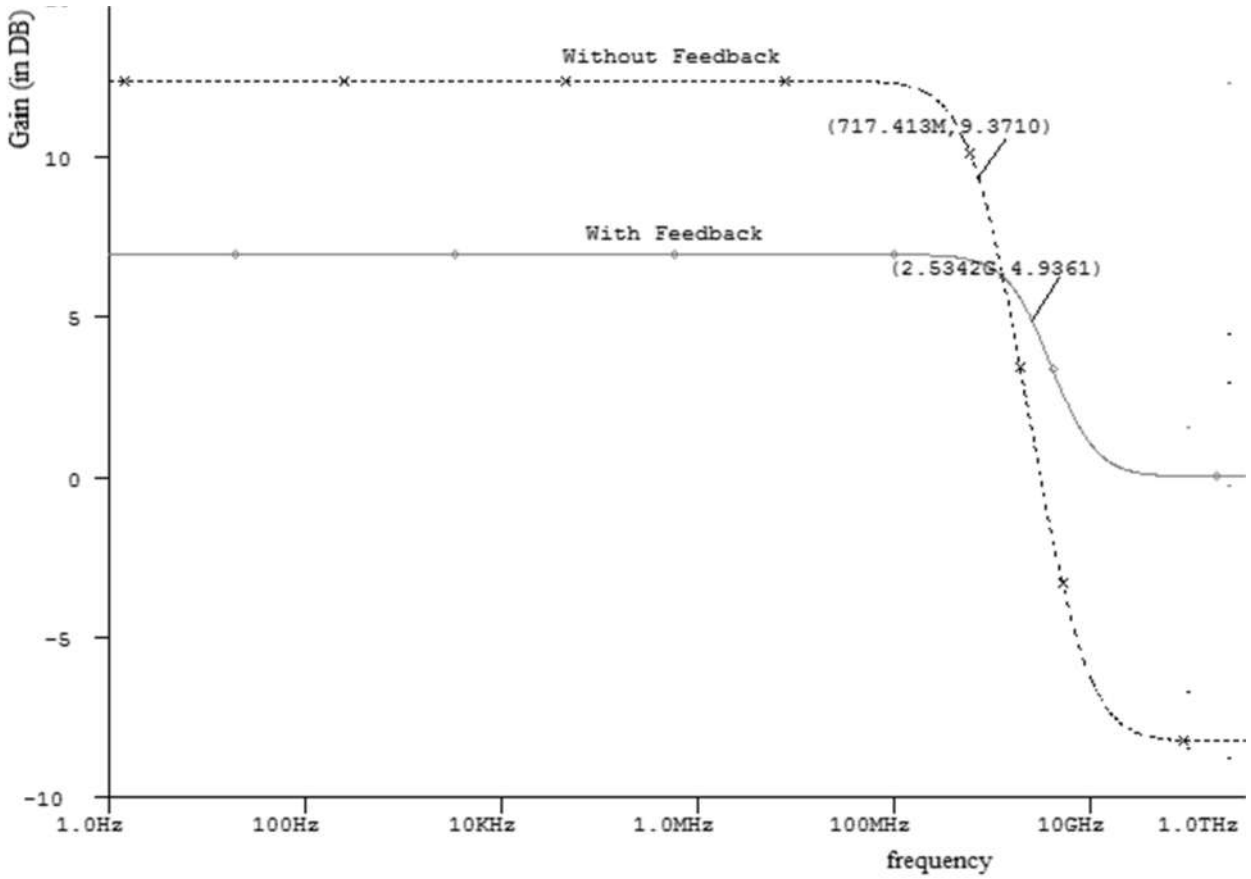


Fig. 4.11 Small signal model of MCML inverter with feedback Resistor

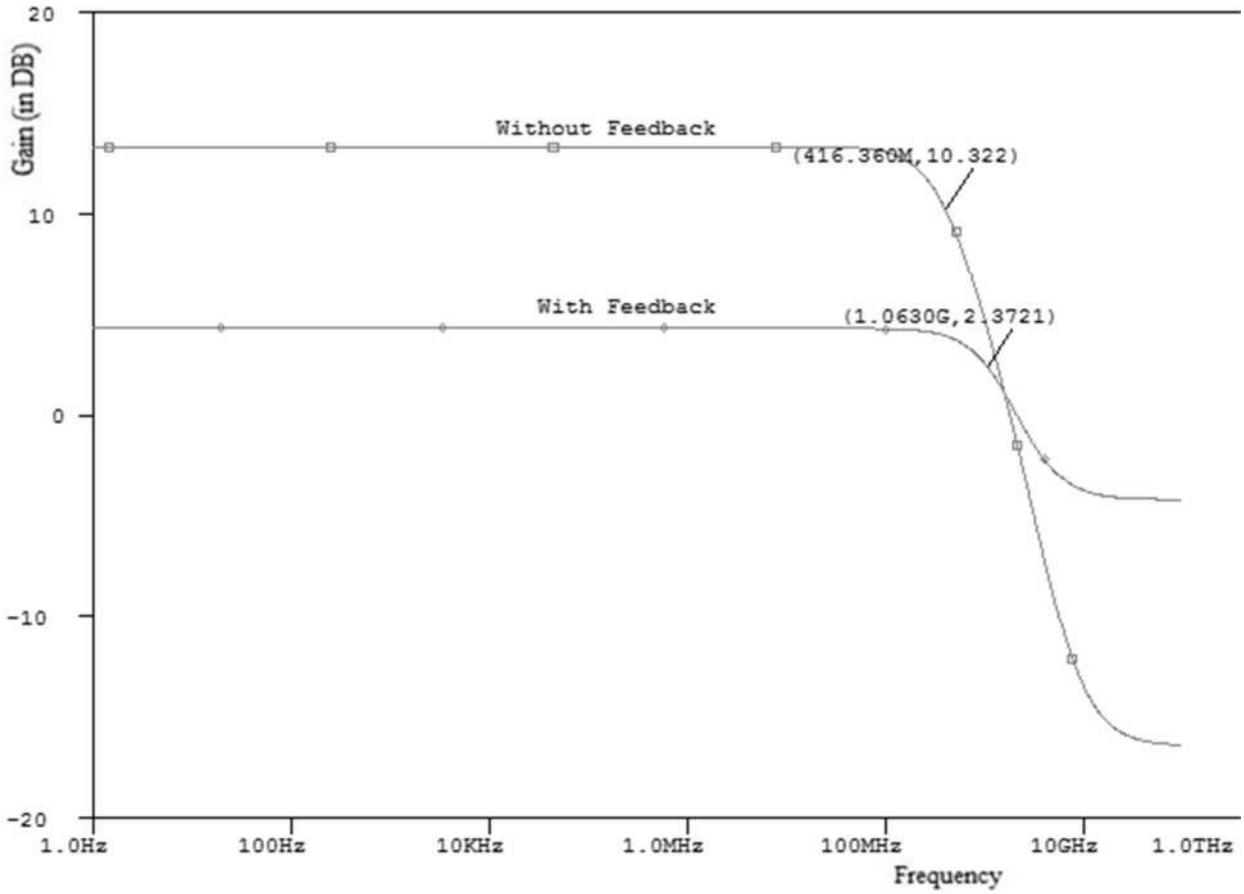
Because of feedback resistor, using Miller's theorem, as shown in Fig 4.11, the effective output resistance decreases, the effective bandwidth of the circuit increases.

$$BW = \frac{1}{\left(R||\left(\frac{R1}{1+1/Av}\right)\right)*(C_{gd,1}+C_{db,1}+C_{gd,3}+C_{db,3}+C_L)} \quad (4.21)$$

Where A_v is the gain of MCML inverter.


Gain (in DB)
Without Feedback
(717.413M,9.3710)
With Feedback
(2.5342G,4.9361)
10
5
0
-5
-10
1.0Hz
100Hz
10KHz
1.0MHz
100MHz
10GHz
1.0THz
frequency

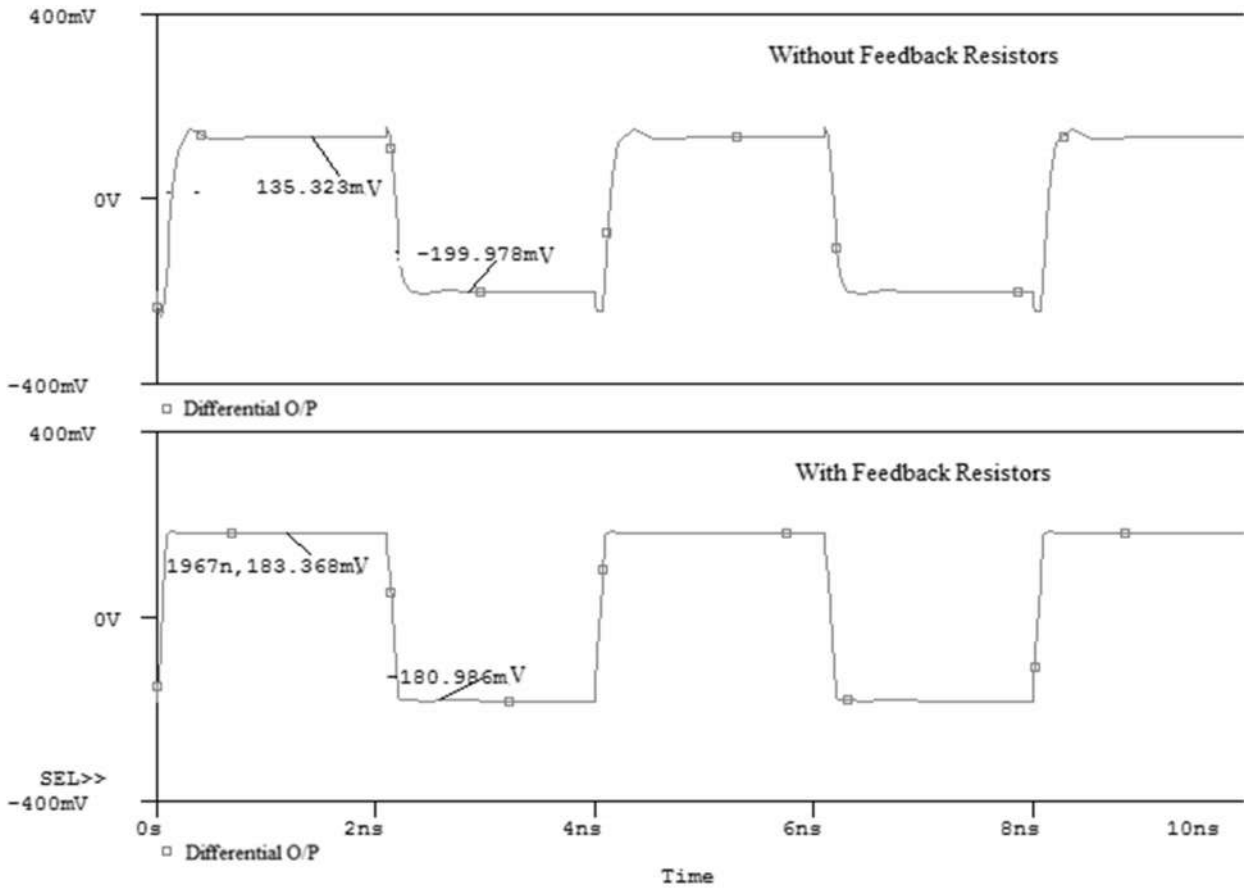
(a)



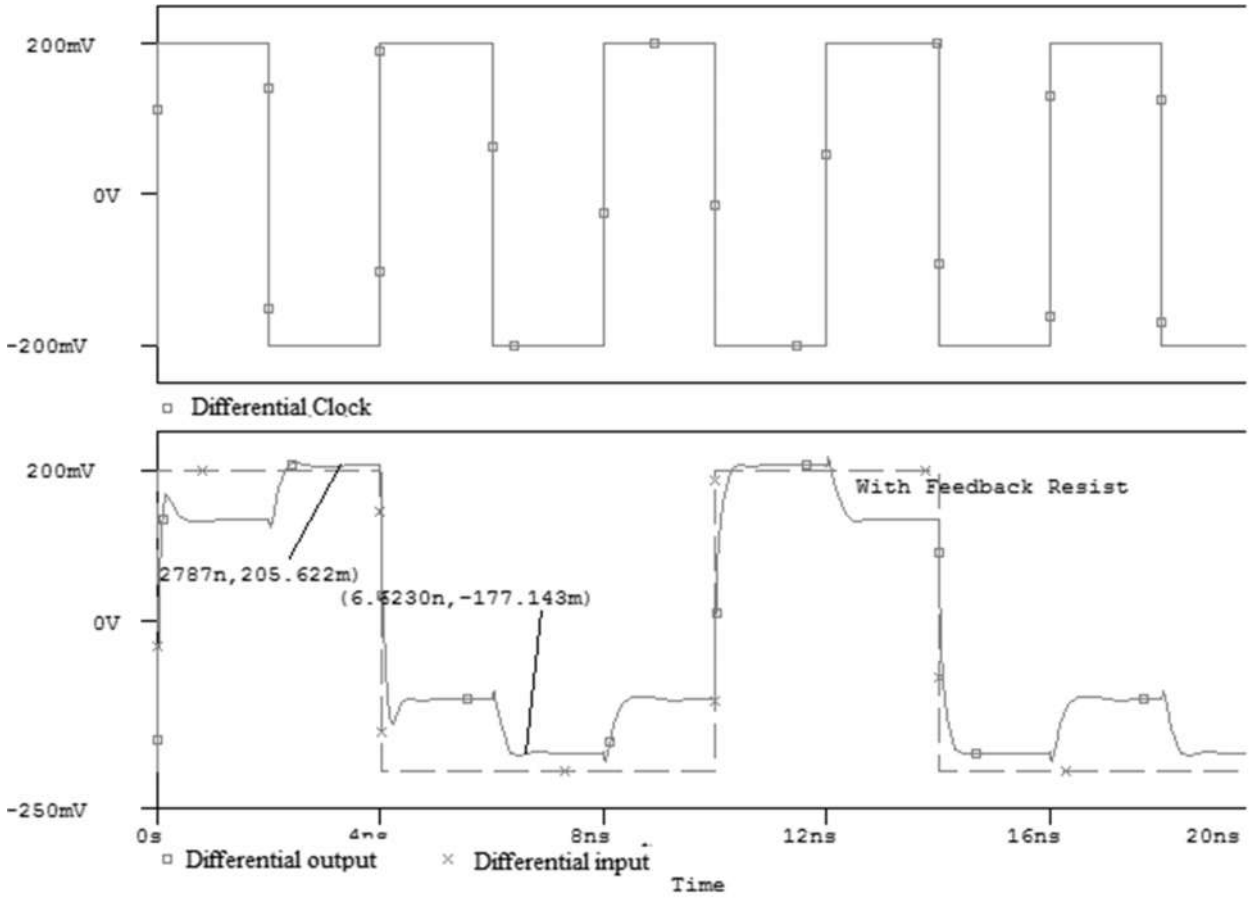
(b)

Fig. 4.12 Simulation result of frequency response of traditional MCML and with feedback resistors in (a) MCML inverters (b) MCML based D-latch

It can be seen that MCML inverter with feedback has larger frequency band as compared to the traditional inverters. If we design an inverter for maximum frequency operation (f_{MAX}), such that $G_F(f_{MAX}) = G_C(f_{MAX})$, then DC gain of the feedback MCML inverter will be less than that of the conventional MCML inverter, i.e. $G_F(0) < G_C(0)$. Fig. 4.14 shows that the effect of threshold-voltage fluctuation has been reduced greatly. The bias offset voltage has been shifted to zero volt for differential output, this implies that because of feedback, the effect on bias-offset voltage and voltage swing has been greatly reduced because of device mismatching among transistors.


400mV
Without Feedback Resistors
0V
135.323mV
-199.978mV
-400mV
Differential O/P
400mV
With Feedback Resistors
1967n,183.368mV
0V
180.986mV
SEL>>
-400mV
0s
2ns
4ns
6ns
8ns
10ns
Differential O/P
Time

(a)



(b)

Fig. 4.13 Effect of feedback transistors on threshold-voltage fluctuation in (a) MCML inverter (b) MCML based D-latch

The effect of feedback resistors on change in bias voltage can be seen in Fig 4.14 that the change in bias voltage because of threshold voltage fluctuation has almost reached to zero because of feedback resistors as compared to the one without feedback resistors shown in Fig 4.3.

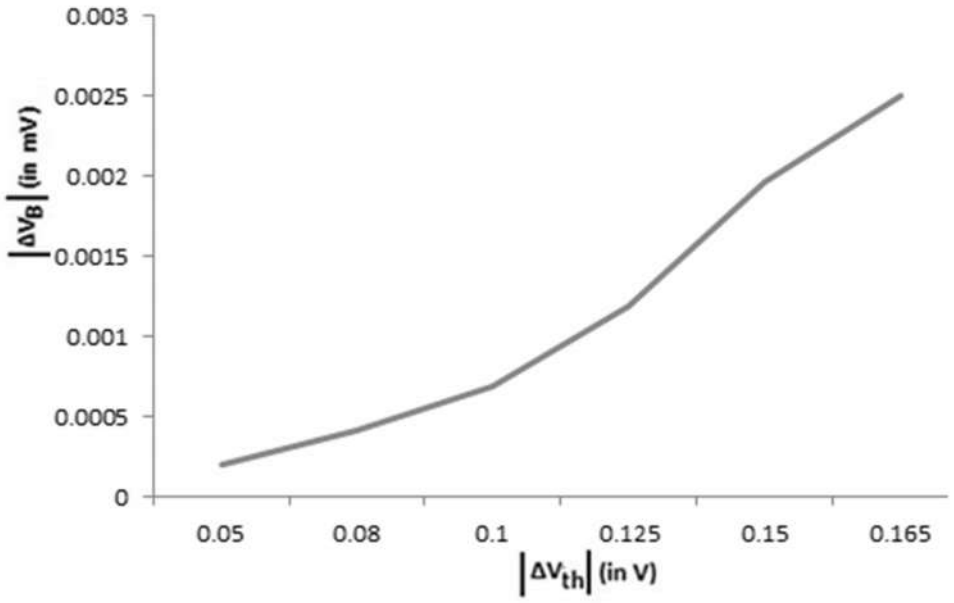


Fig. 4.14 Variations in ΔV_B with respect to the threshold-voltage fluctuation (ΔV_{th}) with feedback transistors**.**

4.6 Feedback In triple-Tail MCML Based D-Latch

The triple-tail MCML based D-latch has been studied in the previous chapter. In this section, the effect of feedback transistors on threshold-voltage fluctuation has been studied on triple-tail based MCML D-Latch.

As we know that, the operation differential CLK signal is to switch on or off the tail transistor, which further aids in evaluating whether the D-latch will work in transparent or hold state. Thus, we can say that in triple-tail based circuits (D-latch/XOR/MUX), after switching of the tail transistor, it behaves as MCML inverter only. Hence, we can deduce that the effect of feedback transistors on threshold-voltage fluctuation over triple-tail based MCML D-latch will be same as

that of that the effect of feedback transistors on threshold-voltage fluctuation on the MCML inverter studied in previous section, mathematically.

Hence, the effect feedback transistors on of threshold-voltage fluctuation among NMOS transistors for triple-tail MCML based D-latch will be

$$G_{FT}(F) = \frac{G_{cT}(0)}{1+F_B G_{cT}(0)} \frac{1}{1-j\left({}^{2\pi f}/_{p\prime}\right){}^{1}/_{T\prime+1}} \tag{4.22}$$

Where $G_{cT}(0)$ is the DC voltage gain of triple-Tail MCML Based D-Latch without feedback, $G_{FT}(F)$ is the differential-mode voltage gain of triple-Tail MCML Based D-Latch with feedback, T' is the loop-gain of feedback transistors i.e. $T' = F_B G_{cT}(0)$ and F_B is the gain of feedback transistors and p' is the pole of triple-Tail MCML Based D-Latch without feedback.

$$|G_{Ft}(f)| = \frac{1}{T\prime+1} \frac{G_{cT}(0)}{\sqrt{1+\left({}^{2\pi f}/_{p\prime(T\prime+1)}\right)^2}} \tag{4.23}$$

Fig. 4.15 shows the circuit of triple-tail MCML based D-latch with feedback connected transistors to reduce the effect of threshold-voltage fluctuation and Fig. 4.17 shows the output waveform of effect of feedback transistors on triple-tail MCML based D-latch with threshold-voltage fluctuation and Fig. 4.18 shows the effect of feedback transistors on the frequency of operation of the triple-tail MCML based D-latch. The bias offset voltage has been shifted to zero volt for differential output, this implies that because of feedback, the effect on bias-offset voltage and voltage swing has been greatly reduced because of device mismatching among transistors. Since, tail-transistors only aid in selection of respective cell, and has no impact on swing, hence there is not much effect of device mismatching among tail transistors and feedback applied to tail-transistors have no effect on AC analysis of the D-latch.

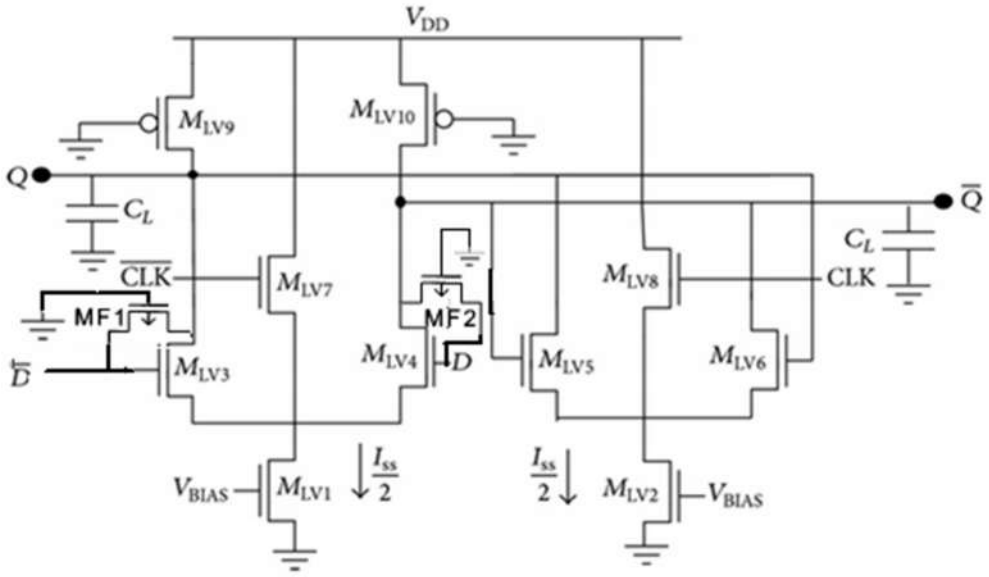


Fig. 4.15 Triple-tail based MCML D-latch with Feedback connected transistors

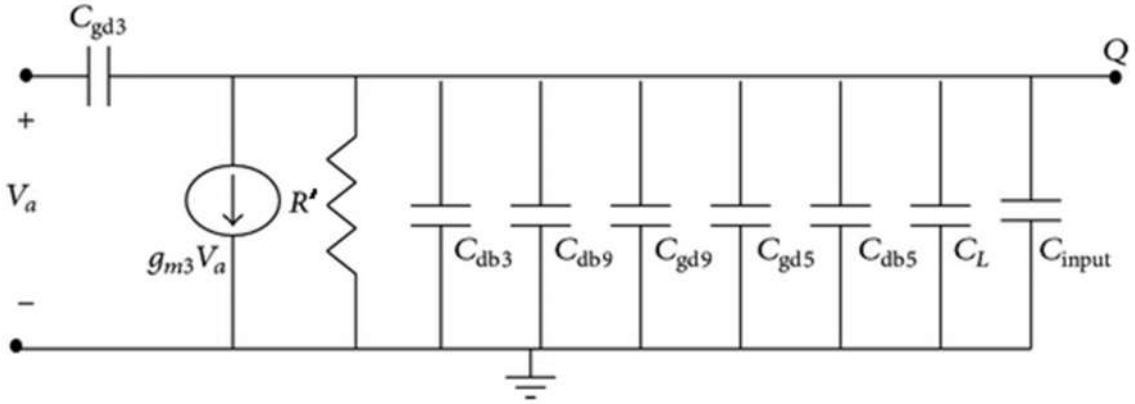


Fig. 4.16 Small signal model of triple-tail MCML based D-latch with feedback resistors

Because of feedback resistor, using Miller's theorem, as shown in fig 4.12, the effective output resistance decreases, the effective bandwidth of the circuit increases.

$$BW = \frac{1}{R' * (C_{gd,1} + C_{db,1} + C_{gd,3} + C_{db,3} + C_L)} \quad (4.24a)$$

$$R' = \left(R_P || \left(\frac{R1}{1 + {}^{1}/_{Av}} \right) \right) \quad (4.24b)$$

Where A_v is the gain of MCML inverter and R_P is the resistance implemented by PMOS load transistors.

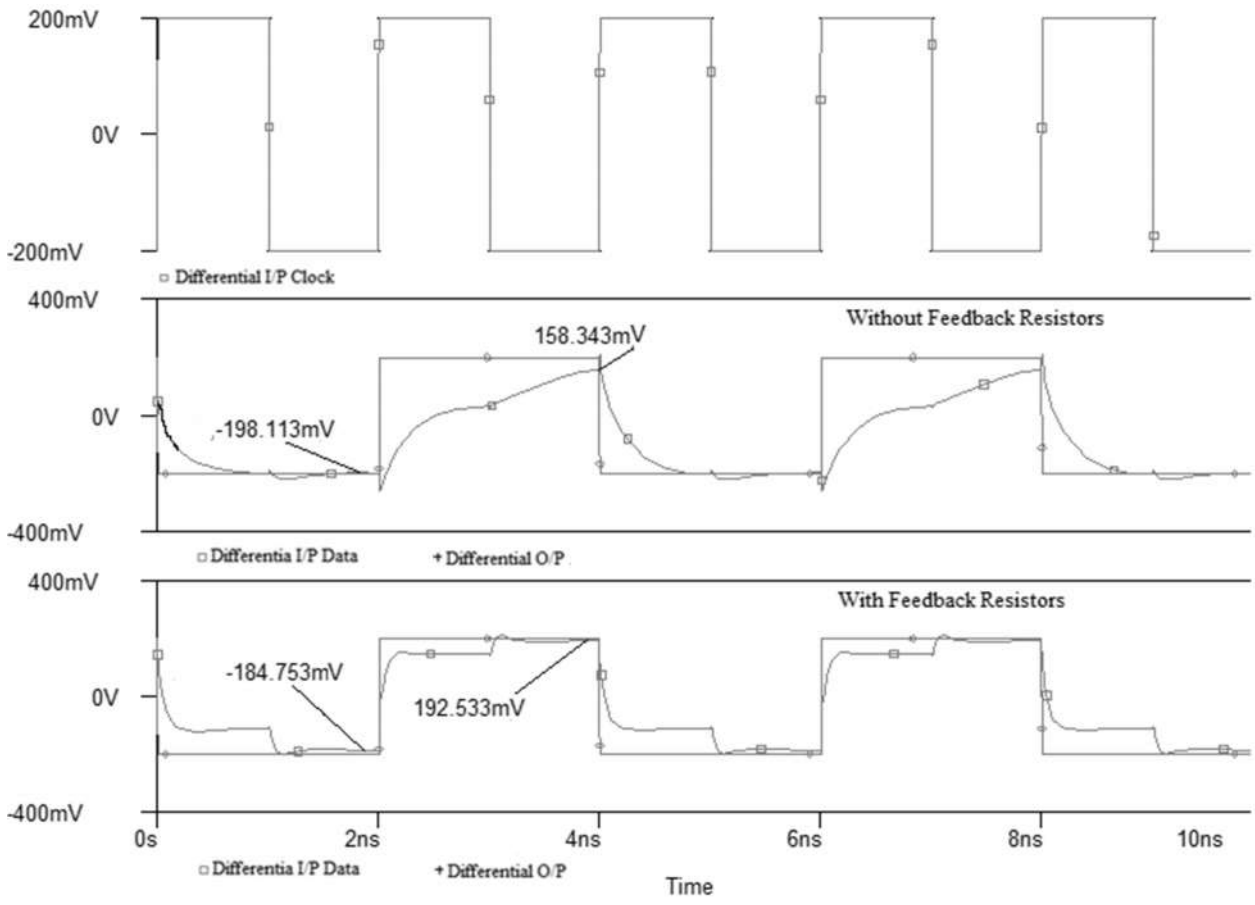


Fig. 4.17 output waveform of effect of feedback transistors on triple-tail MCML based D-latch with threshold-voltage fluctuation

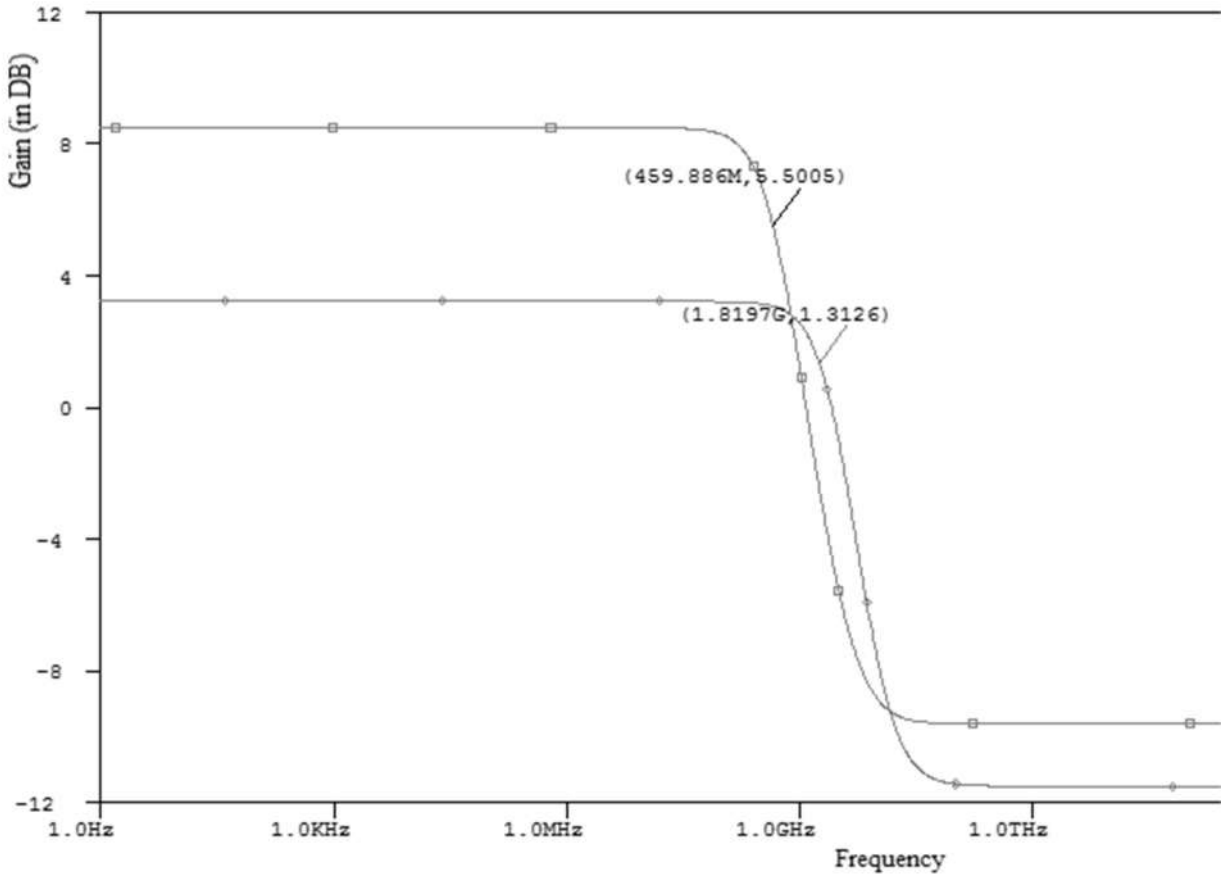


Fig. 4.18 Effect of feedback transistors on the frequency of operation of the triple-tail MCML based D-latch.

It can be noted that, we have used feedback resistance between output nodes and nodes of differential D-inputs only and not used for cross-coupled differential pair ($M_{LV5} - M_{LV6}$) in Fig. 4.15 because if we would connect feedback between the, output nodes will have a conducting path and high voltage (V_{DD}) at one output would get discharged through output node at which low voltage is there, and thus would contaminate the operation of triple-tail MCML based d-latch.

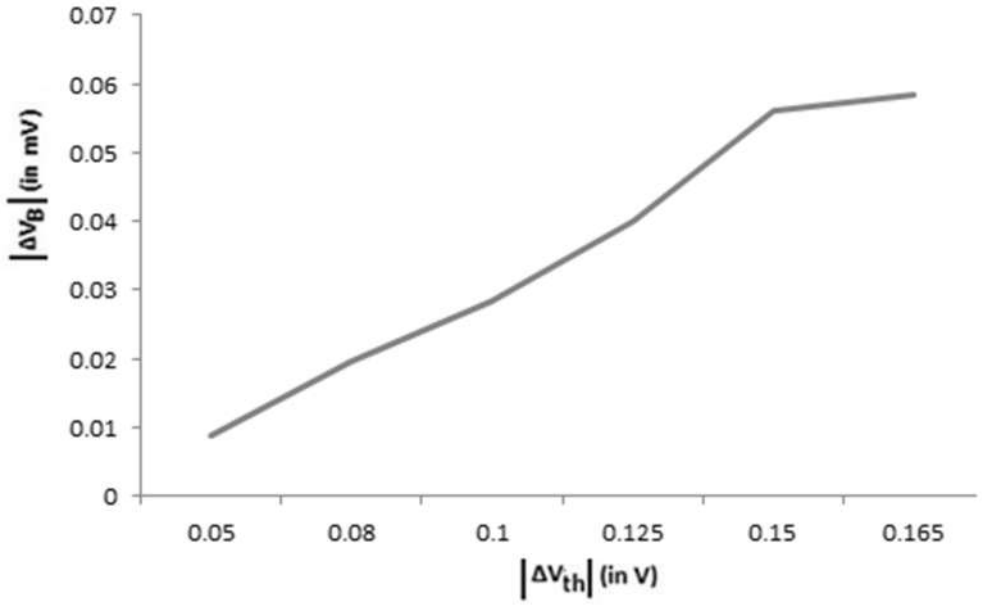


Fig. 4.19 Variations in ΔV_B with respect to the threshold-voltage fluctuation (ΔV_{th}) with feedback transistors in triple-tail MCML based D-latch**.**

The effect of feedback resistors on change in bias voltage can be seen in Fig 4.19, that the change in bias voltage because of threshold voltage fluctuation in triple-tail MCML based D-latch has reduced significantly because of feedback resistors as compared to the one without feedback resistors shown in Fig 4.9.

Chapter 5

Serializer and Deserializer

Serializer and deserializer (also known as SERDES) circuits are now present in every digital high speed applications. For transmission of data in optical fiber systems for telecommunications and various storage applications, serializers and deserializers are proven to be quite useful. For chip-to-chip interconnections, serializer and deserializer circuits can also be used as they help to reduce the pin count. The data rates of serializer and deserializer circuits continue to increase and this improvement of data rate can be achieved through various means.

In this chapter, high data rate for the serializer and deserializer circuits are simulated using feedback triple-tail MCML based D-latch for improvement in both power and frequency.

5.1 Serializer and deserializer overview:

Most of the high-speed communication systems can be categorized into three major components in their simplest form i.e. transmitter, receiver and the communication medium, as shown in Fig. 5.1.

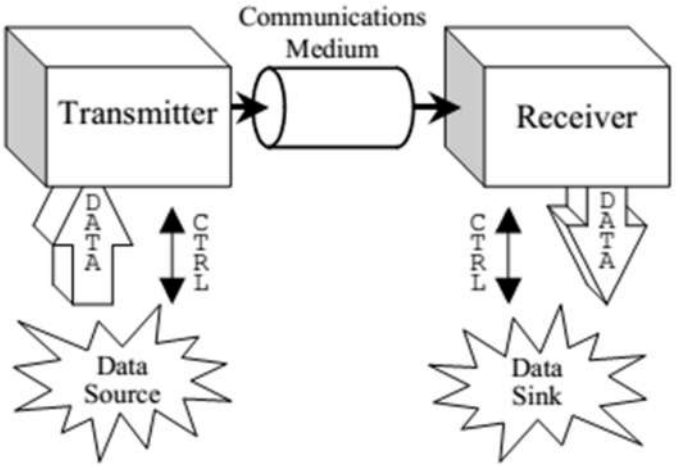


Fig. 5.1 Major components of communication system

- **Transmitter:** It takes parallel data from the data source and then transfers it to output using a serializer. This serial data is sent via communication medium to the receiver, typically with no clocking information.

- **Communication medium:** It consists of medium for communication, as well as the necessary circuitry to process the input and output signals. Channels may require receivers, repeaters and drivers, to maintain the desired final strength at receiver. So basically, together the physical medium, the drivers required for electrical communication between the transmitter and receiver, and repeaters.

- **Receiver:** At receiver, received electrical signal is examined, extraction of bit values is done and the data is again converted to the parallel form. The Receiver must recover the data accurately after it has been handed by the channel, and to do this it usually has to somehow extract clocking information from the serial data stream. For serial to parallel conversion of data, deserializers are required.

SerDes stands for Serializer/Deserializer. The serializer takes parallel data and convert it into serial bit stream. On the other end of the serial link, deserializer converts the received serial data back into parallel data as shown in Fig. 5.2.

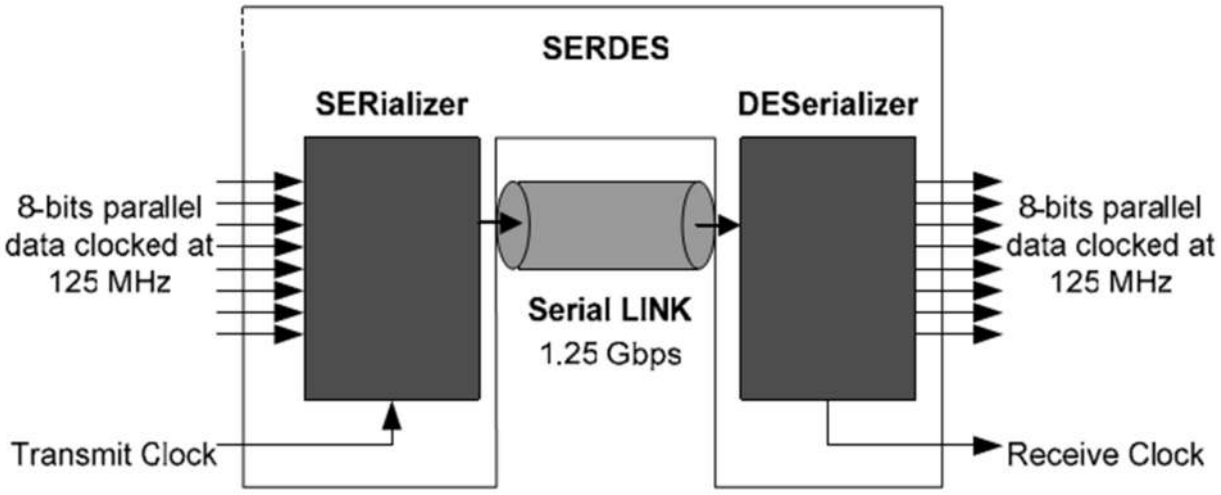


Fig. 5.2 Block diagram of SerDes transreceiver.

5.2 Implementation of Serializer/Deserializer Using MCML:

One of the main application of current-mode logic circuits, because of its high speed and low power requirement at high frequencies, is the implementation of IC for multiplexing/demultiplexing or serializer/deserializer in optical fiber communications, whose structure is shown in Fig. 5.3.

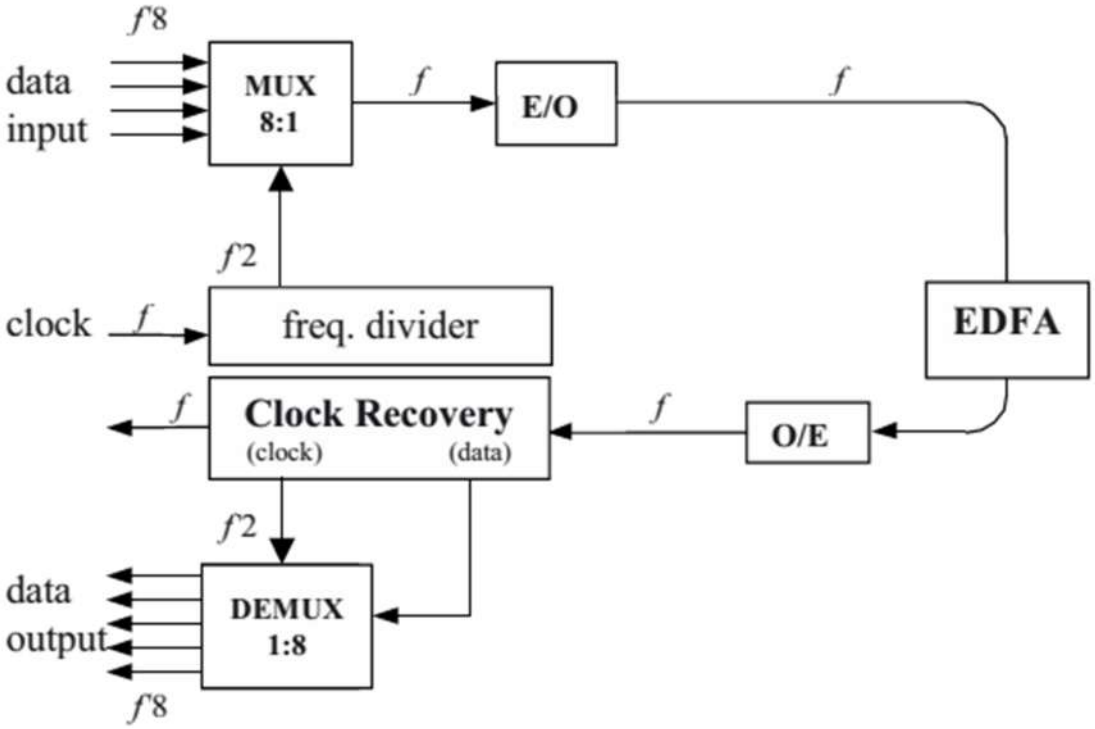


Fig. 5.3 Fiber-optic link block diagram [16]

Here, O/E block is a photodetector that converts optical signals into electrical signals, and E/O block is a semiconductor laser diode that performs the opposite function. To exploit the wide bandwidth of the optical fiber link , parallel input are serially transferred to the channel through serializer or MUX at frequency f, and EDFA (erbium-doped fiber amplifier) amplifies the data. Serial data crossing the optic fiber are then transferred in parallel through a deserializer or DEMUX[16].

5.2.1 1:8 DeMUX or Deserializer:

The schematic of an 1:8 DEMUX or deserializer is shown in Fig. 5.4. Here each 1:2 DEMUX is implemented by the circuit shown in Fig. 5.5.

Deserializer is a circuit that converts incoming one-line data signal (Din) of frequency 'f' in multiple parallel signals (DO0-DO7) which are 0.125 times slower than the incoming data signal, i.e. are of frequency 'f/8', whose operating clocks are obtained by using static frequency dividers.

It is implemented using seven 1:2 DEMUX, which is here operating like nothing but a D-flip-flop. These 1:2 DEMUX are connected in hierarchical manner having three levels, to implement the 1:8 DEMUX, or in a simple manner we can say that output of one is acting as input to one 1:2 DEMUX lower in hierarchy and also is clocked at lower frequency. As it can be seen from Fig. 5.4 that DEMUX in upper most hierarchy operates at full data rate, DEMUX in immediate lower level operates at half of the data rate with respect to the ones in upper hierarchy.

This 1:2 DEMUX is further constructed with d-latches, as shown in Fig. 5.4, which are operating as D flip-flop in master-slave configuration for one output and master-slave-master, for the other output.

Here D-latch is implemented by traditional MCML D-latch, MCML D-latch with feedback resistors, triple-tail D-latch and tripletail d-latch with feedback resistors.

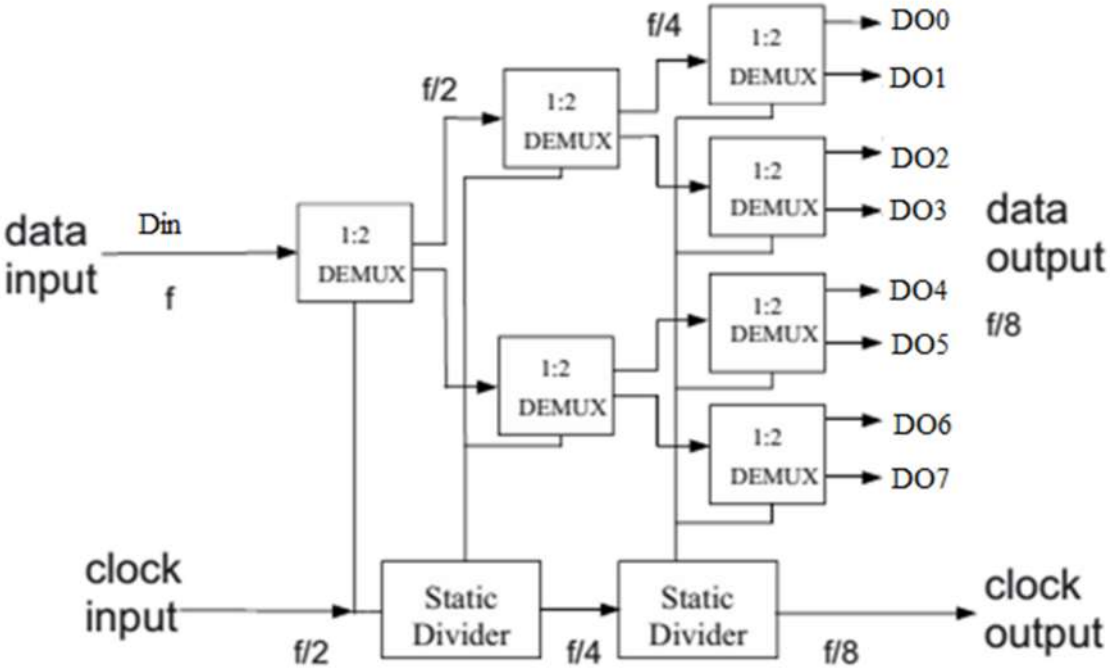


Fig.5.4 Block Diagram of a 1:8 DEMUX [16]

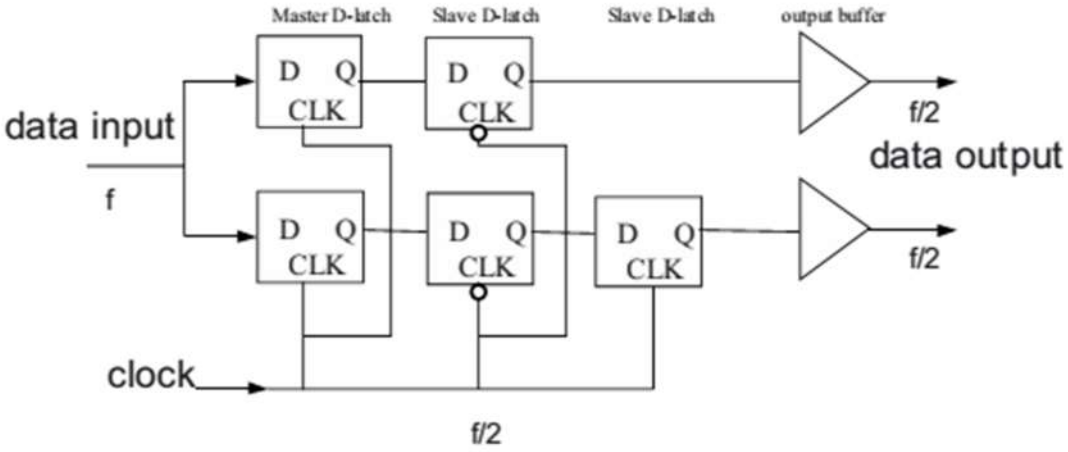


Fig.5.5 Schematic of a 1:2 DEMUX [16]

5.2.2 8:1 MUX or Serializer:

The schematic of an 1:8 MUX or serializer is shown in Fig. 5.6. Here each 2:1 MUX is implemented by the circuit shown in Fig. 5.5.

Serializer is a circuit that converts incoming multiple data line signals (DIN1-DIN7) of frequency 'f/8' in one single output signal (DOUT) which is 8 times faster than the incoming data signals, i.e. is of frequency 'f', whose operating clocks are obtained by using static frequency dividers.

It is implemented using seven 2:1 MUX, which is here operating like nothing but a master-slave configures latches working as D flip-flop. These 2:1 MUX are connected in hierarchical manner having three levels, to implement the 8:1 MUX, or in a simple manner we can say that output of one is acting as input to one 1:2 MUX lower in hierarchy and also is clocked at higher frequency, is serving as input to the other in next level. As it can be seen from Fig. 5.6 that MUX in upper most hierarchy operates at one-eighth of the full data rate, MUX in immediate lower level operates at double of the data rate with respect to the ones in upper hierarchy.

This 2:1 MUX is further constructed with d-latches, as shown in Fig. 5.7, which are operating as d-flipflop in master-slave configuration for one output and master-slave-master, for the other output. Then after, a 2:1 MUX is selecting and passing the output of the two flip-flops.

Here D-latch is implemented by traditional MCML D-latch, MCML D-latch with feedback resistors, triple-tail D-latch and tripletail d-latch with feedback resistors.

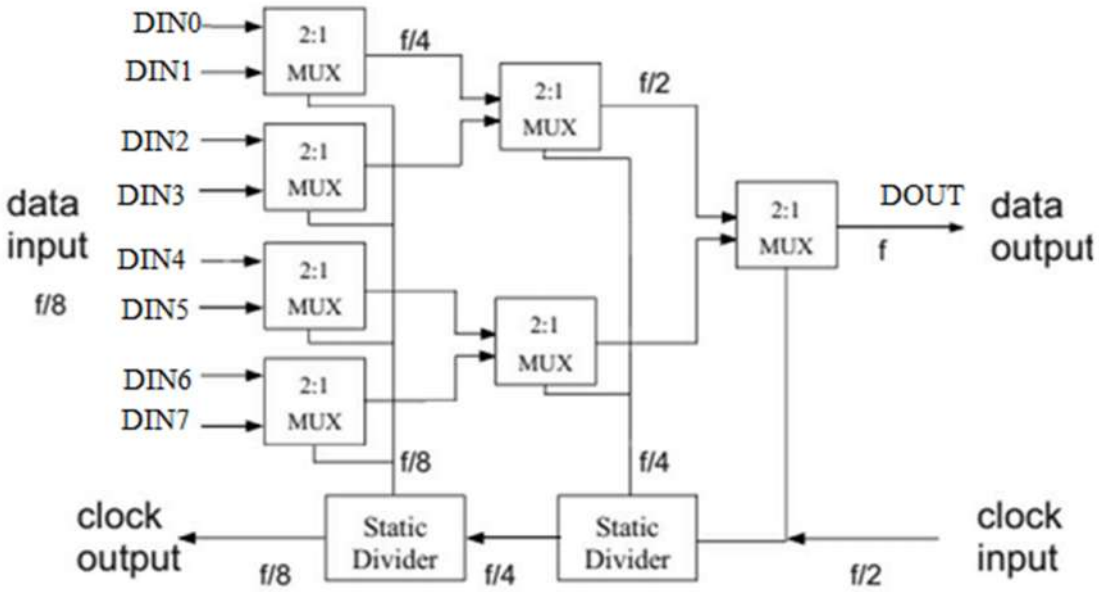


Fig.5.6 Block diagram of 8:1 MUX [16]

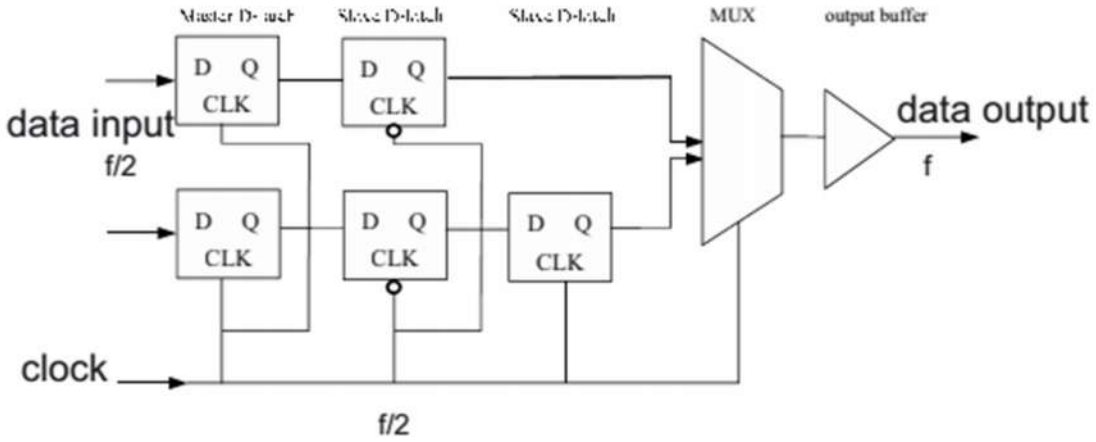


Fig. 5.7 Implementation of 2:1 MUX [16]

5.3 Proposed implementations of Deserializers:

Using above methodology for implementation of serializers, in this section proposed serializers have been presented.

5.3.1 Deserializer employing triple-tail MCML based D-latch with feedback:

Firstly, we propose deserializer which uses triple-tail MCML based D-latch. The design serializes 1.25 Gbps serial data stream to 8-bit parallel data at 156.25 MHz with clock frequency 625 MHz. The simulated result for the signals of the proposed Deserializer for serial data stream "10110000" is presented in Fig. 5.8.

5.3.2 Comparison between deserializers employing different D-latches:

Deserializers have been constructed using different D-latches as their basic block

- MCML D-latch
- MCML D-latch with feedback resistors
- Triple-tail cell based D-latch
- Triple-tail cell based D-latch with feedback

Table 5.1 Comparison between deserializers employing different D-latches

	Deserializer employing			
Parameters	**MCML D-latch**	**MCML D-latch with feedback resistors**	**Triple-tail cell based D-latch**	**Triple-tail cell based D-latch with feedback**
Power (in mW)	3.16	3.16	1.93	1.93
Delay (ps)	210.526	178.34	184.211	163.87
PDP (fJ)	665.26	563.55	355.52	316.27

The results show that triple-tail MCML D-latch with feedback resistors based 1:8 deserializer has improved delay, power and PDP as compared to traditional MCML D-latch based 1:8 deserializer. The delay has decreased from 210 ps to 164 ps which represents an improvement of about 28%. Also the results for power dissipation show an improvement of 64% as compared to deserializer employing traditional MCML based D-latch.. Thus, the proposed triple-tail cell D-latch based implementation of 1:8 demultiplexer, in terms of speed and power for high frequency operations, is best suited.

Because of threshold fluctuation, swing of the output of deserialzers changes to 353mv as compared to without threshold fluctuation which is 400mV.

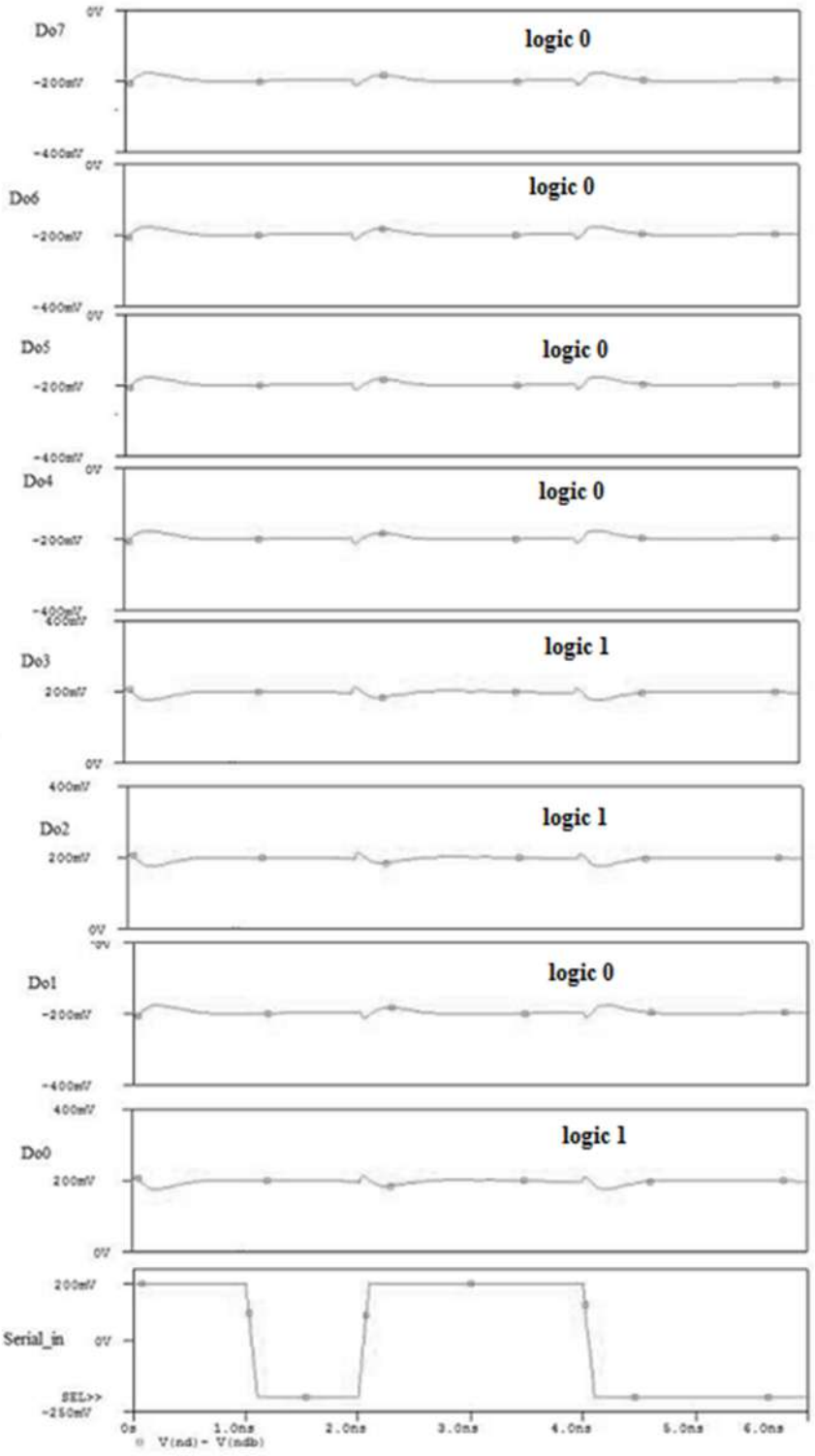


Fig. 5.8 Simulation result of the Deserializer for serial data input "10110000".

5.4 Proposed implementations of Serializers:

Using above methodology for implementation of serializers, in this section proposed serializers have been presented.

5.4.1 Serializer employing triple-tail MCML based D-latch with feedback:

The design serializes 8-bit parallel data at 156.25 MHz into a 1.25 Gbps serial data stream with clocks of frequencies 625 MHz, 312.5 MHz and 156.25 MHz. The simulated result for the signals of the proposed Serializer is presented in **Fig. 5.9**. Here, parallel data input is "1, 1, 1, 0, 0, 1, 1, 1" and used voltages for each individual parallel data input is differential in nature.

5.3.2 Comparison between serializers employing different D-latches:

For comparison, serializers have been constructed using different D-latches as their basic block

- MCML D-latch
- MCML D-latch with feedback resistors
- Triple-tail cell based D-latch
- Triple-tail cell based D-latch with feedback

Table 5.2 Comparison between serializers employing different D-latches

	Serializer employing			
Parameters	**MCML D-latch**	**MCML D-latch with feedback resistors**	**Triple-tail cell based D-latch**	**Triple-tail cell based D-latch with feedback**
Power (in mW)	2.94	2.94	1.85	1.85
Delay (ps)	323.529	279.412	294.34	263.87
PDP (fJ)	951.17	821.47	544.529	488.16

The results show that triple-tail MCML D-latch with feedback resistors based 8:1 serializer has improved delay, power and PDP as compared to traditional MCML D-latch based 8:1 serializer. The delay has decreased from 323 ps to 264 ps which represents an improvement of about 23%. Also the results for power dissipation show an improvement of 59% as compared to deserializer employing traditional MCML based D-latch.. Thus, the proposed triple-tail cell D-latch based implementation of 8:1 serializer, in terms of speed and power for high frequency operations, is best suited.

Because of threshold fluctuation, swing of the output of deserialzers changes to 346mV as compared to without threshold fluctuation which is 400mV.

From area perspective also, less number of transistors are used in triple-tail MCML based D-latch as seen clearly from circuit diagrams of both mentioned in previous chapters, hence less area is required.

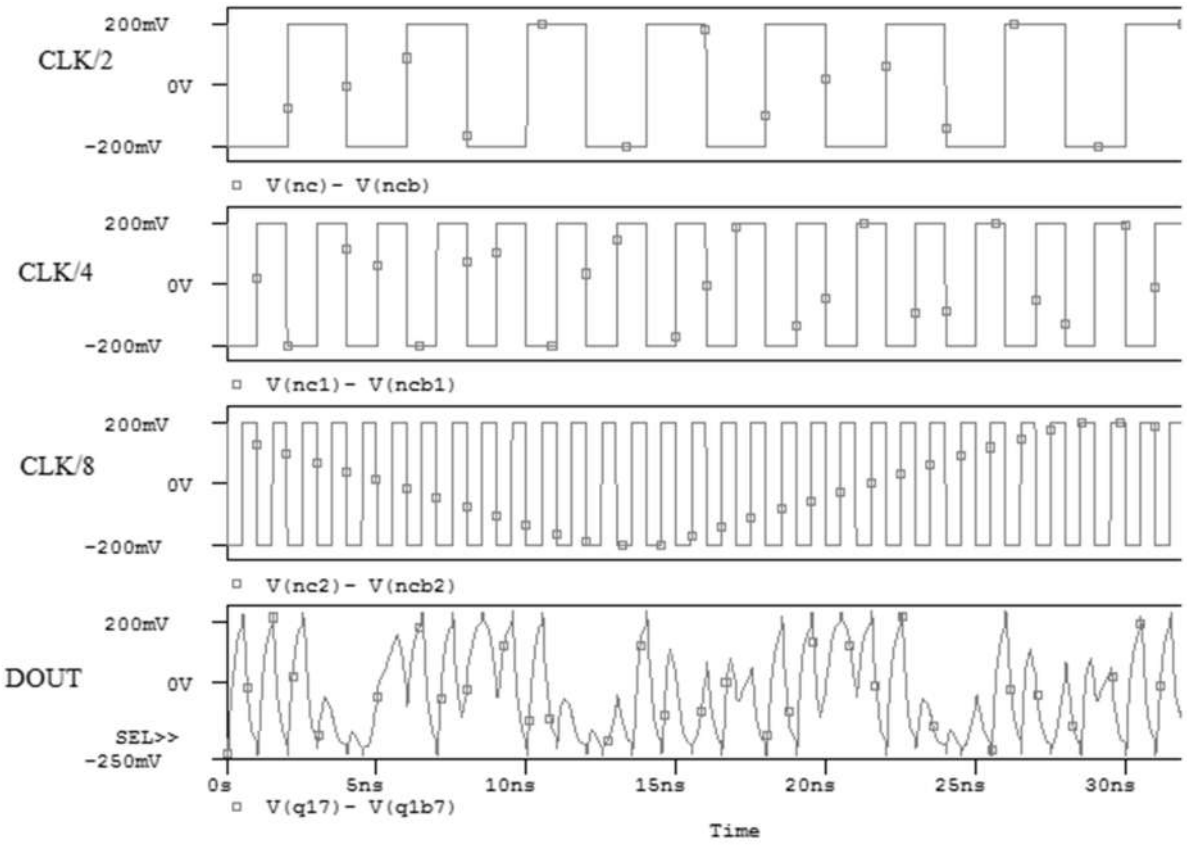


Fig. 5.9 Simulation result of the Serializer for parallel data input "1, 1, 1, 0, 0, 1, 1, 1".

Chapter 6

Conclusion and Future Work

5.1 Conclusion

This thesis focuses on comparison of performance parameters of serializers and deserializers implemented using MCML based D-latch and triple-tail MCML based D-latch, both with and without feedback resistors, and the triple-tail MCML based D-latch with feedback resistors turned out to be more robust, and power efficient and faster serializer and deserializer with covering less area.

First, MCML based D-latch and triple-tail MCML based D-latch has been studied, and the latter topology came out as faster topology and dissipates less power in comparison to traditional MCML based D-latch as it requires lower power supply because it uses one stack of transistors.

Then the impact of threshold voltage fluctuation is considered as because of differential nature of MCML circuits, a little mismatch among devices because of threshold fluctuation its operation is affected tremendously. Effect of NMOS voltage threshold fluctuations have been studied and the swing affected because of threshold voltage fluctuation by 16.17% and in parallel effect of PMOS voltage threshold fluctuations have been derived in both MCML based traditional circuits and triple-tail based d-latch, and the swing affected because of threshold voltage fluctuation among PMOS transistors by 12.07%

To overcome this mismatch, feedback MCML topology has been studied and is also implemented in triple-tail MCML based D-latch, because of which significant improvement in frequency by 74.7% have been observed.

These improved triple-tail MCML based D-latch have been used to construct Serializer/Deserializer, which appears to work at higher frequency, and are more power and area efficient than traditional MCML based D-latch.

5.2 Future Work

While this work attempted to realize more robust, and power efficient and faster serializer and deserializer with covering less area, using feedback resistances between input and output, this same scheme can be implemented in various MCML circuits to reduce the effect of device mismatch due to threshold voltage fluctuation.

This research work can be used in implementation of XOR gate and MUX circuit, implemented using triple tail MCML, which would in all means helps in building the faster gates. Since these circuits are basic building blocks of any arithmetic circuits, hence faster adders, ALUs, CORDIC structure etc. can be constructed and this realm includes many other topologies.

Further, this feedback resistors scheme can also be extended to implement Dynamic MCML based arithmetic structures, which would not only be robust in design and faster than conventional DyCML structures, but also will be power efficient than simple MCML based structures.

References

[1] B. Davari, R. H. Dennard, G. G. Shahidi, "CMOS Scaling for High Performance and Low Power - The Next Ten Years," Proceedings of the IEEE, Vol 83, No. 4, April 1995, p595- 606.

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