CHAPTER-1

INTRODUCTION

1.1 Motivation

The current-mode approach to IC design has clearly had a great impact on IC design. Several new circuits and amplifiers (e.g., the operational floating conveyor or the current-feedback OTA) emerged from this way of thinking. However, there are indeed performance differences between voltage-mode and current-mode circuits. The reason for this is that voltage-mode and current-mode circuits are often built with different design techniques. Voltage-mode circuits often use higher loop gains than current-mode circuits, and current-mode circuits are often made less complex than the voltage-mode circuits. Moreover, current mode circuits are faster than voltage mode circuits.

Analog to Digital Converters (ADCs) are the most commonly used mixed-signal modules which transfer analog blocks output data to digital gates. For example, ADCs are one of the major modules in CMOS sensors where they act as the interface between the sensed environment which has analog data and the sensing network which is usually a digital system. They are also used as interfaces for DSP systems, multimedia systems, and communication networks. Furthermore, ADCs are widely used in current mode multiple-valued memories where they are employed for error correction in refreshing circuitry.

Generally, current mode signal processing has become an alternative for systems with low power supply voltages as the sub-micron technology shrinks, the power supply voltage reduces. Current-mode circuit techniques have some advantages over voltage-mode ones. First, they require lower voltage swing. Second, it is easy to implement basic functions through current mode circuits, like scaling and summation. Third, they increase noise immunity of the system. Furthermore, they provide higher operational speed for the circuit.

The alalog to digital conversion technique proposed in [19] offers a fast conversion as it can potentially convert each two bit in parallel and at the same time. A current comparator proposed in [11] is based on high speed second generation current

conveyor. This project work is carried out successfully by using the ideas of [2], [11] and [19] and has been implemented using 180nm CMOS process parameter with the supply voltage of 1.8V.

1.2 Literature Review

Current mode circuits have used quite regularly due to their wide dynamic range, low voltage operation, wide bandwidth and low power dissipation properties [1]. Comparator is an important part of many analog integrated circuits such as analog to digital converter. Current comparators are used broadly in high data conversion especially in analog to digital converter (ADC). The first current mode comparator is proposed by Traff [2] in 1992. The design structure uses a source follower input stage and a CMOS inverter as a positive feedback. The most important drawback of this comparator is the response time of the circuit which restricts the input frequency range. To improve the above shortcoming a new design is presented in [3] by Huang. This design also improves the properties such as power consumption, offset consideration and wider input dynamic range.

The CMOS current comparator proposed in [4] utilized an offset compensation circuit in order to reduce the offset current due to process mismatch. Cembrano etal [5] presented a nonlinear negative feedback method for the comparator to achieve high-speed for low current and high accuracy. Min and Kim [6] proposed a new comparator using resistive feedback network and the need of offset compensation was removed. Banks and Toumazou reported a power efficient comparator proposed in [8], where advanced positive feedback network is used to improve the circuit characteristics. Tang [10] proposed high speed current comparator by changing the buffer of an existing comparator from class B to class AB operation. Voltage swings are reduced resulting in greater speed for small input currents. A new high-speed current mode comparator proposed in [11] based on second generation current conveyor and positive feedback properties.

The ADCs proposed in [12] and [13] are used in CMOS sensors to interface between the sensed environment and the sensing network. Bell [14] has proposed a generic cell structure of high speed CMOS current mode flash analog to digital converter. Current-mode circuit techniques have some advantages over voltage-mode ones [15]–

[17]. A novel method for converting analog information to digital in current mode is proposed in [19]. In this approach the conversion of each 2 bits at the same time results in fast response.

1.3 Objective and Scope of the Project

The objective of the project is to design two step 4 Bit current mode flash analog to digital converter using current comparator based on CC-II, and also analyze their performance for different values of current and simulate them for minimizing the delay, power and making these circuits electronically tunable.

The analog to digital converters are best suited for the interface between analog and digital environment. The current conveyor based current comparator is best suited for low power, high speed application.

1.4 Organization of Thesis

The thesis is organized as follows:

Chapter 2: It describes the basic of Analog to digital Converter and their characteristics such as gain error, offset error, Integral nonlinearity and Differential nonlinearity. Further different types of voltage mode ADC such as Integrating, Successive approximation, Flash-type, Pipeline, and Algorithmic ADCs are illustrated.

Chapter 3: In this chapter the basic of current conveyor is described. And further first generation current conveyor and second generation current conveyor are illustrated.

Chapter 4: In this chapter the concept of current mirror is illustrated with the basic NMOS current mirror circuit. And it is simulated using SPICE simulation.

Chapter 5: This chapter illustrates the concept of current comparator and current comparators proposed in references are also described. The CC-II based current comparator is also illustrated in this chapter and the simulation is done in PSpice.

Chapter 6: In this chapter the concept of encoding is described through digital encoder. Further 3x2 priority encoder is illustrated and simulated.

Chapter 7: This chapter illustrates the proposed two step current mode flash ADC. The DAC is also illustrated in this chapter. The DAC is simulated in PSpice.

Chapter 8: In this chapter all the building blocks of the proposed current mode flash ADC are simulated individually in PSpice. **Also, the circuit proposed in this dissertation is simulated**. The results are also summarized in this chapter.

Chapter 9: This chapter deals with the conclusion and hints for the future work.

CHAPTER-2

ANALOG TO DIGITAL CONVERTERS

2.1 Introduction

An analog-to-digital converter takes an analog input voltage and after a certain amount of time, produces a digital output code, which represents the analog input.

The basic principle of operation is to use the comparator principle to determine whether or not to turn on a particular bit of the binary number output. It is typical for an ADC to use a digital-to-analog converter (DAC) to determine one of the inputs to the comparator. The general block diagram of an ADC is shown in fig 2.1.

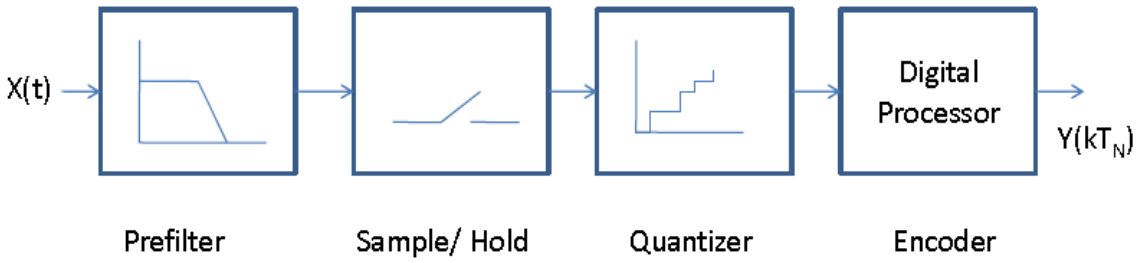


Fig 2.1: General block diagram of an ADC

A prefilter is called an antialiasing filter is necessary to avoid the aliasing of higher frequency signals back in to the baseband of the ADC. The antialiasing filter is followed by a sample and hold circuit that maintains the input analog signal to the ADC constant during the time this signal is converted to an equivalent output digital code. This period of time is called the conversion time of the ADC. The conversion is accomplished by a quantization step. The nature of quantizer is to segment the reference into sub ranges. Typically, there are 2^N-1 sub ranges, where N is the number of bits of the digital output code. The quantization step finds the sub range that corresponds to the sample analog input. Knowing this sub range allow the digital processor to encode the corresponding digital bits. Thus within the conversion time a sampled analog input signal is converted to an equivalent digital output code.

2.2 Characteristics of ADC

- Offset error
- Gain error
- Integral nonlinearity (INL)
- Differential nonlinearity (DNL)
- Aliasing

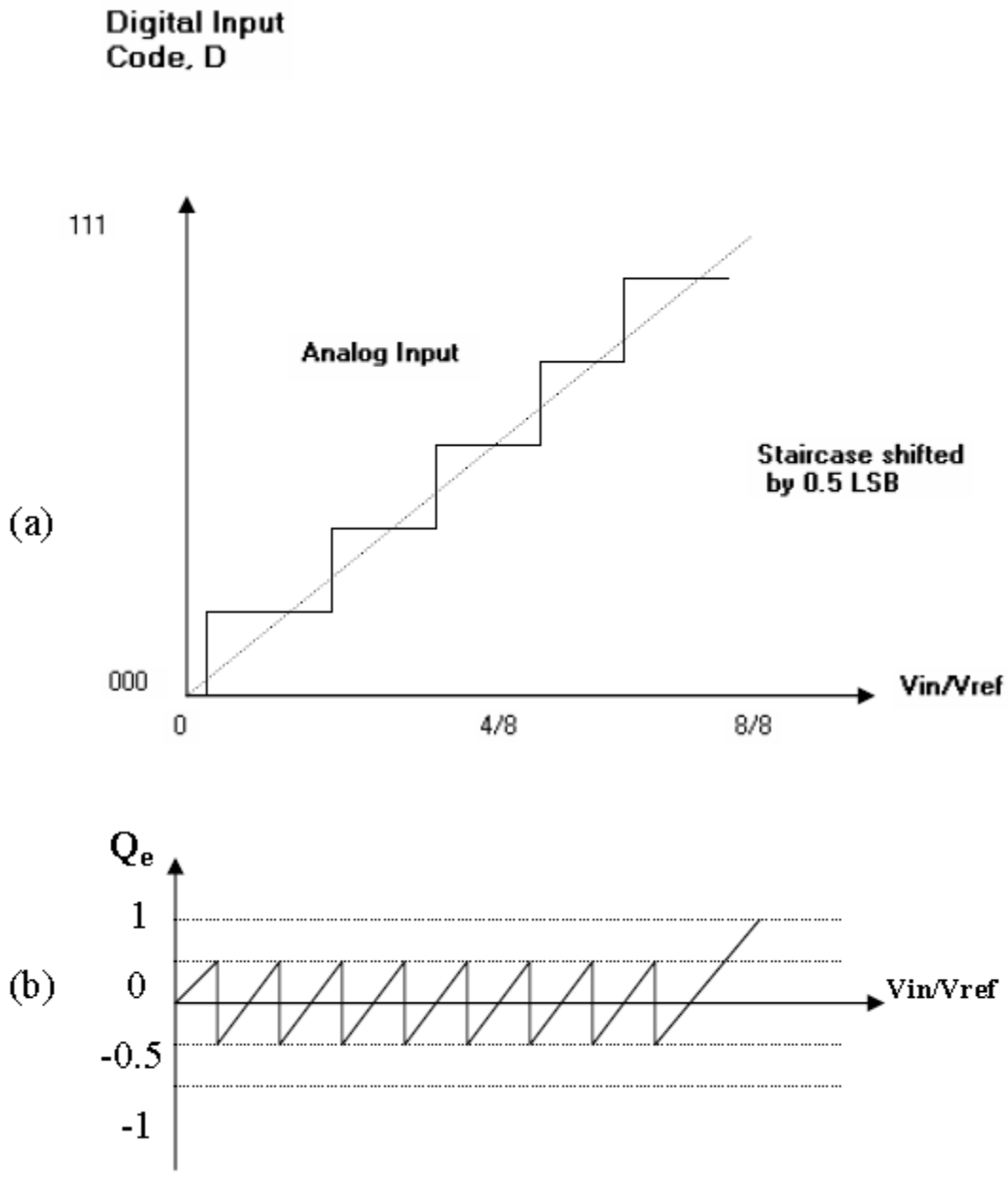


Fig 2.2: (a) Transfer curve for an ideal 3-bit A/D Converter with (b) Quantization error centred about zero.

Fig 2.2(a) shows the digital output D of a 3-bit A/D converter plotted against the analog input V_{in}. Since the input signal is a continuous signal and the output is discrete, the transfer curve of the A/D converter resembles that of a staircase. Another fact to observe is that the 2^N quantization levels correspond to the digital output codes 0 to 7. Thus, the maximum output of the A/D converter will be 111 (2^N-1), corresponding to the value for which $V_{in} / V_{ref} \geq 7/8$. Fig 2.2(b) corresponds to the error caused by the quantization.

The value of 1 LSB for this A/D converter can be calculated using the following equation-

$$1 \text{ LSB} = \frac{V_{REF}}{2^N} \quad \text{..... (2.1)}$$

Quantization Error

Since the analog input is an infinite valued quantity and the output is a discrete value, an error will be produced as a result of the quantization. This error, known as quantization error, Q_e, is defined as the difference between the actual analog input and the value of the output (staircase) given in voltage. It is calculated as-

$$Q_e = V_{in} - S_{taircase} \quad \text{..... (2.2)}$$

where the value of the staircase output, $S_{taircase}$ can be calculated by

$$V_{staircase} = D.\frac{V_{REF}}{2^N} = D.V_{LSB} \quad \text{..... (2.3)}$$

Where D is the value of the digital output code and V_{LSB} is the value of 1 LSB in Volts.

Offset error

Let us shift the infinite resolution characteristic line horizontally until the quantization noise is symmetrical when referenced to this line. The horizontal difference between this line and the infinite resolution characteristic that passes through the origin is “offset error”.

Gain error

It is a difference between the actual characteristics and the infinite resolution characteristic, which is proportional to the magnitude of the input voltage. The gain error can be thought of as a change in the slope of the infinite resolution line above or below a value of one. Gain error can be measured as the horizontal difference in LSBs between actual and ideal finite resolution characteristics at highest digital code.

Integral nonlinearity (INL)

It is the maximum difference between the actual finite resolution characteristics and the ideal finite resolution characteristic measured vertically in percent of LSBs.

INL defines the linearity of the overall transfer curve and can be defined as-

INL= Output value for input code- Output value of the reference line at that point.

Differential nonlinearity (DNL)

It is define as the measure of the separation between adjacent codes measured at each vertical step in percent of LSBs. The differential nonlinearity of an ADC can be written as

$$DNL = (D_{cx} - 1) \text{ LSBs} \quad \text{..... (2.4)}$$

Where, D_{cx} is the size of the actual vertical step in LSBs.

Aliasing

The sampling of the input signal should be done at such a rate that is determined by the Nyquist Criterion. Nyquist criterion defines how fast the sampling rate needs to represent an analog signal accurately. This criterion requires that the sampling rate be at least twice the highest frequency contained in the analog signal.

$$F_{sampling} = 2.F_{MAX} \quad \text{..... (2.5)}$$

Where, $F_{sampling}$ is the sampling frequency required to accurately represents the analog signal and F_{MAX} is the highest frequency of the sampled signal. If the sampling is

done at a rate less than that specified by the Nyquist Criterion, a phenomenon called aliasing would occur.

Aliasing can be eliminated either by sampling at higher frequencies or by filtering the analog signal before sampling and removing any frequencies that are greater than one half the sampling frequency. A pre-alias filter can be used to eliminate any unknown harmonics that could result in aliasing.

2.3 TYPES OF ADC

There are five main types of ADC architectures- Integrating, Successive approximation, Flash-type, Pipeline, and Algorithmic ADCs. Each has benefits that are the unique to that architecture and span the spectrum high speed and resolution.

2.3.1 Integrating ADC

This type of ADC performs the conversion by the input signal and correlating the integrating time with a digital counter. Known as single and dual-slope ADCs, these types of converters are used in high resolution applications but have relatively slow conversions. However, they are very inexpensive to produce and are commonly found in slow-speed, cost conscious applications.

Single-slope Architecture

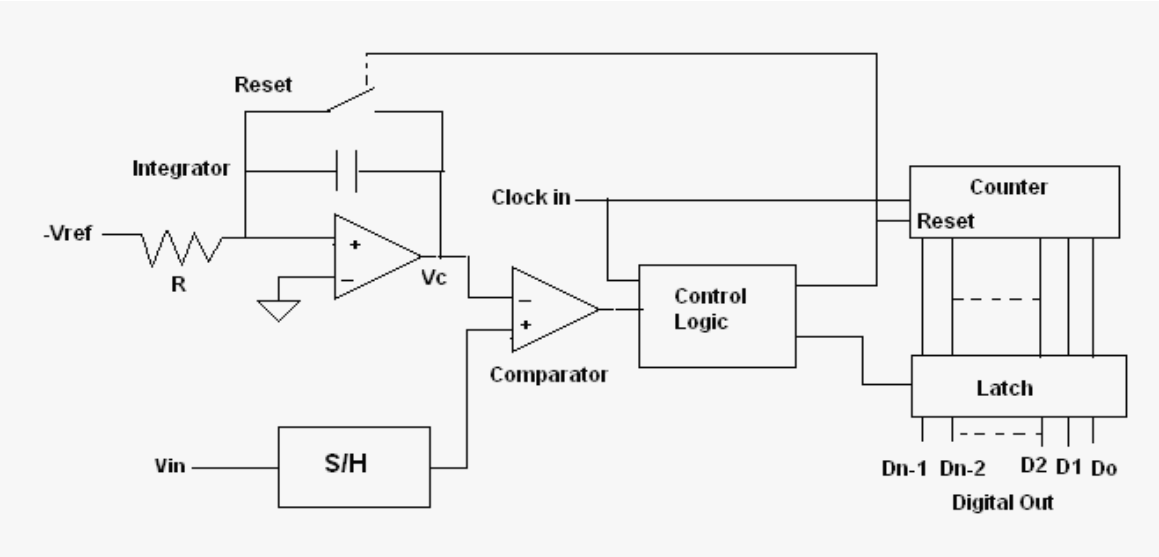


Fig 2.3: Block diagram of single-slope ADC

Fig 2.3 shows the single-slope converter in the block diagram form. A counter determines the number of clock pulses that are required before the integrated value of a reference voltage is equal to the sampled input signal. The number of clock pulses is proportional to the actual value of the input, and the output of the counter is the actual digital representation of analog voltage.

Since the reference is a DC voltage, the output of the integrator should start at zero and linearly increase with the slope that is dependent on the gain of the integrator. The reference voltage is defined as negative so that the output of the inverting integrator is positive. At the time when the output of the integrator surpasses the value of S/H output, the comparator switches states, thus triggering the control logic to latch the value of the counter. The control logic also resets the system for the next sample. Fig 2.4 illustrates the behaviour of the integrator output and the clock.

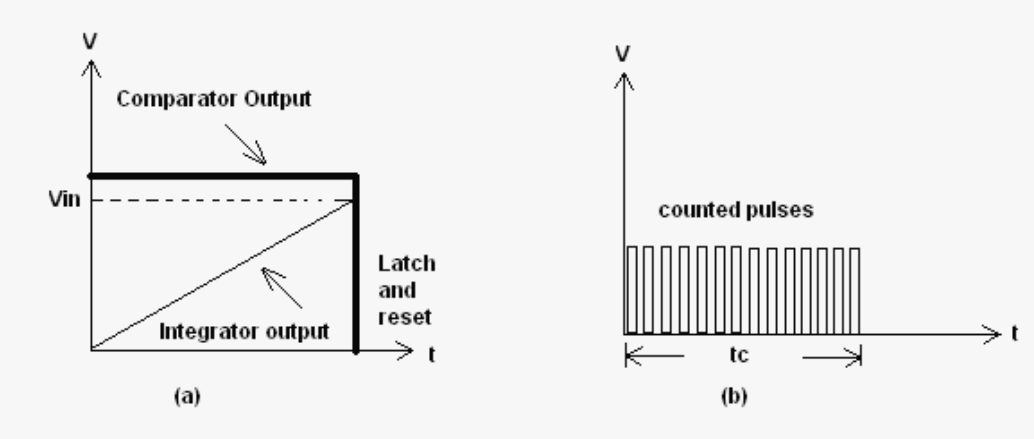


Fig 2.4: Single slope ADC timing diagrams for (a) The comparator inputs and outputs (b) The resulting counted pulses

If the input voltage is very small, the conversion time is very short, since the counter has to increment only a few times before the comparator latches the data. However, if the input voltage is at its full-scale value, the counter must be many times faster than the bandwidth of the input signal.

The conversion time, t_c, is dependent on the value of the input signal and can be described as-

$$tc = \frac{Vin}{Vref} .2^N . Tck \qquad \text{..... (2.6)}$$

Where, T_{ck} is the period of the clock. The sampling rate is inversely proportional to the conversion time and can be written as-

$$fsample = \frac{Vref}{Vin.\,2^N}\,fck \qquad \ldots\ldots\ldots (2.7)$$

Dual-slope Architecture

A slightly more sophisticated design known as the dual-slope integrating ADC shown in Fig 2.5 eliminates most of the problems encountered when using the single slope converter.

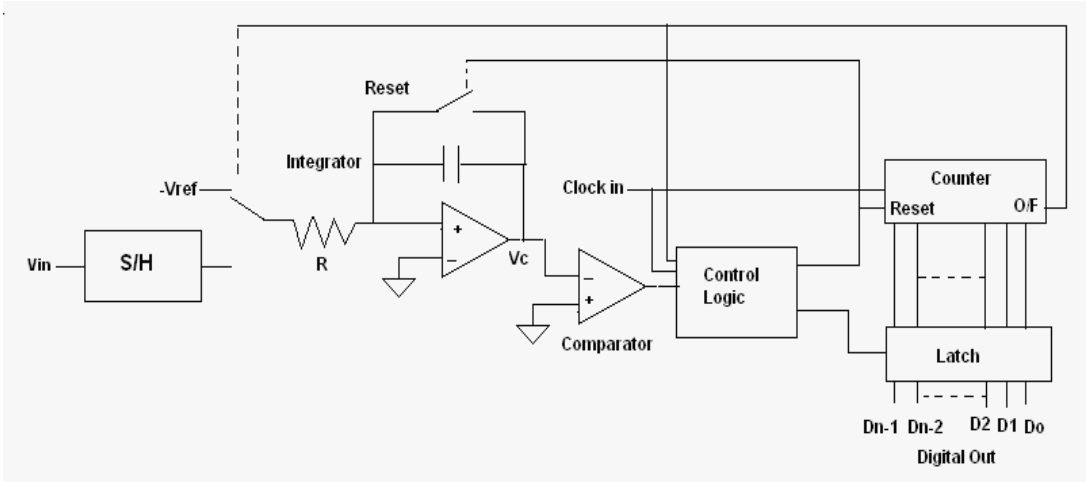


Fig 2.5: Block diagram of dual-slope ADC

Here two integrations are performed, one on the input signal and one on V_{ref}. The input voltage in this case is assumed to be negative, so that the output of the inverting integrator results in a positive slope during the first integration.

Fig 2.6 illustrates the behaviour for the two separate pulses.

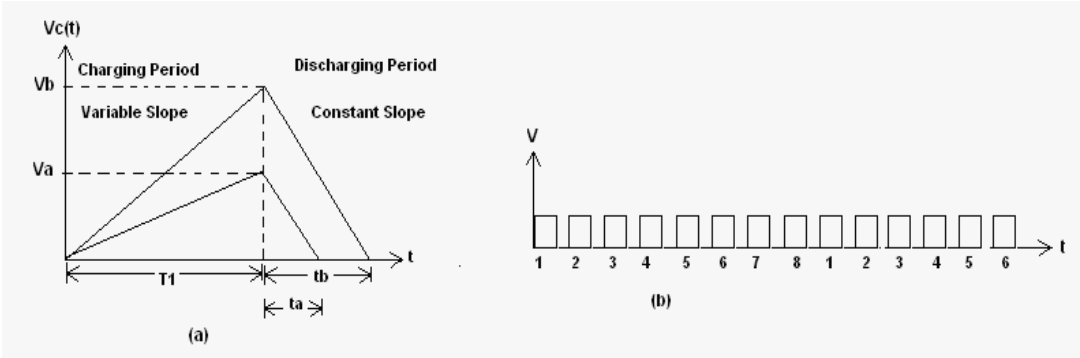


Fig 2.6: Integrating periods and counter output for two separate samples of a 3-bit dual slope ADC

The first integration is of fixed length, dictated by the counter, in which the sampled-and-held signal is integrated, resulting in the first slope. After the counter overflows and is reset, the reference voltage is connected to the input of the integrator. Since V_{in} was negative and the reference voltage is positive, the inverting integrator output will begin discharging back down to zero at a constant slope. A counter again measures the amount of time for the integrator to discharge, thus generating the digital output.

The first slopes varies according to the value of the input signal, while the second slope dependent only on V_{ref}, is constant. Similarly, the time required to generate the first slope is constant, since it is limited by the size of the counter. However the discharging period is variable and results in the digital representation of input voltage.

2.3.2 Successive Approximation ADC

The successive approximation converter basically performs a binary search through all possible quantization levels before converging on final digital answer. The block diagram is shown in figure 2.7. An N-bit register controls the timing of the conversion where N is the resolution of the ADC. V_{in} is sampled and compared to the output of the DAC. The comparator output controls the direction of the binary search and the output of the successive approximation register (SAR) is the actual digital conversion.

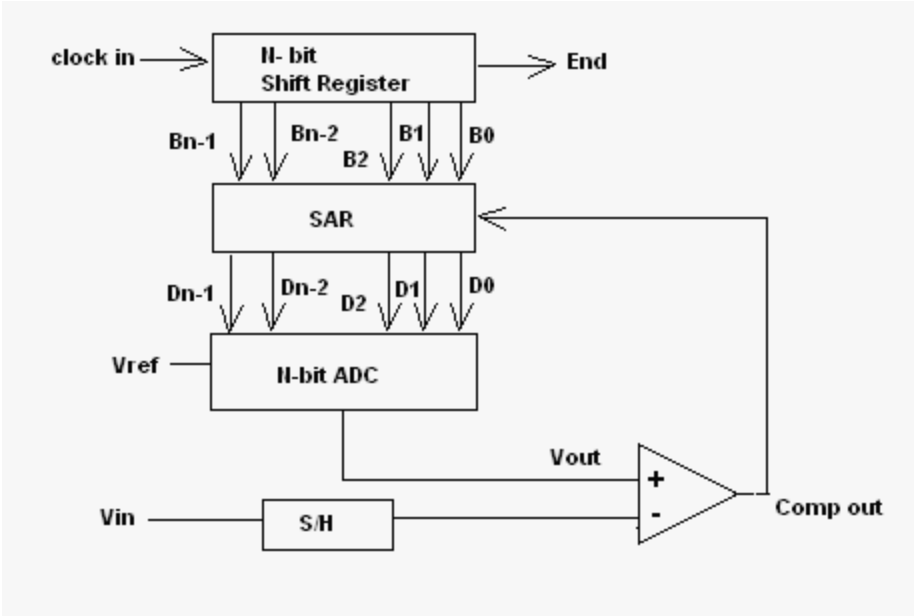


Fig 2.7: Block diagram of successive approximation ADC

The successive approximation algorithm is as follows-

I. A 1 is applied to the input of the shift register. For each bit converted, the 1 is shifted to the right 1-bit position. $B_{N-1} = 1$ and B_{N2} through $B_0=0$.

II. The MSB of the SAR, D_{N-1}, is initially set to 1, while the remaining its, D_{N-2} through D_0, are set to 0.

III. Since the SAR output controls the DAC and the SAR output is 100…0, the DAC output will be set to $V_{ref}/2$.

IV. Next V_{in} is compared to $V_{ref}/2$. If $V_{ref}/2$ is greater than V_{in}, then the comparator output is a 1 and the comparator resets D_{N-1} to 0. If $V_{ref}/2$ is less than V_{in}, then the comparator output is a 0 and the comparator resets D_{N-1} to 1. D_{N-1} is the actual MSB of the final digital output code.

V. The 1 applied to the shift register is then shifted by one position so that B_{N-2} =1 while the remaining all bits are 0.

VI. D_{N-2} is set to 1, D_{N-3} through D_0 remain 0, while D_{N-1} remains the value from the MSB conversion. The output of the DAC will now either equal $V_{ref}/4$ (if D_{N-1} =0) or $3V_{ref}/4$ (if D_{N-1} =1).

VII. Next, V_{in} is compared to the output of the DAC. If the DAC output is greater than V_{in}, the comparator resets D_{N-2} to 0. If V_{in} is less than the DAC output, D_{N-2} remains a 1.

VIII. The process repeats until the output of DAC converges to the value of V_{in} within the resolution of the converter.

2.3.3 Flash ADC

A Flash ADC (also known as a Direct conversion ADC or parallel ADCs) is a type of analog-to-digital converter that uses a linear voltage ladder with a comparator at each "rung" of the ladder to compare the input voltage to successive reference voltages. Flash ADCs are made by cascading high-speed comparators. Flash or the parallel converters have the highest speed of any type of ADC. They utilize one comparator per quantization level (2^N - 1) and 2^N resistors. The reference voltage is divided into 2^N values, each of which is fed into comparator. The input voltage is compared with each reference value and results in a thermometer code at the output of the comparators. This architecture is known as thermometer code encoding. This name is used because the

design is similar to a mercury thermometer, in which the mercury column always rises to the appropriate temperature and no mercury is present above that temperature. The thermometer code is then decoded to the appropriate digital output code. A thermometer code will exhibit all zeroes for each resistor level if the value of V_{in} is less than the value on resistor string and ones if V_{in} is greater than or equal to voltage on the resistor string. A simple 2^N-1: N digital thermometer decoder circuit coveters the compared data into an N-bit digital word.

The architecture of Flash ADC is shown in Fig 2.8.

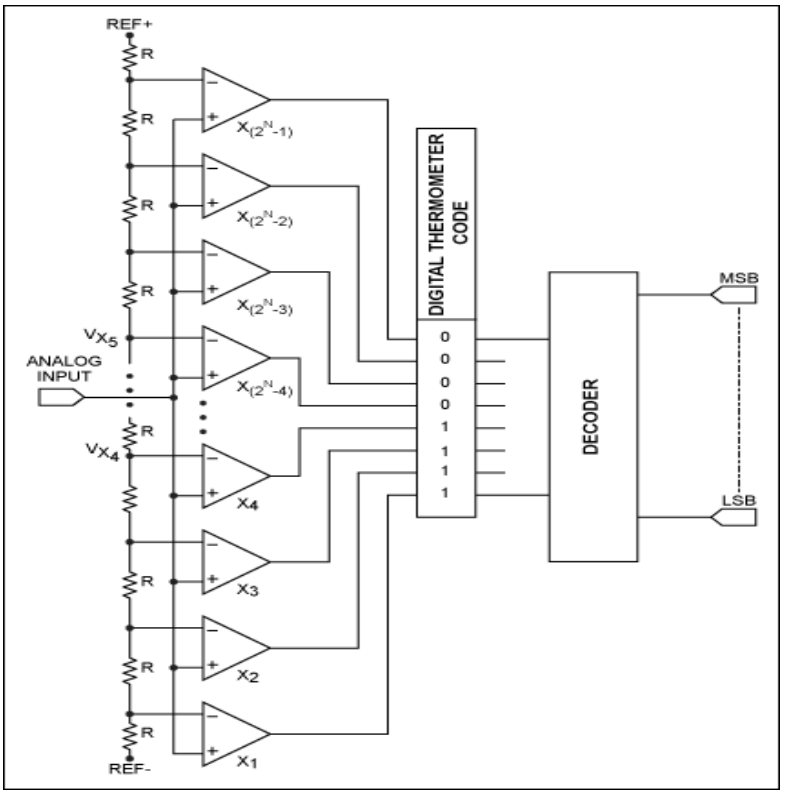


Fig 2.8: Flash ADC architecture

The obvious advantage of this circuit is the speed with which one conversion can take place. Each clock pulse generates an output digital word. The advantage of having high speed is however counter balanced by the doubling of area with each bit of increased resolution. The disadvantages of Flash ADC are the area and power requirements of the 2^N-1 comparators. The speed is limited by the switching of the comparator and the digital logic.

2.3.4 Pipelined ADC

The pipeline ADC is an N-step converter, with 1-bit being converted per stage. Able to achieve high resolution (10-13 bits) at relatively fast speeds, the pipeline ADC consists of N-stages connected in series. The block diagram of pipeline ADC is shown in Fig 2.9.

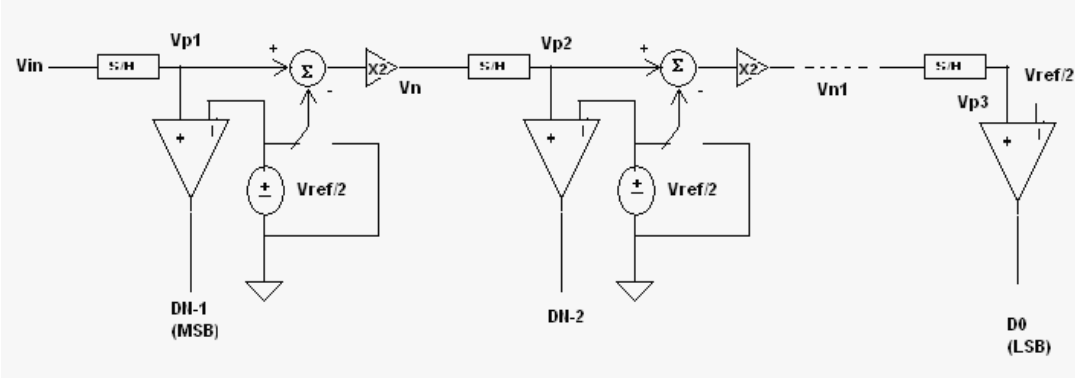


Fig 2.9: Block diagram of Pipeline ADC

Each stage contains a 1-bit ADC (a comparator), a sample and hold, a summer and a gain of two amplifiers.

Each stage of converter performs the following operations-

I. After the input signal has been sampled, it is compared to $V_{ref}/2$. The output of each comparator is the bit conversion for that stage.

II. If $V_{in}>V_{ref}/2$ (comparator output is 1), $V_{ref}/2$ is subtracted from the held signal and result is passed to the amplifier. If $V_{in}<V_{ref}/2$ (comparator output is 0), then the original input signal is passed to the amplifier. The output of each stage in the converter is referred to as the *residue*.

III. Multiply the result of the summation by 2 and pass the result to the sample and hold of the next stage.

A main advantage of the pipeline converter is its high throughput. After an initial delay of N clock cycles, one conversion will be completed per clock cycle. While the residue of the first stage is being operated on by the second stage, the first stage is free to

operate on next samples. Each stage operates on the residue passed down from the previous stage, thereby allowing for fast conversions.

The disadvantage is having initial N clock cycle delay before the first digital output appears. The severity of disadvantage is, of course, dependent on the application.

One interesting aspect of this conversion is its dependency on the most significant stages for accuracy. A slight error in the first stage propagates through the converter and results in a much larger error at the end of the conversion. Each succeeding stage requires less accuracy than the one before, so special care must be taken when considering the first several stages.

2.3.5 Algorithmic ADC

The algorithmic ADC also called cyclic or recirculating converter was has been known and utilized since in various forms since 1960s.

A block diagram of the converter is shown in Fig 2.10.

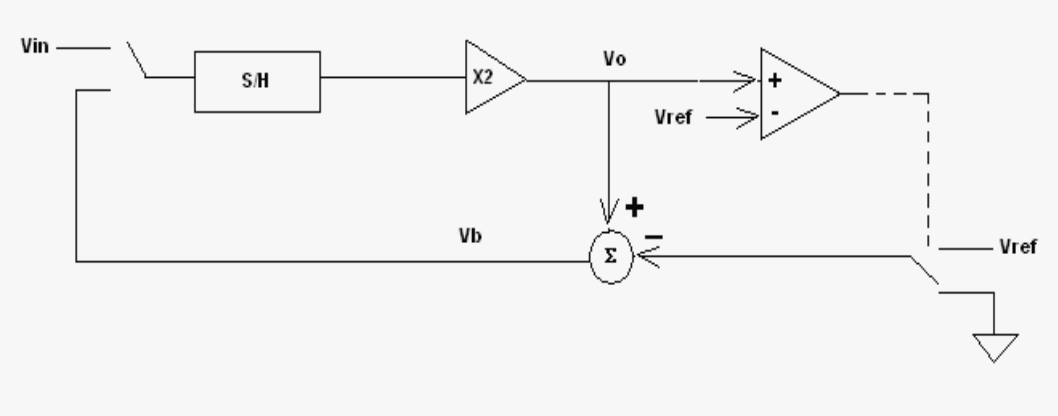


Fig 2.10: Block diagram of the Algorithmic ADC

The algorithmic ADC consists of an analog signal loop which contains-

- A sample-and-hold amplifier
- A multiply-by-two amplifier
- A comparator
- A reference subtraction circuit

The operation of the converter consists of first sampling the input signal onto the sample/hold amplifier. This is done by selecting the input signal instead of the loop signal using select switch. The input signal is then passed to the multiply-by-two amplifier where it is amplified. To extract the digital information from the input signal, the resultant signal, V_o is compared to the reference. If it is larger than the reference, the corresponding bit is set to 1 and the reference is then subtracted off from V_o. Otherwise, this bit is set to 0 and the signal V_o is kept unchanged. The resultant signal, denoted by V_b is then transferred, by means of switch. Back into the analog loop for further processing. This process continues until the desired numbers of bits have been obtained, whereupon a new sampled value of the input signal will be processed. Thus, the digital data comes out from the converter in a serial manner, the MSB first.

The algorithmic ADC can be constructed with very little precision hardware. Its implementation in a monolithic technology can therefore be relatively area-sparing. It also possesses inherent S/H capability because the S/H amplifier is an integral part of the converter. It also possesses floating-point operation capability i.e. the input signal can be amplified 2^n times before the A/D conversion commences. These properties are very desirable for the design of single-chip complete data acquisition system.

CHAPTER-3

CURRENT CONVEYOR

3.1 Introduction

The current conveyor has been around since the original design, or CC-I (which can be regarded as an ideal transistor), was initially proposed by Smith and Sedra in 1968. CC-I was then replaced by a more versatile second-generation device in 1970.

3.2 First Generation Current Conveyor (CC-I)

- It is a 3 terminal device.
- If a voltage is applied to terminal Y, an equal potential will appear on the input terminal X.
- An input current I being forced into terminal X will result an equal amount of current flowing into terminal Y.
- The current I will be conveyed to output terminal Z such that terminal Z has the characteristics of a current source, of value I, with high output impedance.
- Potential of X being set by that of Y, is independent of the current being forced into port X.
- Current through port Y being fixed by X is independent of the voltage applied to Y.

The small signal diagram of CC-I is shown in Fig 3.1 and the representation of CC-I is shown in Fig 3.2.

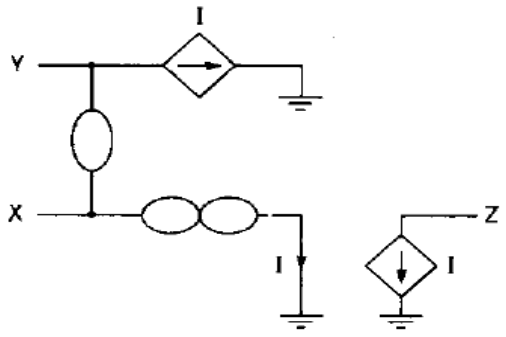


Fig 3.1: Small signal diagram for CC-I

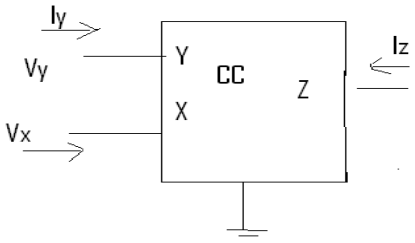


Fig 3.2: Representation for CC-I

MOS implementation

The MOS implementation of first generation current conveyor is shown in Fig 3.3. NMOS transistors M1 and M2 form a current mirror that forces the drain currents of the PMOS transistors M3 and M4 to be equal and hence the voltages at the terminals X and Y are forced to be equal.

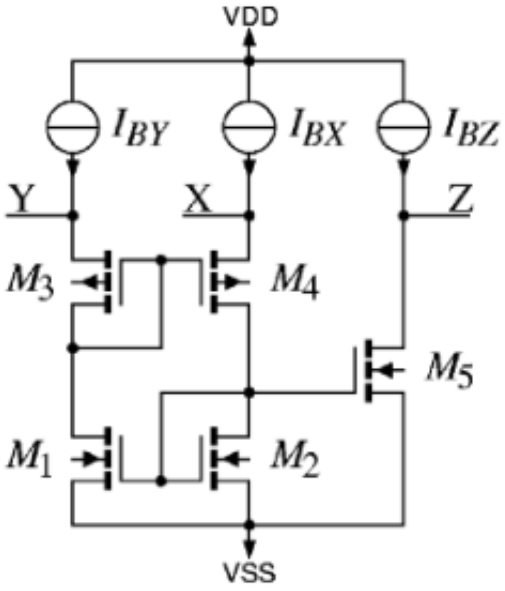


Fig 3.3: MOS implementation of CC-I

The input and output characteristics of CC-I can also be described by the following mathematical matrix:

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix}$$

Where, the variables represent total instantaneous quantity. Note the +ve sign applies for Current Conveyor-I in which both Z and X flow into the conveyor denoted Current Conveyor-I+. The –ve sign apply for the opposite polarity case, denoted Current Conveyor-I-.

3.3 Second Generation Current Conveyor (CC-II)

- It is a four terminal device.
- If a voltage is applied to terminal Y, an equal potential will appear on the input terminal X
- The current in node Y=0
- The current I will be conveyed to output terminal Z such that terminal Z has the characteristics of a current source, of value I, with high output impedance.
- Potential of X being set by that of Y, is independent of the current being forced into port X
- Terminal Y exhibits an infinite input impedance

The representation of CC-II is shown in Fig 3.4.

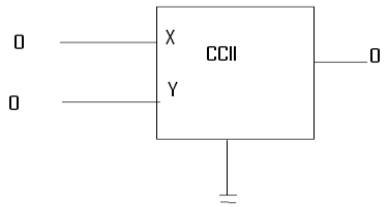


Fig 3.4: Representation of CC-II

To increase the versatility of the current conveyor, a second version in which no current flows in terminal Y was introduced. This building block has since proven to be more useful than Current Conveyor-I. Current Conveyor-II is described by following matrix:

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix}$$

Thus the terminal Y exhibits infinite input impedance. The voltage at X follows that applied to Y thus X exhibits zero input impedance. The current supplied to X is conveyed to the high impedance output Z where it is supplied with either positive polarity (in Current Conveyor-II+) or negative polarity (in Current Conveyor-II-). Subsequently, this current is transferred to the output node via a complementary pair of current mirrors. The small signal diagram of CC-II is shown in Fig 3.5.

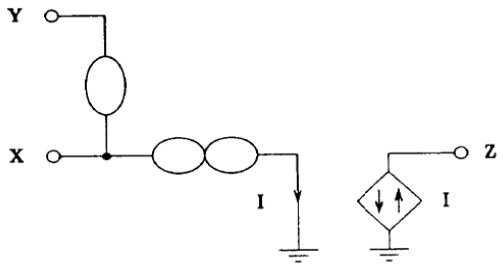


Fig 3.5: small signal diagram of CC-II

By applying a voltage to Y terminal, an identical voltage will appear in node X with no current flow into the Y terminal. The voltage in the X node will results in a current flow to the X node as well as an equal current in node Z. The CCII circuit has some important characteristics such as low input impedance for input current in the node X, high output impedance in the node Z, and low power low voltage design capability. These are very useful options for improving the current mode comparators performance.

3.4 Comparison of Current Conveyor with op-amp

A current conveyor is a building block similar to an operational amplifier and which, when used in conjunction with other components such as resistors, capacitors and diodes, can implement several useful analog sub-systems such as amplifiers, integrators, and rectifiers.

The following subsections make an argument in favour of the current conveyor as an alternative to the simple op-amp.

Area Requirement

A standard simple op-amp uses 10 transistors, a compensation capacitor, and a bias stage. A common version of the current conveyor uses 12 transistors and a bias stage. These two are comparable in area requirements. An op-amp designed for higher frequency operation could use the same number of transistors, but would have higher power consumption.

Compensation

An operational amplifier-based sub-system usually requires negative feedback. However, where the open loop response A(s) of an uncompensated op-amp is greater than unity in magnitude, and the phase shift nears 180°, there can be instability. For this

reason, a compensation capacitor is used to reduce the unity-gain frequency of the op-amp to a point with larger phase margin, thus ensuring stable operation. This procedure results in an op-amp incapable of producing significant gains at high frequencies. However, current conveyor-based building blocks do not use feedback. Stability is ensured since the gains in current and voltage from one node to another are unity.

There is thus no need to compensate a current conveyor. A current conveyor-based design may thus be able to operate at higher frequencies than its op-amp-based counterpart, and still produce significant gains at a savings in silicon area.

Constant Bandwidth

Another advantage of using current conveyors rather than op-amps is that current conveyor-based amplifiers have a constant bandwidth, independent of gain. This is in contrast to op-amp-based amplifiers, which have a constant gain-bandwidth product.

CHAPTER-4

CURRENT MIRRORS

4.1 Introduction

The characteristics of current mirrors find applications in almost all analog and mixed mode circuit structure. Depending on the characteristics of the input output ports, several implementations for the current mirrors are available. The selection of a suitable current mirror for a particular application becomes important, which needs better understanding of all types of current mirrors, so that an appropriate current mirror can be selected.

Current mirrors are used either as active load or as biasing networks. The use of current mirrors in biasing structures results in better insensitivity to the variations in power supply and temperature. They are more economical in terms of die area if used as active loads.

4.2 Basic Current Mirror

As the name suggests, a current mirror is expected to perform the similar functions with the electrical current as the plane optical mirror does for the optical signals. Hence a current mirror is a three terminal device whose output current at any instant of time is independent of voltage applied across its terminals and depends solely on the input current. The output current is the scaled version of the input current. Thus, in other words, a current mirror reverses the direction of current injected into the low impedance input port and allows its true or scaled version to flow into a high impedance output port. However the direction of the output current can also be reversed.

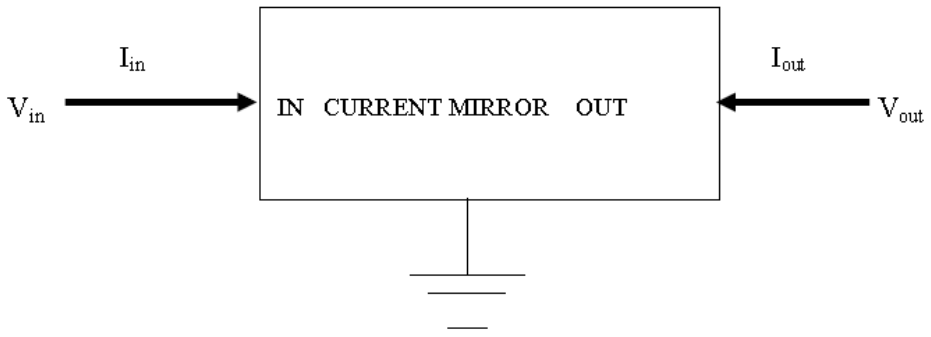


Fig 4.1: Block representation of a Current Mirror

For any high performance system, a current mirror must possess the following characteristics:

- Current transfer ratio, which is precisely set by the (W/L) ratios, independent of temperature.
- Very high output impedance (high R_{out} and low C_{out}). As a result, the output current is independent of output voltages.
- Low input resistance (R_{in}).
- Low input and output compliance voltages.

Almost all analog circuit structures whether they operate as current mode devices or voltage mode devices use current mirror in their design. To name a few such devices, following devices are based on the use of the current mirrors.

- Operational amplifiers.
- Operational trans-conductance amplifiers.
- Operational trans-resistance amplifiers.
- Current feedback amplifiers.
- Current conveyors.
- Operational floating conveyors.
- Digital to analog converters.
- Analog to digital converters.

4.3 Current Mirror Structure

Figure 4.2 illustrate the simple NMOS current mirror structure. In no-saturation region the MOSFET is not a good current source. Hence, it is assumed that both the transistors are in saturation region.

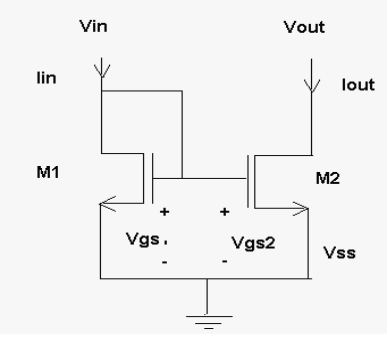


Fig 4.2: Simple current mirror structure

The voltage across the output transistor M2 must be larger than $V_{eff} = (V_{GS} - V_T)$. If the finite output impedance of the transistors are ignored, and it is assumed that both transistors have same size, then M1 and M2 will have same current since they both have same gate source voltage. In the most general case the current transfer function which is defined as the ratio of mirrored current (I_{out}) to the input current (I_{in}) is given by-

$$\frac{Iout}{Iin} = \left[\frac{L_1 W_2}{L_2 W_1}\right]\left[\frac{V_{GS} - V_{T2}}{V_{GS} - V_{T1}}\right]^2\left[\frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}\right]\left[\frac{K_2}{K_1}\right] \quad \text{... (4.1)}$$

Normally, the components of current mirror are processed on the same integrated circuit and all the physical parameters (V_T, K', etc) are identical for both M1 and M2. As a result, the previous equation simplifies to-

$$\frac{Iout}{Iin} = \left[\frac{L_1 W_2}{L_2 W_1}\right]\left[\frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}\right] \quad \text{... (4.2)}$$

If $V_{DS2} = V_{DS1}$, then the above equation further reduces to

$$\frac{Iout}{Iin} = \left[\frac{L_1 W_2}{L_2 W_1}\right] \quad \text{... (4.3)}$$

Thus the current transfer ratio is under the control of a circuit designer.

However the ideal conditions do not exist and there are three sources of non-idealities in a current mirror. There is finite output impedance and the input impedance is also not zero. These parameters are given as

$$V_{in}(\min) = V_{DS}(\text{sat}) + V_T \quad \text{... (4.4)}$$

$$V_{out}(\min) = V_{DS}(\text{sat}) \quad \text{... (4.5)}$$

$$R_{in} = \frac{1}{g_{m1}} \quad \text{... (4.6)}$$

$$R_{out} = \frac{1}{g_{O2}} = \frac{1}{\lambda I_{DQ2}} \quad \text{... (4.7)}$$

There is a trade off between output impedance (R_{out}) and output capacitance (C_{out}). Bigger size transistors achieve higher R_{out}, which is always desired for a current mirror. But there will be higher C_{out} associated bigger size transistors, which obviously degenerates the frequency response of a current mirror.

The advantages offered by a simple current mirror include its simple architecture and high output voltage swing capabilities. However, these mirrors are generally plagued with low output impedance characteristics. This low output impedance may not be sufficient for many applications. Thus there is a need to investigate some other circuit structures for the current mirror applications.

CHAPTER-5

CURRENT COMPARATOR

5.1 Introduction

Comparators have always been, and are still, an important part of electronic systems. Analogue designers have become more interested in current-mode circuits. Current mode circuits have used due to their low voltage operation, wide bandwidth and low power dissipation properties. Comparator is an important component of many analog integrated circuits. Current comparators are used broadly in high data conversion especially in analog to digital converter (ADC).

Comparators are ubiquitous components for many analog systems including data convertors and other front-end signal processing applications. With the ever shrinking feature size of devices, the need for high speed and low voltage operation, designers are considering current-mode implementations.

Simple current comparator

The circuit of simple current comparator is shown in the Fig 5.1.The NMOS current mirror is used to mirror the I_{in-} current and the PMOS current mirror is used to mirror the I_{in+} current to the output node and the difference of both the current is shown in voltage at output node.

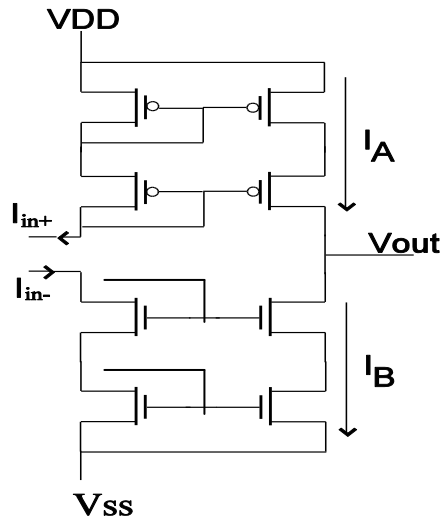


Fig 5.1: Simple current comparator

The first high-speed, low input impedance current comparator was reported by Traff [2] in 1992. The design uses a source follower input stage and a CMOS inverter as a positive feedback is shown in Fig 5.2. Compared with voltage mode comparators the most important drawback of this comparator is the response time of the circuit which restricts the input frequency range.

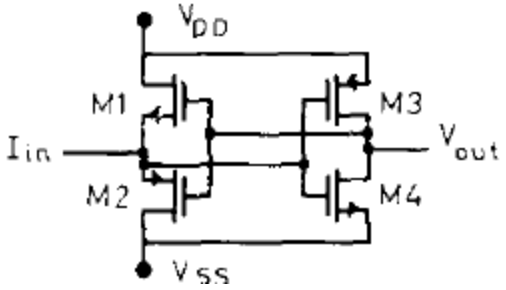


Fig 5.2: Traff's current comparator structure

The input resistance of this structure is approximately **l/gm.** The purpose of using a source follower input stage is to obtain low resistance and the ability of applying feedback to the gates. To achieve sufficient gain for amplifying small voltage variations at the input stage node, positive voltage feedback from a **CMOS** inverter is used. As for the current mirror comparator, short transition times and clocked rail-to-rail sewing is achieved by connecting additional cascaded **CMOS** inverters to the output. By introducing a simple MOS switch between the **CMOS** inverters and the output of the comparator, a clocked differential output is also obtained. This output stage has desirable properties and should preferably is used for better performance. One consequence of the low input resistance is that simpler current mirrors can be used to provide current subtraction to the input node.

One disadvantage of this structure concerns the input voltage to the positive feedback inverter. It does not slew from rail to rail, making neither M3 nor M4 totally shutoff. Thereby a quiescent current will flow, giving rise to a nonzero DC power dissipation. However, there is no quiescent current in the input stage.

Since then, many new design ideas have been developed in order to improve the above shortcoming as well as other properties such as power consumption, offset consideration and wider input dynamic range.

Another **CMOS** current comparator is described by A.T.K. Tang [10] by changing the buffer of Traff's comparator from class B to class **AB** operation so that voltage swings are reduced. And hence results greater speed for small input currents.

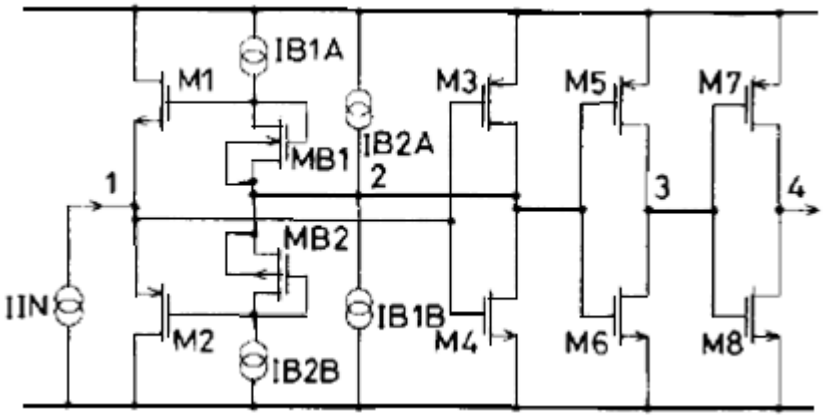


Fig 5.3: Tang's current comparator

In Fig 5.3 Tang's current comparator is shown. The biasing of M1 and M2 transistor is in class AB operation with gate-source voltages of VBI and VB2, respectively. As the magnitude of VBI and VB2 are increased towards the magnitude of Vt1 and Vt2 respectively, the dead band (or rail to rail voltage swing) in the transfer characteristic of the buffer is reduced. This results in smaller voltage swings at V(1) and V(2), hence obtains faster response times. The optimum values for VB1 and VB2 are a compromise between minimising the dead band (i.e. maximising the speed) and having a signal of sufficient amplitude at V(2).

Another current comparator is designed by Bank [8] that is optimised for low power consumption whilst maintaining high speed.

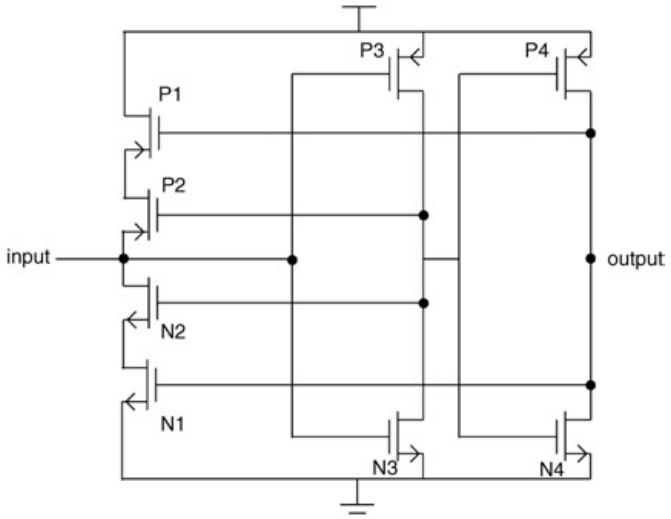


Fig 5.4: Bank's current comparator

A schematic of Bank's current comparator is shown in Fig 5.4. Positive feedback operates at the output nodes of the inverters P3/N3 and P4/ N4, respectively. In the previous state transistors N2 and P2 are closed and transistors N1 and P1 are open. As the voltage on the comparator node is affected by input current so the inverter P3/N3 begins to switch, which results a change in the output and makes the transistors P2 or N2 switched open. Then with a delay of about 10 ns the transistors P1 or N1, respectively, are switched closed [8].

Another high speed, low power and small area CMOS current comparator based on a resistive feedback network is designed by Min and Kim [6].

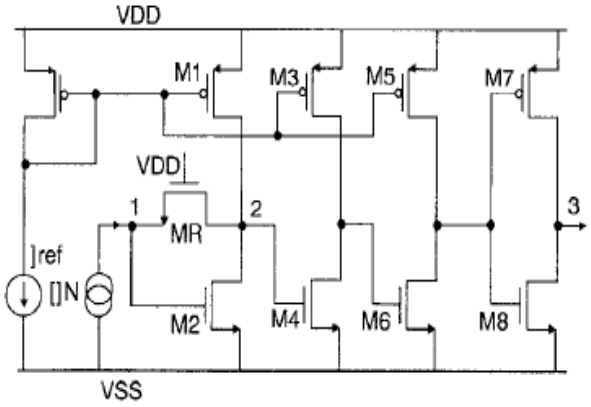


Fig 5.5: Min and Kim's current comparator

The Kim and Min's current comparator comprises three-stage current-source, inverting amplifiers and a CMOS inverter as an output stage. The circuit diagram is shown in Fig 5.5 and resistive feedback is used in the first stage.

5.2 CC-II based Current Comparator Structure

The current comparator concept is illustrated in Fig 5.6. The input current (Iin) is injected into the input stage of current comparator and it is converted to the voltage V_{IN} and then amplified to V_1 by amplifier A_1. Voltage buffer A_2 is acting as transimpedance stage. V_1 is amplified using the high gain amplifier (A_3) to generate the output logic voltage level.

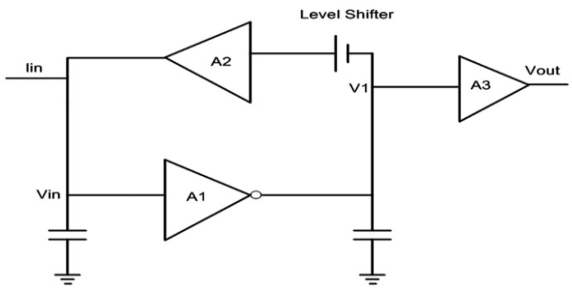


Fig 5.6: Current comparator concept

CC-II is used as the input stage of the current comparator due to the low input impedance at node X and the inherent current to voltage conversion property of the CC-II circuit [11]. The circuit is shown in Fig 5.7.

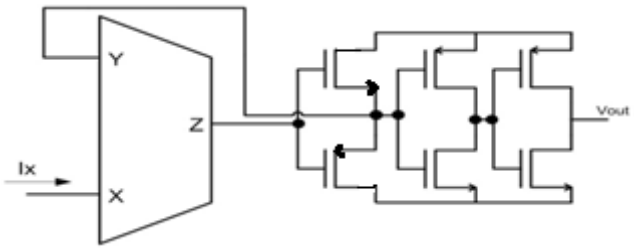


Fig 5.7: CC-II is used as input stage of current comparator

CC-II based current comparator structure is shown in Fig 5.8. The input current is injected into the node X, leads to a proportional voltage at node X. This voltage drives the transistors M9 and M10. Any change in the voltage of node X, changes the current of M9 and M10 with equal current change in the M11 and M12 due to the identical gate to source voltage. In order to reduce the propagation delay of the circuit and increase the sensitivity to input current variation, a positive feedback network is used. Input current variations lead to node X variations and hence an exact voltage variation in the Z terminal. An opposite variation appears in the output of first inverter. Positive feedback network convey this variation to the node Y. Due to the differential pair characteristics, any Y terminal variation results in an increased change in the node X.

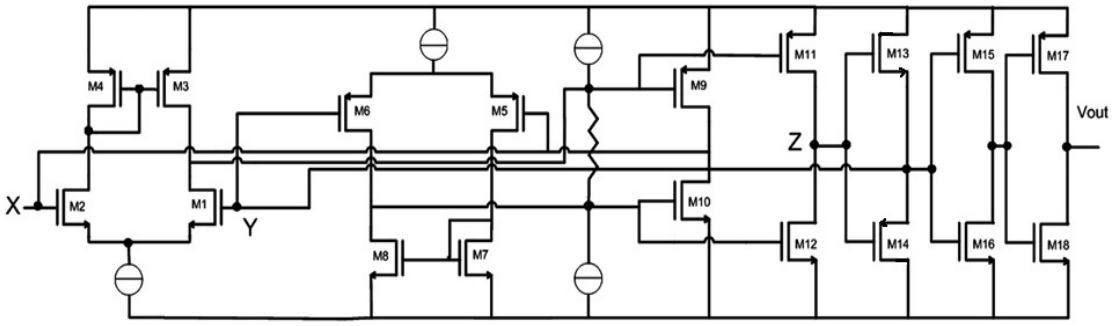


Fig 5.8: Schematic of CC-II based current comparator

Here the current at node X is the difference of input current and the reference current. If the input current is less than the reference current then the output voltage, V_{out} is at logic '0' and if the input current is greater than the reference current then the output voltage, V_{out} is at logic'1'.

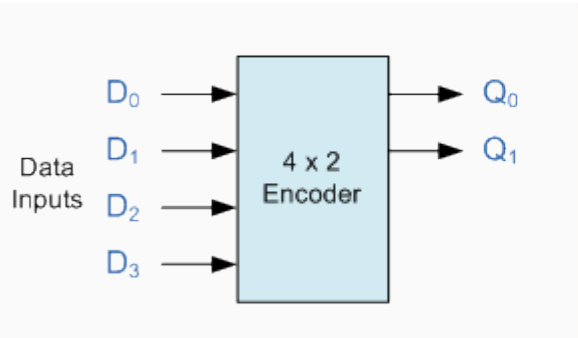
CHAPTER-6

ENCODER

6.1 Digital Encoder

Unlike a multiplexer that selects one individual data input line and then sends that data to a single output line or switch, a Digital Encoder more commonly called a Binary Encoder takes ALL its data inputs one at a time and then converts them into a single encoded output. So we can say that a binary encoder, is a multi-input combinational logic circuit that converts the logic level "1" data at its inputs into an equivalent binary code at its output. Generally, digital encoders produce outputs of 2-bit, 3-bit or 4-bit codes depending upon the number of data input lines. An "n-bit" binary encoder has 2^n input lines and n-bit output lines with common types that include 4-to-2, 8-to-3 and 16-to-4 line configurations. The output lines of a digital encoder generate the binary equivalent of the input line whose value is equal to "1" and are available to encode either a decimal or hexadecimal input pattern to typically a binary or BCD output code.

4-to-2 Bit Binary Encoder



Inputs				Outputs	
D_3	D_2	D_1	D_0	Q_1	Q_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1
0	0	0	0	x	x

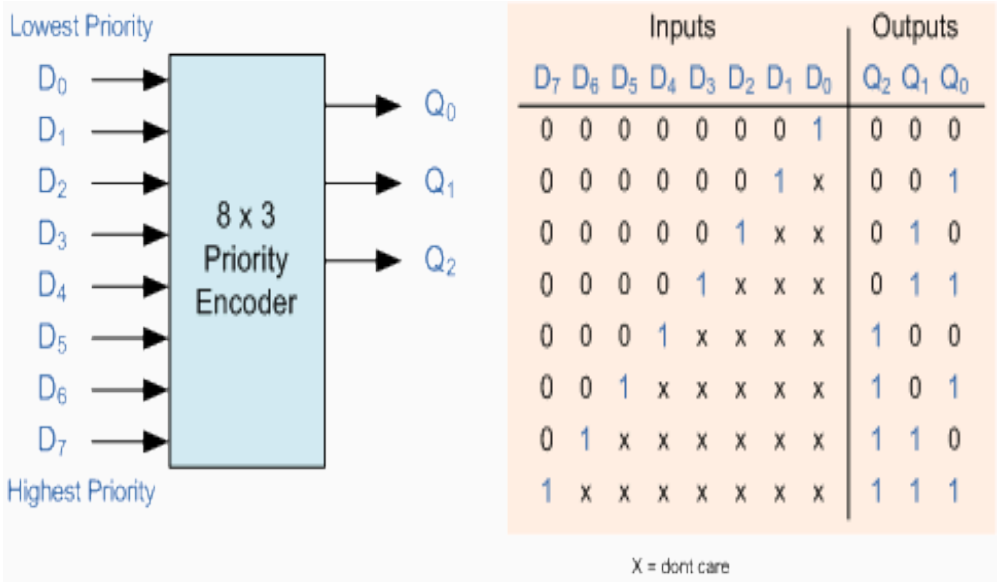
Fig 6.1: 4-to-2 bit binary encoder

One of the main disadvantages of standard digital encoders is that they can generate the wrong output code when there is more than one input present at logic level "1". For example, if we make inputs D_1 and D_2 HIGH at logic "1" at the same time, the resulting output is neither at "01" nor at "10" but will be at "11" which is an output binary number that is different to the actual input present. Also, an output code of all logic "0"s can be generated when all of its inputs are at "0" OR when input D_0 is equal to one.

One simple way to overcome this problem is to "Prioritise" the level of each input pin and if there was more than one input at logic level "1" the actual output code would only correspond to the input with the highest designated priority. Then this type of digital encoder is known commonly as a **Priority Encoder** or **P-encoder** for short.

6.2 Priority Encoder

The Priority Encoder solves the problems mentioned above by allocating a priority level to each input. The priority encoders output corresponds to the currently active input which has the highest priority. So when an input with a higher priority is present, all other inputs with a lower priority will be ignored. The priority encoder comes in many different forms with an example of an 8-input priority encoder along with its truth table shown below.



Inputs								Outputs		
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Q_2	Q_1	Q_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	x	0	0	1
0	0	0	0	0	1	x	x	0	1	0
0	0	0	0	1	x	x	x	0	1	1
0	0	0	1	x	x	x	x	1	0	0
0	0	1	x	x	x	x	x	1	0	1
0	1	x	x	x	x	x	x	1	1	0
1	x	x	x	x	x	x	x	1	1	1

X = dont care

Fig 6.2: 8-to-3 Bit Priority Encoder

An 8-to-3 bit priority encoder is shown in Fig 6.2, which has eight active LOW (logic "0") inputs and provides a 3-bit code of the highest ranked input at its output. Priority encoders output the highest order input first for example, if input lines "D2", "D3" and "D5" are applied simultaneously the output code would be for input "D5" ("101") as this has the highest order out of the 3 inputs. Once input "D5" had been removed the next highest output code would be for input "D3" ("011"), and so on.

6.3 CMOS implementation of 3x2 Priority Encoder

The 3x2 priority encoder is designed using CMOS technology is shown in Fig 6.3. COMP 3, COMP 2 and COMP 1 are the input to the encoder and B_1 and B_0 are the output of the encoder. The structure of priority encoder is designed by the following Table I:

COMP 3	**COMP 2**	**COMP 1**	**B_1**	**B_0**
0	0	0	0	0
0	0	1	0	1
0	1	1	1	0
1	1	1	1	1

Table I: Extraction of B_1 and B_0 bits

The aspect ratio (W/L ratio) used to simulate priority encoder is to be 2µm/.18µm for all the NMOS and PMOS.

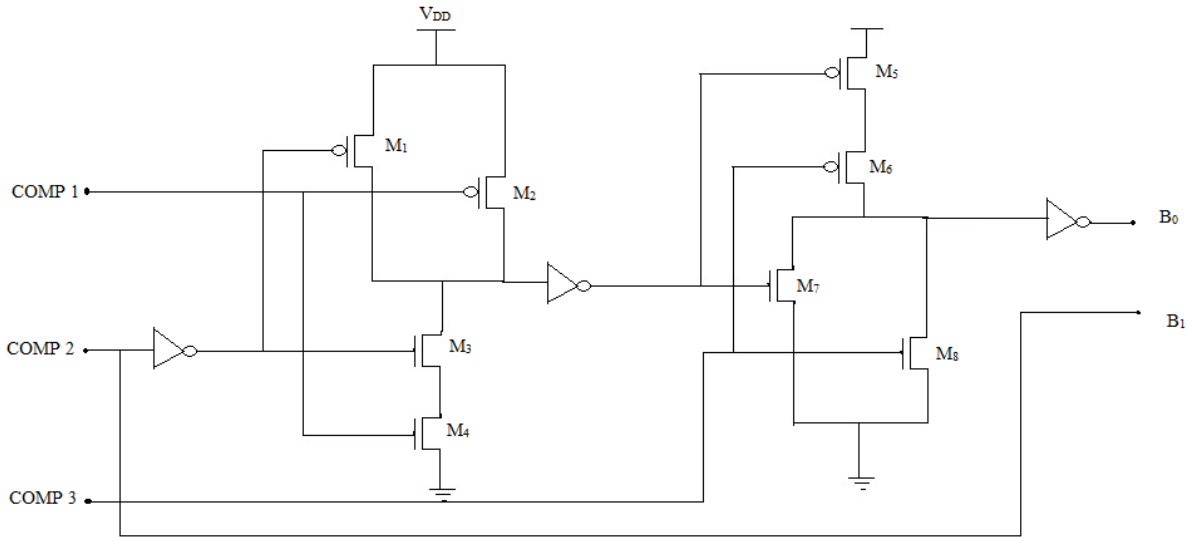


Fig 6.3: CMOS implementation of 3x2 priority encoder

CHAPTER-7

PROPOSED CURRENT MODE FLASH ADC

The block diagram of proposed two step 4 bit current mode flash ADC is shown in Fig 7.1. The Analog to Digital Conversion Method (ADCM) uses a Digital to Analog Converter (DAC). DAC is used after first stage of conversion and it will produce the required current for the second stage of ADC conversion.

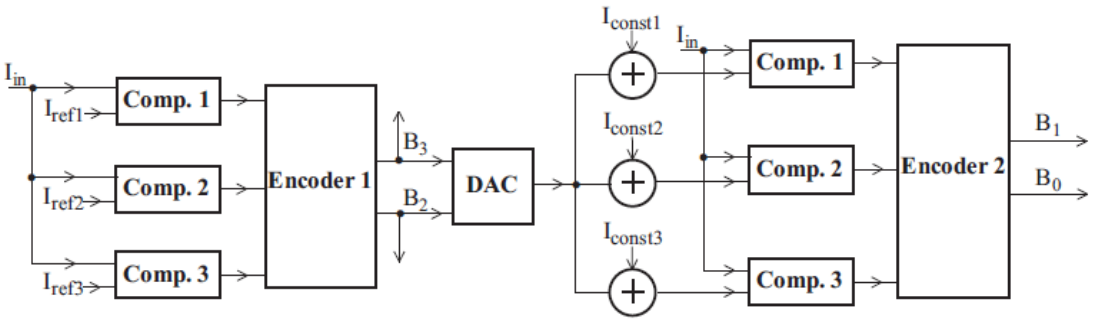


Fig 7.1: Block diagram of the proposed two step 4 bit current mode flash ADC

The proposed two step 4-bit flash ADC is made of a combination of current comparators, current mirrors, DAC, and encoders. The conversion of four bits is performed in two stages. In the first stage, most significant bits, B_3 and B_2, are generated from the analog input value (input current). The other two bits, B_1 and B_0, are produced in the second stage depending on the output values of the first stage. Accordingly, each 2-bit is generated at the same time which decreases the total time of 4-bit conversion.

7.1 Operation

- Input current is given to all the three comparator of first stage and it will remain same for all comparators.
- This input current is also mirrored to the second stage comparators for second stage conversion.
- This is done by making equal aspect ratio (W/L ratio) for all the transistor of the current mirror circuit.

- Reference current is also mirrored to the three comparator of first stage, and finally difference of input current and reference current is supplied to the comparators.
- If input current is greater than the reference current then comparator output is logic '1', otherwise output is logic'0'.
- The output of each comparator is in the form of voltage and it represents thermometric code.
- Now this thermometric code provides input to the 3x2 priority encoder1 and results the MSB B_3 and B_2.
- After this stage two 1 bit DAC are used in parallel for each MSB. Each 1 bit DAC is a simple weighted current source (current mirror). The output of DAC is in the form of analog current.
- This current is added with some constant currents which gives the equal reference currents as in the first stage.
- Again the same procedure will start as in the first stage, the encoder2 gives the output bits B_1 and B_0.

7.2 Approach of ADCM

Corresponding to each N bit in digital output, there will be 2^N levels in analog input. For example, a 4-bit output is equal to a 16-level input.

The minimum difference between each two levels is called step size. For a 4-bit system with an input current in the range of (M_1, M_2) the step size can be calculated as follows:

$$\text{Step size} = (M_2 - M_1) / (2^N - 1) \qquad \text{..... (7.1)}$$

The value of I_{ref} and I_{const} currents for first stage and second stage is totally depends on step size and can be shown by the following formula shown in Table II.

I_{ref_1}	I_{ref_2}	I_{ref_3}
$step \times 2^2$	$step \times 2^3$	$step \times (2^2 + 2^3)$
I_{const_1}	I_{const_2}	I_{const_3}
$step \times 2^0$	$step \times 2^1$	$step \times (2^0 + 2^1)$

Table II: Values of all currents in the proposed Flash ADC block diagram

In the first stage, the analog input, I_{in}, is compared to constant reference currents, I_{ref}, through the current comparators. The output of comparators is '1' when $I_{in} > I_{ref}$ and otherwise '0'. Due to the three current comparator outputs, the *Encoder*1 indicates whether each one of B_3 and B_2 is *'1'* or *'0'* and the result is shown in Table III.

Comp. 3	Comp. 2	Comp. 1	B_3	B_2
0	0	0	0	0
0	0	1	0	1
0	1	1	1	0
1	1	1	1	1

Table III: Extraction of B_3 and B_2 from the output of current comparators

According to Table III, B_3 and B_2 can be extracted as follows:

$$\begin{aligned} B_3 &= Comp.\ 1 \cdot Comp.\ 2 \\ B_2 &= Comp.\ 1 \cdot (Comp.\ 2 \odot Comp.\ 3) \end{aligned} \quad \text{..... (7.2)}$$

It is observed from Table II that if the output of *Comp.i* is '1', the output of *Comp.j* would be also '1' because *Ij* < *Ii* as long as *j* < *i*. Consequently, the equation (7.2) can be modified as follows:

$$\begin{aligned} B_3 &= Comp.\ 2 \\ B_2 &= Comp.\ 3 + (Comp.\ 1 \cdot \overline{Comp.\ 2}) \end{aligned} \quad \text{..... (7.3)}$$

In the second stage, the DAC generates a current corresponding to the values of B_3 and B_2. Two 1 bit DAC are used in parallel to give required output. The figure of 1 bit DAC is shown in Fig 7.2.

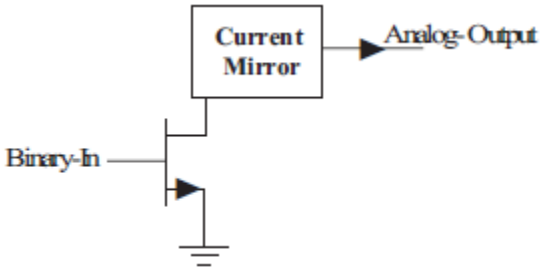


Fig 7.2: 1-bit DAC

If B_3B_2 is equal to '00', the DAC output is '0'. The output current of DAC is generated by the formula ***step*** **× 2^2**, ***step*****×2^3**, and ***step*****×(2^2+2^3)** for digital inputs of '01', '10', and '11', respectively.

The DAC output current is added to each constant current value, I_{const}. The summation result is called the total reference current. The next three parallel current comparators compare the input current I_{in} to each of these total reference currents. Again, the output of comparators is '1' if I_{in} is greater than the total reference current.

Encoder2 decides the value of B_1 and B_0 exactly in the same way as Encoder1 does for B_3 and B_2 respectively. Thus, the equations of (7.3) can be rewritten for Encoder2 in order to extract B_1 and B_0 as follows:

$$\begin{aligned} B_1 &= Comp.\ 2 \\ B_0 &= Comp.\ 3 + (Comp.\ 1 \cdot \overline{Comp.\ 2}) \end{aligned} \quad \text{..... (7.4)}$$

Through this approach the two step 4 bit analog to digital conversion method will be done successfully. The B_3 and B_2 bits are obtain at first stage and the B_1 and B_0 bits are obtain at second stage. The total four bits are obtained with two bits at each stage.

CHAPTER-8

SIMULATION RESULT

In order to verify the results of theoretical propositions, current mirrors, CC-II based current comparator, encoder, and DAC are simulated using OrCad PSpice program. 180nm, Level 7, CMOS process parameters are used for simulation and supply voltage taken is 1.8V. Further, the performance of proposed current mode Flash ADC using CC-II based current comparator is designed and simulated for the input current range 0 to 30μA. The current comparator proposed in [11] is used as an active building block for proposed current mode Flash ADC.

8.1 Simulation for simple Current Mirror

The simple NMOS current mirror structure is illustrated in Fig 4.2. The simulation result is shown for 10μA input current in Fig 8.1. The aspect ratio for M1 and M2 is 0.18/0.18 and 0.18/0.20 respectively.

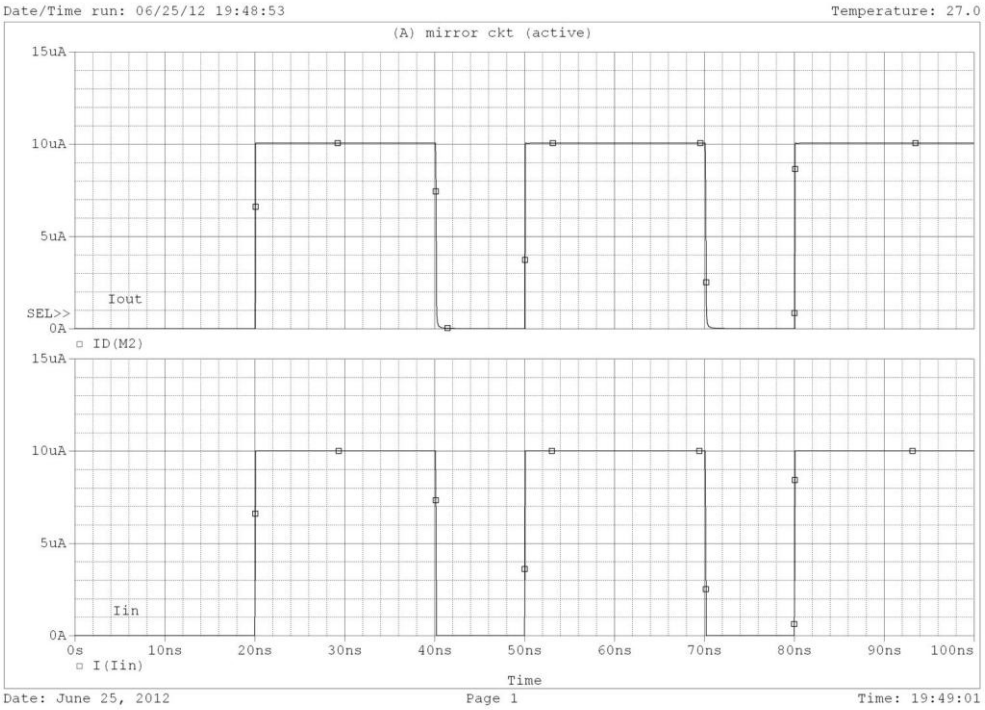


Fig 8.1: Response of simple NMOS current mirror

8.2 Simulation for CC-II based current comparator

The CC-II based current comparator is illustrated in Fig 5.8. The simulation is done for difference between input current and reference current, which is made greater than zero. 15μA input current difference is used for simulation of CC-II based current comparator. The input and output characteristics is shown in Fig 8.2.

The aspect ratio for PMOS and NMOS used in Fig 5.8 is shown in the following Table IV

S.NO	Transistors	Aspect Ratio(um)
1	M1-M12	W=.36 L=.18
2	M13-M16	W=.72 L=.18
3	M17	W=.54 L=.18
4	M18	W=1.8 L=.36

TABLE IV: Transistor sizing

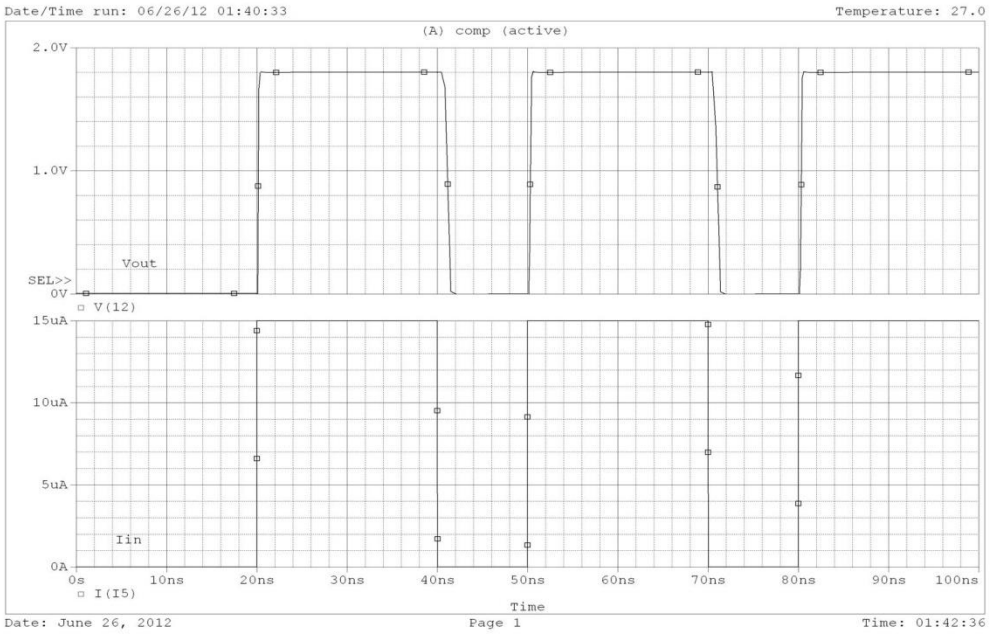


Fig 8.2: Input and output characteristics of CC-II based current comparator

The lower waveform is the difference of input current and reference current. The upper waveform illustrates the corresponding output voltage value of the comparator. Since the current difference is greater than zero the output level is set to supply voltage i.e. 1.8V.

8.3 Simulation for 1 Bit DAC

The schematic of 1 Bit DAC is shown in Fig 8.3 which employs a current mirror circuit as a load. The binary output of encoder works as input for the DAC and it gives the output in form of analog current and this current is used to generate total reference current for second stage. The simulation result of 1 Bit DAC is shown in Fig 8.4.

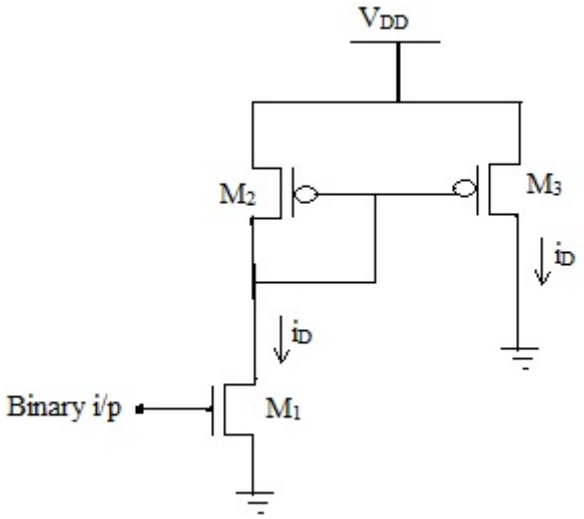


Fig 8.3: Schematic of 1 bit DAC

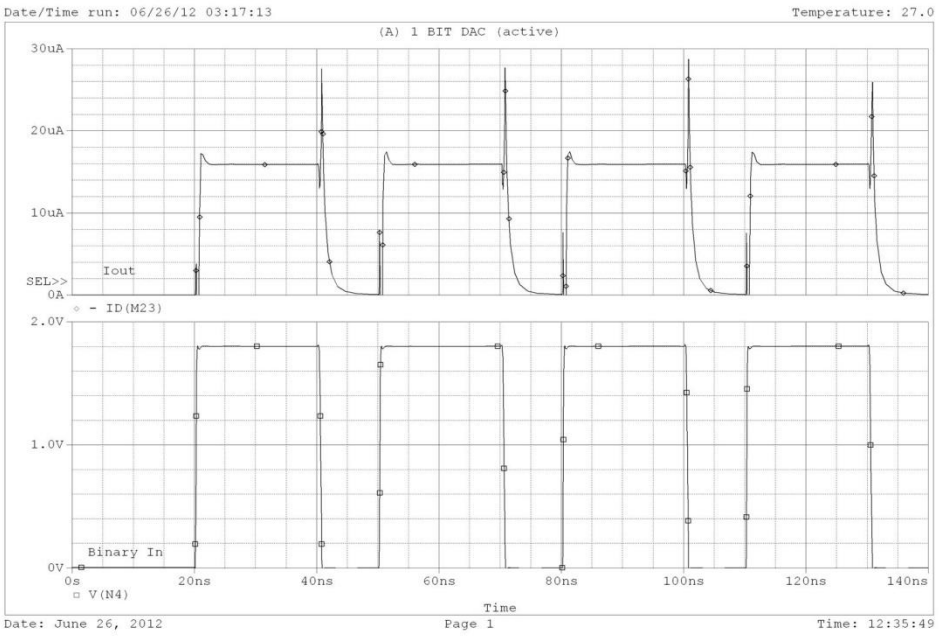


Fig 8.4: Response of 1 Bit DAC

In Fig 8.4, above waveform indicate the current generated by the most significant bit B_3. Since two 1 bit DAC are used in parallel so the current generated by each DAC are added and this will be added to constant current to provide total reference current.

8.4 Simulation for 3x2 priority encoder

The CMOS implementation of 3x2 priority encoder is illustrated in Fig 6.3. The output of the three comparators behaves as the three inputs for the encoder. The input characteristics of encoder are shown in Fig 8.5 with '011' is taken as input combination.

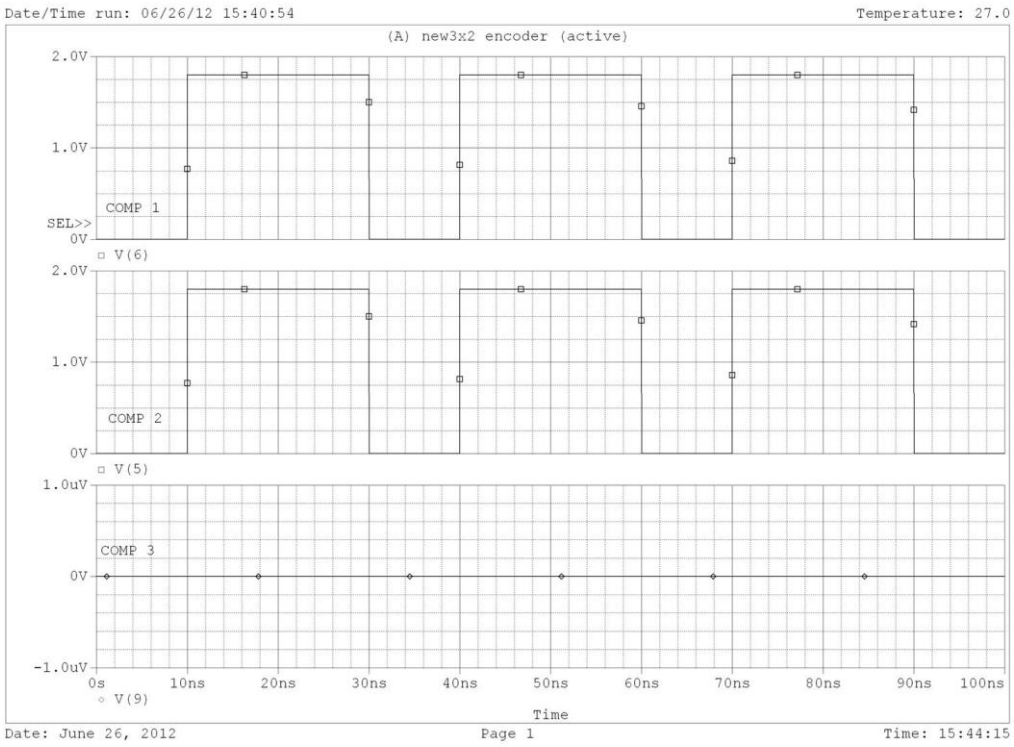


Fig 8.5: Input of 3x2 Priority Encoder

The output characteristic of the priority encoder is shown in Fig 8.6, in which the B_1 and B_0 bits are '0' and '1' respectively according to Table II.

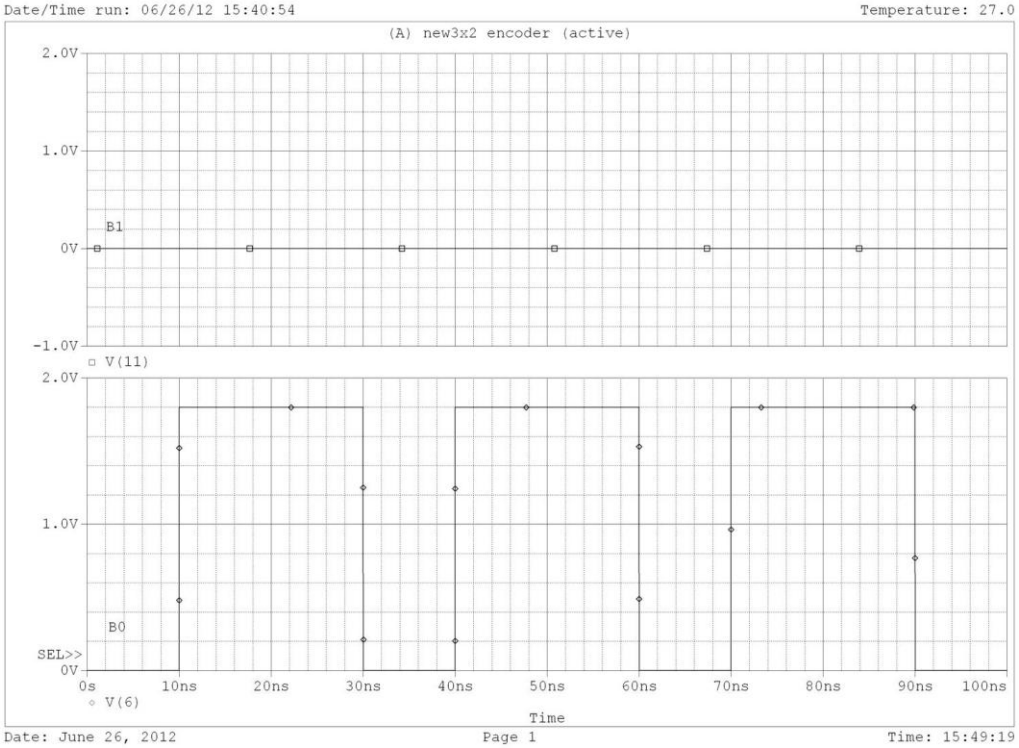


Fig 8.6: Output characteristics of 3x2 priority encoder

8.5 Simulation for Proposed 4 Bit Flash ADC

The block diagram of proposed flash ADC is illustrated in Fig 7.1. Complete structure of proposed Flash ADC is designed by joining all the sub blocks together. The simulation is done for the input range of 0-30μA. The step size for this range of the input current can be calculated by the equation (7.1).

$$\text{Step size} = (30 - 0) / (2^4 - 1)$$

$$\text{Step size} = 2\mu A$$

The reference currents and constant currents can be calculated by using formula written in Table II and all current values are shown in Table V.

I_{ref1}	I_{ref2}	I_{ref3}
8μA	16μA	24μA
I_{const1}	I_{const2}	I_{const3}
2μA	4μA	6μA

Table V: Current values when input is between 0μA and 30μA

The simulation result of the proposed two step 4 bit current mode flash ADC is shown in Fig.8.7. The waveform is shown for 24μA input current and results in $B_3B_2B_1B_0$ bits as 1011, respectively.

Fig 8.7: Resultant 4 bits of proposed flash ADC for 24μA input current

The simulation is done for entire range of input current (0-30μA) and the input output characteristics of proposed 4 bit flash ADC has been successfully obtained. The I/O characteristics of proposed 4 bit flash ADC is shown in Fig 8.8.

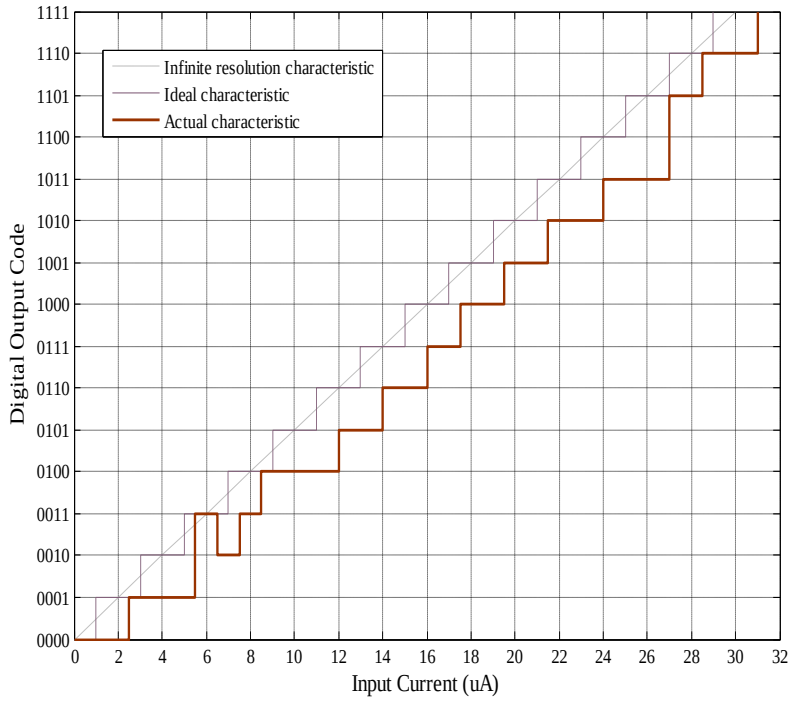


Fig 8.8: I/O characteristics of proposed 4 bit flash ADC

The static characteristics of the ADC can be measured from Fig 8.8 and are as follows:

Offset error = 1 LSB

Gain error = 1 LSB

Integral nonlinearity (INL) = - 1 LSB

Differential nonlinearity (DNL) = + 1 LSB (largest value), -2 LSB (smallest value)

Propagation delay of the proposed 4 bit current mode flash ADC is calculated at different values of input currents. Different propagation delay is shown in Table VI.

Input current (uA)	Propagation delay (nSec)
5	0.838
10	0.719
15	0.649
20	0.540
25	0.412
30	0.371

Table VI: Propagation delay

A graph is drawn for propagation delay by using table V and is shown in Fig 8.9.

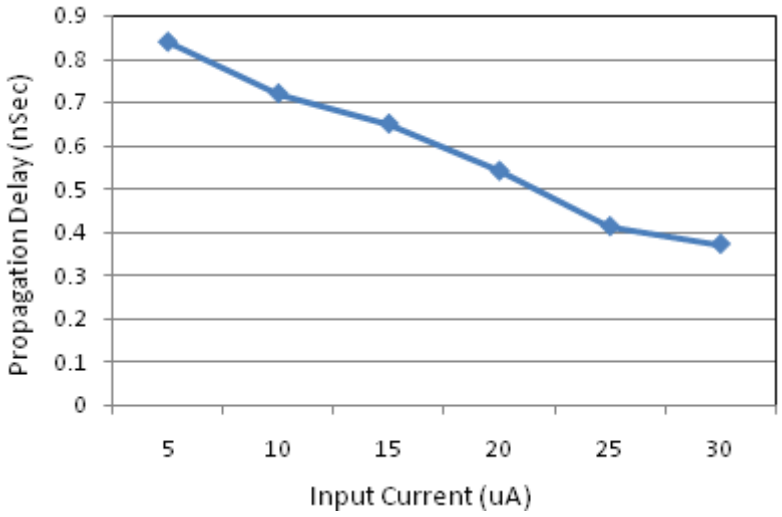


Fig 8.9: Propagation delay for varying input current

It can be seen from Fig 8.9 that, the delay is maximum at lower input current and it gets reduced as the input current is increased.

The total average power of the circuit using Spice simulation is calculated as 1.22 mWatt.

8.6 Comparison with earlier works

The proposed two step 4 bit current mode flash ADC is compared to some previously designed current mode ADC [19] in terms of delay.

According to Fig 7.1, the proposed two step 4 bit Flash ADC requires six comparator in two stages having three comparators in each stage. For delay estimation as only series components are considered, therefore, only 2 comparators in series followed by encoders are considered which effectively results in delay of less than 0.85ns. This result shows that there is a significant improvement in the delay as compared to the work referred in [19] which estimated a delay of 12.47ns.

Lastly, the present work is being compared in terms of occupied area on silicon chips with the earlier works referred in [17], [18] and [20], in terms of decreased modular components. The proposed two step 4 bit current mode flash ADC which uses only six comparators will enjoy less consumed area in comparison with the ADC referred in [17], [18] and [20] which utilize 16 comparators.

CHAPTER-9

CONCLUSION

A two step 4 bit analog to digital conversion is presented. This method has a parallel configuration of comparators and provides conversion of each two bit at the same time resulting in a high conversion speed

The simulation of proposed ADC is completed using 180nm, Level 7, CMOS process technology parameter with a supply voltage of 1.8V. The static characteristics of the ADC as observed are: Gain error is 1 LSB, offset error is 1 LSB, INL is -1 LSB and DNL is +1 LSB (maximum) and -2 (minimum).

The delay for the proposed flash ADC is less than 0.85ns and is very less compared to the previously proposed ADC [19]. Also it offers less delay for higher order of input current as shown in Fig 8.9. The total average power of the proposed flash ADC is 1.22 mWatt.

The present work is being compared in terms of occupied area on silicon chips with the earlier works in terms of decreased modular components. The proposed two step 4 bit current mode flash ADC which uses only six comparators will enjoy less consumed area in comparison with the ADC with 16 comparators as referred in [17], [18], [20].

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APPENDIX

Simulations have been performed using PSpice at 180nm technology and the model files provided by MOSIS (AGILENT) used have the following parameters:

```
.MODEL NMOS NMOS (                                LEVEL   = 7
+ TNOM    = 27             TOX     = 4.1E-9
+XJ       = 1E-7           NCH     = 2.3549E17      VTH0    = 0.3750766
+K1       = 0.5842025      K2      = 1.245202E-3    K3      = 1E-3
+K3B      = 0.0295587      W0      = 1E-7           NLX     = 1.597846E-7
+DVT0W    = 0              DVT1W   = 0              DVT2W   = 0
+DVT0     = 1.3022984      DVT1    = 0.4021873      DVT2    = 7.631374E-3
+U0       = 296.8451012    UA      = -1.179955E-9   UB      = 2.32616E-18
+UC       = 7.593301E-11   VSAT    = 1.747147E5     A0      = 2
+AGS      = 0.452647       B0      = 5.506962E-8    B1      = 2.640458E-6
+KETA     = -6.860244E-3   A1      = 7.885522E-4    A2      = 0.3119338
+RDSW     = 105            PRWG    = 0.4826         PRWB    = -0.2
+WR       = 1              WINT    = 4.410779E-9    LINT    = 2.045919E-8
+XL       = 0              XW      = -1E-8          DWG     = -2.610453E-
9
+DWB      = -4.344942E-9   VOFF    = -0.0948017     NFACTOR = 2.1860065
+CIT      = 0              CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB    = 0              ETA0    = 1.991317E-3    ETAB    = 6.028975E-5
+DSUB     = 0.0217897      PCLM    = 1.7062594      PDIBLC1 = 0.2320546
+PDIBLC2  = 1.670588E-3    PDIBLCB = -0.1           DROUT   = 0.8388608
+PSCBE1   = 1.904263E10    PSCBE2  = 1.546939E-8    PVAG    = 0
+DELTA    = 0.01           RSH     = 7.1            MOBMOD  = 1
+PRT      = 0              UTE     = -1.5           KT1     = -0.11
+KT1L     = 0              KT2     = 0.022          UA1     = 4.31E-9
+UB1      = -7.61E-18      UC1     = -5.6E-11       AT      = 3.3E4
+WL       = 0              WLN     = 1              WW      = 0
+WWN      = 1              WWL     = 0              LL      = 0
+LLN      = 1              LW      = 0              LWN     = 1
+LWL      = 0              CAPMOD  = 2              XPART   = 0.5
+CGDO     = 6.7E-10        CGSO    = 6.7E-10        CGBO    = 1E-12
+CJ       = 9.550345E-4    PB      = 0.8            MJ      = 0.3762949
+CJSW     = 2.083251E-10   PBSW    = 0.8            MJSW    = 0.1269477
+CJSWG    = 3.3E-10        PBSWG   = 0.8            MJSWG   = 0.1269477
+CF       = 0              PVTH0   = -2.369258E-3   PRDSW   = -1.2091688
+PK2      = 1.845281E-3    WKETA   = -2.040084E-3   LKETA   = -1.266704E-
3
+PU0      = 1.0932981      PUA     = -2.56934E-11   PUB     = 0
+PVSAT    = 2E3            PETA0   = 1E-4           PKETA   = -3.350276E-
3    )

.MODEL PMOS PMOS (                                LEVEL   = 7
+ TNOM    = 27             TOX     = 4.1E-9
+XJ       = 1E-7           NCH     = 4.1589E17      VTH0    = -0.3936726
+K1       = 0.5750728      K2      = 0.0235926      K3      = 0.1590089
+K3B      = 4.2687016      W0      = 1E-6           NLX     = 1.033999E-7
+DVT0W    = 0              DVT1W   = 0              DVT2W   = 0
+DVT0     = 0.5560978      DVT1    = 0.2490116      DVT2    = 0.1
+U0       = 112.5106786    UA      = 1.45072E-9     UB      = 1.195045E-
21
+UC       = -1E-10         VSAT    = 1.168535E5     A0      = 1.7211984
+AGS      = 0.3806925      B0      = 4.296252E-7    B1      = 1.288698E-6
```

```
+KETA     = 0.0201833      A1       = 0.2328472      A2       = 0.3
+RDSW     = 198.7483291    PRWG     = 0.5            PRWB     = -0.4971827
+WR       = 1              WINT     = 0              LINT     = 2.943206E-8
+XL       = 0              XW       = -1E-8          DWG      = -1.949253E-
8
+DWB      = -2.824041E-9   VOFF     = -0.0979832     NFACTOR  = 1.9624066
+CIT      = 0              CDSC     = 2.4E-4         CDSCD    = 0
+CDSCB    = 0              ETA0     = 7.282772E-4    ETAB     = -3.818572E-
4
+DSUB     = 1.518344E-3    PCLM     = 1.4728931      PDIBLC1  = 2.138043E-3
+PDIBLC2  = -9.966066E-6   PDIBLCB  = -1E-3          DROUT    = 4.276128E-4
+PSCBE1   = 4.850167E10    PSCBE2   = 5E-10          PVAG     = 0
+DELTA    = 0.01           RSH      = 8.2            MOBMOD   = 1
+PRT      = 0              UTE      = -1.5           KT1      = -0.11
+KT1L     = 0              KT2      = 0.022          UA1      = 4.31E-9
+UB1      = -7.61E-18      UC1      = -5.6E-11       AT       = 3.3E4
+WL       = 0              WLN      = 1              WW       = 0
+WWN      = 1              WWL      = 0              LL       = 0
+LLN      = 1              LW       = 0              LWN      = 1
+LWL      = 0              CAPMOD   = 2              XPART    = 0.5
+CGDO     = 7.47E-10       CGSO     = 7.47E-10       CGBO     = 1E-12
+CJ       = 1.180017E-3    PB       = 0.8560642      MJ       = 0.4146818
+CJSW     = 2.046463E-10   PBSW     = 0.9123142      MJSW     = 0.316175
+CJSWG    = 4.22E-10       PBSWG    = 0.9123142      MJSWG    = 0.316175
+CF       = 0              PVTH0    = 8.456598E-4    PRDSW    = 8.4838247
+PK2      = 1.338191E-3    WKETA    = 0.0246885      LKETA    = -2.016897E-
3
+PU0      = -1.5089586     PUA      = -5.51646E-11   PUB      = 1E-21
+PVSAT    = 50             PETA0    = 1E-4           PKETA    = -3.316832E-
3    )
```