DELHI TECHNOLOGICAL UNIVERSITY

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

DELHI-110042

CERTIFICATE

This is to Certify that the major project work entitled, "**TWO STEP 4 BIT CURRENT MODE FLASH ADC USING CC-II BASED CURRENT COMPARATOR**" submitted by **PRIYANK KUMAR SAXENA (09/VLSI/2k10)** *in partial fulfilment of the requirements for the award of degree of* **Master of Technology** *in* **VLSI Design and Embedded System** *at* **Delhi Technological University** *is an original work carried out under my supervision and has not been submitted for the award of any other degree to the best of my knowledge and belief.*

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ABSTRACT

The evolution of submicron technologies has resulted in the requirement to use low power supply voltages which makes it difficult to design voltage mode circuits with high linearity and wide range. Current mode devices have many advantages over voltage one such as low power, small area and potentially high speed. Analog to Digital Converters (ADCs) are the most commonly used mixed-signal modules which transfer analog blocks output data to digital gates.

The main building blocks of the proposed flash ADC are Current Comparator, Encoder and DAC. A high-speed current comparator based on current conveyor-II is used to design the proposed two step 4 bit current mode flash ADC. Also CMOS implementation of 3x2 priority encoder is used which converts the thermometric code to the binary output code. The conversion of four bits is performed in two stages. In the first stage, most significant bits, B_3 and B_2, are generated from the analog input current. The other two bits, B_1 and B_0, are produced in the second stage depending on the output values of the first stage. The DAC is used in between the two stages of proposed flash ADC and is used to give the output in form of current. This current is used to generate total reference current for second stage.

PSpice is used for simulation of this project with 0.18μm CMOS technology and supply voltage taken is 1.8V. The static characteristics of the ADC such as offset error, gain error, integral nonlinearity (INL) and differential nonlinearity (DNL) are calculated from the simulation result. The delay calculated for the proposed flash ADC is less than 0.85ns. This approach has resulted in major reduction of the response time resulting the wide band application of the circuit. The current mode flash ADC is faster than the other types of ADCs. Therefore proposed work may find wide applications.

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