A DISSERTATION ON

LOW-POWER LOW-VOLTAGE ANALOG DESIGN

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IN

VLSI DESIGN AND EMBEDDED SYSTEM

SUBMITTED BY

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CERTIFICATE

This is to certify that the dissertation entitled **"Low-Power Low-Voltage Analog Design"** submitted by **Vishnu Mahesh Sharma** (2K13/VLSI/25) in partial fulfillment of the requirement for the award of the degree of Master in Technology in VLSI Design and Embedded System from the Department of Electronics and Communication, Delhi Technological University, Delhi is a record of candidate's own work carried out by him under my supervision.

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I hereby declare that the work presented in this dissertation entitled **"Low-power Low-Voltage Analog Design"** has been carried out by me under the guidance of **Dr. Rajeshwari Pandey**, Assistant Professor of Department of Electronics and Communication Engineering, Delhi Technological University, Delhi and hereby submitted for the partial fulfillment for the award of the degree of Masters in Technology in VLSI Design and Embedded System at Department of Electronics and Communication Engineering, Delhi Technological University, Delhi.

I further undertake that the work embodied in this major project has not been submitted for the award of any other degree elsewhere.

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"At times our own light goes out and is rekindled by a spark from another person. Each of us has cause to think with deep gratitude of those who have lighted the flame within us."

-Albert Schweitzer

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ABSTRACT

The increasing demand of portable electronics devices makes supply voltage and power consumption important design parameter. Over the years techniques such as sub-threshold and bulk-driven MOSFETs have been proposed to achieve low power operation. Floating Gate MOSFET (FGMOS) is also a low power, low voltage technique which overcome the limitations of above mentioned techniques. It has some notable features like threshold adjustment and multiple inputs floating gate which make it suitable for realizing analog circuits that can operate at lower supply voltages. Another low power technique is use of current mode circuits instead of conventional voltage mode circuits, which also offer higher speed of operation. In this work both FGMOS and current mode operations are combined to achieve low power operations. New structures of analog building blocks namely current differencing buffered amplifier (CDBA) and differential difference current conveyor (DDCC) are proposed which use FGMOS transistors in place of normal MOSFETs. The proposed FFGMOS based CDBA works for ±0.4V supply voltages with 374 µW power dissipation. This CDBA has current transfer ratio off 0.98 and voltage transfer ratio of 0.98. A second order high filter is implemented using proposed CDBA and verified through simulations. The simulations are done using TSMC 0.18 µm technology file. The proposed FGMOS based DDCC works for ±2V supply voltages. A full wave rectifier using the proposed DDCC is implemented and verified through simulation. The rectifier has -1V to 1V dynamic range of operations and rectifies the input almost without any loss. The simulations are done using 0.5 µm technology file. All the simulations are performed using PSPICE simulation software. It is found that simulated results are in harmony with the expected results.

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1. INTRODUCTION

1.1 State of Art

The demand and requirement of battery operated devices have been increasing exponentially for the past two decades. This apparently makes voltage supply a critical design parameter. In the 90's area and speed or performance were used to be main design constraints but as the level of integration on a chip is increasing power management and power dissipation have also become design goal for VLSI designers. Adding another comfort of portability to the battery operated devices and the issue of supply voltage goes to the next level.

It can be argued that power dissipation can be reduced greatly if supply voltage is scaled down and supply voltage can be scaled downed as dimensions of chip and devices are shrinking. But it is a well known fact in VLSI that the scaling of supply voltage doesn't lead to a proportional scaling in the threshold voltage of the device i.e. threshold is not scaled down by the same factor by which supply is reduced. Thus the need of the devices which have low threshold voltage independent of the scaling comes into the picture. These devices should also be compatible with current fabrication processes so that the reduced threshold doesn't impose a constraint of cost of fabrication.

The appreciable and exceptional steps have already been taken into this direction and now the literature has plenty of the techniques which can support low power operation yet compatible with current fabrication processes. Out of these innovative techniques available in the literature some of the most popular techniques are sub-threshold MOSFETs, bulk driven MOSFETS and Floating Gate MOSFETs etc.

In sub-threshold MOSFETs [1-3], the gate to source voltage of the transistor is kept below the threshold of the transistor and the supply voltage is approximately equal to the threshold voltage. Here the sub-threshold leakage current is used for the operation and since device is working below threshold voltage low supply voltage can be used. Also, in sub-threshold region the operating current is in the range of pico ampere so the power dissipation is also reduced. In literature many low power applications of sub-threshold MOSFETs are found. One of them is "A low power CMOS based voltage reference circuit based on sub-threshold operation" [4]. The voltage reference circuit of [4] provides 621 mV reference voltage and temperature co-efficient of 11.5 ppm/^{0}C by using

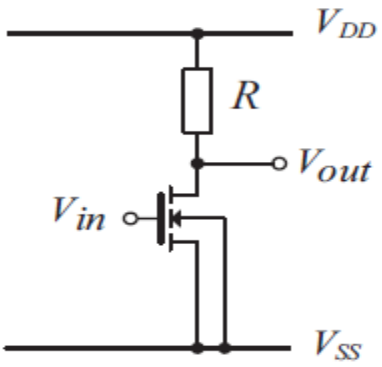
1.5 V voltage supply. Although sub-threshold technique operates for low voltages, but the leakage current in sub threshold region is highly sensitive to temperature thereby making such circuits unfeasible for many applications.

In bulk driven MOSFETs [5-8] the dependence of the threshold voltage on source-body bias is used to reduce the threshold voltage. The source body junction is intentionally made slightly forward biased which reduces the threshold voltage. This attractive feature of bulk driven MOSFETs is exploited by researchers to achieve low power applications. Examples of such applications are "A sub-1 volt CMOS bandgap voltage reference based on body driven technique" [9], which provides mean output voltage 592 mV with ±1.5mV variations and "A high compliance input and output regulated body driven current mirror for deep submicron CMOS" [10], which starts behaving like current source at 1.4 mV and provides output resistance of order of MΩ. But the forward bias source body junction is also a problem in body driven technique. Because, due to the forward source-body biasing some amount of current flows through the body which increases as the forward biased is increased. Which is undesired since it causes loss of accuracy by giving path to some useful amount of current through body of the MOSFET. Therefore, the bulk driven technique is also not suitable for many applications where accuracy or dynamic range of current is one of the important criteria.

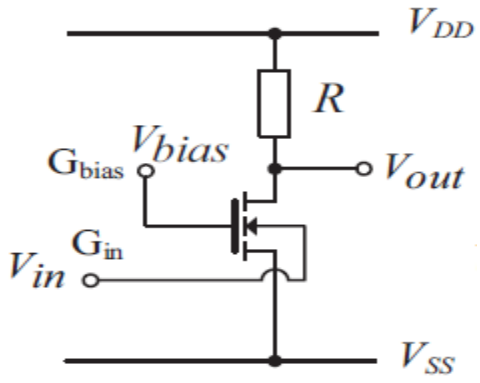
It has been discussed that both sub-threshold and bulk driven techniques are capable of providing low power and low voltage applications but at the cost of leakage current, temperature dependence and accuracy. This is one of the factors which motivated researchers to find other techniques which can facilitate low power and low voltage applications but without much dependence on temperature and loss of accuracy. One of those techniques which emerged as an alternate to bulk driven and sub-threshold operations is floating gate MOSFET (FGMOS).

In Floating Gate MOSFETs [11-13], the threshold voltage depends on the voltage applied on the control gates and by varying these voltages the threshold can also be tuned as per the requirement. Which means FGMOS gives extra liberty of adjustable threshold apart from low threshold. Many transistor based designs such as linear resistance, analog cells such as current mirrors and active building blocks such as operational transconductance amplifier (OTA) have been proposed in the literature which use FGMOS as a replacement of MOSFETs to achieve low power operations.

To get a more clear view of difference between conventional gate driven, bulk driven and FGMOS technique, schematics of common source amplifiers using these three techniques are shown in Figure 1 [14].



(a)



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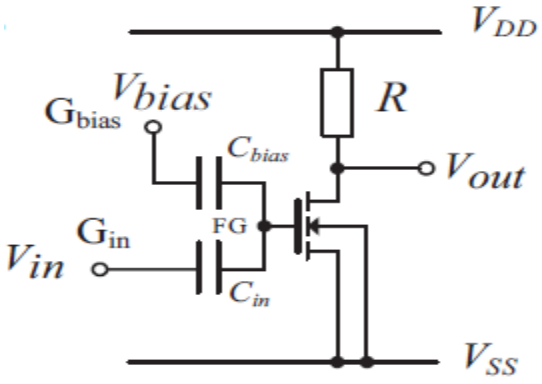


(c)

Figure 1: Common source amplifiers based on (a): conventional gate driven technique (b): body driven technique (c): FGMOS [14]

1.2 Report Organization

In this work, the FGMOS technique is discussed and some of its low power applications are illustrated with simulated results and are compared with its conventional MOS counter parts. In chapter two, the FGMOS is introduced and the reasoning behind its name is explained. The physical structure and equivalent circuit of multiple input FGMOS are also discussed.

In chapter three, the FGMOS SPICE model is explained which is followed by the current-voltage characteristics of FGMOS and its small signal mode. SPICE simulations to demonstrate the programmability of threshold voltage and i-v characteristic are included. Finally FGMOS operation in sub threshold region is presented.

In chapter four, literature survey is presented which lists some popular applications of FGMOS based design in analog domain with its advantages over conventional MOSFET based counterparts. Then transistor level circuits, basic analog cells such as current mirror and active building blocks which use FGMOS are discussed in detail.

In chapter five, advantages of current mode circuits over voltage mode circuits are discussed. Two active building blocks current differencing buffered amplifier (CDBA) and differential difference current conveyor (DDCC) are also discussed and new structures of CDBA and DDCC using FGMOS are proposed and the usefulness of proposed structures is justified by designing a filter based on proposed CDBA and a full wave rectifier based on proposed DDCC.

Chapter six concludes this work with simulations results mentioned collectively at one place and future scope is also discussed there. All the simulations are performed using software PSPICE and parameter files which are used in different circuits are given in appendix.

2. FLOATING GATE METAL OXIDES SEMICONDUCTOR FIELD EFFECT TRANSISTOR

In this chapter a basic introduction of FGMOS is presented and it is explained how the fabrication process of FGMOS is compatible with current CMOS fabrication processes. Then operation and threshold programmability of the device is discussed. This is followed by the introduction of multiple input FGMOS.

2.1 Introduction

The market and demand of battery operated portable electronic devices are increasing continuously. Due to this increased demand, supply voltage has become one of the most critical design aspects in mixed analog over the years. The significance and importance of the supply voltage can also be understood if we consider the static power dissipation which can be reduced if supply voltage is reduced as$P \propto V$. The technology or device which can work on lesser power supply as that of conventional MOSFETs has become new area of research. The innovative steps in this direction are sub threshold MOSFETs, bulk driven MOSFETs, self cascode MOSFETs and Floating Gate MOSFET (FGMOS). Among these techniques, FGMOS has the advantage of not only low threshold but also of adjusting the threshold voltage. Thus the search of having low power devices which have compatibility with today's fabrication process can be considered as the prime motivation behind the design of FGMOS.

2.2 FGMOS and its operation

The floating gate metal oxide semiconductor (FGMOS) device was first **introduced by "D. Kahng" and "S.M. Sze" in 1967 for application as a non-volatile** memory cell. Figure 2 depicts the basic structure of an FGMOS which is of type n in its way of operation. In the figure, there are two metallic gates i.e. "metal-1" and "metal-2" which are separated through a thick layer (ILD2) which is working as an insulating layer here. In this work the "metal-2" gate (upper gate) is called as the control gate and below ILD2, the "metal-1" gate is called as floating gate which is separated from the body (substrate) through a thin layer (ILD1) which is also an insulating one. "Metal-1" is referred as floating gate because it is electrically isolated from both the body and "metal-2". Hence the device is termed as Floating Gate Metal Oxide Semiconductor Transistor.

2.3 Programing of FGMOS transistor in PROMs

Programming of an FGMOS device is based on avalanche through source towards the drain. This is done by applying a high voltage (15-16V for example) between the drain and the source.

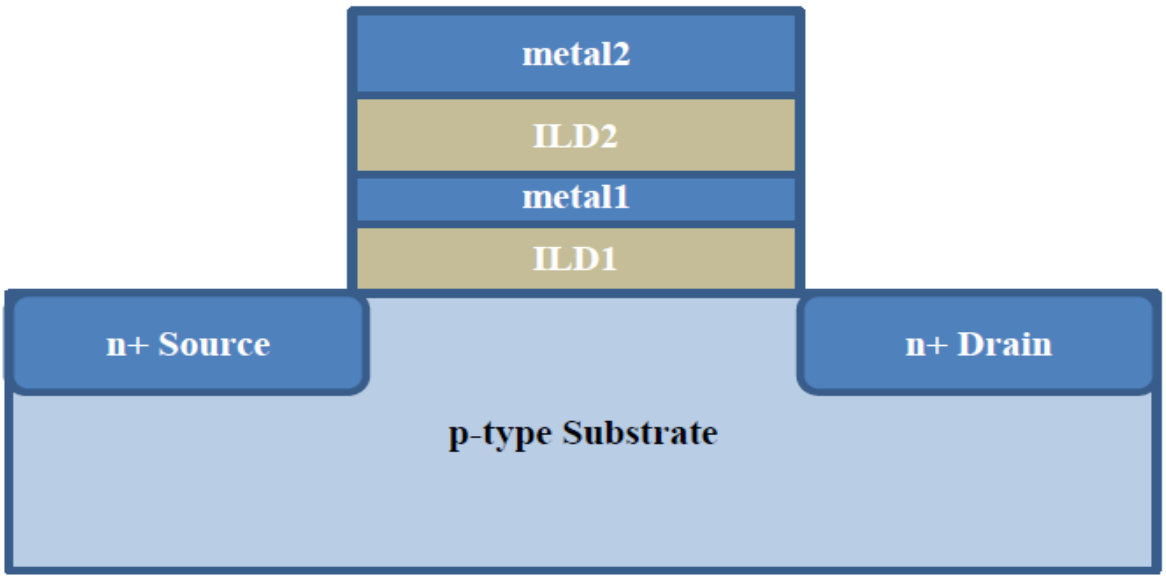


Figure 2: Schematic diagram of FGMOS [15]

The SiO_2 layer in Figure 3 is very thin, thus electron passes through this layer to the floating gate and this gives floating gate electrode an electric charge. Thus the threshold voltage of FGMOS transistor is increased. The increment (change) in threshold voltage is-

$$\Delta V_T = \frac{\Delta Q_{FG}}{C_{FG}} \quad (1)$$

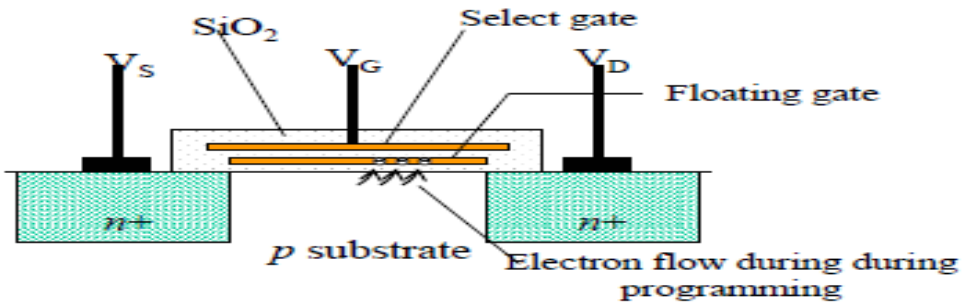


Figure 3: Programming of an FGMOS [16]

This programming technique introduces electrons ONTO the floating gate as it is based on hot electron injection. Another programming technique, based on tunneling effect, can induce negative or positive charge on the floating gate. This charge disappears if the floating gate transistor is exposed in UV light for some time, because SiO_2 layer has very good insulating properties, leakage of the charge on the floating gate occurs slowly and thus it is possible to keep V_T very high for long time (for decades at room temperature). This programming of FGMOS transistor has some applications in analog circuits for example neural networks and circuit trimming. The control on the charge on the floating gate is not easy. In this work, it is assumed that the floating gate has no charge. The I_D-V_{GS} characteristic of an FGMOS, before and after the programming, is depicted in Figure 4.

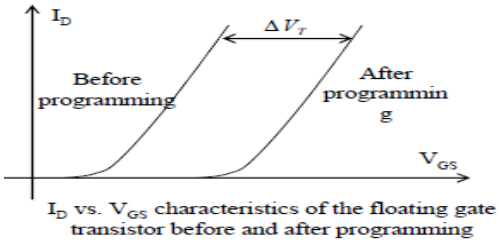
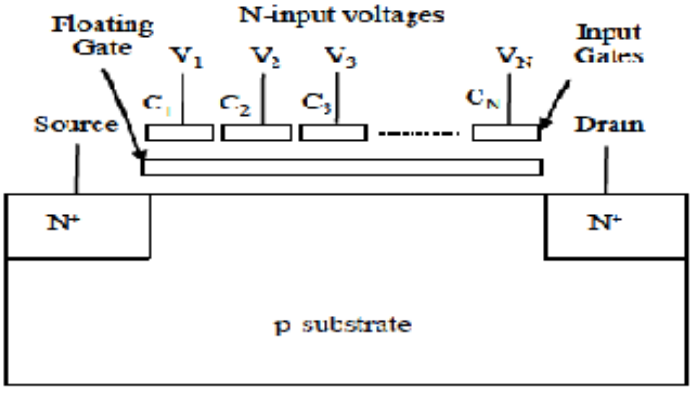


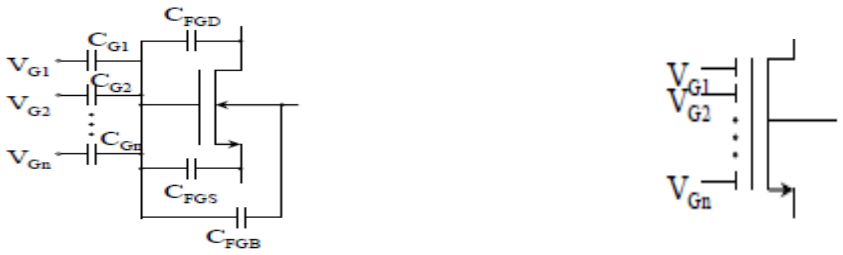
Figure 4: Variation of threshold voltage in FGMOS transistor [16]

2.4 Multiple input FGMOS transistor

An FGMOS transistor with multiple control gates, as shown in Figure 5(a), is called Multiple Input FGMOS (MIFGMOS) transistor. The symbol and equivalent circuit of an MIFGMOS transistor are shown in Figure 5(b) and Figure 5(c) respectively.



(a)



(b) **(c)**

Figure 5: The n-input FGMOS (a): Physical structure (b): Equivalent circuit (c): symbolic representation.

The input control gates are capacitively coupled to the floating gate. It is assumed that V_{FG} denotes the voltage of the floating gate, Q_{FG} denotes the net charge on the floating gate, and V_{Gi} denotes the voltage of i^{th} control gate. So

$$V_{FG} = (Q_{FG} + C_{FGD}V_D + C_{FGS}V_S + C_{FGB}V_B + \sum_{i=1}^{N} C_{Gi}V_{GI}) / C_{TOTAL} \quad (2)$$

Where

$$C_{TOTAL} = C_{FGD} + C_{FGS} + C_{FGB} + \sum_{i=1}^{N} C_{Gi}$$

2.5 Conclusion

In this chapter FGMOS with its physical structure is introduced and the threshold programmability and methods of programmability in context of PROMs are discussed. Also, the multiple inputs FGMOS (MIFGMOS) is also introduced and its voltage equation and equivalent circuit are illustrated.

3. FGMOS CHARACTERIZATION

The physical structure of an FGMOS transistor, without control gate, is same as that of conventional MOSFET. Hence I_D-V_{GS} characteristic of an FGMOS transistor is similar to that of a conventional MOS transistor. Thus FGMOS transistor can be modeled using conventional MOS model in PSPICE. In this chapter the necessity of modeling of FGMOS for PSPICE is discussed and then suitable SPICE models are presented. This is followed by the discussion on threshold voltage variation and current- voltage characteristics of FGMOS using the discussed FGMOS SPICE model. At the end of the chapter the operation of FGMOS in weak inversion region is discussed with drain current equations.

3.1 Simulation Model of FGMOS in SPICE

Since SPICE does not accept floating gate node without branch to ground, a resistor is added with each capacitor and this resistor should have a large value (10^{18} order) to minimize loading effects. It is also desired that DC voltage of floating gate must not be affected by the introduced resistors. To achieve this property time constant of each branch is made equal. The modeled FGMOS for SPICE is shown in Figure 6.

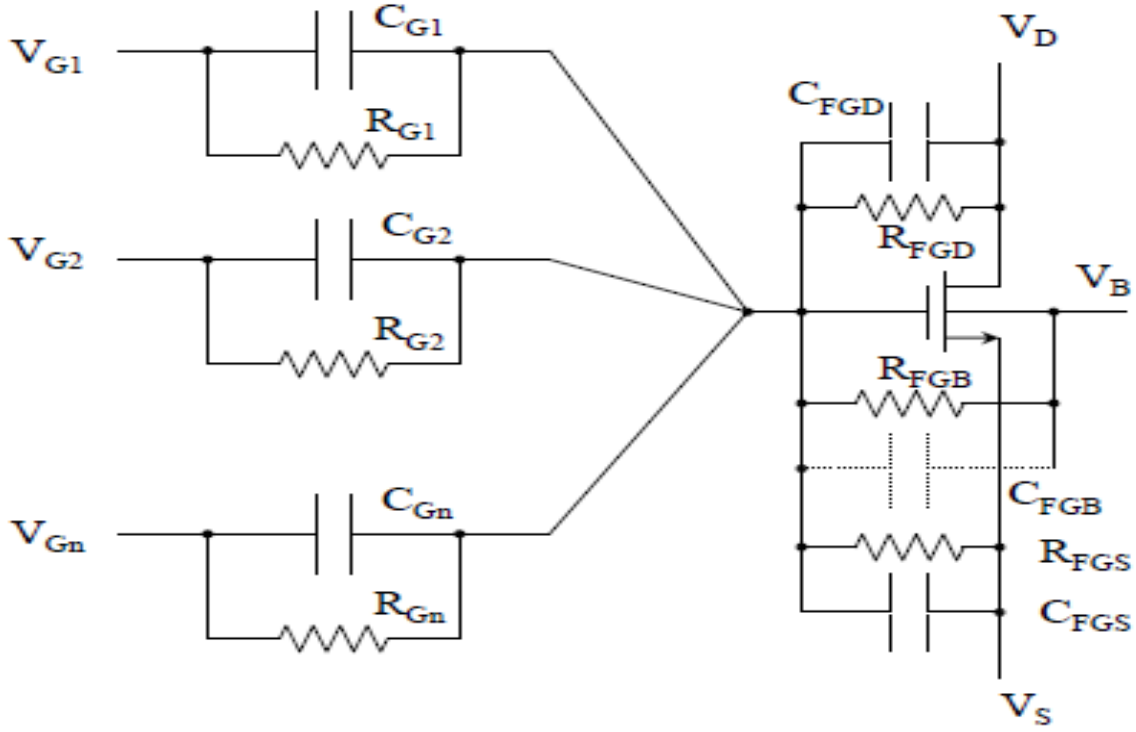


Figure 6: PSPICE modeling of FGMOS transistor [16]

$$R_{G1}\,C_{G1} = R_{G2}\,C_{G2} = \ldots\ldots\ldots\ldots\ldots = R_{FGD}\,C_{FGD} = R_{FGS}\,C_{FGS} = R_{FGB}\,C_{FGB} \quad (3)$$

The above property can be verified by writing DC nodal equation for the floating gate for DC (the effect of capacitors is not considered).

$$V_{FG}\left(\frac{1}{R_{FGD}} + \frac{1}{R_{FGS}} + \frac{1}{R_{FGB}} + \sum_{i=1}^{N}\frac{1}{R_{Gi}}\right) - V_D\frac{1}{R_{FGD}} - V_S\frac{1}{R_{FGS}} - V_B\frac{1}{R_{FGB}} - \sum_{i=1}^{N}\frac{V_{Gi}}{R_{Gi}} = 0 \quad (4)$$

This implies

$$V_{FG} = (C_{FGD}V_D + C_{FGS}V_S + C_{FGB}V_B + (\sum_{i=1}^{N} C_{Gi}V_{Gi})) / C_{TOTAL} \quad (5)$$

If condition (3) is satisfied, condition (5) is obtained.

Till now the initial charge on the floating gate has been neglected. But PSPICE model can be modified as shown in Figure 7, if initial charge is considered.

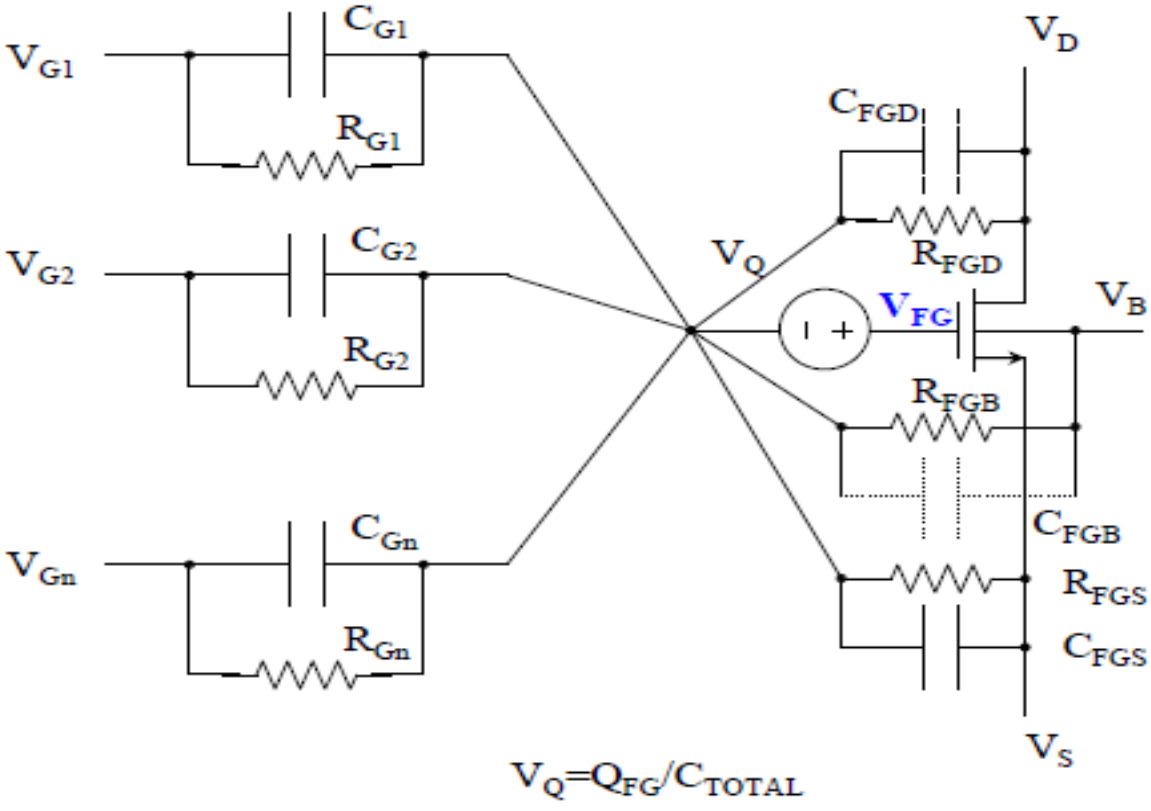


Figure 1: PSPICE modeling of FGMOS transistor with some initial charge [16]

Usually, for an MIFGMOS transistor, $C_{Gi} >> C_{FGD}, C_{FGS}, C_{FGB}$.

3.2 Threshold Voltage Variations of FGMOS

In a two input FGMOS transistor (Figure 8), if a higher DC bias voltage is applied at one gate, which is called biasing gate, and signal is applied at another gate, which is called signal gate, the equivalent threshold $V_{T,equi}$ seen from the signal gate can be adjusted effectively.

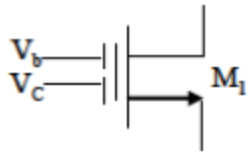


Figure 8: Symbolic representation of a two input FGMOS indicating bias and signal gate

Applying equation (2) and assuming that there is no initial charge on the floating gate i.e. $Q_{FG} = 0$, also applying the approximation that $C_{Gi} >> C_{FGD}$, C_{FGS}, C_{FGB}, the following equation can be written-

$$V_{FGS} = {(C_{G1}V_b + C_{G2}V_i)}/{C_{Total}}$$

$$= K_1V_b + K_2V_i \quad (6)$$

Here

$K_1 = C_{G1}/C_{Total}$ and

$K_2 = C_{G2}/C_{Total}$

This property is suited for low voltage application.

Thus $V_{T,equi}$ seen from the signal gate i.e. from V_i can be written as-

$$V_{T,eq} = {(V_T - V_bK_1)}/{K_2} \quad (7)$$

The $V_{T,eu}$ given by the equation (7) may less than or greater than V_T depending upon the values of K_1, K_2, and V_T.

Figure 9 shows the variation in threshold voltage as the bias voltage is varied. This plot is obtained using 0.5 um parameter file and W/L ratio of the FGMOS is 60 um/1 um.

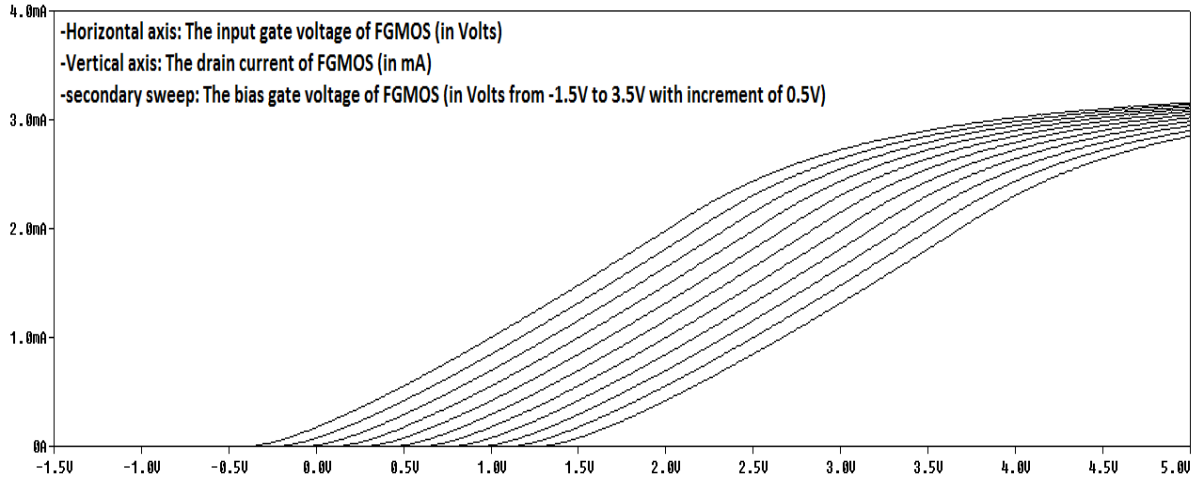


Figure 9: The variation of effective threshold of FGMOS with the bias voltage

3.3 Current-Voltage Characteristics of FGMOS

As it has been discussed at the starting of the chapter 3 current voltage characteristics of FGMOS transistor are similar to that of MOSFET. This happens because if the device is fabricated only with ILD1 and metal-1 in Figure 2, then it would resemble the physical structure of conventional MOSFET. This means if control gate of FGMOS is removed then it will behave as normal MOSFET. Moreover, introduction of control gate provides threshold programmability rather changing the operation of MOSFET. Thus it is necessary to explore how much similarity is there between current voltage characteristics of FGMOS and conventional MOSFET. In the following sections (section 3.3.1 and 3.3.2) I_D-V_{GS} and I_D-V_{DS} characteristics of FGMOS are observed.

3.3.1 I_D-V_{GS} Characteristic of FGMOS

In Figure 10, I_D-V_{GS} characteristic of FGMOS is plotted. This plot is obtained by using 0.5 um parameter file. The aspect ratio W/L of the FGMOS is 60um/1um. The voltage applied at bias gate is 1.5V.

In Figure 11, I_D-V_{GS} characteristic of conventional MOSFET is plotted. This plot is obtained with same parameter file and aspect ratio as that of FGMOS.

Comparing Figure 10 and Figure 11, it is obvious that the threshold voltage of FGMOS for the same aspect ratio is nearly 0.3V as that of 0.6V of conventional MOSFET.

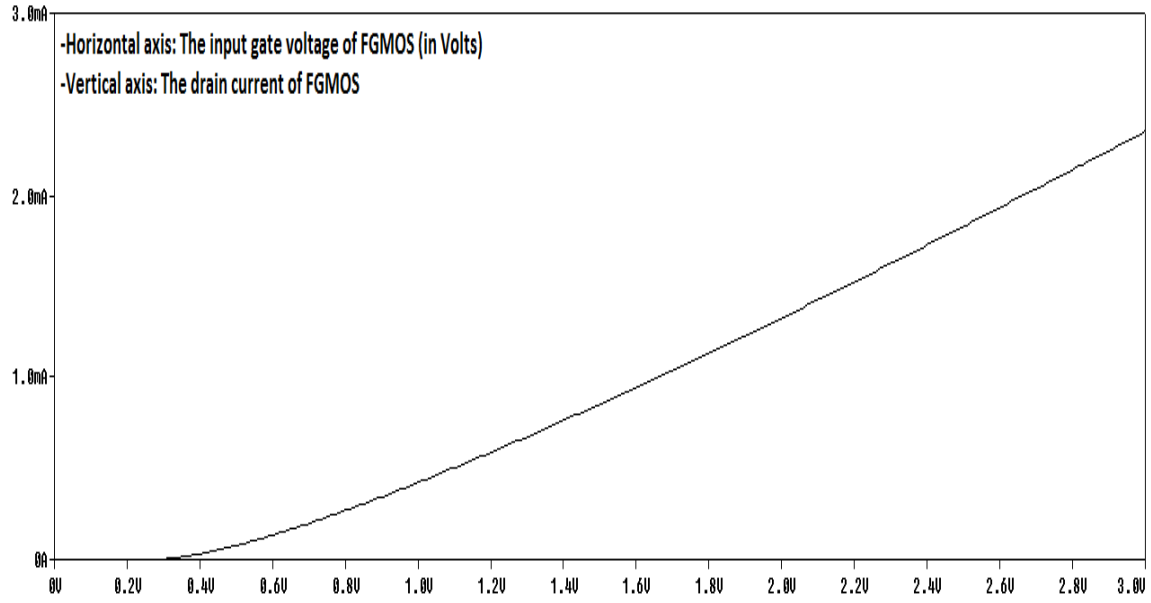


Figure 2: I_D-V_{GS} characteristic of FGMOS

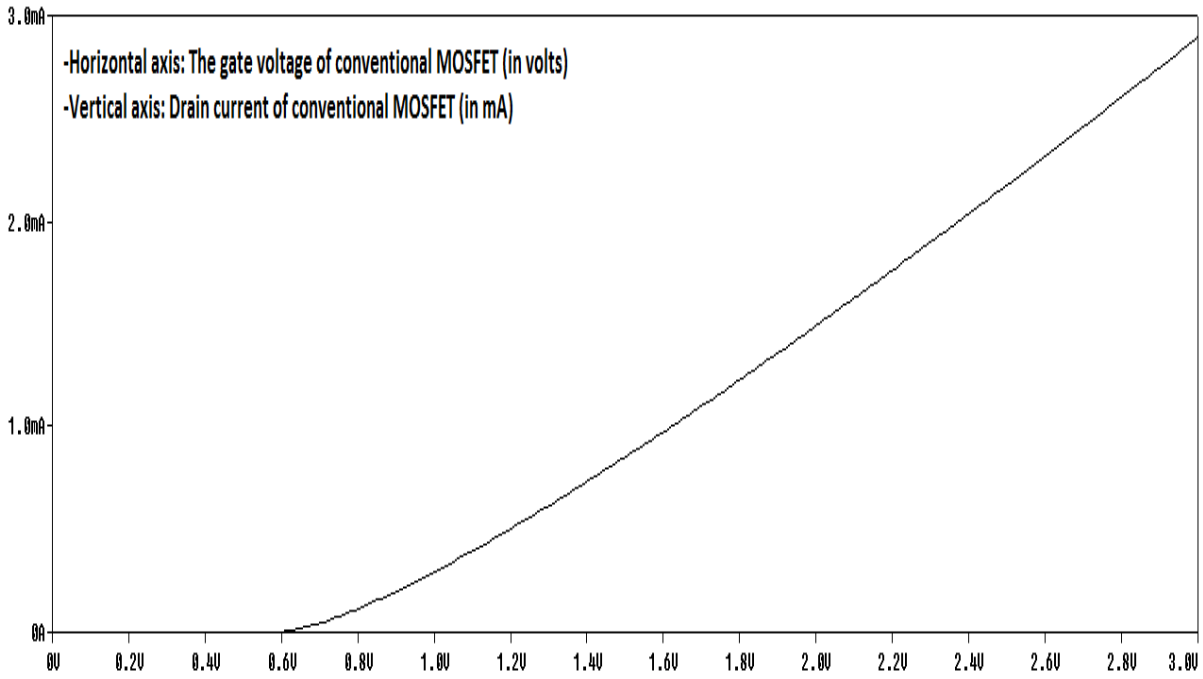


Figure 3: I_D-V_{GS} characteristic of MOSFET

3.3.2 I_D-V_{DS} Characteristic of FGMOS

The drain current equation of an FGMOS transistor is obtained by modifying conventional MOSFET drain equation.

$$I_{DS}^{o} = \left\{\left[\left(\frac{\sum_{i=1}^{N} C_i V_i}{C_T}\right) - V_{SS} - V_T\right] V_{DS} - \frac{1}{2} V_{DS}^2\right\} \quad (8)$$

$$I_{DS}^{S} = \frac{K_n}{2}\left\{\left(\frac{\sum_{i=1}^{N} C_i V_i}{C_T}\right) - V_{SS} - V_T\right\}^2 \quad (9)$$

Here I_{DS}^{o} is the drain current while FGMOS is operating in ohmic region and I_{DS}^{S} is the drain current while FGMOS is operating in saturation region.

Here $K_n = \mu_n C_{ox}(W/L)$ denotes the transconductance parameter, μ_n denotes the electron mobility, C_{ox} stands for capacitance per unit area of gate-oxide, W/L stands for the aspect ratio of the transistor, and V_T ddenotes the threshold voltage of FGMOS transistor. The characteristics obtained after simulation are plotted in Figure 12. This plot is also obtained with W/L ratio equal to 60 um/ 1 um and using 0.5 um parameter file.

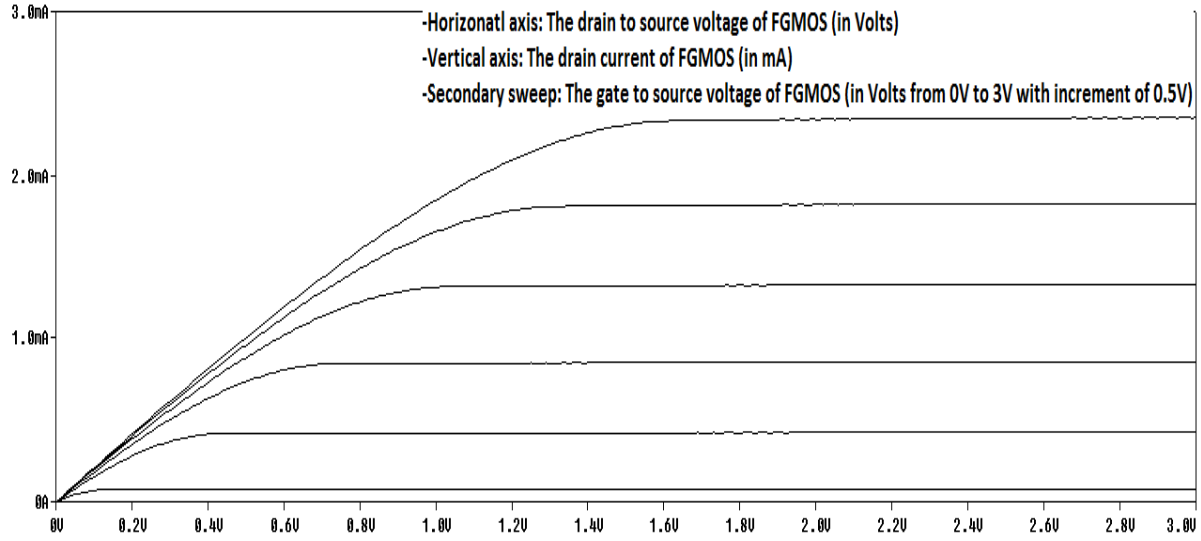


Figure 4: I_D-V_{DS} characteristic of FGMOS

3.4 Small Signal Model of FGMOS

The effective transconductance of a two input FGMOS can be written as

$$g_{m,eff} = K_2 g_{m,FG} = (1 - K_1) g_{m,FG} = g_{m,FG} - K_1 g_{m,FG} \quad (10)$$

Here transconductance seen from the floating gate is $g_{m,FG}$. It can be noted here that the effective transconductance is less than $g_{m,FG}$ by a factor of $K_1 g_{m,FG}$.

To obtain the output impedance of the FGMOS transistor, all the inputs should be connected to AC ground and a voltage source must be applied at the drain of the FGMOS transistor. The small signal model of Figure 13 is used for this purpose.

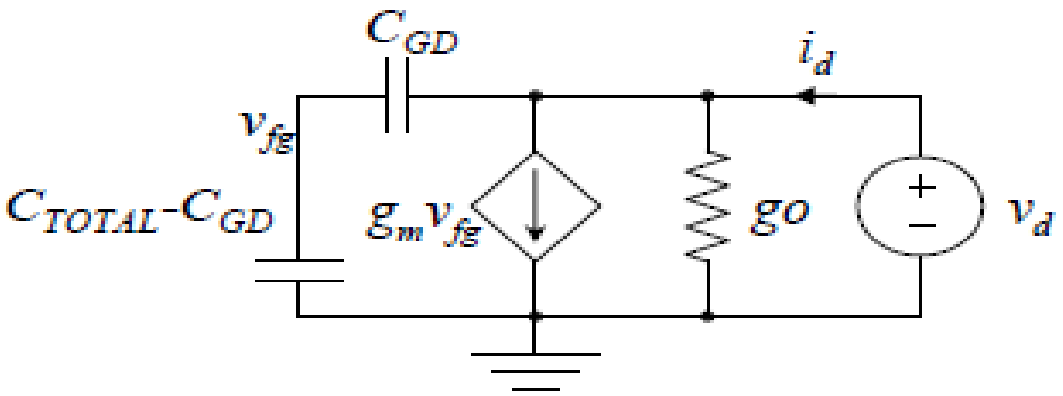


Figure 13: The small signal model of FGMOS transistor

The calculation of $g_{o,eff}$ obtains the following result

$$g_{o,eff} = \left({}^{C_{GD}}/_{C_{Total}} \right) g_m + g_o \quad (11)$$

Equation (11) shows that the output impedance of FGMOS transistor is less than that of MOSFET. This is because in FGMOS there is a DC and AC feedbacks from drain to floating gate through C_{GD}.

3.5 FGMOS Transistor in Sub-threshold region

A conventional MOSFET works in both weak inversion (sub-threshold region) and strong inversion. In fact weak inversion or sub-threshold operation of MOSFET is used for low voltage applications in many analog building blocks. Similarly an FGMOS transistor also works in both sub-threshold and above threshold. The models and equations which have been introduced till now are valid for FGMOS in strong inversion.

In sub-threshold region of operation, surface potential depends upon control gate voltages. Using existing sub-threshold MOSFET models [17-19], a sub-threshold FGMOS model has been developed. The current voltage relationship of MIFGMOS transistor is written as-

$$I_D = \frac{W}{L} I_o \, e^{\frac{\kappa C_{fc}(V_1 + \ldots\ldots\ldots\ldots + V_n)}{C'_{sum} U_t}} \, e^{\frac{\kappa\left(C_{fs} V_{SB} + C_{fd} V_{DB}\right)}{C'_{sum} U_t}} \left(e^{\frac{-V_{SB}}{U_t}} - e^{\frac{-V_{DB}}{U_t}} + \frac{V_{DS}}{V_0}\right) \quad (12)$$

Here $C_{sum}^{'} = C_{sum} - \kappa C_{ox}$ is gate efficiency. The saturation region transconductance is written as

$$g_{m,eff} = {\kappa' I_D}/{U_t} \quad (13)$$

Here $\kappa^{'} = \kappa C_{fc}/C^{'}_{sum}$.

The output conductance of FGMOS in saturation region is written as

$$g_{o,eff} = \left({I_D}/{V_O}\right) + \left({\kappa'' I_D}/{U_t}\right) \quad (14)$$

Here κ” = $\kappa C_{fd}/C^{'}_{sum}$.

3.6 Conclusion

In this chapter SPICE model of FGMOS without floating gate charge and with floating gate charge is explained. Using the SPICE model explained it is also shown that threshold of FGMOS can be reduced considerably by varying the voltage of one of the control gates called bias gate. Once it is explained that working of FGMOS is similar to that of conventional MOSFET, current-voltage characteristics of FGMOS are also plotted using SPICE model. Also, the small signal model of FGMOS for AC analysis is also

discussed. In the end the sub threshold operation and current voltage relationships of FGMOS in sub threshold region are also discussed.

4. ANALOG APPLICATIONS OF FGMOS TRANSISTOR

The FGMOS transistor has many applications in analog circuits. The threshold programmability feature of FGMOS makes it attractive for low voltage applications. Some of popular applications of FGMOS transistor is analog circuits are listed below.

- Multiple input OTAs and Op-amps
- Low voltage circuits such as current mirrors
- Neural networks
- Digital to analog and Analog to digital converter

In this chapter a literature survey is presented enlisting different analog domain applications of FGMOS based designs. In the section 4.2 basic applications such as current mirrors, implementation of resistances and a tunable filter are studied.

4.1 Literature Survey

In literature numerous analog applications of FGMOS are reported which can be divided broadly into three categories as below

i. Transistor level circuits
ii. Basic analog cells
iii. Active building blocks using FGMOS

4.1.1 Transistor Level Circuits using FGMOS

In transistor level circuits applications such as "Linear MOSFET based on FGMOS" [16], "Realization of grounded resistor" [20], Voltage multipliers [21], and voltage squarer [22] etc. are found. Out of these linear MOSFET based on FGMOS and grounded FGMOS resistor are discussed in detail in sections 4.2 and 4.3

"A one quadrant multiplier/divider using FGMOS" is reported in [21]. Schematic of this multiplier/divider is shown in Figure 14.

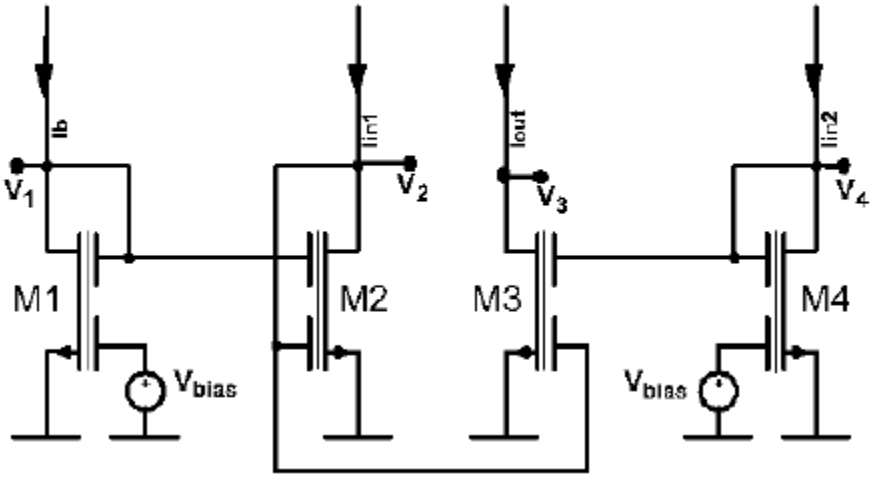


Figure 14: One quadrant multiplier/divider using FGMOS [21]

Applying the translinear principle of [23, 24], the following relation, between $I_{b,}$ I_{in1}, I_{in2} and I_{out} is obtained

$$I_{out}I_b = I_{in1}\, I_{in2} \tag{15}$$

Another transistor level circuit reported in the literature is "Differential voltage squarer using FGMOS" [22]. Schematic of this is shown in Figure 15.

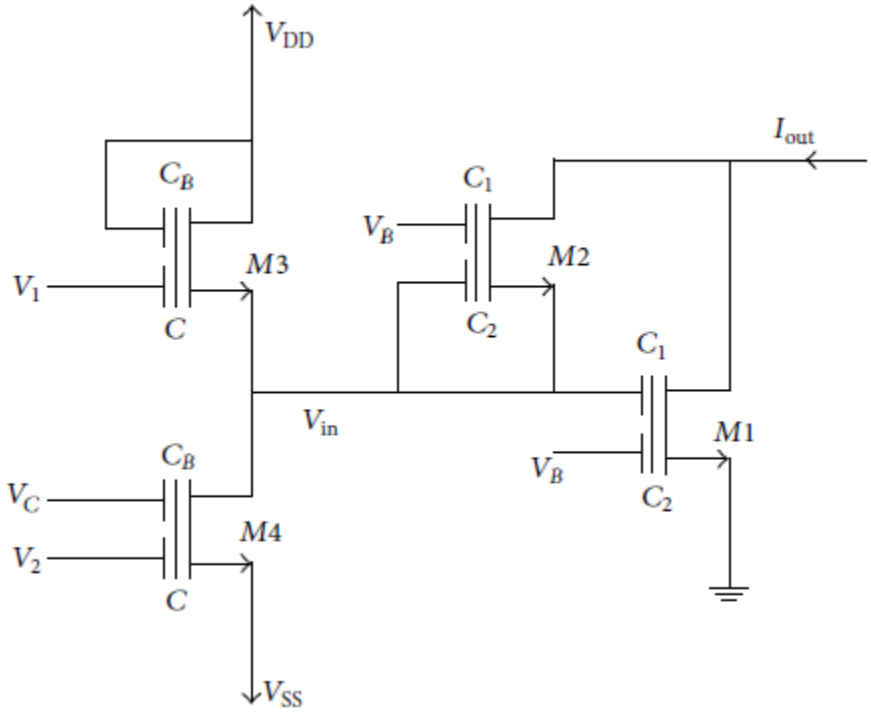


Figure 15: Differential voltage squarer [22]

In voltage squarer of Figure 15, M1-M2 realizes squarer based on FGMOS and M3-M4 realizes voltage attenuator using FGMOS. The square law property of FGMOS gives output current I_{out}-

$$I_{out} = \frac{\beta}{2} k V_{in}^2 \quad (16)$$

Where $\beta = \mu_n C_{ox}(W/L)$ and $k = k_1 = k_2 = (C_i/C_{total})$ of FGMOS transistor.

The voltage attenuator M3-M4 is responsible for generating $V_{in} = V_1 - V_2$ [22]. Thus the expression for output current can be written as-

$$I_{out} = \frac{\beta}{2} k\, \alpha (V_1 - V_2)^2 \quad (17)$$

Where α is the attenuation factor of voltage attenuator.

In this section some novel applications of FGMOS transistor for transistor level circuits are discussed. But applications of FGMOS are not limited to transistor level circuits. In the next section some analog cells such as gilbert's cell are discussed which use FGMOS for its operation.

4.1.2 Analog Cells using FGMOS

Current mirror and gilbert cell are some basic analog cells which are important part of many building blocks. Using FGMOS current mirror [25] and gilbert's cell [26] have been reported in the literature. Apart from simple current mirrors "Wilson current mirror "[27] and "Ultra low voltage current mirror based on FGMOS" [28] also exist in literature. In section 4.5 simple current mirror pair is discussed at length with comparison to conventional MOSFET counterparts. In this section some other applications are described.

The gilbert's cell of [26] with is voltage divider application is introduced here. Schematic of this gilbert's cell based divider is shown in Figure 16, where input differential MOSFETs are replaced with FGMOS transistors.

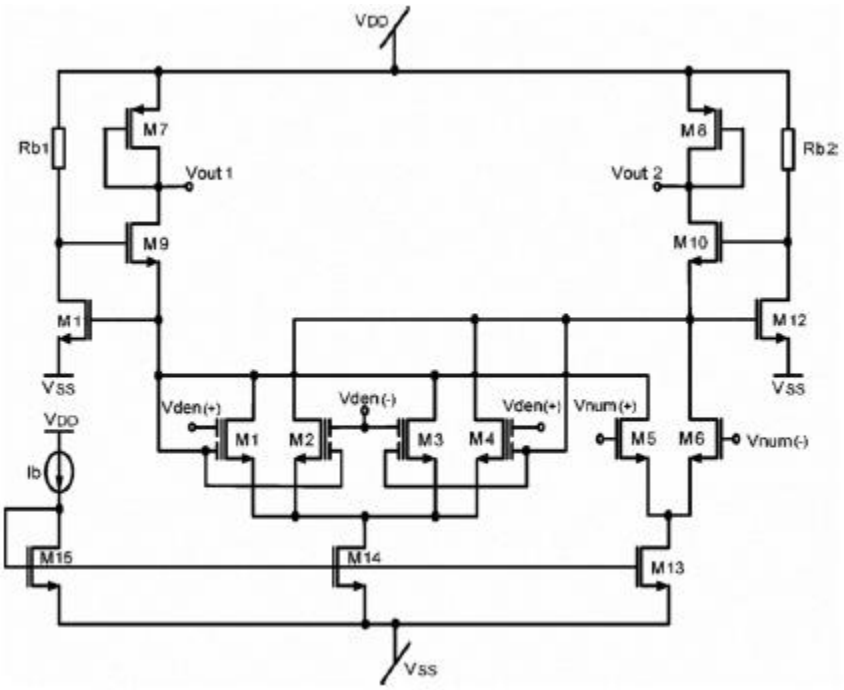


Figure 16: Voltage divider using FGMOS based gilbert's cell [26].

In this divider to get very low input impedance transimpedance amplifier is realized by M7-M12 and cross coupled differential amplifier of gilbert's cell is realized by M1-M4 using FGMOS. The tail current source is realized by M5 and M6 transistors. It has been discussed earlier in the section 2.4 (equation 2) that looking from the floating gate, a FGMOS can work as adder. In the divider of [26] MIFGMOS transistors are used as adders and output voltage is feedback along with input voltage at MIFGMOS adders.

History of analog circuits and designs shows that current mirrors are very much integral part of analog signal processing and many active building blocks use them to perform their operations. In this section it has been shown that current mirrors and other analog cells are implemented with FGMOS which gives rise to the idea that using these cells active building blocks can also be realized i.e. it is possible to achieve low power operations of active building blocks using FGMOS transistors instead of MOSFETs. In the next section some of these active building blocks such as "Operational transconductance amplifier (OTA)", "Current conveyor (CC)" etc. are introduced which are based on FGMOS transistors.

4.1.3 Active Building Blocks using FGMOS

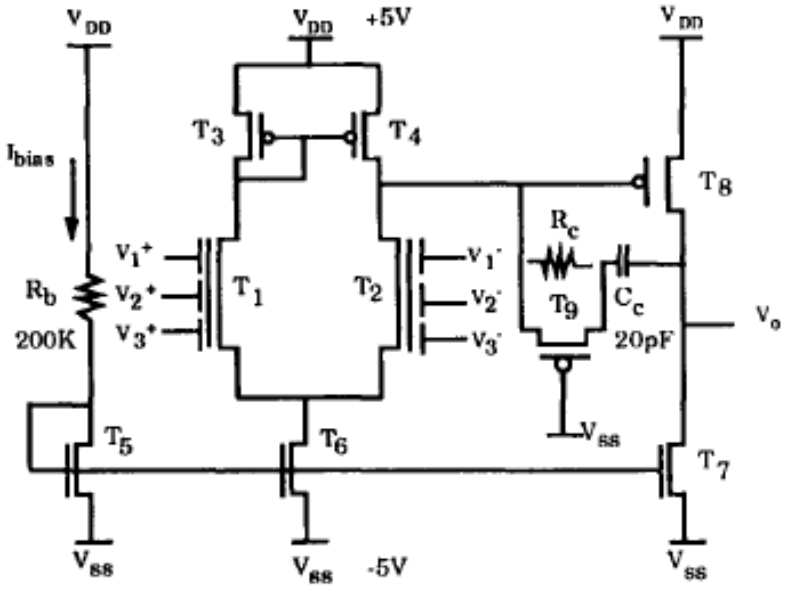
The conventional operational amplifier (op-amp) has only one differential input pair and hence the relation between output of the op-amp and differential input is given as-

$$V_{out} = A\,(V_+ - V_-) \tag{18}$$

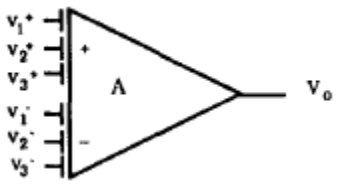
Using MIFGMOS transistor as differential input transistors it is possible to obtain multiple differential input op-amp [29]. The transistor model for MIFGMOS has been discussed in section 2.4. Using that transistor model the output voltage equation of normal op-amp is modified in context of MIFGMOS op-amp of [29] as below-

$$V_{out} = A\,[(V_{1+} - V_{1-}) + (V_{2+} - V_{2-}) + \ldots\ldots\ldots\ldots + (V_{n+} - V_{n-})] \tag{19}$$

The circuit and symbol of multiple input op-amp are shown in Figure 17.



(a)



(b)

Figure 17: Multiple input op-amp (a): circuit (b): symbol

Another popular building block in analog domain is “Operational transconductance amplifier (OTA)”. The realization of OTA using FGMOS has also been reported in literature and similar to MIFGMOS op-amp it has also multiple differential inputs as it also uses MIFGMOS in its structure [29].

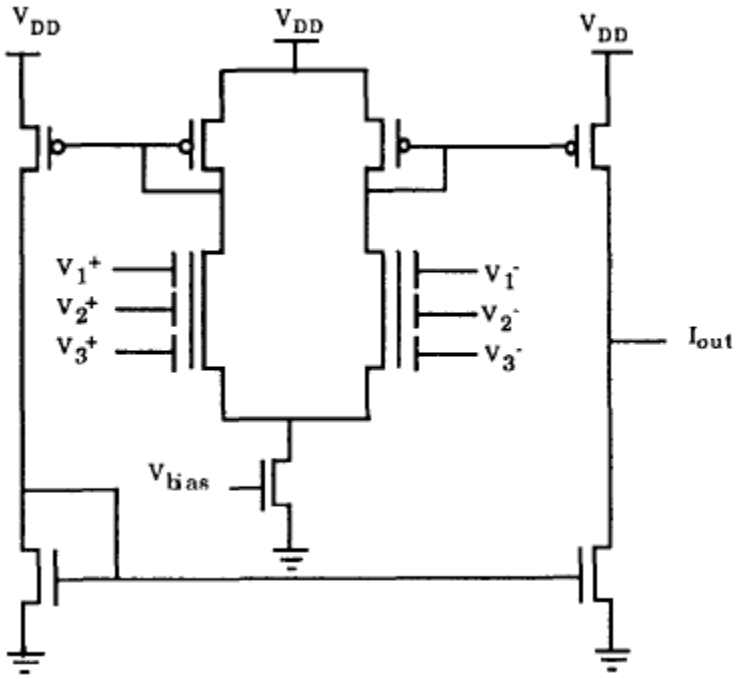
The expression for output current of a conventional OTA is written as-

$$I_{out} = G_m(V_+ - V_-) \quad (20)$$

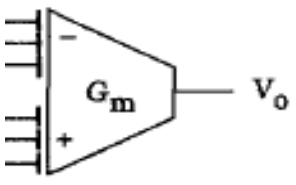
Like multiple input op-amp, the output current equation for multiple input OTA also needs to be modified as below-

$$I_{out} = G_m[(V_{1+} - V_{1-}) + (V_{2+} - V_{2-}) + \ldots\ldots\ldots\ldots + (V_{n+} - V_{n-})] \quad (21)$$

The circuit and symbol of MIFGMOS based OTA is shown in Figure 18.



(a)



(b)

Figure 18: Multiple input OTA (a): circuit (b): symbol

To prove the worth of OTA of [29] a differential integrator [30] is also discussed which use multiple inputs OTA of [29] to perform the task. The circuit of this integrator is shown in Figure 19. In Figure 19, using the output current relation of (21)

$$I_{out} = G_m [(0 - V_o) + (V_+ - V_-)] \quad (22)$$

This, upon solving, reduces to the following equation-

$$V_o (G_m + Sc) = G_m (V_+ - V_-) \quad (23)$$

Solving (23) yields the following equation-

$$V_o = \frac{1}{s\tau+1} (V_+ - V_-) \quad (24)$$

Where $\tau = C/G_m$

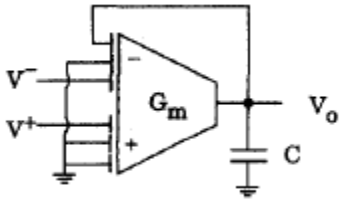


Figure 19: Differential integrator using OTA of [29].

Apart from op-amps and OTAs current conveyor has also been reported [31]. This is a class AB type second generation current conveyor and works on ultra-low voltage.

It has been shown in this section that from transistor level circuits to active blocks, many analog signal processing circuits are reported in the literature. Whereas, transistor level circuits example are resistors and multipliers, analog cell designs example are current mirrors and gilbert's cell and active blocks example are op-amp and OTAs. Some of the applications have been introduced and some the applications were left for detailed discussion in upcoming sections. In the next two sections, linear MOS using FGMOS, grounded resistor using FGMOS and simple current mirrors using FGMOS are discussed in detail.

4.2 Linear MOS transistor based on FGMOS

It is also possible to get linear I_D-V_{GS} characteristic using an FGMOS transistor [16]. For this purpose floating voltage sources are used at the control gates. The circuit for this operation is given in Figure 19.

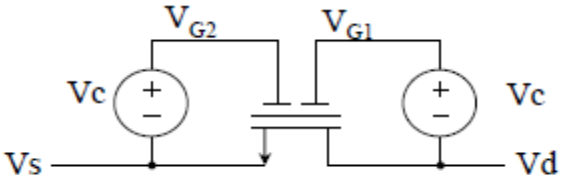


Figure 20: Implementation of linear MOS using FGMOS [16]

In this circuit

$$V_{G1} = V_C + V_D \tag{25}$$

And

$$V_{G2} = V_C + V_S \tag{26}$$

Here the floating gate voltage is written as

$$V_F = k_1(V_C + V_D) + k_2(V_C + V_S) \tag{27}$$

If the transistor is kept in triode region

$$I_{DS} = K_P \frac{W}{L}\left(V_{FGS} - V_T - \frac{V_{DS}}{2}\right)V_{DS} = K_P \frac{W}{L}\left[(k_1 + k_2)V_C + \left(k_1 - \frac{1}{2}\right)V_D + \left(k_2 - \frac{1}{2}\right)V_S - V_T\right]V_{DS} \tag{28}$$

If $k_1 = k_2 = ½$, the above equation can be rewritten as

$$I_{DS} = K_P \frac{W}{L}(V_C - V_T)V_{DS} \tag{29}$$

Equation (19) verifies the linear relationship between V-I.

Figure 21 shows current vs. voltage curves for linear MOS using FGMOS. The plot is obtained using 0.5 um parameter file, aspect ratio W/L is chosen 60 um/1 um.

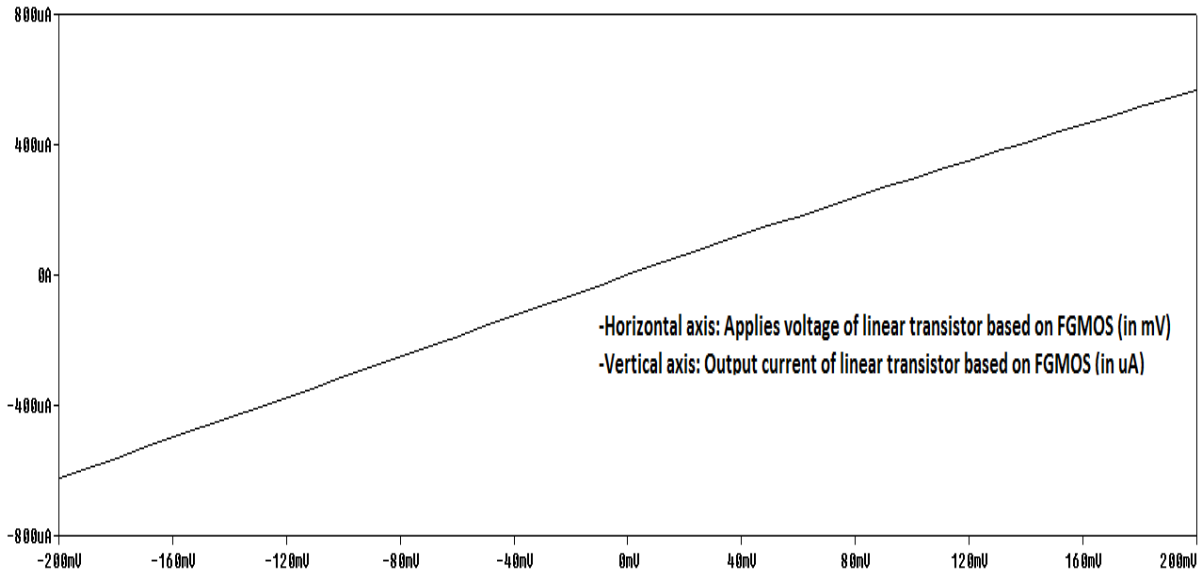


Figure 21: Current vs. voltage curve for linear MOS based on FGMOS

4.3 A controllable grounded resistance based on FGMOS transistor

Another useful application of FGMOS transistor is the implementation of "A voltage controllable grounded resistance" [32] using low supply voltage. Figure 22 shows the circuit for this purpose.

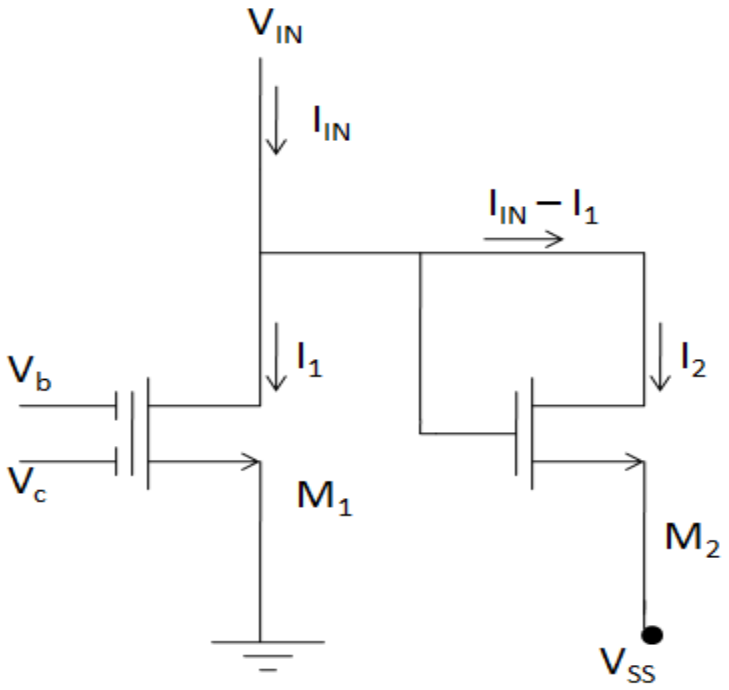


Figure 22: Grounded resistance based on FGMOS transistor [32]

In the figure the current I_1 and I_2 are given by following equations

$$I_1 = K_{n1}\left\{[k_{11}(V_b - V_{ss}) + k_{12}(V_c - V_{ss}) - V_{Tn1}]V_{IN} - \frac{V_{IN}^2}{2}\right\} \quad (30)$$

$$I_2 = \frac{K_{n2}}{2}(V_{IN} - V_{SS} - V_{Tn2})^2 \quad (31)$$

Here K_{ni}, k_{ij}, V_i have their usual meanings.

The total input current is the summation of I_1 and I_2.

$$I_{IN} = I_1 + I_2 \quad (32)$$

To cancel the square terms of V_{IN} the values of k_{n1} and k_{n2} are chosen such that $k_{n1} = k_{n2}$. It has been mentioned already that $k_{11} + k_{12} = 1$ for any FGMOS transistor. Thus the current I_{IN} can be written as

$$I_{IN} = K_{n1}[(k_{11}V_b + k_{12}V_C - V_{Tn1}) - (V_{SS} + V_{Tn2})] + I_{offset} \quad (33)$$

Here I_{offset} is proportional to the square of $V_{ss} + T_{Tn2}$. From equation (33) it is cleared that if the offset current is compensated then a linear relationship between input current and input voltage can be obtained. Using a current mirror which supplies the current equivalent to the $I_{offset,}$ this offset current can be eliminated and perfect relationship can be obtained. The circuit for this purpose is shown in Figure 23.

The aspect ratio of transistors in Figure 23 are listed below-

Transistor number	Aspect ratio (W/L)
M1	2 um/ 0.5 um
M2 and M3	2 um/ 0.5 um
M4 and M5	10 um/ 0.5 um

Table 1: Aspect ratios of transistors of figure 23.

Once the linearity is maintained, the resistance can be given by the following equation-

$$R_{equ} = \frac{V_{IN}}{I_{IN}} = \{K_{n1}[(k_{11}V_b + k_{12}V_C - V_{Tn1}) - (V_{SS} + V_{Tn2})]\}^{-1} \quad (34)$$

The input range of voltage is decided by the voltage that keeps transistor M1 in ohmic region i.e. $0 \leq V_{IN} < (k_{11}V_b + k_{12}V_C - V_{Tn1})$.

The I_{IN} vs. V_{IN} characteristic for this grounded resistance is shown in Figure 24. The plot is obtained using 0.25 um parameter file which is given in appendix.

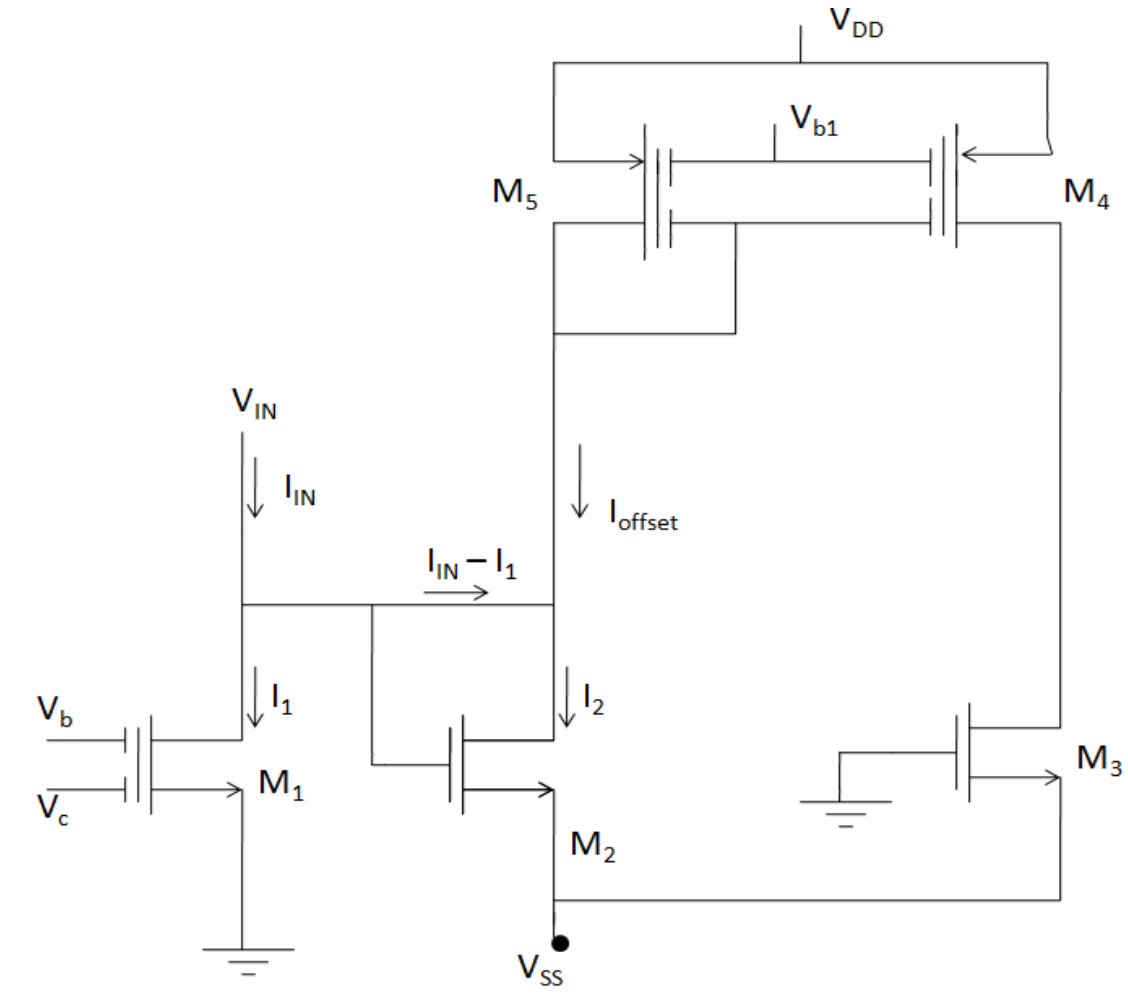


Figure 23: Offset elimination in the grounded resistor based on FGMOS transistor [32]

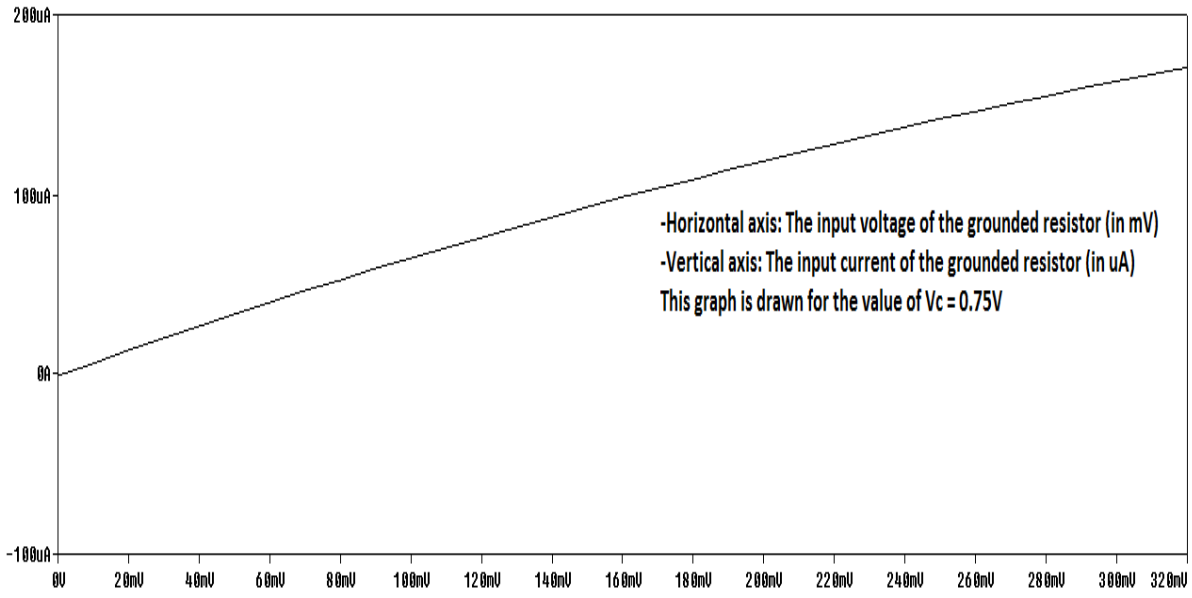


Figure 24: Curve between input current and input voltage for FGVCGR

4.4 Tunable high pass filter using FGVCGR

The above discussed grounded resistor i.e. Floating Gate Voltage Controllable Grounded Resistance (FGVCGR) [32] can be used in many communication and signal processing applications however in this section a simple high pass filter is implemented. The circuit for this realization is shown in Figure 25.

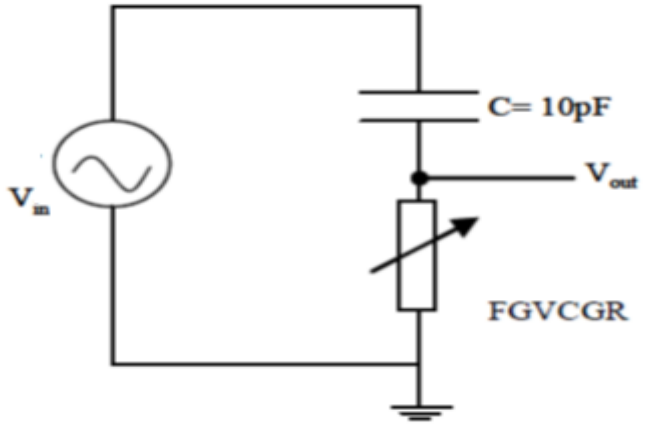


Figure 25: Tunable high pass filter using FGVCGR [32].

The high pass characteristic of this circuit is shown in Figure 26.

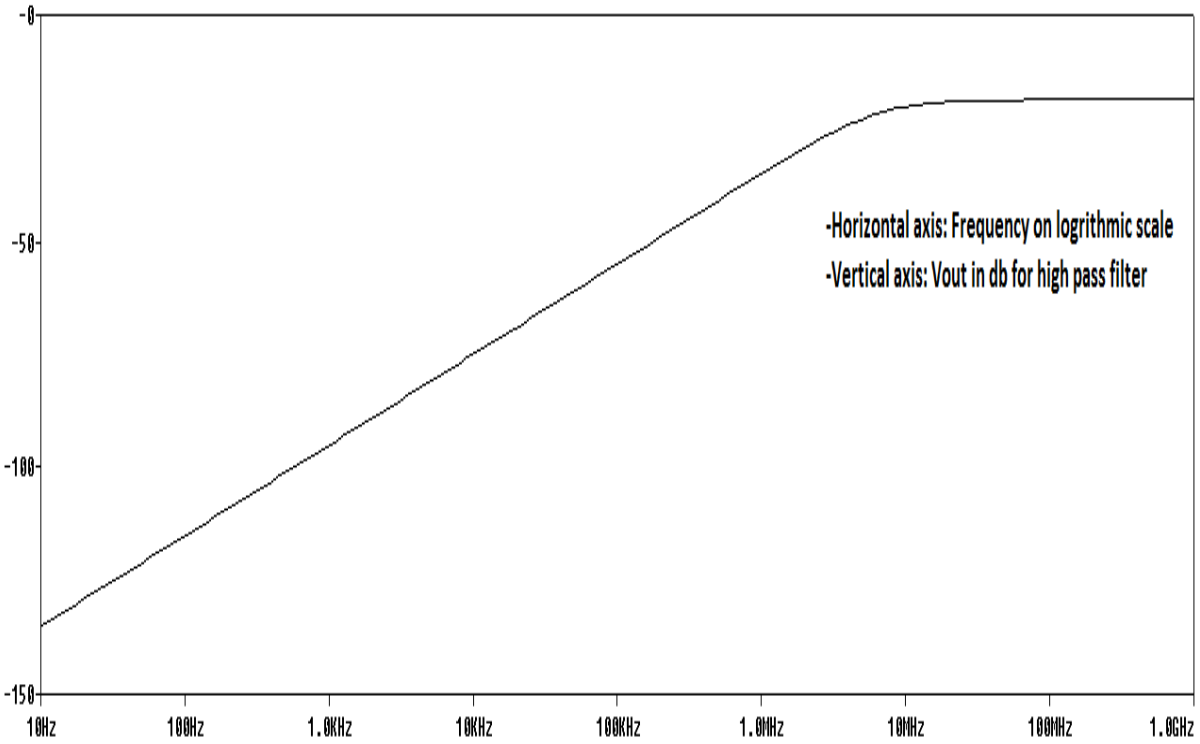


Figure 26: Characteristic of high pass filter using FGVCGR

4.5 Current mirrors based on FGMOS transistors

In this section simple current mirror using FGMOS [16] is discussed. This is also compared with its counterpart using conventional MOSFET transistors.

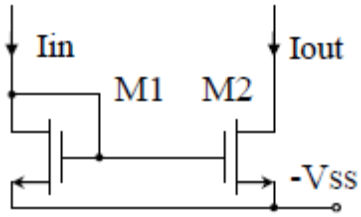


Figure 27: Conventional current mirror

Figure 27 shows the conventional current mirror. It may be noted that in this current mirror there is a voltage drop of $V_T + V_{DSAT}$ at transistor M1. This much of voltage drop is very large in some low voltage applications. Reducing or removing the V_T can be one of the solutions for this problem. It is achieved by replacing the conventional MOSFET pair with FGMOS transistor pair. Figure 28 shows the simple current mirror using FGMOS transistors.

In this current mirror by choosing the proper value of biasing voltage V_b the threshold voltage is reduced and the minimum supply requirement can be lowered. Figure 29 and Figure 30 show the I_D v/s V_{DS} characteristic of conventional and FGMOS based simple current mirrors respectively. Figure 31 and Figure 32 show the input characteristic of conventional and FGMOS based simple current mirrors respectively. All these plots are obtained using 0.5 um parameter file and aspect ratio of all transistors are chosen 60 um/ 1 um.

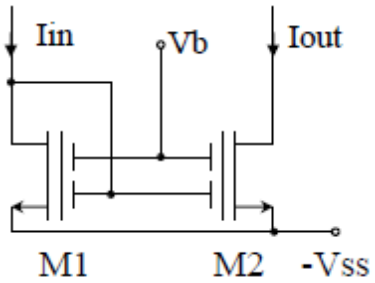


Figure 28: Simple current mirror based on FGMOS transistor

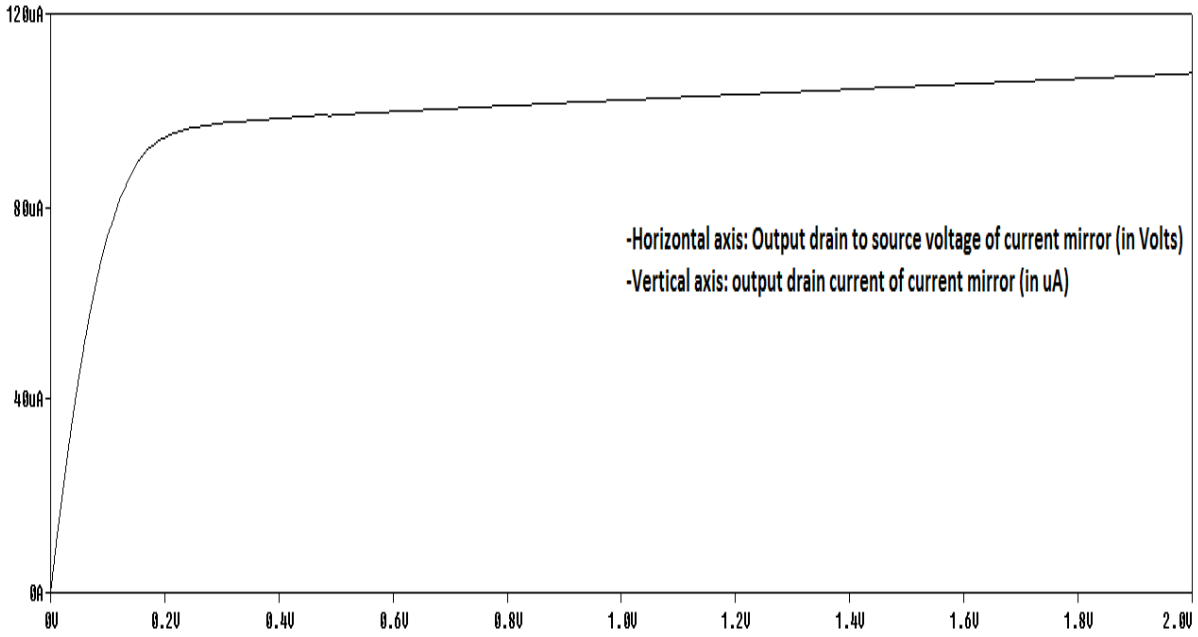


Figure 29: I_D v/s V_{DS} characteristic of conventional simple CM.

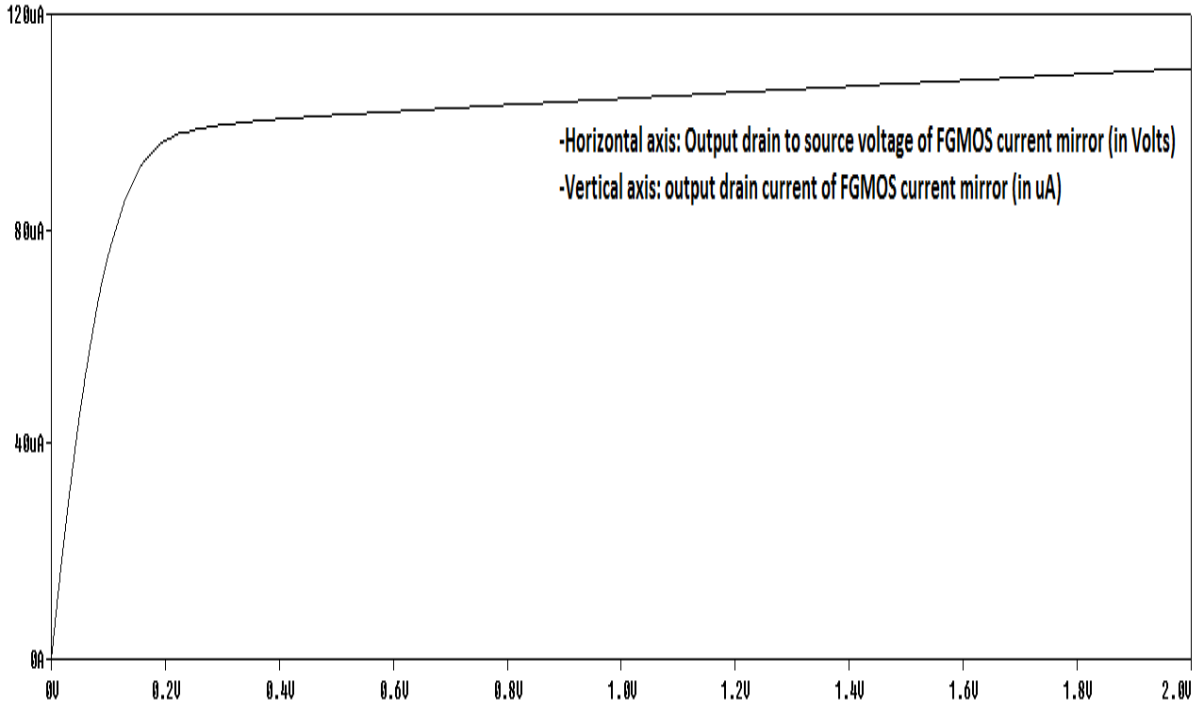


Figure 30: I_D v/s V_{DS} characteristic of FGMOS based simple CM.

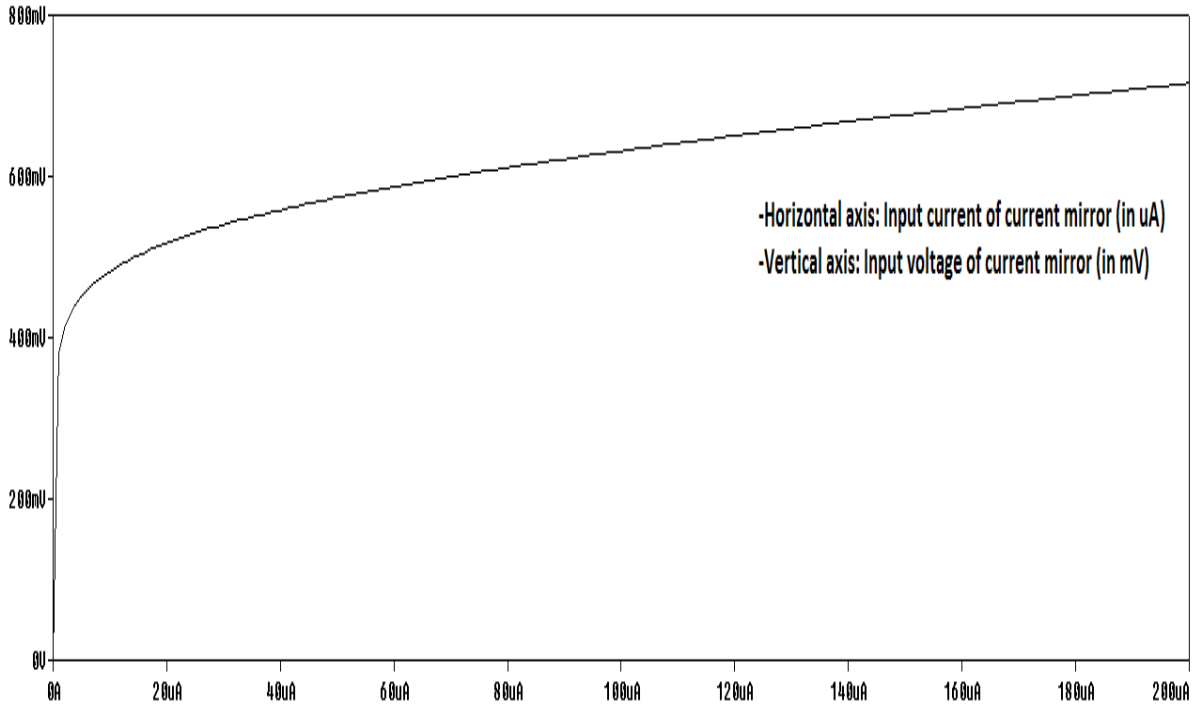


Figure 31: Input characteristic of conventional simple CM

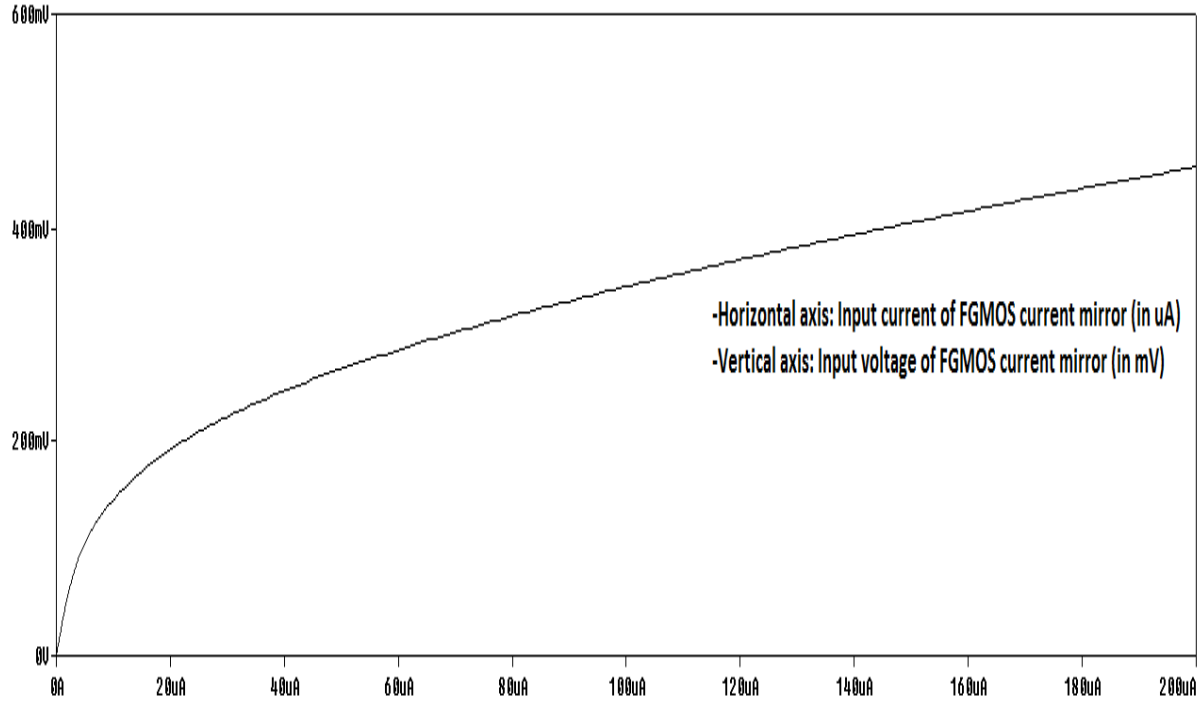


Figure 32: Input characteristic of FGMOS based simple CM.

4.6 Conclusion

In this chapter a literature review of applications of FGMOS in analog domain is presented. It shows that FGMOS are used from transistor level circuit to active building block designs. A voltage multiplier/divider application is discussed. In analog cells, gilbert's cell using FGMOS is discussed and multiple input op-amp and OTA with their operations are explained. Also a differential integrator is illustrated using multiple inputs FGMOS. This is followed by detail discussion of FGMOS based linear MOS, grounded resistor using FGMOS and simple current mirror using FGMOS. Their characteristics are also plotted.

5. CURRENT MODE CIRCUITS, CDBA AND DDCC

One of the major breakthroughs in the field of low power electronics, in recent years, is current mode design and applications, which have emerged as an alternative to voltage mode designs chiefly mainly in analog and mixed mode signal processing applications.

In voltage mode circuits, the dynamic range is limited by the minimum threshold voltage required for the operation of MOSFETs. Thus for low power low voltage applications, voltage mode circuits are not a suitable choice, specially in the field of portable electronics. In case of current mode circuits, the operation is decided by the current and it enables the scope of dynamic range of operation in analog circuits and systems. The accuracy of MOS current mirrors is high and their sensitivity to process variation is also less. This factor also motivates the idea of using MOS transistors with current signals in preference to voltage counterparts. Therefore integrated current mode circuit realization is very much closer to the transistor level as compare to conventional voltage mode circuits. Another problem with voltage mode is speed limitation imposed by parasitic capacitances. If voltage mode signals are widely distributed, the charging and discharging of parasitic capacitances happen with full voltage swing and this causes low speed of operation apart from increased power consumption. Even though, current mode circuits are also unable to avoid high voltage swings at nodes but in case of current mode signals, nodes are generally local having less parasitic capacitances, which enables higher speed of operation with low dynamic power consumption.

The commercial viability of current feedback operational amplifier was a major breakthrough in current mode applications. The reason current mode circuits are receiving researcher's attention considerably, apart from low voltage and low power consumption are-

- Wider bandwidth, in some cases independent of close loop gain.
- Relatively high slew rate
- Some current mode circuits can be used in voltage mode also. This provides additional flexibility.

A large number of current mode active building blocks are available in literature. Some of popular building blocks are current conveyor, current operational amplifier

(COA), operational transconductance amplifier (OTRA), Current differencing buffered amplifier (CDBA), Differential difference current conveyor (DDCC), and differential voltage current conveyor (DVCC). These blocks have been designed using conventional MOSFETs. The FGMOS based integrated designs for current conveyor [31] and OTA [29] are also available in literature. This gave an insight of designing other active blocks using FGMOS.

In this chapter two current mode building blocks namely "Current differencing buffered amplifier (CDBA)" and "Differential differencing current conveyor (DDCC)" have been proposed using FGMOS to achieve low power low voltage operations. These are functionally verified through simulations using 0.18 um parameter file for CDBA and 0.5 um parameter for DDCC on PSPICCE simulation software tool. To justify the worth of proposed building blocks few applications using these blocks are also implemented and verified through simulations.

Before giving the design details of the proposed blocks an introduction of conventional CDBA followed by DDCC is presented. This is followed by description of low voltage CDBA realization [37] and detailed analyses of this structure. This realization is illustrated at length as it has been used to propose FGMOS based CDBA realization. In next section new structure of CDBA using FGMOS is proposed, its DC and AC transfer characteristics and impedance magnitudes are plotted and verified. Using the proposed CDBA a second order high pass filter is implanted and its functionality is verified through SPICE simulations.

As it has been mentioned earlier in this section that another building block which is proposed in this chapter is FGMOS based DDCC. So after proposing CDBA and implementing its application a basic introduction to DDCC is given. This is followed by the terminal relationships of DDCC and its working. Then new structure of DDCC based on FGMOS is proposed and its terminal relations are verified. Finally a full wave rectifier is implemented using the proposed DDCC and its DC and transient responses are obtained, which justifies the usefulness of DDCC.

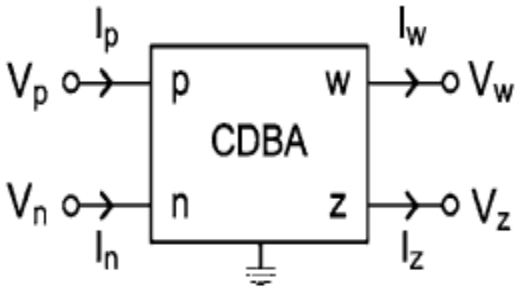
5.1 Current Differencing Buffered Amplifier (CDBA)

CDBA was proposed by "Acar" and "Ozoguz" in 1999 [33]. It comprises unity gain current differential amplifier and unity gain voltage amplifier. Thus it is suitable for both current and voltage mode signal processing applications. It is also suitable for high frequency operations since it is free from many parasitic capacitances.

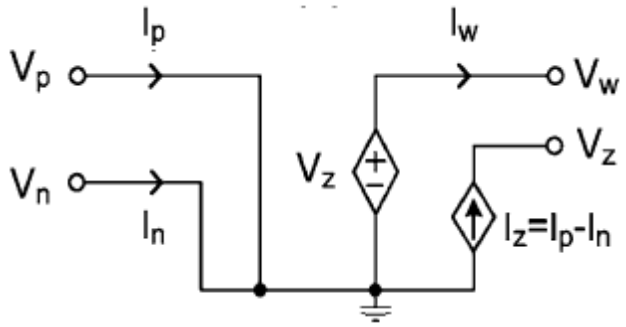
The block diagram and equivalent circuit of the CDBA is shown in Figure 33, where *p* is positive input current terminal, *n* is negative current input terminal, *z* is current output terminal and *w* is voltage output terminal. Its voltage and current characteristics or terminal relationships can be described by the following equations-

$$V_p = V_n\,,\; I_z = \alpha_p I_p - \alpha_n I_n\,, V_w = \beta_z V_z \qquad (35)$$

Where $\alpha_p$and α_n are current gains and β_z is the voltage gain. Ideally, all these gains should be equal to one but practically they are expressed as $\alpha_p = 1-\varepsilon_p$, $\alpha_n = 1-\varepsilon_n$ and $\beta_z = 1- \varepsilon_v$ where ε_p and ε_n are current tracking errors and ε_v is voltage tracking error with $|\alpha_p|$, $|\alpha_n|$ and $|\beta_z| << 1$. I_p and I_n are current inputs of the CDBA whose difference is available at the terminal *z* which means terminal *z* works as a current source. Hence terminals *p* and *n* should have low impedances (ideally zero) and terminal *z* should have high impedance (ideally infinite). Also, the voltage at terminal *w* follows the voltage at terminal *z*, which means terminal *w* is voltage output terminal and should have low impedance (ideally zero).



(a)



(b)

Figure 33: CDBA (a): The block diagram (b): The equivalent circuit

Many realizations of CDBA are available there in the literature. One of them uses two current feedback operational amplifier (CFOA) [34]. Apart from this realization several other realizations have also been reported [35, 36]. However, these realizations have quite high value of terminal resistances, generally of the order of hundred ohms. Also their current transfer ratio and voltage transfer ratio are found to be less than unity. Additionally, most of the CDBAs are operated at high voltage, thereby have much power dissipation.

The prime goal of this work is to propose a CDBA structure which overcomes the supply voltage problem of the existing CDBA realizations by taking the advantage of FGMOS whose threshold can be lowered and hence minimum needed supply voltage can also be lowered.

5.1.1 Low Voltage CDBA circuit [37]

The complete structure of low voltage CDBA [37] is shown in Figure 34, which comprises a current differencing unit (M1 – M8) and voltage follower unit (M9 – M14). This low voltage CDBA is supplied by $\pm$0.6V voltages. The values of bias currents are 56uA and 84uA respectively for I_{B1} and I_{B2}. To obtain very low resistances at terminal p and terminal n, the current subtractor is realized using flipped voltage follower current sources (FVFCS). The circuit for general FVFCS is shown in Figure 35.

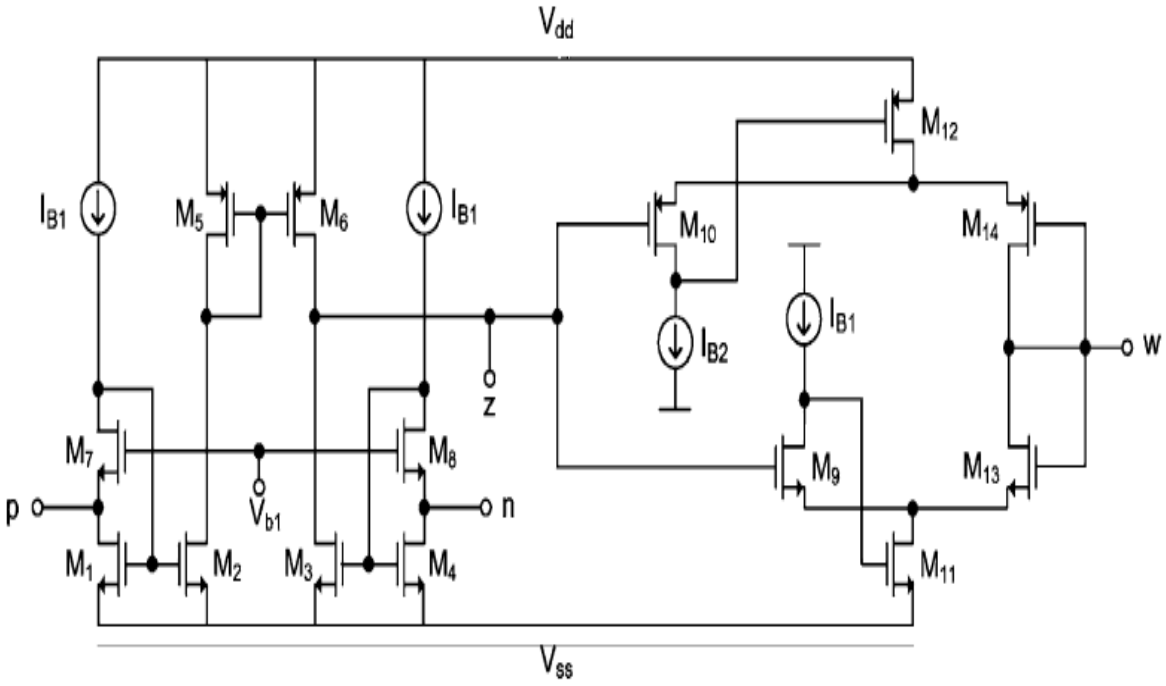


Figure 34: Low voltage CDBA [37].

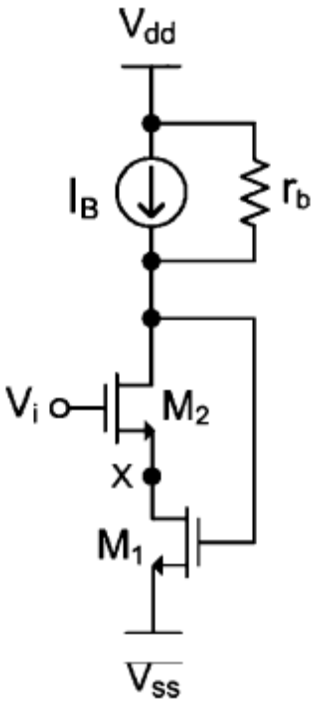


Figure 35: Flipped voltage follower current source.

The mathematical calculation of the input resistance of the FVFCS when seen from the node X gives the following equation

$$R_X = \frac{\frac{1}{g_{m2}}\left(1+\frac{r_b}{r_{02}}\right)//r_{01}}{g_{m1}\,(r_b//\ g_{m2}\,r_{01}r_{02})} \tag{36}$$

Where r_b stands for the output resistance of current source, r_0 stands for the output resistance of transistor and g_m stands for the transconductance of transistor. Generally current source is implemented using MOSFET so for a normal current source $r_b = r_0$ holds true, which reduces equation (36) to-

$$R_X = \frac{2}{g_{m1}\,g_{m2}\,r_{02}} \tag{37}$$

The current subtractor unit of CDBA of Figure 34 is shown independently in Figure 36 for the sake of understanding of its working. In Figure 36, z terminal is named as output terminal as it the difference between p and n is followed at this terminal. The current of z terminal is expressed as follow-

$$i_z = I_{B1} + i_p - (I_{B1} + i_n) = i_p - i_n \tag{38}$$

If transistors M1-M4, M5-M6 and M7-M8 are perfectly matched and all transistors operate into saturation region, then the circuit of Figure 36 works as follow-

The bias current source I_{B1} forces equal current in all the transistors of group M1-M4 causing the gate to source voltage of each transistor to be equal which causes the voltages of the input terminals to be equal. Terminal z is define as output current terminal which means ideally it should have infinite impedance, but practically the impedance looking from the terminal z in figure 36 is given by-

$$R_Z = r_{03}//\,r_{06} \tag{39}$$

The linearity of CDBA of Figure 34 is very high for the entire dynamic range and also has very low offset current at terminal-z.

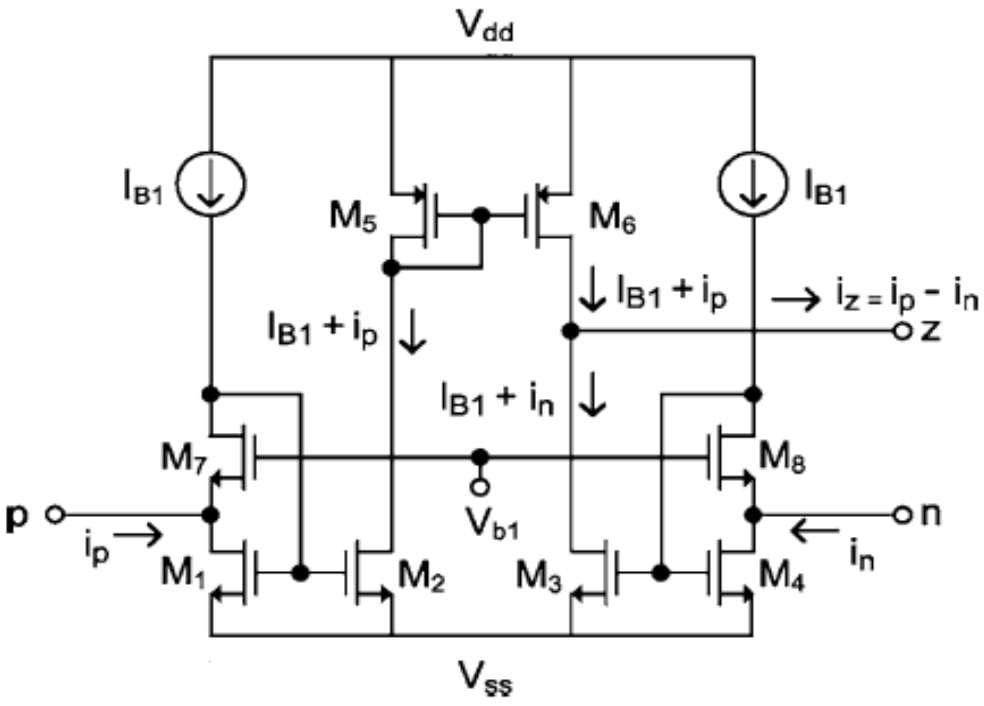


Figure 36: Current subtractor unit of CDBA of Figure 27.

The output stage of the CDBA of Figure 34 is realized using "Differential flipped voltage follower (DFVF)". This DFVF is shown in Figure 37.

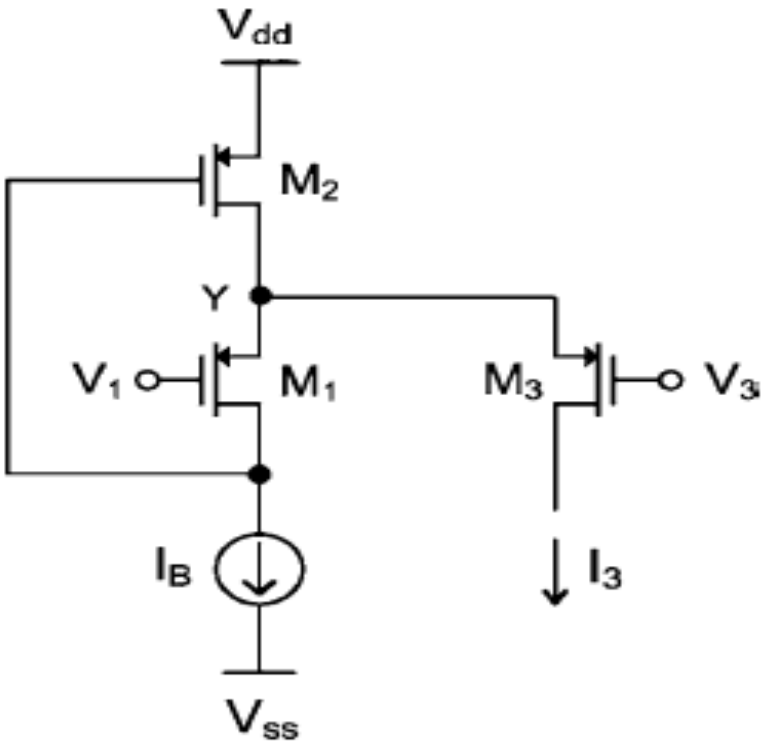


Figure 37: Differential flipped voltage follower

In Figure 37, the voltage of node Y remains constant for large current through transistor M3 with very low impedance. Considering quiescent conditions i.e. $V_1 = V_3$ and assuming the transistor sizes of M1 and M3 to be the same, the condition on Y node is obtained. In transistor M3 current variations are generated by $V_1 - V_3$ differential voltage. These current variations follow the standard MOSFET square law. Additionally, DFVF can be operated at low voltages as minimum voltage supply needed is given by-

$$V_{DD(min)} = V_{Tp} + 2V_{Dsat} \quad (40)$$

A close observation shows that DFVF of Figure 37 is nothing but a class AB voltage buffer in which two complementary DFVF are used. M9 and M11, M10 and M12 are those complementary DFVF whose biasing currents are I_{B2} and I_{B1} respectively.

5.1.2 Proposed FGMOS based CDBA Circuit

It is well known now that the threshold voltage of FGMOS can be lowered or removed which helps in reducing the voltage supply needed. Taking the advantage of this property all the transistor of Figure 34 are replaced with FGMOS counterparts which makes it possible to reduce supply voltage requirement from $\pm$0.6V to $\pm$0.4V. This CDBA is shown in Figure 38. The aspect ratios of all the transistors of Figure 38 are tabulated in table 2.

Transistor	W/L (µm / µm)
M1-M4	3.6/1.80
M5-M8	180/1.80
M9	45/0.36
M10, M12, M14	240/0.36
M11, M13	72/0.36

Table 2: Aspect ratios of transistors of Figure 38.

From equation (10) and (11), it can be noted that the transconductance and output impedance of an FGMOS is lower as compare to conventional MOSFET. So the equations (36), (37) and (39) get modified to (41), (42) and (43), respectively in context of FGMOS.

$$R_X = \frac{\frac{1}{g_{m2,eff}}\left(1+\frac{r_b}{r_{02,eff}}\right)//r_{01.eff}}{g_{m1,eff}\left(r_b// \; g_{m2,eff}\, r_{01,eff} r_{02,eff}\right)} \quad (41)$$

$$R_X = \frac{2}{g_{m1,eff}\, g_{m2,eff}\, r_{02,eff}} \tag{42}$$

$$R_Z = r_{03,eff} // r_{06,eff} \tag{43}$$

From equation (42) it can be observed that the low supply voltage comes at the cost of increased terminal resistance p and n and decreased resistance on terminal z. Also the value of floating gate capacitance is much more than the value of capacitances related to drain and source of conventional MOSFET so although the DC current gains and voltage gains remain almost unaffected by the floating gate capacitances, AC current and voltage gains are depended on value of floating gate capacitances. For the larger value of floating gate capacitances gain becomes very much close to the unity but at the expense of bandwidth. Functional simulation results also verify this theoretical concept.

Figure 39 shows the DC current transfer characteristic. Figure 40 shows frequency variations of p or n terminal impedance magnitude. Figure 41 shows frequency response of current transfer ratio. Figure 42 shows DC voltage transfer characteristic. Figure 43 shows frequency variations of terminal-w impedance magnitude. Figure 45 shows frequency response of voltage transfer ratio. All the plots are obtained using 0.18 um parameter file (appendix). The supply voltages used are ±0.4V.

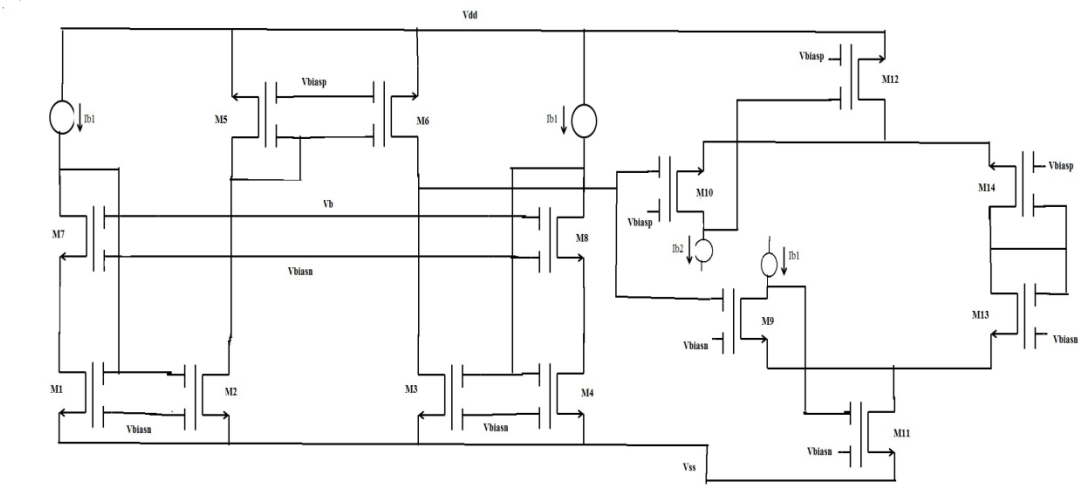


Figure 38: The proposed very low voltage CDBA using FGMOS.

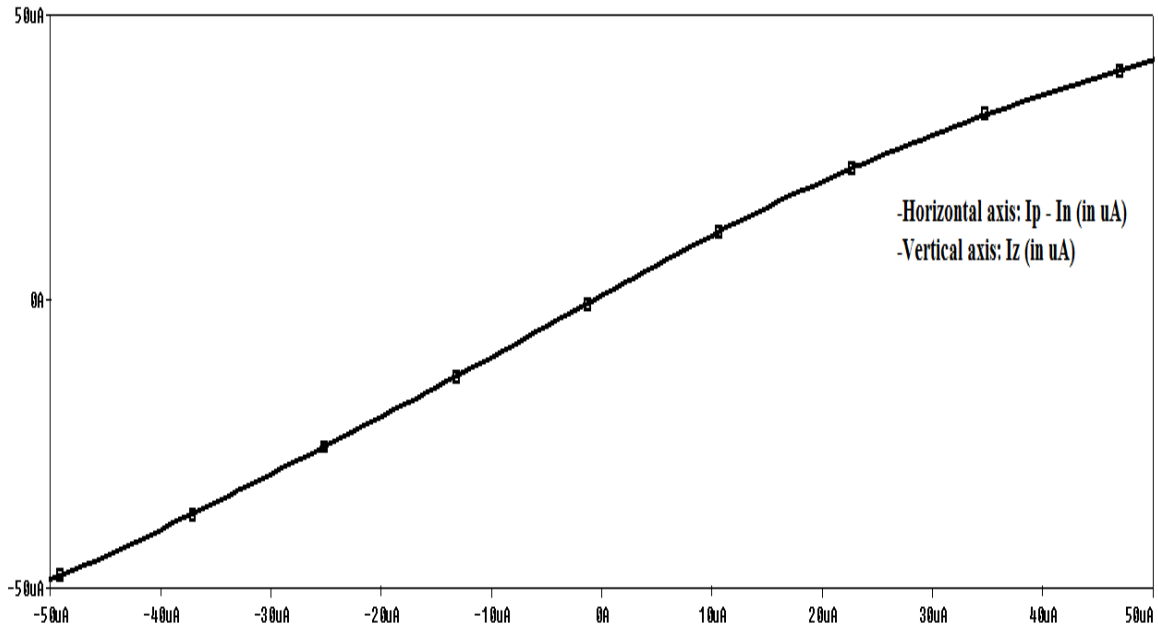
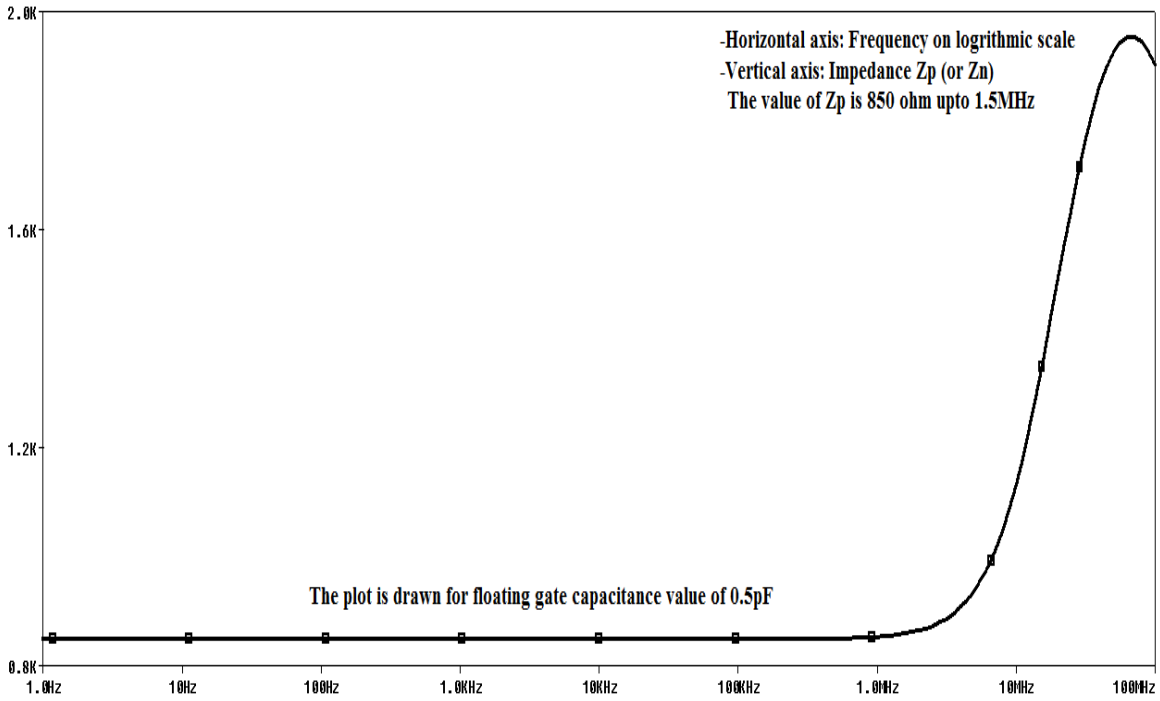
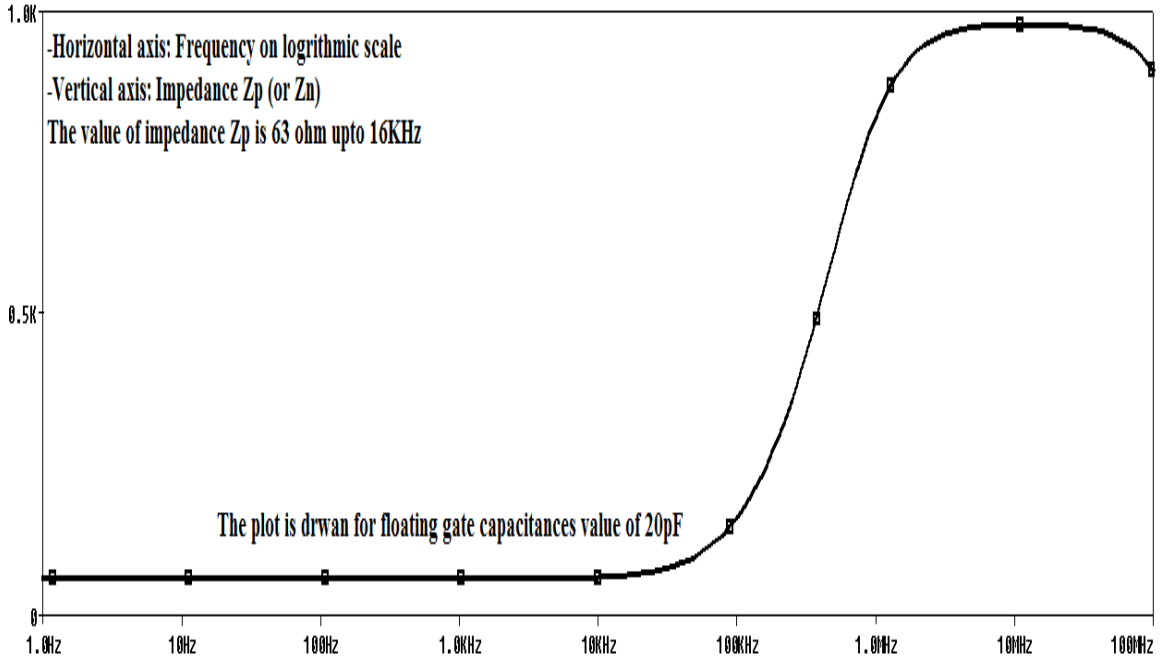


Figure 39: DC current transfer characteristic of proposed CDBA

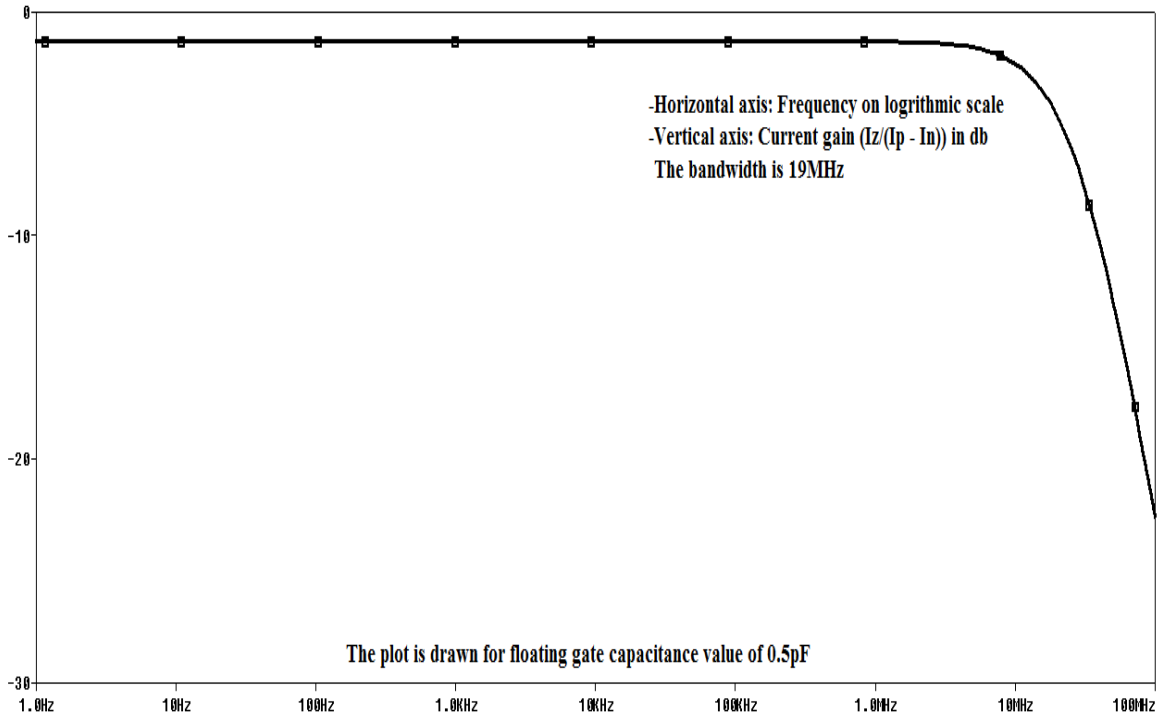


(a)

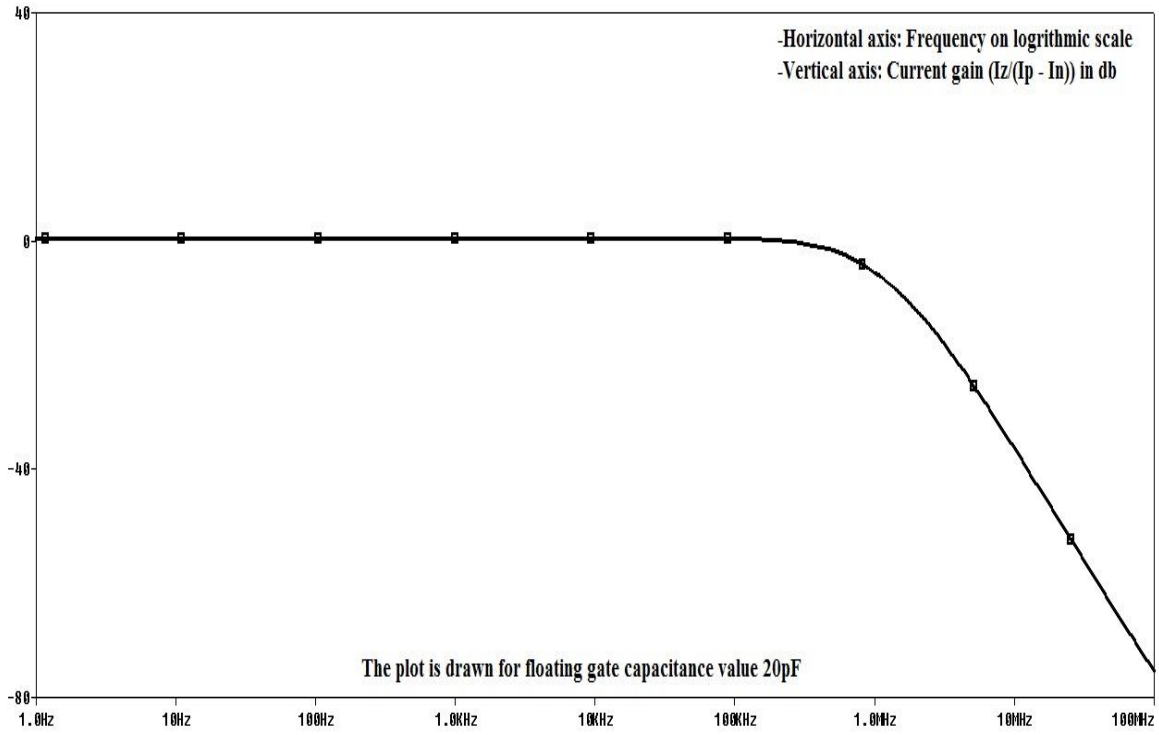


(b)

Figure 40: Frequency variations of input impedance magnitude of proposed CDBA with floating gate capacitance (a): 0.5pF (b): 20pF



(a)



(b)

Figure 41: Frequency response of the current transfer ratio of proposed CDBA with floating gate capacitance (a): 0.5pF (b): 20pF

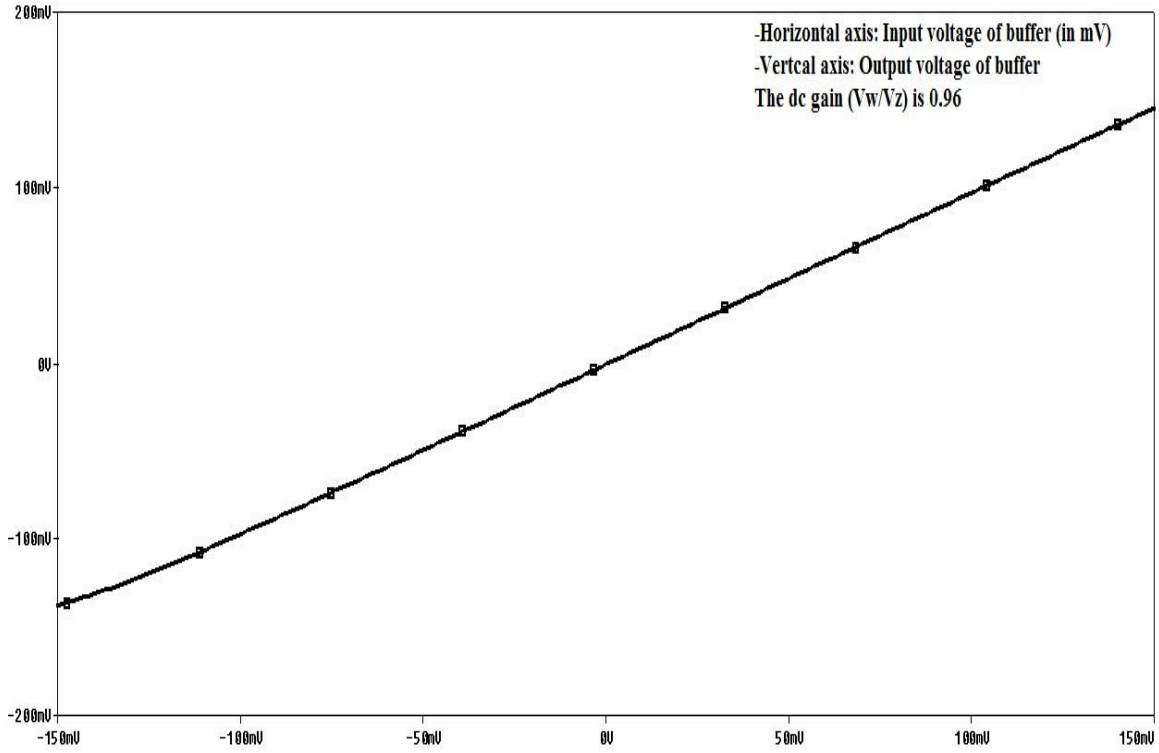
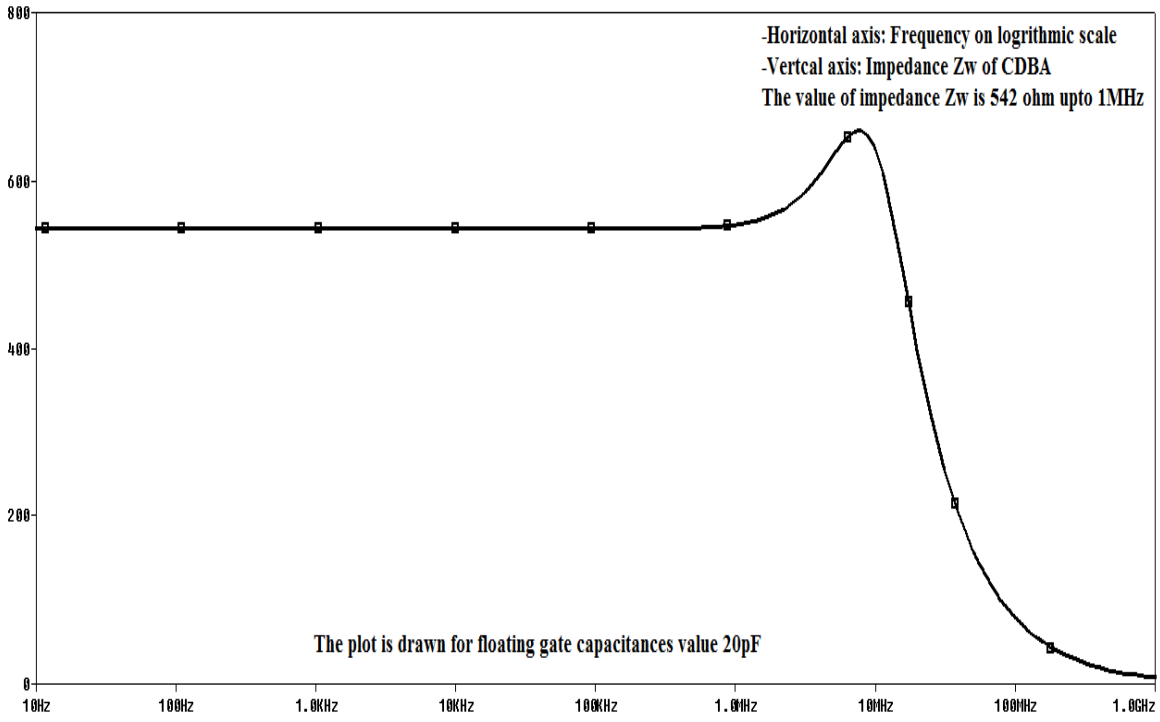
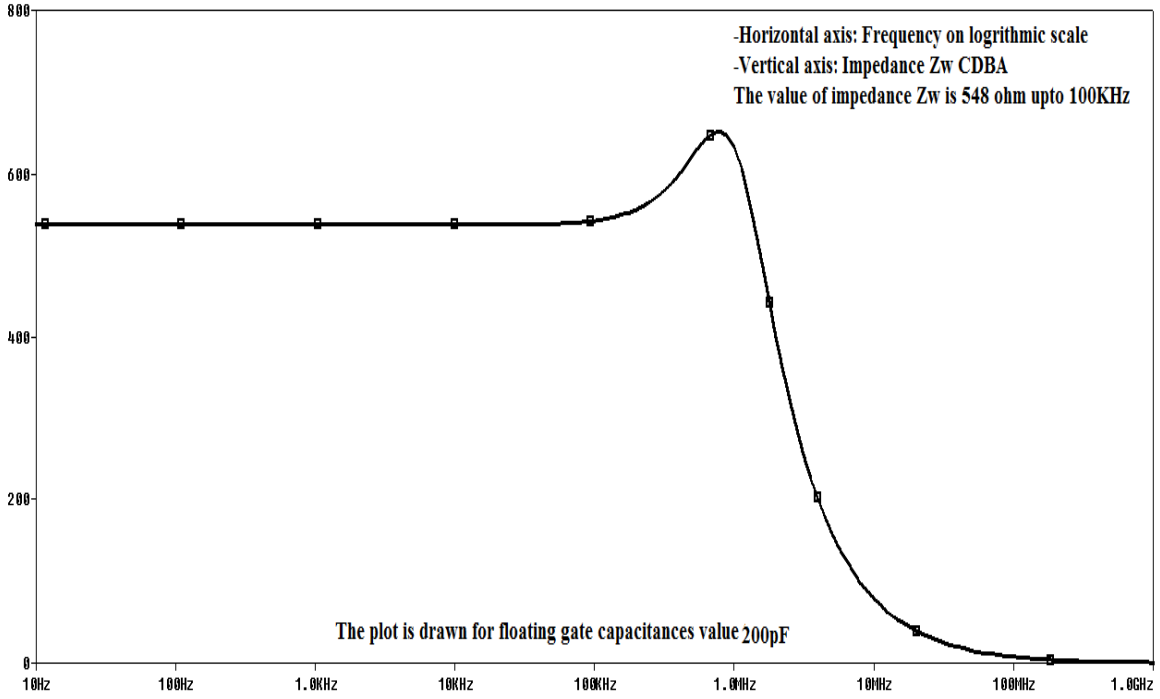


Figure 42: DC voltage transfer characteristic of proposed CDBA

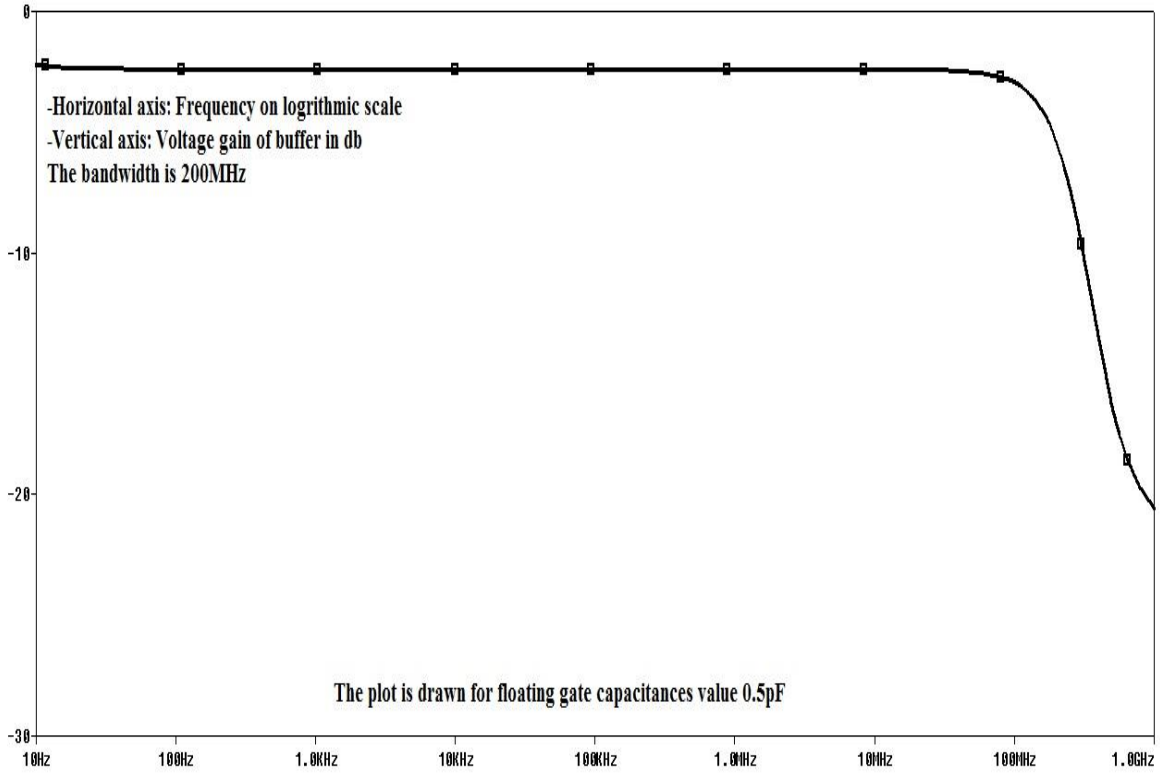


(a)

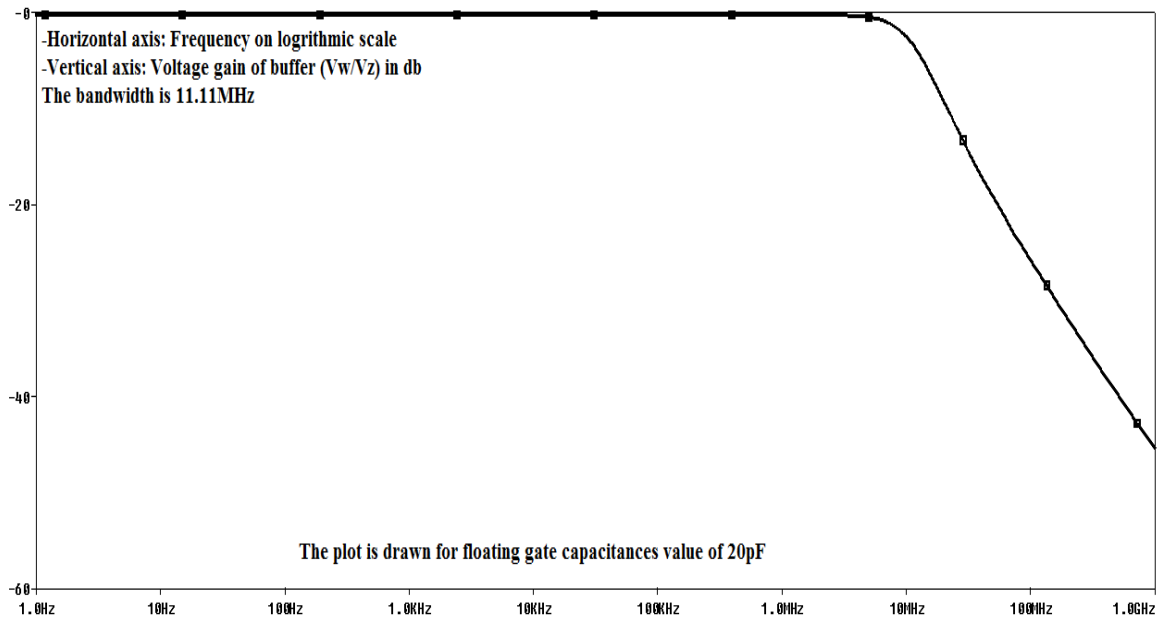


(b)

Figure 43: Frequency variations of terminal-w impedance magnitude of proposed CDBA with floating gate capacitance (a): 20pF (b): 200pF



(a)



(b)

Figure 44: Frequency response of voltage transfer ratio of proposed CDBA with floating gate capacitance (a): 0.5pF (b): 20pF

In this section a FGMOS CDBA is proposed which works for supply voltage of ±0.4V as compare to ±0.6V of [37]. The power dissipation in proposed CDBA is 374 µW as compare to 565.25 µW of [37]. The value of p (n) terminal resistance is 63 Ω as that of 56.4Ω of [37]. The current transfer ratio is 0.98 which is comparable to that of [37]. The current transfer bandwidth is 1.2MHz which is quite low compare to 25MHz of [37] but this decrease in bandwidth happens due to the floating gate capacitances of FGMOS. The voltage transfer ratio is 0.98 which is comparable to 0.978 of [37]. The voltage transfer bandwidth is 11.11 MHz which is again quite low as compare to 474 MHz of [37] and the reason behind the decrease in bandwidth is attributed to floating gate capacitances of FGMOS. The w terminal resistance is 542 Ω which is higher than [37] but this high resistance at w terminal and low bandwidth are compensated by low power consumption and low voltage without any loss in gain of the current difference unit and voltage buffer unit. So it can be concluded that the proposed FGMOS based CDBA fulfills its promise of low power and low voltage operation.

5.1.3 A high pass filter based on the proposed CDBA structure

A second order high pass filter is designed based on the proposed FGMOS based CDBA. The circuit for this filter is shown in Figure 38.

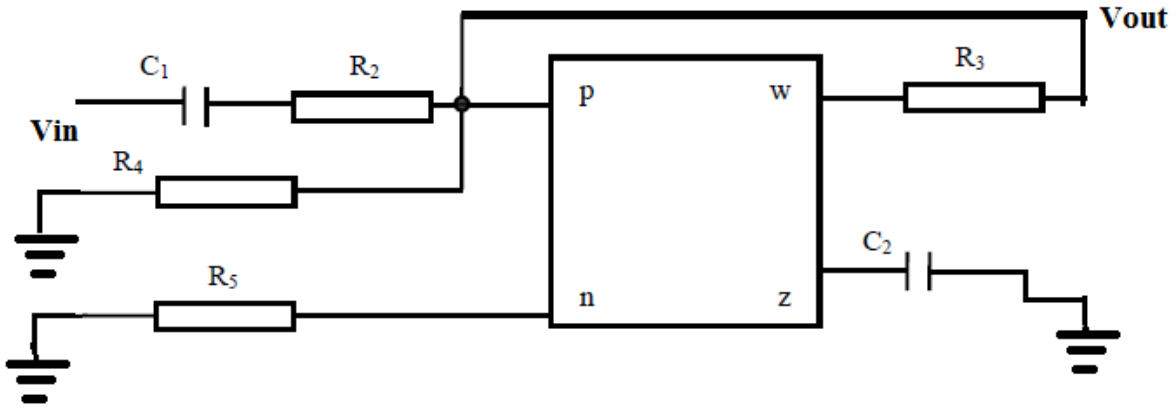


Figure 45: High pass filter using proposed FGMOS based CDBA.

Now in figure 38, applying the terminal voltage equations-

$$V_{out} = \frac{V_{in}s^2}{s^2+\frac{s}{C_1}\left(\frac{1}{R_3}+\frac{1}{R_4}+\frac{1}{R_5}\right)+\frac{1}{R_2 R_3 C_1 C_6}} \quad (44)$$

Here the cut off frequency comes as-

$$\omega_0 = \sqrt{\frac{1}{R_2\, R_3\, C_1\, C_6}} \tag{45}$$

With the values of components as $R_2 = R_3 = R_4 = R_5 = 1k\Omega$ and $C_1 = C_6 = 1nF$, theoretically cut off frequency is 159 KHz but due to the floating gate capacitance simulation shows this frequency is 120 KHz which is not a huge margin of error considering the reduction in voltage supply and power consumption.

The frequency response for this high pass filter is shown in Figure 39.

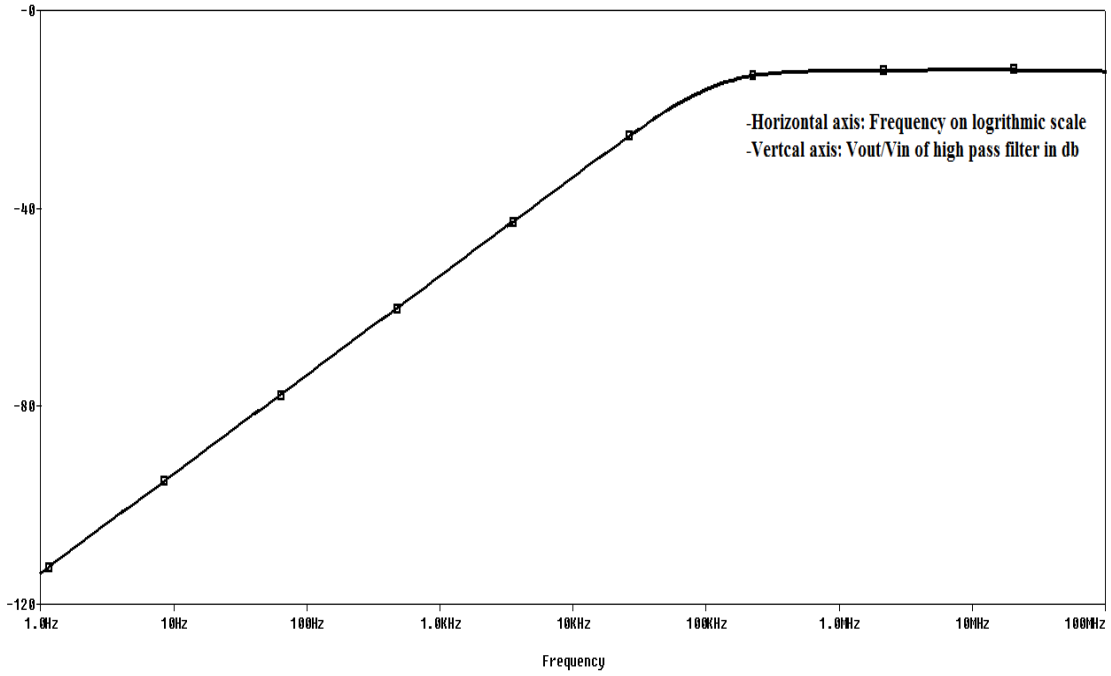


Figure 46: Frequency response of high pass filter of Figure 38.

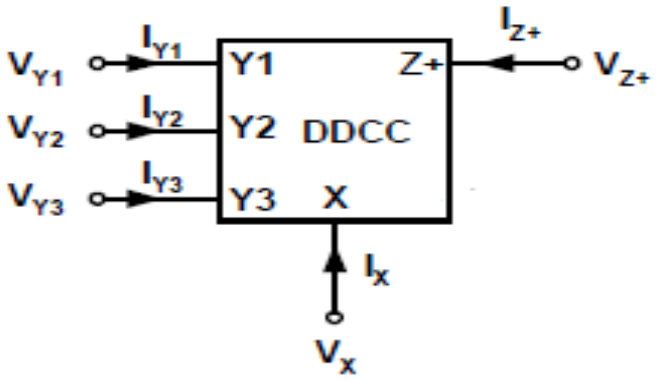
5.2 Differential Difference Current Conveyor (DDCC)

Another very popular current mode active building block is second generation current conveyor (CCII), which was proposed in 1970 [38]. Many applications of CCII are found in literature such as filters, oscillators etc. Differential difference amplifier (DDA) has been proposed recently [39]. The advantages of DDA are high input impedance and arithmetic operation capability. Also, applications of DDA, which are found in literature [39-41], indicates that the component count can be reduced using the DDA. These features make DDA a better choice for analog signal processing applications.

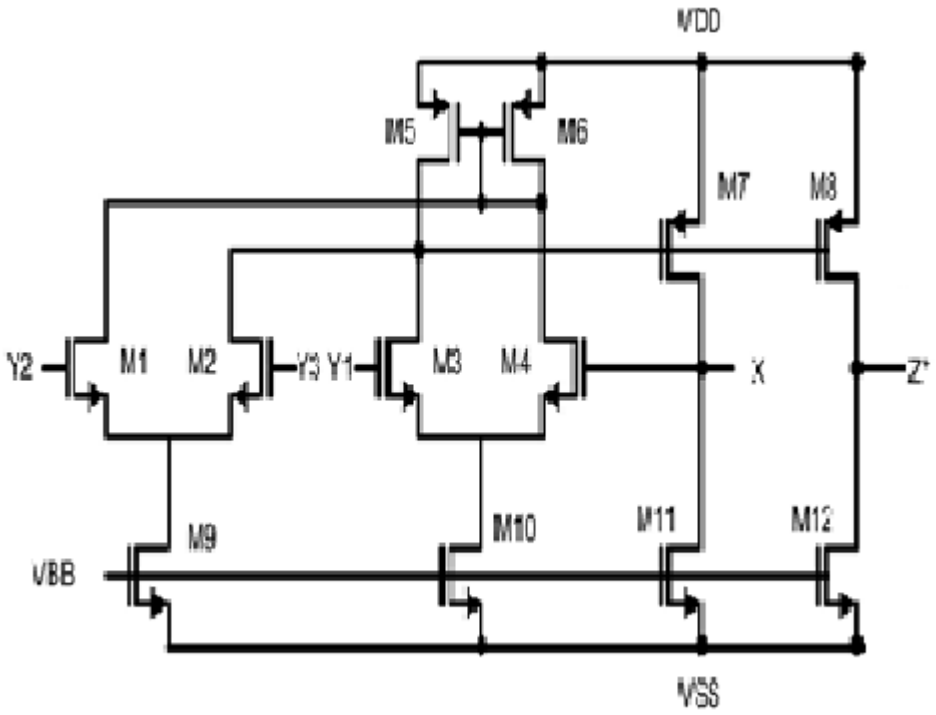
Yet another building block which is a hybrid of DDA and CCII is differential difference current conveyor (DDCC), which has advantages of both fore-mentioned building blocks.

5.2.1 Description of DDCC

The symbol and circuit of DDCC are shown in Figure 40. The terminal relationships of DDCC are given in equation 46. The input transconductance stage comprises two differential units (M1-M2) and (M3-M4), whereas high gain stage is composed of current mirror M5-M6. Differential current is converted into a single ended output current at M7. The current of M7 is duplicated in M8 by using another current source (M12).



(a)



(b)

Figure 47: DDCC (a): The symbol (b): The circuit

$$I_{Y1} = I_{Y2} = I_{Y3} = 0 \quad (46\text{-a})$$

$$V_X = V_{Y1} - V_{Y2} - V_{Y3} \quad (46\text{-b})$$

$$I_z = \pm I_X \quad (46\text{-c})$$

From the working of DDCC the output voltage can be expressed as-

$$V_X = A_0\,[(V_{Y1} - V_{Y2}) + (V_{G3} - V_{Y3})] \quad (47)$$

Solving the equation (47) the following relation is obtained

$$V_X = \frac{A_0}{A_0 + 1}\,(V_{Y1} - V_{Y2} + V_{Y3}) \quad (48)$$

It is known that $A_0 >> 1$, which reduces equation (48) to the following relation-

$$V_X = (V_{Y1} - V_{Y2} + V_{Y3}) \quad (49)$$

5.2.2 Proposed FGMOS based DDCC

The DDCC of [42] uses ±2.5V voltage supply. In this work a new structure of DDCC is proposed where the input differential unit is realized using FGMOS transistors instead of conventional MOSFETs. This facilitates almost same dynamic range of operation as that of DDCC of [42] but with supply voltages ±2V. A full wave rectifier is also designed with this new DDCC. The circuit of proposed DDCC and its characteristics are shown in Figure 41 and Figure 42 respectively. The aspect ratios of all the transistors are tabulated in table 3.

Transistors	W/L (µm/µm)
M1-M4	1.6/1
M5, M6	8/1
M7, M8	20/1
M9 M10	29/1
M11, M12	90/1

Table 3: Aspect ratio of transistors of Figure 41.

All the characteristics are plotted using 0.5 um parameter file (see appendix).

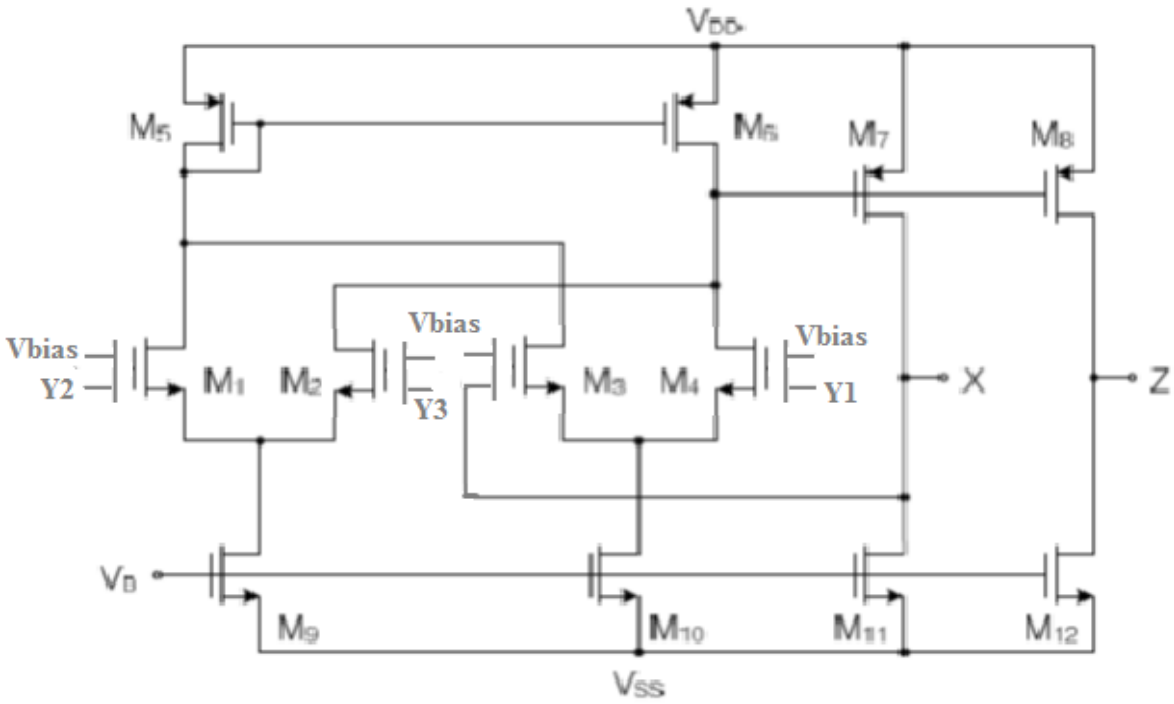
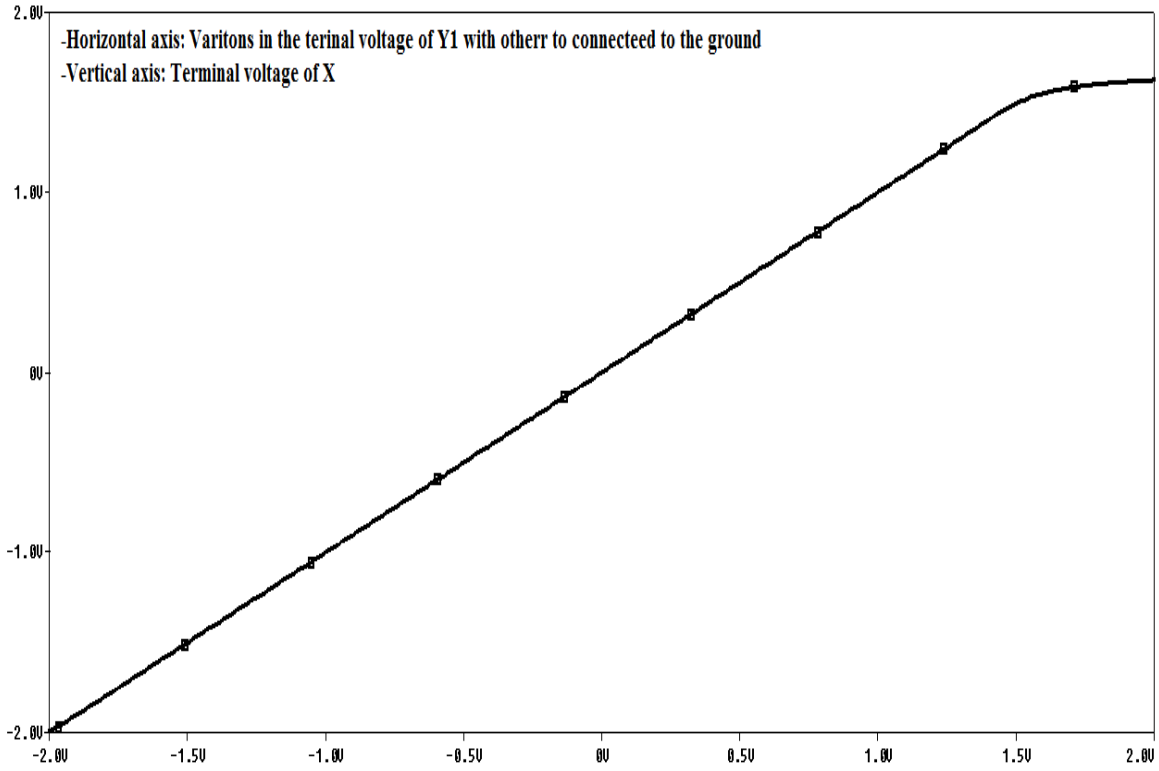
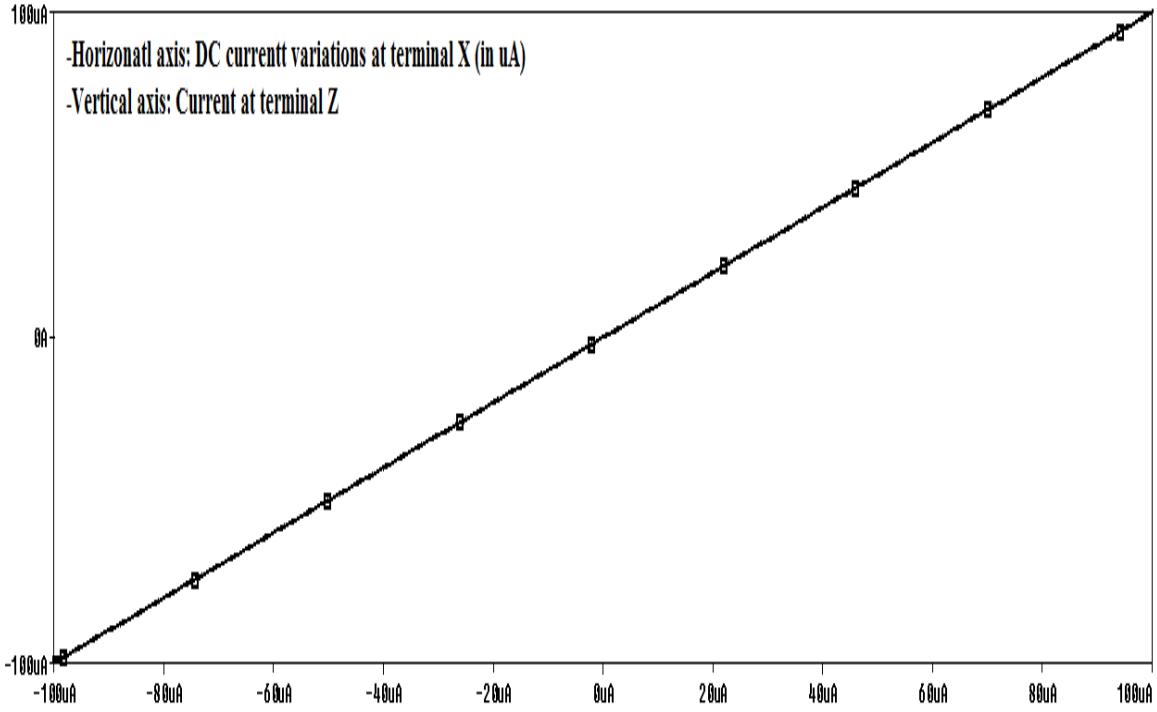


Figure 48: Circuit diagram of proposed DDCC



(a)



(b)

Figure 49: DC characteristics of proposed DDCC (a): Voltage characteristics (b): Current characteristics

In this section FGMOS based DDCC is proposed and its DC characteristics both voltage and currents are plotted. It is found that it works almost for the same dynamic range of operation for which DDCC of [42] works but with low supply voltage. In the propose DDCC supply voltage required is ±2V as compare to ±2.5V of [42]. So it can be concluded that the proposed DDCC provides low voltage operation without any loss in performance as it promises. To prove the worth of the proposed FGMOS based DDCC a full wave rectifier is implemented using this DDCC.

5.2.3 Full Wave Rectifier using proposed FGMOS based DDCC

In this section to justify the usefulness of the FGMOS based DDCC, a full wave rectifier is implemented [42]. The circuit for this purpose is shown in Figure 50 where two DDCCs are used to perform full rectification of the input. Like in full wave rectifiers based on diodes, where for positive cycle of the input one diode is ON and other is OFF and for negative cycle of the input ON and OFF states of diodes are interchanged, in this

full wave rectifier also, one DDCC is on for positive cycle of the input and other DDCC is on for the negative cycle of the input.

If $V_{in} > 0$, then DDCC1 is ON and DDCC2 is OFF.

If $V_{in} < 0$, then DDCC1 is OFF and DDCC2 is ON.

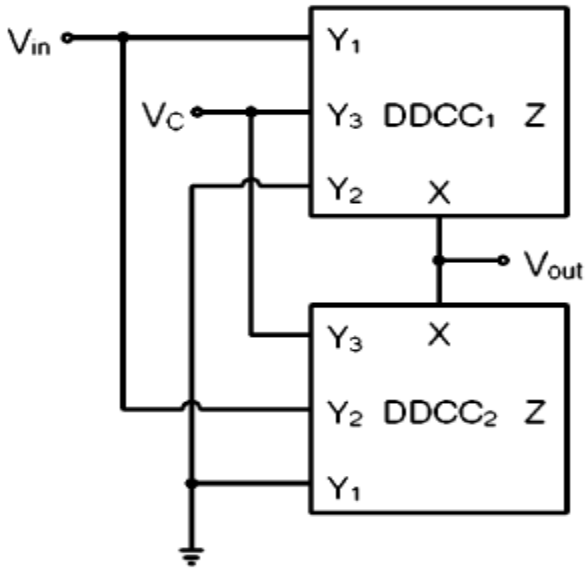
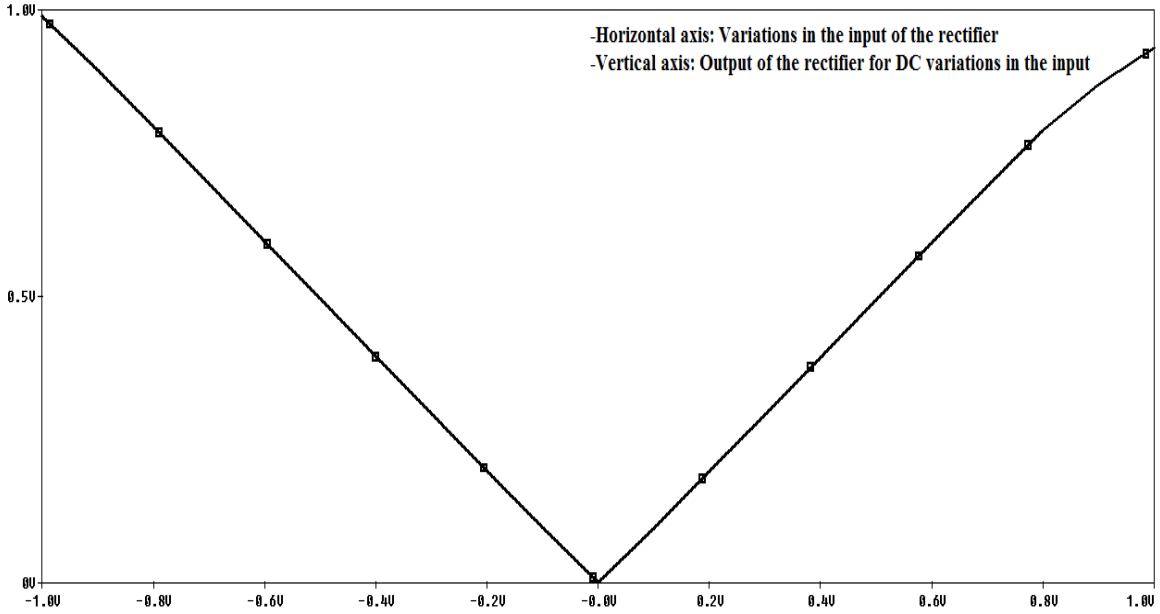
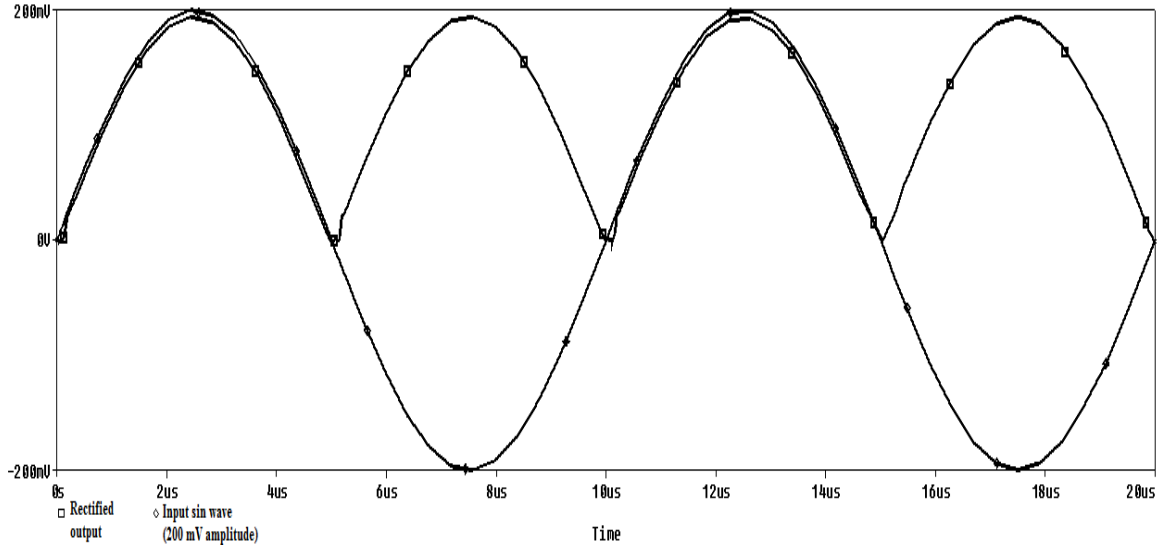


Figure 50: Full wave rectifier using DDCC

Both DC and transient characteristics are verified for the full wave rectifier of Figure 50. It is found that the dynamic range of operation of this rectifier is -1V to 1V which is similar to that of rectifier of [42] in spite of using ±2V power supplies. The transient characteristic is also obtained by applying a sin wave of 200 mV amplitude having frequency of 500 KHz and the output of the rectifier shows almost full rectification. The DC characteristic of rectifier is shown in Figure 51(a) and transient response is shown in Figure 51(b). The simulated output is in close agreement to the theoretical result.



(a)



(b)

Figure 51: (a): DC characteristic of full wave rectifier using proposed DDCC (b) Response of full wave rectifier to a sin input.

5.3 Conclusion

In this chapter the limitations of voltage mode circuits are explained and then it is discussed how current mode circuits are more suitable choice for low power operations and more close to transistor level integration. Then active blocks which have been reported in the literature using current mode are listed.

Out of the numerous current mode active blocks available, two blocks namely CDBA and DDCC are realized using FGMOS transistors to minimize the power consumption. An introduction of CDBA is given followed by description and working of a conventional CDBA block. Then a detailed analysis of low power CDBA [37] is done as this low power CDBA lays ground for the proposed FGMOS CDBA. This is followed by design and characterization of FGMOS based CDBA. The proposed design works for a lower voltage and has less power consumption as compare to the conventional structure [37]. Finally a second order high pass filter was implemented using the proposed CDBA which justifies its practicality.

In the last section, an FGMOS based DDCC is proposed. First a basic DDCC is introduced and its terminal relationships are illustrated with its working and it is explained a DDCC is a hybrid of DDA and CC. Lastly an FGMOS based DDCC is proposed and simulated. It is observed that proposed DDCC has almost same dynamic range of operation as that of [42] and it works on lower supply voltage than that of [42]. In the end a full wave rectifier application of proposed DDCC is implemented and its output is obtained by applying a sin wave input. It is found this rectifier gives almost full rectification. Its dynamic range is also found to be similar to that of rectifier of [42].

6. CONCLUSION AND FUTURE SCOPE

In last one or two decades, voltage supply has become one of the important parameters and various methods and techniques have been introduced to make supply voltage lower. In this work three such techniques, namely, sub-threshold operation of MOSFETs, bulk driven MOSFETs and floating gate MOSFETs are discussed. It is also explained that sub threshold operation of MOSFET has its drain current very much sensitive to temperature and bulk driven MOSFET has current leakage problem. Thereby, they may provide low voltage operation but do suffer from certain undesired phenomena. These limitations of sub threshold MOSFET and bulk driven MOSFET serve as the backdrop for floating gate MOSFETs.

The physical structure of FGMOS is found to be almost similar to conventional MOSFET and hence compatible with current CMOS fabrication processes. The difference is the additional control gates of FGMOS which provide facility of threshold adjustment. It is also discussed FGMOS can have multiple control gates such FGMOS are called multiple inputs FGMOS (MIFGMOS). The equivalent circuit of FGMOS is illustrated.

To simulate FGMOS based circuits in SPICE, it has to be modeled using conventional MOSFET in SPICE environment. The SPICE models with and without floating gate charge are explained. Using SPICE model of FGMOS without any net charge on floating gate, the threshold voltage variation property of FGMOS is illustrated. It is observed that the threshold of FGMOS can be lowered considerably by varying the bias gate voltage of FGMOS. For AC analysis a small signal model is illustrated and it is observed that transconductance of FGMOS is lower than normal MOSFET and output impedance is also lower as compare to conventional MOSFET. The similarity between the characteristics of FGMOS and MOSFET is not limited to strong inversion region of operation but in sub threshold region of operation also there exist similarity and which has been explained with drain current equation.

After this the literature survey showed that many transistor level applications: linear MOSFET based on FGMOS, grounded resistor using FGMOS, voltage divider using FGMOS exist in literature. In this work, some of these applications are discussed in detail. The applications of FGMOS are found in basic analog cells also. Wilson current mirror, Gilbert's cell are also reported in literature using FGMOS. Most importantly, there are active analog building blocks which use FGMOS to achieve low

power operations. Here op-amp and OTAs using FGMOS are illustrated and some applications of multiple input OTA using FGMOS is discussed.

As the work aims at low power operations, advantages of current mode circuits over conventional voltage mode circuits are described. Few of these advantages are higher speed, low voltage supply and large bandwidth. Some active building blocks which use current mode for their operation are mentioned. Out of these active blocks, in this work, "Current differencing buffered amplifier (CDBA)" and "Differential difference current conveyor (DDCC)" are described in detail as in this work new structures of CDBA and DDCC using FGMOS are proposed.

The CDBA with its working and terminal relationship is discussed and a particular realization, low power CDBA [37] is illustrated in detail as this is the motivation behind the proposed FGMOS CDBA. Then FGMOS CDBA is proposed and its DC current and voltage transfer characteristics, AC current and voltage transfer characteristics and its terminal impedance magnitude characteristics are obtained using PSPICE. It is found that the current transfer ratio of the proposed FGMOS based CDBA is 0.98 with bandwidth 1.2 MHz and voltage transfer ratio is found to be 0.98 with bandwidth of 11.11 MHz This is achieved using ±0.4V supply and power dissipation of 374 μW. the p (n) terminal resistance is 63 Ω. And w-terminal resistance is 542 Ω. Although, the bandwidth is compromised but at the same time low power operation is also achieved that too without losing current transfer ratio and voltage transfer ratio. The feasibility of proposed FGMOS based CDBA is proved by implementing a second order high pass filter using this CDBA.

Continuing in the tradition of low power operation of this work, a new structure of DDCC using FGMOS is proposed. First basic DDCC and its working is explained and then FGMOS DDCC is explained. Its DC voltage and current characteristics are plotted and verified using PSPICE. It is found that proposed DDCC works for ±2V supply voltage without losing its dynamic range of operation. In this DDCC the differential unit is realized using FGMOS transistors. To justify the worth of the proposed DDCC a full wave rectifier is implemented and its DC and transient characteristics are also obtained. It is found that this full wave rectifier has dynamic range of -1V to 1V and transient response is obtained by applying 200 mV sin wave having 500 KHz frequency, the output voltage is rectified almost to the full swing of the input sin wave.

It has been discussed in section 5.2 that the bandwidth of proposed CDBA circuits are lower compare to bandwidths of existing works due to the floating gate capacitance effect. So a scope of improvement is there to increase bandwidth of FGMOS based designs. It may be obtained through some frequency compensation techniques or by reducing the effect of floating gate capacitances. This area of research is vast and open. If it is possible to increase bandwidth of FGMOS based designs it will surely be one of the promising technique to achieve low power operations.

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APPENDIX

- **Model parameters of 0.5 µm technology file**

NMOS

{

+ LEVEL=3 UO=460.5 TOX=1E-8 TPG=1 VTO=.62 JS=1.8E-6 XJ=.15E-6
+ RS=417 RSH=2.73 LD=4E-8 ETA=0 VMAX=130E3 NSUB=1.71E17 +PB=
.761 PHI= .905 THETA= .129 GAMMA= .69 KAPPA=0.1 AF=1
+WD=1.1E-7 CJ=76.4E-5 MJ=.357 CJSW=5.68E-10 MJSW=.302 CGSO=1.38E-
10 CGDO=1.38E-10 CGBO=3.45E-10 KF=3.07E-28 DELTA=0.42 NFS=1.2E11

}

PMOS

{

+ LEVEL=3 UO=100 TOX=1E-8 TPG=1 VTO=-.58 JS=.38E-6 XJ=.1E-6
+RS=886 RSH=1.81 LD=3E-8 ETA=0 VMAX=113E3 NSUB=2.08E17
+PB=.911 PHI=.905 THETA=.12 GAMMA=.76 KAPPA=2 AF=1
+WD=1.4E-7 CJ=85E-5 MJ=.429 CJSW=4.67E-10 MJSW=.631
+CGSO=1.38E-10 CGDO=1.38E-10 CGBO=3.45E-10 KF=1.08E-29
+DELTA=0.81 NFS=.52E11

}

- **Model parameter of 0.25 µm technology file**

NMOS

{

+LEVEL = 3

+ TOX = 5.7E-9 NSUB = 1E17 GAMMA = 0.4317311

+ PHI = 0.7 VTO = 0.4238252 DELTA = 0

+ UO = 425.6466519 ETA = 0 THETA = 0.1754054

+ KP= 2.501048E-4 VMAX= 8.287851E4 KAPPA= 0.1686779

+ RSH = 4.062439E-3 NFS = 1E12 TPG = 1

+ XJ= 3E-7 LD = 3.162278E-11 WD = 1.232881E-8

+ CGDO = 6.2E-10 CGSO = 6.2E-10 CGBO = 1E-10

+ CJ = 1.81211E-3 PB = 0.5 MJ = 0.3282553

+ CJSW = 5.341337E-10 MJSW = 0.5

}

PMOS

{

+LEVEL = 3

+ TOX=5.7E-9 NSUB = 1E17 GAMMA = 0.6348369

+ PHI = 0.7 VTO = -0.5536085 DELTA = 0

+ UO = 250 ETA = 0 THETA = 0.1573195

+ KP=5.194153E-5 VMAX=2.295325E5 KAPPA = 0.7448494

+ RSH = 30.0776952 NFS = 1E12 TPG = -1

+ XJ= 2E-7 LD = 9.968346E-13 WD = 5.475113E-9

+ CGDO= 6.66E-10 CGSO = 6.66E-10 CGBO = 1E-10

+ CJ 1.893569E-3 PB = 0.9906013 MJ = 0.4664287

+ CJSW = 3.625544E-10 MJSW = 0.5

}

- **Model parameters of TSMC 0.18 µm technology file**

NMOS

{

+LEVEL = 7

+VERSION = 3.1 TNOM = 27 TOX = 4.1E-9

+XJ = 1E-7 NCH = 2.3549E17 VTH0 = 0.354505

+K1 = 0.5733393 K2 = 3.177172E-3 K3 = 27.3563303

+K3B = -10 W0 = 2.341477E-5 NLX = 1.906617E-7

+DVT0W = 0 DVT1W = 0 DVT2W = 0

+DVT0 = 1.6751718 DVT1 = 0.4282625 DVT2 = 0.036004

+U0 = 327.3736992 UA = -4.52726E-11 UB = 4.46532E-19

+UC = -4.74051E-11 VSAT = 8.785346E4 A0 = 1.6897405

+AGS = 0.2908676 B0 = -8.224961E-9 B1 = -1E-7

+KETA = 0.021238 A1 = 8.00349E-4 A2 = 1

+RDSW = 105 PRWG = 0.5 PRWB = -0.2

+WR = 1 WINT = 0 LINT = 1.351737E-8

***+XL = -2E-8 XW = -1E-8**

+ DWG = 1.610448E-9

+DWB = -5.108595E-9 VOFF = -0.0652968 NFACTOR = 2.4901845

+CIT = 0 CDSC = 2.4E-4 CDSCD = 0

+CDSCB = 0 ETA0 = 0.0231564 ETAB = -0.058499

+DSUB = 0.9467118 PCLM = 0.8512348 PDIBLC1 = 0.0929526

+PDIBLC2 = 0.01 PDIBLCB = -0.1 DROUT = 0.5224026

+PSCBE1 = 7.979323E10 PSCBE2 = 1.522921E-9 PVAG = 0.01

+DELTA = 0.01 RSH = 6.8 MOBMOD = 1

+PRT = 0 UTE = -1.5 KT1 = -0.11

+KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9

+UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4

+WL = 0 WLN = 1 WW = 0

+WWN = 1 WWL = 0 LL = 0

+LLN = 1 LW = 0 LWN = 1

+LWL = 0 CAPMOD = 2 XPART = 0.5

+CGDO = 7.7E-10 CGSO = 7.7E-10 CGBO = 1E-12

+CJ = 1.010083E-3 PB = 0.7344298 MJ = 0.3565066

+CJSW = 2.441707E-10 PBSW = 0.8005503 MJSW = 0.1327842

+CJSWG = 3.3E-10 PBSWG = 0.8005503 MJSWG = 0.1327842

+CF = 0 PVTH0 = 1.307195E-3 PRDSW = -5

+PK2 = -1.022757E-3 WKETA = -4.466285E-4 LKETA = -9.715157E-3

+PU0 = 12.2704847 PUA = 4.421816E-11 PUB = 0

+PVSAT = 1.707461E3 PETA0 = 1E-4 PKETA = 2.348777E-3

}

PMOS

{

+LEVEL = 7

+VERSION = 3.1 TNOM = 27 TOX = 4.1E-9

+XJ = 1E-7 NCH = 4.1589E17 VTH0 = -0.4120614

+K1 = 0.5590154 K2 = 0.0353896 K3 = 0

+K3B = 7.3774572 W0 = 1E-6 NLX = 1.103367E-7

+DVT0W = 0 DVT1W = 0 DVT2W = 0

+DVT0 = 0.4301522 DVT1 = 0.2156888 DVT2 = 0.1

+U0 = 128.7704538 UA = 1.908676E-9 UB = 1.686179E-21

+UC = -9.31329E-11 VSAT = 1.658944E5 A0 = 1.6076505

+AGS = 0.3740519 B0 = 1.711294E-6 B1 = 4.946873E-6

+KETA = 0.0210951 A1 = 0.0244939 A2 = 1

+RDSW = 127.0442882 PRWG = 0.5 PRWB = -0.5

+WR = 1 WINT = 5.428484E-10 LINT = 2.468805E-8

***+XL = -2E-8 XW = -1E-8**

+DWG = -2.453074E-8

+DWB = 6.408778E-9 VOFF = -0.0974174 NFACTOR = 1.9740447

+CIT = 0 CDSC = 2.4E-4 CDSCD = 0

+CDSCB = 0 ETA0 = 0.1847491 ETAB = -0.2531172

+DSUB = 1.5 PCLM = 4.8842961 PDIBLC1 = 0.0156227

+PDIBLC2 = 0.1 PDIBLCB = -1E-3 DROUT = 0

+PSCBE1 = 1.733878E9 PSCBE2 = 5.002842E-10 PVAG = 15

+DELTA = 0.01 RSH = 7.7 MOBMOD = 1

+PRT = 0 UTE = -1.5 KT1 = -0.11

+KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9

+UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4

+WL = 0 WLN = 1 WW = 0

+WWN = 1 WWL = 0 LL = 0

+LLN = 1 LW = 0 LWN = 1

+LWL = 0 CAPMOD = 2 XPART = 0.5

+CGDO = 7.11E-10 CGSO = 7.11E-10 CGBO = 1E-12

+CJ = 1.179334E-3 PB = 0.8545261 MJ = 0.4117753

+CJSW = 2.215877E-10 PBSW = 0.6162997 MJSW = 0.2678074

+CJSWG = 4.22E-10 PBSWG = 0.6162997 MJSWG = 0.2678074

+CF = 0 PVTH0 = 2.283319E-3 PRDSW = 5.6431992

+PK2 = 2.813503E-3 WKETA = 2.438158E-3 LKETA = -0.0116078

+PU0 = -2.2514581 PUA = -7.62392E-11 PUB = 4.502298E-24

+PVSAT = -50 PETA0 = 1E-4 PKETA = -1.047892E-4

}