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CERTIFICATE

This is to certify that the dissertation titled "**Implementation of Single Core L1 L2 Cache with the comparison of Read Policies using HDL**" is a bonafide record of work done by **RenuToppo, Roll No. 2K13/VLS/19** at **Delhi Technological University** for partial fulfilment of the requirements for the degree of Master of Technology in VLSI and Embedded System Design. This project was carried out under my supervision and has not been submitted elsewhere, either in part or full, for the award of any other degree or diploma to the best of my knowledge and belief.

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ACKNOWLEDGEMENTS

I would like to express my deep sense of respect and gratitude to my project supervisor **Dr. S. Indu,** Associate Professor, Electronics and Communication Engineering Department, DTU for providing the opportunity of carrying out this project and being the guiding force behind this work. I am deeply indebted to her for the support, advice and encouragement she provided without which the project could not have been a success.

I am also grateful to **Prof. PR Chadda**, HOD, Electronics and Communication Engineering Department, DTU for his immense support.

I am failing if I miss my special thanks to my friend Siddharth Mohta who supported me at every step while facing several kinds of difficulties.

I would also like to acknowledge Delhi Technological University for providing the right academic resources and environment for this work to be carried out.

Last but not the least I would like to express sincere gratitude to my family and college friends for constantly encouraging me during the completion of work.

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ABSTRACT

This thesis focuses on the comparison of three different replacement policies for Cache memory by using hit rate as the performance criteria. Random, LRU and Pseudo-LRU.

It involves the implementation of 2-way, 4-way and 8-way Set Associative mapping technique for varying cache sizes. For the sake of comparison a 4KB ,8KB ,16KB ,32KB, 64KB,cache memory is taken as base on which the policies are executed. The implementation of the memory controller and the required glue logic is carried out. Test bench is written for simulating the input signals to the memory controllers. At the next level, a higher capacity L2 cache memory is considered and the same process is repeated to estimate the performance with respect to Hit Rate. Verilog language is used for the hardware implementation. Memory controllers for the Main Memory, L1 Cache and L2 Cache are realized using Verilog language.

As we double the Way of cache (2-Way to 4-Way & 4-Way to 8-Way) the performance increases in general, but the percentage increase is not same. 2-Way to 4-Way increased by~3.5%, 4-Way to 8-Way increased by ~0.2%. It implies that we won't get equal performance increment on doubling the Way-Size of cache.

To find the optimized Way-Size we have to strike a balance between the Cache-Size and Hit-Rate. In our case optimized Way-Size is 4. Performance increment also depends upon the program in execution. So the optimized Way-Size can be different for different program.

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ABBREVIATIONS

VLSI	Very Large Scale Integration
DRAM	Dynamic Random Access Memory
SRAM	Static Random Access Memory
L1, L2, L3	Level 1,Level 2,Level 3 caches
CPU	Central Processing Unit
LRU	Least Recently Used
P-LRU	Pseudo-Least Recently Used
CAM	Contents Addressable Memory