A

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Implementation of Gilbert cell mixer for RF receiver

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Certificate

This is to certify that the dissertation titled **"Implementation of Gilbert cell Mixer for RF receiver"** is a bonafide record of work done by **Priyanka, Roll No. 2K13/VLS/17** at **Delhi Technological University** for partial fulfilment of the requirements for the degree of Master of Technology in VLSI and Embedded System Design. This project was carried out under my supervision and has not been submitted anywhere else, either in part or full, for the award of any other degree or diploma to the best of my knowledge and belief.

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Abstract

This thesis focuses on the designing and implementation of radio-frequency CMOS down-conversion mixers for wireless applications. The Gilbert cell has been used as the basic configuration for all mixers. The thesis involves the comparison of performance parameters for double balanced down-conversion mixers using various loads. Two techniques, source degeneration and current bleeding for enhancing the linearity of the mixers are implemented and their effects on mixer performance are observed. The simulations are performed with 1.8 V voltage supply using 180 nm CMOS process. The RF power used is -30 dBm and LO power is set to 5 dBm. A new Ultra Low Power Diode (ULPD) load based down-conversion mixer is also designed and simulated. It is designed to operate at 2.5 GHz RF frequency with 250 MHz Intermediate frequency. The conversion gain provided by the mixer is maximum ~8dB at 2.1GHz RF frequency. The power consumption for the mixer core circuit is ~17mW. The mixer presents good RF to IF port isolation with input return loss less than zero. The Input Third Order Intercept point (IIP3) increases from ~ 9dBm to 15.8 dBm for variation of the source degeneration inductors from 1 nH to 20 nH. The IIP3 obtained is 11.64 dBm at 4 GHz RF frequency with 1nH inductor.

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Abbreviations and Symbols Used

IF	Intermediate Frequency
ULPD	Ultra Low Power Diode
LO	Local Oscillator
RF	Radio Frequency
BaLun	Balanced Unbalanced
CMOS	Complementary Metal Oxide Semiconductor
IIP3	Input referred Third order Intercept Point
IM	Intermodulation
NF	Noise Figure
P_{1dB}	1-dB compression
Wi-Fi	Wireless Fidelity
dBm	Power level in decibel(dB) relative to 1mW
TSMC	Taiwan Semiconductor Manufacturing Company
IMD3	Third-order Intermodulation
IM3	Third-order Intermodulation Distortion Products
GSM	Global system for Mobile
WCDMA	Wideband Code Division Multiple Access
DECT	Digital Enhanced Cordless Telecommunication
UMTS	Universal Mobile Telecommunication System
CSMA	Carrier Sense Multiple Access
GMSK	Gaussian Minimum Shift Keying
IS-54	Interim Standard-54

Chapter 1

Introduction

1.1 Overview

In recent years, the tremendous increase in the demand for cell phones, cordless phones, notebook computers, PDA's (Personal Digital Assistants), pagers etc has led manufactures and researchers of consumer electronics to develop low cost solutions for wireless telecommunication services. The technological advancement in the field of wireless communication has made it possible that a handheld electronic device incorporates multiple services and features such as Bluetooth, PDA, WiFi, GPS(Global Positioning system), e-mail, wireless internet browsing etc. Transceiver is an important device for transmitting and receiving data and multimedia over the wireless links. To accommodate multiple transceivers with other accessories in a small gadget like cell phone, the transceiver required must not only be inexpensive (cost effective) but should also use minimum resources, consume very less power and provide highly integrated circuitry with minimum external components.

As the technology is progressively scaling down due to the shortening of the channel length, leading to miniaturization of transistors, on-chip integration of a transceiver has become feasible. A transceiver IC has brought down the power consumption as well as the cost of the products manufactured. Extensive research is going on wireless transceiver ICs for investigating efficient methods of designing for reducing equipment cost, enhancing battery life by reducing power consumption, minimizing chip area and attaining wider bandwidth to satisfy widespread needs of end users. Designers are putting more and more efforts for finding ways to set up a good compromise among the various tradeoffs involved in designing of RF (Radio Frequency) circuits and transceivers.

Wireless devices employing RFIC technologies are advancing through leaps and bounds as a consequence of the progress in transistor fabrication technologies. Therefore, higher integration density, greater functionality, higher mobility can be obtained with small sized transistors. Bulky inductors and capacitors give good performance at radio frequencies but occupy larger chip area because they cannot be scaled like transistors. It means that for attaining high integration density, use of passive components must be avoided in radio transceivers. Active components can provide very good speed for GSM, WCDMA, Bluetooth (<6 GHz) and sufficient speed of operation for UWB (3.1-10.6 GHz) applications. With the shrinking line widths of the transistors, their silicon area requirement and parasitic capacitances also decrease and thereby increasing its switching speed.

Moreover, the advancement in digital signal processing and high data rate network standards like GSM has increased the usage of digital circuits for radio systems. These digital circuits could be easily implemented with CMOS circuits, consuming very less power and are cheaper also. Though bipolar, SiGe and GaAs technology can provide high performance at radio frequencies, CMOS technology offers technology scaling as well as integration of circuitry for both analog and digital blocks on the same chip. These advantages of lower cost, area, power consumption and transition time have compelled researchers to develop radio frequency transceiver IC's using CMOS technology. However, we need to overcome several challenges such as increased leakage currents, lower trans-conductance gain etc for designing analog and digital circuits in scaled CMOS technology.

Various RF receivers comprising variety of subsystems for improving their performance capabilities are under research. This work is an effort towards developing mixer circuits offering high linearity and consuming very less power. A ring oscillator circuit with minimum propagation delay and wide tuning range is also designed. This ring oscillator can also produce symmetric output waveforms which results in even order harmonic cancellation i.e., highly linear operation.

1.2 Motivation

The invention of wireless telegraphy by Guglielmo Marconi in 1896 for sending morse code has made its way to the present devices such as Bluetooth, WiFi, Zigbee, WLAN, GPS, IEEE 802.11 a/b/g etc. For the procurement of all these services by an electronic device, multiple transceivers are required so that the device is capable of operating in various frequency ranges in accordance with different wireless standards. In addition to wider operating bandwidth, an RF receiver must provide high linearity. Linearity ensures the sensitivity of the receiver. Non-linearity in the communication device produces inter-modulation and cross-modulation products due to the presence of interferers in the band of interest. Mixers and oscillators are the essential blocks in a radio transceiver system.

Mixer, a frequency translation device, performs the task of up-conversion or down-conversion of input signal frequency with the help of a local oscillator. Mixing or frequency translation is performed at the second stage in an RF receiver front-end. The performance of the overall receiver system is immensely dependent on the linearity, Noise Figure and the distortion level of both subsystems. Moreover, to serve the needs of modern electronic equipments, these subsystems area requirement and power consumption must be as minimum as possible. The recent advances in CMOS technology facilitates the designing of low power mixer and oscillator circuits, operating at very low voltage and occupying very small chip area. Fabrication of RF receiver IC with enhanced performance parameters by taking into consideration the various tradeoffs involved is an area of extensive research.

For obtaining progressively high performance of these RFIC subsystems at low operating voltage, minimum leakage, high speed and small power consumption with reduced number of transistors, various circuits have been developed by various researchers. Motivated by this idea and analyzing the feature and capabilities of the existing RF mixers and oscillators, certain modifications are suggested and new designs have been proposed in this work.

1.3 Issues and Challenges

Integration of digital processing capabilities to the modern wireless integrated transmitter and receiver sections has opened the passage of new prospects of designing. The imbalances which were faced by the analog circuit blocks of the transceiver could be reconciled with the use digital circuitry because it offers less inherent mismatches. Reduction in mismatches has improved the rejection of spurs and the inter-modulation products. Besides reducing imbalances of the circuitry, many other advanced techniques of elimination of distortion are automatically incorporated with their use, leading to the improvement in performance and therefore reduction in testing load after production.

Inter-modulation distortions mainly due to the second and third order products deteriorate the dynamic range of operation of a receiver. Various methods for reducing their effects have been proposed and are under research as well. Down-conversion mixer, being the second block in RF chain must not be troubled by the inter-modulation products towards the high end of the operating range of the signal. The demand for the low cost and low power single chip solution has stimulated the evolution of numerous architectures and technologies which are emphasizing more and more on submicron CMOS process. Along with a variety of system architectures, various wireless standards for diverse range of services are existing and other new standards are still evolving, each having different specifications. It is therefore quite challenging to design RF systems satisfying all the specifications. Moreover on a portable device, RF components require only a small space of the whole communication system; still their cost is considerably higher than the cost of DSP and baseband blocks. The main reason behind is that systematic design procedures of RF sections of high capabilities are still very immature and limited. It is evident from the complex procedures involved in the designing of RF components with low noise figure. Generally optimum noise figure is ensured with reference to the impedance of the source. Yet this optimum NF does not comply with the optimum impedance matching, maximum linearity or optimum power consumption of the mixer [1].

Consequently, exploration of techniques for cancelling inter-modulation products as well as providing optimum noise figure is an active area of research.

1.3.1 Motivation for designing a 2.5 GHz mixer

The extensive growth in wireless services and products has severely congested the 900 MHz band of frequency spectrum for networking. In addition to voice, transmission of real time multimedia using wireless network requires extended bandwidth which can be obtained by operating in high frequency band only. The advent of wireless internet and wireless LAN has further overcrowded the high radio frequency unlicensed spectrum. This explosion in the number of devices has increased the probability of interference among various bands. The designers and manufactures are therefore facing challenges of designing receiver with reduced interference levels. The motive of this thesis is to identify the future trends of wireless industry and explore the down-conversion mixer architecture to meet the upcoming wireless demands.

1.3.2 Wireless Standards

Many wireless standards are adopted by different systems. Each standard has different specifications with respect to available frequency band, noise limitation, maximum power, range limitation etc. Therefore, the designers should consider the various specifications for the devices, so that the standards should be adopted for that device.

1.3.3 Design concerns for Wireless Standards

Wireless communication devices support various standards, each defines its own specifications including sensitivity and performance of the receiver as can be seen in Table 1.1. Therefore, these defined standards necessitate the designing of receiver front ends according to the specified frequency band, signal power, data rate and modulation scheme. While designing a mixer, these key requirements must be carefully taken into consideration.

At microwave frequencies, high channel bandwidth is another important consideration. Previously adopted 2G and 3G standards like GSM, DECT, IS-54 and PHS were mainly used for transmitting voice, so channel rate required is only tens of kilobits/second and nearly up to 1 Megabits/second. The era is now changed to evolving new standards such as wireless LAN with which the operating frequency has become two times and channel rate increased upto 20 times high while signal bandwidth has been quadrupled.

Besides facing the challenge of higher operation frequency, researchers have to take the concern of increased inter-modulation distortions due to the enhanced signal bandwidth. The device designed for wider bandwidth can support multiple wireless standards as in the case of cell-phones available today, having both 2G and 3G capabilities.

Table 1.1: Wireless standards [2]

Range	**Long**		**Medium**	**Short**	
System	GSM/DCS	UMTS	802.11	Bluetooth	DECT
Frequency	0.9/1.8GHz	2GHz	5GHz	2.4GHz	1.9GHz
Channel spacing	200 KHz	5MHz	20MHz	1MHz	1.728MHz
Access	TDMA	CDMA	CSMA/CA	CDMA	TDMA
Modulation	GMSK	QPSK	BPSK/QPSK/QAM	GFSK	GFSK
Bit rate	270K	3.84M	5.5-54M	1M	1.152M
R_x sensitivity	-100dBm	-117dBm	-65dBm	-70dBm	-83dBm
Signal S/N+I	9dB	5.2dB	28dB	21dB	10.3dB
R_x NF	9dB	9dB	7.5dB	23dB	18dB
R_x IIP3	-18dBm	-4dBm	-20dBm	-15dBm	-22dBm
Phase Noise	-141dBc @3MHz	-150dBc @135MHz	-102dBc @1MHz	-105dBc @1MHz	-99dBc @2.2MHz
Frequency	0.9/1.8GHz	2GHz	5GHz	2.4GHz	1.9GHz

1.3.4 Impact of wider receiver bandwidth on the signal distortion

If the receiver bandwidth is chosen much higher than the required, more third order inter-modulation components will exist in the band of interest (IF band), causing the deterioration of linearity of the mixer. Moreover, bandwidth is scarce resource in communication so its optimum utilization is necessary while designing any circuit.

1.3.5 Identifying the non-linear elements

In a mixer design, various active as well as passive components are exploited having non-linearities in their operational characteristics. These non-linearities will definitely causes harmonics and inter-modulation distortions, thus degrading the mixer's performance. It is the task of system designer to make suitable arrangements in the circuitry for suppressing non-linearities.

1.3.6 Specifications and trade-off

RF transceivers encounter numerous tradeoffs among various circuit specifications such as Conversion gain, Dynamic range, Linearity, Leakage power, port to port isolation, Noise Figure etc. All these tradeoffs must be considered for different application requirements.

1.4 Research Goal

The aim of this research is to identify the future trends of wireless networking by comprehensively discussing some of the RF CMOS mixers for down-conversion at receiver end. The key objectives of research are:

- Designing of active down conversion mixer for wider unlicensed band applications with CMOS process, applicable in various wireless systems satisfying multiple wireless standards such as Zigbee, Bluetooth, WLAN WiFi etc.
- Effective utilization of source degeneration and current bleeding techniques in the architecture for enhancing linearity of the mixer.
- Minimize the supply voltage and power consumption for the circuit.
- Optimize the various performance metrics of the mixer for the desired applications.
- Determining the effects of various loads on the parameters of the CMOS Gilbert Mixer.

To accomplish these tasks, all the architectures and topologies of the mixers available needs to be investigated properly to identify the advantages and disadvantages of one over the other.

1.5 Contribution of the Thesis

The major contributions of this work are:

- Characterization of various loads for Gilbert cell down-conversion mixers.
- Analysis of effects of loads on the mixer performance.
- Designing and analysis of new methods of implementing loads in the mixer.
- Methods to enhance linearity of the mixers.

Improved modeling of Gilbert cell mixer is demonstrated with appropriate considerations to the mismatches involved in the differential switching transistors. Simulations for Gilbert mixer with various optimized loads have been performed. Agilent's Advanced Design System software tool has been employed for determining performance characteristics.

Finally, a wide band down-conversion mixer with Ultra Low Power Diode (ULPD) based load is presented in this work. The mixer is designed to operate from 100 MHz to 6 GHz frequency range. The mixer is designed to operate at 2.5 GHz RF frequency with 250 MHz Intermediate frequency. The conversion gain provided by the mixer is maximum ~8dB at 2.1GHz RF frequency. The power consumption for the mixer core circuit is ~17mW. The mixer presented has good RF to IF port

isolation with input return loss less than zero. The Input Third Order Intercept point (IIP3) increases from ~ 9dBm to 15.8 dBm for variation of the source degeneration inductors from 1 nH to 20 nH. The IIP3 is 11.64dBm at 4 GHz RF frequency with 1nH inductor.

The ULPD load based mixer employing current injection technique is also simulated which improves the linearity of the mixer without significant loss in conversion gain and noise performance. The mixer is simulated with 1.8V voltage supply using 180nm CMOS process. The RF power is -30 dBm and LO power is set to 5 dBm.

1.6 Thesis Organization

This thesis is organized to provide the progressive information regarding the design of active CMOS down-conversion mixers.

Chapter 2

This chapter gives the general overview of receiver front-end structure and fundamentals of the mixers. It further elaborates the mixer topologies, characterizing and their performance parameters. This chapter emphasizes on the analysis and operation of dual balanced Gilbert cell mixer, followed by detailed survey on its previously implemented loads. Several issues required to be considered in initial phases of designing are also discussed.

Chapter 3

This chapter illustrates the step-by-step design methodology explaining the modelling of various blocks of the Gilbert down-conversion mixer. It also introduces a down-conversion mixer with new load stage.

Chapter 4

This chapter discusses the various simulation and measurement results of the Gilbert mixers implemented using 0.18µm CMOS technology. Performance evaluation and comparison of the designs with some recently reported active CMOS mixers are also provided in this chapter.

Chapter 5

This chapter concludes with the final outcome of the research done justifying, how the work presented in this thesis is significant for exploring the new area of research.

Chapter 2
Literature Review

2.1 Introduction

This chapter presents a general overview of the front end of an RF receiver, to illustrate the significant role played by the down-conversion mixer in a communication system and the various performance parameters used for determining the suitability of the mixer for a particular application.

2.2 Receiver System Architecture

Figure 2.1 shows a typical super-heterodyne receiver. The incoming signal is received through an antenna and the desired frequency band is selected by using band-select filter and rejects out the unwanted out-of–band interferers. The filtered signal is amplified using a low noise amplifier and then subjected to an image reject filter, to remove the image frequency. The frequency signal thus obtained is translated to a lower frequency i.e., intermediate frequency by using a down conversion mixer, followed by a channel select filter. The signal is again down converted using mixer to a baseband signal for further processing.

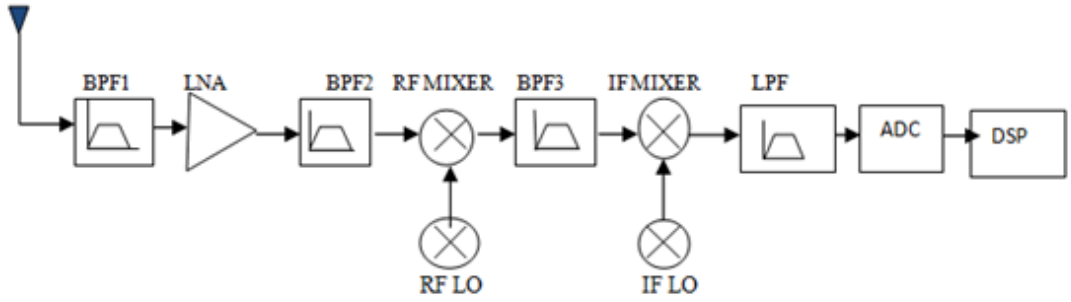

Figure 2.1: Radio Frequency Receiver system architecture

The performance of an RF Receiver is mainly evaluated on the basis of two important parameters i.e., its sensitivity and selectivity. Various other parameters like linearity, noise performance, image rejection ratio and gain distribution greatly influences these fundamental receiver parameters.

Receiver sensitivity: Sensitivity is the minimum possible change in the signal power level at the receiver input which produces enough signal to noise ratio (SNR) at the output and therefore ensures its proper functioning. The wireless receiver can exist inside a cell phone, a base station or any wireless communication standard compliant equipment such as Bluetooth, Zigbee, WLAN etc. Up to this signal power level, Bit Error Rate is within the specified range of the system. If the signal level of the system

drops below this, bit error in the system will be much higher and therefore receiver system must not be operated below this minimum power level specified. For Zigbee wireless standard at 2.4 GHz, IEEE specifies the receiver sensitivity nearly -85 dBm. It means that, if the receiver sensitivity is increased to -90 dBm, radio distance coverage range will be extended. Higher will be the receiver sensitivity, less will be the transmitter power required and therefore lower power consumption and enhanced battery life. For this reason, one must have a radio device of sensitivity as much high as possible. It is expressed in terms of dBm for 50 Ω characteristic impedance in most of the RF systems. Generally, for achieving high sensitivity input impedance of the receiver is properly matched with the source impedance and is usually measured in a noise free environment. Sensitivity of the receiver mainly depends on the noise figure and demodulation scheme used for extracting the desired information.

Receiver Selectivity: While measuring sensitivity of the receiver, interference from other unwanted signals is not considered. Selectivity refers to the capability of a wireless receiver to detect and extract the desired signal in an environment containing many other unwanted interfering signals. Therefore, selectivity is the measure for determining performance of the receiver in the presence of undesirable co-channel as well as adjacent channel interference. Although complete elimination of undesired signals is not possible, but if their levels are low compared to the desired carrier frequency, then error free performance can be achieved. Selectivity is determined by adjacent channel selectivity, third order inter-modulation performance, image rejection, out of band blocker rejection capability of the front end of receiver.

Mixer's role in RF receiver front end: The mixer plays an important block of RF signal chain in the super-heterodyne receiver used for many wireless applications. It enables the tuning of the receiver over a wider frequency band by translating the desired frequency to a fixed intermediate frequency thereby allowing the efficient processing, filtering and demodulation of the signal.

The third order intercept point and noise figure of a receiver circuit are given by:

$$IIP3_{tot} = \frac{1}{IIP3_{(1)}} + \frac{G_1}{IIP3_{(2)}} + \frac{G_1^2 G_2^2}{IIP3_{(3)}} + \ldots \quad (2.1)$$

$$NF_{TOT} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \ldots \quad (2.2)$$

where IIP3 is third order input intercept point, G is the gain of the different stages, NF is the noise figure of the system and F is the noise figure of single stage. Equations 2.1 and 2.2 show that IIP3 point of the second stage and the noise figure F_2 mainly determines the performance of the receiver. Mixer being the second stage critically affects the performance of the overall system.

2.3 Mixer fundamentals

Basic Principle:

There are two methods of performing frequency translation of signals:

(i) Using Non linear components like diode

(ii) Using Linear, time variant circuits.

These circuits can perform the frequency shifting operation which a linear time invariant system cannot. The output of a non linear circuit is given by

$$v_o = \sum_{m=0}^{N} a_m v_{in}{}^m \tag{2.3}$$

Where v_o is the output voltage and v_{in} is the applied input. Equation 2.3 shows that v_o consists of a dc term and the harmonics of input. To perform the frequency translation (mixing) process, a nonlinear or time varying circuit is required. A mixer is a device which performs the frequency shift to a higher or a lower spectrum by multiplying two signals in time domain and multiplication in time domain corresponds to convolution in frequency domain. A mixer behaves ideally as a multiplier circuit so it is represented by a multiplier symbol as shown in Figure 2.2.

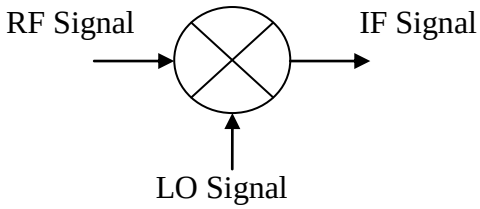

Figure 2.2: Basic symbol for 3 port mixer

The three ports of mixer are: LO (Local oscillator), IF (Intermediate frequency) and RF (Radio frequency). In actual, a mixer is a linear, time varying system with reference to RF port and non-linear time variant system with respect to LO port.

Assuming that two sinusoidal signals $A_1 \cos(\omega_1 t)$ and $A_2 \cos(\omega_2 t)$ are applied as inputs to mixer, then the resultant multiplication expression can be given as:

$$A_1 \cos(\omega_1 t) A_2 \cos(\omega_2 t) = \frac{A_1 A_2}{2} \cos(\omega_1 - \omega_2)t + \frac{1}{2} \cos(\omega_1 + \omega_2)t \tag{2.4}$$

It can be interpreted from Equation 2.2 that the mixer output comprises the sum ($\omega_1+\omega_2$) as well as difference ($\omega_1-\omega_2$) terms of input frequencies. Depending on the desired application, whether up-conversion or down-conversion, one frequency component is filtered out and the other is retained from the mixer output for further processing. The two inputs to the mixer are Radio frequency (RF) signal or

Intermediate frequency (IF) signal and local oscillator (LO) signal based on its requirement as transmitter or receiver. For frequency down-conversion which is employed in the RF receiver circuit, a high frequency RF signal is translated to a lower frequency by mixing it with an LO signal. Since difference frequency (ω_1-ω_2) is desired signal for down conversion, it is allowed whereas (ω_1+ω_2) is attenuated using filter circuits. On the other hand, towards the transmitter side, frequency up conversion is used to translate the baseband signal at low frequency to an RF signal, by multiplying with an LO signal. In this case, sum frequency is kept at output while difference signal is rejected.

2.4 Performance parameters for mixer

2.4.1 Conversion Gain

The capability of a mixer to translate frequency is measured in terms of conversion gain or loss. It can be defined in two ways: - (a) Power conversion gain (b) Voltage conversion gain. By default power conversion gain is considered. The power conversion gain and voltage conversion gains are alike (in terms of dB) when both input and output impedances of the mixer are equal to the impedance of the source.

The voltage conversion Gain can be defined as the ratio of the root mean square value of output IF signal and input RF signal for a down conversion mixer. The power conversion gain is expressed as the ratio of the output power obtained at the load to the available input RF power.

$$G_{c,voltage} = \left(\frac{V_{IF}}{V_{RF}}\right) \qquad G_{C,power} = \left(\frac{P_{IF}}{P_{RF}}\right) \tag{2.5}$$

$$\text{In decibel} \quad (G_C)dB = 10\log\left(\frac{P_{IF}}{P_{RF}}\right) = 10\log\left(\frac{\frac{V_{IF}{}^2}{R_{IF}}}{\frac{V_{RF}{}^2}{R_{RF}}}\right) = 20\log\left|\frac{V_{IF}}{V_{RF}}\right| \tag{2.6}$$

Conversion gain for an active mixer is given by

$$G_{C,dB} = 20\log\left(\frac{4}{\pi} \times G_m \times R_L\right) \tag{2.7}$$

Where G_m is the transconductance of the transistor and R_L is the load resistance of the mixer.

2.4.2 Linearity

In general, RF circuits are assumed to have linear model for obtaining responses to the signals applied at the input. The reason being devices like transistor as well as switching activities introduce nonlinearities in the output. Mixers are also

inherently non-linear in their operation because non-linear or time-varying circuits are employed for frequency shift operation.

The relation between input and output for a non linear system can be given as

$$V_{out} = \alpha_0 + \alpha_1 v_{in}(t) + \alpha_2 {v_{in}}^2(t) + \alpha_3 {v_{in}}^3(t) + \ldots \alpha_i {v_{in}}^n(t) \quad (2.8)$$

where V_{out} is the output voltage, V_{in} is the input voltage and α_k are constants. The non linearities which exist in the system can be explained:-

(a) Harmonics: - If sinusoidal signal is given as input to the mixer, then the circuit non-linearities leads to frequency components which are integral multiples of the fundamental frequency.

$$\text{If } Vin(t) = A\cos\omega t$$

Then for a non linear system, output will be

$$Vout(t) = \alpha_1 A\cos(\omega t) + \alpha_2 A^2 \cos(\omega t) + \alpha_3 A^3 \cos^3(\omega t)$$

Simplification of above equation gives

$$Vout(t) = \alpha_1 \times A\cos(\omega t) + \frac{\alpha_2 \times A^2}{2}(1+\cos(2\omega t)) + \frac{\alpha_3 \times A^3}{4}(3\cos(\omega t) + \cos(3\omega t))$$

$$Vout(t) = \frac{\alpha_2 \times A^2}{2} + \left(\alpha_1 \times A + \frac{3\alpha_3 \times A^3}{4}\right)\cos(\omega t) + \frac{\alpha_2 \times A^2}{2}\cos(2\omega t) + \frac{\alpha_3 \times A^3}{4}\cos(3\omega t) \quad (2.9)$$

where component corresponding to frequency ω is called fundamental component and the rest higher order terms are called 'harmonics'. Even order harmonics can be suppressed by using differential configuration.

(b) Gain compression: - When small signals are considered for determining gain, harmonics are assumed to be negligible. It can be seen from equation 2.9 that, if amplitude A of the signal is small, then the gain $\left(\alpha_1 \times A + \frac{3\alpha_3 \times A^3}{4}\right)$ corresponding to the fundamental component will be quite larger than that of the second and third order harmonics present at the output. However as the value of A becomes substantially larger, variation in gain takes place.

It appears that if $\alpha_1\alpha_3 < 0$, gain of the system decreases as the input amplitude A increases i.e., gain is compressed at higher input values.

In RF circuits this effect is quantified by 1dB-compression Point as explained below.

(c) 1dB Compression Point: - 1 dB compression point (P1dB) is a method used to measure the extent by which nonlinearities affect the performance of a mixer. A large input signal saturates mixer characteristics which leads to the deviation in linear magnitude response and hence reduces its power gain. Thus P1 dB is defined as the

input signal power level that causes the gain of the mixer to drop by one decibel. 1dB-compression point is generally plotted on a log scale representing the variation of the output signal level with respect to the input levels as shown in Figure 2.3.

The straight line shows the magnitude response of a mixer, if it is behaving linearly. At higher input power levels, conversion gain of the mixer degrades, which is shown by a solid line. This degradation occurs as a consequence of the odd order nonlinearities and limiting effects. Conversion gain is mainly limited by two effects called current limiting and/or voltage headroom limiting.

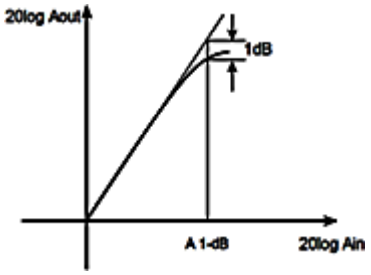

Figure 2.3: Gain compression (1-dB compression point)[9]

If the input signal is larger than the P1dB, this phenomenon leads to the conversion of amplitude modulation (AM) to phase modulation (PM). It means that for a frequency modulated there will be no loss in information but for phase modulated signal, Bit Error Rate (BER) increases significantly.

1dB compression point can be obtained graphically as

$$20\log\left\{\alpha_1 + \frac{3}{4}\alpha_3 A^2(1dB)\right\} = 20\log|\alpha_1| - 1dB \tag{2.10}$$

$$\text{which gives } A(1dB) = \sqrt{0.145\frac{\alpha_1}{\alpha_3}} \tag{2.11}$$

where A is the gain of the system and α are the constants. 1dB compression point is measure of the maximum input range of the mixer circuit.

(d) Intermodulation products: - When two signals with different frequencies are applied as input to a nonlinear system, in addition to harmonics of the input frequencies, certain other spurious frequency components appear at the mixer output. This phenomenon is called intermodulation and the frequency components obtained are called Intermodulation products products.

IM products are problematic for RF systems. If a weak desired signal as well as two strong interferers enters a non linear system then IM products may fall into the band of interest, corrupting desired frequency component. The magnitude of the IM products can be used as a measurement of linearity.

2.4.3 Third Order Intercept Point (IIP3)

The 3rd order intercept point (IP3) is another parameter like 1dB compression point, for determining the extent of nonlinearities in the mixers. The blocking capability of a receiver is affected intermodulation which can be expressed in terms of IIP3. For a mixer, IIP3 is a signal handling capability.

More precisely we can describe IIP3 provides a quantitative measure of the third order non linear products which may occur in a mixer under the multi-tone excitation conditions. When two nearby frequency signals are applied to a nonlinear circuit, intermodulation products are generated different from the harmonics of input frequencies. For two input signals with frequencies $\omega_1$and ω_2, the II order intermodulation products are $\omega_1 \pm \omega_2$ and the 3rd order IM products are $2\omega_1 \pm \omega_2$ and $2\omega_2 \pm \omega_1$. If ω_1 and ω_2 the components have a small difference in their frequency, then the third order intermodulation products appear in the close vicinity of ω_1 and ω_2 as depicted in Figure 2.4.

Thus, it is apparent that a stronger interference signal with a frequency close to the desired signal frequency will corrupt the signal due to 3rd order intermodulation products. The fundamental tone increases in proportion to A, whereas IM3 increases in proportion to A^3 [4].

IP3 is measured by a two tone test. This two tone test is more relevant to evaluate mixer performance where both the wanted signal and interferer may exist. If the amplitudes of both the signals are assumed to be equal, then the magnitude of intermodulation products rises at three times the rate at which the fundamental component increases.

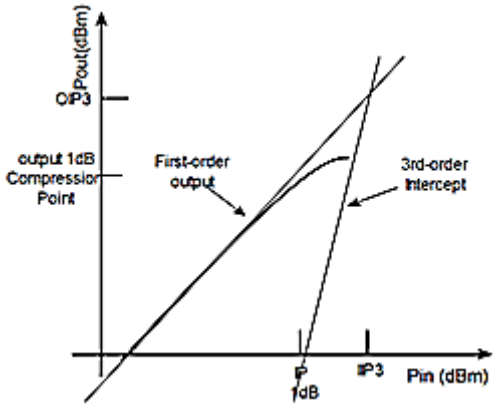

Figure 2.4: Third order intercept point [9]

The intersection point of these two lines is defined as the third order intercept point. IP3 is obtained by, "the extrapolated point where the fundamental tone and 3rd order intermodulation products (IM3) intersect each other. At this point IM3 is equal to 0 dBc. The input power level corresponding to the this point (horizontal coordinate) is called input referred IP3 (IIP3) and output power level is called output power level (vertical coordinate) referred as IP3 (OIP3) and is given by

$$A_{IIP3} = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|} \tag{2.12}$$

2.4.4 Port to port isolation

The isolation must exist between every ports of a mixer. Isolation gives the amount of power coupled from one port of the mixer to the other. Port isolation is a measure of frequency component suppression ability of a mixer among its ports. It is desirable to minimize interaction among RF, IF and LO ports to enhance the sensitivity of the receiver, which may get distorted by the temperature and the process technology variations. In general, isolations in a mixer are given in terms of:

(a) LO-to-IF isolation: - It indicates the amount of LO power which leaks through the IF port at output, also called as LO feed through. This occurs due to the presence of parasitic capacitances and the power supply coupling.

(b) LO-to-RF isolation: - It indicates the LO power leakage through the RF port only, also called as reverse LO feed-through. It is due to the presence of the parasitic capacitances suppression of interactions occurring at the RF port. It is more problematic because of the large separation between the RF and LO frequencies. The isolation between LO and RF ports of the down conversion mixer is important as this feedthrough may cause re-radiation through antenna.

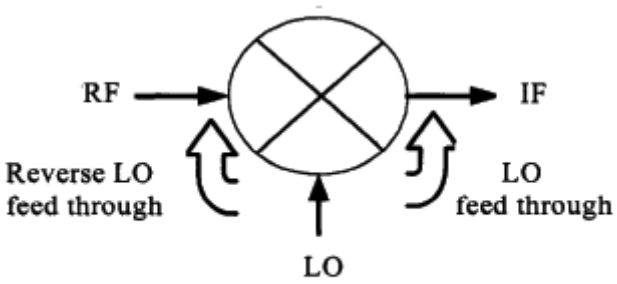

Figure 2.5: Mixer Ports Leakage Signals[9]

When the port impedance and the source impedance are not matched properly, some of the power delivered to the port is reflected back to the source. It is therefore, essential to provide appropriate impedance matching at RF and IF ports to avoid signal reflections. Port to port isolation of a mixer depends on the architecture and topology. Higher the isolation between the mixer ports, the better it is. Since LO signal is quite large as compared to the RF signal, any LO-RF feedthrough or leakage, if not filtered out, may cause problems in the subsequent stages of the signal processing chain. In addition, large RF and LO feedthrough signals at the IF output may saturate the IF port and decrease the Pl dB of the mixer. It also determines the amount of pre-filtering and post-filtering required for the mixer.

2.4.5 Noise Figure

Noise is general term used to describe an unwanted signal which deteriorates the reception of a desired signal in wireless receiver. When considered in case of a mixer, output IF signal is mainly contributed by two input signal frequencies i.e., desired RF signal and the image signal. Noise in case of a mixer is expressed in terms of Noise Figure. Noise Figure (NF) is defined as the ratio of the signal power to noise power ratio at the output.

$$NF = \frac{SNR_{input}}{SNR_{output}} \tag{2.13}$$

where NF is the noise figure of the system, SNR_{input} is signal to noise ratio at the input and SNR_{output} is signal to noise ratio at the output.

For a mixer, it is specified in terms of single sideband (SSB) NF or double sideband (DSB) NF. SSB noise figure is used for the mixers in which the input signal is contained in one sideband and the other sideband is removed by an image rejection filter. DSB noise figure is applied for the mixers where the input signal is contained by both the sidebands. DSB NF is applicable to direct conversion mixers [3].

$$NF_{SSB} \cong NF_{DSB} + 3dB \tag{2.14}$$

where NF_{SSB} is the noise figure of the system and NF_{DSB} is double-sideband noise figure.

2.5 Mixer Topologies

Selection of a particular mixer topology is made based on the various system requirements and inevitable performance trade-offs. The main objective of a system designer is to set a best compromise among different performancw parameters the mixer i.e., Third-order intercept (IP3), Noise Figure (NF), power dissipation, available voltage, integration density (on-chip versus off-chip components) and final cost of the product.

In terms of conversion gain, mixers are generally classified as passive and active mixers: Active mixers can provide conversion gain which suppresses the noise presented by the subsequent IF and baseband stages of the receiver as well as reduces the LO power required for the operation. They are generally implemented using transistors and are widely used in RF applications [5].

On the contrary, passive mixers always exhibit conversion loss rather than gain and can operate at comparatively higher frequencies (>10 GHz). In addition to excellent IM performance, they provide highly linear performance and faster speed. These characteristics make them suitable for microwave and base station circuits [4].

The major drawback of this mixer is the requirement of higher LO power because of the loss incurred by the passive elements used.

Large LO drives, along with good LO-to-IF and LO–to-RF isolation [17], is problematic in low voltage/low power environments, therefore active mixers designed using CMOS technology are preferred for designing integrated circuitry. However, additional gain stages can be used to provide gain to a passive type CMOS mixer and hence to achieve a fully integrated transceiver IC as reported in [6, 7].

2.5.1 Passive Mixers

2.5.1.1 Diode Mixers

(a) Single diode mixer

Diode mixers are widely used for high frequency applications. They are used in discrete circuitry due to their simple configuration, low noise figure and high frequency performance. Even though diode mixers incorporate conversion loss, their exquisite features make them applicable for high performance discrete equipments [8]. Earlier they were used as UHF TV tuners and as demodulators of radar sets. They can also be used as crude demodulator circuits for AM signals by placing a simple RC circuit for output filtering and removing LO signal from input [9].

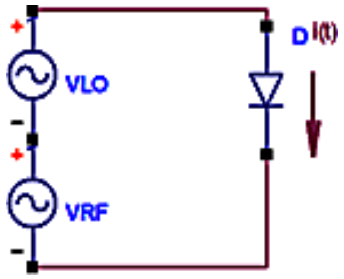

Figure 2.6: Single diode Mixer

In Figure 2.6, a basic single-ended diode mixer is shown which consists of a single diode element. The series combination of RF and LO signals is applied as input for driving the diode. This mixer utilizes the nonlinear V-I (voltage-current) characteristics of the diode for their operation. In a diode, the relationship between the voltage and the current is given by-

$$i(t) = Is\left[\exp\left(\frac{qv(t)}{\eta kT}\right) - 1\right] \tag{2.15}$$

where Is is the saturation current (A), k is the Boltzmann's Constant (J/K), T is the absolute temperature(K), q is the electronic charge (eV) and η is the diode ideality factor (emission coefficient). Using the small-signal approximation and expanding i(t) in Taylor series gives:

$$i(t) = I_0 + Gd_1[v_{RF}(T) + v_{LO}(t)] + \frac{Gd_2}{2}[v_{RF}(t) + v_{LO}(t)]^2 + ... \qquad (2.16)$$

where Gd_1 and Gd_2 are dynamic conductances of the diode. Since the output current comprises numerous harmonics of the input frequency and intermodulation products. V_{RF} and V_{LO} are the amplitudes of the RF and LO inputs respectively. The second order intermodulation products (IM2) obtained from the above equation is:

$$I(t)_{IM2} = \frac{Gd_2}{2} V_{RF} V_{LO} [\cos(\omega_{RF} - \omega_{LO}]t + \cos(\omega_{RF} + \omega_{LO})t] \qquad (2.17)$$

The drawbacks of a single diode mixer are its poor LO-to-RF isolation and inability to provide the conversion gain. Consequently two diode mixers were came into existence to achieve higher port isolation [9].

(b) Single balanced diode Mixer [3]

Figure 2.7 shows a single balanced diode mixer in which LO and RF ports are isolated but the circuit has poor RF to IF isolation. If enough large value of LO drive is provided to ensure proper switching of the diodes independent of the RF signal magnitude. When LO goes positive, both diodes will conduct, therefore RF signal get connected to IF output. Similarly when LO become negative, diodes are reverse biased and open the connection of RF. Hence effectively the mixer acts a commutating circuit. It is evident from the circuit operation that IF and RF ports get connected together in ON condition of diodes. High RF-LO isolation is guaranteed by symmetry conditions. When diodes conduct, only common voltage is developed across the transformer winding by RF voltage signal, as a result no voltage induces at the LO port. However, good amount of filtering is required for obtaining the desired IF output from this mixer.

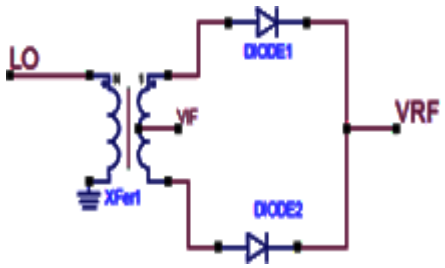

Figure 2.7: Single Balanced diode Mixer

In order to achieve good isolation among the all the ports, the double balanced diode mixer is preferred to single balanced mixers.

(c) Double Balanced Diode Mixer

As shown in Figure 2.8, its configuration comprises four diodes connected in the form of a bridge. The LO drive should be sufficiently large to cause appropriate ON or OFF switching of diodes with changing polarities of the LO voltage.

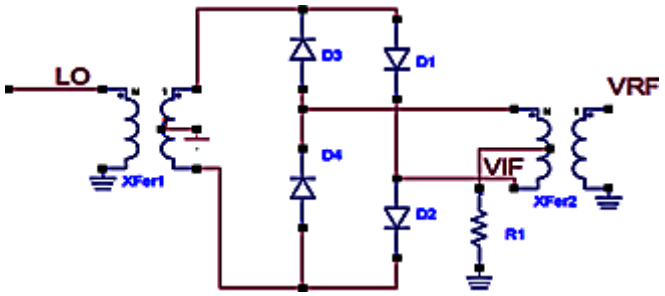

Figure 2.8: Double Balanced diode Mixer

When the LO signal is positive, diodes D3 and D4 are ON and therefore output voltage V_{IF} is equals to V_{RF} and if the LO drive becomes negative, diodes D1 and D2 conducts and voltage V_{IF} becomes equals to $-V_{RF}$. If the circuit is well-matched, the double-balanced diode mixers can provide good isolations [3]. It is clear from Figure 2.8 that the IF signal is connected to the virtual ground of the LO signal, which yields a high LO-to-IF isolation. Furthermore, the IF signal is also connected to the virtual ground of the RF signal. As a result, the RF-to-IF isolation is also large. Since the RF and LO signals share the virtual ground, a high RF-to-LO isolation is also achieved in this mixer [8]. Double balanced diode mixers show more conversion loss compared to single balanced. Its Dynamic range is limited by the breakdown voltage of the diode and can be increased by replacing each diode with a diodes in series but it will require higher LO drive for proper switching [9].

2.5.1.2 Passive CMOS Mixers

(a) FET Resistive Mixer

A transistor can be used a high performance switch and this capability makes the CMOS technology an attractive choice for the designers. High-performance passive mixers can be affordably manufactured using CMOS process.

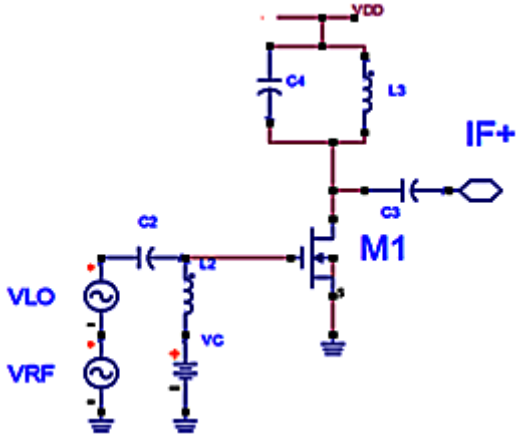

Figure 2.9: FET Resistive Mixer

In a passive FET mixer also called as an FET resistive mixer, RF signal and the LO signal are applied in series to the gate of FET [2]. During its operation, the channel resistance that exists between drain and source of FET is modulated by the large power LO signal while maintaining the transistor in linear region. The channel is

made to switch between fully depleted and fully inverted regions, as a result the channel resistance is either close to infinity or has a low value dictated by the device dimensions [10]. As it requires no drain-source or gate-source biasing to ensure linear operation of FET, it is conceived as a passive mixer.

The basic single resistor mixer can be assumed to have square-law behavior. It means only the second order non-linearity is desirable and the rest higher order terms must be absent in its operation [9]. A Square-law mixer can be realized with a long channel MOSFET transistor. RF and LO signal connected in series with proper dc biasing are applied to the gate input of the transistor. A tuned LC circuit IF load is used at the drain which ideally acts as a short circuit for LO frequency while maintaining a constant drain source voltage for full cycle of LO signal. The key benefit of this is that the unwanted spectral components can be easily filtered out as they are well beyond IF frequency.

It has a simple structure, good noise figure and conversion gain as well. The chief drawback of this type of mixer is its poor isolation at RF to LO and LO to RF ports isolation. Besides this, the amplification of the LO signal by the transistor, reduces LO-IF isolation. Moreover the matching the input with respect to both RF and LO frequencies is difficult to attain. Hence, the matching is performed for the RF signal only which increases LO requirements. As LO increases, isolation of this mixer decreases [9].

(b) Double Balanced Passive CMOS Mixer

It has capability of switching the RF signal directly in the voltage domain and therefore the voltage-to-current (V-I) conversion is not required. It comprises four CMOS switches connected in the form of a bridge. The LO signals are in anti-phase (LO+ and LO-) to ensure that only one diagonal pair of transistors turns ON at any point of time.

When M1 and M4 are on, V_{IF} equals $V_{RF,}$

when M2 and M3 are on, V_{IF} equals $-V_{RF}$.

The relationship between V_{IF} and V_{RF} can be written as the product of three time-varying products and a scaling factor [8]:

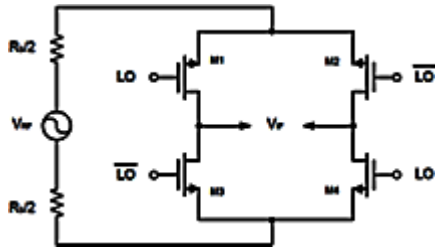

Figure 2.10: Double Balanced Passive CMOS Mixer

The conversion gain varies with type of applied LO signal i.e., square wave or sinusoidal wave.

For sinusoidal input, the conversion gain of the mixer is π/4 or -2.1 dB, and the conversion gain drops to 2/π (-3.92 dB) when a square wave is used [9]. The advantages of this mixer topology are its low power consumption, high linearity and low 1/f noise. Ideally, this mixer has no DC power consumption and 1/f noise. Typical SSB noise figure of 10 dB and IIP3 as high as 10 dBm can be achieved by using this mixer topology.

2.5.2 Active Mixers

2.5.2.1 Single Transistor Mixers

The simple single transistor mixer circuits can be operated in three standard modes of operation: transconductance, drain and resistive mixers [10].

(a) CMOS Transconductance Mixer (Gate Pumped Single FET Mixer)

The strongest nonlinearity parameter of a Field Effect Transistor is its transconductance (g_m), which can be utilized to perform mixing action. Figure 2.9 shows a single FET mixer. Analogous to a single diode mixer configuration, in CMOS transconductance mixer, both LO and RF signals are fed to the same port. The gate is biased close to the pinch off region where g_m tends to 0, to get a large change in g_m from a small variation in the gate voltage whereas in an amplifier the FET is operated in the saturation region.

When LO signals are applied to the gate of transistor, its gate source voltage V_{GS} changes, which in turn swings the transistor between saturation and cut-off regions of operation. Maximizing the LO frequency component of the transconductance waveform optimizes the conversion gain and linearity together with the noise figure.

Certain essential conditions must be ensured for proper mixing operation and maximizing transconductance as well. Firstly LO signal must be large enough so that it can pump g_m value between the high and low states. Secondly, the transistor is biased at the threshold voltage and with peak value of the transconductance equal to the maximum g_m and 50% duty cycle. This condition provides maximum conversion gain for the transconductance mixer [11]. Besides this, linear operation of FET is avoided by keeping a constant and adequately large value drain-source voltage.

Fourier series expansion of the transconductance containing harmonics of the LO frequency is given as [18]:

$$g(t) = g_0 + 2\sum_{n=1}^{\infty} g_n \cos n w_0(t) \tag{2.18}$$

The conversion gain (CG) of this single mixer is

$$G_C = \frac{{g_1}^2 r_o}{4{\omega_{RF}}^2 {C_{gs}}^2 r_g} \tag{2.19}$$

where r_o and r_g are the output and gate resistances of the FET respectively.

The main drawback of the gate pumped single FET mixer is the poor isolation between the RF and LO ports. It is due to the fact that the RF and LO frequencies are generally very close to each other (e.g. separated by several hundred MHz).Therefore very high Q value filter is required in order to distinguish the LO and RF signals. This problem can be solved by using drain-pumped or source-pumped configurations. In the drain-pumped and source-pumped configurations, FET is biased to operate in saturation region as opposed to the gate-pumped configuration.

(b) Drain Pumped Single FET Mixer

In this mixer, RF signal is fed through the gate whereas the LO signal is applied to the drain of the transistor. During operation, the drain-source voltage of the device is modulated by the LO signal. This variation in V_{DS} switches the transistor between linear and saturation regions of operation. The frequency mixing action is achieved by varying transconductance g_m, as well as drain-source conductance of the FET.

The drain-pumped configuration is shown in Figure 2.11. The isolation between RF and LO is often limited by the gate-drain capacitance C_{gd} of the transistor. This mixer provides higher LO-to-RF isolation, but the large LO signal causes poor LO-to-IF isolation [17].

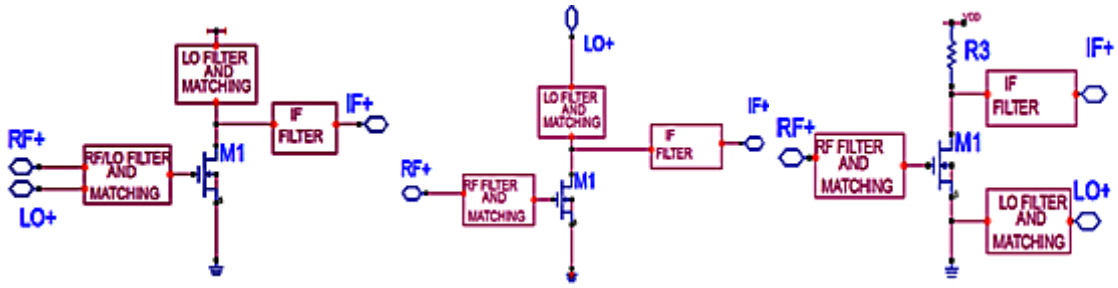

Figure 2.11: FET mixer (a) gate pumped FET mixer (b) drain pumped FET mixer (c) the source-pumped FET mixer

(c) Source Pumped Single FET Mixer

This is an alternate configuration to the drain pumped structure. In this topology, the LO signal is applied at the source of the FET. It provides better LO-to-RF port isolation and requires lower LO power because LO port can be matched to LO frequency [9]. The isolation among the RF, IF and LO ports is comparatively high in this configuration of single FET mixer.

2.5.2.2 Dual Gate Mixers

Dual gate mixer consists of two MOSFET$_S$ connected in a cascode configuration. The RF and LO signals can be connected to the different gates as opposed to the single gate mixer and hence better isolation can be achieved [19].

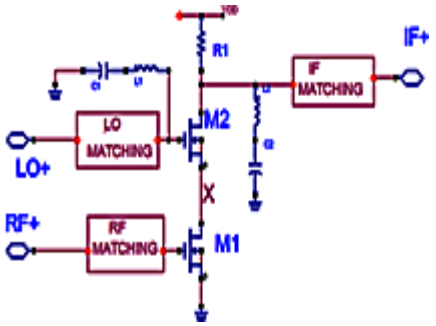

Figure 2.12*:* Dual-Gate Mixer

The second gate can be used for controlling the magnitude of small signal transconductance for the first gate device and hence transconductance gain of the FET which increases the performance of mixer by decreasing LO power requirement. This topology suits very well for CMOS technology because in this mixer configuration sharing of the source and the drain terminals of the two MOSFETs is possible because of cascade connection. This sharing reduces common junction capacitance. Moreover isolation between the RF and LO ports enables the designing of separate matching networks.

The mode of operation in which LO (Local oscillator) signal is connected to the upper gate and the RF signal to the lower gate is more appropriate as seen in previous studies [10-13].This mode improves the linearity because standard methodologies of port matching for RF port can be utilized. In addition, this mode provides better RF-IF isolation. The voltage at common node X i.e. drain voltage of transistor M1 is modulated by the applied LO signal. Thus, mixing of RF and LO signal takes place at node X, analogous to the operation of a single FET drain mixer.

The gate source voltage V_{GS} of the lower transistor Ml to which the RF signal is applied is approximately constant because of small magnitude of the RF signal. The drain-source voltage of M1 is modulated by LO signal which swings M1 between linear and saturation regions. Frequency translation takes place due to the variation in transconductance g_m, and drain-source conductance g_{ds} of Ml. Transistor M2 remains in current saturation for almost entire LO. We get a source follower amplifier (or common drain amplifier) configuration for LO signal and a common-gate amplifier for output IF signal simultaneously. The gate must be grounded for harmonics of IF signal which is achieved by connecting a series resonant circuit tuned to IF frequency as shown in Figure 2.13. Similarly, drain of M2 at LO frequency also needs to be shorted to ground potential. The short circuit maintains the constant drain voltage and ensures that M2 remains in saturation over most of the time.

The shortcomings of this mixer are inevitable as it uses passive components for rejecting LO signal and IF signal harmonics which are difficult to be implemented on RF integrated circuits at low frequencies. In addition, it reduces the conversion gain because of additional series resistance which may be present at the source terminal of lower MOSFET [9]. To avoid instability caused by LO transistor operating as common-gate amplifier, the dual gate mixer can doubly balanced. The double balanced dual gate mixer architecture increases port-to-port isolation and rejects the LO and IF port harmonics without employing passive resonant components.

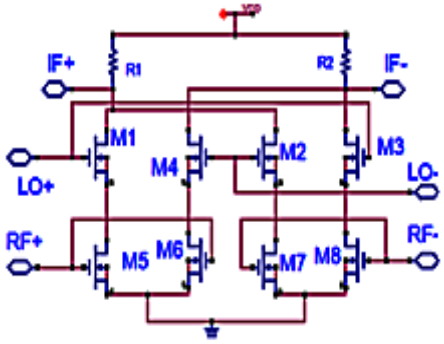

Figure 2.13: Double-Balanced Dual-Gate Mixer

2.5.2.3 Balanced Mixers

(a) Single Balanced Mixers

In single balanced mixer structure, the output IF signal is the differential of the two branch voltages, consequently IF feedthrough from one branch is cancelled by another [16]. In this architecture, transistor M1 forms the transconductance stage, M2 and M3 transistors form the switching stage and resistor R_L acts as the load of the mixer. For its operation, the incoming RF signal voltage is firstly transformed into a current signal by the transconductor M1 followed by the multiplication of signals in current domain. The magnitude of LO signal must be kept large enough for achieving alternate steering of current through LO transistors. This large LO signal (e.g. 0 dBm) therefore requires some amount of filtering to prevent overloading of the subsequent stages in the receiver chain. To ensure proper switching between off and on states at LO frequency, differential LO transistors must be biased somewhat above their threshold voltages [9]. As a result, when one of the LO transistors is ON, other remains off.

To obtain conversion gain, it is essential to bias the RF transconductor properly in saturation. Mixers performing multiplication of the two signals generally exhibit superior characteristics because they can ideally generate only the required mixing products. Since both the inputs signals are applied to the different ports, high degree of inherent isolation among the ports is obtained. Also Down-conversion mixers in general have LO short on the output IF port, which ensures the optimum intermodulation performance. The practical importance of LO short is that LO signal

is typically larger than the RF signal and therefore it is more amplified by the active devices.

Two configurations possible for obtaining differential LO signal are shown in the figure below [21]. In the first configuration, a balun is required at LO input for obtaining differential signal. Since point A is virtually grounded, no LO voltage can act upon RF FET drain. On the other hand, second configuration is simpler, as it eliminates the need of balun at the LO input but at the expense of conversion gain. In the second topology point A is not virtually grounded, consequently, an LO voltage component is added to the drain of RF transistor, which deteriorates the gain of mixer. Therefore the second topology is used only where balun installation is difficult [21].

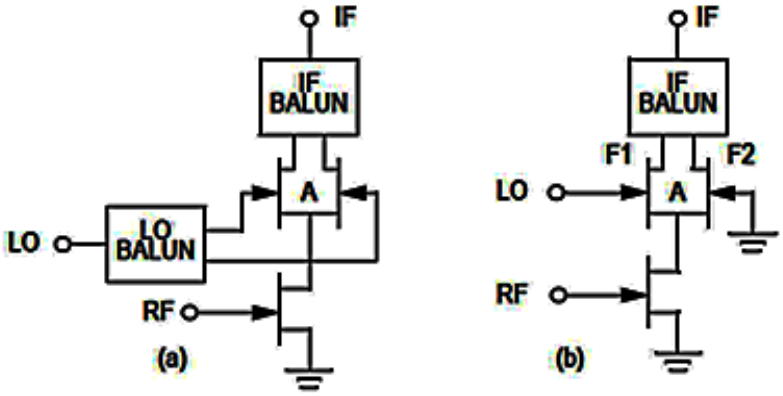

Figure 2.14: Two single balanced FET mixers: (a) conventional and (b) Configured [21]

The expression for output IF current can be obtained by treating the LO signal as a square wave consisting only odd harmonics of the LO frequency. Therefore, when RF current signal is multiplied with the odd-order harmonics of LO signal, certain mixing products are obtained at the output port. It means that the desired IF frequency is accompanied by some other frequency components given by $n\,(t) \times \omega_{LO}$, where n is an integer [16].

$$i_{IF}(t) = \mathrm{sgn}\left[\cos\omega_{LO}t\right]\left(I_{DC} + I_{RF}\cos\omega_{RF}t\right) \tag{2.20}$$

$$I_{RF} = -g_m V_{RF} \tag{2.21}$$

where g_m designates trans-conductance of transistor M1.ω_{LO} is the local oscillator frequency, I_{DC} is the tail current source, V_{RF} and I_{RF} are the RF signal voltage and the current respectively.

The Fourier series expansion of the LO signal (square wave) gives [9]

$$\mathrm{sgn}\left[\cos\omega_{LO}t\right] = \frac{4}{\pi}\cos\left(\omega_{LO}t\right) - \frac{4}{3\pi}\cos\left(3\omega_{LO}t\right) + \frac{4}{5\pi}\cos\left(5\omega_{LO}t\right)\ldots \tag{2.22}$$

By substituting equation 2.22 into 2.20, second order inter-modulation components can be obtained:

$$i_{IF}(t)_{IM2} = -\frac{2}{\pi} g_m V_{RF} \left[\cos(\omega_{RF} t - \omega_{LO} t)\right] + \cos(\omega_{RF} t + \omega_{LO} t) \quad (2.23)$$

Therefore, the voltage conversion gain (CG) of the mixer is:

$$CG = \frac{2}{\pi} g_m R_L \quad (2.24)$$

Even though the single balanced mixer requires two extra transistors, it has a simple and compact structure, so can be conveniently used at high frequencies. As observed in previous papers that, a single balanced mixer designed for 60 GHz applications implemented using 0.13 µm technology can provide a conversion gain of 10 dB with 18 dB NF by consuming only 0.9 mA current at 1.2 V supply voltage[14].

In [15], the single balanced mixer at 24 GHz achieved the power gain as high as 13dB with 17.5dB noise figure using 0.18µm CMOS technology. The current consumption reported for this mixer was 4mA of DC current with a 1.5 V supply. Single balanced mixer provides more isolation for RF-LO port than that of the single FET mixer. However its LO-IF port isolation is poor. From Equation 2.23, it is clear that the LO feed through at the IF output is $= \frac{4}{\pi} I_{DC} R_L \cos(\omega_{LO} t)$.

The amplification of the LO signal by the active devices further disrupts its operation [2]. Since the mixer is usually followed by an amplifier stage in a receiver, filtering becomes essential for suppressing LO portion of the output signal so that the amplifier may not get saturated.

(b) Double Balanced Mixer

The Double Balanced mixer is a combination of two single-balanced mixers and both the inputs LO as well as RF are differential. Though, similar in operation double balanced mixers operates over a wider range with considerable rejection of LO modulated noise and high port to port isolation. Besides this, they also avoid spurious responses that may occur at even order harmonic frequencies of RF and LO [22].

The disadvantages incurred by the use of double balanced mixers are higher power consumption and the requirement of baluns for each port. However active baluns having small physical area can be employed rather than distributed elements like transmission couplers. In addition, increased number of transistors not only increases the complexity of the circuit but also reduce its linearity. Figure 2.15 shows a double balanced mixer configuration with baluns connected at the input. A well known double balanced active FET mixer is a Gilbert cell mixer [22].

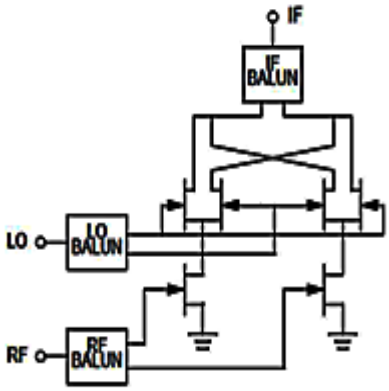

Figure 2.15: Double Balanced Mixer [21]

2.6 Gilbert Cell Mixer

The most popular and widely used active mixer is a Gilbert cell mixer which functions like a four quadrant multiplier. It essentially consists of two single balanced mixers with their outputs cross-coupled together in current domain [20].The RF and LO inputs are fed as well their corresponding IF output is taken in a differential manner. Although it consumes twice as much of power as a single balanced mixer, its excellent port to port isolation, compact structure, high conversion gain and spurious noise cancellation make it suitable to be used as microwave mixers [22].

It consists of two stages i.e., switching (LO) stage and the transconductance (RF) stage. For appropriate operation switching transistors must be biased in linear region and the RF transistors in the saturation region. More accurate balancing of the circuit can be obtained with the use of a tail current source but will consequently increase its power consumption also [21]. During its operation transistors M5 and M6 forming the transconductance stage of Gilbert cell converts the incoming differential RF signal voltage into current. Transistors pairs M1-M2 and M3-M4 forms the two cross-coupled switches which are activated by the differential LO Signal perform mixing of signal by current commutation.

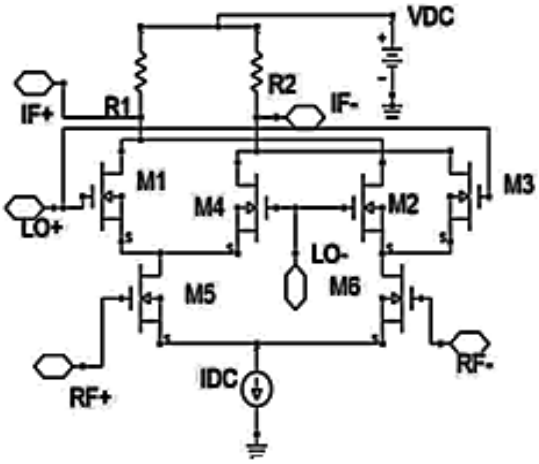

Figure 2.16: Gilbert Cell Mixer

The LO signal applied should be large enough to cause proper switching of current between the two pairs of switches and consequently achieving the desired change in polarity at the output. The RF current is therefore multiplied by an LO signal which is basically a square wave as in case of a single balanced [20] mixer. Qualitatively, it behaves as if two single balanced mixers are connected in anti-parallel configuration with reference to LO signal and parallel configuration for IF signal. As a result the LO signal get cancelled at the output whereas the IF signal comes out differentially [22].
In addition, the outputs are interconnected such that the drain of the LO transistors is virtually grounded for both RF and LO fundamental frequencies, thereby grounding their even order spurious harmonics as well [11].

It eliminates the need of additional circuitry required for LO and RF short at the drain of switching LO quad. Hence considerably high LO to IF isolation can be attained which relaxes the filter parameters required in the subsequent receiver stages. The chief drawback of the Gilbert mixer is its high power consumption due to increase in the number of devices and the necessity of maintaining the active devices in saturation. The current source required for biasing the circuit properly also increases the power consumption. Moreover, device mismatches and the lengths of the signal path followed often limit their port to port isolation and even harmonics cancellation at the output port. Quantitatively, the IF output voltage can be obtained by considering the fact that the two opposite branches of this double balanced mixer are out of phase by 180 degrees. For analyzing the circuitry one can use the superposition principle by which each of the branches is analyzed individually and then the system response is calculated as the difference of these individual responses.

$$I_{01} = I_1 - I_2 = I_{DC} + I_{RF}\cos\omega_{RF}t \tag{2.25}$$

$$I_{02} = I_4 - I_3 = I_{DC} + I_{RF}\cos\omega_{RF}t \tag{2.26}$$

$$I_{OD} = I_{01} - I_{02} = 2.I_{RF}\cos\omega_{RF}t \tag{2.27}$$

Assuming LO signal to be to be a square wave s(t), I_{OD} switching between the LO transistors becomes $2.I_{RF}\cos\omega_{RF}t.s(t)$
Therefore output IF voltage is given by

$$V_{IF} = \frac{4}{\pi} I_{RF}\left[\begin{array}{l}\sin(\omega_{LO}-\omega_{RF})t + \sin(\omega_{LO}+\omega_{RF})t + \\ \frac{1}{3}\sin(3\omega_{LO}-\omega_{RF})t + \frac{1}{3}\sin(3\omega_{LO}+\omega_{RF})t + \ldots\end{array}\right] R_{LOAD} \tag{2.28}$$

From above equation, the resultant Conversion gain will be

$$CG = \frac{2}{\pi} g_m R_{load} \tag{2.29}$$

where CG is the conversion gain, g_m is the transconductance and R_{load} is the load resistance.

The gain equation thus obtained is the maximum conversion gain that a double balanced mixer can achieve under ideal switching conditions. However, in real circumstances perfect switching is not possible. Therefore for some time interval both of the MOS switching pairs are ON and behave like differential amplifiers. It occurs when $|V_{LO}|$, the magnitude of the LO voltage signal is less than the maximum value of input voltage i.e,

$$|v_{in}|_{\max} = \sqrt{2}(V_{GS} - V_T) \tag{2.30}$$

Thus, the Conversion gain which takes these non linearities into consideration may be expressed as:

$$CG \cong \frac{2}{\pi} \frac{\sin(\pi f_{LO} t_s)}{\pi f_{LO} t_s} g_m R_{load} \tag{2.31}$$

The nonlinearities due to switches can be mitigated by two methods so as to get the maximum conversion gain. First method is to increase the LO drive but it might cause the steering of transconductor transistors into the triode region, consequently degrading its gain as well as linearity. Second method is to lower the magnitude of switching voltage $|Vin|_{max}$. Since $|Vin|_{max}$ depends on the gate overdrive V_{GS}-V_T, reduction in its value lowers the switching time t_s and therefore ideal switching conditions are obtained. However for low power applications, lower LO drive method can also be exploited [5, 23].

The linearity is mainly influenced by the switches, tail current source and the trans-conductance stage. The effect of imperfect switching on the linearity was obtained as the summation of the inter-modulation distortion caused due to the switches and the transconductors. The small value of switch ON voltage and the large LO drive is required for reducing such nonlinearities. However, too large value of LO power could increase non linearities due to capacitive loading at the common source nodes [24] of the switching pairs. For proper switching moderate power level of the LO signal must be ensured. Trans-conductors also affect the IIP3 of mixer circuit, for which linearity enhancement techniques like LNA can be employed. The techniques that are popularly used in Gilbert mixer are source degeneration and current bleeding (current injection). Source degeneration uses an inductor or a resistor at the source of trans-conductor transistors whereas in current injection technique, drain current in RF transistors is increased without disturbing bias voltage at the drain of LO transistors.

2.7 Implemented Loads for Double Balanced Gilbert Mixer

Various performance metrics are influenced by the use of different loads in the double balanced Gilbert Mixer design. In this section, a brief introduction of loads to provide

the background for some previous implementations of loads for this mixer configuration are investigated and their effects on mixer parameters are discussed.

2.7.1 Passive resistor load

As discussed earlier, the voltage gain of Gilbert cell mixer mainly depends on the transconductance g_m of the RF transistors and the load resistors and is generally given as:

$$Voltage\ Gain = Kg_m R_L \tag{2.32}$$

where R_L is the load resistor, g_m is the trans-conductance of transistors M1 and M2and K is the process trans-conductance of the FET.

Due to the presence of three stacked transistors in Gilbert mixer, the limitation imposed on the value of load resistor is given by:

$$R_L = \frac{2(V_{DD} - 3V_{DS(SAT)})}{I_{BIAS}} \tag{2.33}$$

where V_{DD} is the applied supply voltage, I_{BIAS} is the tail current for the mixer core, $V_{DS(SAT)}$ is the drain –source voltage in saturation for the transistors.

Also, the transconductance of the transistors given by

$$g_m = \mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{TH}) = \frac{2I_D}{(V_{GS} - V_{TH})} = \frac{I_{BIAS}}{(V_{GS} - V_{TH})} \tag{2.34}$$

It is to be noted that on increasing the I_{BIAS} current, g_m also increases but it will but to satisfy equation (2.34) value of the load resistor must be reduced. It means that there must be an optimized value for the bias current and the resistive load which can provide the maximum gain [25].

Polysilicon resistors when used as the load provides the mixer operation free from flicker noise but they are voltage hungry i.e, require additional voltage headroom [25] due to which the low voltage operation of the circuit is limited. The circuit can work with low voltage supply only if the bias current of the mixer is reduced [47]. In CMOS technology, resistors with strictly controlled value and reasonable physical size are difficult to fabricate [*45*]. Therefore, the use of resistor loads is usually reserved for less demanding applications where wide bandwidth is the important requirement [46].

To increase the linearity of the mixer various techniques have been proposed by researchers Techniques such as current injection and folded configuration can be employed for increasing the value of load without significant loss in voltage

headroom but the power consumption and the area requirement of the circuit will increase. One more technique called source degeneration uses either a resistor or an inductor at the source of RF transistors. The use of inductor for source degeneration is limited as it requires larger implementation area on chip and with its use gain of the mixer decreases with increase in frequency. So, resistive degeneration is generally used. The use of degeneration further limits the size of the load resistor R_L, which can be expressed as:

$$R_{LOAD} = \frac{2\left(VDD - \frac{I_{BIAS}}{2} R_S - 3V_{DS(SAT)}\right)}{I_{BIAS}} \tag{2.35}$$

where Rs is the degeneration resistance at the source, I_{BIAS} is the tail current ,$V_{DS(SAT)}$ is the drain-source voltage in saturation mode, V_{DD} is the supply voltage and R_{LOAD} is the load resistance.

2.7.2 Inductive load

The use of active inductors is very helpful in maximizing conversion gain and power output, but since the inductors are often chosen for their ability to "resonate out "other capacitive components in the circuit, such mixer are often narrowband in performance [27]. It means where wide band operation is desired inductor load cannot be used. Moreover they are very bulky requiring larger area and their desired accurate value is also difficult to obtain. However it does not consume the voltage headroom as in case of resistive load and are generally used for high frequency applications. If an inductor load is tuned to output IF frequency in a single balanced mixer, its LO frequency can be attenuated due to the LO feedthrough at the output may saturate the subsequent receiver stages. However if the IF frequency is high, sharper transition band of the LC load filter is required to eliminate LO feed through effect [28].

With balanced output load, either it is resistive-capacitor (RC) load. Resistor inductor (RL) load or a combination of three (RLC) symmetrical output waveforms are obtained [29]

2.7.3 RLC tuned load

The input to the down conversion mixer used at the receiver end has a broad band and it needs to produce a fixed IF frequency at the output. Therefore gain is desirable only over a narrow band of frequency which is centered around the IF frequency. The chief advantage of using a tuned load is that it removes the headroom limitation. It can provide a larger output swing at the output because at DC ,the inductor in the tuned RLC load get shorted and hence there is no voltage drop across it which results in the more room to design the circuit. At the resonance frequency of the tank both the inductor and capacitor are open circuited and therefore the gain of the mixer becomes g_mR. The admittance function of the RLC load can be given as:

$$Y = G + j\omega C + \left(\frac{1}{j\omega L}\right) = G + j\left(\omega C - \left(\frac{1}{\omega L}\right)\right) \tag{2.36}$$

As observed from the equation 2.36, the admittance tends to infinite value at low as well as high frequency. It is because at low frequencies inductor is short circuited while at high frequencies, the capacitor. However at resonance frequency of the tank circuit admittances due to both get cancelled and the resultant admittance Y = G.

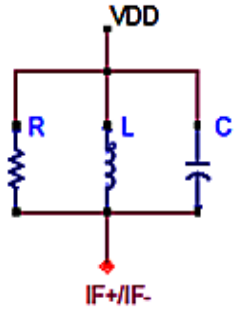

Figure 2.17: RLC Tuned Load

The resonance frequency is expressed as

$$\left[\omega_0 C - \left(\frac{1}{\omega_0 L}\right)\right] = 0$$
$$\Rightarrow \omega_0 = \frac{1}{\sqrt{LC}} \tag{2.37}$$

and the bandwidth $B = \frac{1}{CR}$ [26] (2.38)

The tuned is basically used to get more voltage headroom at the RF and IF ports for the down-conversion mixer. Since, the mixer designed using tuned circuit remains under the required power consumption; current can be increased with ease. Another important advantage that it offers is that its off-chip designing is possible and if the IF output is fed to an off-chip filter, small sized mixer can be designed.

2.7.4 LC tuned load

The parallel LC tank circuit acts as a band-pass filter. When it is used as a load in a down-conversion Gilbert mixer, it rejects out all products except that occurs around IF frequency. Otherwise, the signal obtained by addition of LO frequency and RF frequency may get mixed with the signal at their difference frequency. It means in addition to the desired signal, an image signal is also present at the mixer output.LC load can be used for narrow band operation only but it takes less headroom as compared to the passive resistor load [30].

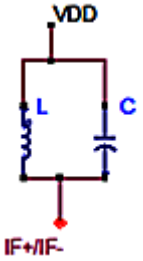

Figure 2.18: LC Tuned Load

2.7.5 PMOS load

If passive load is replaced by an active load (i.e., load realized using MOSFETs), it can significantly reduce the required chip area as well as can yield higher gain for a mixer. The higher conversion gain with active loads is achieved due to its higher small signal resistance.

As seen in equation 2.33 for a passive resistor load there is a limitation on its maximum value. If an active lad is used instead of a passive load then equation 2.33 is not applicable and the minimum voltage supply is decided by drain-source voltage of the transistor and is given by $V_{DDmin} = V_{DSsat}$

An active load can be implemented using **diode connected MOS** (i.e. gate of MOS transistor is connected to the drain of transistor). In this load gate and drain are always at same potential so the transistor used always operation in saturation mode.

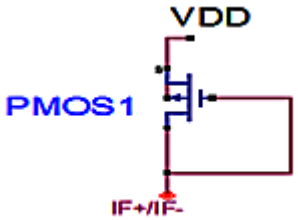

Figure 2.19 PMOS load

The resistance offered by this MOS diode is given by-

$$Rd = \frac{1}{g_m} \tag{2.39}$$

where gm is the transconductance of the MOSFET and R_d is the drain resistance.

This configuration when used as load generally tends to achieve larger bandwidths but has lower gain because it has relatively lower value of output impedance [34]. A PMOS transistor is preferred to an NMOS transistor because it produces less flicker noise compared to same sized NMOS transistor.

Current source load

The diode connected load offers a small and fixed value of resistance. To obtain the large value of resistance, size of the MOS transistor is required to be increased but it will limit the swing of output voltage. The resistance of the MOS diode can be varied by changing the current flowing in the Gilbert cell but will also change the biasing. A current source load can provide high drain resistance in saturation and is expressed as:

$$R_{ds} = \frac{1}{\lambda I_{ds}} \tag{2.40}$$

where λ is the channel length modulation factor and Ids is the drain current in the current source load. The output resistance is modulated by the drain current through the transistor which is controlled by the gate voltage. It can provide variable resistance of high value without any restriction of the unique bias point requirement [34].

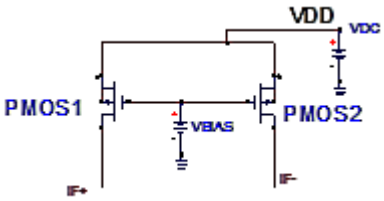

Figure2.20 Current source load

Triode load

MOS resistor when operated in the deep triode region can behave as a resistor. The linear operation of the PMOS is ensured by applying a suitable bias voltage at its gate. The gate voltage applied must be sufficiently low for its operation in triode region so that full output voltage swing is obtained. It provides a unique bias point for a range of input gate voltage [34].The resistance at the drain of a triode load is given by:

$$R_{ds} = \frac{1}{\mu C_{ox} \frac{W}{L}(V_{GS} - V_{TH})} \tag{2.41}$$

Where μ is mobility of holes (electrons) for PMOS (NMOS), C_{OX} is the gate capacitance per unit area, V_{GS} is the gate-source voltage, V_{TH} is the Threshold voltage of transistor and W and L represents the width and the length of the transistor [34].

It takes a voltage headroom of V_{DSmin} which can be as small as 200mV.The drawback involved with the use of active loads is the introduction of additional noise in the mixer circuitry which causes increase in its the noise figure.The effect of flicker noise on the mixer output can be given as:

$$V_{O,n}^2 = 8kTR_L\left(1 + \gamma\frac{2R_L I_{BIAS}}{\pi A} + \gamma\frac{g_m I_{BIAS}}{2(V_{GS} - V_{TH})}\right) \tag{2.42}$$

Where $V_{O,n}$ is the noise voltage at the IF output, k is the Boltzman's constant, T is the absolute temperature in Kelvin, R_L is the load resistance, A is the LO amplitude and γ is the channel noise factor.

They also require additional circuitry to stabilize them against the variations due to voltage, temperature or process technology used, by providing a stable bias circuit [25].

2.7.6 Resistor connected diode connected load

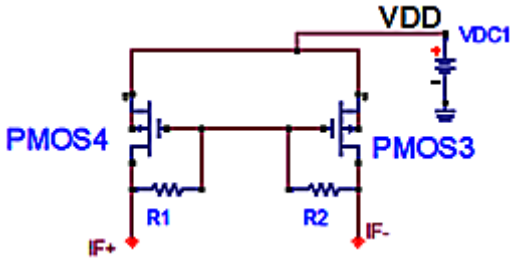

Figure 2.21: Resistor connected diode connected load

In this configuration of load PMOS transistors are used for providing high output impedance and conversion gain of the mixer while two extra identical resistors R1 and R2 are employed for providing differential outputs of the mixer at same DC voltage [31]. By using this load, the drawback of voltage headroom involved with the direct use of resistor is exempted because only voltage drop equal to VDS min is required as in case of simple PMOS load [32]. The resistors provide the required conversion gain to the mixer but the area on chip is increased by the use of passive components.

2.7.7 Resistor connected diode connected load with a current source

The current source at the gate in a resistor connected diode connected load sets the output voltage to a fixed required value.

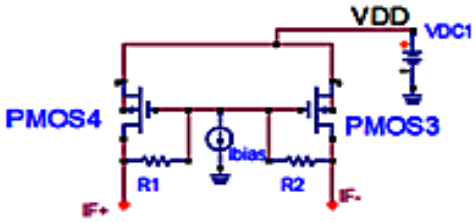

Figure 2.22: Resistor connected diode connected load with a current source

2.7.8 Resistor connected diode connected load with capacitor

RC circuit is also sometimes employed for mixing the proper bias in a resistor connected diode connected load [33].

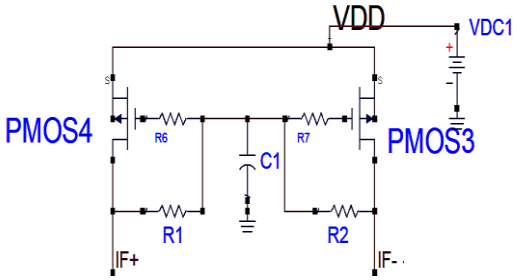

Figure 2.23: Resistor connected diode connected load with capacitor

2.7.9 Current mirror load

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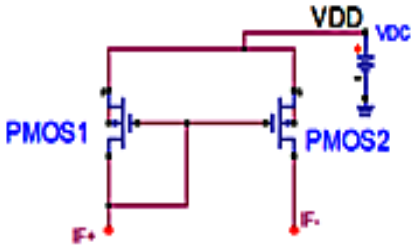

Figure 2.24: Current Mirror load

Current mirror can provide higher conversion gain (due to high output impedance) but at the expense of bandwidth [34].

Chapter 3
Gilbert Mixer Designing

3.1 Introduction

In chapter 2, different structures and configurations of CMOS mixers have been discussed. The evaluation of performance of all the structures is necessary in order to determine the most suitable for designing. Therefore initially one configuration is selected and is considered as the reference design and then its performance characteristics like conversion gain, noise figure, linearity, port to port isolation, power consumption etc are optimized. This reference design then can be utilized for comparing performance of other mixer structures. In the work presented, double balanced Gilbert cell CMOS mixer is chosen as the reference topology because it offers superior and spurious free performance compared to others designed so far.

The designing of the mixer is performed using 0.18μm CMOS technology with Agilent's Advanced Design System as tool for simulations. The first step required for the on-chip implementation of the CMOS mixer is to obtain the models for the MOS transistors, so they were imported into the design from MOSIS. The datasheets for various MOS models were studied to grasp the information regarding their operating ranges, supply voltage required, unity gain frequency etc and thereby the power constraints of various CMOS technologies were determined. For operating the mixer in the GHz range of radio frequencies, designing of impedance matching circuitry is a cumbersome task. However, the problem was resolved by employing baluns at the three ports of the mixer i.e., RF, LO and IF ports. Fabrication of on-chip inductor is also difficult, therefore small value inductors fabricated using CMOS technology could only be used in the design.

3.2 Design Guidelines

Device Sizes and Bias Currents

As the conversion gain (CG) and the noise figure (NF) of the mixer depends upon the trans-conductance g_m of RF transistors, their sizes must be selected properly. The width must be chosen to provide high gain, low noise so as to attain saturation at low drain –source voltage (to reduce the supply voltage requirement).

The transistors used in LO and RF stages should have minimum channel length in order to obtain higher operating frequencies of the transistors. This is because transistor's switching speed is limited by their unity gain frequency f_t. The widths of the RF transistors must be large for higher conversion gain but must not

have very large value otherwise their gate –source capacitances would increase. These capacitances increases noise figure of the transistor and limit the circuit's operation at high frequencies. The optimum width which satisfies both power and the noise constraints of the circuit can be determined from device model parameters.

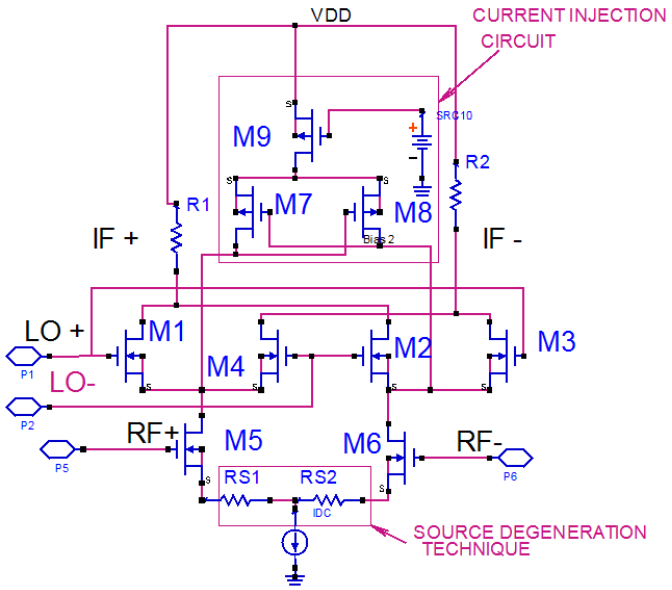

Figure 3.1: Double Balanced Gilbert Mixer Employing Source Degeneration and Current Injection Techniques

Linearity of Signal Path:

(a) Source Degeneration Technique: After fixing the proper bias voltages and currents, linearity of the signal path is ensured. For enhancing linearity of the mixer, source degeneration resistors or source degeneration inductors are added. If a passive resistor is used, mixer becomes almost linear because of the increase in the range of input voltage but the gain is reduced. Degeneration inductor could stabilize the circuit by adding a real and positive component to input impedance and therefore helps in impedance matching also. Capacitive degeneration could not be employed because it introduces a negative resistance $g_m Zs$ into the input impedance which leads to oscillatory behavior. Degeneration inductor best suits to linearity requirement with increasing frequency but gain of the mixer starts decaying and it requires more area on chip as well. The Q factor of the on chip inductor is mainly limited by the metal losses and conduction through substrate occurring in bulk silicon technology. Ordinary digital IC possesses spiral inductors with low Q factor.

(b) Current Injection Technique: In the mixer circuit, RF transistors operate in saturation and therefore their conversion gain and IIP3 is given by $CG = \frac{2}{\pi} R_L \sqrt{K_N I_D}$ and $IIP3 = 4\sqrt{\frac{2}{3}\frac{I_D}{K_N}}$, where $K_N = 2\mu_n C_{ox} \frac{W}{L}$. Both CG and IIP3 are directly

proportional to the square root of the bias current. It seems that both can be simultaneously increased by enhancing this current. However practically with increase in bias current, voltage drop across the load resistor increases, which disturbs the operation of LO switches. To eliminate this drawback, drain current of RF transistors is increased without increasing the current through the switching transistors by using current injection or current bleeding technique as shown in Figure 3.1.Transistors M7 and M8 are used for injecting a dynamic current which is equal to the bias current in the switching pairs, when switching takes place and thereby enhancing the linearity of the path [34].

The next step followed in designing the Gilbert cell mixer is the tuning of the drain nodes for the load of our choice so as to get the desired parameters at the output. Various loads offer certain special characteristics as discussed in section 2.7. For example, LC tuned load provides resonance at the IF frequency, if properly tuned. The improved conversion gain can be achieved, if the inductors with appropriate Quality factor are employed.

3.3 Mixer Design Optimization

Though an automated flow of designing the Double balanced Gilbert Mixer is hard to achieve, here in this section the systematic procedure followed for designing the mixer circuit is described. At the very first step of mixer design, a current mirror circuit is constructed which gives the nearly constant magnitude of current over a wider range of voltage. Designing of current mirror is performed under two constraints. Firstly, the tail current as it decides the conversion gain of the mixer. Secondly, the least possible overhead voltage that should be maintained to avoid variation in tail current. If any of these parameters causes substantial deviation in the tail current in any part of the mixer, parameters fixed for other parts will differ from the actual design, making the process complicated.

The tail current along with the minimum overhead voltage thus obtained is utilized to calculate the sizes of the transistor and to figure out the dc biasing required for trans-conductor. This ensures operation the trans-conductor in the saturation region with a certain margin for variation in the range of drain voltage. Since the transistor sizes of trans-conductor depends on the conversion gain, linearity and the noise figure, they must properly chosen. Initially, linearity and the conversion gain are considered for designing and later on the mixer is optimized for noise figure also.

The range up to which the drain voltage can be varied is limited by the variation due switching of LO transistors. After that, bias voltage for LO transistors and their sizes are determined. The W/L ratios of the commutating switches must be small for reducing the noise voltage while the tail current fixed previously requires their larger values. Higher aspect ratios of switches are desired to keep the residual

gate-source voltage at a minimum value, so that smaller LO voltage can operate the switches, thereby reducing the power consumption. This will assure more ideal switching which otherwise could reduce the gain or might induce more noise. As for trans-conductors, switches are made to work in saturation by considering variations in their gate –source voltage, tail current and the drain voltage. The variation range of voltage at the drain of switches must be largest possible to have distortion free wider variation of IF signal. Now the device sizes and their required biasing voltages for the loads are determined. Loads are also designed to provide the maximum variation range of output IF signal.

Subsequently, the matching networks for both the input ports (RF and IF), are designed so that maximum power is transferred from source to the mixer. If reasonable NF is not obtained from the design, RF port must be impedance matched properly.

Finally circuit is checked for conversion gain, intermodulation distortion and the noise figure and if any of the performance parameter is not proper, procedure is repeated. These are the basic steps for the Gilbert mixer design. Because of the tradeoffs involved, the design procedure as a whole is the optimization of mixer parameters.

Table 3.1: Specifications for designing the mixer

Parameters	Specification	Units
RF Frequency	2.5	GHz
Voltage Gain	>8	dB
Noise Figure (SSB)	< 10	dB
Input IIM3	>10	dBm
Power consumption	<20	mW
Load Impedance	500	ohms
Voltage Supply	1.8	V

3.4 Design Procedure

The mixer is designing is based on the application for which it is to be employed, which in turn decides the figure of merit of particular importance. In some applications, lowest possible noise figure is desired while in the other the high conversion gain and in another higher linearity.

To design the mixer for a specified conversion gain of 8dB, firstly we obtain the value of g_m by rearranging the equation

$$\frac{V_{RF}}{V_{IF}} \approx \frac{2}{\pi}\left(\frac{R_L}{R_S + \frac{1}{g_m}}\right) \tag{3.1}$$

It is the voltage conversion gain of the mixer by employing source degeneration technique. Therefore, g_m of the RF transistor is given by

$$g_m = \left[\frac{2}{\pi}\frac{R_L}{CG} - R_{S.}\right]^{-1} \tag{3.2}$$

With this calculated value of g_m, width W of the transistor is obtained considering L to be the minimum channel length which in our case is 0.18μm.

Since we know

$$g_m = \sqrt{\frac{2K_N W I_D}{L}} \tag{3.3}$$

Rearranging this equation and assuming the drain current to be 3mA we get

$$W = \frac{g_m^2 L}{2K_N I_D} \tag{3.4}$$

Where $K_N = \mu_N C_{OX}$ is the process transconductance.

$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$ Gate oxide capacitance; ε_{ox} is the permittivity of the free space and t_{ox} is the thickness of the oxide and $\mu_N = \mu_0 + 2.\theta.V_{sat}.L$

From model parameters μ_0 =265.18cm^2/V-s, V_{sat} = 1.0179 × 10^5 m/s, θ = 0.5

However, initial simulations are performed with this chosen value, proper switching of the LO transistors are ensured by setting up the gate overdrive voltage between 200mV and 400mV, for that matter, g_m is obtained from equation:

$$g_m = \frac{2I_D}{(Vgs - V_T)} \tag{3.5}$$

However, for low noise figure we need to choose an optimum gate width

$$W_{OPT} \approx \frac{1}{3\omega L C_{OX} R_{Source}} \tag{3.6}$$

Baluns are used for unbalanced to balanced (or single ended to differential) transformation at RF and LO inputs as well as for balanced to unbalanced transformation at the IF output terminals in simulations.

For a balun transformer $$\frac{Z_O}{Z_{in}} = \left(\frac{N_S}{N_P}\right)^2 \quad (3.7)$$

N_s and N_p are the number of turns in secondary and the primary winding respectively.

3.5 Proposed Ultra Low Power Diode load for Gilbert mixer

Two configurations of diode using MOSFET transistors are shown in Figure 3.2. Figure 3.2(a) shows the standard MOS diode with its gate and drain at the same potential. If this diode is reverse-biased, the source of the MOS appears to be connected to the gate. The leakage current that flows is thus characterized by the drain current under the condition V_{gs} = 0 V and $+V_{bs} = -V_D$ (where -ve sign shows the voltage applied to the diode when biased in reverse direction) [40].This leakage current causes considerable increase in power consumption of the circuit. Although, increase in V_{th} of the transistor can reduce the leakage current but will consequently lead to its poor forward drive capability.

ULPD shown in Figure 3.2(b) consists of a combination of NMOS and PMOS transistors, in which gate of NMOS transistor is connected to the source of PMOS transistor and vice versa. When compared to standard MOS diodes, ULP diode has capability of reducing the leakage current strongly while maintaining the similar forward current drive.

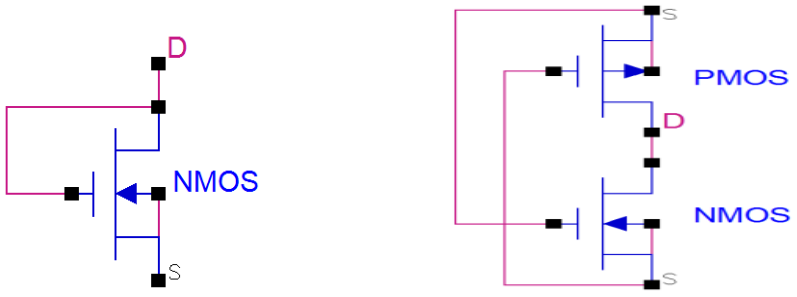

Figure 3.2: (a) Standard MOS Diode (b) Ultra low power diode

When ULPD is in forward mode, it can be regarded as two forward biased standard NMOSFET and PMOSFET connected in series and therefore it has forward current comparable to that of a standard diode in reverse biased mode [40]. As sources of NMOS and PMOS appears to be connected together as well as both operate with negative voltages, their leakage current is small. It operates in moderate or weak inversion regions, depending upon the device thresholds. An important feature of

ULPD is its ability to serve as a resistor by operating the transistors in the linear region [42-48].

The equivalent impedance of ULPD at high frequencies for small input signal is given as-

$$Z(s) = \frac{R + sX}{As^2 + Bs + C} \tag{3.8}$$

As observed in above expression, the Impedance of the ULPD load is a second order function with two poles and a zero. R and X denotes the real and imaginary parts of the zero respectively. A, B and C are the positive coefficients which can be expressed as:

$$R = r_{o1} + r_{o2} \tag{3.9}$$

$$X = (C_{gd1} + C_{gd2})(r_{o1} + r_{o2}) \tag{3.10}$$

$$A = (C_{gd1} + C_{gd2})(C_{gs1} + C_{gs2} + C_{gd2})(r_{o1} + r_{o2}) \tag{3.11}$$

$$B = (C_{gs1} + C_{gs2})(r_{o1} + r_{o2}) + C_{gd1} r_{o2}(1 + g_{m1} r_{o1}) + C_{gd2} r_{o1}(1 + g_{m2} r_{o2}) \tag{3.12}$$

$$C = 1 + g_{m1} r_{o1} + g_{m2} r_{o2} \tag{3.13}$$

Here r_{01} and r_{02} are drain source output resistances, g_{m1} and g_{m2} are transconductances, C_{gs1} and C_{gs2} are gate-source capacitances and C_{gd1} and C_{gd2} are the gate-drain capacitances of the NMOS and PMOS respectively. The additional zero introduced by load enhances the bandwidth of the mixer. As observed in [40], the leakage current is remarkably reduced in ULPD which for a MOS diode exists in nano-amperes range at zero V_{GS}, which dominates with back gate effect in reverse mode [43-44].

ULPD finds applications in level keepers in MT-CMOS circuits, charge pumps [41], memory cells [40] etc. In this paper, it is used as load in Gilbert Mixer.

Chapter 4

Results and Discussions

4.1 Gilbert Cell mixer using Source Degeneration

The simulations have been performed by designing and optimizing the mixer circuit with resistive load for Conversion Gain as well as linearity. For observing the performance of the circuit with the various loads, whole mixer circuit including device sizes, voltage supply and the input power levels is maintained and only load stage is varied. The load stage is optimized such that we get maximum conversion gain without significant loss in linearity.

Table 4.1: Simulation parameters

Parameters	Values
RF Frequency	2500 MHz
LO Frequency	2250 MHz
IF Frequency	250 MHz
RF power	-30 dBm
W/L for transistor	20µm/0.18µm
Supply voltage	1.8V
Tail current	6mA

4.2 Passive Resistor Load and Resistive Source Degeneration

The circuit is simulated with passive resistors as loads on each branch of the double balanced Gilbert mixer. The resistor chosen is of 500 Ω each. Though circuit can provide higher gain with higher value of resistor but it will cause a loss in linearity also. Therefore optimized results for both parameters have been achieved with this value. 10 Ω resistors are used for source degeneration in transconductor.

Table 4.2: Simulation results for passive resistor load based mixer

Conversion Gain (dB)	Input IM3 (dBm)	Output IM3 (dBm)	NF_{SSB} (dB)	NF_{DSB} (dB)	IIP3 (dBm)
10.286	4.473	14.759	8.252	4.828	14.195

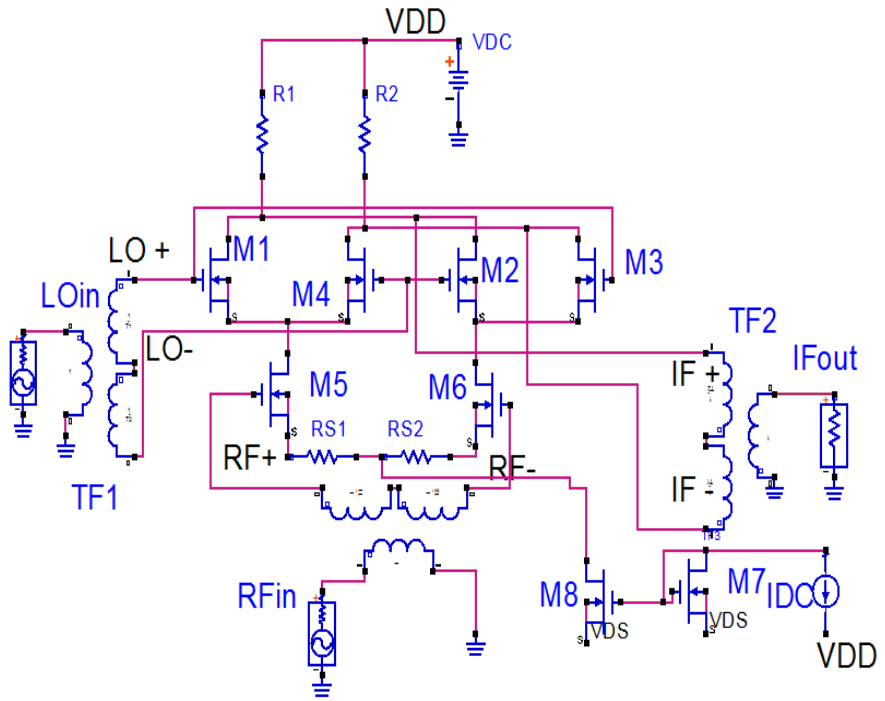

Figure 4.1: Double balanced Gilbert mixer with resistive source degeneration

Table 4.2 shows the various parameters obtained from the simulation of Gilbert mixer where IM3 denotes the third order inter modulation product. NF_{SSB} and NF_{DSB} are the Single Side Band and Double Sideband Noise Figures respectively. IIP3 designates the Input Third Order Intercept Point of the mixer and P_{DC} is the average power consumption of the mixer core circuit expressed in milliwatts (mW).

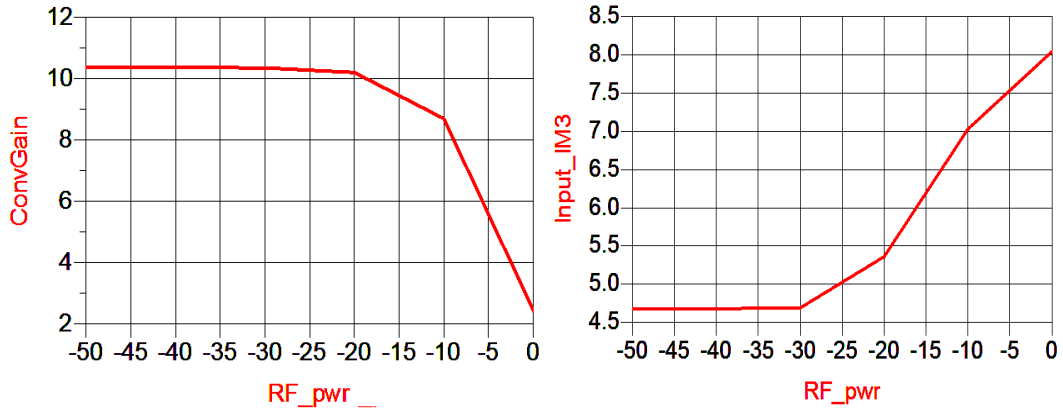

Figure 4.2: Conversion Gain (dB) versus RF Power (dBm) and Input IM3 (dBm) versus RF Power (dBm)

The variation of the conversion gain with input RF power is shown in Figure 4.2. The mixer has achieved the maximum conversion gain 10.358 dB which maintained its constant value up to -20 dBm, beyond which the gain is decreasing with increase in RF power. Figure 4.2 also shows that below -30 dBm RF power, IIP3 is ~4.69 dBm and then there is nearly linear increase in the IIP3 which attains is maximum value ~8.04dB.

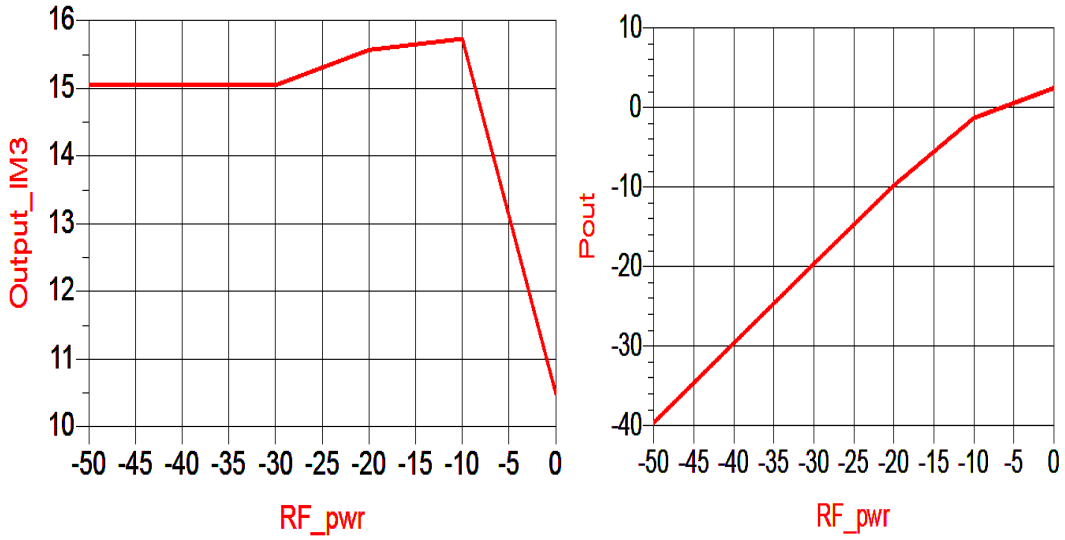

Figure 4.3: Output IM3 (dBm) versus RF Power (dBm) and Pout (dBm) versus RF Power (dBm)

The simulated plot for Output IM3 is shown in Figure 4.3.The plot is almost constant at 15.047 dBm OIM3 and then increases up to 15.731dBm at -10 dBm RF power and then starts decreasing linearly. The output power versus RF power plot shows that IF power at the output almost increases linearly with increase in input power. Output power at -30dBm RF power for which the parameters given in Table 4.2 are obtained is -19.64 dBm.

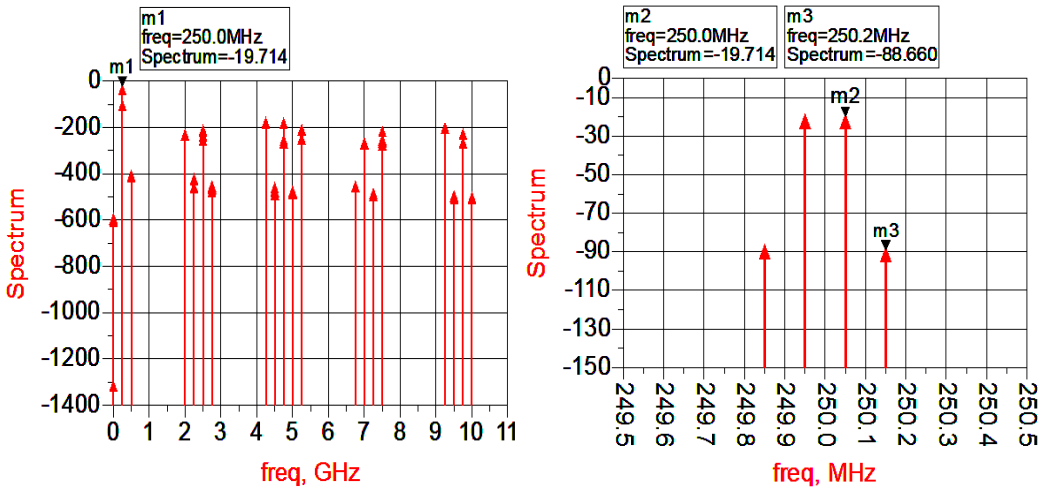

Figure 4.4: Broadband spectrum at output IF port and Spectrum near IF frequency

Figure 4.4 depicts the broadband spectrum of output IF port which has the maximum value at the desired IF frequency. Simulation of spectrum near IF frequency (second plot) shows that peak amplitude is obtained at the wanted intermediate frequency whereas other frequency components are significantly suppressed.

Figure 4.5 shows the variation of conversion gain (in dB) with RF frequency (in GHz). The positive conversion gain is obtained from 250 MHz to 10 GHz with maximum value ~10.57 dB at 1.7 GHz. The IIM3 simulation with respect to RF frequency is shown in Figure 4.5. It can be observed that IIM3 is greater than 4 dBm for the entire frequency range 1 GHz to 10 GHz and is greater than 2 dBm for lower range also. Its maximum value is 10.892 dBm at 5.3GHz.The output IM3 is maximum at 5.1 GHz with 17.806 dBm magnitude and is above 12 dBm upto 7.6 GHz.

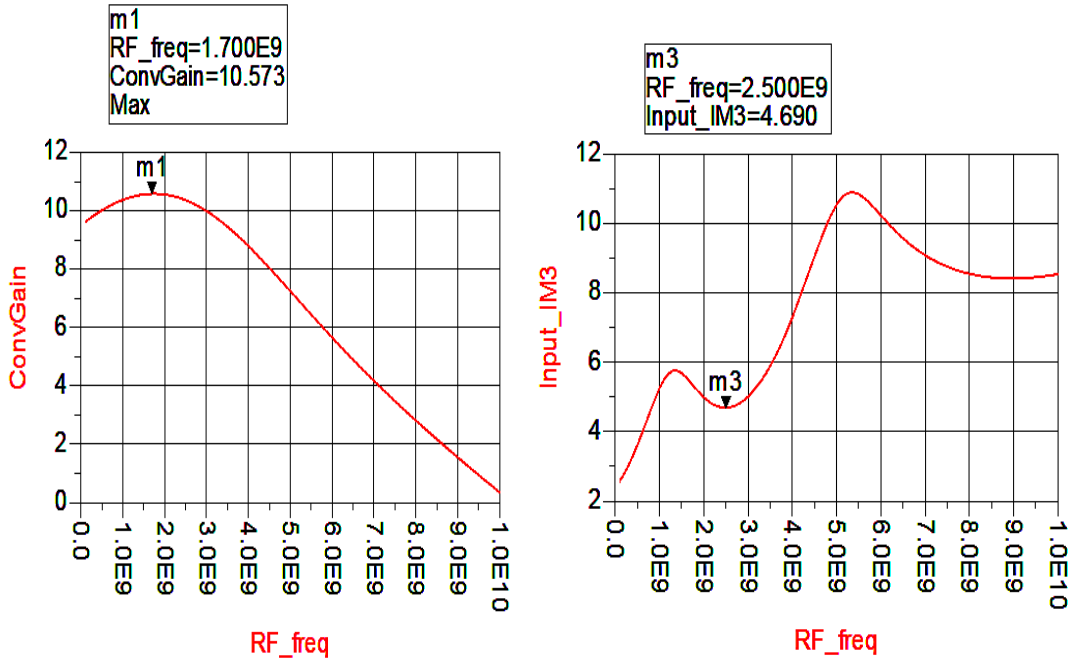

Figure 4.5: Conversion gain (dB) versus RF frequency (GHz) and Input IM3 (dBm) versus RF frequency (GHz)

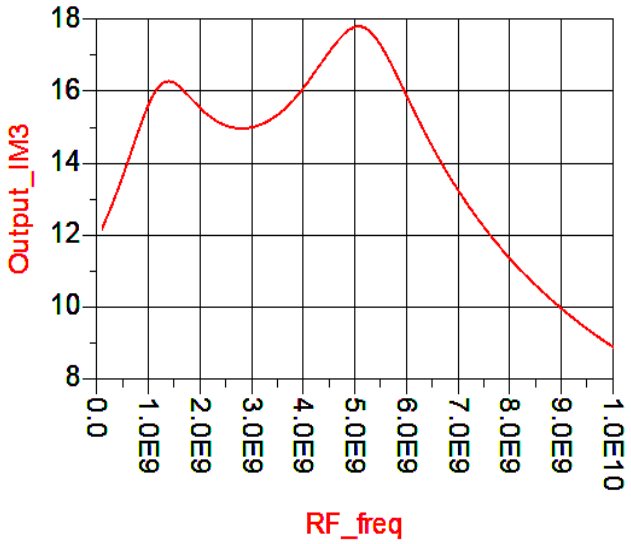

Figure 4.6: Output IM3 (dBm) versus RF frequency (GHz)

4.3 Passive Resistor Load and Inductive Source Degeneration

The circuit is simulated with passive resistors as loads, 500 Ω each. Circuit is simulated under identical conditions as that of resistive degeneration based mixer but with source resistor replaced by inductors of 1nH on either side.

Table 4.3: Simulation results for passive resistor load and inductive source degeneration based mixer

Conversion Gain (dB)	Input IM3 (dBm)	Output IM3 (dBm)	NF_{SSB} (dB)	NF_{DSB} (dB)	IIP3 (dBm)
10.845	3.992	14.837	7.883	4.450	14.345

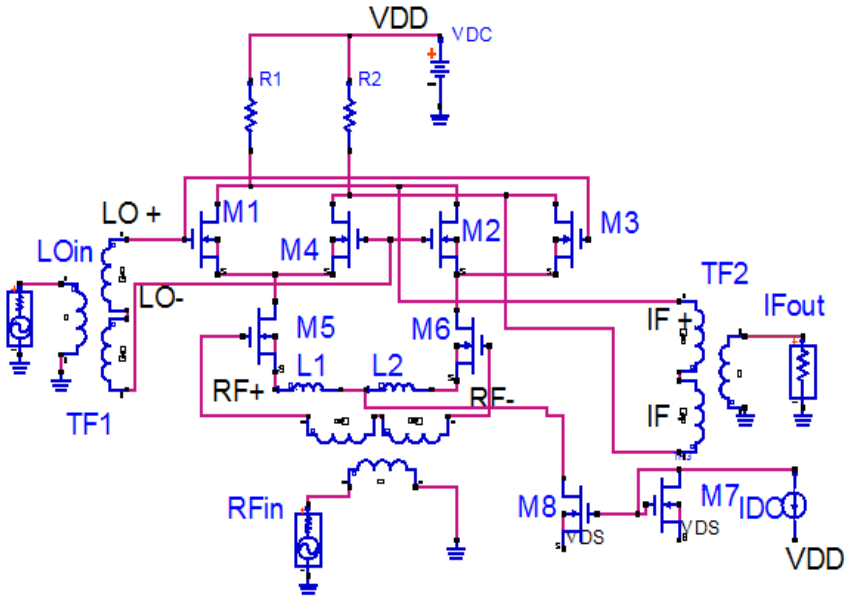

Figure 4.7: Double balanced Gilbert mixer with inductive source degeneration

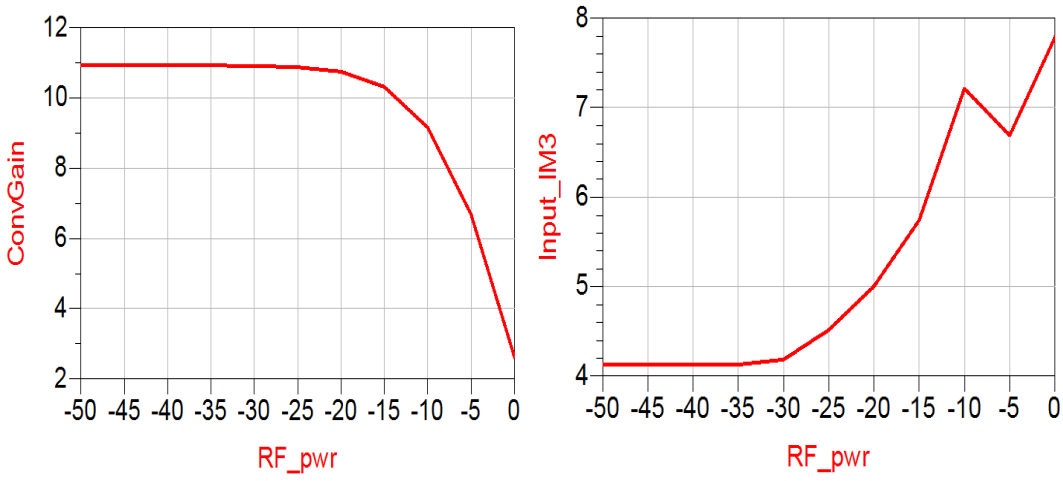

Figure 4.8: Conversion Gain (dB) versus RF Power (dBm) and Input IM3 (dBm) versus RF Power (dBm)

The variation of the conversion gain with input RF power is shown in the Figure 4.8.The mixer has achieved the maximum gain 10.932 dB which maintained its approximately constant value up to -20 dBm, beyond this point the gain is decreasing with increase in RF power. Second plot of Figure 4.8 shows that below -30 dBm RF power, IIP3 is ~4.181dBm and then there is nearly linear increase in the IIP3, after the value of -10 dBm power, IIM3 starts decreasing upto -5dB and then again increases and attains a maximum value ~7.78dB.

The simulated plot for Output IM3 is shown in Figure 4.9.The plot is almost constant at 15.093 dBm OIM3 and then increases up to 16.369 dBm at -10 dBm RF power and then starts decreasing linearly. The output power versus RF power plot of Figure 4.9 (second plot) shows that IF power at the output almost increases linearly with increase in input power. Output power at -30dBm RF power for which the parameters given in Table 4.2 are obtained is -19.085 dBm.

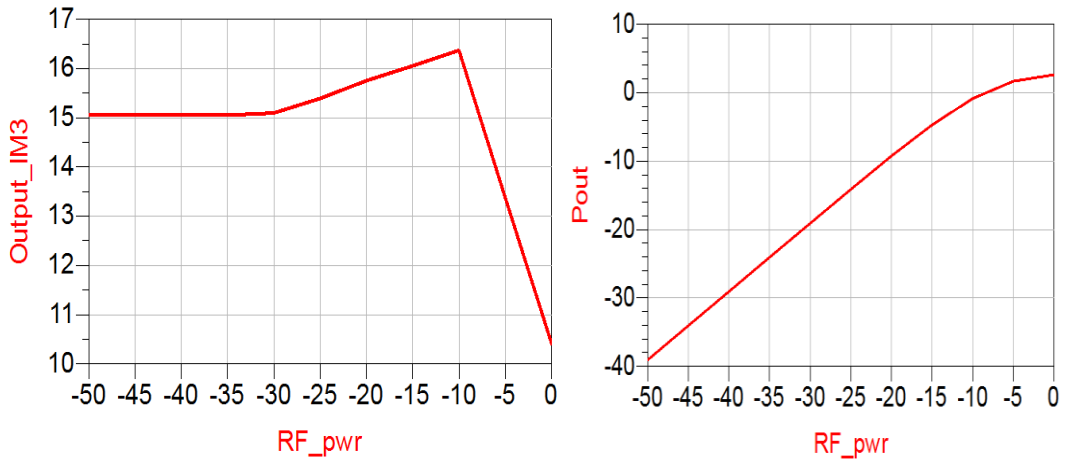

Figure 4.9: Output IM3 (dBm) versus RF Power (dBm) and Pout (dBm) versus RF Power (dBm)

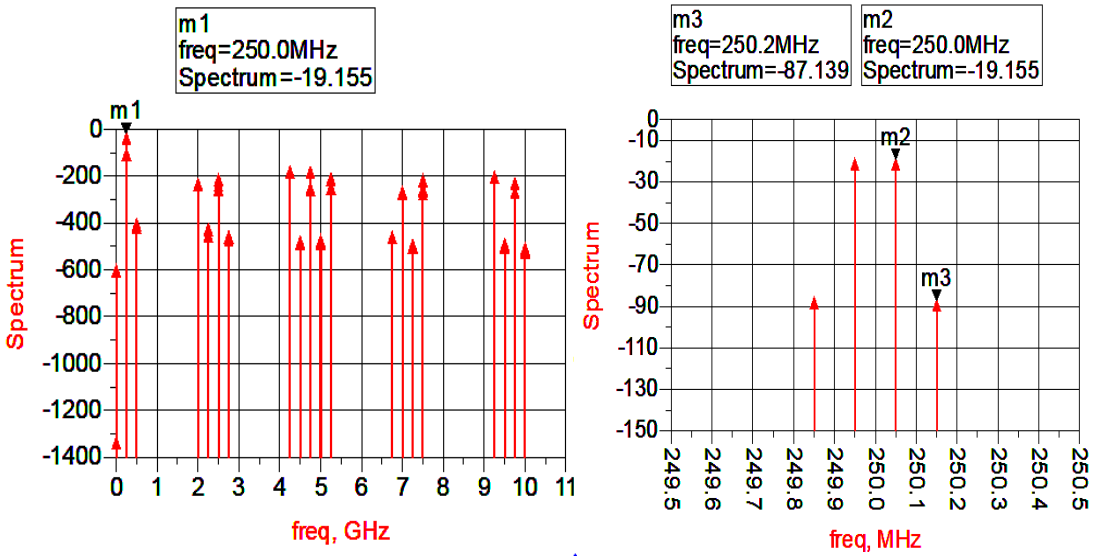

Figure 4.10: Broadband spectrum at output IF port and Spectrum near IF frequency

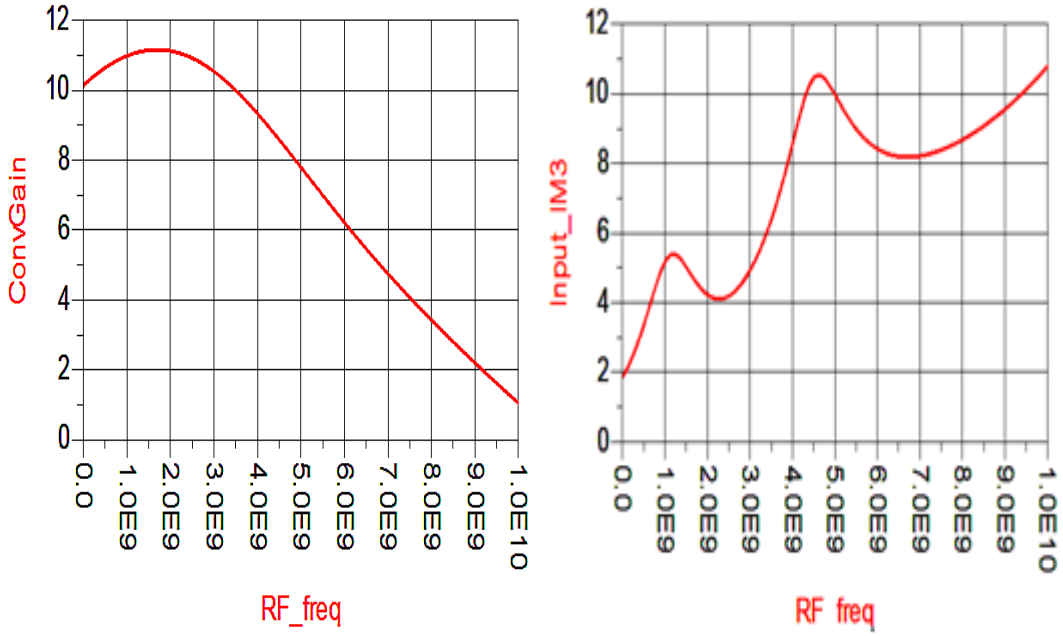

Figure 4.11: Conversion gain (dB) versus RF frequency (GHz) and Input IM3 (dBm) versus RF frequency (GHz)

Figure 4.11 shows the variation of conversion gain (in dB) with RF frequency (in GHz). The positive conversion gain is obtained from 250 MHz to 10 GHz with maximum value ~11.156dB at 1.71GHz. The IIM3 simulation with respect to RF frequency shown in Figure 4.11 (second plot) gives IIM3 greater than 4 dBm for the entire frequency range 1 GHz to 10 GHz and is greater than 2 dBm for lower range also. Its maximum value is 10.49 dBm at 4.71 GHz.

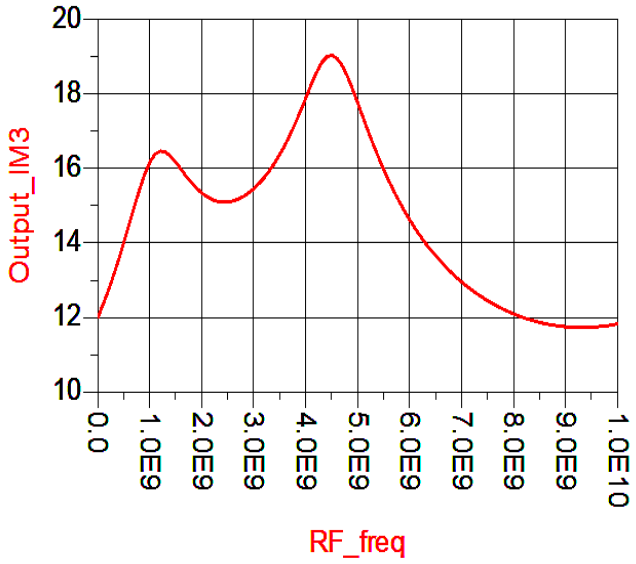

Figure 4.12: Output IM3 (dBm) versus RF frequency (GHz)

The output IM3 is maximum at 4.51 GHz with 19.035 dBm magnitude and is above 12 dBm upto 8 GHz shown in Figure 4.12.

4.4 RLC Tuned Load and Inductive Source Degeneration

The circuit is simulated with loads containing a parallel combination of a resistor R, an inductor L and a capacitor C. Circuit is simulated under identical conditions as that of inductive source degeneration based mixer with inductors L_s of 1nH on either side of the transconductor branches.

R (Ω)	L (nH)	C(pF)	L_S(nH)
500	1	375	1

Table 4.4: Simulation results for passive resistor load and inductive source degeneration based mixer

Conversion Gain (dB)	Input IM3 (dBm)	Output IM3 (dBm)	NF_{SSB} (dB)	NF_{DSB} (dB)	IIP3 (dBm)
11.005	7.097	18.102	78.797	5.156	-7.662

The variation of the conversion gain with input RF power is shown in the Figure 4.13.The mixer has achieved the maximum gain -16.5 dB which maintained its approximately constant value up to -15 dBm, beyond this point the gain is decreasing with increase in RF power. Figure 4.13 (second plot) shows that below -25 dBm RF power, IIP3 is ~3.66 dBm and then there is nearly linear increase in the IIP3 which attains a maximum value ~9.339dB for -5 dBm RF input power.

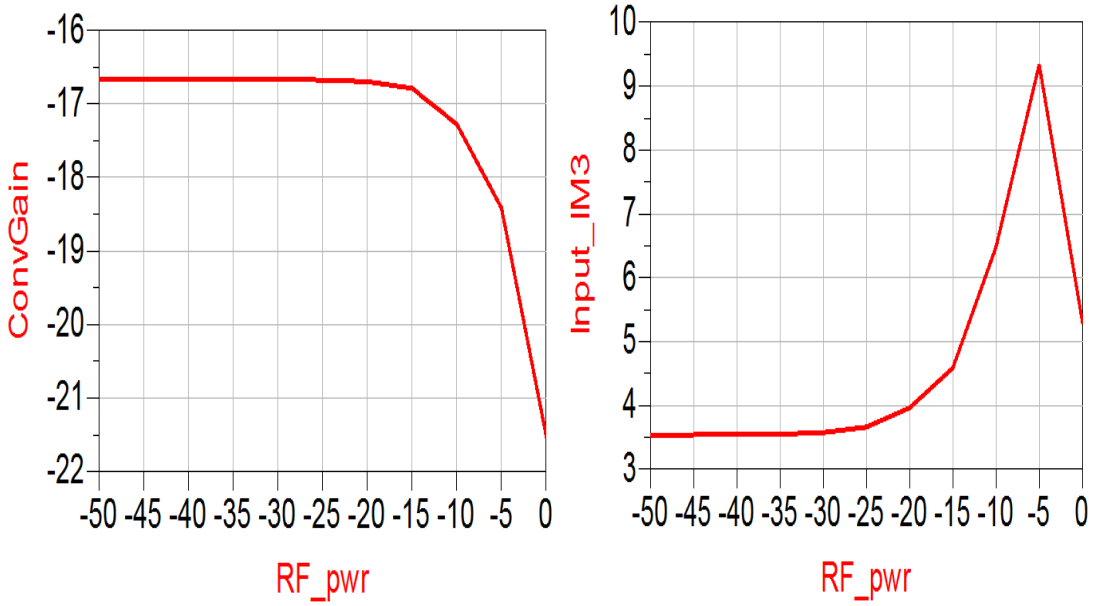

Figure 4.13: Conversion Gain (dB) versus RF Power (dBm) and Input IM3 (dBm) versus RF Power (dBm)

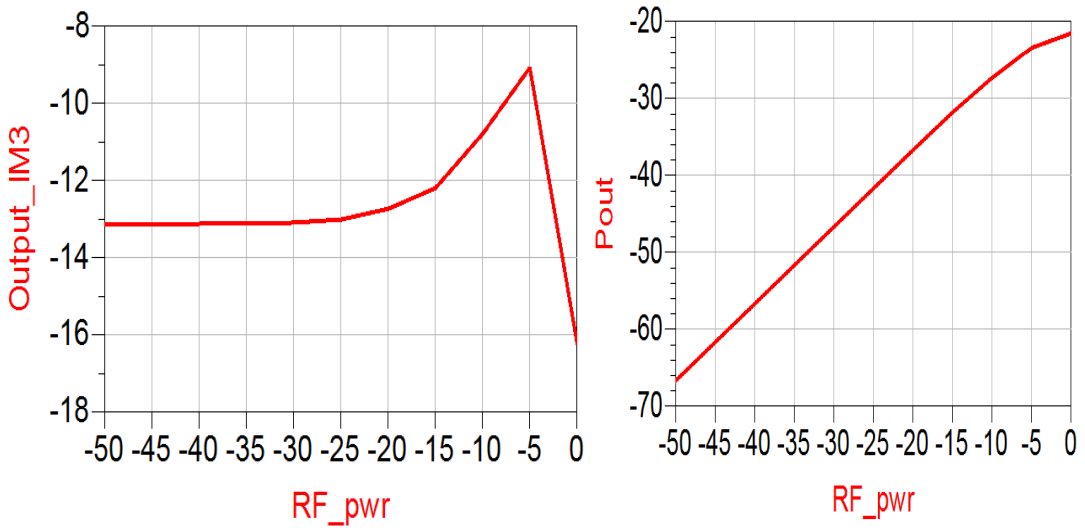

Figure 4.14: Output IM3 (dB) versus RF Power (dBm) and Pout IM3 (dBm) versus RF Power (dBm)

The simulated plot for Output IM3 is shown in Figure 4.14.The plot is almost constant at –12.73 dBm for RF power below -20 dBm and then increases up to -9.03 dBm at RF power of – 5 dBm and then starts decreasing linearly. The output power versus RF power plot of Figure 4.14 (second plot) shows that IF power at the output almost increases linearly with increase in input power. At -30 dBm RF power for which the parameters given in Table 4.3 are obtained is -46.66 dBm.

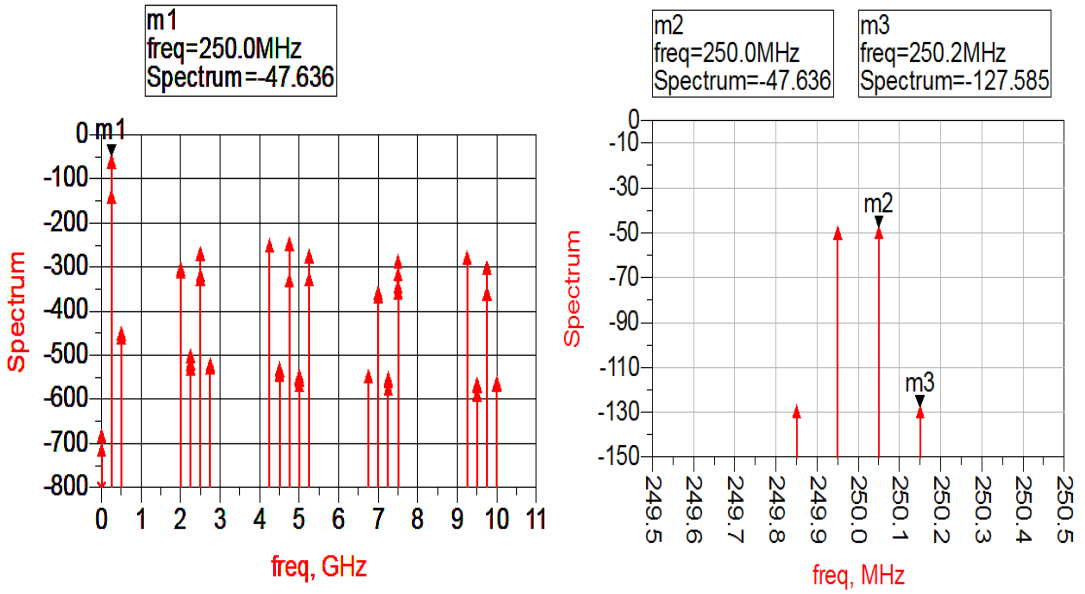

Figure 4.15: Broadband spectrum at output IF port and Spectrum near IF frequency

Figure 4.16 shows the variation of conversion gain (in dB) with RF frequency (in GHz). Due to the presence of the tuned circuit at its load two resonant peaks are obtained at the output, one at the desired RF frequency and the other at the image frequency.

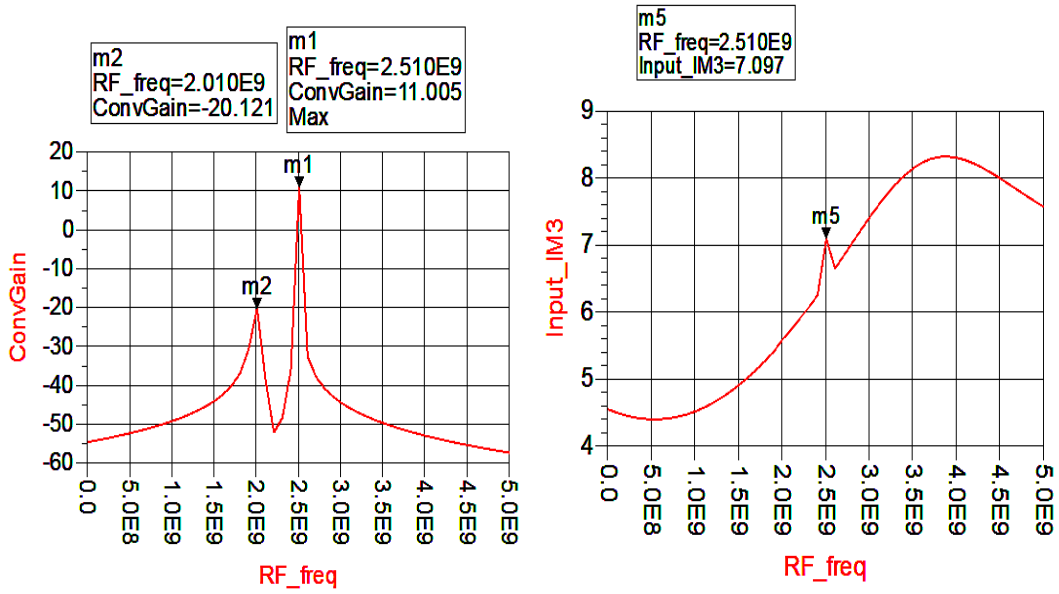

Figure 4.16: Conversion gain (dB) versus RF frequency (GHz) and Input IM3 (dBm) versus RF frequency (GHz)

However, the amplitude of the unwanted image frequency (-20.121dB at 2.01GHz) is very small compared to that at the desired IF frequency (11dB at 2.51GHz), it can be easily removed by filtering. Tuned load provides very high gain and a reasonable linearity at a frequency only so it cannot be used for wideband operation. The input IM3 at 2.51GHz is 7.097dBm and is greater than 4 dB for a wider range.

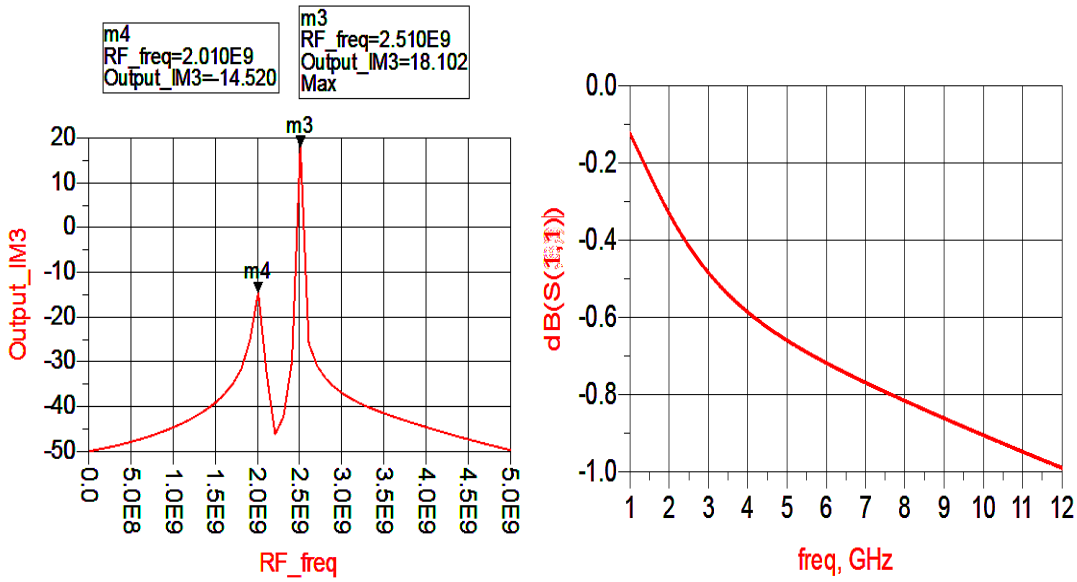

Figure 4.17: Output IM3 (dBm) versus RF frequency (GHz) and S11 (dBm) versus RF frequency (GHz)

In Figure 4.17, two peaks corresponding to desired and the image frequency are shown. However, OIM3 of the mixer is very high at the frequency of interest. At desired RF frequency OIM3 is 18.102 dBm whereas for image frequency it is -14.52 dBm.

4.5 RC Tuned Load and Inductive Source Degeneration

The circuit is simulated with loads containing a parallel combination of a resistor R and a capacitor C. Circuit is simulated under identical conditions as that of inductive source degeneration based mixer with inductors Ls of 1nH on either side of the transconductor branches.

R (Ω)	C(pF)	L_S (nH)
500	375	1

Table 4.5: Simulation results for passive resistor load and inductive source degeneration based mixer

Conversion Gain (dB)	Input IM3 (dBm)	Output IM3 (dBm)	NF_{SSB} (dB)	NF_{DSB} (dB)	IIP3 (dBm)
10.986	6.714	17.70	7.819	4.423	17.7

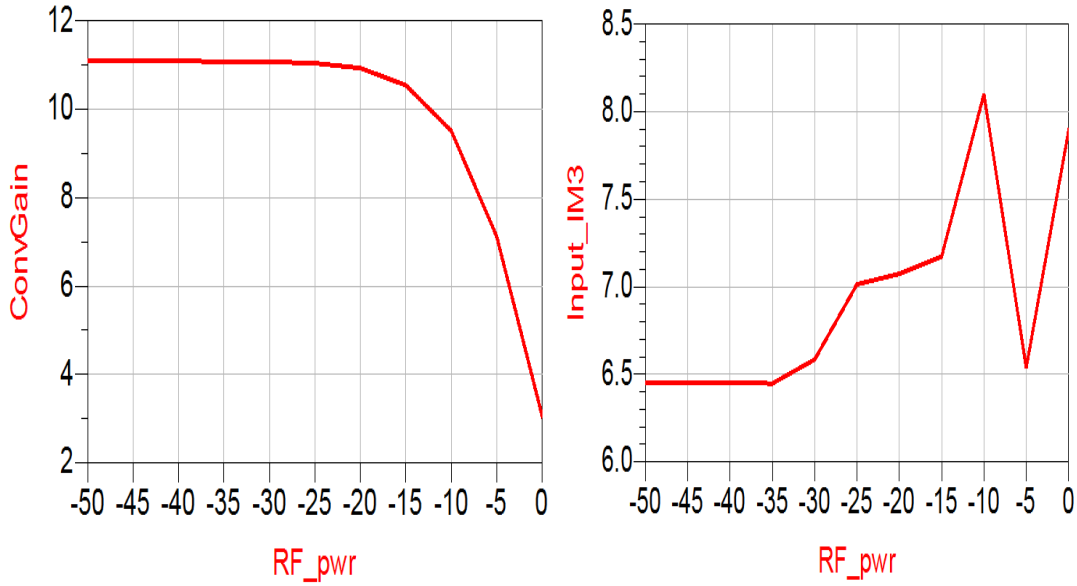

Figure 4.18: Conversion Gain (dB) versus RF Power (dBm) and Input IM3 (dBm) versus RF Power (dBm)

The variation of the conversion gain with input RF power is shown in the Figure 4.18.The mixer has achieved the maximum gain 10.932 dB which maintained its approximately constant value up to -20 dBm, beyond this point, the gain is decreasing with increase in RF power. Figure 4.18 (second plot) shows that RF power below -35 dBm, IIP3 is ~6.5dBm and then there is an increase in the IIP3 which attains a maximum value 8.1dB for -10 dBm RF input power.

The simulated plot for Output IM3 is shown in Figure 4.19.The plot is almost constant at 17.68 dBm for RF power below -10 dBm with maximum value at ~18.05

dBm at -25dBm RF power then starts decreasing linearly. The output power versus RF power plot of Figure 4.19 (second plot) shows that IF power at the output almost increases linearly with increase in input power. At -30 dBm RF power for which the parameters are given in Table 4.5 are obtained is -18.92 dBm.

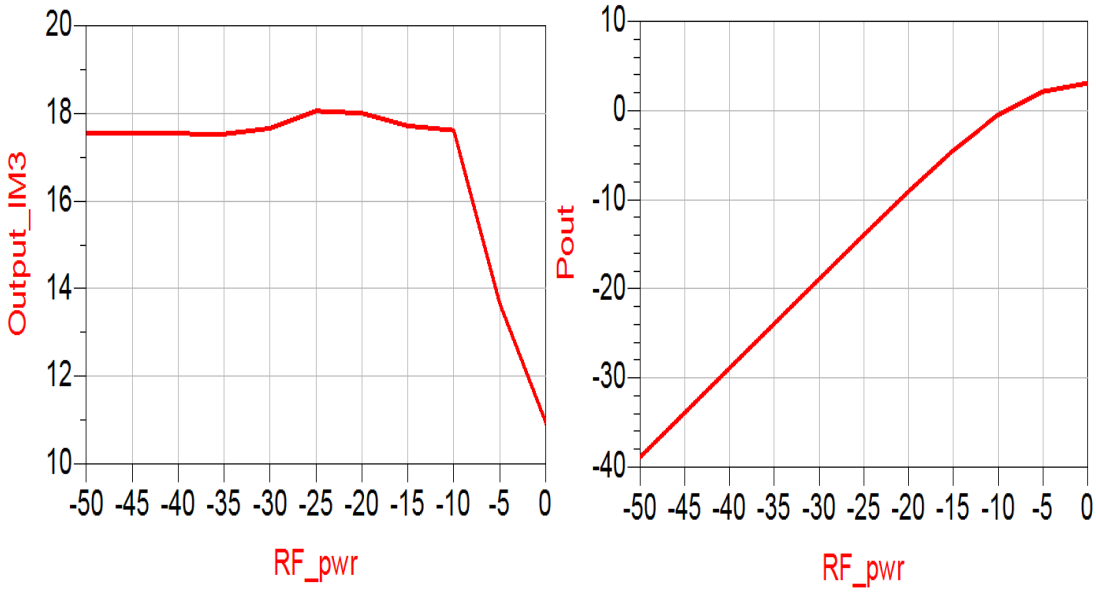

Figure 4.19: Output IM3 (dBm) versus RF Power (dBm) and Pout versus RF Power (dBm)

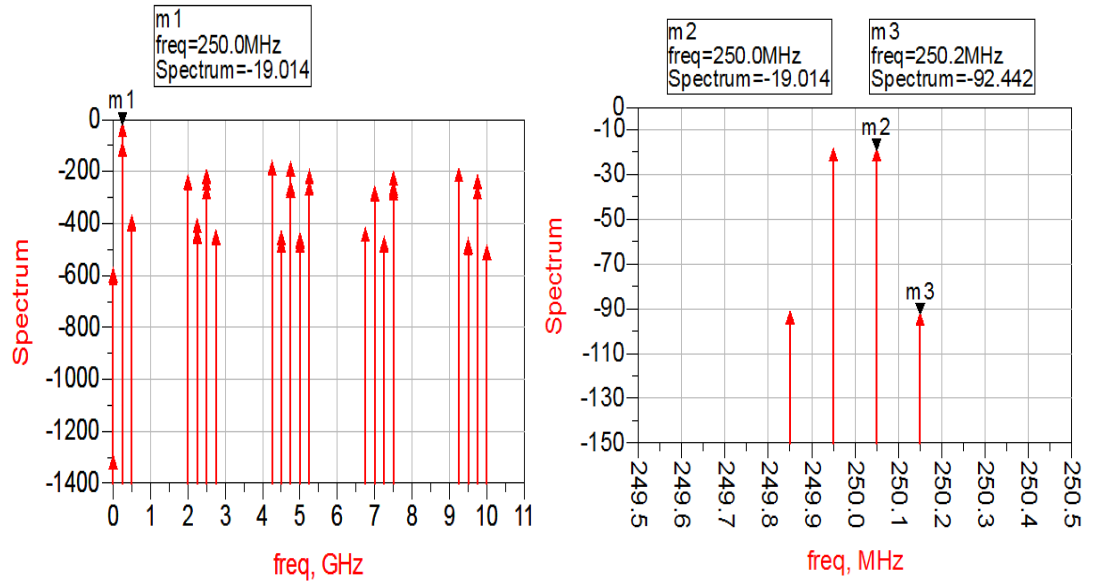

Figure 4.20: Broadband spectrum at output IF port and Spectrum near IF frequency

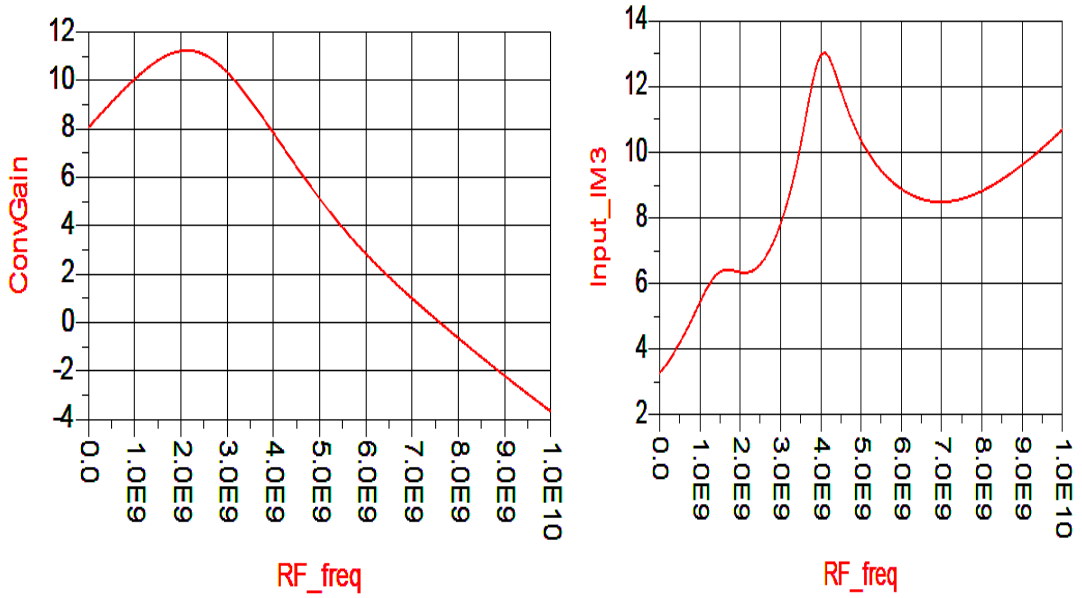

Figure 4.21: Conversion gain (dB) versus RF frequency (GHz) and Input IM3 (dBm) versus RF frequency (GHz)

Figure 4.21 shows the variation of conversion gain (in dB) and IIM3 with RF frequency (in GHz).The positive conversion gain is obtained from 250 MHz to 10 GHz with maximum value 11.243 dB at 2.11 GHz. The IIM3 simulation gives IIM3 greater than 4.6 dBm for the entire frequency range 1 GHz to 10 GHz and is greater than 2 dBm for lower range also. Its maximum value is 13.037 dBm at 4.11 GHz.

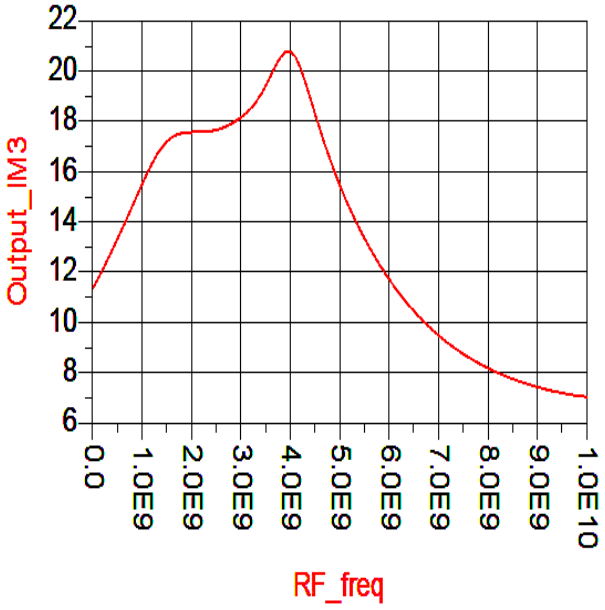

Figure 4.22 Output IM3 (dBm) versus RF frequency (GHz)

In Figure 4.22, OIM3 of the mixer is shown with maximum at 4.01 GHz with value 20.786 dBm.

4.6 LC Tuned Load and Inductive Source Degeneration

The circuit is simulated with loads containing a parallel combination of an inductor L and a capacitor C. Circuit is simulated under identical conditions as that of inductive source degeneration based mixer with inductors Ls of 1nH on either side of the transconductor branches.

L (nH)	C(pF)	L_S(nH)
1.0	375	1.0

Table 4.6: Simulation results for passive LC tuned load and inductive source degeneration based mixer

Conversion Gain (dB)	Input IM3 (dBm)	Output IM3 (dBm)	NF_{SSB} (dB)	NF_{DSB} (dB)	IIP3 (dBm)
7.69	5.178	12.86	6.946	3.627	12.867

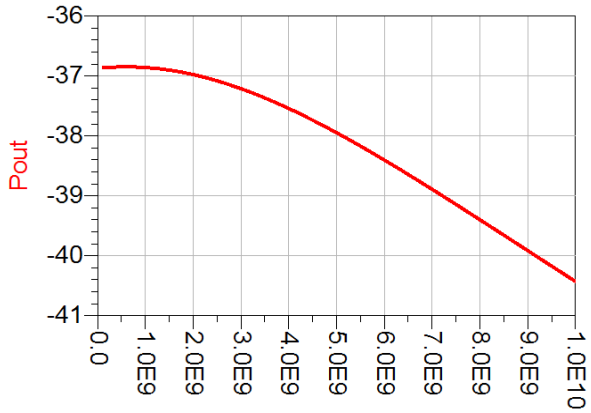

Figure 4.23: Pout IM3 (dBm) versus RF frequency

The output power versus RF frequency plot of Figure 4.37 shows that IF power at the output decreases with increase in input frequency.

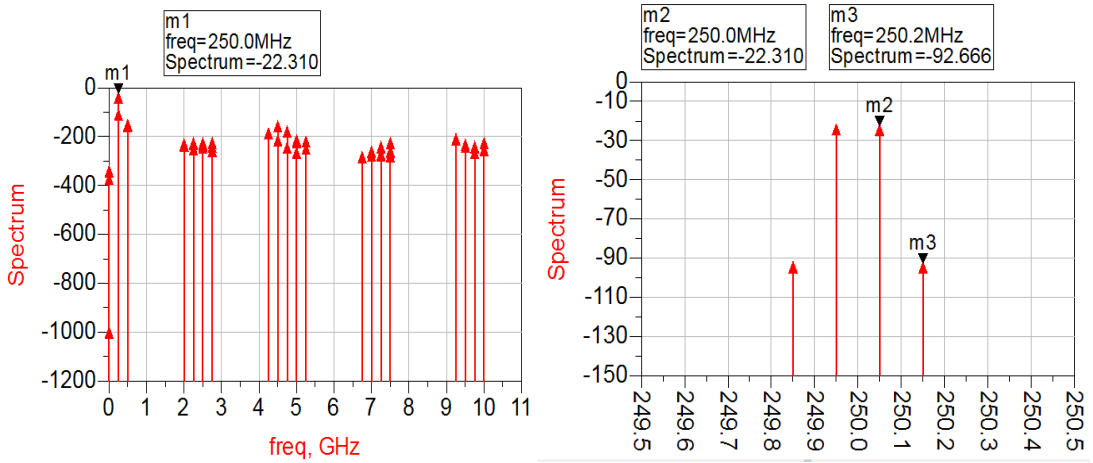

Figure 4.24: Broadband spectrum at output IF port and Spectrum near IF frequency

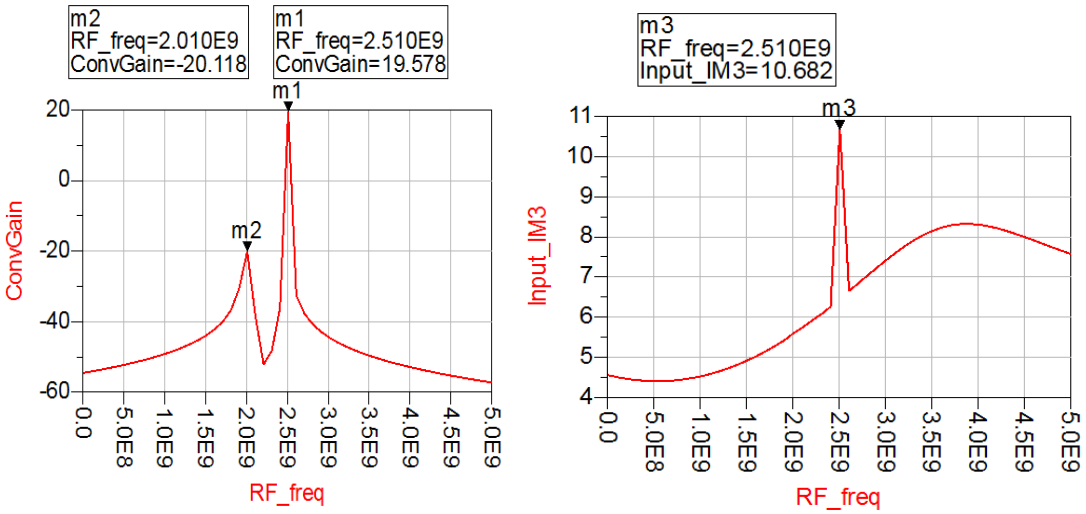

Figure 4.25: Conversion gain (dB) versus RF frequency (GHz) and Input IM3 (dBm) versus RF frequency (GHz)

Figure 4.25 shows the variation of conversion gain (in dB) with RF frequency (in GHz). Due to the presence of the tuned circuit at its load two resonant peaks are obtained at the output, one at the desired RF frequency and the other at the image frequency. However, the amplitude of the unwanted image frequency (-20.118dB at 2.01GHz) is very small compared to that at the desired IF frequency (19.57dB at 2.51GHz) which can be easily removed by filtering. Tuned load provides very high gain and a reasonable linearity at a frequency only so it cannot be used for wideband operation. The input IM3 at 2.51GHz is 10.682dBm and is greater than 4dB for a wider range.

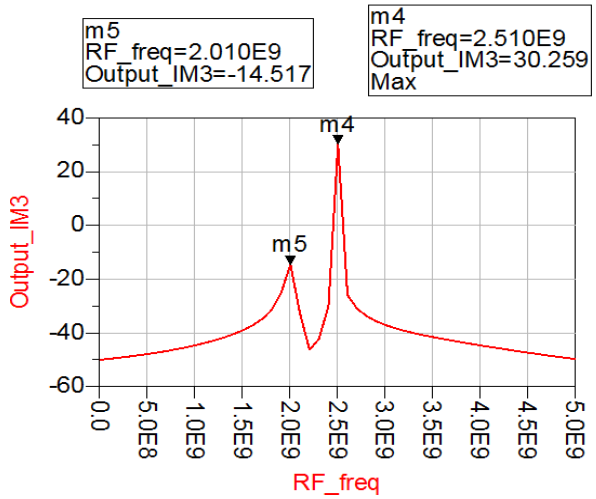

Figure 4.26: Output IM3 (dBm) versus RF frequency (GHz)

In Figure 4.26, two peaks corresponding to desired and the image frequency are shown. However, OIM3 of the mixer is very high at the frequency of interest. At desired RF frequency OIM3 is 30.359 dBm whereas for image frequency, the value of OIM3 is -14.52 dBm.

4.7 PMOS Load and Inductive Source Degeneration

The circuit is simulated with PMOS load operating in saturation region. Circuit is simulated under identical conditions as that of resistive degeneration based mixer wit inductors of 1nH on either side.

PMOS load		Vbias
W=38µm	L=0.18µm	0.84V

Table 4.7: Simulation results for PMOS load and inductive source degeneration based mixer

Conversion Gain (dB)	Input IM3 (dBm)	Output IM3 (dBm)	NF_{SSB} (dB)	NF_{DSB} (dB)	IIP3 (dBm)
8.328	11.944	20.272	10.390	6.932	19.352

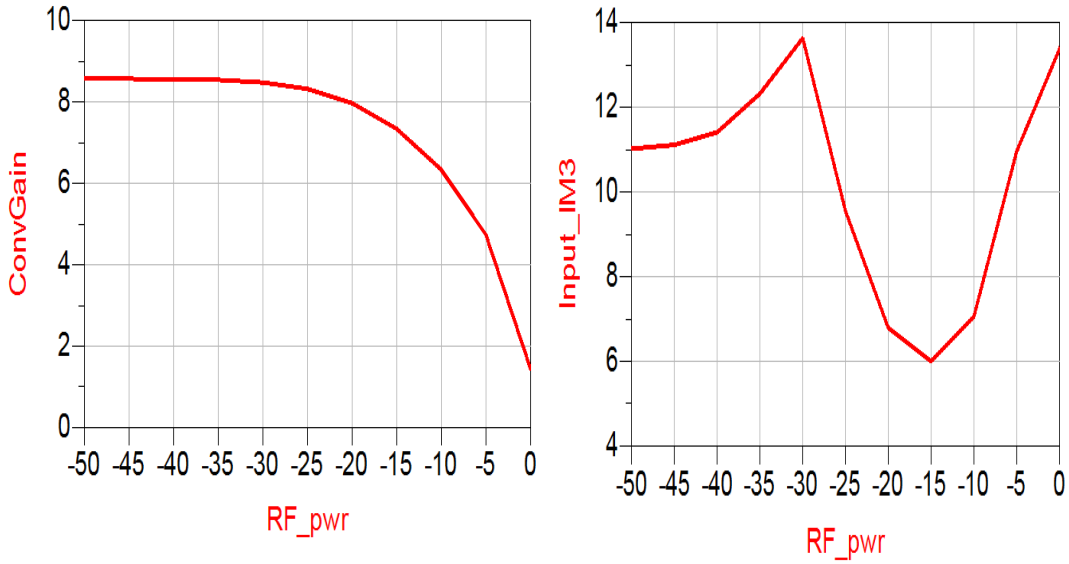

Figure 4.27: Conversion gain (dB) versus RF Power (dBm) and Input IM3 (dBm) versus RF Power (dBm)

The variation of the conversion gain (dB) with input RF power is shown in the Figure 4.27. The mixer has achieved the maximum gain 8.576 dB which maintained its approximately constant value up to -25 dBm, beyond this point the gain is decreasing with increase in RF power. Figure 4.27 (second plot) shows that maximum IIM3 is 13.644 obtained -30 dBm RF power and then it decreases and reaches at minimum value 6 dBm for -15 dBm RF power and then again increases.

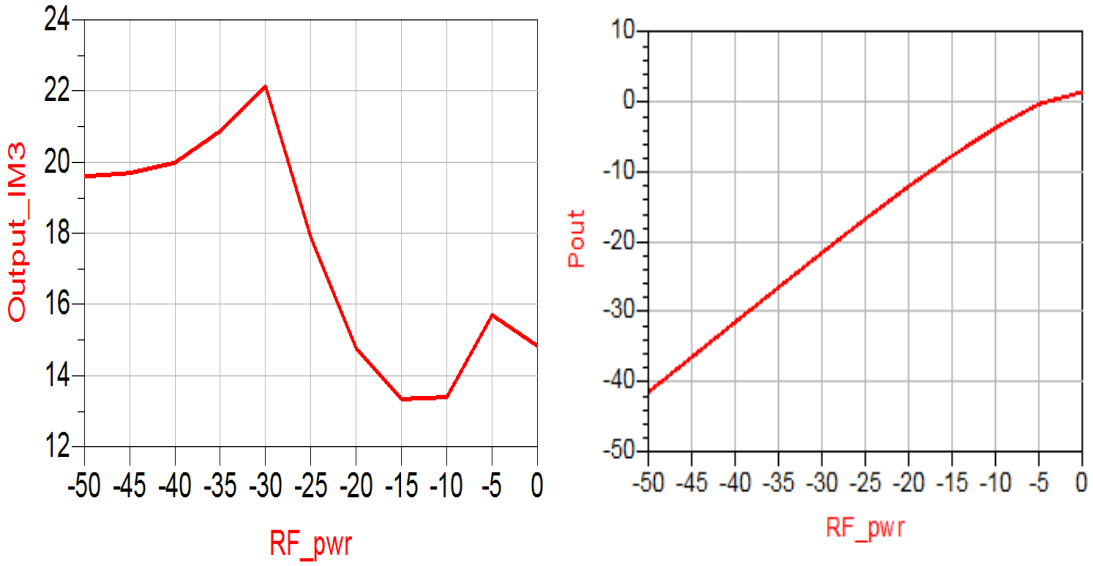

Figure 4.28: Output IM3 (dBm) versus RF Power (dBm) and Pout (dBm) versus RF Power (dBm)

The simulated plot for Output IM3 is shown in Figure 28. The plot has maximum amplitude 22.129 dBm at -30 dBm RF power. The output power versus RF power plot of Figure 4.28 (second plot) shows that IF power at the output almost increases linearly with increase in input power. The output power at -30 dBm RF power (RF_pwr) is -21.515 dBm.

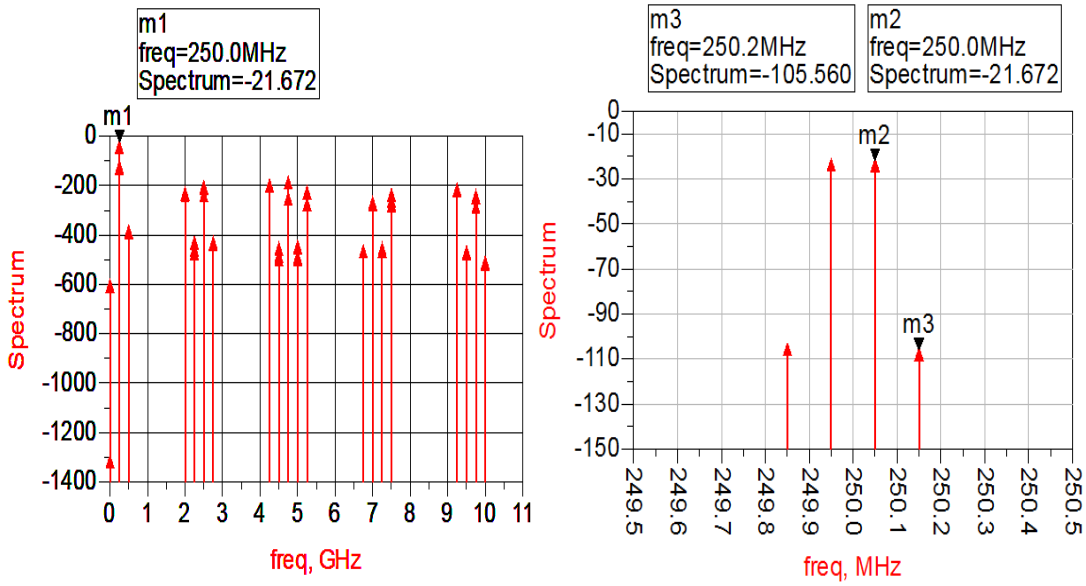

Figure 4.29: Broadband spectrum at output IF port and Spectrum near IF frequency

Figure 4.30 shows the variation of conversion gain (in dB) with RF frequency (in GHz). The positive conversion gain is obtained from 250 MHz to 6.9 GHz with maximum value 8.614 dB at 2.0 GHz frequency. The IIM3 (in dBm) simulation with respect to RF frequency shown in Figure 4.30 (second plot) produces maximum value of 17.078 dBm at 2.7GHz.

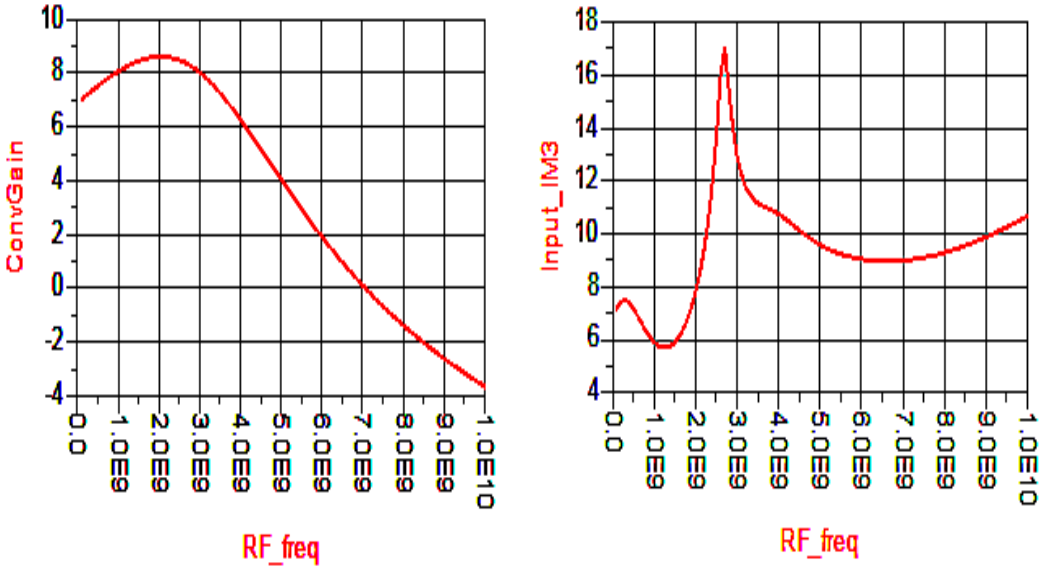

Figure 4.30: Conversion gain (dB) versus RF frequency (GHz) and Input IM3 (dBm) versus RF frequency (GHz)

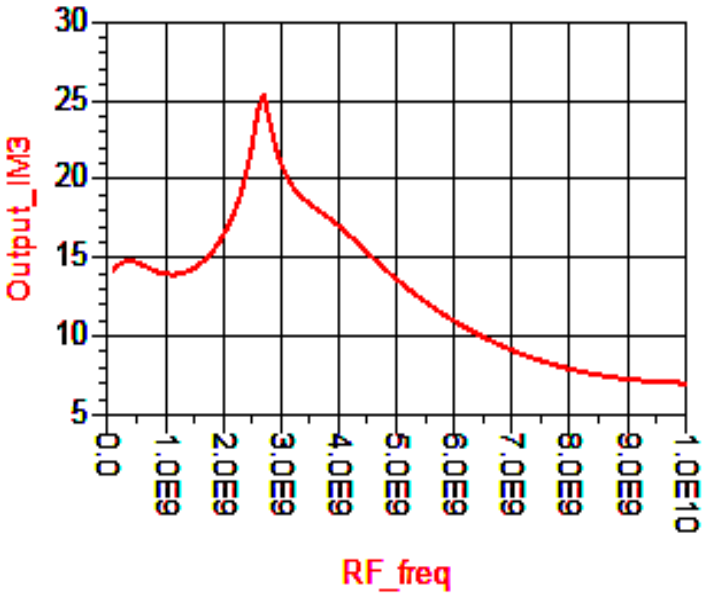

Figure 4.31: Output IM3 (dBm) versus RF frequency (GHz)

The output IM3 is maximum at 2.7 GHz with 25.419 dBm magnitude and is above 7dBm upto 10 GHz RF frequency as shown in Figure 4.31.

4.8 Resistor connected diode connected load (PMOS_R1R2)and Inductive Source Degeneration

The circuit consists of a PMOS load and gate resistors R1 and R2 and source degeneration inductors of 1nH on either of the RF transistors

PMOS load		R1=R2
W=22 µm	L=0.18µm	5KΩ

Table 4.8: Simulation results for PMOS load with R1R2 and inductive source degeneration based mixer

Conversion Gain (dB)	Input IM3 (dBm)	Output IM3 (dBm)	NF_{SSB} (dB)	NF_{DSB} (dB)	IIP3 (dBm)
16.915	5.374	22.289	8.412	4.96	22.289

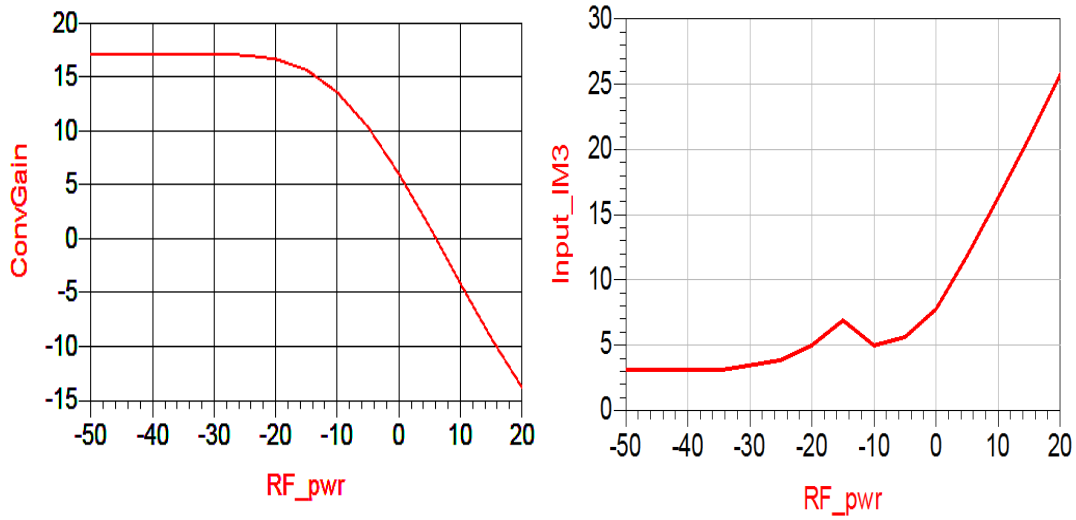

Figure 4.32: Conversion gain (dB) versus RF Power (dBm) and Input IM3 (dBm) versus RF Power (dBm)

The variation of the conversion gain with input RF power is shown in the Figure 4.32. The mixer has achieved the maximum gain 8.576 dB which maintained its approximately constant value up to -25 dBm, beyond this point, the gain is decreasing with increase in RF power. Figure 4.32(second plot) shows that below that maximum IIM3 is 13.644 obtained at -30 dBm RF power and then it decreases and reaches at minimum value 6 dBm for -15 dBm RF power and then again increases.

The simulated plot for Output IM3 is shown in Figure 4.33.The plot has maximum amplitude 22.129 dBm at -30 dBm RF power. The output power versus RF power plot of Figure 4.33 also shows that IF power at the output almost increases linearly with increase in input power. Output power at -30 dBm RF power is -21.515 dBm.

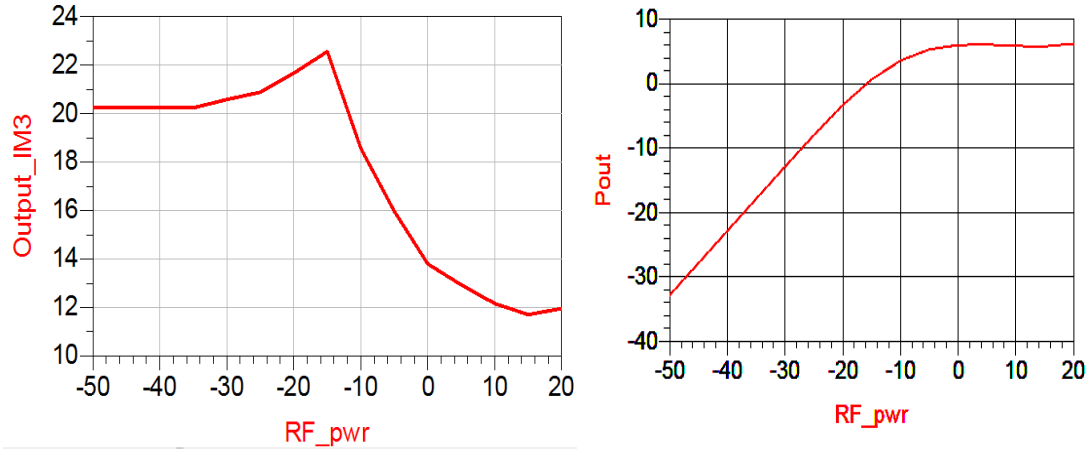

Figure 4.33: Output IM3 (dBm) versus RF Power (dBm) and Pout (dBm) versus RF Power (dBm)

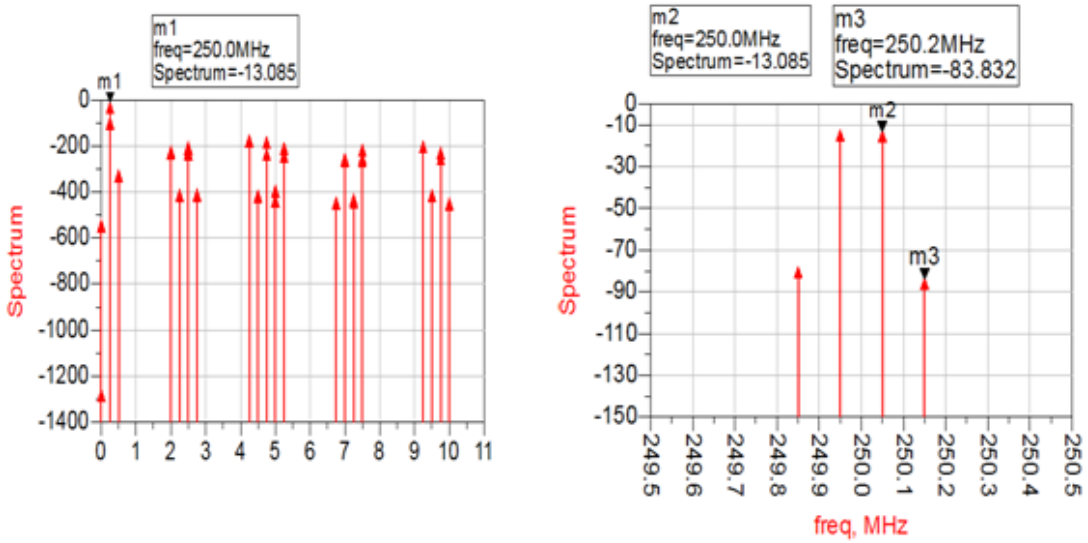

Figure 4.34 Broadband spectrum at output IF port and Spectrum near IF frequency

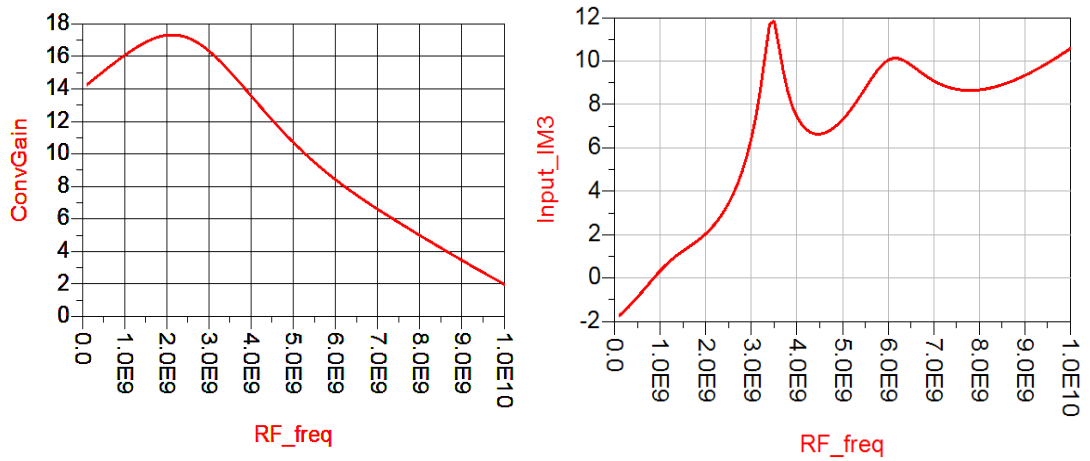

Figure 4.35 Conversion gain (dB) versus RF frequency (GHz) and Input IM3 (dBm) versus RF frequency (GHz)

Figure 4.35 shows the variation of conversion gain (in dB) with RF frequency (in GHz). The positive conversion gain is obtained from 250 MHz to 6.9 GHz with

maximum value 8.614 dB at 2.0 GHz frequency. The IIM3 simulation with respect to RF frequency shown in Figure 4.35 (second plot) gives maximum value 17.078 dBm at 2.7 GHz.

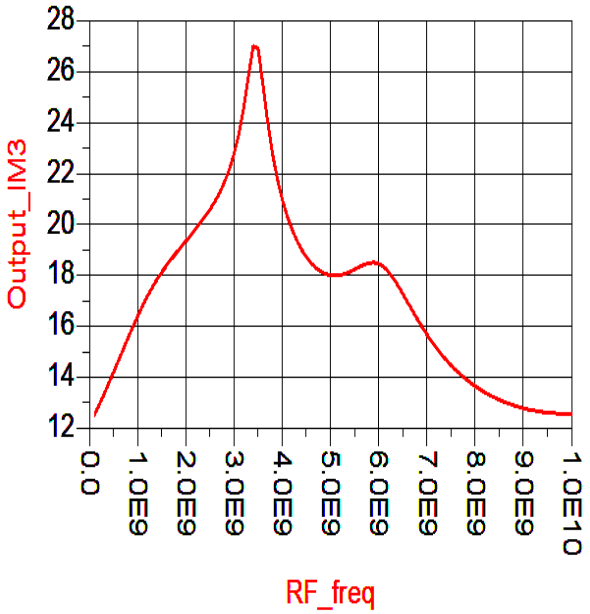

Figure 4.36: Output IM3 (dBm) versus RF frequency (GHz)

The output IM3 is maximum at 2.7 GHz with 25.419 dBm magnitude and is above 7dBm upto 10 GHz RF frequency as shown in Figure 4.36.

4.9 Current Mirror load and Inductive Source Degeneration

The mixer is simulated with current mirror circuit as load and degeneration inductors of 1nH on either side of RF transistors. The W/L ratio for the PMOS transistors at the load is 22(µm)/0.18(µm).

Table 4.9: Simulation results for Current Mirror load and inductive source degeneration based mixer

Conversion Gain (dB)	**Input IM3 (dBm)**	**Output IM3 (dBm)**	**NF_{SSB} (dB)**	**NF_{DSB} (dB)**	**IIP3 (dBm)**
18.266	9.975	28.241	8.405	4.9	22.133

The variation of the conversion gain with input RF power is shown in the Figure 4.37.The mixer has achieved the maximum gain 16.94dB which maintained its approximately constant value up to -25 dBm, beyond this point the gain is decreasing with increase in RF power.

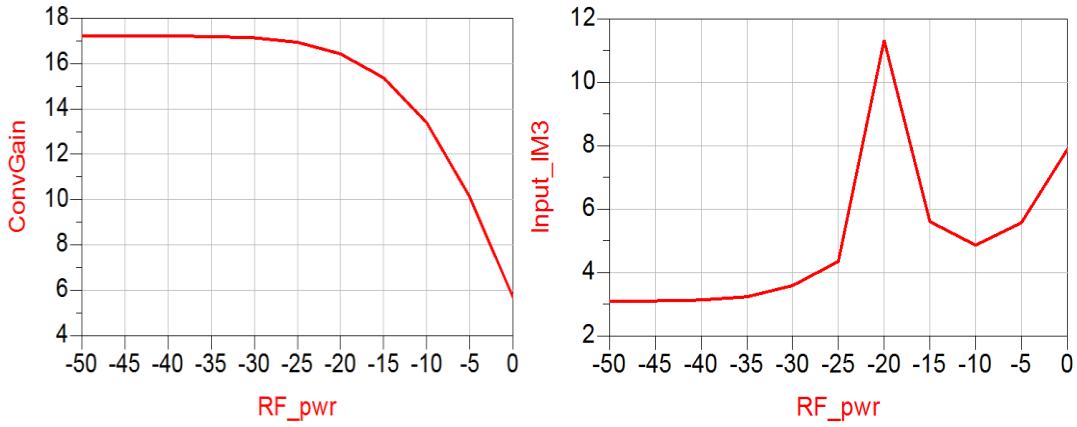

Figure 4.37: Conversion Gain (dB) versus RF Power (dBm) and Input IM3 (dBm) versus RF Power (dBm)

Figure 4.37 also shows that below -30 dBm power input, IIM3 is nearly constant at 3.56 dBm and there is a sharp increase in the curve which reaches a maximum value of ~11.3 dBm for -20 dBm RF power and then again decreases.

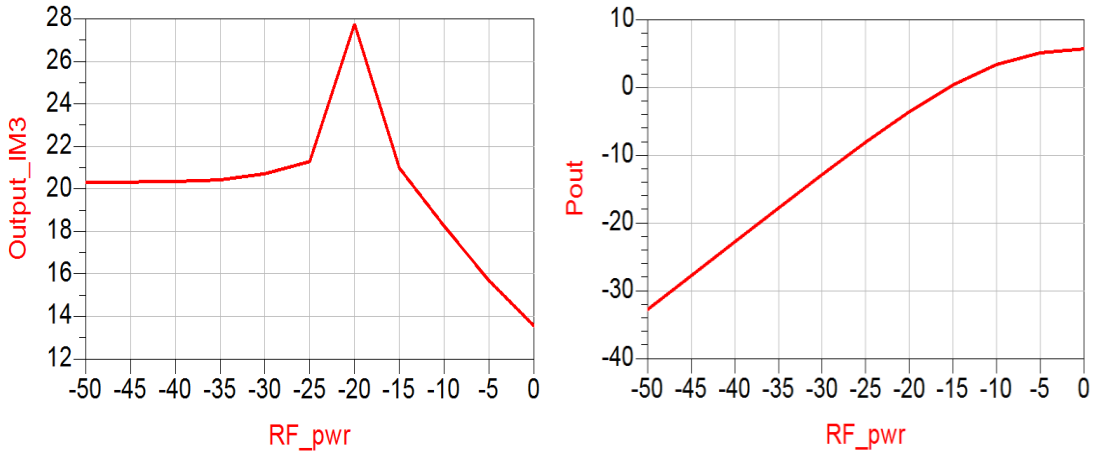

Figure 4.38: Output IM3 (dBm) versus RF Power (dBm) and Pout IM3 (dBm) versus RF Power (dBm)

The simulated plot for Output IM3 is shown in Figure 4.38.The plot has maximum amplitude 21.29 dBm at -25 dBm RF power. The output power versus RF power plot shows that IF power at the output almost increases linearly with increase in input power. Output power for -30dBm input is -12.869 dBm

Figure 4.39 shows the variation of conversion gain (in dB) with RF frequency (in GHz). The positive conversion gain is obtained from 250 MHz to 10 GHz with maximum value 18.763 dB at 2.2GHz frequency. The IIM3 simulation with respect to RF frequency is also shown maximum value is 10.16 dBm at 3.5 GHz.

The output IM3 is maximum at 3.5 GHz RF frequency with 25.78 dBm magnitude and is above ~10 dBm upto 10 GHz RF frequency as shown in Figure 4.41.

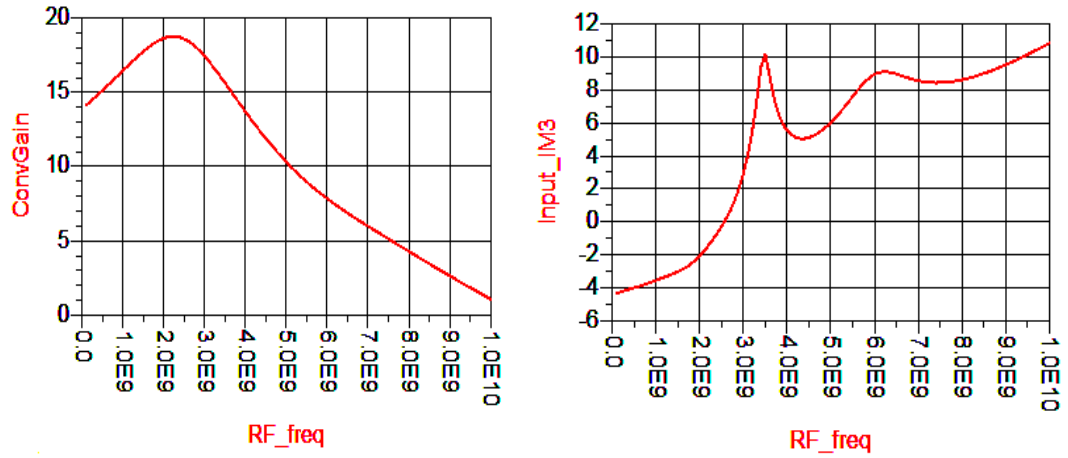

Figure 4.39: Conversion gain (dB) versus RF frequency (GHz) and Input IM3 (dBm) versus RF frequency (GHz)

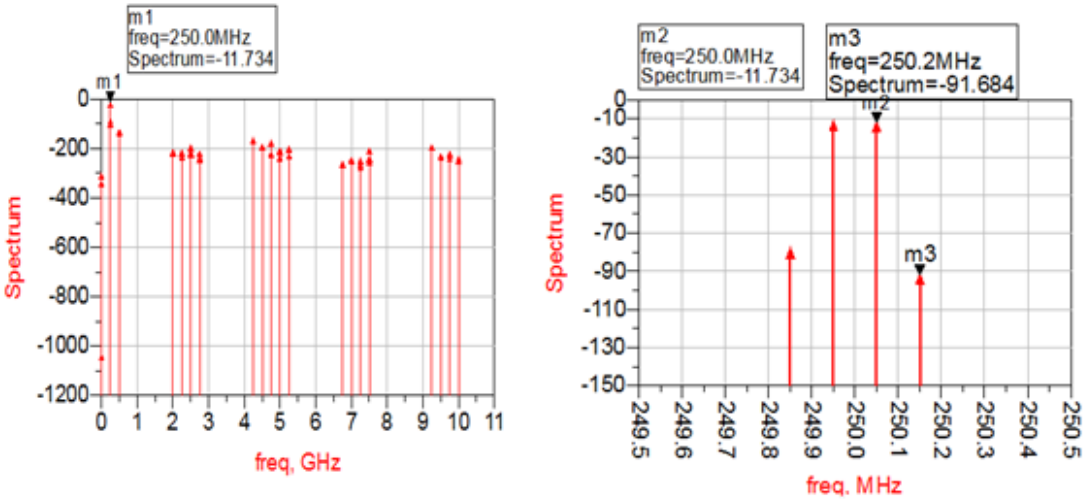

Figure 4.40: Broadband spectrum at output IF port and Spectrum near IF frequency

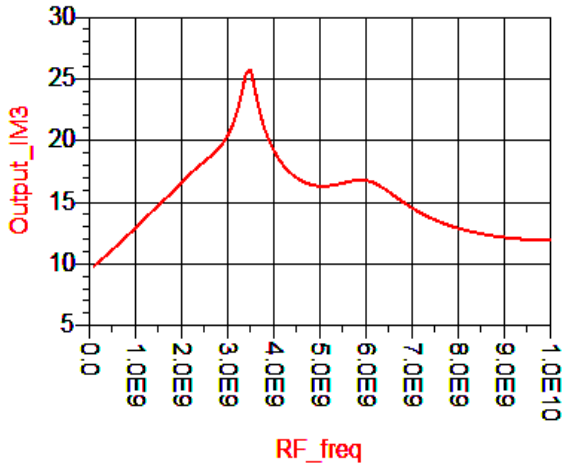

Figure 4.41: Output IM3 (dBm) versus RF frequency (GHz)

4.10 Resistor connected Diode connected MOS with capacitor at load (PMOS_R1R2_C) and Inductive Source Degeneration

The mixer is simulated with current mirror circuit as load and degeneration inductors of 1nH on either side of RF transistors. The W/L ratio for the PMOS transistors at the load is 2.2(µm)/0.18(µm).

Table 4.10: Simulation Results for R1R2_C load and Inductive source degeneration based mixer

Conversion Gain (dB)	Input IM3 (dBm)	Output IM3 (dBm)	NF_{SSB} (dB)	NF_{DSB} (dB)	IIP3 (dBm)
6.108	8.186	14.294	11.138	7.753	13.485

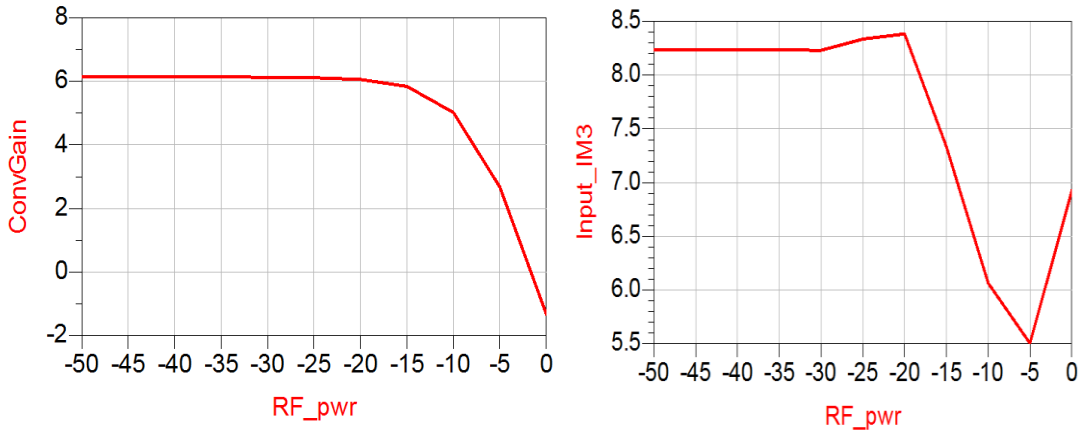

Figure 4.42: Conversion gain (dB) versus RF Power (dBm) and Input IM3(dB) versus RF Power (dBm)

Figure 4.42 shows that the maximum conversion gain is 6dB which is constant upto -15 dBm input RF power and then it continuously decreases.Input IM3 has maximum value 8.36dBm for -20dBm input.

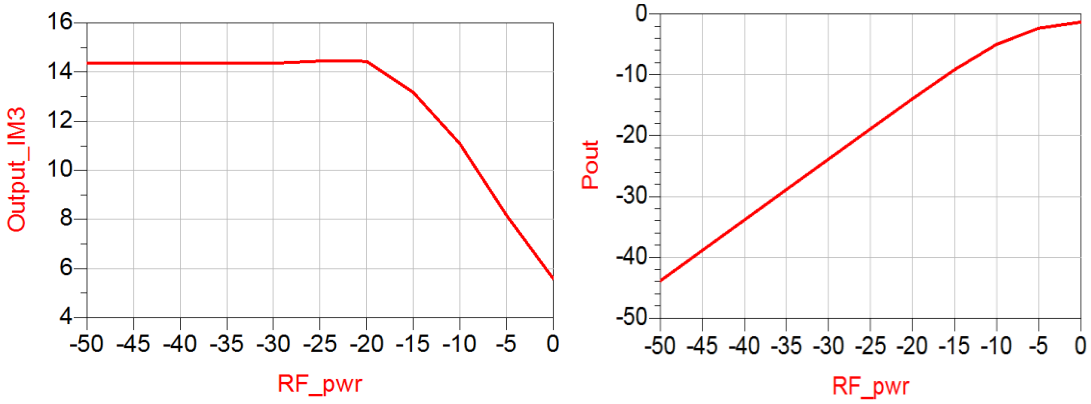

Figure 4.43: Outpur IM3 (dBm) versus RF Power (dBm) and Pout IM3 (dBm) versus RF Power (dBm)

From OIM3 simulation, it has been observed that maximum 14.3 dBm amplitude is obtained which is constant upto -20 dBm input power. The output power versus RF power plot of Figure 4.43 shows that IF power at the output almost increases linearly with increase in input power. Output power at -30 dBm RF power is -23.8 dBm..

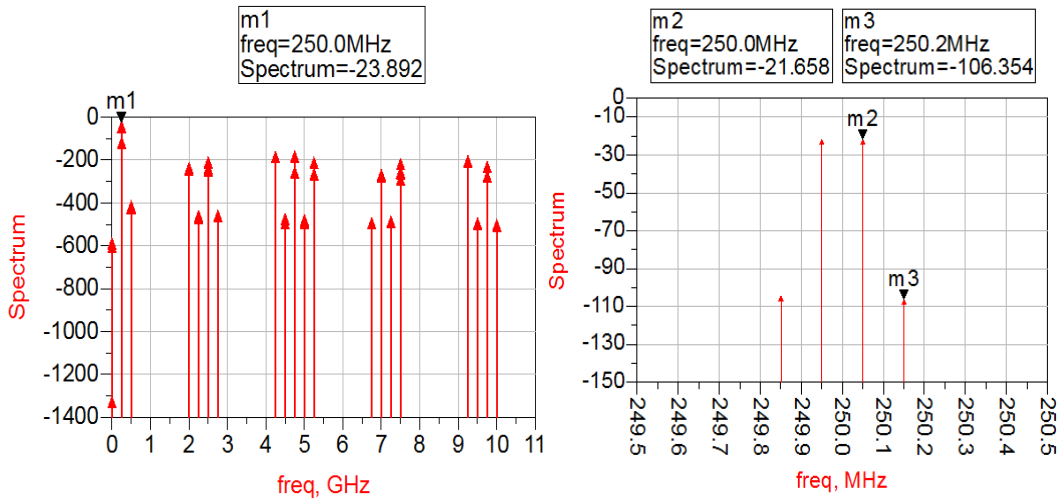

Figure 4.44: Broadband spectrum at output IF port and Spectrum near IF frequency

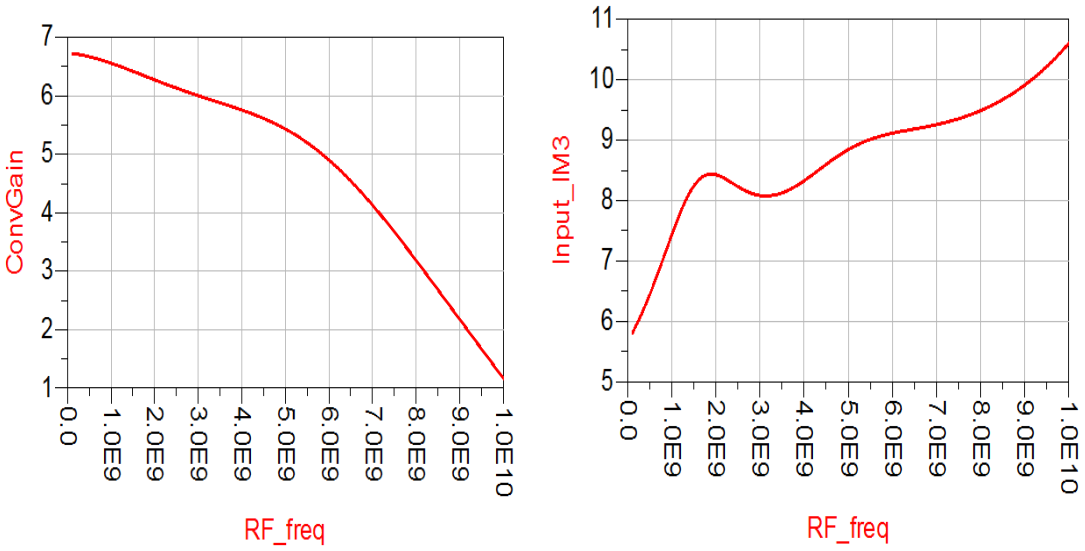

Figure 4.45: Conversion gain (dB) versus RF frequency (GHz) and Input IM3 (dBm) versus RF frequency (GHz)

Figure 4.45 shows the variation of conversion gain (in dB) with RF frequency (in GHz). The conversion gain is >1 from 250 MHz to 10 GHz with maximum value 6.72 dB at 1.0 GHz frequency. The IIM3 simulation with respect to RF frequency shows maximum value 10.6 dBm at 10GHz.

The output IM3 is maximum at 1.8 GHz with 14.7 dBm magnitude and is above 11.8 dBm upto 10 GHz RF frequency as shown in Figure 4.46.

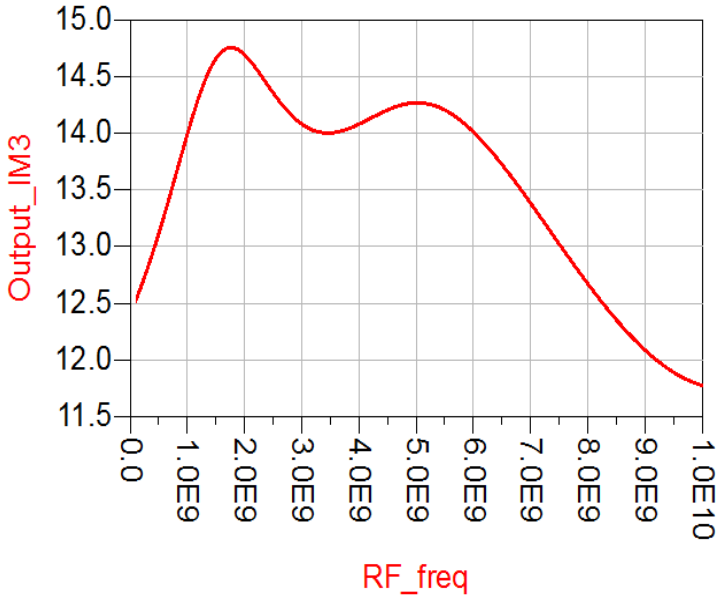

Figure 4.46: Output IM3 (dBm) versus RF frequency (GHz)

4.11 Resistor connected diode connected MOS with current source (PMOS_R1R2_IB) and Inductive Source Degeneration

The mixer is simulated with current mirror circuit as load and degeneration inductors of 1nH on either side of RF transistors. The W/L ratio for the PMOS transistors at the load is 2.2(µm)/0.18(µm).

PMOS LOAD		**R_1=R_2**	**I_{Bias}**
W=22µm	L=0.18µm	5kΩ	1.0µA

Table 4.11: Simulation results for Current Mirror load and inductive source degeneration based mixer

Conversion Gain (dB)	**Input IM3 (dBm)**	**Output IM3 (dBm)**	**NF_{SSB} (dB)**	**NF_{DSB} (dB)**	**IIP3 (dBm)**
16.912	5.469	22.38	8.411	4.96	20.123

Maximum conversion gain is ~17.2 dB which is constant upto -20 dBm input power and then decreases continuously. Maximum IIM3 obtained from simulation is around 7.7 dBm as shown in Figure 4.47.

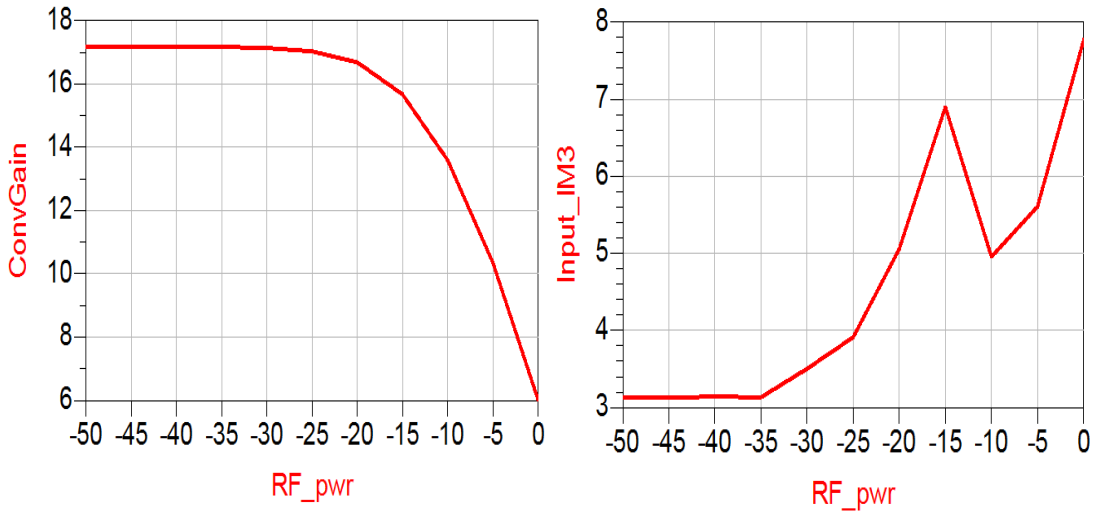

Figure 4.47: Conversion gain (dB) versus RF Power (dBm) and Input IM3 (dBm) versus RF Power (dBm)

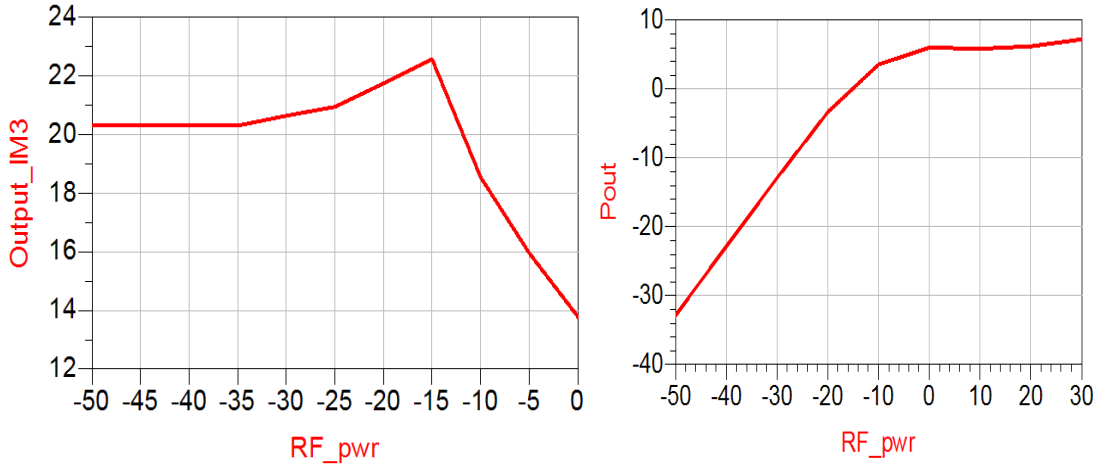

Figure 4.48: Output IM3 (dBm) versus RF Power (dBm) and Output power (dBm) versus RF Power (dBm)

Maximum OIM3 for the mixer is around 22.2 dBm at -15dBm input power. The output power versus RF power plot of Figure 4.48 shows that IF power at the output increases linearly with increase in input power. Output power at -30 dBm RF power is about -12 dBm.

Figure 4.49 shows the variation of conversion gain (in dB) with RF frequency (in GHz). The positive conversion gain is obtained from 250 MHz to 10 GHz with maximum value ~17.3 dB at 2.1 GHz frequency. The IIM3 simulation with respect to RF frequency shown gives maximum value 11.92 dBm at 3.5 GHz .

The output IM3 is maximum at 3.4 GHz with 27.2 dBm magnitude and is above 12 dBm upto 10 GHz RF frequency as shown in Figure 4.51.

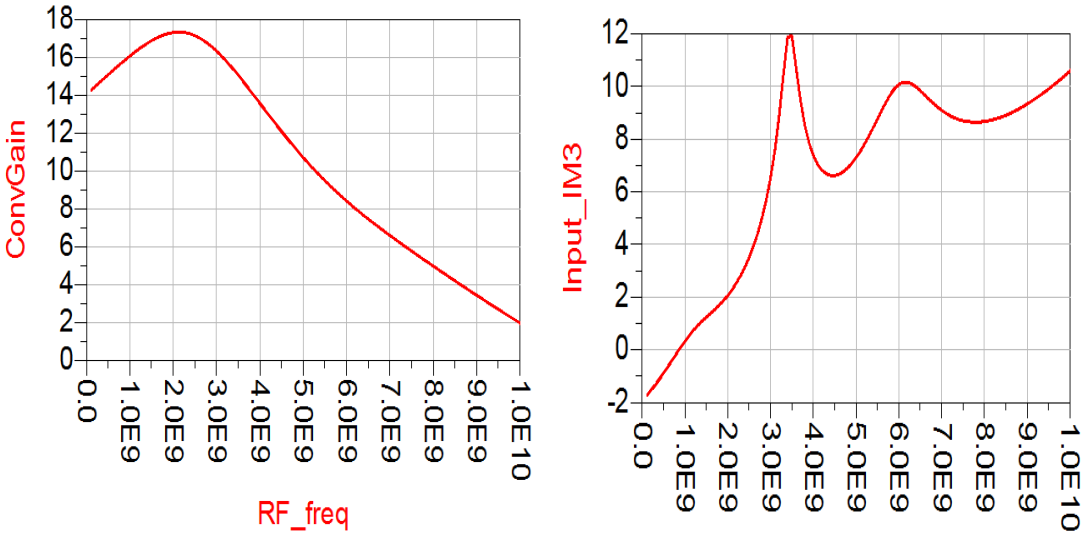

Figure 4.49: Conversion gain (dB) versus RF frequency (GHz) and Input IM3 (dBm) versus RF frequency (GHz)

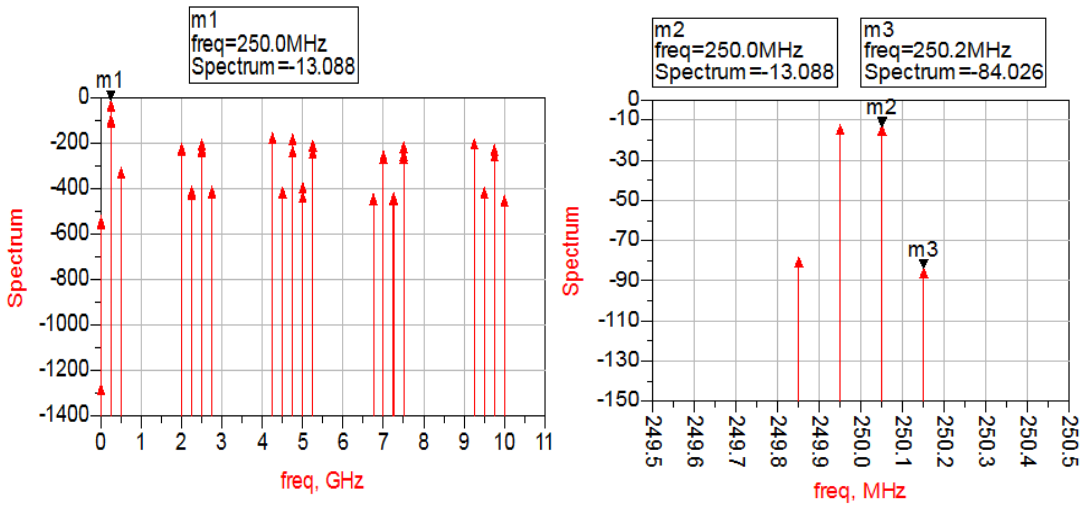

Figure 4.50: Broadband spectrum at output IF port and Spectrum near IF frequency.

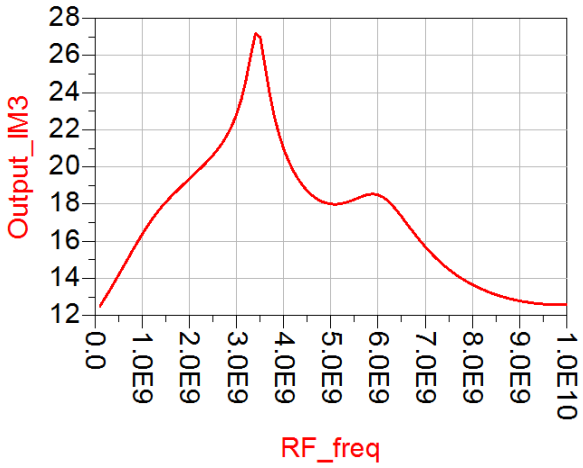

Figure 4.51: Output IM3 (dBm) versus RF frequency (GHz)

4.12 PMOS Load with Current injection and Inductive Source Degeneration

The circuit is simulated with PMOS load operating in saturation region. Circuit is simulated under identical conditions as that of resistive degeneration based mixer with inductors of 1nH on either side.

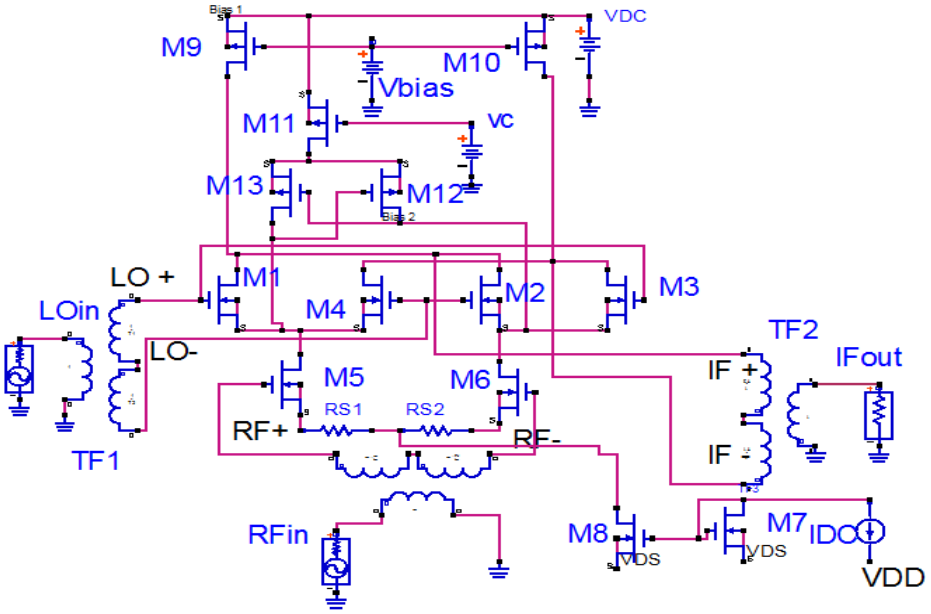

Figure 4.52: PMOS load based Gilbert mixer with current injection method

PMOS load	V_c(V)	Width (M12/M13)	Width (M11)	V_{bias}
W=38µm	1.2	10µm	70µm	0.84V

Table 4.12: Simulation results for PMOS load with current injection and inductive source degeneration based mixer

Conversion Gain (dB)	Input IM3 (dBm)	Output IM3 (dBm)	NF_{SSB} (dB)	NF_{DSB} (dB)	IIP3 (dBm)
19.624	0.760	20.383	8.826	5.316	20.38

The variation of the conversion gain (in dB) with input RF power (dBm) is shown in Figure 4.53.The mixer has achieved the maximum gain 20dB which maintained its approximately constant value up to -25dBm, beyond this point the gain is decreasing with increase in RF power. Figure 4.53 (second plot) shows that maximum IIM3 is 6.9dBm obtained at -15dBm RF power.

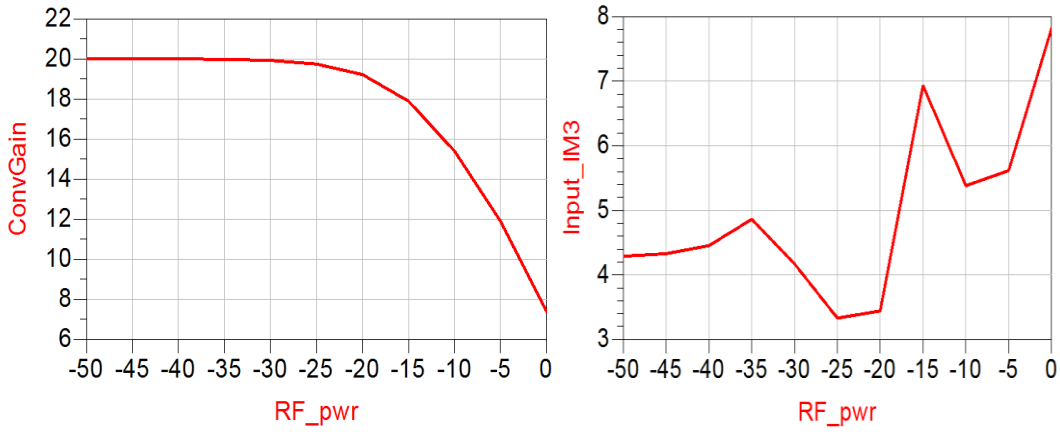

Figure 4.53: Conversion Gain (dB) versus RF Power (dBm) and Input IM3(dBm) versus RF Power (dBm)

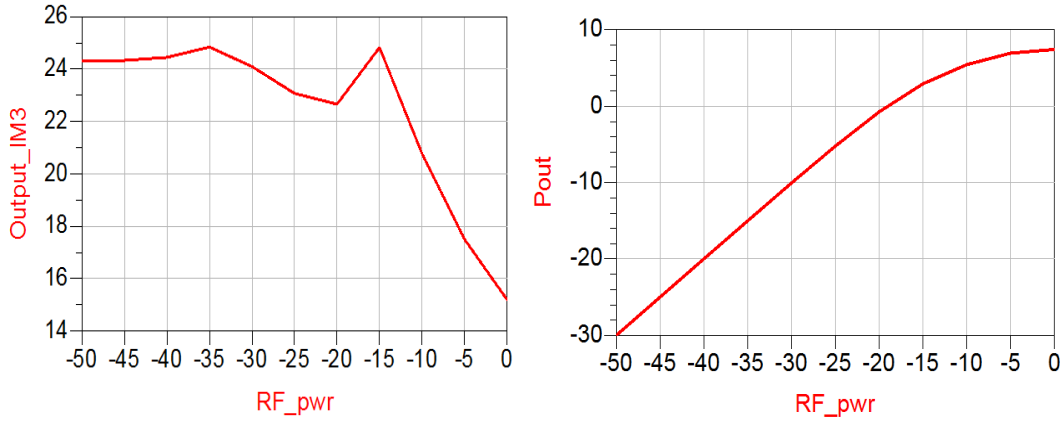

Figure 4.54: Output IM3 (dBm) versus RF Power (dBm) and Pout (dB) versus RF Power (dBm)

The simulated plot for Output IM3 is shown in Figure 4.54.The plot has maximum amplitude 24.84dBm at -15dBm RF power. The output power versus RF power plot shows that IF power at the output almost increases linearly with increase in input power. Output power at -30dBm RF power is -10 dBm.

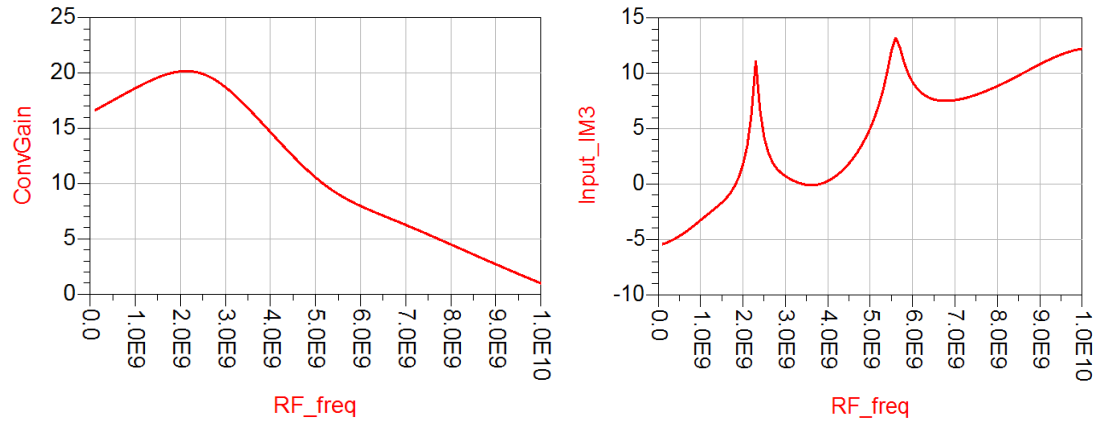

Figure 4.55: Conversion Gain (dB) versus RF frequency (GHz) and Input IM3 (dBm) versus RF frequency (GHz)

Figure 4.55 shows the variation of conversion gain (in dB) with RF frequency (in GHz). The positive conversion gain is obtained from 250 MHz to 10 GHz with maximum value 20dB at 2.1GHz frequency. The IIM3 simulation with respect to RF frequency shows maximum value 13.23dBm at 5.6 GHz.

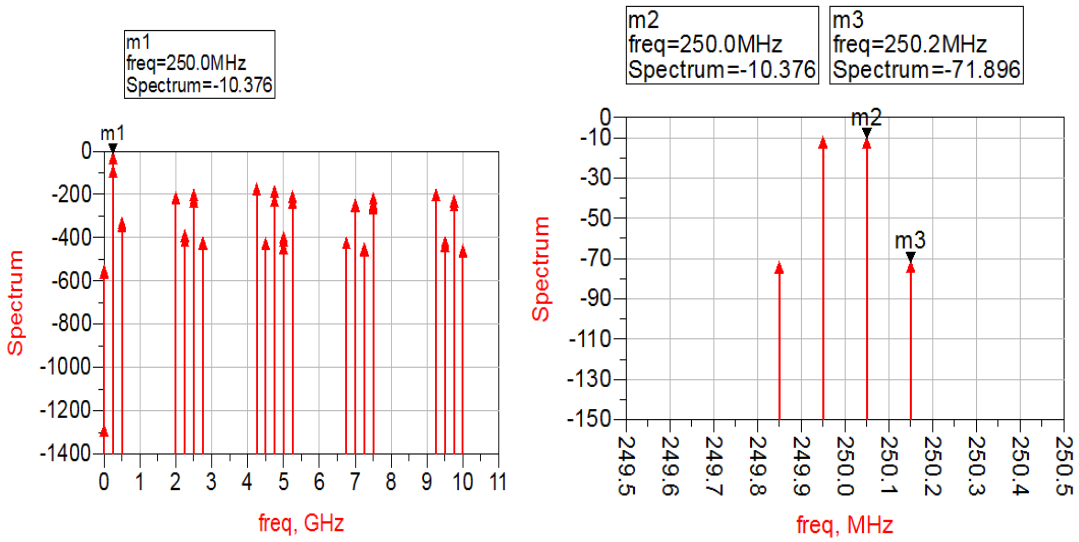

Figure 4.56: Broadband spectrum at output IF port and Spectrum near IF frequency

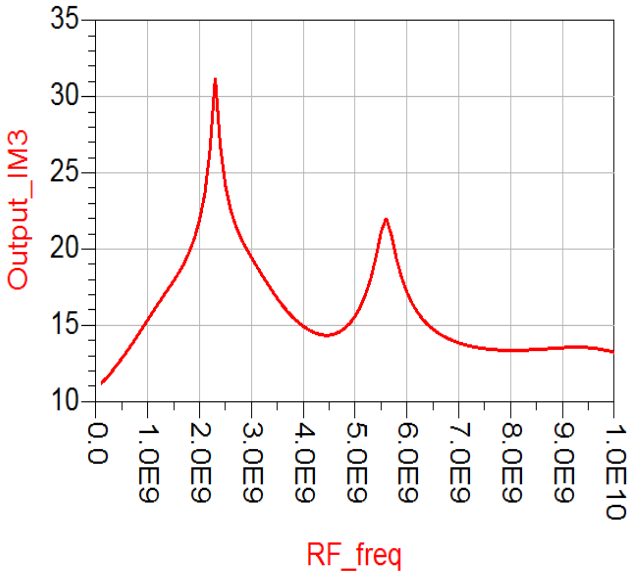

Figure 4.57: Output IM3 (dBm) versus RF frequency (GHz)

The output IM3 is maximum at 2.3 GHz with 31.27dBm magnitude and is above 11dBm upto 10 GHz RF frequency as shown in Figure 4.57.

4.13 Proposed ULPD load with Inductive Source Degeneration

The circuit is simulated with PMOS load operating in saturation region. Circuit is simulated under identical conditions as that of resistive degeneration based mixer with inductors of 1nH on either side.

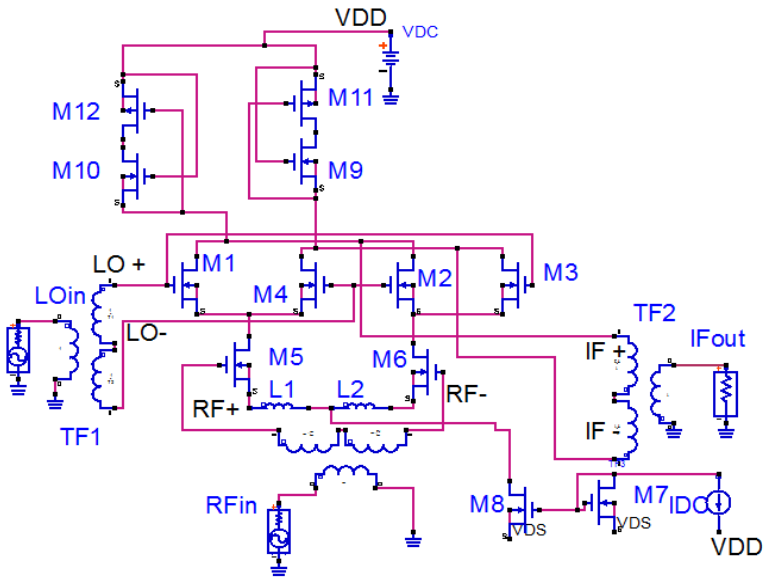

Figure 4.58: Proposed ULPD load based mixer

Table 4.13: Simulation results for Proposed load circuit with inductive source degeneration based mixer

Conversion Gain (dB)	Input IM3 (dBm)	Output IM3 (dBm)	NF_{SSB} (dB)	NF_{DSB} (dB)	IIP3 (dBm)
7.782	8.996	16.778	7.931	4.563	16.46

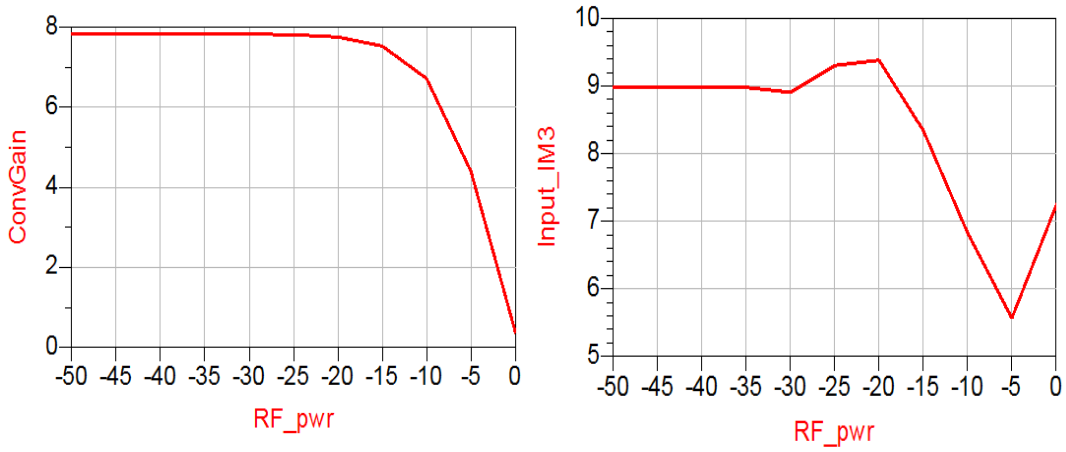

Figure 4.59: Conversion Gain (dB) versus RF Power (dBm) and Input IM3(dBm) versus RF Power (dBm)

The variation of the conversion gain (in dB) with input RF power (in dBm) is shown in the Figure 4.59.The mixer has achieved the maximum gain ~8dB which maintained its approximately constant up to -20dBm, beyond this point the gain is decreasing with increase in RF power. Figure 59(second plot) shows that the value of IIM3 is 9dBm below -30 dBm RF power and has maximum value ~9.5 dBm at -20 dBm RF power.

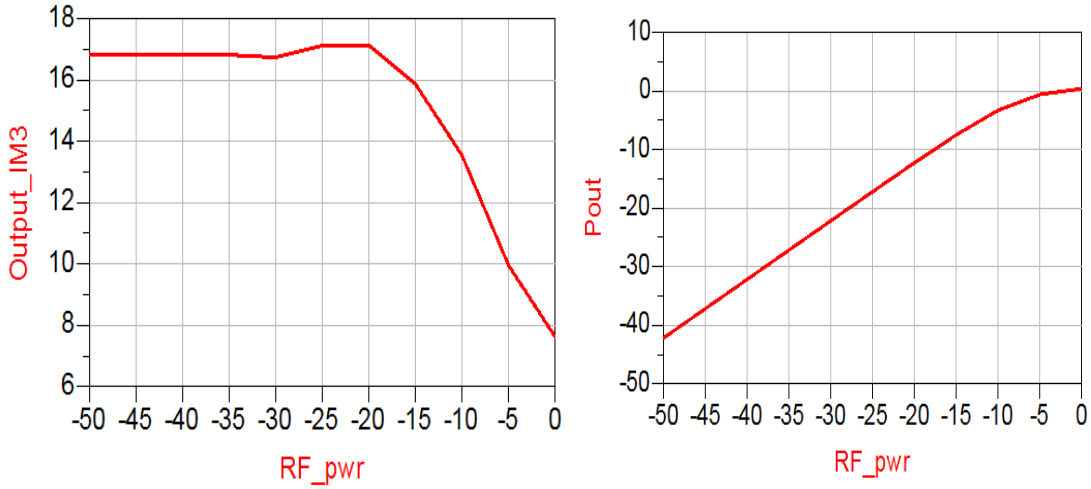

Figure 4.60: Output IM3(dB) versus RF Power(dBm) and Pout IM3(dBm) versus RF Power (dBm)

The simulated plot for Output IM3 is shown in Figure 4.60. The plot has maximum amplitude 16.778 dBm at -20 dBm RF power. The output power versus RF power plot shows that IF power at the output almost increases linearly with increase in input power. Output power at -30 dBm RF power is -22.1 dBm.

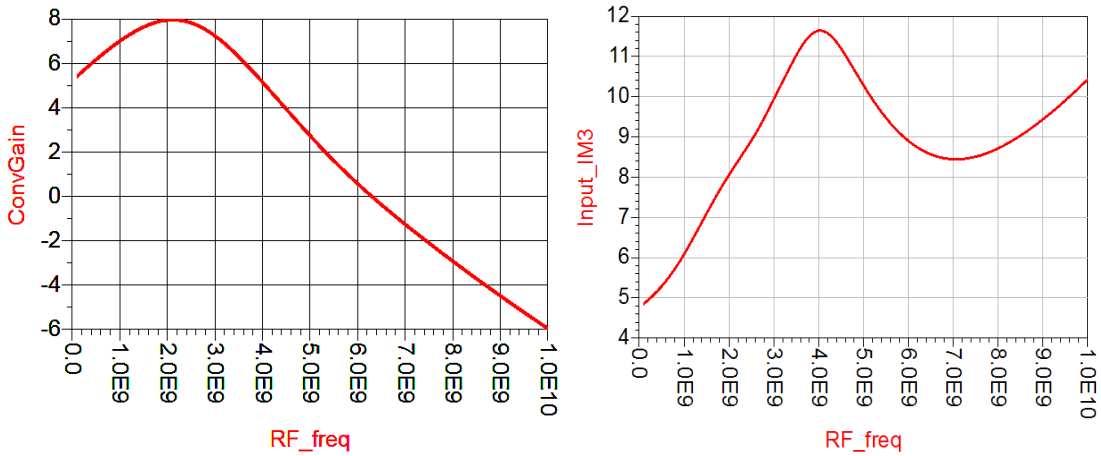

Figure 4.61 Conversion gain (dB) versus RF frequency (GHz) and Input IM3 (dBm) versus RF frequency (GHz)

Figure 4.61 shows the variation of conversion gain (in dB) with RF frequency (in GHz). The positive conversion gain is obtained from 100 MHz to 6 GHz with maximum value ~8dB at 2.1GHz. The mixer achieves the input third order intercept as high as 11.64 dB at 4GHz frequency and 4.85 dB at 100 MHz.

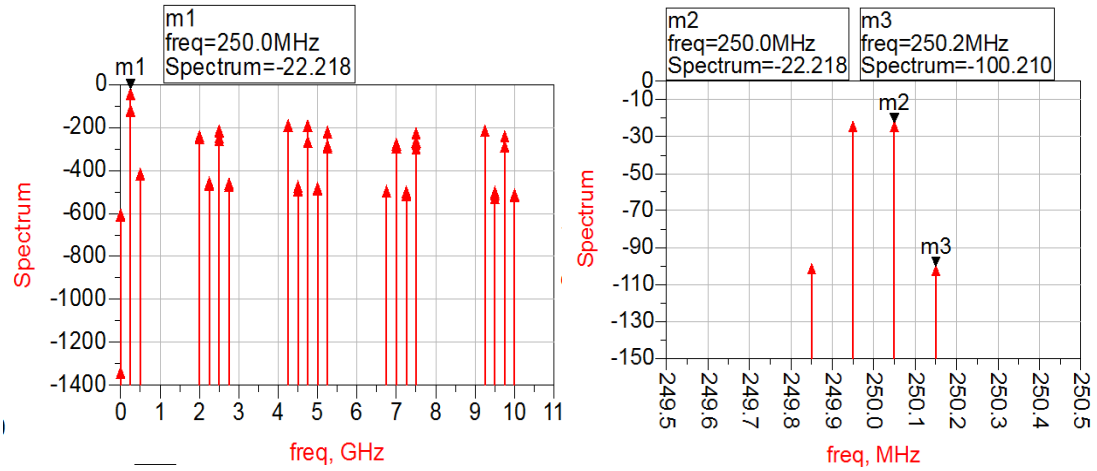

Figure 4.62: Broadband spectrum at output IF port and spectrum near IF frequency

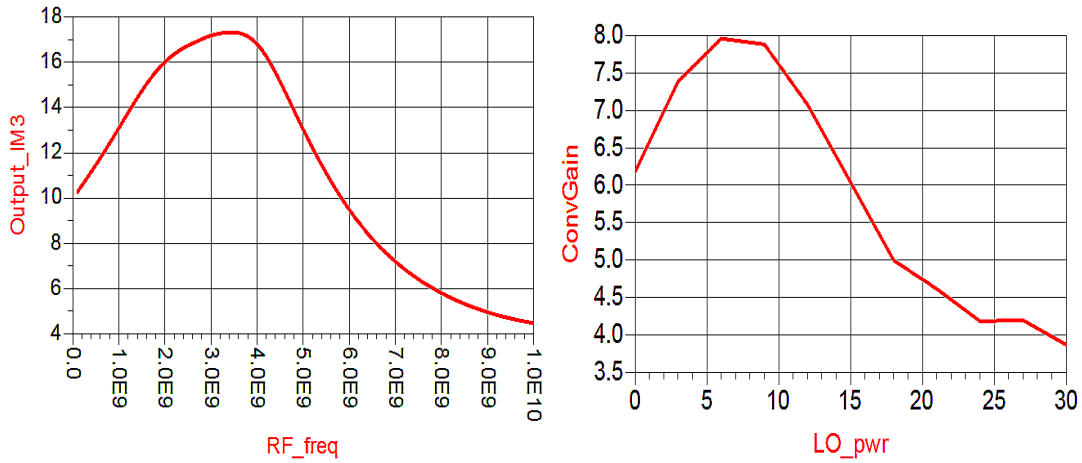

Figure 4.63: Output IM3 (dBm) versus RF frequency (GHz) and Conversion Gain (dB) versus LO power (dBm)

Output IP3 has maximum value ~17.34 at 3.4 GHz RF frequency. The conversion gain is maximum around 8 dBm LO power.

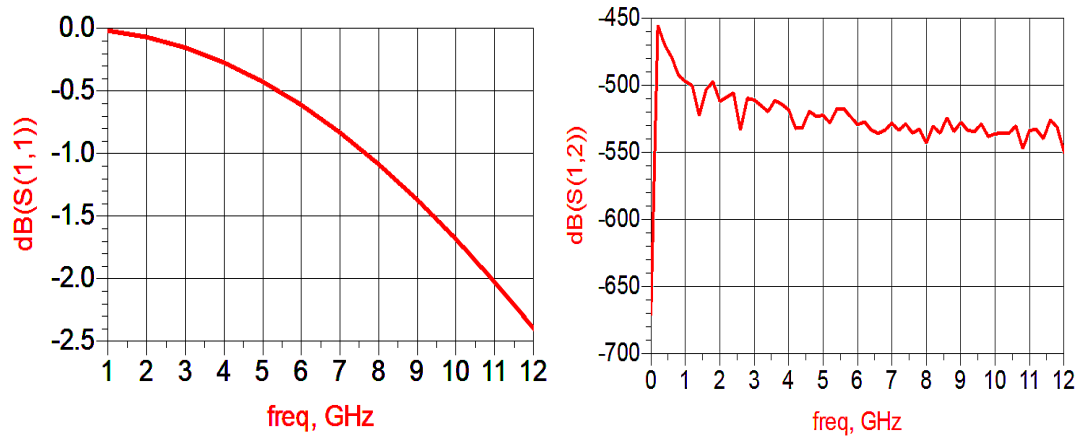

Figure 4.64: S_{11} (dB) versus RF frequency (GHz) and S_{12} (dB) versus RF frequency (GHz)

Figure 4.64 shows the simulated Input RF port return loss and RF-IF port isolation as a function of frequency. S11 obtained is less than 0 dB and S22 is less than -450 dB for the entire frequency range of operation.

4.14 ULPD load with current injection and Inductive Source Degeneration

The circuit is simulated with PMOS load operating in saturation region. Circuit is simulated under identical conditions as that of resistive degeneration based mixer with inductors of 1nH on either side.

Table 4.14: Simulation results for ULPD load with inductive source degeneration based mixer

Conversion Gain (dB)	Input IM3 (dBm)	Output IM3 (dBm)	NF_{SSB} (dB)	NF_{DSB} (dB)	IIP3 (dBm)
7.525	10.737	18.263	8.063	4.67	18.263

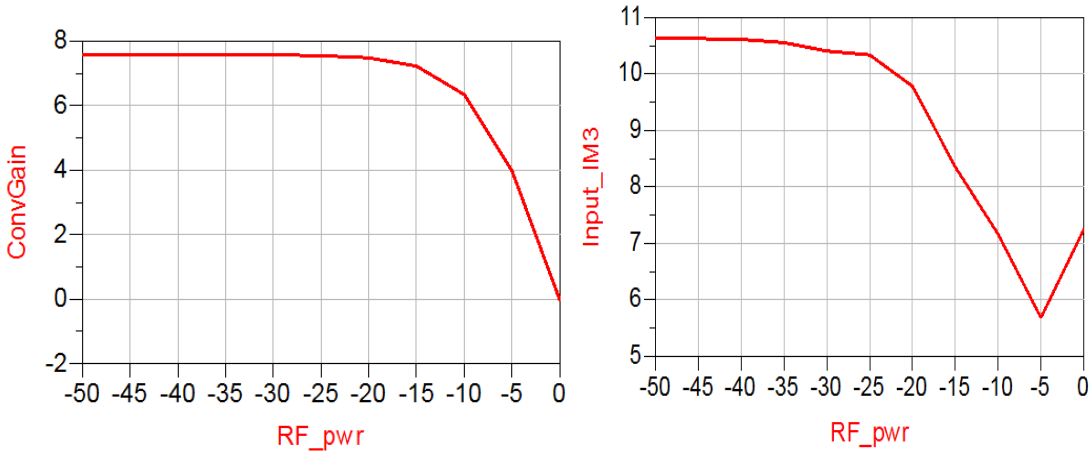

Figure 4.65: Conversion gain (dB) versus RF Power (dBm) and Input IM3(dBm) versus RF Power (dBm)

The variation of the conversion gain (in dB) with input RF power (dBm) is shown in Figure 4.65. The mixer has achieved the maximum gain ~7.5B which maintained its approximately constant up to -15dBm, beyond this point the gain is decreasing with increase in RF power. Figure also shows that IIM3 is ~10.5 dBm below -30 dBm RF power then starts decreasing and reaches its minimum value ~5.7 dBm at -5 dBm RF power.

The simulated plot for Output IM3 is shown in Figure 4.66.The plot has maximum amplitude 18.26 dBm at -20 dBm RF power. The output power versus RF power plot shows that IF power at the output almost increases linearly with increase in input power. Output power at -30dBm RF power is -22 dBm.

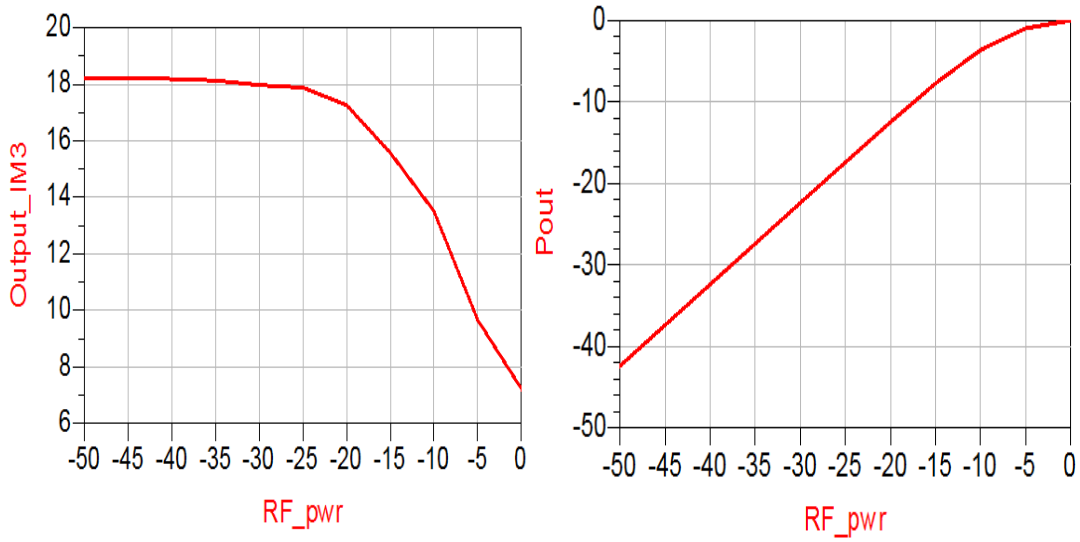

Figure 4.66: Output IM3 (dB) versus RF Power (dBm) and Pout IM3 (dBm) versus RF Power (dBm)

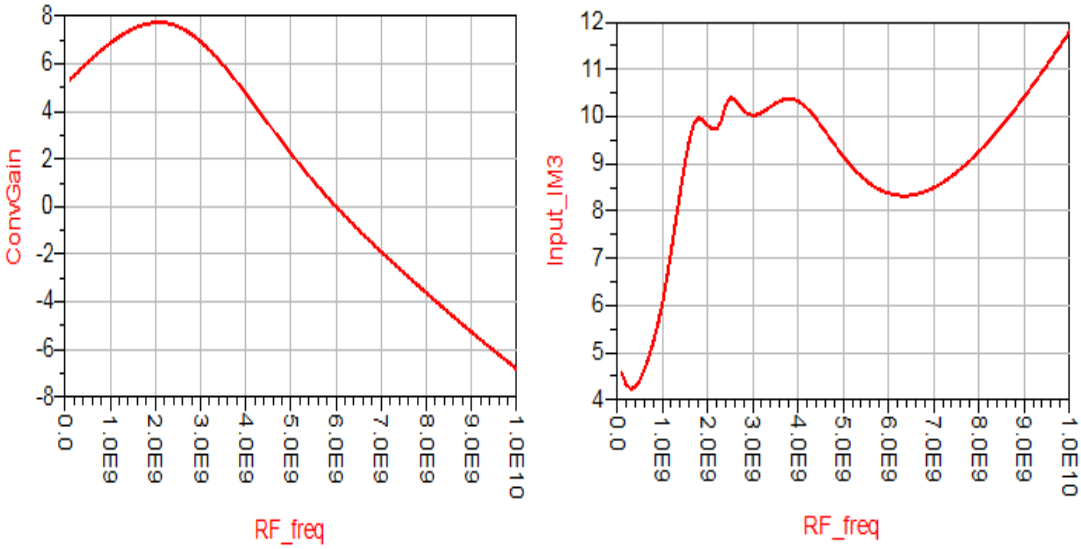

Figure 4.67: Conversion gain (dB) versus RF frequency (GHz) and Input IM3 (dBm) versus RF frequency (GHz)

Figure 4.67 shows the variation of conversion gain (in dB) with RF frequency (in GHz). The positive conversion gain is obtained from 100 MHz to 6 GHz with maximum value ~8dB at 2.1GHz. The mixer achieves the input third order intercept as high as 11.64 dB at 4GHz frequency

Figure 4.68 shows the simulated Input RF port return loss and RF-IF port isolation as a function of frequency. S11 obtained is less than 0db and S22 is less than -600dB for the entire frequency range of operation.

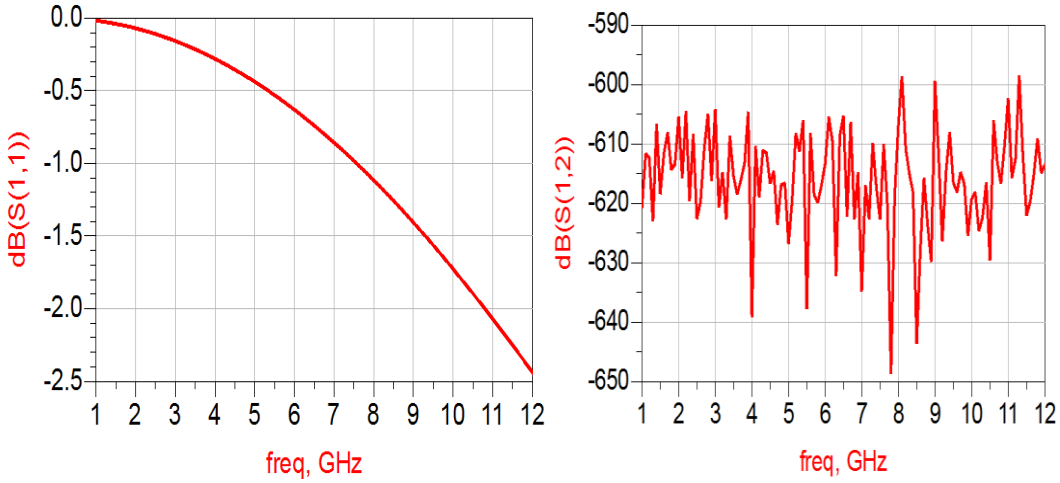

Figure 4.68: S_{11} (dB) versus RF frequency (GHz) and S_{12} (dB) versus RF frequency (GHz)

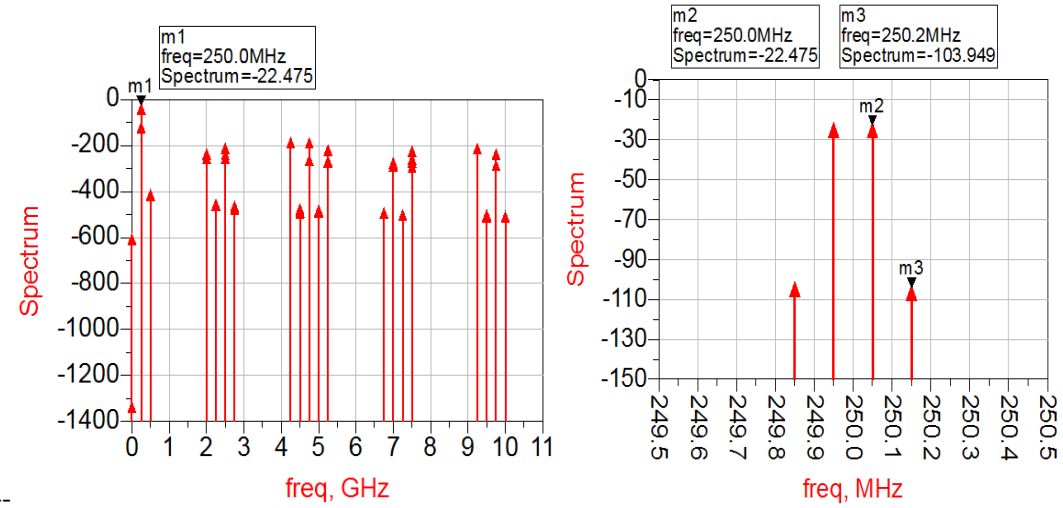

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Figure 4.69: Broadband spectrum at output IF port and Spectrum near IF frequency

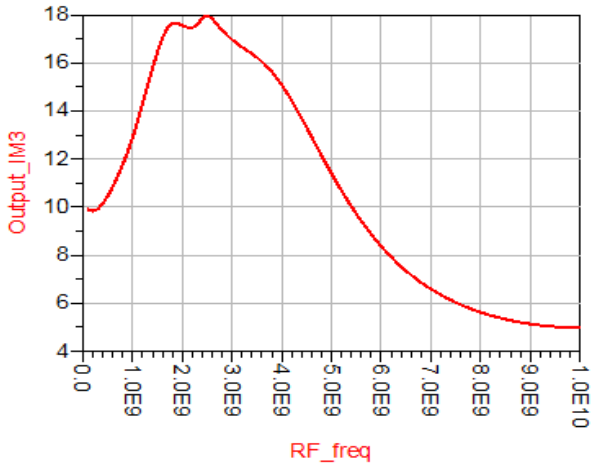

Figure 4.70: Output IM3 (dBm) versus RF frequency (GHz)

Output IP3 has maximum value ~18dBm at 2.5 GHz as shown in Figure 4.70.

Table 4.15: Performance Comparison of Mixers with various Loads

Parameters → / Loads ↓	Conversion Gain (dB)	Input IM3 (dBm)	Output IM3 (dBm)	NF_{SSB} (dB)	NF_{DSB} (dB)	IIP3 (dBm)
***Resistive Load (with Rs)**	10.286	4.473	14.759	8.252	4.828	14.195
Resistive Load (with Ls)	10.845	3.992	14.837	7.883	4.450	14.345
RLC	11.005	7.097	18.102	78.797	5.156	7.662
RC	10.986	6.714	17.70	7.819	4.423	17.7
LC	7.69	5.178	12.86	6.946	3.627	12.867
PMOS	8.328	11.944	20.272	10.390	6.932	19.352
PMOS_R1 R2	16.915	5.374	22.289	8.412	4.96	22.289
Current Mirror	18.266	9.975	28.241	8.405	4.9	22.133
PMOS_R1 R2_C	6.108	8.186	14.294	11.138	7.753	13.485
R1 R2 IB	16.912	5.469	22.38	8.411	4.96	20.123
PMOS Load With Current Injection	19.624	0.760	20.383	8.826	5.316	20.38
ULPD	7.782	8.996	16.778	7.931	4.563	16.46
ULPD with Current Injection	7.525	10.737	18.263	8.063	4.67	18.263

*Note: All configurations use inductive degeneration, except the one in first row.

Table 4.15 shows that maximum gain and linearity is achieved with current mirror load. PMOS load based also provides reasonable gain and linearity and with the use of current injection technique its performance can be further enhanced. While comparing RLC, LC and RC load both gain and linearity are maximum for RLC tuned load but its noise figure is worst among the three. By using resistor at the gate of PMOS load performance parameters can be improved but the expense of area required. when current source is used at the gate of resistor connected diode connected load performance remains almost same ,current source is used for fixing the output voltage .The ULPD load provides good linearity and conversion gain over a wider range. ULPD based configuration also has good noise figure and port to port isolation.

Table 4.16: Performance Comparison of proposed ULPD based mixer Configuration with Other Reported Papers

References / **Parameters**	**This work**	**[35]**	**[36]**	**[37]**	**[38]**	**[39]**
CMOS Technology (µm)	**0.18**	0.18	0.13	0.18	0.18	0.18
CG (dB)	**7.97**	7.5-10.8	3-8	11	15.7	5.9
RF freq (GHz)	**0.5-6**	3.1-8.1	1-10	0.3-25	2.4	1-1.6
Core Mixer Power (mW)	**17**	8	8.4	71	8.1	20.7
S11 (dB)	**< 0**	< -12	-	< -5	-	-
IIP3 (dBm)	**16.46**	-3.4 to -7	-4	-	1	4.1
V_{DD} (V)	**1.8**	1.5	1.2	-	3	1.8

Performance comparison of proposed Ultra Low Power diode (ULPD) based mixer configuration with other reported papers is shown in Table 4.16.

The mixer produces RF to IF port isolation less than -450dB,which is further improved to <-600dB with the use of current bleeding technique. Its IIP3 is also improved from 16.46dBm to 18.263dBm with this technique without any significant change in the conversion gain. At the chosen LO power i.e,5dBm maximum gain is achieved by the mixer.S11 is also less than 0dB with and without using current injection

Table 4.17: ULPD Based Mixer Parameters for different Inductor (L_s) Values (at 2.5 GHz RF Frequency)

Ls (nH)	Conversion Gain(dB)	Input IM3 (dBm)	Output IM3 Point (dBm)
1	7.782	8.996	16.778
5	6.591	11.490	18.081
10	4.217	12.854	17.071
15	2.005	14.319	16.324
20	0.171	15.807	15.978

It is observed from Table 4.17 that linearity of the mixer increases and the corresponding gain decreases as we increase the value of inductor 1nH to 15nH, because of the trade off involved between the conversion gain and the linearity. However, there is a limit up to which Ls (source degeneration inductor) can be increased for linearity enhancement.

Chapter 5

Conclusion and Future Directions

5.1 Summary and Contributions

Comparison of double balanced Gilbert mixers with various loads is performed and observed that for the proposed configuration of mixer designing, high conversion gain as well as linearity can be obtained can be obtained with current mirror load. Lowest noise figure is obtained with LC tuned load. Moreover, tuned load can be used for narrowband operations only. Among the tuned load configurations i.e., RC, RLC and LC, highest conversion gain and linearity is obtained with RLC load.

Gilbert mixer based on the proposed ULPD load provides good performance parameters. It gives reasonably high linearity, good noise performance and small power consumption and adequately large conversion gain can be designed. Besides this, ULPD load enhances the bandwidth of the mixer also.

It is observed that linearity of the mixer increases and the corresponding gain decreases as we increase the value of inductor from 1nH to 15nH, because of the trade-off involved between the conversion gain and the linearity. However, there is a limit up to which Ls (source degeneration inductor) can be increased for linearity enhancement. Current injection technique leads to increase in linearity of the mixer without significant loss of conversion gain.

5.2 Suggestions for future work

In the present work, the double balanced Gilbert mixer circuit is optimized for conversion gain and linearity for various loads by keeping the remaining circuitry same. However better performance may be possible by optimizing the whole circuit according to the loads they use. It can be extended to work well for other parameters as well.

The 0.18µm CMOS process technology used in implementation. Reduction in supply voltage as well as power consumption can be achieved with the use of other recent process technologies like 0.14µm and 0.65µm. The proposed Ultra low power diode load based mixer gives reasonable conversion gain, noise figure, power consumption, bandwidth and linearity. For low voltage operation of mixer with ULPD load emerging multi-V_{th} (Threshold voltage), fully SOI (Silicon on Insulator) CMOS process can be utilized.

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