A

DISSERTATION

on

"Simulation and Analysis of Contact Length Variation in Top Contact and Bottom Contact Organic Field Effect Transistor "

Submitted as a requirement for the practical fulfillment of degree of
Master of Technology

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Submitted By

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DELHI COLLEGE OF ENGINEERING
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as
DELHI TECHNOLOGICAL UNIVERSITY

CERTIFICATE

This is to certify that the dissertation entitled **Simulation and Analysis of Contact Length Variation in Top Contact and Bottom Contact Organic Field Effect Transistor** submitted by **Miss Priyanka Bhati** in the partial fulfillment of the requirement for the award of the degree of M.Tech. in Nano Science and Technology from the Department of Applied Physics, Delhi Technological University, Delhi is a record of candidates own work carried out by her under my supervision.

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DECLARATION

I hereby declare that the work presented in this dissertation entitled **Simulation and Analysis of Contact Length Variation in Top Contact and Bottom Contact Organic Field Effect Transistor** has been carried out by me under the guidance of **Dr. Rishu Chaujar**, Assistant Professor of Engineering Physics department, Delhi Technological University, Delhi and hereby submitted for the partial fulfillment for the award of degree of Master of Technology in Nano Science and Technology at Applied Physics Department, Delhi Technological University, Delhi.
I further undertake that the work embodied in this major project has not been submitted for the award of any other degree elsewhere
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Abstract

Research into organic field effect transistors (OFETs) has made significant advances both scientifically and technologically during the last decade, and the first products will soon enter the market. Printed electronic circuits using organic resistors, diodes and transistors may become cheap alternatives to silicon-based systems, especially in large-area applications.

In OFET organic semiconductor used in the simulation is pentacene which is a p-type semiconductor. It works in the accumulation mode. When gate voltage and drain voltage is applied. This simulation is done with ATLAS. ATLAS is simulation software.

In this thesis work variation in the contact length is observed. How small contact can be obtained. Contact material used in OFET source and drain is Au (Gold). We can reduce the cost by using less amount of Au. If contact length is reduced the cost is reduced. By reducing the contact length we can reduce the geometry of the device. This can be used in the nano organic device.

Chapter 1

INTRODUCTION

1.1 Organic Semiconductors

Organic semiconducting materials have been synthesized and studied for over 5 decades [1]. In the 1950s, drift mobility measurements and the photoconductivity (PC) response of small molecules such as anthracene were examined [1, 2] and although these materials showed semiconducting properties (i. e., conductivities in the range of $10^{-9} - 10^{-6} Scm^{-1}$) [3], their performance and stability were poor. However, with drastic improvements in synthesis and processing of new classes of molecules such as conjugated polythiophenes in the past two decades [4], the prospects of commercially using organic semiconductors (OSCs) in applications such as organic light-emitting diodes (OLEDs), field-effect transistors (OFETs) and the solar cells is now greater than ever.

1.1.1 Organic Semiconductors

Semiconductors based on organic molecular components are mainly composed of hydrogen, carbon, and oxygen. Unlike inorganic semiconductors that are crystalline with band-like charge transport, organic semiconductors are amorphous or polycrystalline in which the charge transport occurs through hopping of charges between delocalized π molecular orbitals.

The semiconducting or conducting properties of organic moelcules can be attributed to the special chemical characteristic of carbon: carbon atoms can form double bonds between each other, as shown in Figure 1.1. One is known as a σ bond formed by the overlap of hybridized sp2 orbitals, and the second is know as a π bond formed by the overlap of the remaining unhybridized pz orbitals. The σ electrons always remain between the carbon atoms, while the π electrons are delocalized over the neighboring molecules in a conjugated system, by which the electrons can gain some freedom to move along the entire chain. The formation of delocalized molecular orbitals defines the frontier electronic levels: the highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO). The HOMO and LUMO levels determine the electrical and optical properties of the organic semiconductor molecules.

Based on different basic units, organic semiconductors can be categorized into two groups: small-molecule organic semiconductors and polymer organic semiconductors. In small molecule organic semiconductors, the carbon atoms form larger molecules typically with benzene rings as the basic

unit and π electrons become delocalized through the molecules, as shown in Figure 1.2(a). The molecular weight of small-molecule semiconductors is usually less than 1000 g/mol. In polymer organic semiconductors as in Figure 1.2(b), the carbon atoms form a long chain and π electrons become delocalized along the chain and form a one dimensional π -conjugated system. The molecular weight of polymeric semiconductors is usually greater than 1000 g/mol.

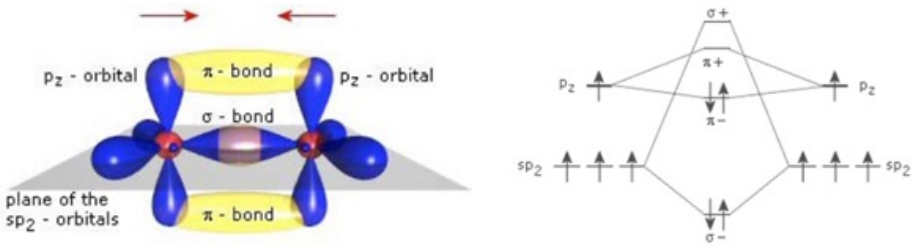

Figure 1.1: Scheme of the orbitals and bonds for two sp_2 hybridized carbon atoms [5]

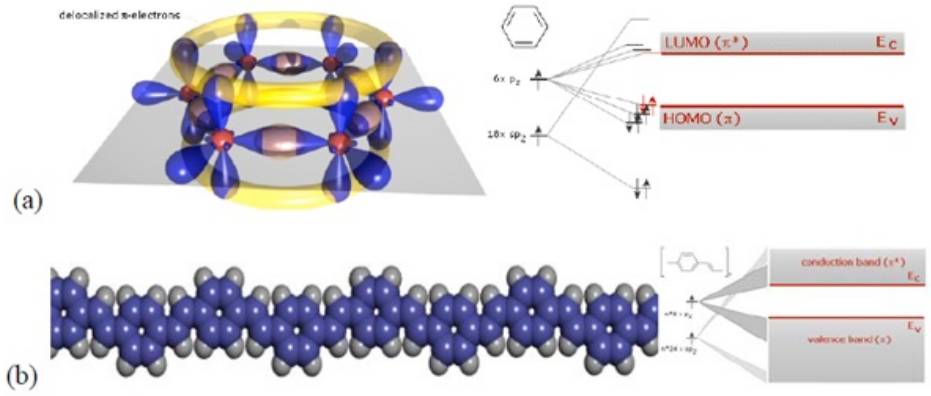

Figure 1.2: (a) Scheme of a benzene ring and energy structure of small-molecule organics. (b) Scheme of a polymer subunit and the energy structure of polymer organics [5]

The discovery of electrical conduction in organic solids dates back nearly 100 years with the observation of photoconductivity and the study of the dark conductivity in anthracene crystals [6, 7]. In 1977, the first highly conducting polymer, chemically and electrochemically doped polyacetylene, was discovered by Heeger, Shirakawa, and MacDiarmid, which won them a Nobel Prize in Chemistry in 2000 [8]. This remarkable observation opened up an entire new field called organic electronics, and a new range of applications for conducting and semiconducting organic materials. Organic electronics generally refers to electronic devices and systems that are based on organic semiconductors, and generally it is applied to three main technological areas: organic light-emitting devices (OLEDs), organic photovoltaic solar cells (referred as OSCs or OPVs), and organic electronic circuits based on organic thin-film field-effect transistors (referred as OTFTs or OFETs). In May 2008, Sony unveiled an ultra thin 11 inch OLED TV with high energy efficiency and brightness [9]. OLEDs could compete

with and eventually replace white and blue GaN-based light-emitting diodes (LEDs) used in mobile phone displays since they do not require backlighting. OPVs are envisioned as future power supplies for large-scale power generation [10]. OFETs have recently gained attention as building blocks for electronic applications that can greatly benefit from lowcost, large-area fabrication and flexible form factors, such as radio-frequency identification tags (RFID) [11], drivers for electronic paper [12] and driving circuits for flat panel displays (FPDs) [13].

1.1.2 OFETs vs. Inorganic Thin-Film Transistors

OFETs, thin-film transistors (TFTs) with organic semiconductors as the active layers, are of great interest as a potential alternative to amorphous Si (α-Si) TFTs. With remarkable progress in the synthesis and purification of organic semiconductors and the processing of these materials into devices, the mobility of the best OFETs has surpassed that of α -Si TFTs [14].

A major advantage of OFETs vs. α -Si TFTs is their compatibility with low-cost, low temperature processes. A typical α -Si: H TFT fabrication process involves the deposition of hydrogenated α -Si as an active layer and silicon nitride as a gate dielectric by plasma enhanced chemical vapor deposition (PECVD) using H_2/SiH_4 (silane) and NH_3/SiH_4, respectively. The process temperature is usually much higher than 250 °C, which enables the use of inexpensive glass as substrate [15]. However, this fabrication process is not compatible with colorless, transparent flexible polymeric substrate materials, which typically require a temperature below 200 °C. OFETs, on other hand, can be processed at much lower temperatures using various simple, low cost techniques, including vacuum thermal evaporation, spin-coating, dip-coating, vapor deposition, microcontact printing, screen printing, etc. The combination of low-temperature processibility with the mechanical flexibility of organic materials thus leads to a wide range of applications in flexible electronics with a potential for very low cost manufacturing.

Secondly, α-Si technology provides only high performance n-channel transport which prevents the use of complementary metaloxidesemiconductor (CMOS) technologies. In contrast, the versatility of synthetic organic chemistry has enabled the tailoring and engineering of both n- and p-type semiconductors, giving rise to many potential candidates for circuit designs based on CMOS technology.

1.2 Organic Field-Effect Transistors

1.2.1 Introduction

Organic Field Effect Transistor (OFETs) is transistor which using organic semiconductor in channel. OFETs have been of great interest for applications, such as display drivers, identification tags and smart cards, because they have advantages of low cost, flexibility and light weight printed electronics, electronic paper (e-paper), electronic skin, etc [16]. A good example of this progress is a 5-order of magnitude increase in the field-effect mobility from 1986 to present [16], making the organic electronic devices a viable replacement for amorphous Si devices.

Despite of improvements in fabrication and characterization of thin-film organic field-effect transistors, the physics of charge injection and transport in these devices is not well understood. Before

we discuss these issues in detail, a basic review of the transistors mode of operation and the different charge injection mechanisms is essential.

1.2.2 Operating mode

OFETs are having four modes are top contact bottom gate(TCBG), bottom contact bottom gate(BCBG), top contact top gate(TCTG) and bottom contact top gate(BCTG). Out of these two are very common TCBG and BCBG.

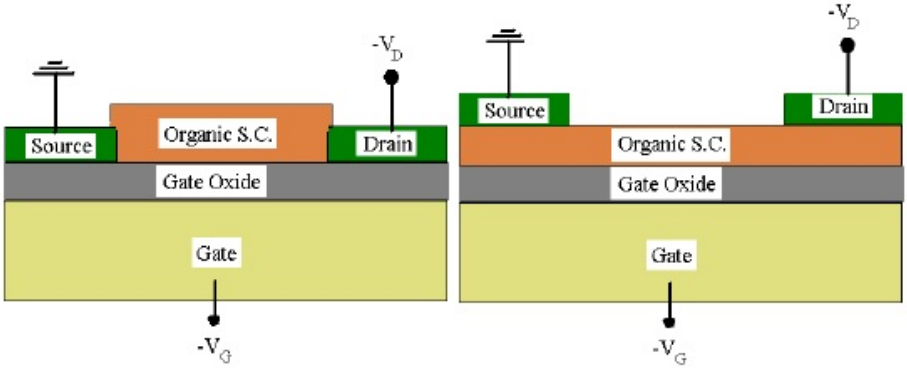

Figure 1.3: (left): A schematic view of a bottom contact OFET. The source electrode is grounded, while the drain and the gate are biased negatively. In this mode, holes are injected from the source and collected at the drain. (right): A top contact OFET with the electrodes patterned on top of the organic polymer.

OFET works in accumulation mode. When gate voltage is applied a charge layer is formed in between this oxide layer and organic layer. This help in current flow when drain voltage is applied. There is a advantage of top contact geometry contact area is large between electrode and organic semiconductor, as compared to the BCBG. But there is one disadvantage also making contact over the semiconductor can damage it, so a safe approach is necessary. Therefore, top contact design is not frequently used.

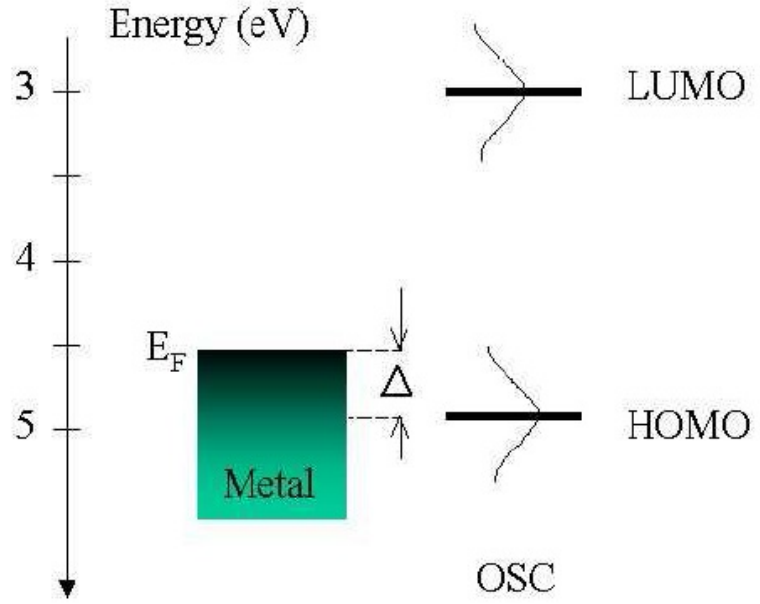

Figure 1.4: The energy diagram showing the band alignment at an OSC/metal interface such as Au/pentacene. Holes are injected from the Fermi level of the metal into a Gaussian energy-dependent state in the HOMO, overcoming an intrinsic energy barrier (adapted from Ref. [3]).

Most OFETs reported in the literature so far show either p-type or n-type behaviour, meaning that the charge carriers are either holes or electrons respectively. P-type OFETs comprise the majority of these devices, showing the best transport properties. However, Very recently, a few groups [17, 18] have shown that ambipolar charge transport is also quite achievable and is a generic property of the OSCs. This can pave the way for fabrication of organic complimentary metal-oxide semiconductor (CMOS) logic circuits.

1.3 Mechanisms of Charge Injection and Transport in Organic Semiconductors

The performance of the organic electronic devices, including thin film field-effect transistors and organic light emitting diodes (OLEDs), depends on the nature of charge injection from the contacting electrodes into the OSC, followed by the effective transport of the carriers through the bulk of the material. In light emitting diodes [19], the effective injection of the holes and electrons from the contacts is followed by transport. Through the bulk, leading to recombination and emission of light. In solar cells [19], holes and electrons are generated upon absorption of light, followed by transport through the device and collection at the electrodes, and in FETs, charge injection at the source is followed by transport through the channel and collection at the drain. Since the underlying principle of operation in all these devices is similar, we will review the different mechanisms of charge injection and transport in the following sections.

1.3.1 Bulk-limited transport

If the contact between the metal and the OSC is Ohmic, with a contact resistance much lower than the resistance of the bulk material, then the current will be easily injected into the organic material and the transport of charge will be dominated by the bulk [19]. By Ohmic contact we mean the electrode, being an infinite reservoir of charge, can maintain a steady state space-charge limited current (SCL) in the device [4]. In the case where the injected charge dramatically changes the electric field configuration in the polymer (i.e., effectively screens the source-drain field) the transport becomes space-charge limited. In this case, the I-V curves look linear if the field due to the applied bias is the dominant E field in the device. The conduction is usually linear in the low source-drain bias since the current density in the polymer is low. At higher fields where the current density is very high, there is a significant concentration of charge carriers in transit between the source and the drain. The screening due to these space charges produces nonlinear I - V characteristics.

It is important to note that space-charge effects are more readily maintained in materials such as organic semiconductors where the mobility is poor. The low mobility greatly restrains the collection of the carriers at the drain or the recombination of opposite charges. In addition to these effects, OSCs are known to have large concentration of highly localized states (i.e., traps, defects etc) that trap mobile charges temporarily or permanently (immobile charges) [4]. All these factors make organic semiconductors the perfect breeding ground for space-charge transport.

1.3.2 Hopping nature of transport in organic semiconductors

The presence of defects and the non-crystalline structure of the organic polymers leads to the formation of localized states. In order to move, charges must hop between these localized states and overcome the energy difference between them, emitting or adsorbing phonons during intra-chain or inter-chain transitions [13].

In OSCs, the constituting molecules are only weakly bound together through van der Waals forces and the traditional view of band formation is not very accurate. In these materials, band energy widths are typically smaller than k BT [4].

In this simple picture, a carrier is initially localized at a particular energy site i, confined approximately within a deep or shallow potential well. Upon receiving enough thermal energy, the carrier can overcome the potential barrier and hop over to a neighbouring site, j. This process is illustrated by the cartoon in Fig. 1.5. Thermally assisted hopping is the dominant mechanism of transport in organic semiconducting materials. Therefore, the mobility and hence the conductivity of (disordered) OSCs exponentially increase with temperature, which is different from temperature dependence of conductivity in crystalline semiconductors such as Si or Ge. The picture of hopping described above is greatly simplified. In reality density of states and the possibility of both short and long range hops to neighbouring sites should be considered [18].

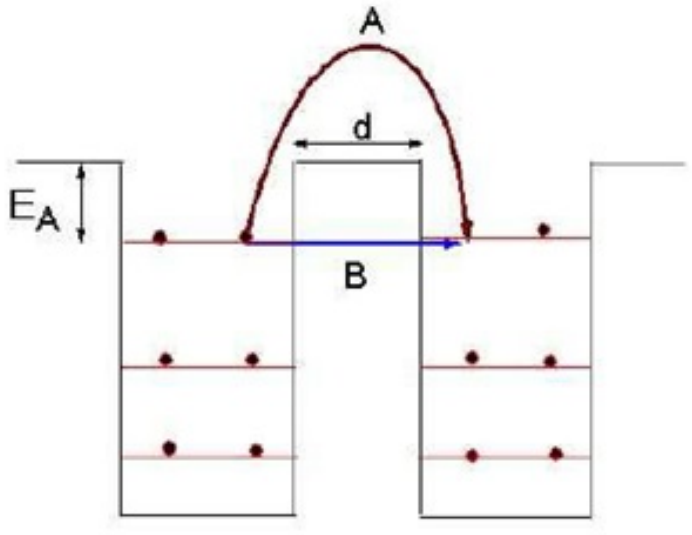

Figure 1.5: Two mechanisms of charge transfer between two localized states: A) Hopping of a charge carrier from one localized state to another upon receiving enough energy to overcome the activation energy barrier E A, and B) direct tunnelling between the 2 states.

1.3.3 Injection-limited transport

In addition to the intrinsic (bulk) properties of the semiconducting polymers in transporting the electronic charge, the interface between the OSC and the contacting electrode (usually a electronic devices. If the bottleneck in charge transport is injection at the contacts, a device is said to be injection or contact limited. In this case, the metal/OSC interface may show Ohmic or nonlinear I-V characteristics. The band offset between the metal work function and the HOMO or LUMO level in the OSC (depending on whether the transport is p- or n-type) is one important factor in determining the type of contact at the interface [3, 20]. If there is a sizable potential energy barrier from the metal into the transporting band in the OSC, the charge injection would be poor and the contact resistance will dominate the device operation. However, many factors such as electrode work function, doping levels, interfacial traps or dipoles etc. influence the band alignment at the interface.

1.4 This Thesis

- Chapter 2 Literature review, contain review of gate dielectric material, influence of higher gate dielectric which reduce the threshold voltage. Flexible gate dielectric for flexible application like display and many more. Threshold voltage and its dependency. Printable circuits and some other application of OFET.

- Chapter 3 Pentacene, structure of pentacene. Charge transport in pentacene. The influence of non-idealities on charge transport like trap, electrode material and electrode geometry. Why

pentacene is P-type. Standing v/s tilt pentacene.

- Chapter 4 Methodology of device simulation contain which method is used to find I_dV_G characteristics of OFET. ATLAS is used in the simulation of OFET.

- Chapter 5 Result and Discussion for top contect contain the channel length modulation. What happen when channel length is varied. Effects on the I_dV_G graphs

- Chapter 6 Result and Discussion for bottom contect contain the channel length modulation. What happen when channel length is varied. Effects on the I_dV_G graphs

- Chapter 7 Conclusion and future prospects.

Chapter 2

LITERATURE REVIEW OF GATE MATERIAL AND SOME OTHER APPLICATIONS OF OFET

The principle of the field-effect transistor (FET) was first proposed by Lilienfeld in 1930. First descriptions of the field effect in organic semiconductors was on 1970, organic FETs (OFETs) have only been identified as potential elements of electronic devices the report by Koezuka and coworkers, in 1987, on a structure based on electrochemically polymerized polythiophene. Polythiophene belongs to the family of conducting (or conjugated) polymers (CPs) that were discovered in the late 1970s.

Now a days small conjugate molecule are also promising material for this application. The performance of OFETs has continuously improved since then, and some OFETs now compete with amorphous silicon FETs, which are now preferred to conventional crystalline silicon FETs in applications where large areas are needed[21].

2.1 Gate Insulator

Different dielectric plays different role in OFET. As in inorganic transistor gate insulator used are SiO_2, Al_2O_3, and HfO_2, various organic materials were also tried for the gate dielectric in OTFTs. In addition, polymethyl methacrylate (PMMA) derivative polymers are one of the new materials for the gate dielectric or buffer layer, exhibiting high field effect mobility and low threshold voltages. Miskiewicz et al. have demonstrated that the surface energy of the dielectric can have large impact on the performance of FETs based on TTF 4SC 18 [22]. Average charge carrier mobility was 30 times increased as a result of proper treating.

2.2 Influence of higher dielectric constant

To use high dielectric constant proper interaction for organic layer and strength is necessary. Another advantage of high materials is a lower operating voltage. There has been shown very clearly the beneficial role that plays the high dielectric constant tantalium oxide (Ta_2O_5) as a gate insulator

in OFETs. It has been shown that using high gate structure provides possibility of injection a higher amount of charge carriers into organic active layers than on the SiO_2/Si gate conventionally used in most OFETs.

2.3 Gate dielectrics on flexible substrates

Generally we use SiO_2 for OFET, and this is grown over inflexible substrate. To make it flexible for flexible electronics, Parashkov et al. have fabricated fully patterned all organic TFTs with a variety of organic polymer insulators and the gates printed on top of the gate dielectric layer. The group has produced OTFTs on flexible polyimide substrates and obtained devices with electrical performance similar to that of OTFTs fabricated with inorganic gate dielectrics and metal contacts.

Majewski et al. have investigated bottom-gate OFETs using a commercially metallized Mylar films coated with an ultra-thin (3.5 nm) SiO_2 layer as a flexible substrate. The OFETs have been fabricated using this substrate, region regular poly(3-hexylthiophene) (rr-P3HT) as a p-type semiconductor, and gold source and drain contacts. This resulted in OFETs that operated with voltages of the order of 1 V.

2.4 Threshold voltage

The threshold voltage V_T is an important parameter that needs to be controlled to ensure proper operation of the circuits. V_T can depend on the time a gate voltage has been applied (bias stress), on the exposure of the device to light, it can be shifted using a polarizable gate insulator or it depends on thickness of the semiconductor layer. Furthermore, a dependence on the work function of the gate electrode has been reported. V_T voltage additionally has been found to depend strongly on the preparation of the surface on which the organic material is deposited. Threshold voltage shifts in thin film as well as single-crystal OFETs have been found to be induced by dipole monolayers on the gate insulator [22]. Thickness of the semiconductor layer influences the values of the threshold voltage and, to a lesser extent, the saturation current. The thickness-dependent part of the threshold voltage results from the presence of an injection barrier at the gold-pentacene contact.

2.5 Printing of circuits

Many printable circuit are there in market now. One example is given by Knobloch et al. [23], which have designed structural and electrical properties of printed polymeric thin films and multilayer to set up PFETs. A fully printed functional integrated circuit in the form of a seven-stage ring oscillator has been presented. The layers have been based on solution processible polymers and filled polymers, which were processed by traditional graphic art printing techniques such as pad printing and blade coating. The circuit layout has been designed to match the characteristics of the applied printing and coating process, so that polymer transistors, inverters, and ring oscillator circuits could be achieved. When applied to OTFT fabrication, all or parts of the transistors constituents, i.e., electrodes, gate

dielectrics, and semiconductors, can be solution processible.

Kim et al. [24] have demonstrated OTFTs based on the ink-jet printed electrodes in which a reduced channel length was accomplished by laser ablation. The carrier mobility values of the fabricated OTFTs with channel lengths of 10, 20, and 50 m were 4.810_{-3}, 4.610_{-3}, and 3.410_{-3} cm2/Vs in the saturation regime, respectively.

2.6 Some applications of OFETs

In the research point of view OFET is still under improvement. There are lot of applications some of them are presented here memory and logic elements, LCD panel driven OTFT and OFETs as chemical sensors. Anthopoulos et al. 25] have shown that organic transistors based on the solution processible methanofullerene [6,6]- -phenyl-C71-butyric acid methyl ester exhibit promising ambipolar charge transport characteristics. This structure was found to allow the realization of logic circuits with good noise immunity. Pinto et al. [26] have shown that a spin coated rr-P3HT single channel split gate OFET functioned as a dual input logic AND gate with an order of magnitude higher mobility. A significant advantage of this architecture is that AND logic devices with multiple inputs can be fabricated using a single rr-P3HT channel with multiple gates. The reversible memory effect due to extrinsic trap states and the bias stress effect originate from totally different mechanisms and can be separated in data analysis [27].

Write-once-read-many-times (WORM) memory devices have been demonstrated using a material system of polyethylene dioxythiophene:polystyrene sulphonic acid and a con- jugated copolymer containing fluorene and a chelated euro- pium complex. Some rewritable devices are characterized by embedding nanoparticles, while others are characterized by the intrinsic memory effects of the materials. The former devices are nanoparticle-based organic memory units in which the organic materials themselves have no memory effects. This flexibility provides, in a single class of material, the ability to achieve complementary logic and even devices such as p-n diodes and more complex systems. Complementary inverter based on interface doped pentacene has been shown to be promising device, which has been demonstrated in[28].

Hur at al. [21] have studied p-channel, n-channel, and ambipolar SWNT FETs with electrodes defined by a high-resolution printing process. Complementary logic gates with these types of devices illustrate their suitability for complex circuits.

Functionalised Graphene electrodes are also used for transparency, light weight and flexibility. The next generation will be of organic because its fabrication is much easier than Si. As mentioned above printable circuit and ink jet printable circuit is possible. You are able to print the circuit anywhere on a plastic substrate.

2.7 Conclusions

Many groups demonstrated the important functionalities of organic gate dielectrics and their effect on the output performance of OFETs. For instance the polymer dielectric that was directly attached to the pentacene layer governed the transport and accumulation of charge carriers. The mechanisms by which PVA facilitates the formation of the n channel in the pentacene active layer biased in the accumulation at the positive VG regime are not completely established as yet. There has been shown very clearly the beneficial role which plays high dielectric constant Ta_2O_5 as a gate insulator in OFETs.

In order to conduct research on physical effects occurring in organic semiconductors, most recent works involving OTFTs have typically employed the selective deposition of metallic conductors through a shadow mask or vacuum deposition followed by photolithographic patterning, an approach that is both time consuming and costly. Hence, it is highly desirable to achieve high-performance especially n-channel OFETs that can be processed at room temperature using standard physical vapour deposition. Light emission from an OFET requires ambipolar transport, as well as efficient radiative decay. Recent experiments have demonstrated ambipolar channel conduction and light emission in conjugated polymer FETs. These achievements make realistic fabrication of suitable in commercial applications the complex active matrix with organic light-emitting diodes (AMOLEDs)[29].

Chapter 3

CHARGE TRANSPORT IN PENTACENE LAYER

Pentacene (from penta=5 and acene=poly cyclic aromatic hydrocarbons with fused benzene ring) is a flat like molecule made up of five linearly fused benzene ring. Interest in pentacene has grown dramatically in recent years as a result of both crystal and thin film behaving as a p-type organic semiconductor which can be employed to manufacture electronic device such as the organic field effect transistor (OFET).

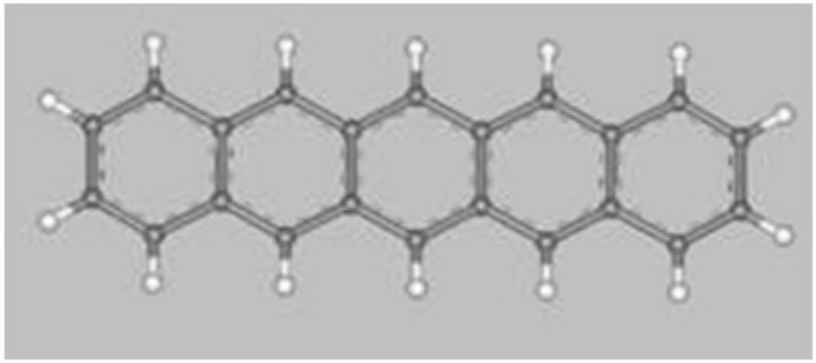

Figure 3.1: Pentacene

Structure Pentacene ($C_{22}H_{14}$) contains only carbon and hydrogen atoms. Its structure is represented in figure 3.1. Pentacene belongs to a group of molecules called polycyclic aromatic hydrocarbons [30]. Molecules of this group have several hydrocarbon rings in which the carbon atoms are alternatingly connected by carbon double and single bonds. More specifically, pentacene is the fifth member in the group of fused benzene rings in a linear arrangement, called the acenes. The first four members are benzene, naphtalene, anthracene and tetracene. Above five rings a linear arrangement becomes less stable and therefore less abundant. The alternation of double and single bonds, also called conjugation, is a result of a specific atomic electronic configuration. In general the electronic configuration of carbon is given by $2s^{22}p^2$. Inconjugated structures two of the three p orbitals of the carbon atom hybridize with the s orbital to form 3s patially localized orbitals. The three orbitals are located in the same plane and the angle. Between n the orbitals is equal, 120. These orbitals are mainly responsible for chemical bonding between carbon atoms. The p orbital left, usually called the pz or-

bital, is spatially localized above an d below this plan e. In conjugated systems these pz orbitals also contribute to chemical bonds in the plane. However, such a bond is much weaker than bonds made from the hybridized orbitals. Therefore, these electrons can also contribute in electronic conduction. This explains the relatively high conductivity of a sheet of graphene. Thermodynamically speaking, pentacene is quite stable. When storing at room temperature in air only one significant impurity species will form, 6,13-pentacenequinone. This species is quite different from pentacene itself due to the attachment of two oxygen atoms and has lost its full conjugation. The quinone can be removed by vacuum sublimation. Pentacene is a crystalline solid at room temperature. In general, pentacene crystals have a triclinic crystal system and have four distinguishable Phases or symmetries [31]. Crystals are composed of layers, in which the long axis of the molecule is oriented almost perpendicular to the plane of the layer. In-plane pentacene molecules are arranged in a herringbone-like way. The relative orientation of the hydrogen atoms between molecules and the angle of the long axis with respect to the plane determine the specific phase of the crystal. Phases are characterized by the spacing between stacked layers, d. The four phases are characterized by d-values of 1.41 nm, 1.45 nm, 1.50 nm and 1.54 nm. Thin films structures can depend on temperature and substrate and the 1.41 nm is most likely to form. Single crystals of pentacene can be grown by vapour transport growth [32]. Thin films of pentacene show an island-type growth mode (Stranski Krastanov), resulting in thin films composed of crystalline grains with typical dimensions of several micrometers depending on substrate and substrate temperature during or after deposition [33].

3.1 Charge transport

3.1.1 Space charge limited current

How to think about charge transport in pentacene? Lets consider the problem in a band picture. Pentacene has a filled valence band (or in molecular terms highest occupied molecular orbital, HOMO) separated from an empty conduction band (in molecular terms lowest unoccupied molecular orbital, LUMO) by a band gap of 2.2 eV which is much larger than kbT=0.03eV (298K). One can inject carriers by either injecting electrons in the conduction band or holes in the valence band. We consider one carrier injection, since pentacene is a hole conductor, or p-type semiconductor.

Metals usually have a lot of intrinsic carriers which are free to move throughout the material, since there are many empty states just above the Fermi level. Pure semiconductors have a band gap and the number of charge carries is limited. Injecting a charge carrier in a semiconductor will give rise to a so called space charge. An increase in the electric field will inject more charge carriers, which space charge will increase the electric field even more giving rise to a current which is quadratically dependent on voltage. The current will be bulk limited. This is in contrast to Ohmic conductors which have a linear dependence on voltage and are injection limited. The quadratic behaviour is also known as space charge limited current (SCLC)

The influence of non-idealities on charge transport

This section will qualitatively describe the influence of three non-idealities on charge transport in pentacene which are important in our case:

- The influence of traps
- The influence of the electrode geometry
- The influence of the electrode material

Traps

The band model above assumes a SC with a gap without (impurity) states in the gap. In reality states will be present. For pentacene thin films the most well known impurities causing trap states in the band gap are water, oxygen and grain boundaries between crystalline islands [32] [34] [35] [36] [37]. The effects of water and oxygen on charge transport are described by Jurchescu et al. [34]. Air can reversible diffusive in pentacene and affects electrical transport significantly. Water reduces electrical transport, because its electric dipole induces energetic disorder and traps charge carriers. Oxygen on the other hand enhances electrical transport and attracts electrons, thereby forming holes. The effect of oxygen can even be enhanced in the presence of light. When exposing a pentacene layer in ambient air to light, current increases by about a factor of two. The polycrystalinity in pentacene thin films causes a non uniform dielectric medium. Minari et al. [38] report an enhancement of mobility (and current) in pentacene thin-film transistors when they are made from a single grain as compared to polycrystalline ones.

Electrodegeometry

To investigate charge transport one can contact a material in several ways. Because of the relative high resistivity of organic SCs, the contact resistance and the resistance of the leads can often be neglected. The most straightforward way of applying contacts to a piece of material is to clamp a thin sheet of material between two electrodes such that the current is flowing perpendicular to the sheet. A major advantage of this geometry is the electric field uniformity. Also, one can easily make large contact areas (A) and thin films (L) such to increase the total current, since R L/ A. Another geometry can be obtained by connecting a sheet of material laterally. In a lateral geometry, the electrodes are attached on top or below the sheet of material such that the current is flowing in the plane of material. The ultimate advantage of this geometry is that one can use multiple electrodes, which is one of our demands. However, the conductance path in this geometry is not well defined since the electric field is not completely homogeneous [39]. The non-uniformity of the electric field in a lateral geometry is caused both by the electrode shape, usually a strip with sharp edges, and by the influence of the substrate. Lateral geometries can be made either by applying electrodes on top or below a film. Applying electrodes on top of pentacene might damage the pentacene and cause an ill defined metal-electrode interface [40].

Electrodematerial

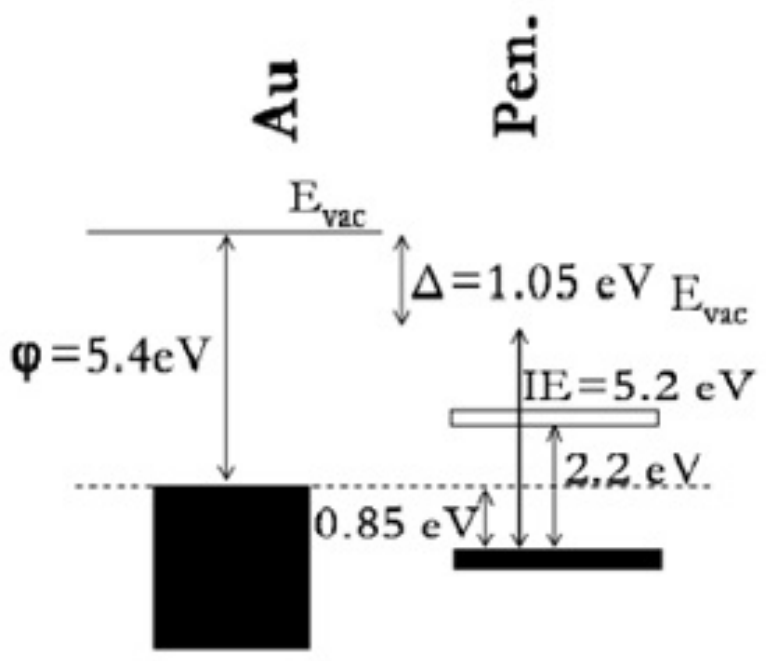

Figure 3.2: Band pictures of pentacene connected to gold. The band picture predicts the effective hole injection barriers. The Fermi level is indicated by the dotted line. G old data is obtained from Koch et al. IE is the ionization energy and is a dipole that arises at pentacene-metal interfaces, which will effectively change the vacuum level.

Pentacene is a hole conductor, since the cation of pentacene (a pentacene molecule missing one electron) is more stable than the anion of pentacene (a pentacene molecule with one additional electron). The easiest way to inject holes in pentacene is to connect it with an electrode which Fermi level is close to the HOMO of the pentacene. We use the same electrode material for the cathode and the anode gold. Schematic energy diagrams of these three situations without bias are given in figure 3.2. In this picture we assume that pentacene maintains its molecular properties, such that the levels are not broadened. Due to a dipole at metal-pentacene interfaces the electrons in both materials experience a different vacuum level. This dipole is formed due to electron transfer from pentacene to the metal. The contacts in the simplified model of figure 3.2 are clearly non-Ohmic and a hole-injection barrier appears of 0.85 eV for a gold/pentacene interface. When introducing a tunnel barrier in between the metal and the pentacene, a dipole will be formed between the oxide and the pentacene. However, the dipole between the pentacene is strongly reduced [41]. Now, charge carriers can cross this barrier by an inelastic tunnel process. In the band picture, at high positive biases a triangular shaped electron barrier arises and one might expect electron injection. Pentacene field effect transistors using both hole and electron injection contacts report pronounced increase of drain currents at large values for the drain-source voltage [42] [43].

Pentacene is having both e- and holes, both can move freely in the pentacene. Hopping of these is by quantum mechanical tunnelling effect. Electron mobility is much lower and even negligible in air

for two reasons.

1. Electron in its lowest unoccupied molecular orbital LUMO is very reactive to H2O molecule which are present in ambient air.

2. Hydroxyl group R-OH at semiconductor insulator interface to act like e- trap which immobilize the negative charge carrier.

Therefore pentacene is p-type only.
Pentacene is most commonly use material in OFET because mobilities for pentacene OFET is range between 0.1cm/Vs and 1cm/Vs have been reported by many groups worldwide. In spite os enormous activities in synthesising and screening for new material for transistor application, pentacene has successfully defended its leading position for the production of OFET[44].
SiO_2 gate dielectric also plays important in accumulation layer between semiconductor/dielectric interface. Pentacene OFET works in hole accumulation i.e. a sufficiently negative voltage (VG) is applied to gate, accumulating holes at the pentacene/SiO_2 interface.
Arrangement of pentacene on SiO_2 shown in figure 3.2 standing and tilted pentacene give mobility value higher. Because in benzene ring -electron reside in molecular orbital (MOs) that have a node in the plane of the molecule and extended into space on other side indicated in figure 3.3. it is clear from figure that standing position of pentacene is better than lying position[46].

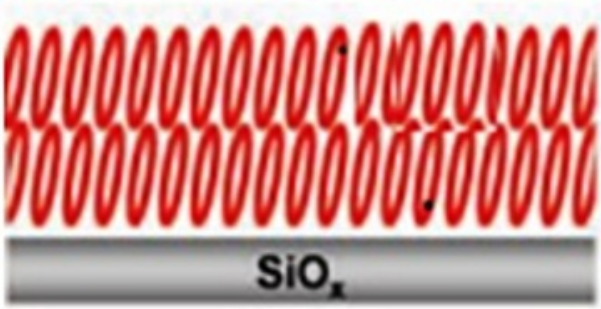

Figure 3.3: Pentacene on SiO_2

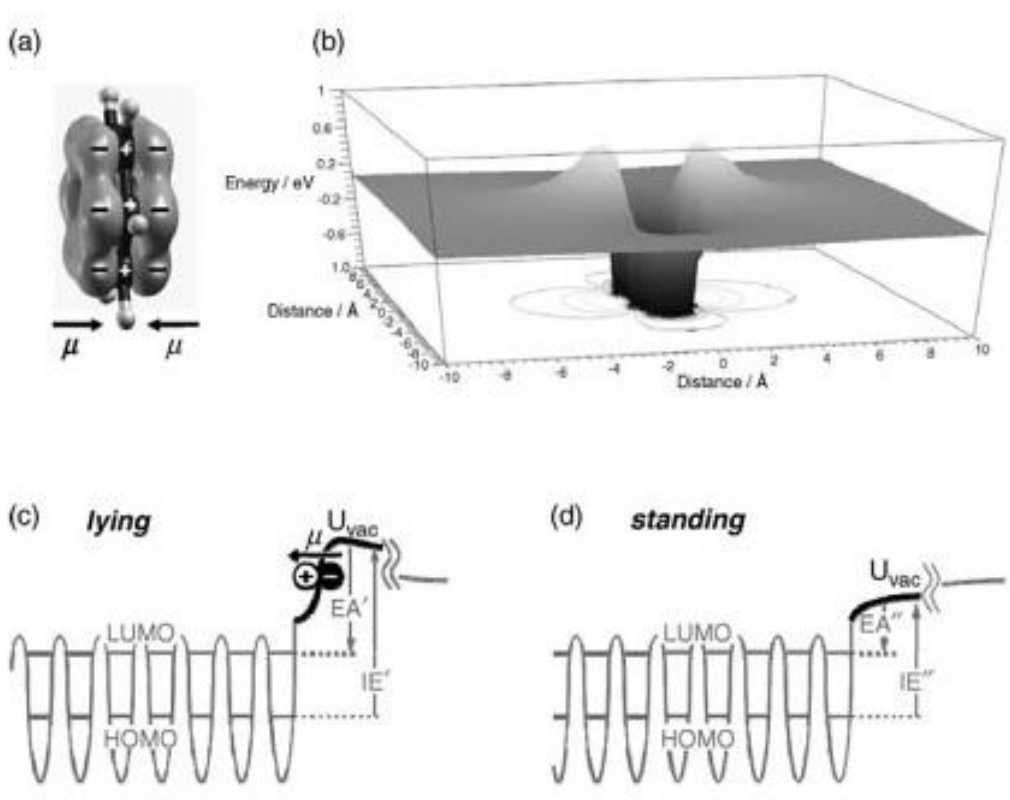

Figure 3.4: (a) Schematic of the quadrupolar charge distribution within benzene (C_6H_6) molecule (b) Plot of calculated electron potential energy in a plane cutting through the molecule (c) Sketch of the energy level in an ordered molecular assembly where the planes of the molecular coincide with the exposed surface. The dipole layer with negative -electron clouds above the positive molecular planes terminates the surface. Also indicated are the highest occupied (HOMO) and the lowest unoccupied molecular orbital (LUMO) as well as the ionization potential (IE) electron affinity (EA), and the electron potential energy in the vacuum immediately outside the surface(U_{vac}). (d) Same as (c) with the planes of the constituent molecule perpendicular to the exposed surface. The energy difference from HOMO and LUMO to U_{vac} IE and EA are smaller than that in (c)[47].

Chapter 4

METHODOLOGY FOR SIMULATION OF OFET AND RESEARCH OBJECTIVE

4.1 Introduction

Simulation of OFET is done with the help of ATLAS. ATLAS provides facility for physically-based two (2D) and three-dimensional (3D) simulation of semiconductor devices.

Physically-based device simulators predict the electrical characteristics that are associated with specified physical structures and bias conditions. This is achieved by approximating the operation of a device onto a two or three dimensional grid, consisting of a number of grid points called nodes. By applying a set of differential equations, derived from Maxwells laws, onto this grid you can simulate the transport of carriers through a structure. This means that the electrical performance of a device can now be modeled in DC, AC or transient modes of operation.

There are three physically-based simulations. These are:

- It is predictive.
- It provides insight.
- It conveniently captures and visualizes theoretical knowledge.

Physically-based simulation is different from empirical modeling. The goal of empirical modeling is to obtain analytic formulae that approximate existing data with good accuracy and minimum complexity. Empirical models provide efficient approximation and interpolation. They do not provide insight, or predictive capabilities, or encapsulation of theoretical knowledge.

Physically-based simulation has become very important for two reasons. One, it is almost always much quicker and cheaper than performing experiments. Two, it provides information that is difficult

or impossible to measure.

The drawbacks of physically-based simulation are that all the relevant physics must be incorporated into a simulator. Also, numerical procedures must be implemented to solve the associated equations. These tasks have been taken care of for ATLAS users. Most ATLAS simulations use two input files. The first input file is a text file that contains commands for ATLAS to execute. The second input file is a structure file that defines the structure that will be simulated. ATLAS produces three types of output files. The first type of output file is the run-time output, which gives you the progress and the error and warning messages as the simulation proceeds. The second type of output file is the log file, which stores all terminal voltages and currents from the device analysis. The third type of output file is the solution file, which stores 2D and 3D data relating to the values of solution variables within the device at a given bias point [45].

4.2 ATLAS Inputs and Outputs

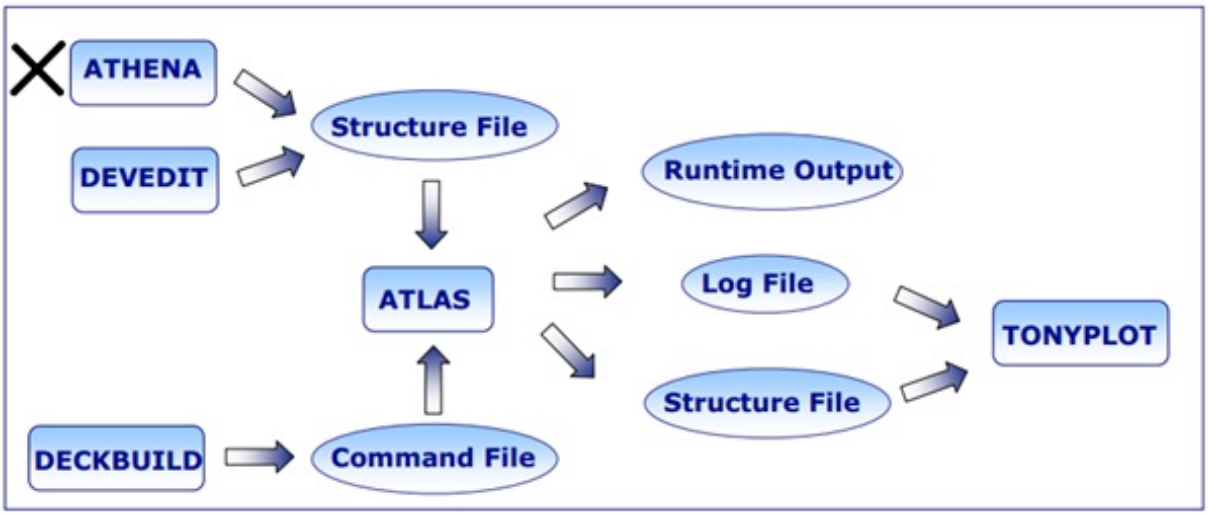

Figure 4.1: ATLAS input and output

4.3 Devedit 2D and Atlas

In my project devedit 2D version 2.6.0.R is used to design the structures of OFET. And for the simulation purpose Atlas version 5.16.3.R is used.

DevEdit can be used to either create a device from scratch or to remesh or edit an existing device. DevEdit creates standard Silvaco structures that are easily integrated into Silvaco 2D or 3D simulators and other support tools. Simulating these structures allows device engineers to examine spread and corner characteristics of devices. DevEdit batch mode allows semi-automatic remeshing of existing structures. DevEdit significantly reduces simulation by remeshing process simulation

structures prior to device simulation. Similarly, DevEdit saves process simulation time by mirroring, stretching or cloning a partial structure or by joining several structures to form a complete device.

DeckBuild is an interactive runtime and input file development environment. Finally TonyPlot is used to view the output or results of the simulation like characteristics plot etc.

Researchobjective

The goal of this work is to investigate, through device simulations and a literature study, device characteristic by varying channel length of OFET. The main advantage of this is by varying the contact length we can determine the smallest contact for the geometry. And this can help in the device scaling. For device in nano range is important for the future technology. But there is short channel effect when we reduce the channel length. So reduction in the contact and maintaining the channel length so that the short channel effect in the device will not occur is the future objective.

Chapter 5

RESULT AND DISCUSSION FOR TOP CONTACT

Higher contact length reduces contact resistance but large contacts (sometimes as large as a millimeter) greatly increase the device size and consume more contact material (e.g., Au). Here, we take top contact OFET and bottom contact OFET for contact length variation. Parameters use in the structure of the OFET are length of the device is 90 micro meter. Width of the gate is 20 nano meter and material of gate electrode is aluminium, width of the gate oxide is 300 nano meter material used in the gate oxide is SiO_2, organic material is pentacene thickness of pentacene is 100 nano meter, source and drain thickness is 20 nano meter, length is varied over 5 micro meter to 40 micro meter.

5.1 Top contact OFET

As contact length increases source and drain resistance start decreasing this decrease in resistance current increases drain current. As shown in figure 5.1 the contacts length is 40μm. The I_d/V_g graph is shown in figure 5.2 sweep from -30V to -10 volt there is a slow increase in the I_d because at higher V_g source and drain resistance is proportional to the contact length. Channel becomes more current demanding and effective charge injection areas balance the source and drain resistance and the channel resistance. Now the source and drain resistance is more in compare to the channel resistance. After -10V there is a steep increase in the current. There is no drastic change in the resistance after -10 volt and the channel is also not current demanding as like higher voltage.
When contact length is decreases by 5μm as shown in figure 5.3 current start decreasing showed in figure 5.4. Resistance increase by decrease contact length. When channel length becomes current demanding transistor characteristic become contact limited current started decreasing as shown in figure 5.6, 5.8, 5.10, 5.12, 5.14.
When contact length decreases beyond the limit, current decreases as shown in figure 5.16. Contact lengths below 5μm are not suitable for this geometry. For this top contact geometry contact length must be equal to and greater than 10μm.

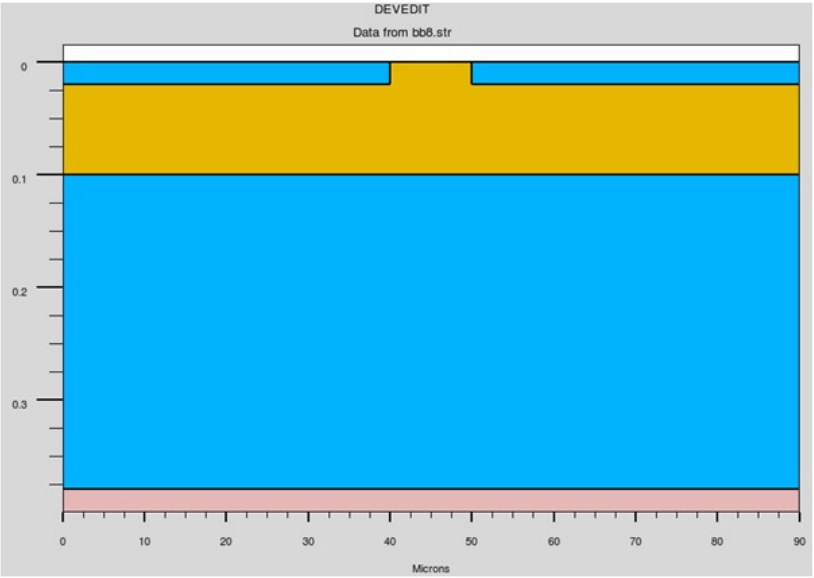

Figure 5.1: Source and drain length is 40 microns

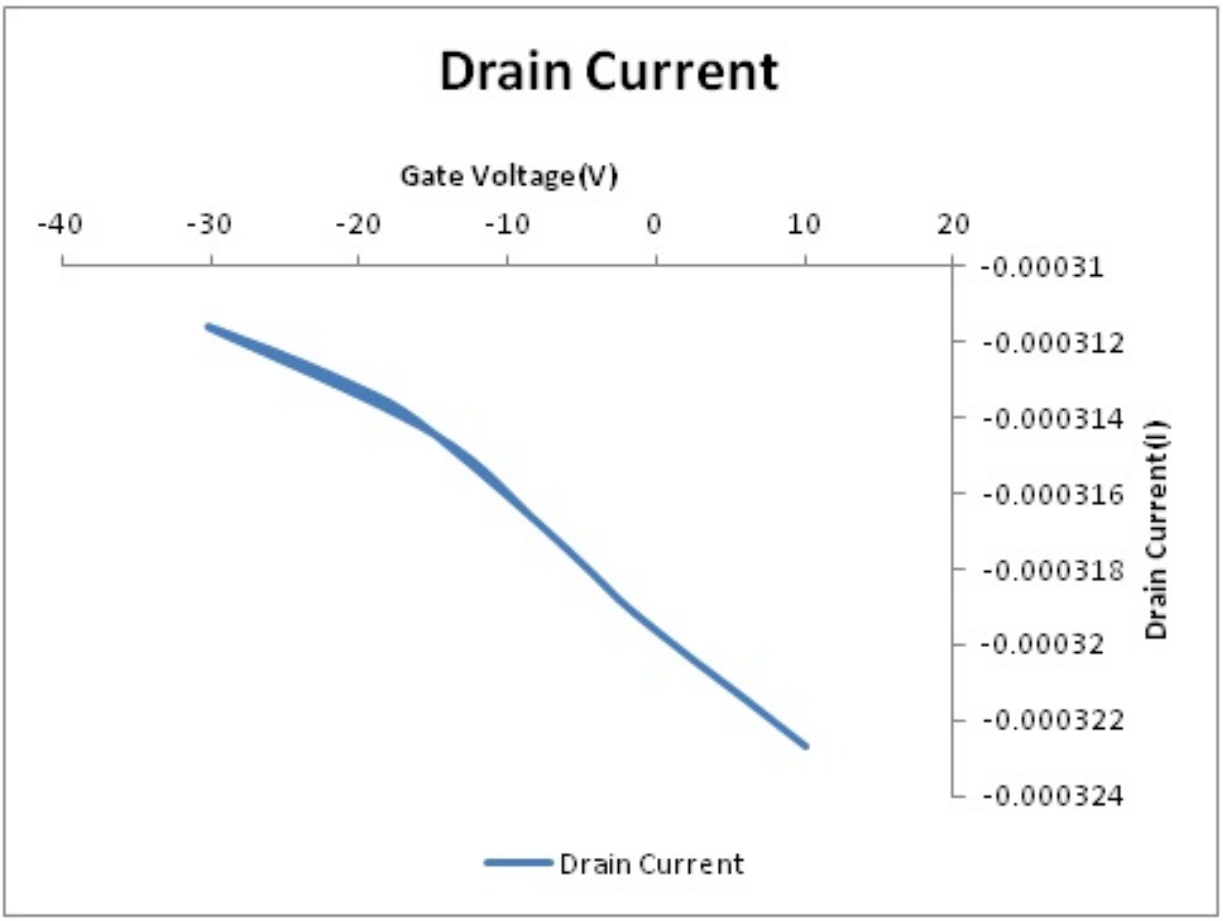

Figure 5.2: Drain Current and Gate Voltage graph for source and drain length is 40 microns

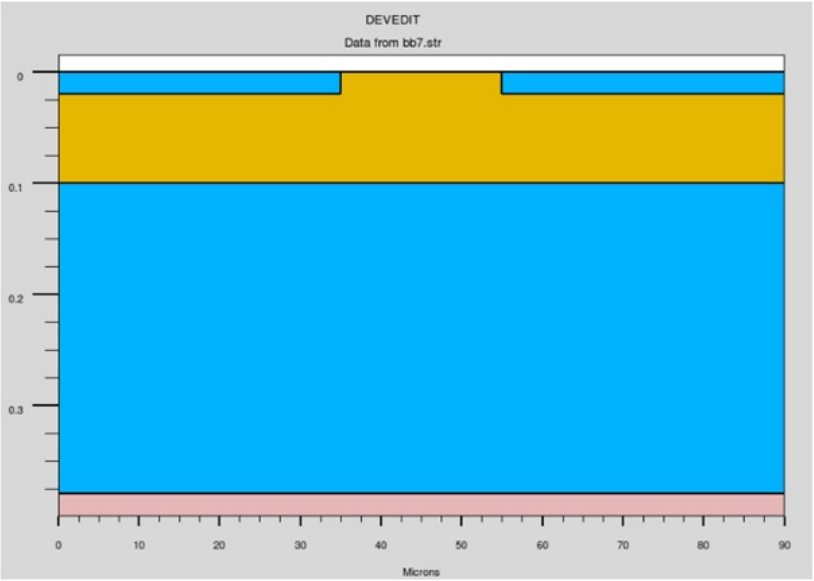

Figure 5.3: Source and drain length is 35 microns

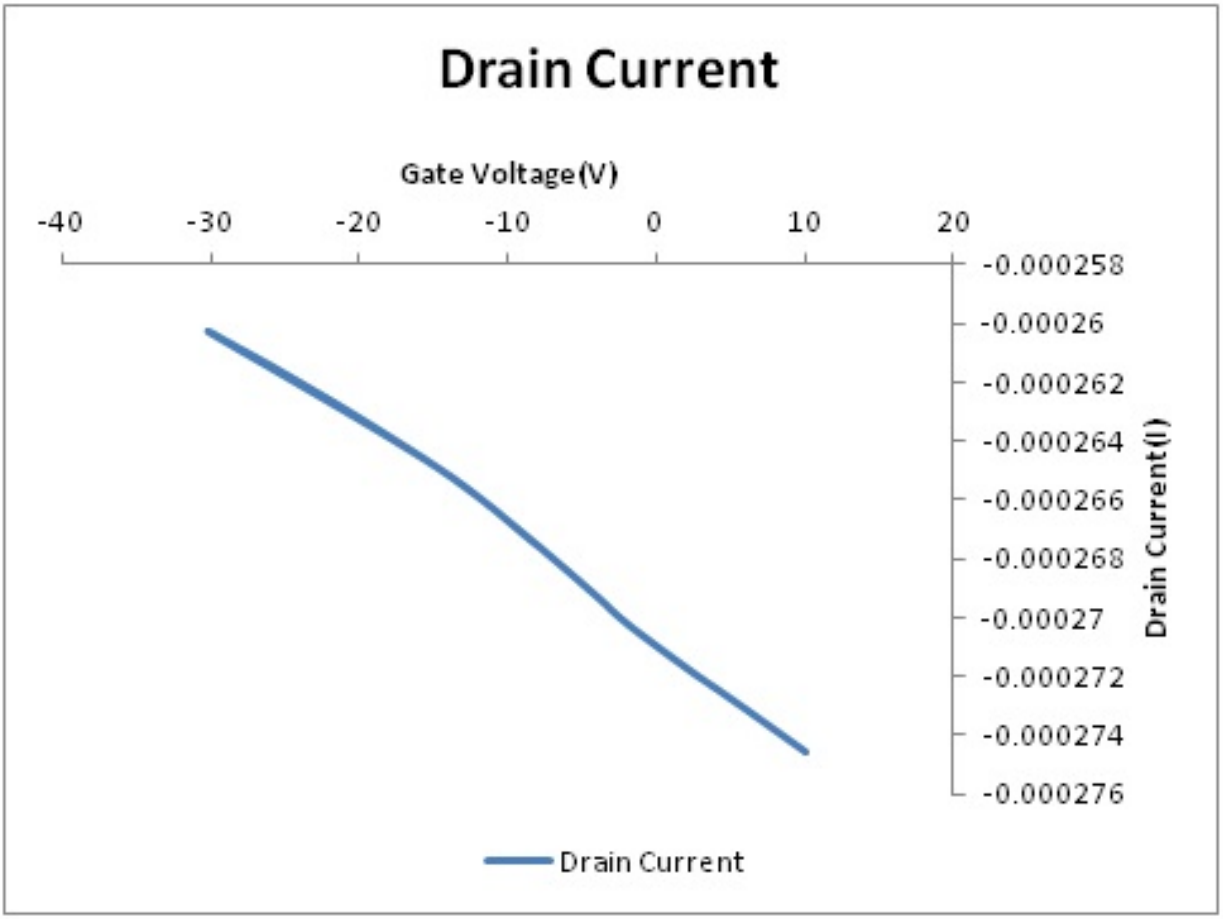

Figure 5.4: Drain Current and Gate Voltage graph for source and drain length is 35 microns

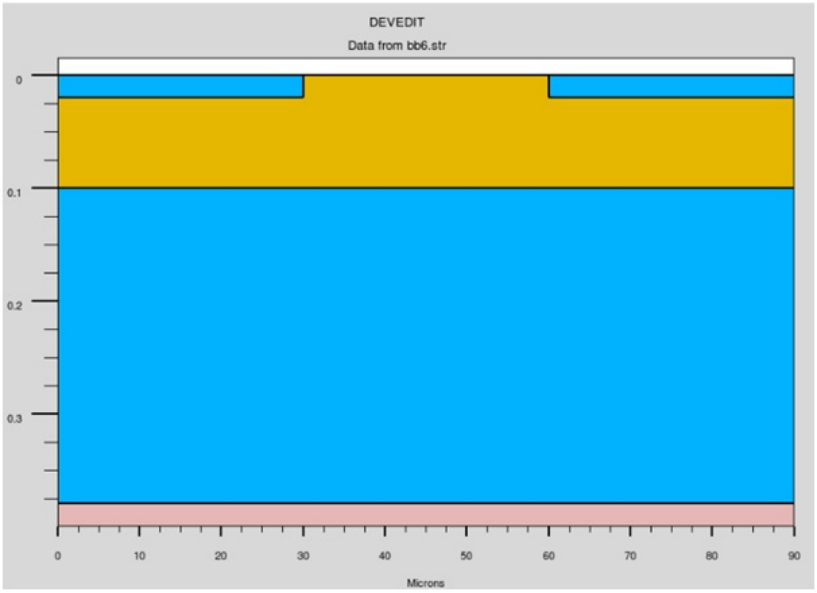

Figure 5.5: Source and drain length is 30 microns

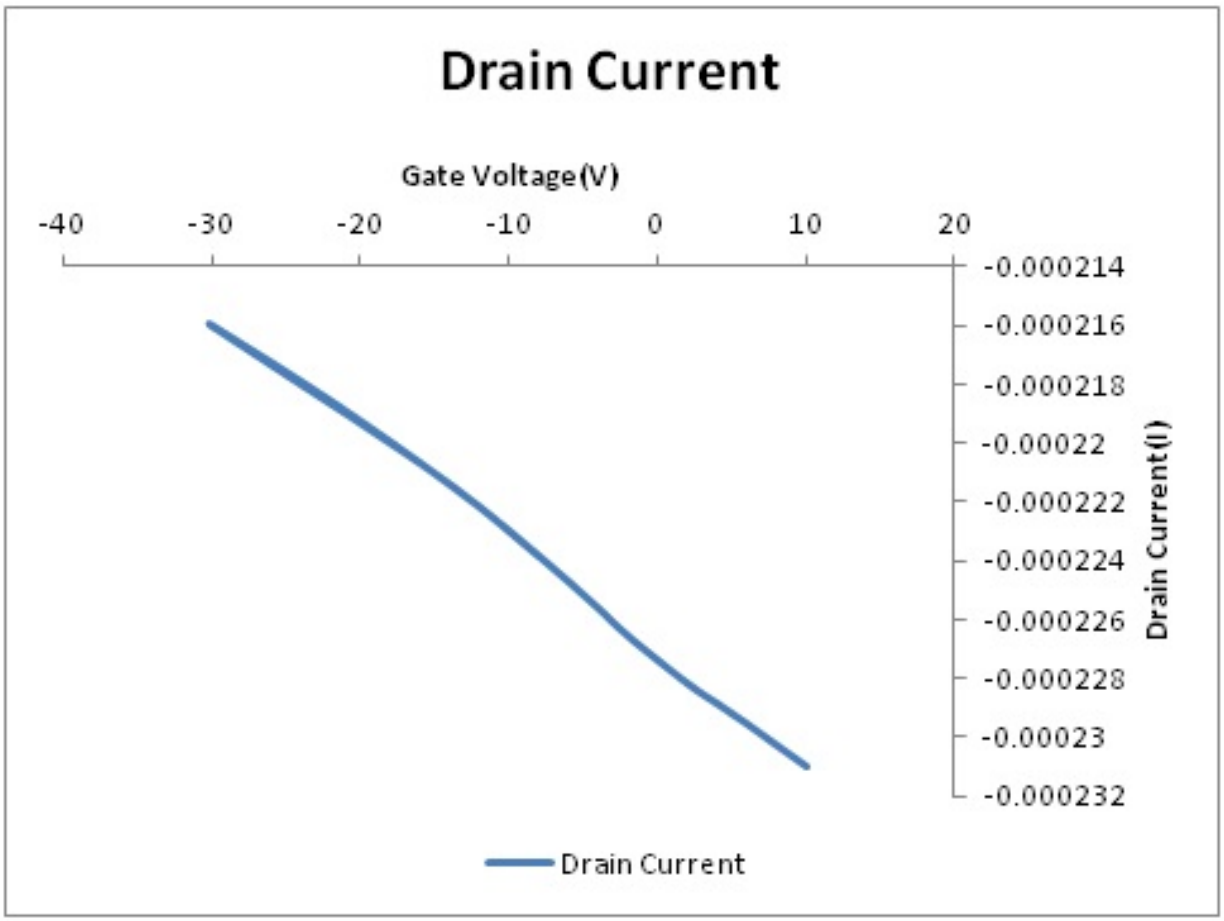

Figure 5.6: Drain Current and Gate Voltage graph for source and drain length is 30 microns

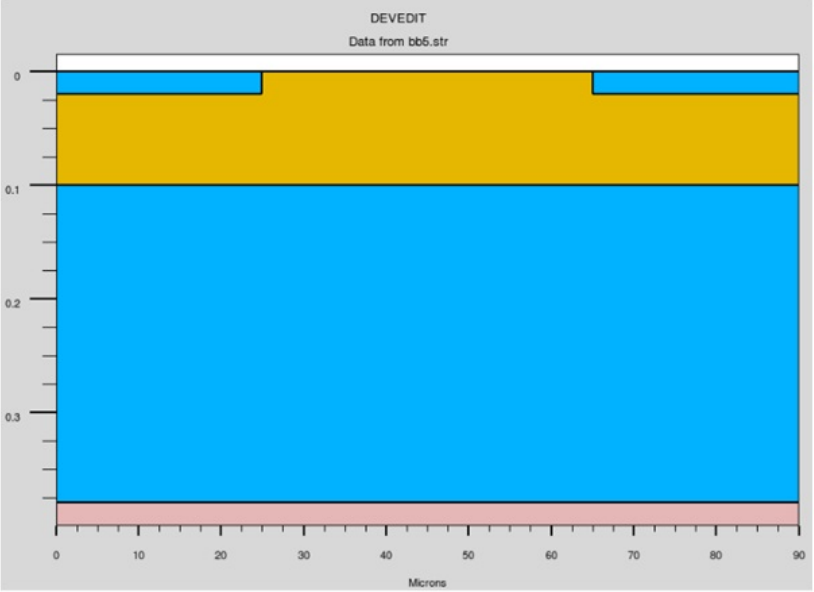

Figure 5.7: Source and drain length is 25 microns

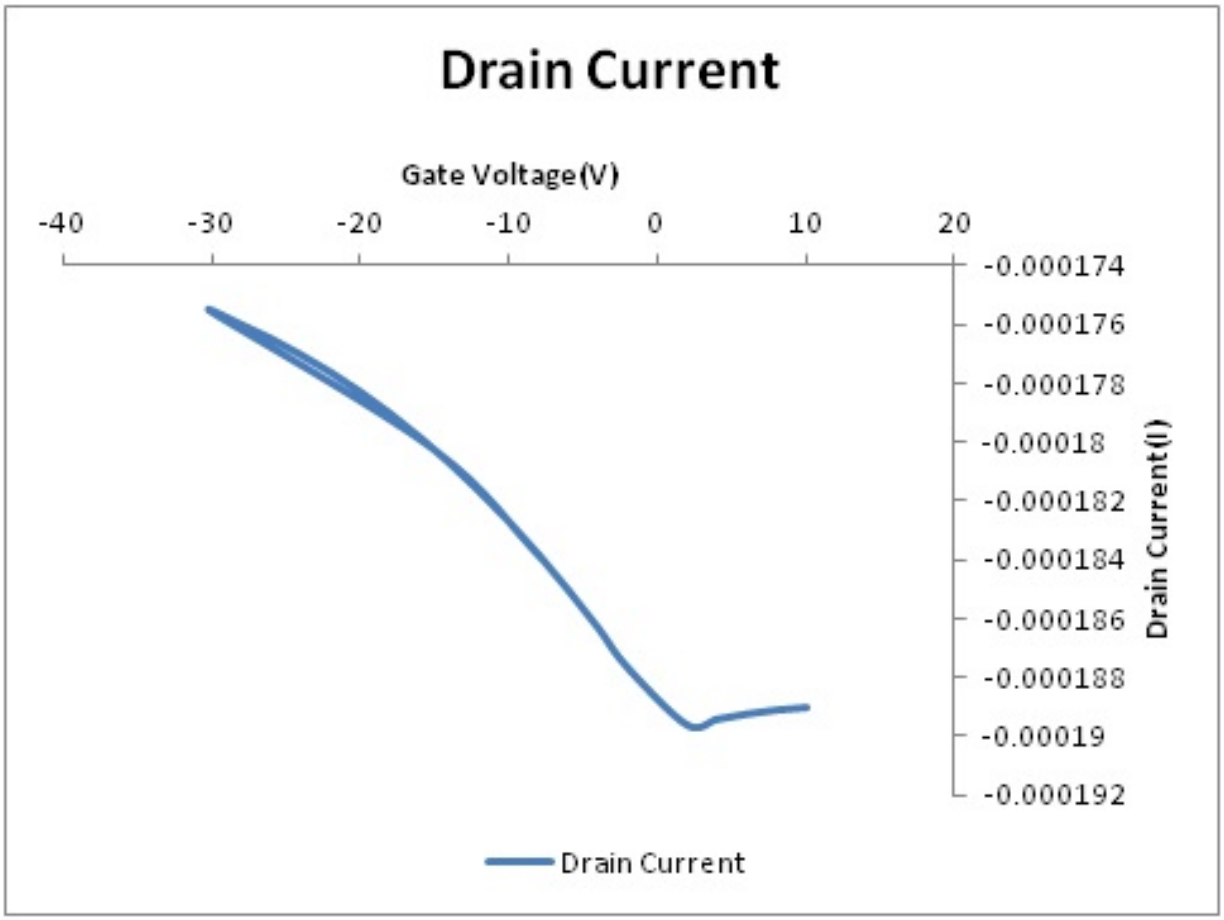

Figure 5.8: Drain Current and Gate Voltage graph for source and drain length is 25 microns

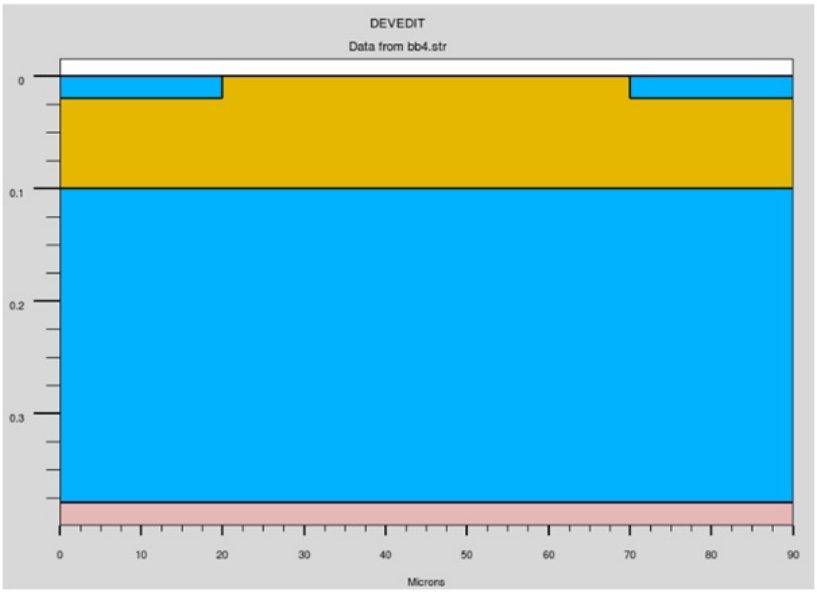

Figure 5.9: Source and drain length is 20 microns

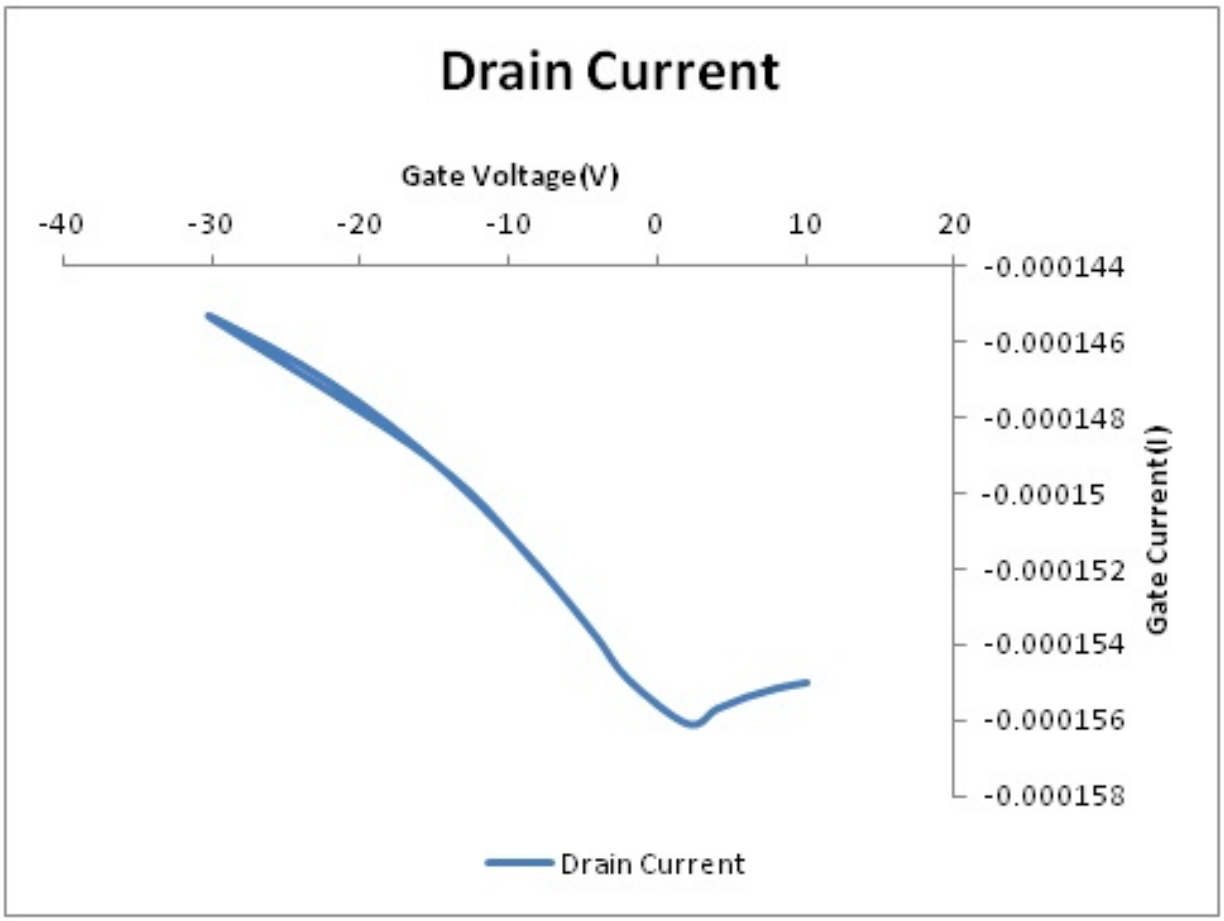

Figure 5.10: Drain Current and Gate Voltage graph for source and drain length is 20 microns

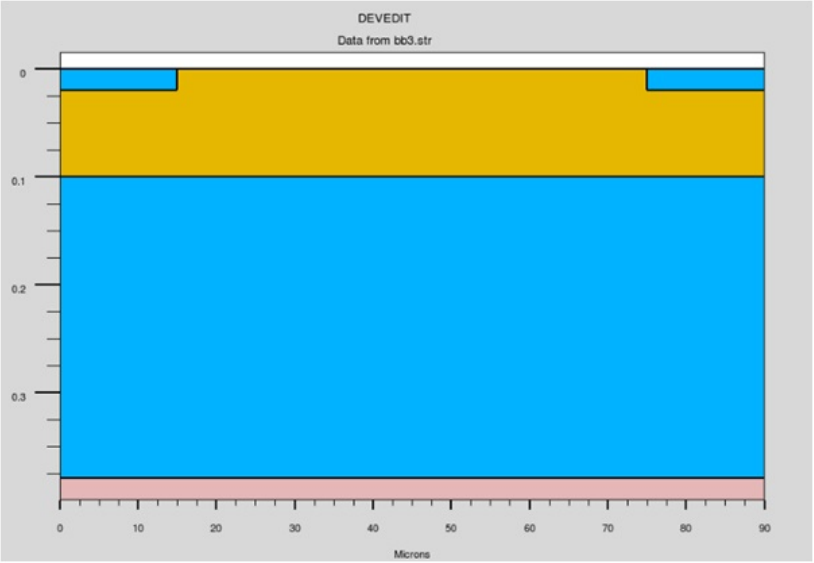

Figure 5.11: Source and drain length is 15 microns

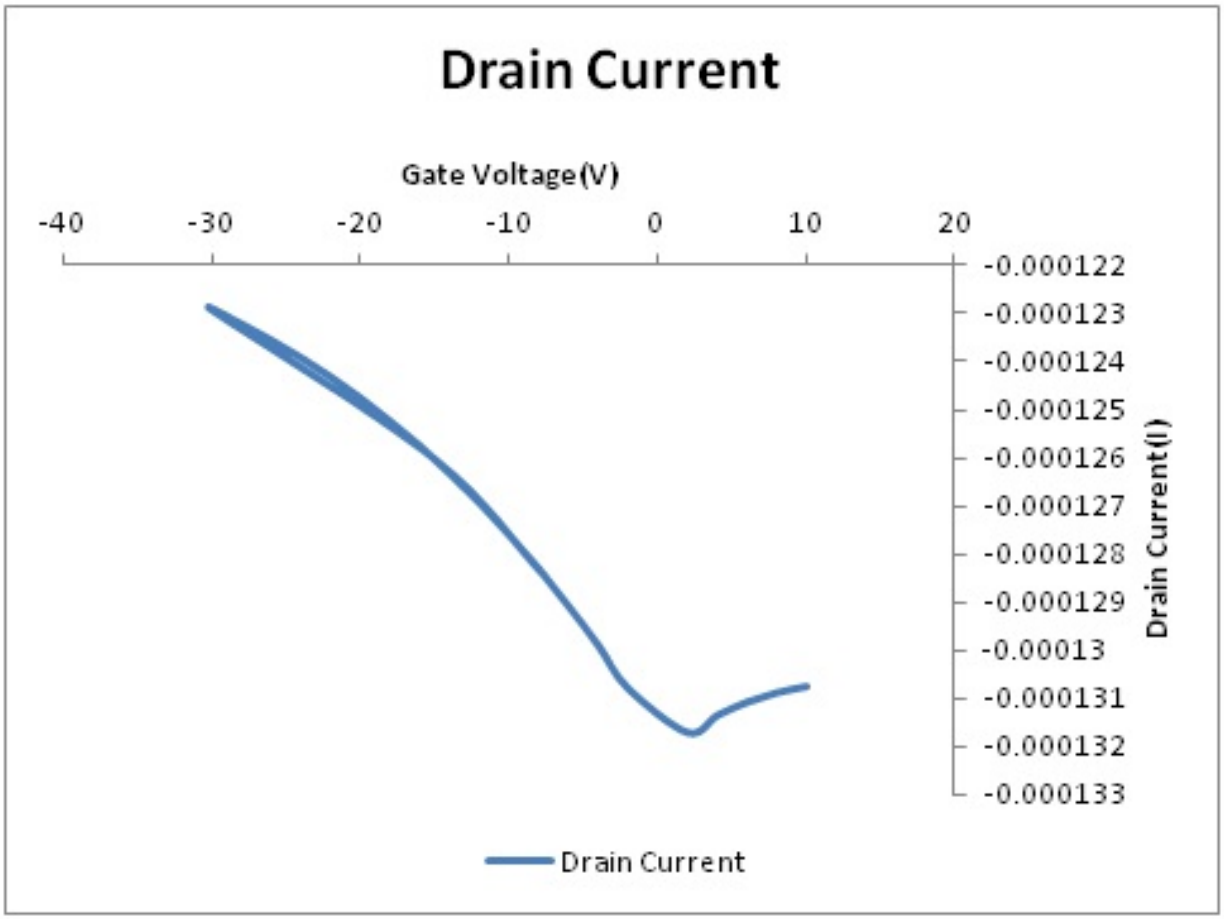

Figure 5.12: Drain Current and Gate Voltage graph for source and drain length is 15 microns

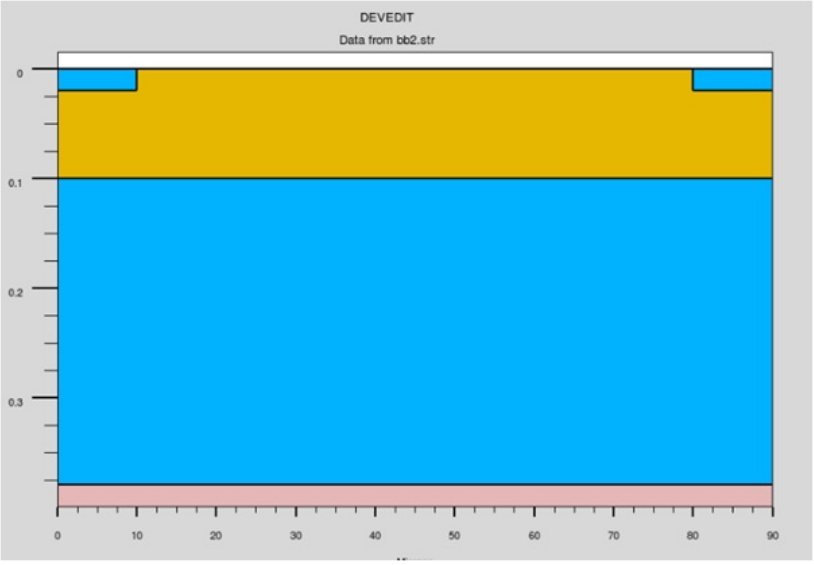

Figure 5.13: Source and drain length is 10 microns

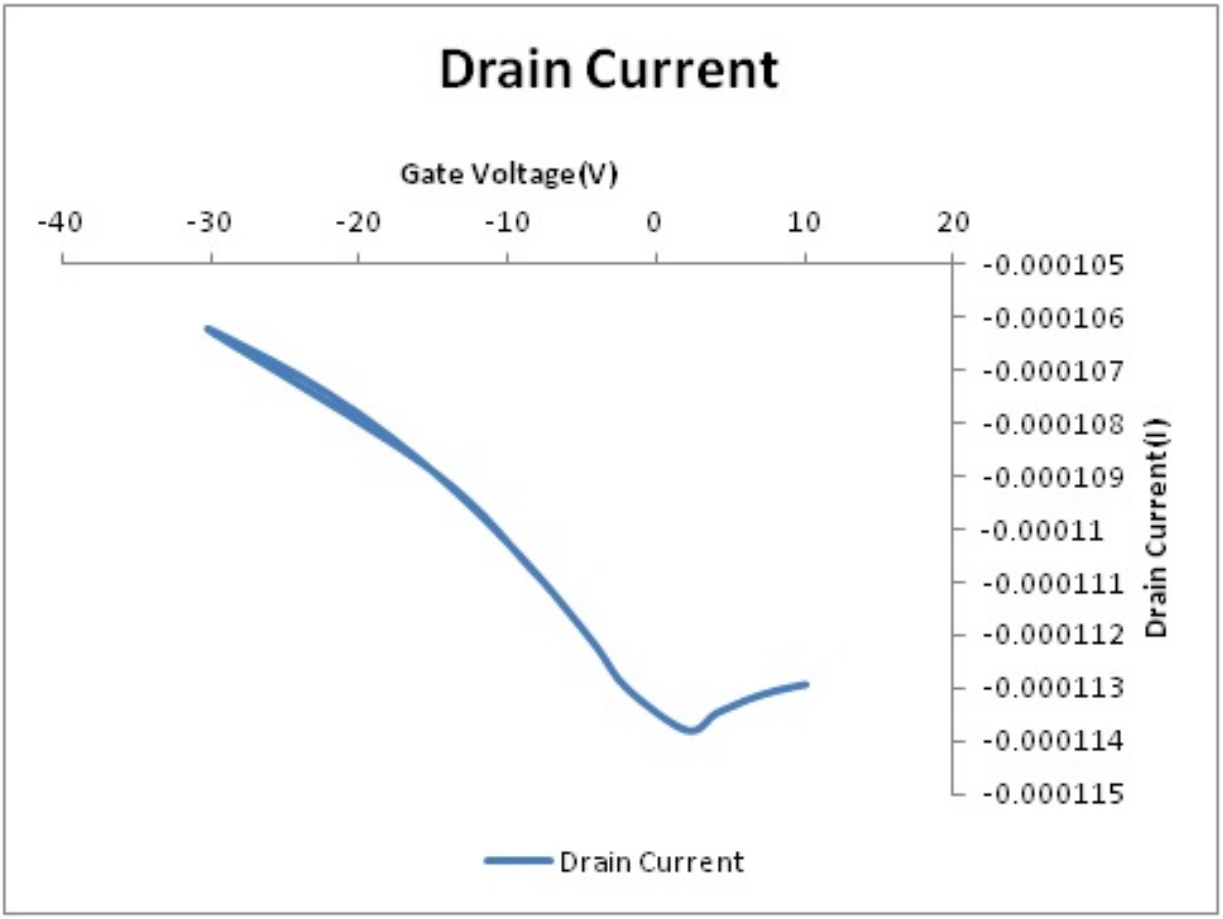

Figure 5.14: Drain Current and Gate Voltage graph for source and drain length is 10 microns

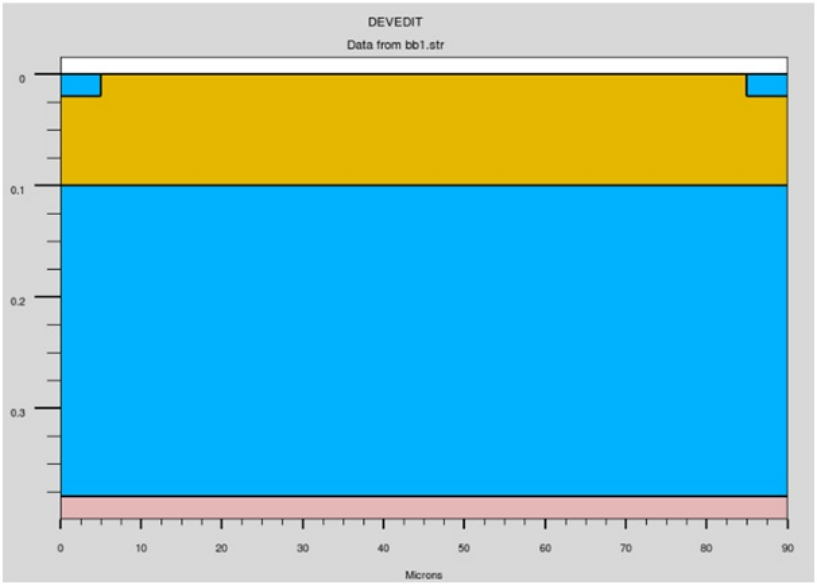

Figure 5.15: Source and drain length is 5 microns

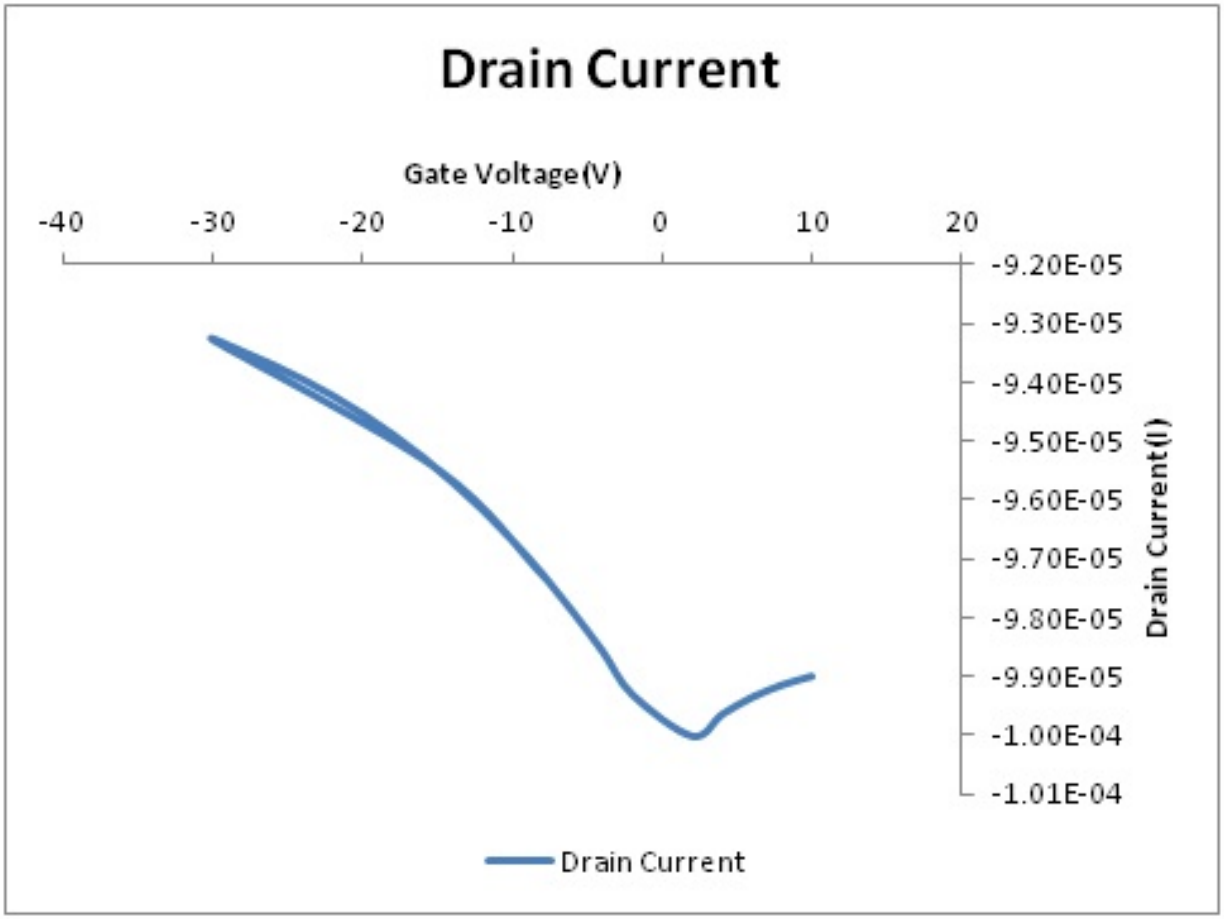

Figure 5.16: Drain Current and Gate Voltage graph for source and drain length is 5 microns

Chapter 6

RESULT AND DISCUSSION FOR BOTTOM CONTACT

6.1 Bottom contact OFET

In bottom contact OFET variation in contact length is also variation in channel length. Drain current increases due to decrease in length of conducting channel. The on/off current ratio is higher for short channel devices over long channel devices. As shown in figure 6.1 the channel length is 10μm, current is increases as negative gate bias is increased showed in figure 6.2 this is different characteristic observed from other channel length device.

Figure 6.3 the channel length is 20μm the characteristic is showed in figure 6.4 is in curve foam because the channel resistance is less than the source resistance. And the charge carrier is more in channel compare to near the source. Injection from two sides one is from the accumulation region and one is from the source length. For injection from source length charge carrier has to travel along the semiconducting layer. As the sweep of gate voltage is from -30V to 10 V the current start increasing due to the resistance in the source and the drain side is more than the channel. Injection of charge is less as compare to the above case.

As the gate voltage is increased, the mobility also increases and thus justies the hopping transport phenomenon in OFETs. The drain current reduces in low eld region, due to charge carriers being localized around the traps. Low field region is near the contacts in bottom contact configuration. Low mobility region creates an obstacle for current conduction in bottom contact conguration, whereas in top contact conguration charge injection/extraction is taking place from side/corner of the contacts and bypassing the low mobility region. Drain current Id is inversely proportionate to L. Mobility also decreases as channel length tends to increase in linear region and in saturation region mobility tends to increase.

In figure 6.6, 6.8, 6.10, 6.12, 6.14 I_d/V_g graph for channel length from 30μm to 70μm in these cases the channel length is increased and drain current is decreased. The contact resistance does not depend upon the channel length, while the channel resistance increases with increase in channel length. Contact resistance is higher in bottom contact devices due to poor morphology.

In figure 6.16 the channel length is 80μm this decide the limit of the contact length for this geom-

etry. The value of the drain current is very less. The value of the contact length for bottom contact geometry is equal to and greater than 10μm.

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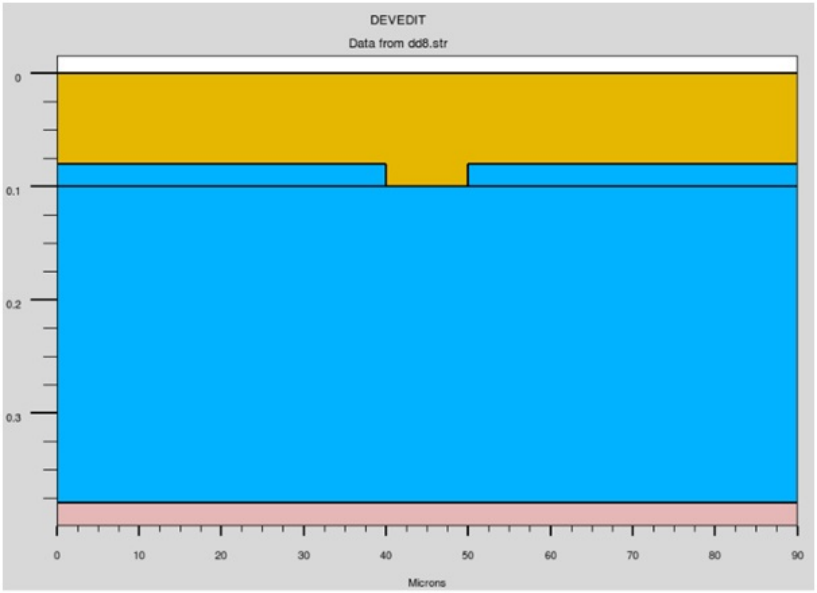

Figure 6.1: Channel length is 10 micron

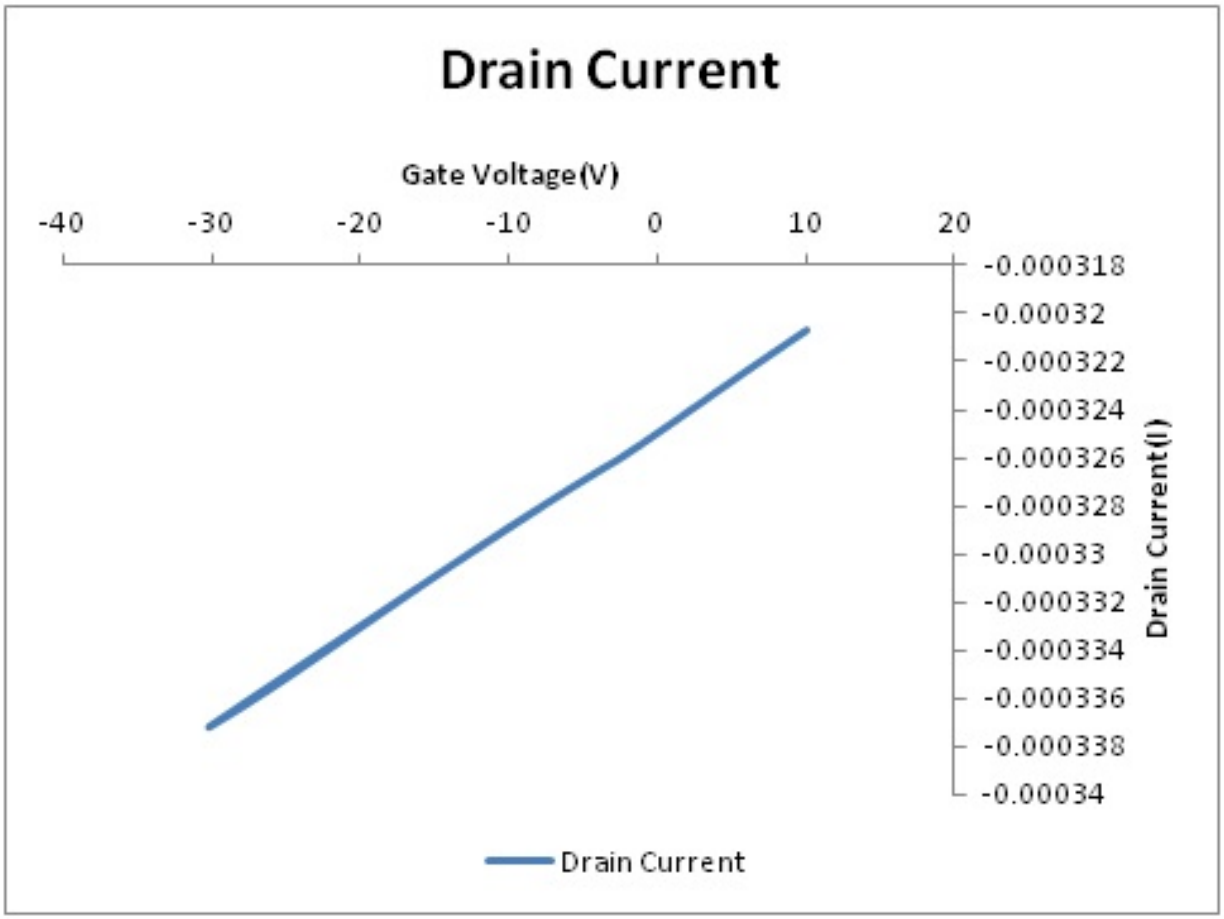

Figure 6.2: Drain Current and Gate Voltage graph characteristics channel length is 10 microns

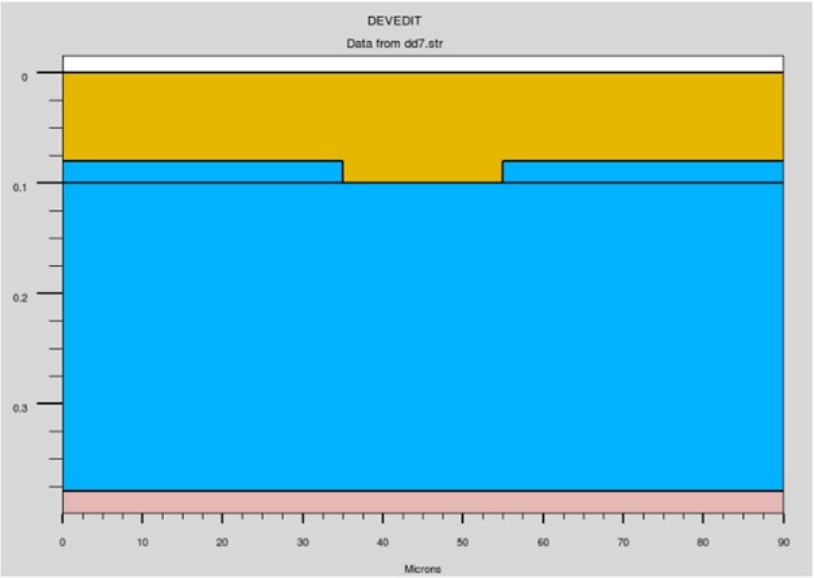

Figure 6.3: Channel length is 20 micron

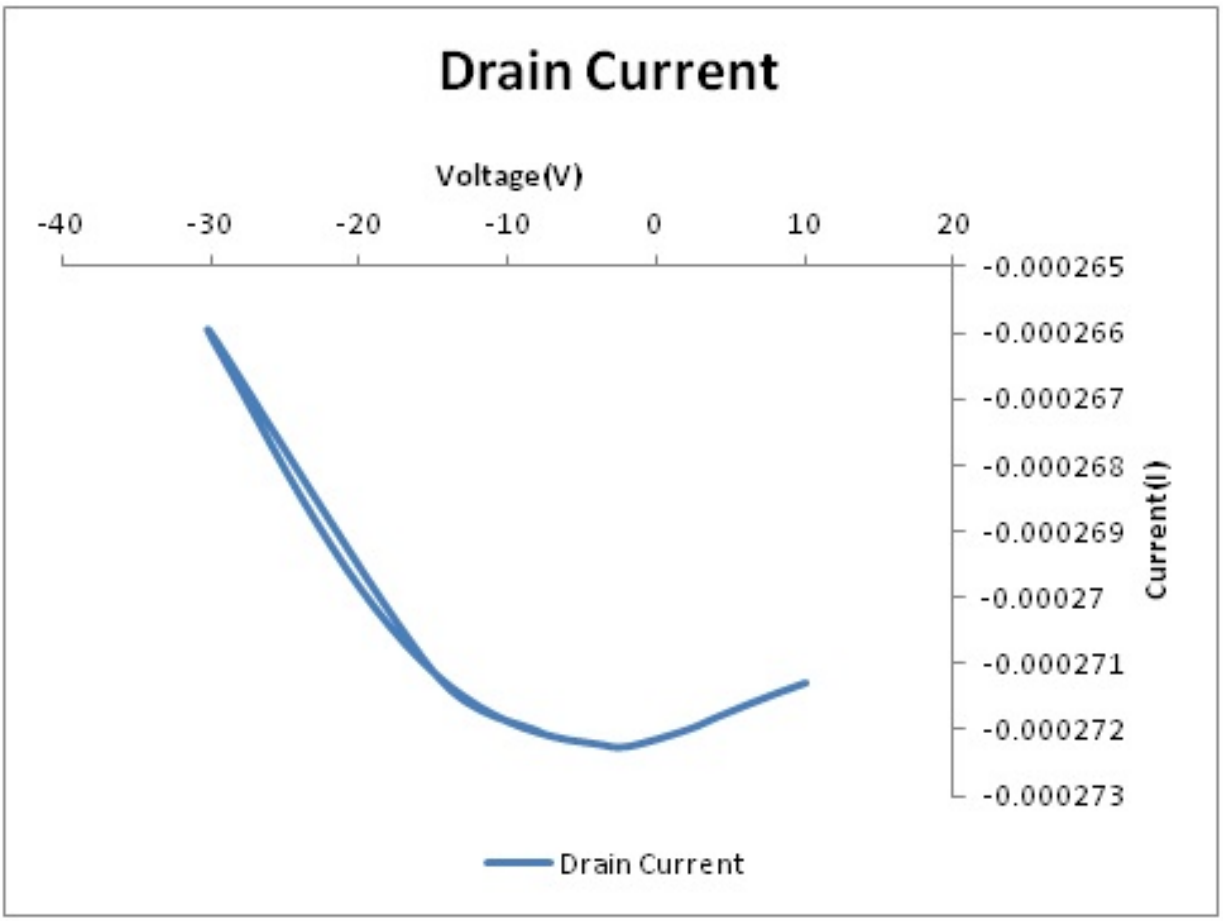

Figure 6.4: Drain Current and Gate Voltage graph characteristics channel length is 20 microns

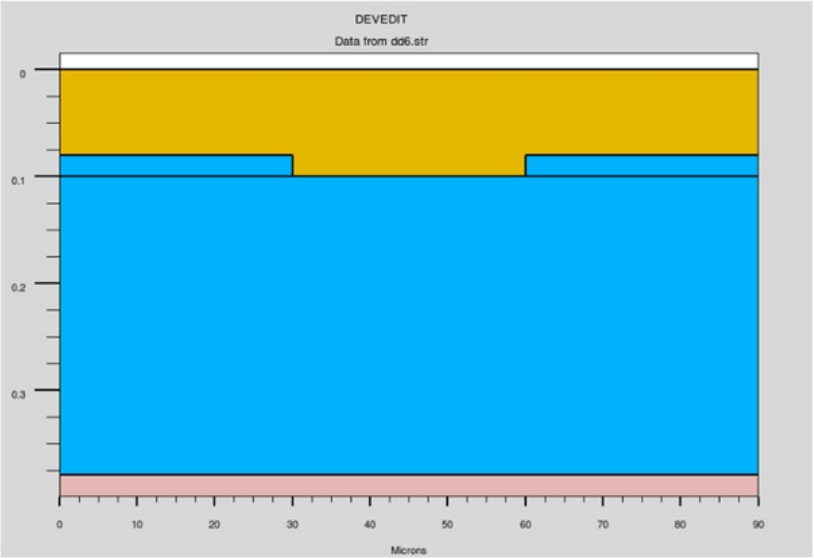

Figure 6.5: Channel length is 30 micron

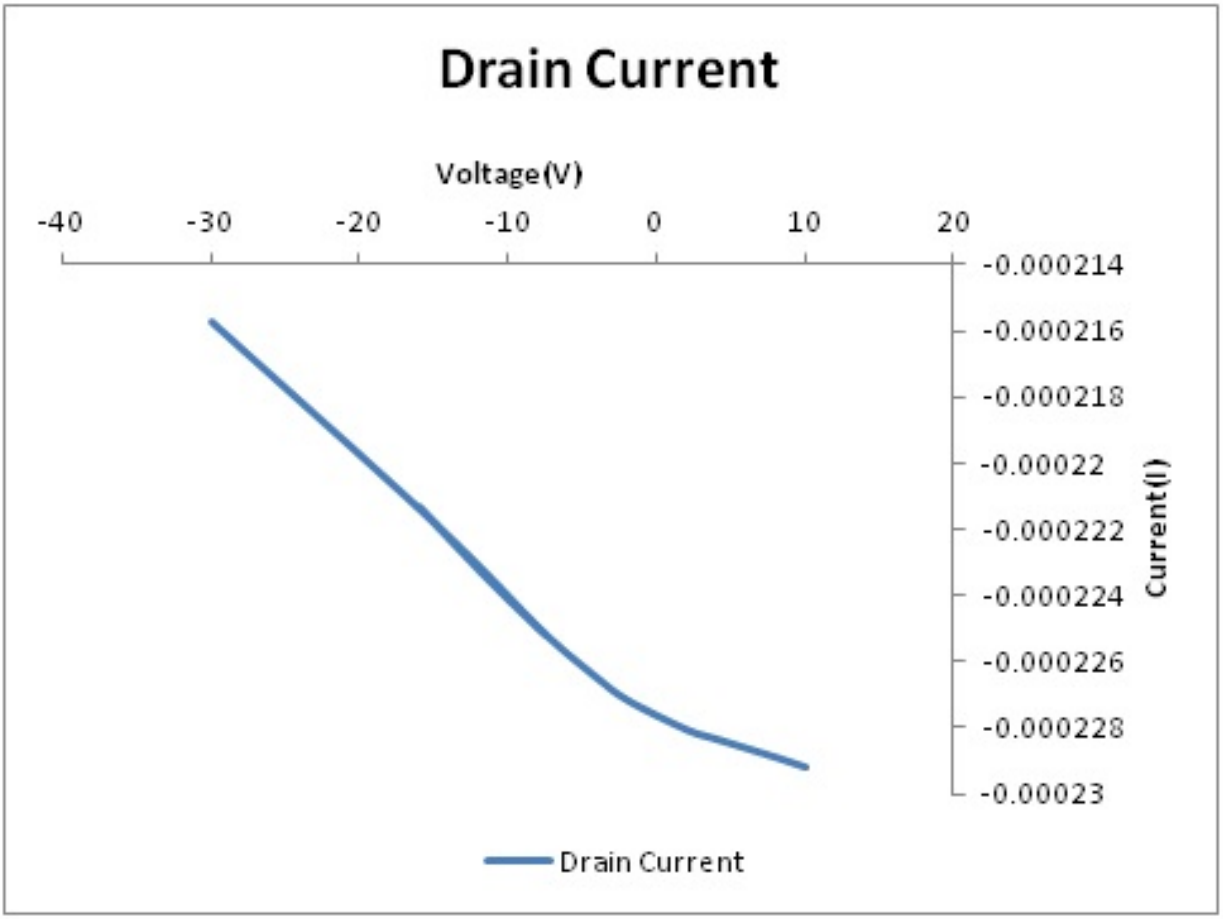

Figure 6.6: Drain Current and Gate Voltage graph characteristics channel length is 30 microns

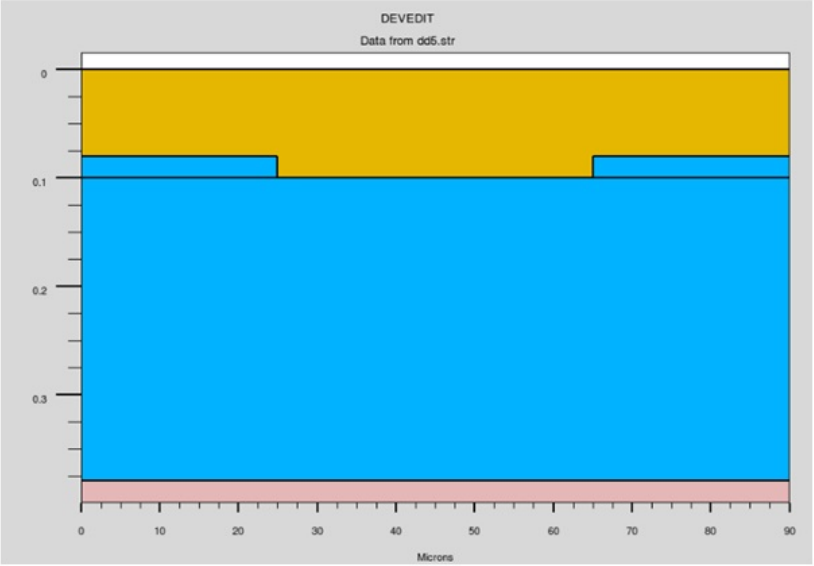

Figure 6.7: Channel length is 40 micron

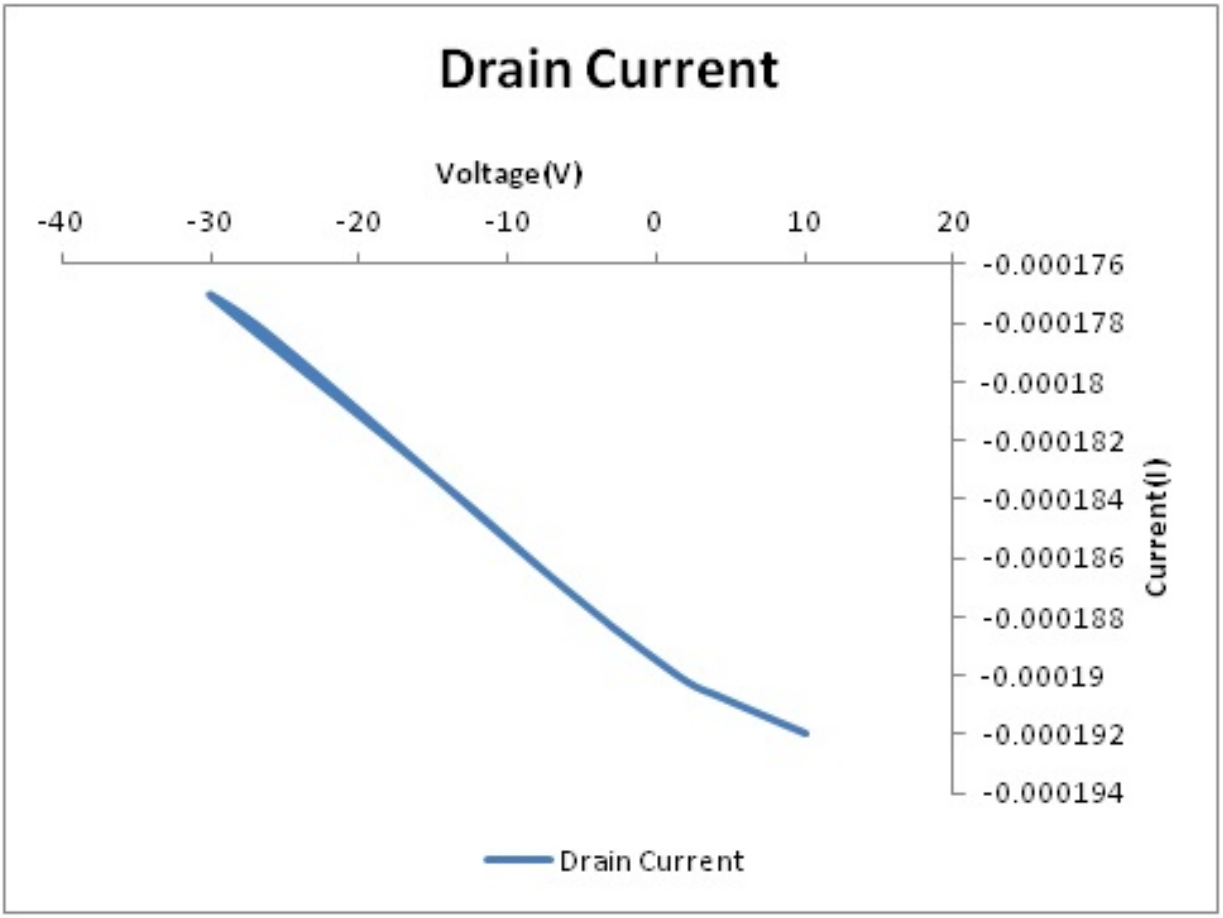

Figure 6.8: Drain Current and Gate Voltage graph characteristics channel length is 40 microns

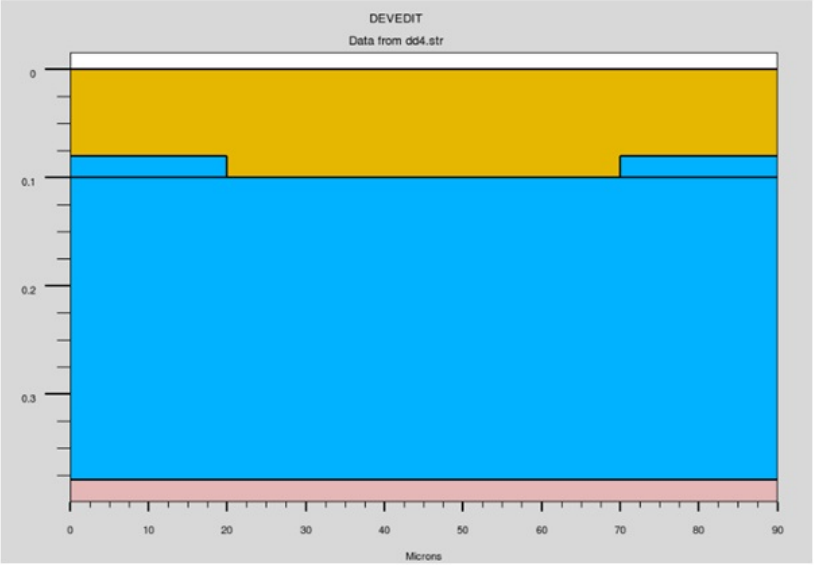

Figure 6.9: Channel length is 50 micron

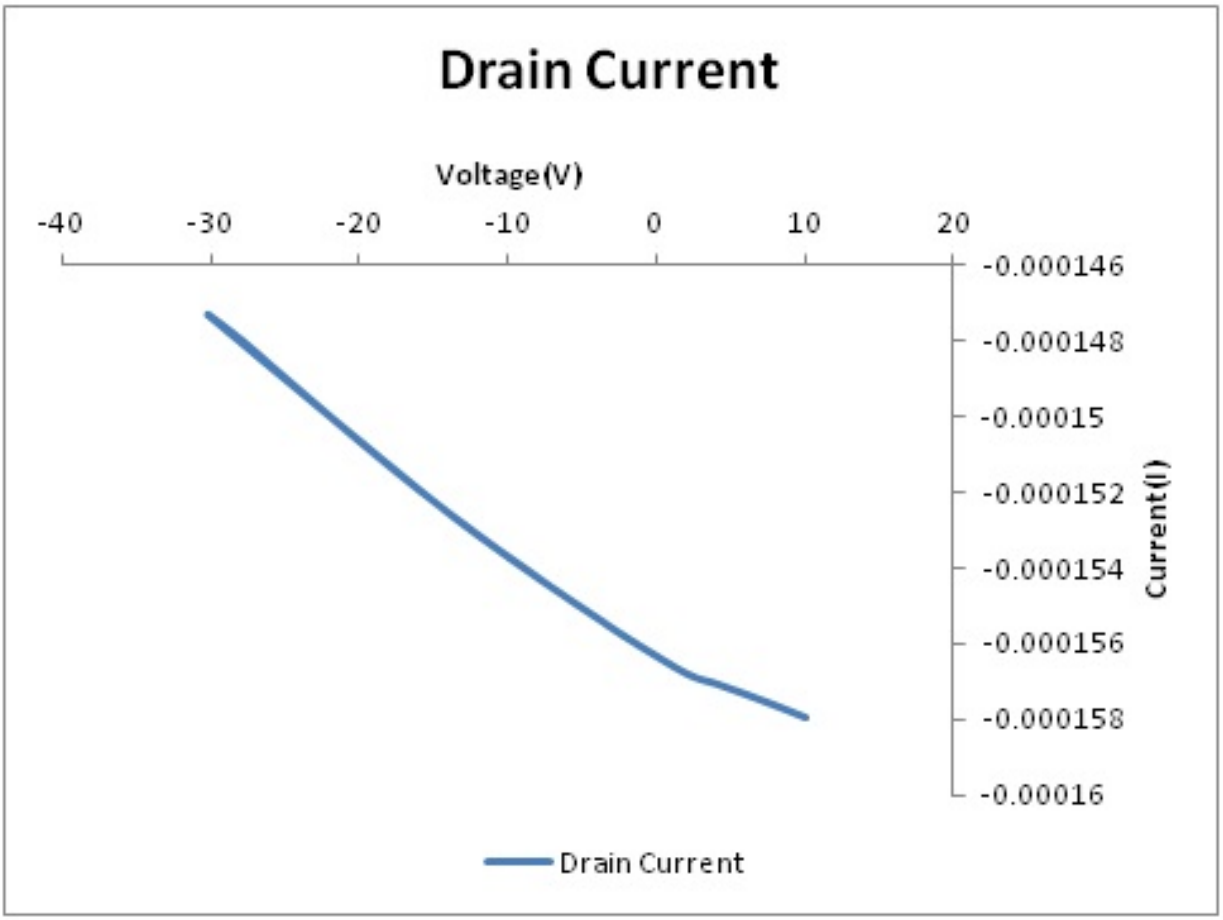

Figure 6.10: Drain Current and Gate Voltage graph characteristics channel length is 50 microns

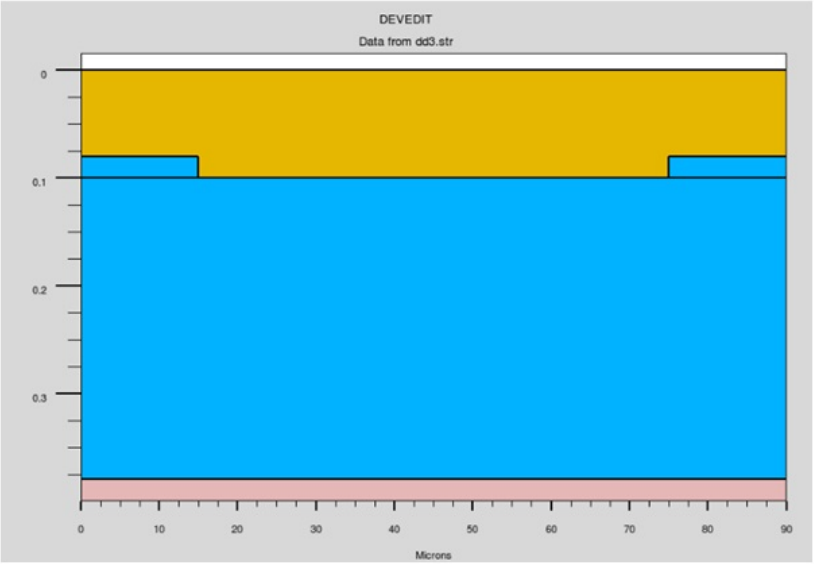

Figure 6.11: Channel length is 60 micron

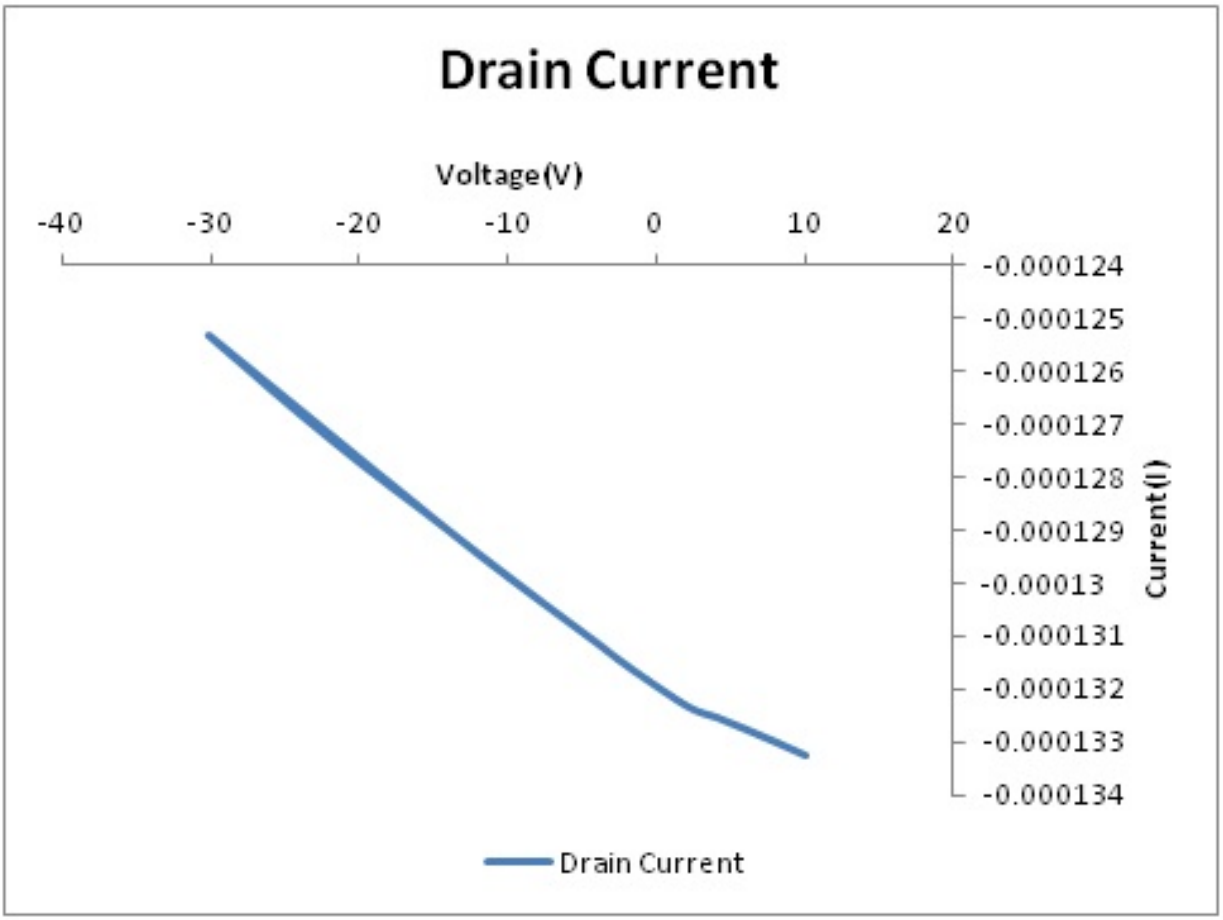

Figure 6.12: Drain Current and Gate Voltage graph characteristics channel length is 60 microns

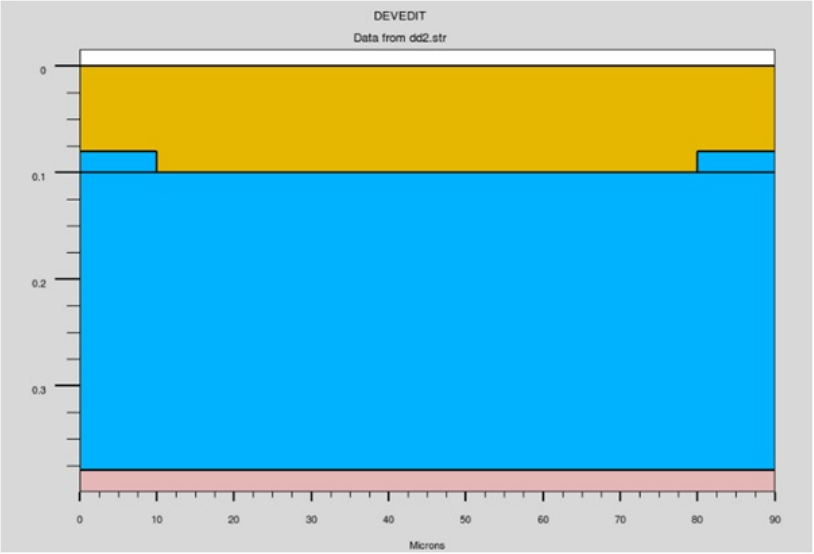

Figure 6.13: Channel length is 70 micron

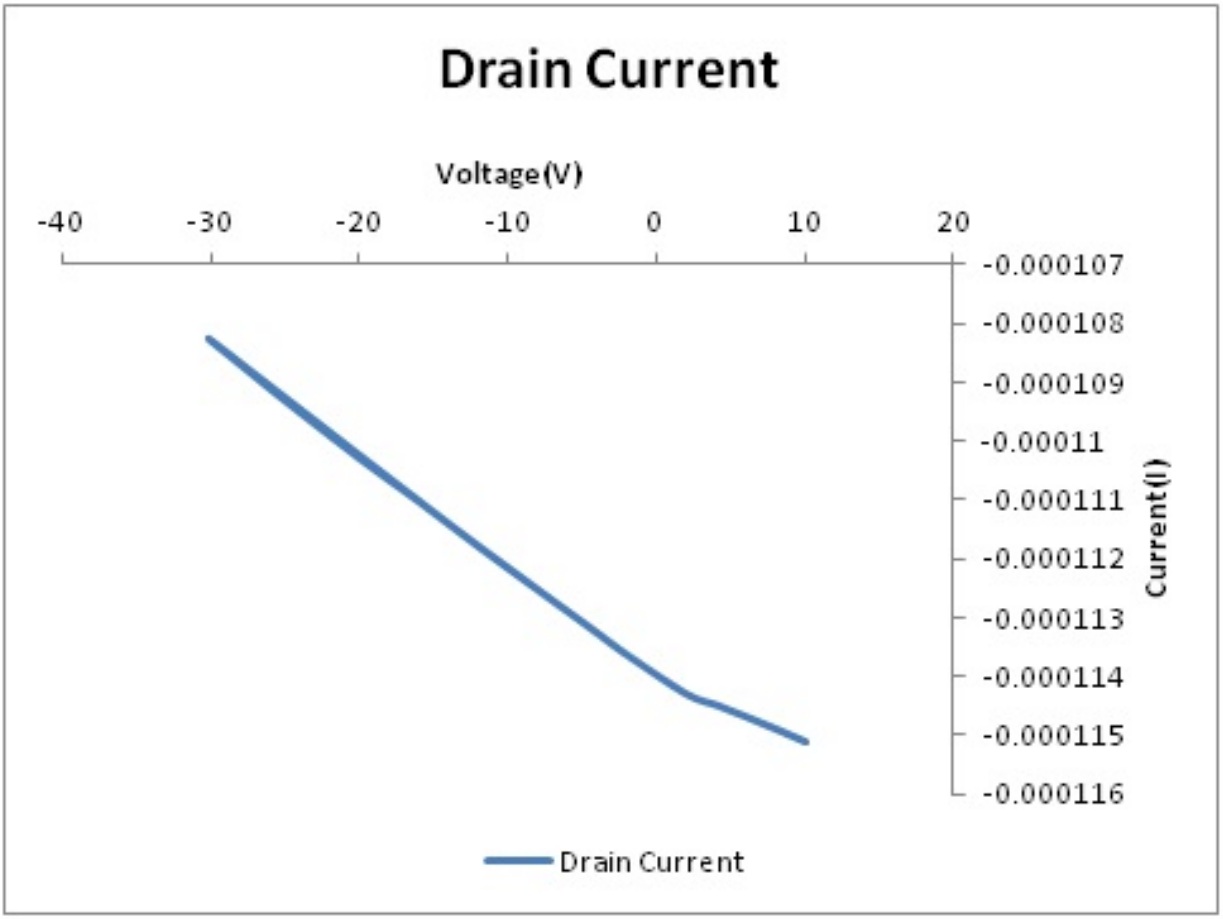

Figure 6.14: Drain Current and Gate Voltage graph characteristics channel length is 70 microns

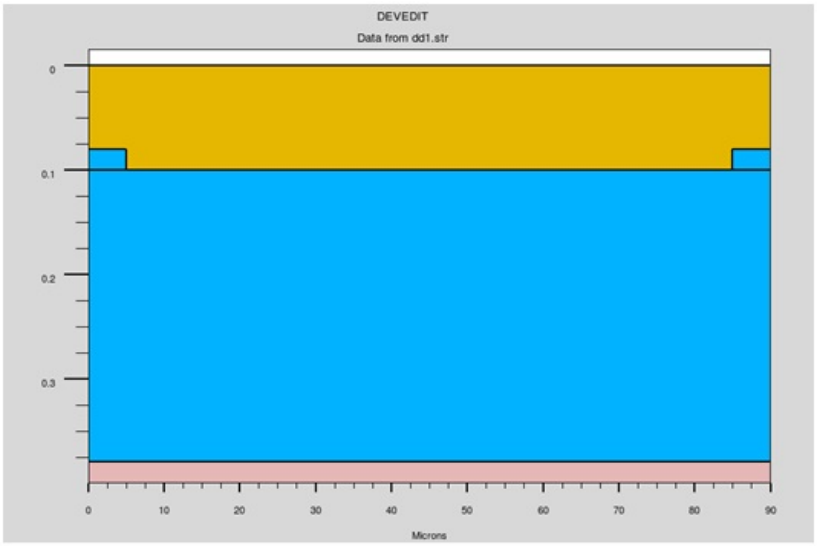

Figure 6.15: Channel length is 80 micron

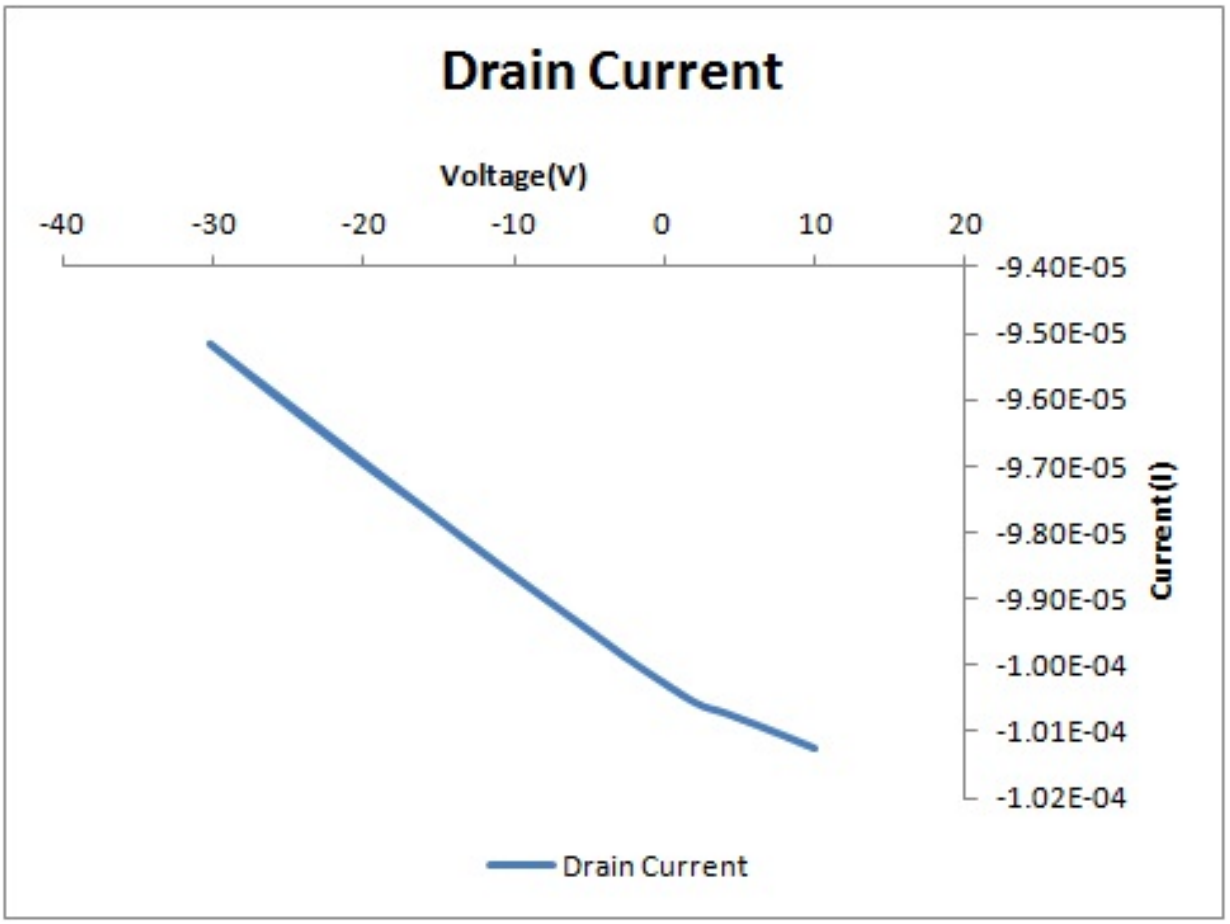

Figure 6.16: Drain Current and Gate Voltage graph characteristics channel length is 80 microns

Chapter 7

CONCLUSION AND FUTURE WORK

In summary this study represents the variation of contact length in top contact and bottom contact geometry. Increasing the contact length the value of drain current is increased in both the case. In top contact device contact resistance is proportional to the length of the contact. Therefore by increasing the contact length the contact resistance also increased that hinder the charge injection and the drain current start decreasing with contact length.

In bottom contact device the contact resistance does not depend upon the channel length, while the channel resistance increases with increase in channel length. Charge injection area from the contact is near the accumulation region or the channel length. There is low mobility region near this charge injection area causes obstacle in the charge injection. This obstacle increases as the channel length increases.

The limitation for the contact length for both the devices is 5μm drain current is very less in this case. Therefore the length for these geometry is 10μm and greater than this.

Future work is to make pentacene as n-type by adding gate insulator polyvinyl alcohol (PVA). It give electron to the accumulation layer. Thus pentacene behave as n-type also. With this n-type and p-type from same material it is easy for complementary structures fabrication. Logic gates can be designed with this.

Chapter 8

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