# CHAPTER-1

# INTRODUCTION

Clock and data recovery (CDR) circuits are used extensively in high-speed transceivers [1]. Such transceivers serve in many applications including digital systems, optical communication, broadband communication, backplane routing and chip-to-chip interconnects. CDR circuits are used primarily in such applications to extract timing information from data, to reduce clock jitter, and to suppress its skew. A vital building block of CDR circuits is the phase detector (PD). The main function of PD is to detect and amplify the phase/frequency difference between the input signal and the output of the local oscillator (LO) employed in the CDR circuit to recover clock and data. The performance of CDR circuits critically depends on the characteristics of the phase detector (PD).

The phase detector is a 3-port configuration. A sinusoidal signal $V_c$ = cosωt is applied as a reference signal to input port 1 of the phase detector. When a phase coherent signal Vs = Cos(ωt- Φ) with a carrier frequency of ω and an instantaneous phase deviation (Φ) is applied to input port 2 of the network, a response signal V(Φ), proportional to the phase deviation (Φ) would be obtained from the output Port 3 [2].

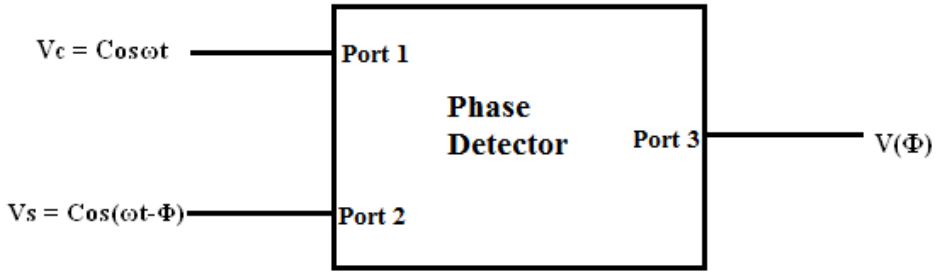


Fig.1. Block diagram of a PD

Phase detectors can be generally categorized into two categories [3] :

1. Linear PD
2. Nonlinear PD.

A linear PD [4] compares the input signal with a reference signal. It detects and amplifies their phase difference. In the lock condition, the phase error of the input ideally drops to zero. So, a linear phase detector does not generate any significant activity on the VCO control line and hence it produces smaller output jitter.

A nonlinear phase detector [5] uses the VCO output to sample the input signal. In this case, in the lock condition, the output of the PD does not drop to zero. So, significant activity is generated on the VCO control line and hence large output jitter is produced.

Recently a significant effort has been made on designing high-speed low-power CMOS PD for telecommunications and digital systems. Many novel configurations and design techniques have emerged. Each of these PD's has it's own advantages and limitations. To the best of the author's knowledge, no PD circuit design based on analog building blocks (ABB) is available in literature. Therefore, an OTRA (a current mode ABB) based phase detector circuit using a simple scheme has been introduced in this thesis work.

An OTRA is a high gain current input voltage output device. The OTRA is not slew limited in the same fashion as voltage op amps [6]. It can provide a high bandwidth independent of the gain. Hence, it does not suffer from constant gain bandwidth product like voltage op amps circuits [5]. It is a three terminal analog building block shown in Figure 2.

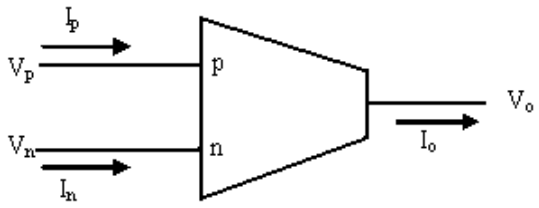


Figure 2. The OTRA circuit symbol.

It is defined by the following matrix equation:

$$\begin{bmatrix} V_p \\ V_n \\ V_O \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ I_O \end{bmatrix} \quad (1)$$

Where Rm is the transresistance gain.

Both the input and output terminals are characterized by low impedance. The input terminals are virtually grounded leading to circuits that are insensitive to stray capacitances [6-9]. Ideally the transresistance gain, Rm, approaches infinity, and applying external negative feedback will force the two input currents, I+ and I– , to be equal.

## REFERENCES


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4) A C. Hogge, “A self correcting clock recovery circuit,” J. Lightwave Tech., vol. LT-3, pp. 1312-1314, Dec. 1985.
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# CHAPTER-2

# LITERATURE REVIEW

Extensive literature review suggests that a few number of phase detector circuit design approaches exists [1-4]. Among the existing phase detector circuits, the Gilbert Cell PD seems to be the earliest and the simplest architecture. Each of these phase detector's has some advantages and limitations. In this chapter, an attempt has been done to introduce those phase detector circuits along with their advantages and limitations.

## 2.1 Gilbert Cell PD

A typical implementation of a Gilbert Cell PD is shown in Figure. 2.1.

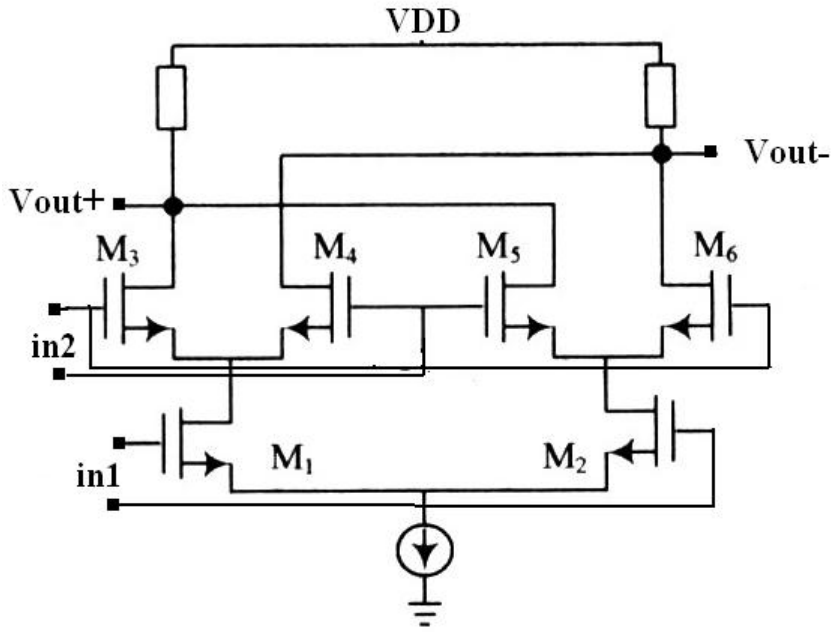


Figure. 2.1. The Gilbert cell PD.

When signals of small amplitude are applied to the input ports of the cell, it behaves as an analog multiplier [5]. If the phase error of the inputs is in the vicinity of go, the average value of the output is linearly proportional to the phase error. An advantage of Gilbert Cell PD is its high operation speed as compared with other implementations. However, it suffers from high static power consumption. Also, the gain of the cell depends on the amplitude of the inputs. Moreover, it cannot detect the frequency error of the inputs.

## 2.2 XOR PD

If the amplitude of the inputs to the Gilbert cell is large, the cell behaves as a XOR gate [5]. As the phase error of the inputs deviates from 90°, the output duty cycle departs from 50%, resulting in a dc output that is proportional to the phase error. The advantage of XOR PD's is the improved acquisition range 0°~ 180°, as shown in Figure.2.2. Its drawback is the dependency of the cell dc output on the duty cycle of the inputs.

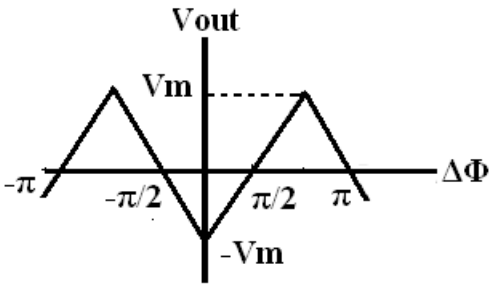


Figure. 2.2. $V_{out}$ ~ phase plot

## 2.3 R-S Latch PD

An edge-triggered PD can be implemented using an R-S latch as shown in Figure. 2.3 [5]. Its differential output changes sign every time a rising edge at one input is followed by a rising edge at the other. The advantages of the R-S latch PD are the independence of the average value of its output on the duty cycle of the inputs and the improved acquisition range ( 0° - 360°), as shown in Figure. 2.3.

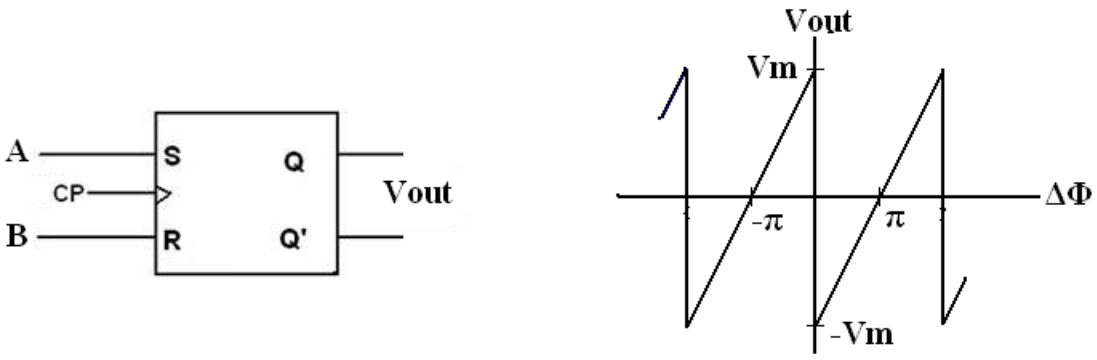


Figure. 2.3. R-S latch PD.

The drawbacks of R-S latch PD include:

(1) CDR circuits employing a R-S latch PD can not perform frequency synthesis because the frequency of its output is the same as that of the inputs.
(2) CDR circuits may lock to a higher harmonic of the input as it generates a nonzero dc output if the frequency of one of its inputs is an integer multiple of that of the other.
(3) Output jitter exists due to the metastability that occurs in the lock condition.

## 2.4 D-Flip flop PD

To detect both the phase and frequency differences of incoming signals, phase-frequency detectors (PFD) are needed. The block diagram of a D-flip flop PFD is shown in Figure. 2.4 [5].

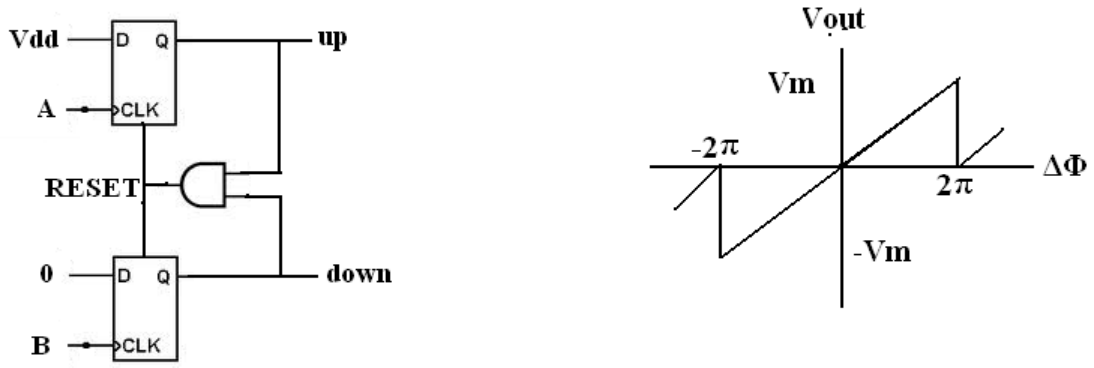


Figure. 2.4 D-flip flop PFD

It employs two edge-triggered, resettable D flip-flops with their *D* inputs connected to logic HIGH. Signals *A* and *B* act as the clock input of the two flip-flops. If $Q_A = Q_B = 0$, a LOW-to-HIGH transition on *A* causes $Q_A$ to go HIGH. Subsequent transitions on *A* will have no effect on $Q_A$. When *B* goes from LOW to HIGH, the AND gate activates the RESET of both flip-flops, resetting both $Q_A$ and QB. The outputs $Q_A$ and QB are called UP and DOWN signals. The advantages of this PFD are the improved acquisition range and lock speed as it detects both the frequency and phase errors of the inputs. As shown in Figure. 2.4, the PFD has a constant gain over the phase error range $\mp 2\pi$ . The D-Flip flop PDF suffers from a number of drawbacks, namely:

(1) When the delay between UP and DOWN signals becomes comparable to their switching delay in the vicinity of the lock condition, a dead zone is generated, causing the output to jitter.

(2) Output jitter exists due to the metastability that occurs in the lock condition.
(3) Sensitive to input data patterns.

## 2.5 Two-XOR PD

The block diagram of the CDR circuit employing a two-XOR PD is shown in Figure.2.5 [6]. The VCO generates eight differential clock signals *CLK$_1$* through *CLK4* each spaced by 45°.

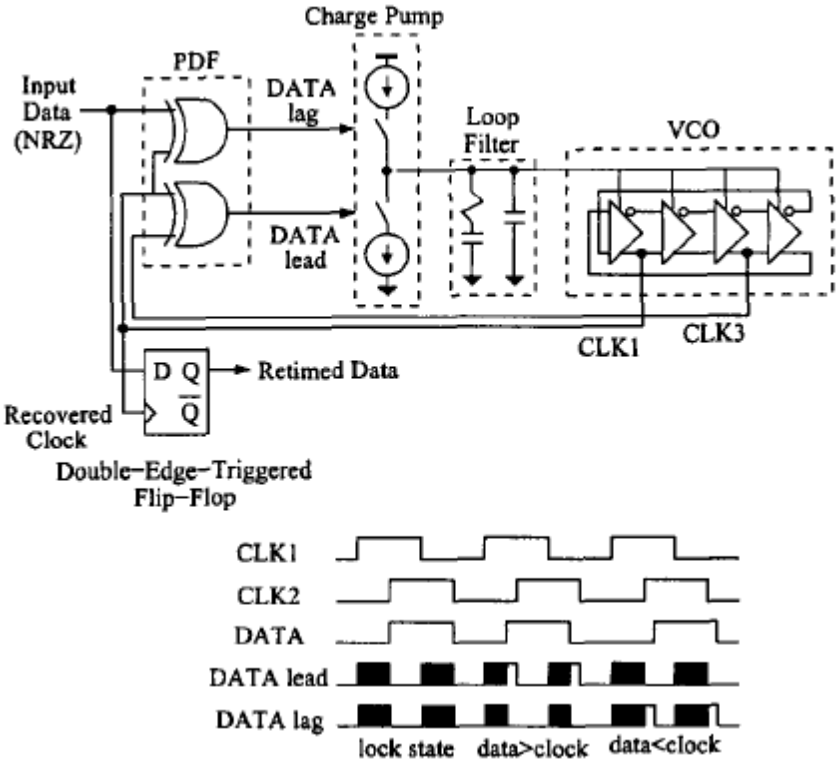


Figure.2.5 Two- XOR PD

The PD generates two signals: $DATA_{lead}$ by XORing $CLK_1$ and $CLK_3$ and $DATAl_{ag}$ by XORing $CLK_1$ and the input data. $DATA_{lead}$ is periodic. The opposite applies to $DATA_{lag}$. While $DATA_{lead}$ acts as the charge-down signal that increases VCO output frequency, $DATA_{lag}$ as the charge-up signal that reduces VCO output frequency. The waveform of the detected signal is shown in Figure. 6, A lock condition is achieved if the input data is phase-aligned with $CLK_3$. $DATA_{lead}$ is considered as a reference signal and $DATA_{lag}$ as an error signal. By comparing these two signals, phase and frequency errors can be detected. An example of phase correction is when the input data leads $CLK_3$, the high state of $DATA_{lead}$ is longer than that of $DATA_{lag}$. The surplus part of $DATA_{lead}$ reduces the charge in the loop filter and shortens the clock period. An example of frequency correction is when the input data frequency is smaller than that of $CLK_3$, the surplus part of

$DATA_{lag}$ reduces the charge in the loop filter, thus, speeding up the clock. The advantages of this technique include simple implementation, a large acquisition range, and high lock speed as it detects both phase and frequency errors of the input signals. This type of PDS, however, is sensitive to input data pattern and the metastability that occurs in the lock condition.

## 2.6 Sample & Hold PD

The schematic of a sample & hold (S/H) PD is shown in Figure. 2.6 [7]. It is realized as a master-slave S/H circuit (an analog D flip-flop). Each rising transition of $D_{in}$ samples VCO output. The circuit generates an output that is linearly proportional to the phase error of the inputs**.**

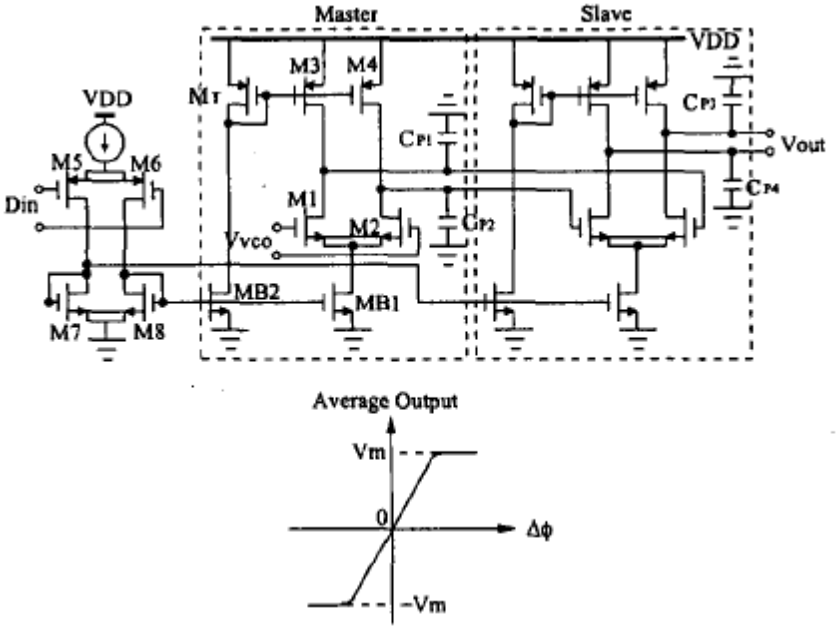


Figure. 2.6. Sample and Hold PD

Both the master and slave stages are realized using a differential pair whose tail current and load device turn off simultaneously, thereby storing the instantaneous value of $V_{VCO}$ on the parasitic capacitances $C_{p1}$-$C_{p4}$. The geometry of transistors $M_T$, $M_3$, and $M_4$ is chosen such that when *MT* is on, *M3* and *M4* are forced into the triode region, eliminating the need for common-mode feedback. The control of the S/H circuit is implemented using PMOS transistors to allow operation from a low-supply voltage. The behavior of the PD in the vicinity of lock can be seen from its characteristics in Fig.2.6. The advantages of S/H PDs are low power consumption and low activity on VCO control line in the lock condition. S/H PDs are sensitive to input data pattern. Although the flip flop is implemented using analog circuitry, the speed of the PD is limited by that of the current steering circuitry.

## 2.7 Bang-bang PD

The block diagram of the CDR circuit employing a bang-bang PD is shown in Figure.2.7 [9]**.** Five positive edge-triggered D-flip-flops (DFF) are used to sample the input data.

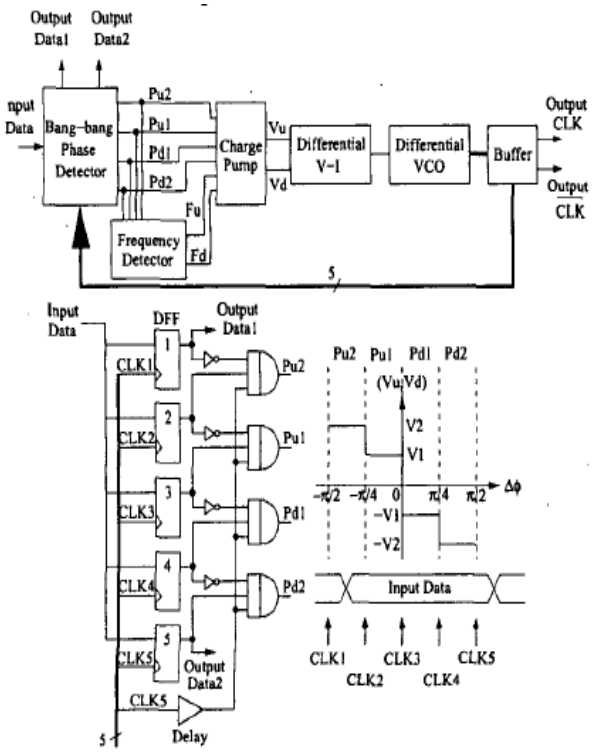


Figure. 2.7. Bang-bang PD.

The VCO generates five clock signals $CLK_1 \sim CLK_5$ phase shifted by $\pi/4$. The PD generates Pull $P_{u1}$ $P_{u2}$, $P_{d1}$ and $P_{d2}$, which provide the digitized phase error information. These signals are fed to a frequency detection circuit where frequency acquisition is performed. The optimum sampling point occurs when $CLK_3$ is phase-aligned with the input data transitions. The PD output pulses represent the occurrence of the data transitions between the adjacent sampling clocks. Their width is fixed at half the clock period. The time delay of the Delay unit connected to $CLK_5$ is equal to a flip flop propagation delay. The PD output controls the charge pump to create four differential voltage steps $\mp V1$ and $\mp V2$ at the input of the VCO. The direction of the voltage steps depends on the occurrence of the data transition versus $CLK_3$**.** These voltage steps result in corresponding frequency steps $\mp \Delta f1$ and $\mp \Delta f2$ **.**A larger step is used in the vicinity of lock to enhance the acquisition range and lock speed. A smaller one is used during the lock condition to reduce the activity on the VCO control line. An advantage of this technique is the reduced activity on VCO control line. Its drawback is the metastability that occurs in the lock condition.

## 2.8 Half-Rate Phase Detectors

At very high speeds, it may be difficult to design oscillators that provide an adequate tuning range with reasonable jitter. For this reason, CDR circuits may sense the input random data at full rate but utilize a VCO running at half the input rate. This technique also relaxes the speed requirements of the phase detector and, in some CDR configurations, the frequency dividers Called *half-rate* architectures, such CDR topologies require a phase detector that provides a valid output while sensing a full-rate random data stream and a half-rate clock.

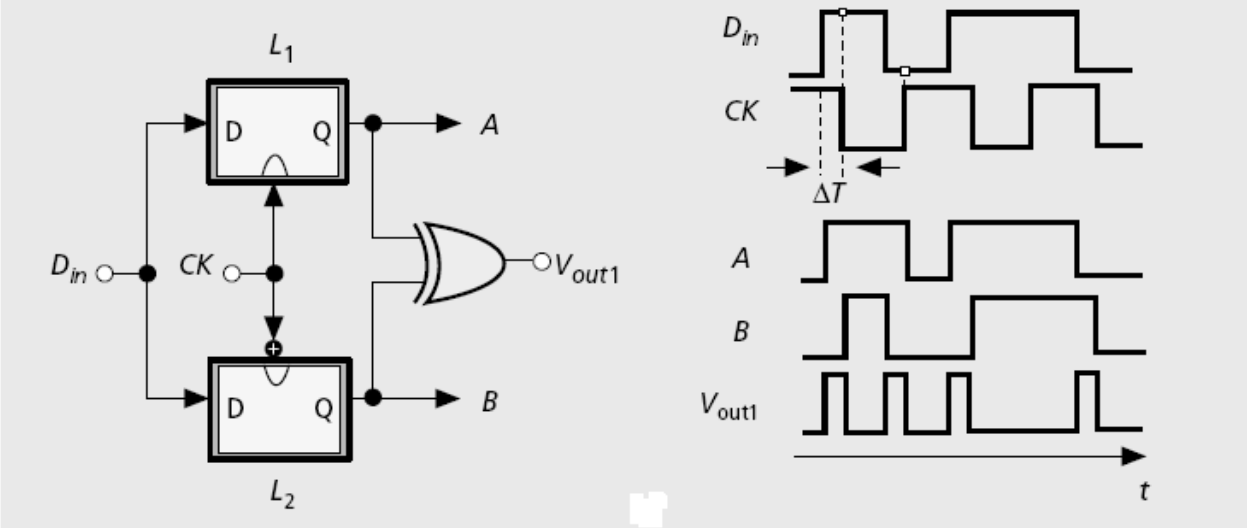


Figure 2.8(a) A linear half-rate PD

It is important to note that none of the above PDs studied thus far can operate with a half-rate clock. However, data transitions may be detected properly if *both edges* of the half-rate clock are utilized to sample the input data. Consider the topology shown in Figure 2.8(a), where two D latches, *L*1–*L*2, operate on opposite edges of the clock. Note that each latch is transparent for half of the clock cycle, passing data transitions to its output. Assuming *Din* leads *CK* by Δ*T* and *L*1 is transparent when *CK* is high, we observe that *A*1 goes high *before CK* falls and remains high until *CK* rises. In other words, *L*1 produces a pulse width equal to *TCK*/2 + Δ*T*. On the other hand, if *L*2 is transparent when *CK* is low, *A*2 goes high when *CK* falls and remains high only until *Din* falls. That is, *L*2 generates a pulse width of *TCK*/2⊕ Δ*T*. Thus, *A*1 ⊕ *A*2 exhibits a pulse of width Δ*T* for each data transition. The above study implies that the simple topology of Figure 2.8(a) can indeed operate as a linear phase detector because it:

• Detects data edges

• Produces proportional pulses

However, as with the Hogge topology, this circuit must also provide a reference output to uniquely represent the phase error for different data transitions. To this end, let us follow the latches with two more (creating a master-slave flip flop in each path) and XOR the outputs (Figure. 2.8 b). In the presence of data transitions, the outputs of *L*3 and *L*4 change on the falling and rising edges of the clock, respectively. As a result, $C \oplus D$ contains a pulse width of *TCK*/2 for each input data edge, serving as the reference output [8].

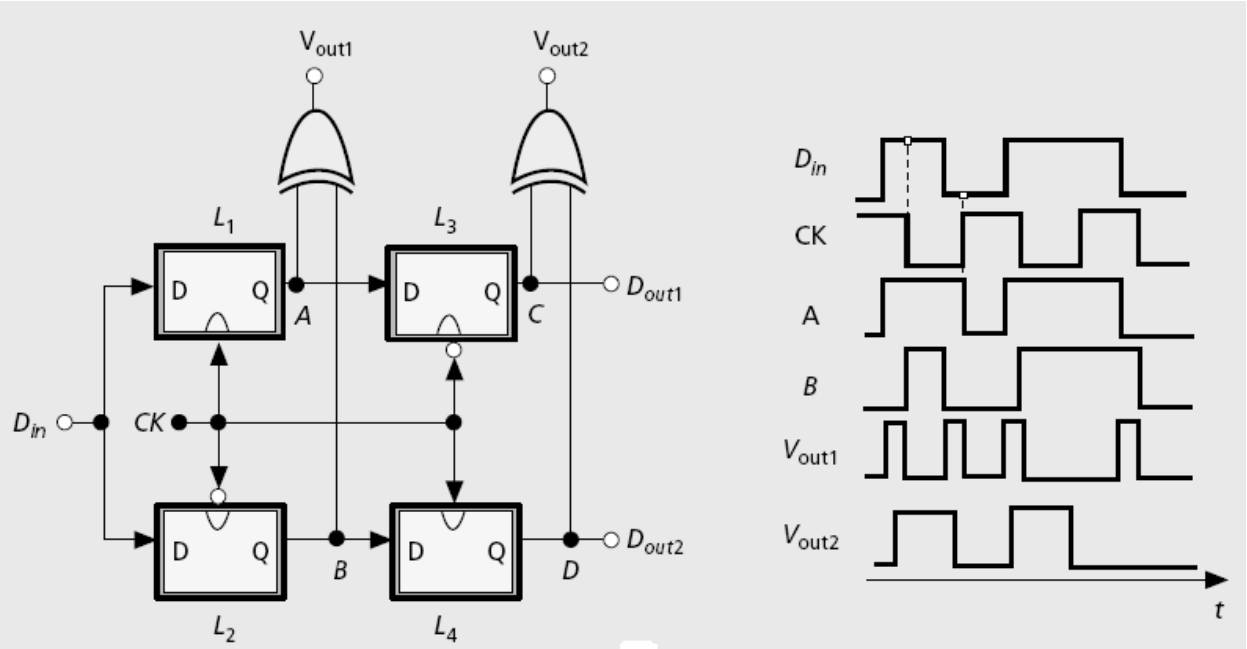


Figure 2.8(b) A complete half-rate PD

How does a CDR loop employing the PD of Figure 2.8(b) lock to random data? If the clock edge is to strobe the data in the middle of the eye, the proportional pulses are *TCK*/4 s wide, whereas the reference pulses are *TCK*/2 s wide. The disparity between the average values of these outputs is removed by scaling down the *effect* of the output of the second XOR by a factor of two, that is, halving the corresponding current source in the charge pump. The half-rate PD of Fig.2.8(b) also retimes and demultiplexes the data, producing two streams at the outputs of *L*3 and *L*4. The linear characteristic of the circuit allows simple formulation of the loop dynamics.

Let us now consider the early-late method for half-rate operation. Since the Alexander PD already requires sampling on both clock edges for full-rate detection, it must employ additional phases of the clock if it is to operate in the half-rate mode. Shown in Figure 2.8'(a), the solution involves sampling the data by both the in-phase and quadrature phases of the clock, $CK_I$ and $CK_Q$, respectively.

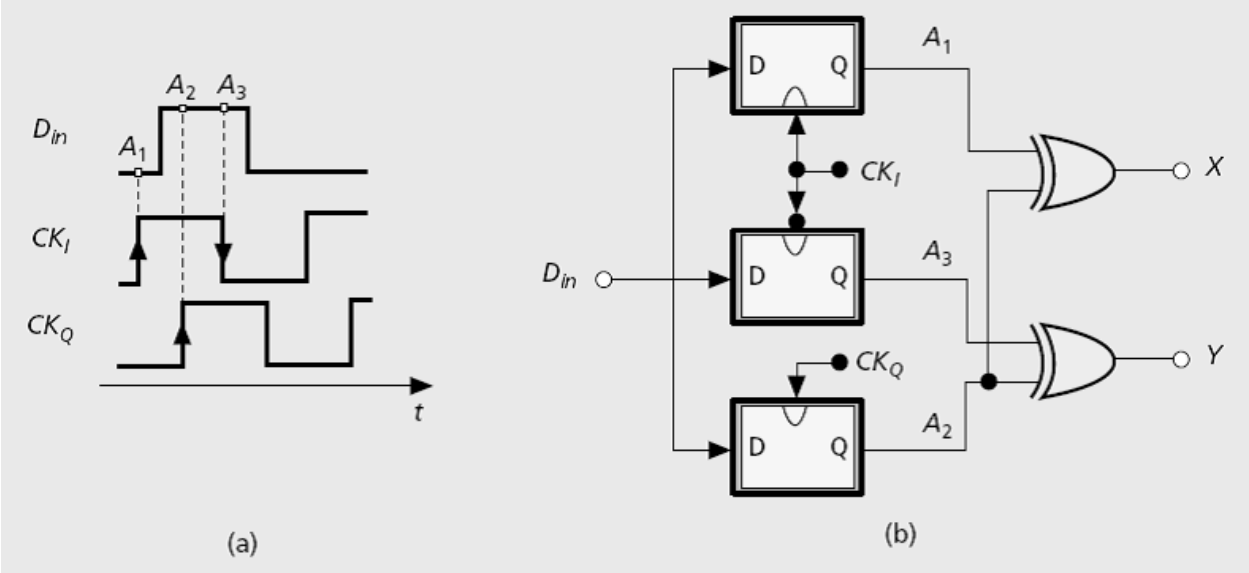


Fig. 2.8'(a) The use of quadrature clocks for half-rate phase detection; (b) A half-rate binary PD.

Now, $A_1$, $A_2$, and $A_3$ play the same role as the consecutive samples in a full-rate counterpart. As depicted in Fig. 2.8'(b), the implementation incorporates three FFs sampling the data by $CK_1$ and $CK_Q$, and two XOR gates producing $A_1 \oplus A_2$ and $A_2 \oplus A_3$. Under the locked condition, the rising edge of $CK_Q$ occurs in the vicinity of the data zero crossings.

## 2.9 Hogge PD

How can a PD detect data transitions if it samples the data by the VCO output? A single DFF fails to operate as a phase detector if it is used in such a mode. However, recognizing that a DFF produces a delayed replica of the input data, we can arrive at a synchronous edge detector (Figure. 2.9a). Since sample B changes only on the CK edges, Y = Din $\oplus$ B contains pulses whose width represents the phase difference between Din and CK. It is important to note that (a) the circuit produces a pulse for each data transition, providing edge detection, and (b) the width of the output pulses varies linearly with the input phase difference, suggesting that the circuit can operate as a linear PD. We call this type of output proportional pulses.

It may appear that the topology of Figure 2.9(a) satisfies the requirements of a phase detector and can therefore be used as such. Unfortunately, however, the average value of the output is a function of the data transition density, failing to uniquely represent the phase difference for various data patterns. For example, the average output remains unchanged if the transition

density falls by a factor of two and the phase difference rises by the same factor. In other words, two different phase errors may result in the same dc output, leading to false lock.

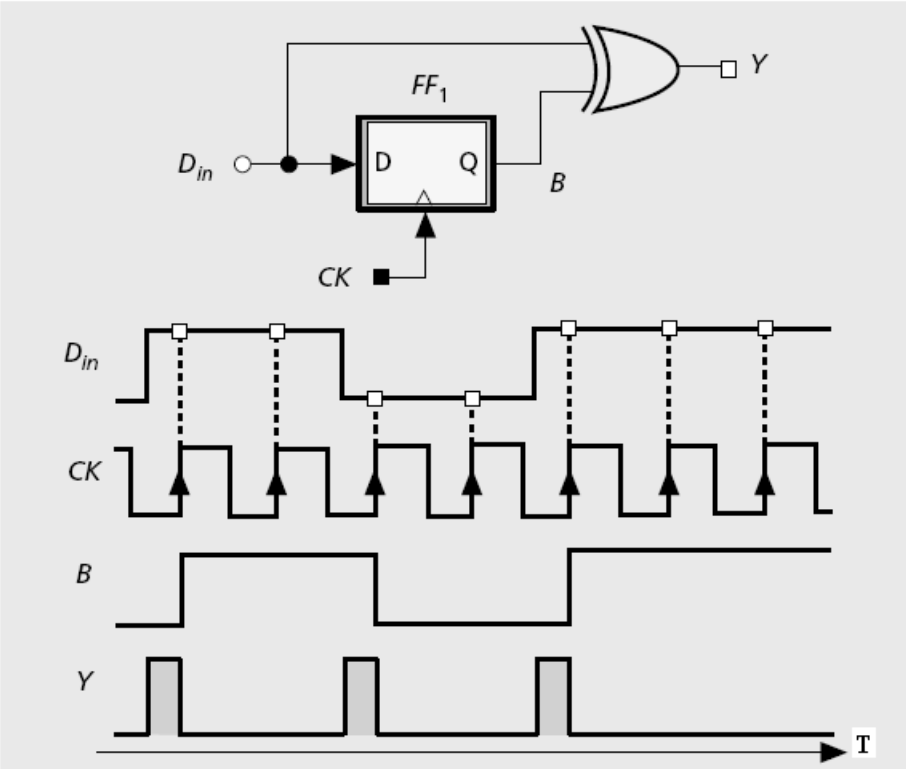


Figure 2.9(a) A simple PD using synchronous edge detection

To overcome the above ambiguity, the proportional pulses must be accompanied by reference pulses. The latter are pulses that appear only on data edges but exhibit a constant width, eliminating the pattern dependency. How can reference pulses be generated? We note that if the retimed data (at point B) in Figure 2.9(a) is delayed by half a clock cycle, TCK/2, and XORed with itself, pulses of width TCK/2 are produced for each data transition. As depicted in Figure 2.9(b), the difference between the areas under X and Y can be viewed as the PD output, eliminating the ambiguity due to transition density. Note that under locked condition, X and Y produce equal pulse widths. This circuit is called the Hogge phase detector [4]. Let us summarize our thought process thus far. In order to avoid skews in the decision circuit, we choose to sample the data by the clock even in the PD. This in turn requires explicit edge detection, carried out by a DFF and an XOR gate. Finally, we produce a reference pulse to eliminate ambiguity for different data transition densities.

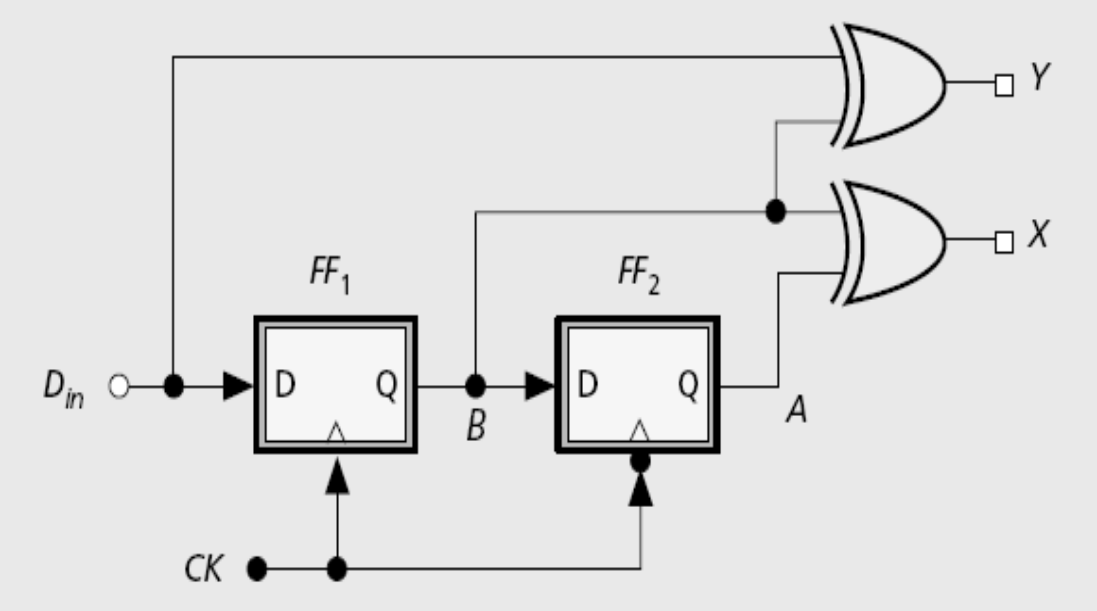


Figure 2.9(b) A Hogge PD

Recall that the principal motivation behind the above development is to retime the data inside the PD. Does the Hogge PD accomplish this? Indeed, both flip flops in Figure 2.9(b) operate as decision circuits as well, thereby providing retimed data. It is instructive to examine the behavior of the Hogge PD in the presence of finite delays in the flip flops. Owing to the *CK*-to-*Q* delay, Δ*T*, of *FF*1, *B* changes Δ*T* seconds after the clock rises, yielding a pulse at the *Y* output that is Δ*T* s wider than the actual phase difference between *Din* and *CK*. On the other hand, the *CK*-to-*Q* delay of *FF*2 simply *shifts* the pulses at *A* by Δ*T*, still producing a pulse width equal to one clock period. As a result, *X* continues to produce pulses of width *TCK*/2 for each data transition. This means, with a zero input phase difference, the proportional pulses are wider than the reference pulses by Δ*T* s. Thus, under locked condition, *Din* and *CK* must sustain a skew of Δ*T* to equalize the widths of the *X* and *Y* pulses.

The above skew effect becomes a serious issue at high speeds. Since Δ*T* can be a significant fraction of the clock period, a systematic phase offset of several tens of degrees may arise after the loop is locked, degrading the clock phase margin and hence the jitter tolerance. In order to resolve this difficulty, we can either narrow the proportional pulses by Δ*T* [11] or widen the reference pulses by the same amount. A drawback of the Hogge PD stems from the half-cycle skew between the two XOR outputs [10,11]. Under locked condition, the PD produces the reference pulse *after* the proportional pulse, thereby creating a skew of *TCK*/2 between the two. As a result, the VCO phase (which is proportional to the integral of the control voltage) is severely disturbed. The phase detector can be modified to ameliorate this issue [11]. The Hogge topology is a linear PD, generating a small average as the phase difference approaches zero.

Thus, a charge pump driven by a Hogge PD experiences little “activity” when the CDR loop is locked. This behavior is in contrast to that of the bang-bang PD.

## 2.10 The Alexander Phase Detector

The Alexander configuration is another example of PDs providing inherent data retiming. Following our reasoning for the Hogge PD, we note that this property requires that the data be sampled by the clock, but a single DFF does not suffice. Nonetheless, if the clock strobes the data waveform at multiple points in the vicinity of expected transitions, the resulting samples can provide the necessary information.

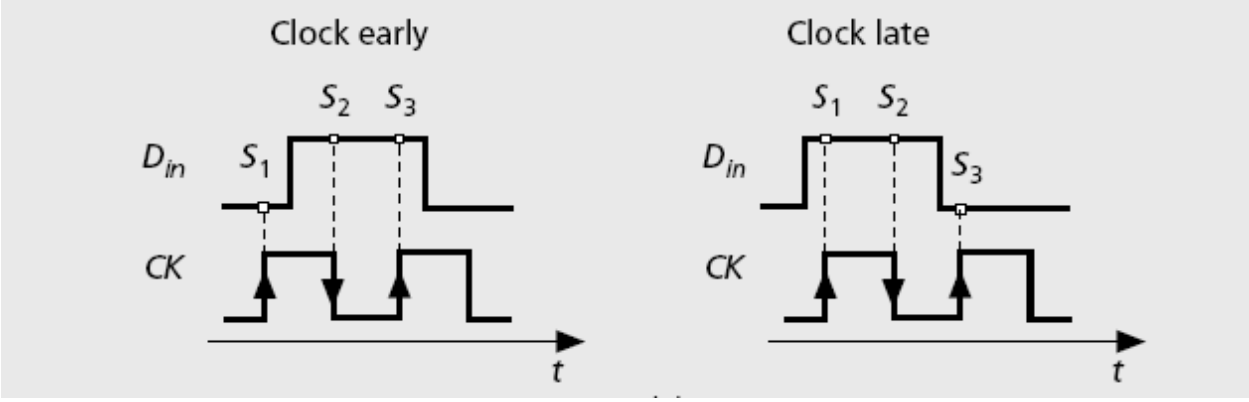


Figure 10(a) Three-point sampling of data by clock

Figure 10(a) illustrates the Alexander PD principle, also known as the early-late detection method. Utilizing three data samples taken by three consecutive clock edges, the PD can determine whether a data transition is present, and whether the clock leads or lags the data. In the absence of data transitions, all three samples are equal and no action is taken. If the clock leads (is early), the first sample, S1, is unequal to the last two. Conversely, if the clock lags (is late), the first two samples, S1 and S2, are equal but unequal to the last sample, S3. So, S1 $\oplus$ S2 and S2 $\oplus$ S3 provide the early late information:

• If $S1 \oplus S2$ is high and $S2 \oplus S3$ is low, the clock is late.

• If $S1 \oplus S2$ is low and $S2 \oplus S3$ is high, the clock is early.

• If $S1 \oplus S2 = S2 \oplus S3$, no data transition is present.

The foregoing observations lead to the circuit topology shown in Figure 10(b) [12]. Flip flops FF1 and FF2 sample their D inputs on the rising edge of CK, producing S3 and S1, respectively. Flip flop FF3 samples Din on the falling edge of CK, and flip flop FF4 delays this sample by half a clock cycle, generating S2. Note that the sampling points are defined by FF1 and FF3; the other two FFs merely serve as delay elements.

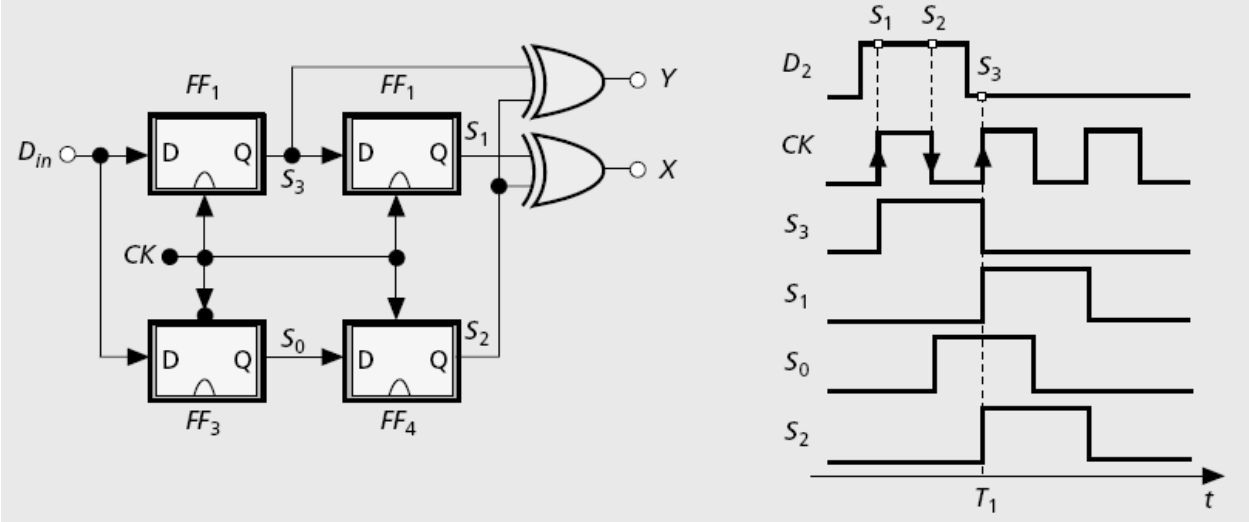


Figure 10(b) An Alexander phase detector

Let us examine the waveforms at various points in the Alexander PD to gain more insight into its operation. As depicted in Figure 11(b), the first rising edge of CK samples a high data level. The second rising edge of CK then accomplishes two tasks: it produces a delayed version of the first sample at the output of FF2 and samples the low level on the input data. The values of S1 and S2 are therefore valid for comparison at t = T1, remaining constant for one clock period.

On the first rising edge of CK in Figure 10(b), FF1 samples a high level on the input data, and on the next rising edge, FF2 reproduces this level. The key point here is that the choice of clock phases for the four FFs ensures that S1, S2, and S3 reach valid levels for comparison at t = T1, and remain at these levels for one clock period. As a result, the XOR gates always generate valid outputs simultaneously.

The Alexander PD is a bang-bang system, exhibiting a very high gain in the vicinity of $\Delta\phi = 0$. Consequently, a CDR loop utilizing this PD locks such that S2 coincides with the data zero crossings. While exhibiting a bang-bang characteristic, the Alexander PD offers two critical advantages over a simple DFF PD, namely:

I. It retimes the data automatically, producing a valid data waveform at the output of FF1 and FF2 in Figure 10(b).
II. In the absence of data transitions, it generates a zero dc output, leaving the oscillator control undisturbed.

As a result, for long data runs, the VCO frequency drifts only due to device electronic noise rather than due to a high or low level on the control line.

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# CHAPTER-3

## CMOS REALIZATION OF OTRA

Operational transresistance amplifier (OTRA) has been realized in a number of configuration by using CMOS circuits [1-2]. A few of these configurations are realized in this chapter using SPICE as simulation tool. OTRAs are commercially available from several manufacturers under the name of current differencing amplifier but it was not widely used until recently [3]. These commercial realizations do not provide internal ground at the input port and they allow the input current to flow in one direction only. The former disadvantage limited the functionality of the OTRA whereas the latter forced to use external dc bias current leading to complex and unattractive designs [6]. In recent years, several high-performance CMOS OTRA realizations have been presented in the literature [2, 4]. This leads to growing interest for the design of OTRA-based analog signal processing circuits.

## 3.1 OTRA REALIZATION-I

CMOS realization of OTRA as presented in [6] is shown in Fig. 3.1. It consists of a differential current controlled current source (DCCCS) followed by a voltage buffer.

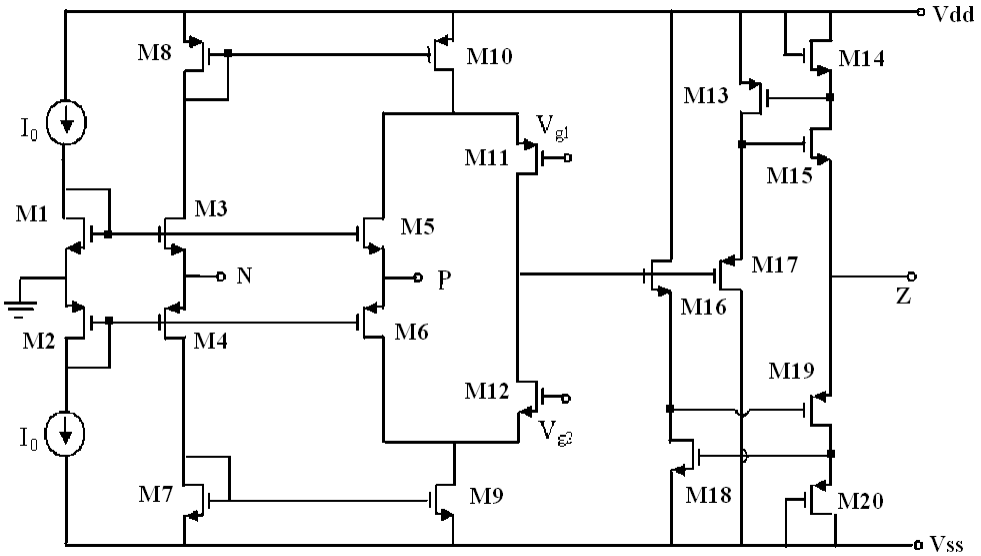


Fig.3.1 CMOS Realization of OTRA

In this circuit, the aspect ratio of the transistor M3 (M4) should be twice as large as those of M1 (M2) and M5 (M6). If the transistor M5 and M6 are removed, the implementation in Fig. 3.1 becomes a CFOA, composed of a CMOS CCII followed by the voltage buffer. Since the OTRA can be considered as a collection of current and voltage-mode unity gain cell, this element is free from many parasitic and is expected to be suitable for high-frequency operation. The Spice schematic of OTRA is shown in Fig 3.2 and its simulated DC response is shown in Fig.3.3.

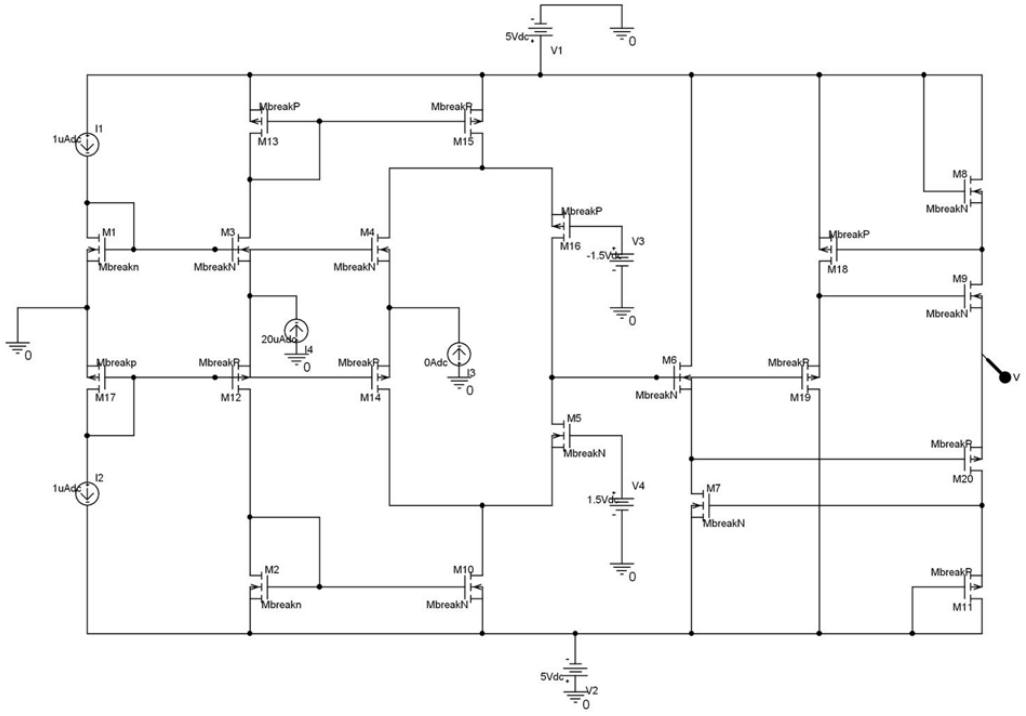


Fig.3.2 Spice schematic of CMOS Realization of OTRA (Internal Block 1)

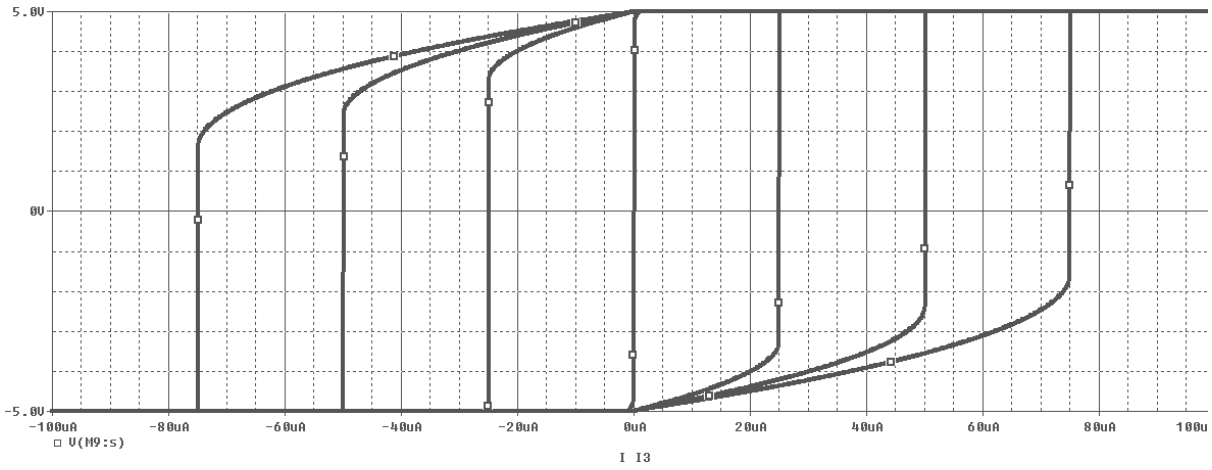


Fig.3.3 DC Response of the OTRA Circuit

## 3.2 OTRA REALIZATION-II

The OTRA presented in [3] is shown in Fig.3.4. It is based on the cascaded connection of the modified differential current conveyor (MDCC) [5] and a common source amplifier. The MDCC provides the current differencing operation, whereas the common source amplifier provides high gain.

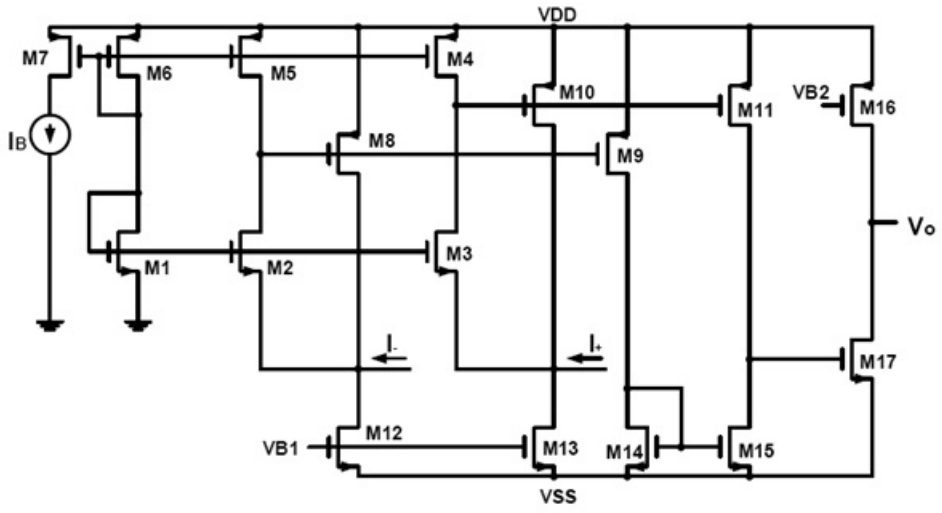


Fig.3.4 CMOS Realization of OTRA

The current mirrors formed by (M4-M7) forces equal currents ($I_B$) in the transistors M1, M2 and M3. This operation drives the gate to source voltages of M1, M2 and M3 to be equal and consequently, forces the two input terminals to be virtually grounded. The current mirrors formed by the transistor pairs (M4 and M5), (M8 and M9), (M10 and M11) and (M14 and M15) provide the current differencing operation, whereas the common source amplifier (M17) achieves the high gain stage [2]. In this operation it is assumed that each of the groups of the transistors (M1-M3), (M4-M7), (M8 and M9), (M10 and M11), (M12 and M13) as well as (M14 and M15) are matched and all the transistors operate in saturation region. The Spice schematic of the circuit proposed in [3] is shown in Fig 4.5 and simulated DC response of the same is shown in Fig 3.6.

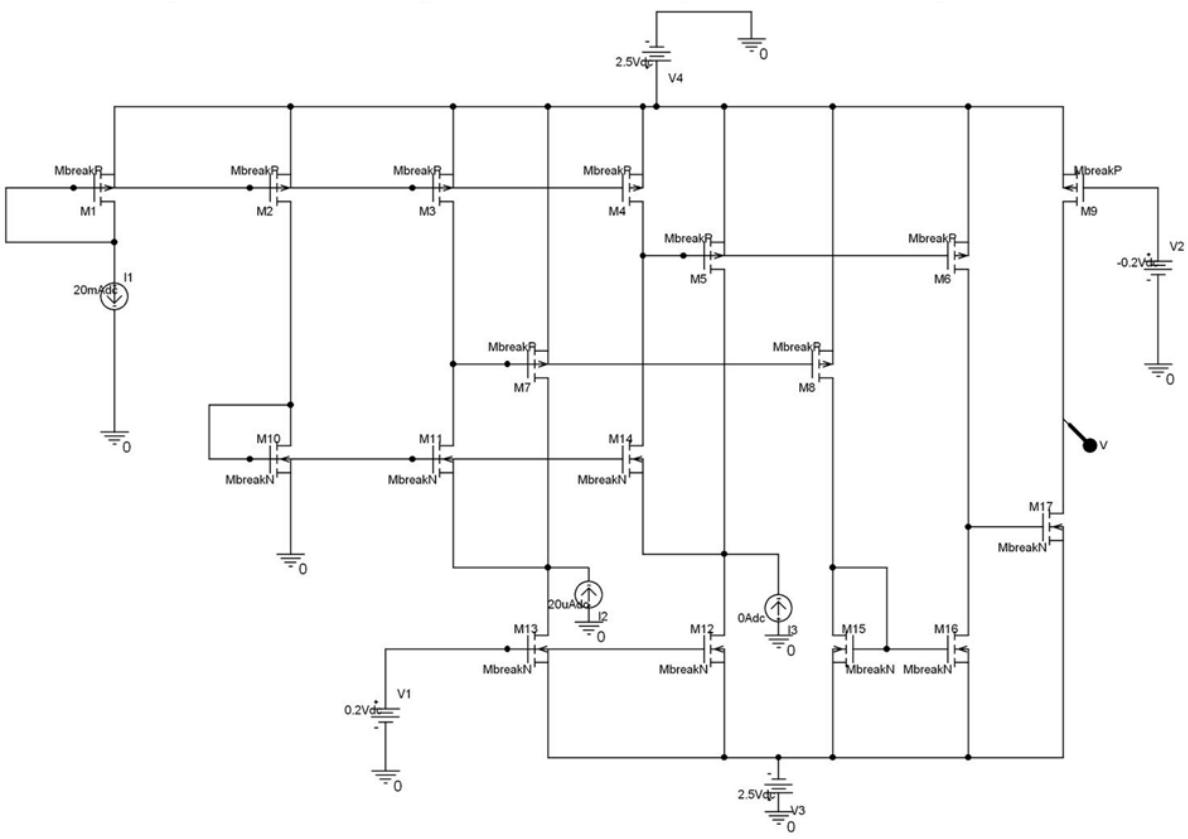


Fig.3.5 Spice schematic of CMOS realization of OTRA (Internal Block 2)

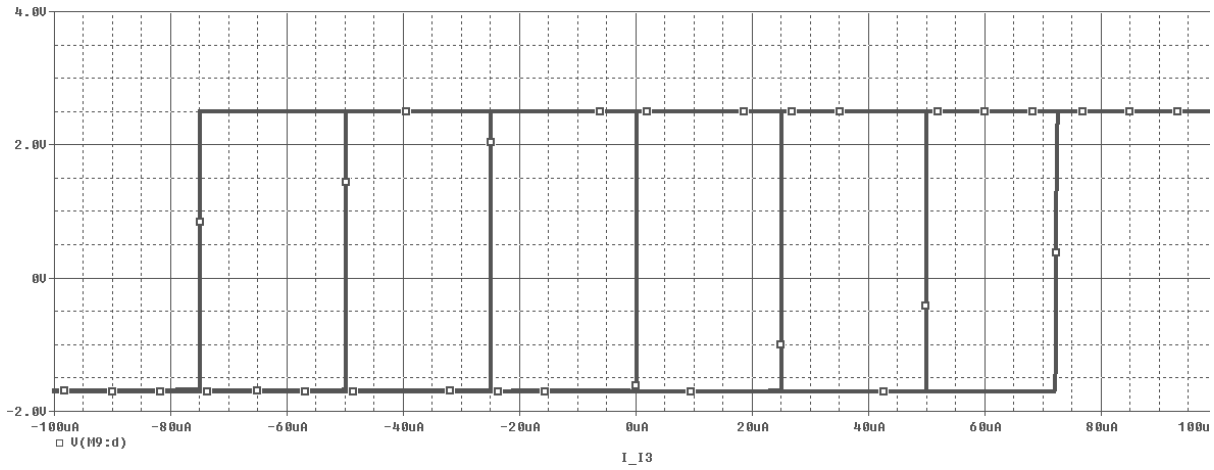


Fig.3.6 DC Response of the OTRA Circuit

## 3.3 OTRA REALIZATION-III

Another CMOS realization of the low power wide band OTRA as presented in [4] is shown in Fig. 3.7. It is based on the cascaded connection of the modified differential current conveyor (MDCC) and a common source amplifier. Assuming that each of the groups of the transistors (M1-M3), (M5 and M6), (M8-M11) and (M12 and M13) are matched and assuming that all the transistors operate in the saturation region, the circuit operation can be explained as follows:

The current mirrors formed by (M8-M11) forces equal currents ($I_B$) in the transistors M1, M2 and M3. This operation drives the gate to source voltages M1, M2 and M3 to equal and, consequently, forces the equal terminals to be virtually grounded. The current mirrors formed by the transistor pair (M10 and M11) and (M12 and M13) provide the current differencing operation, whereas the common source amplifier (M14) achieves high gain. The modified OTRA has smaller number of current mirrors than the OTRA introduced in [2] which reduces the transistor mirror mismatch effect and also increases the frequency capabilities. Moreover, this OTRA uses smaller number of transistors which reduces the power dissipation. The Spice schematic of the OTRA is shown in Fig.3.8. The simulated DC response is shown in Fig.3.9.

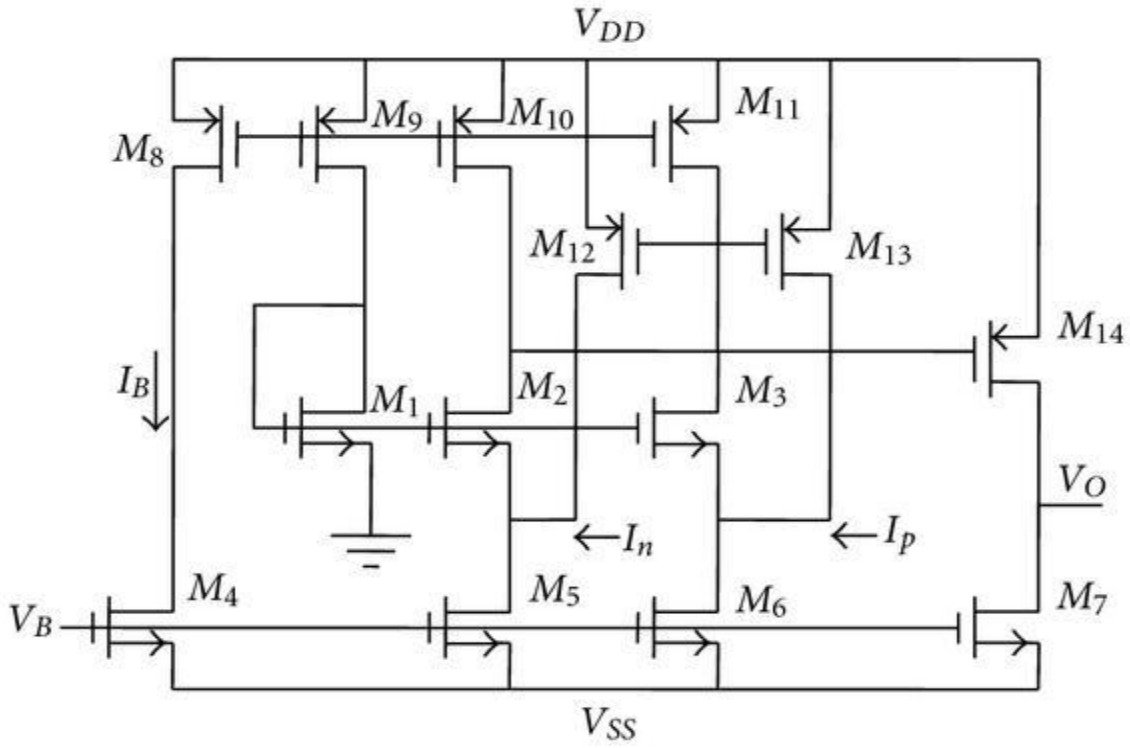


Fig.3.7 CMOS Realization of OTRA

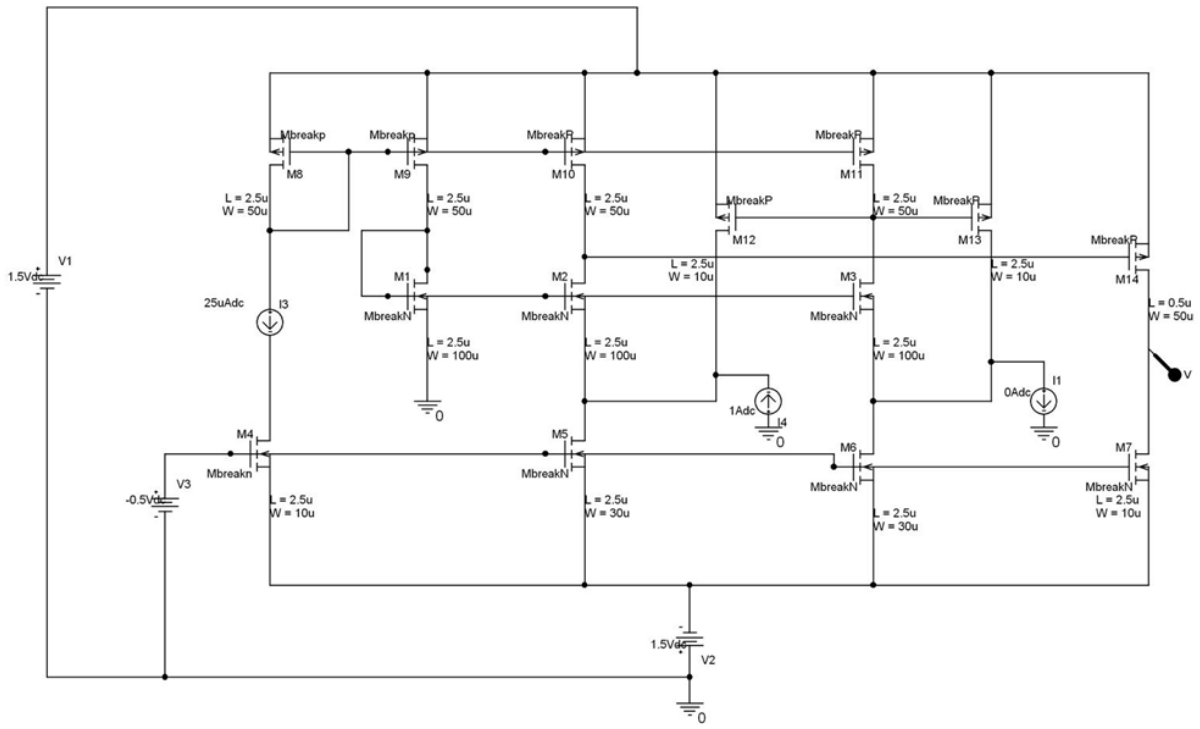


Fig.3.8 Spice schematic of CMOS realization of OTRA (Internal Block 3)

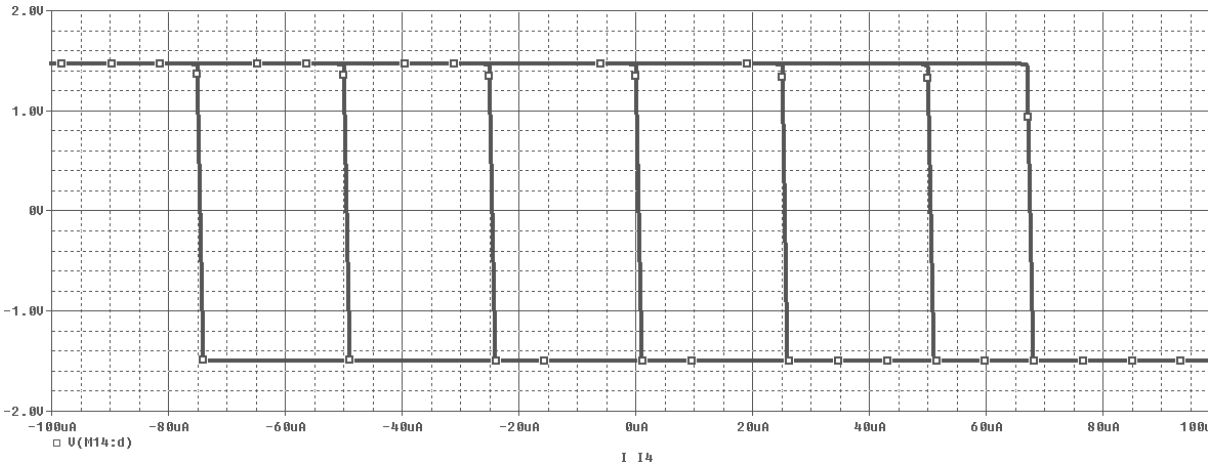


Fig.3.9 DC response of the realized OTRA

## 3.4 OTRA REALIZATION-IV

The AD844 is a high speed monolithic operational amplifier fabricated using Analog Devices' junction isolated complementary bipolar (CB) process. It combines high bandwidth and very fast large signal response with excellent dc performance. Although optimized for use in current to voltage applications and as an inverting mode amplifier, it is also suitable for use in many non- inverting applications. The AD844 can be used in place of traditional op amps, but its current feedback architecture results in much better ac performance, high linearity and an exceptionally clean pulse response.

This type of op amp provides a closed-loop bandwidth which is determined primarily by the feedback resistor and is almost independent of the closed-loop gain. The AD844 is free from the slew rate limitations inherent in traditional op amps and other current-feedback op amps.

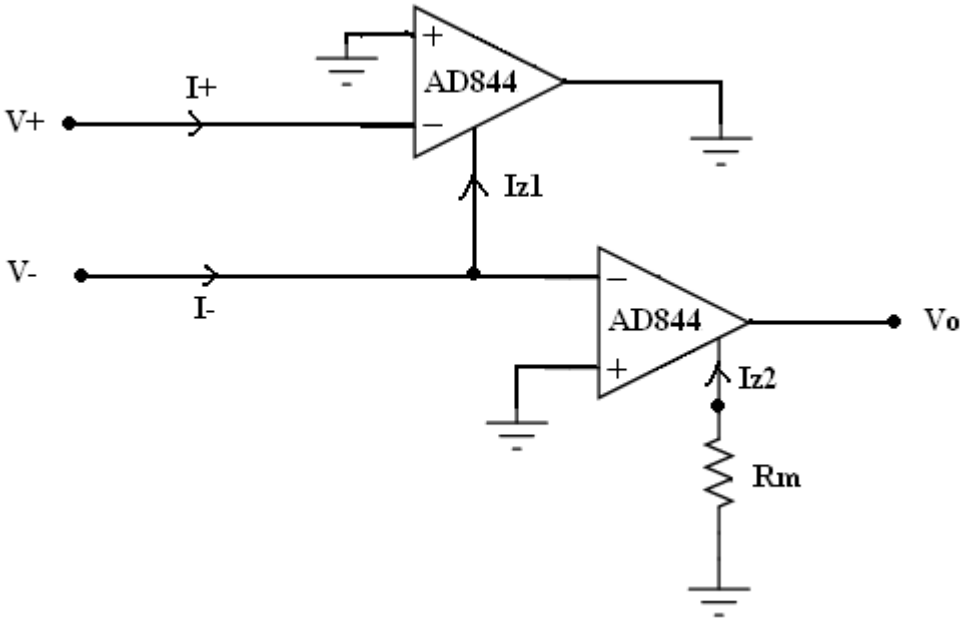


Fig.3.10 CFOA Realization of OTRA

In order to simulate the virtual ground for the two input terminals of the OTRA, the non-inverting terminals of the AD844ANs have been grounded. TheAD844AN differs from the conventional operational amplifier in that the voltage on the non inverting signal input is transferred to the inverting input. Thus an inherent virtual short exists between these two terminals without any external negative feedback path. Owing to this characteristic, the following relations can be obtained.

$$V_{+} = V_{1-} = V_{1+} = 0 \quad \& \quad V_{-} = V_{2-} = V_{2+} = 0 \tag{3.1}$$

Another feature of the AD844AN is that the current into the inverting terminal is equal to the current into the slewing node $T_Z$ & the output voltage is the same as the voltage appearing at this pin.

$$I_{T1} = I_{1-} = I_{1+} \tag{3.2}$$

$$V_{o1} = V_{T1} = V_{2-} = 0 \tag{3.3}$$

$$I_{T2} = I_{2-} = I_{-} - I_{T1} = I_{-} - I_{+} \tag{3.4}$$

$$V_{o} = V_{o2} = V_{T2} = -R_{m} * I_{T2} = R_{m} * (I_{+} - I_{-}) \tag{3.5}$$

Thus wiring two CFOAs in this manner shown in Figure 3.10, the terminal equations of OTRA can be realized. Fig 3.11 is the schematic of OTRA realized using CFOAs and Fig3.12 shows the DC response.

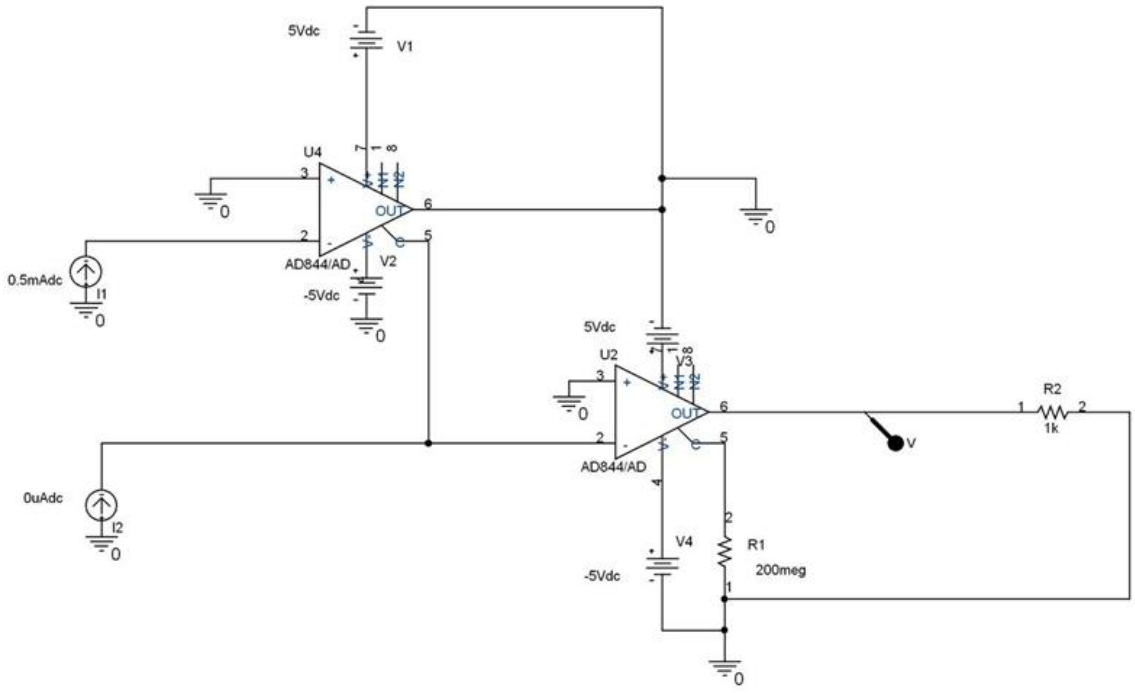


Fig.3.11 CFOA realization of OTRA (Internal Block 4)

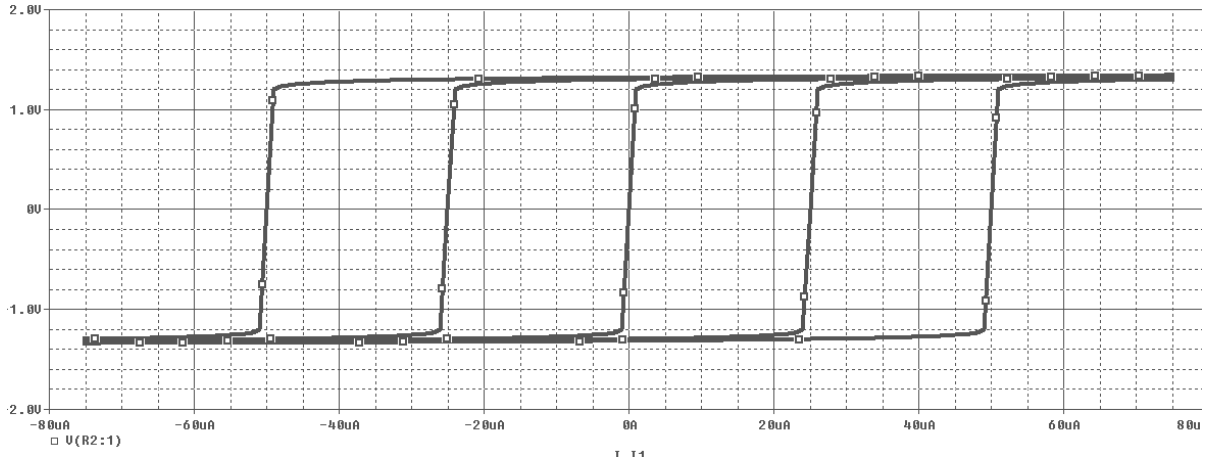


Fig.3.12 DC response of the realized OTRA

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# CHAPTER-4

## PROPOSED LINEAR PHASE DETECTOR

After going through the available literature work on linear Phase Detector (PD), it has been found that no PD circuit design based on analog building blocks (ABB) is available. So, in this thesis work, an OTRA (a current mode ABB) based phase detector using a simple scheme has been presented. As described above, the bandwidth of the OTRA is independent of the closed loop gain and is suitable for high frequency applications which make the proposed linear Phase Detector (PD) suitable for high frequency applications.

## 4.1 ARCHITECTURE

The OTRA based phase detector is shown in Fig. 4.1. It consists of two OTRAs, a CMOS XOR circuit and an RC integrator. To interface the XOR gate with the integrator, a buffer circuit is used so that the loading effect of the integrator can be avoided. Both the OTRAs are used in open loop configuration to work as comparator.

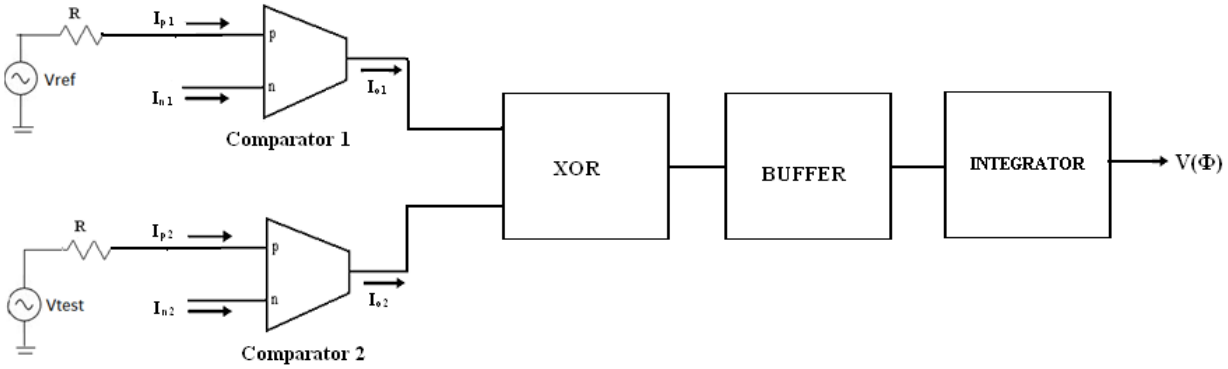



Fig.4.1 Proposed PD circuit

## 4.2 MATHEMATICAL ANALYSIS

A reference sinusoidal is applied to the comparator 1 and comparator 2 is driven by another sinusoidal signal whose phase is to be detected. Considering a sinusoidal signal to be applied at comparator1 is represented as

$$V_{ref} = V_m \cos \omega t \quad (4.1)$$

The current $i_{p1}$ through p terminal of OTRA1 is given by

$$i_{p1} = \frac{V_m}{R} \cos \omega t \quad (4.2)$$

The current $i_{n1}$ for OTRA 1 being zero, the output of the comparator will be at positive saturation level $+V_{sat}$ for positive half cycle of $v_{ref}$. During the negative half cycle of input voltage the comparator output will be zero. Thus comparator1 provides a periodic rectangular output as shown in Fig. 4.2(a). Representing $+V_{sat}$ by A, the output of the comparator can be expressed as

$$V_1(t) = \begin{cases} A; & 0 < t \leq T/2 \\ 0; & T/2 \leq t \leq T \end{cases}$$

An another sinusoid of same frequency, delayed in phase by an angle $\Phi$ is applied to the comparator 2 which can be expressed as

$$V_{test} = V_m \cos(\omega t - \Phi) \quad (4.3)$$

The current $i_{p2}$ through p terminal of OTRA2 can be computed as

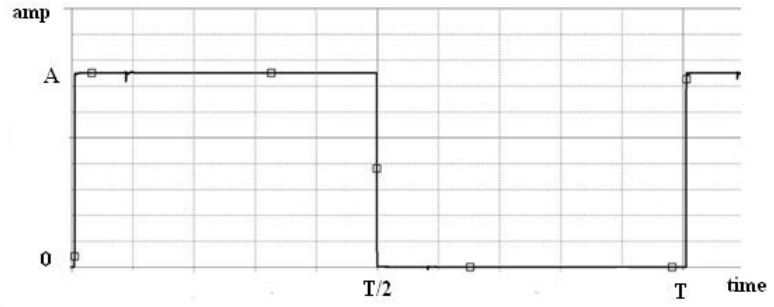
$$i_{p2} = \frac{V_m}{R} \cos(\omega t - \Phi) \quad (4.4)$$

Since the $i_{n2}$ is zero the output of comparator 2 will be similar as that of output of comparator 1 but delayed in time by $\Phi/\omega$ as depicted in Fig. 4.2(b) and can be expressed as

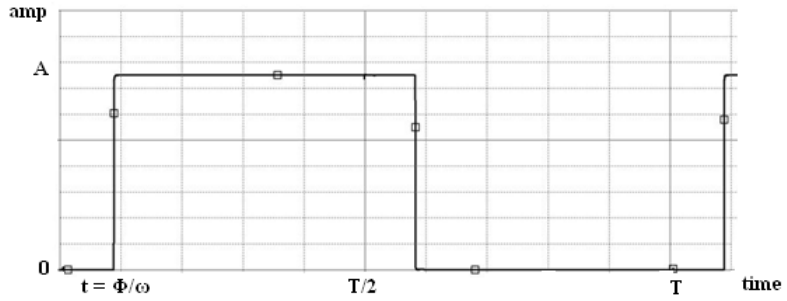
$$V_2(t) = \begin{cases} 0; & 0 < t \leq \frac{\Phi}{\omega} \\ A; & \frac{\Phi}{\omega} \leq t \leq \frac{T}{2} + \frac{\Phi}{\omega} \\ o; & \frac{T}{2} + \frac{\Phi}{\omega} \leq t \leq T + \frac{\Phi}{\omega} \end{cases} \quad (4.5)$$

The outputs of the comparators serve as input to a XOR gate which gives a pulsed output of period $\Phi/\omega$ , as shown in Fig. 4.3 and represented as

$$\mathrm{V}_3(\mathrm{t}) = \begin{cases} A; 0 < t \leq \frac{\Phi}{\omega} \\ A; \frac{T}{2} \leq t \leq \frac{T}{2} + \frac{\Phi}{\omega} \\ 0; otherwise \end{cases} \quad (4.6)$$




(a)




(b)

Fig. 4.2 Output of comparators (a) ($v_1$ (t)). (b) ($v_2$ (t))

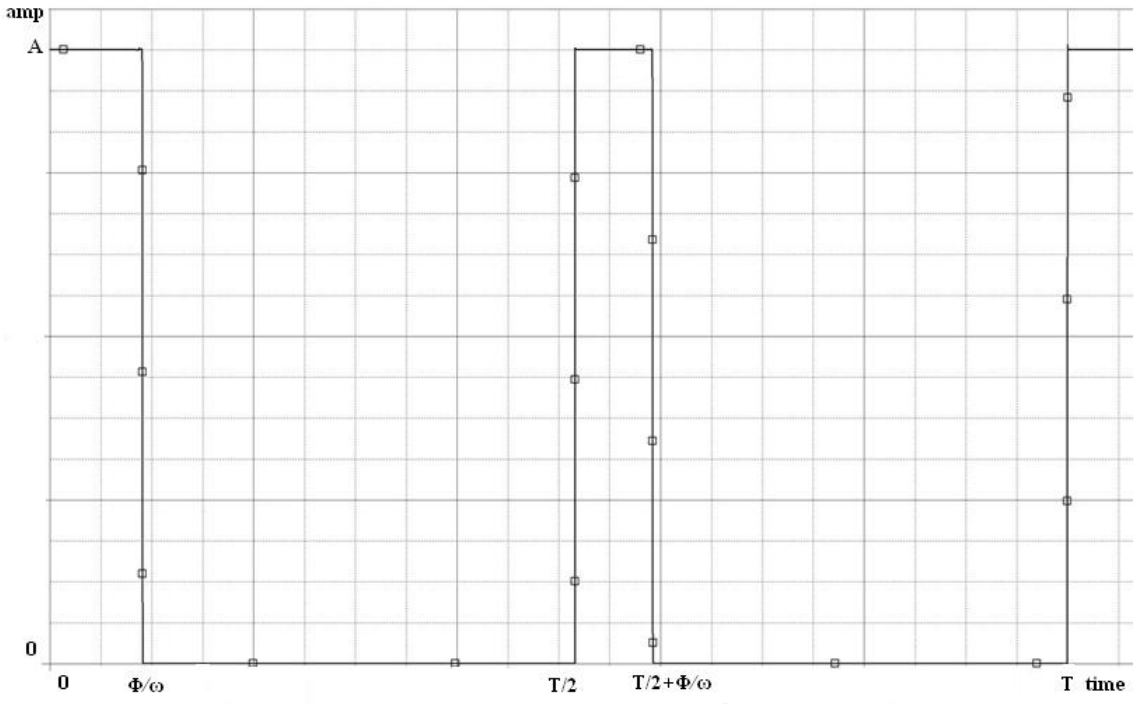



Fig. 4.3 Output of XOR Gate

The output of the XOR Gate is integrated to obtain V($\Phi$), the output of the proposed phase-detector, which is given by

$$V(\Phi) = A[1 - e^{-t/RC}]$$

$$= A[1 - \{1 - \left(\frac{t}{RC}\right) + \left(\frac{t}{RC}\right)^2 - \left(\frac{t}{RC}\right)^3 + \cdots\}] \quad (7)$$

For RC $\gg$ $t$, V ($\Phi$) may be expressed as

$$V(\Phi) = A[1 - \left\{1 - \left(\frac{t}{RC}\right)\right\}]$$

$$= \frac{At}{RC} \quad (4.8)$$

Let the output of the XOR Gate be integrated from t=0 to t=T/2;

$$V(\Phi) = \frac{A\Phi}{RC\,\omega} \quad (4.9)$$

Equation (4.9) clearly shows that the proposed PD produces an output voltage proportional to the phase delay of the applied sinusoidal signal.

## 4.3 SIMULATION RESULTS

The workability of the proposed PD circuit is verified through SPICE simulations using 0.35 µm CMOS process parameters. The CMOS implementation of the OTRA described in REALIZATION-II is used and is reproduced in Fig.4.4.

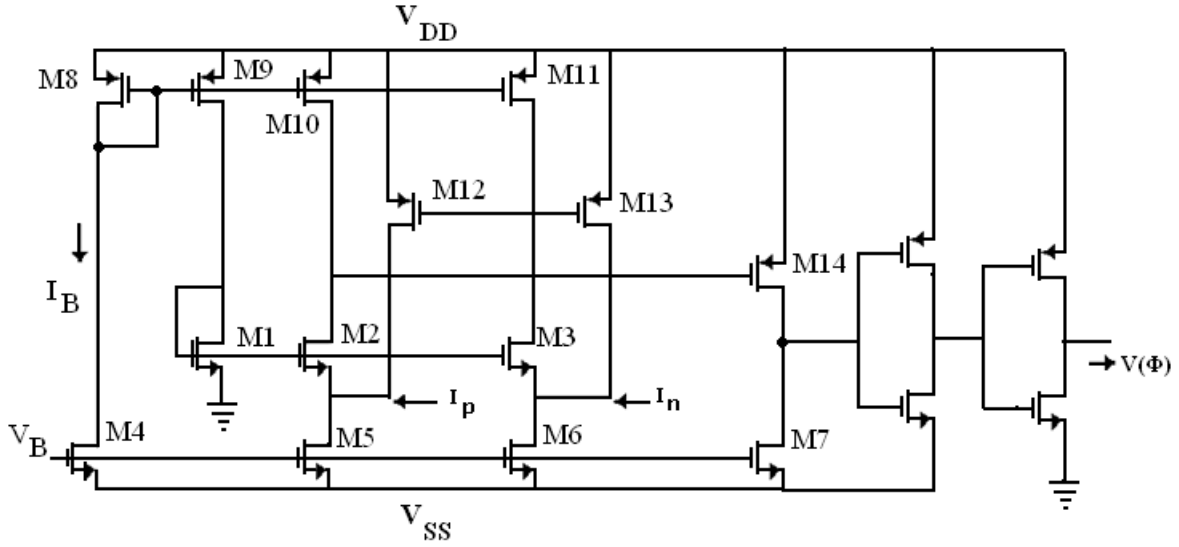



Fig.4.4 CMOS Implementation of OTRA

Supply voltages are taken as ± 1.5V. Fig.5.5 shows current waveform $i_{p1}$ (corresponding to reference sinusoidal signal $v_{ref}$ ) of 1KHz frequency applied at p terminal of comparator 1 along with current waveforms $i_{p2}$ applied at p terminal of comparator 2 for three test signals of same frequency but phase - delay (Φ) of 30°, 60° and 90° respectively. The outputs of comparator 1 and comparator 2 for applied inputs are shown in Fig. 4.6(a) and Fig. 4.6(b) respectively. The output of the XOR gate is shown in Fig.4.7. It can be observed from Fig.4.7 that with increasing phase delay (Φ) the duration of the output waveform of the XOR gate increases. The simulated output pulse duration for Φ = 30°, Φ = 60° and Φ = 90° are observed to be 90.578 $\mu$s, 174.123 $\mu$s and 257.595 $\mu$s respectively. The output of the proposed PD V(Φ), as obtained by integrating the XOR output is shown in Fig.4.8. The simulated power dissipation of the proposed circuit is 39 mw. For this simulation R=5KΩ and C=5$\mu F$.

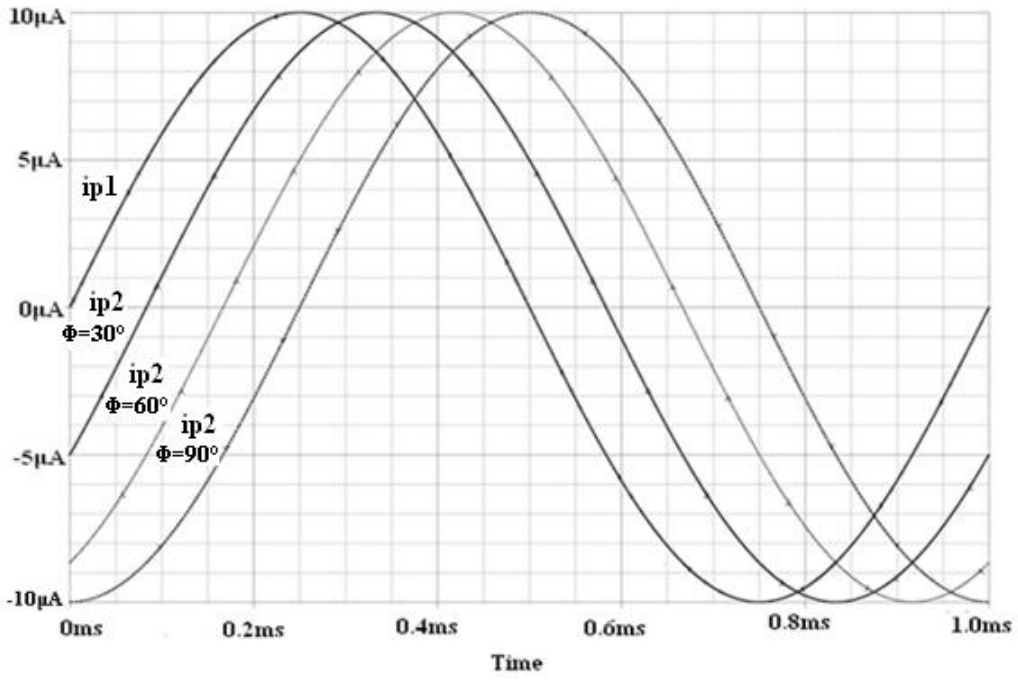



Fig. 4.5 Input waveforms to Phase Detector

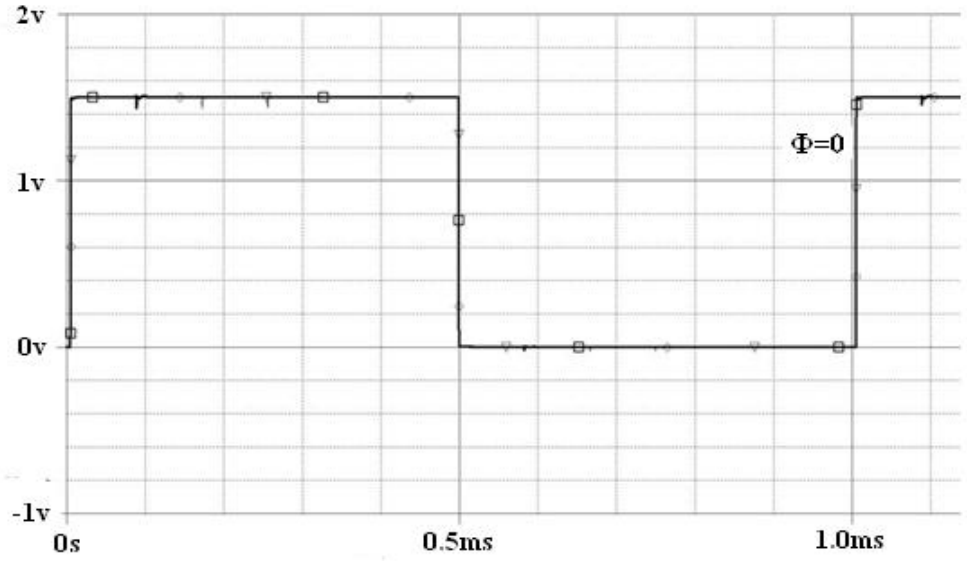



Fig. 4.6(a) Output waveform of Comparator 1

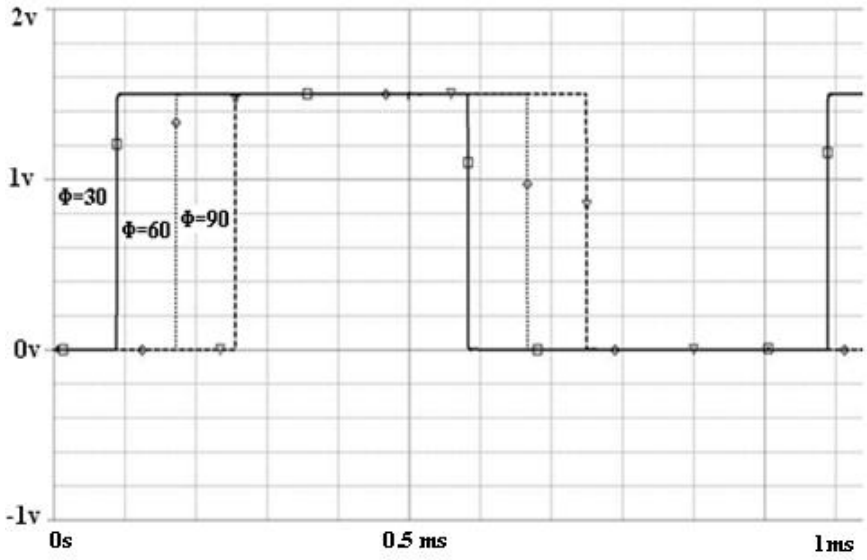



Fig. 4.6(b) Output waveforms of Comparator 2

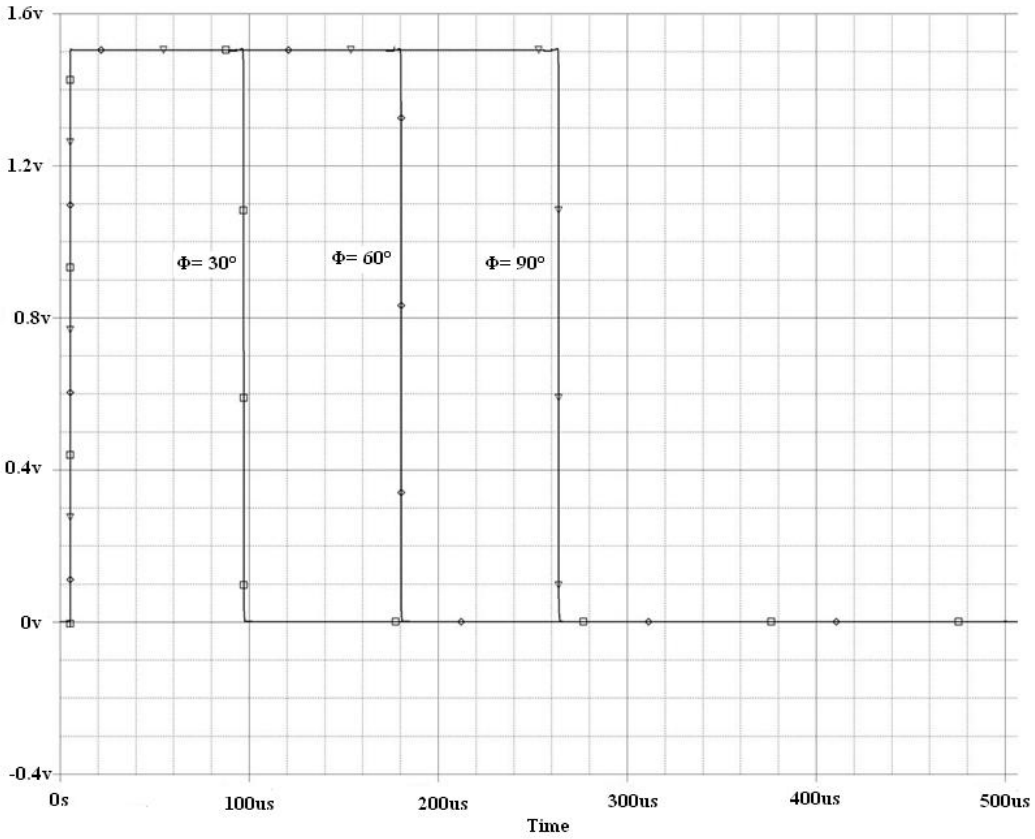



Fig. 4.7 Output of XOR gate

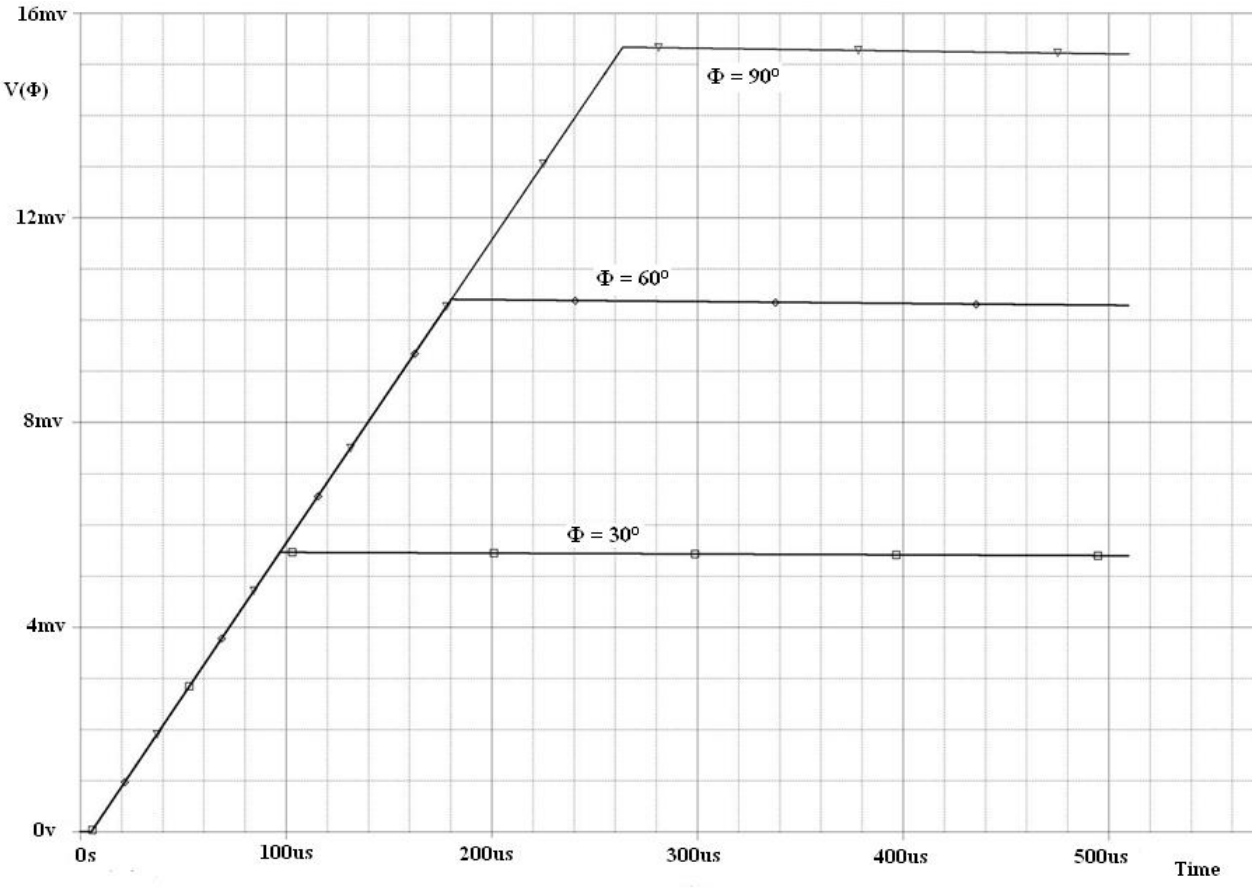



Fig.4.8. Output Voltage, V(Φ)

**Table1: Theoretical Output∼ Simulated Output**

| **Phase, Φ** | **Theoretical Output** | **Simulated Output, V(Φ)** |
|---|---|---|
| 30° | 5 Mv | 5.395 Mv |
| 60° | 10 Mv | 10.235 Mv |
| 90° | 15 Mv | 15.103 Mv |

It may be noted from the above table that with increase in phase (Φ), output voltage V(Φ) increases linearly. It can be seen that

$$V(\Phi) \propto \Phi \text{ volt}$$

Empirically it is observed that the proportionality constant is dependent on the time-constant of the integrator. Hence, with the help of output waveform V(Φ), the phase deviation (Φ) present in any sinusoidal signal can be calculated .

# CONCLUSIONS & FUTURE WORK

In this thesis work, an Operational Trans-Resistance Amplifier (OTRA) based Linear Phase Detector circuit has been presented. As described in the preceding paragraph, the proposed circuit produces an output voltage proportional to the phase of the applied input signal. The theoretical results have been presented through SPICE simulations. It can be seen from the previous table that the simulation results are compatible with the theoretical results. . The power dissipation of the proposed linear phase detector is very less (in mV).

All the components of the proposed linear phase detector except the buffer has been composed of active elements.In future, this component may be replaced by any other active-element circuit which would reduce the power requirement of the proposed phase detector circuit.