CHAPTER 1

INTRODUCTION

1.1Background

Analog VLSI can address almost all real world problems and finds exciting new information processing applications in variety of areas such as integrated sensors, image processing, speech recognition, hand writing recognition etc. All conventional analog circuits namely op amps, voltage to frequency converters , voltage comparators etc are voltage mode circuits (VMCs) , which suffer from low bandwidth arising due to stray and circuit capacitances and are not suitable in high frequency applications . The need for low-voltage low power circuits is immense in portable electronic equipments like laptop computers, pace makers, cell phones etc. The VMCs [1] are rarely used in low-voltage circuits as the minimum bias voltages depend on the threshold voltages of the MOSFETs. However, in current mode circuits (CMCs) the current decides the circuit operation and enables the design of system that can operate over wide dynamic range. The low end of circuit operating range is limited by the leakage current and noise flow level while the high end is decided by degradation of the trance conductance per unit current available above the threshold voltage. Higher bandwidth very low operating voltage, better linearity, low power consumption, and simple architecture are the key advantages offered by current mode processing. During the last few decades, the current mode processing has emerged as low voltage design technique for analog design and has become a viable alternative because of its inherent advantages over voltage mode circuits.

Due to the advantages offered by current mode processing it is becoming powerful tool for the development of high performance analog circuits and systems. The maturity of current mode signal processing is seen from the development of systems based on the current mode approach. A wide spectrum of applications includes important areas such as continuous-time and sampled-data filters through general analog interfacing, A/D and D/A converters to current-mode neural networks.

1.2 Motivation

Advances in current mode processing has led to the emergence of new analog building blocks as detailed in [39] and refrences cited there in. Current difference buffered Amplifiers (CDBA) is one such building block of relatively recent origin which exploits all advantages offered by current mode processing. The block diagram of CDBA is shown in Fig. 1.1. The CDBA contains a Current Differencing Unit (CDU) and a voltage unity-gain buffer. It has two low-impedance terminals, p and n. The difference of currents I_p and I_n flows out of the z terminal and the corresponding voltage drop on the external impedance connected at z terminal is copied by the buffer to the w output. Due to low input impedance terminals, CDBA is free from parasitic capacitances and hence is appropriate for high frequency operation. It provides further flexibility to the designers, enabling a variety of circuit designs, as it can operate in both current and voltage mode.

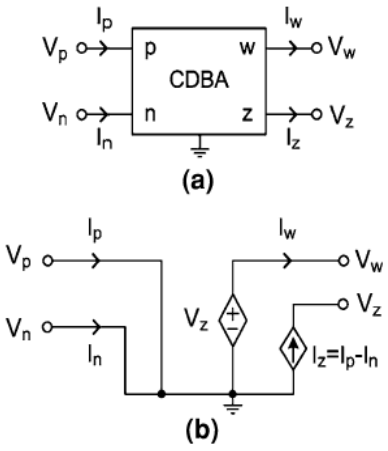

Fig 1.1 (a) Symbol of CDBA (b) equivalent circuit of CDBA

1.3 Objective and scope of work

Keeping in view the above discussions this project is undertaken with a motive to develop the analog application using low power, low voltage CDBA. The following are the objectives of this dissertation:

- To study and analyse different types of low voltage low power CMOS current differential buffer amplifier.

- To study and analyse different types of analog application using low voltage low power CMOS current differential buffer amplifier.
- Comparative analyses of different simulated analog application in terms of various performance parameters.
- To propose new circuit designs

To achieve this aim, initially literature review was done and various existing designs are studied and implemented. In order to implement these analog applications a low voltage, low power CMOS current differential buffer amplifier proposed in [21] is used. Literature review also suggested the areas which could be explored to propose new designs. It is well known that active inductance simulation has been an important research topic in active network synthesis and finds application in areas such as filter design, oscillator design, phase shifters and parasitic element cancellation. Keeping this in view a new grounded inductor topology is proposed. Signal generators are an important class of circuits and find wide application in electronic system design. The available literature on CDBA suggested that the area of nonlinear signal generation has not been explored much and has lot of potential. This resulted in proposition of an monostable multivibrator. A feedback controller circuit using single CDBA is also presented in this work which can be used for system performance improvement. The proposed designs are simulated using SPICE to test their functionality. The simulated results are also compared with the theoretical results.

1.4 Organization of the Dissertation

In chapter 2 literature review is presented illustrating the research that has already been done by the authors in perspective of CMOS Current differential buffer amplifier (CDBAs).

In chapter 3 internal structure of a low voltage low power CMOS CDBA is explained and is characterized through PSPICE using TSMC 0.18 µm CMOS process parameters.

Chapter 4 deals with various existing signal processing and generation applications of CDBA such as filters, multiplier, floating inductor etc. Various applications are implemented using low voltage low power CMOS current differential buffer amplifier. These implementations are then simulated using PSPICE.

Chapter 5 presents the new proposed circuits using CDBA such as a multi output filter, a grounded inductor, a monostable multivibrator and a PID controller using single active element and the effect of various circuit parameters is also evaluated.

Chapter 6 concludes the dissertation and future scope of work is also presented.

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CHAPTER 2

Literature Review

2.1 Introduction

Traditionally, most analog signal processing operations have been accomplished employing the voltage as the signal variable and Op-Amps were the main building blocks for the realization of analog circuits during the decades of seventies and eighties. However the performance of these op-amp based circuits are limited due to constant gain bandwidth product and slew limitation of op-amp. Due to the increasing demand for operation in the high frequency region and the finite gain-bandwidth product associated with operational amplifiers, a change from voltage mode circuits was required. Recently, current mode analog integrated circuits in CMOS technology have received considerable interest and has resulted in emergence of variety of ABB and current conveyor (CC) proposed by Smith and Sedra [11] is the oldest and most popular block amongst those. It has been used by many researchers to design different circuits with different properties. Current feedback operational amplifier (CFOA) a yet another analog block which is commercially available as AD844 was developed by analog devices as a high speed op-amp which did not suffer from slew rate limitations and gain bandwidth conflict for medium and low frequency applications. Recently CDBA has emerged as an effective alternate analog building block which is a high gain current input, voltage output amplifier [12]. It was first proposed by Acar and Ozoguz [2] and is derived from current feedback operational amplifier (CFOA). CDBA, being a current processing analog building block, inherits all the advantages of current mode technique and therefore is ideally suited for high frequency applications [18].

It can operate in both current and voltage mode thereby providing a further flexibility and enables a variety of circuit designs. This building block (CDBA) have been employed by many researchers to design analog signal processing circuits with different properties [4-10].

2.2 Literature Review

A variety of papers have been reported on CDBA during the last one and a half decade. This includes various CMOS realization of CDBA and wide variety of signal processing and generation applications such as filters, floating inductor, multiplier oscillator, multivibrator etc.

2.2.1 Reported work on CDBA realization

Tarim and Kuntman [12] proposed a high performance current differencing buffered amplifier by using two second generation current conveyors (CCII) and a voltage buffer. This design offered uses only MOS transistors and is designed to be implemented in CMOS technology.

Sawangarom, Tangsrirat and Surakampontom [13] proposed the NPN based current differencing buffered amplifier. It was shown that the CDBA based on NPN transistor can operate with a minimum power supply of 2 volts. NPN based CDBA consist of two blocks, current differencing circuit and voltage follower. The current differencing circuit is obtained by using two unity gain current amplifier and the current mirror reflects the current to output port.

M. Steyaert, W. Dehaene, J. Craninckx, M.Walsh and P. Real [14] proposed that to realize the same transconductance with transistors of the same gate length, a PMOS gate length must be 3 times wider than a NMOS. This is because the junction capacitance per unit area is approximately 2 times larger for PMOS than for NMOS. In order to avoid the limitation of the high frequency operation effecting from PMOS transistors, the CDBA should be designed so that signals pass through only NMOS transistors. Therefore W.Tangsrirat, K. Klahan, K. Kaewdang and W. Surakampontorn [15] proposed a low voltage wide band NMOS based CDBA, which has a low resistance at both the current-input terminals (p, n) and at the output-voltage terminal (w). It was shown by them that the CDBA based on NMOS transistor was superior in terms of supply voltage and frequency range. It can operate at minimum supply voltage of ±1.25 volts. The realization of NMOS based CDBA was based on the modification of low impedance current conveyor (CCII+) to function as a current differencing circuit and a voltage buffer circuit.

The existing CDBAs do not use low-voltage power supplies and have quite high input terminal resistances, high power consumption, most of them suffer from limited output voltage swing.

Therefore Cem Cakir, Shahram Minaei, and Oguzhan Cicekoglu [16] proposed a low voltage low power CDBA which overcome these drawbacks. Supply voltages of this circuit are chosen as ±0.75 V. The current subtractor circuit exploits the flipped voltage follower current sources (FVFCS). A FVFCS is characterized by very low supply requirements and low impedance at input terminals [17, 18].

Cem Cakir and Oguzhan Cicekoglu [19] in 2008 proposed a low power high performance CDBA, a modification over [16]. This circuit can be operated with the power supplies down to ±0.75V and it also consumes less power than its counterparts. This circuit is based on the flipped voltage follower current sources (FVFCS) which give rise to very low input resistances at the input ports. Output stage of this CDBA offers low output impedance and a moderate output swing. This circuit is a class AB voltage buffer which is based on the differential FVF (DFVF) topology [20].

Cem Cakir, Shahram Minaei, and Oguzhan Cicekoglu [23] in 2009 proposed a low voltage low power CMOS CDBA. The circuit can operate with the minimum supply voltage of ±0.6 volts. Low voltage CDBA circuit, which is based on the use of current differencing circuit and voltage buffer. This circuit offers very low terminal resistance at n and p terminal and consumes much less power as compare to the other CDBA circuits available in literature.

2.3 CDBA Applications

2.3.1 Filters

Various filters have been designed by using CDBA. These filters can be classified into four categories: current mode, voltage mode, trans-impedance mode and trans-admittance mode [4].

Bilgin Metin, Oguzhan Cicekoglu and Kirat Pal proposed a voltage mode all pass filter [5] with a single CDBA which is suitable for high performance analog signal processing.

A voltage mode second order all pass/notch filter with single CDBA was proposed by Cem Cakir, Shahram Minaei, and Oguzhan Cicekoglu [23] which is suitable for low Q applications. Cem Cakir and Oguzhan Cicekoglu [19] also proposed current mode second order notch filter.

A current mode universal filter designed using two CDBAs and six passive elements is proposed by Sawangarom, Tangsrirat and Surakampontom in [13]. This circuit can simultaneously realize

the three current transfer function namely low pass, band pass and high pass functions without changing circuit configurations.

A voltage mode multi input single output type multifunction biquad [6] using single CDBA was proposed by A.U Keskin, using this biquad all standard five filter functions (low pass, high pass, band pass, notch and all pass) can be realized without changing the circuit topology.

S. Pisitchalermpong, T. Pukkalanun, W. Tangsrirat and W. Surakampontom [7] proposed a voltage mode multiple output multi functional biquadratic filters which realizes low pass, high pass, band pass, band stop and all pass transfer functions at low resistance output which directly enables cascading to next stage.

Mehmet Sagbas and Muhammet Köksal [8] proposed a multimode multifunction filter. This filter is eligible to obtain all transfer function characteristics (trans-impedance mode, trans-admittance mode, voltage mode and current mode).

2.3.2 Oscillators

R. Nandi, P. Venkateswaran, Soumik Das and M. Kar [9] proposed CDBA-based realization of electronically tunable band pass (BP) / low pass (LP) filters and voltage controlled quadrature oscillator (VCQO). The circuit uses the CDBA building block along with a multiplier (ICL-8013) element.

A sinusoidal quadrature oscillator with current controlled amplitude was proposed by Danucha Prasertsom and Worapong Tangsrirat [10]. This circuit consists of two CDBAs, three virtually grounded resistors, and two grounded capacitors. The oscillation condition and the oscillation frequency of the circuit are independently controlled by a single resistor, whereas the oscillation amplitude is electronically controlled by an external DC current.

A multiphase sinusoidal oscillator using grounded capacitors was proposed by Sumaytee Pisitchalermpong, Worapong Tangsrirat and Wanlop Surakampontom [22]. The proposed MSO circuit, which is composed of n cascaded CDBA-based lossy integrators and a CDBA-based inverter, can generate n sinusoidal output voltages with phase difference of 180°/n.

Ali Umit Keskin [23] proposed a design of minimum Component Oscillators (MCO) using Negative Impedance (NIC) approach based on CDBA. The NIC based oscillator synthesis procedure consists of two steps: a) A grounded NIC circuit of a given type of active element is found, b) a shunt branch to NIC is connected so that, any real terms are removed in complex plane and a symmetric pole pair is placed on the imaginary axis.

2.3.3 Multivibrators

Rajeshwari Pandey, Neeta Pandey, Sajal K. Paul, Kashish Anand, and Kranti Ghosh Gautam [26] proposed three voltage mode square wave generator circuits using single CDBA. One of the circuits uses passive element adjustment to control the duty cycle, whereas electronic control is used in the other circuit.

2.3.4 Multipliers

A Four Quadrant Analog Multiplier Employing Single CDBA was proposed by ALI U¨mit Keskin [27] consist of single CDBA, two NMOS transistor and a resistor. This design is fully-integrated, simplifies the implementation and reduces the component count while maintaining good performance.

Linearly Tunable Transconductor Using Modified CDBA was proposed by Ali Zeki, Ali Toker and Serdar o¨ Zog˘ uz [28], With a slight modification in current differencing buffered amplifier (CDBA), a new block, namely differential-input current feedback amplifier (DFCA), is obtained. It is shown that, with two additional MOSFETs, this modified CDBA structure can be utilized as a linearly tunable transconductor, which can also be converted to a variable-gain amplifier or an analogue multiplier.

2.2.5 Passive Component Realization

Worapong Tangsrirat and Wanlop Surakampontorn [24] proposed an electronically tunable lossless floating inductance simulator. The floating inductance circuit uses only three current controlled CDBAs (CC-CDBA) and a grounded capacitor. Its equivalent inductance can linearly be tuned by means of the external bias current of the CC-CDBA. Without the employment of any external passive resistors, the proposed inductance simulation circuit is attractive for integrated circuit (IC) implementation.

Ali Ümit Keskin and Erhan Hancioglu [25] introduce two different current differencing buffered amplifiers (CDBA)-based synthetic floating inductance circuits. Both configurations use a grounded capacitor. They are fully integrable and provide the advantages of electronic tuning.

CHAPTER 3

Realization of CDBA

Current-mode circuits are useful for the low voltage operation and therefore, they have been receiving a great deal of interest as an alternative to voltage-mode circuits especially for analog signal processing applications. In addition to the low voltage operation, popularity of current-mode circuits can be attributed to some other features such as larger dynamic range, low power consumption and higher speed.

The current differencing buffered amplifier can operate in both current-mode and voltage-mode, which provides flexibility. Moreover, it is free from many parasitic capacitances and appropriate for high frequency operation.

3.1 CDBA Terminal Characteristics

The block diagram and the equivalent circuit of the CDBA are shown in Fig 3.1 CDBA basically consists of two fundamental building blocks, which are namely current subtractor and voltage follower. The current and voltage characteristics of the ideal CDBA can be described by the following equations;

$$I_Z = I_P - I_n, V_W = V_Z, V_P = V_n = 0 \quad (1)$$

And for practical CDBA equation become

$$I_Z = \alpha_p I_P - \alpha_n I_n, V_W = \beta_v V_Z, V_P = V_n = 0 \quad (2)$$

Where α_p and α_n are current gains, and β_v is the voltage gain. They should be equal to unity in the ideal case.

In practice, they can be expressed as

$$\alpha_p = 1 - \varepsilon_p, \alpha_n = 1 - \varepsilon_n, \beta_v = 1 - \varepsilon_v \quad (3)$$

With

$$|\varepsilon_p| \ll 1, |\varepsilon_n| \ll 1, |\varepsilon_v| \ll 1,$$

ε_p and ε_n denote the current-tracking errors and ε_v denotes voltage-tracking error. It is clear that p and n are current-mode input terminals which have ideally zero impedance. The current of the terminal-z is equal to the difference of the input currents, I_p and I_n. Therefore, it is defined as the current output which has ideally infinite impedance. Moreover, the voltage of terminal-w follows that of terminal-z. Hence, terminal-w is the voltage output that should have zero impedance.

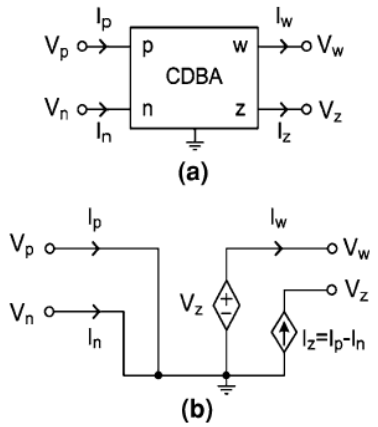

Fig 3.1 CDBA (a) Block diagram (b) Equivalent circuit

3.2 Low voltage Low power CMOS CDBA

Low voltage CDBA circuit [21] is based on the use of the current differencing circuit (M_1–M_8) and the voltage buffer (M_9–M_{14}). The circuit is supplied by the voltages of ±0.6 V. The performance of the CDBA is verified with PSPICE using 0.18 µm, level 7 parameters provided by TSMC.

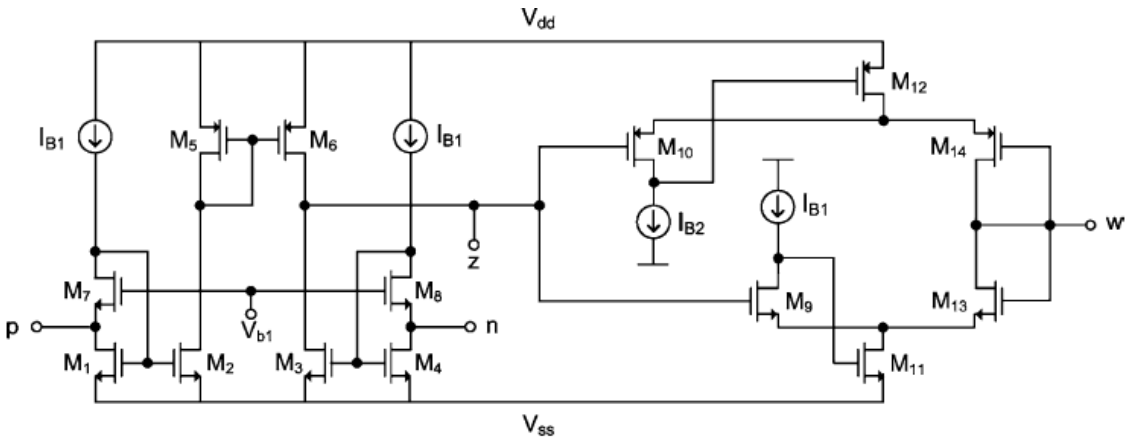

Fig 3.2 CMOS realization of CDBA

The aspect ratios of the transistors are reported in Table 3.1. The bias currents I_{B1} and I_{B2} are selected as 56 µA and 84 µA, respectively.

Table 3.1 Aspect Ratios of the transistors

Transistor	**W/L (µm/µm)**
M_1, M_2, M_3, M_4	3.6/1.8
M_5, M_6	180/1.8
M_7, M_8	180/1.8
M_9	45/0.36
M_{10}	240/0.36
M_{11}	72/0.36
M_{12}	240/0.36
M_{13}	72/0.36
M_{14}	240/0.36

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Due to the n-well process “B”-bulk-terminals of all NMOS transistors are shorted to the most negative power supply, namely Vss; and “B” terminals of all PMOS transistors are shorted to their “S”-source-terminals. These connections can be seen in Figure 3.3(a) and 3.3(b). It can be

note that, three-terminal (drain, gate and source) MOSFET symbols are used in circuit schematics to avoid complexity.

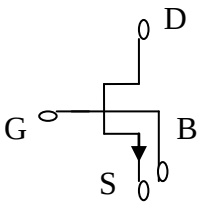

Figure 3.3(a)

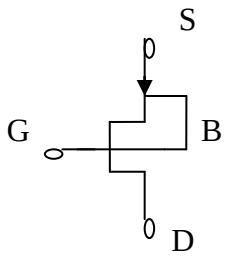

Figure 3.3(b)

Figure 3.3(a) NMOS and Figure 3.3(b) PMOS transistor's "B"-bulk-terminal connections.

The current subtractor circuit is based on the flipped voltage follower current sources (FVFCS) which provide very low input resistances at the input terminals. The FVFCS is shown in Fig.3.4

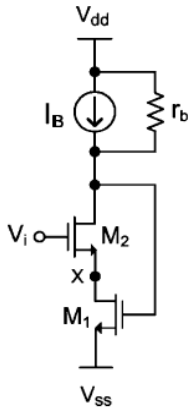

Fig 3.4 Flipped voltage follower current source

The current subtractor circuit is illustrated in Fig 3.2 which consists of the transistors M_1 to M_8. Current of the terminal-z follows the difference of the currents of terminal-p and terminal-n. Hence, we name terminal-z as current output. The current of the terminal-z can be expressed as follows:

$$\mathbf{i_z = I_{B1} + i_p - (I_{B1} + i_n) = i_p - i_n} \qquad (\mathbf{4})$$

Assuming that each group of transistors, (M_1–M_4), (M_5–M_6) and (M_7–M_8) is matched and all transistors operate in the saturation region, the circuit operates as follows: The current source, I_{B1} forces equal currents of 56 µA in the transistors (M_1–M_4). Thus, the gate to source voltages of these transistors will be equal, which forces the voltages of the two input terminals to be zero. Since terminal-z is defined as the current output, it should ideally have infinite impedance. Following Figure 3.5 displays the DC current transfer characteristic of the CDBA [21]. It can be seen that this CDBA has a high linearity over the entire dynamic range (I_{B1} = 56 µA) and also has very low offset current on terminal-z, which is 0.05 µA.

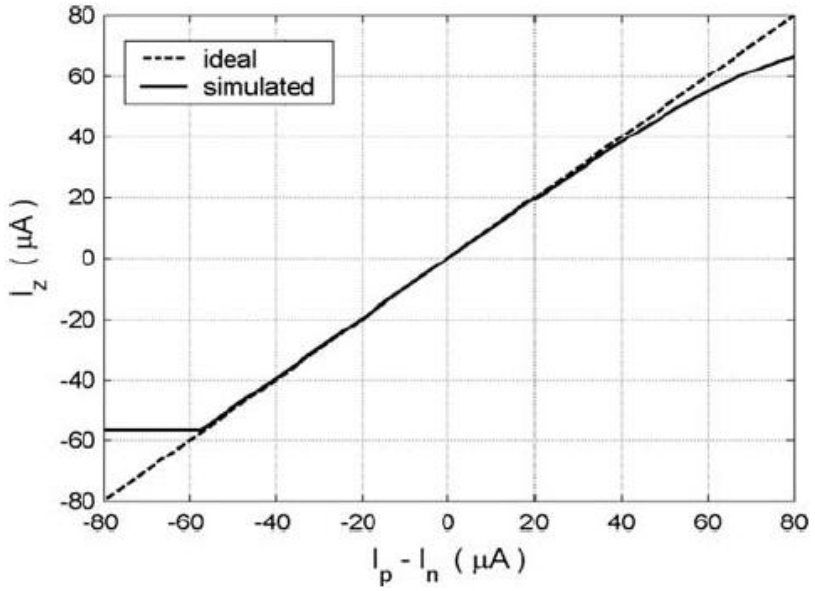

Figure 3.5 the DC current transfer characteristic of the CDBA [21]

The output stage of the proposed CDBA is based on the differential flipped voltage follower (DFVF), which is shown in Fig 3.6. The impedance at node Y is very low and its voltage remains approximately constant for large currents through transistor M_3. If we consider quiescent conditions when $V_1 = V_3$, and assuming the same transistor sizes for M_1 and M_3, the condition is satisfied. A differential voltage V_1–V_3 generates current variations in M_3 that follow the MOS square law. Another important characteristic of the DFVF is that it can also be operated with very low supply voltage. The minimum supply voltage is found as

$$\mathbf{V_{DD}(min) = V_{Tp} + 2V_{DSsat}} \qquad \mathbf{(5)}$$

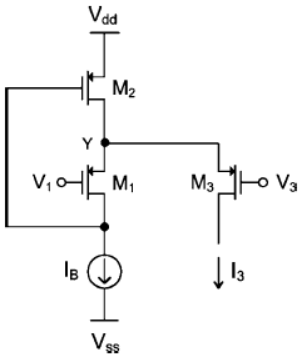

Fig 3.6 Differential flipped voltage follower

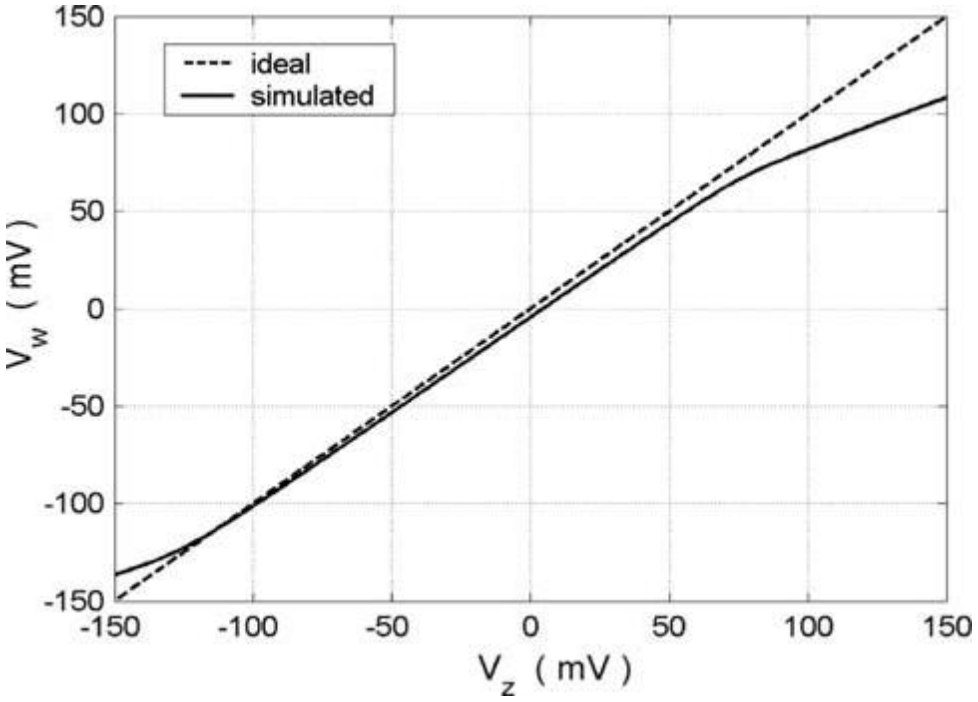

Figure 3.7 the DC voltage transfer characteristic of the CDBA [21]

Figure 3.8 illustrates the AC transfer characteristics of the CDBA. The current and voltage transfer ratios,α_p, α_n and β_v are found to be 0.981, 0.981 and 0.978, respectively. It can be observed that the -3 dB frequencies of $\frac{I_z}{I_p}, \frac{I_z}{I_n}$ *and* $\frac{V_w}{V_z}$ are approximately equal to 25 MHz, 25 MHz and 474 MHz, resp. and Schematic simulation results are summarized in Table 3.2.

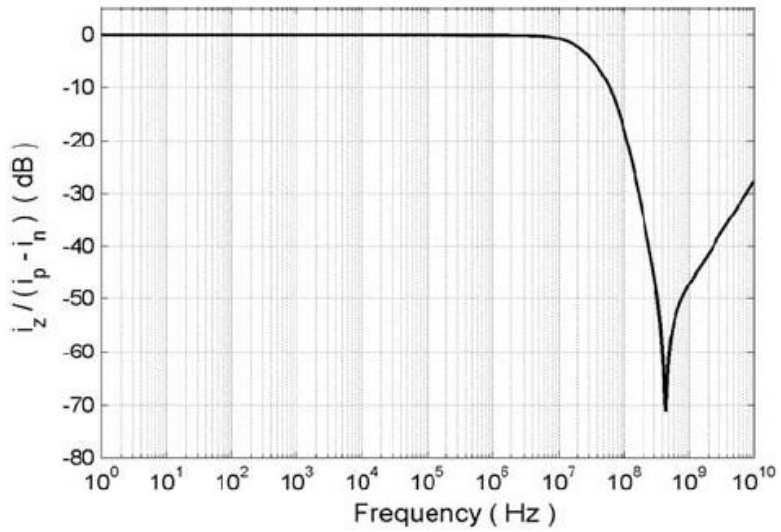

Fig 3.8 AC transfer characteristics of the CDBA-frequency response of the current transfer ratio [21]

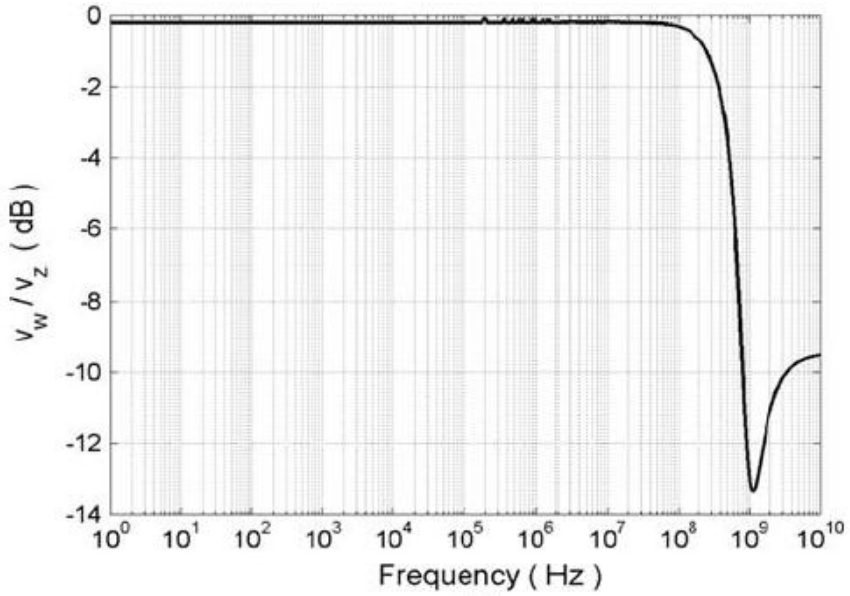

Fig3.9 AC transfer characteristics of the CDBA-Freq. response of the voltage transfer ratio [21]

3.3 Simulation Results for CMOS realization of CDBA

The CMOS CDBA circuit presented in Fig [3.2] is simulated using 0.18 µm, level 7 CMOS process parameters provided by TSMC, DC Characteristics of the CDBA are shown in Fig.3.10 and Fig.3.11

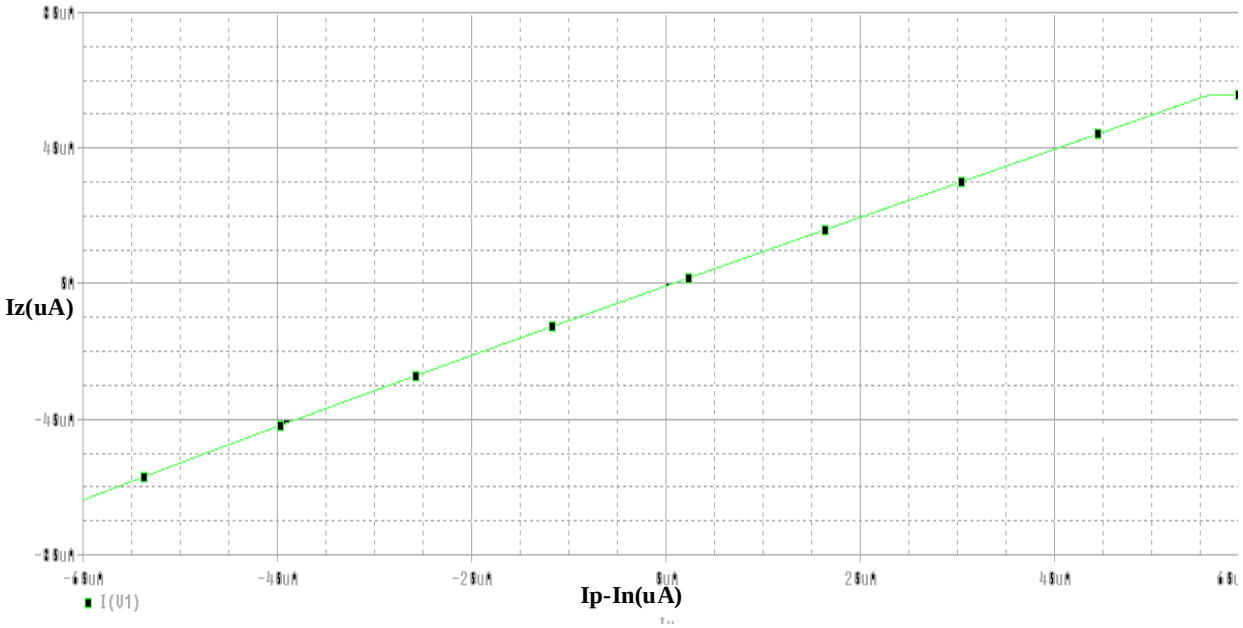

Fig 3.10 PSPICE Simulation for current transfer characteristics

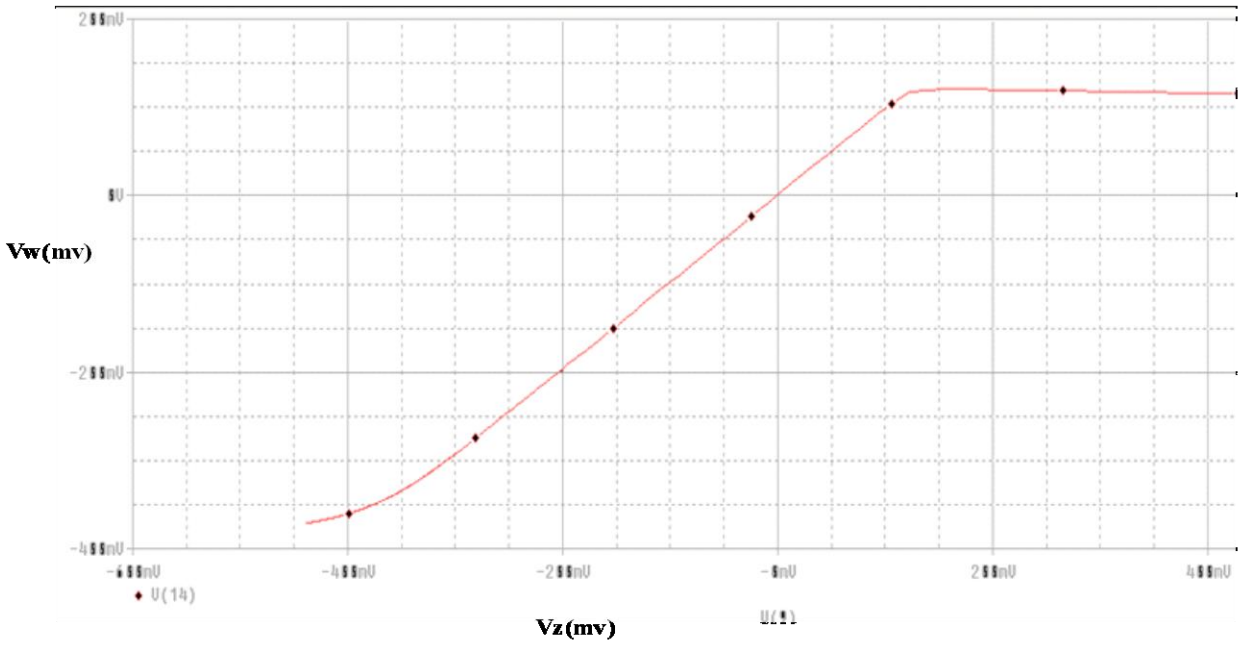

Fig 3.11 PSPICE Simulation for voltage transfer characteristics

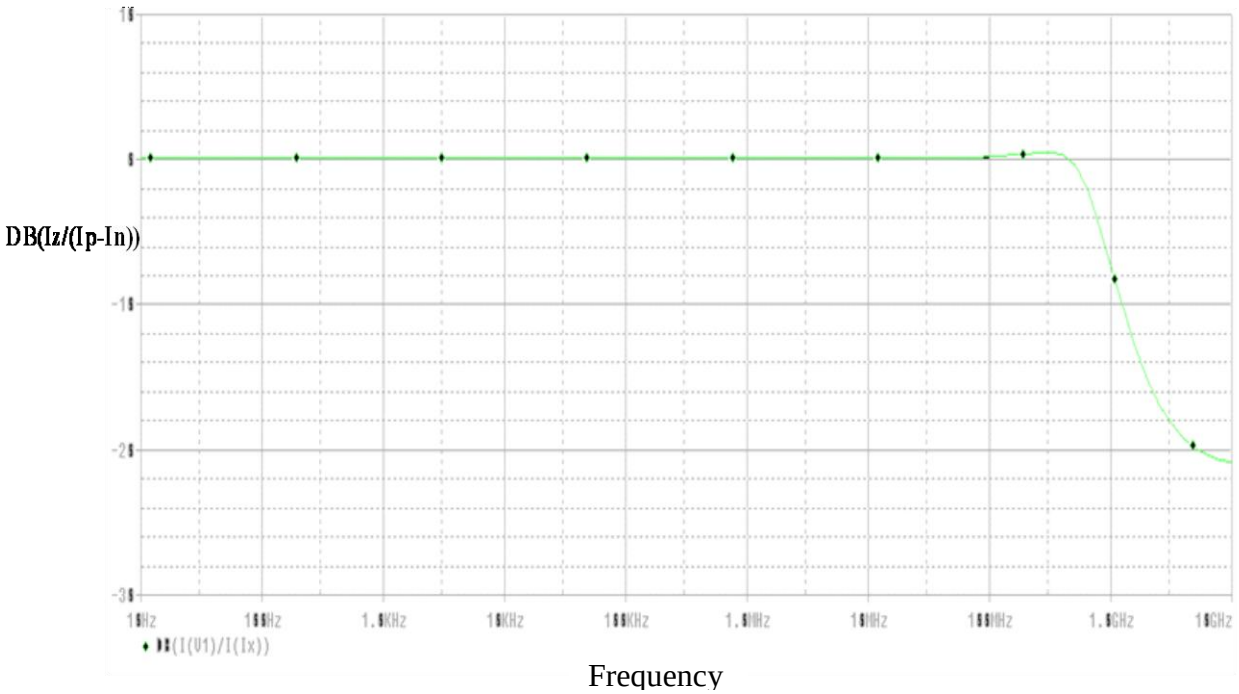

Fig 3.12 PSPICE Simulation for frequency response of the current transfer ratio

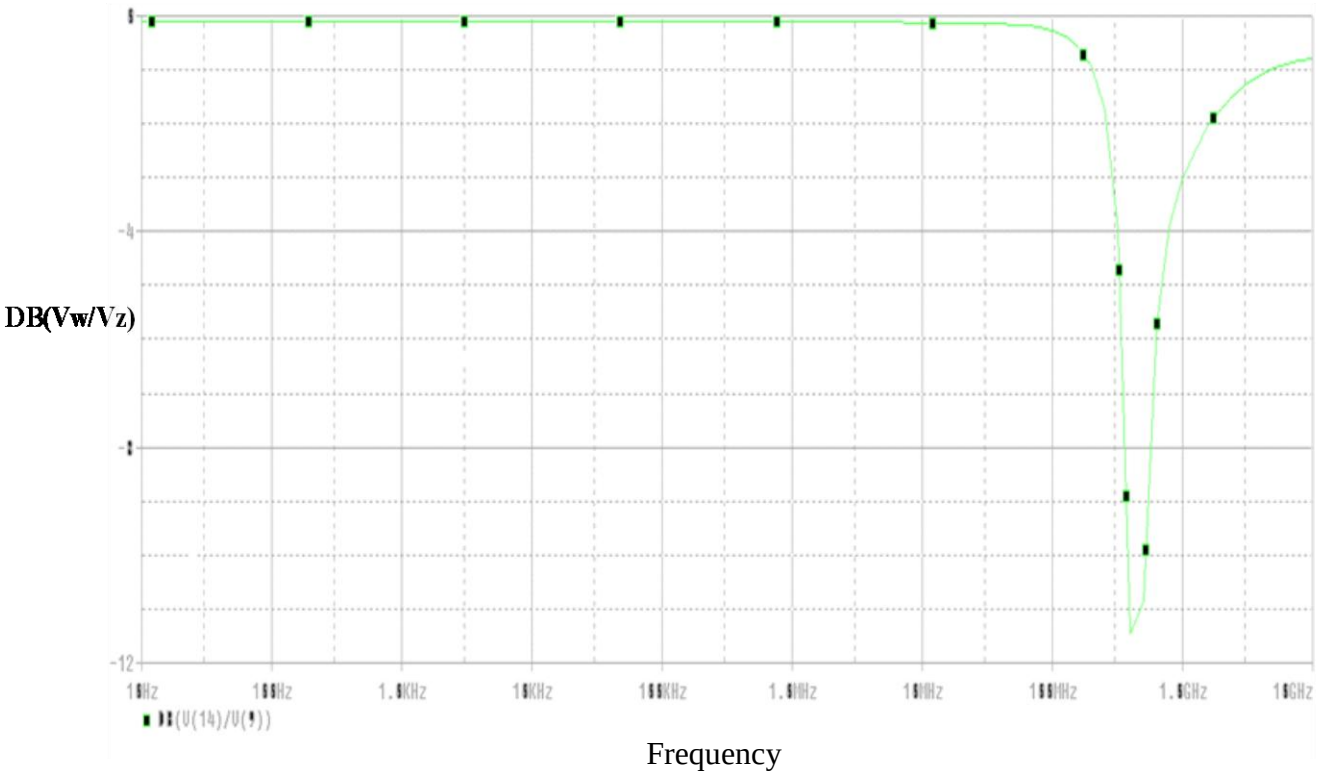

Fig 3.13 PSPICE Simulation for frequency response of the voltage transfer ratio

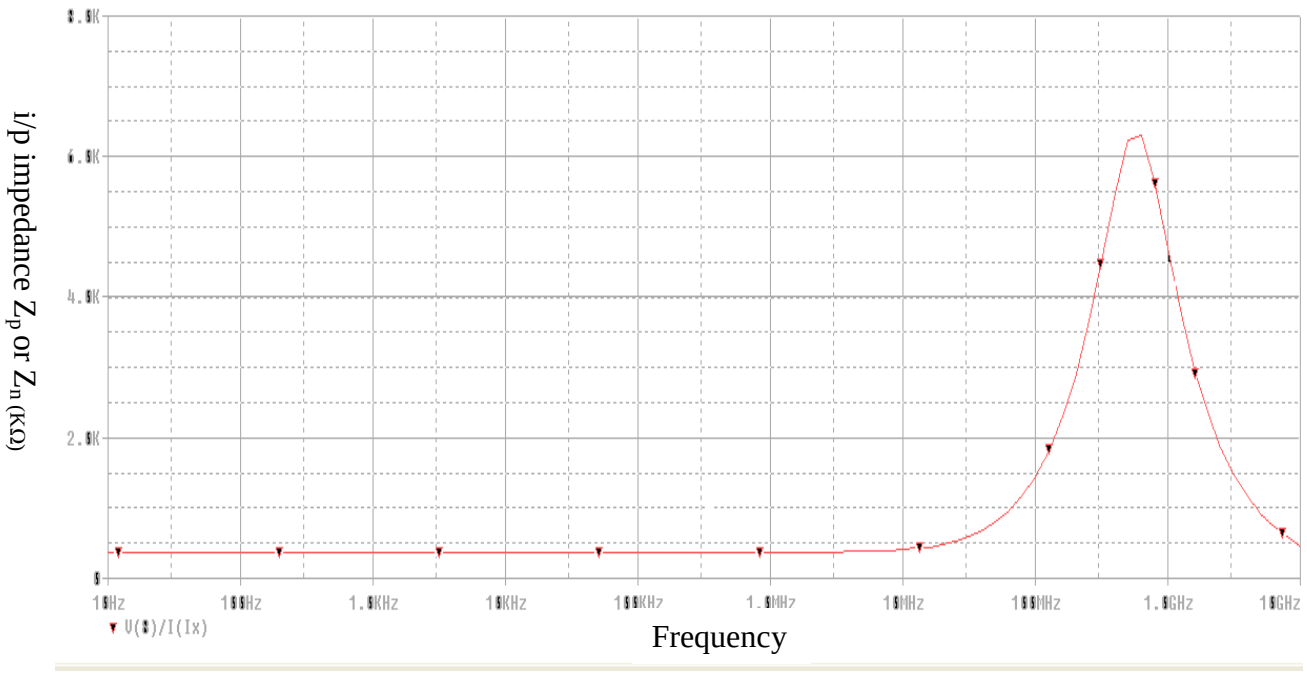

Fig 3.14 PSPICE Simulation for frequency variation of the input impedance magnitudes

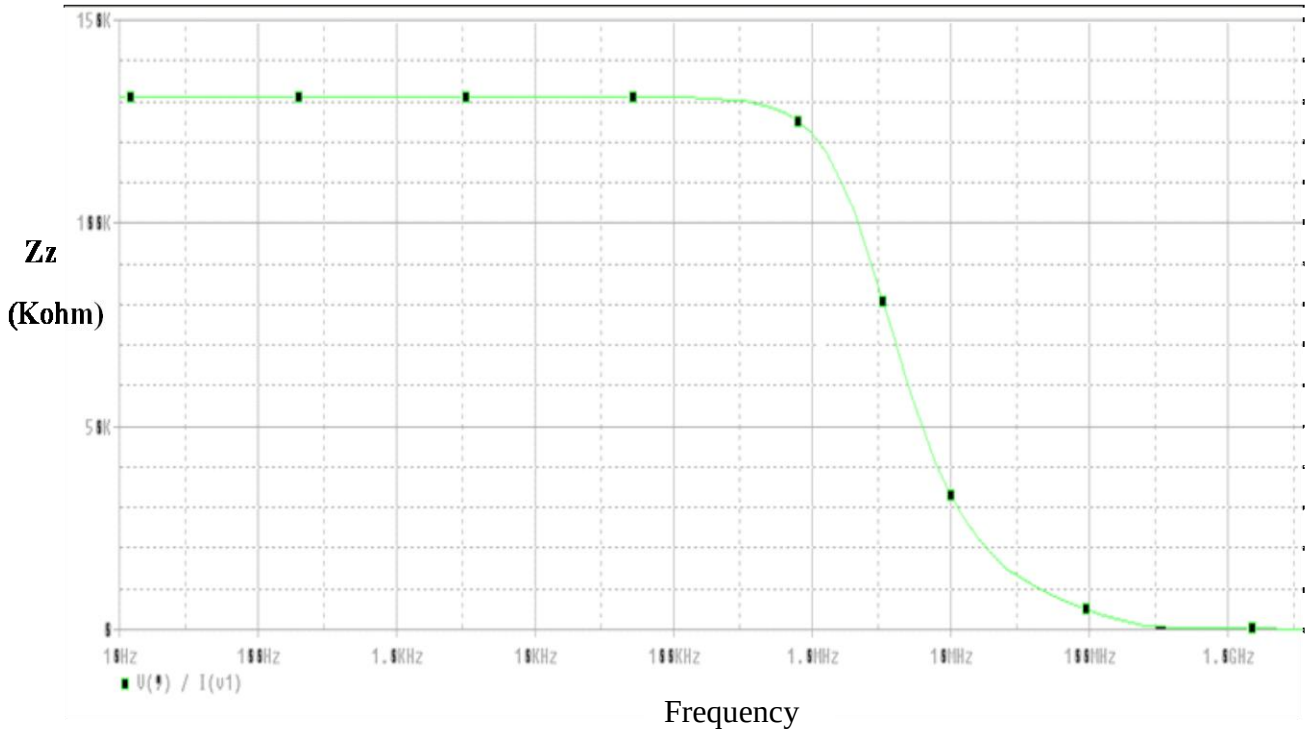

Fig 3.15 PSPICE Simulation for frequency variation of the terminal-z impedance magnitude

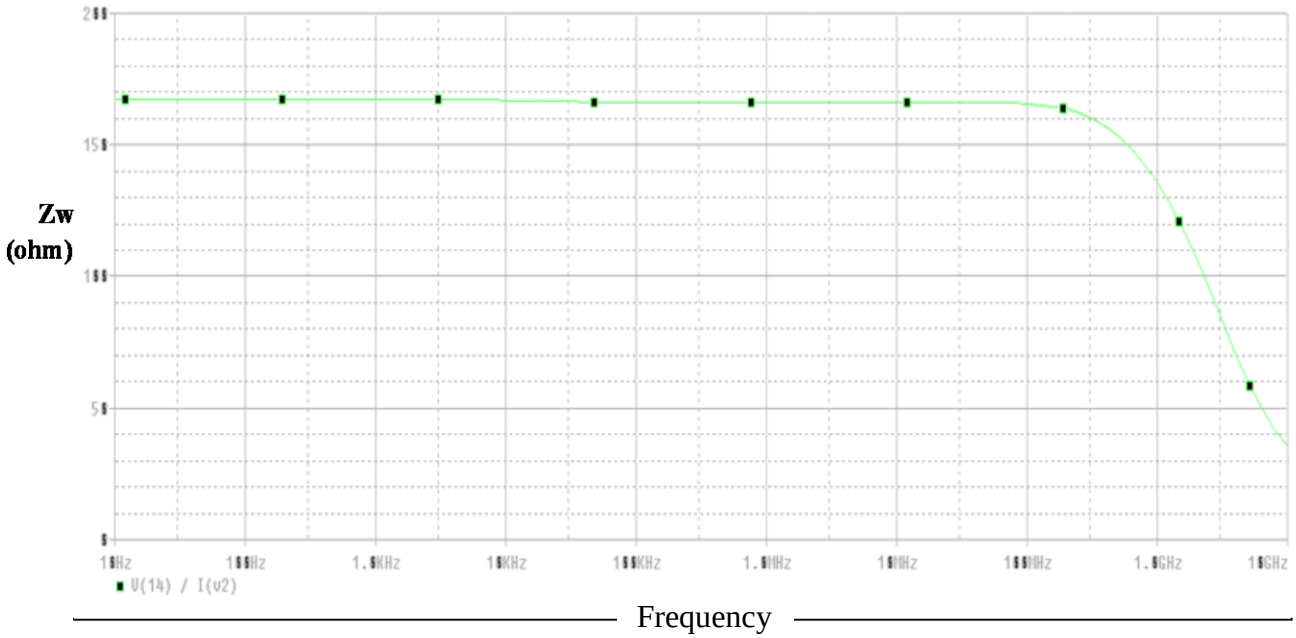

Fig 3.16 PSPICE Simulation for frequency variation of the terminal-w impedance magnitude

Therefore, Figures 3.10-3.16 shows that the simulation results are very close to the results obtained in [21].

The current and voltage transfer ratios, α_p, α_n and β_v are found to be 0.9992, 0.9992 and 0.934, respectively by using 0.18µm, level7 parameters provided by TSMC. It can be observed that the -3 dB frequencies of $\frac{I_z}{I_p}$, $\frac{I_z}{I_n}$ and $\frac{V_w}{V_z}$ are approximately equal to 500 MHz, 500 MHz and 169 MHz, resp. and Schematic simulation results are summarized in Table 3.2

Table 3.2 Performance of the CDBA simulated in PSPICE using parameter TSMC 0.18µm and schematic used in [21]

Parameter	**Property of simulated schematic**	**Property of schematic[21]**
Supply voltage (V)	±0.6	±0.6
Bias voltage,$V_{b1}(V)$	0.45	0.45
Current transfer ratio, $\alpha = {I_Z}/{(I_P - I_n)}$	0.9992	0.981
Current transfer BW (MHz)	500	25
Voltage transfer ratio, $\beta = {V_w}/{V_z}$	0.934	0.978
Voltage transfer BW (MHz)	169	474
Terminal-p resistance (Ω)	360	56.4
Terminal-n resistance (Ω)	360	56.4
Terminal-z resistance (KΩ)	131	157
Terminal-w resistance (Ω)	167	270

CHAPTER 4

CDBA Analog Application

4.1 Introduction

Current-mode active components have two distinct advantages: they give rise to wide bandwidths and high slew rate. On the other hand, many of today's analog signal processing applications require voltage-mode operation. Therefore, it is advantageous to implement current-mode active elements in voltage-mode circuits. In this chapter various applications of the CDBA available in literature such as voltage-mode filters, multiplier and floating inductor have been studied and implemented. The workability of the realized structures are verified through PSPICE simulations.

4.2 Filters

4.2.1 Realization of Voltage mode second order all pass/notch filter.

This configuration is presented in [21] which uses single CDBA, three resistors and two capacitors. The configuration is shown in Fig 4.2.1 and the transfer function is expressed by (6).

$$\frac{V_o}{V_i} = \frac{s^2+s\left(\frac{1}{C_2R_2}-\frac{1}{C_1R_1}\right)+\frac{1}{C_1C_2R_2R_3}}{s^2+s\left(\frac{1}{C_2R_2}+\frac{1}{C_1R_3}\right)+\frac{1}{C_1C_2R_2R_3}} \qquad (6)$$

If condtion given by (7) is satisfied

$$\frac{1}{C_1R_1} = \frac{2}{C_2R_2} + \frac{1}{C_1R_3} \qquad (7)$$

A second-order all pass filter is obtained;

$$\frac{V_o}{V_i} = \frac{s^2-s\left(\frac{1}{C_2R_2}+\frac{1}{C_1R_3}\right)+\frac{1}{C_1C_2R_2R_3}}{s^2+s\left(\frac{1}{C_2R_2}+\frac{1}{C_1R_3}\right)+\frac{1}{C_1C_2R_2R_3}} \qquad (8)$$

The natural frequency, W_o and quality factor, Q for the filter can be expressed as;

$$W_o = \sqrt{\frac{1}{C_1 C_2 R_2 R_3}}, Q = \frac{\sqrt{C_1 C_2 R_2 R_3}}{C_1 R_3 + C_2 R_2} \quad (9)$$

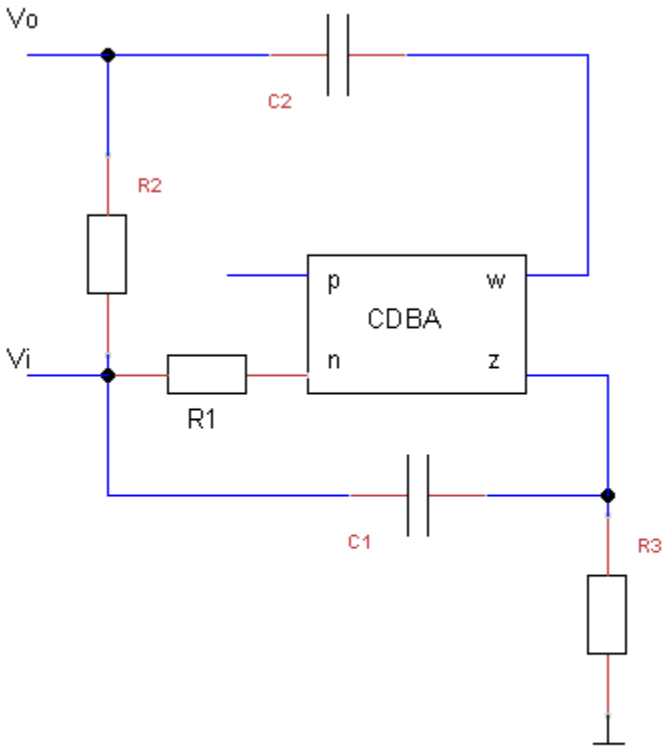

Fig 4.2.1 voltage-mode second-order all pass/notch filter configuration [21]

Figure 4.2.2(a) shows gain response of second order all pass filter. By taking the matching condition into consideration, external component values are chosen as R_1 = 2 KΩ, R_2 = 6 KΩ, R_3 = 6 KΩ, C_1 = 25 pF and C_2 = 25 pF. Then the center frequency of the circuit is measured as f_c = 1.08 MHz, which is in close agreement with the theoretical one. If the matching condition, $C_1R_1 = C_2R_2$ put in (6) a second-order notch filter is obtained;

$$\frac{V_o}{V_i} = \frac{s^2+\frac{1}{C_1C_2R_2R_3}}{s^2+s\left(\frac{1}{C_2R_2}+\frac{1}{C_1R_3}\right)+\frac{1}{C_1C_2R_2R_3}} \qquad (10)$$

Figure 4.2.2(b) shows gain response of second order notch filter.If the component values are chosen as R_1 = 10 KΩ, R_2 = 10 KΩ, R_3 = 2 KΩ, C_1 = 20 pF and C_2 = 20 pF, then the center frequency of the circuit is found as f_c = 1.8 MHz.

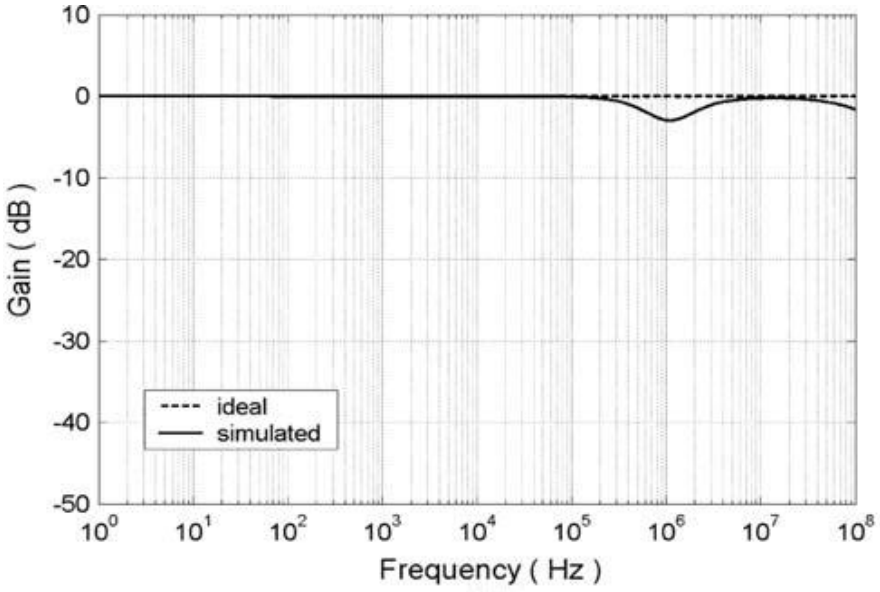

Fig 4.2.2 (a) Gain response of second order all pass filter[21]

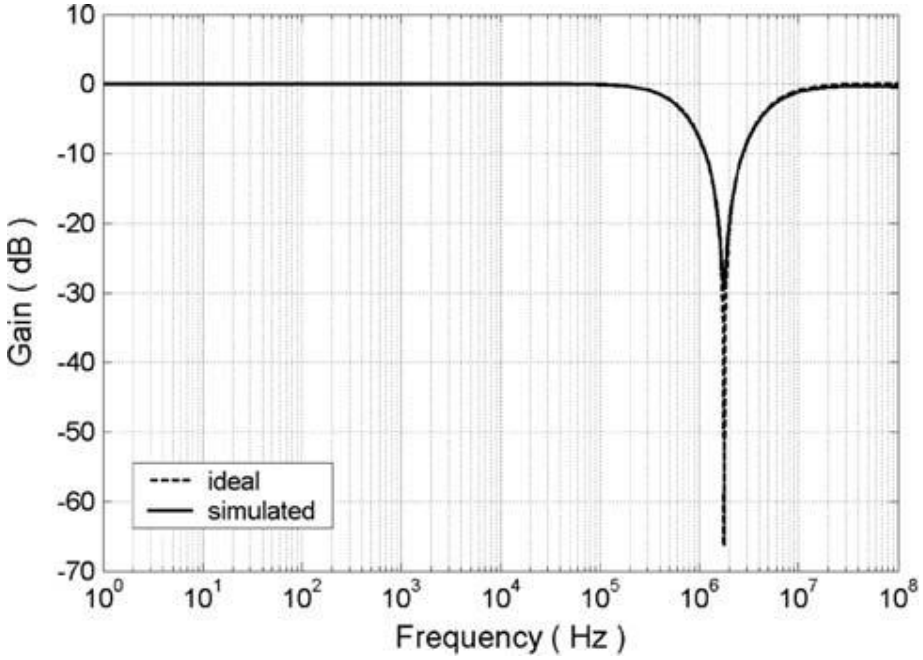

Fig 4.2.2.(b) Gain response of second order notch filter[21]

4.2.2 Simulation Result of all pass and notch filter

Figure 4.2.3 and 4.2.4 shows gain and phase response of second order all pass filter using TSMC 0.18UM parameters in PSPICE. By taking the matching condition into consideration, external component values are chosen as R_1 = 2 KΩ, R_2 = 6 KΩ, R_3 = 6 KΩ, C_1 = 25 pF and C_2 = 25 pF. Then the center frequency of the circuit is measured as f_c = 1.25 MHz, which is in close agreement with the theoretical one.

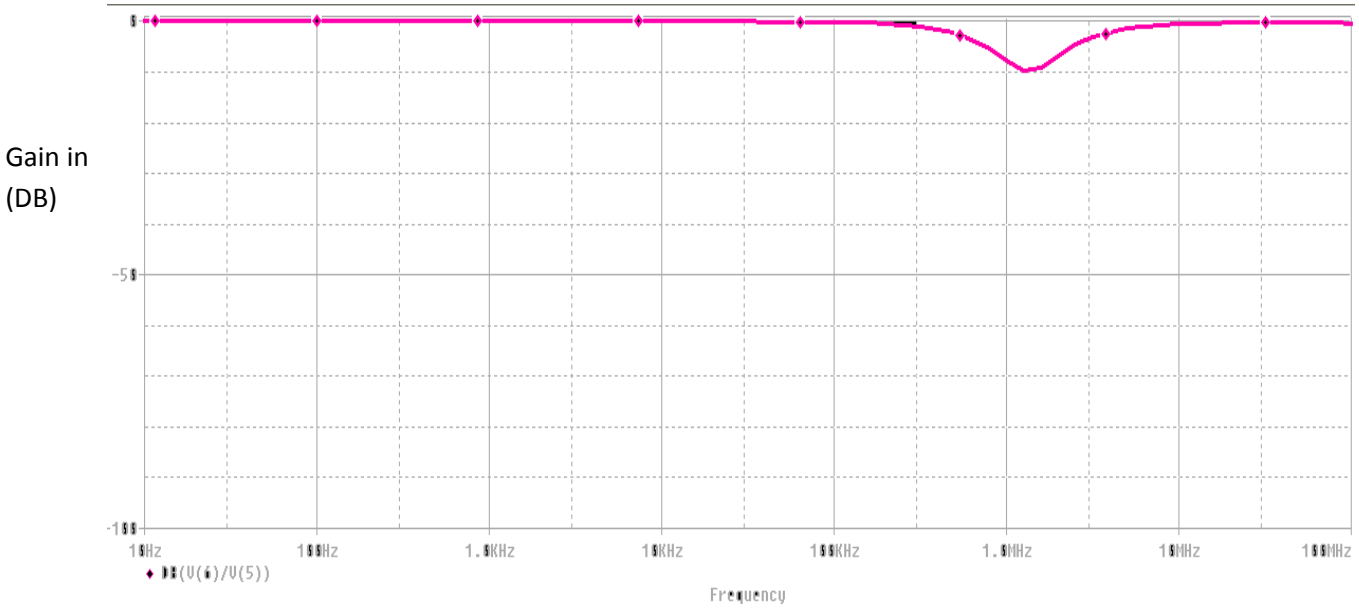

Fig 4.2.3 PSPICE simulation for the Gain response of all pass filter

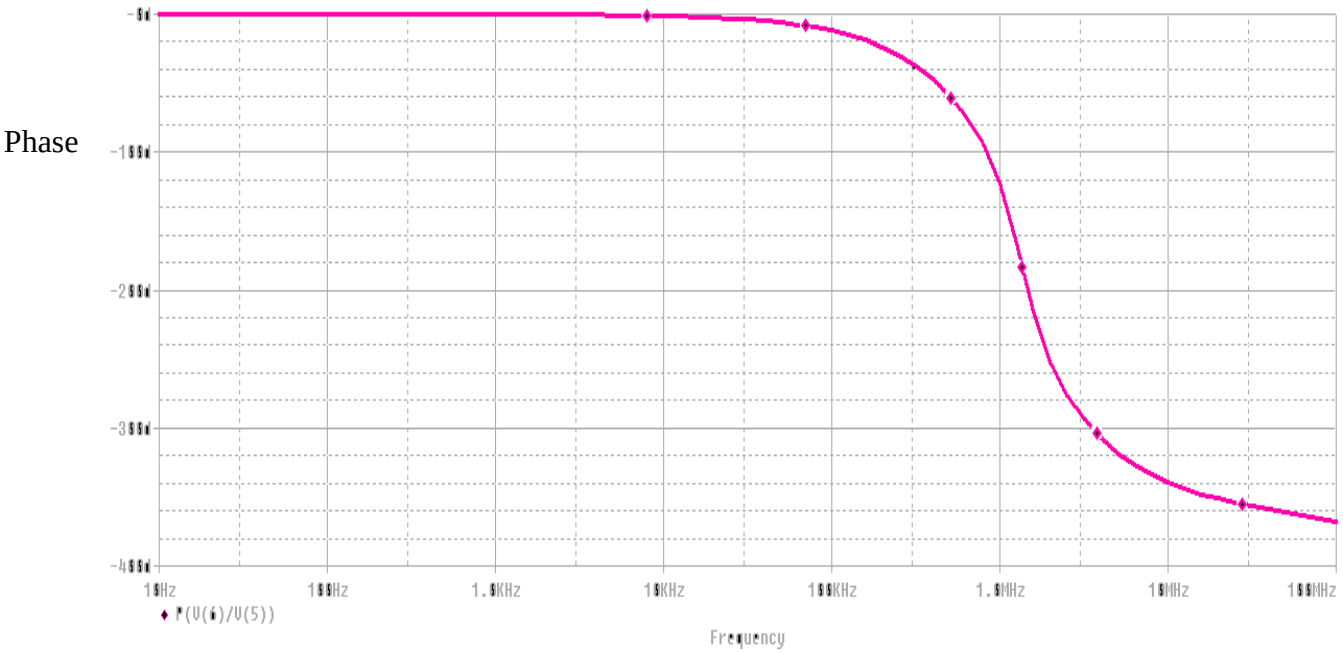

Fig 4.2.4 PSPICE simulation for the phase response of all pass filter

Figure 4.2.5 and 4.2.6 shows gain phase response of second order notch filter respectively.If the component values are chosen as R_1 = 10 KΩ, R_2 = 10 KΩ, R_3 = 2 KΩ, C_1 = 20 pF and C_2 = 20 pF, then the center frequency of the circuit is found as f_c = 1.58 MHz.

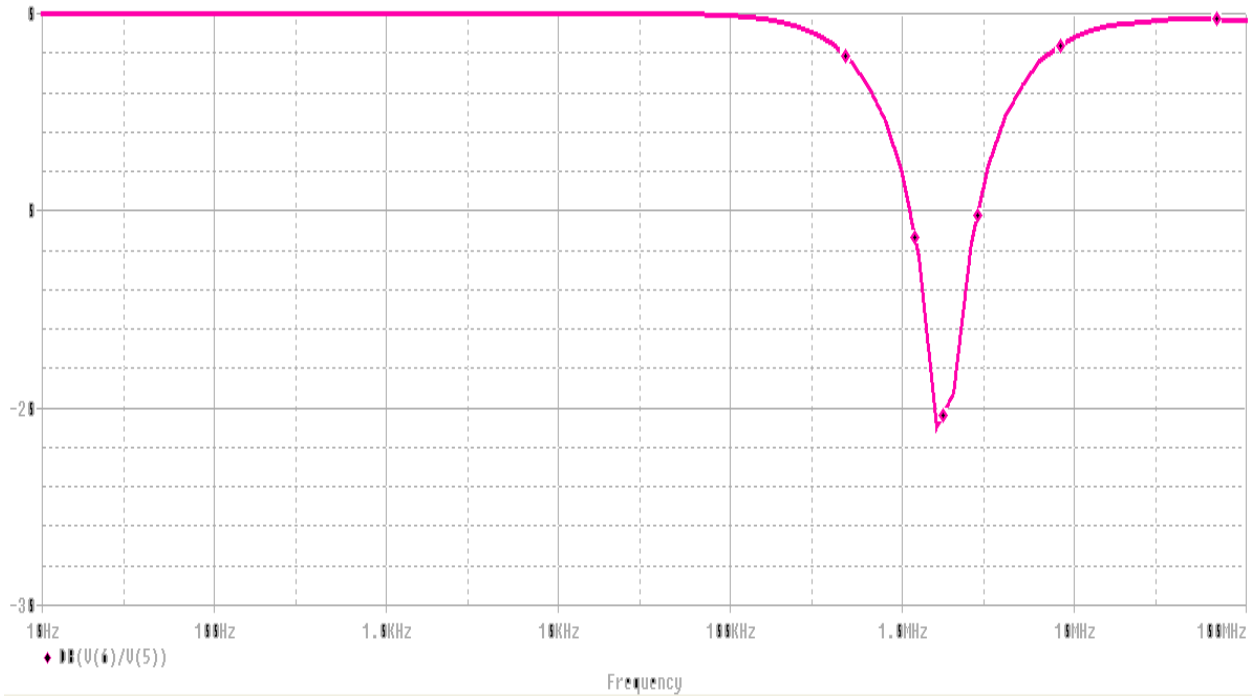

Fig 4.2.5 PSPICE simulation for the Gain response of notch filter

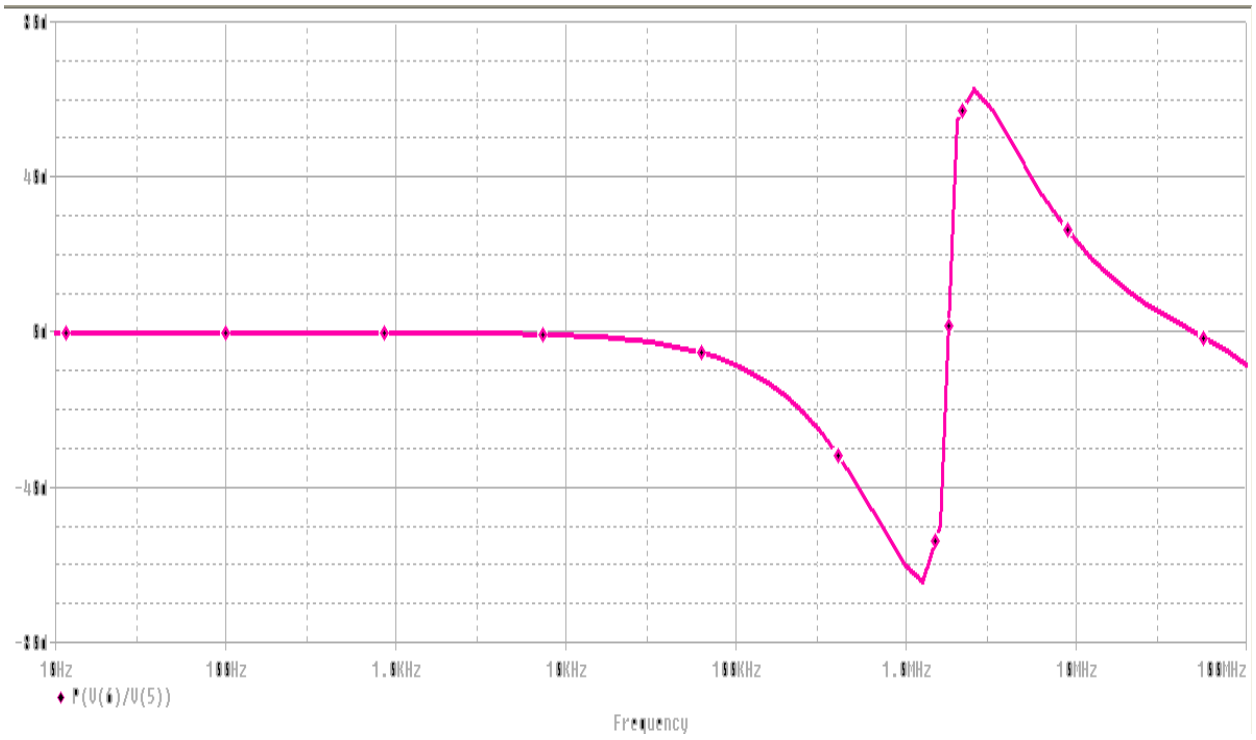

Fig 4.2.6 PSPICE simulation for the Phase response of notch filter

4.3 A Four Quadrant Analog Multiplier Employing Single CDBA

Four quadrant analog multiplier (FQAM) circuits perform real time multiplication of two bipolar Signals V_x and V_y by preserving the correct polarity relationship, produce an output

$$V_o = KV_xV_y \quad (11)$$

K being a scale factor. They find wide applications in communication. In this section the use of CDBA is proposed in the realization of a FQAM with single-ended voltage output. It is shown that the CDBA simplifies the design of such multipliers [27],

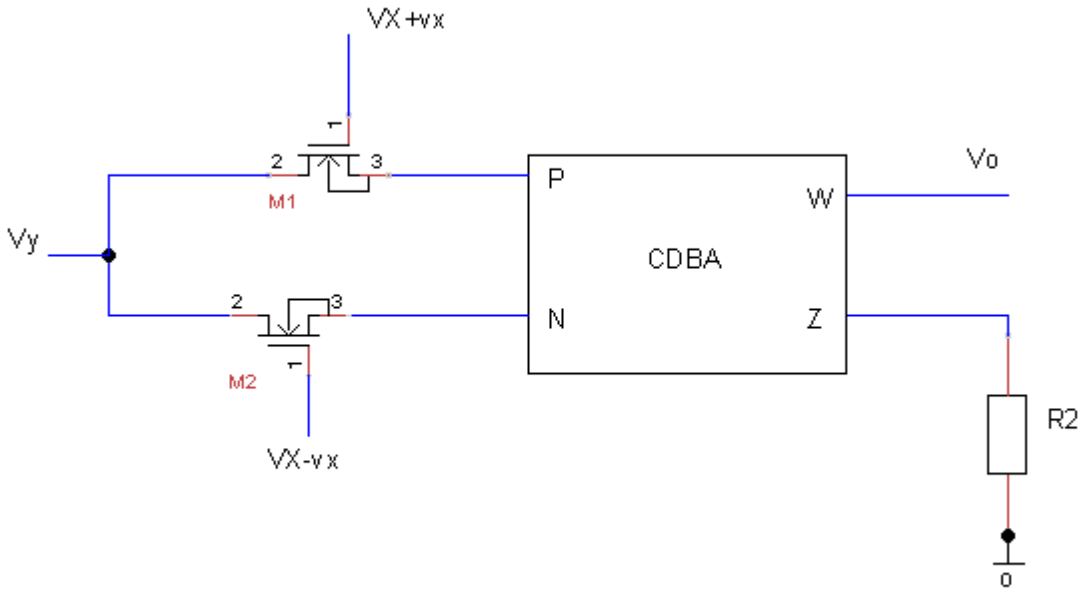

Fig 4.3.1 Multiplier circuit using CDBA

In the configuration shown in Fig.4.3.1, the MOSFETs, M_1, M_2 are working in the linear region. V_x and V_y are time varying voltage signals, while V_X and V_Y are the bias voltages, and CDBA inputs keep the sources of the two MOSFETs, M_1 and M_2, virtually grounded. Here, the output currents are obtained from current equation in linear region [27]

Where,

$$V_{GS} = V_X + V_x \; and \; V_{DS} = V_y, \quad (12)$$

$$KM_1 = KM_2 = K, \quad (13)$$

$$I_p = K\left(V_X + V_x - V_T - {}^{V_Y}/_{2}\right)V_y \qquad (14)$$

$$I_n = K\left(V_X - V_x - V_T - {}^{V_Y}/_{2}\right)V_y \qquad (15)$$

The difference of these currents provides

$$I_Z = I_p - I_n = 2KV_xV_y \qquad (16)$$

If we apply external resistance, then there will be an output voltage V_Z which represents the multiplication of two input voltages. A 1.2V (peak to peak), 10 kHz voltage signal V_y, is multiplied by 1 kHz, V_x of the same amplitude. Fig4.3.2 shows resulting multiplication (Modulation) signal at the output [27].

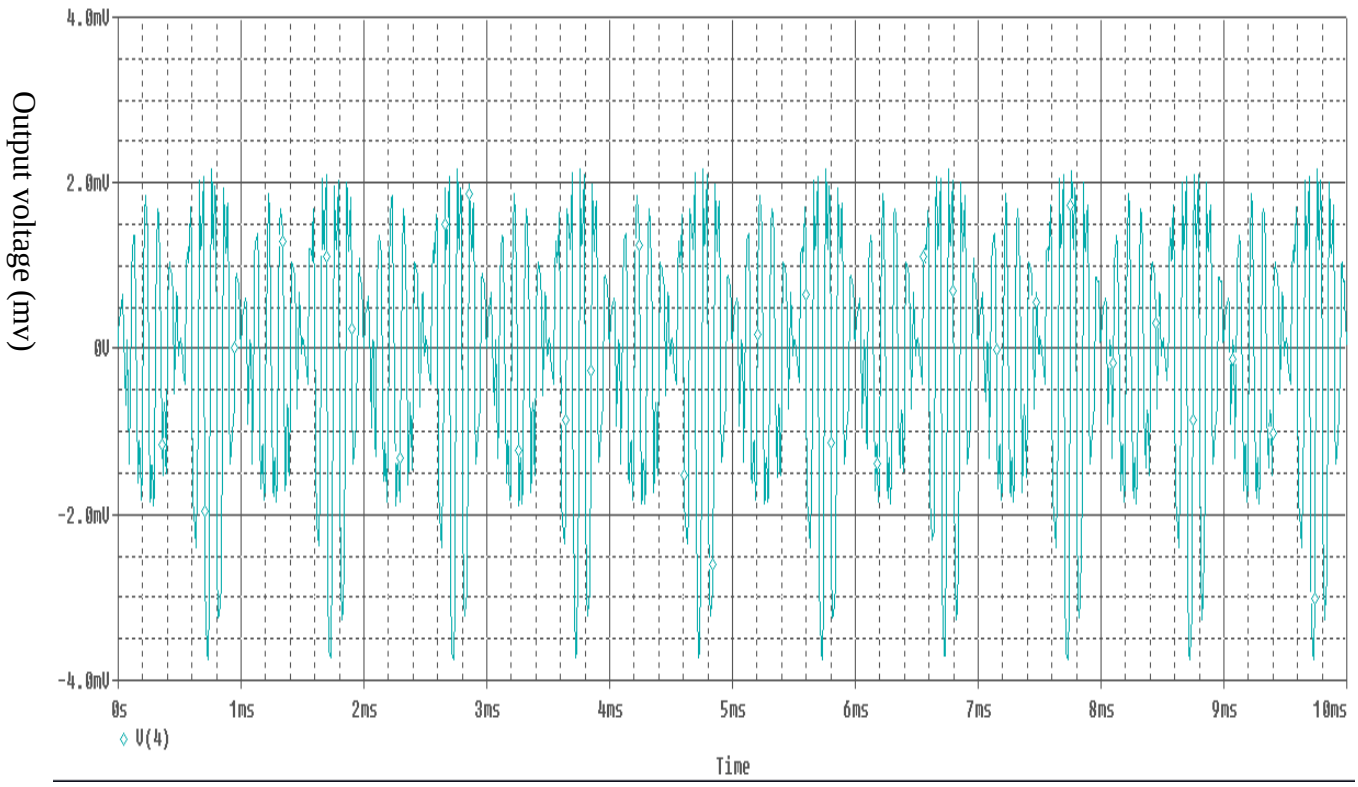

Fig 4.3.2 Multiplier output of circuit in Fig 4.3.1

4.4 Floating inductor

In literature various components are realized using CDBA as the active element. In this chapter a synthetic floating inductance [24] circuit is studied and a filter is realized based on it. CDBA based tunable floating inductor (FI) configuration. Here, $CDBA_1$ and $CDBA_2$ along with MRC_1 and MRC_2 constitute a gyrator circuit [25]. Therefore, a floating inductor can be synthesized easily by cascading two identical gyrators and placing a grounded capacitor C at their connection terminal. This will yield a FI whose inductance can be tuned electronically by adjusting the gate voltages of the respective MOSFETs in MRCs.

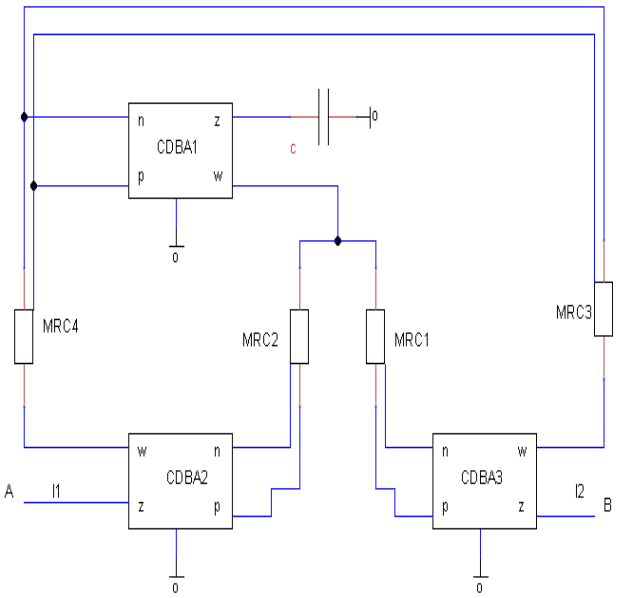

Fig 4.4.1 Tunable, floating inductor using three CDBAs

In the MOS resistive circuit (MRC) shown in Fig.4.4.2, both the even and odd nonlinearities are cancelled by subtraction of the drain-source currents of transistors operating in their triode region. Because the transistors have equaled drain and source voltage.

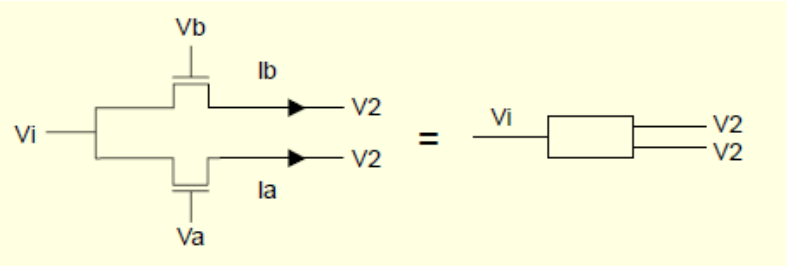

Fig 4.4.2 MOSFET resistive circuit (MRC) nonlinearity cancellation

4.4.1 Series resonance using floating inductor

To verify the functionality of the FI a series resonance circuit as shown in Fig. 4.4.3 is designed and simulated. The simulation results are shown in Fig. 4.4.4 for component values R_S= 20Ω C_S=1nF and L_{eq}=0.45H.The simulated resonance frequency is calculated as 7 KHz that is in good agreement with theory.

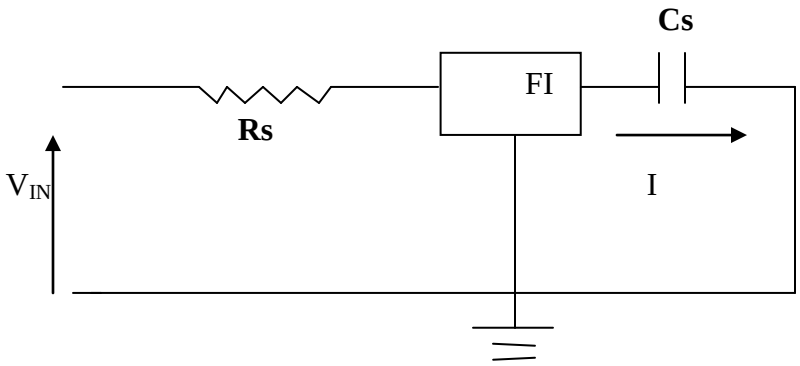

Fig 4.4.3 Series resonance circuit using CDBA-based floating inductance

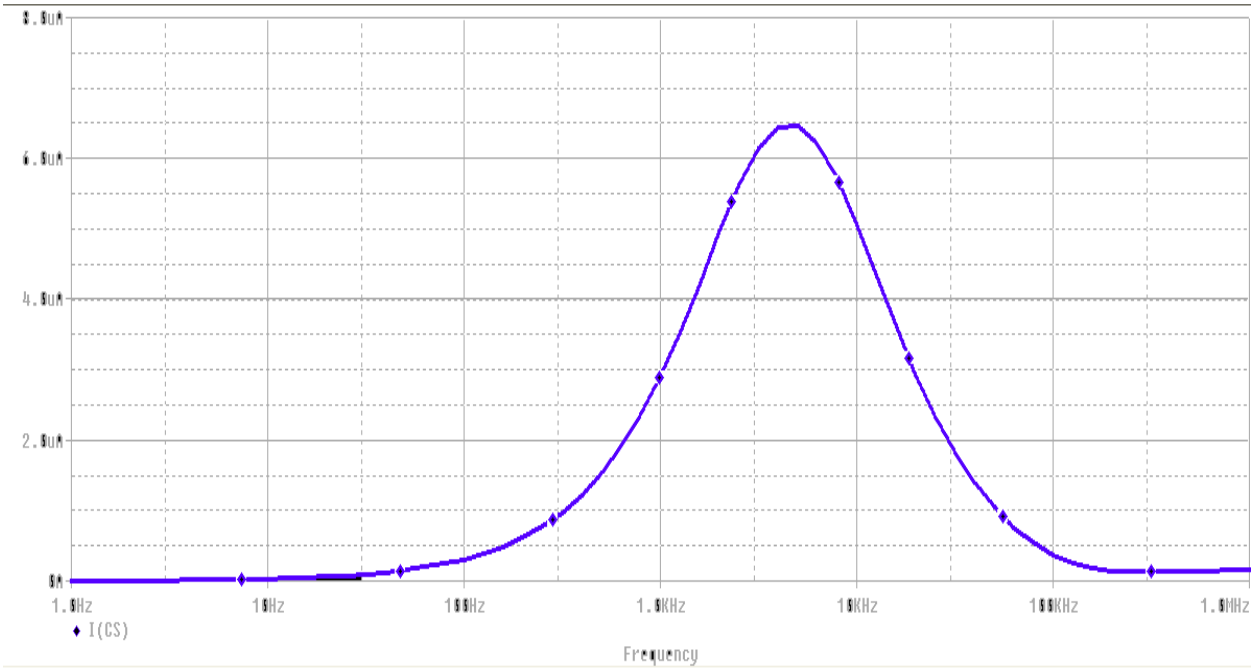

Fig 4.4.4 PSPICE simulation for the response of series resonance circuit

CHAPTER 5

Proposed work

5.1 Realization of Single CDBA based Filter

In this thesis, a new CDBA based CM multi output filter has been proposed. The circuit employs a single CDBA, two resistors and two capacitors. The circuit is capable of implementing simultaneously three basic filtering functions LP, BP and HP without any change of circuit topology. The transfer function are explained in the equation 7(a) and 7(b).

$$\frac{I_{LP}}{I_{IN}} = \frac{1}{R_2C_2\left(s+\frac{1}{R_1C_2}\right)} \qquad (7(a))$$

$$\frac{I_{HP}}{I_{IN}} = \frac{C_1S}{C_2\left(s+\frac{1}{R_1C_2}\right)} \qquad (7(b))$$

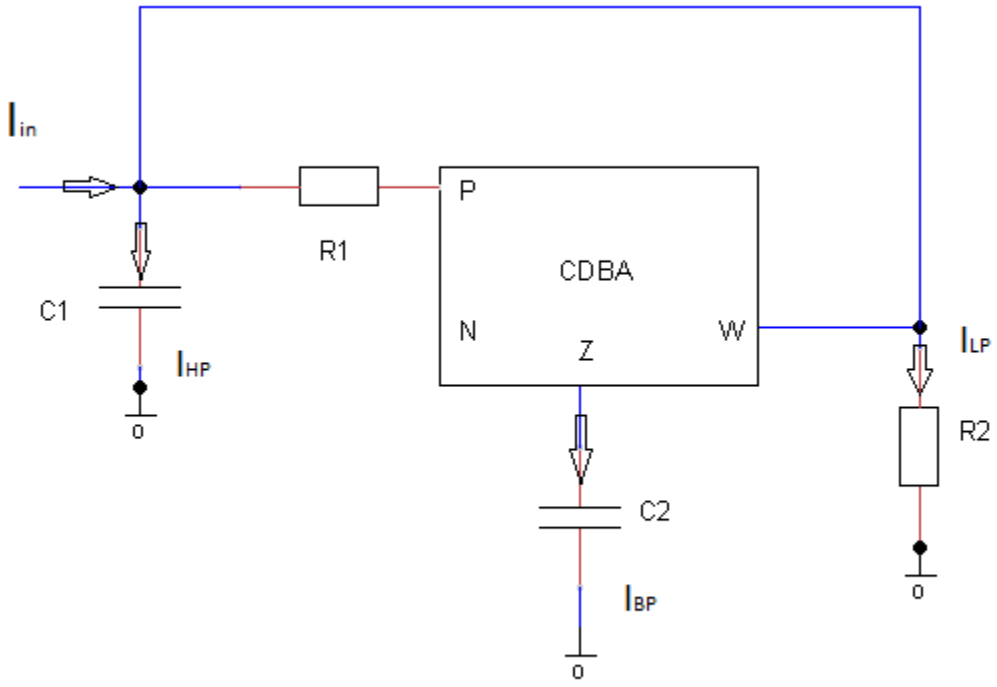

Fig 5.1.1 Proposed CM multi output filter

5.1.1 Simulation Results

The proposed circuit has been simulated using a PSPICE simulation program. Fig 5.1.2 shows the simulated results of the basic responses obtained with $C_1=C_2=1nF$, $R_1=R_2=1K\Omega$. The cut off frequency for LP is 129 KHz, for HP is 200 KHz and center frequency for BP is 160KHz.

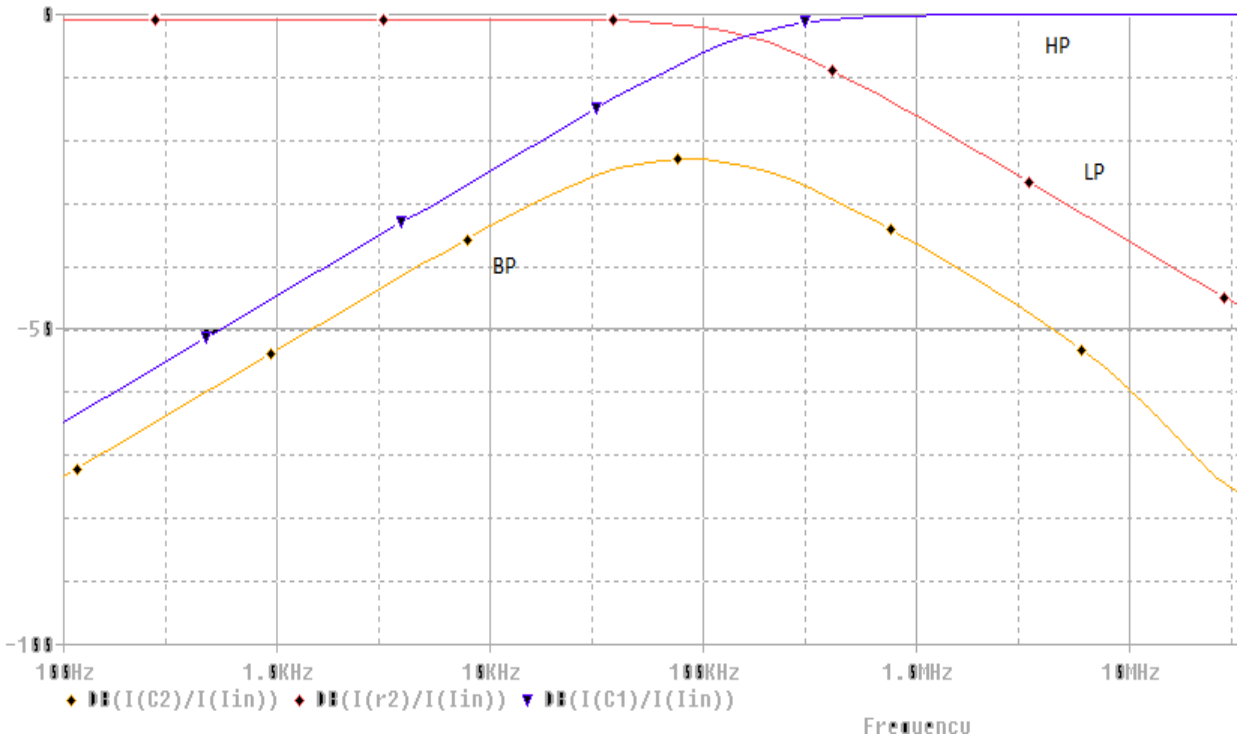

Fig 5.1.2 Magnitude responses of LP, HP and BP filter

5.2 Realization of Monostable multivibrator using single CDBA.

A monostable multivibrator (MMV) has one stable state and one quasi-stable state. The circuit remains in its stable state till an external triggering pulse causes a transition to the quasi-stable state. The circuit comes back to its stable state after a time period T. Thus it generates a single output pulse in response to an input pulse and is referred to as a one shot or single shot. An external trigger signal generated due to charging and discharging of the capacitor produces the transition to the original stable state. So, monostable multivibrator is one which generates a single pulse of specified duration in response to each external trigger signal. The circuit for the monostable multivibrator is shown in Figure 5.2.1. It uses a single CDBA block, two resistors, a single diode and a capacitor. The resistor R_1 forms a positive feedback loop. The load resistance R_2 connected to the z terminal is large enough to drive the device output V_o into saturation level V^+_{sat}. This results in charging of the capacitor present in the feedback loop. When the voltage across the capacitor reaches a value at which the current through R_2 is not large enough to maintain the output voltage at V^+_{sat} the output switches to zero and the capacitor does not charge in the opposite direction due to diode as shown in Figure 5.2.2

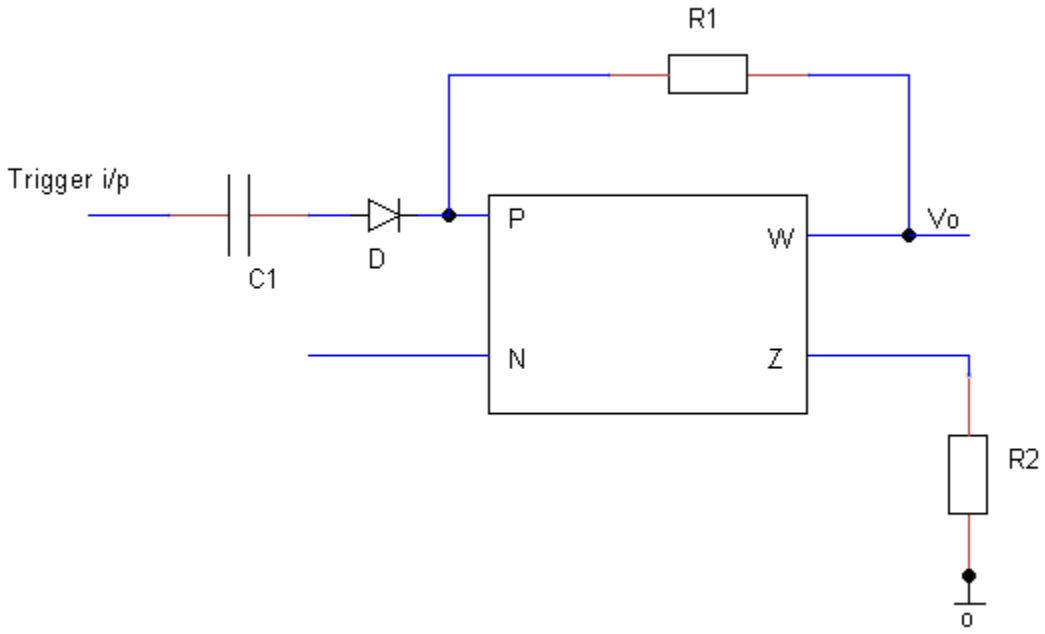

Fig.5.2.1 Monostable multivibrator circuit

5.2.1 Simulation result of monostable multivibrator

Simulations were carried out to investigate the output of that circuit configuration of Figure 5.2.1 can offer before the output signal gets distorted. Supply voltage of ±0.6 V was used for simulations. Figure 5.2.2 shows the trigger input and the output waveform of the proposed circuit. The simulated output obtained with component values as 1 KΩ, 1 KΩ and 10 µF. From the simulated output in Figure 5.2.2 T_{on} time is observed as 40µs.

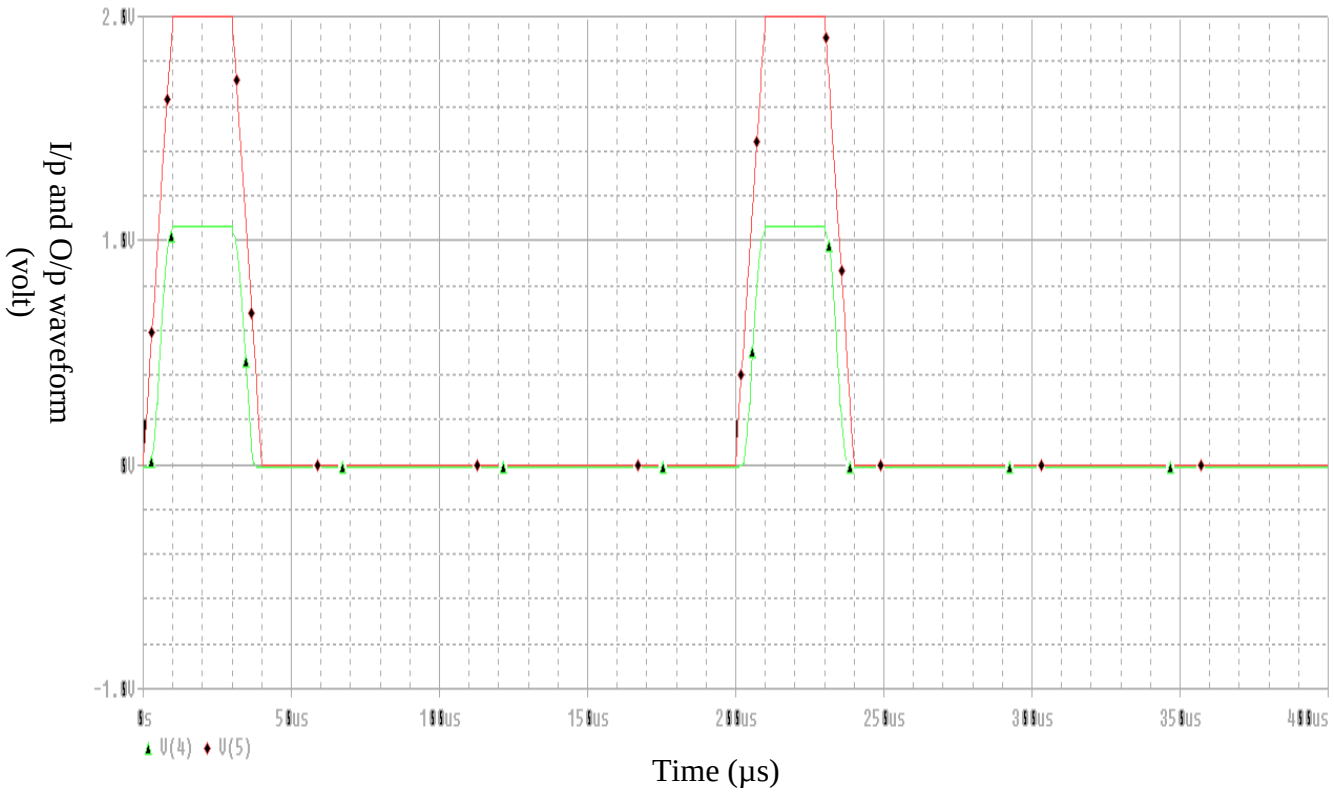

Figure 5.2.2 PSPICE simulation of input and output waveform in monostable multivibrator

5.3 Grounded inductor

A topology of lossless grounded inductor has been proposed using CDBA. Two applications using the proposed inductors are also included. PSPICE simulation has been included to demonstrate the performance and verify the theoretical analysis.

The proposed lossless grounded inductor topology is shown in Figure 5.3.1. Routine analysis of the circuit of Figure 6.2.1 for inductor topology, input admittance is given by [30]

$$Y_{in}(s) = \left(G_1 + G_2 + G_4 - \frac{G_2 G_4}{G_3}\right) + \frac{C_1 G_3}{s G_1 G_2 G_5} \qquad (18)$$

This input admittance will be purely inductive provided that

$$G_1 + G_2 + G_4 = \frac{G_2 G_4}{G_3} \qquad (19)$$

The equivalent inductance value is given by

$$L_{eq} = \frac{C_1 G_3}{G_1 G_2 G_5} \qquad (20)$$

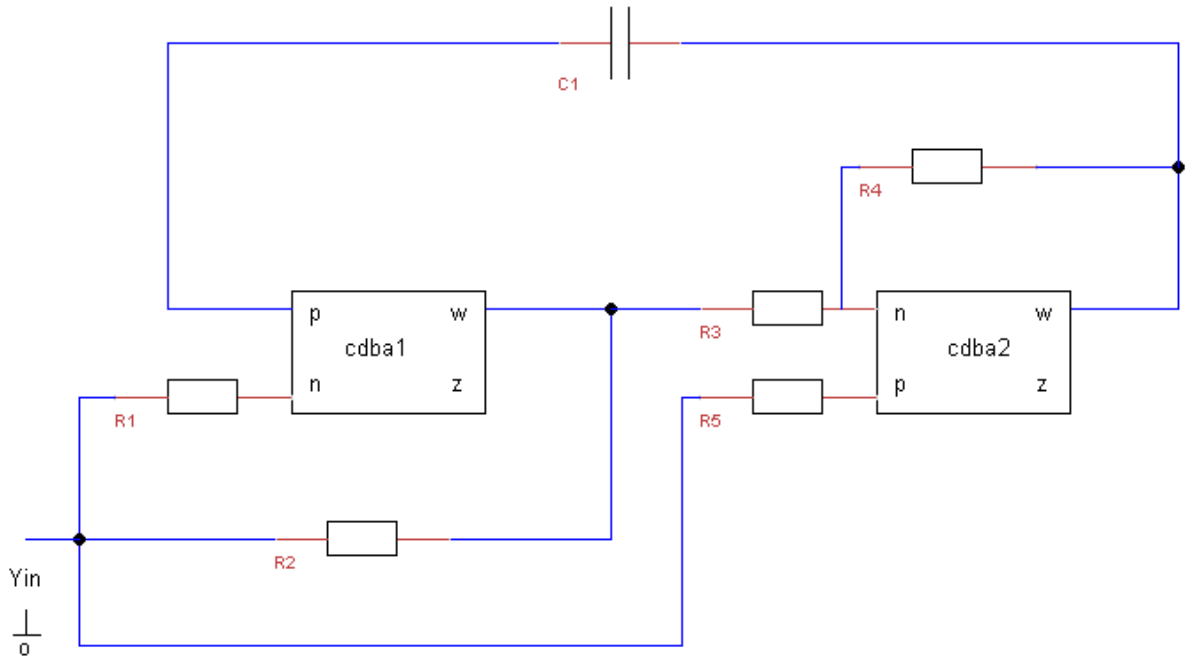

Figure 5.3.1 Inductor simulation topology

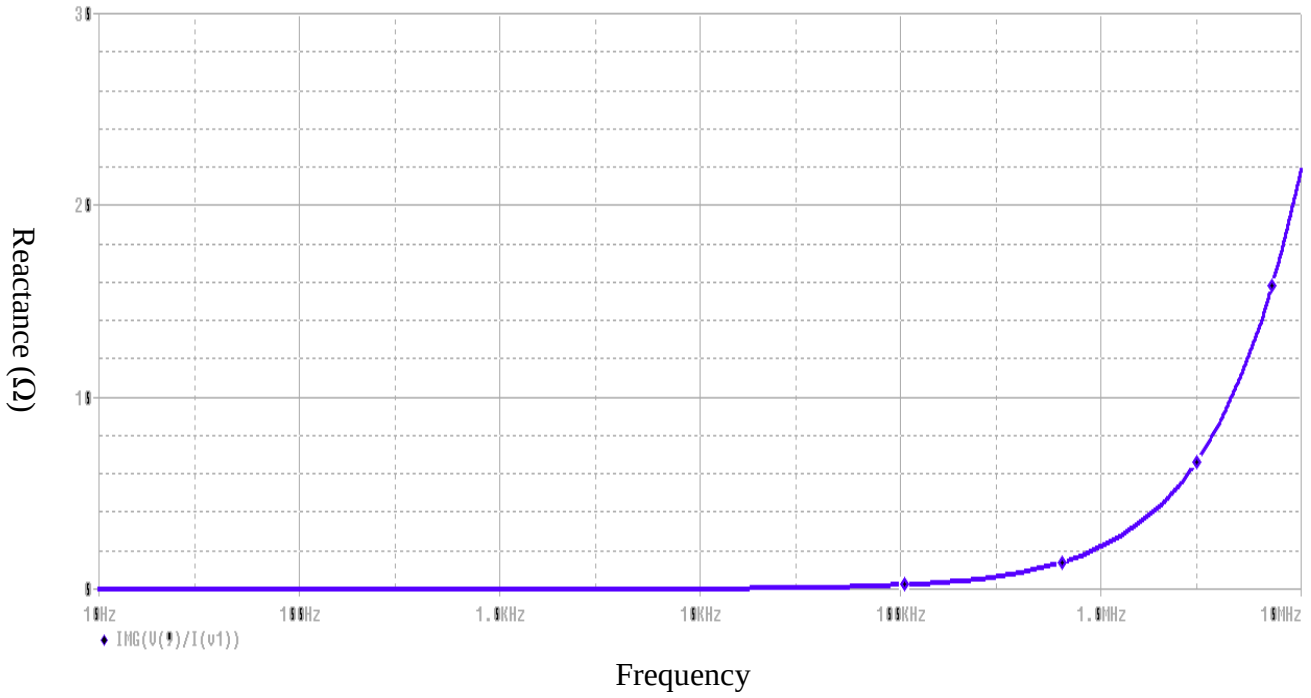

Figure 5.3.2 Impedance versus frequency response of topology of Figure 5.3.1

Similarly, Figure 5.3.2 shows the frequency response of the impedance of the inductor of value $L_{eq} = 10\mu H$ as obtained with component values of $R_1=R_2=R_4=R_5=1K\Omega$, $R_3=3K\Omega$, and $C_1=30pF$ for inductor topology given in Figure 5.3.1. In the inset, the variation of impedance in lower frequency range is shown.

5.3.1Application of Grounded inductor

In this section some applications of the proposed topology have been presented. The topology may be used for constructing filter and oscillator circuits [30].

5.3.1.1 High-pass Filter

A high pass filter, as shown in Figure 5.3.3, can be constructed using proposed inductor. The transfer function for high pass response is obtained as

$$\frac{V_O}{V_{in}} = \frac{S^2}{S^2 + \frac{S}{CR} + \frac{1}{L_{eq}C}} \tag{21}$$

Where $w_o = \frac{1}{\sqrt{L_{eq}C}}$ and $Q = R\sqrt{\frac{C}{L_{eq}}}$ (22)

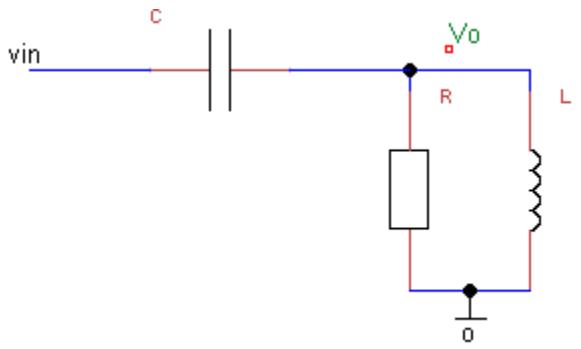

Figure 5.3.3 high pass filter using grounded inductor

Simulation Results

The functionality of the high pass filter is verified using the inductor topology of Figure 5.3.1 and designed for lower cutoff frequency of 503.2 KHz. The component values are obtained as 300 Ω, 1 nF and 0.1 mH. The value of 0.1mH is obtained using inductor topology of Figure5.3.1 with component values of $R_1=R_2=R_4=R_5=1$ KΩ, $R_3=3$ KΩ, and $C_1=300$ pF. The frequency response of the filter simulated using PSPICE is depicted in Figure 5.3.4. Simulated value of lower cutoff frequency is obtained as 505 KHz which is in close agreement to the theoretical value of 503.2 KHz.

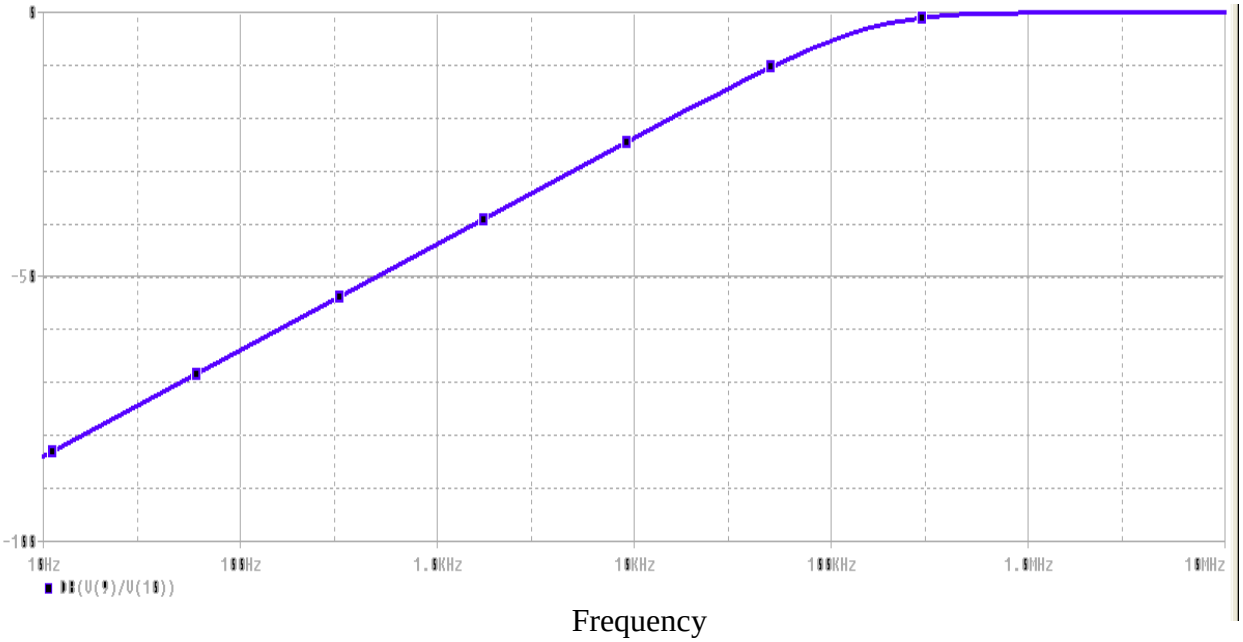

Figure 5.3.4 frequency response of the high pass filter using the inductor topology in fig5.3.1

5.3.1.2 Band-pass Filter

The proposed inductor topologies may also be used to obtain band-pass response using the circuit given in Figure 5.3.1 the transfer function for band-pass response is obtained as

$$\frac{V_o}{V_{in}} = \frac{\frac{s}{CR}}{s^2 + \frac{s}{CR} + \frac{1}{L_{eq}c}} \qquad (23)$$

Where $$w_o = \sqrt{\frac{1}{L_{eqc}}} \qquad (24)$$

And

$$Q = R\sqrt{\frac{c}{L_{eq}}} \qquad (25)$$

The theoretical proposition is verified using the topology of Figure 5.3.1. A band-pass filter is designed having center frequency of 503.3 KHz. The component values are obtained as 1 KΩ, 1 nF and 0.1 mH. The value of 0.1 mH is obtained for inductor topology of Figure 5.3.1 with component values of R_1=R_2=R_4=R_5=1 KΩ, R_3=3 KΩ, and C_1=300 pF. The frequency response of the filter simulated using PSPICE is depicted in Figure 5.3.6. The simulated results are in close agreement with the theoretical prediction.

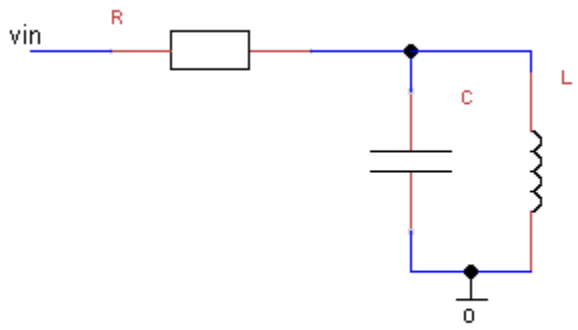

Figure 5.3.5 band pass filter using grounded inductor

Simulation Results

The functionality of the band pass filter is verified using the inductor topology of Figure 5.3.1 and designed for center frequency of 503.3 KHz. The component values are obtained as 300 Ω, 1 nF and 0.1 mH. The value of 0.1 mH is obtained for inductor topology of Figure 5.3.1 with component values of $R_1=R_2=R_4=R_5=1$ KΩ, $R_3=3$ KΩ, and $C_1=300$ pF. The frequency response of the filter simulated using PSPICE is depicted in Figure 5.3.6. The simulated results are in close agreement with the theoretical prediction.

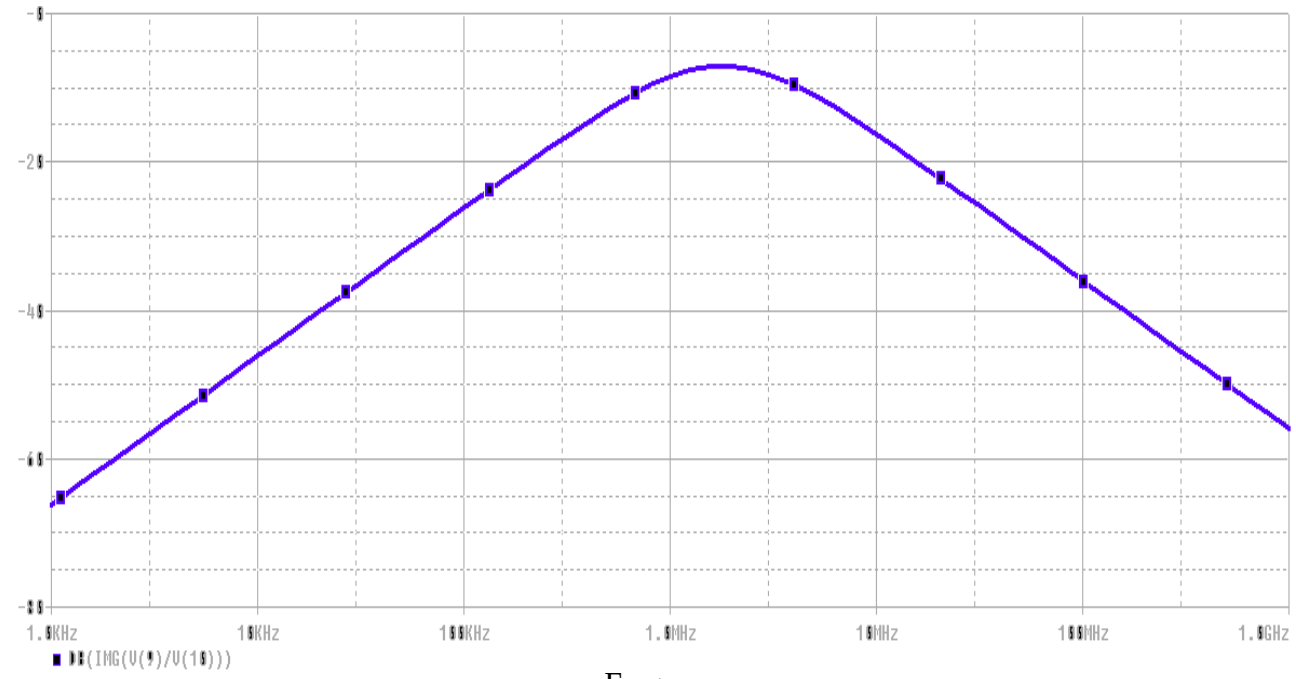

Figure 5.3.6 frequency response of the band pass filter using the inductor topology in fig5.3.1

5.4 PID controller using single CDBA

A detailed overview of the circuit allowing the realization of PID controller with single active CDBA element is proposed. Classical implementations of the PID controller contain several active elements to realize the transfer function. For instance, parallel structure using operational amplifiers (Op Amp) [35] requires five amplifiers: differential input amplifier, P, I, D transfers and adder. Some recent work presents the PID controllers in voltage or current mode with alternative building blocks. For instance [36], [37], [38] show the PID controllers based on CCII current conveyors, OTA or CDTA, respectively. All these circuits allow independent tuning of P, I and D components, however, despite the high circuit complexity and power consumption. These parameters can affect the power efficiency, cost, as well as the competitiveness of the analog control to their discrete-time counterparts.

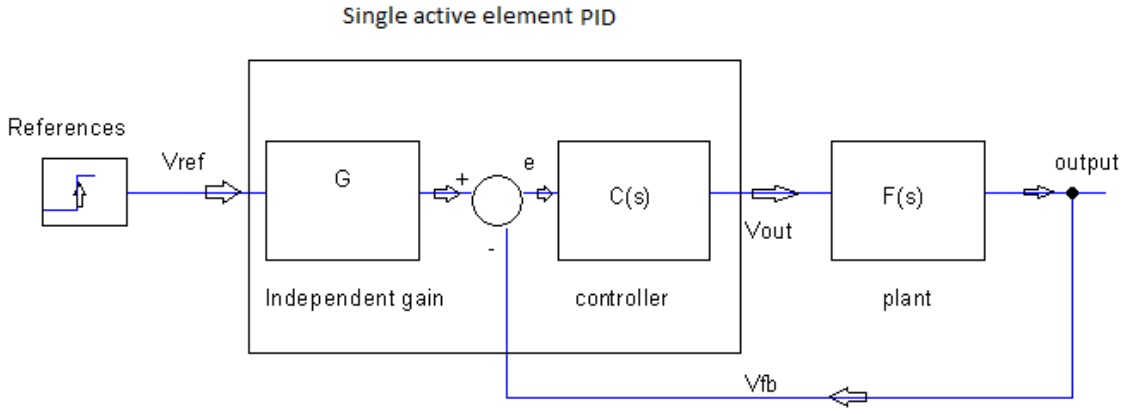

Fig 5.4.1 Structure of SISO closed loop system with single active element PID controller C(s) [32]

Compared to these solutions, utilization of single active element controllers ([35] and [37] for Op Amp and OTA respectively) can offer a very cost-effective solution for many applications, such as the smart portable devices. The controller with single active element is depicted on the block scheme of a SISO system in Fig. 5.4.1.

We notice that the controller realizes following functions:

• Differential block

• Transfer function of PID controller

• Independent gain G to adjust the reference input

• Symmetrical transfers $|V_{OUT}/V_{REF}| = G \cdot |V_{OUT}/V_{FB}|$

5.4.1 Basic of the PID Controller

The controller transfer function can be defined in many different ways. From the electrical point of view, we focus mainly on the transfer function numerator (*n*) and denominator (*d*) orders. As shown in Fig.5.4.2, the ideal PID controller has two numerator zeros and one pole in the origin of the complex plane. Its high frequency gain increases to infinity. On this account, the ideal PID is unrealizable (non-causal system). Therefore, we use practically a controller with derivative filtering, having identical numerator and denominator orders [31]. This controller can be written in the transfer function form (1):

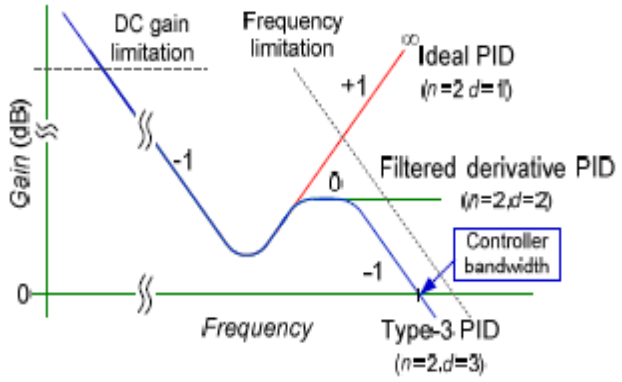

Fig 5.4.2 Frequency transfers with indicated slopes of ideal, filtered derivative and type-3 PID controller.

$$C(s) = k\left(1 + \frac{1}{T_1 s} + \frac{T_d s}{\alpha T_d s + 1}\right) \qquad (26)$$

Where T_i and T_d are the integrator and differentiator time constants, k is the gain and α the filtering factor. However, Fig. 5.4.2 shows that derivative filtered controller (26) has ideally infinite frequency bandwidth, limited in reality by the active element frequency range. This limitation is inaccurate and can results in some unpredictable behaviour. In applications as the switched DC/DC converters, the accurate control of the high frequency gain is obtained by an

additional 1st order lag transfer 1/(s/p_2+1). Thus, all Fig. 5.4.2 controllers can be written in zero-pole form (rad/s):

$$C(s) = K\frac{(s/z_1 + 1)(s/z_2 + 1)}{s(s/p_1 + 1)(s/p_2 + 1)} \qquad (27)$$

Where $p_1 = p_2 = \infty$ corresponds to the ideal PID, $p_1 < \infty$, $p_2 = \infty$ to the derivative filtered (or type-2) controller (1) and p_1, $p_2 < \infty$ to controller with additional first-order lag (referred as type-3 controller). Conversion between the controller forms (1) and (2) can be done by solving ordinary quadratic equations [31].

5.4.2 CDBA Based Controller

The controller with CDBA is shown in Fig.7.2.1. It includes one (–) and one (+) impedance input (polarities can be reversed)[32].

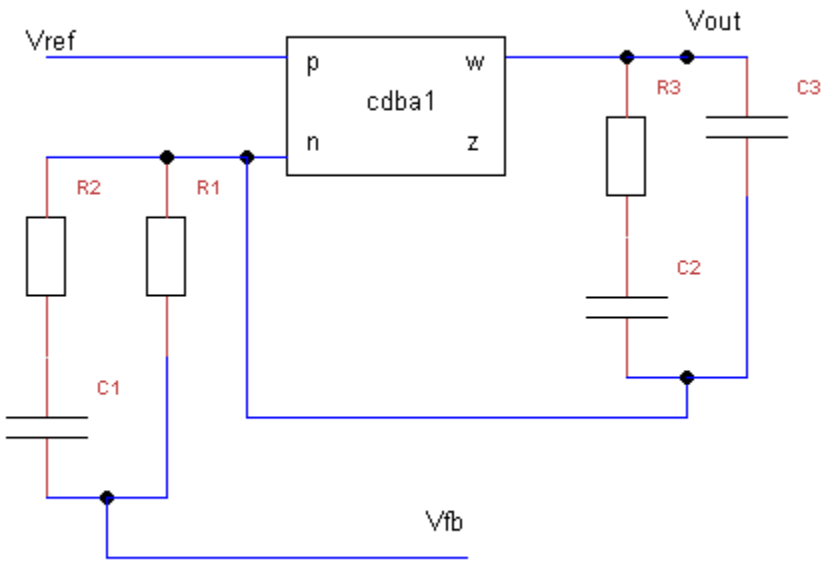

Fig.5.4.3 Controller with current differential buffer amplifier

The transfer functions V_{OUT}/V_{FB} and V_{OUT}/V_{REF} are

$$\frac{V_{OUT}}{V_{FB}} = -\frac{1}{R_1(C_2+C_3)} \frac{(R_3C_2S+1)(C_1(R_1+R_2)S+1)}{S(R_2C_1S+1)\left(\frac{C_2C_3}{C_2+C_3}R_3S+1\right)} \quad (28)$$

$$\frac{V_{OUT}}{V_{REF}} = 1 + \frac{1}{R_1(C_2+C_3)} \frac{(R_3C_2S+1)(C_1(R_1+R_2)S+1)}{S(R_2C_1S+1)\left(\frac{C_2C_3}{C_2+C_3}R_3S+1\right)} \quad (29)$$

5.4.3 Simulation results

Simulations were carried out to investigate the output of that circuit configuration of Figure 5.4.3 Supply voltage of ±0.6 V was used for simulations. Figure 5.4.4 and 5.4.5 shows the input transfer and output transfer function variation against frequency of the used circuit. The simulated output obtained with component values as R_1=813Ω, R_2=390Ω, R_3=2.16Ω, C_1=4.51nF, C_2=2.52nF and C_3=10nF is shown in Figure 5.4.3.

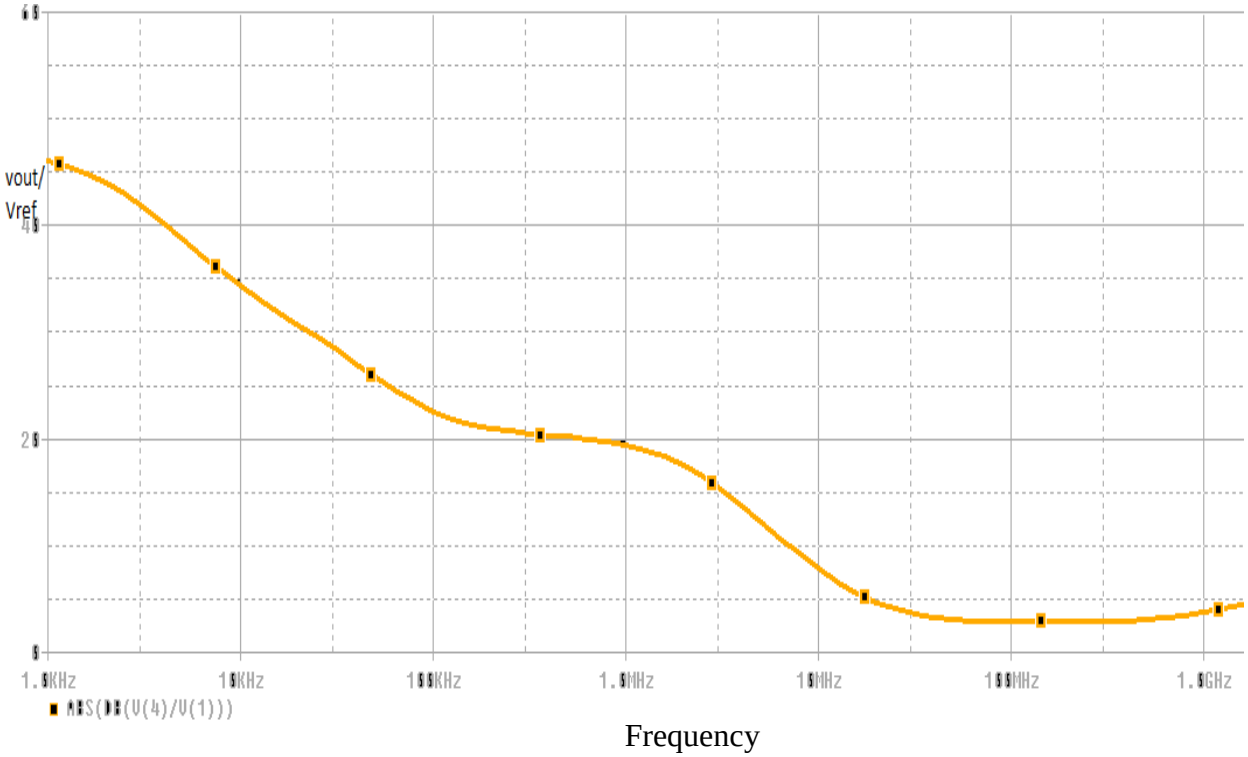

Fig.5.4.4 simulated transfer function of V_{out}/V_{ref} versus frequency

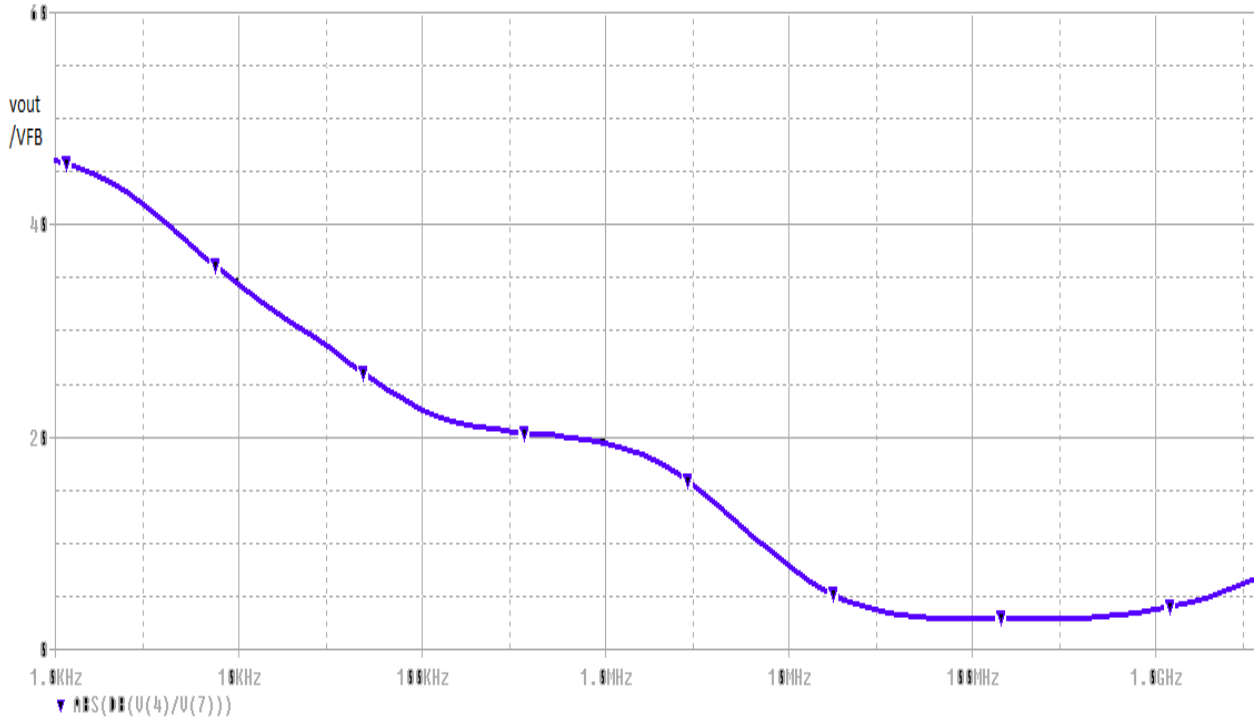

Fig.5.4.5 simulated transfer function of V_{out}/V_{ref} versus frequency

The controller has asymmetrical transfers from V_{FB} $and V_{REF}$ to the output. This affects only the low frequency part of the characteristics. Optionally, $R_1 - R_2 - C_1$ circuit recopied to the (+) input can resolve this problem.

Chapter 6

Conclusion and Future scope

In this thesis, a detailed study of the Current Difference Buffer Amplifier (CDBA) has been presented. CDBA being a current mode building block inherits the advantage of current mode processing such as large dynamic range, higher slew rate, low power consumption, less complex circuitry and higher signal bandwidth. CDBA can operate in both voltage and current mode, thus provides further flexibility and enables a variety of circuit design.

The presented work is broadly divided in three sections. In the first section an extensive literature review on CDBA block and its applications has been done. In second section CMOS realizations of CDBA and few existing applications of CDBA are studied. Further a low voltage low power CMOS CDBA presented in [21] is simulated and characterized. This CDBA block is then used for verification of CDBA based applications available in literature. In concluding section few new circuit applications of CDBA are proposed. These circuits include a CM multi output filter, a grounded inductor topology, monostable multivibrator and a single CDBA based PID controller configuration. For each of the proposed circuit, a detailed analysis is formulated. Also, to verify the working of these proposed circuits SPICE simulations are carried out. The simulated results are found in close agreement of theoretical propositions.

The need for low-voltage low power circuits is immense in portable electronic equipments like laptop computers, pace makers, cell phones etc. During the last few decades, the current mode processing has emerged as low voltage design technique for analog design and has become a viable alternative over voltage mode circuits and is becoming powerful tool for the development of high performance analog circuits and systems. Keeping the benifits of current mode processing and the advantages offered by CDBA in view there is a tremendous scope of utilizing CDBA in analog circuit design.

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APPENDIX

0.18 µm, level 7 parameters provided by TSMC for NMOS

LEVEL = 7		
+DSUB = 0.0217897	+ TNOM = 27	TOX = 4.1E-9
+XJ = 1E-7	NCH = 2.3549E17	VTH0 = 0.3750766
+K1 = 0.5842025	K2 = 1.245202E-3	K3 = 1E-3
+K3B = 0.0295587	W0 = 1E-7	NLX = 1.597846E-7
+DVT0W = 0	DVT1W = 0	DVT2W = 0
+DVT0 = 1.3022984	DVT1 = 0.4021873	DVT2 = 7.631374E-3
+U0 = 296.8451012	UA = -1.179955E-9	UB = 2.32616E-18
+UC = 7.593301E-11	VSAT = 1.747147E5	A0 = 2
+AGS = 0.452647	B0 = 5.506962E-8	B1 = 2.640458E-6
+KETA = -6.860244E-3	A1 = 7.885522E-4	A2 = 0.3119338
+RDSW = 105	PRWG = 0.4826	PRWB = -0.2
+WR = 1	WINT = 4.410779E-9	LINT = 2.045919E-8
+XL = 0	XW = -1E-8	DWG = -2.610453E-9
+DWB = -4.344942E-9	VOFF = -0.0948017	NFACTOR = 2.1860065
+CIT = 0	CDSC = 2.4E-4	CDSCD = 0
+CDSCB = 0	ETA0 = 1.991317E-3	ETAB = 6.028975E-5
+DSUB = 0.0217897	PCLM = 1.7062594	PDIBLC1 = 0.2320546
+PDIBLC2 = 1.670588E-3	PDIBLCB = -0.1	DROUT = 0.8388608
+PSCBE1 = 1.904263E10	PSCBE2 = 1.546939E-8	PVAG = 0
+DELTA = 0.01	RSH = 7.1	MOBMOD = 1
+PRT = 0	UTE = -1.5	KT1 = -0.11
+KT1L = 0	KT2 = 0.022	UA1 = 4.31E-9
+UB1 = -7.61E-18	UC1 = -5.6E-11	AT = 3.3E4
+WL = 0	WLN = 1	WW = 0
+WWN = 1	WWL = 0	LL = 0
+LLN = 1	LW = 0	LWN = 1

+LWL = 0	CAPMOD = 2	XPART = 0.5
+CGDO = 6.7E-10	CGSO = 6.7E-10	CGBO = 1E-12
+CJ = 9.550345E-4	PB = 0.8	MJ = 0.3762949
+CJSW = 2.083251E-10	PBSW = 0.8	MJSW = 0.1269477
+CJSWG = 3.3E-10	PBSWG = 0.8	MJSWG = 0.1269477
+CF = 0	PVTH0 = -2.369258E-3	PRDSW = -1.2091688
+PK2 = 1.845281E-3	WKETA = -2.040084E-3	LKETA = -1.266704E-3
+PU0 = 1.0932981	PUA = -2.56934E-11	PUB = 0
+PVSAT = 2E3	PETA0 = 1E-4	PKETA = -3.350276E-3)

0.18 µm, level 7 parameters provided by TSMC for PMOS

```
  LEVEL   = 7

+ TNOM    = 27              TOX     = 4.1E-9
+XJ   = 1E-7                NCH     = 4.1589E17       VTH0    = -0.3936726
+K1   = 0.5750728           K2      = 0.0235926       K3      = 0.1590089
+K3B= 4.2687016             W0      = 1E-6            NLX     = 1.033999E-7
+DVT0W   = 0                DVT1W   = 0               DVT2W   = 0
+DVT0 = 0.5560978           DVT1    = 0.2490116       DVT2    = 0.1
+U0= 112.5106786            UA      = 1.45072E-9      UB      = 1.195045E-21
+UC      = -1E-10           VSAT    = 1.168535E5      A0      = 1.7211984
+AGS     = 0.3806925        B0      = 4.296252E-7     B1      = 1.288698E-6
+KETA    = 0.0201833        A1      = 0.2328472       A2      = 0.3
+RDSW    = 198.7483291      PRWG    = 0.5             PRWB    = -0.4971827
+WR      = 1                WINT    = 0               LINT    = 2.943206E-8
+XL      = 0                XW      = -1E-8           DWG     = -1.949253E-8
+DWB     = -2.824041E-9     VOFF    = -0.0979832      NFACTOR = 1.9624066
+CIT     = 0                CDSC    = 2.4E-4          CDSCD   = 0
+CDSCB   = 0                ETA0    = 7.282772E-4     ETAB    = -3.818572E-4
+DSUB    = 1.518344E-3      PCLM    = 1.4728931       PDIBLC1 = 2.138043E-3
+PDIBLC2 = -9.966066E-6     PDIBLCB = -1E-3           DROUT   = 4.276128E-4
+PSCBE1  = 4.850167E10      PSCBE2  = 5E-10           PVAG    = 0
+DELTA   = 0.01             RSH     = 8.2             MOBMOD  = 1
+PRT     = 0                UTE     = -1.5            KT1     = -0.11
+KT1L    = 0                KT2     = 0.022           UA1     = 4.31E-9
+UB1     = -7.61E-18        UC1     = -5.6E-11        AT      = 3.3E4
+WL      = 0                WLN     = 1               WW      = 0
+WWN     = 1                WWL     = 0               LL      = 0
+LLN     = 1                LW      = 0               LWN     = 1
+LWL     = 0                CAPMOD  = 2               XPART   = 0.5
+CGDO    = 7.47E-10         CGSO    = 7.47E-10        CGBO    = 1E-12
+CJ      = 1.180017E-3      PB      = 0.8560642       MJ      = 0.4146818
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+CJSWG = 4.22E-10	PBSWG = 0.9123142	MJSWG = 0.316175
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+PK2 = 1.338191E-3	WKETA = 0.0246885	LKETA = -2.016897E-3
+PU0 = -1.5089586	PUA = -5.51646E-11	PUB = 1E-21
+PVSAT = 50	PETA0 = 1E-4	PKETA = -3.316832E-3