CHAPTER 3

TEST SYSTEM AND RESULTS

In modern distribution systems, proliferation of non linear loads causes power quality problems such as voltage sags, harmonics, voltage imbalance etc. To mitigate these problems, custom power devices are used in the system. DSTATCOM is a shunt connected custom power device which helps in maintaining the voltage profile and improves the power factor also. This chapter discusses the test system and the MATLAB model of DSTATCOM. The performance of the system with/without DSTATCOM with a variety of loads is also discussed.

3.1 Test System

In this project a test system is employed with three phase source (415 V, 50 Hz) feeding a variety of consumer loads. The source is connected to load by a feeder impedance (R = 0.05Ω, L=1mH). The DSTATCOM is connected in shunt configuration at the PCC. The modeled system is tested on different load conditions such as linear load, non linear load, unbalance loads and phase out conditions. A single line diagram of test system is shown below in Fig 3.1. The system parameters are listed in Appendix.

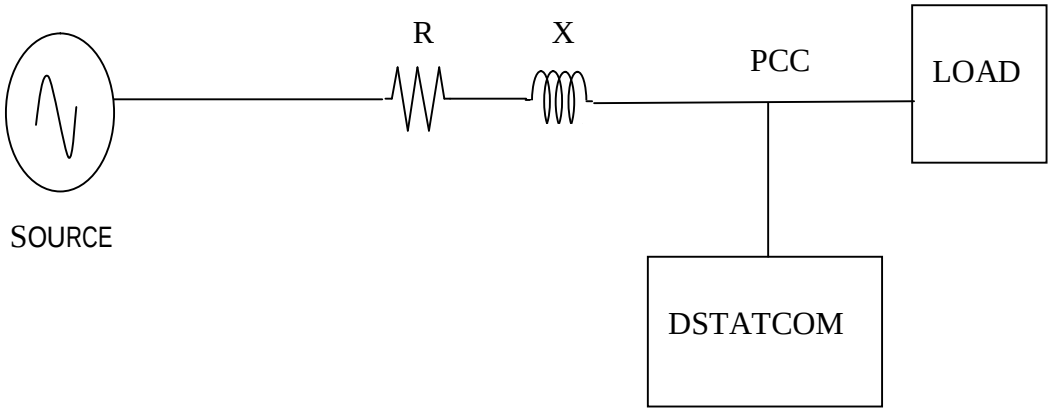

Fig 3.1 Single Line diagram of Test System

3.2 Control Schemes for DSTATCOM

Many algorithms for DSTATCOM control have been proposed. In this work, two control algorithms namely IRPT and SRF have been developed to control DSTATCOM. Fig 3.2 shows the basic model of the system using Simulink/SimPower systems of MATLAB environment. It shows the 3-phase supply connected to linear (R-L) load via feeder impedances. The DSTATCOMN is modeled as a VSC with three legs, each leg having 2 IGBT switches. A Dc link capacitor of value 1500µF is placed at the DC link. This VSC is interfaced to the system through coupling transformer which is represented in the form of interface inductors (value 2.2mH) as shown in the figure. Small ripple filter connected in delta configuration is suitably placed to reduce switching harmonics. The control of the DSTATCOM is discussed next, using IRPT and SRF techniques.

3.2.1 Control of DSTATCOM using Instantaneous Reactive Power (IRP) Theory

Fig 3.3 discusses the control of DSTATCOM based on IRPT. In this control algorithm the compensating currents are calculated by transforming the 3-phase quantities into 2-phase quantities in α-β frame. Fig 3.3a shows the conversion of load current and PCC voltage into i_α, i_β and v_α, v_β. The instantaneous active (p) and reactive power (Q) is calculated in α-β frame in Fig 3.3b using eq^n 3.1 shown below. Now the reference active power (Pref) is generated as shown in Fig 3.3c. A PI controller is used to maintain the DC link voltage whose output refers to the switching losses occurring across the VSC which is to be supplied by the DSTATCOM. Now the reference active power (Pref) and reactive power (Q) are used to calculate the required compensating currents for making the source power factor to unity as shown in Fig 3.3d using equations 3.2 & 3.3. Now as shown in Fig 3.3e, this reference compensating currents are passed through hysteresis current controller to generate the gating pulses for the 6 IGBT switches of the VSC.

$$p = v_\alpha i_\alpha + v_\beta i_\beta \qquad 3.1$$

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \frac{1}{\Delta} \begin{bmatrix} v_\alpha & -v_\beta \\ v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} p \\ q \end{bmatrix} \qquad 3.2$$

$$\begin{bmatrix} i^*_{sa} \\ i^*_{sb} \\ i^*_{sc} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1/\sqrt{2} & 1 & 0 \\ 1/\sqrt{2} & -1/2 & \sqrt{3}/2 \\ 1/\sqrt{2} & -1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i_0 \\ i_\alpha \\ i_\beta \end{bmatrix} \qquad 3.3$$

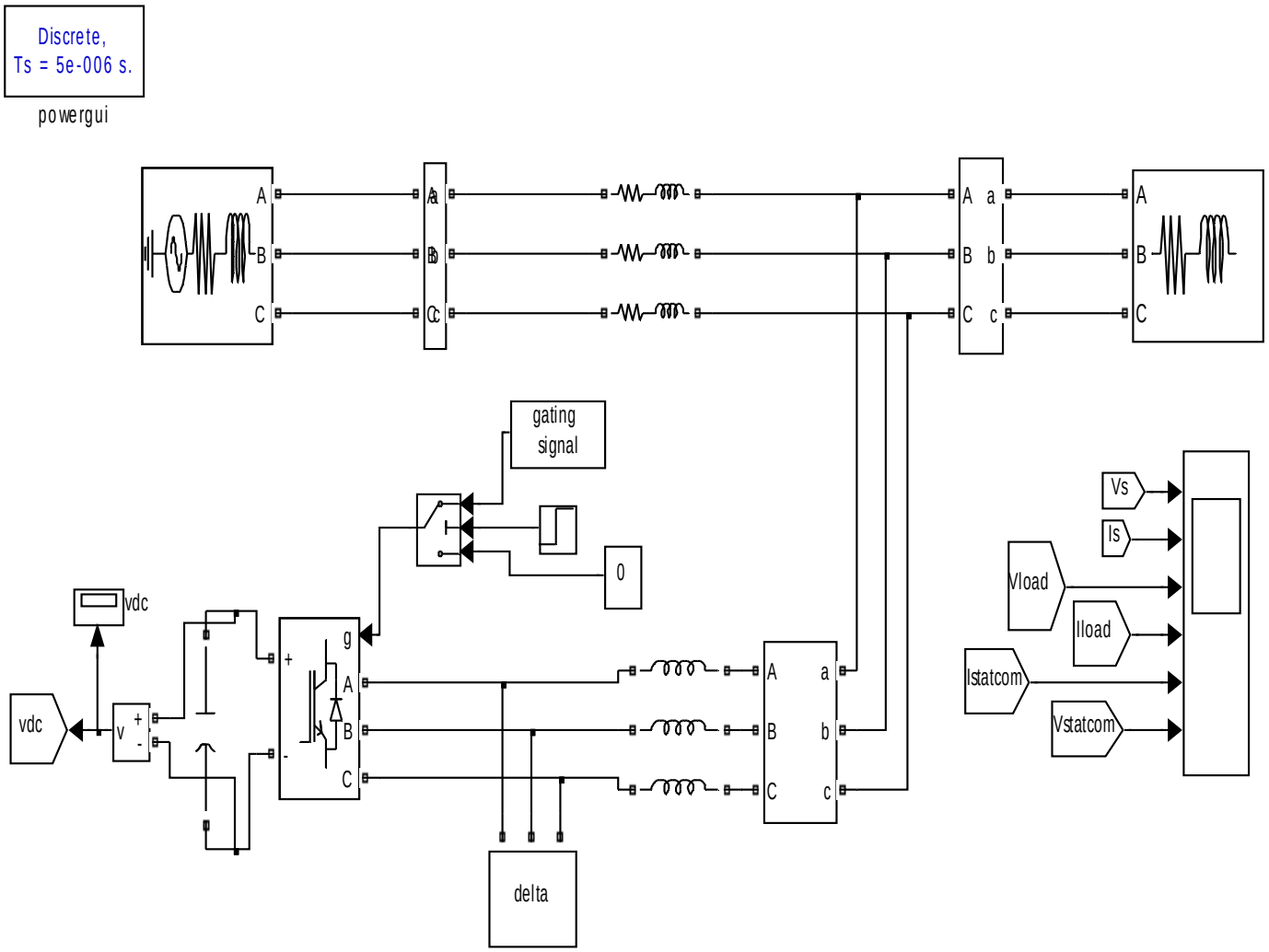

Fig 3.2 Simulink model of Test System

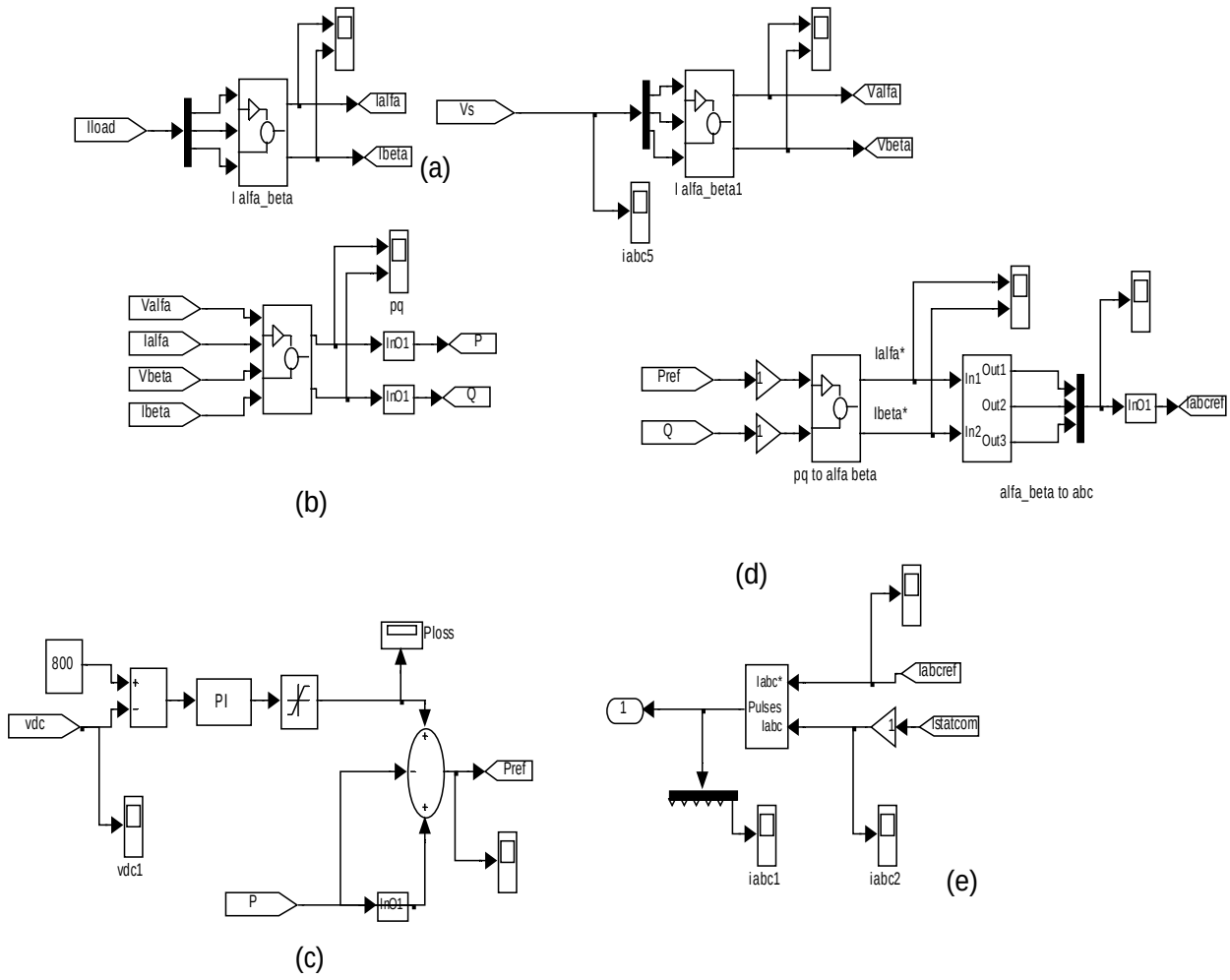

Fig 3.3 Simulink model of IRPT control algorithm

3.2.2 Control of DSTATCOM using Synchronous Reference Frame (SRF) Theory

Fig 3.4 discusses the control of DSTATCOM based on SRF theory. In this control algorithm the 3-phase quantities are converted into synchronously rotating d-q frame. From these d-q quantities the required compensating currents are calculated. The phase angle required for d-q conversion is calculated using PLL as shown in Fig 3.4a. The 'd' component of reference compensating current is generated using one PI controller connected over dc link voltage, while

the ‘q’ component is calculated from PI controller connected over terminal voltage as shown in Fig 3.4b. Now these dq components of compensating currents are converted to abc components and then these abc components are passed through hysteresis current controller to generate the gating pulses for the 6 IGBT switches of VSC.

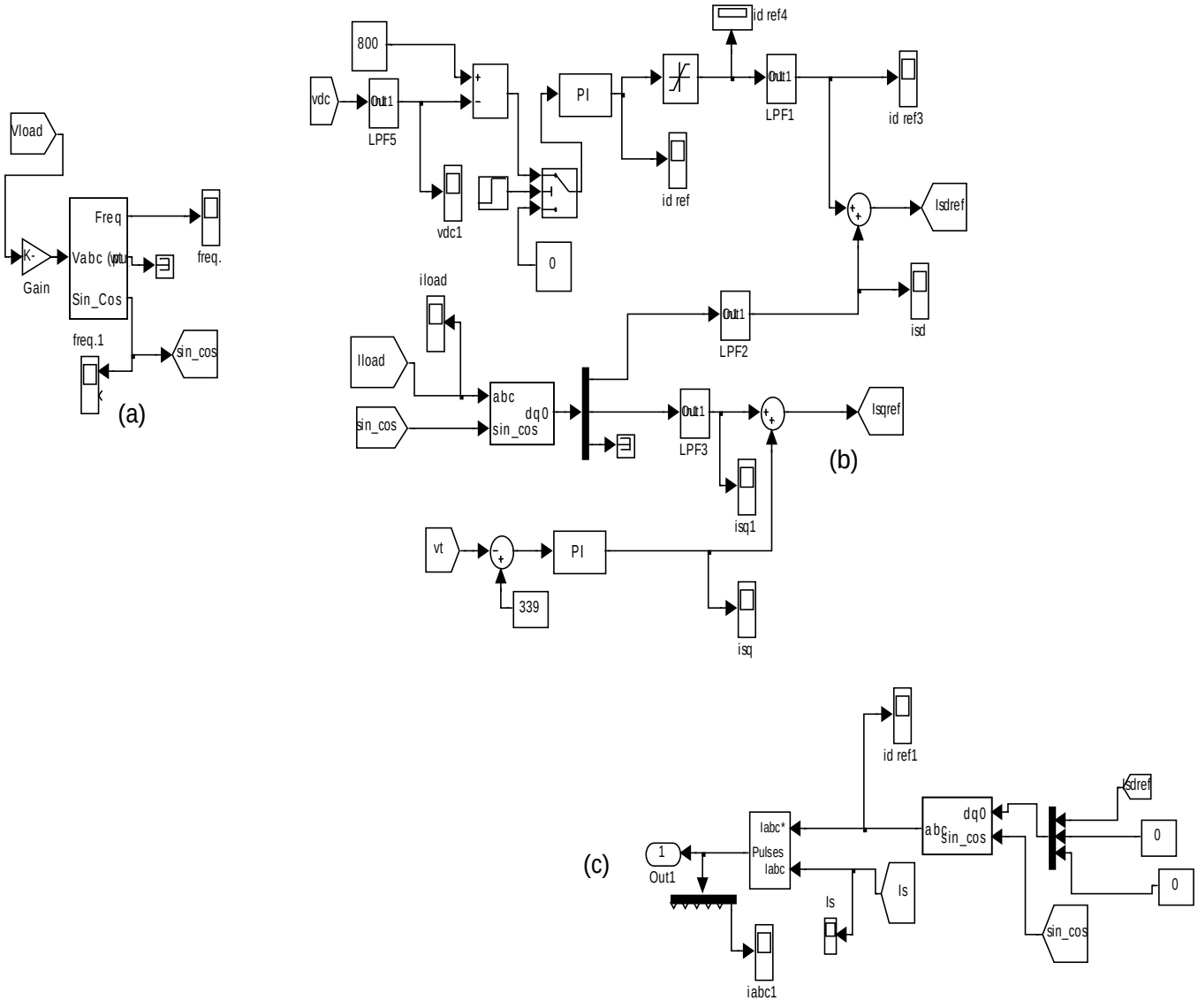

Fig 3.4 Simulink model of SRF algorithm

3.2.3 Performance Evaluation of DSTATCOM

Both the control algorithms have been used in the test system to maintain the PCC voltage at the reference value. The reference value of voltage is taken as 1pu which is 339 V (rms) phase to ground. The results for both the algorithms are shown below in Fig 3.5 & 3.6.

A. Performance of DSTATCOM with IRPT Control Algorithm

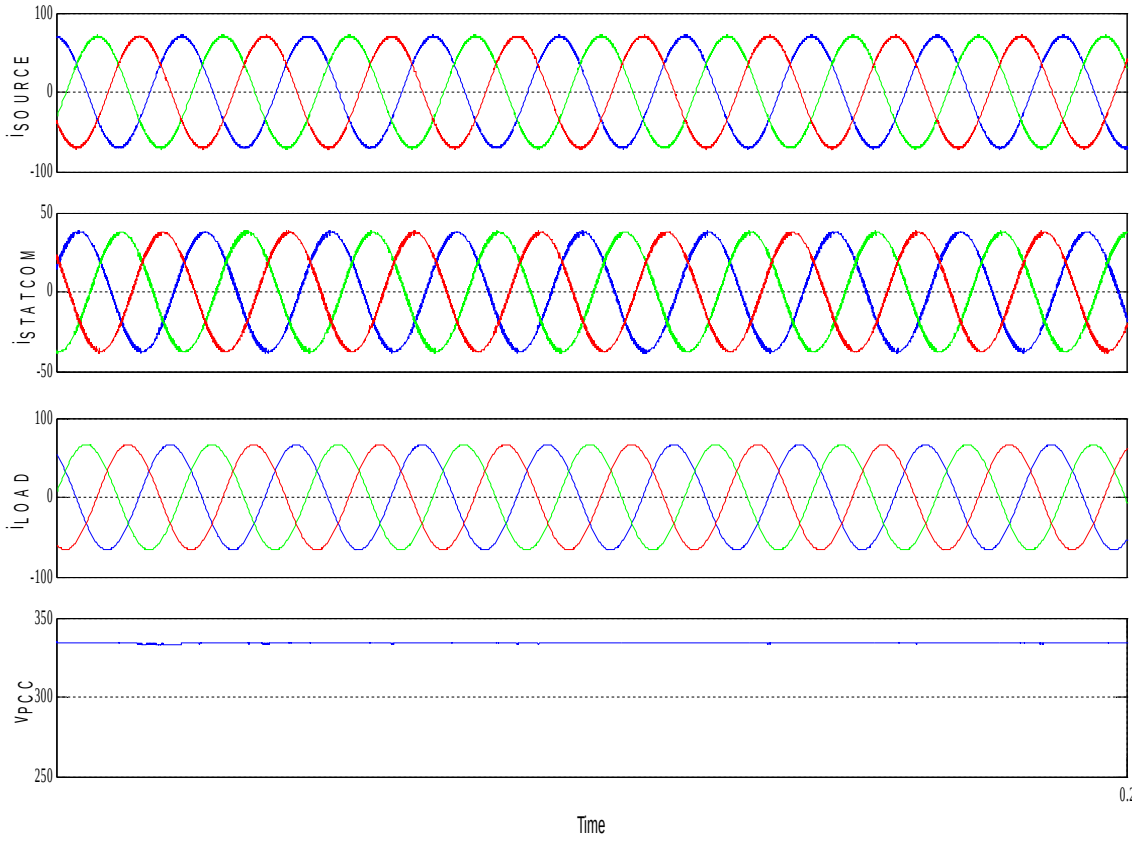

Fig 3.5 IRPT Results

Fig 3.5 shows the system response when DSTATCOM is controlled using IRPT scheme. In IRPT control algorithm the voltage at PCC is maintained at the reference value but the value of Total Harmonic Distortion (THD) in the source current comes out to be 3.56% which is high. The results show the plots of supply currents (i_{source}), DSTATCOM currents ($i_{statcom}$), Load currents (i_{load}) and the voltage at PCC (V_{PCC}) w.r.t time. A linear R-L load drawing active power

of 20 kW and reactive power of 30 kVAR is considered. The IRPT scheme is able to regulate the voltage to the desired reference voltage of 339 V.

B. Performance of the DSTATCOM with SRF Theory

Fig3.6 shows the system response when DSTATCOM is controlled using SRF Theory. The results show the plots of supply currents (i_{source}), DSTATCOM currents ($i_{statcom}$), Load currents (i_{load}) and the voltage at PCC (V_{PCC}) w.r.t time.

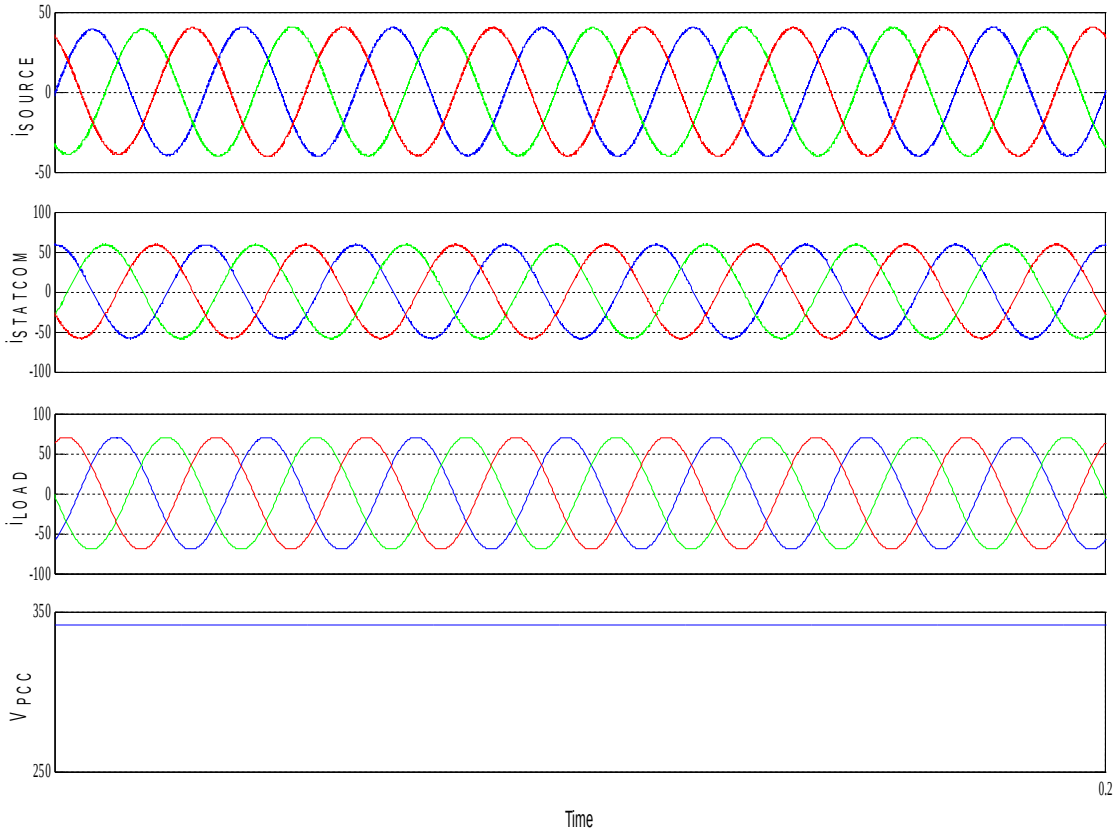

Fig 3.6 SRF Theory Results

A comparison of both the SRF and IRPT theories on the same test system with the same load parameters shows that while the voltage at PCC is regulated in both schemes, but the supply currents are more sinusoidal and THD is comparatively lower in case of SRF scheme. The supply current has THD of 1.09% with SRF scheme while THD is of the order of 3.56% with IRPT.

3.3 Load Compensation using DSTATCOM

The performance evaluation of DSTATCOM with linear load, nonlinear load and unbalanced load is discussed next.

3.3.1 Linear Load

In distribution systems, loads on the system keeps on changing resulting in voltage change at PCC. DSTATCOM can be suitably controlled to maintain the voltage level by supplying the required reactive power to the load. In this test case, a load drawing active power value of 20 kW and reactive power value of 10kVAR is considered and the value of PCC voltage is monitored with and without DSTATCOM. The PCC voltage level improves in case of DSTATCOM and maintained at reference value of 1pu. The DSTATCOM starts working after a delay of 0.03 sec. Fig 3.7 show results of the test system without DSTATCOM. It shows the plots of supply currents (i_{source}), DSTATCOM currents ($i_{statcom}$), Load currents (i_{load}) and the voltage at PCC (V_{PCC}) w.r.t time. Fig 3.8 show results of the test system with DSTATCOM. The results show the plots of supply currents (i_{source}), DSTATCOM currents ($i_{statcom}$), Load currents (i_{load}), voltage at PCC (V_{PCC}) and the DC link voltage (V_{DC}) w.r.t time. The DSTATCOM maintains the voltage at PCC to its reference value of 339 V which dips to a value of 330 V without DSTATCOM.

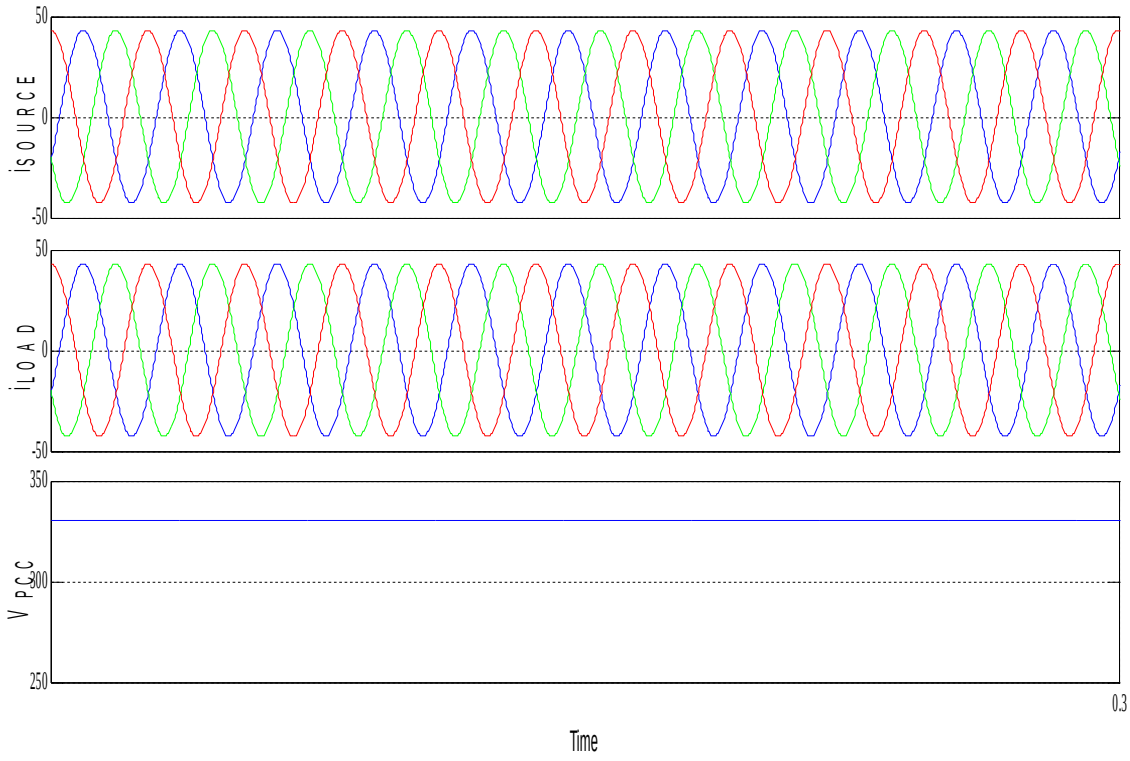

Fig 3.7 Results without DSTATCOM for a linear load

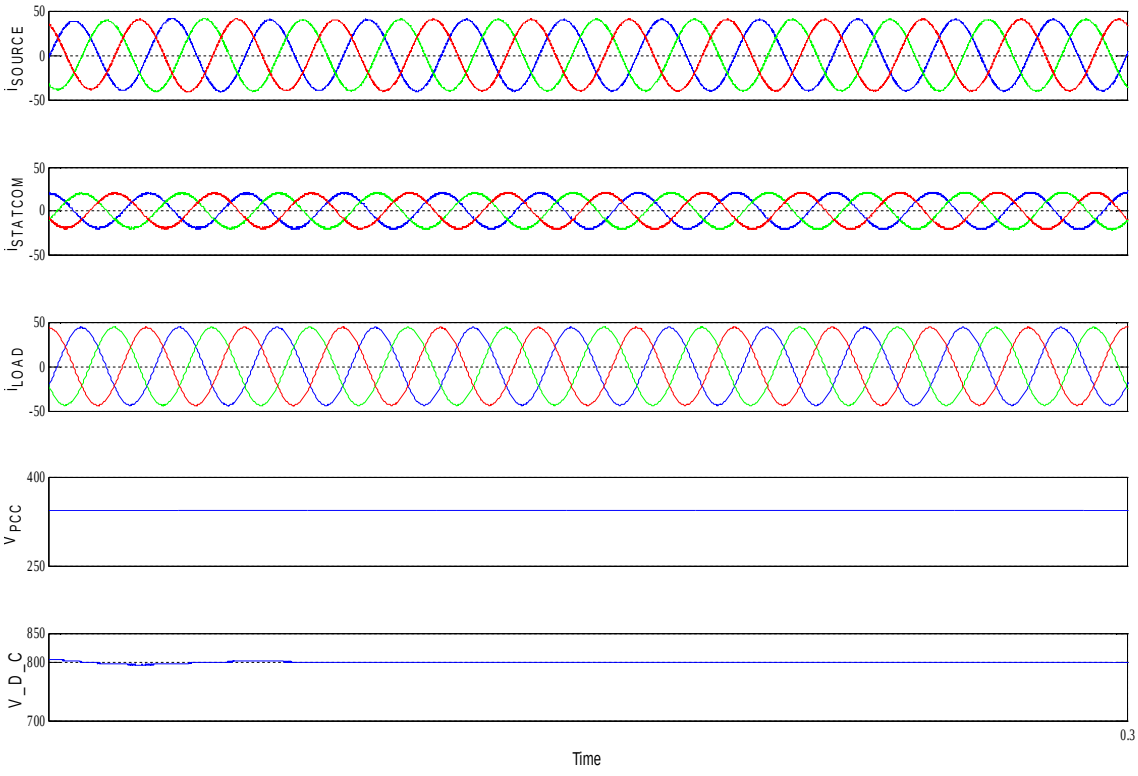

Fig 3.8 Results with DSTATCOM for a linear load

3.3.2 Non-Linear Load

In this case a universal diode bridge with different combinations of resistance, inductance and capacitance connected across it is taken as non linear load.

A. With R connected at end of diode rectifier

In this case a resistance of 500 Ω is connected across the diode bridge and after a time of 0.2 sec. another resistance in parallel of same value is switched on into the system.The source currents due to non linear load are distorted as shown in Fig 3.9. It shows the plots of supply currents (i_{source}), DSTATCOM currents ($i_{statcom}$), Load currents (i_{load}) and the voltage at PCC (V_{PCC}) w.r.t time. Fig 3.10 shows the plots of supply currents (i_{source}), DSTATCOM currents ($i_{statcom}$), Load currents (i_{load}), PCC voltage (V_{PCC}) and DC link voltage (V_{DC}) w.r.t time. DSTATCOM makes the source current sinusoidal and maintains the PCC voltage and DC link voltage to their reference values. DSTATCOM also improves the THD level of source currents from 29.35% to 3.26% as shown in Fig 3.11 & 3.12.

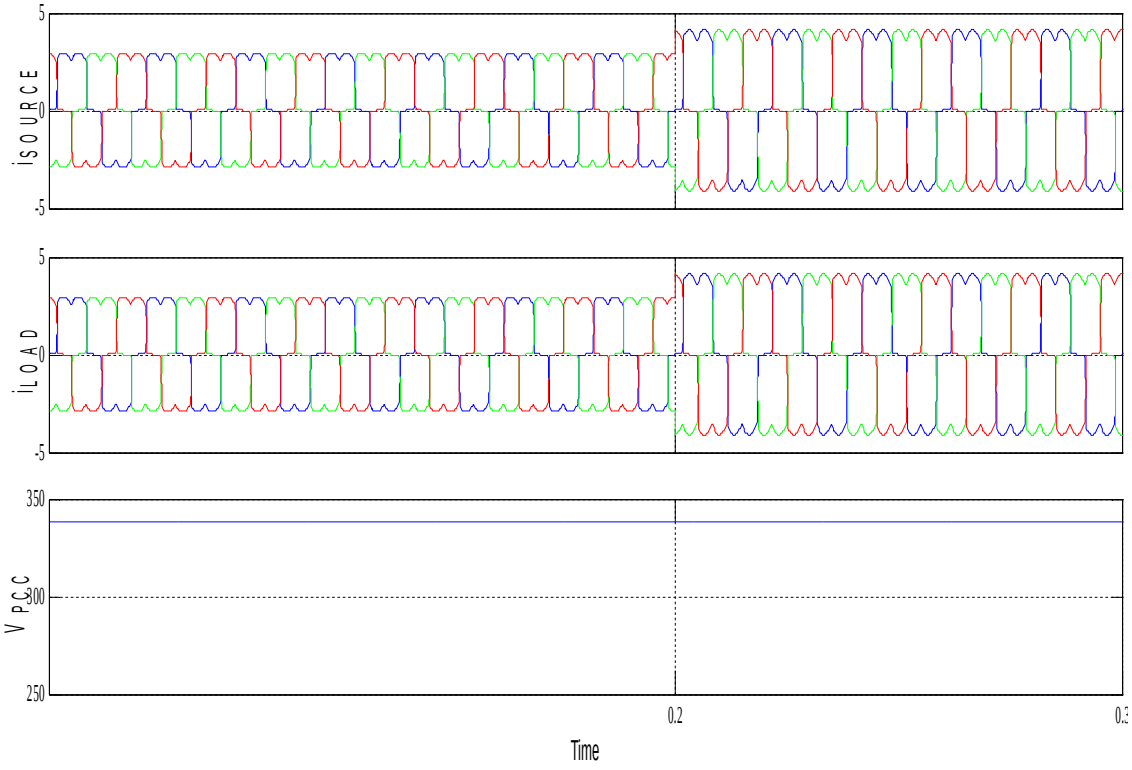

Fig.3.9 Results without DSTATCOM for a universal diode bridge with resistance switching

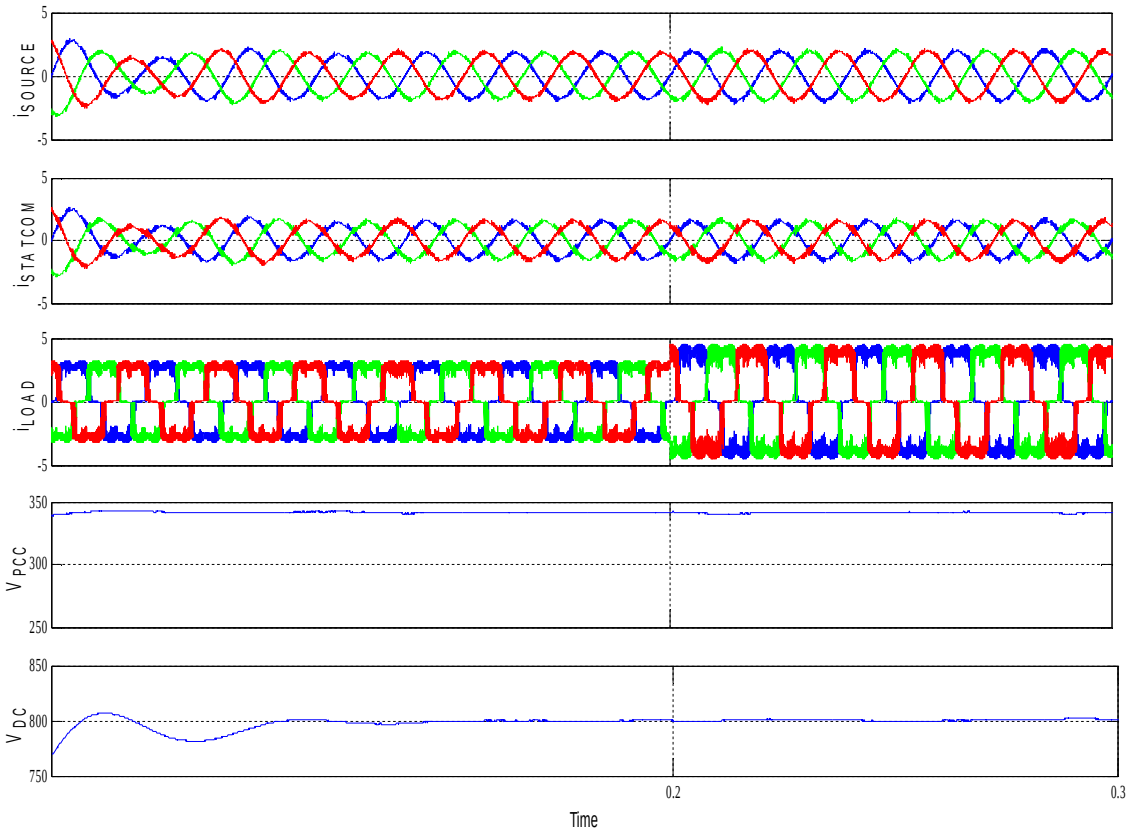

Fig. 3.10 Results with DSTATCOM for a universal diode bridge with resistance switching

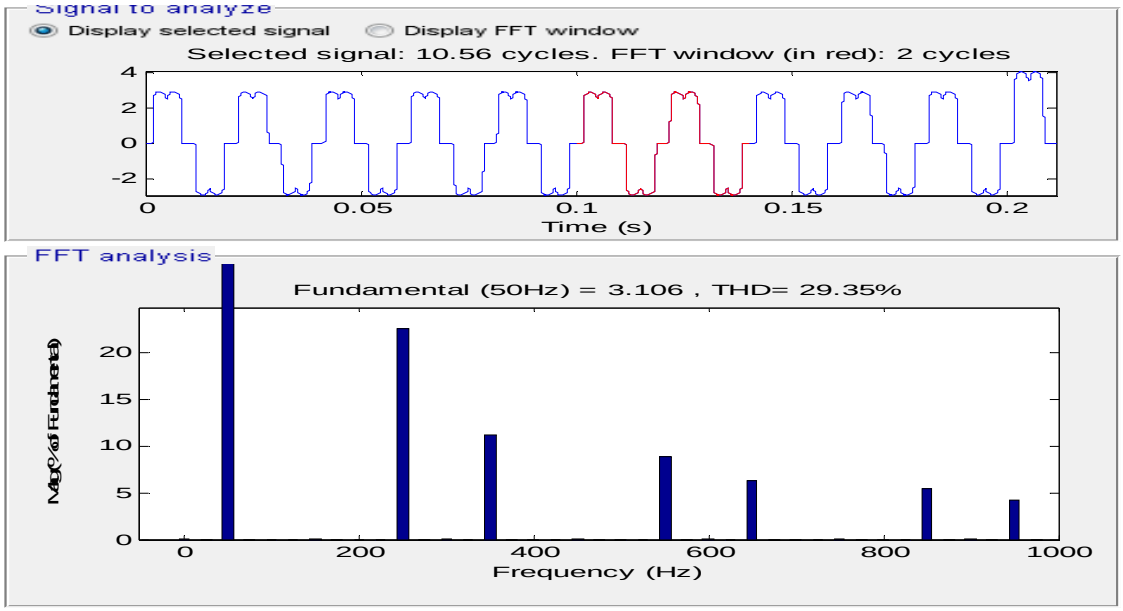

Fig. 3.11 Source current THD for a universal bridge without DSTATCOM for R Switching

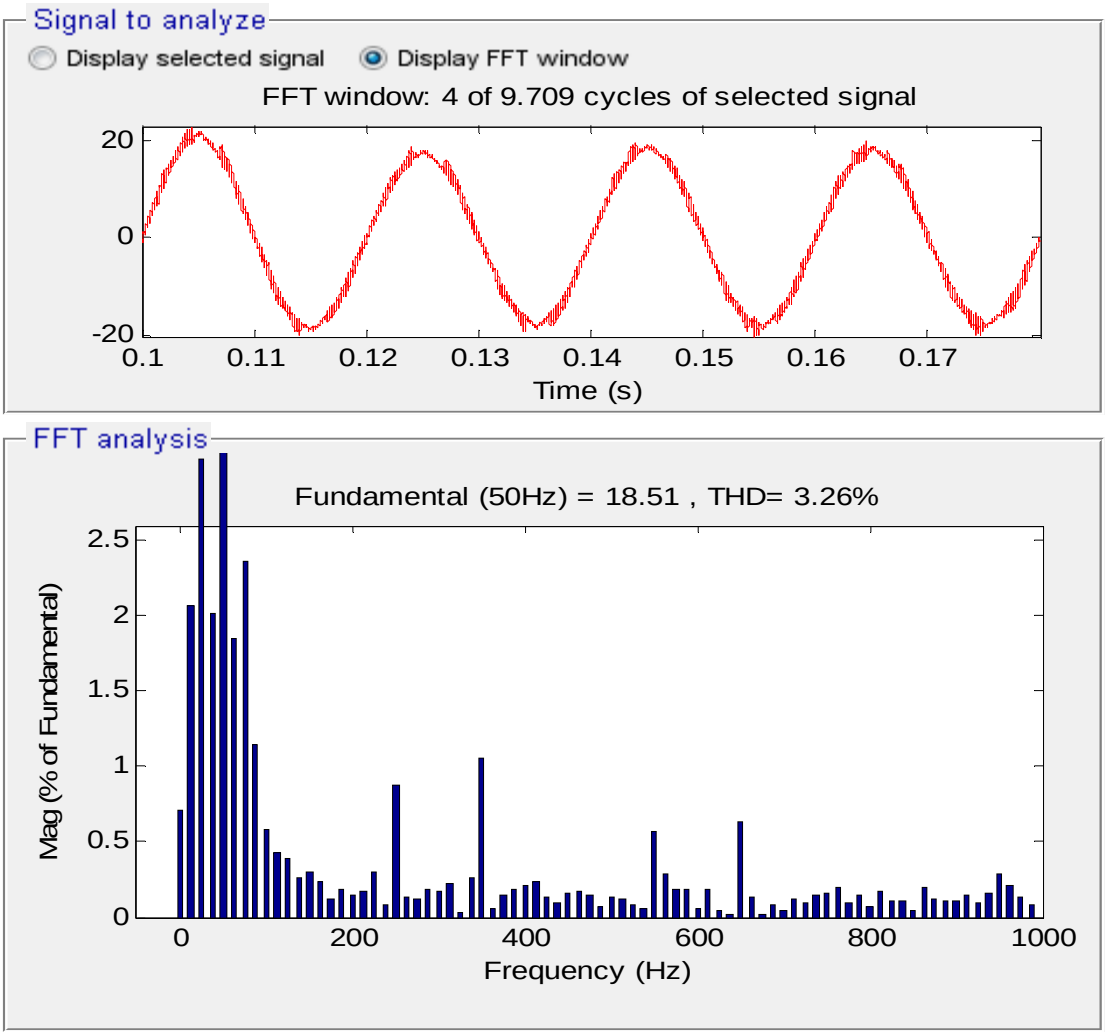

Fig. 3.12 Source current THD for a universal bridge with DSTATCOM for R Switching

B. With R-L connected at end of diode rectifier

In this case a series combination of resistance and inductance of values 500 Ω and 300 mH respectively is connected across the bridge. The source currents become distorted due to non linearity of the load as shown in Fig 3.13. DSTATCOM helps to maintain the PCC voltage and DC link voltage and the source currents becomes sinusoidal as shown in Fig 3.14. THD level improves from 29.65% to 3.05% with the help of DSTATCOM. Results of THD analysis are shown in Fig 3.15 & 3.16.

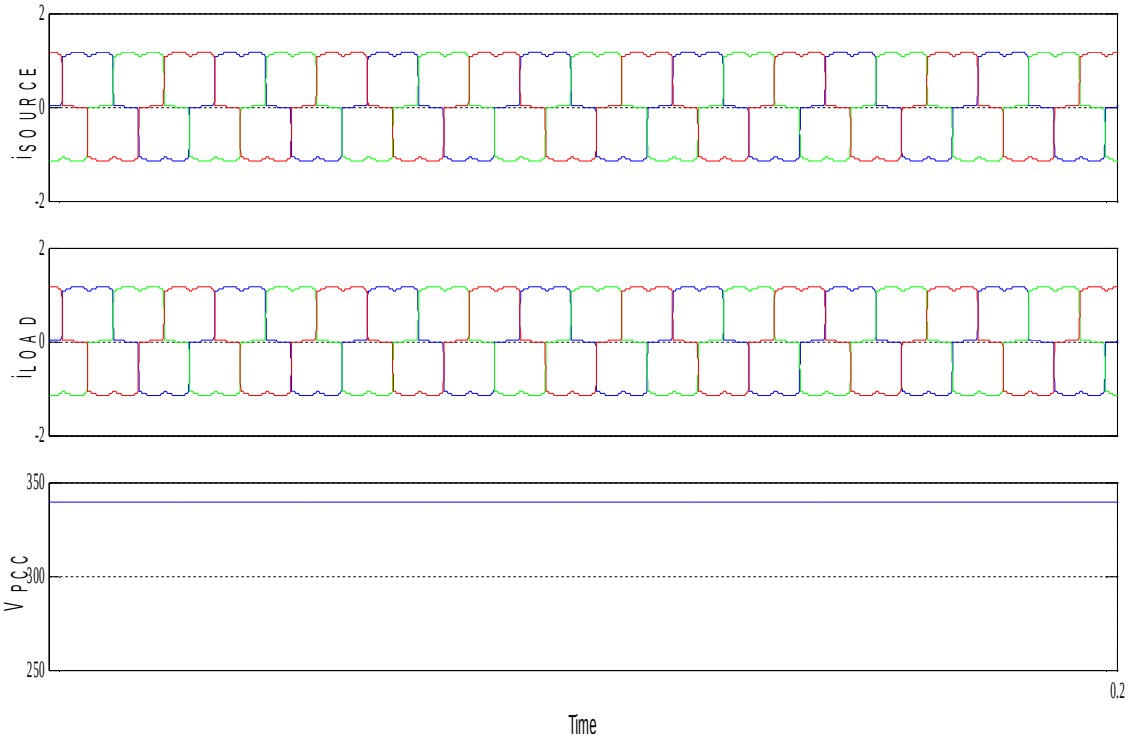

Fig.3.13 Results without DSTATCOM for a universal diode bridge with RL load

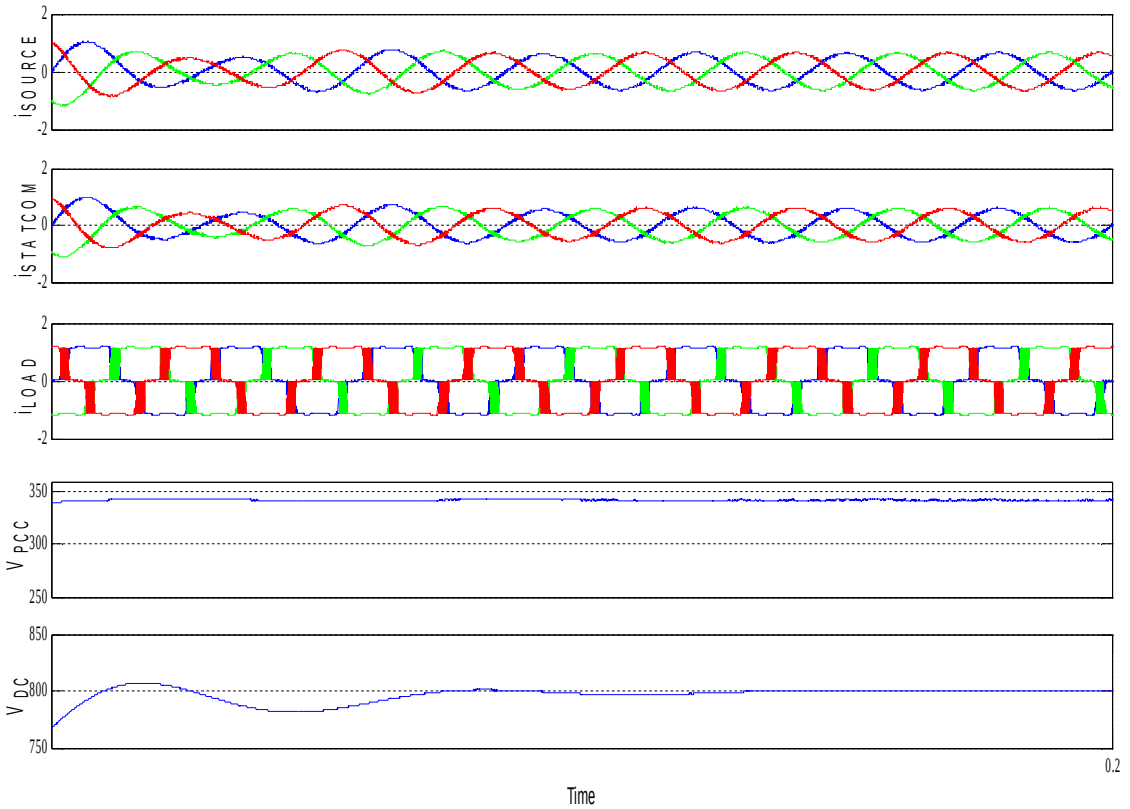

Fig.3.14 Results with DSTATCOM for a universal diode bridge with RL load

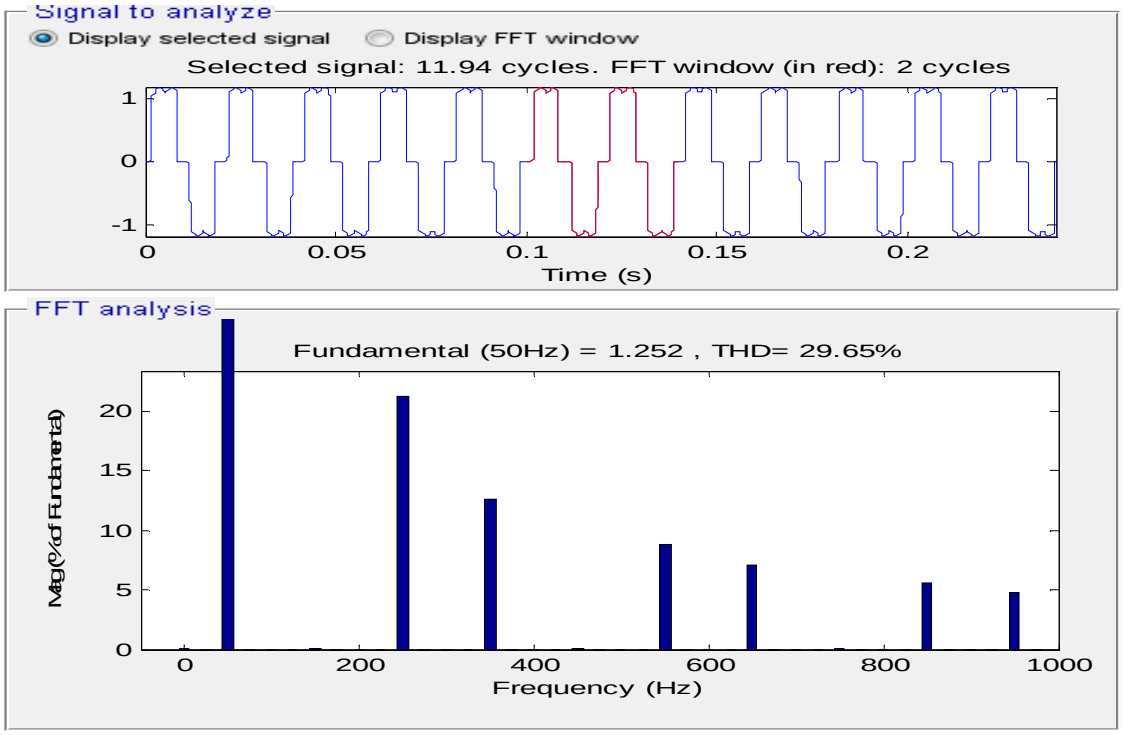

Fig. 3.15 Source current THD for a universal bridge without DSTATCOM for RL Load

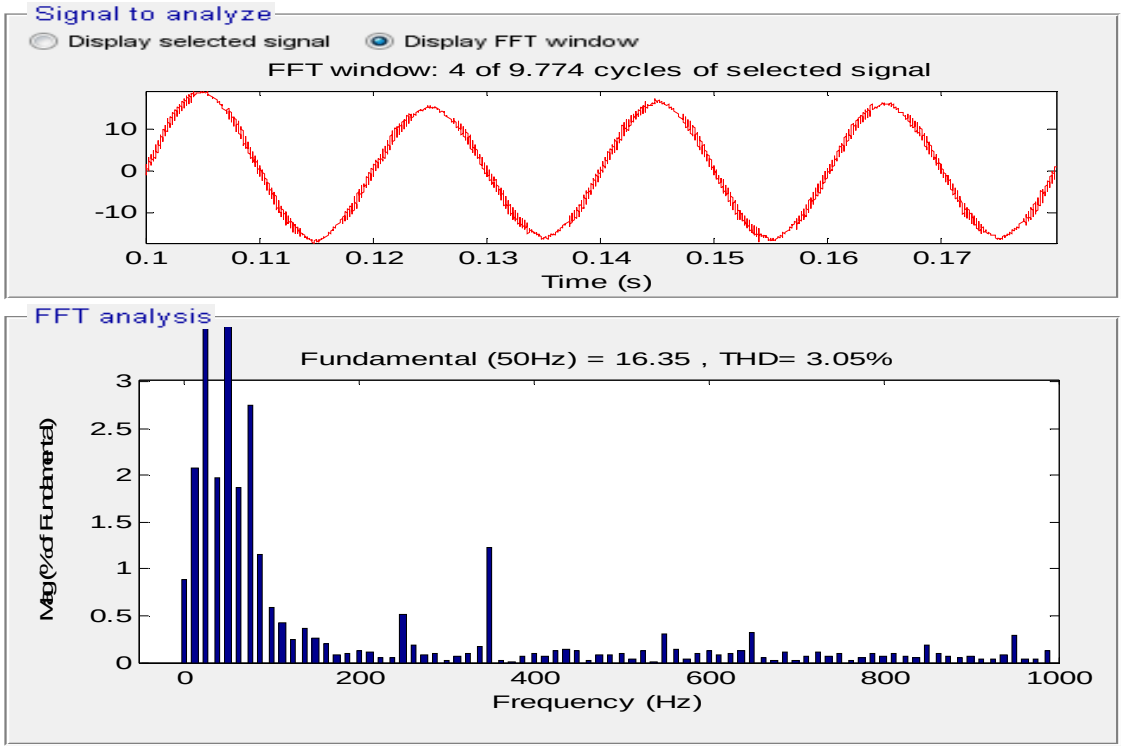

Fig. 3.16 Source current THD for a universal bridge with DSTATCOM for RL Load

C. With RLC load connected at the end of diode rectifier

In the last case a capacitor of value 200 µF is coneected in parellel with the above series RL load. Fig 3.17 shows the plots of supply current (i_{source}), DSTATCOM currents ($i_{statcom}$) and Load currents (i_{load}) of phase 'R' and also the voltage at PCC (V_{PCC}) w.r.t time. The distorted source currents become sinusoidal after installation of DSTATCOM as shown in Fig 3.18.The Dc link voltage is also maintained at its reference value of 800 V. The THD value in source current without DSTATCOM is 132.63% which reduces to a better value of 4.75% with DSTATCOM as shown in Fig 3.19 & 3.20.

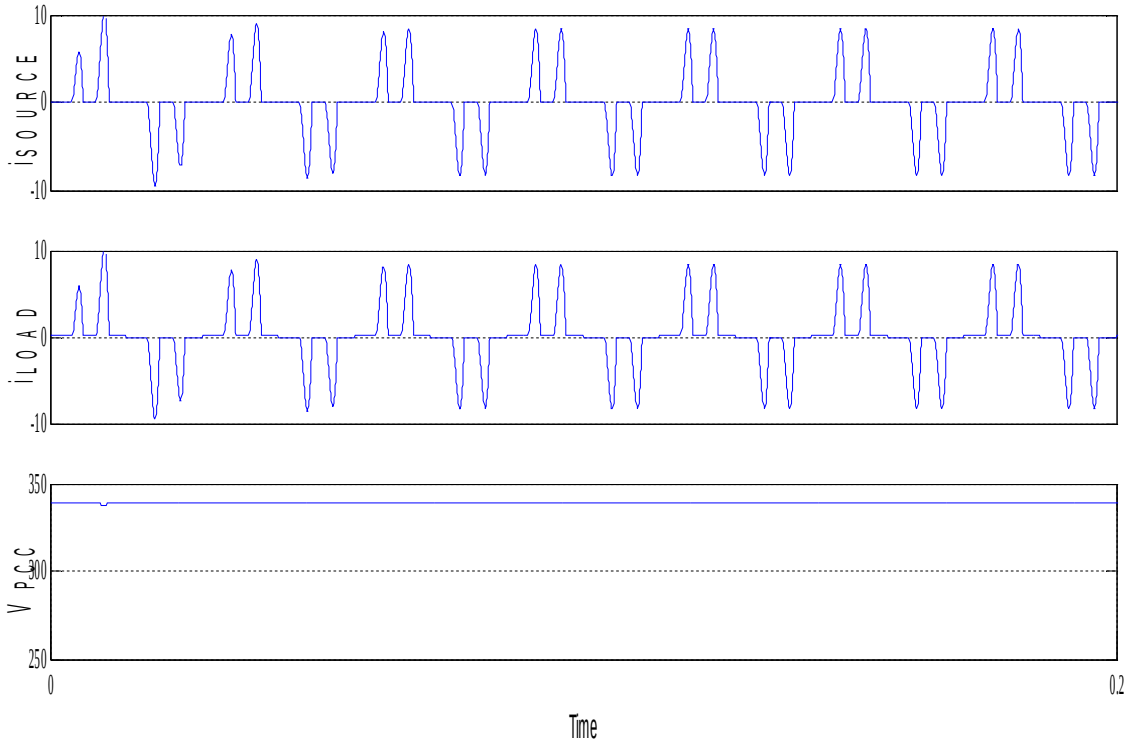

Fig.3.17 Results without DSTATCOM for a universal diode bridge with RLC load

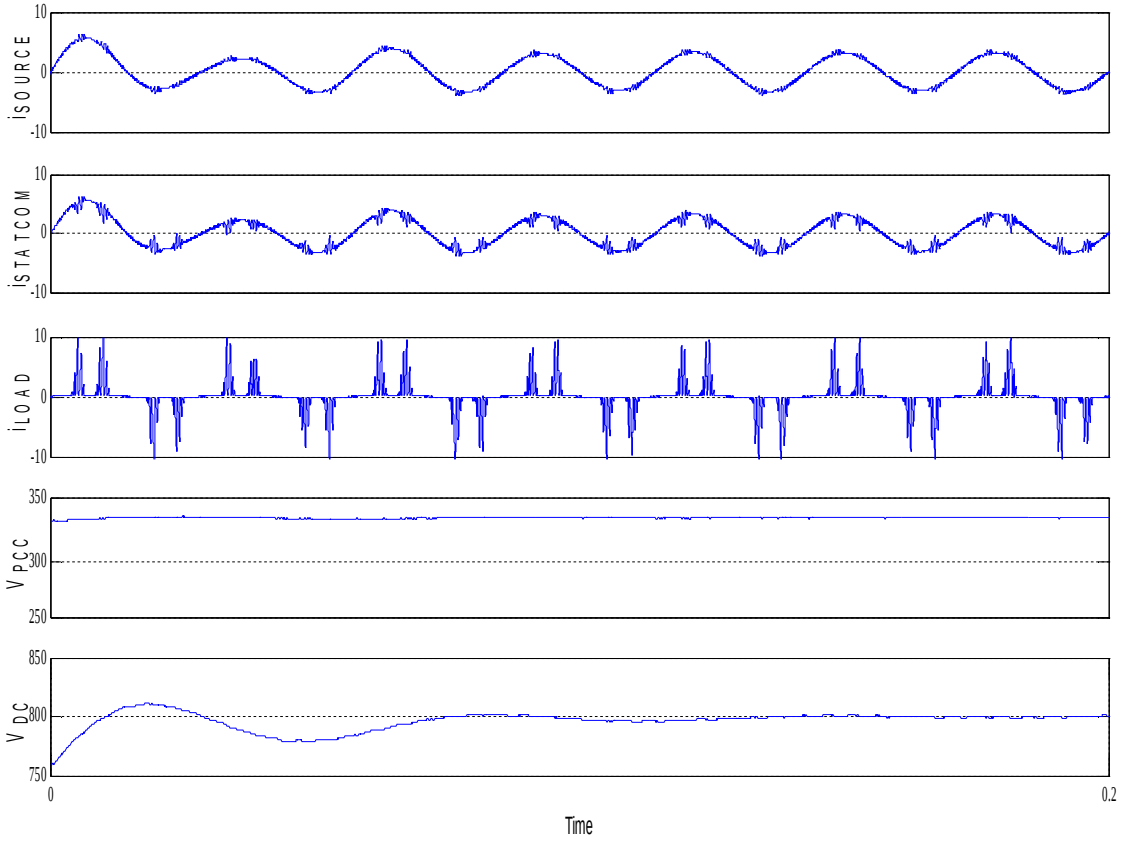

Fig.3.18 Results with DSTATCOM for a universal diode bridge with RLC load

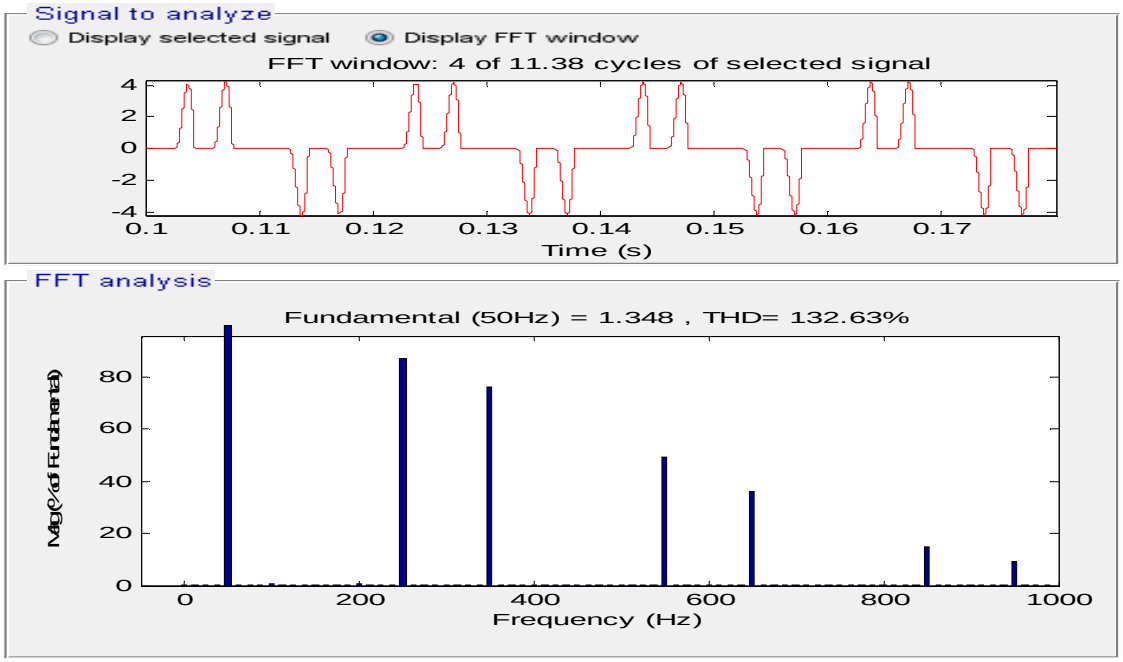

Fig. 3.19 Source current THD for a non linear RLC load without DSTATCOM

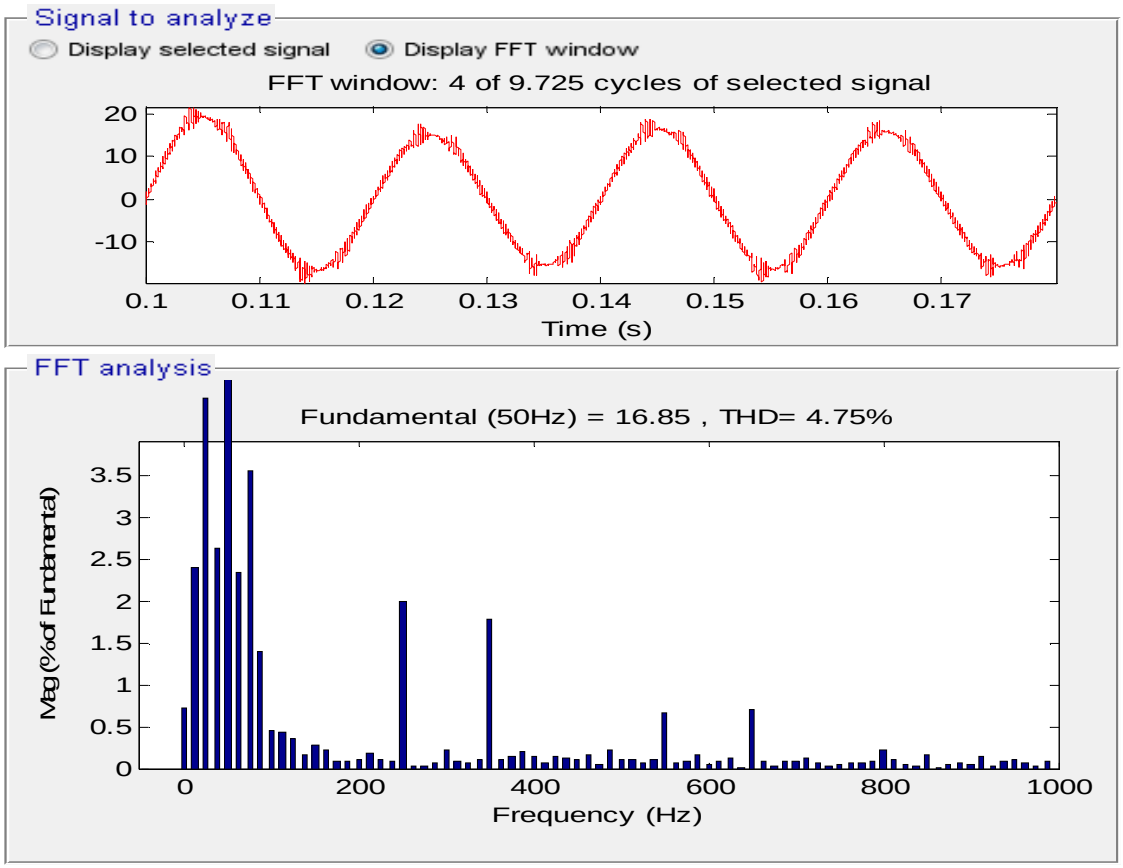

Fig. 3.20 Source current THD for a non linear RLC load with DSTATCOM

Table 3.1 Comparison of THD analysis for different non-linear loads

Universal diode bridge with	THD without DSTATCOM	THD with DSTATCOM
R	29.35%	3.26%
RL	29.65%	3.05%
RLC	132.63%	4.75%

3.3.3 Unbalanced Load

In this case a unbalanced load is taken with different values of impedance across each phase.

Phase R: R= 70 Ω, L= 200mH

Phase Y: R= 100 Ω, L= 225mH

Phase B: R = 50 Ω, L= 175mH

Fig 3.21 shows the response of system with unbalanced load. It is observed that the load currents are unequal as the load impedance for all the 3 phases is different.However, with the installation of DSTATCOM, the supply currents are sinusoidal balanced and 120^0 phase displaced.The Dc link voltage is regulated to its reference value of 800 V using PI controller. The PCC voltage also improves after installation of DSTATCOM. Results after installation of DSTATCOM is shown in Fig 3.22.

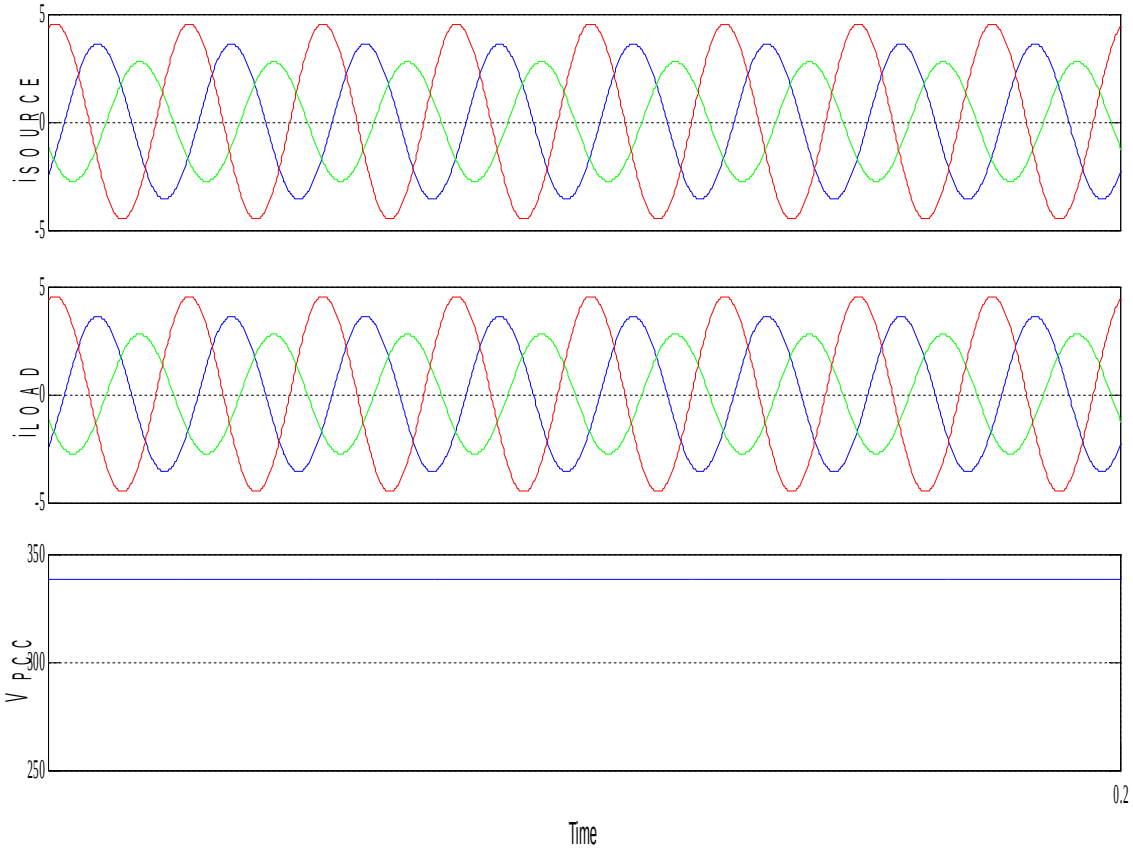

Fig. 3.21 Results in unbalanced condition without DSTATCOM

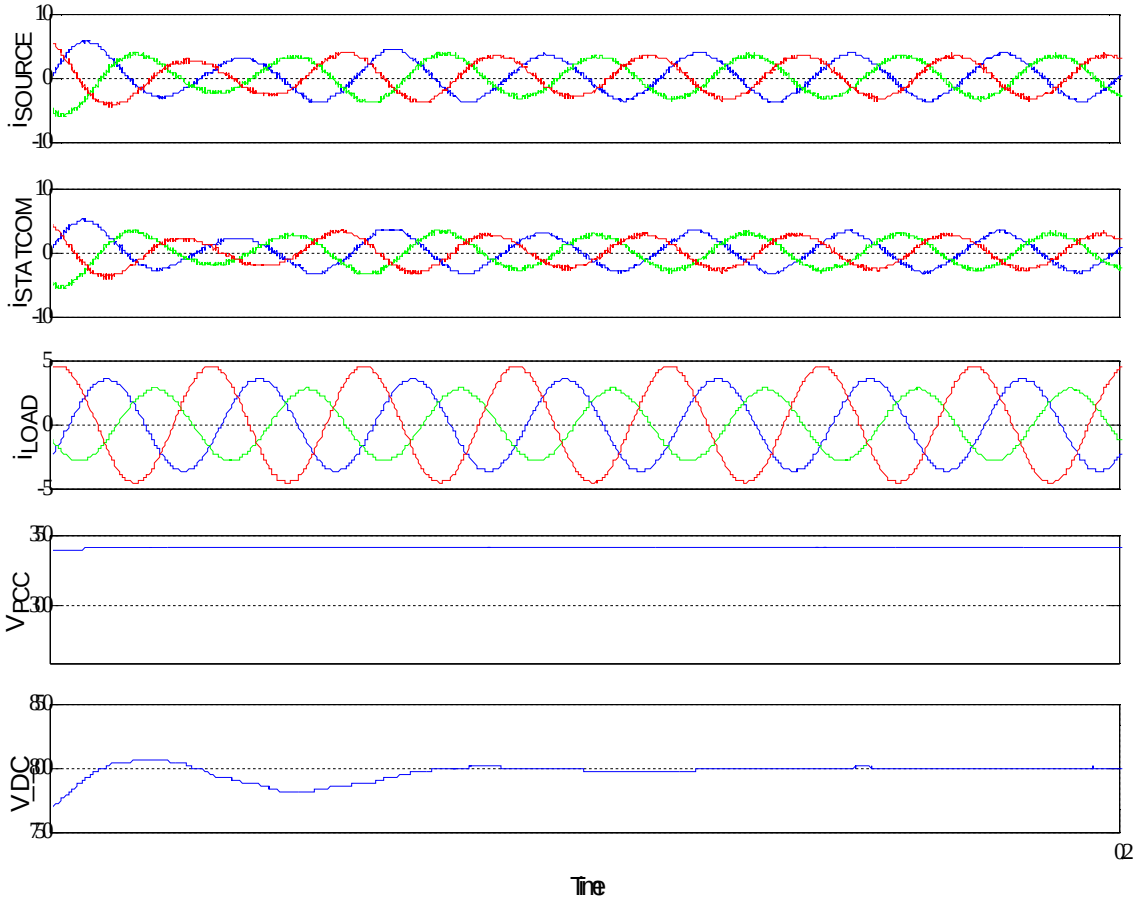

Fig. 3.22 Results in unbalanced condition with DSTATCOM

3.4 Dynamic Performance of DSTATCOM

Voltage sag is the major problem which occurs in distribution systems due to dynamic load changes, non linear loads, unbalance loading etc. DSTATCOM is used in distribution systems to mitigate these problems. The performance of DSTATCOM is tested under dynamic load changes.

3.4.1 Dynamic Linear Load Change

In this case a 3-phase series RL load drawing active power component 20kW and reactive power component 10kVAR is considered. Another linear 3-phase series RL load is switced on for a duration of 0.2 sec between 0.2 and 0.4 sec. The additional load draws active power component of 10kW and reactive power of 10kVAR. Fig 3.23 shows the response of system with load

change. It shows the plots of supply currents (i_{source}), DSTATCOM currents ($i_{statcom}$), Load currents (i_{load}) and the voltage at PCC (V_{PCC}) w.r.t time. At t= 0.2 sec as load is increased, there is a voltage dip in PCC voltage which remains upto t= 0.4 when the load is decreased to its previous value. DSTATCOM is able to regulate PCC voltage and DC link voltage to their reference values as shown in Fig 3.24. The figure shows the plots of supply currents (i_{source}), DSTATCOM currents ($i_{statcom}$), Load currents (i_{load}), PCC voltage (V_{PCC}) and DC link voltage (V_{DC}) w.r.t time.

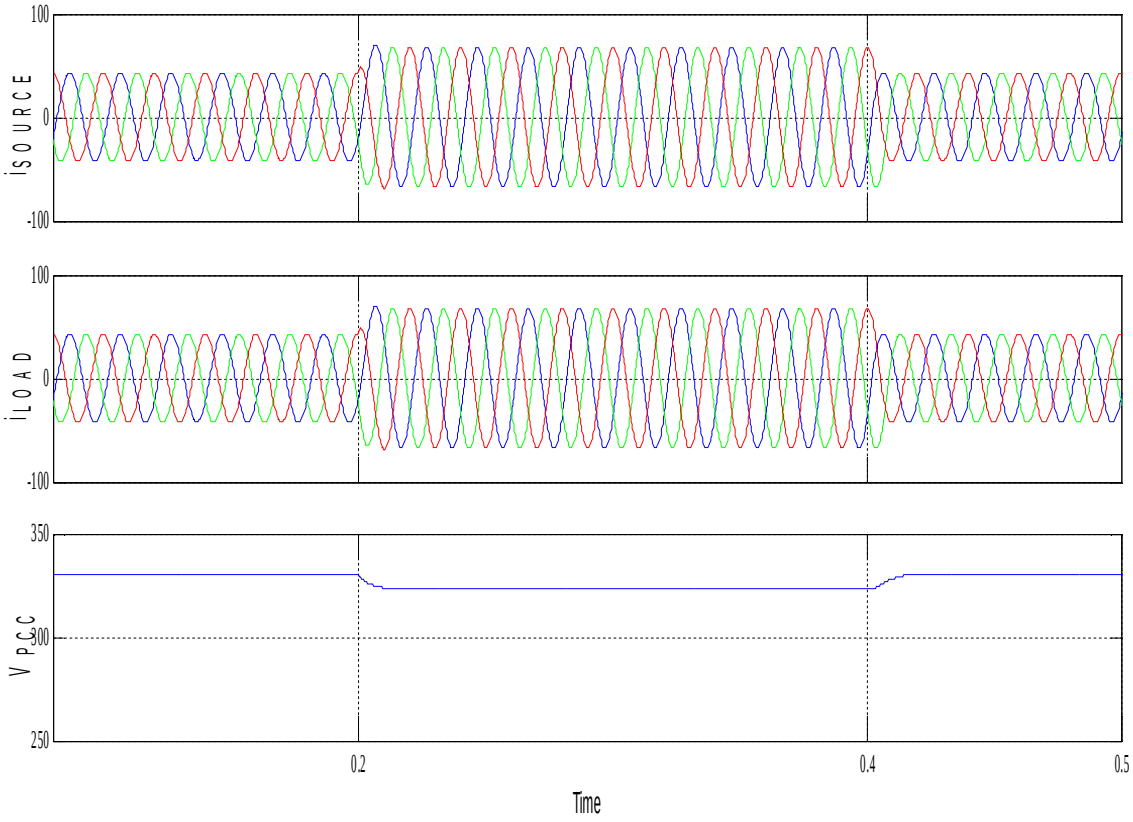

Fig 3.23 Results without DSTATCOM for change of load

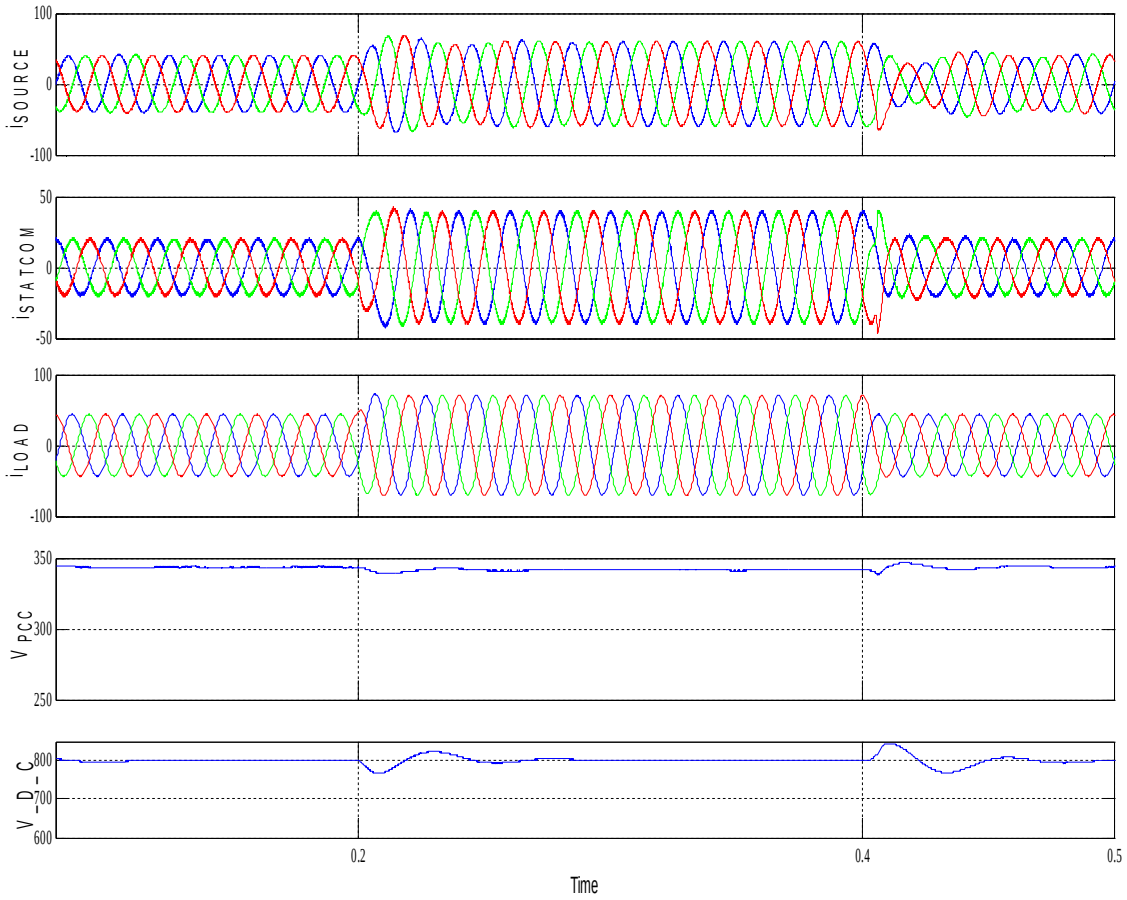

Fig 3.24 Results with DSTATCOM for change of load

3.4.2 Phase-out Condition

Sometimes in distribution systems voltage swell occurs due to phase out condition. In this case a similar condition is created by taking out 'R' phase from the system for a time of 0.2 sec between 0.2 and 0.4 sec. Another phase 'Y' is taken out for a duration of 0.06 sec between 0.28 and 0.34 sec. The effect of DSTATCOM is monitored under phase out condition. Fig 3.25 shows the response of system with phase out. It shows the plots of supply currents (i_{source}), DSTATCOM currents ($i_{statcom}$), Load currents (i_{load}) and the voltage at PCC (V_{PCC}) w.r.t time. When the single phase 'R' is taken out at 0.2 sec, the PCC voltage swells and unbalancing occurs in source current. After a delay of 0.08 sec another phase 'B' is taken out for duration of 0.06 sec, more amount of swell is seen in the PCC voltage. When the DSTATCOM is installed in the system the PCC voltage level maintains at the reference value and the source currents also becomes sinusoidal. Fig 3.24 shows the response of system with DSTATCOM. It shows the

plots of supply currents (i_{source}), DSTATCOM currents ($i_{statcom}$), Load currents (i_{load}), PCC voltage (V_{PCC}) and DC link voltage (V_{DC}) w.r.t time. DC link voltage is also regulated at its reference value of 800 V.

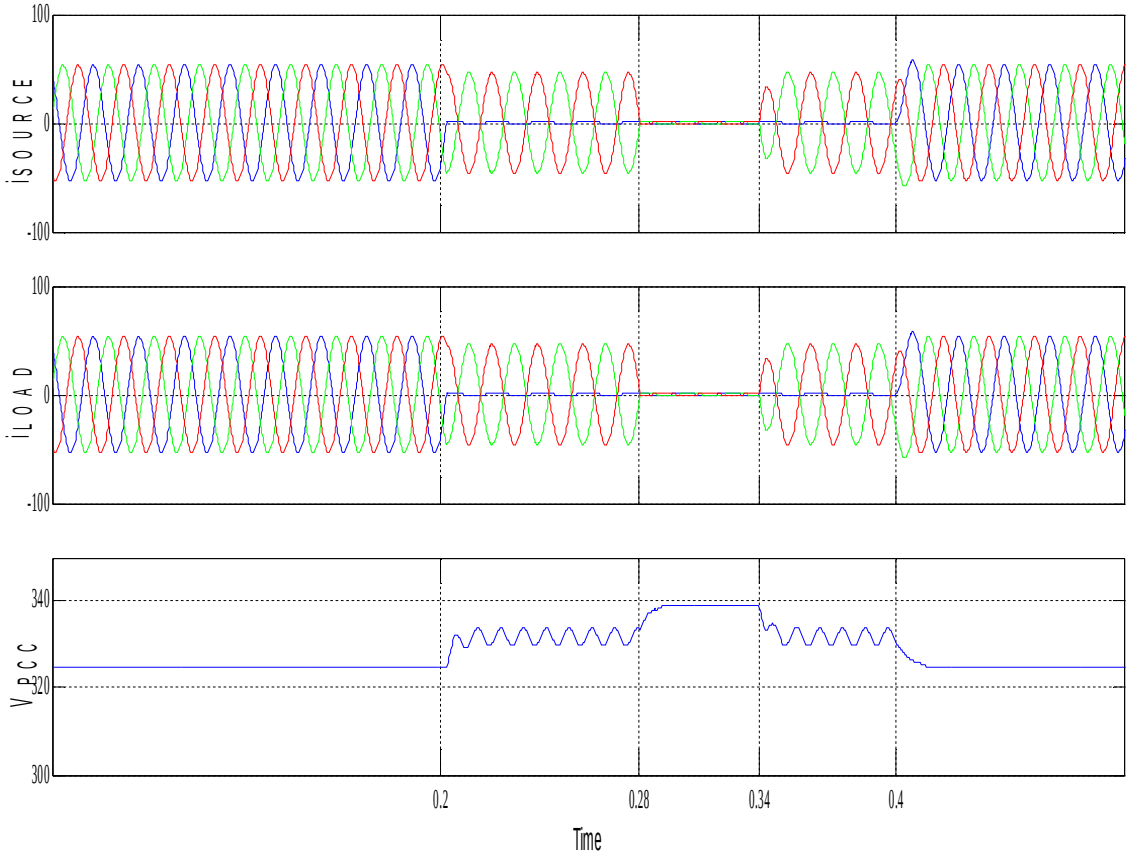

Fig. 3.25 Results without DSTATCOM in Phase-out condition

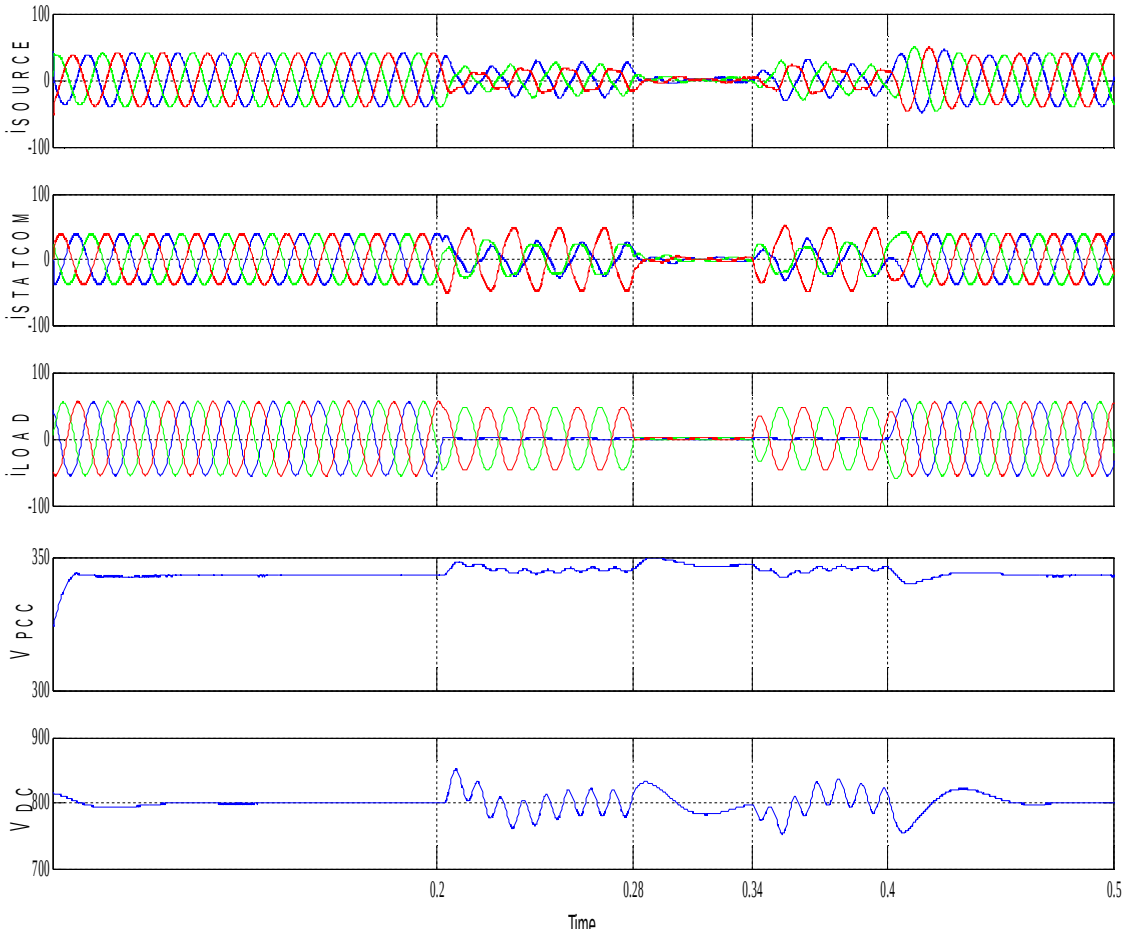

Fig. 3.26 Results with DSTATCOM in Phase-out condition

3.5 Battery Energy Storage System (BESS)

The loads are fluctuating in case of distribution systems. BESS is used for delivering the extra amount of active and reactive power required by the load such that the source currents become sinusoidal and the PCC voltage is maintained at its reference value. The performance of BESS is tested under dynamic linear load change condition for maintaining the source currents constant and equal sharing of active power between source & BESS. SRF algorithm is used for control of BESS. The configuration of BESS as shown in Fig 3.27 consists of a battery at the DC link; hence the DC link voltage remains constant. A DC battery (800 V) has a linked small series resistance (R_1) connected in with a parallel combination of a resistor (R_2) and a large capacitor (C_2). A DC link capacitor (C_1) is also connected as shown. The parameters values are shown in the appendix.

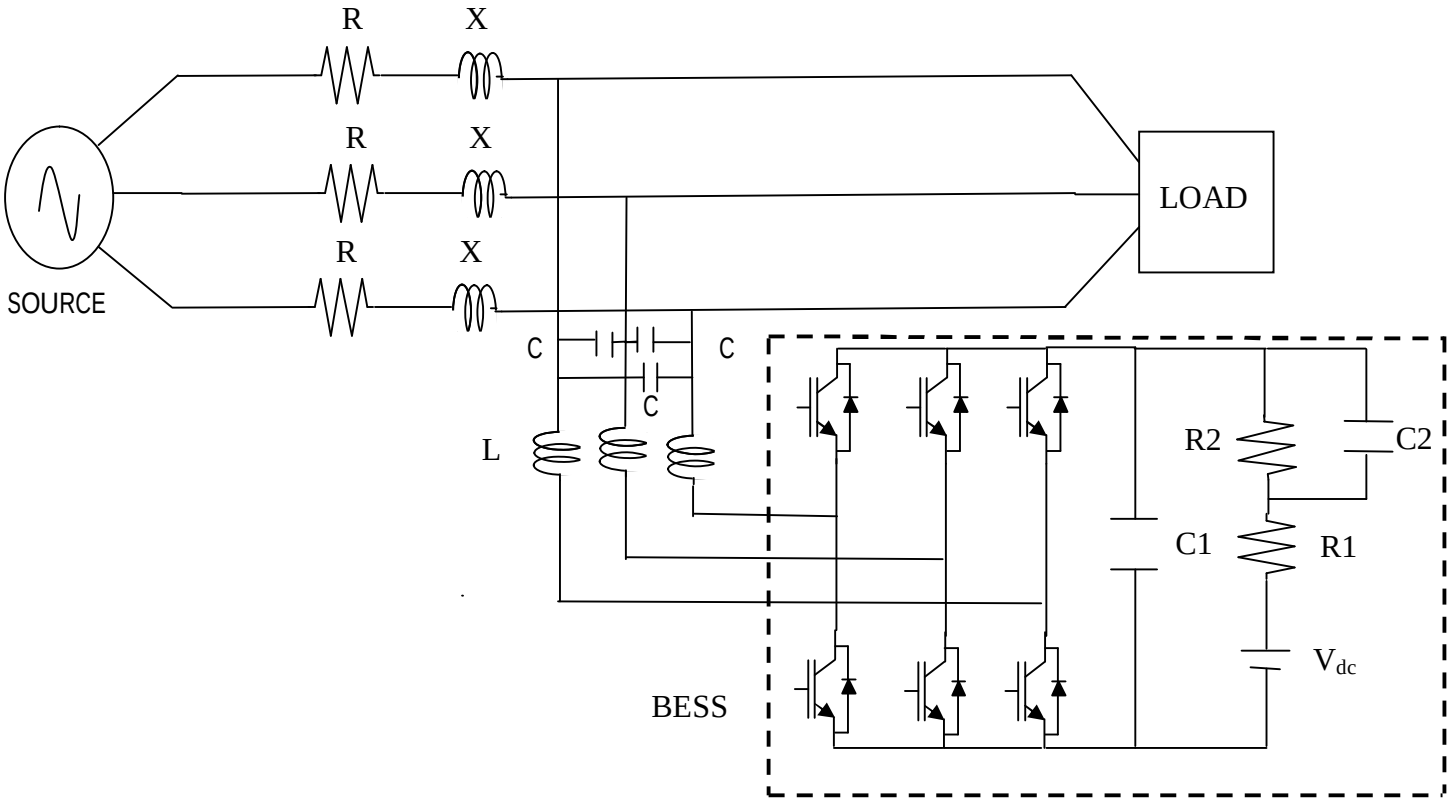

Fig 3.27 Schematic diagram of system with BESS connected in shunt configuration

A. Equal Sharing of Active Power

In this case a 3-phase series RL load drawing active power component 20kW and reactive power component 10kVAR is considered. Another linear 3-phase series RL load is switced on for a duration of 0.1 sec between 0.15 and 0.25 sec. The additional load draws active power component of 10kW and reactive power of 10kVAR. Fig 3.28 shows the response of system with load change. It shows the plots of supply currents (i_{source}), DSTATCOM currents ($i_{statcom}$), Load currents (i_{load}), PCC voltage (V_{PCC}) and Dc link voltage (V_{DC}) w.r.t time. The amount of active power required by the load is equally shared by the source and BESS as shown in Fig 3.29. The total reactive power is delivered by the BESS and the controller is tuned to maintain the PCC voltage and DC link at their reference values of 339 V and 800 V respectively. At t= 0.15 sec, as

load is increased the additional active power required by the load is also equally shared by the source and BESS. The additional reactive power is delivered by BESS. Fig 3.29 shows the plots of active and reactive powers delivered by the source and BESS.

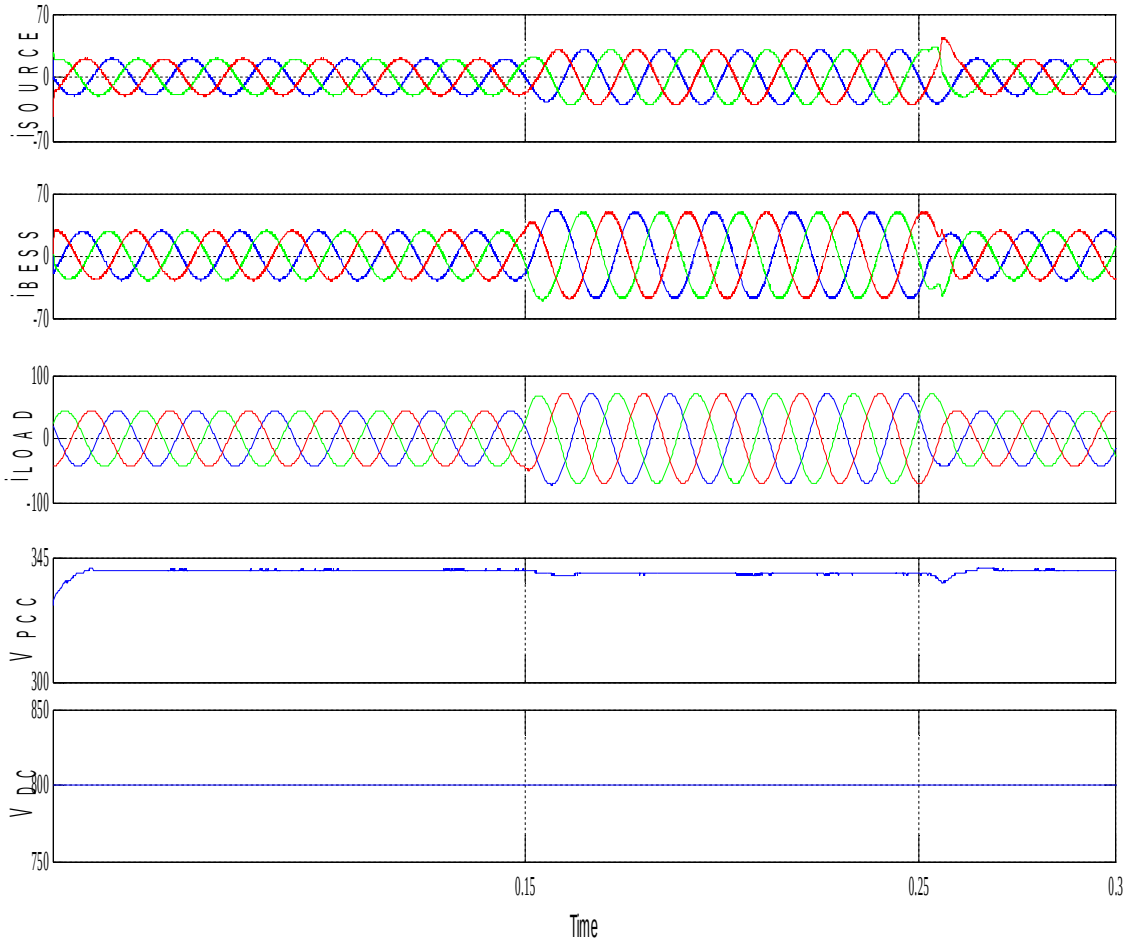

Fig 3.28 BESS Equal Active Power Sharing Results

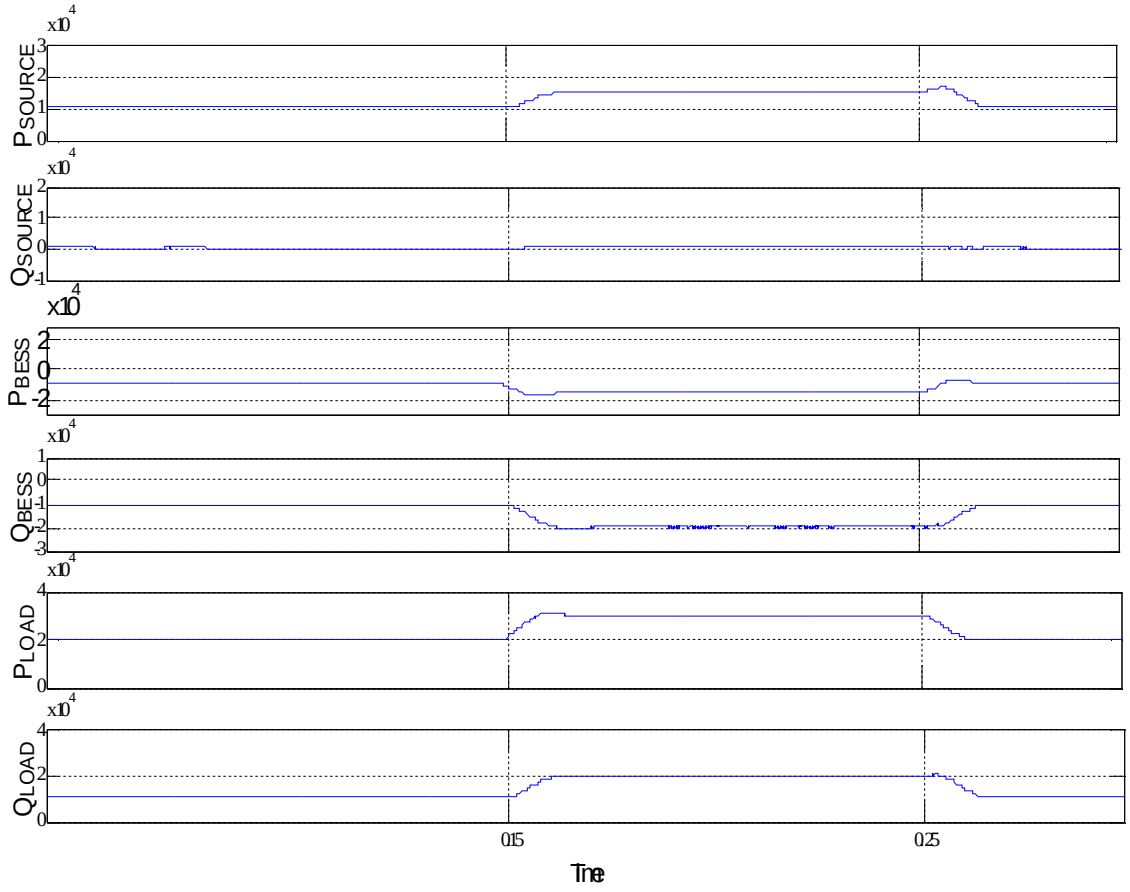

Fig 3.29 BESS Equal Sharing Power Results

B. Constant Source Power

In this case a 3-phase series RL load drawing active power component 20kW and reactive power component 10kVAR is considered. Another linear 3-phase series RL load is switched on for a duration of 0.1 sec between 0.15 and 0.25 sec. The additional load draws active power component of 10kW and reactive power of 10kVAR. Fig 3.30 shows the response of system with load change. It shows the plots of supply currents (i_{source}), DSTATCOM currents ($i_{statcom}$), Load currents (i_{load}), PCC voltage (V_{PCC}) and Dc link voltage (V_{DC}) w.r.t time. The amount of active power delivered by the source is maintained constant at10kW, while the additional active (10kW) and reactive power (10kVAR) is supplied by the BESS as shown in Fig 3.31. The PCC voltage and DC link are regulated at their reference values of 339 V and 800 V respectively. Fig 3.31 shows the plots of active and reactive powers delivered by the source and BESS. The supply currents have a peak amplitude of 45A which is maintained constant.

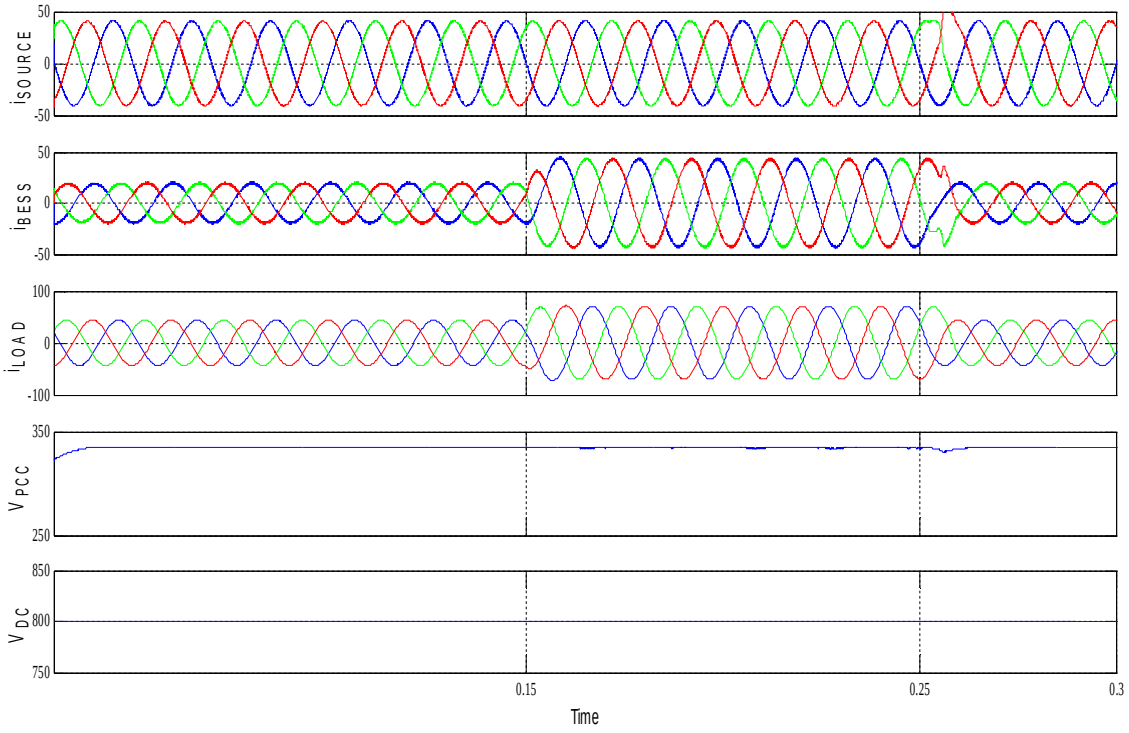

Fig 3.30 BESS Constant Source Current Results

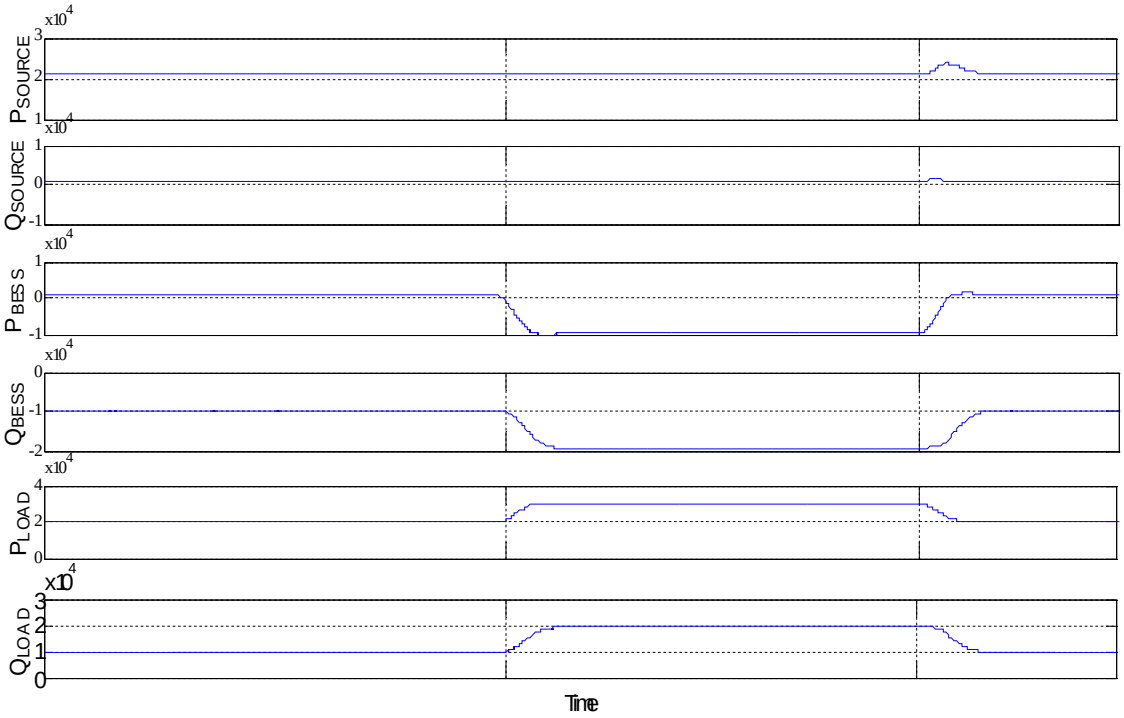

Fig 3.31 BESS Power Results for Constant Source Power

CHAPTER- 4

CONCLUSIONS

1. In this work Power Quality (PQ) problems such as harmonics, voltage sag, voltage swell etc have been studied and some of the solution (Custom Power Devices such as DSTATCOM, DVR and UPQC) for improving these problems also have been studied.
2. DSTATCOM has been modeled and simulated in MATLAB environment. Two different control algorithms namely SRF and IRPT have been studied and SRF theory was found to be better as compared to IRPT.
3. The performance of DSTATCOM has been analyzed for linear and non-linear loads under steady state as well as dynamic conditions. DSTATCOM has been found to regulate PCC voltage under varying load condition and load unbalancing. The performance of DSTATCOM with non-linear loads is found to be satisfactory and is able to reduce the supply current THD to less than 5% level as per IEEE 519 standards, even when the load current THD is as high as 132%.
4. BESS has been modeled and simulated for real as well as reactive load sharing. The performance results of BESS with equal load sharing and constant source current under dynamic load conditions are satisfactory.

CHAPTER-5

SCOPE OF FUTURE WORK

In this work it is shown that DSTATCOM and BESS can regulate the PCC voltage to its reference value under different load conditions. The work can be expanded in the following area:

1. DVR can be modeled for protecting sensitive loads from the distortion in the supply side voltage.
2. UPQC can also be studied for providing series and shunt compensation at the same time.
3. DSTATCOM applications in wind turbine generator and isolated diesel generator system can be studied.
4. Various control algorithms for DSTATCOM control can also be studied.
5. Application of DSTATCOM to improve distribution system performance with balanced and unbalanced fault conditions can also be considered in future work.