CHAPTER 1 INTRODUCTION

1.1 INTRODUCTION

Dynamic logic has been very widely used. This logic family offers a various arousing features compared to static logic, especially reduced transistor count almost half compared to static logic as well as lower load capacitance and hence improved speed [1].

Dynamic logic circuit is the main digital circuits, with a clock as a controlling signal. Comparing with the complementary logic circuit which is having both Pull-up and Pull-down network, dynamic logic circuit has only one network. Dynamic logic circuits consume nearly half of the transistor count as well as the layout area [5–7]. Parasitic capacitances are used to stored the voltage at the output of the dynamic node , which is typically buffered before it is sent to the next stage. This voltage is affected by the charge sharing. Advantage of dynamic logic circuit is having smaller area and higher speed. According to the theory, the dynamic logic circuit will uses precharge and evaluation phases of the clock cycle. During the precharge phase, a lot of extra noise are introduced into the system compared with the static logic circuit[9]. A noticeable amount of power is waisted due to these periodic precharge phases.

Here we propose a Low power pseudo dynamic buffer structure for the dynamic logic circuit. Using this dynamic buffer structure, the precharge pulse is obstructed at the input of the dynamic buffer and is supress from being propagated to the output of the dynamic gate. As a result, power typically consumed during the precharge phase is saved. According to the proposed structure will dramatically reduce the output noise as well as considerable power consumption compared to the traditional dynamic buffer circuits[8].

As the use of high performance battery operated system increased, the demand for low power blocks has also increased. With the clock frequencies approaching 1GHz and more,

the arithmetic blocks must keep pace with the continued demand for low power consumption. The purpose of this work is to present high speed with minimum power budget circuits which are the fundamental parts of various complex circuits. For footed domino logic circuit implementation, our proposed scheme has both complimented and non-complimented output, one of the main advantages of our scheme is that due to present of complimented output we can fabricate universal gates. The NAND and NOR gates are universal gates which can implement any Boolean function without need to use any other gate type.

1.2 CMOS CIRCUITS PERFORMANCE PARAMETERS

To compare the performance of CMOS Domino logic Topology Circuits following are the main parameters of interest.

1. Power dissipation
2. Propagation delay
3. Energy consumption (power - delay product)
4. Area

1.2.1 POWER DISSIPATION

The average power consumption in conventional CMOS digital circuits can be expressed as the sum of three main components, namely (1) dynamic (switching) power consumption, (2) the short-circuit power consumption, and (3) the leakage power consumption. If the system or chip includes circuits other than conventional CMOS gates that have continues current paths between supply and the ground, a fourth static power consumption should also be considered [9].

1.2.1.1 SWITCHING POWER DISSIPATION

This component represents the power dissipated during a switching event that is when the output node voltage of a CMOS logic gate makes a logic transition. In digital CMOS circuits, switching power is dissipated when energy is drawn from the power supply to charge up the output node capacitance. During this charge-up phase, the output node voltage typically makes a full transition from 0 to V_{dd} and one-half of the energy drawn from the power supply is dissipated as heat in the conducting PMOS transistors. Note that no energy is drawn from the power supply during the charge-down phase, yet the energy stored in the output capacitance during charge-up is dissipated as heat in the conducting NMOS transistors, as the output voltage drops from V_{dd} to 0 [9].

The switching power consumption is proportional to the load capacitance, supply voltage and clock frequency.

$$P_{avg} = V^{2}_{dd} * C_{load} * f_{clk} \quad (1.1)$$

where

P_{avg} = average switching power dissipation

C_{load} = load capacitance

V_{dd} = supply voltage

f_{clk} = clock frequency

1.2.1.2 SHORT-CIRCUIT POWER DISSIPATION

The switching power dissipation examined above is purely energy required to charge up the parasitic load capacitances in the circuit, and the switching power is independent on the rise and fall times of the input signals. When a CMOS circuit is driven by the input voltage waveforms with finite rise and fall times, both the NMOS and PMOS transistors in the circuit may conduct simultaneously for a short amount of time, the power

consumption during this short time called as short-circuit power dissipation. Power consumed because of the current flowing from power supply to ground during transistor switching [10].

1.2.1.3 LEAKAGE POWER DISSIPATION

The NMOS and PMOS used in a CMOS logic gate generally have nonzero leakage currents. The leakage power dissipation caused due to sub threshold leakage currents .As the threshold voltage of the device increases, sub threshold current decreases which cause to decrease the leakage power consumption [11].

1.2.2 PROPAGATION DELAY

The propagation delay of the circuit is used to determine the speed of the circuit. The delay is a function of the slopes of the input and output signals of the gate. The propagation delay times t_{phl} and t_{plh} determine the input to output signal delay during the high-to-low and low-to-high transitions of the output [9].

t_{PHL} is the time delay between the $V_{50\%}$ transition of the rising input voltage and the $V_{50\%}$ of the falling output voltage. Similarly, t_{PLH} is defined as the time delay between the $V_{50\%}$ transition of the falling input voltage and the $V_{50\%}$ transition of the rising output voltage. The earliest input signal which takes maximum propagation delay to reach the latest output is the critical path. The delay (in nanoseconds) is the period between the applying of input pattern and the availability of output. The propagation delay t_p is defined as the average of the two.

$$\mathbf{t_p = (t_{PLH} + t_{PHL})/2} \quad (1.2)$$

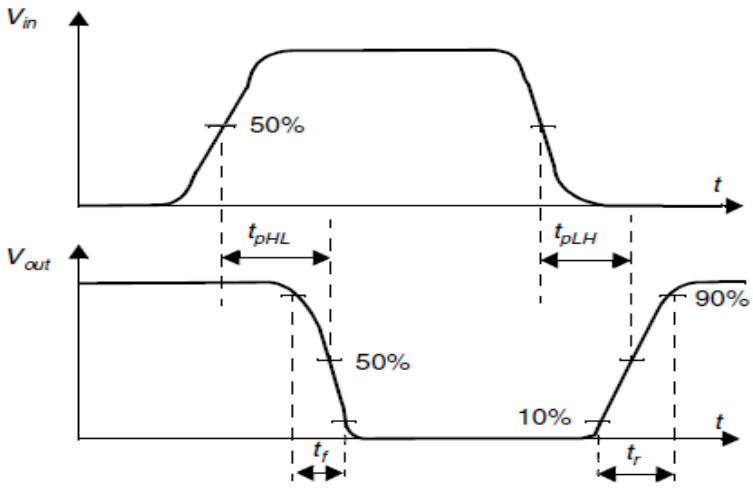

Fig 1.1 Wave forms to show propagation delay.

1.2.3 ENERGY CONSUMPTION (POWER - DELAY PRODUCT)

The power-delay product is a fundamental parameter which is often used for measuring the quality and the performance of a CMOS process and gate design. As a physical quantity, power delay product can be interpreted as the average energy consumed by a gate while switching its output from low to high and high to low.

This index serves as a better term to compare the power behaviors of two designs working at different frequencies.

1.2.4 AREA (NUMBER OF TRANSISTORS)

An objective in the design of digital VLSI circuits is to minimize silicon area per logic gate so as to have large number of gates per chip. Area reduction occurs in three different ways: through advances in processing technology that enables the reduction of the minimum device size, through advances in circuit design techniques, and through careful chip layout. Smaller devices, however, have lower current-driving capability, which tend to increase the delay.

1.3 ORGANIZATION OF THE THESIS

The thesis is organized as follows in chapter 2, we have gone through the conventional domino logic gate and previously proposed domino logic; in this we have discussed the working , advantage , disadvantage and problem of domino logic. In Chapter 3, proposed domino logic is discussed. Chapter 4, present simulations result, schematic, waveform, variation in power dissipation of various logic functions with different input. Chapter 5, gives the concluding remarks.

CHAPTER 2 CMOS DOMINO LOGIC

2.1 STANDARD DOMINO LOGIC

A standard footed domino gate is shown in Fig. [2.1]. It consists of a complimentary MOSFETS, NMOS logic and a static inverter, it uses clocking scheme and charge storage property of MOSFET to implement the logic functions [12].

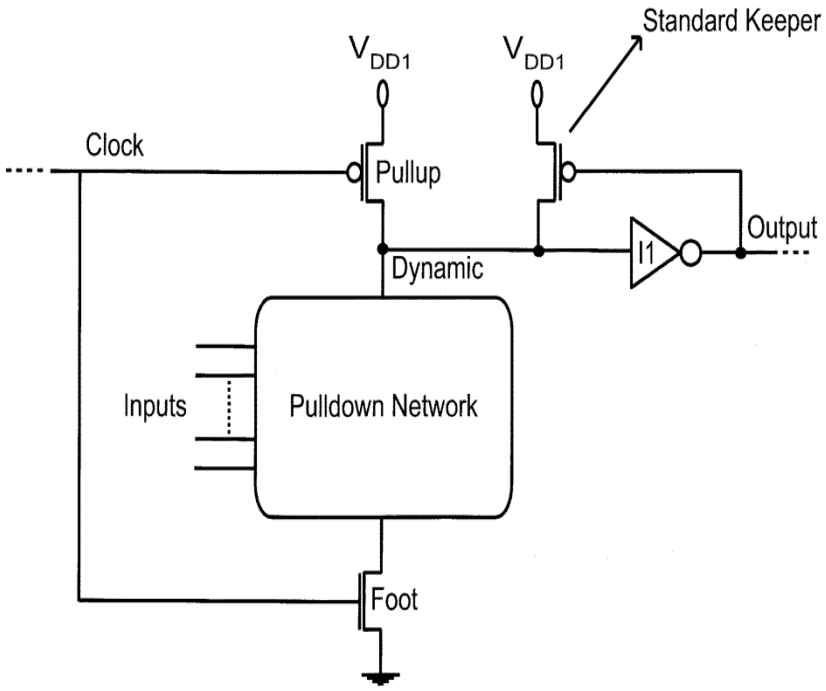

Fig. 2.1 Standard domino logic with keeper circuit**.**

The clock drives a complimentary pair of MOSFETS MP (pull-up) and MN (pull-down) these control the operation of the circuit and provide synchronization. The clocking

signal defines two different modes of operations precharge mode when clock is “0” and evaluation mode when clock is “1”.

2.1.1 PRECHARGE PHASE

When the clock signal is low, the domino logic circuit is in the precharge phase. During this phase, the dynamic node is charged to vdd by the pull-up transistor. The output transitions low, turning on the keeper transistor [12].

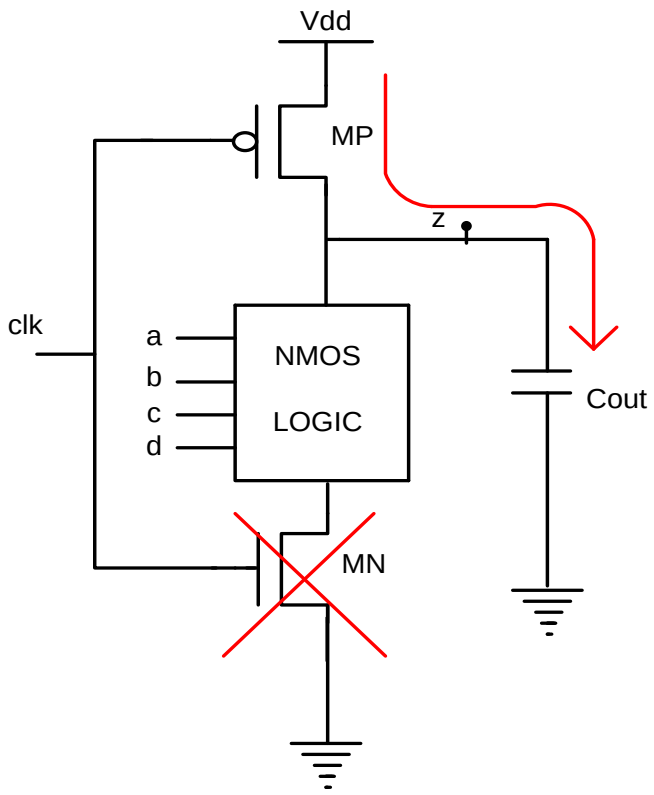

Fig. 2.2 Precharge phase of Standard domino logic circuit.

2.1.2 EVALUATION PHASE

When the clock transitions high, the circuit enters the evaluation phase. In this phase, provided that the necessary input combination to discharge the dynamic node is applied, the circuit evaluates and the dynamic node is discharged to ground. If the circuit does not

evaluate in the evaluation phase, the high state of the dynamic node is preserved against coupling noise, charge sharing, and subthreshold leakage current by the keeper transistor until the pull-up transistor is turned on at the beginning of the following precharge phase [12].

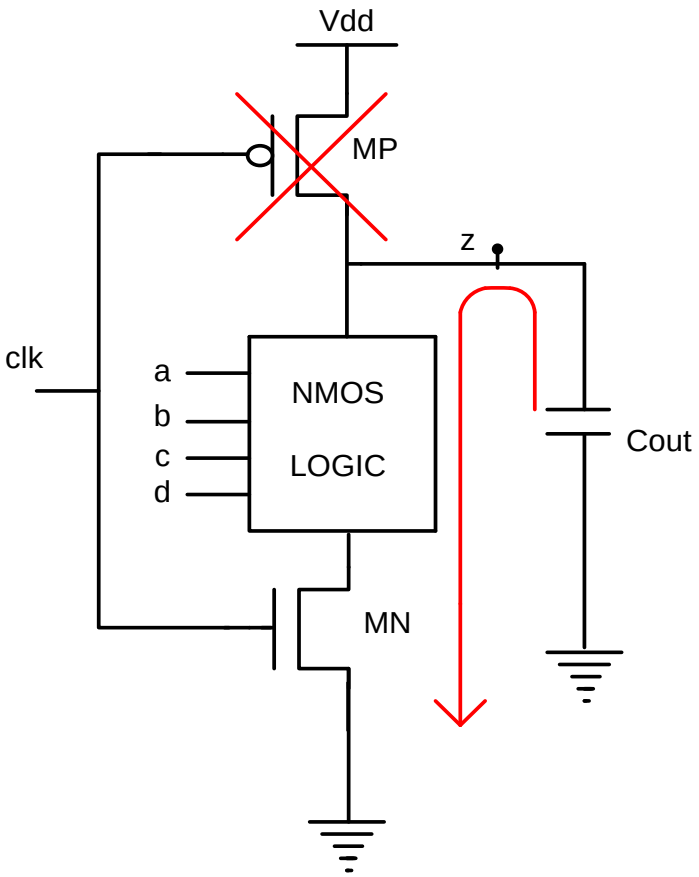

Fig. 2.3 Evaluation phase of Standard domino logic circuit.

The foot transistor (see Fig. 2.1) controlled by the clock signal divides the operation of a domino logic circuit into two distinct phases independent of the timing of the input signals. The isolation of the pull down network from ground in the precharge phase eases the relative timing of the input and clock signals in cascaded multistage footed domino circuits. If the necessary input combination to discharge the dynamic node is applied during the precharge phase, the pull-down transistors cannot alter the state of the dynamic node as the pull-down path to ground is blocked by the foot transistor. The foot transistor has a

nonzero resistance and parasitic capacitance that degrades the evaluation speed of a domino circuit. The foot transistor is typically sized significantly larger than the pull-down network transistors to minimize this speed degradation. Increasing the size of the foot transistor, however, increases the power dissipation since the foot transistor switches every clock cycle.

2.1.3 AND LOGIC OPERATION USING CONVENTIONAL DOMINO LOGIC

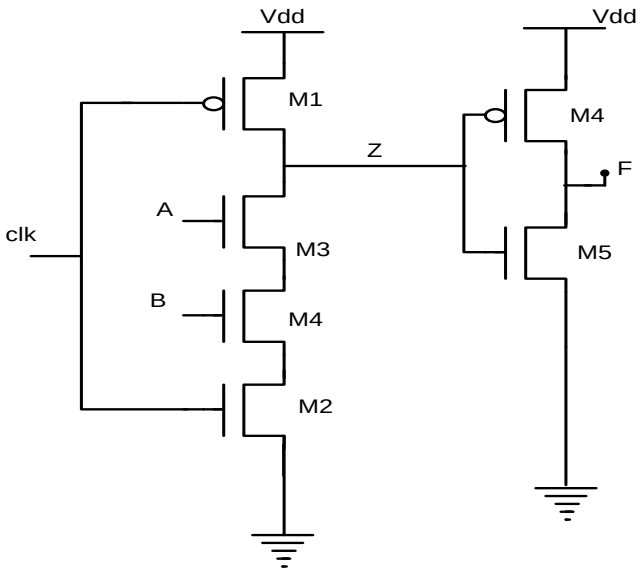

Fig. 2.4 A CMOS domino logic two-input AND gate.

The AND gate shown in Figure 2.4 can be used to illustrate the functionality, the speed advantage, and also some of the challenges involved in using this logic family. In Figure 2.4 it can be seen that the two functional inputs, A and B, are also attended by the clock signal, Clk. At first glance this may seem strange, since an AND gate should be a purely combinational circuit, which unlike latches and flip-flops does not require the presence of the clock signal. Domino logic is, however, a clocked logic family, which means that every single logic gate has a clock signal present. When the clock signal turns low, node Z (which is called the evaluation or internal node – some authors refer to it as the dynamic node) goes high, causing the output of the gate to go low. This represents the only

mechanism for the gate output to go low once it has been driven high. The operating period of the cell when its input clock and output are low is called the
precharge phase or cycle. The next phase, when the clock is high, is called the evaluate phase or cycle. During the evaluate phase the output of the domino AND cell can go high provided that both inputs A and B are high, which causes the evaluation node, Z, to be driven to a low value.

The evaluate phase is the functional operating phase in domino cells, with the precharge phase enabling the next evaluate phase to occur.

2.1.4 ADVANTAGE

The dynamic logic offers high speed due to small input capacitance. The static logic uses both PMOS and NMOS devices to construct a logic gate. On the other hand, the dynamic logic typically uses only NMOS devices for logic functions, and uses only one PMOS device per gate clocked for a precharge - evaluation style operation. For dynamic circuits, the structure itself leads to a small input capacitance and results in a short gate delay. The simple structure also attracts designers to implement a more complex function in a single gate, which facilitates the reduction of logic depth to earn more speed advantage.

2.1.5 DISADVANTAGE

The output logic is unstable during the precharge phase and as a result the cascading performance is limited and the propagation of the precharge pulse from dynamic node through the static buffer results in increased power consumption due to increase in switching activity.

2.1.6 PROBLEM STATEMENT

During every precharge phase the output pull down low regardless of input combination. The output is not stable during precharge phase. The power consumption significantly arises due to high switching activity of the dynamic circuit.

2.2 SOURCE OF POWER CONSUMPTION

The CMOS circuits both digital and analog consume more and more power as millions of transistors are integrated into a single chip. The sources of power consumption [9] in the CMOS can be classified into four parts as shown in Eq. (2.1).

$$P_{avg} = P_{dynamic} + P_{short} + P_{leakage} \tag{2.1}$$

(1) Dynamic/Active Power Consumption

(2) Short Circuit Power Dissipation

(3) Leakage power Dissipation

Where P_{avg} is the total power dissipation [16] in a CMOS circuit, $P_{dynamic}$ is the dynamic power, P_{short} is the short-circuit power, $P_{leakage}$ is the leakage power.

2.3 PSEUDO DYNAMIC BUFFER DOMINO LOGIC

The Pseudo dynamic Buffer (PDB) domino logic (reported logic) given by Fang Tang [8] overcomes this problem of precharge propagation using the circuit given in Fig. 2.5. In this topology of the buffer, the source of the buffer's NMOS transistor M5 is connected to node B instead of Gnd. Using such a circuit topology, the value at dynamic node Z cannot discharge during Precharge phase because, the evaluation transistor M2 is turned off and hence the output is not affected.

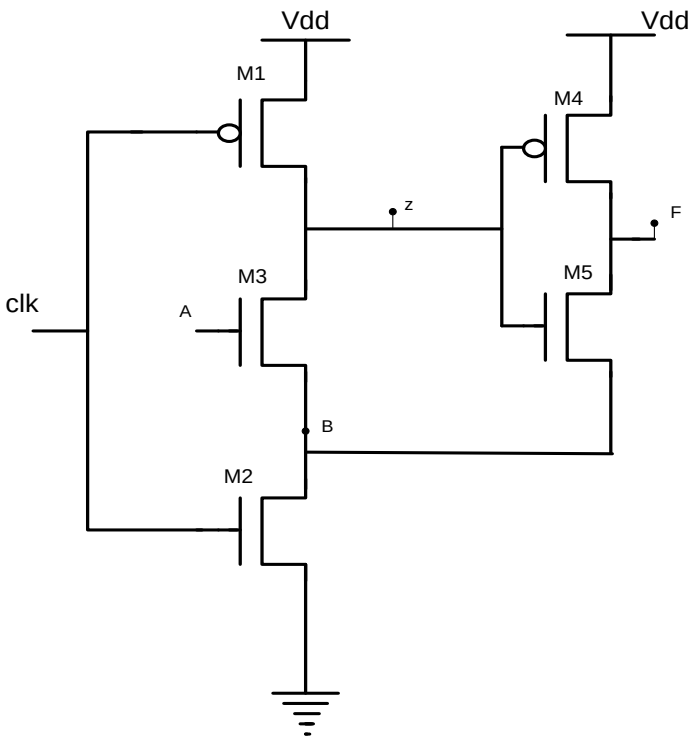

Fig.2.5 Domino logic circuit using the pseudo dynamic buffer.

For evaluation phase the discharging of the dynamic node will depend upon the input combination, hence the logic is maintain.

2.3.1 AND LOGIC OPERATION USING PDB-BASED DOMINO LOGIC

Figure 2.6 shows the schematic of two input AND logic using pseudo dynamic buffer domino logic system. In this scheme the source of the buffer's NMOS transistor M5 is connected to node B instead of Gnd. So, the value at dynamic node Z cannot discharge during the Precharge phase because, the evaluation transistor M2 is turned off and hence the output is not affected.

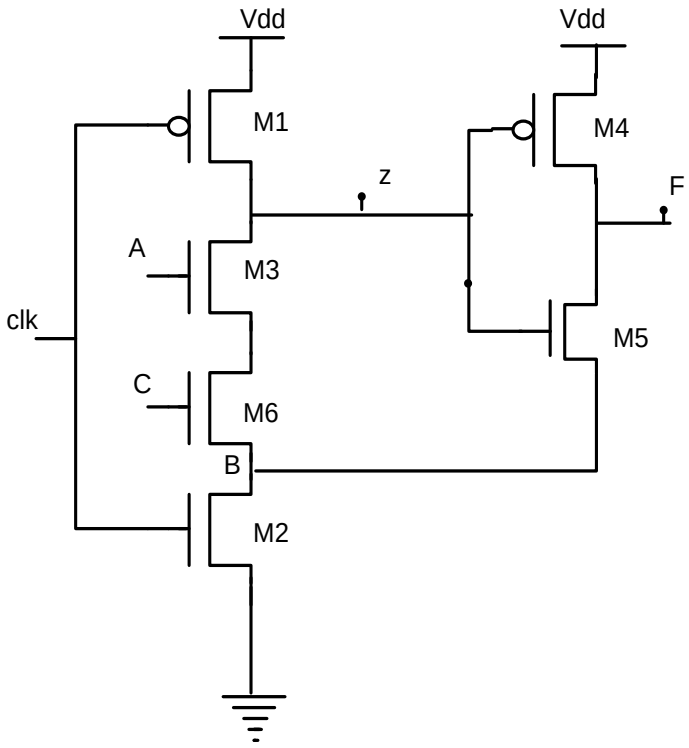

Fig. 2.6 AND logic circuit using the pseudo dynamic buffer.

For PDB AND domino Logic, when the inputs logic A and C are low, the floating node Z is always high and then, the output node F is kept low regardless of the operating phase. On the other hand, if the input A and input C are high, during the evaluation phase, node Z is discharged to Gnd as well as node B, resulting in enabling the PMOS transistor M4, while pulling up the output F to V_{dd}. During the Precharge phase, node Z is charged up to V_{dd}, followed by the voltage at node B. Since the NMOS evaluation transistor M2 is disabled, the output node Z is held high (same value as the previous evaluation phase).

The simulated output waveform of 2-input PDB-based AND domino logic is given in Fig 2.7, the output is high only for the time period when both the inputs are high verifying the AND logic.

Power consumption analysis in the PDB domino logic [8], the precharge pulse is prevented from propagating to the output node of the buffer, resulting in a decreasing current consumption in the output stage of the domino gate.

Fig 2.7 Output waveform of 2-input PDB AND domino logic.

Ideally, if the precharge pulse propagating is completely prevented and the input logic is fixed to‘1’, the power saving Z of the proposed scheme compared to conventional domino logic can be approximately given as

$$\eta = \frac{P_{total} - P'_{total}}{P_{total}} \tag{2.2}$$

The power saving of this scheme comes from reducing the output node activity. Typically there are three limits which can degrade the power saving. The first one is the logic activity rate. The power saving is maximized when it is fixed to‘1’, because the output node F is also fixed to‘1’and capacitors C_{buf} and C_{load} are not be charged. When the logic activity is increased, the output stage consumes more power and as a result, the power saving of the proposed scheme is reduced. The second non-ideal restriction is due to the internal capacitance. In the conventional scheme, the NMOS transistor’s source of the output stage is always connected to ground. Therefore, the parasitic capacitor in this source

node does not consume power. However, in the proposed domino scheme, the capacitance of node B consists of the parasitic capacitors of both the first stage NMOS transistors and the output stage NMOS transistor. As a result, the cap load in this scheme is increased leading to larger power consumption. The third limit is the charge sharing, which is mainly generated due to a finite clock slew rate. During the clock transition from‘1’to‘0’, the voltage at node B will be charged from both node Z and node F, leading to a output charge sharing.

2.3.2 AND LOGIC OPERATION WITH KEEPER CIRCUIT USING PDB-BASED DOMINO LOGIC

To overcome the problem of charge sharing keeper circuit is used [13], shown in fig 2.8. It consists of an inverter and a PMOS transistor connected to the output node.

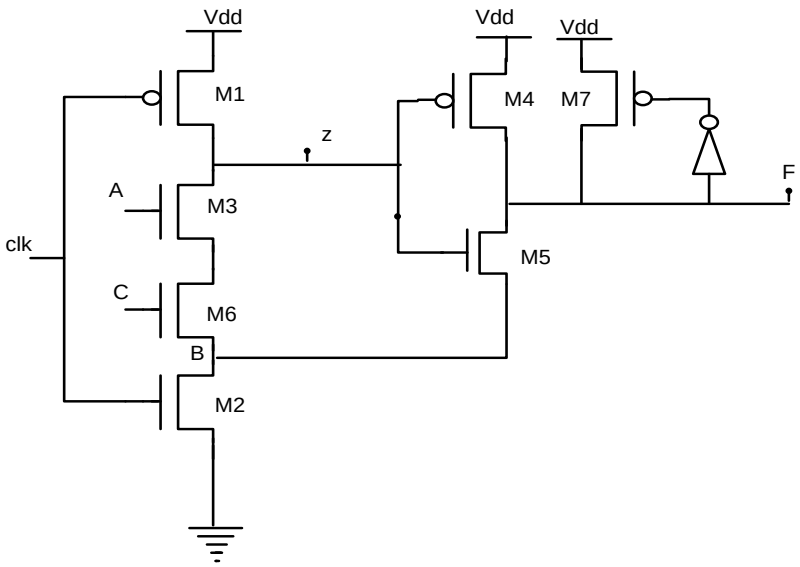

Fig 2.8 Pseudo dynamic buffer AND logic circuit with keeper Circuit.

When the output node (F) is high, the output of keeper inverter is low which turn on the keeper PMOS transistor and the output node is charged up to VDD. Using the keeper circuit the problem of charge sharing is removed but the power consumption of the circuit increases due to increase in extra transistors.

CHAPTER 3 PROPOSED CMOS DOMINO LOGIC

3.1 INTRODUCTION

In the proposed implementation of the buffer, the transistor M4 is connected between dynamic node-Z1 and transistor M6, the drain of transistor M4 is connected to dynamic node-Z1 and source of transistor is connected to Gate of transistor M6 and input of transistor M4 is clock pulse.

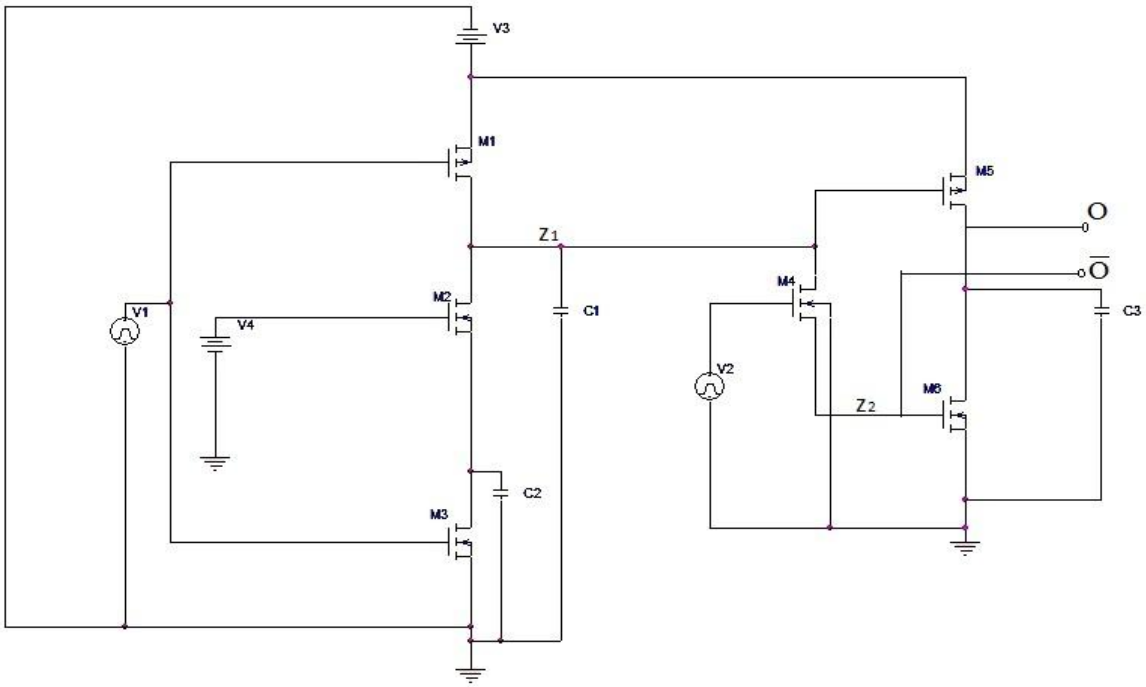

Fig. 3.1 Domino logic buffer circuit using the proposed domino logic.

Using this topology the value of node-Z1 cannot propagate to output O during Precharge phase since both transistors M4 and M5 are OFF. Advantage of this topology is that complimented output is also available at the source of transistor M4, as shown in Fig.3.1.

3.2 IMPLEMENTATION OF AND/NAND LOGIC USING PROPOSED SCHEME

Fig. 3.2 shows schematic of AND/NAND logic gates using proposed method of Domino logic system. When the clock signal is low, the dynamic logic circuit is in the precharge phase. During this phase, the dynamic node (Z_1) is charged to V_{dd} by the pull-up transistor (M1). And when the clock signal is high, the circuit enters into the evaluation phase. In this phase, dynamic node is discharged according to the input combination, the circuit evaluates and the dynamic node is discharged to ground.

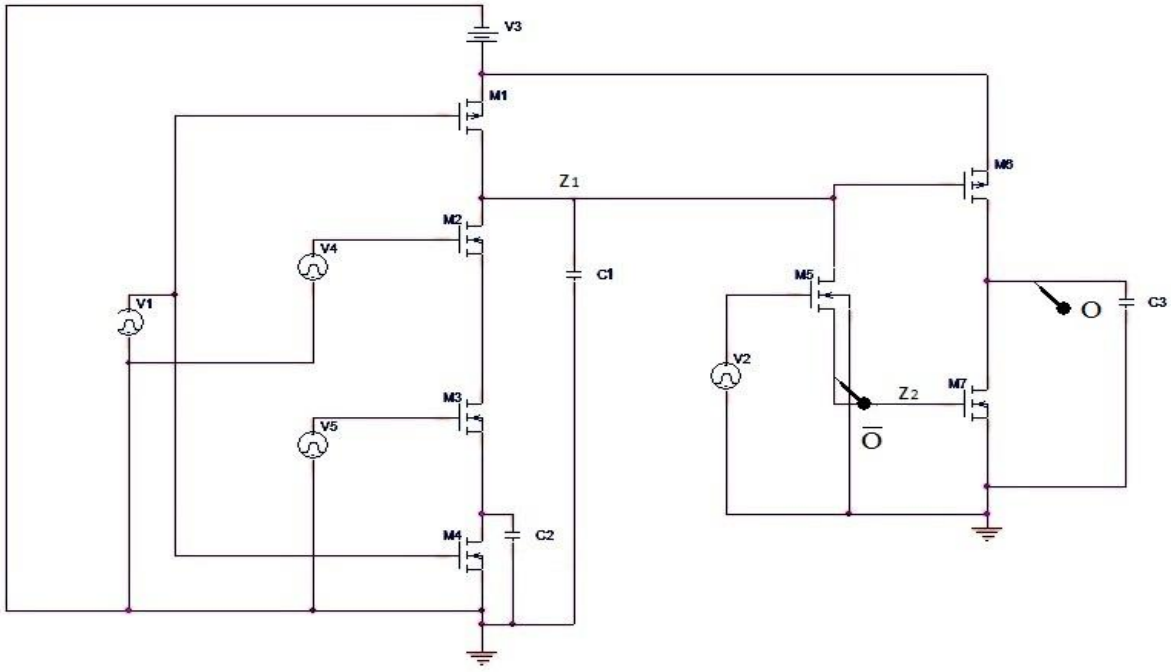

Fig. 3.2 Two-input AND/NAND Domino logic using proposed Logic.

The operation of the above circuit depends upon the input pulse V4 and V5. When both the input V4 and V5 are low, the value at dynamic node-Z_1 become high during Precharge phase. Now during evaluation phase transistor M1 is OFF and M4 is ON but node Z_1 will not discharge through M2 since it is OFF but will discharge through M5. Due to this node Z_2 becomes high which turns ON the transistor M7 and hence output O becomes low while output $\bar{O}$ high.

When both the input V4 and V5 are high, during evaluation phase the dynamic node Z_1 become low enabling the transistor M6 to be ON, the output is pulled up to V_{dd} through transistor M6. During Precharge phase, the transistor M1 get ON and M5 get OFF turning OFF the transistor M7, the value at the dynamic node Z_1 has no path to discharge since foot transistor M4 is also OFF, so the output is unaffected and maintain its previous value, i.e. high and since transistor M6 is OFF the value at node-Z_1 is not propagated to node-Z_2 and node-Z_2 is low, so for the both phases we are getting output at O and complimented output at node Z_2 independent of low value of clock pulse.

3.3 POWER CONSUMPTION ANALYSIS

Power consumption analysis [8] in the proposed domino logic, the precharge pulse is prevented from propagating to the output node of the buffer, resulting in a decreasing current consumption in the output stage of the domino gate. Ideally, if the precharge pulse propagating is completely prevented and the input logic is fixed to'1', the power saving of the proposed scheme compared to conventional domino logic can be approximately given as

$$\eta = \frac{P_{total} - P'_{total}}{P_{total}} \tag{3.1}$$

The power saving of the proposed scheme comes from reducing the output node activity. Typically there are two limits which can degrade the power saving. The first one is

the logic activity rate. The power saving is maximized when it is fixed to‘1’, because the output node O is also fixed to‘1’. When the logic activity is increased, the output stage consumes more power and as a result, the power saving of the proposed scheme is reduced.

As discussed in chapter 2 that the dynamic power [9] possesses large portion of power dissipation in the total circuit power consumption. The dynamic power is the result of charging and discharging the parasitic capacitances of the circuit and a quadratic function of the supply voltage (V_{dd}). The dynamic power can be expressed as Eq. (3.2).

$$P_{dynamic} = \alpha_T * C_l * V_{dd}^2 * f_{clk} \tag{3.2}$$

Where α_T is the switching activity factor, C_l is the loading capacitance, and f_{clk} is the operating frequency. The Eq. (3.2) suggests the four parameters that we can apply to reduce the dynamic power consumption in the system. . The proposed low power design techniques reduce the dynamic power dissipation based on switching activity reduction.

3.3.1 SWITCHING ACTIVITY REDUCTION

The output of conventional domino buffer is given in Fig. 3.3(a) in the figure there are unwanted transition from 0 to 1 and from 1 to 0, these unwanted transition consume power. The switching activity factor α_T for conventional buffer output is 2 per clock pulse hence the power consumption increases [9].

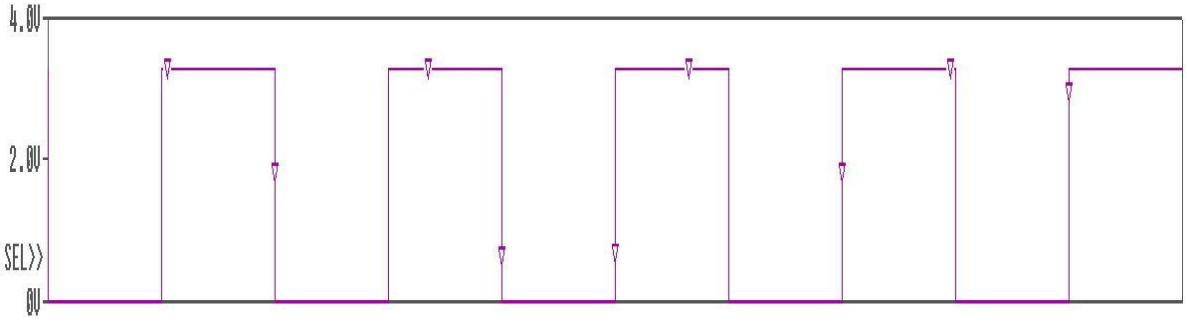

Fig. 3.3 (a) Output waveform of Conventional domino logic buffer.

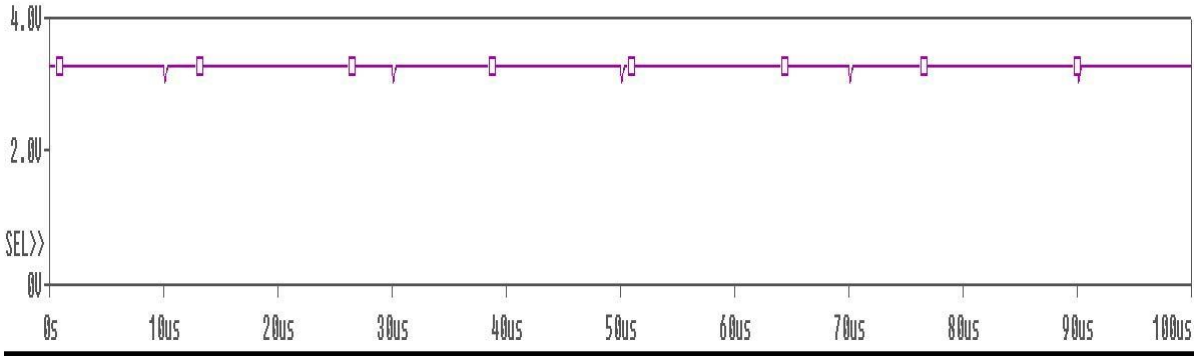

Fig. 3.3 (b) Output waveform of Domino logic buffer using proposed Logic.

Whereas in output waveform of proposed domino buffer given in Fig 3.3(b), the unwanted switching from 0 to 1 and from 1 to 0 is reduced, here the switching activity factor is 1 per clock cycle hence reducing the power consumption of the circuit and achieving stable output. When using 180nm technology and setting Vdd=1.8 V, clock frequency f_{clk}=200 MHz, C_{load}=50 pF, the power consumption of a conventional domino buffer is 4.5 µW. while the power consumption in proposed domino logic buffer is 23.2 pW, indicating power reduction due to switching activity reduction.

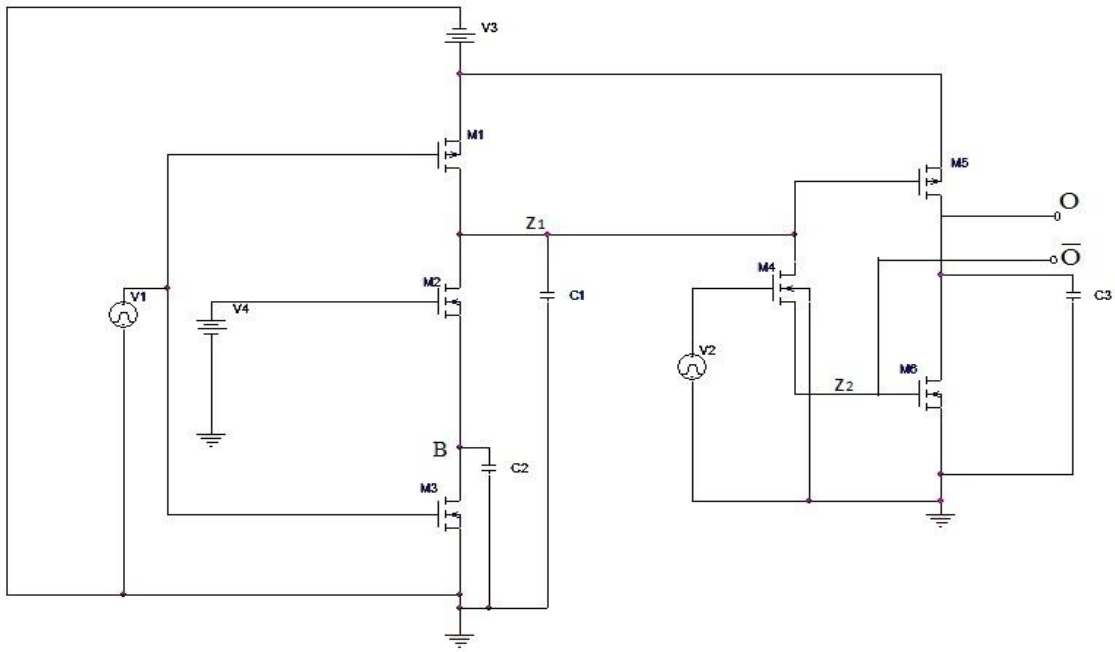

Fig. 3.4 Domino logic buffer circuit using the proposed domino logic.

The second limit is the charge sharing, which is mainly generated due to a finite clock slew rate. During the clock transition from‘1’to‘0’, the voltage at node B will be charged from node Z1, leading to an output charge sharing with refer to fig 3.4. The charge sharing problem could be alleviated by using a number of solutions, namely:

1) Using dual power supply techniques. Vdd2 used for supplying the dynamic buffer has higher voltage than Vdd1, by which the voltage drop at the output node due to charge sharing could be compensated.
2) Increasing the channel length of M6 resulting in less current flowing from output node O to ground. This will result in a smaller voltage drop at output node O and prevents charge sharing.
3) Increasing the load capacitance at node O. That is C3 > C2, the charge sharing effect could be minimized.

Solution 1 uses a dual power supply to compensate for the voltage drop at the output node. Using such an approach, no extra parasitic or load capacitance is required and ideally, the charge sharing can be minimized or completely eliminated. However, because the PMOS transistor of the buffer cannot be fully turned off, a large leakage current is an issue that needs to be addressed in the case of dual supply solution, particularly in deep submicron CMOS technologies.

Solution 2, by increasing the channel length of M6, a lesser amount of charge is shared by transistor M6 and as a result, the charge sharing at the output node can be alleviated. However, this method cannot completely solve charge sharing issue and it also increases the delay.

Solution 3, increases the load capacitance at the output node and involves extra power consumed proportionally to the load capacitance [15]. Similarly to solution 2, this approach also suffers from charge sharing issue.

3.4 ADVANTAGE

The main advantage of proposed domino logic is that both complimented and non-complimented outputs are available at the same time. Since complimented output is available universal logic gates can be realized through proposed logic.

A universal gate is a gate which can implement any Boolean function without need to use any other gate type. The NAND and NOR gates are universal gates. In practice, this is advantageous since NAND and NOR gates are economical and easier to fabricate and are the basic gates used in all IC digital logic families. In fact, an AND gate is typically implemented as a NAND gate followed by an inverter.

CHAPTER 4 SIMULATION & RESULT OF VARIOUS LOGIC FUNCTION

4. 1 TOOLS USED:

4.1.1 PSPICE A/D

PSpice A/D simulates analog-only, mixed analog/digital, and digital-only circuits. PSpice A/D's analog and digital algorithms are built into the same program so that mixed analog/digital circuits can be simulated with tightlycoupled feedback loops between the analog and digital sections without any performance degradation. After you prepare a design for simulation, Orcad Capture generates a circuit file set. The circuit file set, containing the circuit netlist and analysis commands, is read by PSpice A/D for simulation. PSpice A/D formulates these into meaningful graphical plots, which you can mark for display directly from your schematic page using markers[16].

PSpice A/D Basics provides the basic functionality needed for analog and mixed-signal design without the advanced features in the full PSpice A/D package.

4.1.2 ANALYSES RUN WITH PSPICE A/D

4.1.2.1 DC SWEEP & OTHER DC CALCULATIONS

These DC analyses evaluate circuit performance in response to a direct current source. Table 1 summarizes what PSpice A/D calculates for each DC analysis type[16].

Table 1 DC Analysis

DC analysis	PSpice A/D computes
DC sweep	Steady-state voltages, currents, and digital states when sweeping a source, a model parameter, or temperature over a range of values.
Bias point detail	Bias point data in addition to what is automatically computed in any simulation.
DC sensitivity	Sensitivity of a net or part voltage as a function of bias point.
Small-signal DC transfer	Small-signal DC gain, input resistance, and output resistance as a function of bias point.

4.1.2.2 AC SWEEP AND NOISE

AC analyses evaluate circuit performance in response to a small-signal alternating current source. Table 2 summarizes what PSpice A/D calculates for each AC analysis type[16].

Table 2 AC Analysis

AC analysis	PSpice A/D computes
AC sweep	Small-signal response of the circuit (linearized around the bias point) when sweeping one or more sources over a range of frequencies. Outputs include voltages and currents with magnitude and phase.
Noise	For each frequency specified in the AC analysis: • Propagated noise contributions at an output net from every noise generator in the circuit. • RMS sum of the noise contributions at the output. • Equivalent input noise.

4.1.2.3 TRANSIENT ANALYSIS

These time-based analyses evaluate circuit performance in response to time-varying sources. Table 3 summarizes what PSpice A/D calculates for each time-based analysis type[16].

Table 3 Time-Based Analysis

Time-based analysis	PSpice A/D computes
Transient	Voltages, currents, and digital states tracked over time. For digital devices, you can set the propagation delays to minimum, typical, and maximum. If you have enabled digital worst-case timing analysis, then PSpice A/D considers all possible combinations of

	propagation delays within the minimum and maximum range.

4.1.2.4 PARAMETRIC ANALYSIS

For parametric analyses, PSpice A/D steps a circuit value in a sequence that specify and runs a simulation for each value. Table 5 shows the circuit values that you can step for each kind of analysis[16].

Table 4 Parametric and Temperature Analysis

Analysis	PSpice A/D computes
Parametric	global parameter model parameter component value DC source operational temperature

4.2 DESIGN AND SIMULATION OF PDB-BASED DOMINO LOGIC:

4.2.1 PSEDUO DYNAMIC BUFFER

Fig 4.1 shows pseudo dynamic buffer domino logic circuit (reported circuit), simulated on Cadence Capture Lite Edition. In this topology, the source of the buffer's NMOS transistor M5 is connected to node B instead of Gnd.

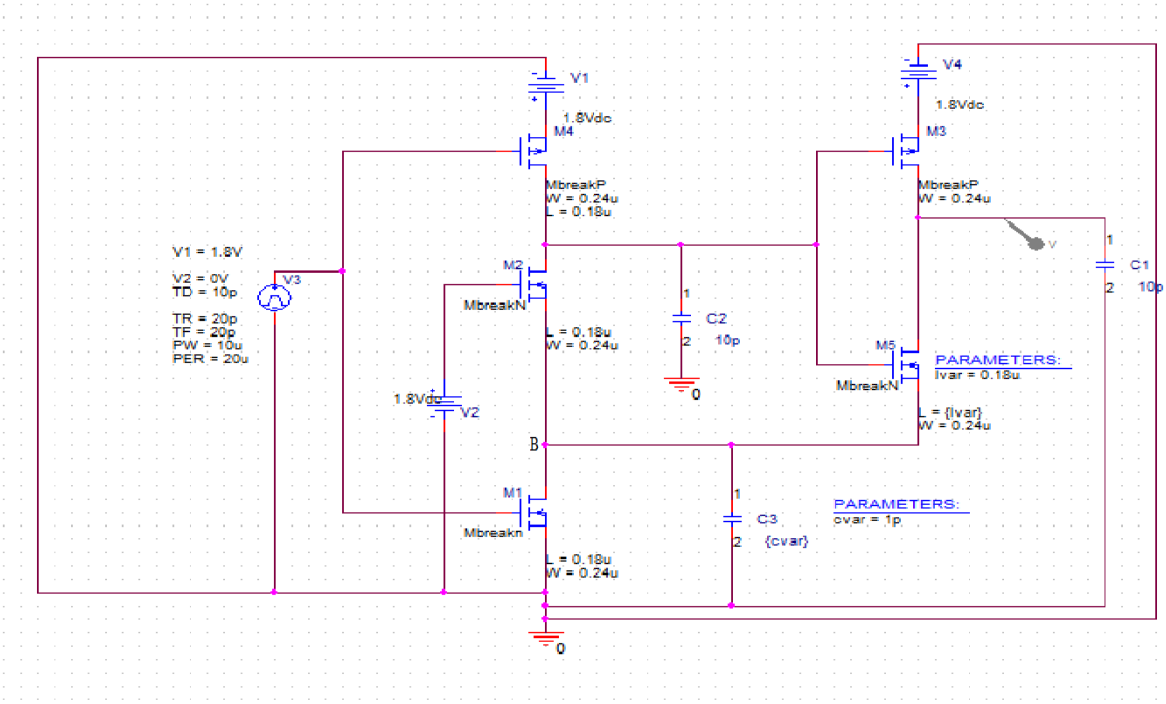

Fig 4.1 Schematic of PDB domino logic.

Using circuit topology as in Fig 4.1, the value at dynamic node Z cannot discharge during Precharge phase because, the evaluation transistor M2 is turned off and hence the output is not affected.

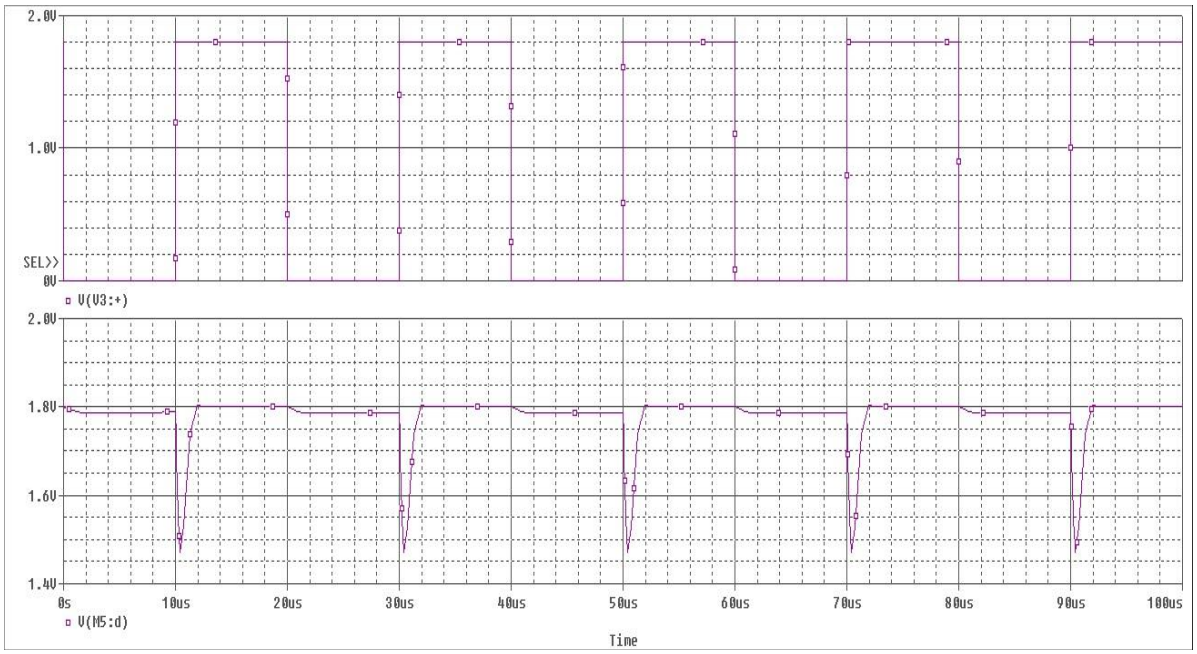

Fig 4.2 Output waveform of PDB domino logic.

The simulated output waveform of PDB domino logic is given in Fig 4.2, the output is high for the entire clock cycle with small value of charge sharing.

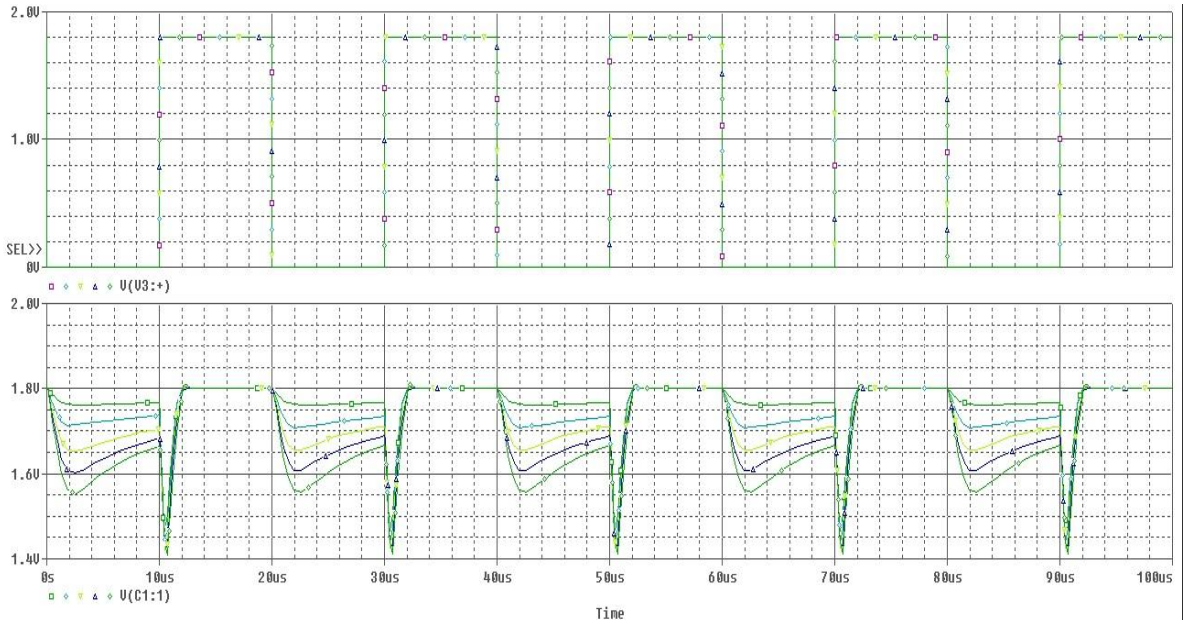

Fig 4.3 Output waveform of PDB domino logic with varying load capacitance

Fig. 4.3 shows Output waveform of PDB domino logic with varying values of load capacitances.

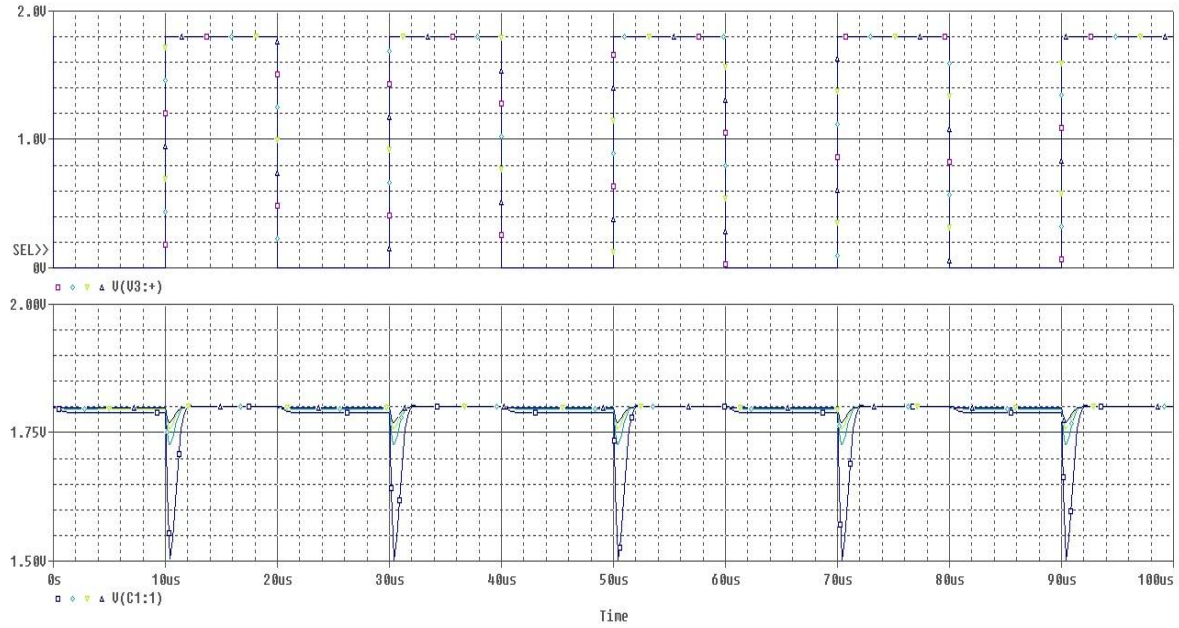

Fig 4.4 Output waveform of PDB domino logic with varying channel length of M5

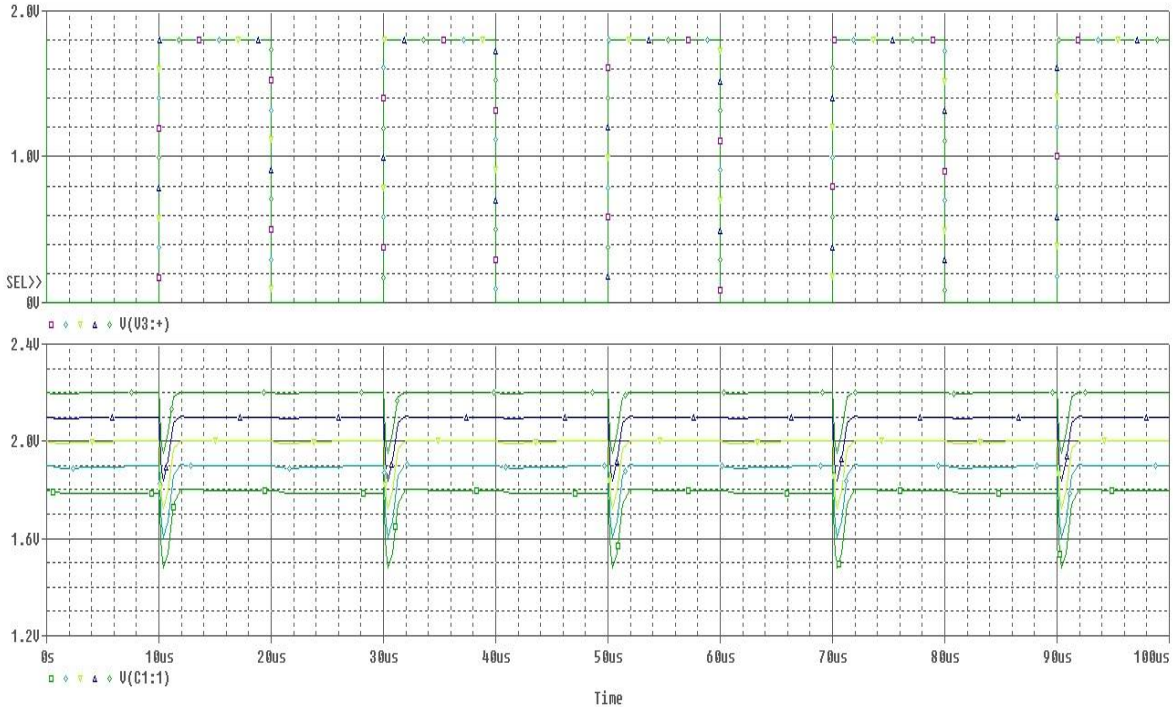

Fig 4.5 Output waveform of PDB domino logic with varying voltage supply

Fig. 4.4 and Fig. 4.5 shows output waveform of PDB domino logic with varying channel length of transistor M5 and varying voltage supply.

4.2.2 PDB-BASED AND/NAND LOGIC:

Fig 4.6 shows 2-input pseudo dynamic buffer based AND domino logic circuit (reported circuit), simulated on Cadence Capture Lite Edition. In this topology, the source of the buffer's NMOS transistor M5 is connected to node B instead of Gnd. Using such a circuit topology, the value at dynamic node Z cannot discharge during Precharge phase because, the evaluation transistor M2 is turned off and hence the output is not affected.

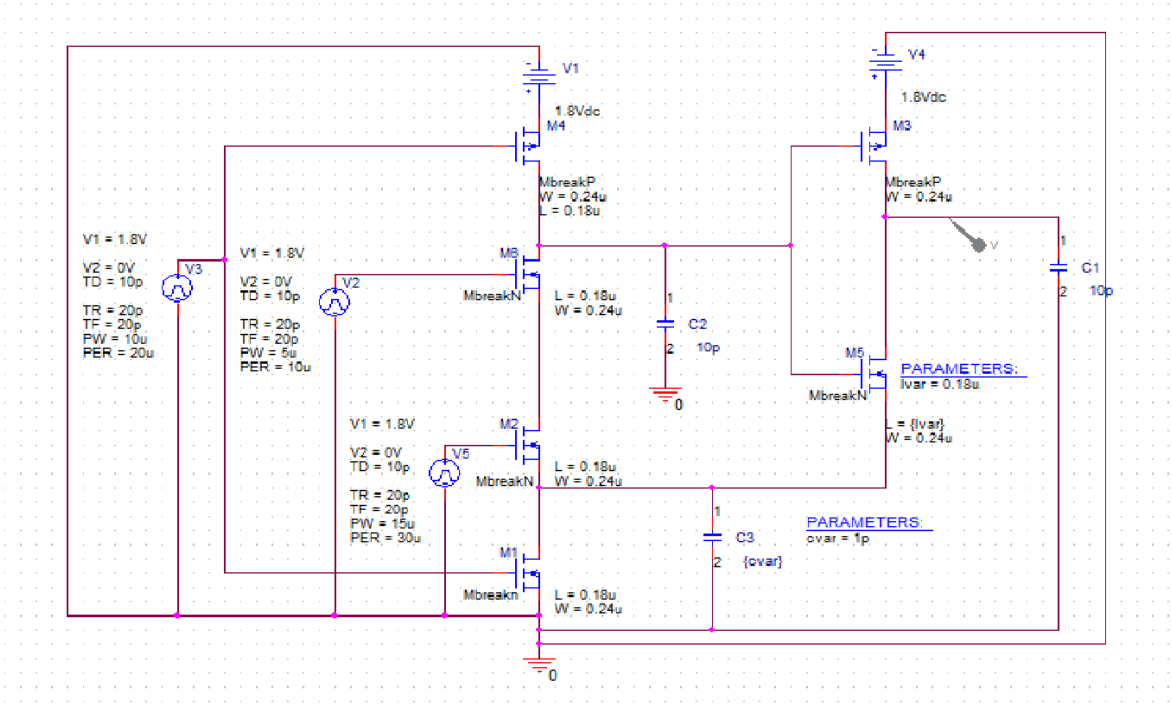

Fig 4.6 Schematic of 2-input PDB AND domino logic.

The simulated output waveform of 2-input PDB-based AND domino logic is given in Fig 4.7, the output is high only for the time period when both the inputs are high.

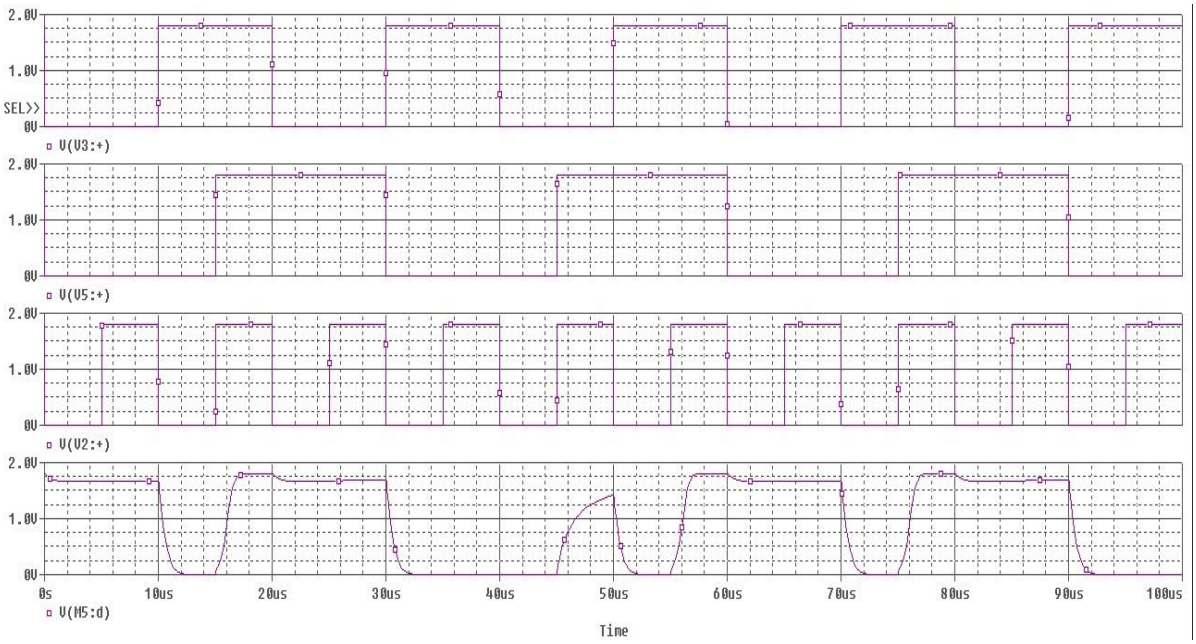

Fig 4.7 Output waveform of 2-input PDB AND domino logic.

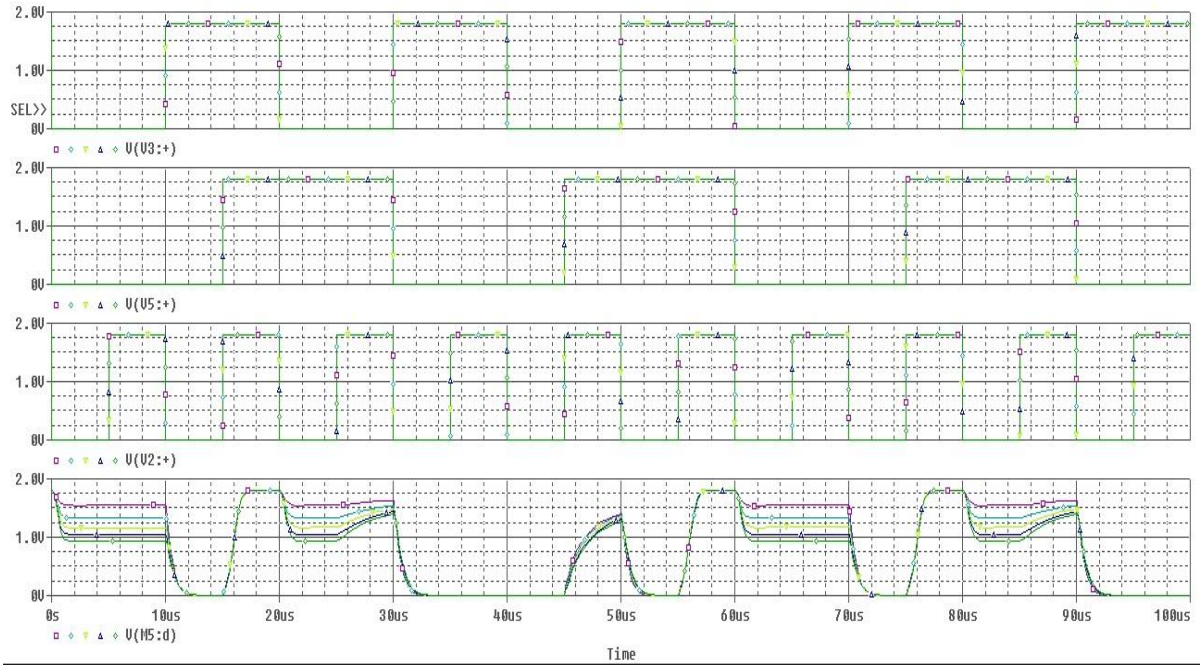

Fig 4.8 Output waveform of 2-input PDB AND domino logic with varying load capacitance.

Fig. 4.8 shows output waveform of 2-input PDB AND domino logic with varying values of load capacitances.

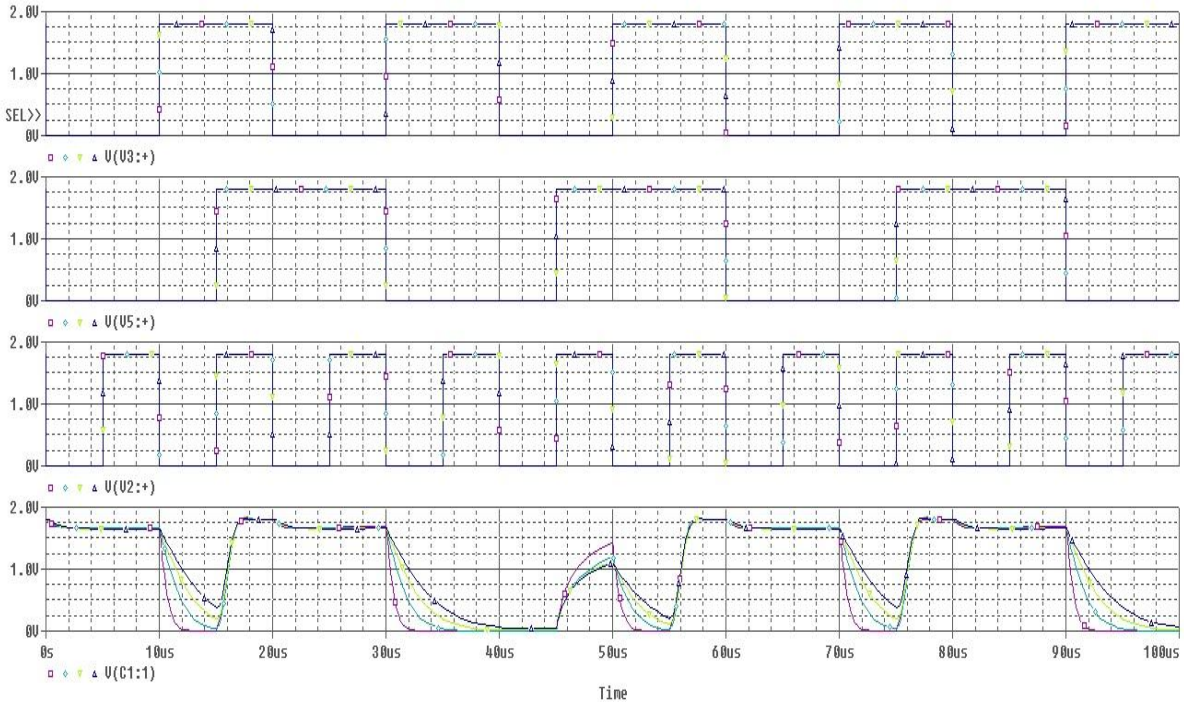

Fig 4.9 Output waveform of 2-input PDB AND domino logic with varying channel length of M5.

Fig. 4.9 shows output waveform of 2-input PDB AND domino logic with varying values of channel length of transistor M5.

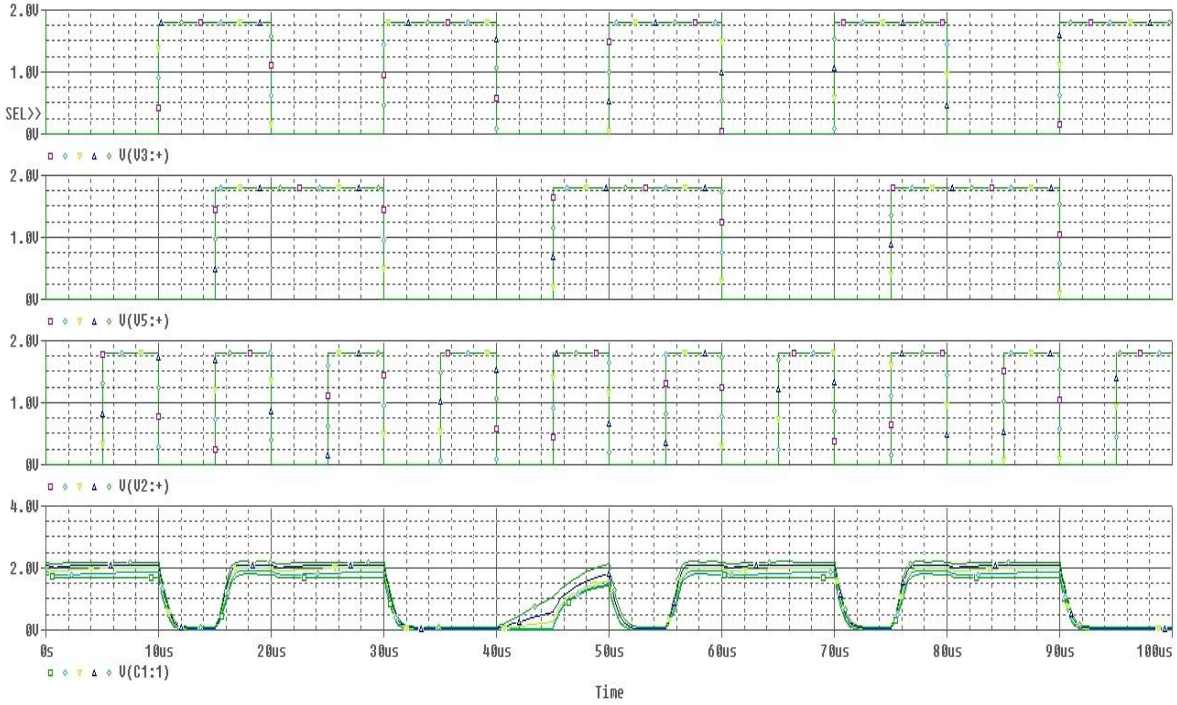

Fig 4.10 Output waveform of 2-input PDB AND domino logic with varying values of supply voltage.

Fig. 4.10 shows output waveform of 2-input PDB AND domino logic with varying values of supply voltage.

4.3 DESIGN AND SIMULATION OF PROPOSED DOMINO LOGIC:

4.3.1 PROPOSED DOMINO LOGIC BUFFER

Fig. 4.11 shows schematic of proposed method of Domino logic system. When the clock signal is low, the domino logic circuit is in the precharge phase. During this phase, the dynamic node is charged to vdd by the pull-up transistor (M1). And when the clock signal is high, the circuit enters the evaluation phase.

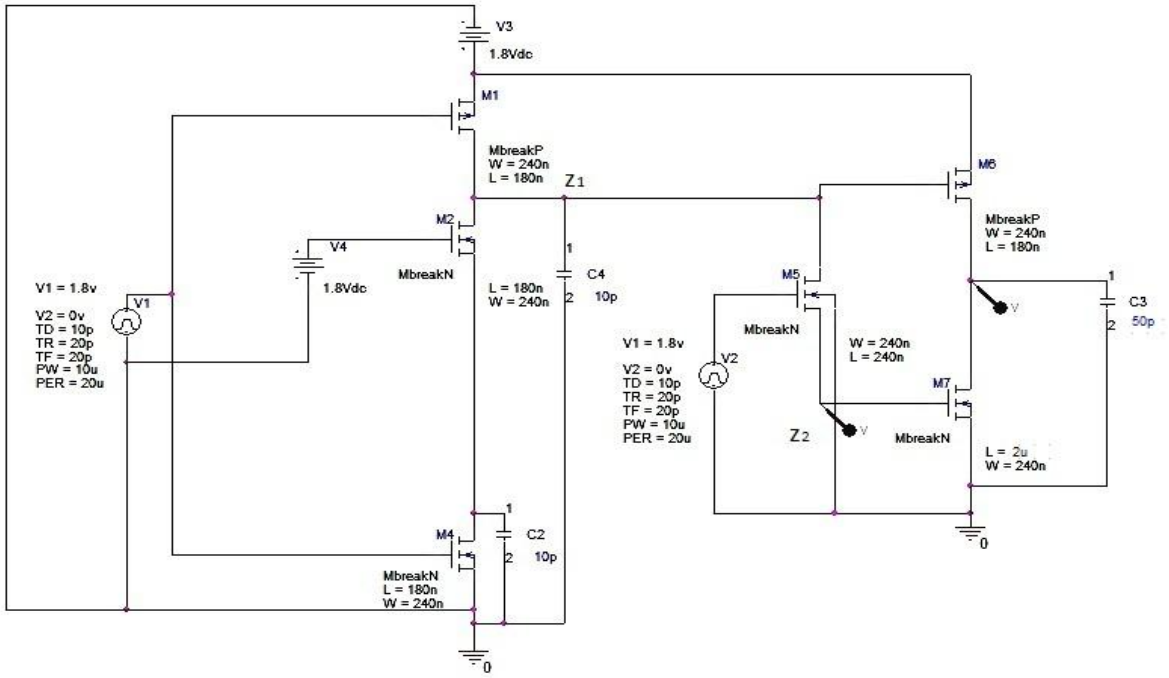

Fig 4.11 Schematic of proposed domino logic as a buffer.

Fig. 4.12 shows output waveform of proposed method of Domino logic system.

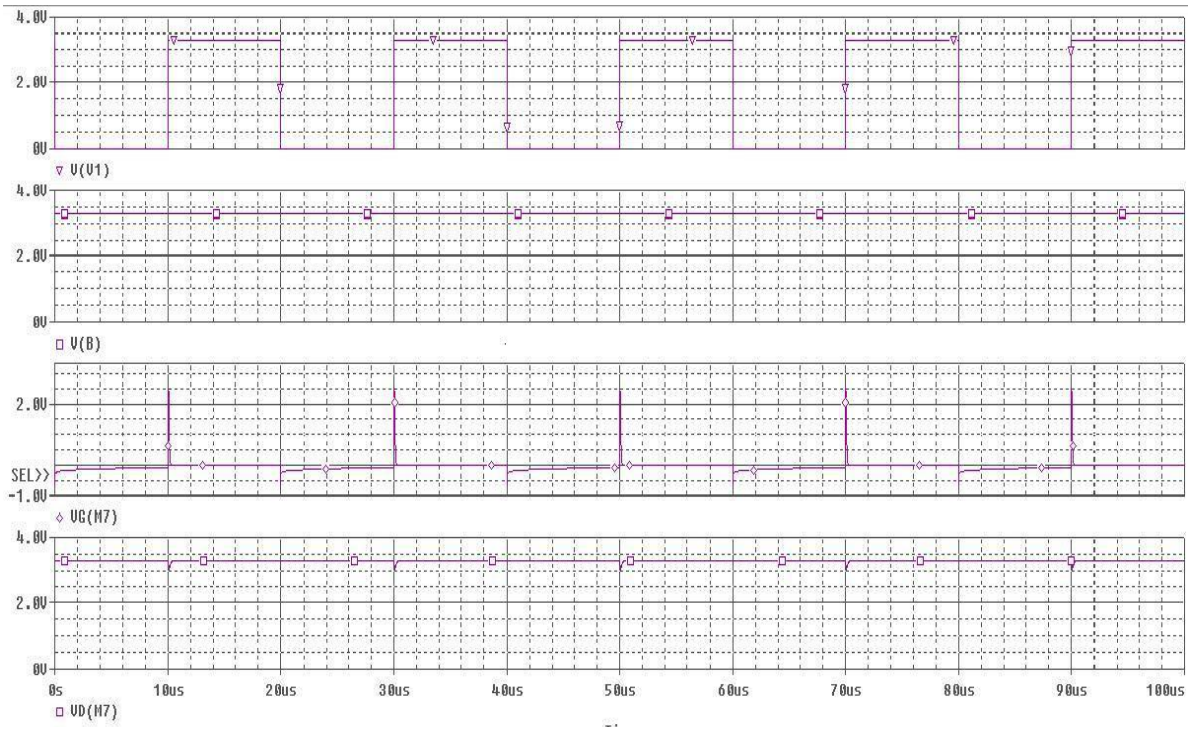

Fig 4.12 Output waveform of proposed domino logic as a buffer.

4.3.2 AND/NAND LOGIC GATE USING PROPOSED SCHEME

Fig 4.13 shows schematic of AND/NAND logic gates using proposed method of Domino logic system. When the clock signal is low, the domino logic circuit is in the precharge phase. During this phase, the dynamic node is charged to vdd by the pull-up transistor (M1). And when the clock signal is high, the circuit enters the evaluation phase. In this phase, provided that the necessary input combination to discharge the dynamic node is applied, the circuit evaluates and the dynamic node is discharged to ground.

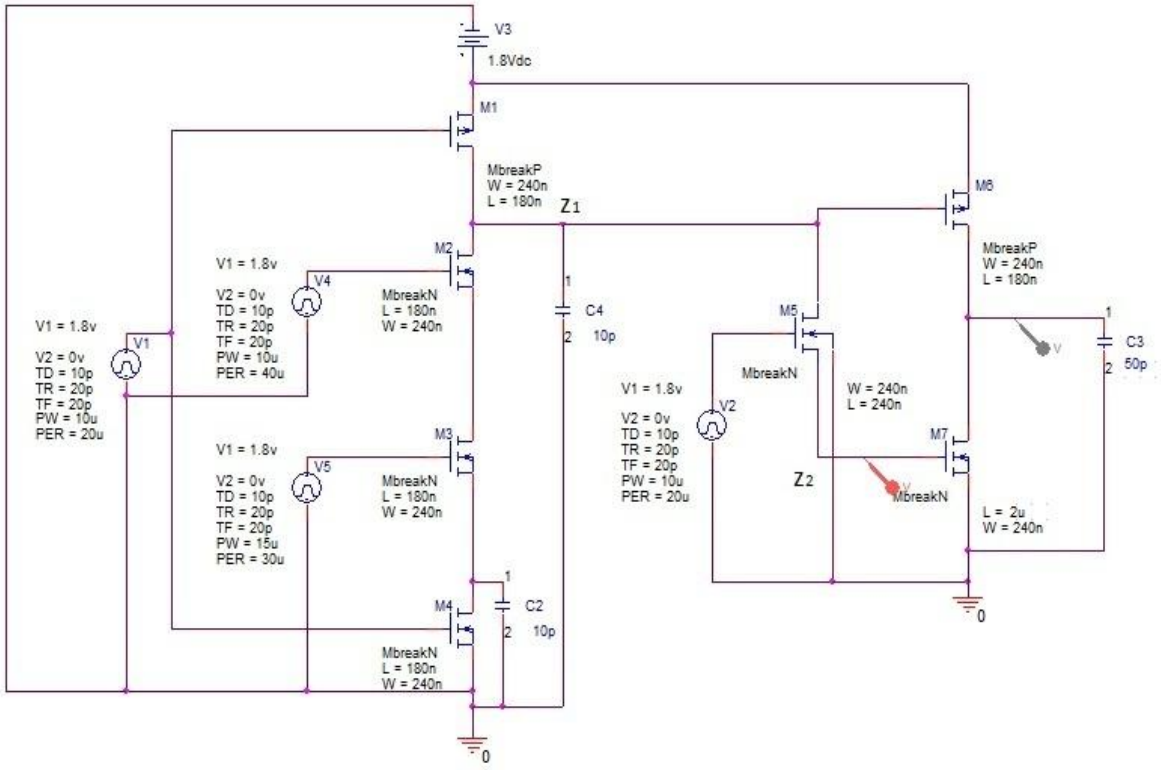

Fig 4.13 Schematic of proposed AND/NAND domino logic.

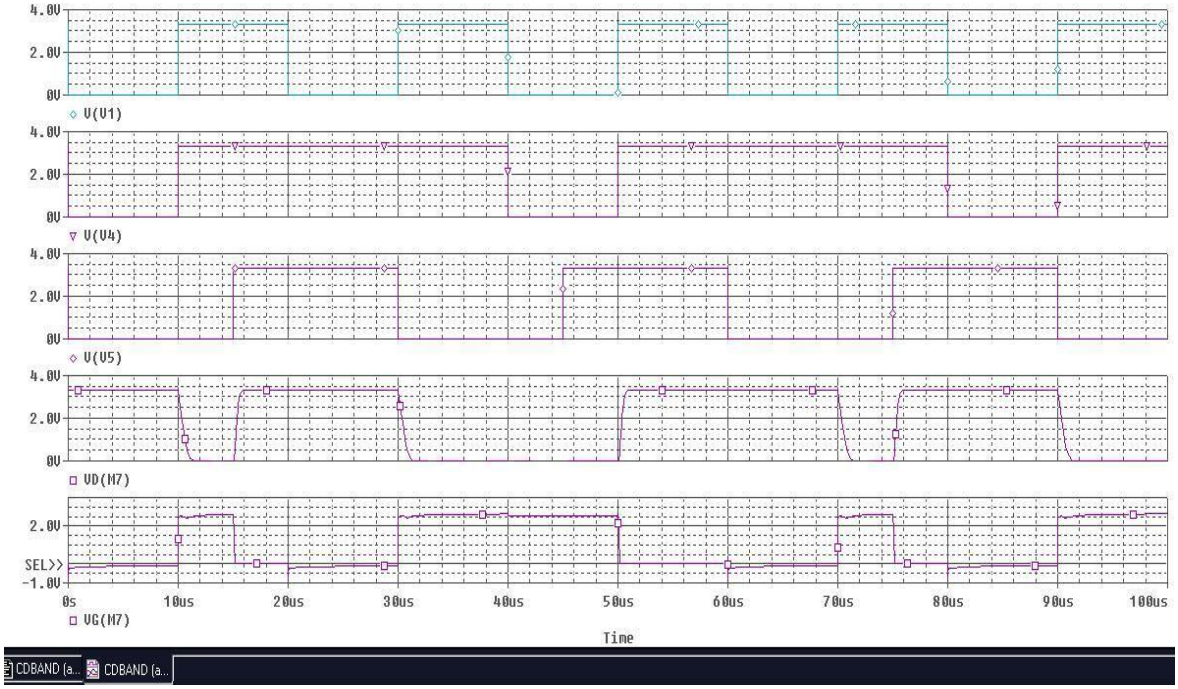

Fig 4.14 Output waveform of proposed AND/NAND domino logic.

The simulated output waveform of 2-input proposed AND/NAND domino logic is given in Fig 4.14, the output is high only for the time period when both the inputs are high.

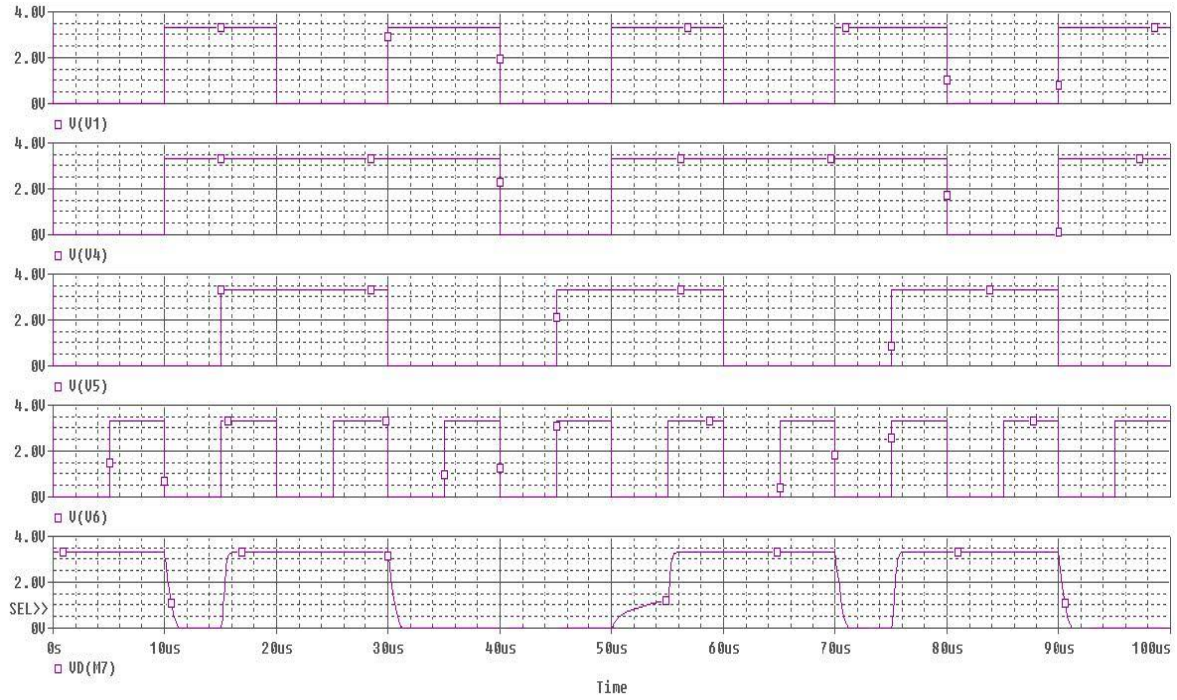

Fig 4.15 Output waveform of proposed 3 input AND domino logic.

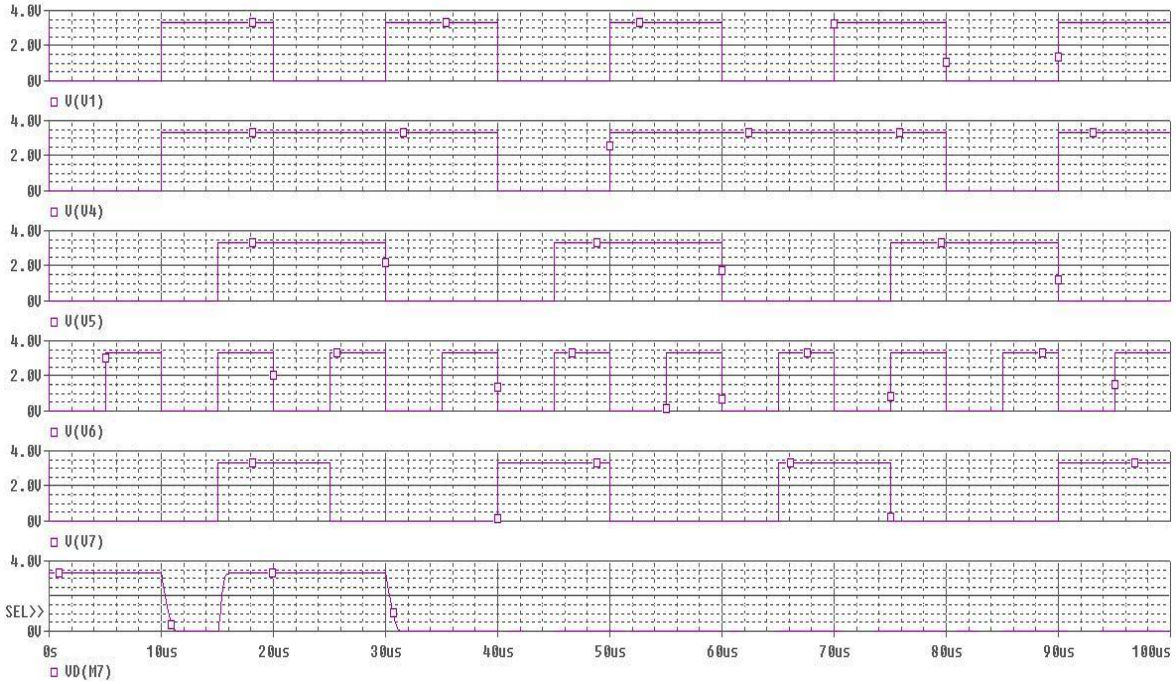

Fig 4.16 Output waveform of proposed 4 input AND domino logic.

Fig 4.15 and Fig 4.16 shows the output for 3-input and 4-input Proposed AND domino logic.

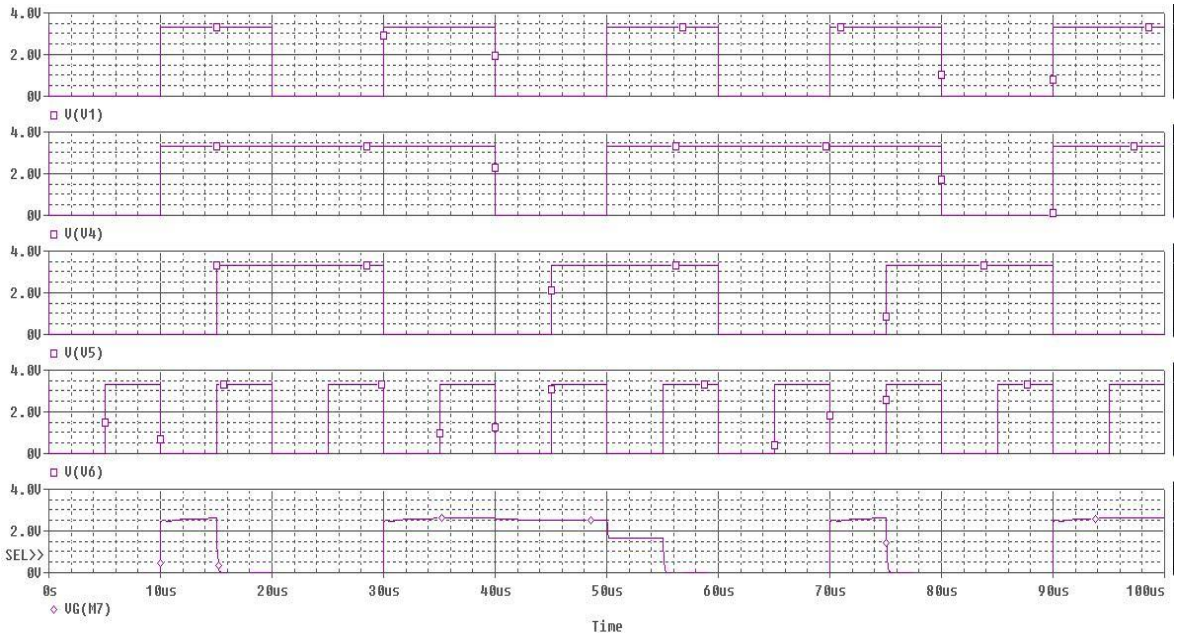

Fig 4.17 Output waveform of proposed 3 input NAND domino logic.

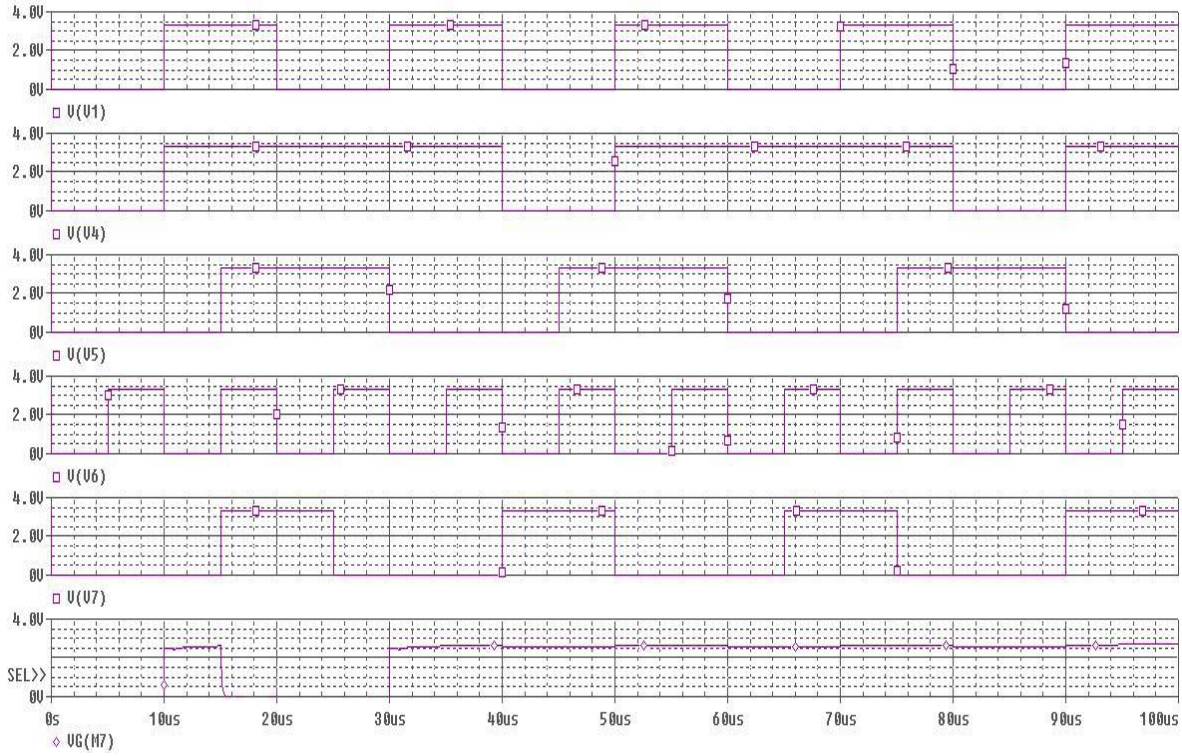

Fig 4.18 Output waveform of proposed 4 input NAND domino logic.

Fig 4.17 and Fig 4.18 shows the output for 3-input and 4-input Proposed NAND domino logic.

4.3.3 OR/NOR LOGIC GATE USING PROPOSED SCEME

Fig 4.19 shows 2-input proposed OR/NOR domino logic circuit simulated on CADENCE PSpice AD. When the clock signal is low, the domino logic circuit is in the precharge phase. During this phase, the dynamic node is charged to vdd by the pull-up transistor (M1). And when the clock signal is high, the circuit enters the evaluation phase. In this phase, provided that the necessary input combination to discharge the dynamic node is applied, the circuit evaluates and the dynamic node is discharged to ground.

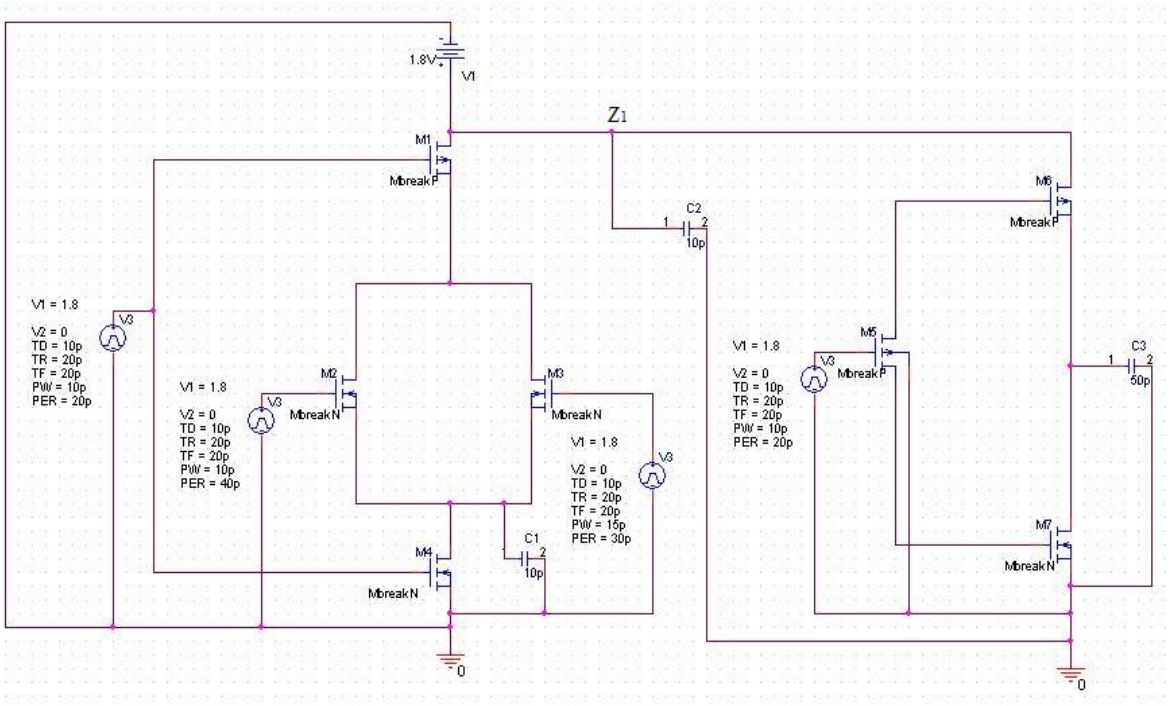

Fig 4.19 Schematic of proposed 2-input OR/NOR domino logic.

The simulated output waveform of 2-input proposed OR/NOR domino logic is given in Fig 4.20, the output is high for the time period when any of both the two input is high.

Fig 4.20 Output waveform of proposed 2-input OR/NOR domino logic.

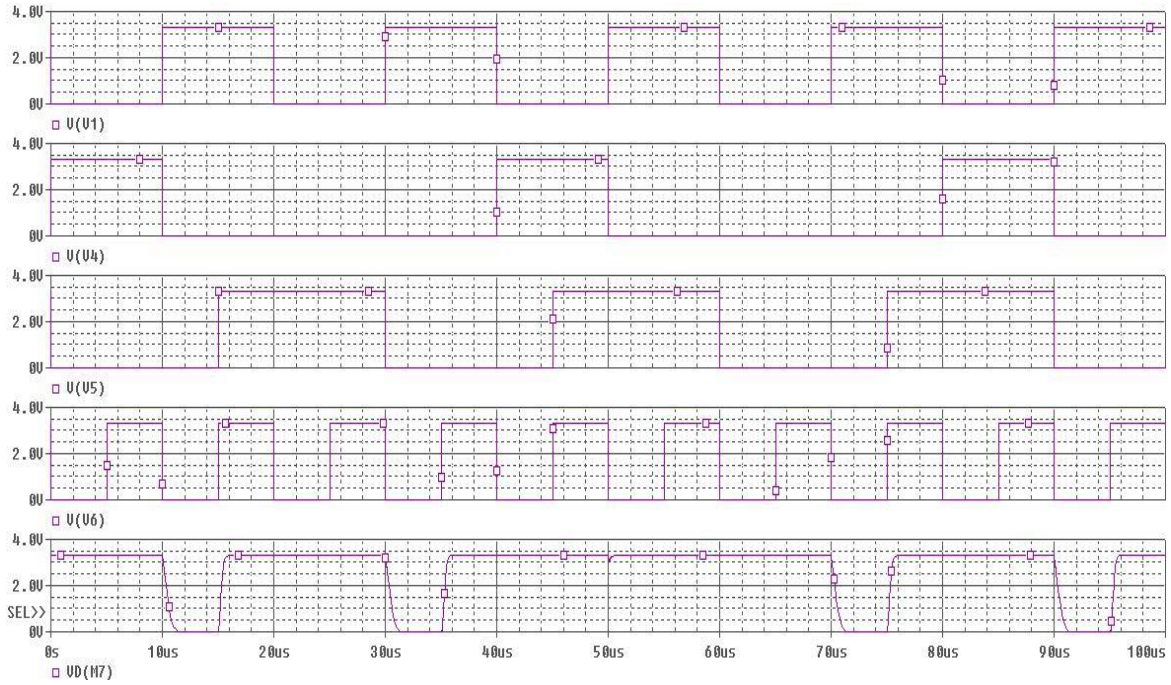

Fig 4.21 Output waveform of proposed 3-input OR domino logic.

Fig 4.21 and Fig 4.22 shows the output for 3-input and 4-input Proposed OR domino logic.

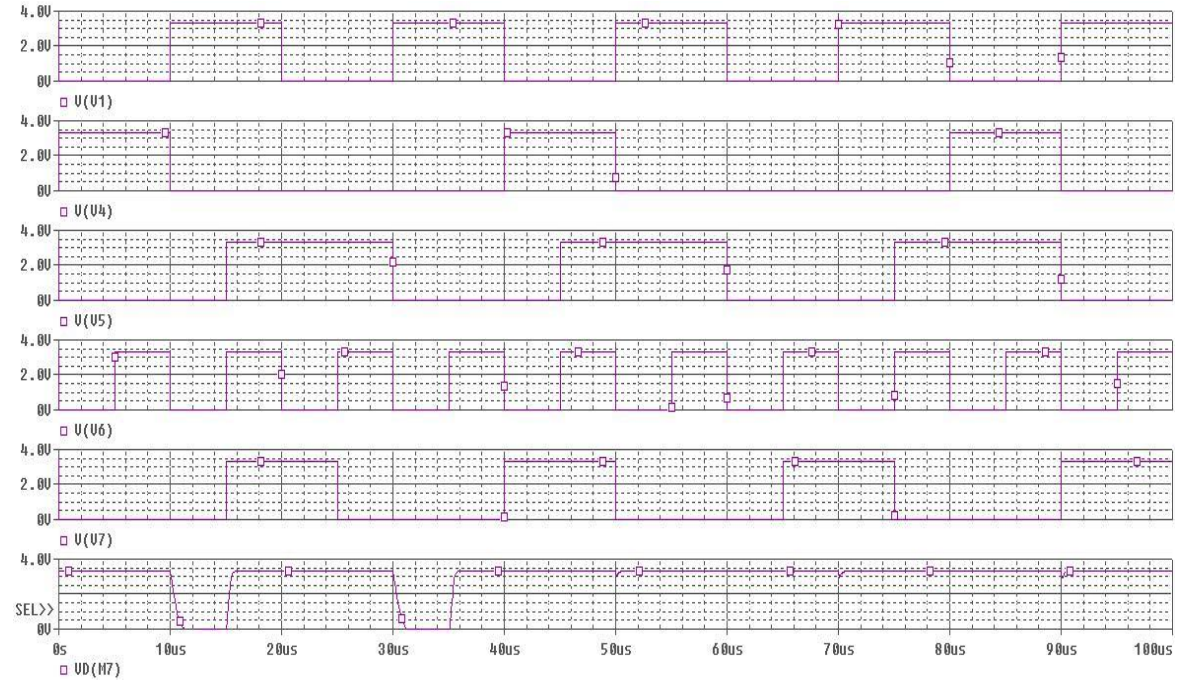

Fig 4.22 Output waveform of proposed 4-input OR domino logic.

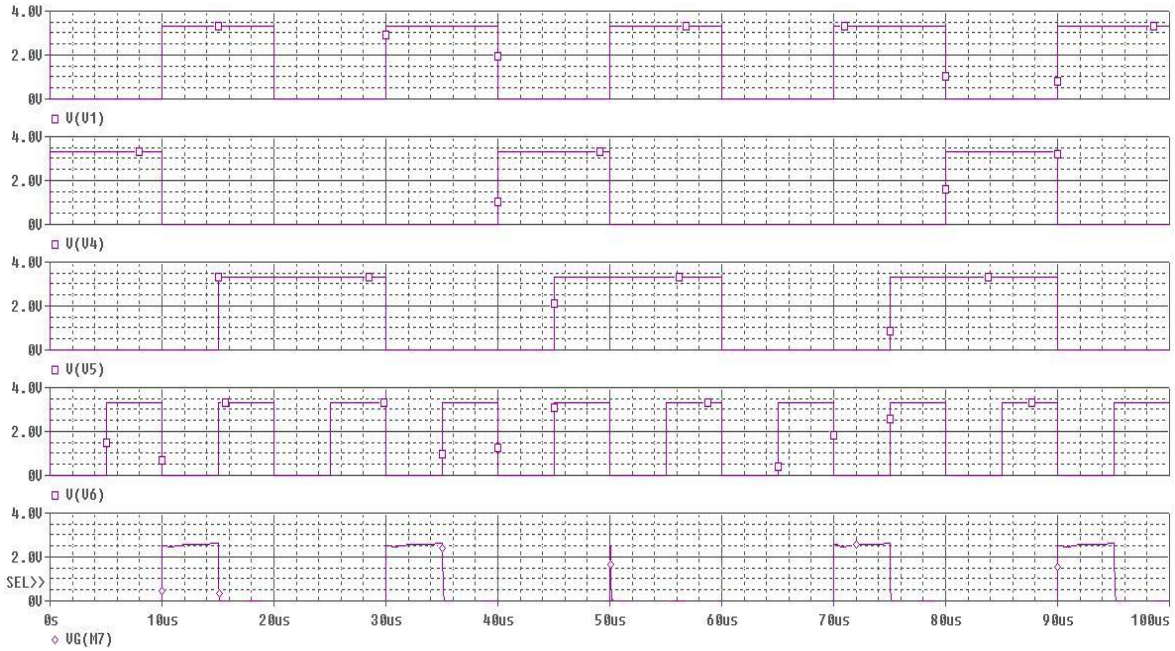

Fig 4.23 Output waveform of proposed 3-input NOR domino logic.

Fig 4.23 and Fig 4.24 shows the output for 3-input and 4-input Proposed NOR domino logic.

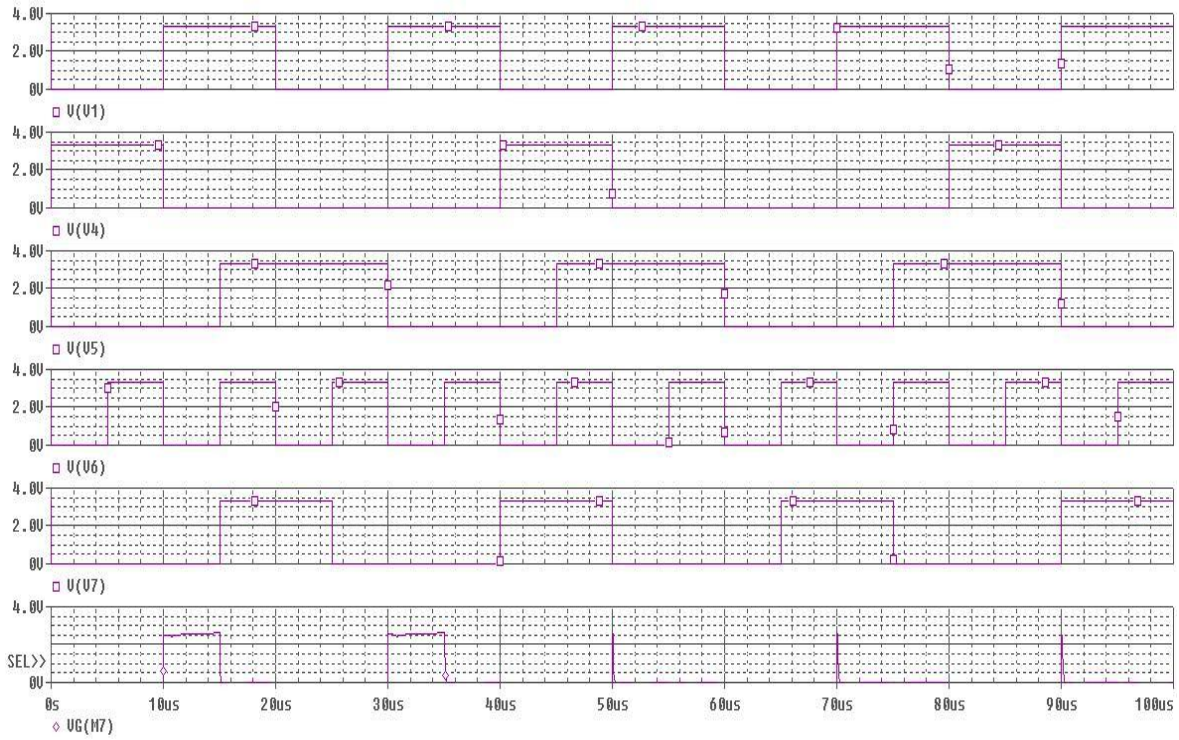

Fig 4.24 Output waveform of proposed 4-input NOR domino logic.

Table 5 shows comparison between power and delay of conventional domino logic and proposed domino logic, power consumption of the proposed logic is less than conventional in every case, because of reduction in switching activity in the proposed circuit.

TABLE 5

POWER COMPARISON OF CONVENTIONAL AND PROPOSED DOMINO LOGIC

Logic functions with different input	Conventional Power(µw)	Proposed Power(pw)
2-input AND	18.4	23.2
3-input AND	22	23.2
4-input AND	29.1	23.2
2-input OR	16.1	23.2
3-input OR	17.5	23.2
4-input OR	21.9	23.2

Proposed circuit is also compared with Reported (Pseudo dynamic buffer domino logic) circuits for non-complimented output and the result are given in table 6.

TABLE 6

POWER COMPARISON OF REPORTED AND PROPOSED DOMINO LOGIC

Logic functions with different input	Reported Power(µw)	Proposed Power(pw)
2-input AND	9	23.2
3-input AND	12.3	23.2
4-input AND	15.7	23.2
2-input OR	7.74	23.2
3-input OR	9.6	23.2
4-input OR	11.6	23.2

The main advantage of proposed circuit is that it has both complimented and non-complimented output, having complimented output benefits us to design universal gates i.e. NAND and NOR logic gates. The power consumption of proposed circuit for NAND and NOR logic is less than the reported NAND and NOR circuits, the reduction in the power consumption in proposed circuits is due to reduced number of transistor. In the proposed circuit the power consumption for both complimented and non-complimented output is same because the proposed circuit is having both complimented and non-complimented output

Result shows that power consumption of proposed logic circuit are less than the reported logic circuits.

CHAPTER 5 CONCLUSION & FUTURE WORK

New low power high speed domino logic has been proposed for footed domino logic system. The proposed logic uses the MOSFET capacitance to store chare and produce output. A transistor is connected between dynamic node and NMOS transistor of output stage, the propagation delay reduces due to reduction in number of stages and power consumption reduced due to reduction of number of transistor. The main advantage of this topology is that complimented output is available at source terminal of the extra transistor connected, which benefits us to design universal gates. A universal gate is capable of implementing any logic function. So the proposed logic has low power with high speed and capable of implementing any logic function.

For universal gates the proposed logic shows improved power dissipation than reported logic.

This new design is appropriate to be applied for construction of large low-power high-performance VLSI systems and it can work better in the future at higher technology such as 130 nm or 90nm technology.

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