CERTIFICATE

This is to certify that the dissertation entitled "**LOW POWER PSEUDO DYNAMIC BUFFER WITH DYNAMIC LOGIC**" is the work of Mr. Mayank Srivastava (Roll No.: 2k11/VLS/07), a student of M.Tech.(VLSI Design and Embedded System) in Delhi Technological University (Formerly DCE). This work is completed under my direct supervision and guidance and forms a part of Master of Technology (Electronics and Communication) course and curriculum. He has completed her work with utmost sincerity and diligence.

The work embodied in this major project has not been submitted to any other Institute/University for the award of any other degree to the best of my knowledge.

DATE:-
PLACE:- Delhi

Dr. RajivKapoor

(Project Guide)

Professor and HOD

Department of Electronics and Communication Engineering,

DelhiTechnologicalUniversity (formerly DCE),

Delhi– 110042

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Mayank Srivastava
(2K11/VLS/07)
ELECTRONICS & COMMUNICATION ENGINEERING
DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi college of Engineering)

ABSTRACT

Dynamic logic circuit is the main digital circuits, with a clock as a controlling signal. Comparing with the complementary logic circuit which is having both Pull-up and Pull-down network, dynamic logic circuit has only one network. Dynamic logic circuits consume nearly half of the transistor count as well as the layout area. Parasitic capacitances are used to stored the voltage at the output of the dynamic node, which is typically buffered before it is sent to the next stage. This voltage is affected by the charge sharing. Advantage of dynamic logic circuit is having smaller area and higher speed. According to the theory, the dynamic logic circuit will uses precharge and evaluation phases of the clock cycle. During the precharge phase, a lot of extra noise are introduced into the system compared with the static logic circuit. A noticeable amount of power is waisted due to these periodic precharge phases.

Here we propose a Low power pseudo dynamic buffer structure for the dynamic logic circuit. Using this dynamic buffer structure, the precharge pulse is obstructed at the input of the dynamic buffer and is supress from being propagated to the output of the dynamic gate. As a result, power typically consumed during the precharge phase is saved. According to the proposed structure will dramatically reduce the output noise as well as considerable power consumption compared to the traditional dynamic buffer circuits.

TABLE OF CONTENTS

LIST OF FIGURES

List of Figures Page no.

LIST OF TABLES