Design and Implementation of Non-Linear Signal Processing Circuits

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CERTIFICATE

This is to certify that the thesis entitled, "**Design and Implementation of Non-Linear Signal Processing Circuits**" is a bonafide work submitted by Satya Narayan Agarwal (2K11/C&I/12) in partial fulfillment of the requirements for award of the degree in M.Tech in Control & Instrumentation under my supervision.

This work has not been submitted earlier in any university or institute for the award of any degree/diploma to the best of my knowledge.

Prof. Pragati Kumar
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ABSTRACT

Non-Linear signal processing circuits are used in various streams of engineering such as communication, control system, digital design, etc. Various types of signal processing methods are used according to applications and requirements. CMOS based non-linear signal processing circuit is less power consuming.

In this dissertation various types of Non-Linear Circuits have been implemented such as multiplier, divider, vector magnitude calculator, sine shaper, and log and antilog amplifier. These circuits have been implanted using off the shelf available components as well as integrable versions using both bipolar as well as CMOS transistors. The off-the-shelf available building blocks used include uA741, AD844, CA3080.

Log and antilog amplifier circuits are implemented using uA741, the four quadrant multiplier and divider circuit are implemented using AD844, CMOS based operational transconductance (OTA) circuit is also presented and implementation of two quadrant multiplier circuit using that OTA is presented.

Translinear circuit principle is used to implement vector magnitude calculator, sine shaper circuit, and linearized four quadrant multiplier.

Lastly, implementation of CMOS based squarer and multiplier is also presented.

LIST OF FIGURES

LIST OF SYMBOLS

S.No.	Symbols	Descriptions
1.	g_m	Transconductance
2.	Z_i	Input Impedance
3.	Z_o	Output Impedance
4.	V_{SS}	Source Supply Voltage
5.	V_{DD}	Drain Supply Voltage
6.	I_o	Bias Current
7.	I_b	Bias Current
8.	w.r.t.	With respect to
9.	OTA	Operational Transconductance Amplifier
10.	CC	Current Conveyor
11.	CFA	Current Feedback Amplifier
12.	CFA	Current Feedback Operational Amplifier
13.	CDBA	Current Differencing Buffer Amplifier
14.	FTFN	Four Terminal Floating Nullors
15.	CMOS	Complementary Metal Oxide Semiconductor
16.	OA	Operational Amplifier
17.	Op amp	Operational Amplifier
18.	VLSI	Very Large Scale Integration
19.	VCO	Voltage Controlled Oscillators
20.	WTA	Wideband transconductance amplifier
21.	VCVS	Voltage Controlled Voltage Source
22.	VCCS	Voltage Controlled Current Source

23.	CCVS	Current Controlled Voltage Source
24.	CCCS	Current Controlled Current Source

CONTENTS

CHAPTER-1

INTRODUCTION

1.1 INTRODUCTION TO SIGNAL PROCESSING:

This dissertation presents design and implementation of some non-linear signal processing circuits. Before the details of work presented in this dissertation, some introduction to signal processing is given in the following section.

Signal processing is the enabling technology for the generation, transformation, and Interpretation of information. It comprises the theory, algorithms, architecture, implementation, and applications related to processing information contained in many different formats broadly designated as signals. Signal refers to any abstract, symbolic, or physical manifestation of information with examples that include: audio, music, speech, language, text, image, graphics, video, multimedia, sensor, communication, geophysical, sonar, radar, biological, chemical, molecular, genomic, and medical, data, or sequences of symbols, attributes, or numerical quantities.

Signal processing uses mathematical, statistical, computational, heuristic, and/or linguistic representations, formalisms, modelling techniques and algorithms for generating, transforming, transmitting, and learning from analog or digital signals, which may be performed in hardware or software. Signal generation includes sensing, acquisition, extraction, synthesis, rendering, reproduction and display. Signal transformations may involve filtering, recovery, enhancement, translation, detection, and decomposition. The transmission or transfer of information includes coding, compression, securing, detection, and authentication. Learning can involve analysis, estimation, recognition, inference, discovery and/or interpretation.

Signal processing is essential to integrating the contributions of other engineering and scientific disciplines in the design of complex systems that interact with humans and the environment, both as a fundamental tool due to the signals involved and as a driver of new design methodologies. As such, signal processing is a core technology for addressing critical societal challenges that include healthcare, energy systems, sustainability, transportation, entertainment, education, communication, collaboration, defence, and security.

1.2 DIFFERENT APPROACHES FOR SIGNAL PROCESSING:

The various type of a sampled data can be described of their time and amplitude characteristics grouped in four categories:

- Discrete amplitude Discrete time(D-D)
- Discrete amplitude Discrete time(D-C)
- Continuous amplitude Discrete time(C-D)
- Continuous amplitude Continuous time(C-C)

The first letter refers to amplitude and second letter refers to the time characteristics. The example of the signal is presented in Fig. 1.1

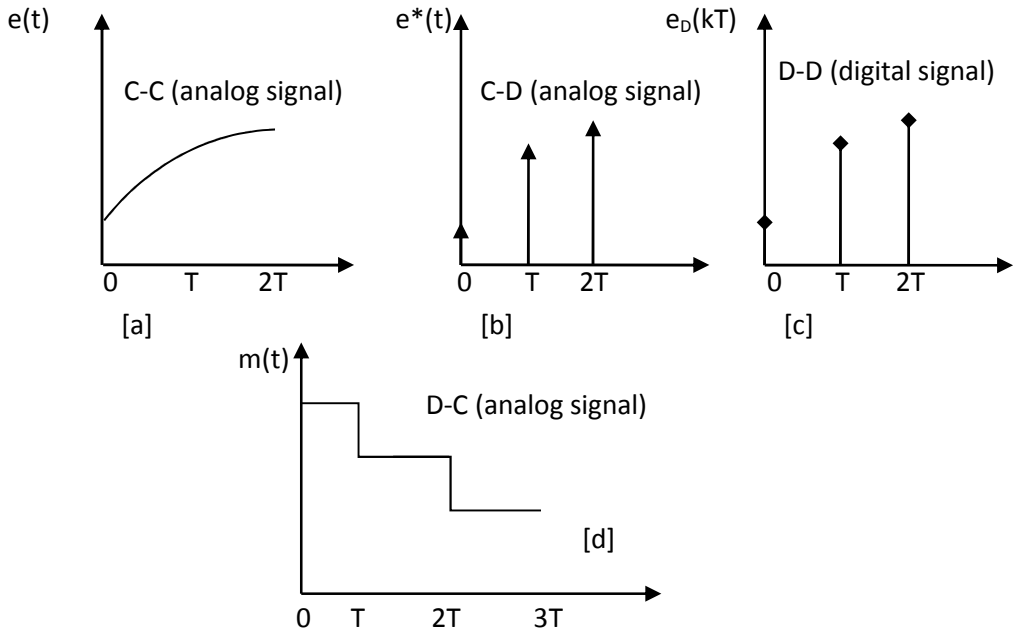

Fig. 1.1 Signal Classifications in digital signal processing system

This classification is a broad one and many a times there are overlaps in certain applications. There are certain are certain applications (i.e. A/D , D/A conversion) which can fall into more than one category.

Broadly signal processing techniques can be classified into three categories namely analog signal processing, digital signal processing and mixed mode signal processing [1].

Each of these techniques is described as follows:

1.2.1 Analog signal processing:

Analog signal processing is conducted on analog signals by different way of signal processing. Analog signals mathematically represent as a set of continuous values and

digital signal represent a series of discrete quantities to represent signal. Analog signal generally represented as a voltage, electric current, or around components in the electronic devices. An error or noise affecting such physical quantities will result in a corresponding error in the signals represented by such physical quantities. The magnitude of an analog signal can take on any value; that is the amplitude of an analog signal exhibit a continuous various over its range of activity. The vast majority of signals in these analog circuits signal processed using analog signal process. An example of voltage signal is represented in Fig. 1.1(a)

The various analog signal processing techniques used are

Convolution, Fourier transform, Laplace transforms and bode plot [2-3].

1.2.2 Digital Signal processing

In most general form Digital Signal processing refers to the processing of analog signal by means of discrete time operation implemented on digital hardware. In digital signal processing the input and output signals are analog but the processing is done on the equivalent digital signals. A digital signal processing system can be understood as follows:

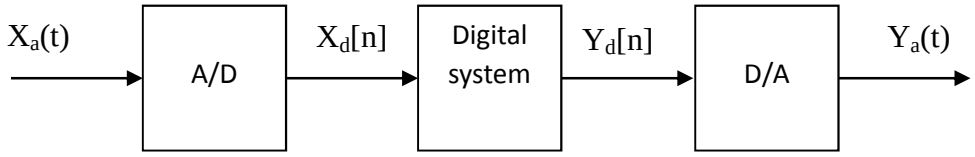

Fig 1.2 Block Diagram of DSP system

The analog-to-digital (A/D) converter transforms the analog signal X_a (t) at the system input into a digital signal X_d [n]. An A/D converter can be thought of as consisting of a sampler (creating a discrete time signal), followed by a quantizer (creating discrete levels).

The digital system performs the desired operations on the digital signal $X_d[n]$ and produces a corresponding output $Y_d[n]$ also in digital form. The digital-to-analog (D/A) converter transforms the digital output $Y_d[n]$ into an analog signal $Y_a(t)$ suitable for interfacing with the outside world. In some applications, the A/D or D/A

converters may not be required; we extend the meaning of DSP systems to include such cases. Basically digital signal processing is classified into following domain [3]:-

Time and space domain, frequency domain, z-plane domain

1.3 MIXED MODE SIGNAL PROCESSING

In many cases it is advantageous to replace analog filter by digital filters. But, there are a few cases where we cannot do so. Some of the examples of such cases are: - floating-gate-based field programmable analog array, VLSI analog computer/digital computer accelerator, signals from a sensor, microphone, antenna or cable [5-6]. In these cases the input to the processor is analog. To process such kind of signals we require low-noise amplifiers (LNAs), variable gain amplifiers (VGAs), filters, oscillators and mixers.

After digitisation we use digital signal processing methods. Hence the processor in these cases is neither analog nor digital rather they are mixed case of the two. A few of the application of mixed mode signal processing are:-

Data and biomedical instrumentation

Sensor interfaces such as airbags and accelerometers.

1.4 CURRENT MODE AND VOLTAGE MODE SIGNAL PROCESSING

Signal processing techniques can be dividing into current and voltage mode techniques in addition to analog, digital and mixed mode techniques.

The above two methods are described as follows:

1.4.1 Current mode signal processing

In this mode of signal processing, current is used as a signal parameter. As current is employed as the signal parameter the voltage swing becomes limited. This results in increased signal handling capability even at reduced supply voltages which makes it suitable to be employed in mixed analog-digital IC's operating at supply voltages of 3.3V. Current-mode circuits have been receiving significant attention in analogue signal processing circuits [9, 13]. A new amplifier called the current feedback amplifier (CFA) [10, 11] has been realized to circumvent the finite-gain-bandwidth limitation of the conventional operational amplifier. It can provide not only constant band-width independent of the closed-loop gain but also high slew rate (i.e. 2000

V/us) [11]. It can be also used as a second generation current conveyor (CCII) [3] by using its compensation node [12].

Current mirror, current copier and switched current filters are some of the building blocks used in the implementation of current mode signal processing [5-7]. An example of current mode signal processing is D/A and A/D Converters. D/A conversion require the weighted addition of identical signal quantities, the implementation of which can be classified into one of the three basic categories: Current scaling, voltage scaling and charge scaling. Among these, current scaling is preferable with regard to speed and linearity. This can be implemented, employing R/2R precision resistor networks in conjunction with n equal current sources, for an n-bit conversion. In order to dispense with the need for thin film resistors and laser trimming, arrays of equal MOS current sources have been used [7], but create problems of linearity if one tries to reduce current levels in order to lower dissipation, due to increased mismatch between the MOS unit current sources. But if lateral bipolar transistors are used, instead of the MOSFET'S, for the realization of the unit current sources [8], mismatch among them can be significantly reduced, since mismatch between bipolar devices does not increase at low current levels.

1.4.2 Voltage mode signal processing

In this mode of signal processing, voltage is used as a signal parameter. Since most of the quantities in electrical system are represented in the form of voltage, it is the dominant mode of signal processing. This might sentimentally be identified with the advent of the triode vacuum tube. In grounded-cathode amplifiers, its grid voltage, with near-zero grid current, modulated the anode current, filter design [8]. This was converted back to voltage mode by the anode load impedance for use by later stages: the tube current was an incidental variable. However, the persistence of voltage mode up to the present has much stronger practical justifications, chiefly in the matter of power sources. Voltages can readily be probed by instruments to be displayed and accurately measured without breaking circuit branches. Even when hiding behind finite impedance, they can drive other compatible circuit switch only a moderate effect on their magnitude. They are of obvious importance in both analog and digital practice.

1.5 CONCLUSION

In Chapter 2, Non-linear circuit have been discussed using off the shelf-available building blocks such as AD844 (CFA), CA3080 (OTA), µA741 (Op-Amp)

In Chapter 3, Trans-linear(TL) circuit principle have been discussed and non-linear circuit based on TL principle using bipolar transistor such vector magnitude calculator, four quadrant multiplier, sine wave generator are implemented.

In Chapter 4, Non-linear circuits are implemented using CMOS technology (low power consumption) such as squarer, multiplier, adder (used in multiplier circuit) have been discussed.

In Chapter 5, Conclusion and future scope of presented work is discussed.

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CHAPTER-2

NON-LINEAR SIGNAL PROCESSING CIRCUITS USING OFF THE SHELF AVAILABLE BUILDING BLOCKS

INTRODUCTION

Extensive literature survey reveals that a large number of active building blocks (ABB) has been realised till now [1-3]. Many useful non-linear signal processing circuits have been realised from these ABB also [4-6]. Some significant ABB's are uA741, AD844 and CA3080. In this chapter, a brief description of these IC's has been presented. Along with this, some important non- linear signal processing circuits realised from these ABB's have been described in this chapter i.e. log and antilog amplifier, multiplier, divider etc.

2.1 OPERATIONAL AMPLIFIER:

The heart of the analog building block for non-linear signal processing is a device called voltage operational amplifier (VFA) more popularly known as op-amp. A very commonly used internally compensated op-amp which may be found in many less demanding signal processing applications in uA741. It can be used to perform many useful mathematical operations such as multiplication, subtraction, division, integration, differentiator etc. of the input signals [7]. The most important application of the op-amp is as an amplifier. Some of the important characteristics of this VFA are:

1. High gain (of the order of a million)
2. High input impedance, low output impedance ($R_O \approx 100\Omega\,, R_i \approx 1M\Omega$)
3. Use with split supply, usually +/- 15V
4. Use with feedback, with gain determined by the feedback network
5. Bandwidth(1MHz) and slew rate(0.5V/µsec.) are limited

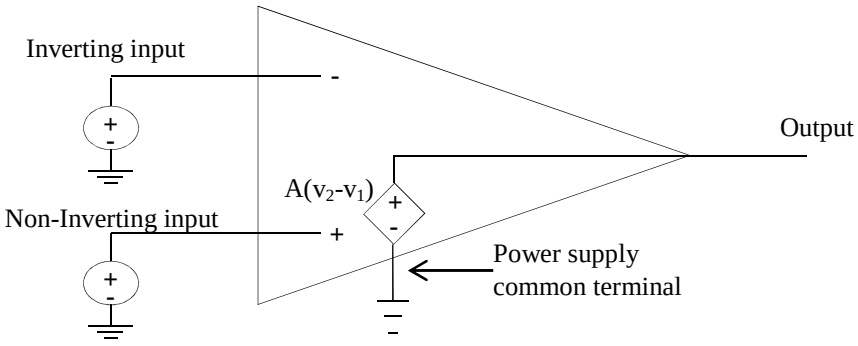


Figure 2.1 Micromodel of VFA

2.2 LOGARITHMIC AMPLIFIER

A logarithmic Amplifier is a circuit which provides output in the logarithmic form of the provided input signal. The following op-amp circuit can be used as a logarithmic amplifier.

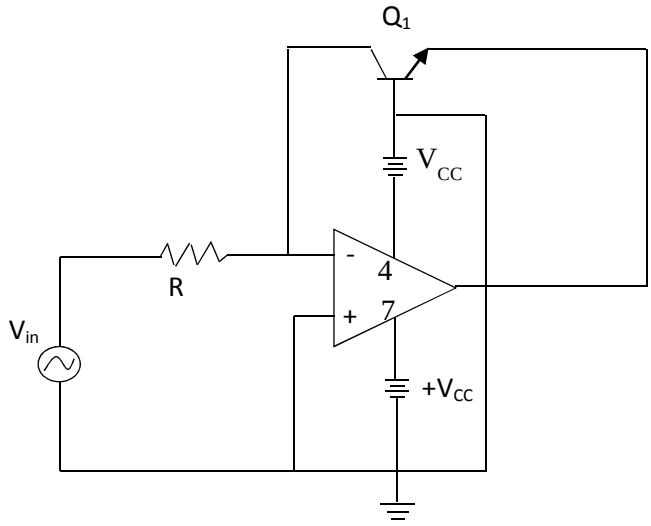


Fig. 2.2 Logarithmic Amplifier using uA-741

$$V_{BE} = -V_{out} \tag{2.1}$$

$$I_c = I_{so}.e^{[(\frac{V_{BE}}{V_T})-1]} \tag{2.2}$$

$$V_{BE} = V_T \ln(I_c/I_{so}) \tag{2.3}$$

Where I_{so} is the saturation current of the emitter-base diode and V_T is the thermal voltage of the transistor 2N2222.

Due to the virtual ground at the op amp differential input,

$$I_c = V_{in}/R_1$$

And

$$V_{out} = -V_T \ln(V_{in}/I_{so}R_1) \tag{2.4}$$

Simulation Result of Logarithmic Amplifier

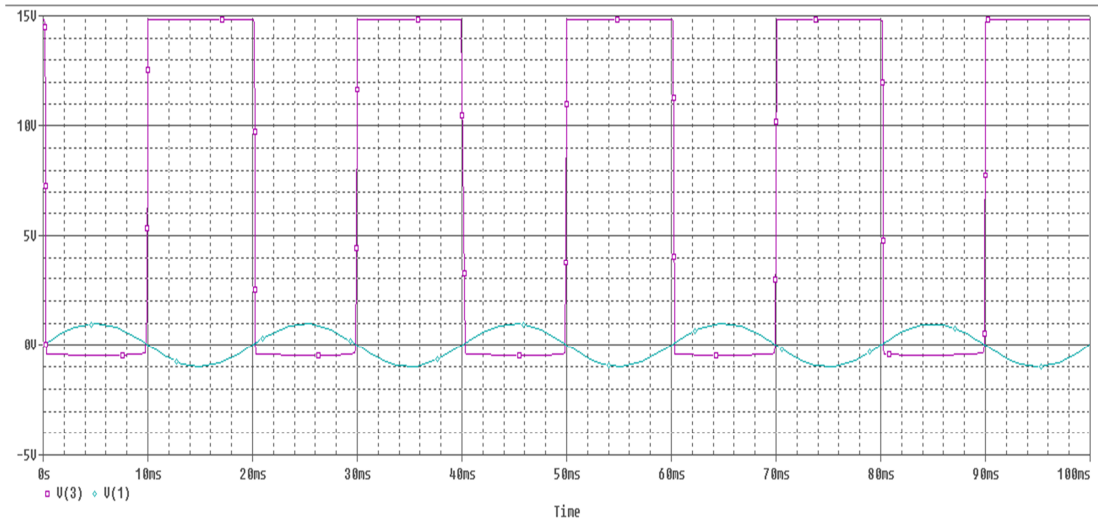
The circuit shown in fig. 2.2 was simulated in PSpice with the following values of input voltage and frequency

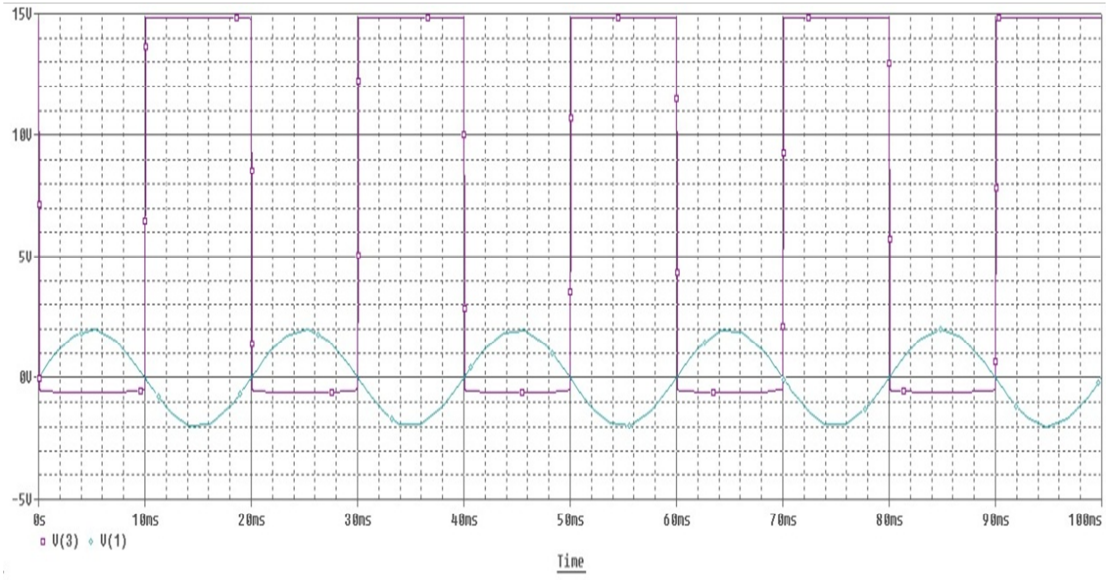
The output of the above logarithmic amplifier shown in fig. 2.3 for different values of voltages and R_1

When input at inverting terminal is 1V sine wave with 50 Hz frequency, R_1=1K output result is logarithmic of that sine wave shown in fig. 2.3(a)

When input at inverting terminal is 2V sine wave with 50 Hz frequency, R_1=10K output result is logarithmic of that sine wave shown in fig. 2.3(b)

When input at inverting terminal is DC sweep from 0.1V to 10V shown in fig. 2.3(c), R_1=1K output result is logarithmic, shown in fig. 2.3(d)





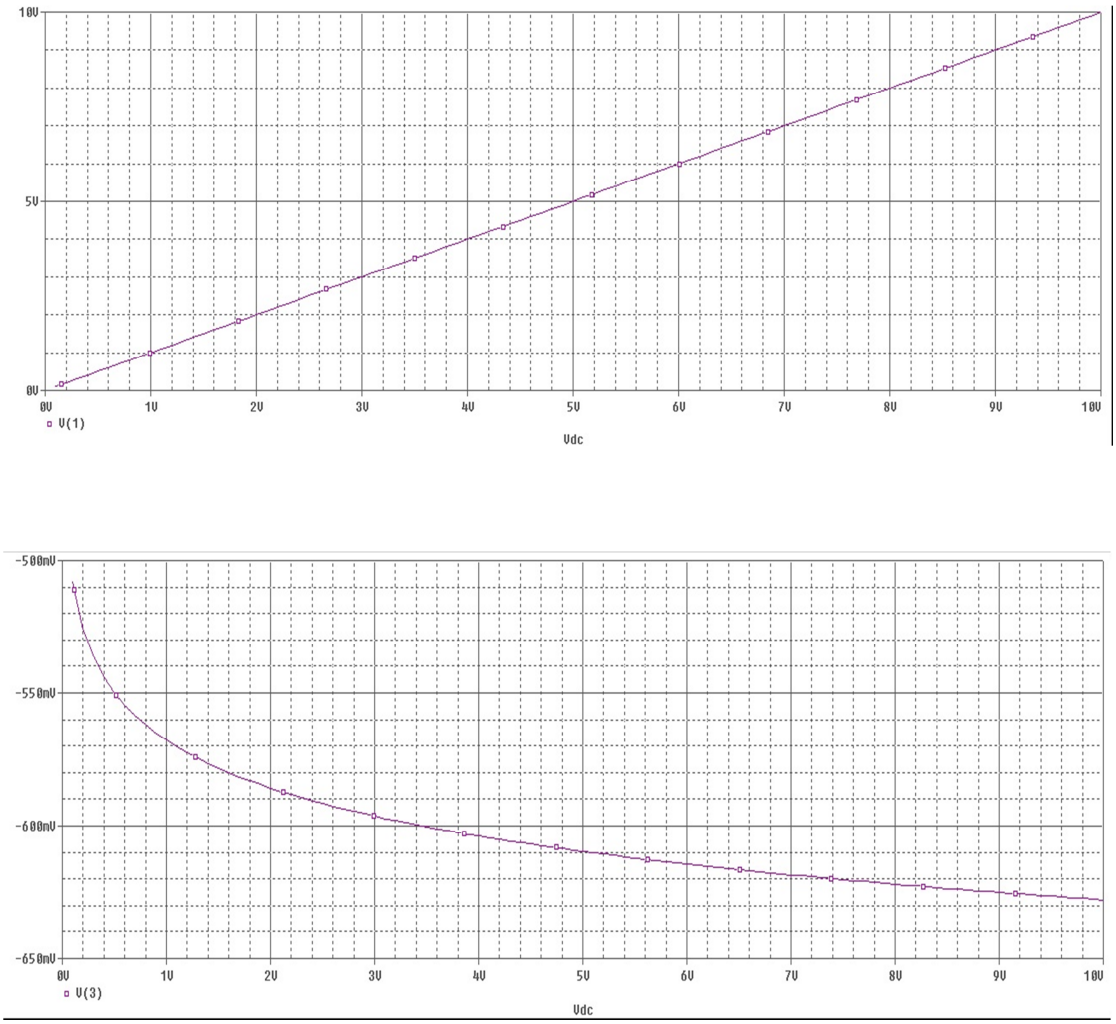


Fig. 2.3(a), (b), (c) & (d) simulation results of Logarithmic Amplifier using uA-741

The output voltage is expressed as the natural log of the input voltage. Both the saturation current I_{so} and the thermal voltage are temperature dependent, hence, temperature compensating circuits may be required.

2.3 ANTILOGARITHMIC OR EXPONENTIAL AMPLIFIER

An Antilogarithmic or Exponential Amplifier is a circuit which provides output in the exponential form of the provided input signal. The following op-amp circuit can be used as an antilogarithmic amplifier.

The relationship between the input voltage V_{in} and the output voltage V_{out} is given by:

$$V_{out} = -R.I_{so}.e^{(V_{in}/V_T)} \quad (2.5)$$

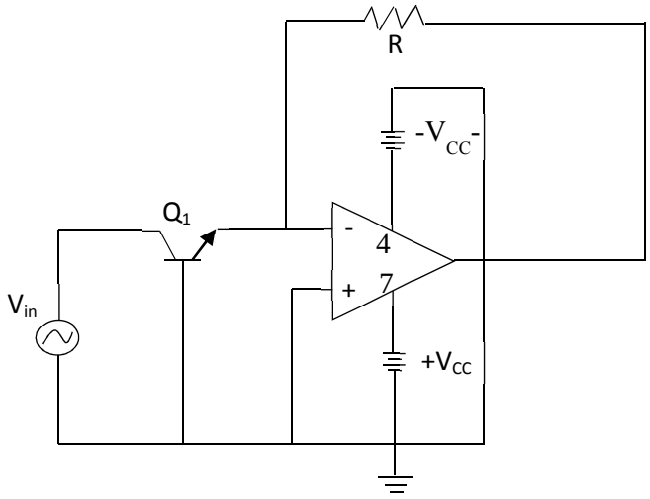


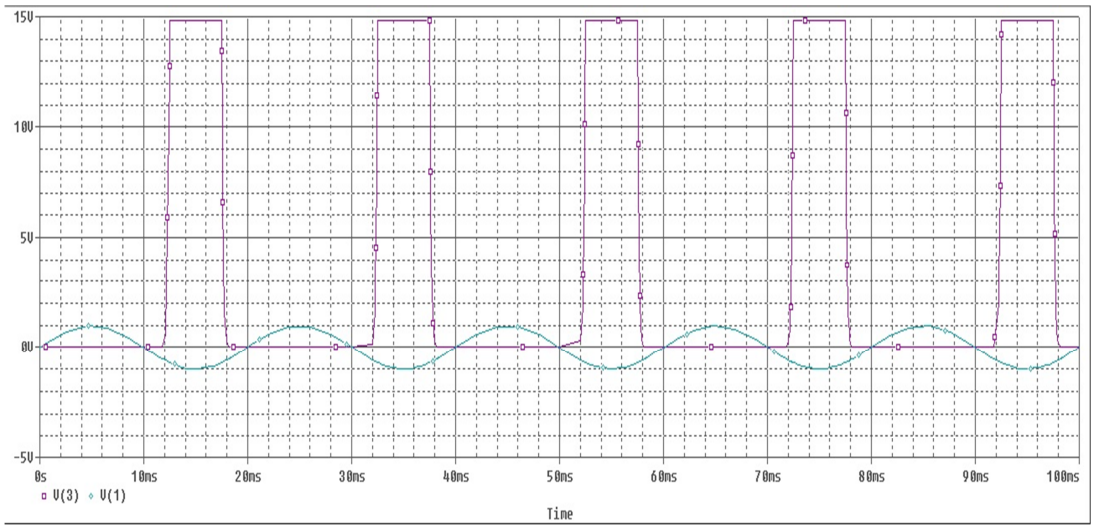
Fig. 2.4 Antilogarithmic amplifier using uA-741

Where I_{so} is the saturation current of the emitter-base diode and V_T is the thermal voltage of the transistor 2N2222.

Simulation Result of Antilogarithmic Amplifier

When input inverting terminal is 1V sine wave with 50 Hz frequency, R_1=1K out result is antilogarithmic of that sine wave shown in fig. 2.5(a)

When input inverting terminal is 2V sine wave with 50 Hz frequency, R_1=10K out result is logarithmic of that sine wave shown in fig. 2.5(b)



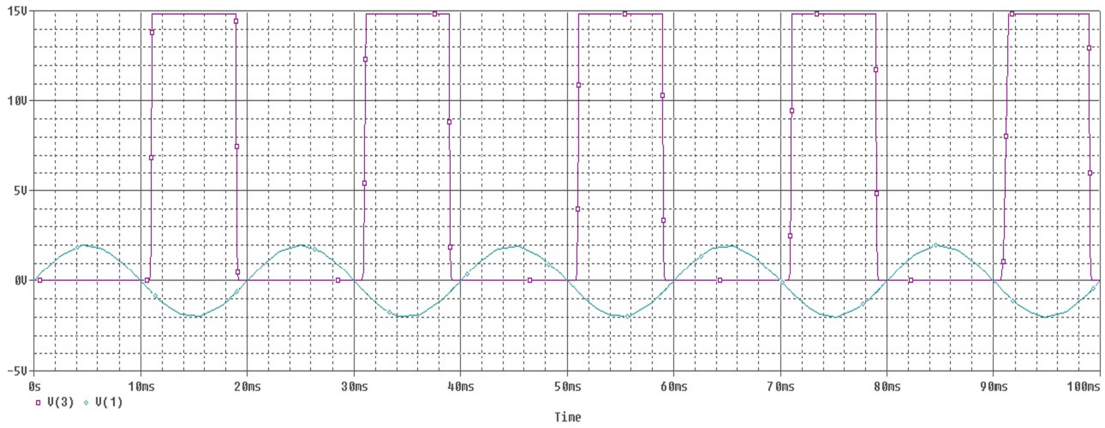


Fig. 2.5(a) & (b) simulation result of antilogarithmic circuit using uA-741

2.4 OTA (CA3080A)

It is well accepted that an OTA is one of the essential active building blocks in the design of analog circuits such as, for example, active filters, active networks and oscillators [8, 9]. This is due to the fact that an OTA is a low-cost device that has only a single high-impedance node and its transconductance gain g_m can be linearly controlled by means of an external bias current. The implementation of analog circuits in such a way that employs only OTA as standard cells will not only be easily constructed from readily commercial available IC, but also significantly simplified the design. In addition, the OTA-based circuit that requires no external passive element would facilitate its integrate-ability and programmability [10]. Although, in the past, circuit techniques that employ OTAs to implement analog multiplier have been presented [11-12], however, they are voltage-mode circuits, only multiplication functions are realized, and the circuit bandwidths are only about 2MHz .A current mode temperature compensated multiplier circuit using OTAs as active circuit elements has been presented [13].

OTA is a differential VCCS (Voltage Controlled Current Source) in which output current is controlled by input voltage source and it is characterized by transconductance (g_m). The output current of the OTA is given (refer the reference [14] for details) by the following equation

$$I_o = g_m(V_+ - V_-), \tag{2.6}$$

Where V_+ and V_- are voltages on non-inverting and inverting input terminal of OTA. The block-diagram of OTA is shown in figure 2.6.

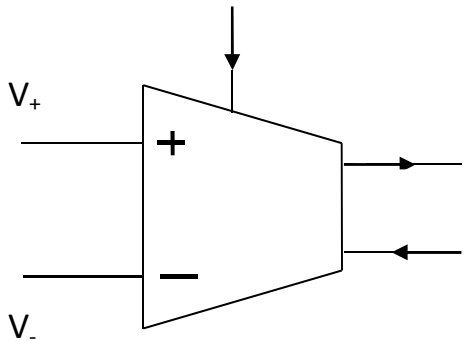


Fig 2.6 OTA Block-Diagram

The trans-conductance is taken such as below

$$g_m = \sqrt[2]{(\mu_n C_{ox} \frac{W}{L} I_b)} \tag{2.7}$$

$$g_m = \frac{I_C}{2V_T} \tag{2.8}$$

Where μ_n, C_{ox}, W/L and I_b are the electron mobility of NMOS, gate oxide capacitance per unit area, transistor aspect ratio and bias current of the OTA, respectively. In above equation, it can observe that the transconductance g_m is adjustable by a supplied bias current I_b.

2.4.1 Ideal Characteristics

Characteristics of ideal OTA (details are cited in reference [14]) can be summarized as below:

Input impedance (Z_{in})= ∞, Output Impedance (Z_0) = ∞, Bandwidth = ∞ .

2.4.2 Schematic Circuit Diagram

Fig. 2.7 shows the complete schematic of OTA using MOS transistors [2].

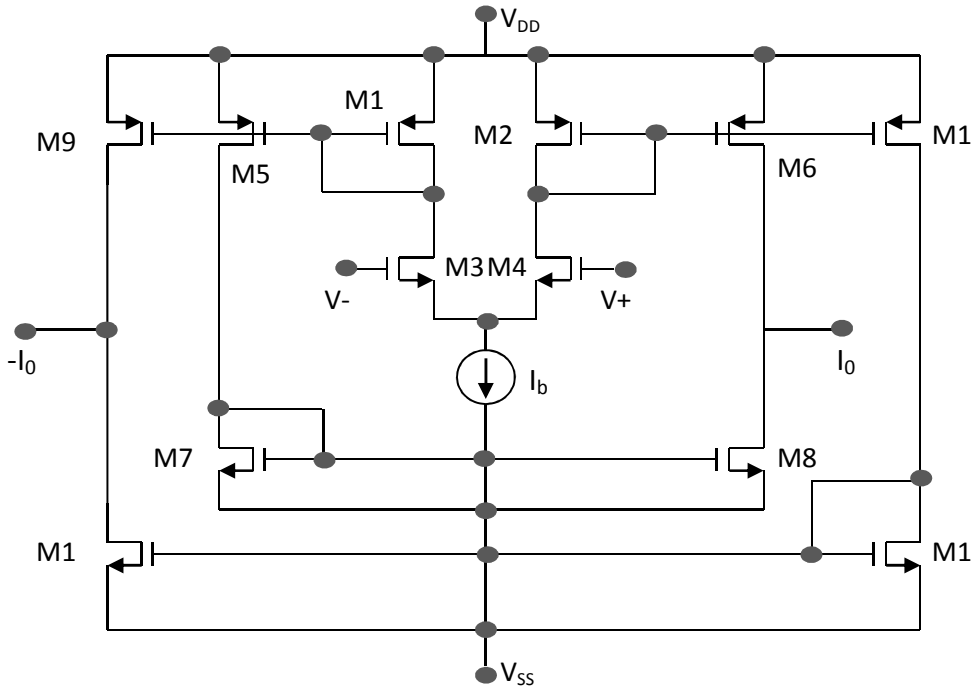


Fig 2.7 Complete Schematic Diagram of OTA

2.4.3 Two quadrant Multiplier circuit using OTA

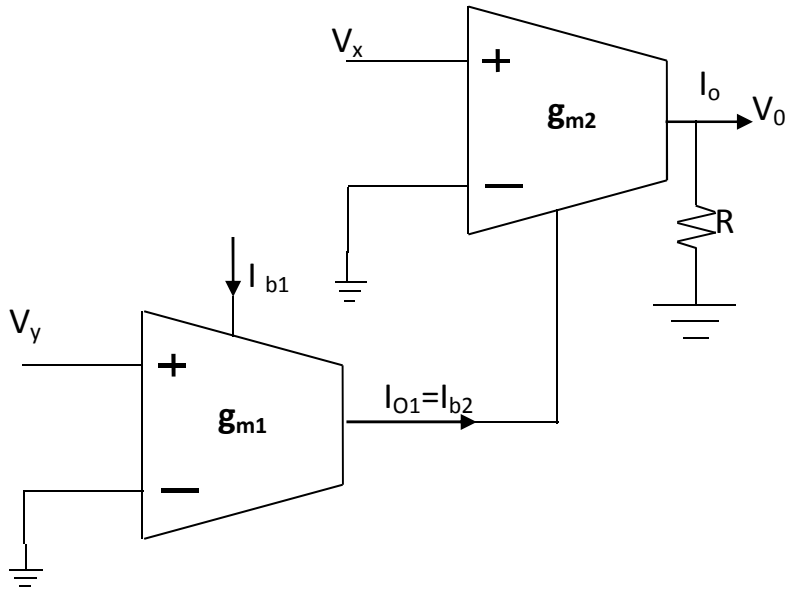


Fig. 2.8 Two quadrant Multiplier circuit using OTA

Where V_x and V_y are two input of two OTA at non-inverting terminal.

Since output current equation of OTA as equation (1) state

$$I_{o1} = g_{m1} V_y \tag{2.8}$$

And $g_{m1} = I_{b1}/2V_T$

For second OTA,$I_{b2} = I_{o1}$ this implies $g_{m2} = I_{b2}/2V_T$

Output of second OTA

$$I_{o2} = g_{m2}V_x \text{ and } I_{o2} = V_xV_yg_{m1}/2V_T \quad (2.9)$$

The input voltage of V_x and V_y is $\pm 50mV$

Simulation result of OTA multiplier

The circuit shown in fig. 2.9 was simulated in P-Spice for different values of g_m with the following Macro model of OTA.

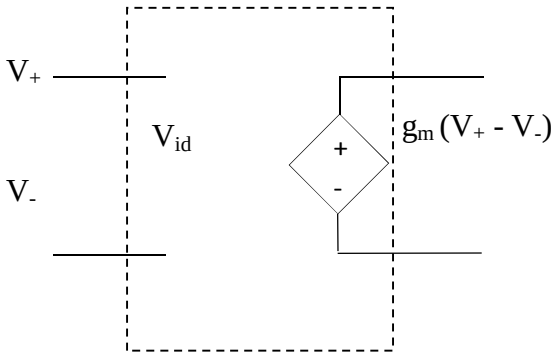


Fig. 2.9 macro model of OTA

The implementation of two quadrant OTA(CA3080) multiplier is done for following values

g_m = 2.75 mΩ^{-1}, setting the value of g_m using 100K potentiometer

and output resistance is 150 Ω. For these values input and output of multiplier is shown in Table 1

Table 1

Vy = 16.6 mV		**Vy = 20.7mV**		**Vy = 38.4 mV**		**Vy = 20.7 mV**		**Vy = 27.0 mV**		**Vy = 38.4 mV**	
Vx (mV)	**Vo (mV)**	**Vx (mV)**	**Vo (mV)**	**Vx (mV)**	**Vo (mV)**	**-Vx (mV)**	**-Vo (mV)**	**-Vx (mV)**	**-Vo (mV)**	**-Vx (mV)**	**-Vo (mV)**
10.4	2.6	10.4	2.8	10.3	3.6	12.0	0.3	11.0	0.1	11.2	0.2
12.3	3.1	14.5	3.8	13.4	4.7	16.8	1.6	12.4	0.5	15.4	1.6
14.7	3.7	18.4	4.8	19.4	6.6	19.7	2.4	13.4	0.8	20.0	3.3
17.2	4.2	22.2	5.7	22.2	7.5	23.2	3.3	18.0	2.2	24.6	4.8
20.8	5.0	24.1	6.1	25.7	8.6	25.9	4.1	20.7	3.0	26.5	5.2
24.6	5.9	25.9	6.5	29.0	9.4	28.6	4.6	21.8	3.3	29.8	6.5
29.0	6.7	28.1	7.0	31.9	10.2	30.5	5.1	27.3	4.9	32.3	7.1
34.8	7.8	30.5	7.5	34.2	10.8	32.0	5.5	32.1	6.2	34.8	8.0
38.8	8.5	34.4	8.3	37.4	11.5	34.5	6.0	37.6	7.6	37.0	8.7
41.8	8.9	37.0	8.8	40.7	12.3	40.0	7.2	40.0	8.1	39.9	9.5
46.2	9.5	44.1	10.0	45.0	13.0	44.2	8.0	44.1	9.1	44.0	10.6

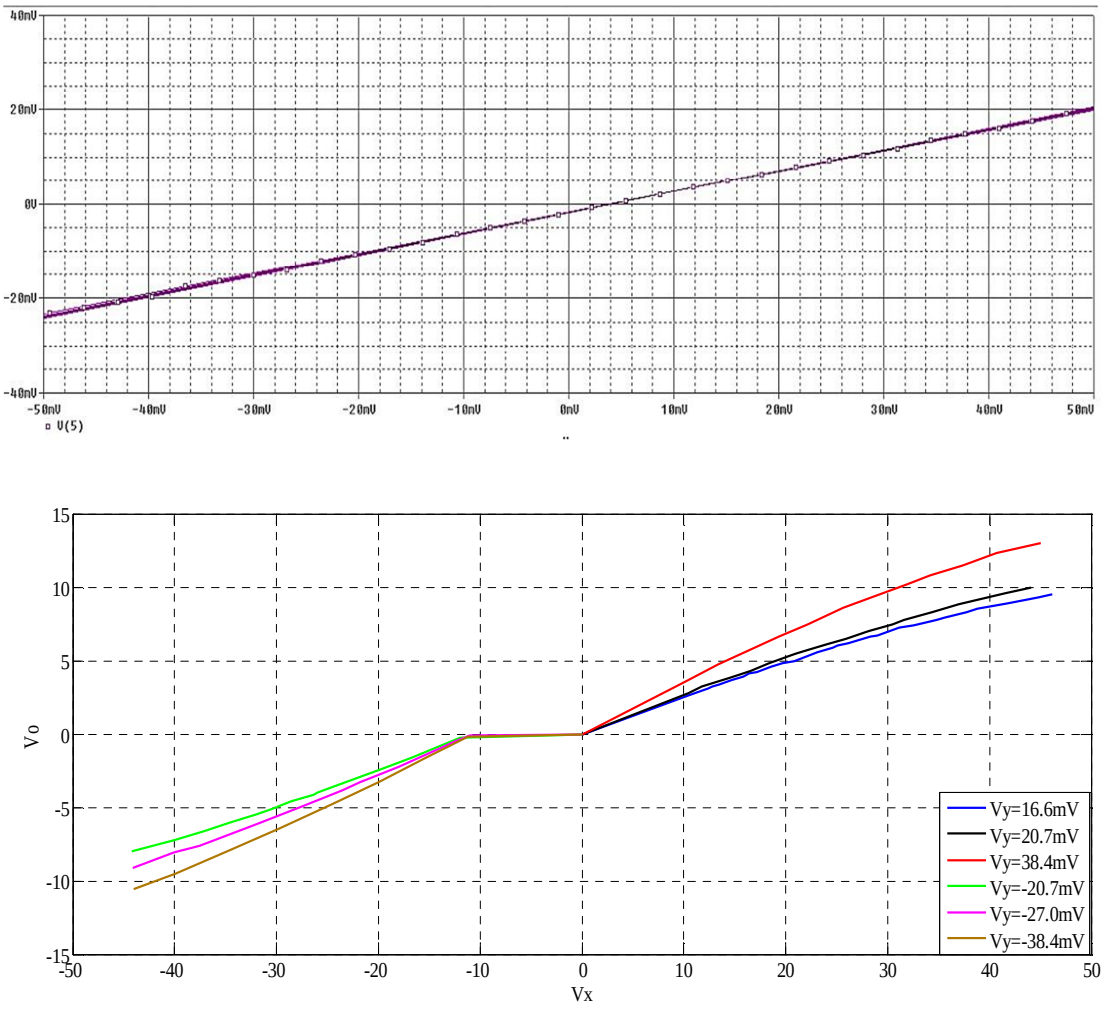


Fig. 2.10 OTA multiplier output (a) Simulation (b) Experimental

2.5 CURRENT FEEDBACK AMPLIFIER

Recently, the current feedback operational amplifier has become more popular and is widely being used in the electronics and telecommunications industries. It offers some very good features over the voltage feedback operation amplifier. The two great features of the CFA are improved slew rate and decoupling of closed loop of bandwidth and gain for low to medium values of gain [16- 18]. This device can be operating in both current and voltage modes, provides flexibility and enables a variety of circuit designs. In addition, it provides very advantageous features such as high slew rate, free from parasitic capacitances, wide bandwidth and simple implementation [19]. Presently the CFA can be commercially found, for example AD844 of Analog Devices Inc. [23]. It can be employed to realize filters, amplifier, oscillators, inductance, simulators etc. [20].

Although the CFA is better than the VFA in slew rate and bandwidth, the CFA has some disadvantages. These are the input offset voltage (V_{OS}), input offset current (I_{OS}), common mode input range (CMIR), common mode rejection ratio (CMRR), power supply rejection ratio (PSRR), and open loop gain. VFAs are generally used for precision and general purpose applications. CFAs are used in high frequency applications especially over 100MHz.

The port relationship of CFA are given by shown in following equation

$$\begin{bmatrix} V_X \\ I_Y \\ I_Z \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_Y \\ V_Z \\ I_X \end{bmatrix} \text{and} V_O = V_Z \tag{2.10}$$

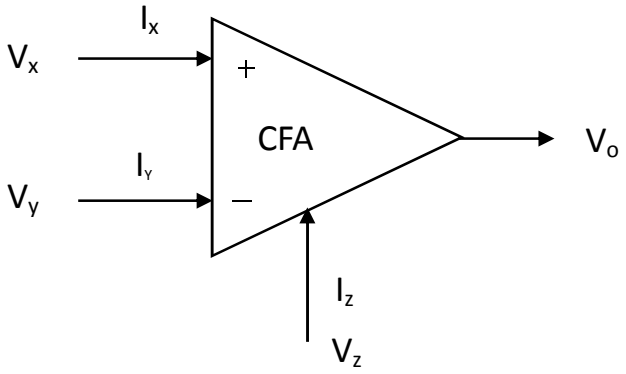


Fig. 2.11 Block diagram of CFA

2.5.1 Multiplier circuit using CFA

The analogue multiplier circuit with two CFAs is shown in Fig. 2.12. It consists of two CFAs, eight NMOS transistors biased in the triode region. The drain current of an NMOS in triode can be expressed by [21].

Basic multiplier circuit

Figure 2.14 shows CFA based multiplier circuit. The transistors M_1, M_2, M_3, and M_4 are matched transistors and operate in the triode region. CFA inputs keep the sources of the two transistors M_1 and M_2 virtually grounded. The drain current for the MOS transistor operating in triode region is given by

$$I_D = k\frac{W}{L}((V_{GS} - V_T) - \frac{I_D V_{DS}}{2}))V_{DS} \tag{2.11}$$

$$I_D = k\frac{W}{L}(V_{GS} - V_T)^2 \tag{2.12}$$

Using equation (2.11, 2.12) the currents through and terminals of CFA, that is respectively, can be expressed as approaches infinity the input currents are forced to be equal resulting in where is a proportionality constant and is the inverse of difference of gate voltages of M_3 and M_4.

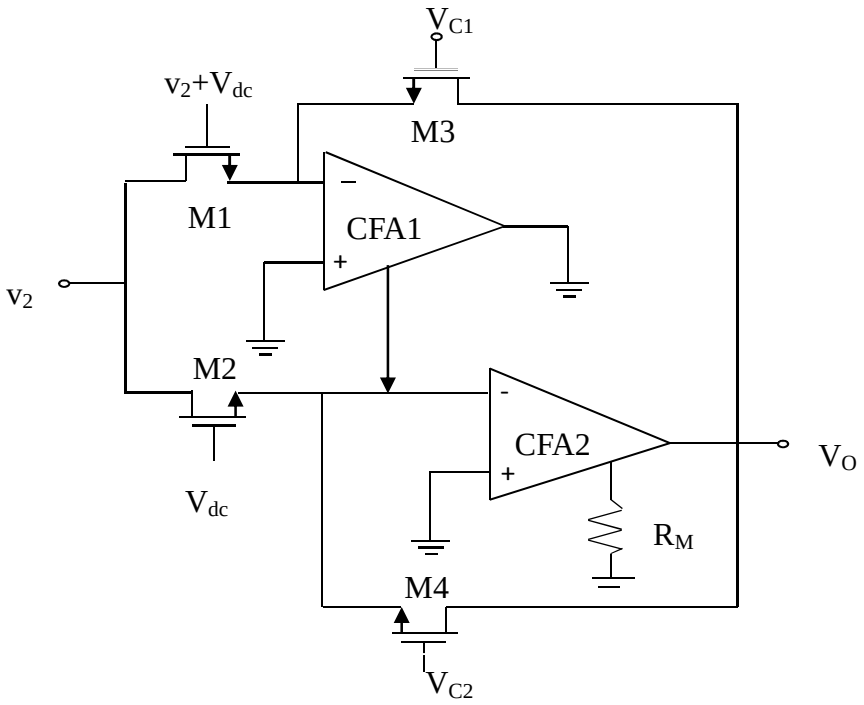


Fig. 2.12 Multiplier circuit using CFA [21]

So current through low impedance terminal of CFA1 and CFA2 is represented by I_{X1} and I_{X2} respectively. Since drain of M_1, M_3 and M_2, M_4 are connected to low impedance terminal of CFA1 and CFA2 which are biased so they would operate in triode region. So current terminal X1 and X2 of CFA will be

$$I_{X1} = k\frac{W}{L}((V_{DC} + v_1 - V_{TN}) - \frac{v_2}{2}))v_2 + k\frac{W}{L}((V_{C1} - V_{TN}) - \frac{V_O}{2}))V_O \qquad (2.12)$$

$$I_{D2} = k\frac{W}{L}((V_{DC} - V_{TN}) - \frac{v_2}{2}))v_2 + k\frac{W}{L}((V_{C2} - V_{TN}) - \frac{V_O}{2}))V_O$$

So current at terminal X2 will be difference I_{X1} and I_{D2} we calculated

$$I_{X1} - I_{D2} = k\frac{W}{L}\{v_1 v_2 + V_O(V_{C2} - V_{C1})\} = I_{X2}$$

So voltage across R_m will be $I_{X2}R_m = V_0$ after doing analysis we found that

$$V_O = \frac{KR_m v_1 v_2}{1 + KR_m(V_{C2} - V_{C1})}$$

Where $K = k\frac{W}{L}$

Since we R_m in mega-ohm so after approximation we gate

$$V_O = \frac{v_1 v_2}{(V_{C2} - V_{C1})} \tag{2.13}$$

Here we take $V_{C2} = 1.25V$ and $V_{C1} = 1V$, finally we get multiplier output equation as

$$V_O = \frac{v_1 v_2}{K1} \tag{2.14}$$

2.5.2 Implementation Scheme for Superimposition of a Small Signal on DC Bias

As can be seen from Figure 2.12 the gate voltage of M_1 is $(V_{DC} + v_1)$ which is a small signal superimposed over a dc bias. This voltage addition can be implemented using a scheme in Figure 2.13 where v_x in is a small signal voltage and is a bias voltage.

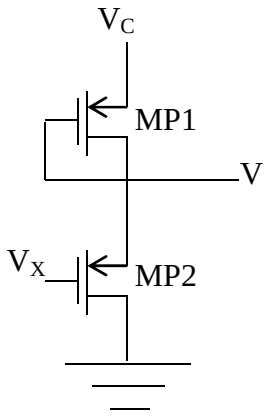


Fig. 2.13 Scheme for implementing an AC superimposed on DC bias

If M_{P1} and M_{P2} are identical transistor and operated in saturation region then their drain currents will be equal resulting in

$$\frac{1}{2}k\frac{W}{L}((v - V_c) - V_{TP}))^2 = \frac{1}{2}k\frac{W}{L}((v_x - v) - V_{TP}))^2 \tag{2.15}$$

which gives,

$$v = \frac{(V_C + v_x)}{2} \tag{2.16}$$

The voltage given by (2.16) can be used as the gate voltage for transistor M_1 of Fig.2.12. Similarly gate voltage for transistor M_2 can be obtained from (2.16) by making v_x = 0. Substituting these values of gate voltages in (2.13) the output of the multiplier gets modified to

$$v_O = K' v_1 v_2 \tag{2.17}$$

Where

$$K' = \frac{K}{2}$$

2.5.3 The MOS based multiplier structure

The complete MOS based multiplier structure is depicted in Fig.2.13 which incorporates the voltage addition scheme of Fig 2.12.

As the transistors M_1, M_2, M_3 and M_4 need to operate in the triode region for proper operation of the multiplier so the following conditions should be satisfied

$$\left(\frac{(V_C+v_1)}{2} - V_{TN}\right) > v_2, \tag{2.18}$$

$$\left(\frac{(V_C)}{2} - V_{TN}\right) > v_2, \tag{2.19}$$

$$(V_{C1} - V_{TN}) > v_O, \tag{2.20}$$

$$(V_{C2} - V_{TN}) > v_O, \tag{2.21}$$

Now using equations (2.16) along with (2.18 - 2.21) the conditions for input signals v1 and v2, can be

$$V_{TP} < v_1 < (V_C + 2V_{TP}), \tag{2.22}$$

$$v_2 < \frac{(V_C+v_1)}{2} - V_{TN}, \tag{2.23}$$

These equation define that the dynamic input range of multiplier circuit controlled by V_C .

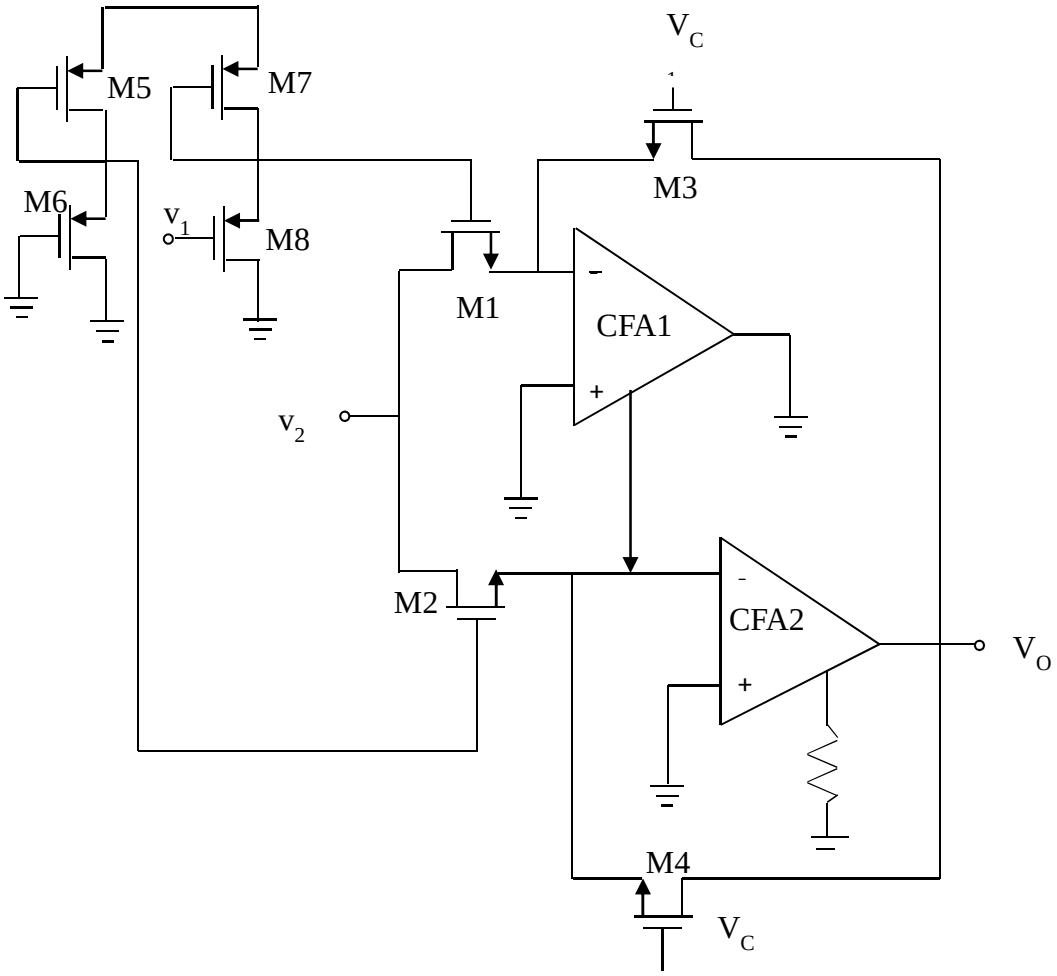


Fig. 2.14 Multiplier Circuit using CFA with DC bias [21]

Simulation results of Multiplier circuit using AD844 (CFA)

The circuit shown in fig. 2.14 was simulated in P-Spice with W/L =1u/0.5u and the following range of input

For DC input range is

$-300\ mV < V_1 < +300\ mV$ and $-150\ mV < V_2 < +150\ mV$

For AC input range is

(1) V_1 =50 mV; V_2 =150 mV with frequency 1 KHz

(2) $V_1 = V_2$ =150 mV with frequency 2 KHz & 5 kHz

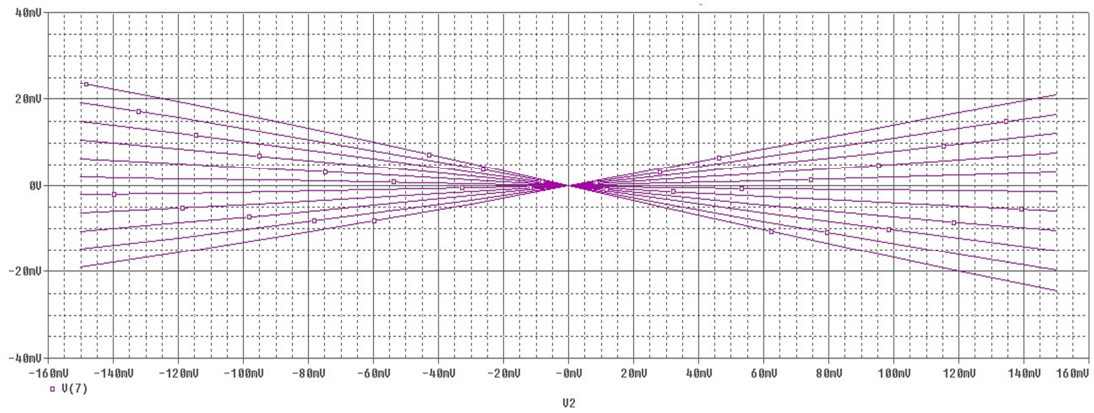


Fig. 2.15 Multiplier output using CFA

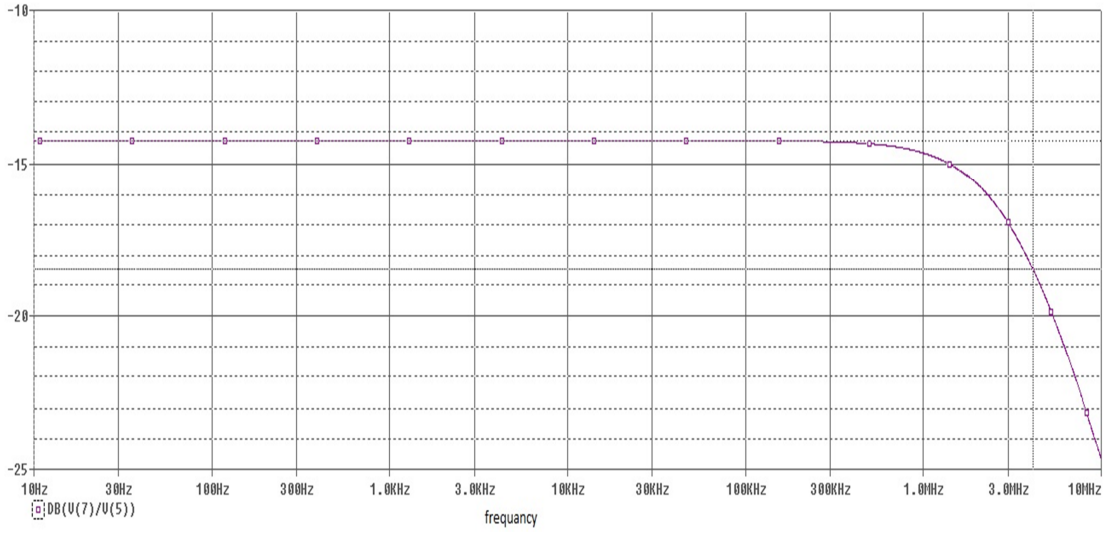


Fig. 2.16 Frequency response of multiplier

Fig. 2.17 Input and Output of multiplier circuit at $f_1=f_2=1$ KHz

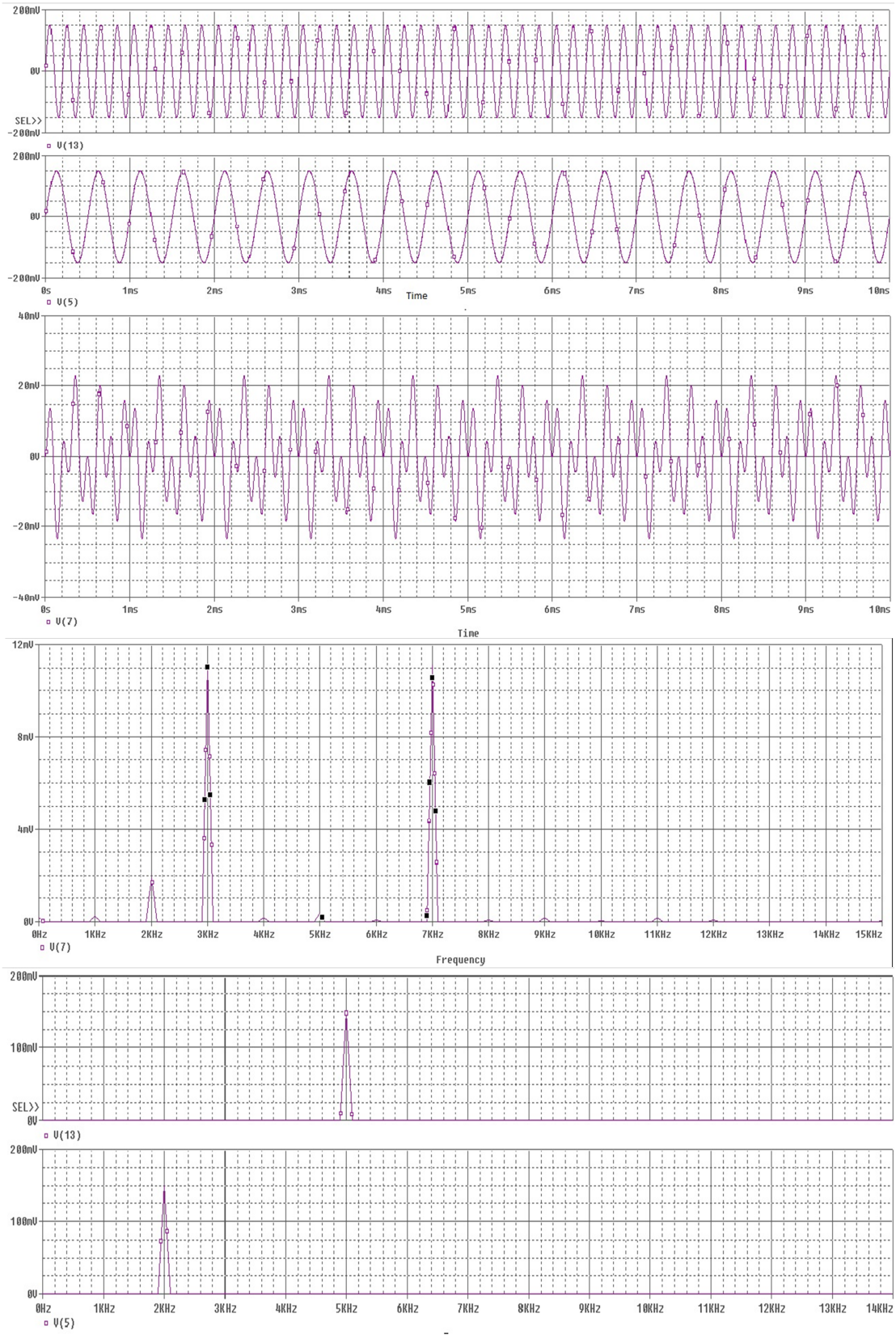


Fig. 2.18 Input and output of multiplier circuit at f_1=2 KHz and f_2= 5 KHz

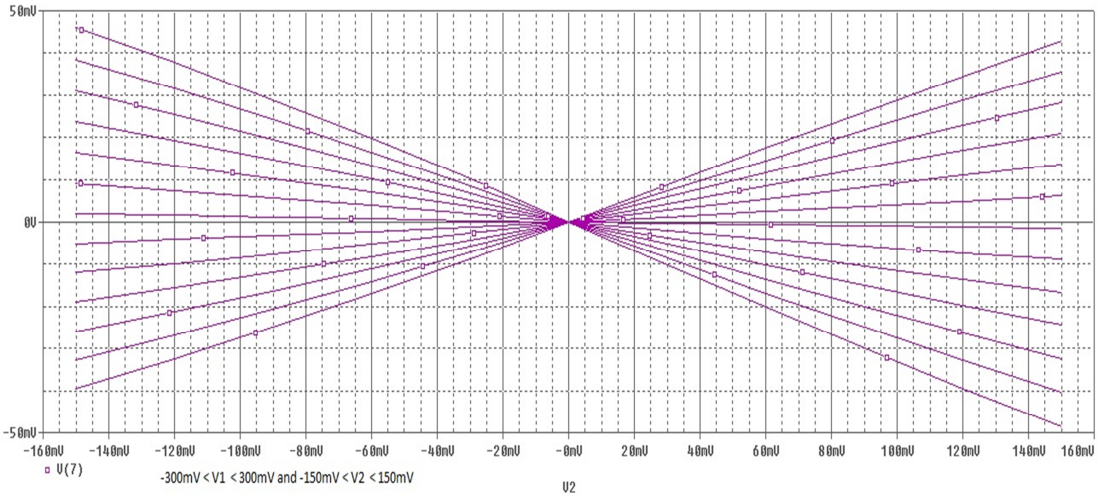


Fig. 2.19 DC response of multiplier circuit using CFA

2.5.4 Divider circuit using CFA

An analog divider is an important building block in analog computation, fuzzy control and instrumentation etc. [1-2]. Many analogue continuous-time and sampled-data divider circuits have been presented in the literature [14-18]. Most of them have used conventional operational amplifiers as building blocks to synthesize the division function. However, the finite-gain-bandwidth product of the operational amplifiers will limit the high frequency operation and accuracy of the divider.

The analog division circuit with two CFAs [5] is shown in Fig. 2.20. It consists of two CFAs, two NMOS transistors biased in the triode region and a resistor. The drain current of an NMOS transistor biased in the triode region can be expressed by [24]

$$I_D = k\frac{W}{L}((V_{GS} - V_T) - \frac{I_D V_{DS}}{2}))V_{DS} \tag{2.24}$$

$$I_X = \frac{V_1}{R} + k\frac{W}{L}((V_G + V_T) - \frac{V_O}{2}))V_O \tag{2.25}$$

$$I_Z = k\frac{W}{L}((V_G + V_T) - \frac{V_O}{2}))V_O \tag{2.26}$$

Since$I_Z = I_X$

$$V_1 = k\frac{W}{L}V_O V_X R$$

$$V_O = \frac{V_1}{KRV_X} \tag{2.27}$$

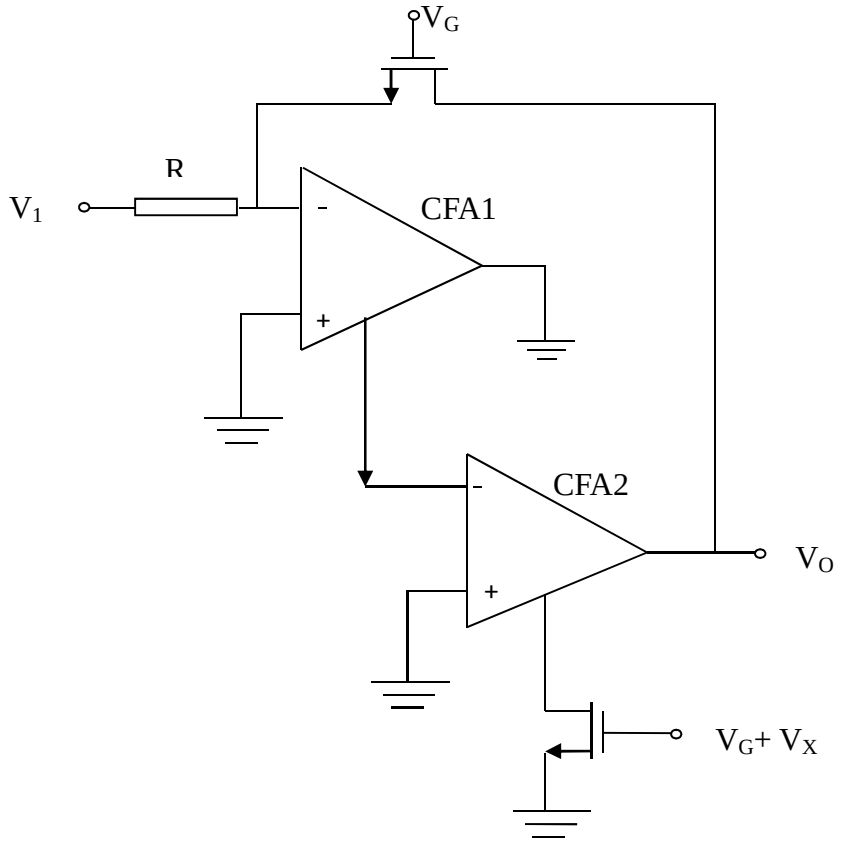


Fig. 2.20 Divider circuit using CFA [5]

Simulation results of Divider circuit

The circuit shown in fig. 2.20 was simulated in P-Spice using CMOS 0.5µm from MOSIS technology with W/L of

M_1=2.5µ/0.1µ

M_2=1.85µ/0.5µ

When V_x varies from -1.1 V to 2 V, the output of Divider circuit is shown in Fig. 2.21

Frequency response of divider circuit is shown in Fig. 2.22 (a) and (b). In Fig. 2.22 (a) frequency response of V_o/V_1 in dB is shown where V_x is DC signal and V_1 is set at 1.1 V AC signal. The -3 dB BW is about 4 MHz.

In Fig. 2.22 (b) frequency response of V_o/V_x in dB is shown where V_1 is DC signal and V_1 is set at 1.1 V AC signal. The -3 dB BW is about 4 MHz.

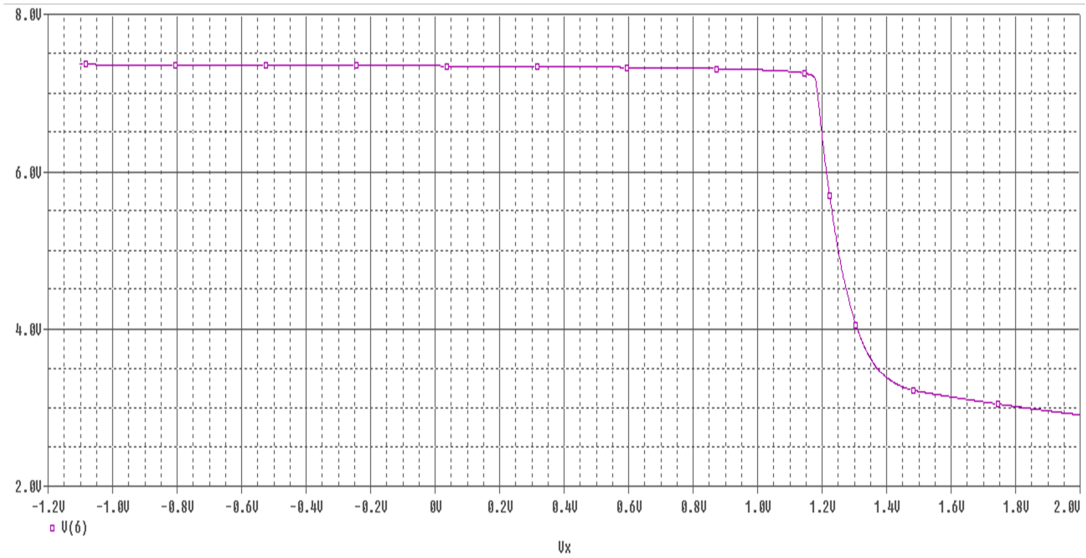


Fig. 2.21 Divider circuit output

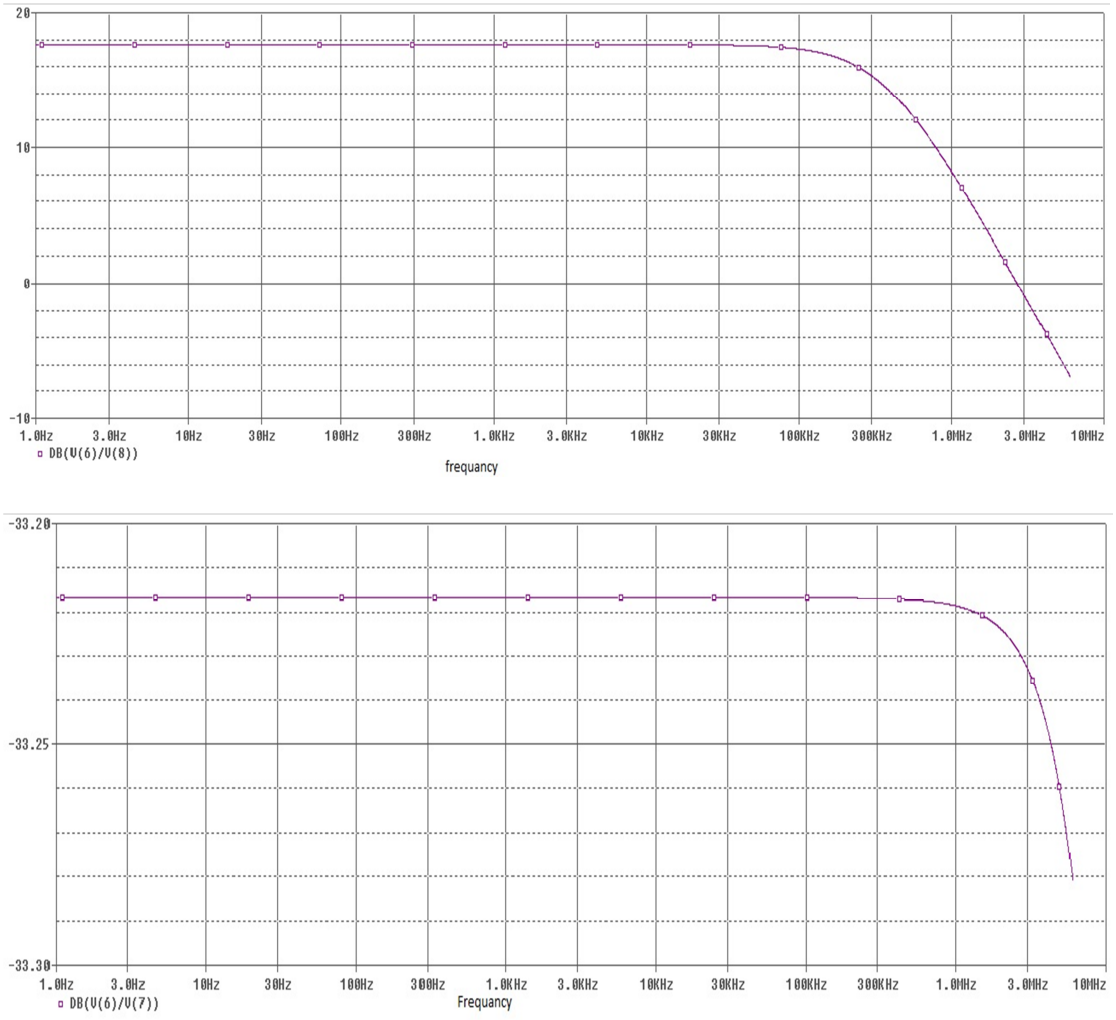


Fig. 2.22 Frequency response of Divider Circuit with (a) V_o/V_1 (b) V_o/V_x in dB

2.6 CONCLUSION

In this chapter; implementation of non-linear signal processing circuits was presented using off-the-shelf available building blocks such uA741, AD844, CA3080. The non-linear circuit implemented was log and antilog amplifier using uA741, multiplier and divider circuits using AD844, two quadrant multiplier using MOS based multiplier circuit, two quadrant multiplier circuit on bread board using IC CA3080.

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CHAPTER-3

IMPLEMENTATION OF NON LINEAR SIGNAL PROCESSING CIRCUITS USING TRANSLINEAR CIRCUIT PRINCIPLE

INTRODUCTION

In previous chapter, Non-linear signal processing circuits were implemented using off-the-shelf available building blocks. In this chapter, translinear circuit principle (TLP) is discussed and a class of non-linear signal processing circuit using TLP is presented i.e. vector magnitude calculator, sine shaper circuit, four quadrant multiplier. The concept was first introduced by Gilbert [1] and is also mentioned in [2], in this approach, the actual nonlinear operation is executed by only one network element: a carrier domain device (CDD). Generally speaking, a carrier domain device is an element comprising an extended bipolar transistor structure where the carrier injection is compressed into a small area (domain) by enforced emitter crowding. In addition, in this domain the signal transfer can be changed by an external variable. Gilbert applied this principle to his new four-quadrant multiplier [3]. To start with, a brief description of the idea of the translinear principle has been presented first followed by a few practical examples.

3.1 TRANSLINEAR PRINCIPLE

In 1975, Barrie Gilbert coined the term translinear by noting that the trans-conductance for a bipolar junction transistor varies linearly with the current. This term also applies to the behaviour of a MOSFET when operated in weak inversion or sub-threshold. An emerging class of circuits, referred to as translinear circuits [3-6], has been shown to provide a solid foundation for building circuits that can compute a large variety of functions. A subset of this class of circuits, known as log-domain filters, has also proven useful for performing various kinds of filtering operations. This principle is stated as:

In a closed loop, containing an even number of translinear elements (TEs) with an equal number of terms arranged clockwise and counter-clockwise, the product of the currents through the clockwise TEs equals the product of the currents through the counter-clockwise TEs or

$$\prod_{n\varepsilon CW} I_n = \prod_{n\varepsilon CCW} I_n \tag{3.1}$$

The TLP is dependent on the exponential current-voltage relationship of a circuit element. Thus, an ideal TE follows the relationship

$$I = \lambda I_s e^{\frac{\eta V}{V_T}} \tag{3.2}$$

where I_s is a pre-exponential scaling current, λ is a dimensionless multiplier to I_s, η is a dimensionless multiplier to the gate-emitter voltage and V_T is the thermal voltage kT/q.

In a circuit, TEs are described as either clockwise (CW) or counterclockwise (CCW). If the arrow on the emitter point clockwise, it's considered a CW TE, if it points counterclockwise, it's considered a CCW TE.

Originally, this concept was based on the fundamental property of bipolar transistors, namely transconductance. This property, when applied in circuits arranged in loops of junction voltages and having inputs and outputs in the form of currents, allows the implementation of exact temperature-insensitive signal processing functions. Gilbert distinguished between translinear circuits of a general kind (simply exploiting transconductance linear with current) and circuits based on Translinear loops.

To generalize, the translinear concept is applied to devices having transconductance linear with an electrical variable such as current or voltage. For the class of devices having transconductance linear with current

$$g = \frac{dI}{dV} = AV \tag{3.3}$$

On integrating

$$I = A\frac{V^2}{2} + B \tag{3.4}$$

When the integration constant B equal to zero, (3.4) represents an MOS transistor operating in strong inversion and in saturation, with I the drain current and V the gate-source drive voltage (V-V_{th}). In brief, a generalized translinear (GTL) circuits is a circuit having inputs and outputs in the form of currents and voltages & whose primary functions arise from the exploitation of the proportionality of transconductance to an electrical variable in certain electronic devices so as to result in fundamentally exact, temperature-insensitive algebraic transformations. When the electrical variable referred to is a current, the devices are bipolar transistors and the circuits are of the well-known bipolar-translinear (BTL) variety. Alternatively, when the electrical variable is a voltage, the devices are field-effect (e.g., MOS) transistors and the circuits can be classified as MOS Translinear (MTL). A third alternative, when the variable is a charge, has not yet been explored; it could possibly lead to an interesting new class of circuits.

3.2 VECTOR MAGNITUDE CALCULATION

The circuit calculated magnitude of vector signal represented by $V_X + iV_Y$ [6]. Here we represented real part of vector signal by V_X and imaginary part by V_Y. So magnitude of that vector signal will be $V_O = \sqrt{V_X^2 + V_Y^2}$ across the resister R_2 as shown in figure 3.4

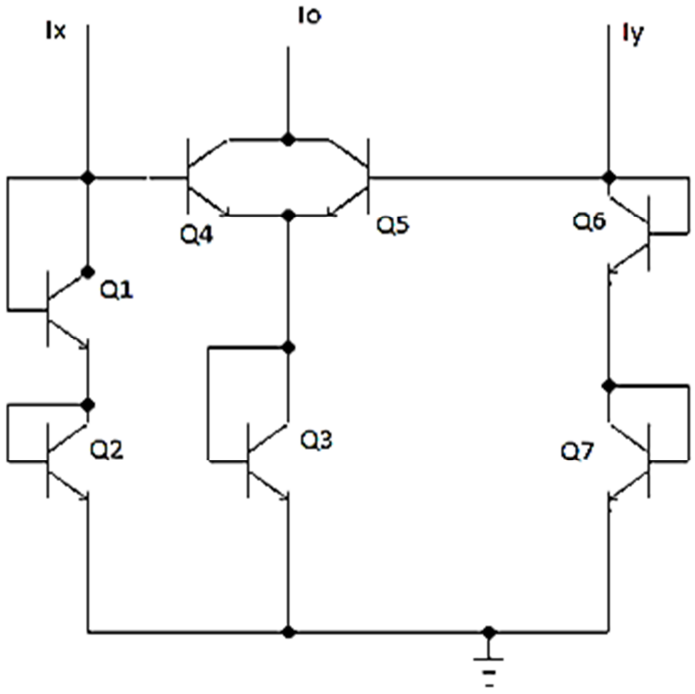

Figure 3.1 Vector Magnitude calculator current mode circuit

For calculation of output voltage we take separate loop current mode vector magnitude calculator where I_X and I_Y are the two input in fig. 3.1. Here we apply the TL principle since are the bipolar transistor are identical. The TL principle applied to loop containing transistor Q1, Q2, Q3 and Q4 gives

$$I_{C1}I_{C4} = I_{C1}I_{C2} = I_X^2 \tag{3.5}$$

Where

$$I_{C3} = I_O$$

For the loop containing Q3, Q5, Q6 and Q7

$$I_{C3}I_{C5} = I_{C6}I_{C7} = I_Y^2 \tag{3.6}$$

For Q4 and Q5

$$I_{C4} + I_{C5} = I_O$$

Combining equation (3.5) and (3.6) into equation

$$I_O = \sqrt{I_X^2 + I_Y^2} \tag{3.7}$$

For voltage mode operation we add additional circuit which make voltage signal into current signal respectively as shown in the figure.

Voltage to current convertor circuit:

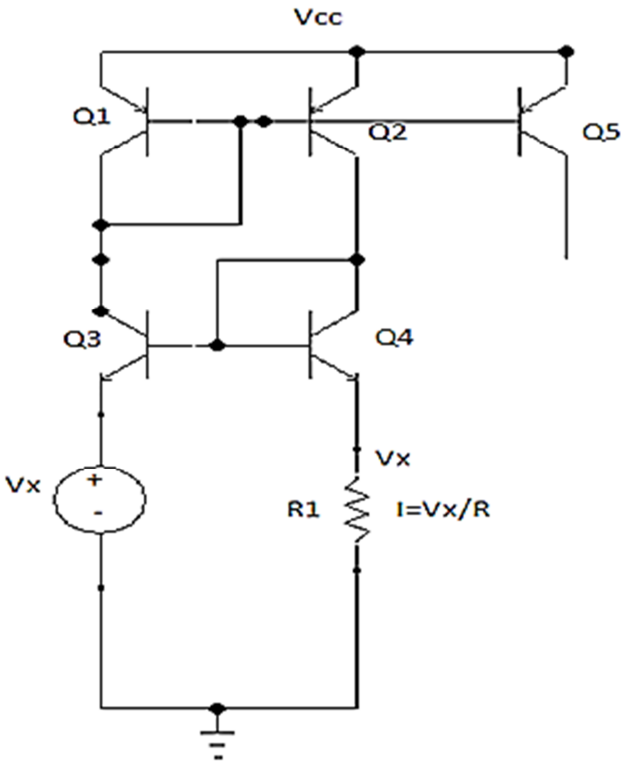

Fig. 3.2 The voltage to current convertor circuit

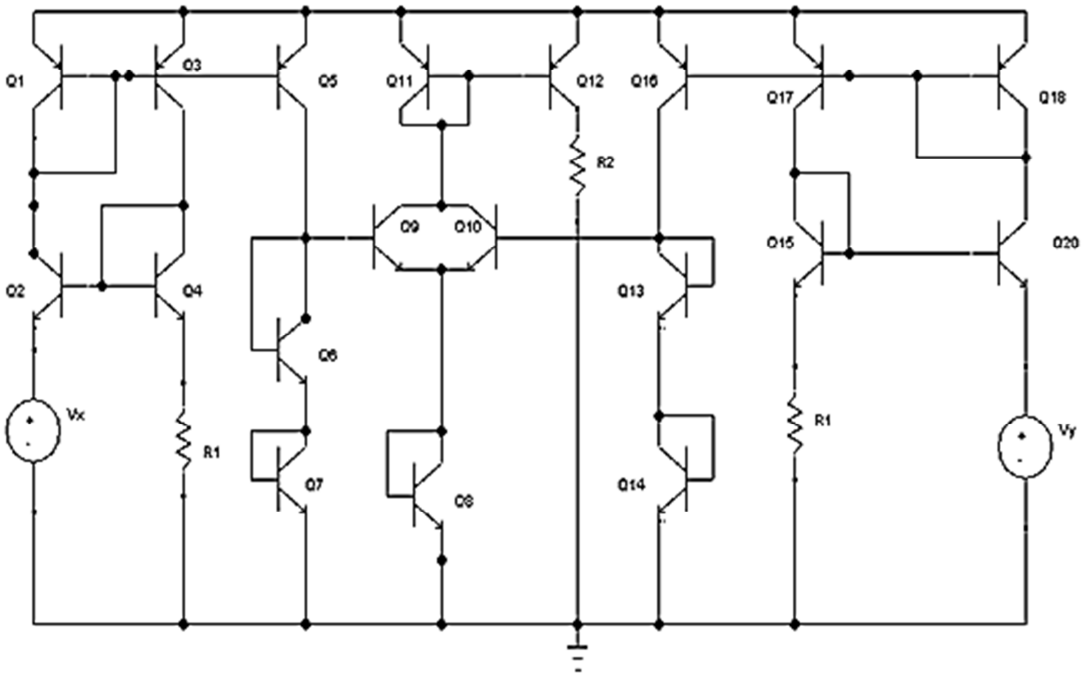

Fig. 3.3 vector magnitude voltage mode circuit [6]

3.2.1 Simulation Result of vector magnitude circuit

The circuit shown in fig.3.4 was simulated in P-Spice using transistor 2N2222 (model parameter given in Appendix A). Simulation results of vector magnitude circuit is shown in figure 3.4when V_X is varies 0V to 2V in step of 0.2V and V_Y kept at 2V. Vector magnitude output shows some variation with theoretical value. Theoretical graph is also plot for same values as given in simulation profile.

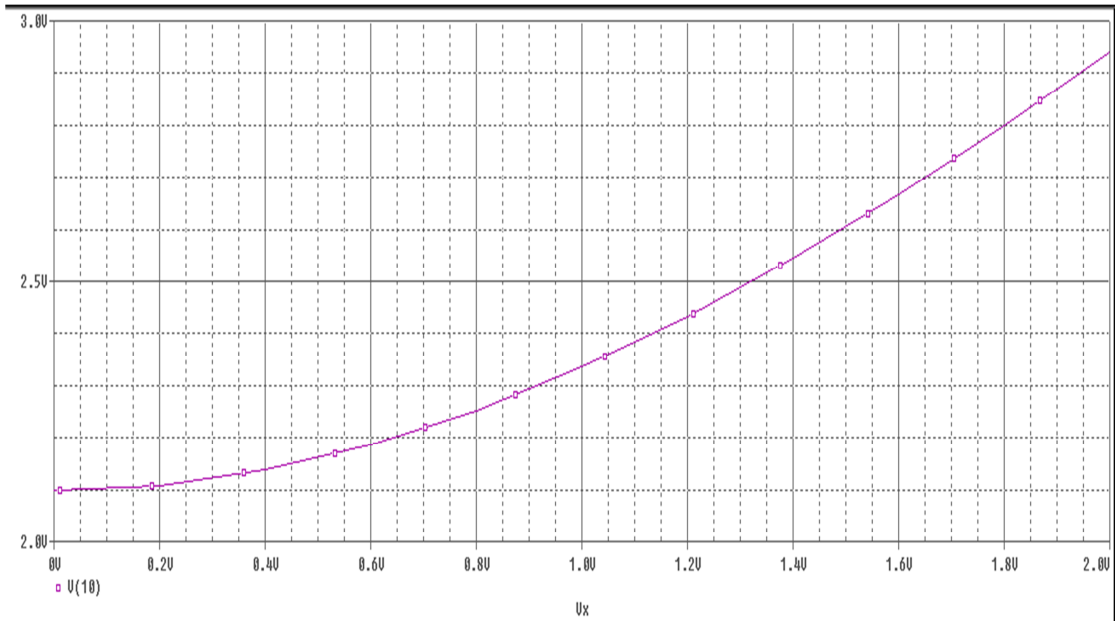

Fig.3.4 (a) simulation output of vector magnitude calculator

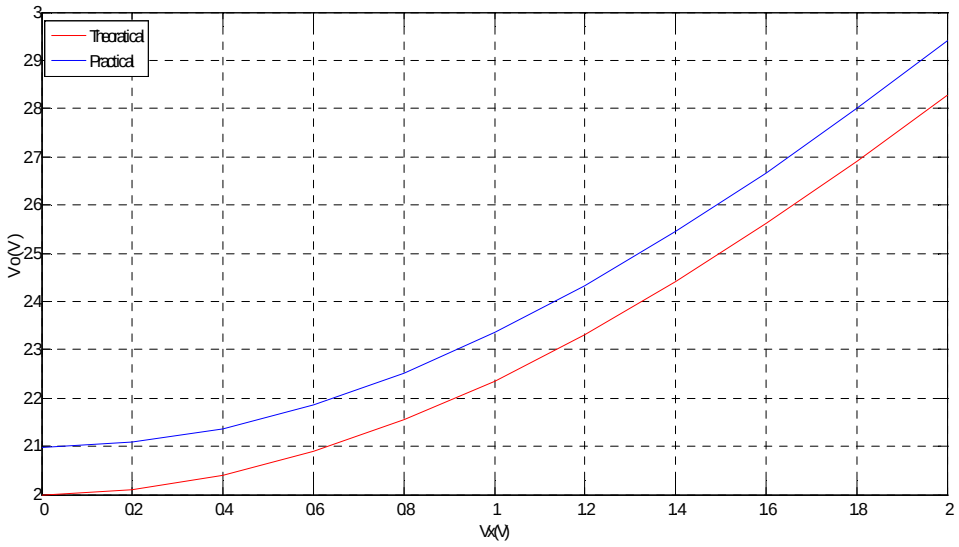

Fig.3.4 (b) Comparison between Theoretical and simulation result of vector magnitude

3.3 SINE WAVE SHAPER CIRCUIT

There are at least three well known techniques for generating a sine wave: A sinusoidal continuous time oscillator, for instance a Wien-Bridge oscillator; a digital function synthesizer , which has been widely used in modem function generators; and analog sine shapers, which evolved from linear segment approximation methods [7] and the use of a single differential BJT pair [14] to the ingenious circuit of Barrie Gilbert, which is based on a hyperbolic tangent series approximation using a group of differential BJP pairs [7, 8]**.** Clearly, there is not one only technique which is absolutely better than the others, since it all depends on the envisaged application and its requirements. Sinusoidal oscillators produce quite accurate signals, but are not always adequate for integration - the need for large value capacitors, when operating at low frequencies is one of those impediments. The digital synthesis, certainly provides the highest achievable accuracy and stability, but demands an expressive processing power, silicon area and energy consumption. The third alternative, analog sine shapers are simpler to implement and occupy small area, but suffer from thermal drift, offset errors and other imperfections that are properties of any analog circuit.

Despite all Sine Shaper gives good accuracy and area-saving. In CMOS technology the hyperbolic tangent approach has been used to generate a sine wave with MOS transistors operating in weak inversion, since in this mode of operation MOS

transistors show a current versus voltage characteristics that is similar to BJT‘s [9]. In this paper a similar circuit is described, which is also implemented in CMOS technology, but using lateral-pnp bipolar transistors instead and using less transistors in the sine generation cell than in the circuit described in [9].

Sine-wave generator using bipolar transistor circuit diagram:

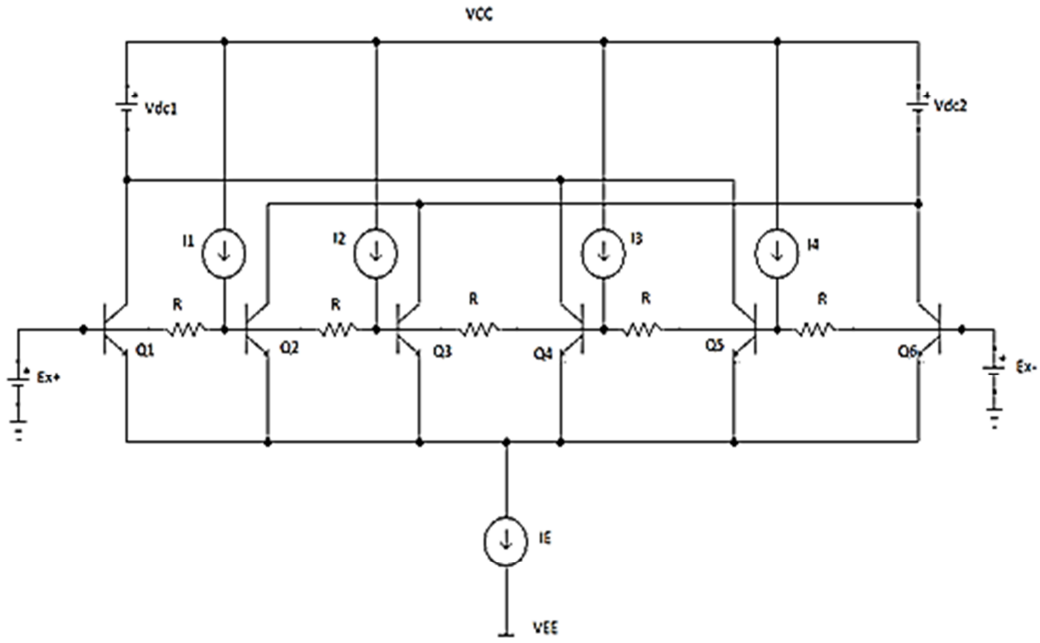

Fig.3.5 sine wave shaper circuit [6]

Analysis of sine-wave circuit:

As shown in the figure that Q1, Q2, Q3 and Q4, Q5, Q6 made differential pair arrangement

3.4.1 Analysis of general SINE network

The general network comprises N identical, isothermal, and ideal transistors, N-1 identical resistor and N-2 identical current source, where N greater then equal to 4 and assumed here to be even, resulting in overall function having odd-order symmetry. The differential voltage E_x determine the instantaneous angle of the function; the current I_E determines its magnitude.

The voltage at each base node results from the superimposition of a fixed component due to the linear division of E_x as follows:

$$V_{Bn} = (n-1)\left\{\frac{(n-1)IR}{2} + \frac{E_x}{N-1}\right\} \tag{3.8}$$

The locus of this array of voltages forms a parabola, the apex of which is centered when $E_x = 0$, and moves to the left orright as E_x is increased or decreased, respectively, IR is steered mainly into the (n-p-n) transistor whose base is most positive, the acuity of switching being dependent on the bias factor

$$\alpha = \frac{IR}{kT/q} = \frac{E_B}{kT/q} \tag{3.9}$$

For a locally-symmetric voltage distribution, the zero crossing of the output function occur when ever adjacent bases are at the same voltage

$$V_{Bn} = V_{B(n+1)} \tag{3.10}$$

Solving equation (1), (2) and (3) gives

$$E_x = (n-1)\left\{\frac{N}{2} - n\right\} E_B \tag{3.11}$$

From these equation we state that E_x must change by (N -1)$E_B$to move from one zero-crossing to the next. The equivalent angle is therefore

$$x = \frac{\pi E_x}{(N-1)E_B} \tag{3.12}$$

Substituting E_x in the equation (3.5) we gate modified value of V_{Bn} in terms of E_B

$$V_{Bn} = (n-1)\left\{\frac{(n-1)}{2} + \frac{x}{\pi}\right\} E_B \tag{3.13}$$

The corresponding collector can be I_{Cn} calculated as follows:

$$I_{Cn} = I_E \frac{e^{\frac{V_{Bn}}{kT/q}}}{\sum_{n=1}^{N} e^{\frac{V_{Bn}}{kT/q}}} \tag{3.14}$$

And using the equation (3.12) and (3.13) this becomes

$$I_{Cn} = I_E \frac{e^{\alpha(n-1)\left\{\frac{(n-1)}{2}+\frac{x}{\pi}\right\}}}{\sum_{n=1}^{N} e^{\alpha(n-1)\left\{\frac{(n-1)}{2}+\frac{x}{\pi}\right\}}} \tag{3.15}$$

Finally, the normalized output is obtained by summing alternate collector currents in anti-phase as follows:

$$F(x,\alpha,N) = \frac{I_{out}}{I_E} = (-1)^{N/2} \frac{\sum_{n=1}^{N}(-1)^n e^{\alpha(n-1)\left\{\frac{(n-1)}{2}+\frac{x}{\pi}\right\}}}{\sum_{n=1}^{N} e^{\alpha(n-1)\left\{\frac{(n-1)}{2}+\frac{x}{\pi}\right\}}} \tag{3.16}$$

Where the factor $(-1)^{N/2}$ used for the alternation in the effective phase of the functions as pairs of devices are added to the network

This expression provides little insight, but numerical evaluation soon proves the close similarity between this function and the sine over angular ranges up to $\pm(N-2)\pi/2$ radians. Using a method suggested by Gilbert [6] and developed by Boyle it has been shown that for $N \to \infty$ and small values of α

$F(x,\alpha) \to \eta \sin(x)$ Exactly

Where,η is the network efficiency

$$\eta = 2\exp(-\frac{\pi^2}{2\alpha}) \qquad (3.17)$$

This agree very closely with numerically calculated efficiency using equation (3.16), for $\alpha < 3.5$ above which the distortion becomes excessive.

3.4.2 Simulation Result of Sine shaper Circuit

The circuit shown in fig.3.6 was simulated in P-Spice Simulation result of sine shaper circuit for the input (E_x) where E_x varies from -5V to +2V.

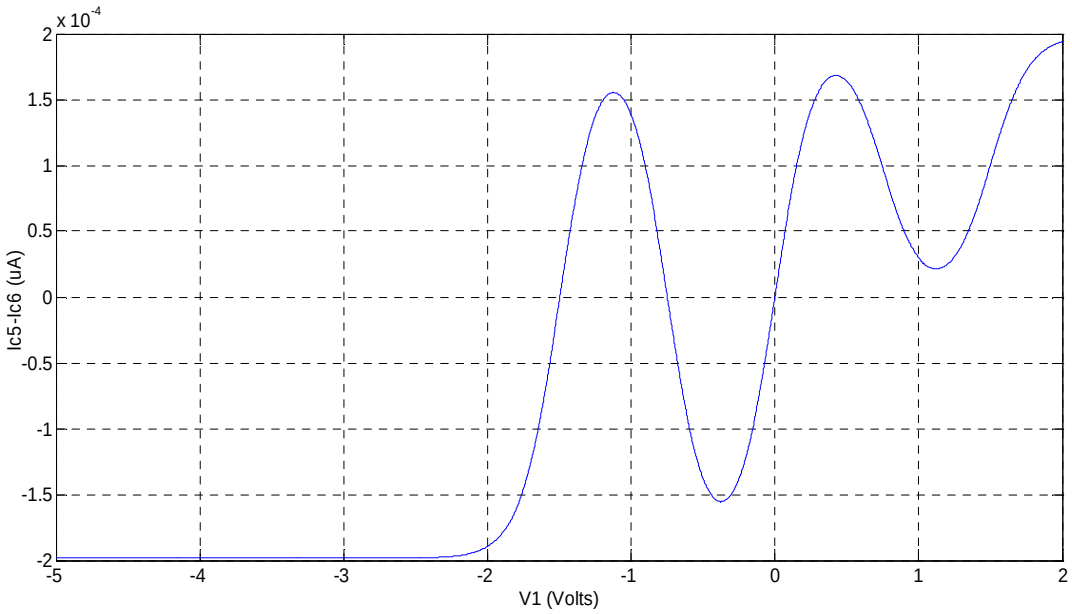

Fig. 3.6 Sine wave shaper output

3.5 FOUR QUADRANT MULTIPLIER

Analog multiplier circuits produce an output that is proportional to the product of two input signals. They find wide application in communication circuits. Such as mixers,

balanced modulators, and phase detector. The Gilbert multiplier cell, [12] forms the basis of many multiplier circuits.

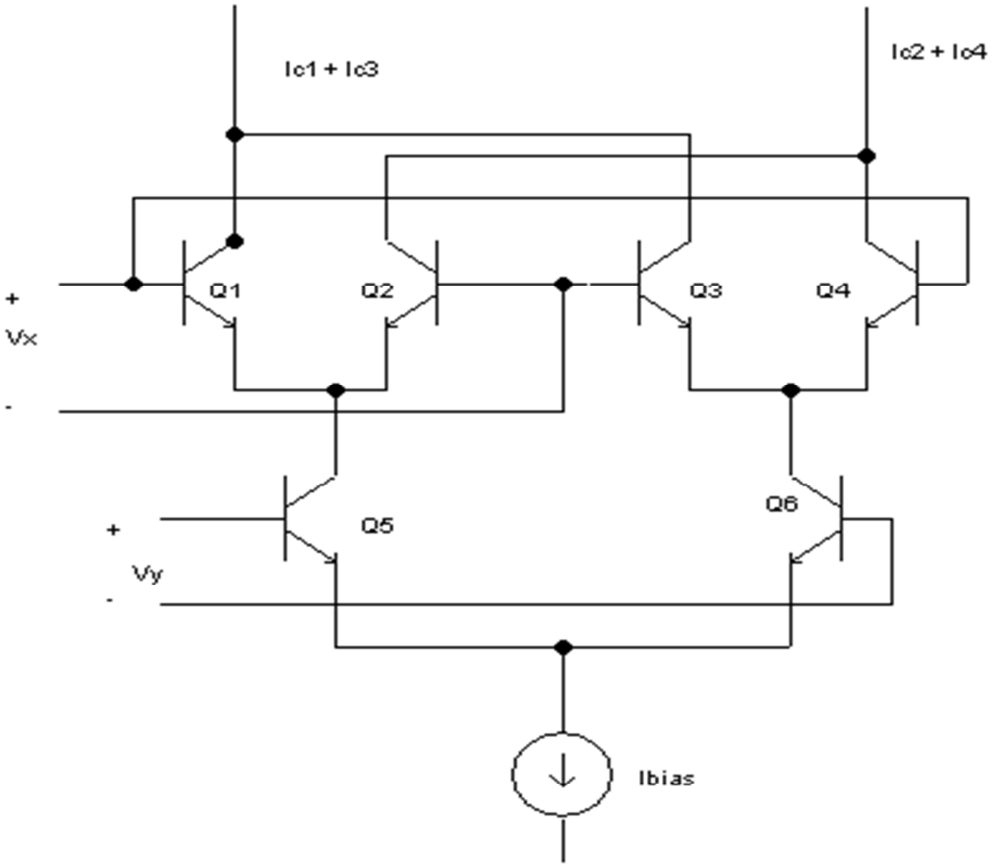

Fig. 3.7 Gilbert multiplying cell in current mode [1]

The Gilbert cell consists of two cross coupled differential pairs Q1, Q2 and Q3, Q4 fed serially by third differential pair Q5 and Q6. The x-input signal is applied to the upper differential pairs and the y-input signal is applied to the lower differential pair. The output is taken differentially at the collectors of the cross-coupled pairs, expressed as

$$I_O = (I_{C1} + I_{C3}) - (I_{C2} + I_{C4}) \tag{3.18}$$

$$I_O = (I_{C1} - I_{C2}) + (I_{C4} - I_{C3}) \tag{3.19}$$

As expressed by the right hand term in equation (3.18), the output is equal to the difference in the differential collector currents of the two upper differential pairs. The differential output current of a single pair is given by equation

$$I_{C1} - I_{C2} = I_S e^{\left(\frac{V_{BE1}}{V_T}\right)} - I_S e^{\left(\frac{V_{BE2}}{V_T}\right)} = I_{EE} tanh\left(\frac{qV_{12}}{2kT}\right) \tag{3.20}$$

Where base currents have been neglected; V_{12} is the differential input voltage

$$I_O = (I_{C5} - I_{C6}) tanh\left(\frac{qV_X}{2kT}\right) \tag{3.21}$$

Substituting for the differential current of the lower differential pair, equation (3.21) becomes

$$I_O = I_{bias} tanh\left(\frac{qV_Y}{2kT}\right) tanh\left(\frac{qV_X}{2kT}\right) \tag{3.22}$$

The product is nonlinear in V_X and V_Y. However, the amplitude of the signals are much smaller than the thermal voltage $/q$, then the tanh function are approximately linear, given by

$$I_O \approx \left(\frac{q}{2kT}\right)^2 I_{bias} V_X V_Y \tag{3.23}$$

Two remove this restriction on the signal amplitude, the input signals can be pre-processed to compensate for the tanh nonlinearity. In this regard, consider the circuit

Here, the modulation parameter x in the current source represents an input signal; its value can be vary -1 to +1. The voltage difference between the emitters of two transistors is given by

$$\Delta V = V_{be2} - V_{be1} \tag{3.24}$$

Applying the trigonometric identity

$$\tanh^{-1} x = \frac{1}{2} \ln\left(\frac{1+x}{1-x}\right) \tag{3.25}$$

This shows that the circuit in fig.3.7 can be used to compensate for the tanh nonlinearity of the differential pairs in the multiplier circuit. This compensation needs to be applied only to x input because fig. 3.6 $(I_{C5} - I_{C6})$ varies as $\tanh(V_Y)$,the lower differential pair (Q5, Q6) can be eliminated if the y inputs are supplied as currents. Such a linearized multiplier circuit is shown in fig. 3.8 In this circuit, the x and y signals are proportional to the input voltage signal as:

$x = K_X V_X$ and y= $K_Y V_Y$

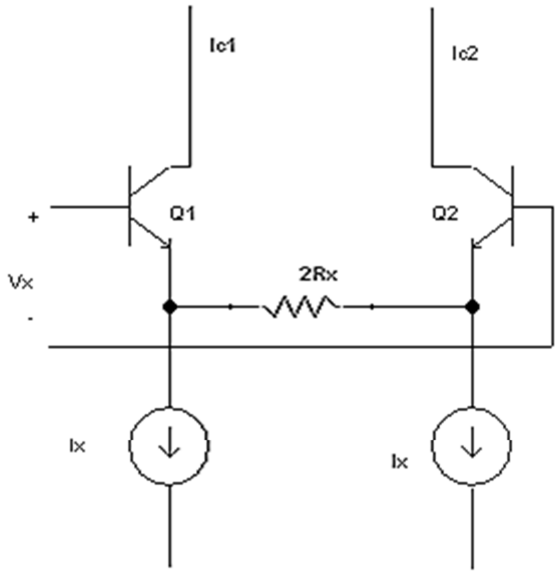

Fig.3.8 Emitter degeneration circuit

the output current

$$I_O = (I_{C1} + I_{C3}) - (I_{C2} + I_{C4})$$

$$I_O = [(1+y)I_Y - (1-y)I_Y]tanh\left(\frac{q\Delta V}{2kT}\right) \tag{3.26}$$

Using equation (3.24) and (3.25), the result in

$$I_O = 2I_Y xy = 2(K_X K_Y I_Y)V_X V_Y$$

For the multiplier to function with voltage signals a differential voltage to current convertor is needed at the inputs.

3.5.1 Emitter degeneration voltage to current convertor:

Here we describe the voltage to current convertor which is used in multiplier circuit. As shown in the fig. 3.9 that a resistor is connected to differential pair transistor Q1 and Q2 for the circuit shown in fig. 3.9. The base emitter voltage will be

$$V = V_{be1} + I_{c1}R - I_{c2}R - V_{be2} \tag{3.27}$$

Here base current has been neglected. If $I_E R \gg kT/q$,then to base emitter voltage can be approximated to equal and that gives:

$$\frac{V}{R} = (I_{c1} - I_{c2}) \tag{3.28}$$

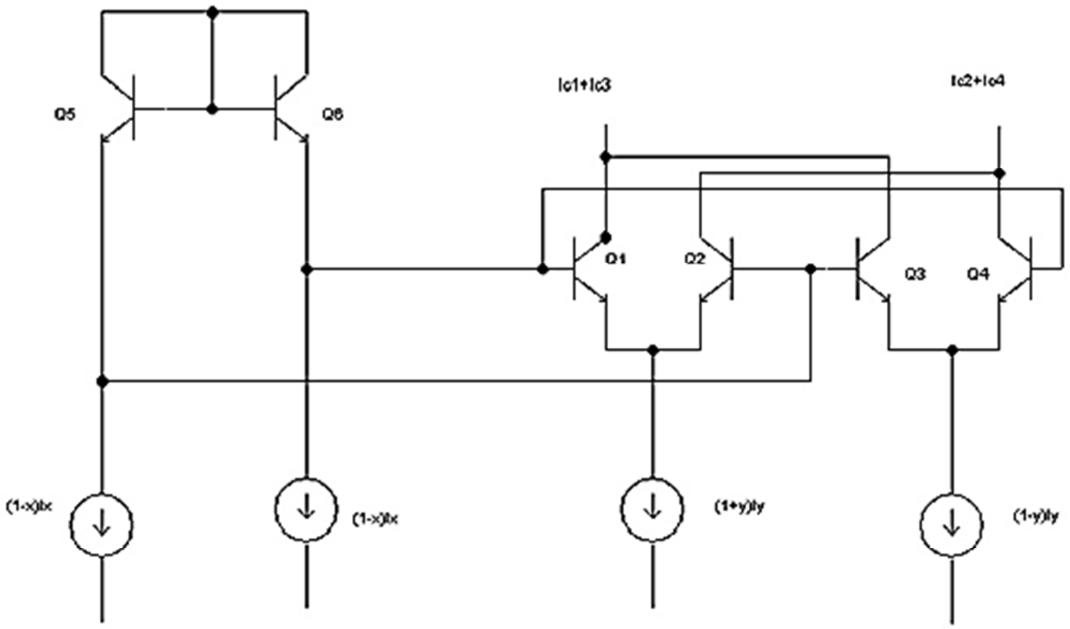

Fig. 3.9 Linearized Multiplier

And also

$$I_{c1} + I_{c2} = 2I_E \tag{3.29}$$

Combining equation (3.28) and (3.29) gives

$$I_{c1} = \left(1 + \frac{V}{2I_E R}\right) I_E = (1 + x)I_E \tag{3.30}$$

And

$$I_{c2} = \left(1 - \frac{V}{2I_E R}\right) I_E = (1 - x)I_E \tag{3.31}$$

Where $x = \frac{V}{2I_E R}$

Simulation result of multiplier circuit using BJT

So after employing voltage to current converter in fig.3.7 our final four quadrant analog multiplier is shown in fig 3.10 and output voltage taken as shown in figure across the differential pair transistor Q5 and Q8, this would be

$$V_Z = \frac{2R_Z}{I_X R_X R_Y} V_X V_Y \tag{3.32}$$

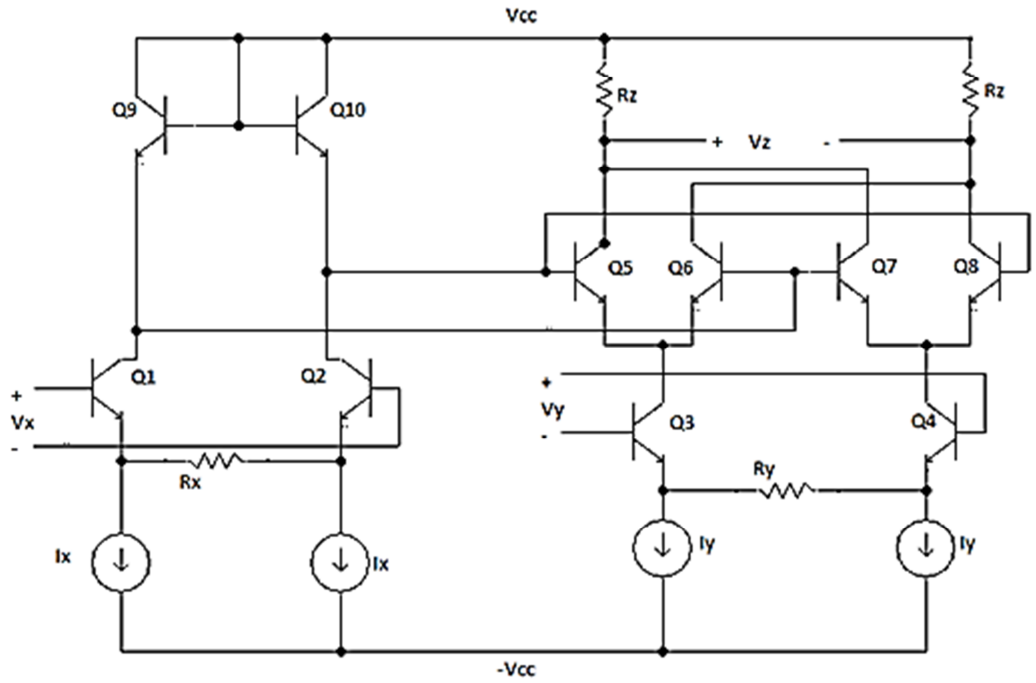

Fig.3.10 Four quadrant multiplier circuit in voltage mode for large range of input [12]

Simulation result of multiplier circuit using BJT

The values of the resistorR_X, R_Y and R_Z are taken such that $\frac{2R_Z}{I_X R_X R_Y} = 0.1$ and $V_Z = 0.1 V_X V_Y$

Here we take $R_X = 15K$, $R_Y = 15$K and $R_X = 11.25K$

And value of current $I_X = I_Y = 1mA$

Input range of multiplier is given

$-10V < V_Y <$ +10V

$-10V < V_X <$ +10V

The supply voltage is $\pm 15V$ this allows inputs in excess of $\pm 10V$ to be used.

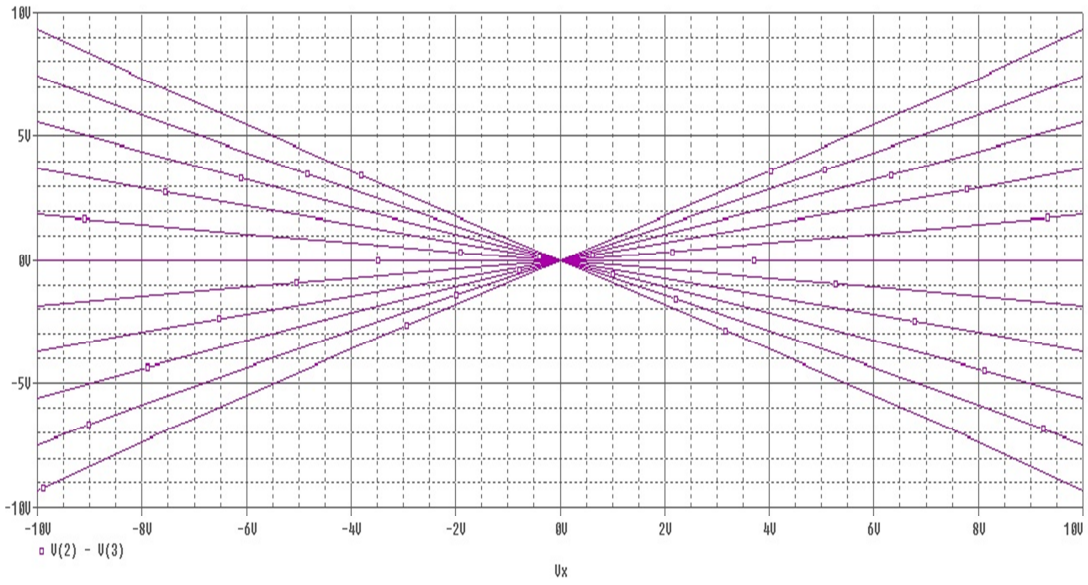

Fig 3.11 Simulation result of four quadrant multiplier circuit

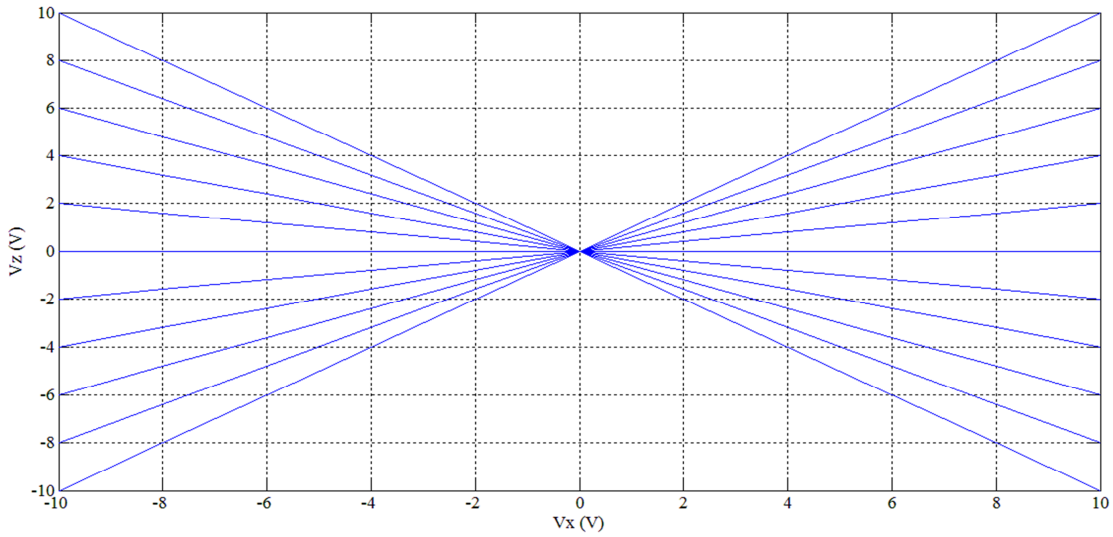

Fig. 3.12 theoretical output of four quadrant multiplier circuit

3.6 CONCLUSION

In this chapter, Introduction to translinear circuit principle (TLP) was discussed and a class of non-linear signal processing circuit using TLP is presented i.e. vector magnitude calculator, sine shaper circuit and four quadrant multiplier.

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CHAPTER-4

CMOS IMPLEMENTATION OF NON-LINEAR SIGNAL PROCESSING CIRCUITS

INTRODUCTION

In the previous chapter, Implementation of Non-linear circuits based on translinear principle were discussed. In this chapter, CMOS based non-linear circuits are discussed such as squarer, multiplier. CMOS Implementation of adder circuit is also presented which may be used as fundamental part of analog multiplier circuit.

4.1 CMOS SQUARER CIRCUIT REALIZATION

Squaring circuit is a nonlinear signal processing function which is very useful in instrumentation, communication, and control systems. Nonlinear circuits [1–12] have been published. Some nonlinear circuits operated in the voltage mode [1, 2] and some others were designed to operate in the current mode [3–7]. In the recent past, the analog circuit design using the current mode approach has gained considerable attention. This stems from its inherent advantages of wide bandwidth, high slew rate, low power consumption, and simple circuitry [5]. However, some sensors and transducers give an output signal as a voltage signal; for example, voltage transformer and a thermocouple. So the voltage mode analog circuits are still needed. To design a circuit that can be connected to voltage or current mode analog circuit, the versatile analog multiplier using an operational transconductance amplifier (OTA) [8] was proposed, but it acquired error due to finite input resistance. Then, the versatile analog multiplier using second generation current controlled current conveyor (CCCII) [9] was reported, but it consumed more power consumption.

Squarer circuit is most widely used in signal processing. They are generally used for squaring a signal which can be further used for multiplier and frequency multiplier circuits. The squarer consists of a mixed signal circuit, a voltage inverting amplifier, a differential amplifier, a current mirror, and a voltage divider. The mixed signal circuit formed from transistors M_1 and M_2 shown in Fig. 4.2 acts as mixing the input voltage (V_{in}) and the input current (I_{in}), and gives the output as the voltage signal (V_1).

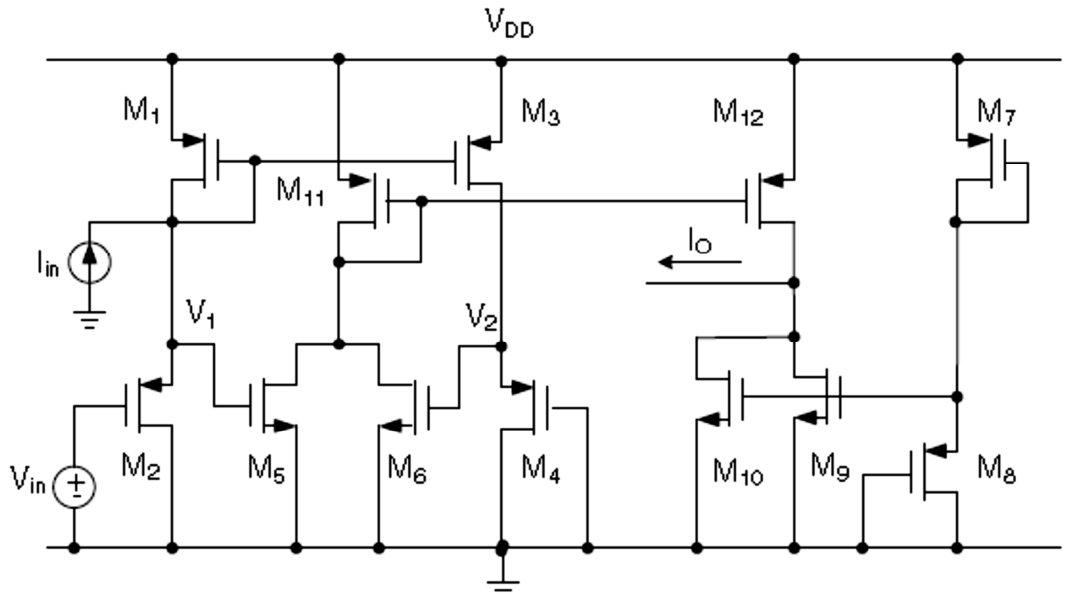

Fig 4.1 CMOS Squarer circuit [10]

Applying Kirchhoff's current law at node V_1 obtains

$$I_{in} = I_{D2} - I_{D1} \tag{4.1}$$

Since $I_D = K_N(V_{GS} - V_{TN})^2 \qquad V_{GS} > V_{TN}, V_{DS} \geq V_{GS} - V_{TN}$ (4.2)

$$I_D = K_P(V_{GS} - V_{TP})^2 \qquad V_{GS} < V_{TP}, V_{DS} \leq V_{GS} - V_{TP} \tag{4.3}$$

Where $K_N = 0.5\mu_n C_{OX} W/L$ and $K_P = 0.5\mu_p C_{OX} W/L$ are the transconductance parameters of NMOS and PMOS, respectively. V_{TN} and V_{TP} are the threshold voltages of respectively. V_{GS} and V_{DS} are the gate to source voltage and the drain to source voltage, respectively.

Now $$I_{D1} = K(V_1 - V_{DD} - V_{TO})^2$$

$$I_{D2} = K(V_{in} - V_1 - V_{TO})^2$$

So from equation (4.1)

$$I_{in} = I_{D2} - I_{D1} \tag{4.4}$$

$$I_{in} = K(V_{in} - V_1 - V_{TO})^2 - K(V_1 - V_{DD} - V_{TO})^2$$

$$I_{in} = K(V_{in} - V_1 - V_{TO} + V_1 - V_{DD} - V_{TO})(V_{in} - V_1 - V_{TO} - V_1 + V_{DD} + V_{TO})$$

$$I_{in} = K(V_{in} - V_{DD} - 2V_{TO})(V_{in} - 2V_1 + V_{DD})$$

$$V_{in} - 2V_1 + V_{DD} = \frac{I_{in}}{K(V_{in} - V_{DD} - 2V_{TO})}$$

$$V_1 = \frac{V_{in}}{2} + \frac{I_{in}}{2K(V_{DD}+2V_{TO}-V_{in})} + \frac{V_{DD}}{2} \quad (4.5)$$

The voltage inverting amplifier formed from transistors M_3 and M_4, and the drain current of M_3 is equal to that of M_4. The voltage V_2 is calculated by using equation

$$V_2 = -\left[\frac{V_{in}}{2} + \frac{I_{in}}{2K(V_{DD}+2V_{TO}-V_{in})}\right] + \frac{V_{DD}}{2} \quad (4.6)$$

The differential amplifier consists of the transistors M_5 and M_6 which are perfectly matched, and the summation of the drain current of M_5 and M_6 can be expressed as

$$I_{D5} + I_{D6} = 2K\left[\left(\frac{V_{in}}{2} + \frac{I_{in}}{2K(V_{DD}+2V_{TO}-V_{in})}\right)^2 + \left(\frac{V_{DD}}{2} - V_{TO}\right)^2\right] \quad (4.7)$$

The voltage divider circuit, consisting the transistors M_7 and M_8 which are perfectly matched, is used for generating voltage signal $V_{DD}/2$. The summation of the drain current of M_9 and M_{10} can be expressed as

$$I_{D9} + I_{D10} = 2K\left(\frac{V_{DD}}{2} - V_{TO}\right)^2 \quad (4.8)$$

The mixed signal circuit is applied to the squarer which makes the squarer circuit versatile means we can apply voltage and current input.

The mixed signal circuit shown in fig 4.2

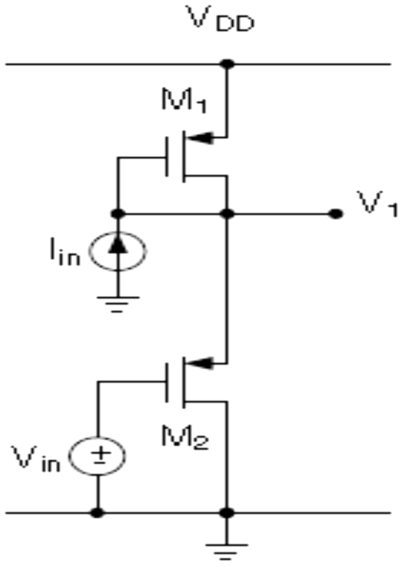

Fig 4.2 Mixed signal circuit

Suppose that the ratio of the current mirror formed from transistors M_{11} and M_{12} is equal to 1:1, and the output current of the squaring circuit can be defined and expressed as

$$I_o = I_{D5} + I_{D6} - I_{D9} - I_{D10} \tag{4.9}$$

Thus,

$$I_o = 2K\left(\frac{V_{in}}{2} + \frac{I_{in}}{2K(V_{DD} + 2V_{TO} - V_{in})}\right)^2$$

Note that if V_{in}= 0, the output current will be the square of I_{in}

$$I_o = 2K\left(\frac{I_{in}}{2K\left((V_{DD} + 2V_{TO} - V_{in})\right)}\right)^2 \tag{4.10}$$

and if I_{in} = 0, the output current will be the square of V_{in}

$$I_o = 2K\left(\frac{V_{in}}{2}\right)^2 \tag{4.11}$$

From (4.10) and (4.11), it can be shown that the squarer circuit is the versatile squarer.

The input range of the squarer is determined by the saturation condition of M_5 and M_6, and expressed as

$$V_{TO} - \frac{V_{DD}}{2} \leq \frac{V_{in}}{2} + \frac{I_{in}}{2K(V_{DD}+2V_{TO}-V_{in})} \leq \frac{V_{DD}}{2} - V_{TO} \tag{4.12}$$

The Eq. 4.12 shows that the input range depends on difference of $V_{DD}/2$ and V_{TO}. Consider the body effect on the squarer circuit. All the NMOS transistors have sources connected to the ground, while all PMOS transistors, except M_2, M_4, and M_8 which have an independent n-well, have sources connected to the positive supply rail. This causes no variation in the threshold voltage because the source to body voltage is maintained equal to zero at all times. In addition, this squarer used only two CMOS transistors connected between power supply lines in order to operate under low power supply voltage.

4.1.1 Simulation Results of Squarer

The squarer circuits was simulated in PSpice using the 0.5µm MOSIS CMOS models with NMOS threshold voltage V_{TN} = 0.42 V and PMOS threshold voltage V_{TP} = -0.55 V. The aspect ratios of transistors are given in Appendix A.

The bias voltage was set to V_B = 0.465 V and the output terminal was connected to $V_{DD}/2$. Substituting V_{TN} = 0.42 V and I_{in} = 0 into Eq. 4.12, the input range of the squarer circuit is related to V_{DD} in Table 4.1.

TABLE 4.1: voltage input range of squarer

V_{DD}	Voltage input range (V_{in})	$\frac{\Delta V_{in}}{\Delta V_{DD}} \times 100\%$
1.5	-0.66V<V_{in}<0.66V	88%
1.4	-0.56V<V_{in}<0.56V	80%
1.3	-0.46V<V_{in}<0.46V	71%
1.1	-0.26V<V_{in}<0.26V	47%
1.0	-0.16V<V_{in}<0.16V	32%
0.9	-0.06V<V_{in}<0.06V	13%

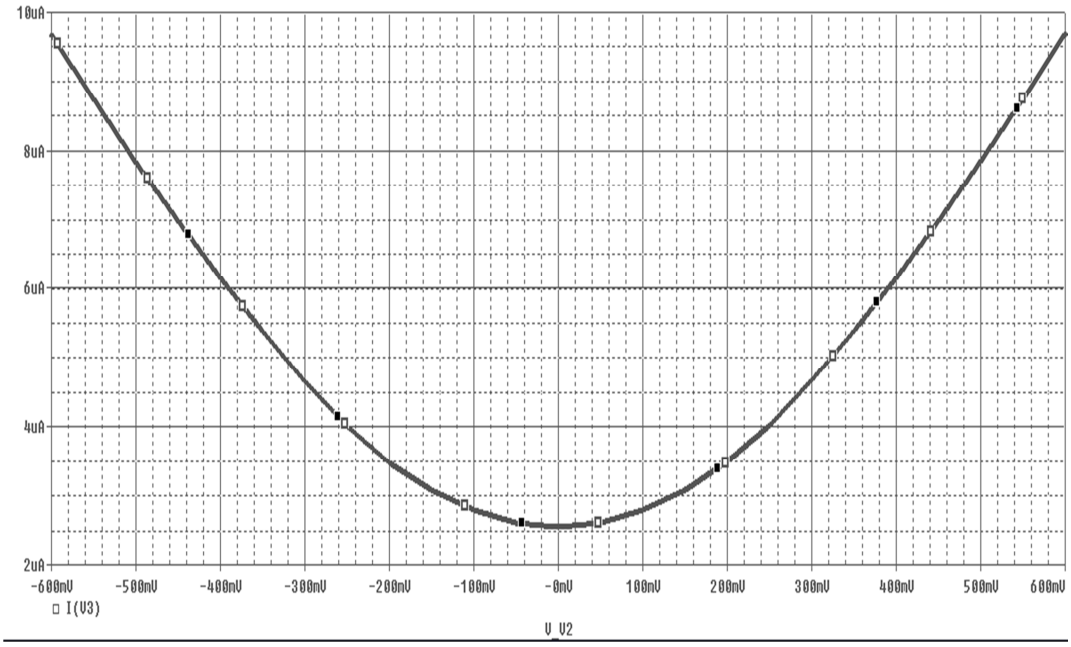

Fig.4.3 DC characteristic of squarer of votage input

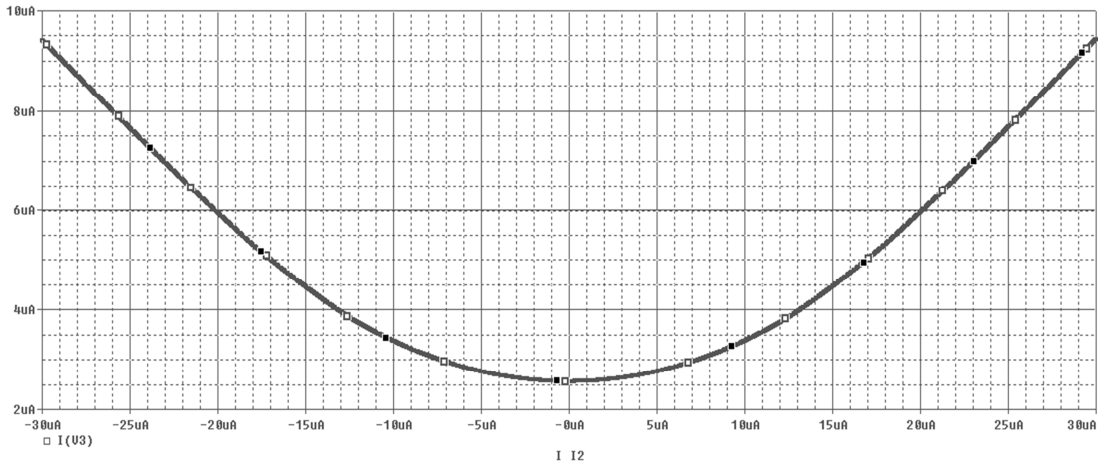

Fig.4.4 DC characteristic of squarer of current input

4.2 CMOS IMPLEMENTATION OF ANALOG ADDER CIRCUIT

Adder is important block we want to multiply to analog signal. Since basic idea of multiplication is such that:

Suppose there are two analog signals A and B, then to obtain multiplication of these signal we can write it as $(A+B)^2-(A-B)^2=4AB$; so first we have to add these signals and then squaring of these signals we get multiplication.

The adder circuit shown in Fig.4.5 which consist a current mirror, the identical four transistors M_{11}-M_{14}, and the tail current source formed by transistor M_{20} and M_{21}

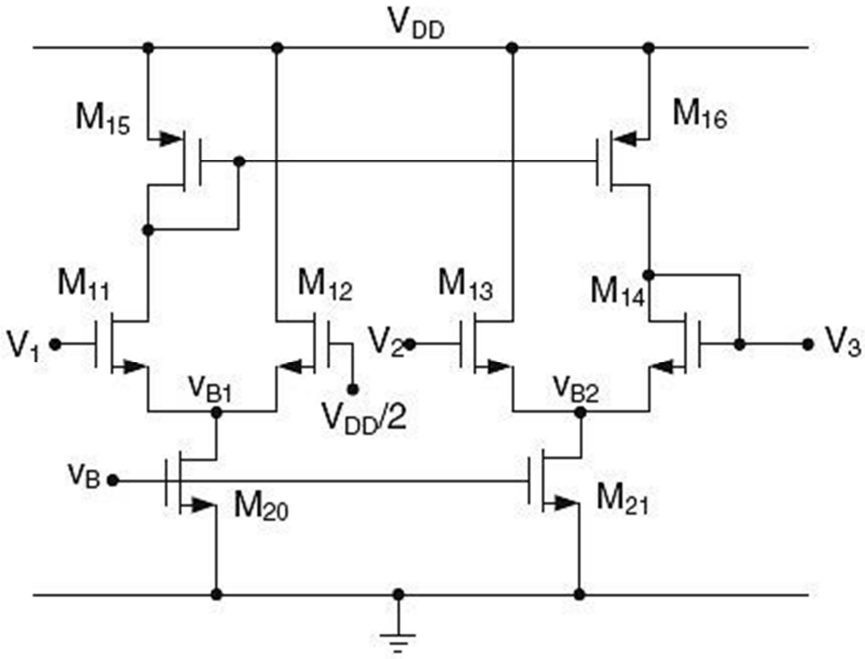

Fig.4.5 Analog adder circuit [10]

Consider Fig. 4.5, if the groups of the transistors (M_{11}-M_{14}), (M_{15}-M_{16}), and (M_{20}-M_{21}) are perfectly matched, it finds $I_{D11} = I_{D14}$ and $I_{D12} = I_{D13}$. Then we can express the relation of the voltage signals V_1, V_2 and V_3 as follows

Since drain current I_{D11} can written as

$$I_{D11} = K(V_1 - V_{B1} - V_{TO})^2 \tag{4.13}$$

Since $I_{D11} = I_{D14} = K(V_1 - V_{B1} - V_{TO})^2$

Now I_{D12} can be written same way

$$I_{D12} = K\left(\frac{V_{DD}}{2} - V_{B1} - V_{TO}\right)^2 \tag{4.14}$$

And I_{D13} will be

$$I_{D13} = K(V_2 - V_{B2} - V_{TO})^2 \tag{4.15}$$

Since all transistors M_{20} and M_{21} is identical, applied gate to source voltage also equal so drain current through these transistor is also equal.

From Fig.4.5 it clearly indicates that

$$I_{D11} + I_{D12} = I_{D13} + I_{D14}$$

We already know that

$$I_{D11} = I_{D14};$$

$$I_{D12} = I_{D13}$$

$$K\left(\frac{V_{DD}}{2} - V_{B1} - V_{TO}\right)^2 = K(V_2 - V_{B2} - V_{TO})^2$$

$$\frac{V_{DD}}{2} - V_{B1} - V_{TO} = V_2 - V_{B2} - V_{TO}$$

$$V_2 = \frac{V_{DD}}{2} - V_{B1} + V_{B2}$$

Now writing the drain current equation for M_{14}

$$I_{D14} = K(V_3 - V_{B2} - V_{TO})^2$$

$$K(V_1 - V_{B1} - V_{TO})^2 = K(V_3 - V_{B2} - V_{TO})^2$$

$$V_1 - V_{B1} - V_{TO} = V_3 - V_{B2} - V_{TO}$$

$$V_1 - V_{B1} + V_{B2} = V_3$$

$$V_3 = V_1 + V_2 - \frac{V_{DD}}{2} \tag{4.16}$$

4.2.1 Simulation Results of Adder

In fig. 4.6 we add two DC signals $V_1$and V_2 their range are given as

$0.5V < V_1 < 0.8V$ and $0.7V < V_2 < 1.1V$

V_1 is shown on X-axis and V_o addition of V_1 and V_2, is shown on Y-axis.

Output V_o comes in the range of 0.45V to 0.85V

In fig. 4.7 we add two AC signals

V_1=100mV, 1 KHz and V_2=100mV, 2 KHz

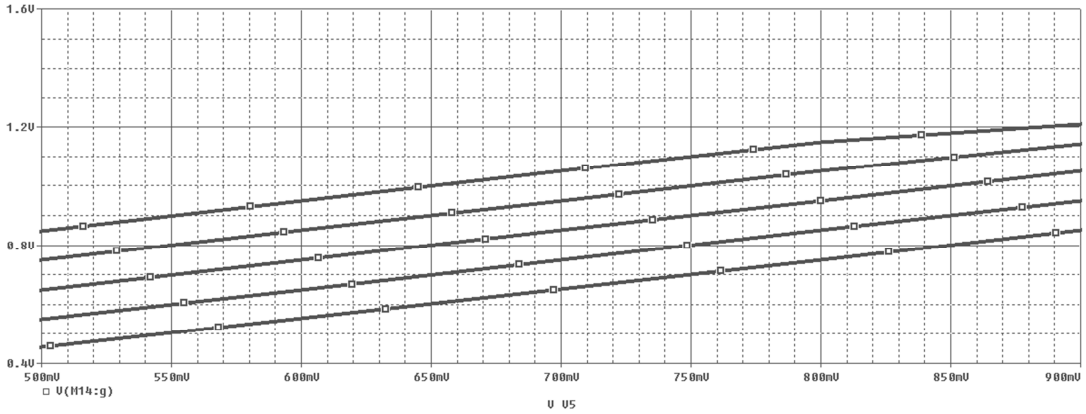

Fig.4.6 DC characteristic of analog adder circuit

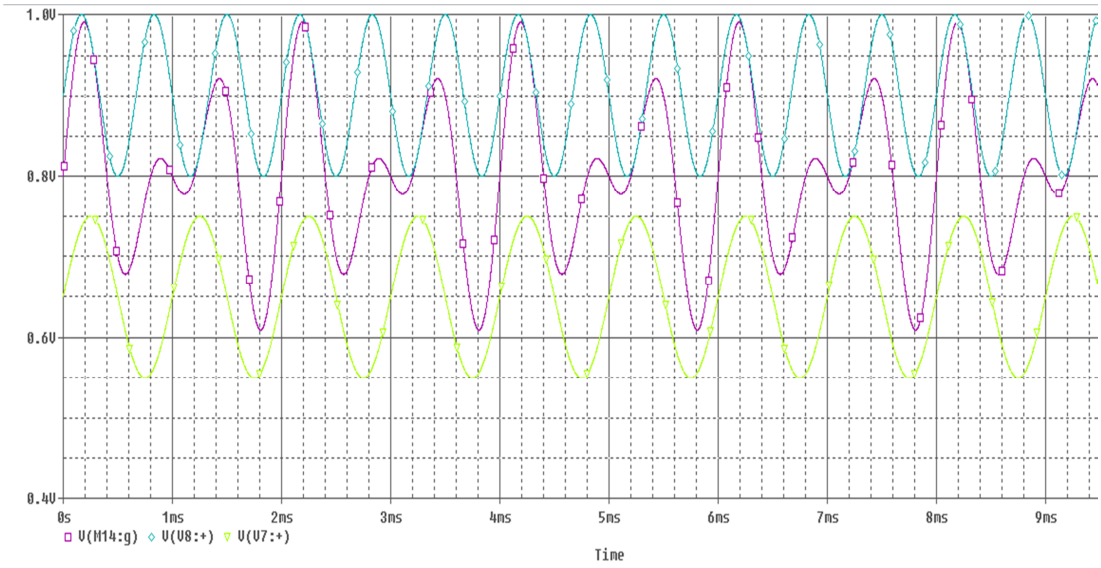

Fig.4.7 AC characteristic of analog adder circuit

4.3 CMOS IMPLEMENTATION OF ANALOG MULTIPLIER

The early attempts to realize multipliers used the triode region of operation in FET transistors. Later on, this mode of operation was used to build multipliers in an indirect way, via application of linear transconductance amplifiers [8]. The triode region is nowadays widely used in continuous-time filters where the FET's are used as controlled resistors, but its application in multipliers, squares, and square-rooters is only occasional. These circuits are designed using mainly the saturation (pinch-off) region of operation.

Yet the operation of the given circuits is based on the saturation operation. The circuits include the nested connection of two devices (this connection is sometimes used in current mirrors with a large ratio of the output and input currents). In this connection one of the devices will be in the pinch-off region.

The versatile CMOS analog multipliers [10, 11] and the two-output multiplier [12] that has low power consumption were proposed, but their output depended on the body effect. In this section, we implemented the circuits that have low power consumption and are free from the body effect. In addition, the circuits in which their inputs can take the current signal or the voltage signal are interesting for application as versatile blocks in library of circuit architectures for automated circuit design [13, 14].

Analog multipliers are important circuit blocks for many applications such as frequency mixers, variable frequency oscillators, adaptive filters, etc. In order to improve the overall power efficiency of such applications which is now regularly required for modern analog and mixed signal design dedicated for portable equipments, the analog multiplier to be used must be able to operate under a reduced supply voltage and consume low current. In CMOS technology, a low-voltage high performance four-quadrant analog multiplier circuit may be implemented by cascading six identical 2-input "combiner" cells Fig.4.8 [14]. This topology has been particularly popular in RF applications for the implementation of up and down-conversion mixers. Since each combiner may be realized by a source drain coupled MOSFET pair connected to a resistor, the required supply voltage is very low (e.g., 1.2V). Although, the circuit has a very wide bandwidth, its linearity is degraded when component mismatch is concerned.

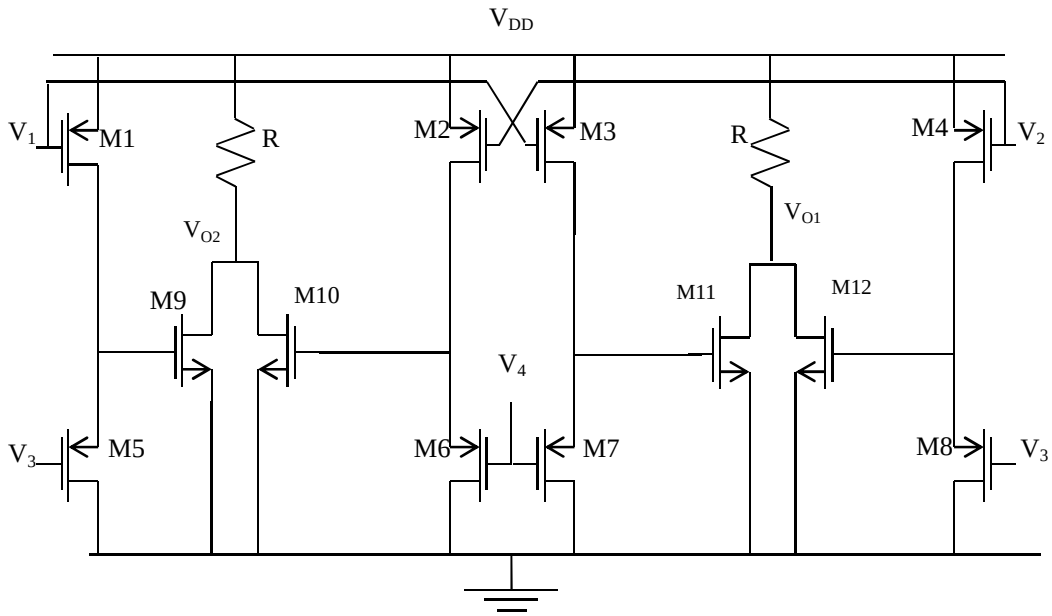

Fig.4.8 Four quadrant analog multiplier circuit [14]

Differential input voltages, defined by $V_{id1} = V_1 - V_2$ and $V_{id2} = V_3 - V_4$, are applied to input terminals of the four subtractor cells (M_1 & M_5, M_2 & M_6, M_3 & M_7 and M_4 & M_8), the outputs of which are connected to input terminals of the two combiner cells (M_9, M_{10} & R and M_{11}, M_{12} & R). In order to bias the circuit to operate in the saturation region, the minimum supply voltage requirement is

$$V_{dd} = 2V_{effp} - |V_{tp}|$$

where V_{effp} is the effective (or saturation) voltage of the *p*-channel devices M_1-M_8. Note that, for modern sub-micron CMOS process technologies with $|V_{TP}| < 0.6V$ and by careful selection of the device aspect ratios, this circuit can be made to operate under a supply voltage of $V_{DD} = 1V$.

4.3.1 Simulation Results of multiplier

Simulation result of CMOS multiplier of two multiplier shown in fig.4.9 $V_2=V_4=0V$

When V_1 varies from -200mV to +200mV R=5.7k

And V_3 varies from -50mV to +50mV

For AC signal V_1 is 100mV peak amplitude with 500 Hz sinusoidal wave and V_2 is 150mV peak amplitude with 5 kHz sinusoidal wave.

V_{DD}=1V, all PMOS and NMOS W/L is 0.5u/0.5u and 0.5u/0.3u respectively.

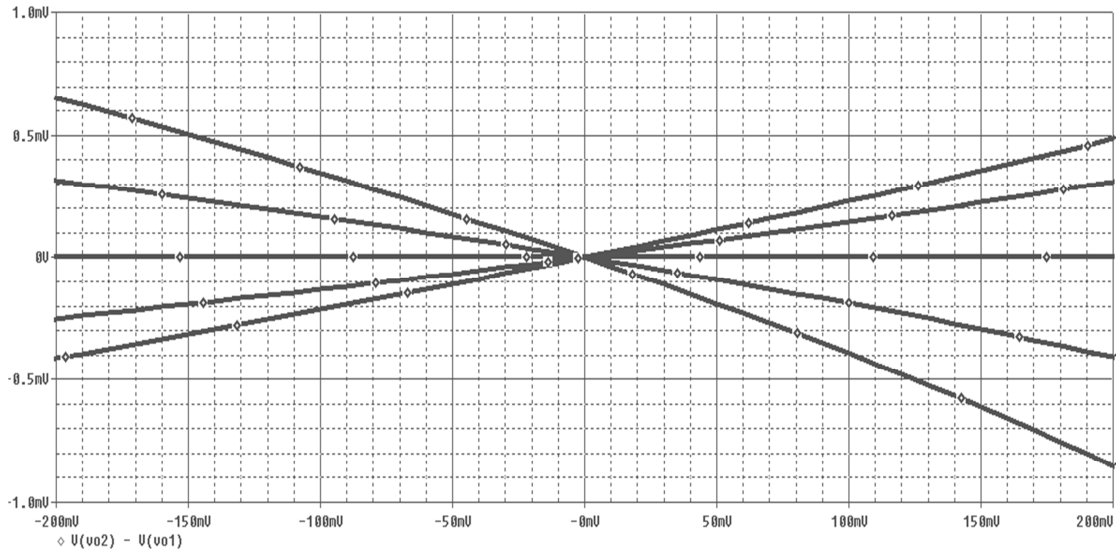

Fig.4.9 Output of CMOS based Multiplier circuit with DC input

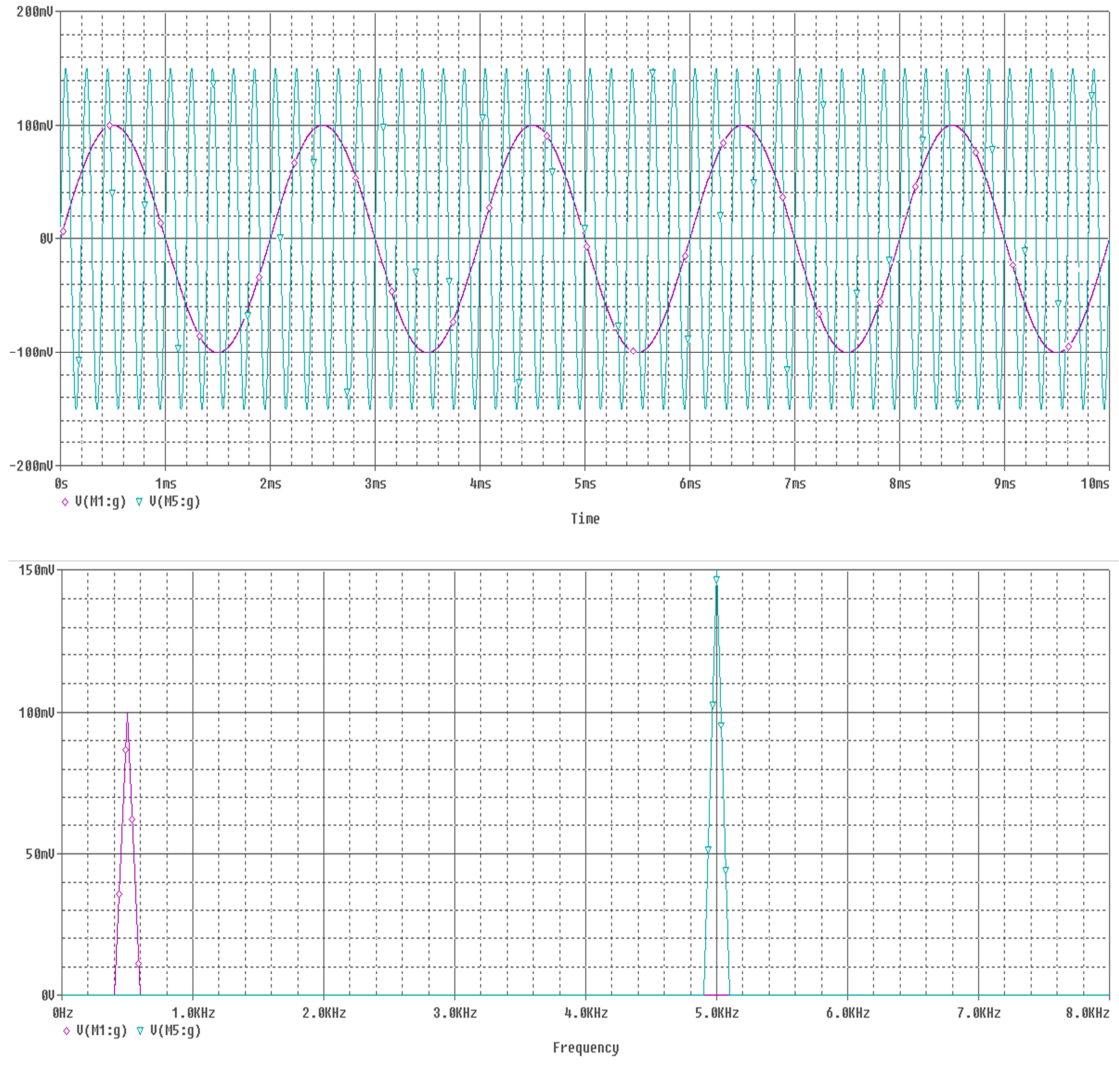

Fig.4.10 CMOS based Multiplier circuit input Transient and FFT response

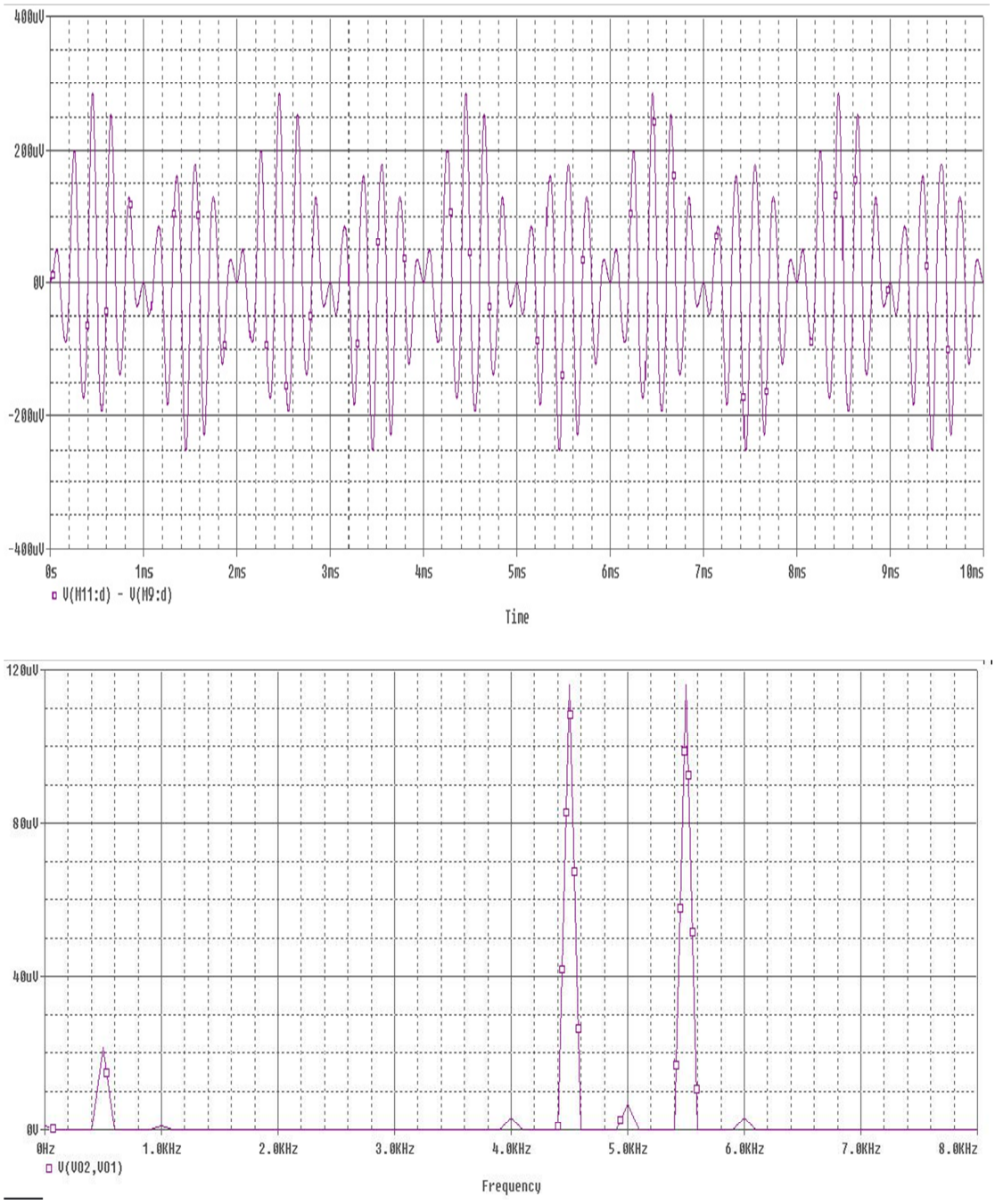

Fig.4.11 CMOS based Multiplier circuit output Transient and FFT response

4.4 CONCLUSION

In this chapter; Non-linear signal processing circuits using CMOS was implanted. The circuits were squarer, adder and four quadrant multiplier circuit. AC and DC response of these of this circuit was presented along with FFT.

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CHAPTER 5

SUMMARY AND FUTURE SCOPE

5.1 SUMMARY

In this dissertation, design and implementation of non-linear signal processing circuits has been presented, with

1. Off-the shelf -available building blocks (AD844, CA3080, µA-741),

2. Bipolar transistor using Translinear circuit principle

3. CMOS technology

The non-linear signal processing circuits have become essential part of healthcare, energy systems, sustainability, transportation, entertainment, education, communication, collaboration, defence, and security.

In chapter I, the general description of the signal processing and its area of application were discussed. It includes the type of signal processing such as current mode, voltage mode, mixed mode and describes their advantage and applicability.

In chapter II, characteristics of various types of off-the-shelf-available building blocks have been discussed and some practical circuits using Active Building Blocks have been presented. Multiplier and divider circuit using current feedback amplifier (CFA) have been discussed. OTA multiplier circuit hardware implementation is also done and results have been placed in this chapter.

In chapter III, a brief discussion on Gilbert Translinear Principle has been presented and some non-linear circuit based on TL principle have been presented such as vector magnitude calculator, four quadrant multiplier, and Sine function shaper circuit. These circuits are implemented using bipolar technology and deviation of simulation from theoretical calculated output expression has been presented.

In chapter IV, Low power consumption CMOS technology using non-linear signal processing circuit has been discussed. The versatile squarer circuit using CMOS have been presented and DC and AC response of squarer has been discussed. The frequency doubler circuit using squarer is also presented. An adder circuit which is used in multiplier circuit has been presented and addition for DC and AC signal is shown. A four quadrant multiplier circuit is also presented using CMOS technology.

5.2 FUTURE SCOPE

In this dissertation emphasis was on implementation of various types of non-linear signal processing circuits and understanding their behaviour. The class of circuits discussed in this dissertation included multipliers, dividers, squares etc. it has been recognized by many researchers that both BJT as well as MOSFETs are basically non-linear devices and their exploitation can be done optimally in non-linear applications. Log-domain filtering, oscillator design using the transistors working in non-linear region are some of the areas in which the work carried out in this dissertation may be extended. Thus there is ample scope for extending this work.

APPENDIXES

Appendix A

PSpice model files used for Process and electrical parameters CMOS 0.5um from MOSIS Technology

*MOSIS Technology

*Valid range for n channel and p channel models‟ >= 0.4um, W >= 0.53um.

*AMI Semiconductor Barcelona

*Spice Level3 Parameters

.MODEL NMOS1 NMOS LEVEL=3 PHI=0.7 TOX=9.5E-09 XJ=0.2U TPG=1

+ VTO=0.7 DELTA=8.8E-01 LD=5E-08 KP=1.56E-04

+ UO=420 THETA=2.3E-01 RSH=2.0E+00 GAMMA=0.62

+ NSUB=1.40E+17 NFS=7.20E+11 VMAX=1.8E+05 ETA=2.125E-02

+ KAPPA=1E-01 CGDO=3.0E-10 CGSO=3.0E-10

+ CGBO=4.5E-10 CJ=5.50E-04 MJ=0.6 CJSW=3E-10

+ MJSW=0.35 PB=1.1

*SPICE LEVEL3 PARAMETERS

.MODEL PMOS1 PMOS LEVEL=3 PHI=0.7 TOX=9.5E-09 XJ=0.2U TPG=-1

+ VTO=-0.95 DELTA=2.5E-01 LD=7E-08 KP=4.8E-05

+ UO=130 THETA=2.0E-01 RSH=2.5E+00 GAMMA=0.52

+ NSUB=1.0E+17 NFS=6.50E+11 VMAX=3.0E+05 ETA=2.5E-02

+ KAPPA=8.0E+00 CGDO=3.5E-10 CGSO=3.5E-10

+ CGBO=4.5E-10 CJ=9.50E-04 MJ=0.5 CJSW=2E-10

+ MJSW=0.25 PB=1

PSpice model files used for Process and electrical parameters CMOS 0.35um from TSMC process

*TSMC 0.35um CMOS, code SCN4ME_SUBM

* Spice Level3 Parameters

.MODEL CMOSN NMOS (LEVEL = 3

+TOX = 7.9E-9 NSUB = 1E17 GAMMA = 0.5827871

+PHI = 0.7 VTO = 0.5445549 DELTA = 0

+UO = 436.256147 ETA = 0 THETA = 0.1749684

+KP = 2.055786E-4 VMAX = 8.309444E4 KAPPA = 0.2574081

+RSH = 0.0559398 NFS = 1E12 TPG = 1

+XJ = 3E-7 LD = 3.162278E-11 WD = 7.046724E-8

+CGDO = 2.82E-10 CGSO = 2.82E-10 CGBO = 1E-10

+CJ = 1E-3 PB = 0.9758533 MJ = 0.3448504

+CJSW = 3.777852E-10 MJSW = 0.3508721)

.MODEL CMOSP PMOS (LEVEL = 3

+ TOX = 7.9E-9 NSUB = 1E17 GAMMA = 0.4083894

+ PHI = 0.7 VTO = -0.7140674 DELTA = 0

+ UO = 212.2319801 ETA = 9.999762E-4 THETA = 0.2020774

+ KP = 6.733755E-5 VMAX = 1.181551E5 KAPPA = 1.5

+ RSH = 30.0712458 NFS = 1E12 TPG = -1

+ XJ = 2E-7 LD = 5.000001E-13 WD = 1.249872E-7

+ CGDO = 3.09E-10 CGSO = 3.09E-10 CGBO = 1E-10

+ CJ = 1.419508E-3 PB = 0.8152753 MJ = 0.5

+ CJSW = 4.813504E-10 MJSW = 0.5)

PSpice model files used for Process and electrical paramet Transistor 2N2222

.model NX1 NPN RB= 524.6 IRB= 0 RBM= 25 RC= 50 RE= 1

+IS= 12E-18 EG= 1.206 XTI= 2 XTB= 1.538

+ BF= 137.5 IKF= 6.974E-3 NF= 1.0 VAF= 159.4 ISE= 36E-16 NE= 1.713 BR= 0.7258

+IKR= 2.198E-3 NR= 1.0

+ VAR= 10.73 ISC= 0 NC=2 TF= 0.425E-9 TR=0.425E-8 CJE= 0.214E-12 VJE=0.5 MJE=0.28 CJC= 0.983E-13

+ VJC=0.5 MJC=0.3 XCJC=0.034 CJS= 0.913E-12 VJS=0.64 MJS= 0.4 FC= 0.5

.model PX1 PNP RB= 327 IRB= 0 RBM= 24.55 RC= 50 RE= 3 IS= 75.5E-18 EG= 1.206

+XTI= 1.7 XTB= 1.866

+ BF= 110.0 IKF= 2.359E-3 NF= 1.0 VAF= 51.8 ISE= 25.1E-16 NE= 1.65

+BR= 0.4745 IKR= 6.478E-3 NR= 1.0

+ VAR= 9.96 ISC= 0 NC=2 TF= 0.610E-9 TR= 0.610E-8 CJE= 0.180E-12 VJE=0.5 MJE=0.28 CJC= 0.164E-12

+ VJC=0.8 MJC=0.4 XCJC=0.037 CJS= 1.03E-12 VJS=0.55 MJS= 0.35 FC= 0.5

Appendix B

Dimensions of CMOS Transistors Used Fig. 4.1:

Table 1: W/L ratio of squarer circuit

Transistor	W/L(µm/µm)
M_1-M_4	10/1
M_5-M_{10}	1/1
M_{11}-M_{12}	10/0.5

Dimensions of CMOS Transistors Used in Fig. 4.6

Table:2

Transistor	W/L(µm/µm)
M_{11}-M_{14}	10/0.5
$M_{15}M_{19}$	5/0.5
M_{20}-M_{21}	5/0.5