CHAPTER – I

INTRODUCTION

1.1 Introduction

The present work describes the current mode / voltage mode active building blocks introduced in the domain of analog signal processing after the introduction of Current Conveyor by Smith and Sedra in 1969 [1]. There had been several major developments in the area of analog circuits and signal processing which have taken place during the past four decades. There is a bulk of material available about the various active blocks developed post Current Conveyors. In this dissertation an attempt has been made to highlight some of these current mode / voltage mode active blocks and implementation of some of these blocks has also been studied and discussed.

Introduction of Current Conveyor was necessary because of the limitations posed by the traditional Operational amplifier which is a highly versatile element. With opamps many circuits, both linear and non linear, can be realized successfully. Extensive research had been carried out from mid-sixties to mid-eighties on the design of various linear and non-linear analogue circuits using integrated circuit (IC) op-amps. Since opamp based circuits employ RC elements, their monolithic IC implementation was difficult because precise tuning of the time constant RC was difficult to implement. Moreover their limited performance due to less bandwidth, slew rate etc. forced the analog designers to look for other active blocks [2]. Switched capacitor circuits was one solution where the resistor was replaced by a periodically switched capacitor but it again posed problems like aliasing and clock feed through [3].

In eighties Operational Transconductance Amplifiers (OTA) was introduced. The OTA-C circuits employ only transconductors and capacitors to build various functional circuits and thus, do not require any resistors; moreover, their internal structure is also resistor-less, thus adding to its advantage list. In OTA circuits the transconductance can be controlled electronically through an external DC bais voltage / current making its gain variable (programmable). The period 1985-95 witnessed a phenomenal research activity on the various aspects of OTAs and OTA-C circuits. Publications showing possible ideas related to the design of OTAs (bipolar,CMOS and biCMOS) as well as application circuits using OTAs , have still not been completely exhausted.

The developments in digital circuit design particularly, CMOS digital circuits, have had a profound influence on the developments in analogue circuits particularly in those cases where both digital and analogue parts are to be integrated on the same chip using the same technology (CMOS). Even though the digital systems have many advantages over the analog type the latter can't still be avoided as the natural world is analog. The various developments in the field of integrated circuit (IC) technology, again, posed various challenges to analog designers to match the analog system with their fast growing digital counterparts. It is such requirements which have resulted in continued research on efficient analog circuit designs especially current-mode (CM) techniques and circuits for evolution of elegant and efficient solutions to many contemporary problems in mixed-mode circuit design problems. The current mode approach to signal processing is often considered to have one or more of the following advantages: higher frequency range of operation, lower power consumption, higher slew rates, improved linearity and better accuracy [4]. Before describing the developments in analog signal processing and circuit designs we will first analyze some of the basics of signal processing.

1.2 Analog signal proc essing vs Digital signal processing

The signal processing operations involved in many applications like communication systems, control systems, instrumentation, biomedical signal processing etc can be implemented in two different ways

(1) Analog or continuous time method and

(2) Digital or discrete time method.

The analog approach to signal processing was dominant for many years and it uses analog circuit elements such as resistors, capacitors, transistors, diodes etc. With the advent of digital computer and later microprocessor, the digital signal processing has become dominant now a days. The analog signal processing is based on natural ability of the analog system to solve differential equations that describe a physical system. The solutions are obtained in real time. In contrast digital signal processing relies on numerical calculations. The method may or may not give results in real time. The digital approach has two main advantages over analog approach (1) Flexibility: Same hardware can be used to do various kind of signal processing operation, while in the core of analog signal processing one has to design a system for each kind of operation. (2) Repeatability: The same signal processing operation can be repeated again and

again giving same results, while in analog systems there may be parameter variation due to change in temperature or supply voltage [5]. Added to these ,digital signal processing has many advantages added to its list like, better noise immunity than analog signals. They are compact and much cheaper than their analog counterpart. Digital signals can be encrypted so that only the intended receiver can decode it. It Enables transmission of signals over a long distance and it enables multi-directional transmission simultaneously[6].

Taking these advantages into account, the designers are forced to look for digital solutions rather than analog in VLSI systems. Even then, analog circuits are fundamentally necessary in many of today's complex, high performance systems. This is caused by the reality that naturally occurring signals are analog. Practically all signals in the physical world are continuous in both amplitude and time, and hence always analog techniques will be required for conditioning of such signals before they can be processed by digital signal processing circuits. Therefore analog circuits act as a bridge between the real world and digital systems. Another important reason for the existence of analog signal processing is the bandwidth, which can be some order of magnitudes higher, if the signal is processed in analog circuits than in digital.

1.3 Current mode signal processing vs. Voltage mode signal processing

Any signal processing done in electric or electronic circuits is performed by means of more or less organized movement of charge, where voltages and currents are usually the variables and time, resistances, capacitances and inductances are parameters of the circuit defining the properties of the signal processing. The main reason for using only voltages and currents in analog signal processing is that active devices, which are exploited in analog electronics, operate mostly with resistances (conductance), as parameters for controlling the signal processing. The signal is then processed by miscellaneous voltage-current and current-voltage conversions, amplification, weighted addition and multiplication, etc [7]. Historically voltage has been used as the main variable for signal processing, probably because the thinking in terms of voltages is easier and simpler for the designers, than the thinking in terms of currents. However, during the years the analog electronics became practically only voltage processing and most of the building blocks used in analog electronics (like opamps) are typical voltage processing circuits.

In order to increase the speed of circuits for analog signal processing and to decrease the supply voltages of integrated circuits, designers devote their attention to the so-called current mode. Here the individual circuit elements should interact by means of currents and not with voltages.

The difference between voltage and current processing circuits is that a single output terminal of a current processing block is able to supply only a single input terminal**,** since the inputs of current processing blocks cannot be arranged into a serial connection. Therefore, if more input terminals are required to be supplied by the same input signal, it is necessary to design current processing building blocks with multiple outputs giving the same output signal while in voltage processing circuits a single voltage-output terminal can supply more voltage-input terminals connected in parallel.

1.4 Scope and outline of the work presented in thesis

The basic elements in analog signal processing namely, VFA (Voltage Feedback Amplifier), CFA (Current Feedback Amplifier), OTA (Operational Transconductance Amplifier), and particularly Current Conveyors (CC) are either modified or extended in an effort to increase the application potential of the element giving the form of a new element with any improved feature like simple internal structure, lower power consumption, or improved speed of operation or electronic tunability etc.

This thesis is primarily directed towards the study of various active elements of current mode and voltage mode which were introduced after the Current Conveyors. In this thesis the newly introduced active elements are categorized into three classes as:

Current Conveyors and its derivatives,

Opamps, FTFNs, Hybrid Opamp-CC,

Other Active elements

New active blocks introduced in each of these classes are discussed in the following chapters.

Practical realisation of few of the newly introduced active blocks with commercially available units like AD844 and LM13600 is attempted by simulating their various applications using PSPICE.

References

1. Smith, K.C. and Sedra, A. S., 'The current conveyor: a new circuit building block'. IEEE Proc. CAS, 1968, vol. 56, no. 3, p. 1368-1369.
2. Kuntman, H. A. 'New Advances and Possibilities in Active Circuit Design' 10th International Conference on Development and application systems, Suceava, Romania, May 27-29, 2010
3. Schaumann, R. and Valkenberg, M. E. 'Design of Analog Filters', Oxford University Press, 2004.
4. Biolek, D., Senani, R., Biolková, V. and, Kolka, Z. 'Active Elements for Analog Signal Processing: Classification, Review, and New Proposals' RADIOENGINEERING, VOL. 17, NO. 4, DECEMBER 2008
5. http://nptel.iitm.ac.in
6. http://digital-signal-process.blogspot.in/2011/01/advantage-of-digital-over-analog-signal.html
7. Igor Mucha "New circuit principles for integrated circuits"

   Part 2: Special Function Blocks for Analog Current Signal Processing, Ph.D thesis, BRNO University of Technology-2010

CHAPTER-II

CURRENT CONVEYOR AND ITS DERIVATIVES

2.1 Introduction

Due to the advances made in integrated circuit (IC) technology during the last two decades, circuit designers have quite often exploited the potential of current-mode analog techniques, using current as the medium of signal processing for evolving elegant and efficient solutions to several circuit design problems.

Consequently, current mode circuits are receiving significant attention due to their larger dynamic range, higher band-width, greater linearity, simpler circuitry, lower power consumption, and reduced chip area as compared to their voltage mode counterparts like Operational Amplifiers. In recent years, due to the integration suitability with CMOS technology, current mode devices are finding even more consideration in circuit designs. Analog building blocks, such as current conveyors (CCII) and current controlled current conveyor (CCCII), have emerged as a very useful device to develop various analog signal processing circuits like filters.

The second-generation current conveyor (CCII) is one of the most versatile current-mode building block. Since its introduction it has been used in a wide range of applications and several circuit realizations have been proposed for its implementation.

Current conveyors were introduced in the late sixties, early seventies by Smith and Sedra [1- 2]. In the first years of their appearance the performance of current conveyors was severally limited by the available technologies, which did not allow well-matched devices on fabricated chips. Since the technologies have improved in the eighties, the current conveyors gained the attention of many analog designers. Today the current conveyors have developed to very useful building blocks of analog electronics. They are parts of a number of very often used circuits, like active filters, transimpedance and `current feedback' operational amplifiers, voltage and current operational amplifiers and other more, and their main application areas are in high-speed, high-frequency circuits for both voltage and current signal processing.

2.2 Characteristics of First and Second generation Current Conveyor , (CCI and CCII)

The First generation current conveyor introduced by Smith and Sedra was defined as a three-port device, which can be represented by the figure 2.1

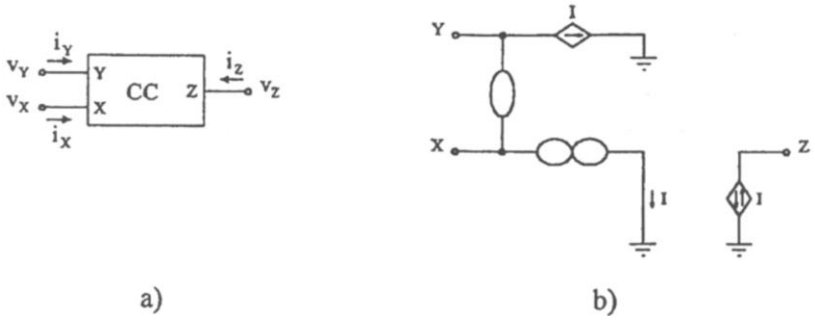


Fig 2.1 CCI (a) Symbol (b) Nullator-Norator representation

This device operates so that the voltage applied to its high-impedance Y-terminal appears also at its low-impedance X-terminal. The current being forced into the X-terminal is conveyed to the high impedance output terminal Z of the current conveyor as well as to its input terminal Y.

Mathematically the performance of the current conveyor can be described by the hybrid equation [3]

$$\begin{bmatrix} I_y \\ v_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix}$$

where the + sign applies for positive current conveyors denoted as CCI+, in which the current flows into both the X- and Z-terminal in the same direction, and the - sign stands for the opposite polarity of the X-to-Z-terminal current transfer of the negative current conveyor CCI-.Somehow this model of Current conveyor didn't become popular.

Later in 1970 a second generation current conveyor was proposed by Smith and Sedra to increase the versatility of the previous generation. In this device no current flows into its input terminal Y and so the mathematical representation of the CCI becomes

$$\begin{bmatrix} I_y \\ v_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & +1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix}$$

for the CCII, where again the + sign denotes the positive X-to-Z current transfer of the positive current conveyor CCII+ and the - sign determines the negative X-to-Z

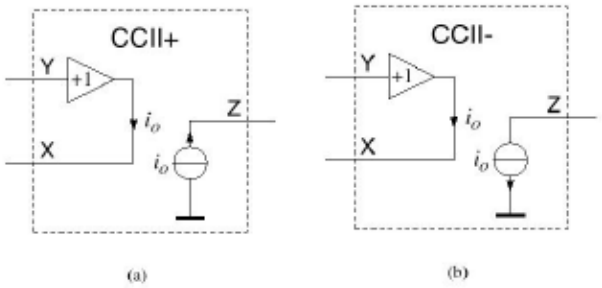


Fig 2.2 (a) The positive conveyor CCII+, $i_z = i_x$. (b) The negative conveyor CCII-, $i_z = - i_x$.

This current-conveyor differs from the first generation conveyor in that the terminal Y is a high impedance port, i.e. there is no current flowing into Y. The Y-terminal of the second generation current- conveyor is a voltage input and the Z-terminal is a current output, the X-terminal can be used both as a voltage output and as a current input. Therefore, this conveyor can easily be used to process both current and voltage signals unlike the first generation current- conveyor or the operational amplifier [4]. The principle of second generation conveyor is shown in Fig 2.2.

Ever since the introduction of Current Conveyors several variations have been proposed to improve the performance resulting into a large number of active blocks that could be classified as derivatives of Current Conveyors. Now we will narrow down the discussion to some of the recently introduced derivatives of Current Conveyors.

2.2 Fully Differential Current Conveyor II (FDCCII)

In 2000 a new active element called Fully differential current conveyor (FDCCII) was proposed [5] to improve the dynamic range in mixed mode application where fully differential signal processing was required.

FDCCII is an important generalization of the conventional CCII. The *x*, *y*, and *z* terminals occur here in pairs. The basic circuit equations of the CCII are now valid for differences of voltages or currents which correspond to these pairs. FDCCII is thus designed for applications with fully differential architecture for fast signal processing.

The circuit symbol of FDCCII is shown in fig 2.3. The Y_1 and Y_2 terminals are high impedance terminals while X_1 and X_2 terminals are low impedance ones.

The differential input voltage V_{Y12} applied across Y_1 and Y_2 terminals is conveyed to differential voltage across the X_1 and X_2 terminals; i.e., ($V_{X12} = V_{Y12}$). The input currents applied to the X_1 and

X_2 are conveyed to the Z_1 and Z_2 terminals that is, ($I_{z1}=I_{x1}$ and $I_{z2}=I_{x2}$). The Z_1 and Z_2 terminals are high impedance nodes suitable for current outputs.

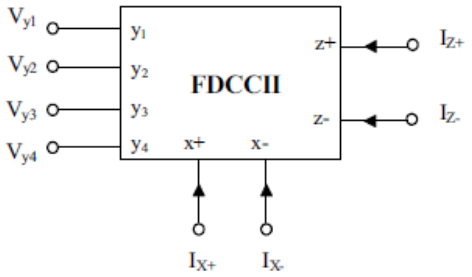


Fig 2.3 The circuit symbol of FDCCII

Taking the Non idealities in to account the voltage current relationship of FDCCII can be characterized by:

$$\begin{bmatrix} V_{x+} \\ V_{x-} \\ I_{z+} \\ I_{z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \beta_1 & -\beta_2 & \beta_3 & 0 \\ 0 & 0 & -\beta_1 & \beta_2 & 0 & \beta_4 \\ \alpha_P & 0 & 0 & 0 & 0 & 0 \\ 0 & \alpha_N & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_{x+} \\ I_{x-} \\ V_{y1} \\ V_{y2} \\ V_{y3} \\ V_{y4} \end{bmatrix}$$

Where ideally $\beta_1 = \beta_2 = \beta_3 = \beta_4 = 1$ and $\alpha_N = \alpha_P = 1$ that represent the voltage and current transfer ratios of the FDCCII .respectively. The CMOS realization of the as proposed by Alzaher, Elwan, and Ismail [6] FDCCII is shown below. In Fig 2.4

All transistors are assumed to be operating in the saturation region.

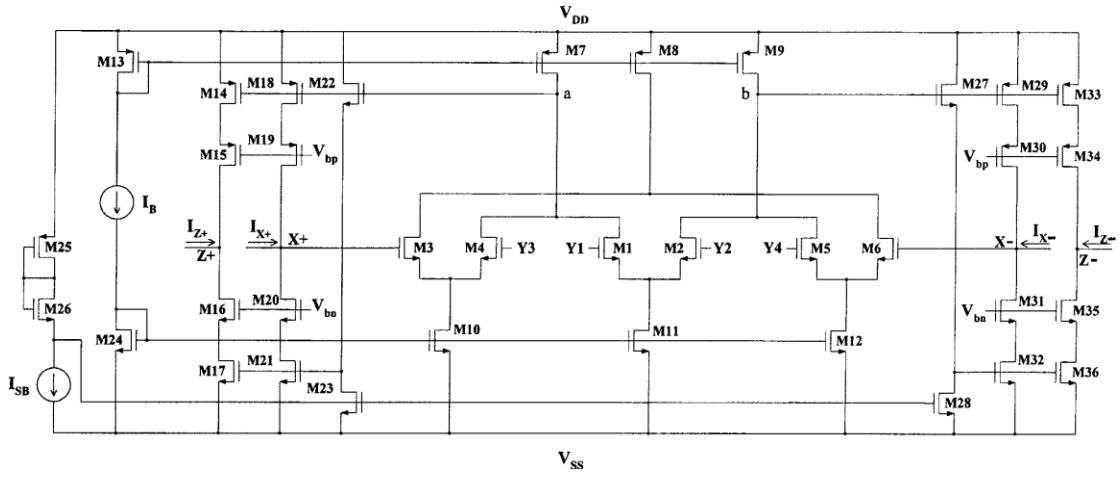


Fig 2.4 CMOS realization of FDCCII

The applications of FDCCIIs in filters and oscillators design using only grounded passive components were demonstrated in [7] [8] A current mode multifunction filter configuration was proposed using FDCCII by Kacar, Metin, Kuntman and Cicekoglu [9].

Four first order voltage mode cascadable all-pass sections using FDCCII as single active element and three grounded passive components were proposed by Jitendra Mohan, Maheshwari, and Chauhan. [10]

2.4 Operational Floating Current Conveyor (OFCC)

The OFCC is a five-port network, comprised of two inputs and three output ports, as shown in Fig. 2.5. The OFCC combines the features of current feedback (CFB) operational amplifier, second generation current conveyor and operational floating conveyor (OFC) [11]. In this diagram, the port labeled X represents a low-impedance current input, port Y is a high-impedance input voltage, W is a low-impedance output voltage, and Z+, and Z- are the high-impedance current outputs with opposite polarities.

Fig 2.5 Block diagram representation of OFCC

The OFCC operates where the input current at port X is multiplied by the open loop transimpedance gain Z_t to produce an output voltage at port W. The input voltage at port Y appears at port X and, thus, a voltage tracking property exists at the input port. Output current flowing at port W is conveyed in phase to port Z+ and out of phase with that flowing into port Z-, so in this case, a current tracking action exists at the output port [12]. Thus, the transmission properties of the ideal OFCC can be conveniently described as:

$$\begin{bmatrix} i_y \\ v_x \\ v_w \\ i_{z+} \\ i_{z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & Z_t & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ i_w \\ v_{z+} \\ v_{z-} \end{bmatrix}$$

Where i_Y and v_Y are the inward current and voltage at the Y port, respectively as shown in Fig 2.5 i_X and v_X are the input current and voltage at the X port, respectively. i_W and v_W are the output current and voltage at W port. respectively i_{Z+} and v_{Z+} are the output current and voltage at Z+ respectively .Z_t represents the impedance between X and W ports.

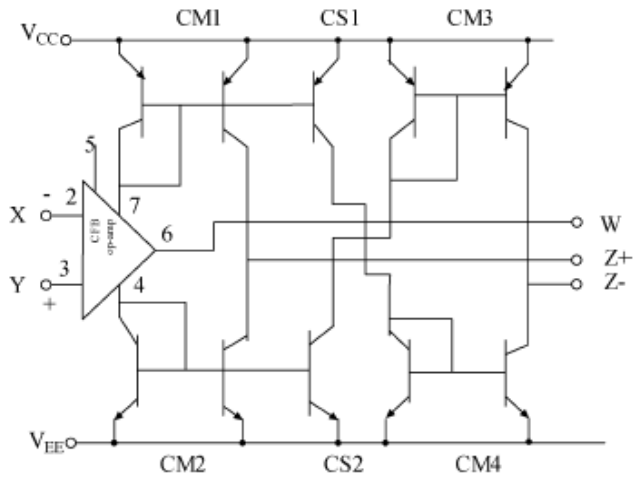


Fig. 2.6 Circuit scheme of OFCC

The OFCC can be implemented by applying the principle of supply current sensing to a current feedback (CFB) op-amp, such as illustrated in Fig. 2.6. The current mirrors CM1 and CM2 establish the output current at port Z+. Also, CM1 and CM2 and their cross-coupling with the current mirrors CM3 and CM4 through the current steering transistors CS1 and CS2 generate a complementary output current at port Z. The OFCC is basically designed to be used in a closed loop configuration, with current being fed back from port W to port X. OFCC is designed with a feedback resistor (negative feedback) between W and X. This feedback resistor allows the OFCC to operate at a positive or negative current-conveyor while simultaneously reducing the input resistance at X port [13]. Also, the negative feedback improves the dc stability as well as the transfer function accuracy [14, 15]. The OFCC, as a current-mode device, shows flexible properties with respect to other current or voltage-mode circuits. A new CMIA circuit based on an OFCC has been proposed by Ghallab, Badawy, Kaler, and Maundy[16].

2.5 Current Controlled Current Conveyor (CCCII)

Current mode circuits like current conveyors are getting significant attention in current analog ICs design due to their higher band-width, greater linearity, larger dynamic range, simpler circuitry, lower power consumption and less chip area.

In 1996 Fabre proposed a second generation current controlled conveyor (CCCII) constructed by bipolar transistors based on CCII and BJT translinear loop [17]. The parasitic resistance at terminal X is given by $R_X=V_T/2I_b$ and it will be able to be controlled by biasing current I_b and is inversely proportional to the biasing current I_b. This gives electronic programmability of CCCII.

It is well accepted that the configurations possessing inbuilt electronic tunability [18] property can easily be adapted for signal processing in integrated circuits environment. The basic second generation current conveyor (CCII) does not have in built tuning property, whereas second generation current controlled current conveyor (CCCII) has, owing to the adjustability of intrinsic resistance at port X of CCCII by bias current.

Since its introduction a variety of CCCII circuits have been proposed: CCCII with negative intrinsic resistance [19]; CCCII based on Wilson current mirror [18]; CCCII operating in radio frequency; CCCII in pseudo-class AB operating in radio frequency. The applications based on CCCII are very extensive: such as current mode filters, oscillators, amplifiers, radio frequency oscillators and low noise amplifiers, ASK/FSK modulators and so on several CMOS implementation of CCCII was also proposed [18].

Description

Fig. 2.7 show the symbol of the second generation Current Controlled Conveyor (CCCII). A CCCII-based circuit, whether positive, negative or dual output, provides electronic tunability and wide tunable range of its resistance at X-terminal [21]. The CCCII requires no external resistors; hence it is very suitable in the design of integrated filters and oscillators. Also, as the CCCII is current controlled current source, the CCCII based circuit is very suitable for high frequency operation.

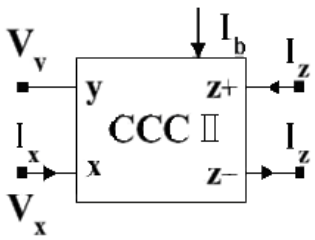


Fig 2.7 Symbol of CCCII

The relationship between the voltage and current variables at input and output ports X, Y and Z of the CCCII can be expressed by the following matrix,

$$\begin{bmatrix} V_x \\ I_y \\ I_z \end{bmatrix} = \begin{bmatrix} R_x & 1 & 0 \\ 0 & 0 & 0 \\ \pm 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix}$$

where the sign ± refers to plus-type or minus-type CCCII, respectively, and R_X denotes the intrinsic resistance at X terminal. R_X is adjustable by a supplied bias current I_b which can be expressed through a class AB trans-linear loop, which is used as input section.

$$I_y = 0 \quad (1)$$

$$V_x = V_y + I_x R_x \quad (2)$$

$$I_z+ = I_x \quad (3)$$

$$I_z- = -I_x \quad (4)$$

A new wideband second generation current controlled conveyor (CCCII) introduced by Barthélemy and Fabre [19] in 2002 and the proposed circuit exhibits an intrinsic resistance at port that is negative. It can also be connected to implement negative controlled resistances that can be either grounded or floating. The new conveyor described in this brief operates in a similar manner but exhibits an intrinsic controlled resistance R_X that is negative. Fig. 1shows the equivalent circuit used to describe a positive/negative type second generation current controlled conveyor (CCCII), [2]. This is equivalent to an ideal positive/negative type CCII in series with an intrinsic resistance at X which value is positive and controlled from the DC bias current I_0.

The voltage and current relationship of the new conveyor with a negative intrinsic controlled resistance is as given

$$\begin{bmatrix} I_y \\ V_X \\ I_{Z1} \\ I_{Z2} \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & -|R_x(I_o)| & 0 \\ 0 & 1 & 0 \\ 0 & -1 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix}$$

here I_{Z1} is the positive-type output current and I_{Z2} the negative-type one.

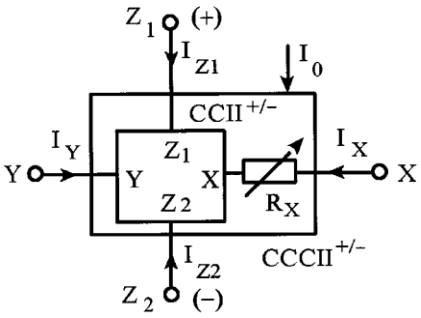


Fig 2.8 Equivalent symbol; of + / - type CCCII

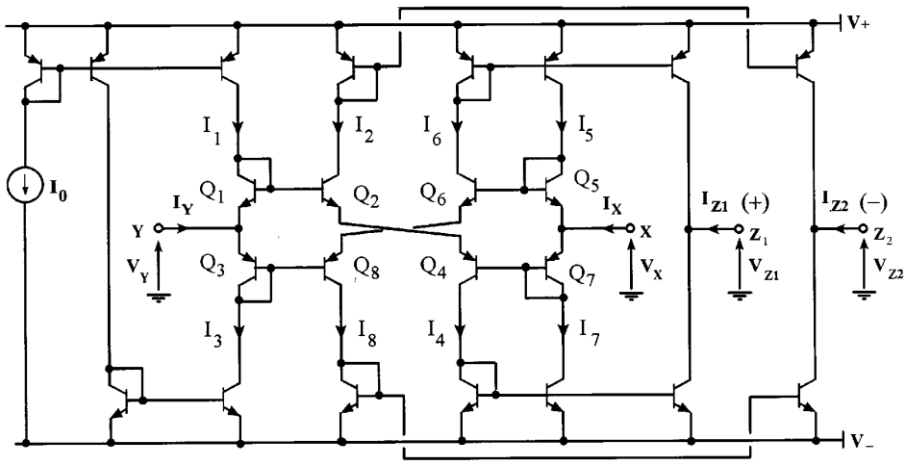


Fig 2.9 The proposed CMOS implementation of CCCII± with negative intrinsic resistance[19]

2.6 Current Controlled Fully Balanced Current Conveyor (CFBCCII)

The circuit symbol of CFBCCII is shown in Fig. 2.10, where I_B denotes the bias current of CFBCCII. Here, Y+, Yare differential voltage input terminals, X+ and X- behave as differential voltage tracking terminals, Z1+, Z2+ and Z1-, Z2- are the current output terminals. The number of current output terminals Z can be extended if necessary. Its ideal port characteristics can be expressed as:

$$\begin{cases} I_{y+} = I_{y-} = 0 \\ V_{x+} - V_{x-} = (V_{y+} - V_{y-}) + (I_{x+} - I_{x-})R_x \\ I_{z1+} - I_{z1-} = I_{z2+} - I_{z2-} = I_{x+} - I_{x-} \end{cases}$$

Where R_X is the parasitic resistance of terminal X

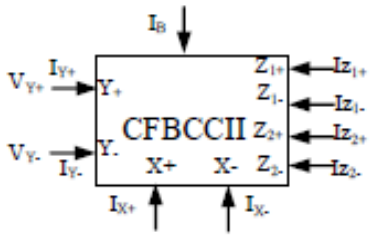


Fig . 2.10 Symbol of CFBCCII

The circuit frame diagram of CFBCCII is given in Fig. 2.11. The circuit is made up of four blocks: the differential voltage input stage, the second-generation current controlled current conveyor (CCCII), voltage-sampling circuit, and the common mode feedback circuit (CMFB). The basic principle of the circuit is analyzed as follows: There are two signal-feed paths in the circuit, the feedforward and thefeedback path. The feedforward path consists of a differential input stage and two CCCIIs. Differential voltage signals are added to the differential input stage, and the voltages would be transferred to the points A and B. The current controlled current conveyors (CCCII) are employed to transfer VA and VB to the output terminals. The feedback path consists of voltage sampling circuit and CMFB circuit [21].

The voltages of the points A and B will be sampled in the voltage sampling block, where the common-mode (CM) voltage VCM is generated. The CMFB circuit is employed to suppress the CM signals, by comparing VCM and VRCM, VCM is forced to follow VCM = VRCM, in this way, the CM signal can be effectively suppressed.

The CFBCCII with fully balanced structure can suppress common-mode signals, and its port relation has electronic programmability. The produced filters from systematic method have fully balanced structure which can reduce even order distortion and common-mode interference effectively. Moreover, the frequency of the filters is electronically adjustable.

The realization of the CFBCCII circuit is illustrated in Fig. 2.12

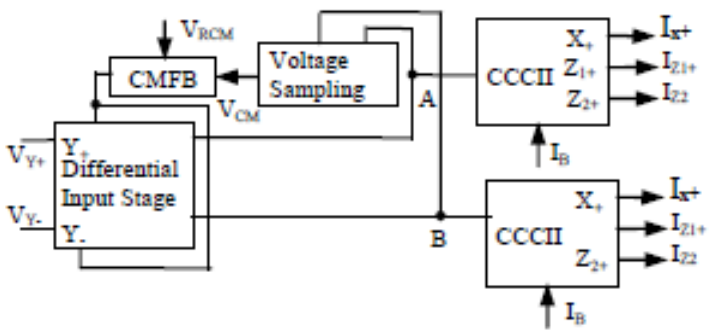


Fig 2.11 Frame diagram of CFBCII

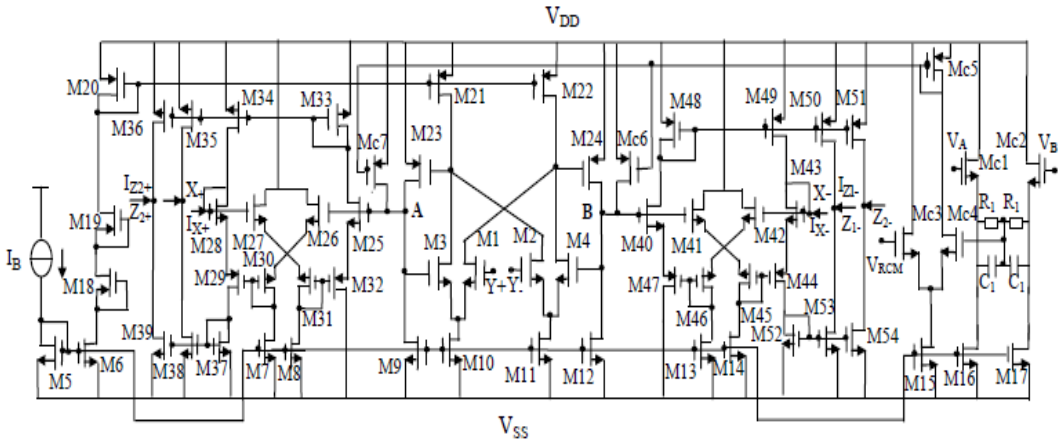


Fig 2.12 Circuit realization of CFBCCII

2.7 Universal Current Conveyor, UCC

A current conveyor is generally a four (or five) terminal device which (when arranged with other electronic elements in specific circuit configurations) can perform many useful analog signal processing functions. Many new types of current conveyors have been designed since the first introduction in 1968 (CCI). There have been the second-(CCII) and the third-generation (CCIII) [22] current conveyors and recently the inverting second generation current conveyor (ICCII) [23]. All these types could be divided into categories which describe the current transfer between X-terminal and output Z-terminal; "+" is for positive transfer (both currents have the same direction), and *"-"* is for negative transfer.

Universal current conveyor proposed by Betva,'Vrba ,Zeman and Musil in 2000 was a versatile building block that was able to replace any type of then existing current conveyor.[24]. The universal current conveyor is an eight port building block. It has three high impedance inputs (differential Y1 , Y2 and summing Y3), one low impedance input X and four current outputs (Z1 , Z2 , $\overline{z1}, \overline{z2}$,). Outputs $\overline{z1}, \overline{z2}$ are complementary to outputs Z1, Z2. The matrix description of UCC and its symbol are given in figure below:

$$\begin{bmatrix} i_{y1} \\ i_{y2} \\ i_{y3} \\ v_x \\ i_{z1} \\ i_{z2} \\ i_{\overline{z1}} \\ i_{\overline{z2}} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_{y1} \\ v_{y2} \\ v_{y3} \\ i_x \\ v_{z1} \\ v_{z2} \\ v_{\overline{z1}} \\ v_{\overline{z2}} \end{bmatrix}$$

Fig 2.13 Matrix description of UCC

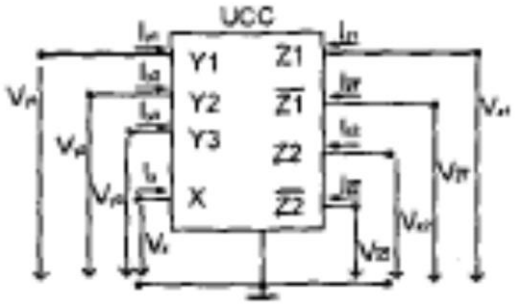


Fig 2.14 Symbol of UCC

All existing types of current conveyor could be realized with the help of UCC providing suitable connection between its terminals. Procedures realizing some of the current conveyors with single high impedance input terminal can be given as in table below shows the possible realizations of current conveyors with differential input.

Type	Inputs	Outputs	Connected	Grounded
CCI-	Y1→Y	$\overline{Z1} \rightarrow Z$	Y1, Z1	Y2, Y3 $Z2, \overline{Z2}$
CCI+	Y1→Y	$Z2 \rightarrow Z$	Y1, Z1	Y2, Y3 $\overline{Z1}, \overline{Z2}$
CCI+/-	Y1→Y	$Z2 \rightarrow Z$ $\overline{Z1} \rightarrow \overline{Z}$	Y1, Z1	Y2, Y3 $\overline{Z2}$
CCII-	Y1→Y	$\overline{Z1} \rightarrow Z$		Y2, Y3 $Z1, Z2, \overline{Z2}$
CCII+	Y1→Y	$Z1 \rightarrow Z$		Y2, Y3 $Z2,$ $\overline{Z1}, \overline{Z2}$
CCII+/-	Y1→Y	$Z1 \rightarrow Z$ $\overline{Z1} \rightarrow \overline{Z}$		Y2, Y3 $Z2, \overline{Z2}$
CCIII-	Y1→Y	$\overline{Z2} \rightarrow Z$	Y1, $\overline{Z1}$	Y2, Y3 $Z1, Z2$
CCIII+	Y1→Y	$Z1 \rightarrow Z$	Y1, $\overline{Z1}$	Y2, Y3 $Z2, \overline{Z2}$
CCIII+/-	Y1→Y	$Z1 \rightarrow Z$ $\overline{Z2} \rightarrow \overline{Z}$	Y1, $\overline{Z1}$	Y2, Y3 $Z2$
ICCI-	Y2→Y	$\overline{Z1} \rightarrow Z$	Y2, Z1	Y1, Y3 $\overline{Z2}, Z2$
ICCI+	Y2→Y	$Z2 \rightarrow Z$	Y2, Z1	Y1, Y3 $\overline{Z1}, \overline{Z2}$
ICCI+/-	Y2→Y	$Z2 \rightarrow Z$ $\overline{Z1} \rightarrow \overline{Z}$	Y2, Z1	Y1, Y3 $\overline{Z2}$
ICCII-	Y2→Y	$\overline{Z1} \rightarrow Z$		Y1, Y3 $Z1, Z2, \overline{Z2}$
ICCII+	Y2→Y	$Z1 \rightarrow Z$		Y1, Y3 $Z2,$ $\overline{Z1}, \overline{Z2}$
ICCII+/-	Y2→Y	$Z1 \rightarrow Z$ $\overline{Z1} \rightarrow \overline{Z}$		Y1, Y3 $Z2, \overline{Z2}$
ICCIII-	Y2→Y	$\overline{Z2} \rightarrow Z$	Y2, $\overline{Z1}$	Y1, Y3 $Z1, Z2$
ICCIII+	Y2→Y	$Z1 \rightarrow Z$	Y2, $\overline{Z1}$	Y1, Y3 $Z2, \overline{Z2}$
ICCIII+/-	Y2→Y	$Z1 \rightarrow Z$ $\overline{Z2} \rightarrow \overline{Z}$	Y2, $\overline{Z1}$	Y1, Y3 $Z2$

CMOS Implementation

A universal current conveyor was designed in CMOS form using CMOS technology AMS 1.2µm. The circuitry of UCC is shown in Fig. 2.15. All transistors operate in the saturation region.

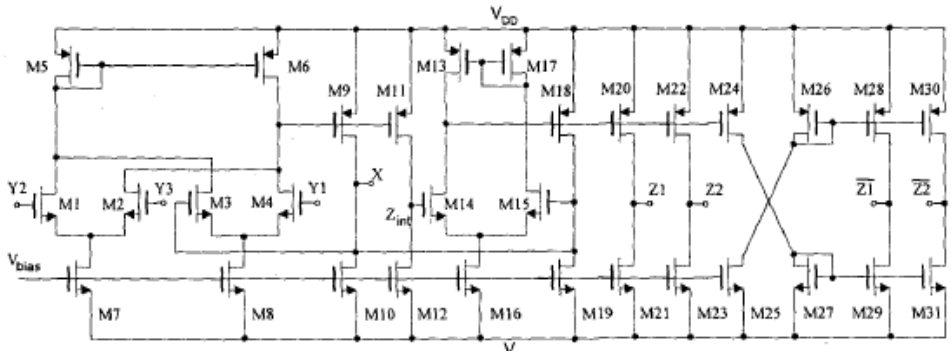


Fig 2.15 CMOS implementation of Universal Current conveyor

2.8 Fully Balanced Second Generation Current - Conveyor, FBCCII

The second-generation current conveyor (CCII) is one of the most versatile current-mode building block. The CCII is a single ended device, however, most modern high-performance analog integrated circuits incorporate fully balanced signal paths. This is because fully balanced operation improves the performance of analog systems in terms of noise rejection, dynamic range and harmonic distortion [25] and reduces the effect of coupling between various blocks [26]. Moreover, most modern systems employ both analog and digital parts on the same chip. A fully balanced architecture of the analog part becomes more essential as it provides immunity to digital noise.

Alzaher, Elwan, and Ismail proposed in their paper in 2003 the design of a fully balanced secondgeneration current conveyor (FBCCII) which is obtained by sensing the output currents of a fully balanced version of CMOS differential difference amplifier (DDA) [27]

(FBCCII) is a six-terminal device and we give it the symbol shown in Fig 2.16. The FBCCII can be described by

$$\begin{bmatrix} I_y \\ v_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix}$$

However, here all signals are in differential form

(i.e., $V_{dx} = V_{xp} - V_{xn}$, $V_{dy} = V_{yp} - V_{yn}$, $I_{dx} = I_{xp} - I_{xn}$, $I_{dz} = I_{zp} - I_{zn}$).

In addition, all CM (common mode)output signals should be ideally zero (i.e.$V_{cmx} = (V_{xp} + V_{xn})/2 = 0$, $I_{cmx} = (I_{xp} + I_{xn})/2 = 0$, $I_{cmz} = (I_{zp} + I_{zn})/2 = 0$)). In FB system, there is no need for inverters

as the input or the output terminals can be exchanged to change the transfer function polarity. Thus, both the positive and negative CCII types have the same fully balanced realization.

A fully balanced architecture of the DDA (FBDDA) is designed in a similar manner as the conventional op-amp resulting in a differential output ($V_{op} = -V_{on}$). A current sensed FBDDA is obtained by copying the currents through the two output terminals (V_{op} and V_{on}) to two additional current ports (I_{zp} and I_{zn}) using current mirrors. The current sensed FBDDA can be configured as a FBCCII by feeding back the two output voltage terminals (V_{op} and V_{on}) to two of the inputs (V_{pn} and V_{nn}), respectively. Thus the feedback results in $V_{dy} = V_{dx}$ and I_{dz} becomes equal to I_{dx}. Also, the feedback action develops the required low input impedance at the terminals.With unity gain feedback, the proposed FBCCII exploits the entire frequency operating range of the FBDDA that is its unity gain frequency.

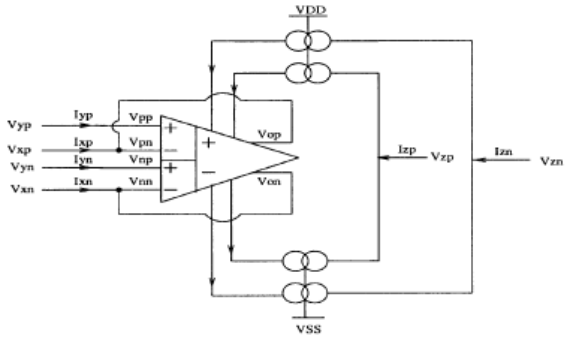


Fig 2.16 Fully balanced realization of CCII [27]

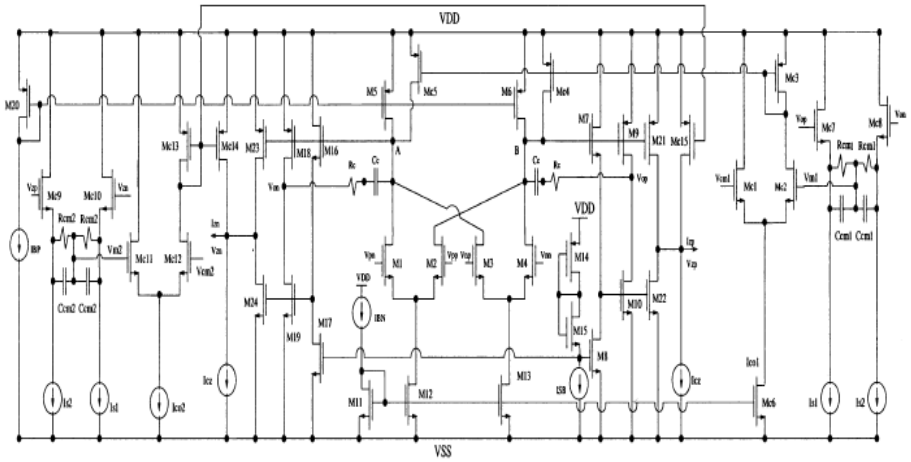


Fig 2.17 CMOS implementation of FBCCII

2.9 Dual-X Current Conveyor, DXCCII

One active element which has been recently popularized by analog circuit designers is dual-X second generation current conveyor (DXCCII). It was introduced in 2002 by Zeki,, Toker [28]. The DXCCII is a combination of conventional second generation current conveyor and inverting second generation current conveyor (ICCII) [1], [2]. It is more versatile as it combines the features of both CCII and ICCII.

A DXCCII, shown in Fig. 2.18 is characterized by the following ideal terminal relationship:

$$\begin{bmatrix} I_y \\ V_{XP} \\ V_{XN} \\ I_{ZP} \\ I_{ZN} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ -1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_y \\ I_{XP} \\ I_{XN} \end{bmatrix}$$

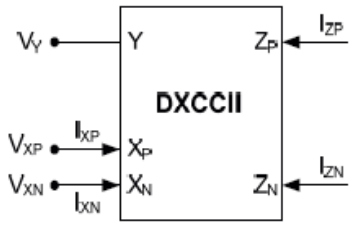


Fig . 2.18 Symbolic representation of DXCCII

Maheshwari, Ansari in their paper proposed 15 practical realizations of DXCCII some using only AD-844 and rest with AD-844 and opamps [29].

Its known fact that AD-844 is equivalent to a second generation current conveyor with additional feature of buffered voltage output and has been a natural choice for realizing current conveyor and its assorted off shoots. One such realization of DXCCII using AD844 proposed by Maheshwari,r Ansari is given in figure below

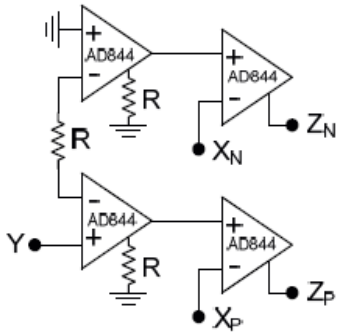


Fig 2.19 Practical realization of DXCCII using AD844

2.10 Modification of Third Generation Current Conveyor, MCCII

The third generation current conveyor (CCIII) presented by Fabre [22] is shown to be a useful active element to pick up the current of a floating passive element. However it is shown that Fabre's conveyor can also be used to implement different circuit blocks. A CMOS implementation of CCIII is presented in [30]. CCIII can be considered as a current controlled current source with unity gain. The use of controlled sources with unity gain in the design of active- RC filters leads to structures with tight design equations. In order to relieve these, it may be useful to insert a gain larger than unity. In a recent work, a new active building block, modified CCIII (MCCIII) is introduced to realize this property and to provide new possibilities in the circuit synthesis using this element [31].

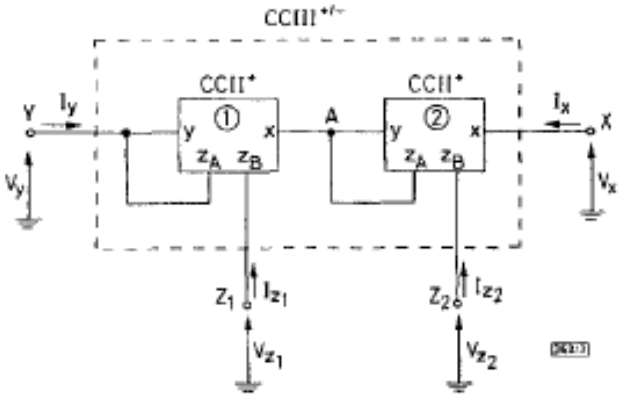


Fig 2.20 CCIII as proposed by Fabre using two CCII+

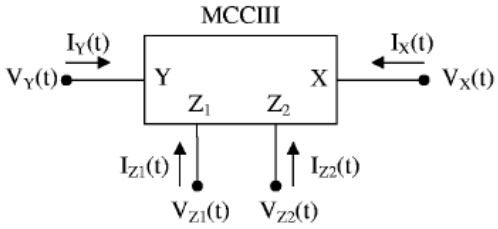


Fig 2.21 Ideal modified Third generation current conveyor

An ideal modified third generation current conveyor shown in Fig. 2.21 is characterized by the following constitutive relations.

$$\begin{bmatrix} I_y \\ V_x \\ I_{z1} \\ I_{z2} \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & -k & 0 & 0 \\ 0 & 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_{z1} \\ V_{z2} \end{bmatrix} \quad \text{.....(a)}$$

According to this equation, the element offers a current gain of –1 between ports X and Y, a current gain of 1 between ports X and Z_2 and a current gain of –k (usually k=2) between ports X and Z_1. The latter property enables new possibilities in circuit design.

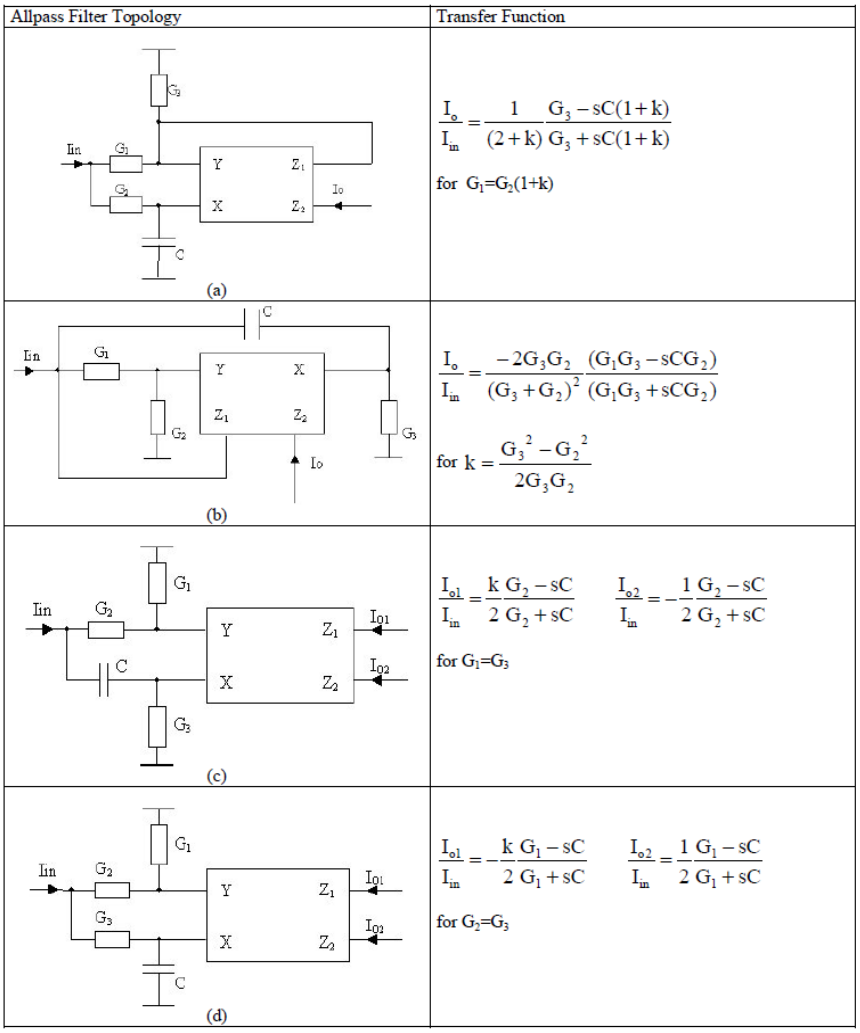


Fig 2.22 MCCIII based all pass filters and related transfer functions

Fig. 2.22 Illustrates current-mode allpass filters as proposed by Bodur , Kuntman, Cicekoglu [28] using a single MCCIII. The related transfer functions are also given in Fig. 2.22. Note that the multiplier k provides flexibility to obtain any desired gain value for the allpass transfer function which is not possible for the standard CCIII.

References

1 K.C. Smith, A .Sedra. 'The current conveyor: a new circuit building block'. IEEE Proc. CAS, 1968, vol. 56, no. 3, p. 1368-1369.

2 A. Sedra, K.C. Smith, 'A second generation current conveyor and its application'. IEEE Trans., 1970, CT-17, p. 132-134.

3 Igor Mucha 'New circuit principles for integrated circuits' Part 2: Special Function Blocks for Analog Current Signal Processing, Ph.D thesis, BRNO UNIVERSITY OF TECHNOLOGY-2010

4 Indu.Prabha Singh, K. Singh and S.N. Shukla 'Current Conveyor: Novel Universal Active Blocks'-JPSET, Vol. 1, Issue 1-2010

5 El-Adway, A. M. Soliman and H. O. Elwan, A Novel Fully Differential Current Conveyor and its Application for Analog VLSI, IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, Vol. 47, No. 4, 2000, pp. 306-313.

6 H. Alzaher, H. Elwan, and M. Ismail, 'CMOS fully differential secondgeneration current conveyor,' Electron. Lett., vol. 36, pp. 1095–1096, June 2000.

7 M. Chang, B. M. Al-Hashimi, C. I. Wang and C. W. Hung, "Single Fully Differential Current Conveyor Biquad Filters," IEE Proceedings on Circuits, Devices and Systems, Vol. 150, No. 5, 2003, pp. 394-398.

8 J. W. Horng, C. L. Hou, C. M. Chang, H. P. Chou, C. T. Lin and Y. Wen, "Quadrature Oscillators with Grounded Capacitors and Resistors Using FDCCIIs," ETRI Journal., Vol. 28, 2006, pp. 486-494.

9 F. Kacar, B. Metin, H. Kuntman and O. Cicekoglu 'Current-mode multifunction filters using a single FDCCII' ELECO -2009,Dec-2009

10 J. Mohan, S. Maheshwari, D. S. Chauhan 'Voltage Mode Cascadable All-Pass Sections Using Single Active Element and Grounded Passive Components' Circuits and Systems, 2010, 1, 5-11**,** Published Online July 2010 (http://www.SciRP.org/journal/cs) .

11 Y. H. Ghallab, M. Abo El-Ela, and M. Elsaid, 'Operational floating current conveyor: Characteristics, modeling and experimental results,' in Proc. ICM, Kuwait, 1999, pp. 59–62.

12 J. Azhari and H. Fazalipoor, "A novel current-mode instrumentation amplifier (CMIA) topology," IEEE Trans. Instrum. Meas., vol. 49, no. 6, pp. 1272– 277, Dec. 2000.

13. Y. H. Ghallab, W. Badawy, Karan V. I, S. Kaler and Brent J. Maundy, 'A novel current -Mode Instrumentation Amplifier Based on Operational Floating Current Conveyor' IEEE Trans. Instrum measu., vol. 54, no. 5, October 2005

14. S. J. Azhari and H. Fazalipoor, 'A novel current-mode instrumentation amplifier (CMIA) topology,' IEEE Trans. Instrum. Meas., vol. 49, no. 6, pp. 1272– 277, Dec. 2000.

15. S. J. G. Gift, 'An enhanced current-mode instrumentation amplifier,' IEEE Trans. Instrum. Meas., vol. 50, no. 1, pp. 85–88, Jan. 2001.

16. Y. H. Ghallab, W. Badawy, , Karan V. I. S. Kaler and Brent J. Maundy, 'A novel current -Mode Instrumentation Amplifier Based on Operational Floating Current Conveyor' IEEE Transactions on Instrumentation and measurement, vol. 54, no. 5, october 2005

17. A. Fabre, O. Saaid, F. Wiest, and C. Boucheron 'High Frequency Applications Based on A new Current Controlled Conveyor' IEEE Transactions On Circuits And Systems-I: Fundamental Theory And Applications, Vol. 43, No. 2, February 1996.

18. W. Chunhua, S. Zhixing, L. Haiguang " New CMOS Current-controlled Second Generation Current Conveyors" 978-1-4244-1708-7/08 ,2008 IEEE

19. H. Barthelemy and A. Fabre. A second – generation current controlled conveyor with negative intrinsic resistance. IEEE Transactions on Circuit Systems-I. 2002, **49**: 63-65.

20. A.Fabre, O. Saaid, F. Wiest, and C. Boucheron, "Current controllable bandpass filter based on translinear conveyors," Electron. Lett, vol. 31,pp.1727–1728, 1995.

21. W. Chunhua, L. Yang, Z. Qiujing, F. Yu **'**Systematic Design of Fully Balanced Differential Current-Mode Multiple-Loop Feedback Filters Using CFBCCII' Radioengineering, vol. 19, no. 1, April 2010

22. A.Fabre.: 'Third-generation current conveyor: A new helpful active element', Elec. Letters, Vol. 31, NOS, pp. 338-339, Mar. 1995

23. L.A.Awad, and A.M Soliman:'Inverting second generation current conveyors: the missing building blocks, CMOS realizations and applications', Int.J.Electronics, 1999, Vol. 86, pp. 413-43.

24. D. BEČVÁŘ, K.. VRBA, V.ZEMAN, V. MUSIL, 'Novel universal active block: a universal current conveyor'. In Proc. of the IEEE Int. Symp. on CAS. Geneva (Switzerland), vol. 3, 2000. p. 471-473.

25. D. Johns and K. Martin, Analog Integrated Circuit Design. New York: Wiley, 1997, ch. 6.

26. J. Rudell, J.-J. Ou, T. Cho, G. Chien, F. Brianti, J. Weldon, and P. Gray, "A 1.9-GHz wide-band IF double conversion CMOS receiver for cordless telephone application," IEEE J. Solid-State Circuits, vol. 32, pp. 2071–2088, Dec. 1997.

27. H. A. Alzaher, H. Elwan, and A.M. Ismail 'A CMOS Fully Balanced Second-Generation Current Conveyor' IEEE Transactions on circuits and systems-II :Analog and digital signal processing , Vol.50, No.6, JUNE 2003.

28. A. Zeki, A. Toker, 'The dual-X current conveyor (DXCCII): a new active device for tunable continuous-time filters'. International Journal of Electronics, 2002, vol. 89, no. 12, p. 913-923.

29. S. Maheshwari., M.S. Ansari 'Catalog of Realizations for DXCCII using Commercially Available ICs and Applications' Radioengineering, VOL. 21, NO. 1, April 2012

30. A Piovaccari, 'CMOS integrated third generation current conveyor', Electron. Letters, 31, no. 15, pp. 1228-1229, 1995.

31. H. Kuntman, O. Cicekoglu and S. Ozoguz. 'A modified third generation current conveyor, its characterization and applications', Frequenz, Vol.56, pp.47-54, 2002

CHAPTER III

OPAMPs, FTFNs, HYBRID OPAMP – CCs

3.1 Four Terminal Floating Nullor and Multioutput- FTFN

Active devices widely used in current mode circuit are usually a second-genertion current conveyor (CCII),a current feedback op-amp (CFOA), a four terminal nullor (FTFN) and operational transconductance amplifier(OTA).

However it has been shown that the FTFN is more flexible and versatile building block than other active devices [1]. Interest in using FTFNs to design current mode circuits has increased recently due to the fact that FTFN-based structures provide a number of potential advantages such as: complete absence of passive component matching requirement , minimum number of employed passive elements and improvement of high frequency characteristic.

Many FTFN realization schemes are based on the use of conventional op-amps as the major active element. These realization schemes are less appropriate for high frequency applications and are uneconomical for applying to an integrated circuit form. In monolithic form their realization becomes too complicated.

Jiraseri-amornkun, Chipipop and Surakampontorn in 2001 proposed an alternate form for realizing a monolithically integrable multi output FTFN [2]. Which offers higher gain and wider dynamic range.

Circuit Description

FTFN is a high gain transconductance amplifier with floating input or can be called as an Operational Floating Amplifiers (OFAs) [3]. Figure below shows a nullor model of a FTFN, which is equivalent to an ideal nullor.

The port relations of the FTFN can be characterized as

$$V_1 = V_2 \qquad I_1 = I_2 = 0 \qquad I_{01} = -I_{02}$$

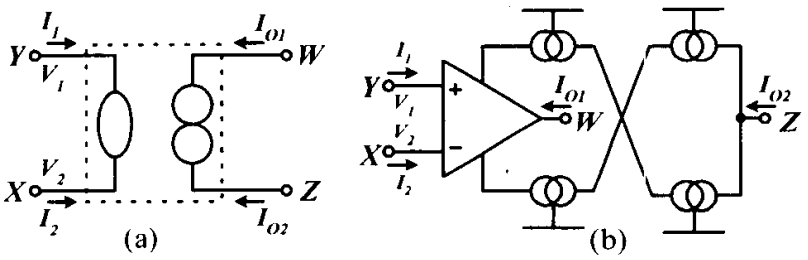


Fig 3.1. Model of an FTFN (a) Nullor model (b) Traditional implementation

The output impedance of the W and Z ports are generally arbitrary. However most of the FTFNs are traditionally realized from the basic type shown in Fig.3.1b, where the output impedance of the W port is very low while that of Z port is very high. This type of FTFN is also called operational mirrored amplifiers (OMAs) [4].

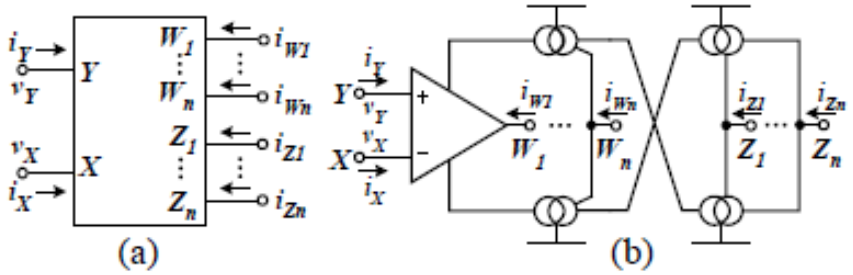


Fig 3.2. (a) Symbol of multioutput FTFN (b) Possible implementation of multioutput FTFN

Fig 3.2 (a) shows the schematic diagram of multi-output FTFN as proposed by Jiraseri-amornkun, Chipipop and Surakampontorn, [2] it can be characterized by the relation

$V_1 = V_2$ $I_1 = I_2 = 0$ $I_{01} = I_{02} = - I_{03}$

The bipolar integrated form of the multioutput FTFN is shown in figure below

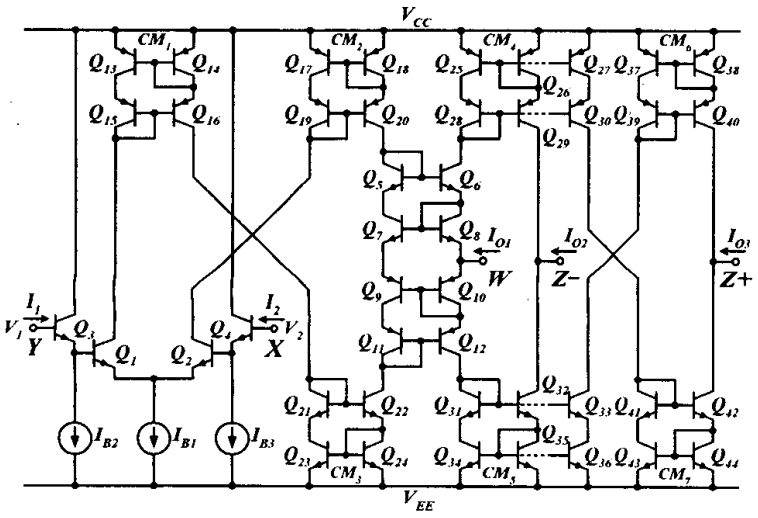


Fig 3.3 The bipolar integrated form of the multioutput FTFN

An alternative realization scheme for realizing a monolithically integrable multi-output FTFN or multi-terminal floating nullor (MTFN), which provides electronically variable current gain was proposed by Tangsrirat in 2008 [5]. The proposed circuit is based on the use of a transconductance amplifier, an improved translinear cell and some current mirrors.

Fig. 3.4 shows the cascade npn current mirror that can adjust the current gain by the external bias currents, where I_{in} and I_{out} are respectively the input and output signal currents.

Transistors Q_1 to Q_4 function as a classical translinear loop, and the currents I_1 and I_2 are the external DC bias currents [6]. In addition, the cascade stages Q5 and Q6 provide the high output impedance and also lead to minimize the severe peaking of the frequency responses [7]. Applying the translinear principle and assuming that all the transistors are well matched with the common-emitter current gains $\beta >> 1$, then the relationship of the collector currents can be characterized by the following equation:

$$I_{C1}I_{C3} = I_{C2}I_{C4}$$

where $I_{C1} = I_1$, $I_{C2} = I_2$, $I_{C3} =$ Iin and $I_{C4} = I_{out.}$ Therefore, the output current $I_{out.}$ of this circuit becomes

$$I_{out.} = k.I_{in}$$

where k is the current gain of the mirror and equals to the ratio of the external bias currents I_1 / I_2.

Cascade npn current mirror with adjustable current gain

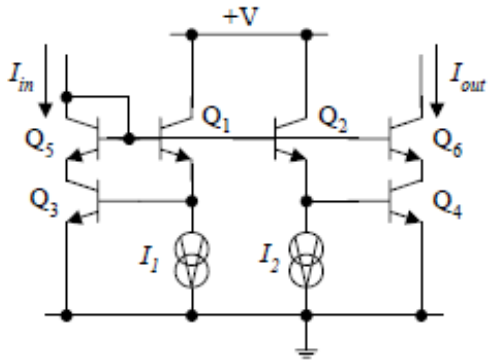
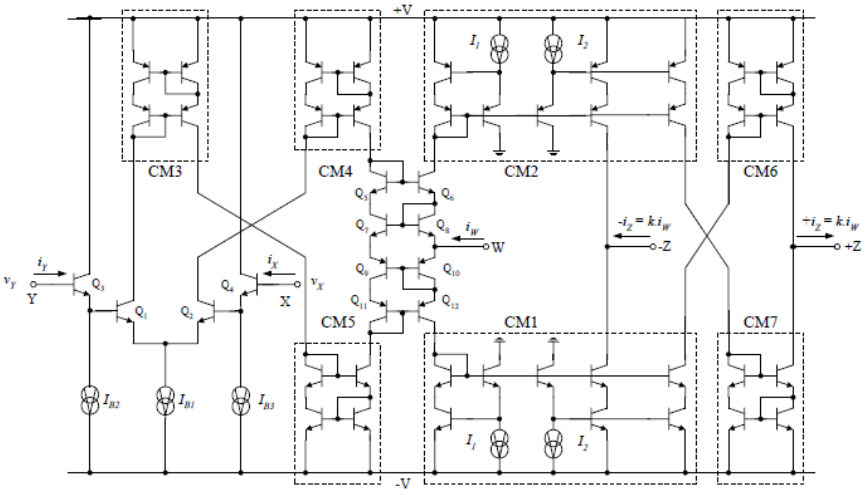
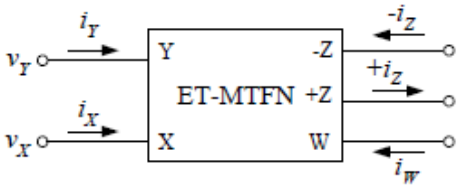


Fig 3.4 Cascade npn current mirror with adjustable current gain

The circuit implementation and representation of the proposed electronically tunable MTFN, namely ET-MTFN, is shown in Fig. **3.5** below,



(a)



(b)

Fig **3.5** ET-MTFN (a) bipolar realization , (b) its symbol

3.2 Tunable FTFN

Even though FTFN structures have a number of potential advantages till the intial years of last decade tunable FTFN (TFTFN), whose current gain can be varied was not practically realized. The FTFN whose the current gain can be electronically tuned is more attractive, flexible and suitable for design and implementation of the frequency selective systems, suchas, biquads, oscillators and so forth. It was the team of Tangsrirat, Dumawipata and Surakampontorn who in 2001 proposed the realization of FTFN with variable current gain [8].

In [8] a simple circuit technique for realizing the FTFN with variable current gain is proposed. The circuit realization uses an op amp in input together with current mirrors with adjustable current gain to constitute output Z, which can be adjusted current transfer ratio between port W and Z by tuning the extemal bias current. Some applications using the proposed tunable FTFN were given with the simulation results and it showed that the characteristics of the resulting circuit become an electronically tunable.

The circuit implementation and circuit representation of the proposed tunable FTFN, namely TFTFN, with variable current gain deduced from an ideal FTFN are shown in Fig. 3.6**.** The circuit consists of an opamp, two complementary current mirrors with controlled gain CM1 - CM2, and two standard improved Wilson current mirrors CM3-CM4. Therefore, the current flowing through the port W will reflect to the port Z, which has the current transfer ratio as $k = iz / iw$**,** and consequently this TFTFN will provide a unity voltage transfer between port Y and X**,** and a current transfer between port W and Z that the gain value is equal to k**.** In the same way as mention from eqn.(l), a four-port device that realizes TFTFN can be rewritten as :

$$i_y = i_x = 0 \text{ , } v_x = v_y \text{ and } i_z = \text{k } i_w$$

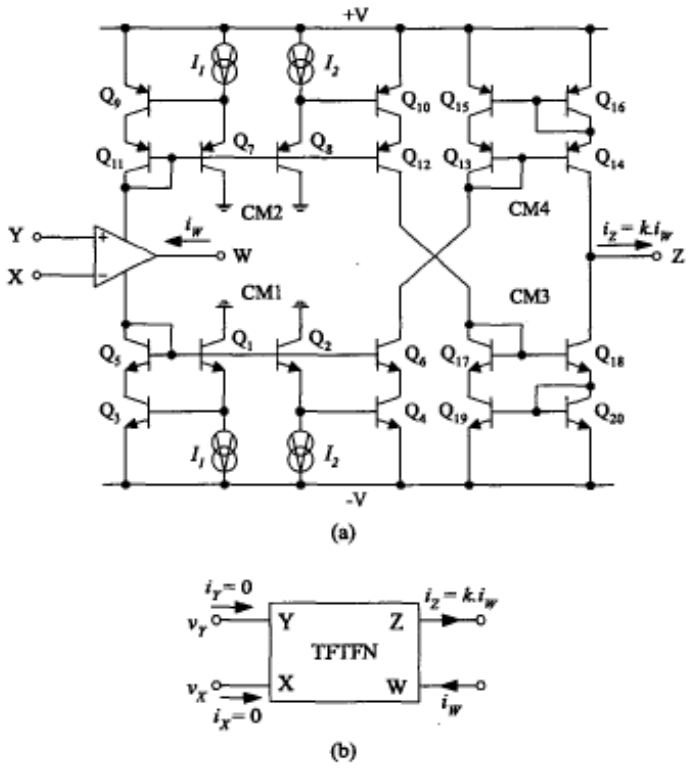


Fig **3.6** TFTFN with variable current gain (a) circuit diagram (b) symbol

A similar practical implementation of FTFN with variable voltage and current gain was proposed by Hirunporm, Unhavanich, Tangsrirat, and Surakampontorn.in 2007[9]. The proposed tunable FTFN offers independently variable dc voltage and current gains while remaining a constant bandwidth. Moreover, the dc gains of the circuit can be tuned by adjusting grounded resistors without effecting the useful bandwidth. The performances of the proposed variable-gain FTFN using a commercial AD844 IC is verified.

3.3 Fully Balanced FTFN , FBFTFN

The four-terminal floating nullor (FTFN) combines both voltage and current mode capabilities is a more versatile analog building block than the operational amplifier (opamp) or the second-generation current conveyor (CCII) [10–14]. It has been used in several applications ranging from current amplifiers, voltage to current converters, gyrators, floating immittances to active-RC filters and sinusoidal oscillators.

In modern systems, analog and digital circuits are implemented in the same integrated circuit (IC) chip. Therefore, it is required to implement the analog part using fully balanced architecture. Fully balanced systems are more immune to digital noise. In addition, fully balanced architectures are used in high performance analog applications to enhance the dynamic range, reduce harmonic distortion, and minimize the effect of coupling between various blocks [15]. The single single-ended FTFN is, therefore, not suitable for mixed analog and digital Circuits.

A method was proposed by Alzaher and Mohammed Ismail [16] for the design and implementation of fully balanced FTFN (FBFTFN) using the proposed circuit, any single ended FTFN based circuit can be converted to its fully balanced architecture. This paves the way for FTFN-based circuits to be used in IC applications. A low-power class AB CMOS realization of the proposed FBFTFN is fabricated in a 1.2- m chip. Proposed FBFTFN provides solutions for fully balanced realizations of both voltage and current-mode circuits.

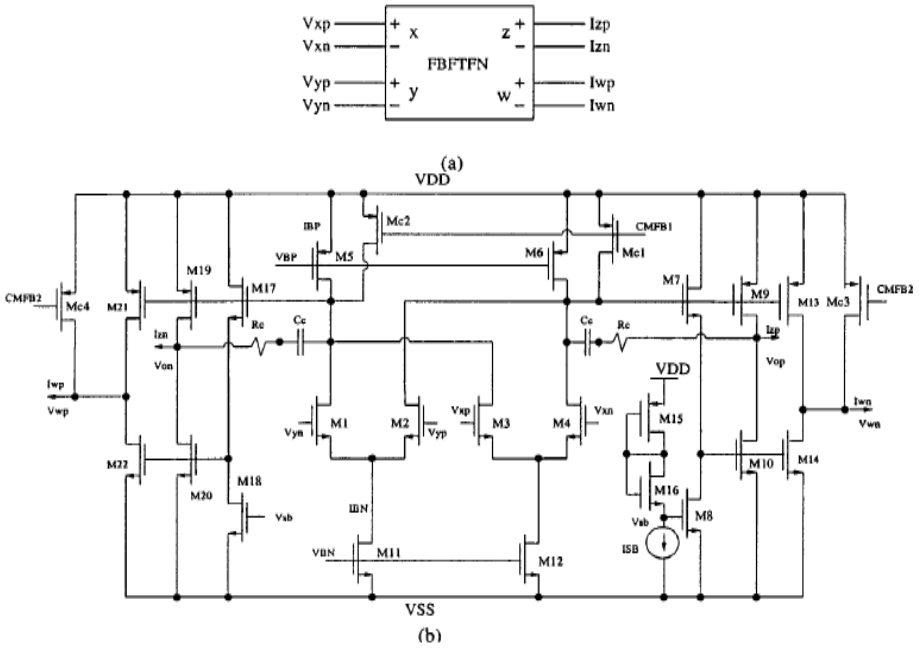


Fig **3.7** FBFTFN (a) Symbol (b) CMOS implementation

According to the FTFN definition, its fully balanced version is an eight terminal device that can be characterized by the following equations:

$$I_{xp} = I_{xn} = I_{yp} = I_{yn} = 0$$

$$V_{dx} = V_{xp} - V_{xn} = V_{dy} = V_{yp} - V_{yn}$$

$$I_{dz} = I_{zp} - I_{zn} = -I_{dw} = -(I_{wp} - I_{wn}).$$

The proposed low-power CMOS realization is shown in Fig. **3.7**(b). It has been fabricated in a 1.2- m N-well CMOS process with the device sizes shown in Table I. Like the op amp, the circuit consists mainly of two stages: a differential-input single ended output transconductance stage (differential pair with active loads) and a second gain stage. Class AB output stages are used to achieve well determined low standby power consumption with good output current driving capability instead of the conventional class A (common-source amplifier) counterparts

Device sizes

Device Names	W/L (μm/μm)
M_1, M_2, M_3, M_4	198/3.0
M_5, M_6	99/3.0
M_7, M_8, M_{17}, M_{18}	9/4.8
M_9, M_{13}, M_{15}, M_{19}, M_{21}	180/2.4
M_{10}, M_{14}, M_{16}, M_{20}, M_{22}	72/2.4
M_{11}, M_{12}	150/2.4
M_{c1}, M_{c2}	99/3.0
M_{c3}, M_{c4}	180/2.4

3.4 Current Feedback Amplifiers, CFA

Among the various current –mode active building blocks, the current feedback amplifier (CFA) or current feedback operational amplifier (CFOA) is an interesting active component, especially suitable for a class of analog signal processing [17-19]. This device can operate in both current and voltage modes, provides flexibility and enables a variety of circuit designs. In addition, it can offer advantageous features such as high-slew rate, free from parasitic capacitances, wide bandwidth and simple implementation [20-22]. Presently, the CFA can be commercially found, for example AD844 of Analog Devices Inc. [23]. It can be employed to realize filters], amplifiers, oscillators], inductance simulators, and etc.

Conventionally, the electrical characteristics for applications of the CFAs cannot be adjusted by electronic methods, which this means that they cannot be controlled by currents and/or voltages. Although, they can be achieved by passive element adjustments, the electronic control method is being more popular more than those by passive elements (i.e. resistors and capacitors) due to it can be easily adapted to automatic or microcontroller-based controls. In addition, the CFA can not be controlled by the parasitic resistance at current input port so when it is used in a circuit, it must unavoidably require some external passive components, especially the resistors. This makes it not appropriate for IC implementation due to occupying more chip area, high power dissipation and cannot be electronic controllable. If it is employed for an off-the-shelf design, the circuit

description is composed of a large number of external passive elements. Thus, a modified-version CFA whose parasitic resistance at current input port can be controlled by an input bias current, called current controlled current feedback amplifier (CC-CFA**),** was proposed by Siripruchyanun, Chanapromma, Silapan, and Jaikla [24]. To reduce offset phenomenon, a BiCMOS technology was used for realizing the proposed element. In addition, the voltage follower was also developed to reduce the offset output current and voltage. The CFA properties can be shown in the following equation

$$\begin{bmatrix} I_y \\ V_X \\ I_Z \\ V_w \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} I_x \\ V_y \\ V_z \\ V_w \end{bmatrix}$$

The symbol and the equivalent circuit of the CFA are illustrated in Fig. 3.8(a) and (b), respectively. A circuit implementation of CFA can be achieved by using second-generation current conveyor (CCII) as input stage, followed by a buffered amplifier as depicted in Fig. 3.8(c).

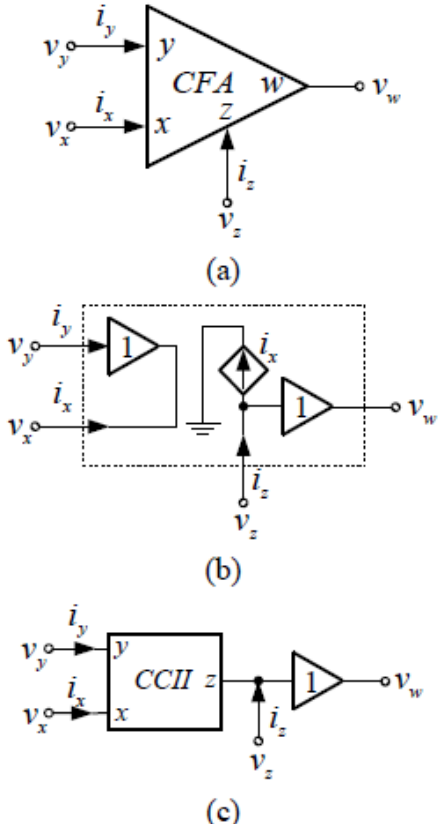


Figure **3.8**. CFA (a) Symbol (b) Equivalent circuit (c) Element implementation

3.5 Basic Concepts of CC-CFA

CC-CFA properties are similar to the conventional CFA, except that the CC-CFA has finite input resistance *Rx* at the *x* input terminal. This parasitic resistance can be controlled by the bias current I_B as shown in the following equation

$$\begin{bmatrix} I_y \\ V_X \\ I_Z \\ V_w \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ R_x & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} I_x \\ V_y \\ V_z \\ V_w \end{bmatrix}$$

Where, $R_x = \frac{V_T}{2I_B}$

V_T is the thermal voltage, which is 26mV at room temperature.

The symbol and equivalent circuit of the CC-CFA are illustrated in Fig. 3.9 (a) and (b), respectively. In similar, we can realize the CC-CFA by using second-generation current controlled current conveyor (CCCII) as input stage, followed by a buffered amplifier as illustrated in Fig. 3.9 (c).

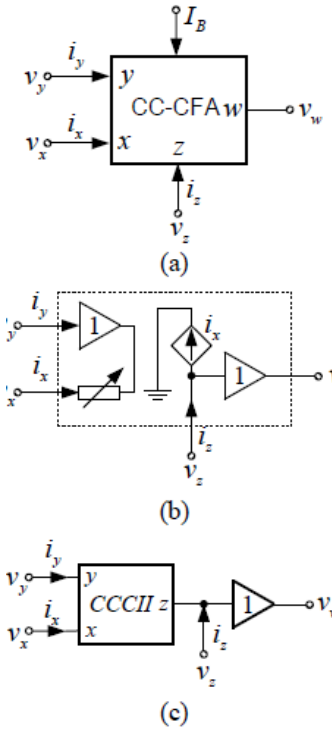


Figure **3.9**. CC-CFA (a) Symbol (b) Equivalent circuit (c) Element implementation

The proposed CC-CFA consists of two principal blocks: a second generation current controlled current conveyor and the modified voltage buffer, as explained. The proposed realization of the CC-CFA in BiCMOS technology is shown in Fig. 3.10. The second-generation current-controlled current conveyor as input stage consists of mixed translinear loops (Q6-Q9). The mixed loops are DC biased by I_B using current mirrors (M1-M3 and M10- M11). The output z-terminal that generates the current of x terminal is realized using CMOS (M4- M5 and M12-M13). The buffered amplifier is realized using BJTs and CMOS (Q10-Q22 and M14-M21, respectively). Only npn transistors are employed in this topology, which enables to achieve high frequency. A traditional high frequency class AB voltage follower, providing better linearity than its equivalent class A structure, could be implemented but such technology requires complex and costly additional mask levels that constrain several companies to use only "standard" BiCMOS technology, which high frequency pnp bipolar junction transistor is not available [24].

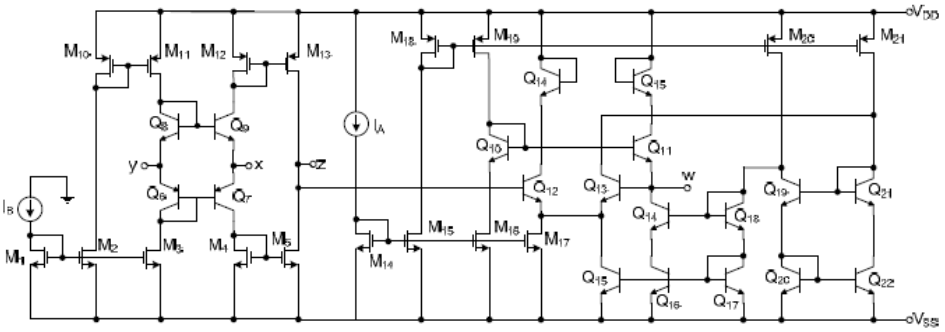


Figure **3.10**. BiCMOS current controlled current feedback amplifier

The proposed CC-CFA shows low distortions, low output offset errors and wide bandwidth of frequency responses and it is very appropriate to realize in commercially purposed integrated circuit for employing in instrumentation/measurement systems, battery powered, portable electronic equipments or wireless communication systems.

3.5 Operational Conveyor, OC

In a basic current conveyor shown in figure 3.11,in ideal case the voltage Vx at the inverting input x tracks the voltage V_y at the high impedence non-inveriting input y and the current Iz at the high impedance output z is equal to the input current Ix flowing in to the inverting input. The impedance seen at the input x is ideally zero. But in a practical current conveyor, the buffer

connecting terminal y to x has an output impedance $R_x \neq 0$ which is the impedance seen at x. As a result $V_x \neq V_y$ and the accuracy of the system transfer function is affected since it depends on R_x which is a low tolerance component .

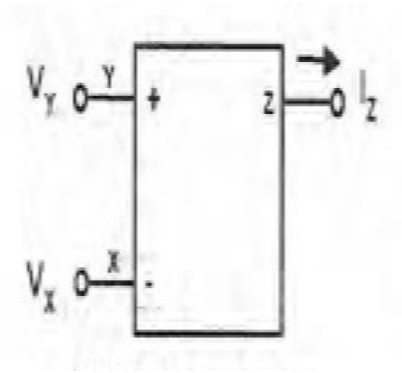


Fig **3.11** the current conveyor

Inorder to overcome this problem Gift (2001) [25] introduced a circuit referred to as operational conveyor. It consists of an operational amplifier (OA) and a current conveyor (CC) in a hybrid arrangement shown in Fig. 3.12 (Z is an external impedance and not part of the circuit). The input terminals of the current conveyor are included in the feedback loop of the operational amplifier with the effect that R_x is virtually eliminated from the system transfer function.

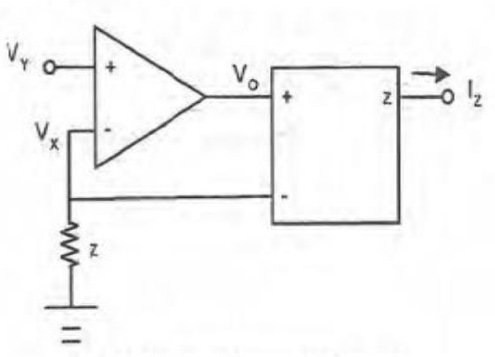


Fig. **3.12** The Operational Conveyor with impedance Z

Characteristics of the Operational Conveyor

Three of the parameters which characterize the performance of a current conveyor are the voltage transfer ratio V_x / V_y and the transfer function. Now these parameters for the OC is found that the voltage transfer ratio is found to be close to unity,

At low frequencies the transfer function of Operational Conveyor is found to be

$$\frac{I_o}{V_i}(DC) = -\frac{1}{R_1}$$

Which is independent of R_X, (refer the figure given below)

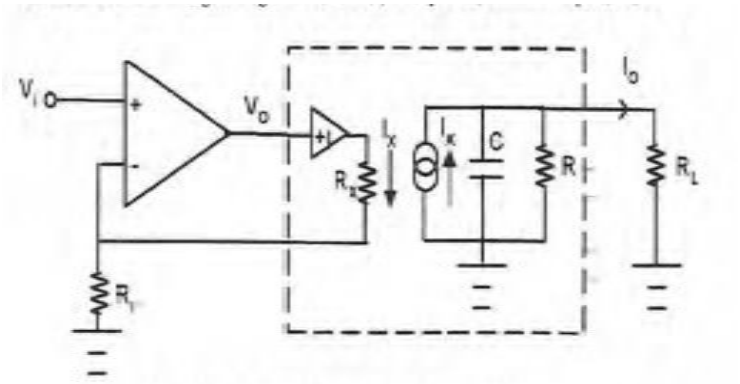


Fig **3.13** Operational Conveyor in non-inverting configuration

References

1. R. Senani, ‘A novel application of four-terminal floating nullors’. Proceedings of the IEEE, 1987, vol. 75, p. 1544-1546.

2. A. Jiraseree-amornkun, B. Chipipop and W. Surakampontorn, ‘Novel Translinear-Based Multi-Output FTFN,’ Proceeding of ISCAS2001, pages 180-183, 2001.

3. TH .Laopoulos, S .Siskos, M. Bafleur, PH. Givelin and E.Tournier ‘Design and application of an easily integrable CMOS operational floating amplifier for the mega hertz range’ Analog Integrated Circuits and Signal Processing 7, 1995, pages 103-111.

4. H.J. Huijsing and C.F. Veelenturf ‘Monolithic class AB operational mirrored amplifier’ Electronics Letter, 17, 1981, pages 119-120.

5. W. TANGSRIRAT ‘Electronically Tunable Multi-Terminal Floating Nullor and Its Applications’ Radioengineering, vol. 17, no. 4, December 2008.

6. B. GILBERT, ‘Current-mode circuits from a translinear viewpoint: A tutorial’, in Analog IC Design: The Current-Mode Approach, C. TOUMAZOU, F.J LIDGEY and D.G. HAIGH, Eds. London,U.K.: Peter Peregrinus, 1990, p.11-91.

7. S. J. Azhari and H. Fazalipoor, ‘A novel current-mode instrumentation amplifier (CMIA) topology,’ IEEE Trans. Instrum. Meas., vol. 49, no. 6, pp. 1272– 277, Dec. 2000.

8. W. Tangsrirat, S. Unhavanich, T. Dumawipata and W. Surakampontorn ‘FTFN with Variable Current Gain’ IEEE Catalogue No. 01 CH37239 0-7803-7011 - I / 01 / 2001 IEEE.

9. J. Hirunporm, S. Unhavanich, W. Tangsrirat, W. Surakampontorn ‘Composite Four-Terminal Floating Nullor with Variable Voltage and Current Gains’ ECTI-CON 2007 The 2007 ECTI International Conference

10. H. Carlin, ‘Singular network element,’ IRE Trans. Circuit Theory, vol. CT-11, pp. 67–72, Mar. 1964.

11. J. Huijsing and J. De Korte, ‘Monolithic nullor—A universal active network element,’ IEEE J. Solid-State Circuits, vol. 12, pp. 59–64, Feb. 1977.

12. E. H. Nordholt, ‘Extending op amp capabilities by using a current- source power supply,’ IEEE Trans. Circuits Syst., vol. CAS-29, pp. 411–414, June 1982.

13. M. Higagimura, ‘Realization of current-mode transfer function using four-terminal floating nullor,’ Electron. Lett., vol. 27, pp. 170–171, Jan.1991.

14. C. Toumazou, F. Lidgey, and C. Makris, ‘Extending voltage-mode op amps to current-mode performance,’ in Proc. Inst. Elect. Eng. Circuits Devices Syst., vol. 137, 1990, pp. 116–130.

15. D. Johns and K. Martin, Analog integrated circuit design. New York: Wiley, 1997, ch. 6.

16. H. Alzaher and M. Ismail ‘A CMOS Fully Balanced Four-Terminal Floating Nullor’ IEEE Transactions on Circuits and Systems—I: Fundamental theory and applications, vol. 49, no. 4, April 2002.

17. Comlinear Corp., ‘Designer’s guide for 200 series op amp,’ Application note 200-1, 4800 Wheaton Drive, Ft. Collins, CO 80525, 1984.

18. Analog Devices: ‘Linear products data book.’ Norwood MA, 1990.

19. A. Fabre, ‘Insensitive voltage mode and current mode filters from commercially available transimpedance opamps,’ Proc. IEE (G), vol. 140, pp. 319–321, 1993.

20. S.-I. Liu and Y.-S. Hwang, ‘Realization of R– L and C–D impedances using a current feedback amplifier and its applications ,’ Electronics Letters, vol. 30, no. 5, pp. 380– 381, 1994.

21. C.-M. Chang, C.-S. Hwang, and S.-H. Tu, ‘Voltage-mode notch, lowpass and bandpass filter using current-feedback amplifiers,’ Electronics Letters, vol. 30, no. 24, pp. 2022–2023, 1994.

22. M. T. Abuelma’atti and S. M. Al-shahrani, ‘New universal filter using two current feedback amplifiers,’ International Journal of Electronics, vol. 80, pp. 753–756, 1996.

23. Analog Devices: ‘Linear products data book’ Norwood MA, 1990.

24. M. Siripruchyanun, C. Chanapromma, P. Silapan, W. Jaikl ‘BiCMOS Current-Controlled Current Feedback Amplifier (CC-CFA) and Its Applications’. WSEAS Transactions on Electronics, Issue 6, Volume 5, June 2008

25. S. Gift ‘Hybrid current conveyor-operational amplifier circuit’ -International journal of electronics -2001

CHAPTER IV

OTHER ACTIVE DEVICES

4.1 Current Differencing Buffered Amplifier, CDBA

As an active building block, operational amplifier played a predominant role in the last two decades and an enormous number of publications exist in the literature on various circuit examples so that the design engineer can make choice of them. However, opamp-based circuits exhibit several drawbacks in their performance arising from the limited bandwidth and slew-rate of these active elements. Therefore, current-mode approach has been increasingly recognized as a way to overcome the opamp drawbacks and to realize high speed systems. In the recent years new current-mode active building blocks like second generation current conveyors (CCII+ and CCII−), current-feedback opamps (CFOA) received considerable attention due to their larger dynamic range and wider bandwidth [1, 2]. In addition, different types of active elements like electronically controlled current-conveyor (ECCII), differential voltage current conveyor (DVCC), differential difference current conveyor (DDCC), third generation current conveyor(CCIII), dual output operational transconductance amplifier (DO-OTA) and four terminal floating nullor (FTFN) are presented in the literature.

Current differencing buffered amplifier (CDBA) is introduced by Acar and Ozoguz to provide further possibilities in the circuit synthesis and to simplify the implementation [3,4]. The CDBA can offer such as high-slew rate, wide bandwidth and simple implementation for internally grounded input terminals [5]. Moreover CDBA is suitable for integrated circuit (IC) implementation in both bipolar and CMOS technologies [6]-[11]. Since the CDBA can be considered as a collection of current and voltage-mode unity gain cells, it has large dynamic range and quite wide bandwidth similar to its current-mode counterparts such as, current feedback operational amplifiers (CFAs) and second generation current conveyors (CCIIs).

Many applications based on CDBA were reported in the literature. Many applications of CDBA has demonstrated that the CDBA is a versatile active building block for voltage-mode and current-mode signal processing applications.

Circuit Description OF CDBA

The circuit symbol of the current differencing buffered amplifier (CDBA) is shown in Figure 4.1, where p and n are input terminals, w and z are output terminals.

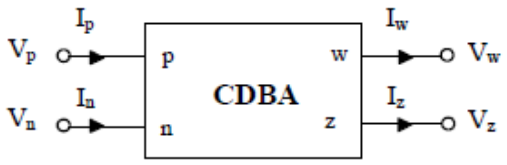


Fig 4.1 Symbol of CDBA

CDBA is characterized by the equation given below

$$\begin{bmatrix} I_z \\ V_w \\ V_p \\ V_n \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 & -1 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_z \\ i_w \\ i_p \\ i_n \end{bmatrix}$$

According to the above matrix equation and equivalent circuit shown Figure 4.1 the current through z-terminal is the difference of the currents through p-terminal and n-terminal, hence, the z-terminal is called current output; p- and n-terminals are non-inverting and inverting input terminals, respectively. Since the voltage at the w-terminal follows the voltage of z-terminal, it is called voltage output. The input terminals, through which i_p and i_n flows, are internally grounded, where ideally the input impedance of the terminals p and n are internally zero.

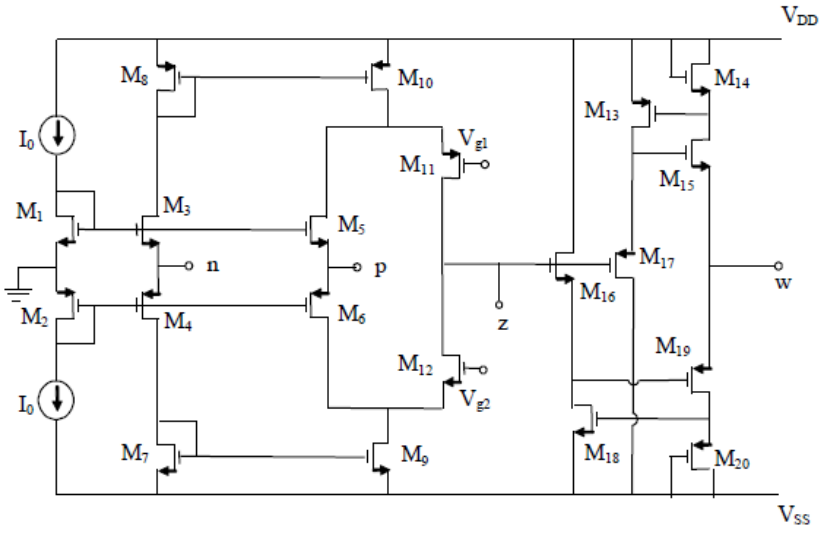


Fig 4.2 CMOS implementation of CDBA

CDBA contains the so-called CDU (Current Differencing Unit) and the voltage unity-gain buffer. Basically, CDU is a current conveyor of the MDCC type: It has two low-impedance terminals, *p* and *n*. The difference of currents I_p and I_n flows out of the *z* terminal and the corresponding voltage drop on the external impedance is copied by the buffer to the *w* output. That is why the additional impedances are necessary for implementing the feedbacks from the voltage output to the current inputs. It is inconvenient from the point of view of simplicity and low power consumption. Another drawback is the impossibility of direct electronic control of circuit parameters such as that for the OTA-based applications.

This problem is solved via two different approaches. The CC-CDBA (Current Controlled CDBA) is described in [12], DC-CDBA (Digitally Controlled CDBA) [13].

4.2 Current Controlled CDBA, CC-CDBA

CDBA offers advantage of high impedance current output as well as a buffered voltage output. The finite parasitic resistance at the two input ports of the CDBA (P and N) can be used as an advantage if made controllable. In 2003 Maheshwari and Khan proposed the current controlled CDBA[12], in which the parasitic resistances are current-controlled using mixed translinear input loops and current mirrors.

Already discussed CDBA is characterized by the following port relationship

$$V_p = V_n = 0, \qquad I_z = I_p - I_n , \qquad V_w = V_z . \qquad \text{.....(a)}$$

Here the two input terminals (P and N) offer a finite parasitic resistance [97]. These parasitic resistances can be current-controlled in a CCCDBA whose symbol and bipolar implementation are given in Figure 4.3. The circuit implementation of Figure 4.3 (b) consists of mixed translinear loops [14] (transistor 1-6) realizing two input terminals with a ground potential. The mixed loops are dc biased by Io using mirrors (transistors 7-13). The output Z-terminal that generates the current difference of P- and N-terminals is realized using transistors (14-21). The buffered output (W) is realized using transistors (22-25). The P- and N- terminal resistance can be obtained by the following relationship [15].

$$R_{p,n} = V_T / 2I_o \qquad \text{.....(b)}$$

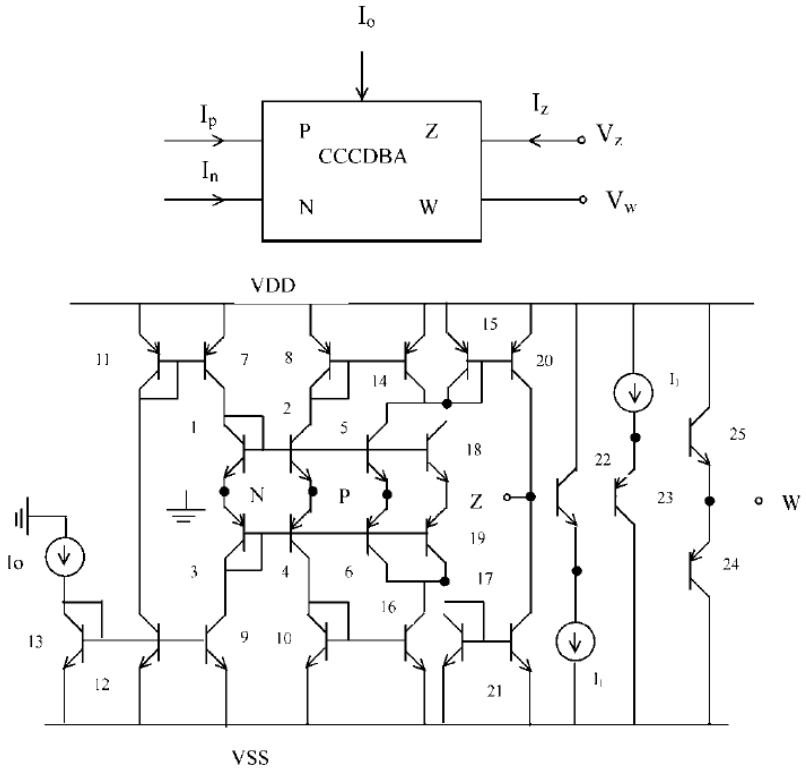


Fig 4.3. CC-CDBA (a) Symbol (b) Implementation

From Eq.(b) it is clear that the P- and N- resistances can be varied by external bias current (I_o) of the CCCDBAs. By replacing the current sources used in buffer stage by transistorized circuitry the proposed CCCDBA can be IC implemented.

4.3 Digitally Controlled CDBA, DC-CDBA

In analog signal processing area, there are many engineering applications which require programmable characteristics such as, adaptive filters, music synthesizers, formant speech synthesizers and tracking filters. Generally, analog or digital tuning can be employed to control the circuit parameters. However, in low-voltage applications, there is a limitation on the allowable range of the analog tuning voltage. Hence, in these applications, the digital control is more attractive [16]. Therefore, digitally programmable tuning characteristics have been an ongoing research topic for a number of years. In 2008 Prasertsom, Tangsrirat, Surakampontorn proposed a low voltage digitally controlled CDBA, DC-CDBA which is realized by interconnecting a current differencing circuit, a current division network (CDN), and a unity-gain

voltage amplifier[13]. The novel CDN circuit is also proposed in order to provide the digital control of the current gain of the DC-CDBA.

Circuit Descriptions

The proposed DC-CDBA is a versatile analog building block, described symbolically as shown in Fig. 4.4 (a) and mathematically by the following matrix equation.

$$\begin{bmatrix} I_z \\ V_w \\ V_p \\ V_n \end{bmatrix} = \begin{bmatrix} 0 & 0 & \alpha & -\alpha \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_z \\ i_w \\ i_p \\ i_n \end{bmatrix} \quad \ldots\ldots\ldots\ldots \quad (1)$$

Where α is the current gain that is controlled digitally. According to eq.(1), this device consists of three stages as shown in Fig. 4.4(b). The input stage is a current differencing circuit to provide the difference of the input currents (i_p and i_n) through the terminals *p* and *n* into the x-terminal current (i_x). The second stage is a CDN, which is based on the linear current division principle. At this stage, the current *ix* is copied to the z-terminal and is digitally controlled by the current gain parameter α. The last stage is simply a voltage buffer, since the voltage at the w-terminal follows the voltage of the z-terminal.

4.3.1 Current Differencing Circuit

Fig**.** 4.5 shows the proposed CMOS current differencing circuit, which is composed of two unity-gain current amplifiers (M1A-M5A) and (M1B-M5B) . Due to the current mirror M7-M8, the signal current flowing out of the terminal x (i_x) can be expressed as:

$$i_x = i_p - i_n \quad \ldots\ldots\ldots (2)$$

In this case, the input resistances of the terminals *p* and *n* can also be written as [11],

$$r_p = \left(\frac{1}{g_{m1A}}\right)\left(\frac{1}{1+F_p}\right) \quad \text{and} \quad r_n = \left(\frac{1}{g_{m1B}}\right)\left(\frac{1}{1+F_n}\right) \quad \ldots\ldots\ldots (3)$$

where g_{miA} and g_{miB} represent respectively the transconductance of the transistors M_{iA} and M_{iB} (i = 1, 2, 3, 4,5)

$$F_p = \left(\frac{g_{m2A}g_{m4A}r_{oB}}{g_{m2A}+g_{m3A}}\right) \quad \text{and} \quad F_n = \left(\frac{g_{m2B}g_{m4B}r_{oB}}{g_{m2B}+g_{m3B}}\right)$$

Therefore, the input resistances r_p and r_n are very low due to the factors from the feedback $(1+F_p)$ and $(1+F_n)$, respectively.

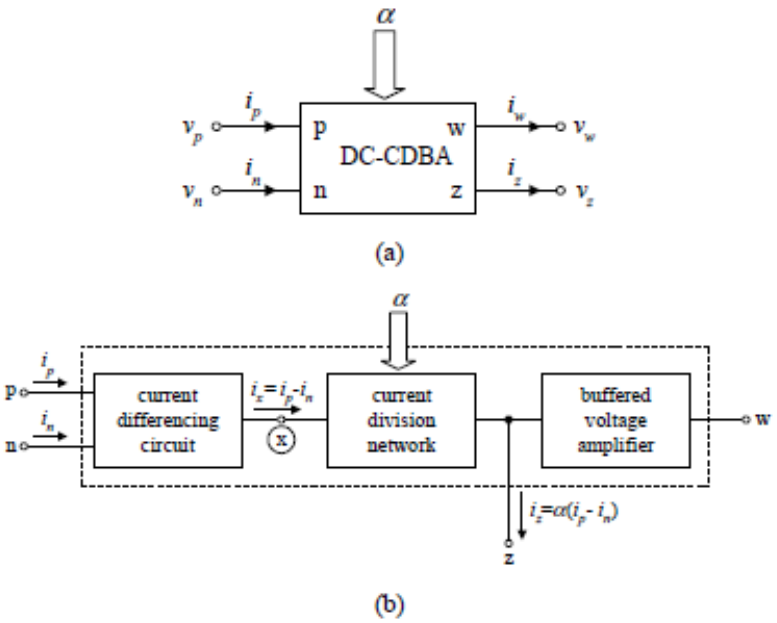


Fig 4.4. (a) Circuit Symbol (b) Block diagram of DC-CDBA

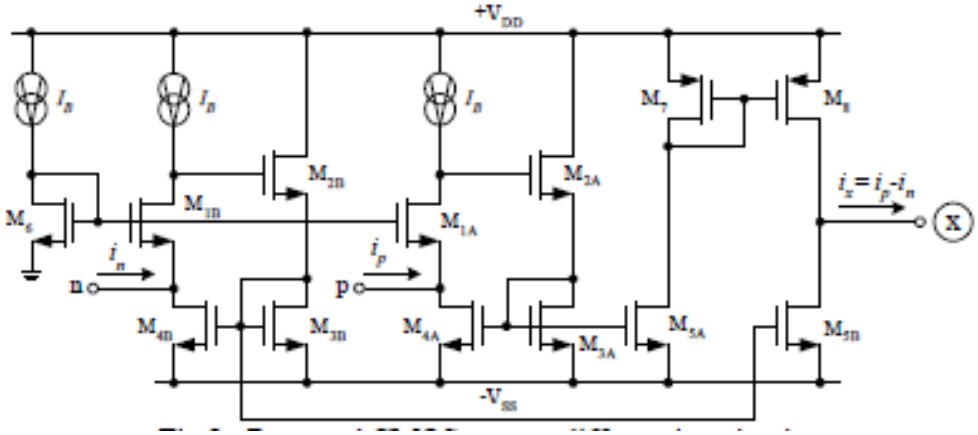


Fig 4.5 CMOS of Current differencing circuit

4.3.2 Current Division Network

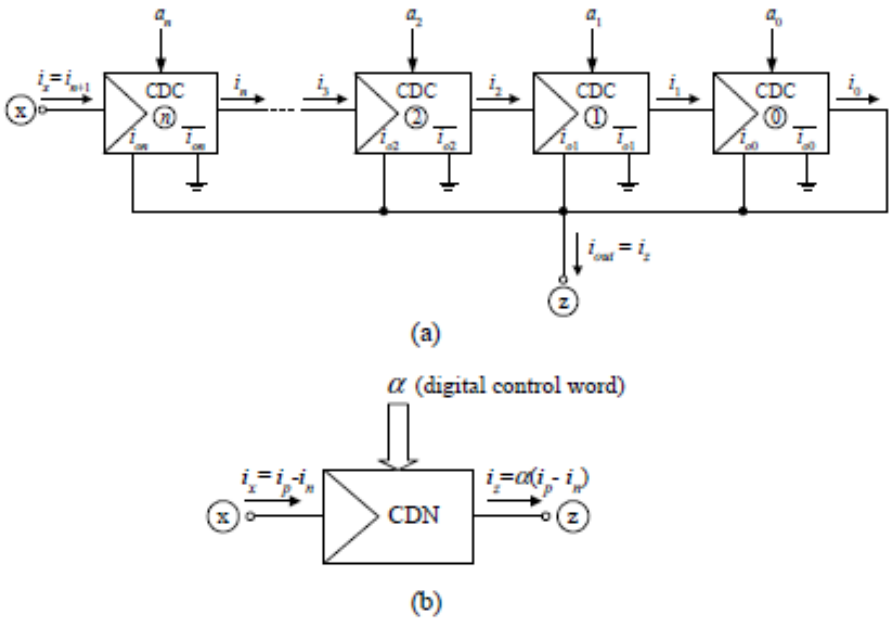


Fig 4.6 CDN (a) Circuit diagram (b) Circuit Symbol

The current division network (CDN), consisting of *n* CDCs, is shown in Fig.4(a). As can be seen, the output current i_i of the CDC_i (i = 0, 1, 2, …, n) is used as an input current of the next stage and the current i_0 is added to i_{oi}. Therefore, the output current (i_{out}) of the proposed CDN can be described by

$$i_{out} = \left(\frac{1}{2^{n+1}}\right)\left[1 + \sum_{i=0}^{n} a_i 2^i\right] i_x$$

$$\propto = \frac{i_z}{i_p - i_n} = \frac{i_{out}}{i_x} = \left(\frac{1}{2^{n+1}}\right)\left[1 + \sum_{i=0}^{n} a_i 2^i\right] \quad \text{.....(4)}$$

From eq.(4), the current gain (α) of the proposed CDN can be controlled digitally, where α is less than, or equal to, unity.

4.4 Current Differencing Transconductance Amplifier, CDTA

A new active element with two current inputs and two kinds of current output, namely the Current- Differencing Transconductance Amplifier (CDTA) was Proposed by Biolek [17] and the element is a synthesis of the known CDBA (Current-Differencing Buffered Amplifier) and OTA

(Operational Transconductance Amplifier) elements to facilitate the realization of current-mode analog filters.

Despcription

A simple model of ideal CDTA element is in Fig. 4.7. Analogously to the CDBA, it has difference current inputs *p* and *n*. The difference of these currents flows from terminal *z* into an outside load. The voltage across the *z* terminal is transferred by a transconductance *g* to a current that is taken out as a current pair to the *x* terminals. This last element part is the familiar transconductance operational amplifier (OTA). In general, the transconductance is controllable electronically through an auxiliary port that is not shown in Fig. 4.7.

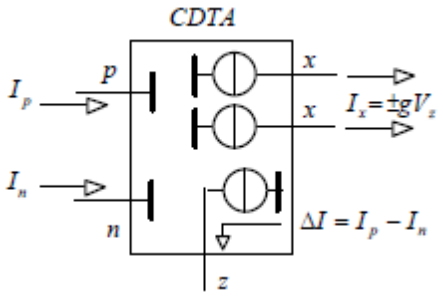


Fig 4.7 Behavioral model of CDTA

The pair of output currents from the *x* terminals, shown in Fig. 4.7, may have three combinations of directions:

1. Both currents can flow out.

2. The currents have different directions.

3. Both currents flow inside the CDTA element.

Accordingly we can mark them as CDTA++, CDTA+-, and CDTA-- elements. It is suitable to mark the current directions in the circuit symbol by the signs + (outside) and – (inside) as shown in Fig. 4.8(a)

The proposed symbol of CDTA is in Fig. 4.8 (a). Also in Fig. 4.8 (b) is given a possible implementation of CDTA using the familiar CCII+ and OTA components.

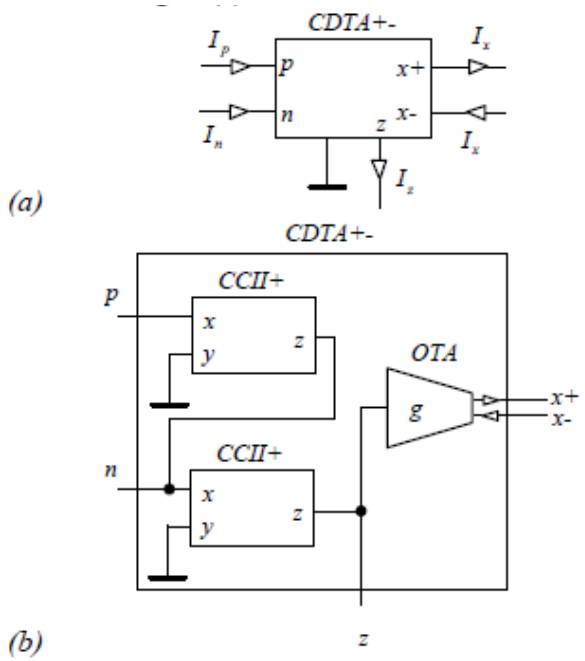


Figure 4.8(a) Symbol of the CDTA element, (b) its implementation by current conveyors and by OTA with double current output.

Marking the voltages of *p*, *n*, *x*, and *z* terminals in Fig. 4.8 (a) with symbols *Vp*, *Vn*, *Vx*, and *Vz*, then for the CDTA+- element the following equations are true:

$$\begin{bmatrix} I_z \\ I_{x+} \\ I_{x-} \\ V_P \\ V_n \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 1 & -1 \\ g & 0 & 0 & 0 & 0 \\ -g & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_z \\ V_{x+} \\ V_{x-} \\ I_P \\ I_n \end{bmatrix}$$

The CDTA element proposed by Biolek enables an easy implementation of multiple-input current integrators. That is why it seems to be a promising building block of current-mode filters.

Compared with CDBA, the CDTA element is less universal in the sense that – to avoid all additional current-to-voltage-to-current conversions- it does not enable setting the summing coefficients simply by means of outside *R* and *C* components. The voltage mode prototypes provide more design freedom.

CMOS realization of the CDTA element is shown in Fig.4.10 [18]. The CDTA is a universal active building block for implementing many signal processing functions including sinusoidal oscillators. Recently, a single-CDTA-based SRCO circuit has been reported by Prasad et al. [19]. Which enables independent control of the frequency of oscillation (FO) and the condition of oscillation (CO).

The modified CDTA was proposed by Biolek, Keskin, Biolkova [20] its schematic symbol is shown in 4.9. It has a pair of low-impedance current inputs p and n, and an auxiliary terminal z, whose outgoing current is the difference of input currents. In addition to the CDTA, a copy of the z-terminal current is also available at the zc high-impedance terminal. Therefore this modified CDTA element is called ZC-CDTA (Z Copy CDTA).

4.5 Z Copy CDTA , ZC-CDTA

Similar to the CDTA, this element provides a pair of x-terminals whose currents are equal in magnitude, but flow in opposite directions, and the product of transconductance (gm) and voltage at the z-terminal determines their magnitudes. The circuit equations of the ZC-CDTA are as follows

$$\begin{bmatrix} V_p \\ V_n \\ I_z \\ I_{zc} \\ I_{x+} \\ I_{x-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & g_m & 0 & 0 & 0 \\ 0 & 0 & -g_m & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ V_z \\ V_{zc} \\ V_{x+} \\ V_{x-} \end{bmatrix}$$

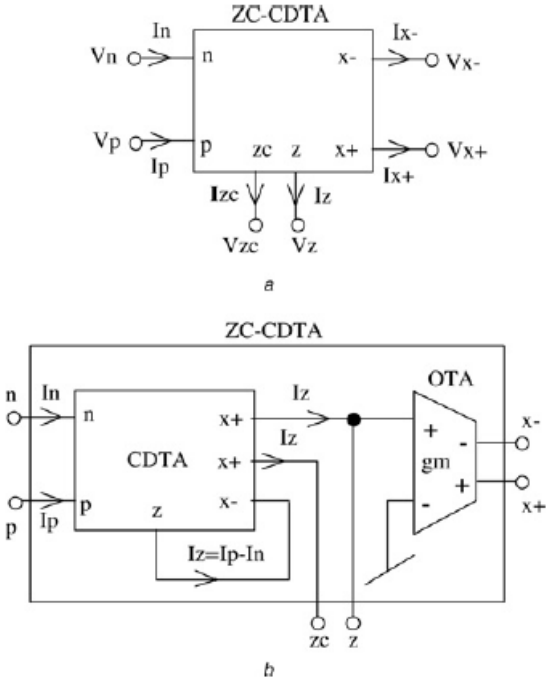


Fig 4.9 (a) Symbol of ZC-CDTA (b) ZC-CDTA implementation based on CDTA and OTA

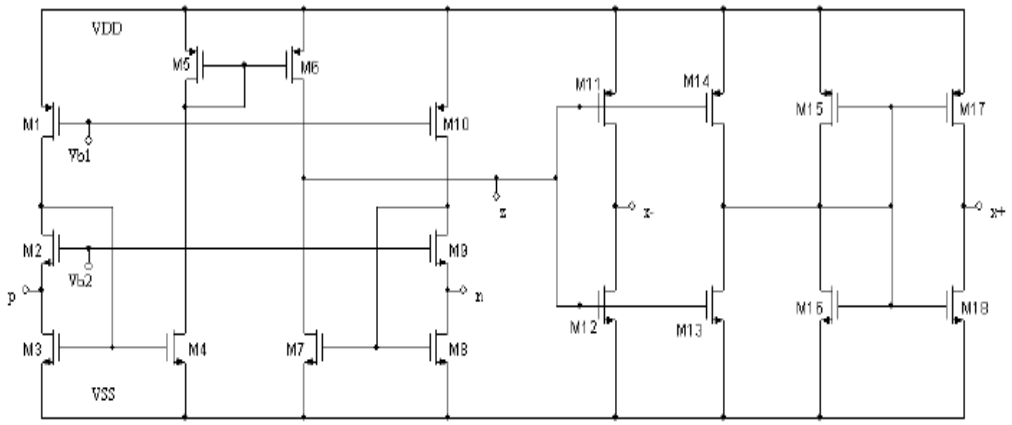


Fig 4.10 CMOS realization of CDTA

4.6 Modified CDTA, MCDTA

Another modification of CDTA was attempted by *LI in 2011* [21] by means of adding a transconductance amplifier and several current mirrors in the traditional CDTA. Number of *x* port and *z* port for the CDTA can be extended and a modified CDTA (MCDTA) was realized. Its circuit representation and equivalent circuit are shown in Fig. 4.11. The terminal relation of MCDTA can be characterized by the following set of equations:

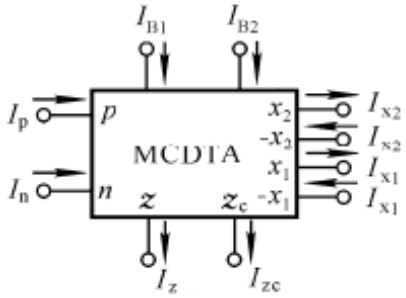
$$V_p = V_n = 0 \qquad I_{zc} = I_z = I_p - I_n$$

$$I_{x1} = g_{m1} V_z \,, \qquad I_{x2} = g_{m2}\, V_z$$

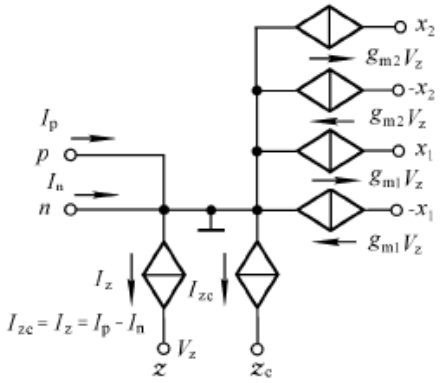
Here, g_{m1} and g_{m2} represent transconductance gains of two different balanced operational transconductance amplifiers, respectively. For a MCDTA implemented with bipolar technology, g_{m1} and g_{m2} can be expressed as follows:

$$g_{m1} = \frac{I_{B1}}{2V_T} \,, g_{m2} = \frac{I_{B2}}{2V_T}$$

Here, I_{B1} and I_{B2} are bias currents of MCDTA. V_T is the thermal voltage.



(a)



(b)

Fig 4.11 (a) Symbol of MCDTA ,(b) Equivalent circuit of MCDTA

4.7 Current Controlled CDTA

Current differencing transconductance amplifier (CDTA), has provided new possibilities in the current-mode circuit. The CDTA seems to be a versatile component in the realization of a class of analog signal processing circuit; especially analog frequency filters. It is really current-mode element whose input and output signals are currents. In addition, output current of CDTA can be electronically adjusted. Besides, the modified version of CDTA wherein the intrinsic resistances at two current input ports can be electronically controlled has been proposed by Siripruchyanun, Jaikla, [22]. This CDTA is called current controlled current differencing transconductance amplifier (CCCDTA).

The schematic symbol and the ideal behavioral model of the CCCDTA are shown in Fig**. 4.12**(a) and (b). It has finite input resistances: R_p and R_n at the p and n input ports, respectively. These

intrinsic resistances are equal and can be controlled by the bias current I_{B1}. The difference of the i_p and i_n input currents flows from port z. The voltage V_z on z terminal is transferred into current using transconductance g_m, which flows into output terminal x. The g_m is tuned by I_{B2}.

In general, CCCDTA can contain an arbitrary number of x terminals, providing currents I_x of both directions.

The characteristics of the ideal CCCDTA are represented by the following hybrid matrix

$$\begin{bmatrix} V_p \\ V_n \\ I_z \\ I_x \end{bmatrix} = \begin{bmatrix} R_p & 0 & 0 & 0 \\ 0 & R_n & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & \pm g_m \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ V_x \\ V_z \end{bmatrix}$$

If the CCCDTA is realized using CMOS technology [23]. , R_p, R_n and g_m can be respectively written as

$$R_p = R_n = \sqrt{\frac{1}{k_R I_{B1}}} \; ; \quad k_R = 8\mu_n C_{ox} \left(\frac{W}{L}\right)_{8-11} = 8\mu_n C_{ox} \left(\frac{W}{L}\right)_{12-15}$$

And

$$g_m = \sqrt{k_g I_{B2}} \; ; \; k_g = \mu_n C_{ox} \left(\frac{W}{L}\right)_{29,30}$$

Here k is the physical transconductance parameter of the MOS transistor. The CMOS implementation of the CCCDTA is shown in Fig. 4.13.

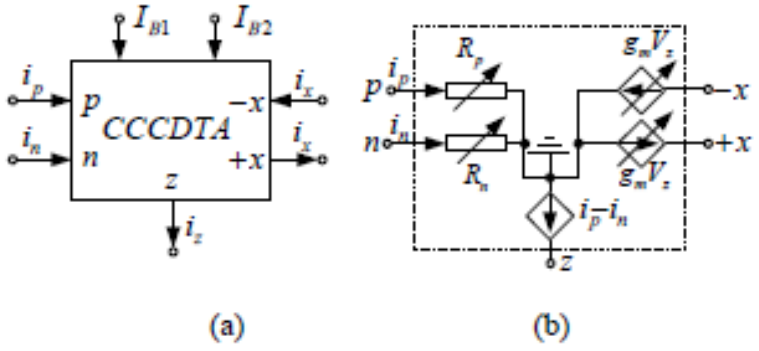


Fig 4.12. (a) symbol (b) Equivalent Circuit

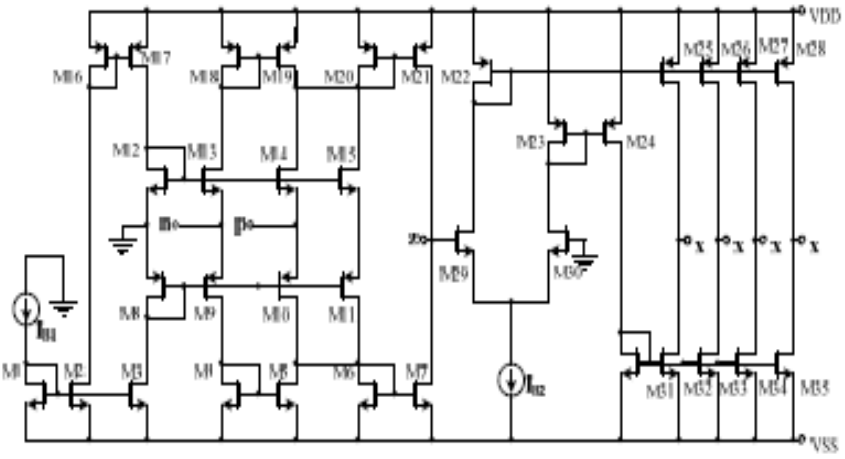


Fig 4.13 Schematic of the CMOS CCCDTA.

4.8 CurrentConveyor Transconductance Amplifier , CCTA

The CCTA (Current Conveyor Transconductance Amplifier) is the newly designed type of analog block proposed by Prokop and Musil in 2005**,** [24] that was inspired by transimpedance amplifier (current feedback amplifier whi ch is built from CCII conveyor followed by voltage buffer). CCTA is designed for usage mostly in current mode circuits but it is also good choice in case of hybrid (voltage-current) circuits. Behavioral model of the CCTA is shown in Fig. 4.14. From its behavior the possible internal structure can be visible (Fig. 4.15). The CCTA consists from two basic blocks. The input is represented by the current conveyor CCIII that is followed by double output transconductance opamp (OTA).

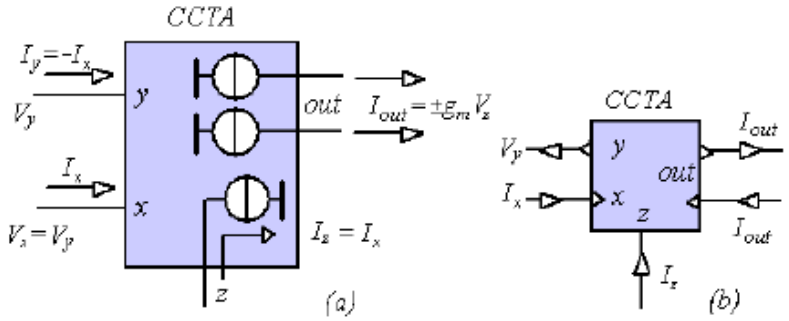


Figure 4.14: (a) Behavioral model of CCTA, (b) example of schematic symbol of CCTA

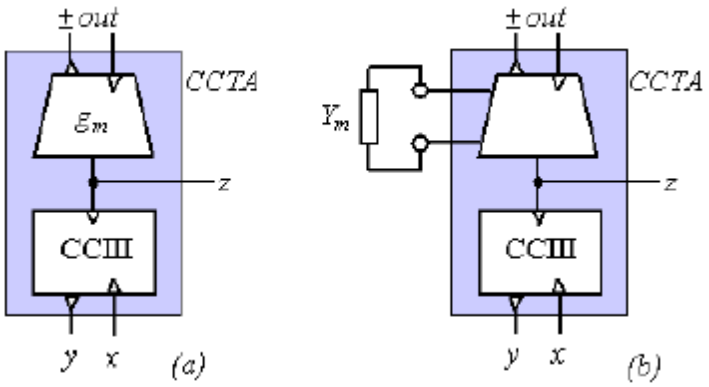


Figure 4.15: (a) CCTA element as a connection of CCIII and OTA element

(b) CCTA with possibility to choose "transconductance" by an outside two-pole

The input behavior is mostly given by properties of the CCIII conveyor that is described below. Conveyor output current flows out of the CCTA terminal "z" into an outside load. The voltage across the z-terminal is converted through a transconductance gm into a two output currents with opposite polarity. The transconductance can be either fixed or given by external component or controlled electronically from an auxiliary terminal as well. The CCTA may be reasonably useful, for example, in current sensing applications. In fact, if a current, at a generic point into a network, has to be sensed, the current "probe" should be able to make flow a current with very low series impedance while the sensed current can be further processed (amplified, filtered etc.).

If the terminal "z" is not connected (high impedance) the CCTA with terminal "y" grounded can be also used as a COA (current operational amplifier). [25].

The CCTA is brought in as the new convenient element for current mode signal processing, which should be very convenient for several applications, e.g. sensor output signals processing. CCTA is supposed for usage mostly in current mode circuits but it is also good choice in case of voltage mode and/or hybrid (voltage-current) circuits (e.g. V/I converters). This modern active device is a newly designed type of analog block that was inspired by transimpedance amplifier (current feedback amplifier which is basically built from CCII conveyor followed by voltage buffer), but CCTA expects even much more versatility in circuit applications.

4.9 Current Controlled CCTA, CC-CCTA

One drawback of CCTA is that it can not control the parasitic resistance at input port so when it is used in some circuits, it must unavoidably require some external passive components, especially the resistors. This makes it not appropriate for IC implementation due to occupying more chip area. In addition, the CCTA has a third-generation current conveyor (CCIII) as input stage which has flexibility for applications less than a second- generation current conveyor (CCII). A modified-version CCTA, which is named current controlled current conveyor transconductance amplifier (CCCCTA) was proposed by Siripruchyanun and Jaikla [26], where the parasitic resistance at current input port can be controlled by an input bias current, and then it does not need a resistor in practical applications.

Basic concepts of CCCCTA

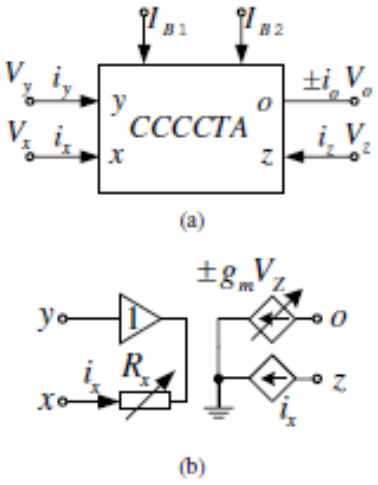


Fig 4.16 The CCCCTA (a) symbol (b) equivalent circuit

CCCCTA properties are similar to the conventional CCTA, except that the CCCCTA has finite input resistance *Rx* at the *x* input terminal. This parasitic resistance can be controlled by the bias current I_{B1} as shown in the following equation

$$\begin{bmatrix} I_y \\ V_x \\ I_z \\ I_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ R_x & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & \pm g_m & 0 \end{bmatrix} \begin{bmatrix} I_y \\ V_y \\ V_z \\ V_o \end{bmatrix}$$

Where

$$R_x = \frac{V_T}{2I_m} \ , g_m = \frac{I_{B2}}{2V_T}$$

where g_m is the transconductance gain of the CCCCTA and V_T is the thermal voltage. The symbol and the equivalent circuit of the CCCCTA are illustrated in Fig. 4.16(a) and (b), respectively

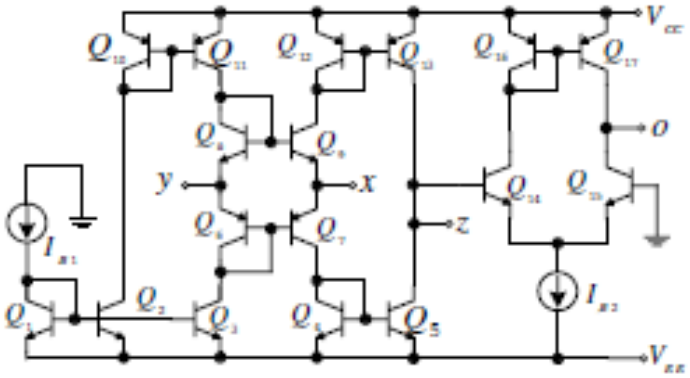


Fig 4.17 Realisation of CCCCTA using Bipolar technology

4.10 Modified -CCCCTA

CCCCTA which is relatively newly proposed current mode active building block [26], can be operated in both current and voltage modes, providing flexibility. In addition, it can offer several advantages such as high slew rate, high speed, wider bandwidth and simpler implementation. Moreover, in the CCCCTA one can control the parasitic resistance at X (R_X) port by input bias current. A modified CCCCCTA was proposed by Pandey, Bazaz, and Manocha [27] with the various advantages such as output current gain controllability, resistorlessness, and compactness in chip area added to the original unit.

The MO-CCCCTA properties can be described in the following matrix equation

$$\begin{bmatrix} I_y \\ V_x \\ I_{z\pm} \\ I_{o\pm} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ R_x & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & \pm g_m & 0 \end{bmatrix} \begin{bmatrix} I_x \\ V_y \\ V_z \\ V_o \end{bmatrix}$$

The MO-CCCCTA has a finite input resistance R_X at the X input terminal and an additional transconductance g_m amplifier in the output side. The parasitic resistance R_X and the

transconductance g_m can be controlled by bias currents I_{b1} and I_{b2}, respectively. A BJT-based MO-CCCCTA [27] is illustrated, and the intrinsic resistance (R_X) and transconductance (g_m) are expressed as

$$R_x = \frac{V_T}{2I_{b1}} \ , g_m = \frac{I_{b2}}{2V_T}$$

where I_{bi} (i = 1, 2) and V_T are the bias currents and the thermal voltage, respectively.MO-CCCCTA has been employed owing to the various advantages such as output current gain controllability, resistorlessness, and compactness in chip area.

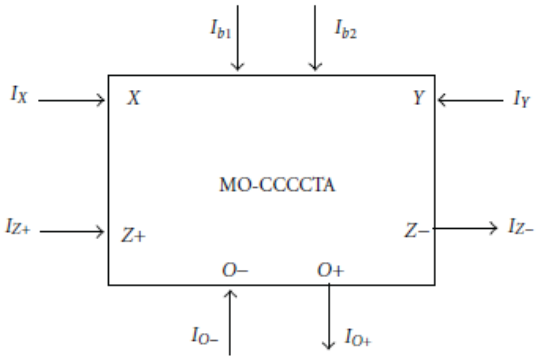


Fig 4.18. Functional symbol of MO-CCCCTA

CMOS implementation of the active block is shown in figure 4.19**,**

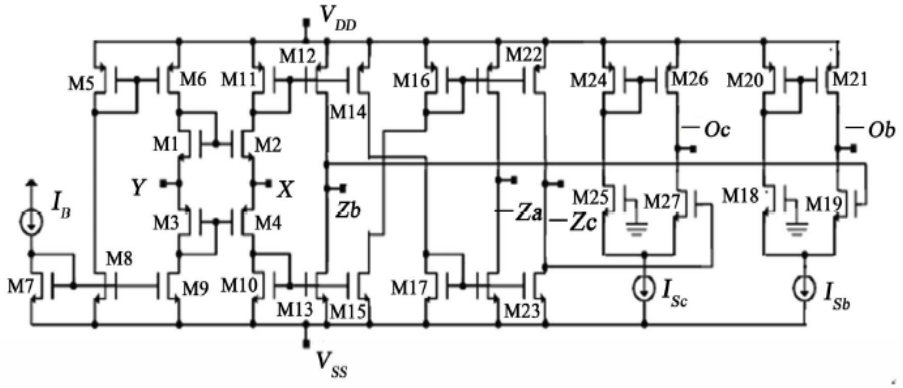


Fig 4.19. CMOS implementation of MO-CCCCTA

4.11 Differential Voltage CCTA, DVCCTA

It is well known that DVCC has some advantages, specially for applications demanding differential and floating inputs, over CCII or CCCII owing to two high input impedance terminals for DVCC compared to one high input impedance terminal for CCII or CCCII.

However, DVCC does not have a powerful inbuilt tuning property in contrast to CCCII. Recently proposed active building block namely differential voltage current conveyor transconductance amplifier (DVCCTA) [28] has DVCC as input block and is followed by TA. The DVCCTA has all the good properties of CCTA or CCCCTA including the possibility of inbuilt tuning of the parameters of the signal processing circuits to be implemented and also all the versatile and special properties of DVCC such as easy implementation of differential and floating input circuits[29-31]. However, the same may be implemented using separate DVCC and OTA analog building blocks, but it will be more convenient and useful, if DVCCTA is implemented in monolithic chip which will result in compact implementation of signal processing circuits and systems.

Circuit Description

The DVCCTA is based on DVCC [28] and consists of differential amplifier as input, current mirrors and transconductance amplifier. The port relationships of the proposed DVCCTA as shown in Fig. 4.20 can be characterized by the following matrix:

$$\begin{bmatrix} I_{y1} \\ I_{y2} \\ V_x \\ I_{z+} \\ I_{z-} \\ I_{o-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & -g_m & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{y1} \\ V_{y2} \\ I_x \\ V_{z+} \\ V_{z-} \\ V_{o-} \end{bmatrix}$$

where g_m is transconductance of the DVCCTA

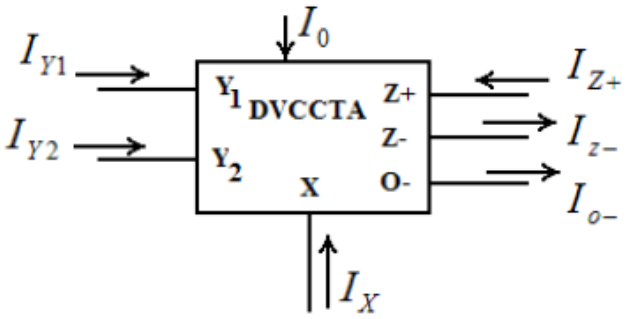


Fig. 4.20 Circuit symbol of DVCCTA

depicted in Fig. 4.21 the value of gm is given as $\sqrt{2\mu C_{ox}\,(W/L)I_{ox}}$ which can be adjusted by bias current I_0. The TSMC 0.25_m CMOS [32] process model parameters and supply voltages of V_{DD} = -V_{SS} = 1.25V and V_{BB}=-0.8V are used. The aspect ratio of various transistors is given below.

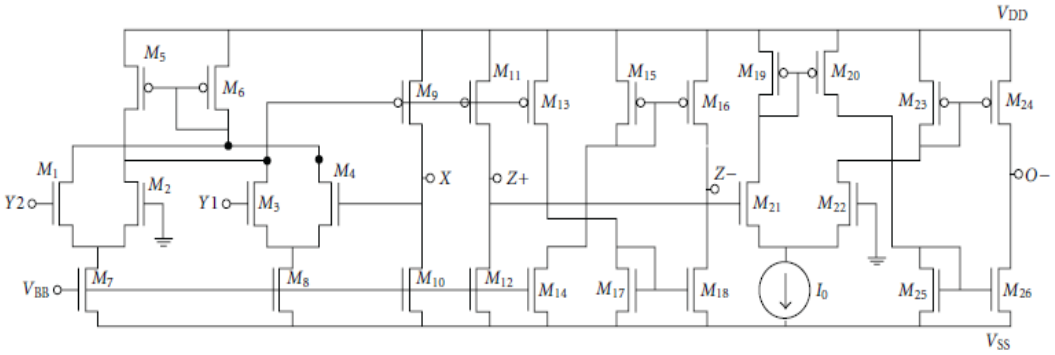


Fig. 4.21 CMOS model of VDCCTA

Aspect ratio of various transistors

Transistor	Aspect ratio (W(μm)/L(μm))
M_1–M_4	10/0.5
M_5, M_6	5/0.5
M_7, M_8	27.25/0.5
M_9, M_{11}, M_{13}, M_{15}, M_{16}	8.5/0.5
M_{10}, M_{12}, M_{14}, M_{17}, M_{18}	44/0.5
M_{19}, M_{20}, M_{23}–M_{26}	5/0.5
M_{21}, M_{22}	27/0.5

4.12 Differential Difference CCTA , DDCCTA

The DDCCTA element is based on the use of the DDCC as an input stage and the OTA as an output stage. The DDCCTA can easily be implemented from a DVCCTA by adding the Y3 terminal as shown in Fig. 4.221, the port characteristics of the DDCCTA can be described by the following expressions:

$i_{Y1} = i_{Y2} = i_{Y3} = 0$, $v_X = v_{Y1} - v_{Y2} + v_{Y3}$,

$i_Z = i_X$, $i_O = g_m v_Z$

where g_m is the transconductance parameter of the DDCCTA.

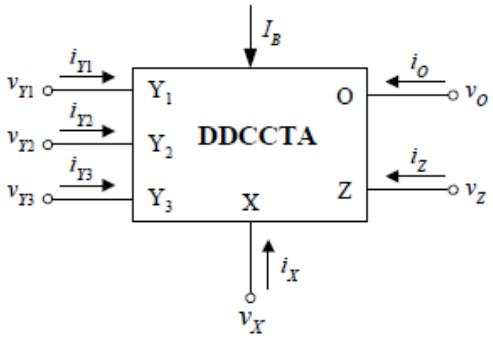


Fig. 4.22 Circuit symbol of DDCCTA

The internal structure of the DDCCTA in CMOS technology is shown in Fig. 4.23. The scheme is based on the internal circuit of the DDCC [33], which is followed by a TA [34]. In this case, the transconductance gain (g_m) of the DDCCTA can be given by:

$$g_m = \sqrt{\mu C_{ox} \frac{W}{L} I_B}$$

where I_B is an external DC bias current, μ is the effective channel mobility, C_{ox} is the gate-oxide capacitance per unit area, W and L are channel width and length, respectively. It should be noted that the g_m-value of the DDCCTA can be adjustable electronically by I_B.[35].

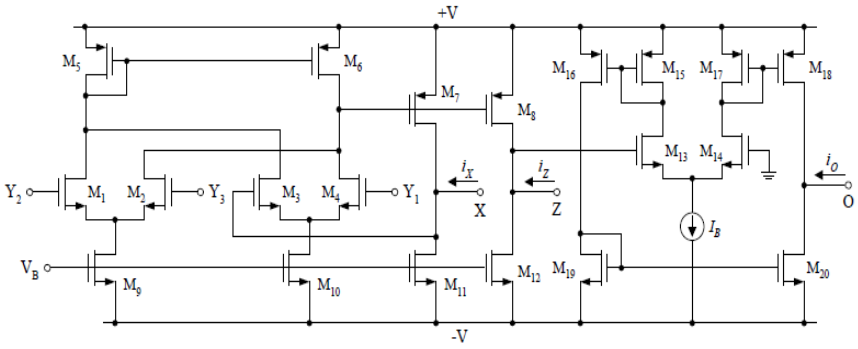


Fig. 4.23 CMOS internal structure of DDCCTA

4.13 Voltage Differencing Transconductance Amplifier, VDTA

VDTA, can be compared with CDTA, the previously introduced active element. In CDTA, differential input current (I_p, I_n) flows over the Z terminal. The voltage drop at the terminal Z is transferred to current at the terminal X by a transconductance gain. In VDTA, differential input voltage (V_{VP} ,V_{VN}) is transferred to current at the terminal Z by first transconductance gain and the voltage drop at the terminal Z is transferred to current at the terminals X+ and X- (negative of X+) by second transconductance gain. Both transconductance are electronically controllable by external bias currents. Compared to other active blocks discussed so far, the advantageous feature of VDTA is that this new element exhibits two different values of transconductances so that several applications such as biquad filters, oscillator, inductance and FDNR (frequency dependent negative resistor) simulator can be realized with a single active block employing one or two capacitors. Another important feature, this block can be used easily at transconductance mode applications owing to input terminals is voltage and output terminals is current.

Circuit description

The circuit symbol of the proposed active element, VDTA, is shown in Fig. 4.24, where V_P and V_N are input terminals and Z, X+ and X- are output terminals. All terminals exhibit high impedance values. Using standard notation, the terminals relationship of an ideal VDTA can be characterized by:

$$\begin{bmatrix} I_z \\ I_{x-} \\ I_{x-} \end{bmatrix} = \begin{bmatrix} g_{m1} & -g_{m1} & 0 \\ 0 & 0 & g_{m2} \\ 0 & 0 & -g_{m2} \end{bmatrix} \begin{bmatrix} V_{VP} \\ V_{VN} \\ V_Z \end{bmatrix}$$

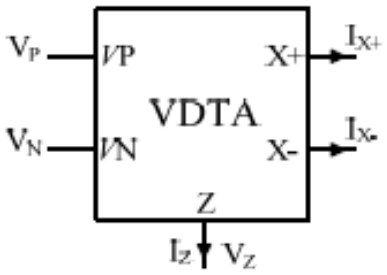


Fig. 4.24. The circuit symbol of VDTA

Consequently, the above describing-equations, the input stage and output stage can be simply implemented by floating current sources. According to input terminals, an output current at Z terminal is generated. The intermediate voltage of Z terminal is converted to output currents. The new CMOS realization of the VDTA is shown in Fig. 4.25.

The introduced circuit employs two Arbel-Goldminz transconductances [36]. Input and output transconductance parameters of VDTA element in the circuit are determined by the transconductance of outputs transistors. It can be approximated as

$$g_{m1} = (g_3 + g_4)/2 \quad , g_{m2} = (g_5 + g_8)/2 \qquad \text{or } g_{m2} = (g_6 + g_7)/2$$

where g_i is the transconductance value of *i*th transistor defined by

$$g_i = \sqrt{I_{Bi}\mu_i C_{ox}\left[\frac{W}{L}\right]_i} \ ,$$

μ_i is (i = n, p) the mobility of the carrier for NMOS (n) and PMOS (p) transistors, C_{OX} is the gate-oxide capacitance per unit area, W is the effective channel width, L is the effective channel length and I_{Bi} is bias current of *i*th transistor.[37].

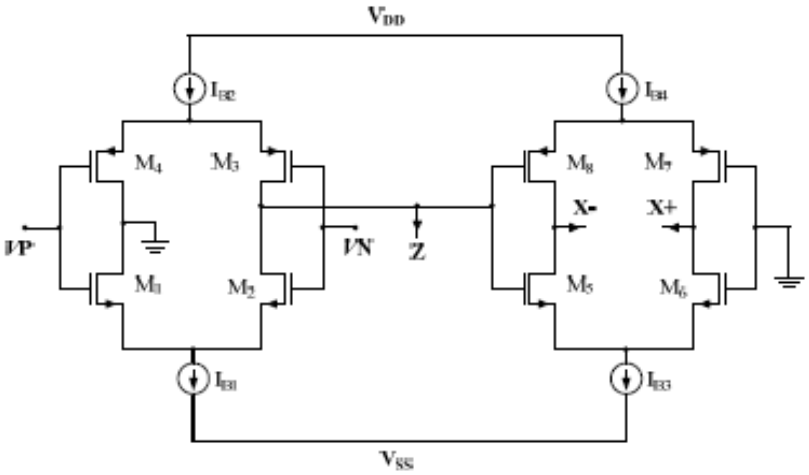


Fig . 4.25 CMOS implementation of VDTA

4.14 Current Follower Transconductance Amplifier, CFTA

This new active element was introduced by Herencsar, Koton, Vrba, and Lattenberg in 2008 [38]. The element is a combination of the Current Follower (CF) and the Balanced Output Transconductance Amplifier (BOTA). The ideal behavioural model of the CFTA element is shown in Fig. 4.26(a). The element is a combination of the Current Follower (CF), which is the input part of the designed element, and the Balanced Output Transconductance Amplifier (BOTA) [39-40], which forms the output part of the element. The schematic symbol of the CFTA element is shown in Fig. 4.26(b)

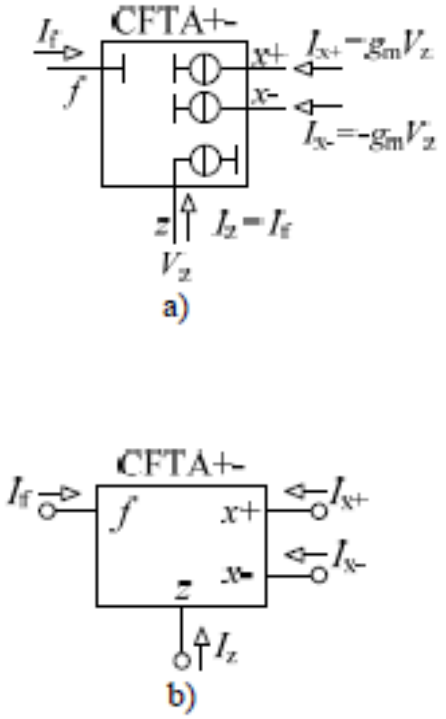


Fig 4.26 (a) Behavioral model of CFTA+ element (b) Schematic symbol of CFTA+

The element has been defined in compliance with network convention i.e. all currents are flowing into the circuit. The element has one low impedance current input *f*. Current from the terminal *f* is transferred by the Current Follower to auxiliary terminal *z*. The voltage V_z on this terminal is transformed into current using the transconductance *g*m, which flows into output terminals *x*+ and *x*-.

Relations between the individual terminals of the CFTA+- element can be described in matrix form as follows:

$$\begin{bmatrix} I_z \\ I_{x+} \\ I_{x-} \\ V_f \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 1 \\ g_m & 0 & 0 & 0 \\ -g_m & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_z \\ V_{x+} \\ V_{x-} \\ I_f \end{bmatrix}$$

4.15 Z-Copy CFTA, (ZC-CFTA)

The active element CFTA is a simplified variant of the CDTA (Current Differencing Transconductance Amplifier) element [17], [41]. In CDTAs, mostly one of the input terminals p or n is not used may cause some noise injection into the monolithic circuit. Moreover, the current differencing property at an input stage can be achieved by the current feedback connection via the

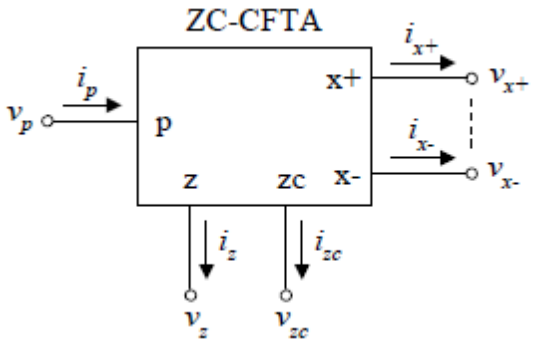
±x terminals. This implies that the input terminals p or n do not necessarily require for some applications.

In order to alleviate the mentioned problems, the simplified version of the CDTA so-called Z-copy current follower transconductance amplifier (ZC-CFTA) was firstly suggested in [20]. The ZC-CFTA is slightly modified from the conventional CDTA by replacing the current differencing unit with a current follower and complementing the circuit with a simple current mirror for copying the z-terminal current. Thus, the ZC-CFTA element can be thought of as a combination of the current follower, the current mirror and the multi-output operational transconductance amplifier. As a consequence, a number of applications based on ZC-CFTAs can be extended. The symbolic notation and equivalent of the ZCCFTA are shown in Fig. 4.27. The ZC-CFTA element consists of low-impedance input p, high-impedance outputs z, zc, x and x+. The input current from the terminal p (i_p) is respectively transferred to the terminal z (i_z) and auxiliary terminal zc (i_{zc}) by a current follower and a current mirror. The voltage drop at the terminal z (v_z) is transformed into output currents via a multi-output transconductance stage with a transconductance gain (g_m). Using standard notation, the port relations of the ZC-CFTA can be defined by the following matrix equation [42].

$$\begin{bmatrix} v_p \\ i_z \\ i_{zc} \\ i_{x+} \\ i_{x-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & +g_m & 0 & 0 & 0 \\ 0 & -g_m & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_p \\ v_z \\ v_{zc} \\ v_{x+} \\ v_{x-} \end{bmatrix}$$

where $+g_m$ and and $-g_m$ correspond for the positive output current (i_{x+}) and negative output current (i_{x-}), respectively.

In general, the g_m-value is electronically controllable by external bias current/voltage.



(a)

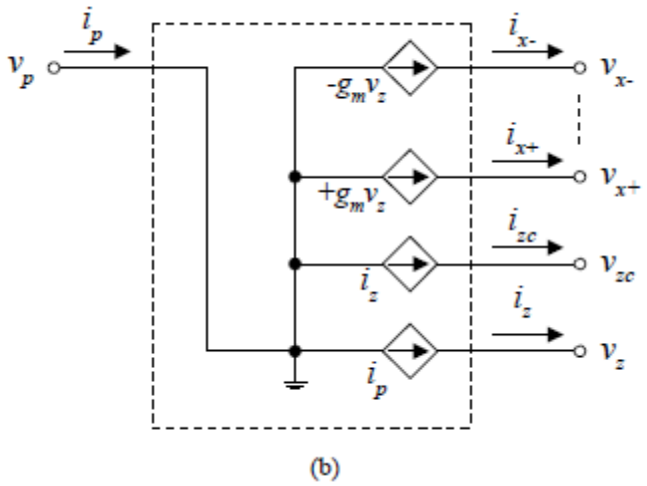


Fig . 4.27 (a) Electrical Symbol (b) Equivalent circuit of ZC-CFTA

4.16 Voltage Differencing Buffered Amplifier , VDBA

In [20], the circuit principle called VDBA (Voltage Differencing Buffered Amplifier) is proposed as an alternative to the existing CDBA (Current Differencing Buffered Amplifier) [3] the input stage of VDBA is composed of the differential-input OTA. The voltage buffer is connected to the OTA current output. This structure is semi-differential. A method of augmenting the voltage buffer by an inverting output is also mentioned in [29] with the corresponding abbreviation DOBA (Differential Output Buffered Amplifier). Replacing the voltage buffer in the VDBA by the DOBA yields a fully differential circuit element.

According to the methodology in [20] such an element should be specified as VDDOBA (Voltage Differencing Differential Output Buffered Amplifier). A specific drawback of the VDDOBA consists in the necessity to implement both the voltage buffer and the inverter. Among other shortcomings, it implies a more complicated circuit structure. Therefore, another solution was Proposed by Biolkova and Kolka and Biolek [43] which is based only on voltage buffers, concurrently providing more versatility than VDDOBA. To differentiate it from VDDOBA, it was termed FB-VDBA (Fully Balanced VDBA).

Circuit description

The proposed schematic symbol and behavioral model of the FB-VDBA are in Fig. 4.28 (a) and (b). The model can be described by the following set of circuit equations:

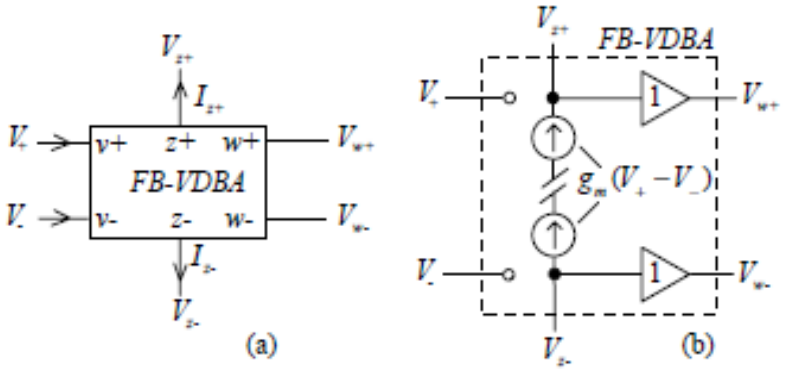


Fig. 4.28 (a) schematic symbol (b) behavioral model of VDBA

$$\begin{bmatrix} I_{z+} \\ I_{z-} \\ V_{w+} \\ V_{w-} \end{bmatrix} = \begin{bmatrix} g_m & -g_m & 0 & 0 \\ -g_m & g_m & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_+ \\ V_- \\ V_{z+} \\ V_{z-} \end{bmatrix}$$

FB-VDBA has a pair of high-impedance voltage inputs *v*+ and *v*-, a pair of high-impedance current outputs *z*+ and *z*-, and two low impedance voltage outputs *w*+ and *w*-. The input stage can be simply implemented by a differential-input differential output OTA. When connecting two identical grounded resistors to the *z*+ and *z*- terminals, the voltage drops on them will be of equal value but different directions. The output voltages of *w*+ and *w*- terminals thus will be *Vw*- = -*Vw*+. In this way, the voltage inversion is achieved without the utilization of voltage inverter.

4.17 Current Follower/Inverter Buffered Transconductance Amplifier (CFBTA, CIBTA).

In 1999 and 2003, two papers were published which introduced new circuit elements: CDBA (Current Differencing Buffered Amplifier) [1] and CDTA (Current Differencing Transconductance Amplifier) [2]. Both contain the so–called Current Differencing Unit (CDU) with two low-impedance terminals, *p* and *n*, and one high-impedance terminal, *z*. The difference of currents I_p and I_n flows out of the *z* terminal and the corresponding voltage drop on the external impedance is either copied by the voltage buffer to the *w* output of the CDBA or transformed by the Multiple- Output Operational Transconductance Amplifier (MO–OTA) to the *x*–terminal currents *Ix* of the CDTA. Many applications of CDBA and CDTA in the analog signal processing area have been described in the literature. Their survey as well as a comparison of these universal blocks was summarized in [20].

In order to simplify the internal construction of both devices, the CDU can be replaced by a simple current follower or inverter. It is shown in [20] that the universality of the resulting element is still preserved when the output stage is represented by a multiple–output OTA, providing the currents of both directions. An extension of the above Approach was proposed by Bajer, Vavra and Biolek [44] in which the conventional CDTA is modified such that the CDU is replaced by the current follower or inverter, and the *z*–terminal voltage is buffered by the voltage follower. The first modification simplifies the input stage, which improves the dynamic performance and power consumption, and the second one increases the circuit universality.

The symbols and behavioral models of proposed active elements are in Fig. 4.29 (a) and (b). The corresponding circuit equations can be arranged in the following matrix form:

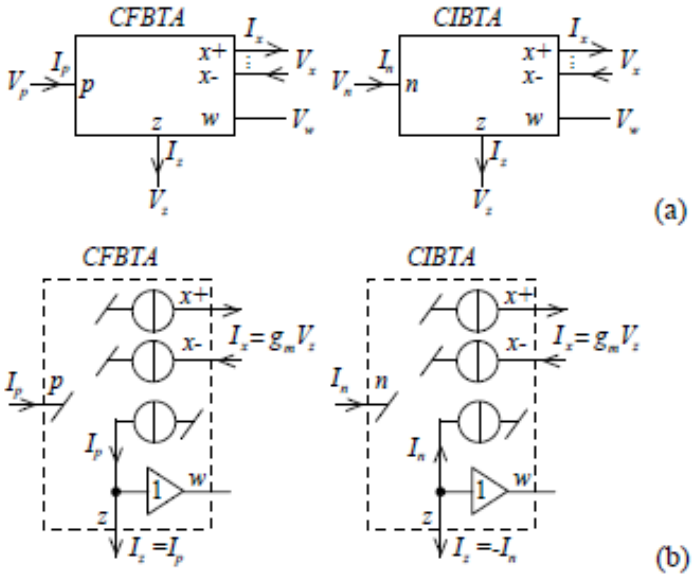


Fig. 4.29 (a) Symbol (b) Equivalent circuits of CFBTA and CIBTA

$$\begin{bmatrix} I_z \\ V_w \\ I_x \\ V_{p(n)} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & (-)1 \\ 1 & 0 & 0 & 0 \\ g_m & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_z \\ I_w \\ V_x \\ I_{p(n)} \end{bmatrix}$$

According to the above Equations and equivalent circuits, the *p* and *n* input terminals behave as grounded because their voltages are zero. The *z*-terminal current is a copy of the *p* or *n* terminal current, flowing out of the device for CFBTA and into the device for CIBTA. Moreover, the *z* terminal voltage is copied to the low–impedance *w* terminal and transferred to the *x* terminal currents via the OTA transconductance *gm*.

CFBTA and CIBTA, represent two main improvements in comparison to the well–known CDBA and CDTA: 1) simplified input stage in the form of current follower or inverter, and 2) more universal output stage, containing both the multiple–output OTA for providing current outputs and the voltage buffer for supplying subsequent blocks with voltage–type signal.

REFERENCES

3. K.C. Smith, A. Sedra, 'The current conveyor: a new circuit building block'. IEEE Proc. CAS, 1968, vol. 56, no. 3, p. 1368-1369.

4. A. sedra, K.C. Smith, 'A second generation current conveyor and its application'. IEEE Trans., 1970, CT-17, p. 132-134.

5. C. Acar, S. Özoguz, 'A new versatile building block: Current differencing buffered amplifier suitable for analog signal processing filters', Microelec J, vol.30, pp.157–160, 1999.

6. S. Özoguz, A. Toker, M. A. İbrahim, C. Acar, 'A new versatile building block: Current differencing amplifier and its applications', In Proceedings of The European Conference on Circuit Theory and Design, ECCTD'99,pp. 90-93, 1999.

7. F. Kaçar, Y. Özcelep 'CDBA Based Voltage-Mode First-Order All-pass Filter Topologies' F.Kaçar AND Y. Özçelep / IU-JEEE Vol. 11(1), (2011), 1327-1332

8. S. Ozoguz, A. Toker and C. Acar, 'Current-mode continuous-time fully-integrated universal filter using CDBAs', Electron. Lett., vol.35, no.2, pp.97-98, 1999.

9. W. Tangsrirat, W. Surakampontorn and N. Fujii, 'Realization of leapfrog filters using current differential buffered amplifiers' , IEICE Trans. Fundamental., vol. E86-A, pp.318-326, 2003.

10. H. Sedef and C. Acar, 'On the realization of voltage-mode filters using CDBA', Frequenz, vol.54, pp.198-202, 2000.

11. N. Tarim and H. Kuntman, 'A high performance current differencing buffered amplifier', Proceedings of International Conference on Microelectronics, Rabat, Morocco, pp.153-156, 2001.

12. C. Acar and H. Sedef, 'Realization of nth-order current transfer function using current differencing buffered amplifiers', Int. J. Electron., vol.90, no.4, pp.277-283, 2003.

13. W. Tangsrirat, K. Klahan, T. Dumawipata and W. Surakampontorn, 'Low-voltage NMOS-based current differencing buffered amplifier and its application to current-mode ladder filter design', Int. J. Electron., vol.93, no.11, pp.777-791, 2006.

14. S. Maheshwari and I. A. Khan, 'Current- controlled current differencing buffered amplifier: implementation and applications,' Active and Passive Electronic Components, vol. 27, pp. 219-227, 2004.

15. D. Prasertsom , W. Tangsrirat , W. Surakampontorn 'Low-Voltage Digitally Controlled Current Differencing Buffered Amplifier' 2008 IEEE.

16. A .Fabre 'Dual translinear Voltage/Current converter' Electronics letter 19 1030-1031

17. A. Fabre, O. Saaid, F. Wiest, and C. Boucheron, 'Current controllable bandpass filter based on translinear conveyors,' Electronic Letters, vol. 31, pp. 1727-1728, 1995.

18. A.A. El-Adawy, A.M. Soliman and H.O. Elwan, 'Low-voltage digitally controlled CMOS current conveyor', Int. J. Electron. Commun. (AEU), vol.56, no.3, pp.137-144, 2002.

19. D. Biolek, 'CDTA-Building block for current-mode analog signal processing', Proc. ECCTD'03, Cracow, Poland, 2003, Vol. III, pp.397-400.

20. A. Uygur , H. Kuntman , 'Low voltage current differencing transconductance amplifier in a novel allpass configuration' The 13th IEEE Mediterranean Electrotechnical Conference MELECON 2006, May 16-19, 2006 Torremolinos (Málaga), Spain.

21. D. Prasad , D.R .Bhaskar, A.K.Singh : 'Realisation of singleresistance- controlled sinusoidal oscillator: a new application of the CDTA',WSEAS Trans. Electron., 2008, 5, (6), pp. 257–259

22. D. Biolek, R. Senani, V. Biolková, Z. Kolka 'Active Elements for Analog Signal Processing: Classification, Review, and New Proposals' Radioengineering, vol. 17, no. 4, December 2008

23. Y. LI 'Current-Mode Sixth-Order Elliptic Band-Pass Filter Using MCDTAs' Radioengineering, vol. 20, no. 3, September 2011

24. M. Siripruchyanun, W.Jaikla, 'Current-controlled current differencing transconductance amplifier and applications in continuous-time signal processing circuits'. Analog Integrated Circuits and Signal Processing, 2009, vol. 61, p. 247-257.

25. W.Jaikla, P. Prommee 'Electronically Tunable Current-mode Multiphase Sinusoidal Oscillator Employing CCCDTA-based Allpass Filters with Only Grounded Passive Elements' Radioengineering, vol. 20, no. 3, September 2011

26. R. Prokop, V. Musil ‘New modern circuit block ccta and some its applications’Electronics 2005 21 – 23 September, Sozopol, Bulgaria.

27. U. Kumar,: ‘Current Conveyors: A review of the State of the Art’. IEEE Circuits and Systems Magazine, Vol. 3, No. 1, pp. 10-13.

28. M. Siripruchyanun and W. Jaikla, ‘Current controlled current conveyor transconductance amplifier (CCCCTA): a building block for analog signal processing,’ Electrical Engineering, vol. 90, no. 6, pp. 443–453, 2008

29. N. Pandey, R. Bazaz, and R.Manocha ‘MO-CCCCTA-Based Floating Positive and Negative Inductors and Their Applications’ Hindawi Publishing Corporation Journal of Electrical and Computer Engineering Volume 2011, Article ID 150354, 8 pages

30. A. Jantakun, N. Pisutthipong and M. Siripruchyanun, ‘A Synthesis of Temperature Insensitive/Electronically Controllable Floating Simulators Based on DV-CCTAs’, floating simulators based on DV-CCTAs. In The proceedings of the 2009 6th international conference on electrical engineering/ electronics, computer, telecommunications, and information technology (ECTI-CON 2009) (pp. 560–563). Pattaya, Thailand.

31. H. O. Elwan, and, A. M Soliman, ‘Novel CMOS differential voltage current conveyor and its applications’, IEE Proc.-Circuits Devices Syst., Vol. 144, No.3, pp. 195-200, 1997.

32. M. A. Ibrahima, S. Minaeib, H. Kuntman, ‘A 22.5MHz current-mode KHN-biquad using differential voltage current conveyor and grounded passive elements’, Int J Electron Commun (AEU), vol. 50, 2005, pp. 311 – 318

33. T. M..Hassan, A. M. Soliman, ‘New CMOS DVCC realization and applications to instrumentation amplifier and active-C filters’ Int J Electron Commun (AEU) Vol. 64, 2010

34. N. Pandey,and S. K. Paul, ‘Analog Filters based on 0.25 μm CMOS Differential Voltage Current Conveyor Transconductance Amplifier(DVCCTA)’ 2011 IEEE

33. W. Chiu, S. I.Liu, H. W. Tsao, J.J. Chen, ‘CMOS differential difference current conveyors and their applications’. IEE Proc. Circuits Devices Syst., 1996, vol. 143, no. 2, p. 91-96.

34. D. R.Bhaskar, A.K. Singh, R. K.Sharma, R. Senani, New OTA-C universal current-mode/trans-admittance biquads. IEICE Electronics Express, 2005, vol. 2, p. 8-13.

35. W. Tangsrirat, O. Hannumsin ‘High-Input Impedance Voltage-Mode Multifunction Filter Using a Single DDCCTA and Grounded Passive Elements’ Radioengineering, vol. 20, no. 4, December 2011.

36. A. F. Arbel, L. Goldminz, ‘Output stage for current-mode feedback amplifiers, theory and applications. Analog Integrated Circuits and Signal Procesing’, 1992, vol.2, no 3, p. 243 – 255

37. A. Yeşil, F.Kaçar, H.Kuntman ‘New Simple CMOS Realization of Voltage Differencing Transconductance Amplifier and Its RF Filter Application’ Radioengineering, vol. 20, no. 3, September 2011

38. N.Herencsar, J.Koton, K.Vrba, and I.Lattenberg, ‘Current follower transconductance amplifier (CFTA) - a useful building block for analog signal processing’, Journal of Active and Passive Electronic Devices, vol. 6, no. 3-4, pp. 217-229, 2011. ISSN: 1555-0281.

39. R. L. Geiger and E. Sánchez-Sinencio. ‘Active Filter Design Using Operational Transconductance Amplifiers: A Tutorial’, IEEE Circ. and Dev. Mag., 1, pp.20-32. 1985

40. T. Deliyannis, Y. Sun and J. K. Fidler. ‘Continuous-Time Active Filter Design’. USA, Boca Raton: CRC Press.1999

41. W. Tangsrirat and W. Surakampontorn. ‘Systematic realization of cascadable current-mode filters using current differencing transconductance amplifiers’, Frequenz,60(11-12), pp.241-245, 2006.

42. J.Satansup, W.Tangsrirat, ‘single-input five-output electronicallty tunable current-mode Biquad Consisting of Only ZC-CFTAs and Grounded Capacitors’ Radioengineering, vol. 20, no. 3, September 2011

43. V. Biolkova and Z. Kolka and D. Biolek ‘Fully Balanced Voltage Differencing Buffered Amplifier and its Applications’ 2009 IEEE

44. J. Bajer , J. Vavra and D. Biolek ‘A new building block for analog signal processing: current follower/inverter buffered transconductance amplifier’ 2009 IEEE

CHAPTER V

RESULTS & DISCUSSIONS

5.1 Introduction

Some of the active building blocks which have been described in the previous chapters have been implemented / being implemented by different research groups working in this area using either off the shelf available discrete components or they have presented Bipolar / CMOS implementations of their designs. In the present chapter we present simulation results of some of these blocks in different application using off the shelf components. The realization of various active element circuitry is done with commercially available ICs like AD844 (CFOA) and LM13600 (OTA). The circuits are simulated using Orcad-Pspice 9.1 version.

5.2 Current Conveyor Transconductance Amplifier (CCTA)

Recently there is a growing interest in synthesizing current-mode circuits because of their many potential advantages such as, larger dynamic range, higher signal bandwidth, greater linearity, simpler circuitry and lower power consumption [1], [2]. Many active elements able to function in current-mode such as OTA, current conveyor, current differencing buffered amplifier (CDBA), current feedback amplifier (CFA), and current differencing transconductance amplifier (CDTA) have been introduced in response to these demands.

The current conveyor transconductance amplifier (CCTA) [3], is a versatile component in the realization of a class of analog signal processing circuits, especially analog frequency filters. It is supposed for usage mostly in current-mode circuits, but it is also a choice in case of voltage mode and/or hybrid (voltage-current) circuits (e.g. V/I converters). In addition, it can also adjust the output current gain. The mentioned CCTA is implemented by connection of CMOS transistors is not easy to really experiment therefore the practical implementation of CCTA was proposed by Jaikla, Silapan, Chanapromma and Siripruchyanun in 2008 by using the commercially available ICs like AD844 (CCII) and LM13600N (OTA). [4].

Basic Concept of CCTA has already been discussed in 4.8

Practical Realization of CCTA

The Figure 5.2.1 below shows the implementation of CCTA using commercially available ICs

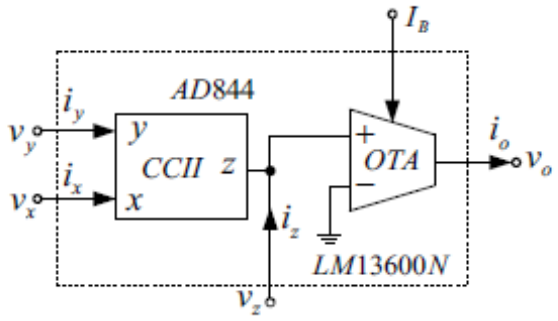


Fig 5.2.1 Implementation of CCTA using AD844

It consists of two principal blocks: a second generation current conveyor (AD844) as input stage and a transconductance amplifier (LM13600N) as output stage. The transconductance can be adjusted by input bias current of the LM13600N.

A sinusoidal oscillator was designed with the proposed CCTA as shown in figure 5.2.2

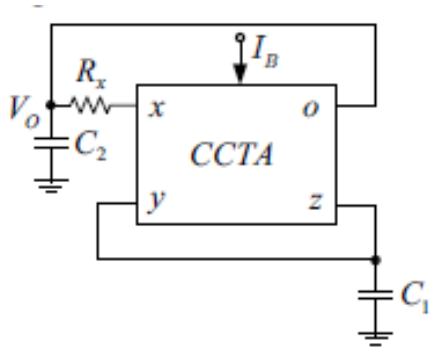


Fig 5.2.2 CCTA based sinusoidal oscillator

It consists of only single CCTA, 1 resistor and 2 grounded capacitors. Considering the circuit in Fig. 5.2.2 and using the CCTA properties, yields the characteristic equation of the circuit to be

$$s^2 C_1 C_2 R_x + s(C_1 - C_2) + g_m = 0$$

From the above equation, it is seen that the proposed circuit can be set to be an oscillator if

$$C_1 = C_2$$

And it is called the condition of oscillation ,thus the characteristic equation of the system becomes,

$$s^2 + \frac{g_m}{C_1 C_2 R_x} = 0$$

The oscillation frequency of such a system will be

$$\omega_o = \sqrt{\frac{g_m}{C_1 C_2 R_x}} = \sqrt{\frac{I_B}{2V_T C_1 C_2 R_x}}$$

It can be seen that, from the above expression that the oscillation frequency (ω_o) can be controlled by the bias current.

The circuit in figure **5.2**.2 is simulated using AD844 and LM13600 with the component value listed below

C_1 = 1nF

C_2 = 1.07nF (slightly larger than C1 for the oscillations to start)

R_x = 1 kΩ

I_B = 100µA

And the baising voltages are fixed to ±12V

The actual simulated circuit using AD844 and LM13600 using Orcad-Capture is shown in Figure 5.2.3. The confirmed performance of the oscillator can be seen in Fig. 5.2.4 showing the simulated response of the oscillator.

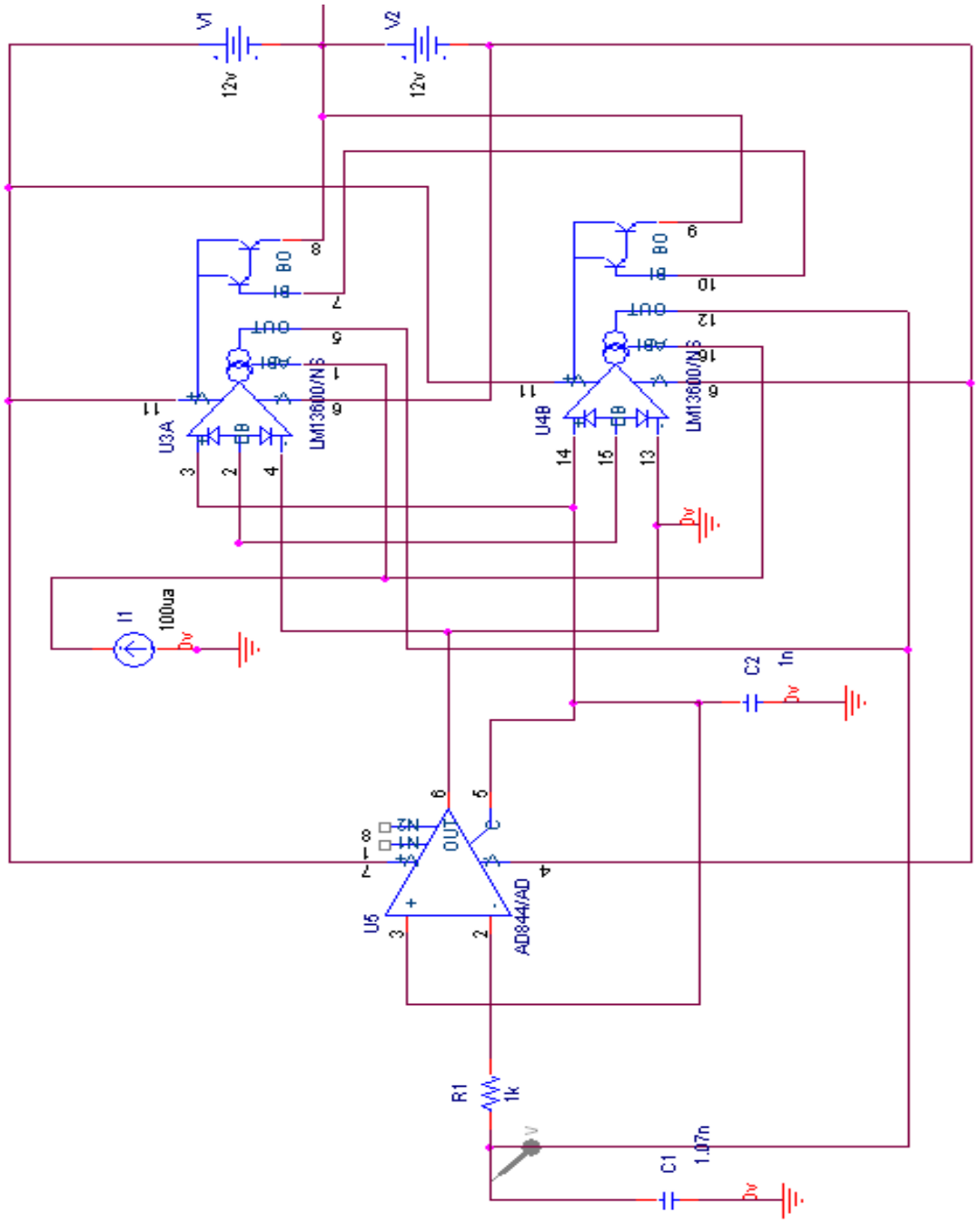


Fig **5.2**.3 CCTA based Sinusoidal oscillator simulated using AD844 and LM13600

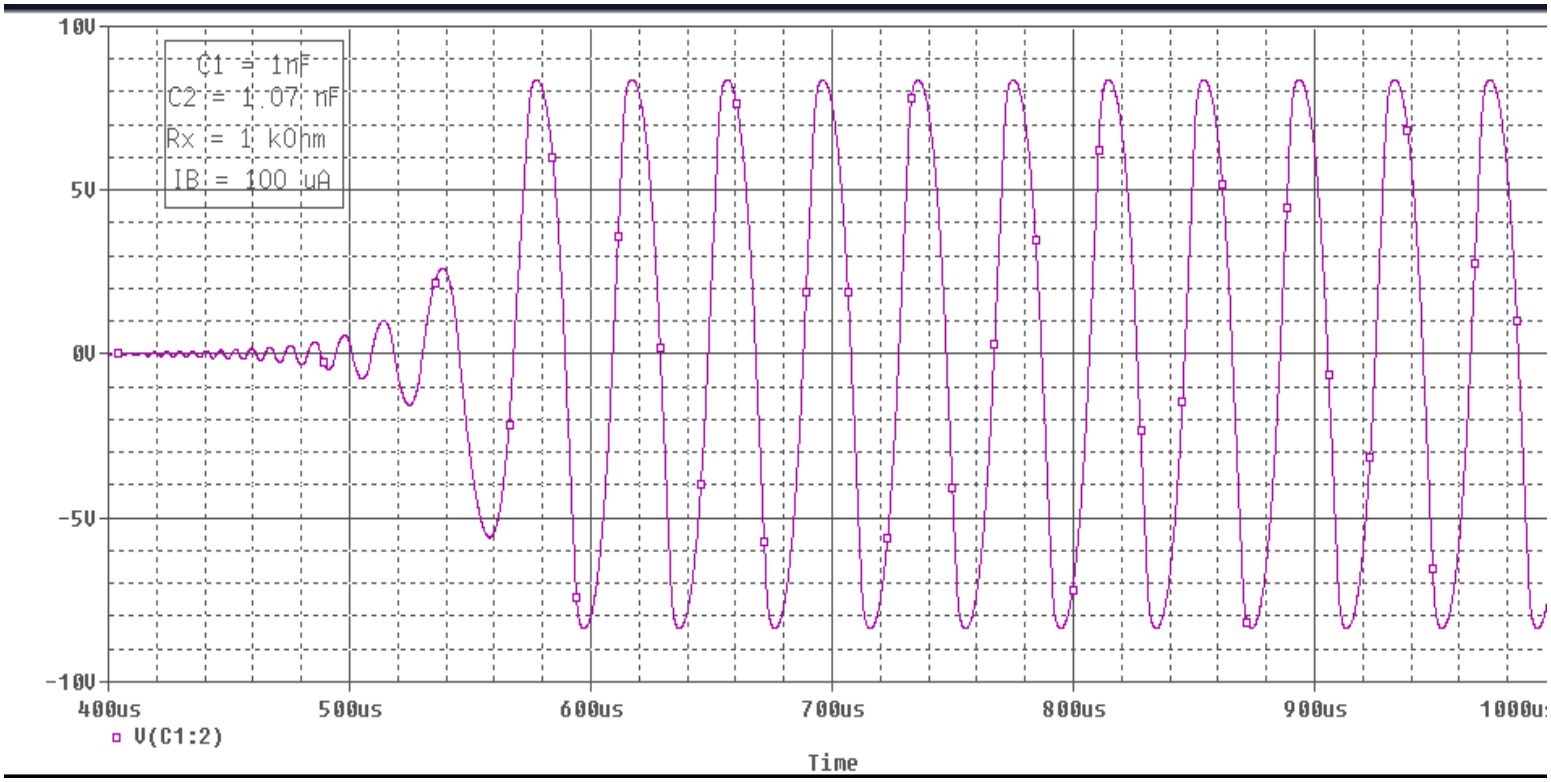


Fig 5.2.4 CCTA based sinusoidal oscillator response using Pspice

5.3 Practical implementation of Current Controlled Current Feedback Amplifier

Among the various newly introduced current mode active blocks the current feedback amplifier (CFA) or current feedback operational amplifier (CFOA) is an interesting active component, especially suitable for a class of analog signal processing applications. This device can operate in both current and voltage modes, provides flexibility and enables a variety of circuit designs. In addition, it can offer advantageous features such as high-slew rate, free from parasitic capacitances, wide bandwidth and simple implementation, Presently, the CFA can be commercially found, for example AD844 of Analog Devices Inc. [5]. It can be employed to realize filters, amplifiers, oscillators, inductance simulators, and etc. A modified-version CFA whose parasitic resistance at current input port can be controlled by an input bias current, called current controlled current feedback amplifier (CC-CFA)**,** was proposed by Siripruchyanun, Chanapromma, Silapan, and Jaikla [6] and the details of it has already been discussed in 3.4.

The implementation of CC-CFA by using the commercially available ICs, was proposed by Chanapromma, Maneetien and Siripruchyanun [7] which uses AD844 as a current conveyor and LM13600N (OTA) as an electronically tunable floating resistance simulator to perform as the parasitic resistance at current input port. The performances of proposed CC-CFA are verified by PSPICE simulation and experimental results it is found that they show good agreement as mentioned.

Implementation of CC-CFA using AD844 and LM13600

The implementation of CC-CFA is shown in Fig. 5.3.1. It consists of two principal blocks: floating resistance simulator implemented by 2 OTAs (LM13600N), modified from single dual output OTA-based floating resistance simulator, and CFA (AD844). The floating simulated resistance: R_x connected with x input terminal of the CFA can be controlled by I_B as shown in figure.5.3.1

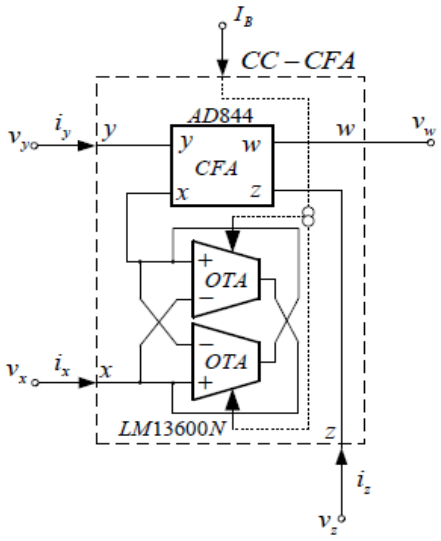


Fig 5.3.1. Implementation of CC-CFA using commercially available active blocks

Application of the above implementation can be verified by an inverting amplifier circuit. The voltage inverting amplifier based on the CC-CFA is shown in Fig**. 5.3**.2. By straightforward analysis of the circuit in Fig. 5.3.2, the output voltages of the circuit can be obtained as

$$V_o = -\frac{I_B R_L}{2V_T} V_{in} \qquad \text{.....(1)}$$

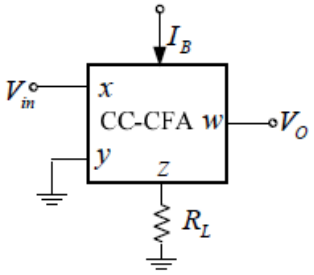


Fig 5.3.2. Non-Inverting voltage amplifier

It can be seen from Eq. (1) that the circuit in Fig. 5.3.2 can perform as voltage amplifier whose voltage gain can be electronically controlled via control current I_B.

The circuit in Fig. 5.3.2 is simulated using Orcad-Pspice version 9.1 and the actual implementation of it with AD844 and LM13600 is as shown in Fig 5.3.3.

Fig 5.3**.**4displays the output voltages as a function of the input bias current I_B whereas V_{in}=20mV_p. These figures prove that the magnitude of the output voltage can be easily/electronically controlled in accordance with the theoretical anticipations, as depicted in Eq. (1).

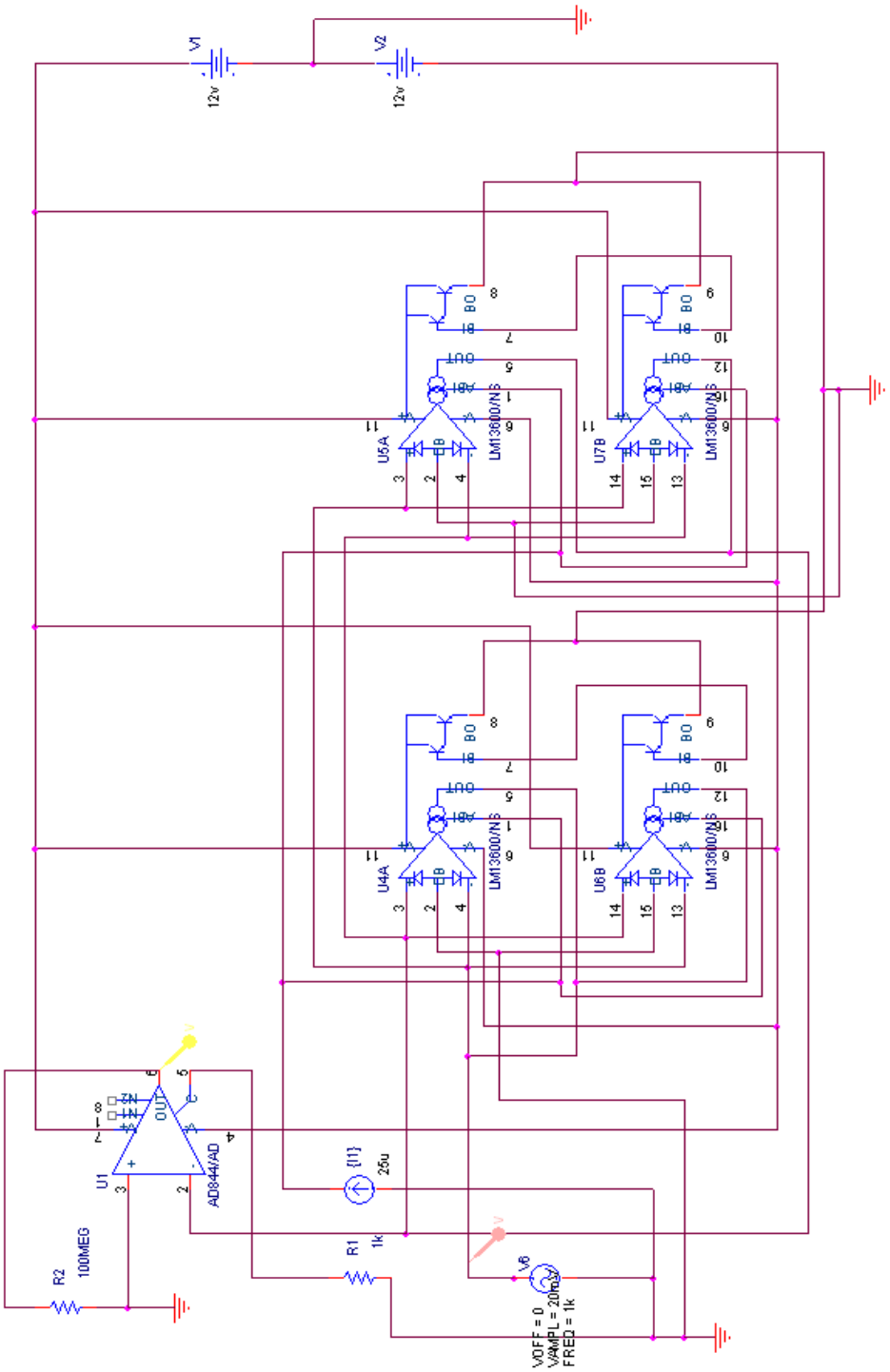


Fig **5.3**.3 CC-CFA based Non-inverting amplifier realized using AD844 and LM13600

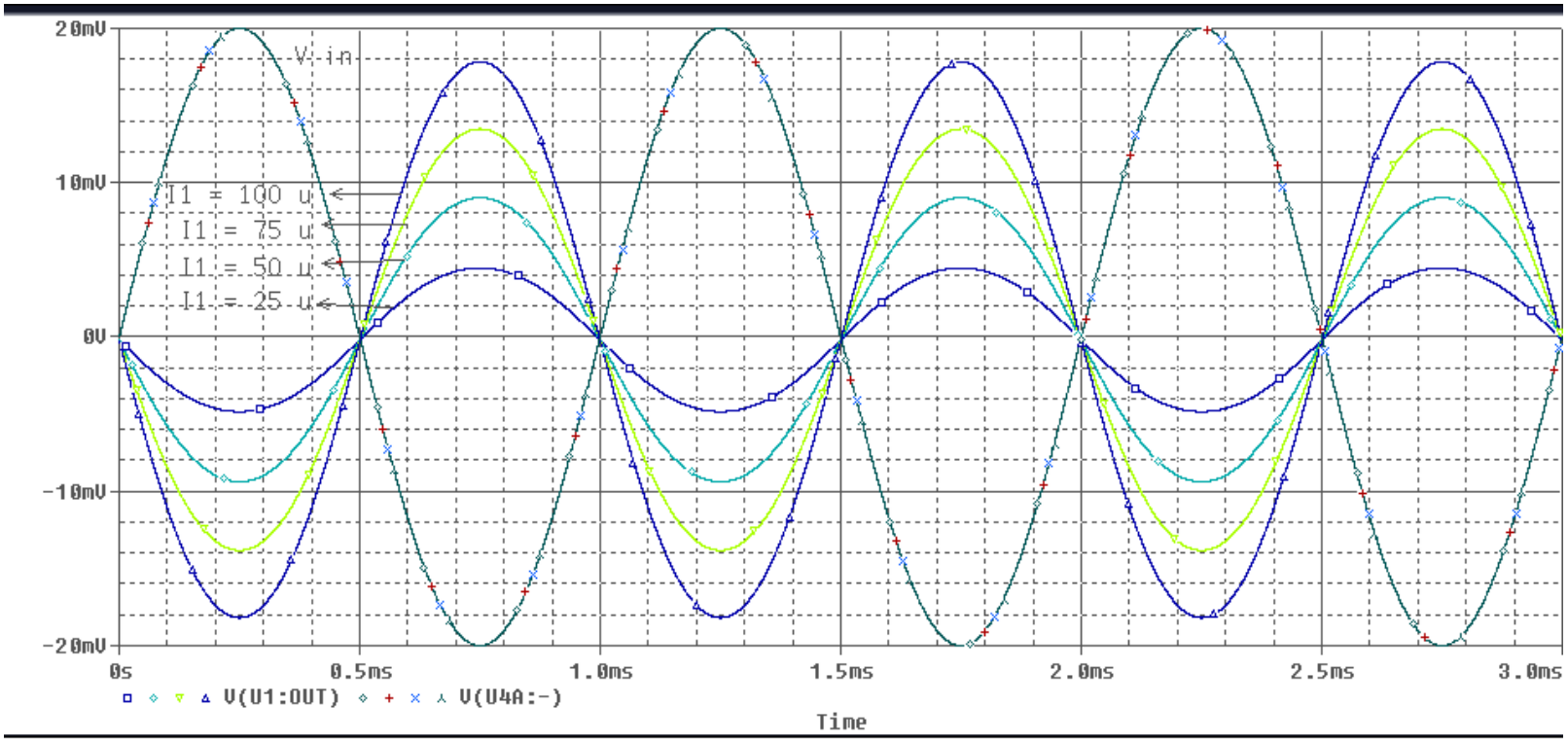


Fig 5.3.4 simulation results showing change of output voltage when I_B is set to 25µA, 50µA ,75 µA and 100µA, respectively

5.4 Practical implementation OF Current Differencing Buffered Amplifier

Current differencing buffered amplifier (CDBA) is one of the current-mode components introduced [87] at the beginning of last decade. It offers wide range of features such as high slew rate, freedom from parasitic capacitance, wide bandwidth, and simple implementation [8]. Since the CDBA consists of a unity-gain current differential amplifier and a unity-gain voltage amplifier, this element would be suitable for the implementation of voltage and current-mode signal processing applications. As far as the applications of the CDBA are concerned, various voltage-mode filters and oscillators have been reported in literature. Only few can perform both biquadratic filter and oscillator in the same circuit configuration [9]. The configuration presented in [9], it is restricted to only bandpass filter function design and cannot another type of the standard biquadratic function characteristics. Moreover, it generates a single-phase output voltage when it performs as a sinusoidal oscillator. There was no CDBA-based circuit configuration, which could realize the universal biquad filter and quadrature oscillator both in the same circuit configuration till in 2007 Tangsrirat, Pukkalanun, and Surakampontorn proposed CDBA-Based Universal Biquad Filter and Quadrature Oscillator in the same circuit[10]. Where, a the voltage-mode universal biquadratic filter and sinusoidal quadrature oscillator using two CDBAs, four virtually grounded resistors, and two capacitors were proposed. The first proposed CDBA-based biquad filter can realize lowpass (LP), bandpass (BP), highpass (HP), bandstop (BS), and allpass (AP) biquadratic functions without changing the circuit topology. The filter also provides an orthogonal control of the natural angular frequency (ωo) and the bandwidth (BW). Moreover, a CDBA-based sinusoidal quadrature oscillator circuit can be realized by slightly modifying the first proposed CDBAs-based circuit configuration.

All passive components used in the circuit realization are grounded / virtually grounded, which is insensitive to the effects of the stray capacitance. The oscillation condition and the frequency of oscillation can be controlled independently through different virtually grounded resistors. The circuit proposed was realized with commercially available IC AD844.

Detail description of CDBA is given in 4.1

Although the CDBA can be realized by using several well-known circuit techniques, one possible practical implementation is given in Figure 5.4.1

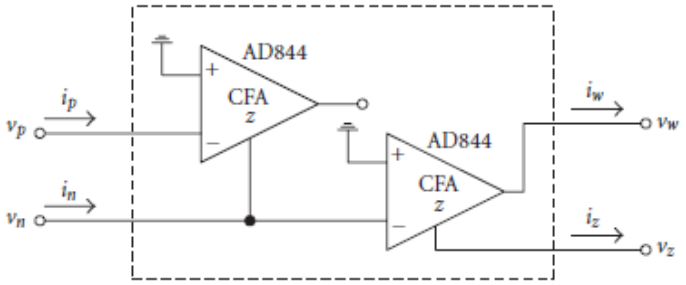


Fig 5.4. 1 .Implementation of CDBA using two CFAs (AD844)

CDBA-Based Universal Biquad Filter

Figure 5.4.2shows the proposed voltage-mode universal biquadratic filter, which consists of only two CDBAs, four virtual-grounded resistors, and two capacitors.

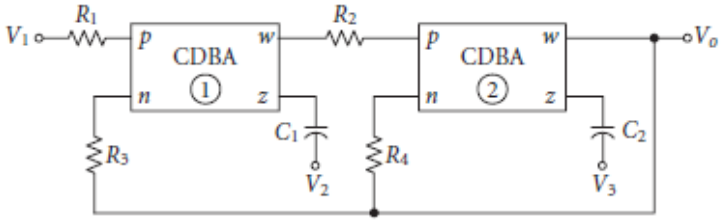


Fig 5.4.2.CDBA based Universal biquad filter

By straight- forward analysis, the single output voltage function realized by this configuration is found to be

$$V_o = \frac{s^2V_3 + (s/R_2C_2)V_2 + (1/R_1R_2C_1C_2)V_1}{s^2 + (s/R_4C_2) + (1/R_3R_2C_1C_2)} \qquad \text{……..(1)}$$

From (1), by choosing the component values of $R1 = R3$ and $R2 = R4$, we can see that

(1) if $V_1 = V_{in}$ (an input voltage signal), and $V_2 = V_3 = 0$ (grounded), the LP response can be realized with the passband gain HLP = 1;

(2) if $V_2 = V_{in}$ and $V_1 = V_3 = 0$, the BP response can be realized with the passband gain HBP = 1;

(3) if $V_3 = V_{in}$ and $V_1 = V_2 = 0$, the HP response can be realized with the passband gain HHP = 1;

(4) if $V_1 = V_3 = V_{in}$ and $V_2 = 0$, the BS response can be realized with the passband gain HBS = 1;

Clearly, the filter can be used as a voltage-mode three-input single-input universal filter that can realize all the standard types of the biquad filter functions.

Also the natural angular frequency (ω_o), the bandwidth (BW), and the quality factor (Q) in all cases are given by

$$\omega_o = \frac{1}{\sqrt{R_A R_B C_1 C_2}}$$

$$\text{BW} = \frac{1}{R_B C_2}$$

$$Q = \sqrt{\frac{R_B C_2}{R_A C_1}}$$

where $R_A = R_1 = R_3$ and $R_B = R_2 = R_4$

Simulation settings

The supply voltages were taken as ±12 V. The passive component values were chosen as $R_1 = R_2 = R_3 = R_4 = 10$ kΩ and $C_1 = C_2 = 1$nF, which is designed to obtain a universal filter with a natural angular frequency of $fo = \omega o/2\pi \approx 15.91$ kHz and the quality factor of $Q = 1$.

The Pspice simulation of the above filter circuit is shown in figures 5.4.3 and 5.4.4

Simulation results shows the frequency of oscillation as 15.85 kHz

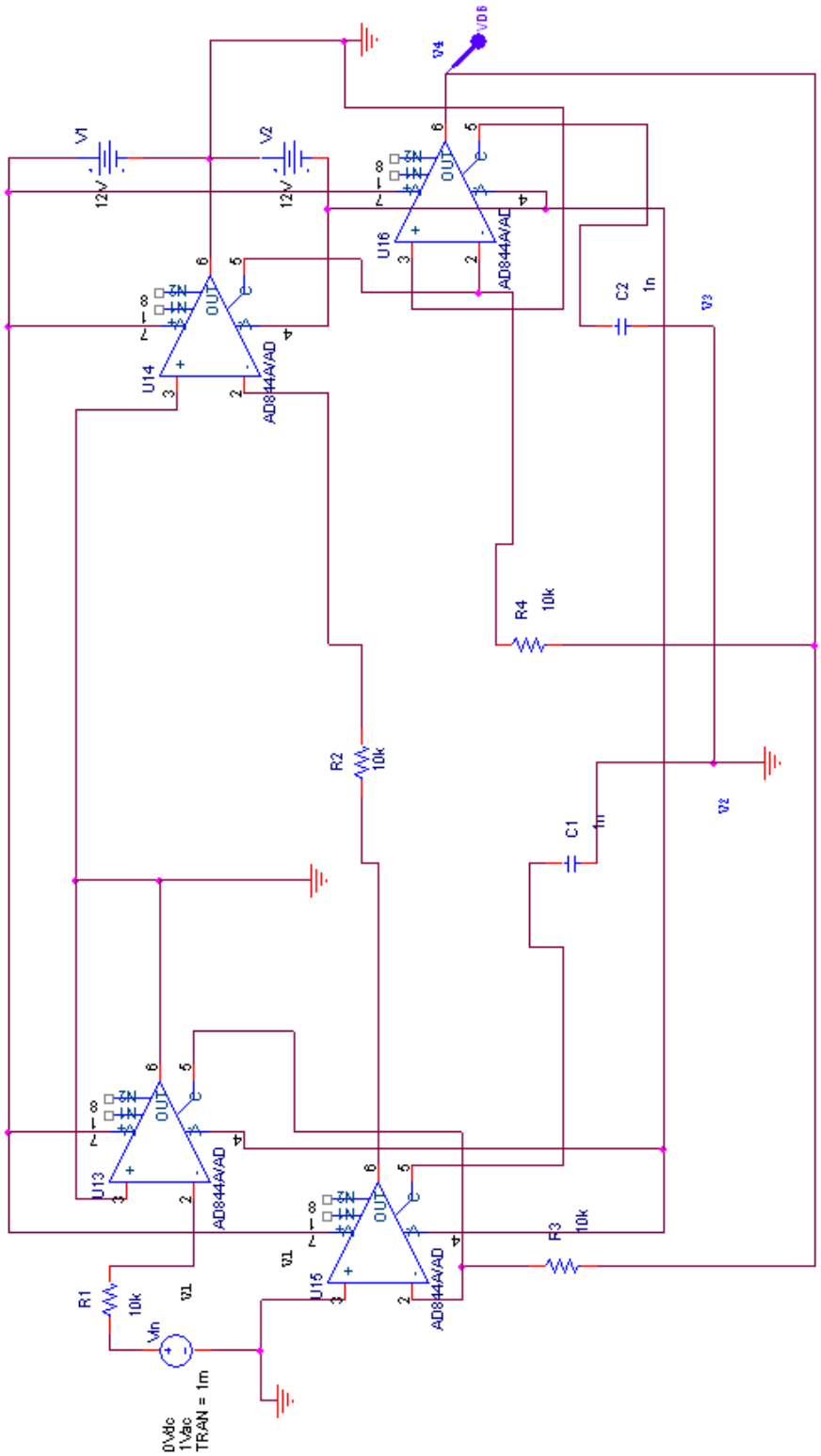


Fig 5.4.3 .CDBA Biquad Universal Filter (Low – pass mode)

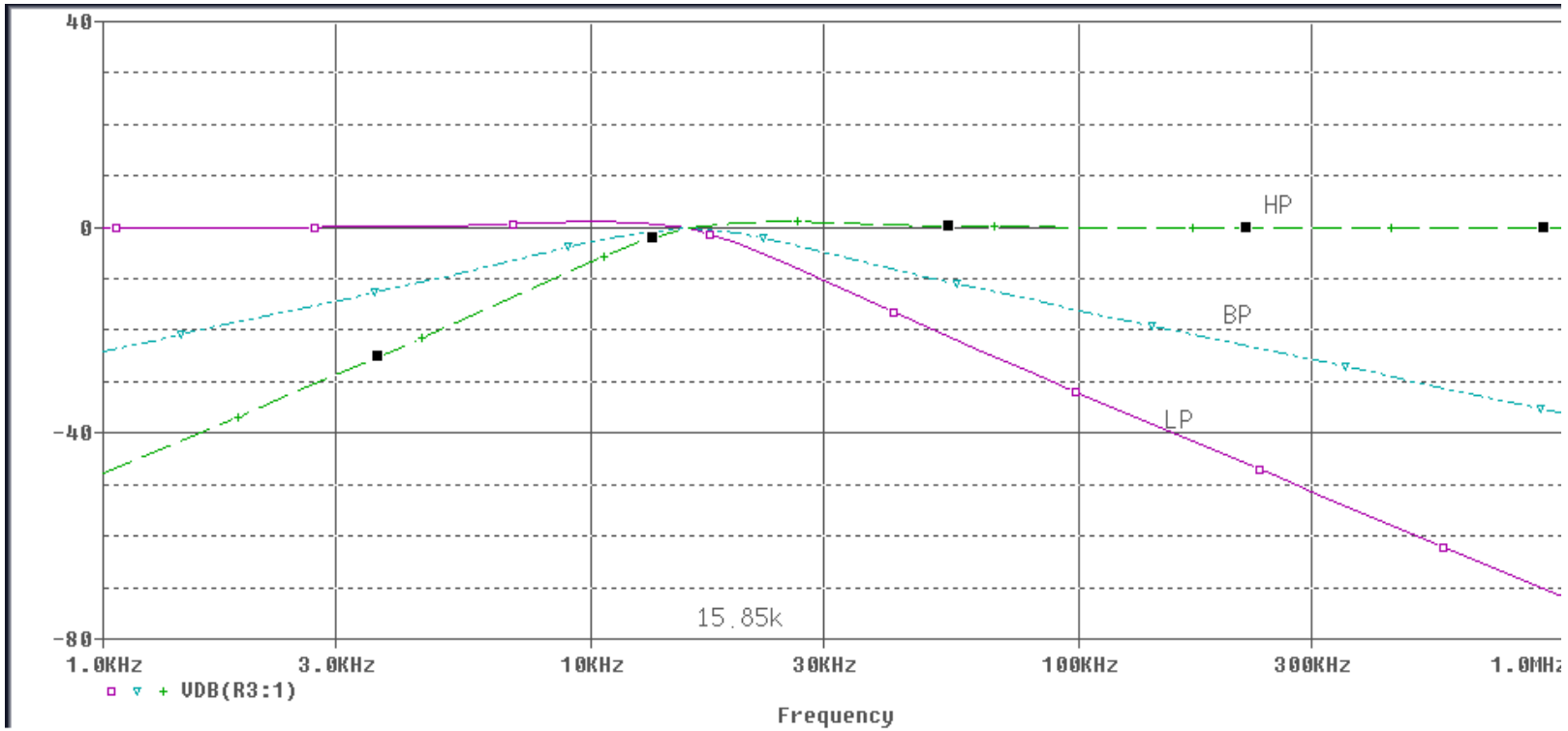


Fig 5.4.4. simulated frequency characteristics for the LP, BP, and HP filter functions of the proposed CDBA based multifunction biquad filter

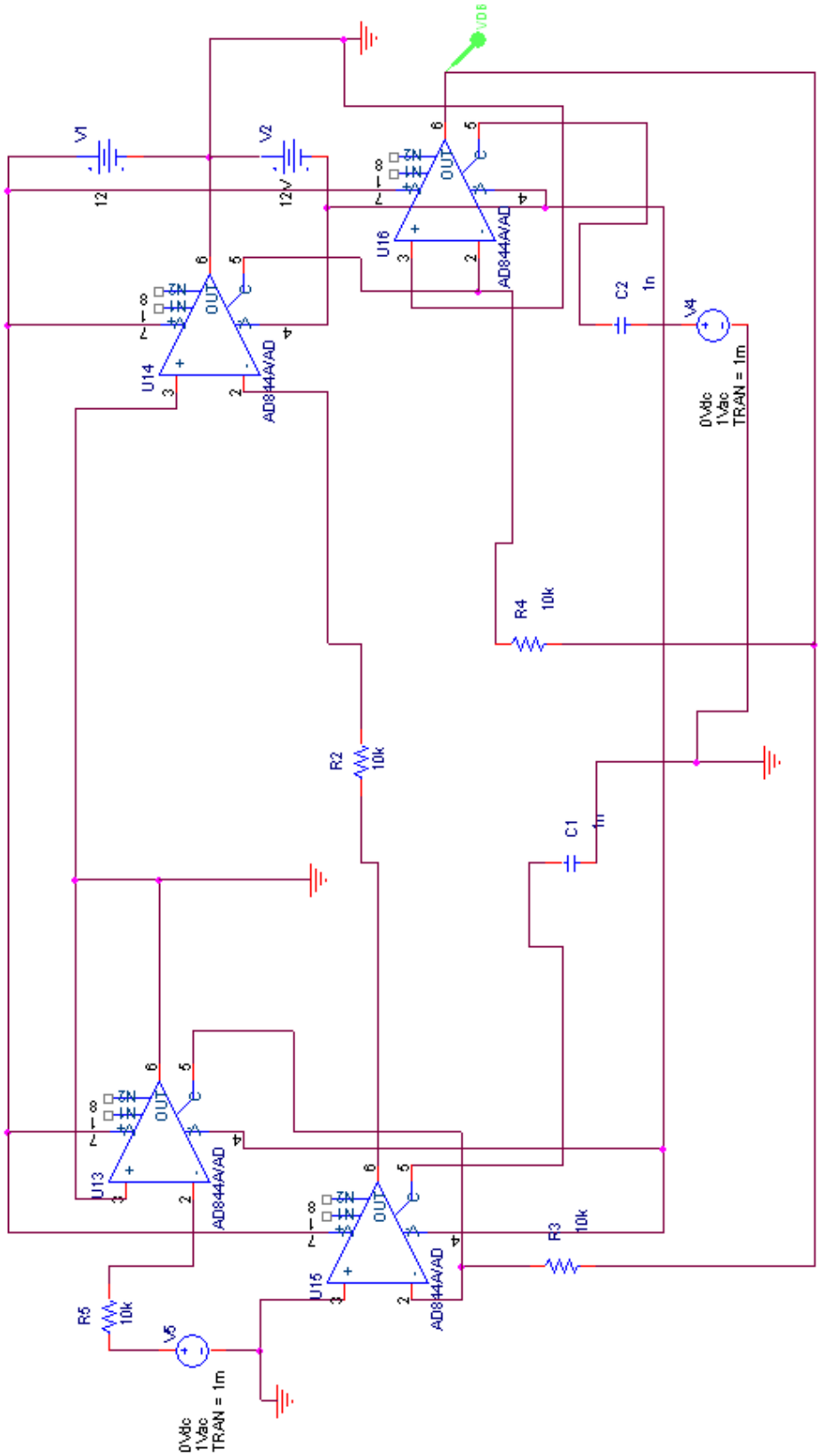


Fig 5.4.5 .CDBA Biquad Universal Filter (Band -stop mode)

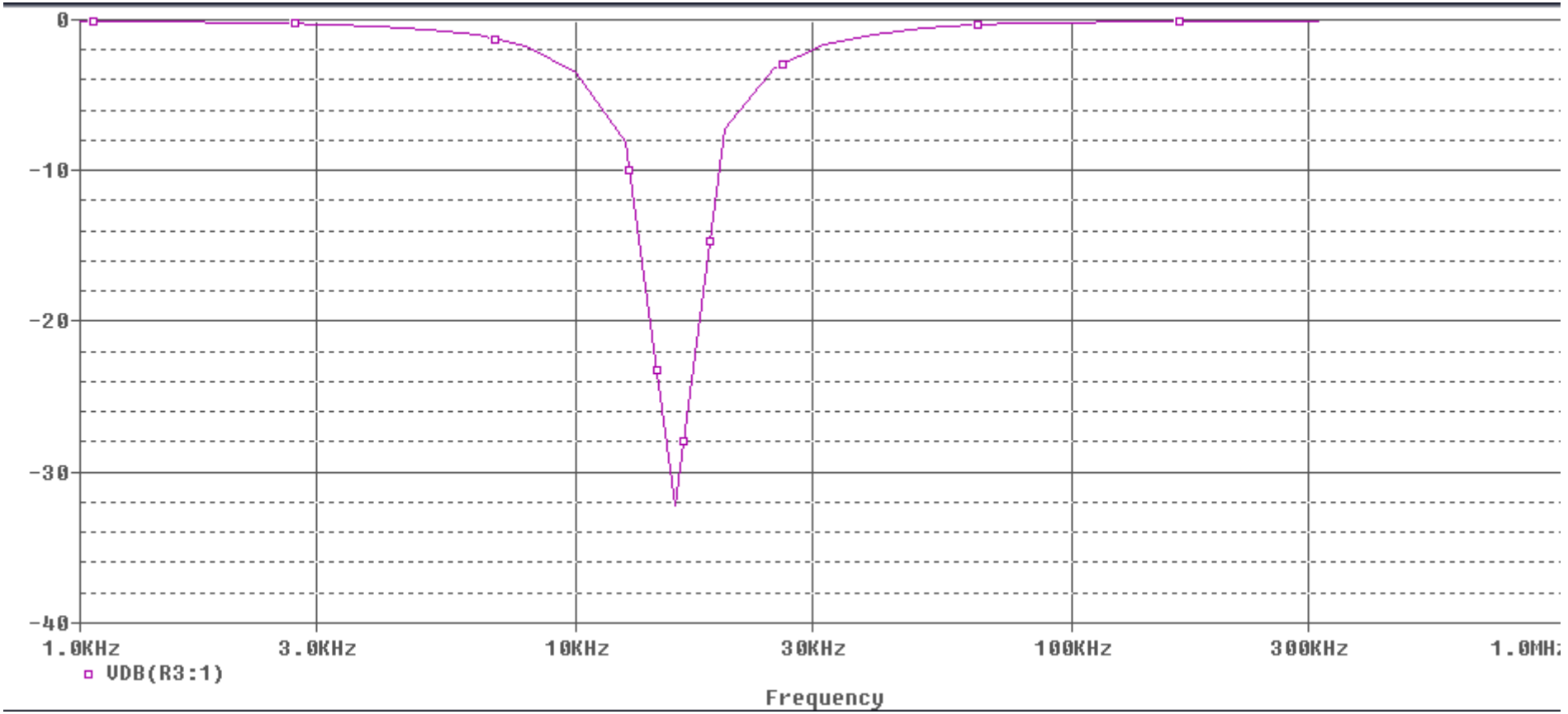


Fig 5.4.6. Simulated frequency characteristics of Band-stop filter

5.4.1 CDBA-based Quadrature Oscillator

From the first configuration of Figure 5.4.2 setting $V_1 = V_2 = V_3 = 0$ V (grounded) and connecting the resistor R_1 between the terminals p and w of the CDBA2, the CDBA-based sinusoidal quadrature oscillator can be obtained as shown in Figure 5.4.7

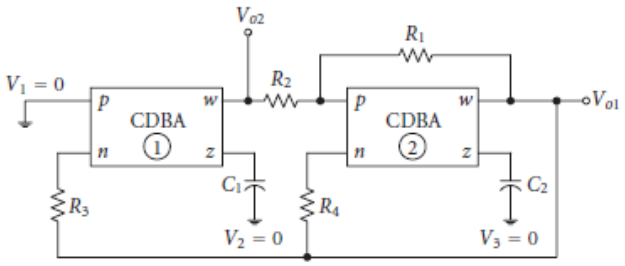


Fig 5.4.7 CDBA-based sinusoidal quadrature oscillator

In this case, the characteristic equation of the second proposed configuration can be given by

$$s^2C_1C_2 + sC_1\left(\frac{1}{R_4} - \frac{1}{R_1}\right) + \left(\frac{1}{R_2R_3}\right) = 0$$

The oscillation condition and the oscillation frequency (ω_o) of this configuration can be obtained, respectively, as

$$R_1 = R_4$$

$$\omega_o = \frac{1}{\sqrt{R_2R_3C_1C_2}}$$

From the configuration of Figure 5.4.7the relationship between two quadrature output voltages V_{o1} and V_{o2} can be expressed as

$$\frac{V_{o2}}{V_{o1}} = -\frac{1}{sR_3C_1}$$

where the phase shift is $\varphi = 90^\circ$. This guarantees that the proposed oscillator circuit provides the quadrature outputs V_{o1} and V_{o2}.

The above described circuit is simulated using the following passive component values

$R_1 = R_2 = R_3 = 10$ kΩ and $C_1 = C_2 = 1$nF. The simulated quadrature output waveforms V_{o1} and V_{o2} of the oscillator are illustrated in Figure5.4.9 here the value of $R_4 = 10.5$ kΩ was chosen to be slightly larger than R_1 to ensure that the oscillations will start. The simulated frequency was measured as 15.37 kHz, which is lower than the theoretical value of 15.91 kHz, owing to the parasitic elements R_x, z, and C_z of the AD844.Figure 5.4.8 shows the actual layout of the circuit shown in Fig 5.4.7

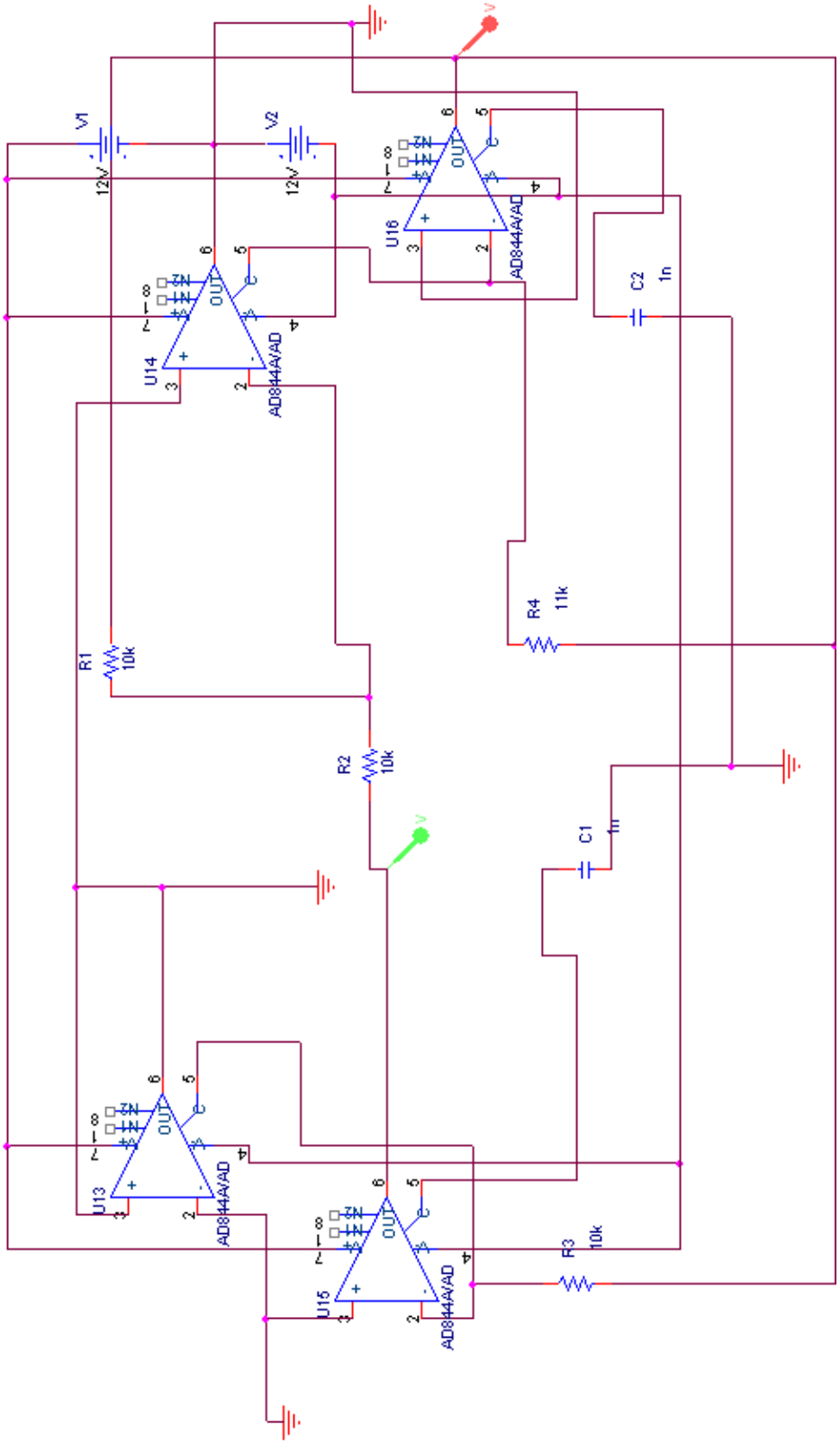


Fig 5.4.8 Practical realization of CDBA –based quadrature oscillator using AD844

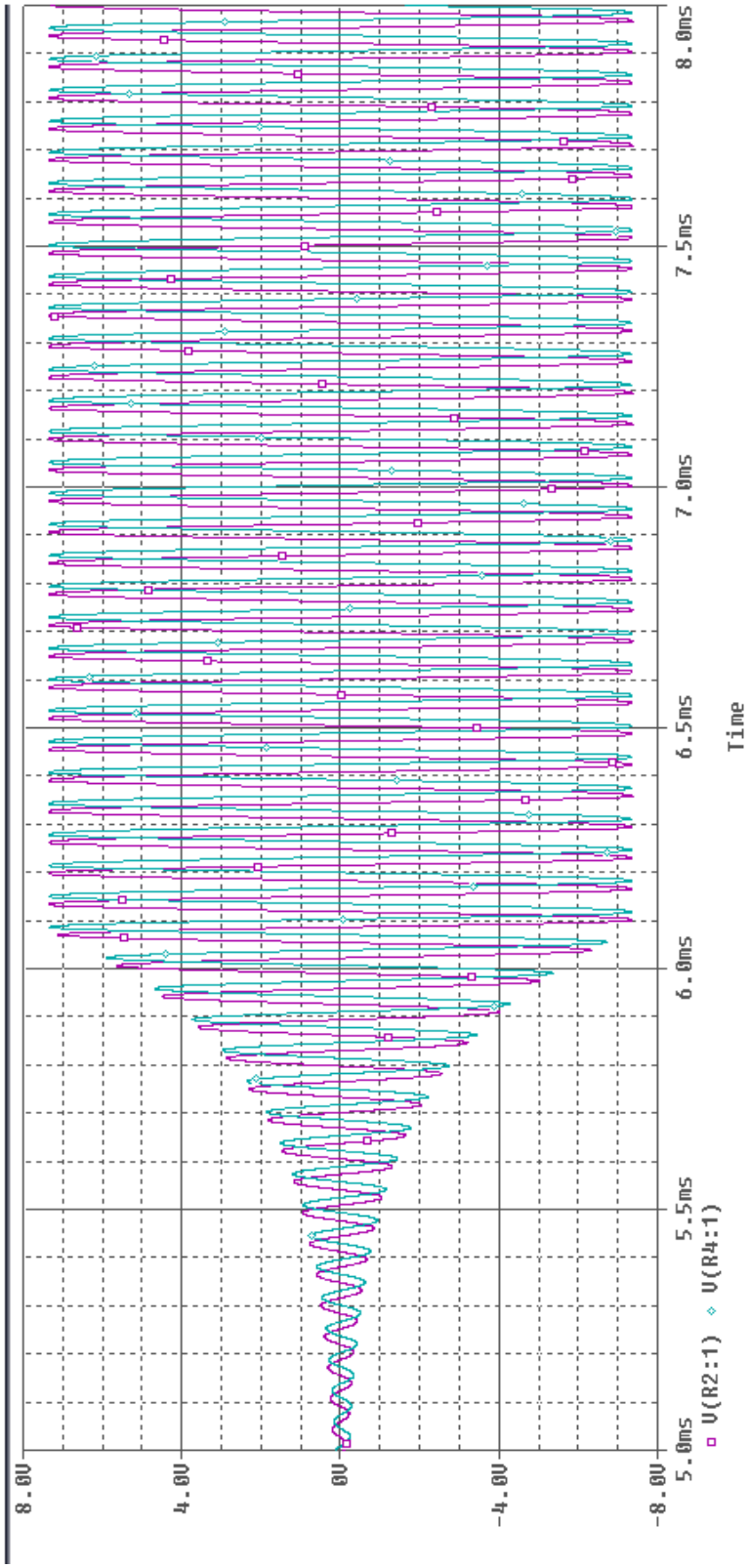


Fig 5.4.9 Simulation result of CDBA based quadrature Oscillator

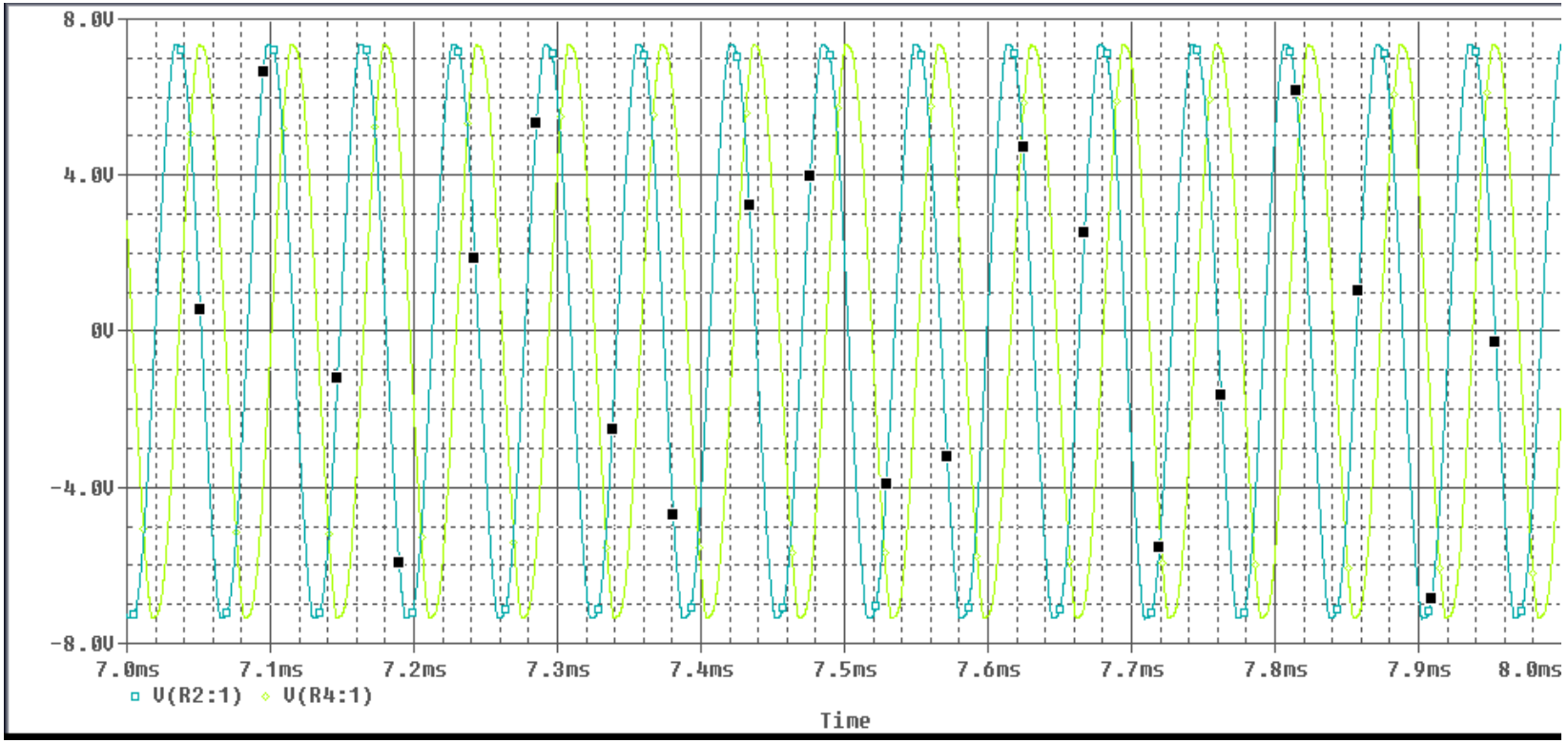


Fig 5.4.10 waveforms of V_{01} and V_{02} showing the phase-shift of 90^{o}

5.5 SUMMARY AND SCOPE FOR FUTURE WORK

In the present work a survey of the active building blocks introduced in the domain of analog signal processing after the introduction of Current Conveyor has been presented. Particular emphasis has been put on those works which have been presented during the last one decade.

Scope for future work : The work presented in this thesis has concentrated mainly on the active building blocks introduced in the domain of analog signal processing after the introduction of current conveyors. This work may be extended to classification of these works from the point of view of specific applications (filters/oscillators/non-linear applications etc.). Another useful classification could be in terms of implementation technologies employed and power consumption etc. Thus there is ample scope for extending this work in future.

A chapter wise summary of the project is as follows:

Chapter I of the thesis gives an overview of signal processing, it identifies, compares both the types namely Analog and Digital types of signal processing. This chapter gives a brief introduction followed by comparison of current mode and voltage mode of signal processing. It also includes the general outline of the thesis.

Chapter II of the thesis briefly describes about the significance of current mode circuits and the various active blocks that is introduced of current mode type after Current Conveyors generally called the derivatives of Current Conveyors. At the start of the chapter the characteristics of first and second generation current conveyors are described before describing their latest derivatives. General application of each of them is added to their description.

Chapter III of the thesis gives a description about the FTFNs ,Opamps and the various hybrid varieties of Opamp and Current conveyors ,the developments in each of the classes is discussed.

Chapter IV of the thesis gives the details of evolution of some of very versatile active blocks like CDBAs , CDTAs and their various derivatives with added potentials.

Chapter V of the thesis presents the simulation results for some of the applications of those active building blocks which can be constructed using off-the shelf available components. Finally Summary of the thesis and scope for future work in this area are outlined.

References

1. B. Gilbert, 'Current-mode circuits from a translinear viewpoint : A tutorial', in Analog IC Design : The Current-Mode Approach, TOUMAZOU, C., LIDGEY, F.J., and HAIGH, D.G., Eds. London,U.K. : Peter Peregrinus, 1990, p.11-91.

2. D.R. Bhaskar, V.K. Sharma, M. Monis and S. M. I. Rizvi, 'New current-mode universal biquad filter,' Microelectronics Journal, vol.30, pp. 837-839, 1999

3. R. Prokop, V. Musil 'New modern circuit block CCTA and some its applications" Electronics' 2005 21 – 23 September, Sozopol, BULGARIA

4. W. Jaikla, P. Silapan, C. Chanapromma and M. Siripruchyanun 'Practical Implementation of CCTA Based on Commercial CCII and OTA' 2008 International Symposium on Intelligent Signal Processing and Communication Systems (ISPACS2008)Thailand.

5. Analog Devices: "Linear products data book." Norwood MA, 1990

6. M. Siripruchyanun, C. Chanapromma, P Silapan, W. Jaikl 'BiCMOS Current-Controlled Current Feedback Amplifier (CC-CFA) and Its Applications'. WSEAS TRANSACTIONS on ELECTRONICS, Issue 6, Volume 5, June 2008

7. C. Chanapromma, N. Maneetien and M. Siripruchyanun 'A Practical Implementation of CC-CFA Based on Commercially Available ICs and Its Applications' 2009 IEEE

8. S. Ozoguz, A. Toker and C. Acar, 'Current-mode continuous-time fully-integrated universal filter using CDBAs', Electron. Lett., vol.35, no.2, pp.97-98, 1999.

9. U. Keskin, 'Voltage-mode high-Q band-pass filters and oscillators employing single CDBA and minimum number of components,' International Journal of Electronics, vol. 92, no. 8, pp. 479–487, 2005.

10. W. Tangsrirat, T. Pukkalanun, and W. Surakampontorn 'CDBA-Based Universal Biquad Filter and Quadrature Oscillator' , Hindawi Publishing Corporation Active and Passive Electronic Components Volume 2008, Article ID 247171